Design of Active Power-Factor-Correction Converters for Environmentally Green Energy Management Systems

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CERTIFICATE OF ORIGINALITY

I hereby declare that this thesis is my own work and that, to the best of my knowledge and belief, it reproduces no material previously published or written nor material which has been accepted for the award of any other degree or diploma, except where due acknowledgement has been made in the text.

(Signed)

Wen Wei (Name)

ABSTRACT

The input stage of a conventional AC – DC converter is often a rectifier bridge followed by a large bulk capacitor. As a result, the circuit draws pulsed current from the mains, which will lead to poor utilization of the capacity of the AC power source and produce harmonic pollution. In order to reduce the harmonic currents and meet the regulatory requirements such as EN 61000-3-2, both passive and active power-factor-correction (PFC) circuits have been widely used. Compared with passive circuits, active circuits can operate over a wider line voltage range and have smaller size. Therefore, for most applications, active circuits are used.

In low power applications, single-stage active PFC converters are attractive for their low cost and simplicity. A typical single-stage PFC converter includes two parts: an input-current waveform shaper and an isolated DC – DC converter. These two parts are integrated with a shared switch and controller. However, the active switch in a single-stage PFC circuit often suffers large voltage spike during switching because of the unavoidable leakage inductance of the transformer. Such voltage spike can increase the switching loss and lower the conversion efficiency. It can even damage the switch if the voltage rating of the switch is not high enough. When the switching frequency is pushed higher, the problem will become even worse.

In order to solve the voltage spike problem, a novel single-switch high-power-factor regulator with low output current ripple is proposed in this thesis. The proposed regulator employs a modified-boost converter cell as

the input stage and a double-ended forward converter cell as the output stage. In the modified-boost cell, only one clamping capacitor is necessary to suppress the voltage spike and to recycle the energy trapped in the transformer leakage inductance. The modified-boost cell operates in discontinuous conduction mode (DCM) and a high power factor is attained. In the double-ended forward cell, near-zero output current ripple is achieved and an integrated transformer is used to reduce the number and size of the magnetic components. The basic circuit topology and the operation principle of the proposed regulator are explained. Design considerations are given. Simulation and experimental results are reported to verify the operation and performance of the proposed regulator.

For high power applications, single-ended boost converters operating in continuous conduction mode (CCM) have been widely adopted as the front-end of PFC regulators. Compared with DCM operation, CCM operation has better utilization of power devices, lower conduction loss, and lower input current ripple. However, the large reverse-recovery current of the output rectifier in a CCM boost converter will cause not only extra switching loss, but also severe electromagnetic interference (EMI) noise. Two-channel interleaved boost converters have been proposed by many articles to eliminate the reverse-recovery problem while keeping the input current smooth. In such a two-channel boost converter, each individual channel can operate in DCM or critical conduction mode (CRM). The combined input current is continuous and smooth because of the interleaving arrangement. The two inductors in a two-channel boost converter can be directly coupled to reduce the number of the magnetic

components and to attain good current sharing characteristics between the two channels. However, since both the inductors have considerable number of turns, the large inductor current ripple in each channel will cause a high copper loss.

In order to improve the efficiency, a two-channel interleaved boost converter using an integrated magnetic component to reduce the core and copper losses is proposed. The integrated magnetic component functions as three inductors. All inductor windings are wound on a single EI or EE core. In the proposed winding arrangement, inductors can be designed to have smaller inductances and lower copper losses. The windings on the two outer legs of the integrated magnetic component are inversely coupled, which helps to reduce the ripple of the magnetic flux. The design of the proposed integrated magnetic component and its electrical circuit model are discussed. Experimental results show that the proposed approach can offer significant improvement in efficiency.

In order to further increase the power level, a highly efficient three-channel interleaved CCM boost converter is also proposed for high power applications. This converter consists of effectively three channels and the current in each channel is discontinuous. However, the overall input inductor current is continuous and smooth. In the converter, three inversely-coupled integrated inductors are employed to control the sharing of the three output rectifier currents. As a result, the current in each output rectifier is decreased in steps and finally reduced to zero before the associated active switch is turned on to start the next cycle of operation. All the output rectifiers are softly turned off. A very high efficiency is attained because the

reverse-recovery loss is eliminated. The winding arrangement of the inversely-coupled integrated inductors (three inductors with inverse coupling between any two) is discussed and the equivalent-circuit model is derived. The principle of operation of the converter and the design issues are explained. The converter is verified by simulation and experimental setup and the results show good agreement with the theoretical predictions.

PUBLICATIONS

Journal Papers

[1] Wei Wen, Kam-Wah Siu, and Yim-Shu Lee, "A novel single-switch, near-zero-output-current-ripple AC/DC converter with high power factor," *Journal of Power Supply*, Vol. 1, no. 3, pp. 173-178, Dec. 2002. (In Chinese.)

[2] Wei Wen, Kam-Wah Siu, and Yim-Shu Lee, "Design of a single-switch high-power-factor regulator with near-zero output current ripple," *IEEE Transactions on Industrial Electronics* (accepted).

[3] Wei Wen, Yim-Shu Lee, Martin Hoi-Lam Chow and David Ki-Wai Cheng, "A three-phase interleaved continuous-inductor-current-mode boost converter with zero diode reverse-recovery loss," submitted to *IEEE Transactions on Aerospace and Electronic Systems*.

Conference Paper

[1] Wei Wen and Yim-Shu Lee, "A two-channel interleaved boost converter with reduced core loss and copper loss, " submitted to *35th IEEE Power Electronics Specialists Conference*, June 2004, Aachen (accepted).

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CHAPTER 1

INTRODUCTION

1.1 Environmentally Green Energy Management System

Conventionally, the electricity supplied by power utilities to a consumer is in AC form. In future, the demand of DC power will become increasingly large [1,2]. Computer systems and communication equipment will increase the need for rectified AC mains supply. Electric vehicles, which are powered by electricity, have reappeared because of the growing concerns on environmental protection issues [3]-[7]. Electric vehicles will represent a new load category in future. One of the key issues associated with electric vehicles is the battery charging requirement [8]-[10]. Recharging electric vehicle batteries using high power battery charger will become essential in future homes.

On the other hand, the growing number of loads that are sensitive to power system disturbances makes power quality more critical. Power disturbances can cause incorrect operation of protective devices and abnormal operation of consumer equipment. Some kinds of loads, like audio visual systems and fire alarm systems, not only are very sensitive to power disturbances, but also can proliferate power disturbances because of their nonlinear nature. In addition, home automation systems [11]-[14], which can increase comfort and security around the house, also require a reliable and "neat" source of energy.

In order to tackle the problems of increasing demand in DC power and growing concerns on power quality, a DC power distribution system was proposed by P. W. Lee and Y. S. Lee in 1999 for adoption in the future [1]. Fig.1.1 shows the overall design of the proposed DC power system.

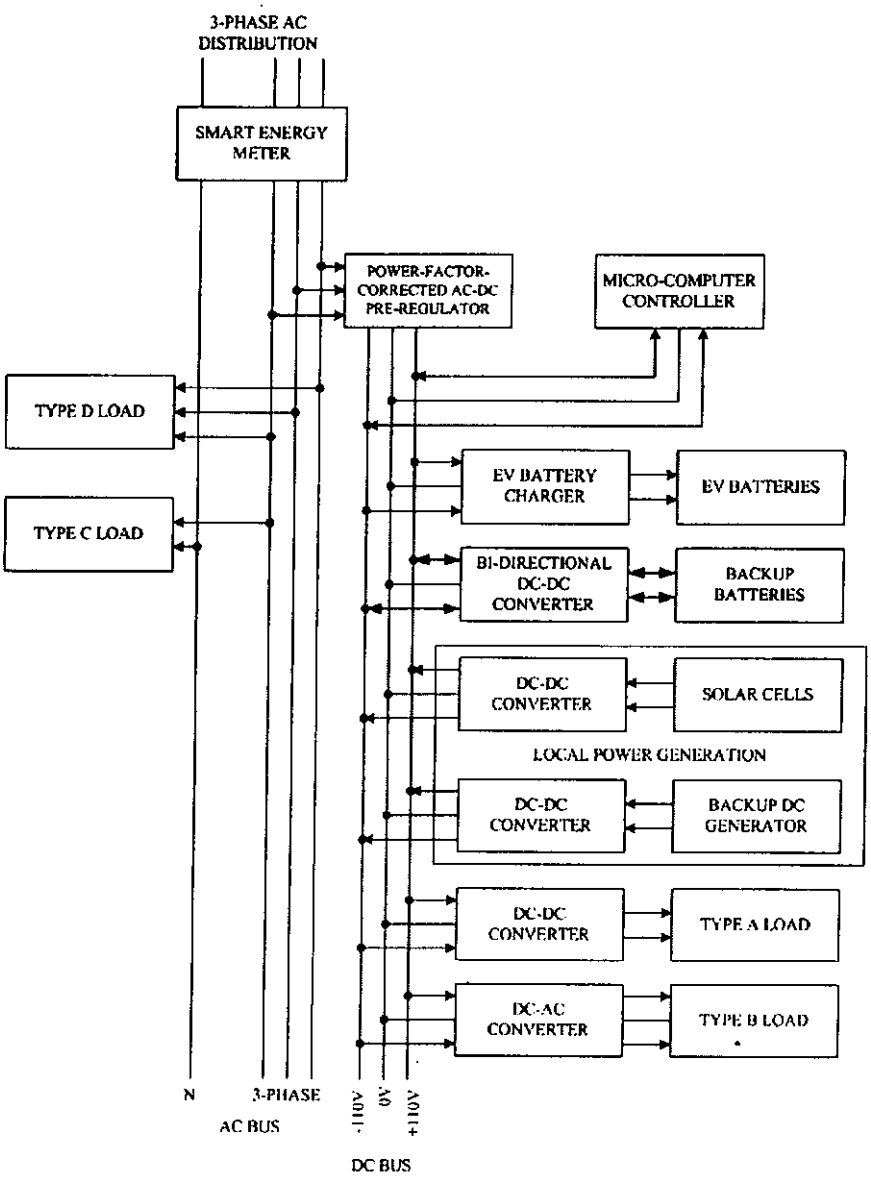


Fig. 1.1 The DC power system proposed by P. W. Lee and Y. S. Lee.

In the proposed DC power system, there are four classes of loads:

TYPE A LOAD: DC-operated equipment.

TYPE B LOAD: AC-operated equipment which require power factor correction and/or uninterruptible power.

TYPE C LOAD: Single-phase AC-operated equipment which do not require power factor correction and uninterruptible power.

TYPE D LOAD: Three-phase AC-operated equipment.

In the system, the DC bus derives power from an AC source via a power-factor-correction AC-DC converter. DC-operated equipment can draw power from the DC bus without the need of rectification. Backup batteries, solar cells, and DC generators can help provide uninterruptible power via corresponding DC-DC converters. Paralleling DC power sources is relatively simple because it does not require the conventional AC waveform shaping and synchronization. All the blocks are monitored and controlled by the micro-computer controller, which would help to realize home automation. The design of the DC distribution system is aimed at improving efficiency, cost effectiveness, compatibility, modularity, and safety.

1.2 Power Factor (PF) and Power Factor Correction (PFC)

One of the most important parts of the proposed DC power system is the power-factor-correction rectifier. Such a rectifier is responsible for converting AC to DC and it should have low harmonic currents and high power factor.

For sinusoidal voltages and currents, the power factor is given by [15].

$$PF = \cos\theta \tag{1-1}$$

where θ is the phase angle between the voltage and current.

PF can also be defined as the ratio of the real power to the apparent power.

$$PF = \frac{\text{Real Power}}{\text{Apparent Power}} = \frac{\text{Real Power}}{V_{in,rms} \cdot I_{in,rms}} \tag{1-2}$$

where $V_{in,rms}$ and $I_{in,rms}$ are RMS values of line voltage and line current, respectively.

If the current waveform is distorted, it will have harmonic components at multiple frequencies besides its fundamental frequency. The total harmonic distortion (THD) is the ratio of the total harmonic current to the fundamental component of the current. Assuming there is no DC offset, the THD can be defined as

$$THD = \sqrt{\frac{\sum_{n \neq 1} I_n^2}{I_1^2}} \tag{1-3}$$

where I_1 is the fundamental current and I_n is the nth harmonic current.

The relationship between PF and THD is

$$PF = \sqrt{\frac{1}{1 + THD^2}} \tag{1-4}$$

The goal of PFC is to reduce the harmonic content of the current waveform and keep the phase angle between the voltage and current small.

One of the reasons to limit the harmonic currents and to improve the power factor is to maximize the use of the full current rating of the available

AC power source. While harmonic currents do not contribute to the power delivery, they do contribute to the RMS value of the current waveform. For example, a 220V, 10A system with a power factor of 0.5 is able to supply only 1.1kW of power without tripping the line circuit breaker. But if the power factor can be improved to one, the maximum output power can be increased to 2.2kW.

In order to set limits on harmonic currents, several regulations have been issued. A well-known European requirement is EN 61000-3-2 [16]. This specification sets limits on harmonic currents for any power supplies sold in the European Union (EU). Implementation of such regulations has accelerated the development of PFC for switching power supplies. Tables 1.1, 1.2, and 1.3 show the IEC harmonic limits for equipment of Class A, C, and D, respectively.

Table 1.1 Limits for Class A Equipment

Harmonic order, n	Maximum permissible harmonic current, A
3	2.30
5	1.14
7	0.77
9	0.40
11	0.33
13	0.21
$15 \le n \le 39$ (Odd harmonic only)	$0.15 \times \frac{15}{n}$
2	1.08
4	0.43
6	0.30
$8 < n < 40$ (Even harmonic only)	$0.23 \times \frac{8}{n}$

Table 1.2 Limits for Class C Equipment

Harmonic order, n	Maximum permissible harmonic current expressed as percentage of the input current at the fundamental frequency, %
2	2
3	30 × PF
5	10
7	7
9	5
$11 \leq n \leq 39$ (Odd harmonics only)	3

Table 1.3 Limits for Class D Equipment

Harmonic order, n	Maximum permissible harmonic current per watt, mA/W	Maximum permissible harmonic current, A
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.4
11	0.35	0.33
13	0.296	0.21
$15 \leq n \leq 39$ (Odd harmonic only)	$\frac{3.85}{n}$	$0.15 \times \frac{15}{n}$

Class A is balanced three-phase equipment and all equipment not covered by other classes. Class B applies to portable tools and its limits are 1.5 times the corresponding values in Table 1.1. Class C covers lighting equipment, including dimmers. Class D is personal computers, computer monitors, and television receivers.

1.3 Background

The conventional method to derive DC power from an AC line without power factor correction is to employ a rectifier bridge with a simple capacitor input filter. Consider a single-phase AC input circuit as shown in Fig. 1.2.

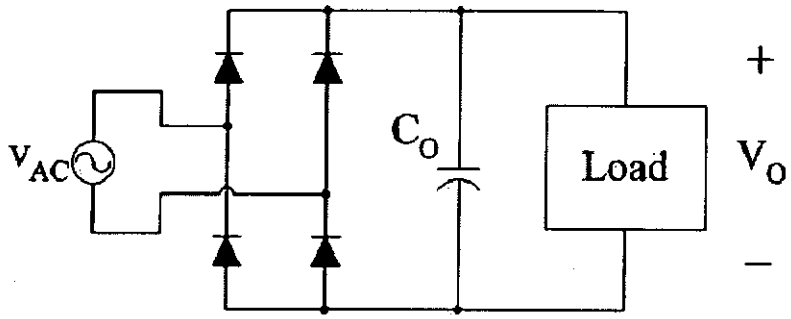


Fig. 1.2 Conventional structure of AC – DC without PFC.

In this structure, the input filter capacitor C_O is charged to nearly the peak AC line voltage, supporting an unregulated DC bus. Here, C_O should be large enough to meet the hold-up requirement. Because the rectifier bridge only conducts when instantaneous line voltage is above the DC bus, the line current waveform becomes narrow pulses with very high peak value for each half line cycle. The waveforms of line voltage and line current are shown in Fig. 1.3.

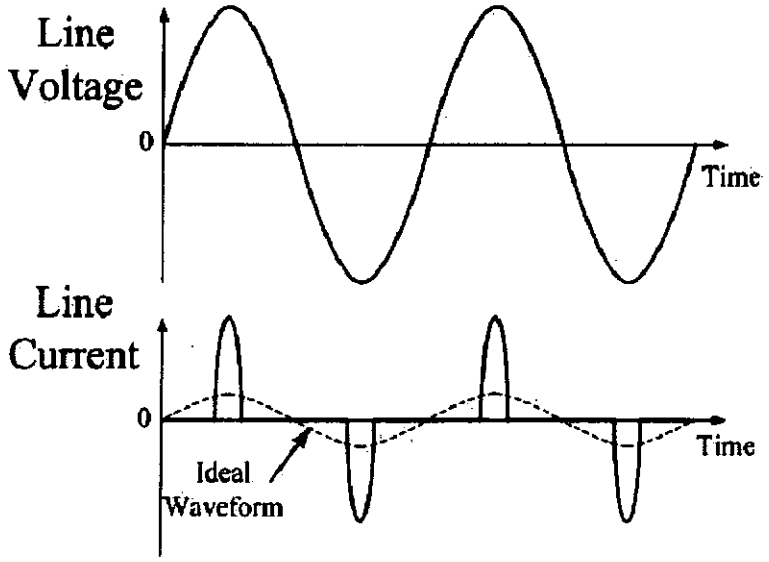


Fig. 1.3 Line voltage and current waveforms without PFC.

The line current waveform is far from sinusoidal and its typical input power factor is only 0.5 ~ 0.65. High harmonic currents exist in the line and causes line noises.

Both passive and active techniques can be used to lower the harmonic currents and improve the power factor. Fig. 1.4, Fig. 1.5, and Fig. 1.6 show three examples of passive power factor correction circuits [17]-[19].

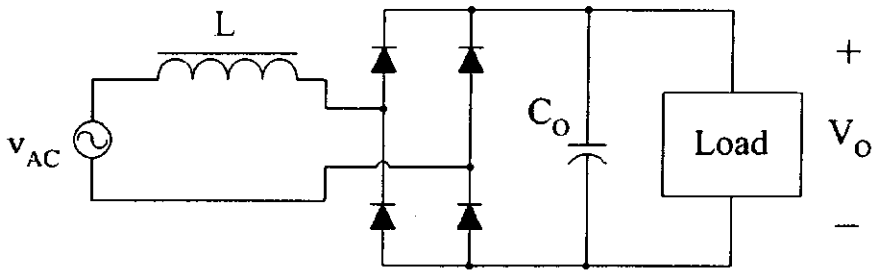


Fig. 1.4 Passive method to improve PF by adding a large inductor L.

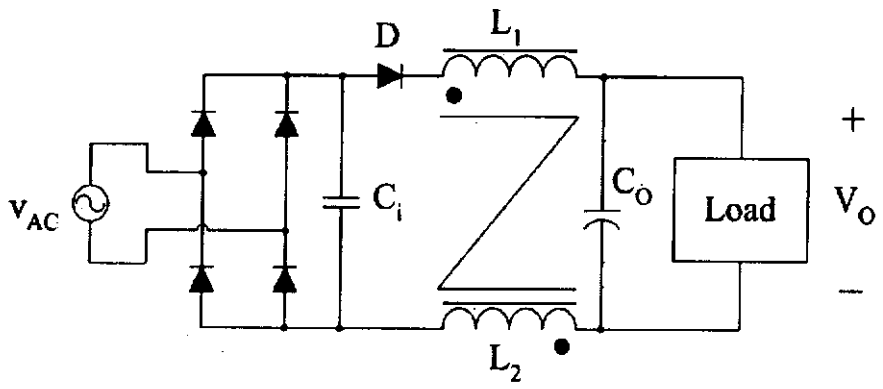


Fig. 1.5 Passive method to improve PF by adding LCD.

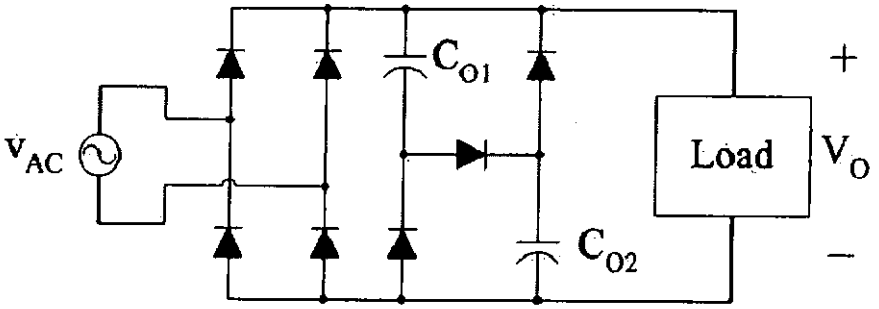


Fig. 1.6 "Valley fill" circuit.

Generally, passive techniques rely on a combination of inductors and capacitors to smooth out the current waveform. Although this approach is very simple and inexpensive, it is very hard to optimize for universal line operation. In order to meet the THD requirements, inductors and capacitors are usually very large and heavy. Therefore, passive approach is used only in low power and fixed line voltage applications.

High switching frequency (typically over 30kHz) active techniques have been widely used in PFC applications. Compared with the passive method, active techniques can further improve power factor, operate over a wide line voltage range, and reduce the size and cost of magnetic devices

and bulk capacitor. Therefore, for high power applications, active PFC is a better solution.

1.4 Objective and Outline of the Thesis

1.4.1 Objective

The objective of this research project is to study the design of active power-factor-correction converters for environmentally green energy management systems. Novel topologies are proposed to perfect the performance of PFC and to improve the efficiencies of the converters. Integrated Magnetics [20]-[27], which can integrate two or more magnetic components into a single magnetic core, will be incorporated into the circuits to reduce the number of magnetic components.

Only single-phase AC input is considered in this thesis. However, for three-phase AC input, three single-phase active rectifiers can be paralleled to drive a single DC output bus. Such a modular design can improve the reliability of the system.

1.4.2 Outline of the Thesis

Chapter 2 will review the operation of active PFC circuits. Some basic concepts are introduced first. Then basic topologies for active PFC circuits are discussed. Several single-stage PFC circuits are presented next. Finally, the operation modes and control methods of the boost topology are explained in detail.

Chapter 3 proposes a novel single-switch high-power-factor regulator with low output current ripple which is suitable for low power applications.

The proposed regulator achieves a high power factor and near-zero output current ripple. It also eliminates the need for an extra clamping switch to recycle the energy trapped in the transformer leakage inductance. The basic circuit topology and the principle of operation of the proposed regulator will be explained first. Next, design considerations will be given. Simulation and experimental verification, based on the analysis in the former sections, will be reported finally.

Chapter 4 proposes a two-channel interleaved boost converter using an integrated magnetic component to reduce the core and copper losses. With the proposed winding arrangement, inductors can be designed to have smaller inductances and lower copper losses. The windings on the two outer legs are inversely coupled and the AC flux ripple in the center leg is cancelled. The derivation and electrical circuit model of the proposed integrated magnetic component are discussed. The principle of operation and design considerations are given. Experimental results are presented to verify the performance of the proposed integrated magnetics.

Chapter 5 presents a three-channel interleaved CCM boost converter using inversely-coupled integrated inductors. Three channels have been used to share the output power. All the output rectifiers in the proposed converter can be turned off softly and a very high efficiency is obtained. The winding arrangement of the inversely-coupled integrated inductors is discussed and the equivalent-circuit model is derived. The principle of operation of the converter and the design issues are also explained. Finally, the operation and performance of the converter is verified by simulation and experimental setup.

In Chapter 6, the last chapter, conclusions and suggestions for future research are given.

CHAPTER 2

ACTIVE PFC CIRCUITS

2.1 Introduction

Active PFC circuits are often interposed between the input rectifier bridge and the bulk filter capacitor, as shown in Fig. 2.1.

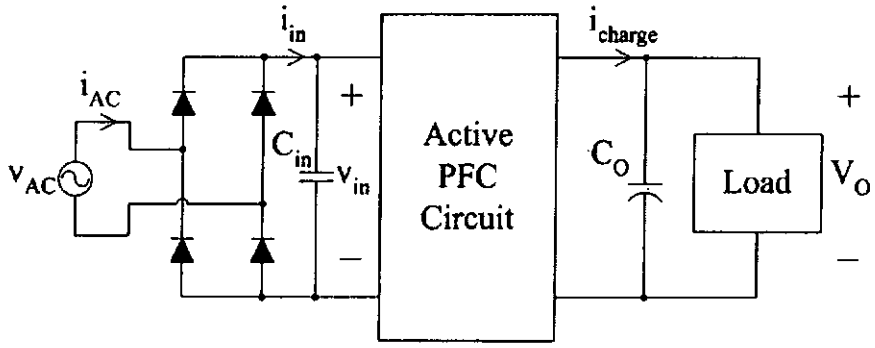


Fig. 2.1 Typical diagram for an active PFC system.

In Fig. 2.1, C_{in} is a small high frequency filter capacitor. Because active PFC circuits operate at a switching frequency much greater than the line frequency, the switching frequency component will be filtered by C_{in}. As a result, the input current i_{in} contains only the low frequency component. Active PFC circuits are programmed to draw an i_{in} which varies in direct instantaneous proportion to the input voltage v_{in}. Consequently, the voltage and current waveforms on the input side of the rectifier bridge are in phase with each other. Compared with the passive method, active techniques can

improve the PF to 0.999 and limit the harmonics below 3% if necessary [28]. Typical waveforms of active PFC circuits are shown in Fig. 2.2.

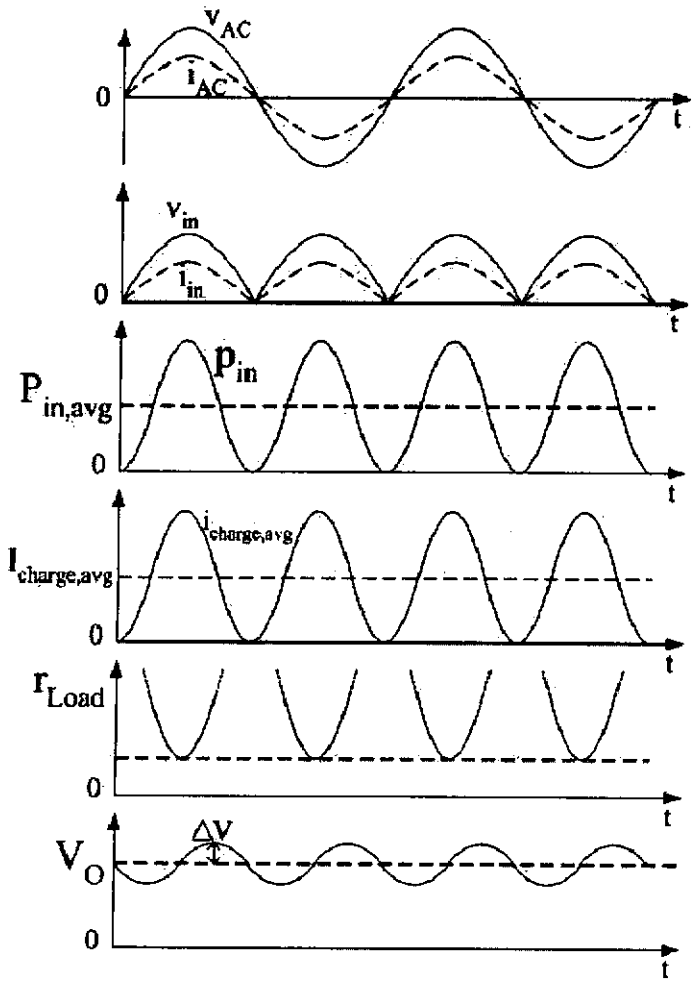


Fig. 2.2 General waveforms for active PFC circuits.

In Fig. 2.2, p_{in} is the instantaneous input power and $P_{in,avg}$ is the average value of p_{in}. $i_{charge,avg}$ is the average value of i_{charge} and $I_{charge,avg}$ is the average value of $i_{charge,avg}$. Because the active PFC circuit has relatively high PF, we can assume that the expressions of v_{in} and i_{in} are (for each half line cycle):

$$v_{in} = \sqrt{2} \cdot V_{in,rms} \sin(\omega t) \qquad (2\text{-}1)$$

$$i_{in} = \sqrt{2} \cdot I_{in,rms} \sin(\omega t) \tag{2-2}$$

where $V_{in,rms}$ and $I_{in,rms}$ are the RMS values, and ω is angular frequency, of the AC line input.

The instantaneous input power can be found as follows:

$$\begin{aligned} p_{in} &= v_{in} \cdot i_{in} \\ &= 2V_{in,rms} \cdot I_{in,rms} \cdot \sin^2(\omega t) = V_{in,rms} \cdot I_{in,rms} \cdot [1 - \cos(2\omega t)] \end{aligned} \tag{2-3}$$

The average input power is

$$P_{in,avg} = V_{in,rms} \cdot I_{in,rms} \tag{2-4}$$

Supposing the bulk capacitor C_O is large enough to hold the DC bus voltage V_O fairly constant, from (2-3) and (2-4) we have

$$i_{charge,avg} = \frac{p_O}{V_O} = \eta \cdot \frac{p_{in}}{V_O} = \eta \cdot \frac{P_{in,avg}}{V_O} \cdot [1 - \cos(2\omega t)] \tag{2-5}$$

$$I_{charge,avg} = \eta \cdot \frac{P_{in,avg}}{V_O} \tag{2-6}$$

where η is the conversion efficiency.

From (2-5) and (2-6), the load "seen" by the active PFC circuit can be found as [29]

$$\begin{aligned} r_{Load} &= \frac{V_O}{i_{charge,avg}} = \frac{V_O^2}{\eta \cdot P_{in,avg} \cdot [1 - \cos(2\omega t)]} \\ &= \frac{R}{1 - \cos(2\omega t)} \end{aligned} \tag{2-7}$$

where R is the equivalent DC power load.

From (2-7) it can be seen that, the load "seen" by the active PFC circuit reaches its minimum value when $\omega t = \frac{\pi}{2}$. The maximum value of r_{Load} is infinity, which occurs at $\omega t = 0$ or π.

It should be noted that the output voltage V_O is only crudely regulated. The AC component of $i_{charge,avg}$ produces a small ripple voltage at twice the line frequency on the DC bus, as shown in Fig. 2.2. However, this resulting narrow DC bus voltage range permits the downstream converters to be designed to have lower cost, better reliability and higher efficiency.

The main drawback of active PFC techniques is the complexity of design and the cost of manufacturing and packaging (compared with passive techniques). Moreover, active PFC circuits can produce large EMI.

2.2 Topologies for Active PFC Circuits

Three basic power circuit topologies – boost, buck, and buck-boost – can be used as active PFC circuits. In fact, these three topologies form the basis for other active PFC techniques. In this section, these three topologies will be introduced first. Sepic and Cuk topologies, which can be considered as combinations of basic topologies, will next be discussed briefly.

2.2.1 Boost Converter

Fig. 2.3 shows the circuit of a boost converter. As the most popular topology used in PFC applications, boost converter has many attractive features. The inductor is in series with the input path, which makes the input current smooth (not switched). This minimizes the line noise and makes EMI filter design easier. In addition, line spikes are absorbed by the inductor, which will increase the circuit reliability. The location of the inductor also makes it easy to use current mode control to program the input current, because the inductor current is exactly the same as the input current.

The transistor switch is with a ground reference, which makes it easy to drive. Although the output voltage V_O is required to exceed the maximum peak line voltage, which may be considered as too high in some applications, such a feature enables converter to operate over the full line voltage range, from zero to the maximum peak value.

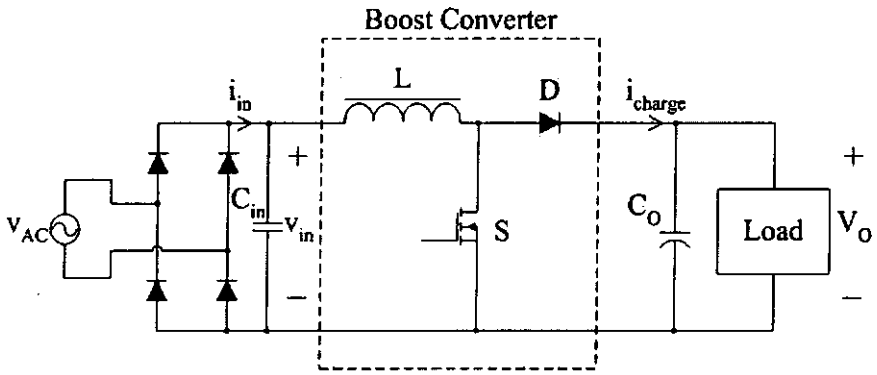


Fig. 2.3 Boost converter.

The main disadvantage of boost topology is the inability to limit current because there is no series switch between the input and output. Overload or startup overcurrent conditions can not be controlled or limited. Conventionally, an extra rectifier is needed to parallel between the input and output, providing a lower impedance path to protect the inductor and output rectifier during overload and startup conditions. Moreover, isolation between input and output can not be easily implemented. For peak current mode control, slope compensation is difficult to accomplish with the boost topology because the inductor current down slope varies considerably with v_{in}.

2.2.2 Buck Converter

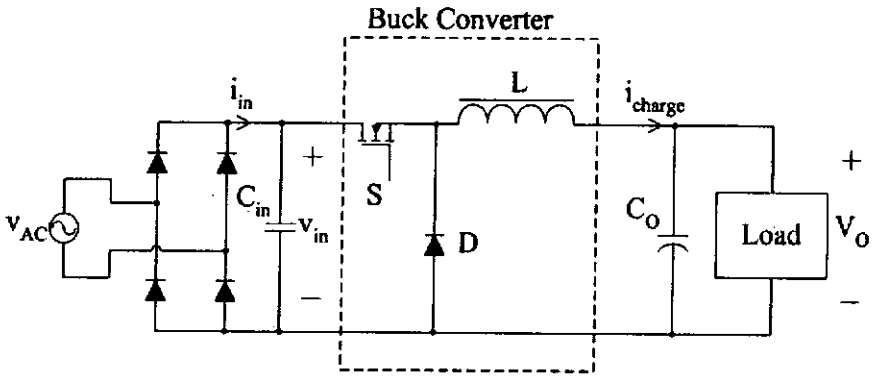


Fig. 2.4 Buck converter.

Fig. 2.4 shows the circuit of a buck converter. A Buck converter requires that the output voltage V_O to be less than the input voltage v_{in}. This makes it unsuitable for PFC because it does not work when v_{in} falls below V_O. The chopped input current waveform results in more noise and EMI than the comparable boost topology. The switch is also difficult to drive since it is floating. However, it is very easy to provide current limit because an active switch is placed between the input and output.

2.2.3 Buck-Boost Converter

Fig. 2.5 shows the circuit of a buck-boost converter. It should be noted that in a buck-boost converter the output voltage V_O is opposite in polarity to the input voltage v_{in}. In order to provide polarity inversion, the inductor L must be replaced by a transformer, which is shown in Fig. 2.6.

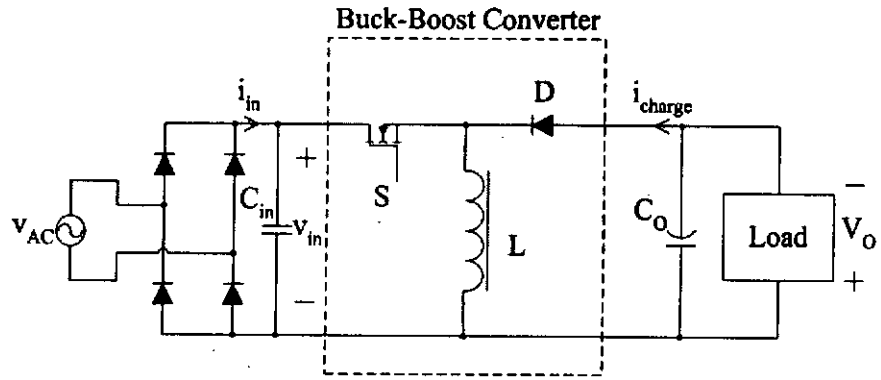


Fig. 2.5 Buck-boost converter.

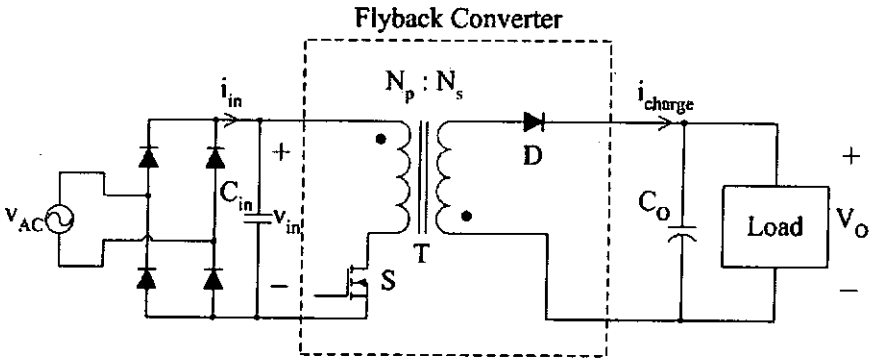


Fig. 2.6 Flyback converter.

The converter shown in Fig. 2.6 is often called as "flyback converter". A buck-boost converter is the special case of a flyback converter when the transformer turn ratio $N_p : N_s = 1:1$.

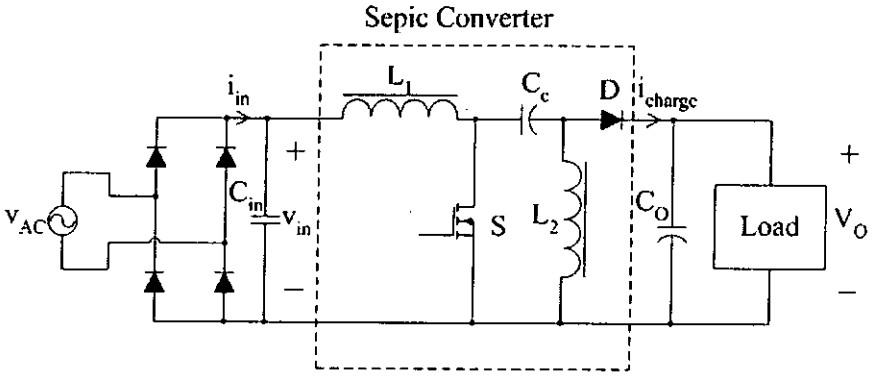
Compared with a boost converter, a flyback converter can control and limit the start-up inrush current and the overload current. The output voltage can be higher or lower than the instantaneous input voltage. In addition to possible polarity inversion, the transformer can also provide isolation between input and output, relieving the downstream converters of this isolation requirement. The location of the transistor switch also makes it

easy to drive. Furthermore, when a flyback converter operates in discontinuous mode, the amplitude of its input current can automatically follow the input voltage (assuming constant switching frequency and duty cycle) [30]. No current loop control is required (for discontinuous operation).

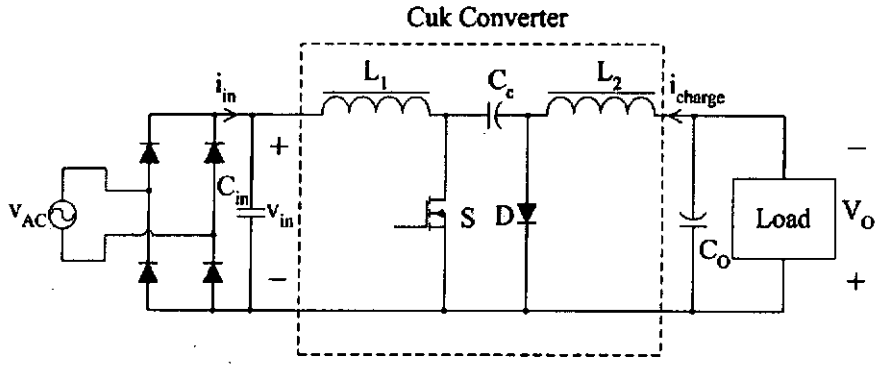
However, since the input current waveform is chopped, it produces the EMI problems and requires more input filtering. When the converter operates in discontinuous mode, high peak current will also increase the transistor switch current rating requirement. In addition, the leakage inductance of the transformer will cause large voltage spike on the transistor switch during turn-off. A passive or active snubber or higher rating switch will be needed.

2.2.4 Sepic and Cuk

As shown in Fig. 2.7, both Sepic [31] and Cuk [32] converters have two inductors: one located at the input and the other located at the output. A Sepic converter can be regarded as a combination of boost topology and buck-boost topology, while a Cuk converter can be considered as a combination of boost topology and buck topology.



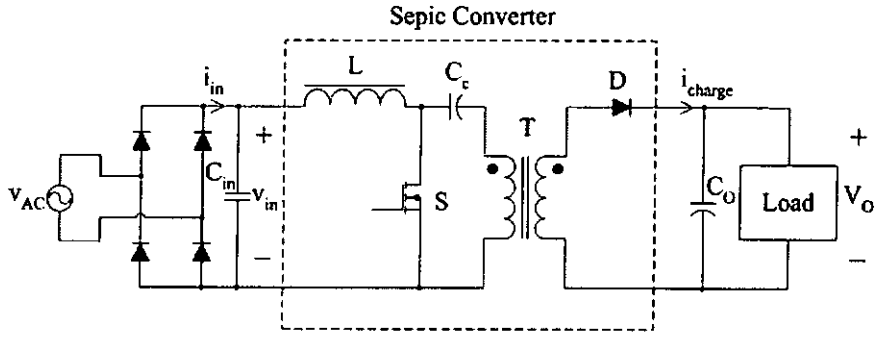
(a)



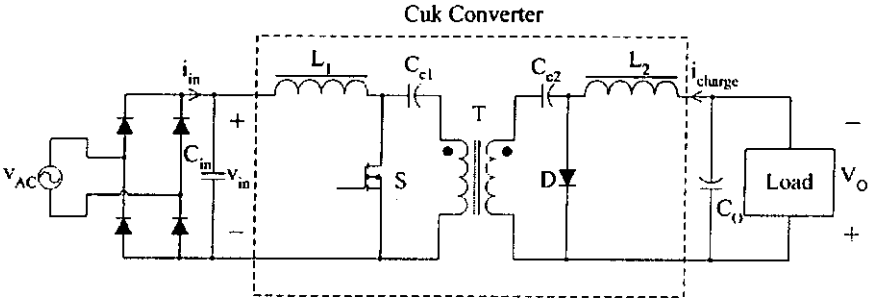
(b)

Fig. 2.7 Sepic (a) and Cuk (b) converters.

The transformer isolated versions of Sepic and Cuk converters are shown in Fig. 2.8.



(a)



(b)

Fig. 2.8 Isolated Sepic (a) and isolated Cuk (b) converters.

Both Sepic and Cuk converters can have continuous input current, reducing the need for input noise filtering. Inrush and overload current limiting is practically easy to achieve. Only a single switch is used and its location makes the gate drive easy to design. The use of a transformer can provide isolation and output polarity inversion. In addition, when they operate in discontinuous mode, unity power factor can be attained even without current loop control [33]. Articles [34] and [35] found that when the two inductors in Fig. 2.7 (or the inductors and transformers in Fig. 2.8) are coupled together, the dynamic response can be improved and the high frequency ripple of the input current can be steered away.

However, compared with the basic topologies, these converters need more components and have higher voltage and current stresses. The transformer leakage inductance can also cause large voltage spikes and difficulty energy recovery problems.

2.3 Active Single-Stage PFC Circuits

The converters discussed so far are often referred as "PFC Pre-regulators". Their main role is to attain high power factor and low harmonic currents. The output voltage V_O is only crudely regulated. In order to get the required DC bus, a DC – DC converter is often deployed after the bulk capacitor, which is shown in Fig. 2.9.

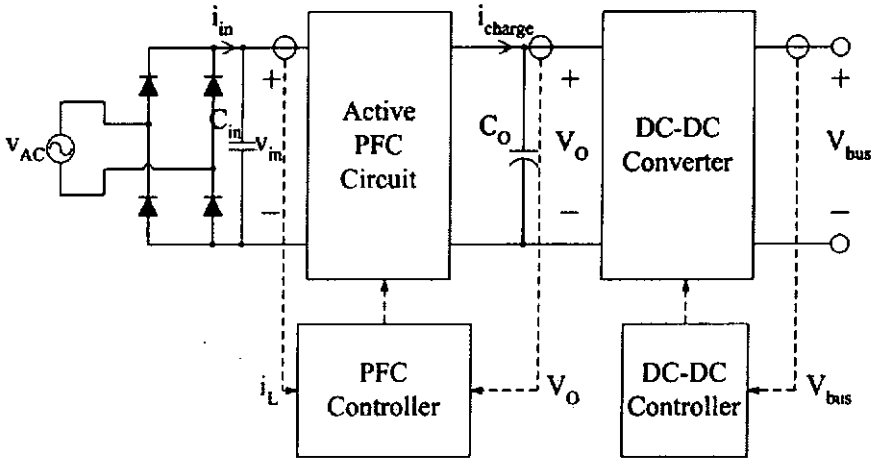


Fig. 2.9 A two-stage active PFC circuit.

The DC – DC converter in Fig. 2.9 can be regarded as the "load" of the active PFC circuit. So Fig. 2.9 is essentially the same as Fig. 2.1. In Fig. 2.9, the two converters are controlled independently. Thus, both high quality input-current waveform and fast output voltage regulation are achieved. Since the two converters employ different active components and controllers, they are referred to as a "two-stage PFC" circuit.

However, for low power applications (typically below 200W), the two-stage PFC is not an optimized design, because of the cost of additional semiconductor switches and control circuitry. In order to get a cost-effective solution, single-stage PFC circuits are proposed [36]-[45]. A single-stage PFC circuit includes two parts: an input-current waveform shaper and an isolated DC – DC converter. These two parts are integrated with a shared switch and controller. Fig. 2.10 shows the typical structure of a single-stage PFC circuit.

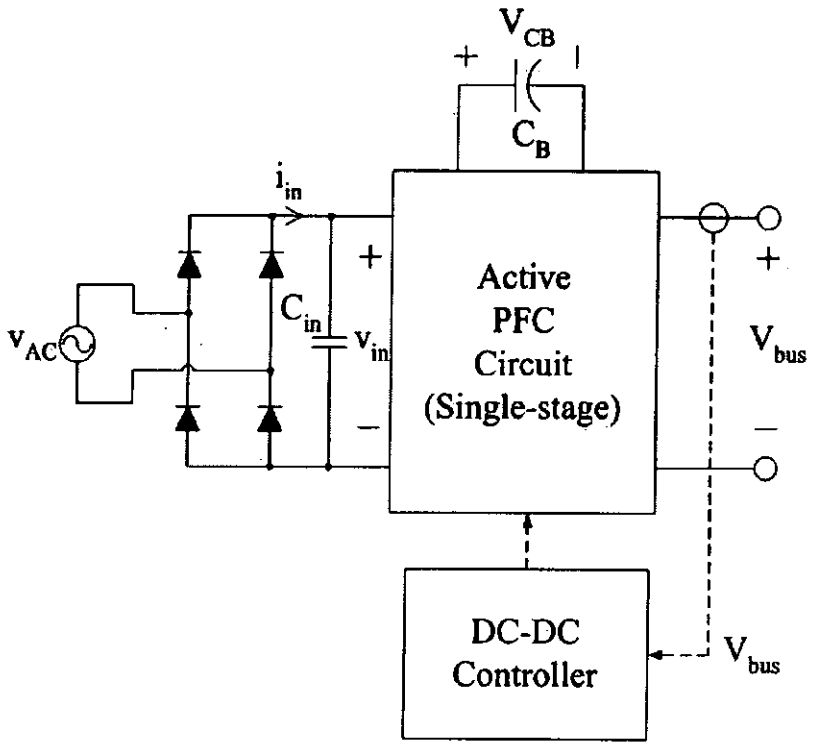


Fig. 2.10 A single-stage active PFC circuit.

The energy storage device C_B serves as a buffer between the input-current waveform shaper and the DC – DC converter. It also provides the hold up time. A fast control loop is used to control the output bus voltage. A reasonably good input current waveform is still maintained due to the natural characteristics of the input-current waveform shaper of the single-stage PFC converter.

Here several typical examples of single-stage PFC circuits will be briefly introduced.

2.3.1 Dither Rectifier

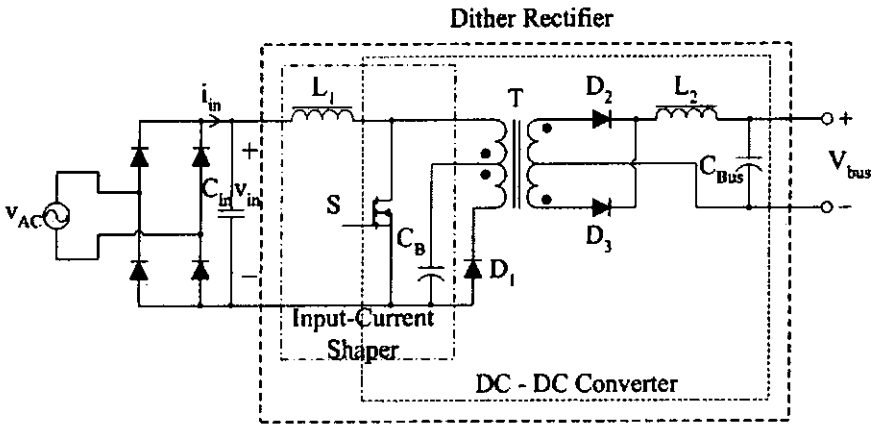


Fig. 2.11 Dither rectifier.

Fig. 2.11 shows the circuit of a Dither rectifier [38]. This is an early form of the single stage PFC circuit that integrates a boost input-current waveform shaper with a DC – DC converter. Both pulse width modulation (PWM) and frequency modulation (FM) were applied in the control circuit to regulate the output voltage and keep the voltage across the energy storage device C_B constant. Although the input current was not actively controlled, the rectifier still had a very high power factor (about 0.992). However, the circuit suffered wide frequency variation and the efficiency was low.

2.3.2 Boost Integrated with Flyback Rectifier/Energy Storage/DC-DC Converter (BIFRED) and Boost Integrated with Buck Rectifier/Energy Storage/DC-DC Converter (BIBRED)

Fig. 2.12 and Fig. 2.13 show the circuits of BIFRED and BIBRED [39]. BIFRED integrates the boost input-current waveform shaper with a flyback

converter while BIBRED integrates the boost input-current waveform shaper with a buck converter. The energy storage capacitor C_B is in the series path of the energy flow in both circuits. The boost input-current waveform shaper operates in discontinuous conduction mode (DCM) to achieve automatic input-current waveform shaping. The DC – DC converter operates in continuous conduction mode (CCM) to lower the conduction loss. However, in such an operation mode, the voltage on C_B has a strong dependency on the output load. For universal input applications, it will suffer from high voltage stress at light load. Articles [40] and [42] proposed to use frequency modulation method to keep voltage under control during light load. Article [41] showed that if both the input-current waveform shaper and the DC – DC converter operate in DCM, the voltage across the energy storage capacitor can be independent of the load and the input current waveform can be significantly improved.

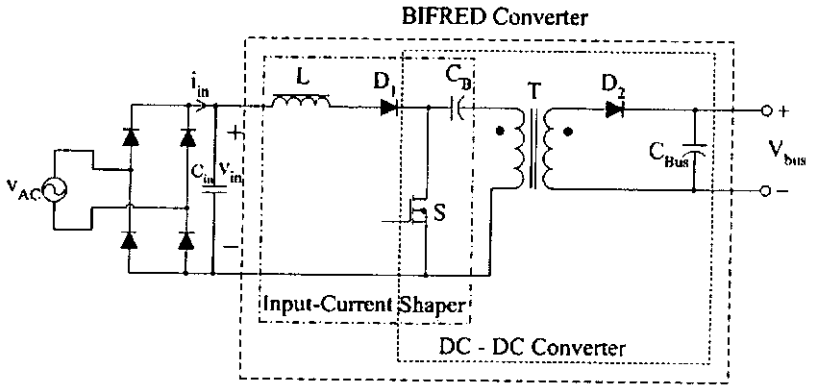


Fig. 2.12 BIFRED converter.

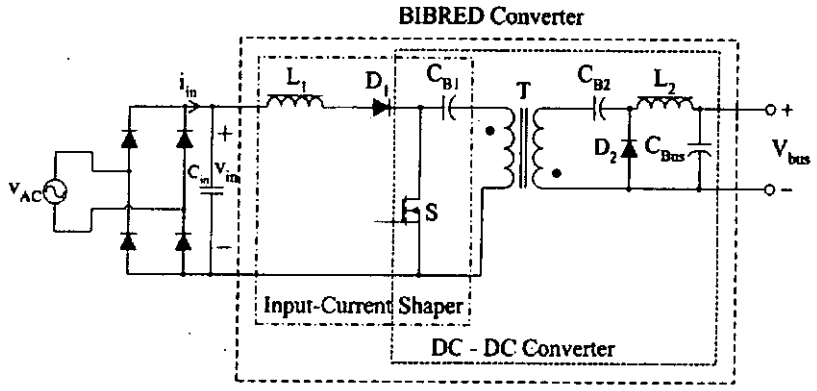


Fig. 2.13 BIBRED converter.

2.3.3 Single-Stage Isolated Power-Factor-Corrected Power Supply (SSIPP)

Fig. 2.14 shows the circuit of a SSIPP converter [43]. Similar to BIFRED and BIBRED, SSIPP integrates a boost input-current waveform shaper with a DC – DC converter. However, in SSIPP, the energy storage capacitor C_B is in the parallel path of the energy flow. The boost input-current waveform shaper operates in DCM to achieve automatic input-current waveform shaping, while the DC – DC converter can operate in either DCM or CCM. Article [43] suggested that the DC – DC converter should operate in DCM to avoid high voltage stress at high input voltage and light load. But DCM operation will lead to higher conduction loss, larger ripple, and larger filter. For this reason, CCM operation is preferred for low voltage applications and switching frequency modulation methods were reported to alleviate the voltage across the energy storage capacitor [44][45].

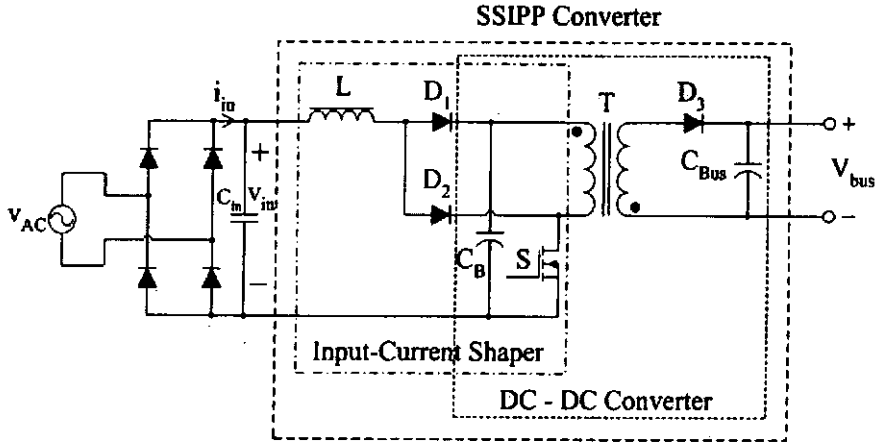


Fig. 2.14 SSIPP converter.

2.4 Operation of the Boost Converter

From the analysis above, it can be seen that boost topology is the most appropriate topology for active PFC applications. For two-stage PFC circuits, boost converters are often used as the "front-end" because of its smooth input current waveform, simplicity, and high conversion efficiency. For single-stage PFC circuits, boost topology has been widely employed as the input-current waveform shaper. Boost converters usually operate in CCM in two-stage PFC circuits while in single-stage PFC circuits, DCM will offer automatic input-current waveform shaping. Therefore, it is necessary to discuss the operation modes of the boost topology in detail.

According to the inductor current waveform, the boost converter can operate in three modes, CCM, critical conduction mode (CRM), and DCM. In this section, three operation modes of the boost converter and the corresponding control methods will be introduced. The advantages and disadvantages of each operation mode will also be discussed.

2.4.1 CCM Operation

2.4.1.1 Introduction

Let us redraw the schematic of the boost converter in Fig. 2.15. The AC source, the rectifier bridge, and the input filter capacitor C_{in} are replaced by a DC source.

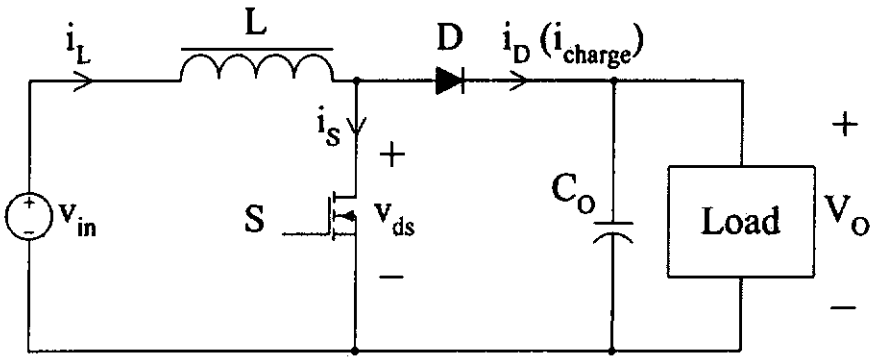


Fig. 2.15 Simplified boost converter.

The current waveforms of CCM operation are shown in Fig. 2.16.

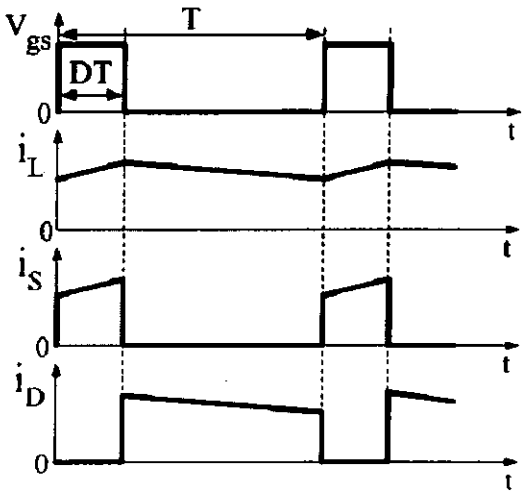


Fig. 2.16 Main waveforms for CCM operation.

In CCM operation, the inductor current i_L will not be reduced to zero after a switching cycle during steady state. The inductor current has a small ripple and its peak value is close to the average value. In this operation mode, the inductor L usually has a very large inductance.

Because the voltage-second applied on the inductor should balance for each cycle, we have

$$v_{in} \cdot DT = (V_O - v_{in}) \cdot (1 - D)T \tag{2-8}$$

$$D = 1 - \frac{v_{in}}{V_O} \tag{2-9}$$

where D is the duty cycle and T is the switching period.

From (2-9) it can be seen that, as the line voltage varies, the duty cycle will vary accordingly. D will become maximum when input line voltage is close to zero while the minimum value of D will occur at the peak value of input voltage. In this operation mode, the boost converter usually operates at constant frequency and variable duty cycle to achieve PFC.

The small ripple current can reduce the conduction losses in both the switch and the output rectifier. However, from Fig. 2.16 it can be seen that, when the switch is turned on, the output rectifier still has forward current flowing in it. Since the rectifier needs time to recover and it can not be turned off immediately, the output capacitor is nearly shorted to ground at this instant. Very large current spikes can be observed both at the rectifier and at the switch, which are shown in Fig. 2.17.

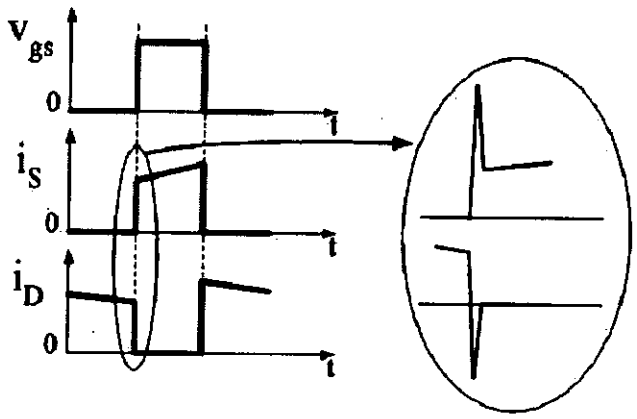


Fig. 2.17 Reverse recovery effect.

Such spikes will not only lower the conversion efficiency but also cause severe electromagnetic interference noise. Therefore, in CCM operation, passive snubbers and active techniques are often employed to reduce the effects of the reverse recovery current. As a result, the efficiency of a CCM boost converter would be significantly improved.

2.4.1.2 Control Methods

A. Average Current Mode Control

Because the inductor current is the input current, if we want to program the input current half sine, average current mode control [46] is ideal. Average current mode control has the advantage of directly controlling the average inductor current, which is equal to the input current, the quantity we want to control in a PFC circuit. Fig. 2.18 shows the simplified control block diagram.

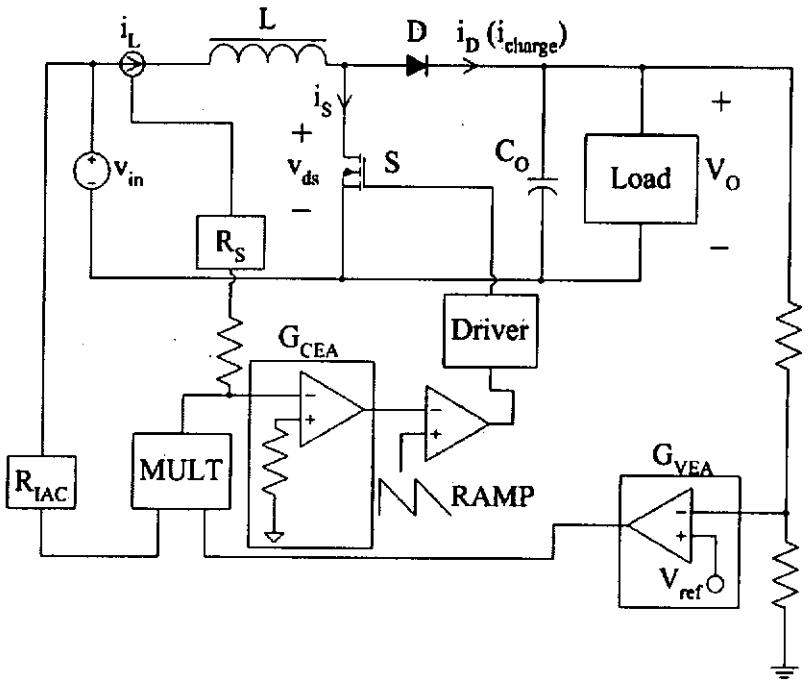


Fig. 2.18 Simplified block diagram of average current mode control.

The output voltage of the PFC converter V_O is typically divided down and monitored by the inverting input of the voltage error amplifier G_{VEA}. The non-inverting input of G_{VEA} is biased at a reference voltage V_{ref}. The error between the two inputs are amplified and connected to the multiplier. Another input of the multiplier is the AC full wave rectifier haversines, which is monitored through R_{IAC}. The multiplier is the heart of a PFC controller and its output provides the current reference as the AC voltage traverses sinusoidally from zero to peak line, as shown in Fig. 2.19.

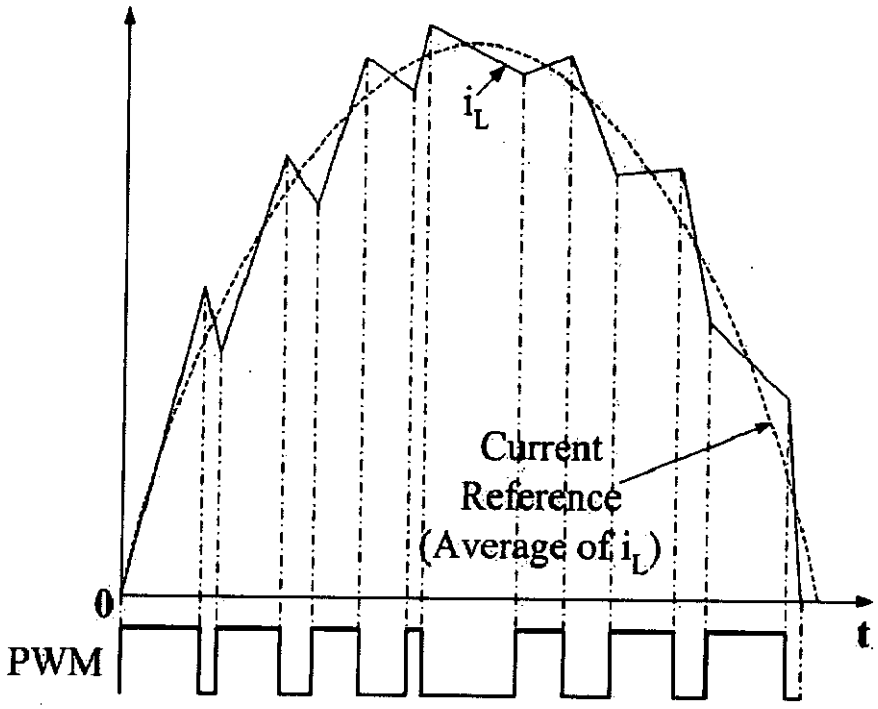


Fig. 2.19 Inductor current waveform for average current mode control.

The inductor current i_L is sensed and compared with the reference. The error between them is amplified by the current error amplifier G_{CEA}. Because of the high gain of G_{CEA}, the gain-bandwidth characteristic of the current loop can be tailored for optimum performance. The average inductor current can track the current reference with a high degree of accuracy. Finally, the output of G_{CEA} is compared to a large amplitude sawtooth (oscillator ramp) and the output of the comparator is used as the gate drive signal.

Average current mode control can achieve very high power factor and it does not require slope compensation. It can function well even when the converter crosses into DCM. In addition, noise immunity is excellent in average current mode control.

Average current mode control method can be used to sense and control the current in any circuit branch. For example, it can be used to control the input current accurately with buck and flyback topologies, and to control output current with boost and flyback topologies.

B. Peak Current Mode Control

Since the ripple of the inductor current in CCM boost is quite small and the peak value of the inductor current is close to the average value, peak current mode control can also be used to achieve PFC. Fig. 2.20 shows the control block diagram.

One of the main differences between average current mode control and peak current mode control is that, the peak current mode control does not use a current error amplifier. The current reference provided by the multiplier is directly compared with the peak value of the inductor current sensed by R_S. The output of the comparator is used as the gate drive signal. In peak current mode control, slope compensation must be added to ensure stability when duty cycle exceeds 50%.

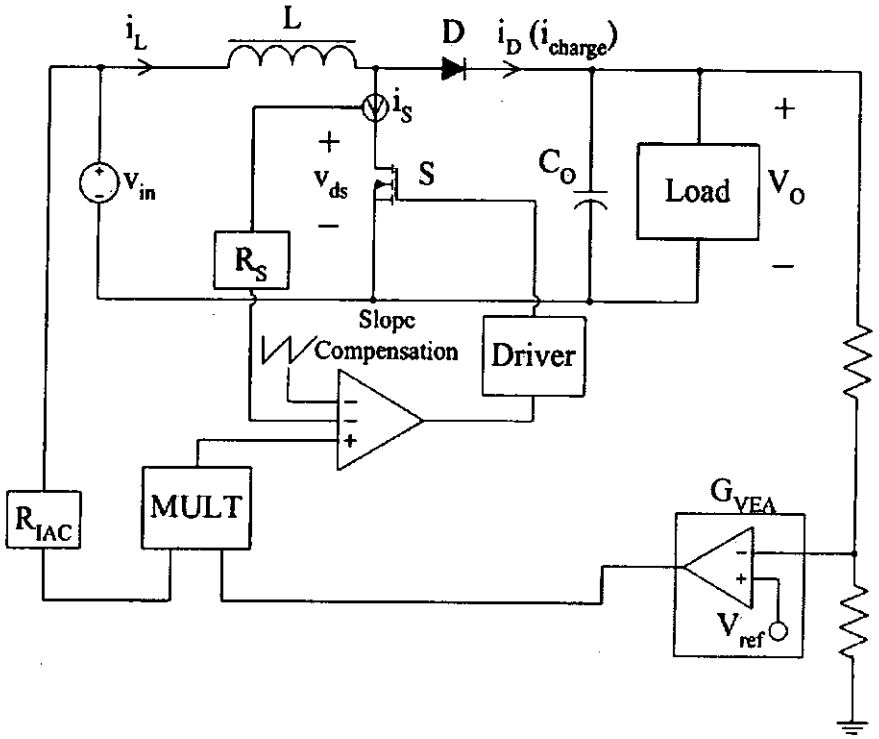


Fig. 2.20 Block diagram of peak current mode control.

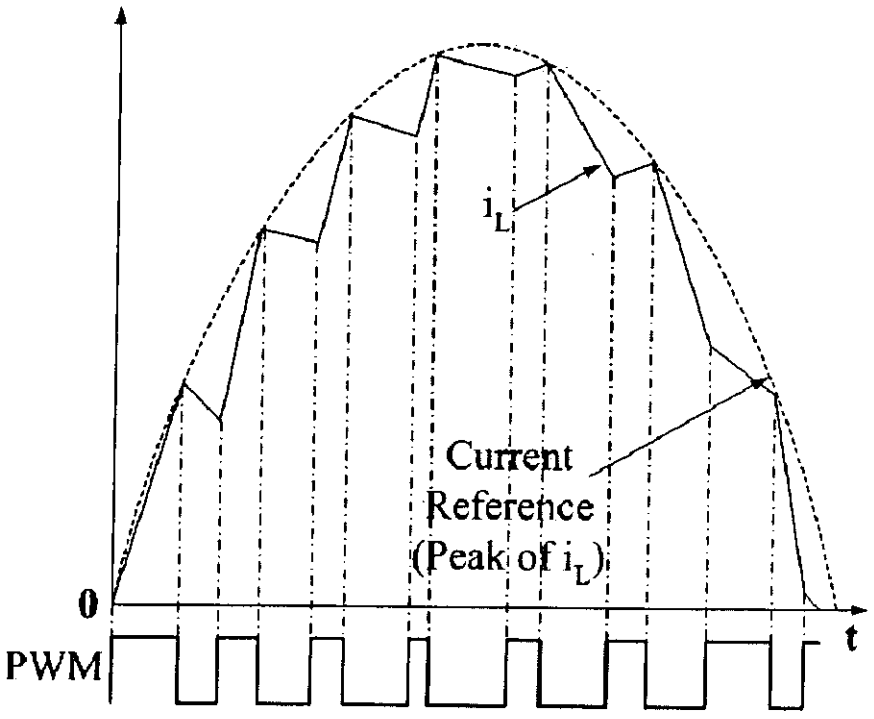


Fig. 2.21 Inductor current waveform for peak current mode control.

Inductor current waveform is shown in Fig. 2.21 and it can be seen that, peak inductor current, not the average inductor current, is controlled. In order to minimize the error between peak and average value of inductor current, the ripple component should be very small but this means the current ramp is shallow and this makes the control very noise sensitive.

C. Hysteretic Control

Both the average current mode control and peak current mode control are fixed frequency method. Another control technique, hysteretic control [47], will need to vary the switching frequency. Fig. 2.22 shows the block diagram of hysteretic control.

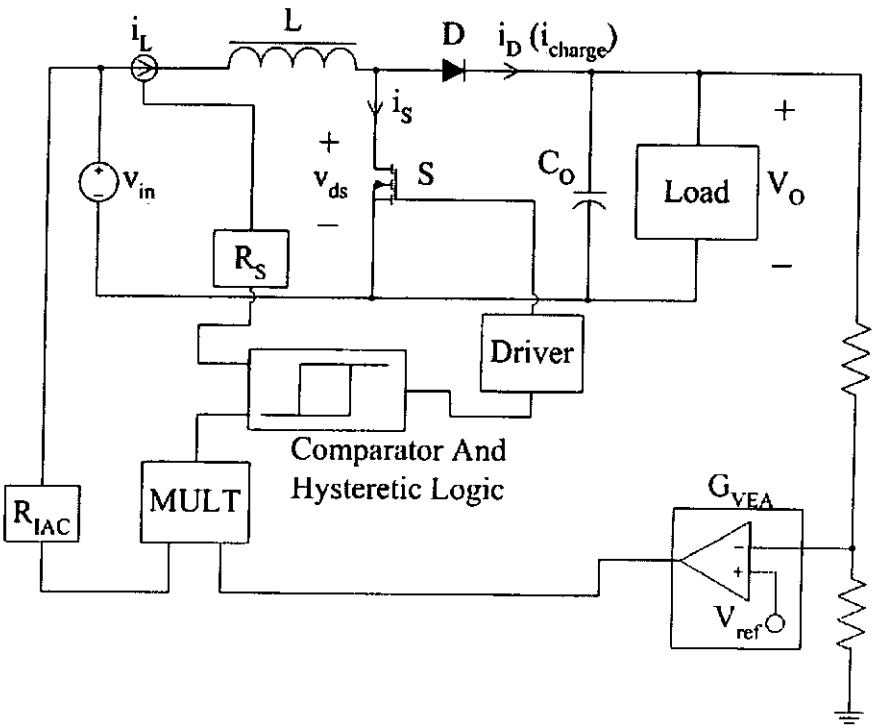


Fig. 2.22 Hysteretic control for a boost converter in CCM operation.

The output of the multiplier forms two current references: $i_{L,max}$ and $i_{L,min}$. These references track the sinusoidal line voltage waveform. The switch will be on until the inductor current reaches the peak current level $i_{L,max}$. Then the switch will be turned off and the inductor current changes to decrease. Once the inductor current is reduced to the valley current level $i_{L,min}$, the switch is turned on again. As a result, the inductor current will be limited between the upper and lower levels. The associated current hysteresis band can be a fixed amount or proportional to the instantaneous average current. Fig. 2.23 shows the inductor current waveform.

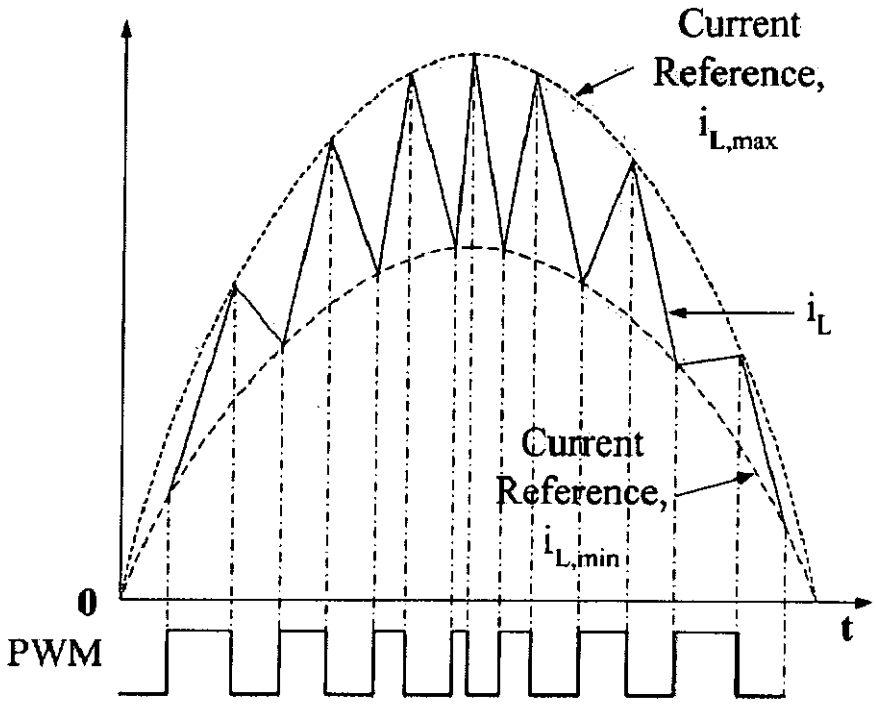


Fig. 2.23 Inductor current waveform for hysteretic control.

In this control technique, variable frequency is required to accommodate the hysteresis band. However, the switching frequency could

span several times over the whole load range. Moreover, it is not desirable in applications requiring synchronization.

2.4.2 CRM Operation

2.4.2.1 Introduction

In CRM operation, the inductor current operates on the border between CCM and DCM. The switch is turned on immediately after the inductor current has reached zero. Therefore, the inductor current starts and returns to zero each cycle and its waveform can be considered as a series of consecutive triangles, as shown in Fig. 2.24.

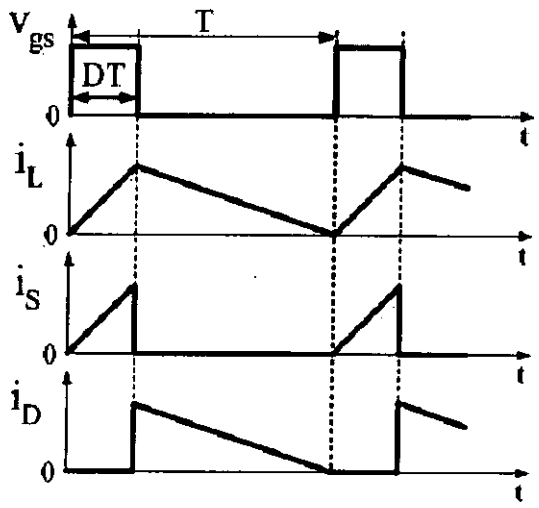


Fig. 2.24 Main waveforms for CRM operation.

From Fig. 2.24 it can be seen that the peak value of the inductor current is limited to exactly twice that of the average current. For the same average level, it will have a larger ripple current than that in CCM operation. Thus, it will have a higher conduction loss. However, the inductor L can be designed with smaller inductance and reduced size.

The expression of the duty cycle D of CRM boost converter is same with (2-9), which means that D will vary according to the line voltage. The expression of the average inductor current over a switching cycle can be found as

$$i_{L,avg} = \frac{v_{in}}{2L} \cdot DT \tag{2-10}$$

From equation (2-10) it can be seen that, in order to achieve high power factor, the on time should be "fixed" for one line half-cycle. Since D will vary according to the instant line voltage, switching frequency will need to change as well to keep the on time constant. Generally, the minimum switching frequency will coincide with full load operation during the peak of the input voltage. In contrast, the maximum frequency occurs at light load, when the input voltage nears the zero crossing point.

From Fig. 2.24 it can be found that, the inductor current must be zero before the next switching cycle. The boost rectifier reverse recovery loss will be eliminated and the efficiency of the converter can be improved. In practical circuits, a dead time is usually added before the switch is turned on. Such a dead time will help the switch to turn on under the condition of reduced voltage stress, which will further improve the efficiency. However, variable frequency operation with large ripple current will increase the filter requirements.

2.4.2.2 Control Methods

Control technique of CRM operation can be envisioned as hysteretic current control with the lower current level set at zero [48][49]. Fig. 2.25 shows the control block diagram.

This control diagram is similar to that of peak current mode control. But the switching frequency of peak current mode control is fixed and the turn-on of the switch is initiated by the controller IC during the beginning of each cycle. For CRM operation, the turn-on of the switch is initiated by the "zero current detect (ZD)". Once the inductor current has reached zero, the switch will be turned on. The switch will keep on until the peak value of the inductor current reaches the threshold set by the multiplier. Fig. 2.26 shows the current waveforms.

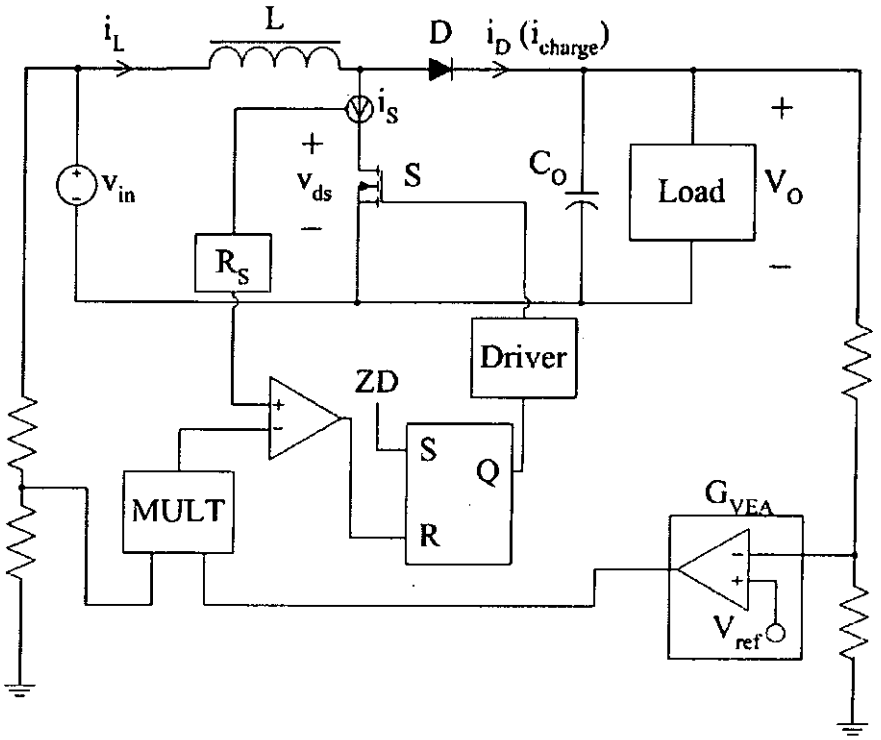


Fig. 2.25 Block diagram of CRM PFC control.

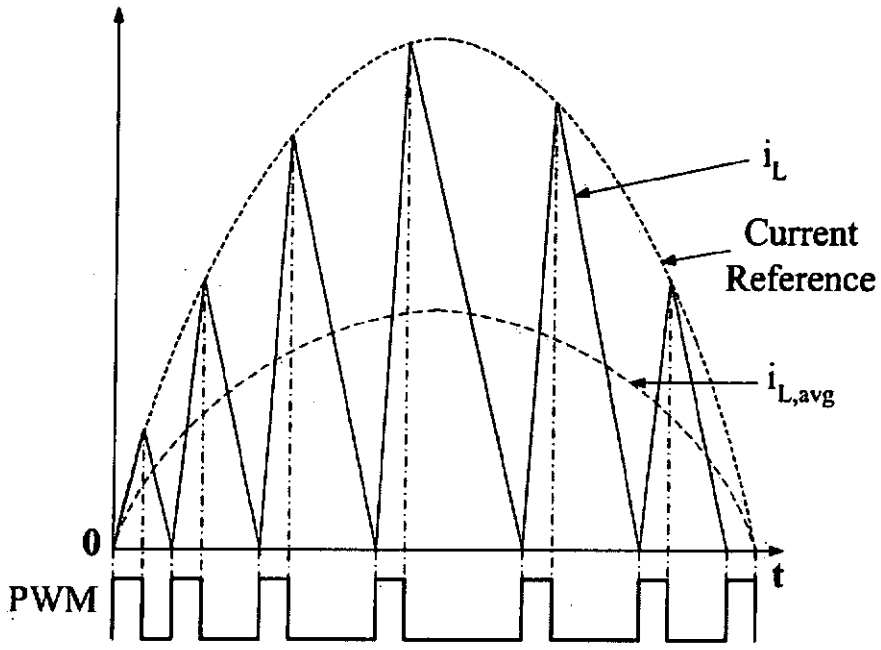


Fig. 2.26 Inductor current waveform for CRM PFC control.

Such CRM PFC control is very simple, and because the average inductor current is exactly half of the peak inductor current, the average value is controlled and high power factor (larger than 0.98) can be attained. This is different from the case in peak current mode control where only the peak value of the inductor current is programmed.

Equation (2-10) tells us that the control on CRM PFC is actually a controlled on-time technique. In fact, the controller can be designed in a much simpler manner [50]. Fig. 2.27 shows the simplified block diagram of UC3852.

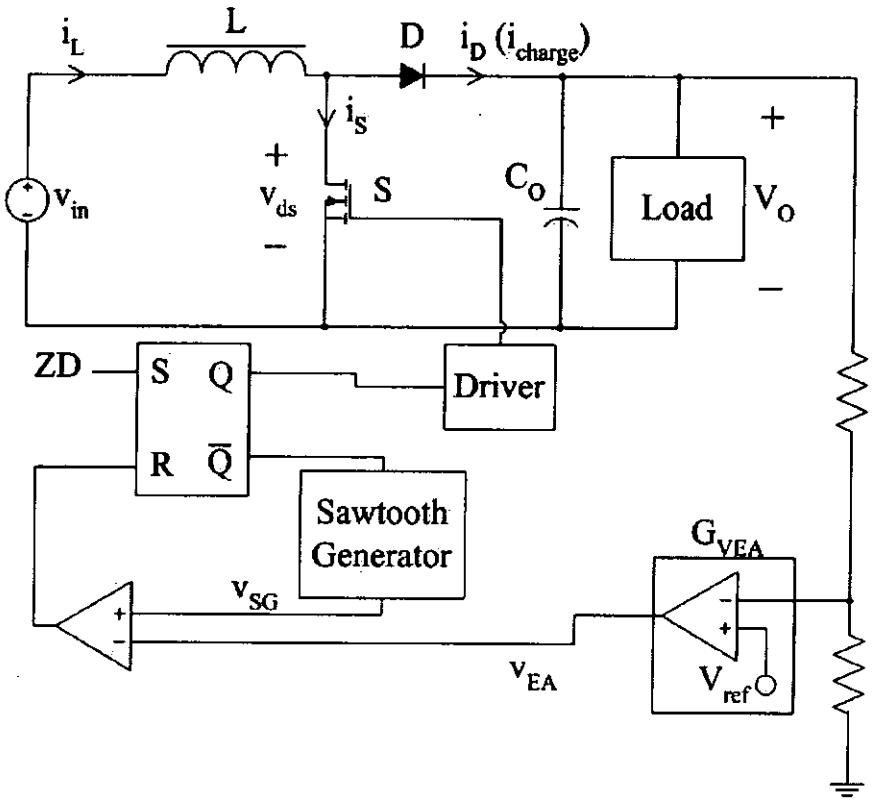


Fig. 2.27 Simplified block diagram of the controlled on-time technique.

No analog square, multiply, and divide functions are required to control the inductor current. The "fixed" on-time is determined by a voltage error amplifier which monitors the output voltage. When the switch is turned on, output voltage of the sawtooth generator v_{SG} rises at a constant rate. Once it reaches the voltage level of v_{EA}, the required on-time has been reached and the switch will be turned-off. At the same time, v_{SG} will be reset. The switch will remain off until the inductor current reaches zero, then the switch can be retriggered which initiates the subsequent cycles. Fig. 2.28 shows the main waveforms of the control circuit.

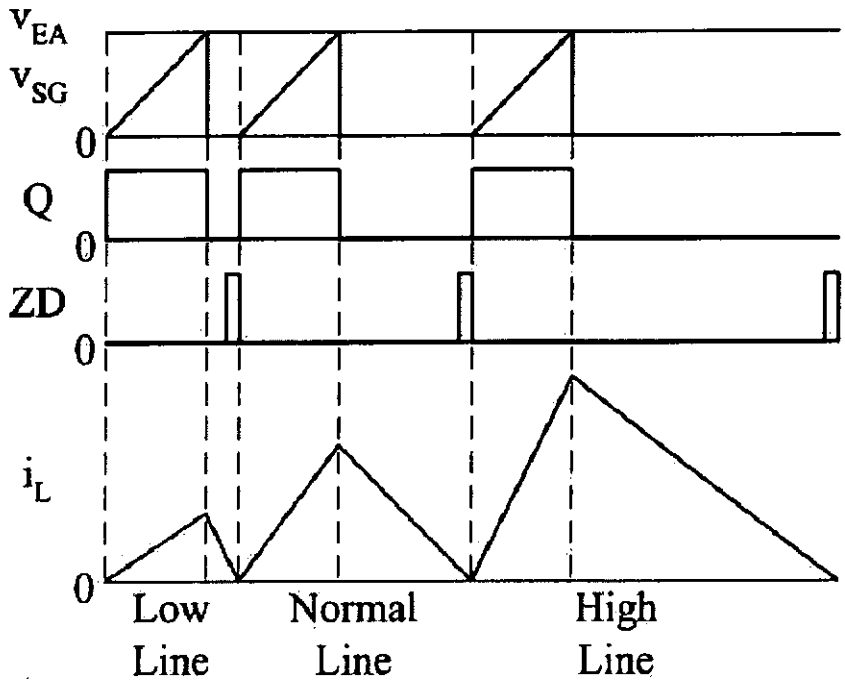


Fig. 2.28 Main waveforms of the control circuit.

2.4.3 DCM Operation

2.4.3.1 Introduction

In DCM operation, the inductor current is discontinuous. It will be reduced to zero before the end of the switching cycle and remain zero until the beginning of next cycle. Fig. 2.29 shows the waveforms.

Compared with CCM and CRM, DCM operation has the maximum ripple current for the same average current level. The peak value and the average value of the inductor current do not have a fixed relationship. High peak current will further increase the conduction loss so DCM operation is only suitable for low power applications.

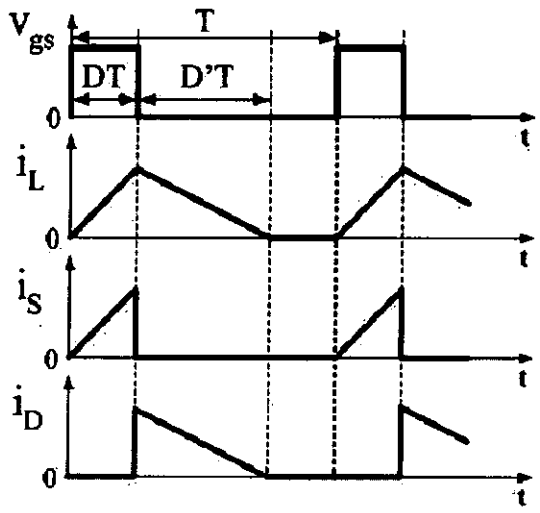


Fig. 2.29 Main waveforms for DCM operation.

From Fig. 2.29 the relationship between D and D' can be found as

$$v_{in} \cdot DT = (V_o - v_{in}) \cdot D'T$$
$$D = \frac{V_o - v_{in}}{v_{in}} \cdot D' \tag{2-11}$$

Utilizing (2-11), the expression of the average inductor current over a switching cycle is

$$i_{L,avg} = \frac{v_{in}}{L} \cdot DT \cdot (D + D')T \cdot \frac{1}{2T}$$
$$= \frac{v_{in}}{2L} \cdot D^2T \cdot \frac{V_o}{V_o - v_{in}} \tag{2-12}$$

For fixed frequency operation, duty cycle D should vary according to the change of the item $(\frac{V_o}{V_o - v_{in}})$ in order to achieve perfect PF.

2.4.3.2 Control Methods

When the boost converter operates in DCM, average current mode control still functions well to program the input current. High power factor

can be achieved because of the high gain of the current error amplifier. It should be noted that, even without active control on input current, relatively high power factor and low current distortion could still be achieved in DCM operation, although (2-12) shows that under such a condition perfect power factor can not be attained. From (2-12) it can be seen that, as long as the output voltage V_O is larger than the peak value of the line voltage in certain extent, harmonic content of the line current can meet the regulation requirement [51]. This is why the single-stage PFC circuits always use only one output voltage control loop and let the input current loop open. Fig. 2.30 shows the typical line voltage and line current waveforms when DCM boost converter operates without active control on input current.

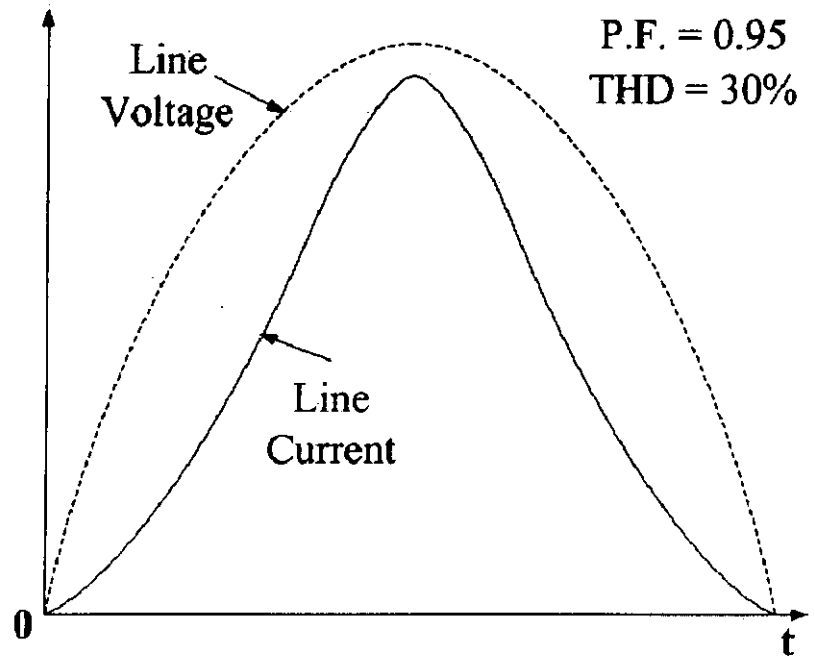


Fig. 2.30 Line voltage and current waveforms for DCM operation without active current control.

2.5 Summary

In this chapter, some basic concepts on the operation of active PFC circuits are introduced. Three basic topologies: boost, buck, and buck-boost are discussed briefly. They have been widely used as pre-regulators and, in fact, other active PFC circuits can be derived from these basic topologies. Sepic and Cuk topologies, which can be considered as the combinations of basic topologies, are discussed next. Single-stage PFC circuits, which have developed in recent years, are also introduced. Four typical converters are presented and each of them integrates an input-current waveform shaper and an isolated DC – DC converter.

Because the boost converter is the most popular topology used in active PFC applications, its three operation modes are explained in detail. Features of each operation mode and the corresponding control methods are given.

CHAPTER 3

DESIGN OF A SINGLE-SWITCH HIGH-POWER-FACTOR REGULATOR WITH NEAR-ZERO OUTPUT CURRENT RIPPLE

3.1 Introduction

PFC is becoming increasingly important because of the growing concern about the harmonic contents of the AC line currents of power supplies and the adoption of standards such as EN 61000-3-2. As discussed in Chapter 2, although adding a PFC pre-regulator [28], [52]-[55] to the switching power supply can achieve both high quality input-current waveform shaping and fast output voltage regulation, it is not the optimized design for low power applications. The main drawback is the high cost due to an increase in the device count. Therefore, in low power applications, single-stage active PFC circuits are preferred [36]-[45], [56]-[62].

The family of SSIPP was proposed in [43] and this family of power supplies has the features of fast regulation and single PWM control loop. It is believed that such supplies will find wide applications in low-cost low-power consumer products. However, the active switch in a SSIPP circuit often suffers large voltage spike during switching because of the unavoidable leakage inductance of the transformer. Such voltage spike can

increase the switching loss and lower the conversion efficiency. It can even damage the switch if the voltage rating of the switch is not high enough. At high switching frequency, the problem will become worse. A passive snubber circuit [57][58] may be used to reduce the voltage spike but the snubber itself will increase the loss of the circuit. Articles [59] and [60] utilized "regenerative clamping" to suppress the spike. As a result, not only the conversion efficiency, but also the PF of the circuit were improved. However, extra rectifiers were needed in regenerative clamping. Active clamping method was used in articles [61] and [62] and it was found that more than 3% improvement in conversion efficiency could be attained [61]. However, an extra active switch was needed and this increased the cost of the circuit.

In this chapter, an improved version of the SSIPP is proposed. The proposed circuit has the following features:

1) It has an improved power factor.
2) It achieves near-zero output current ripple in the regulator.
3) It uses an integrated transformer [20]-[27] to reduce the size and the number of magnetic components.
4) It solves the voltage spike problem due to the transformer leakage inductance with minimal components.

The basic circuit topology and the principle of operation of the proposed regulator will be explained first. Next, design considerations will be given. Simulation and experimental verification, based on the analysis in the former sections, will be reported finally.

3.2 Principle of Operation

In this section, the basic circuit topology and the principle of operation of the proposed regulator will be described.

3.2.1 Basic Circuit Topology

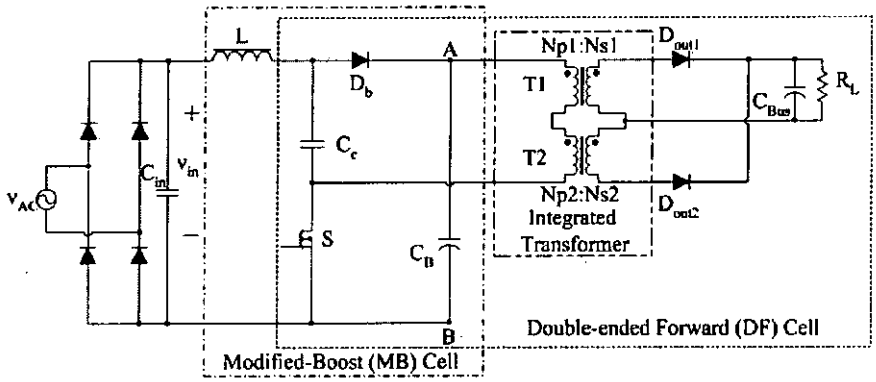
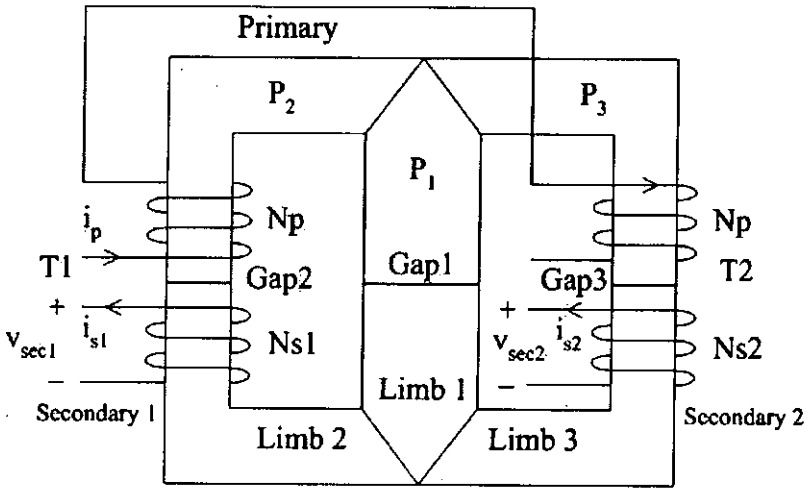


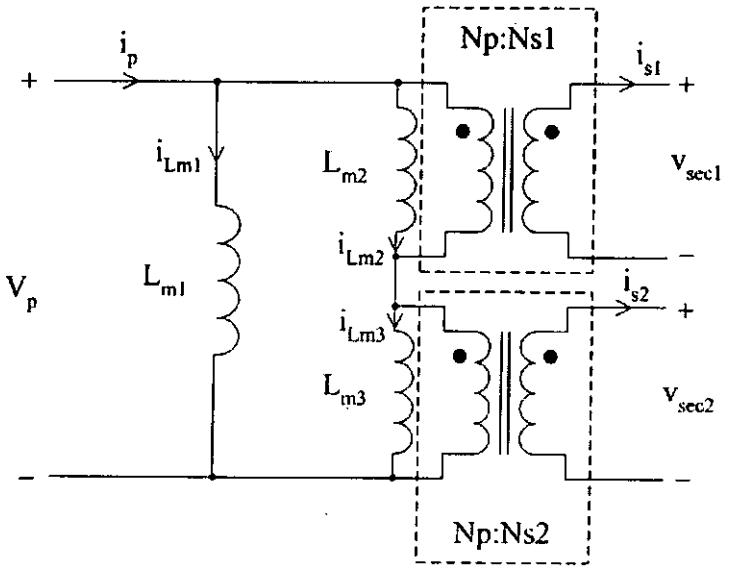
Fig. 3.1 The proposed regulator.

The proposed regulator is shown in Fig. 3.1. This circuit can be understood as a cascaded connection of a modified-boost (MB) converter followed by a double-ended forward (DF) converter [63]-[65], as identified by the dotted-line boxes. The input-current waveform shaper is called as *Modified-Boost* converter because it includes a clamping capacitor C_c in the conventional boost circuit. These two converters, which will be referred to as cells in this chapter, share the same switch S and bulk capacitor C_B. The MB cell is designed to operate in DCM, acting as an inherent power factor corrector. The DF cell is designed to function as a fast-response post-regulator. Nodes A and B serve as the output terminals of the MB cell and, at the same time, the input terminals of the DF cell. C_B is an energy-storage

capacitor and C_c is the clamping capacitor that performs the functions of clamping the switch voltage stress and recycling the energy trapped in the transformer leakage inductance. C_{Bus} is the output filter capacitor.



(a) Winding arrangement of integrated transformer (T1 and T2)



(b) Equivalent circuit

Fig. 3.2 Integrated transformer.

In the DF cell, an integrated transformer is used instead of two individual transformers, to reduce the number of magnetic components. The practical winding arrangement of the integrated transformer is shown in Fig. 3.2(a), where P_1 , P_2 , and P_3 are the magnetic permeances of the corresponding limbs of the transformer. Two secondary windings are wound on the two outer legs of the core. In order to minimize the leakage of the transformer, primary winding is divided into two parts. These two parts are also wound on two outer legs and connected by a single wire. Air gap is added in each limb to prevent saturation of the magnetic core. The equivalent circuit of the integrated transformer is shown in Fig. 3.2(b). The circuits inside the dotted-line boxes are ideal transformers and L_{m1} ($L_{m1} = N_p^2 \cdot P_1$), L_{m2} ($L_{m2} = N_p^2 \cdot P_2$), and L_{m3} ($L_{m3} = N_p^2 \cdot P_3$) are the magnetizing inductances. This equivalent circuit will be used to replace the two transformers in Fig. 3.1 to facilitate the analysis of the regulator.

3.2.2 Principle of Operation

In explaining the principle of operation of the proposed modified-boost double-ended forward (MBDF) regulator, the following assumptions are made:

- The MB input cell operates in DCM.
- The circuit has reached the steady-state operation.
- The primary inductance of the integrated transformer is large enough to keep the primary current i_p continuous (shown in Fig. 3.4).
- The filtering capacitors C_{Bus} and C_B in Fig. 3.1 are functionally constant voltage sources within a switching cycle.

- The clamping capacitor C_c has a reasonably large capacitance so that the ripple component of the voltage across it is small when compared with the DC component.

As shown in Fig. 3.3 (where the thick lines indicate the conducting paths) and with the aid of the switching waveforms shown in Fig. 3.4, the operation of the regulator consists of the following three stages:

1) Stage 1 (T0-T1)

a) At T0, S is turned on and diode D_{out2} is reversely biased.

b) The charge on C_c assists v_{in} to charge up L in a resonant manner. The initial resonance current is zero. Because of the relatively large capacitance of C_c, the current in L will increase nearly linearly.

$$v_{in} + V_{Cc} = L\frac{di_L(t)}{dt} \tag{3-1}$$

Solving (3-1), we have

$$i_L(t) = \frac{v_{in} + V_{Cc}}{L}(t - T0) \tag{3-2}$$

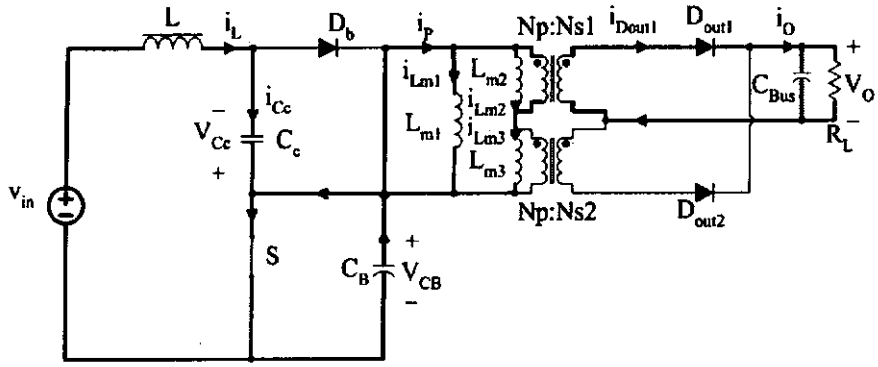
c) L_{m1}, L_{m2}, and L_{m3} are charged up by V_{CB}, NV_O, and $(V_{CB} - NV_O)$ respectively, producing an output current of $i_O = N(i_{Lm3} - i_{Lm2})$.

$$V_{CB} = L_{m1}\frac{di_{Lm1}(t)}{dt} \tag{3-3}$$

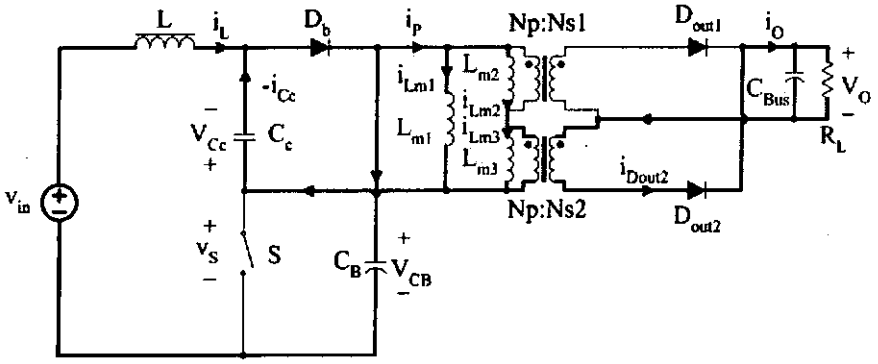
$$NV_O = L_{m2}\frac{di_{Lm2}(t)}{dt} \tag{3-4}$$

$$V_{CB} - NV_O = L_{m3}\frac{di_{Lm3}(t)}{dt} \tag{3-5}$$

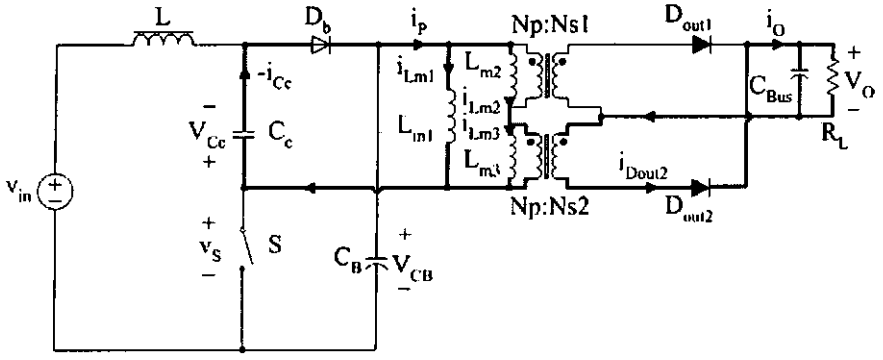
where the turn ratio $N = \frac{Np}{Ns1} = \frac{Np}{Ns2}$.



(a)



(b)



(c)

Fig. 3.3 Three stages of the converter: (a) Stage 1 (T0-T1); (b) Stage 2 (T1-T2); (c) Stage 3 (T2-T3).

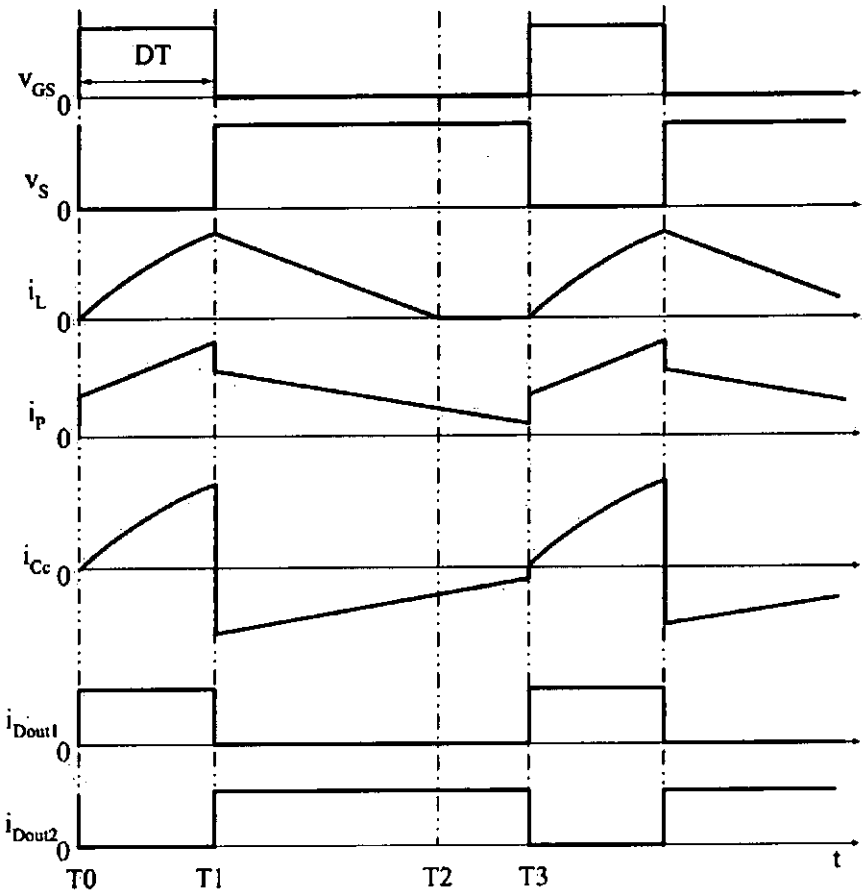


Fig. 3.4 Key voltage and current waveforms.

d) The primary current $i_P = i_{Lm1} + i_{Lm3}$

$$\frac{di_P}{dt} = \frac{d(i_{Lm1} + i_{Lm3})}{dt} = \frac{V_{CB}}{L_{m1}} + \frac{V_{CB} - NV_O}{L_{m3}} \quad (3\text{-}6)$$

2) Stage 2 (T1-T2)

a) At T1, S is turned off and diode D_{out1} is reversely biased.

b) v_S is clamped at ($V_{CB} + V_{Cc}$).

c) i_L is diverted to charge up C_B.

$$V_{CB} - v_{in} = -L\frac{di_L(t)}{dt} \tag{3-7}$$

Combining (3-2) with (3-7) we have

$$\begin{aligned} i_L &= \frac{v_{in} + V_{Cc}}{L} \cdot (T1 - T0) - \frac{V_{CB} - v_{in}}{L}(t - T1) \\ &= \frac{v_{in} + V_{Cc}}{L} \cdot DT - \frac{V_{CB} - v_{in}}{L}(t - T1) \end{aligned} \tag{3-8}$$

where D is the duty cycle and T is the switching period.

d) Due to the leakage and primary inductances of the transformer, i_P will continue to charge up C_c. L_{m1}, L_{m2}, and L_{m3} are discharged by V_{Cc}, $(V_{Cc} - NV_O)$, and NV_O respectively, producing an output current of $i_O = N \cdot (i_{Lm3} - i_{Lm2})$ through diode D_{out2}.

$$V_{Cc} = -L_{m1}\frac{di_{Lm1}(t)}{dt} \tag{3-9}$$

$$V_{Cc} - NV_O = -L_{m2}\frac{di_{Lm2}(t)}{dt} \tag{3-10}$$

$$NV_O = -L_{m3}\frac{di_{Lm3}(t)}{dt} \tag{3-11}$$

e) The primary current $i_P = i_{Lm1} + i_{Lm2}$

$$\begin{aligned} \frac{di_P}{dt} &= \frac{d(i_{Lm1} + i_{Lm2})}{dt} \\ &= -\left(\frac{V_{Cc}}{L_{m1}} + \frac{V_{Cc} - NV_O}{L_{m2}}\right) \end{aligned} \tag{3-12}$$

3) Stage 3 (T2-T3)

a) At T2, the current in inductor L falls to zero.

$$i_L(T2) = 0 \tag{3-13}$$

Substituting (3-8) into (3-13), we have

$$\begin{aligned} T2 &= T1 + \frac{v_{in} + V_{Cc}}{V_{CB} - v_{in}} \cdot DT \\ &= \frac{V_{CB} + V_{Cc}}{V_{CB} - v_{in}} \cdot DT + T0 \end{aligned} \tag{3-14}$$

(Note that T1 = T0 + DT.)

b) L_{m1}, L_{m2}, and L_{m3} continue to be discharged and i_O continues to flow through diode D_{out2}.

c) v_S continues to be clamped at $(V_{CB} + V_{Cc})$.

Once the switch S is turned on at T3, the switching operations described above will start again. Although the principle of operation of the proposed regulator is quite simple, it is very effective in reducing the voltage stress of switch S, recycling the trapped energy, and achieving near-zero output current ripple.

3.3 Design Considerations

The determination of V_{CB}, the design of inductor and integrated transformer, and the selection of clamping capacitor C_c will be described in this section.

When the circuit has reached the steady-state operation, according to the volt-second balance on inductors L_{m1}, L_{m2}, and L_{m3}, we have

$$\begin{cases} i_{Lm1}(T0) = i_{Lm1}(T3) \\ i_{Lm2}(T0) = i_{Lm2}(T3) \\ i_{Lm3}(T0) = i_{Lm3}(T3) \end{cases} \tag{3-15}$$

The input voltage to the MB cell is given by

$$v_{in}(t) = V_{in,pk} \cdot |\sin(\omega t)| \tag{3-16}$$

3.3.1 Determination of V_{CB}

Substituting (3-3) – (3-5) and (3-9) – (3-11) into (3-15), we have:

$$\begin{cases} \dfrac{V_{CB}}{V_{Cc}} = \dfrac{1-D}{D} \\ V_{Cc} = \dfrac{NV_O}{1-D} \\ V_{CB} = \dfrac{NV_O}{D} \end{cases} \tag{3-17}$$

Equations (3-17) give the steady-state relationships among V_{CB}, V_{Cc}, and V_O. They are the same as the counterparts of a single double-ended forward converter.

To ensure the MB cell operates in DCM, we must have

$$\max(T2 - T0) \le T \tag{3-18}$$

Substituting (3-14) into (3-18), the following expression can be obtained

$$\max\left(\frac{V_{CB} + V_{Cc}}{V_{CB} - v_{in}} \cdot DT\right) \le T \tag{3-19}$$

We define the output-input voltage gain K as

$$K = \frac{NV_O}{V_{in,pk}} \tag{3-20}$$

Substituting (3-16), (3-17), and (3-20) into (3-19), we have

$$D \le K + \frac{1}{2} - \sqrt{K^2 + \frac{1}{4}} \tag{3-21}$$

The relationship between duty cycle D and K is given in Fig. 3.5. It is clear that, in order to keep the MB cell operating in DCM, the boundary values of D become larger as K increases. When K varies from zero to one, the boundary value of D is always less than 0.4.

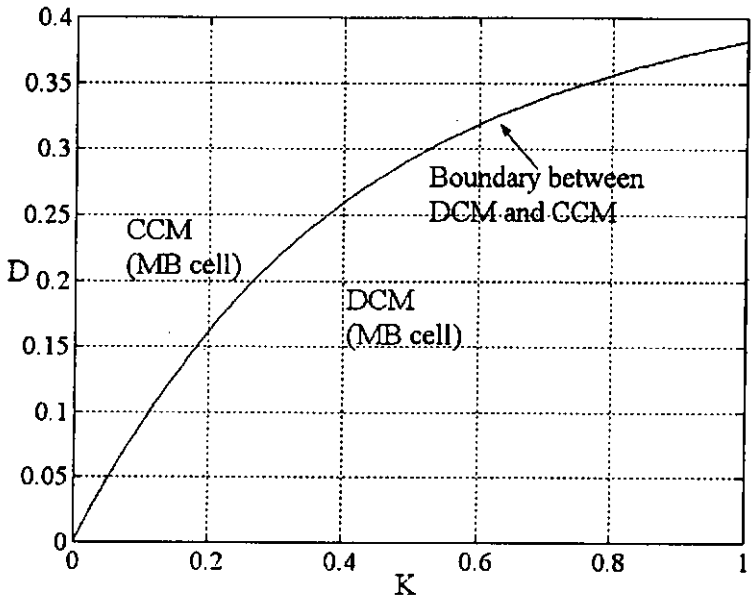


Fig. 3.5 Duty cycle D as a function of K ($=\frac{NV_O}{V_{in,pk}}$).

From (3-2), (3-8), and (3-14), the averaged MB input current (averaged over a switching period T) is found as:

$$i_{L,avg} = \frac{V_{CB} + V_{Cc}}{2L} \cdot D^2T \cdot \frac{v_{in} + V_{Cc}}{V_{CB} - v_{in}} \tag{3-22}$$

The input power P_{in} and the output power P_{out} can be expressed as

$$\begin{aligned} P_{in} &= \frac{\omega}{\pi}\int_0^{\pi/\omega} v_{in}(t)\cdot i_{L,avg}dt \\ &= \frac{V_{in,pk}}{2\pi L}(V_{CB}+V_{Cc})D^2T\cdot\int_0^{\pi}\sin(\omega t)\cdot\frac{V_{in,pk}\sin\omega t + V_{Cc}}{V_{CB}-V_{in,pk}\sin\omega t}d(\omega t) \end{aligned} \tag{3-23}$$

$$P_{out} = V_O \cdot I_O = \frac{V_O^2}{R_L} = P_{in}\cdot\eta \tag{3-24}$$

where R_L is the load resistance and η is the conversion efficiency.

Substituting (3-23) into (3-24) and combining (3-17) and (3-20), we have

$$\frac{\eta \cdot N^2 TR_L}{2\pi L(V_{CB}/V_{in,pk} - K)} \cdot \left[\int_0^{\pi} \sin(\omega t) \cdot \frac{(V_{CB}/V_{in,pk}) \cdot K/(V_{CB}/V_{in,pk} - K) + \sin(\omega t)}{V_{CB}/V_{in,pk} - \sin(\omega t)} d(\omega t) \right] = 1 \quad (3\text{-}25)$$

Defining $\alpha = \frac{2\pi L}{N^2 TR_L}$, we then have

$$\frac{\eta}{\alpha \cdot (V_{CB}/V_{in,pk} - K)} \cdot \left[\int_0^{\pi} \sin(\omega t) \cdot \frac{(V_{CB}/V_{in,pk}) \cdot K/(V_{CB}/V_{in,pk} - K) + \sin(\omega t)}{V_{CB}/V_{in,pk} - \sin(\omega t)} d(\omega t) \right] = 1 \quad (3\text{-}26)$$

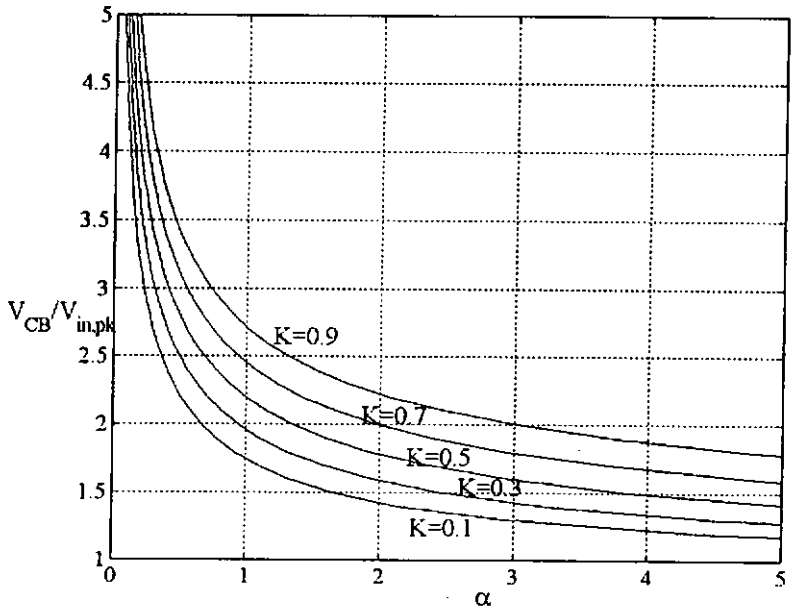


Fig. 3.6 ($V_{CB}/V_{in,pk}$) as a function of α for different values of K ($= \frac{NV_O}{V_{in,pk}}$).

From (3-26), it can be seen that the voltage conversion ratio ($V_{CB}/V_{in,pk}$) is load dependent. Fig. 3.6 shows the relationship between ($V_{CB}/V_{in,pk}$) and α under different K, assuming $\eta = 0.8$. For a given value of α, a larger K gives a larger voltage conversion ratio ($V_{CB}/V_{in,pk}$). If K is given, a larger α gives a lower voltage conversion ratio (and therefore a lower V_{CB}). However, as α decreases, which is corresponding to the decrease of the loading current, ($V_{CB}/V_{in,pk}$) will become larger and larger. This is similar to that of a conventional SSIPP employing a DC – DC cell in CCM operation.

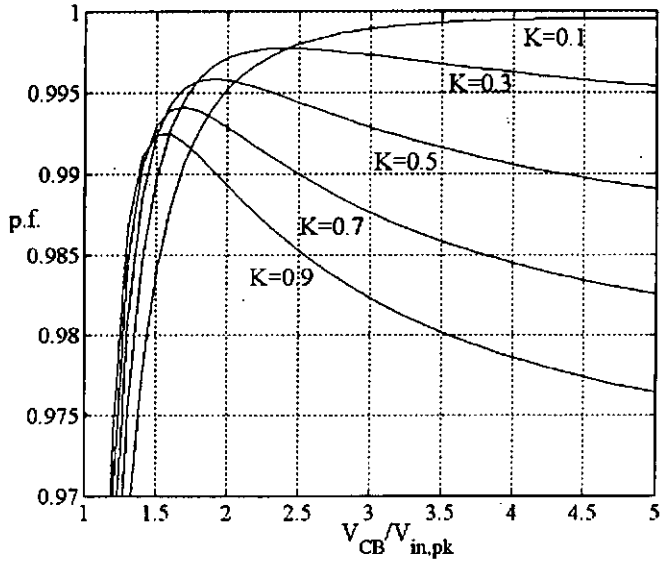
It should be understood that the graphs shown in Fig. 3.6 are based on the assumption of continuous primary current of integrated transformer. The condition for such an assumption will be discussed later.

From (3-16) and (3-22), the RMS value of input current $I_{L,rms}$ is given by

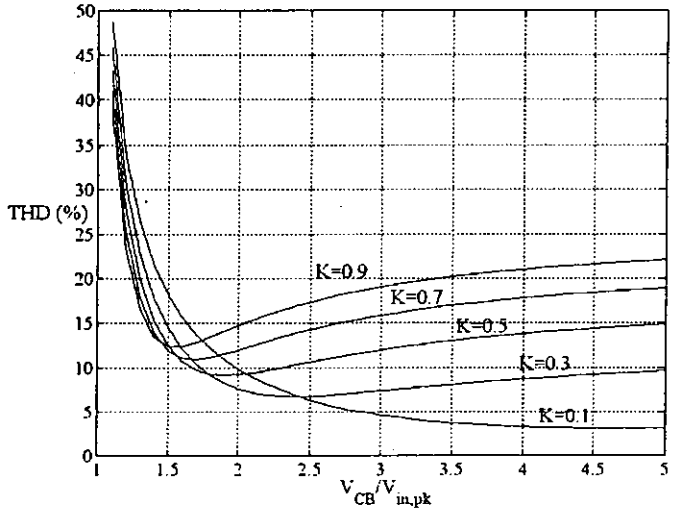
$$I_{L,rms} = \sqrt{\frac{\omega}{\pi}\cdot\int_0^{\pi/\omega} i_{L,avg}^2 dt} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left[\frac{V_{CB}+V_{Cc}}{2L}\cdot D^2T\cdot\frac{V_{Cc}+V_{in,pk}\cdot\sin(\omega t)}{V_{CB}-V_{in,pk}\cdot\sin(\omega t)}\right]^2\cdot d(\omega t)} \quad (3\text{-}27)$$

Based on (3-16), (3-23), and (3-27), expressions of power factor and THD can be found. Fig. 3.7(a) is a set of graphs showing the relationship between ($V_{CB}/V_{in,pk}$) and the power factor of the system for different K. Fig. 3.7(b) is a set of graphs showing the relationship between ($V_{CB}/V_{in,pk}$) and the THD of line current for different K. It can be seen that, for example, for

K = 0.5, a high PF ($PF > 0.99$) and a low THD ($THD < 15\%$) can be achieved when ($V_{CB} / V_{in,pk}$) is between 1.5 and 2.0.



(a)



(b)

Fig. 3.7 Power factor (a) and THD (b) as functions of ($V_{CB} / V_{in,pk}$) for different values of K ($= \frac{NV_O}{V_{in,pk}}$).

3.3.2 Design of Inductor L

It is critical to select a proper inductor L to ensure that the MB cell operates in DCM. From (3-21) we can find the critical duty cycle at the boundary point between CCM and DCM.

$$D_{critical} = K + \frac{1}{2} - \sqrt{K^2 + \frac{1}{4}} \tag{3-28}$$

From (3-17), (3-20), and (3-28), we have

$$\frac{V_{CB}}{V_{in,pk}} = \frac{K}{D_{critical}} = \frac{K}{K + \frac{1}{2} - \sqrt{K^2 + \frac{1}{4}}} \tag{3-29}$$

Substituting (3-29) into (3-26) gives

$$\alpha_{critical} = \frac{\eta}{\left(\frac{K}{K + \frac{1}{2} - \sqrt{K^2 + \frac{1}{4}}} - K\right)} \cdot \left[\int_0^{\pi} \sin(\omega t) \cdot \frac{\frac{K}{\frac{1}{2} - K + \sqrt{K^2 + \frac{1}{4}}} + \sin(\omega t)}{\frac{K}{K + \frac{1}{2} - \sqrt{K^2 + \frac{1}{4}}} - \sin(\omega t)} d(\omega t)\right] \tag{3-30}$$

Discontinuous conduction operation is assured by choosing $\alpha \le \alpha_{critical}$ in the DCM MB cell, as shown in Fig. 3.8. Then inductance L should be chosen as

$$L \le \alpha_{critical} \cdot \frac{N^2 T R_{L,min}}{2\pi} \tag{3-31}$$

where $R_{L,min}$ refers to the minimum load resistance.

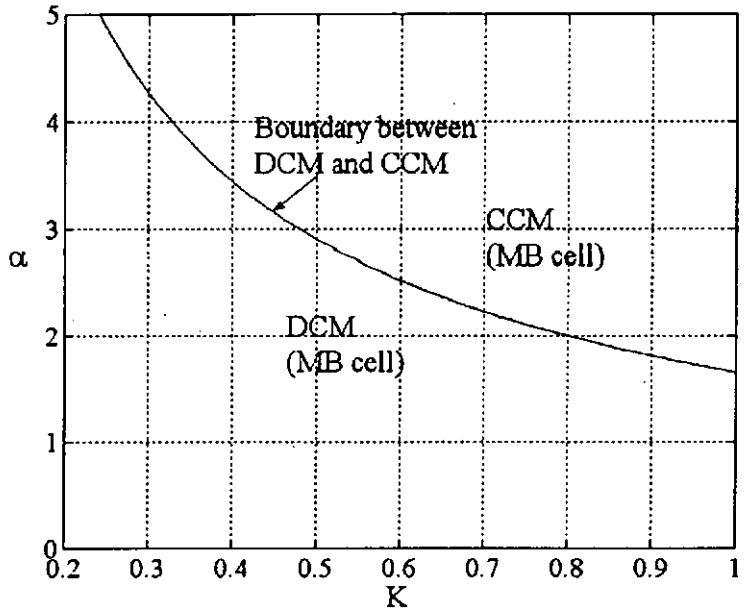


Fig. 3.8 α as a function of K ($= \frac{NV_o}{V_{in,pk}}$).

3.3.3 Design of Integrated Transformer

In order to achieve zero output current ripples, we should have

$$\frac{di_o}{dt} = \frac{d(i_{Lm3} - i_{Lm2})}{dt} = 0 \tag{3-32}$$

From (3-3) – (3-5), (3-9) – (3-11), and (3-32), we have

$$\frac{V_{CB} - NV_o}{L_{m3}} - \frac{NV_o}{L_{m2}} = 0 \tag{3-33}$$

$$(-\frac{NV_o}{L_{m3}}) - (-\frac{V_{Cc} - NV_o}{L_{m2}}) = 0 \tag{3-34}$$

Substituting (3-17) into (3-33) and (3-34), we have

$$\frac{L_{m2}}{L_{m3}} = \frac{D}{1 - D} \tag{3-35}$$

Equation (3-35) is the condition for zero output current ripples. Since the duty cycle D will change according to loading current, the condition of (3-35) should be met at full load.

In the design of the circuit, a sufficiently large primary inductance of the integrated transformer should be used to keep the primary current continuous. This condition is necessary in order to minimize the output current ripple. The condition can be found from the energy balance of the bulky capacitor C_B. As described in the principle of operation, the bulky capacitor C_B is discharged by the primary current in **Stage 1**, and charged by the inductor current in **Stage 2**. Assume that the primary current operates at the boundary between continuous and discontinuous conditions. Since the energy should be balanced over a line cycle, from (3-17), (3-20), Fig. 3.4, and Fig. 3.9, we can find that

$$\frac{1}{\pi}\int_0^{\pi}\frac{1}{2}\cdot\frac{V_{CB}-V_{in,pk}\sin(wt)}{L}\cdot\left[\frac{V_{Cc}+V_{in,pk}\sin(wt)}{V_{CB}-V_{in,pk}\sin(wt)}\cdot DT\right]^2 d(wt) = \frac{I_{O,boundary}}{N}\cdot DT+\frac{(DT)^2}{2}\cdot\left(\frac{V_{CB}}{L_{m1}}+\frac{NV_O}{L_{m2}}\right) \quad (3\text{-}36)$$

$$\int_0^{\pi}\frac{\left[\frac{K}{1-D}+\sin(wt)\right]^2}{\frac{K}{D}-\sin(wt)}d(wt)=\alpha_{boundary}\cdot\frac{K}{D}+\pi K\left(\frac{L}{DL_{m1}}+\frac{L}{L_{m2}}\right) \quad (3\text{-}37)$$

where $\alpha_{boundary}=\frac{2\pi L\cdot I_{O,boundary}}{N^2TV_O}=\frac{2\pi L}{N^2TR_{L,boundary}}$.

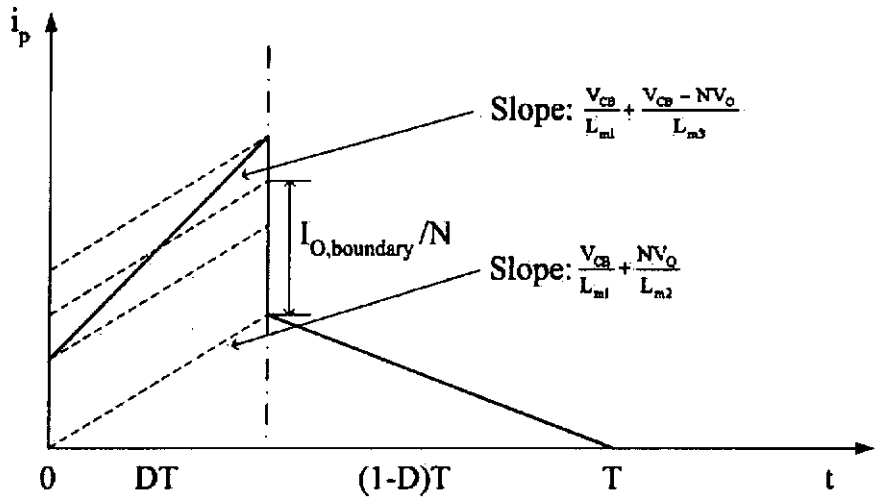
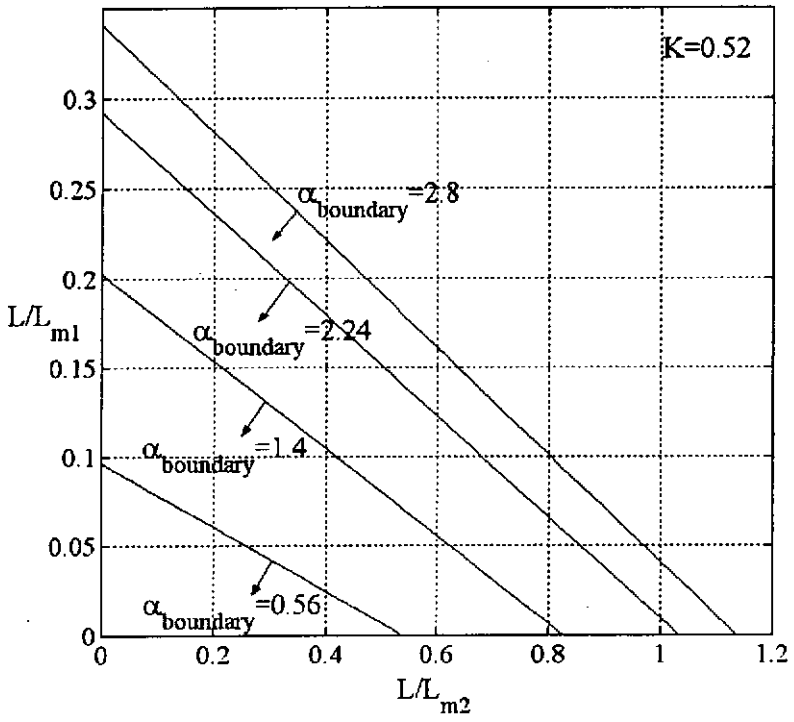


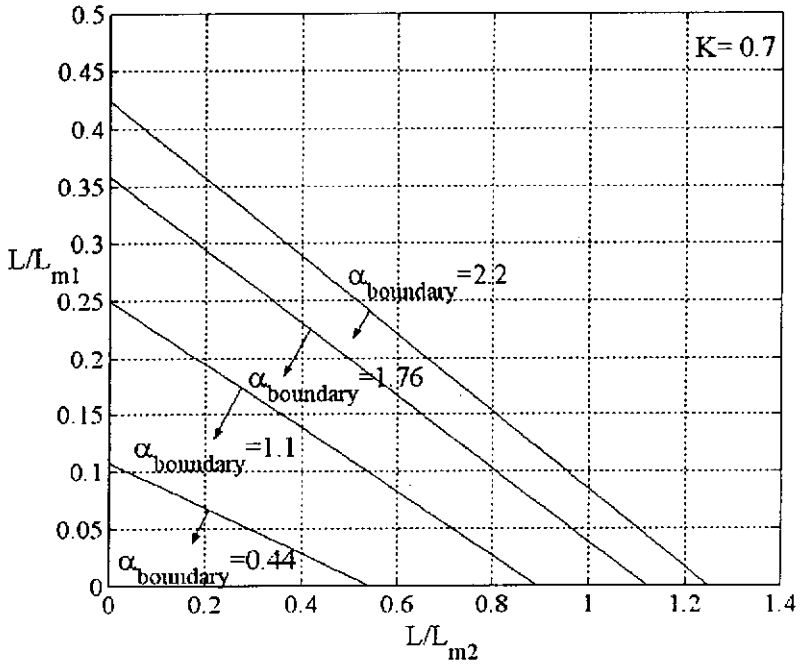
Fig. 3.9 i_p in one switching cycle (at the boundary between continuous and discontinuous modes).

When $\alpha \geq \alpha_{boundary}$, the primary current will be continuous. Otherwise, if α is too small (that is, when the load resistance R_L is sufficiently large), the primary current will become discontinuous. Equation (3-37) can therefore be used to find the condition to keep the primary current continuous.

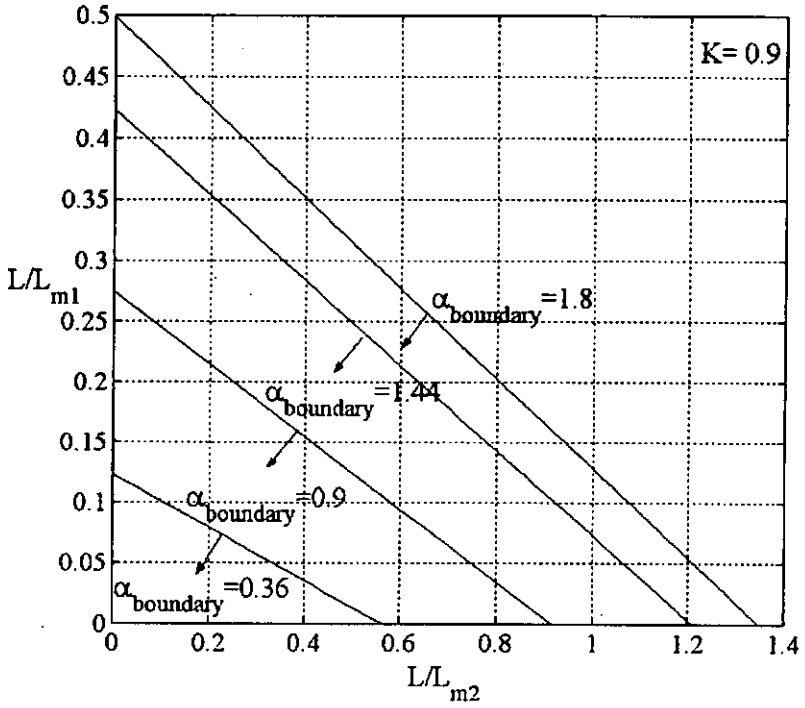
From (3-37), it is interesting to note that, in order to determine L_{m1} and L_{m2}, inductor L should be determined first. Combining with (3-26), equation (3-37) can be used to generate curves to facilitate the design of the integrated transformer (shown in Fig. 3.10 (a), (b), and (c)).


K=0.52
$\alpha_{boundary}$=2.8
$\alpha_{boundary}$=2.24
$\alpha_{boundary}$=1.4
$\alpha_{boundary}$=0.56
L/L$_{m1}$
L/L$_{m2}$
0
0.05
0.1
0.15
0.2
0.25
0.3
0.2
0.4
0.6
0.8
1
1.2

(a)


K= 0.7
$\alpha_{boundary}$=2.2
$\alpha_{boundary}$=1.76
$\alpha_{boundary}$=1.1
$\alpha_{boundary}$=0.44
L/L$_{m1}$
L/L$_{m2}$
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5
0.2
0.4
0.6
0.8
1
1.2
1.4

(b)



(c)

Fig. 3.10 Integrated transformer design guidelines for different values of K ($=\frac{NV_o}{V_{in,pk}}$): (a) K=0.52; (b) K=0.7; (c) K=0.9.

We shall illustrate the design procedure of the integrated transformer with a simplified example. Suppose the converter is to be operated from an 110 V_{rms} AC main. The output voltage is DC 28 V and the maximum output power is 100 W. We can find $K = 0.52$ by assuming the turn ratio $N = 2.9$. From Fig. 3.5 and Fig. 3.8, D is found to be about 0.3 and α is found to be about 2.8.

Assuming that the switch frequency is 200 kHz, the value of L can be found as

$$L = \frac{N^2 TR_{L,min}}{2\pi} \cdot \alpha = 147 \text{ uH}$$

L was finalized as 134 uH.

Suppose that (3-37) will be met at $\alpha_{boundary} = 1.4$ (about 50% load). In Fig. 3.10(a), all the points in the region labeled "$\alpha_{boundary} = 1.4$" will meet the requirement. We can choose a point where L/L_{m1} is about 0.1 and L/L_{m2} is about 0.42, resulting in the boundary operation in the DF cell at 50% load. Therefore, L_{m1} and L_{m2} are determined as 1340 uH and 319 uH, respectively. From (3-35), L_{m3} can be found as 744 uH. The number of primary winding Np is determined as

$$Np = \frac{NV_O \cdot (1-D)T}{\Delta B \cdot A_3} \tag{3-38}$$

where ΔB denotes the flux excursion and A_3 represents the cross-sectional area of limb 3. By choosing ΔB = 0.15 T and using magnetic core ETD44 with A_3 = 0.88 cm^2, Np is determined as $Np \geq 21.5$. From this result, the number of primary and secondary windings were selected as Np = 29 Turns and Ns1 = Ns2 = 10 Turns.

The magnetic permeances of the three limbs of the magnetic core P_1, P_2, and P_3 ($P = \frac{1}{S} = \frac{\mu_0 \mu_r A}{l_e}$, where S, A, and l_e are reluctance, cross-sectional area and path length, respectively) are

$$P_1 = \frac{\mu_0 \mu_r A_1}{\mu_r \cdot l_{e,G1} + l_{e,c1}} \tag{3-39}$$

$$P_2 = \frac{\mu_0 \mu_r A_2}{\mu_r \cdot l_{e,G2} + l_{e,c2}} \tag{3-40}$$

$$P_3 = \frac{\mu_0 \mu_r A_3}{\mu_r \cdot l_{e,G3} + l_{e,c3}} \tag{3-41}$$

where $l_{e,Gj}$ (j = 1, 2, 3) is the length of air gap.

It should be noted that air gaps $l_{e,G1}$, $l_{e,G2}$, and $l_{e,G3}$ are necessary due to the DC magnetizing current. From (3-39) – (3-41), $l_{e,G1}$, $l_{e,G2}$, and $l_{e,G3}$ can be determined as 0.1mm, 0.28mm, and 0.1mm, respectively.

The primary current is designed to enter into continuous conduction at 50% load. If the loading current is less than this level, primary current will become discontinuous. Although the output current will be discontinuous under this situation, such design is helpful to prevent any further increase of the voltage across the bulk capacitor C_B due to the decrease of the load, as shown in Fig. 3.6.

3.3.4 Selection of Clamping Capacitor C_c

It should be noted that C_c and L form a resonant circuit in **Stage 1** while C_c, L_{m1}, and L_{m2} form a resonant circuit in **Stage 2** and **Stage 3**. The resonant frequency in these stages should be sufficiently low.

$$\begin{cases} \pi\sqrt{L \cdot C_c} >> DT \\ \pi\sqrt{\dfrac{L_{m1} \cdot L_{m2} \cdot C_c}{L_{m1} + L_{m2}}} >> (1-D)T \end{cases} \tag{3-42}$$

The first condition implies that the half resonant period formed by L and C_c should be much longer than the on time of the switch S. The second condition implies that the half resonant period formed by L_{m1}, L_{m2}, and C_c should be much longer than the off time of the switch S. The conditions in (3-42) ensure a low voltage ripple across the clamping capacitor C_c.

3.4 Simulations and Experimental Results

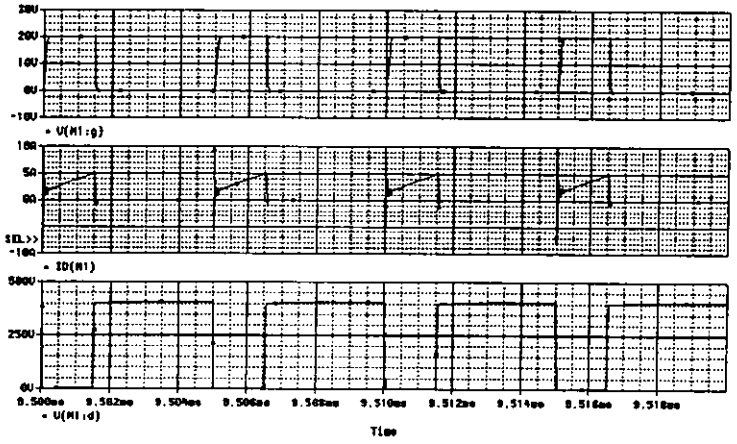
Based on the design rules developed above, the proposed regulator was designed to have the following parameters:

1) Input Voltage: v_{AC} = 110 V_{rms};
2) Output Voltage: V_O = 28 V;
3) Output Power: P_{out} =100 W;
4) Switching Frequency: f_s = 200 kHz;
5) L = 134 uH;
6) Diode D_b: MUR 860;
7) Diodes D_{out1} and D_{out2}: MBR 20200;
8) C_c = 0.22 uF;
9) C_B = 220 uF;
10) C_{Bus} = 1000 uF;
11) Switch S: NTP 8N50;
12) Integrated transformer:

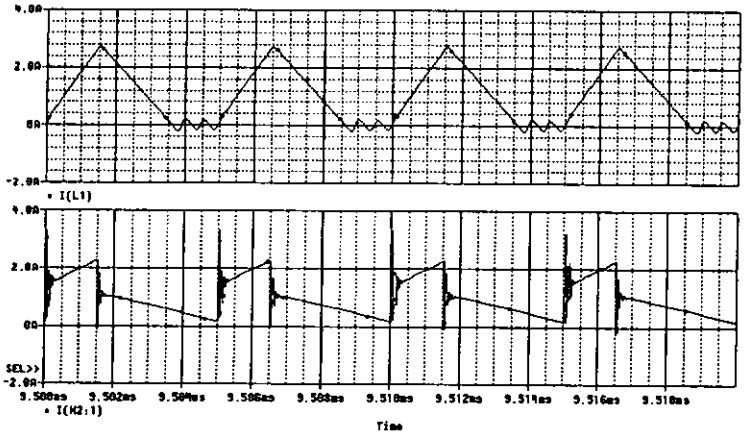
    Core: ETD44; Initial permeability μ_r: 2300; Saturation flux density B_{sat}: 500 mT; Primary: 29 turns of #38 AWG ×96; Secondary: 10 turns of #38 AWG× 160; Gap in limb 1: 0.10 mm; Gap in limb 2: 0.28 mm; Gap in limb 3: 0.10 mm

3.4.1 Simulation Results

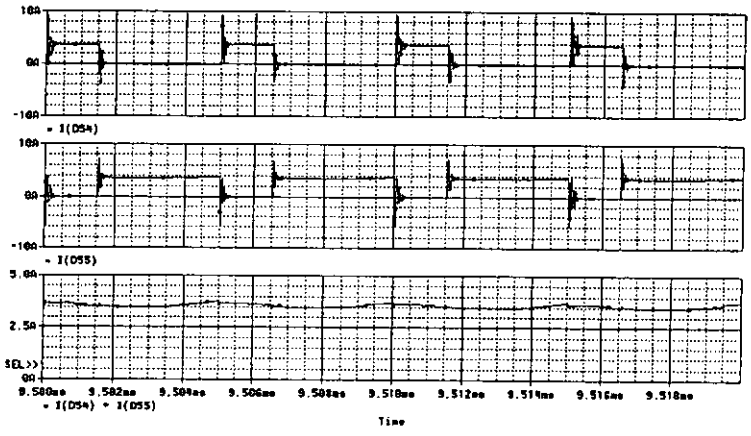
Fig. 3.11(a), (b), and (c) show the waveforms of the proposed regulator with an input DC voltage of 110 V.



(a) Top trace: v_{GS} ; Middle trace: i_S ; Bottom trace: v_S



(b) Top trace: i_L ; Bottom trace: i_p



(c) Top trace: i_{Dout1} ; Middle trace: i_{Dout2} ; Bottom trace: $(i_{Dout1} + i_{Dout2})$

Fig. 3.11 Simulation waveforms.

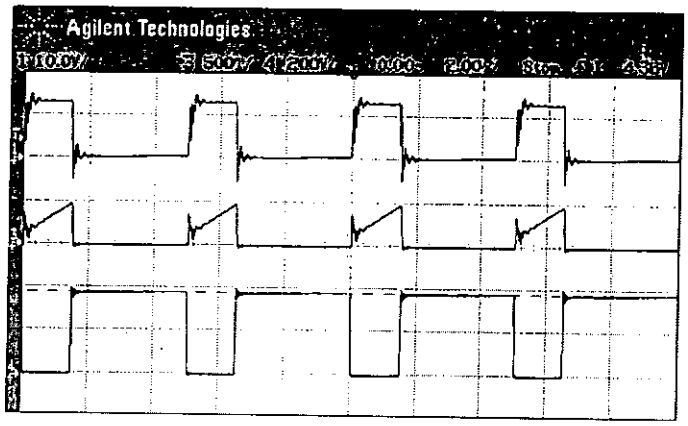
When the switch S was turned off, the drain-to-source voltage of S, v_S, was clamped at ($V_{CB} + V_{Cc}$), which was nearly constant. The waveform of i_L indicated that the MB cell operated in DCM. The waveform of ($i_{Dout1} + i_{Dout2}$) confirmed that the output current ripple was small.

3.4.2 Experimental Results

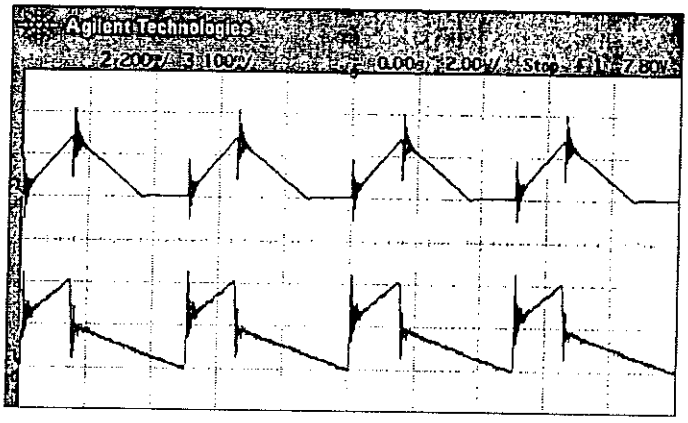
An experimental prototype was built to verify the circuit operation described in the principle of operation section. Before putting the prototype to an AC line test, the DC operation of the prototype was first studied. The input voltage was DC 110 V and the output voltage was DC 28 V. The output power was 100 W.

Fig. 3.12(a) shows the measured waveforms of the gate voltage v_{GS}, the drain current i_S and the drain-to-source voltage v_S of switch S. Fig. 3.12(b) shows the waveforms of the input inductor current i_L and the primary current i_p of the integrated transformer. Fig. 3.12(c) shows the waveforms of the output diode currents. These waveforms agreed well with those obtained by simulation. The waveforms of input inductor current i_L indicated that the MB cell was operating in DCM. The waveform of ($i_{Dout1} + i_{Dout2}$) confirmed that the output current ripple was small.

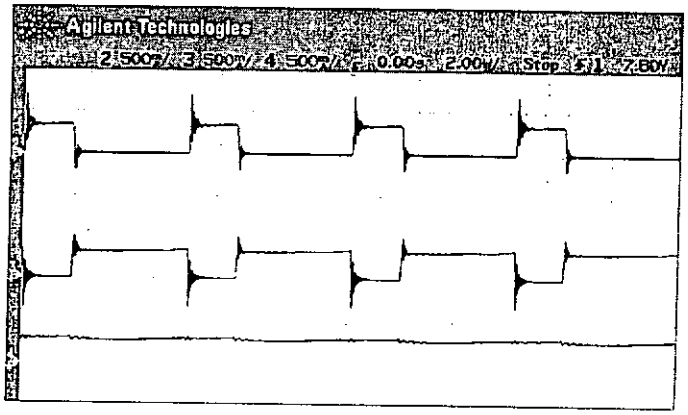
The PFC performance of the prototype was then tested for an AC input of 110 V_{rms} (50 Hz) and a DC output of 28 V. The waveforms of the line voltage and line current for an output power of 100 W are shown in Fig. 3.12 (d). The measured power factor and the THD of the line current were 0.99 and 15% respectively, indicating a high power factor and low THD of the line current. The measured efficiency was between 80% ~ 85%.



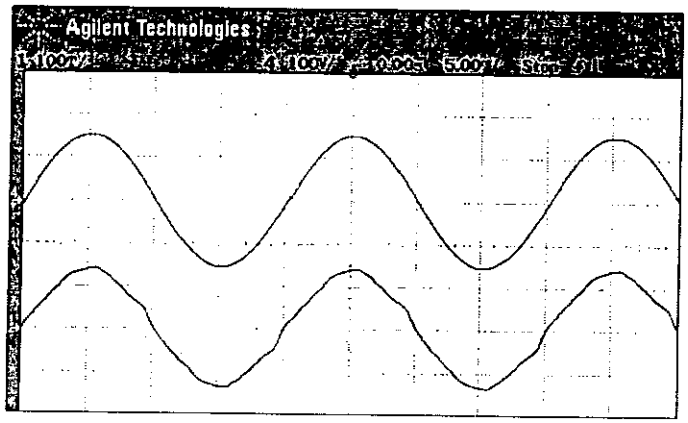
(a) Top trace: v_{GS} @10V/div; Middle trace: i_S @5A/div; Bottom trace: v_S @200V/div



(b) Top trace: i_L @2A/div; Bottom trace: i_P @1A/div



(c) Top trace: i_{Dout1} @5A/div; Middle trace: i_{Dout2} @5A/div; Bottom trace: $(i_{Dout1} + i_{Dout2})$ @5A/div



(d) Top trace: Input line voltage @100V/div; Bottom trace: Input line current @1A/div

Fig. 3.12 Measured waveforms.

3.5 Summary

The characteristics of a novel single-switch high-power-factor regulator with low output current ripple are studied in this chapter. By employing a modified-boost converter cell as the input stage and a double-ended forward converter cell as the output stage, a high power factor and near-zero output current ripple are achieved. This regulator also eliminates the need for an extra clamping switch to recycle the energy trapped in the transformer leakage inductance and to reduce the switch voltage stress. The analysis, design, simulation, and experimental results are reported to verify the operation and performance of the proposed regulator.

CHAPTER 4

A TWO-CHANNEL INTERLEAVED BOOST CONVERTER WITH REDUCED CORE LOSS AND COPPER LOSS

4.1 Introduction

For high power applications, single-ended boost converters have been widely adopted as the front-end of PFC regulators for their simplicity, high conversion efficiency, and relatively low cost. Compared with the other operation modes, CCM operation, which is shown in Fig. 4.1(a), has better utilization of power devices, lower conduction loss, and lower input current ripple. However, at high power level, the large reverse-recovery current of the output rectifier in a CCM operation boost converter will cause not only extra switching loss, but also severe electromagnetic interference noise. This phenomenon can be explained as follows: When the boost switch is turned on, because the output rectifier can not be turned off immediately, reverse recovery effect causes the output capacitor nearly shorted to ground at this instant. Very large current spikes can be observed both at the rectifier and at the switch, which will cause extra switching loss and EMI noise.

According to [66], the diode reverse-recovery is affected by its reverse voltage, forward current, current slew rate, temperature, etc. One effective way to alleviate the reverse-recovery problem is to softly turn off the

rectifier by controlling its $\frac{di}{dt}$ during the period of switch turn-on [67]-[74].

In references [67] and [68], a small inductor in a new parallel channel was used to control the decreasing rate of the rectifier current. The rectifier was softly turned off and the conversion efficiency could be dramatically improved by more than 3% at low line, where the reverse-recovery loss is the most significant [67]. But these topologies need extra auxiliary circuits and complexity is a major drawback. The active-clamp approach [69]-[71] can alleviate the reverse-recovery problem and achieve zero-voltage switching. Reference [69] also proved that, as far as efficiency is concerned, with softly turning off the rectifier, the effect of the reverse-recovery speed of the rectifier is practically eliminated. However, active-clamped circuits usually require auxiliary switches and isolated gate drivers. On the other hand, lossless passive snubbers [72]-[74] can be effective to control the $\frac{di}{dt}$ of the rectifier by inserting an inductor in such a way that the inductor is in series with the rectifier during the turn-on of the switch. However, passive snubbers require many passive components and they increase voltage or current stress on the semiconductor components.

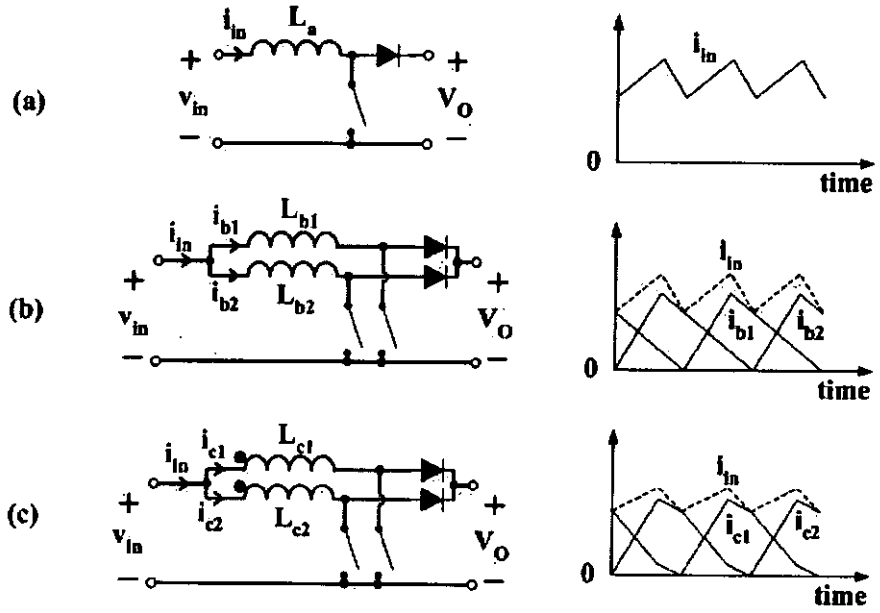


Fig. 4.1 Single-channel and two-channel boost converters ((a) a single-channel boost converter; (b) a two-channel boost converter; (c) a two-channel boost converter with coupled inductors).

An alternative to minimize the reverse-recovery problem while keeping the input current smooth is to use two-channel interleaved boost converters. An example is shown in Fig. 4.1(b). In a two-channel interleaved boost converter, each individual channel can operate in critical conduction mode (CRM) [75] – [78] or discontinuous conduction mode (DCM) [79] to eliminate the reverse-recovery problem. Although the current ripple in each channel is large, the combined input current is continuous and smooth. As a result, the DM – EMI can be managed with a reasonably sized input filter. It should be noted that, for the same average level, the inductor current in CRM operation mode would have a smaller RMS value than that in DCM operation mode. In addition, when the individual channel operates in CRM, reduced switch turn-on loss can be easily achieved by timing the switch to

turn on when the voltage across it has reached a minimum value. Therefore, in order to attain a high efficiency, all the converters discussed later will be supposed to operate in CRM.

Two-channel interleaved direct-coupling boost converters have been used in [66][80][81], as shown in Fig. 4.1(c). In [66], three inductors are used but it is equivalent to a pair of directly coupled inductors. By coupling the inductors, the number of the magnetic components can be reduced to one. Article [80] found that with two directly-coupled inductors, the boost converter channels can have very good current sharing characteristics even in the presence of relatively large duty cycle mismatch. However, since both the inductors have considerable number of turns, the large inductor current ripple in each channel will cause a high copper loss. Furthermore, when the two windings are wound on the outer limbs of a single EI or EE core, AC fluxes generated by the two windings are added in the center leg. Such a large AC flux ripple in the center leg will further increase the core loss. All these losses will lower the efficiency of the converter.

In order to improve the efficiency, this paper proposes an improved two-channel interleaved boost converter using an integrated magnetic component to reduce the core and copper losses. The integrated magnetic component functions as three inductors. All inductor windings are wound on a single EI or EE core. The windings on the two outer legs are inversely coupled. With the proposed winding arrangement, inductors can be designed with smaller inductances so fewer turns can be used. The flux ripple in the center leg can also be greatly cancelled. As a result, copper loss and core loss will be reduced and the overall efficiency can be improved.

The structure of this chapter is: firstly, the proposed integrated magnetics will be derived and its electrical circuit model will be given. Secondly, the operation and characteristics of the proposed integrated magnetics will be discussed. Thirdly, design considerations will be present. Finally, experimental results will be demonstrated.

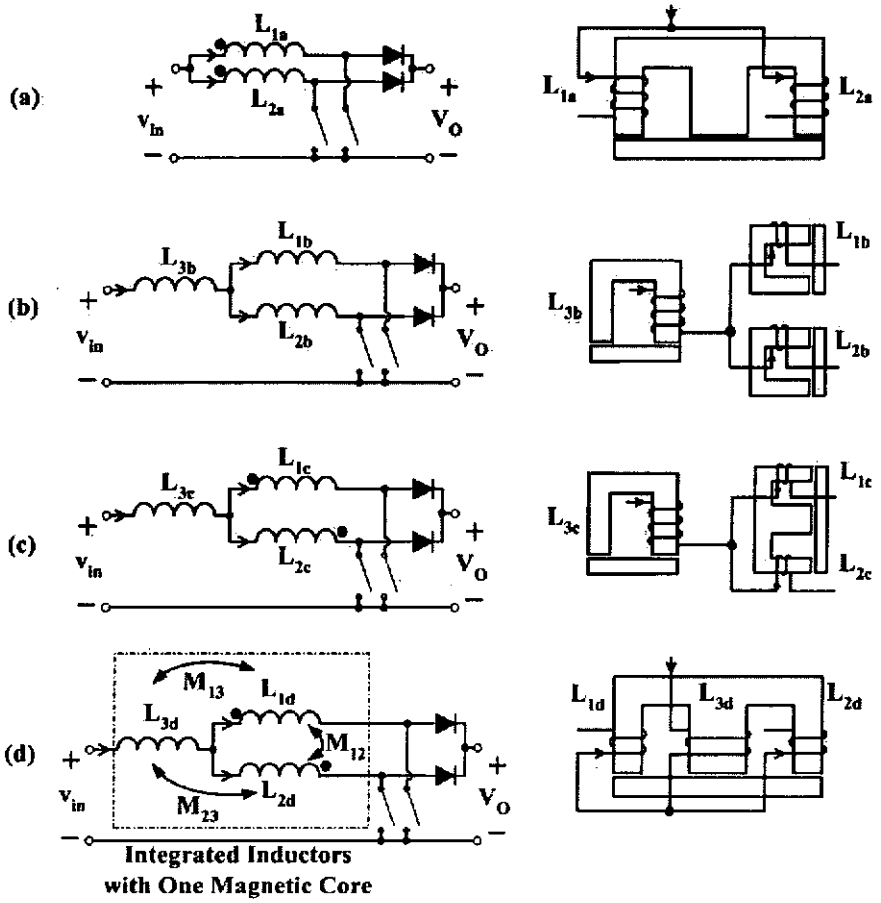


Fig. 4.2 Derivation of the proposed integrated magnetics.

4.2 A New Integrated Magnetics for Direct-Coupling Inductors

A new integrated magnetics for direct-coupling inductors is proposed here. This section will discuss the derivation of the proposed integrated magnetics and derive its equivalent electrical circuit model.

4.2.1 Derivation of the Proposed Integrated Magnetics

Fig. 4.2 shows how the new integrated magnetics is obtained. In Fig. 4.2, circuits are shown on the left and the inductor winding arrangements and core structures are shown on the right.

Fig. 4.2(a) represents the existing structure for two direct-coupling inductors. Windings are wound on the two outer legs and air gaps are added in order to prevent saturation. The thickness of the air gap in the center leg should be carefully tuned to obtain the desired coupling coefficient. In this structure, large AC fluxes generated by the two windings are added in the center leg, which will cause large core loss. The numbers of turns of the windings are great and the large ripple inductor current will increase the copper loss.

The coupled inductors shown in Fig. 4.2(a) can be represented by an equivalent circuit with three uncoupled inductors, as shown in Fig. 4.2(b). In Fig. 4.2(b), L_{3b} can be regarded as the mutual inductance between the two-coupled inductors shown in Fig. 4.2(a) and L_{1b} and L_{2b} are the leakage inductances. Here, it should be noted that the current flowing through L_{3b} is the combined input current so it is quite smooth. As a result, the AC flux in inductor L_{3b} is small and it is expected to have smaller core loss. Although

the currents flowing through L_{1b} and L_{2b} still have large ripple, core losses are possible to be reduced because L_{1b} and L_{2b} are very small in this structure so small cores can be used. If the coupling coefficient between the two inductors shown in Fig. 4.2(a) is high enough (that is, L_{1b} and L_{2b} are small enough), the number of turns of all the inductors shown in Fig. 4.2(b) can be much smaller than that in Fig. 4.2(a). As a result, copper loss can be dramatically reduced. However, the number of magnetic components in this structure increases and it is not the optimized design.

In order to reduce the number of magnetic components and reduce the overall inductances, two inductors, L_{1c} and L_{2c}, can be inversely integrated into a single EI or EE core, as shown in Fig. 4.2(c). Inverse coupling can increase the equivalent inductance and therefore, the practical values of L_{1c} and L_{2c} can be smaller. Although inductor L_{3c} will become larger at the same time, the overall inductances are reduced so fewer turns can be used. Because the two inductors are wound on the outer legs and inversely coupled, the flux in the center leg has a very small AC ripple [82]. Therefore, with proper design, core loss in this structure is similar to that in Fig. 4.2(b).

The number of magnetic components and the inductances of the inductors can be further reduced and a new integrated magnetics is proposed in Fig. 4.2(d). Only one magnetic core is used. Inductor L_{1d} and L_{2d} are still inversely coupled. M_{12} is the mutual inductance between L_{1d} and L_{2d}. M_{13} is the mutual inductance between L_{1d} and L_{3d} while M_{23} is the mutual inductance between L_{2d} and L_{3d}. Compared with the structure in Fig. 4.2(a), from the analysis later it can be found that the overall inductance of this

structure can be designed with smaller value and copper loss can be reduced. The inverse coupling between L_{1d} and L_{2d} will help to cancel the flux ripple in the center leg of the core so smaller core loss can be achieved.

Although the proposed integrated magnetics seems more complex at the first glance, such an integrated magnetics can be replaced by a very simple electrical model.

4.2.2 Electrical Model of the Proposed Structure

The complete circuit schematic with the proposed integrated magnetics is shown in Fig. 4.3. The winding arrangement and the corresponding gyrator model [20] – [27] of the proposed structure are shown in Fig. 4.4(a) and Fig. 4.4(b), respectively. P_1, P_2, and P_3 are the permeances of the corresponding limbs of the core (including the air gaps). N_1, N_2, and N_3 are the numbers of turns of the windings. Air gaps g1, g2, and g3 are added in each limb to prevent saturation. In the gyrator model, C_1, C_2, and C_3 are used to model the permeances P_1, P_2, and P_3, respectively. i_{C1}, i_{C2}, and i_{C3} are used to model the $d\Phi/dt$ of the corresponding limbs of the core. The windings are modeled by the magnetomotive force (MMF) sources.

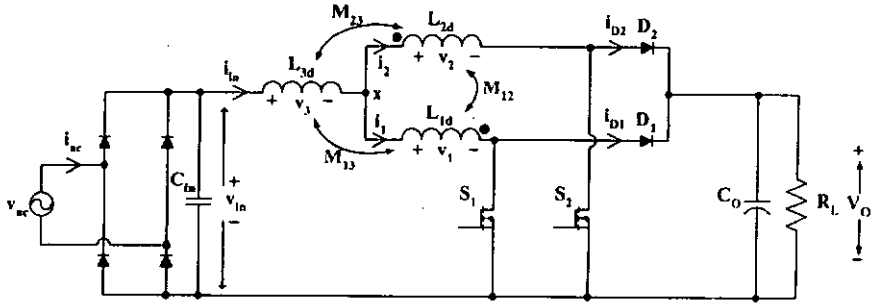
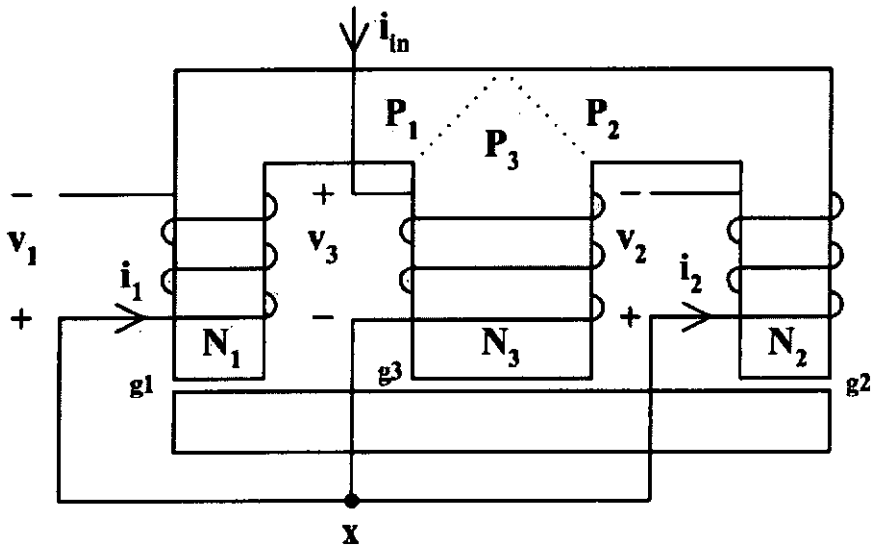
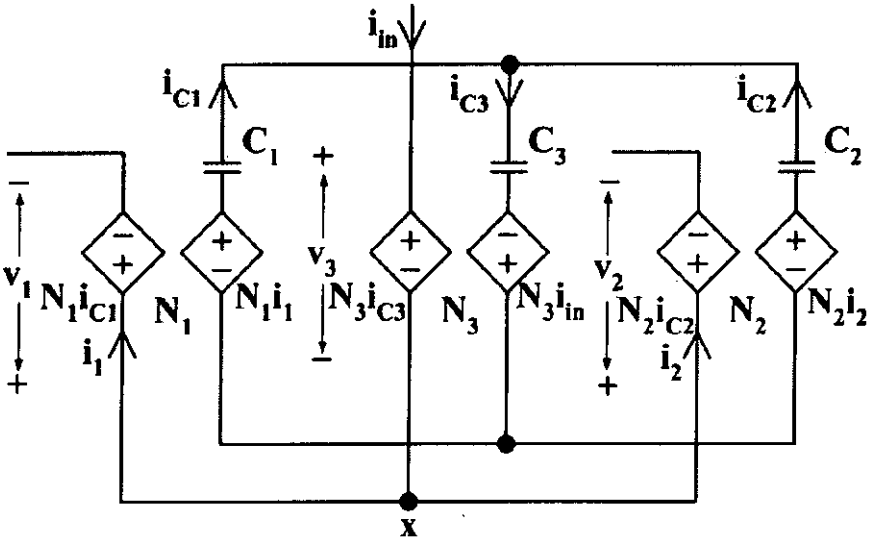


Fig. 4.3 A two-channel interleaved boost converter with the proposed integrated magnetics.



(a) Winding arrangement and core structure of the proposed integrated magnetics



(b) Gyrator model of the proposed integrated magnetics

Fig. 4.4 Winding arrangement and the corresponding gyrator model of the proposed integrated magnetics.

From Fig. 4.4(b) we can find the expressions for i_{C1}, i_{C2}, and i_{C3} as follows:

$$\begin{aligned} i_{C1}(s) &= N_1 i_1(s)\cdot\frac{C_1(C_2+C_3)}{C_1+C_2+C_3}\cdot s - N_2 i_2(s)\cdot\frac{C_1C_2}{C_1+C_2+C_3}\cdot s \\ &\quad + N_3 i_{in}(s)\cdot\frac{C_1C_3}{C_1+C_2+C_3}\cdot s \end{aligned} \tag{4-1}$$

$$\begin{aligned} i_{C2}(s) &= -N_1 i_1(s)\cdot\frac{C_1C_2}{C_1+C_2+C_3}\cdot s + N_2 i_2(s)\cdot\frac{(C_1+C_3)C_2}{C_1+C_2+C_3}\cdot s \\ &\quad + N_3 i_{in}(s)\cdot\frac{C_2C_3}{C_1+C_2+C_3}\cdot s \end{aligned} \tag{4-2}$$

$$\begin{aligned} i_{C3}(s) &= N_1 i_1(s)\cdot\frac{C_1C_3}{C_1+C_2+C_3}\cdot s + N_2 i_2(s)\cdot\frac{C_2C_3}{C_1+C_2+C_3}\cdot s \\ &\quad + N_3 i_{in}(s)\cdot\frac{(C_1+C_2)C_3}{C_1+C_2+C_3}\cdot s \end{aligned} \tag{4-3}$$

From the equations above, the voltages across the inductor windings can be derived as follows:

$$\begin{aligned} v_1(s) &= N_1 i_{C1}(s) \\ &= N_1^2\frac{C_1(C_2+C_3)}{C_1+C_2+C_3}\cdot s i_1(s) - N_1N_2\frac{C_1C_2}{C_1+C_2+C_3}\cdot s i_2(s) \\ &\quad + N_1N_3\frac{C_1C_3}{C_1+C_2+C_3}\cdot s i_{in}(s) \end{aligned} \tag{4-4}$$

$$\begin{aligned} v_2(s) &= N_2 i_{C2}(s) \\ &= -N_1N_2\frac{C_1C_2}{C_1+C_2+C_3}\cdot s i_1(s) + N_2^2\frac{(C_1+C_3)C_2}{C_1+C_2+C_3}\cdot s i_2(s) \\ &\quad + N_2N_3\frac{C_2C_3}{C_1+C_2+C_3}\cdot s i_{in}(s) \end{aligned} \tag{4-5}$$

$$\begin{aligned} v_3(s) &= N_3 i_{C3}(s) \\ &= N_1N_3\frac{C_1C_3}{C_1+C_2+C_3}\cdot s i_1(s) + N_2N_3\frac{C_2C_3}{C_1+C_2+C_3}\cdot s i_2(s) \\ &\quad + N_3^2\frac{(C_1+C_2)C_3}{C_1+C_2+C_3}\cdot s i_{in}(s) \end{aligned} \tag{4-6}$$

Supposing the air gaps in the two outer legs have the same thickness, we have $C_1 = C_2 = C$. Assuming $N_1 = N_2 = N$, $r_C = \frac{C_3}{C}$, and $r_N = \frac{N_3}{N}$, we have

$$L_{1d} = L_{2d} = N^2 \frac{r_C + 1}{r_C + 2} C \tag{4-7}$$

$$L_{3d} = r_N^2 N^2 \frac{2r_C}{r_C + 2} C \tag{4-8}$$

$$M_{12} = -N^2 \frac{1}{r_C + 2} C \tag{4-9}$$

$$M_{13} = M_{23} = r_N N^2 \frac{r_C}{r_C + 2} C \tag{4-10}$$

It should be noted that

$$i_{in} = i_1 + i_2 \tag{4-11}$$

Substituting (4-11) into equations (4-4) ~ (4-6) and assuming $L_{1d} = L_{2d} = L_d$ and $M_{13} = M_{23} = M_3$, Fig. 4.3 can be simplified and shown in Fig. 4.5. It can be seen from Fig. 4.5 that in the electrical circuit model, L_d and L_{3d} are changed to $(L_d + M_3)$ and $(L_{3d} + M_3)$, respectively. The mutual inductance is changed from M_{12} to $(M_{12} + M_3)$.

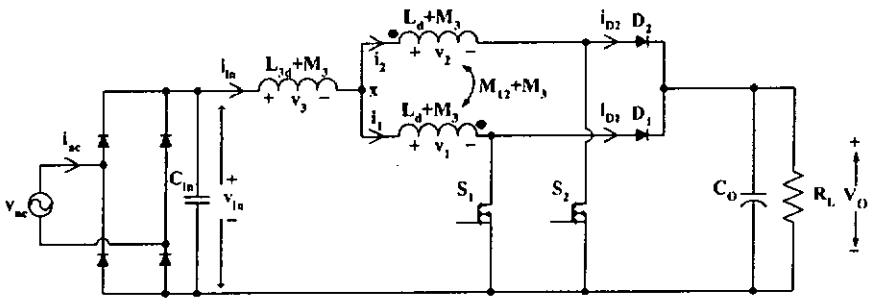


Fig. 4.5 Equivalent electrical circuit.

4.3 Operation and Characteristics of the Proposed Integrated Magnetics

The operation and characteristics of the proposed integrated magnetics will be analyzed in this section. In order to facilitate the analysis, some assumptions are made: (a) The converter has reached its steady-state and each channel operates in CRM; (b) Rectified input voltage v_{in} can be regarded as constant during a switching cycle; (c) The integrated inductors have zero leakage inductance; (d) The output capacitor C_O is large enough to smooth out the switching output voltage ripple and V_O is essentially constant within a switching cycle. Before the analysis, two parameters are defined here (referring to Fig. 4.5):

$$m = \frac{M_{12} + M_3}{L_d + M_3} \tag{4-12}$$

$$n = \frac{L_{3d} + M_3}{L_d + M_3} \tag{4-13}$$

Here m can be regarded as the equivalent coupling coefficient and n is the ratio of the two inductances.

4.3.1 Operation of the Integrated Magnetics

Main voltage and current waveforms are shown in Fig. 4.6 and it can be seen that the operation of the integrated magnetics can be divided into four stages both for $D < 0.5$ and $D > 0.5$. Voltage of point x, which we can define as v_x, is very important in the operation since it will affect the waveforms of all the inductor current. According to Fig. 4.5, the following equations can be obtained:

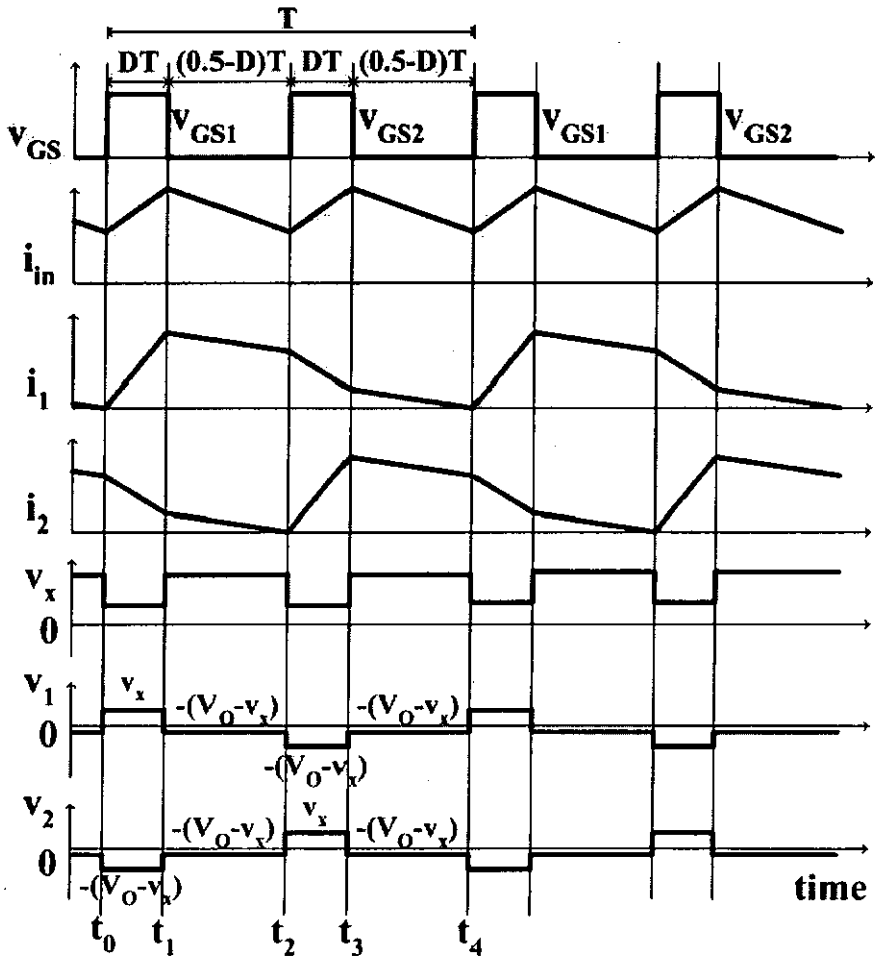
$$v_1 = (L_d + M_3)\frac{di_1}{dt} + (M_{12} + M_3)\frac{di_2}{dt} \quad (4\text{-}14)$$

$$v_2 = (L_d + M_3)\frac{di_2}{dt} + (M_{12} + M_3)\frac{di_1}{dt} \quad (4\text{-}15)$$

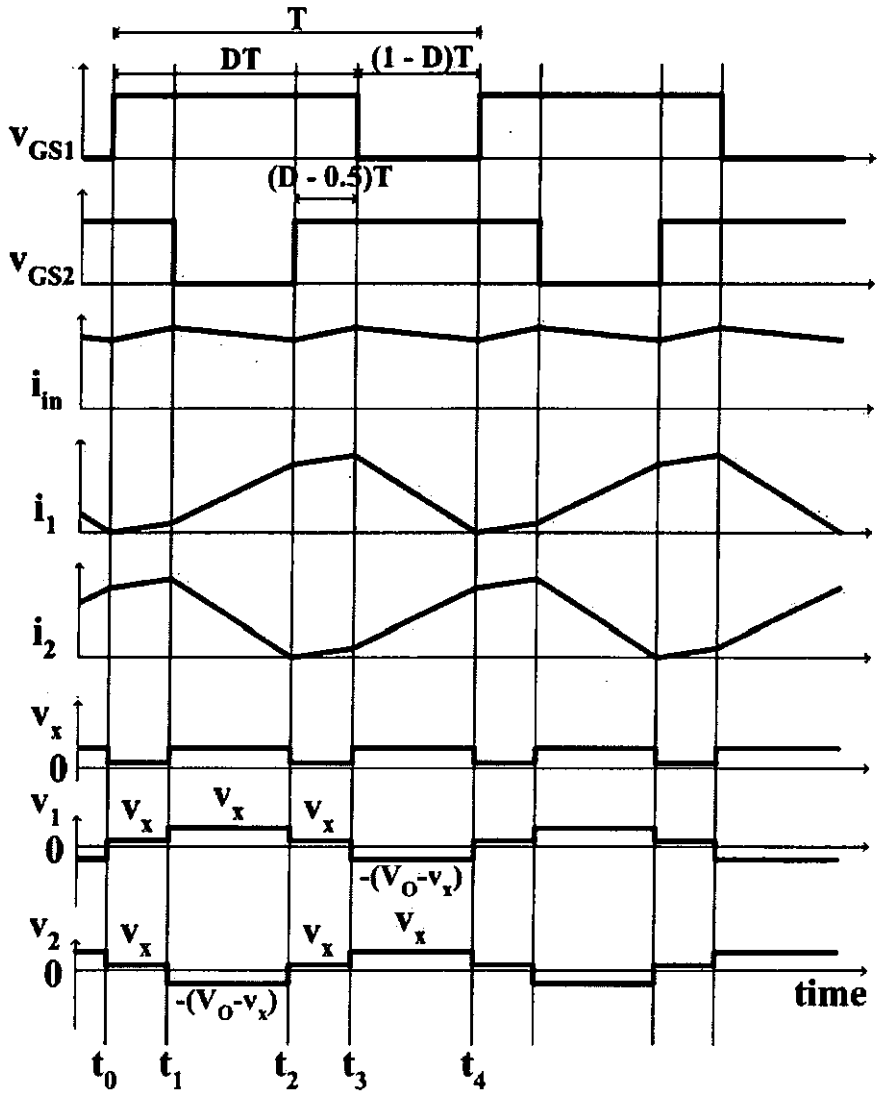
$$v_3 = v_{in} - v_x = (L_{3d} + M_3)\frac{di_{in}}{dt} = (L_{3d} + M_3)\frac{d(i_1 + i_2)}{dt} \quad (4\text{-}16)$$

Substituting (4-14) and (4-15) into (4-16) and combining with (4-12) and (4-13), we have

$$v_{in} - v_x = \frac{n}{m+1}(v_1 + v_2) \quad (4\text{-}17)$$



(a) Main voltage and current waveforms when D < 0.5



(b) Main voltage and current waveforms when D > 0.5

Fig. 4.6 Main voltage and current waveforms of the converter with proposed integrated magnetics.

In order to find the expression of v_x, the relationship between v_1 and v_2 should be found first. As can be seen from Fig. 4.6, there are only four combinations of v_1 and v_2. Follows are the detailed relationships between v_1

and v_2 and based on these, the corresponding expressions of v_x can be attained from (4-17):

$$\begin{cases} v_1 = v_x \\ v_2 = -(V_O - v_x) \end{cases}, \; v_x = \frac{(m+1)v_{in} + nV_O}{m+1+2n} \tag{4-18}$$

$$\begin{cases} v_1 = v_x \\ v_2 = v_x \end{cases}, \; v_x = \frac{(m+1)v_{in}}{m+1+2n} \tag{4-19}$$

$$\begin{cases} v_1 = -(V_O - v_x) \\ v_2 = -(V_O - v_x) \end{cases}, \; v_x = \frac{(m+1)v_{in} + 2nV_O}{m+1+2n} \tag{4-20}$$

$$\begin{cases} v_1 = -(V_O - v_x) \\ v_2 = v_x \end{cases}, \; v_x = \frac{(m+1)v_{in} + nV_O}{m+1+2n} \tag{4-21}$$

From (4-18) ~ (4-21) we can see that v_x is not a fixed value. It will change according to the different combinations of v_1 and v_2. In one switching cycle, three different voltage values will be applied on each winding to change the slope of the inductor current.

Because the two inductors in Fig. 4.5 are coupled together, they can not be considered as two independent inductors. Similar to the analysis in [82], the inductor current waveforms can be found according to the equivalent inductances in different time intervals. This equivalent inductance is used to find the slope rate of the inductor current. Because the current waveforms of i_1 and i_2 are almost the same, except a half cycle delay between them, we will analyze the equivalent inductances for i_1 only. From (4-12), (4-14), and (4-15) we have:

$$v_1 - m \cdot v_2 = (L_d + M_3)(1 - m^2)\frac{di_1}{dt} \tag{4-22}$$

The equivalent inductance L_E for i_1 can be defined as:

$$v_1 = L_E \frac{di_1}{dt} \tag{4-23}$$

By using the relationship between v_1 and v_2 shown in (4-18) ~ (4-21), we can find the expressions of equivalent inductances L_E for i_1. The results are summarized in Table 4.1 (for D < 0.5) and Table 4.2 (for D > 0.5) (where $g = \frac{(m+1)v_{in} - (m+1+n)V_O}{(m+1)v_{in} + nV_O}$). The slope rate of i_1 in different time intervals can be calculated by using the appropriate v_1 and L_E.

Table 4.1 Detailed expressions for v_x and L_E (D < 0.5 and referring to Fig. 4.6(a)).

Time Intervals	v_1 and v_2	v_x	L_E for i_1
$t_0 \sim t_1$	$\begin{cases} v_1 = v_x \\ v_2 = -(V_O - v_x) \end{cases}$	$v_x = \frac{(m+1)v_{in} + nV_O}{m+1+2n}$	$L_E = \frac{(L_d + M_3)(1-m^2)}{1 - m \cdot g}$
$t_1 \sim t_2$	$\begin{cases} v_1 = -(V_O - v_x) \\ v_2 = -(V_O - v_x) \end{cases}$	$v_x = \frac{(m+1)v_{in} + 2nV_O}{m+1+2n}$	$L_E = (L_d + M_3)(1+m)$
$t_2 \sim t_3$	$\begin{cases} v_1 = -(V_O - v_x) \\ v_2 = v_x \end{cases}$	$v_x = \frac{(m+1)v_{in} + nV_O}{m+1+2n}$	$L_E = \frac{(L_d + M_3)(1-m^2)}{1 - \frac{m}{g}}$
$t_3 \sim t_4$	$\begin{cases} v_1 = -(V_O - v_x) \\ v_2 = -(V_O - v_x) \end{cases}$	$v_x = \frac{(m+1)v_{in} + 2nV_O}{m+1+2n}$	$L_E = (L_d + M_3)(1+m)$

Table 4.2 Detailed expressions for v_x and L_E ($D > 0.5$ and referring to Fig. 4.6(b)).

Time Intervals	v_1 and v_2	v_x	L_E for i_1
$t_0 \sim t_1$	$\begin{cases} v_1 = v_x \\ v_2 = v_x \end{cases}$	$v_x = \frac{(m+1)v_{in}}{m+1+2n}$	$L_E = (L_d + M_3)(1+m)$
$t_1 \sim t_2$	$\begin{cases} v_1 = v_x \\ v_2 = -(V_O - v_x) \end{cases}$	$v_x = \frac{(m+1)v_{in} + nV_O}{m+1+2n}$	$L_E = \frac{(L_d + M_3)(1-m^2)}{1-m \cdot g}$
$t_2 \sim t_3$	$\begin{cases} v_1 = v_x \\ v_2 = v_x \end{cases}$	$v_x = \frac{(m+1)v_{in}}{m+1+2n}$	$L_E = (L_d + M_3)(1+m)$
$t_3 \sim t_4$	$\begin{cases} v_1 = -(V_O - v_x) \\ v_2 = v_x \end{cases}$	$v_x = \frac{(m+1)v_{in} + nV_O}{m+1+2n}$	$L_E = \frac{(L_d + M_3)(1-m^2)}{1-\frac{m}{g}}$

4.3.2 Characteristics of the Proposed Integrated Magnetics

In order to make a comparison between the proposed integrated magnetics with the existing two-winding structure shown in Fig. 4.2(a), the equivalent electrical model shown in Fig. 4.5 is further simplified. Fig. 4.7 shows the procedure. The coupled inductors can be replaced by three uncoupled inductors so Fig. 4.7(a) can be changed to Fig. 4.7(b). It should be noted that the physical point x is hidden in Fig. 4.7(b) and finally a pair of coupled inductors can be attained, which is shown in Fig. 4.7(c). In Fig. 4.7(c), the inductance of the inductor is $(L_d + L_{3d} + 2M_3)$ and the mutual inductance is $(L_{3d} + M_{12} + 2M_3)$.

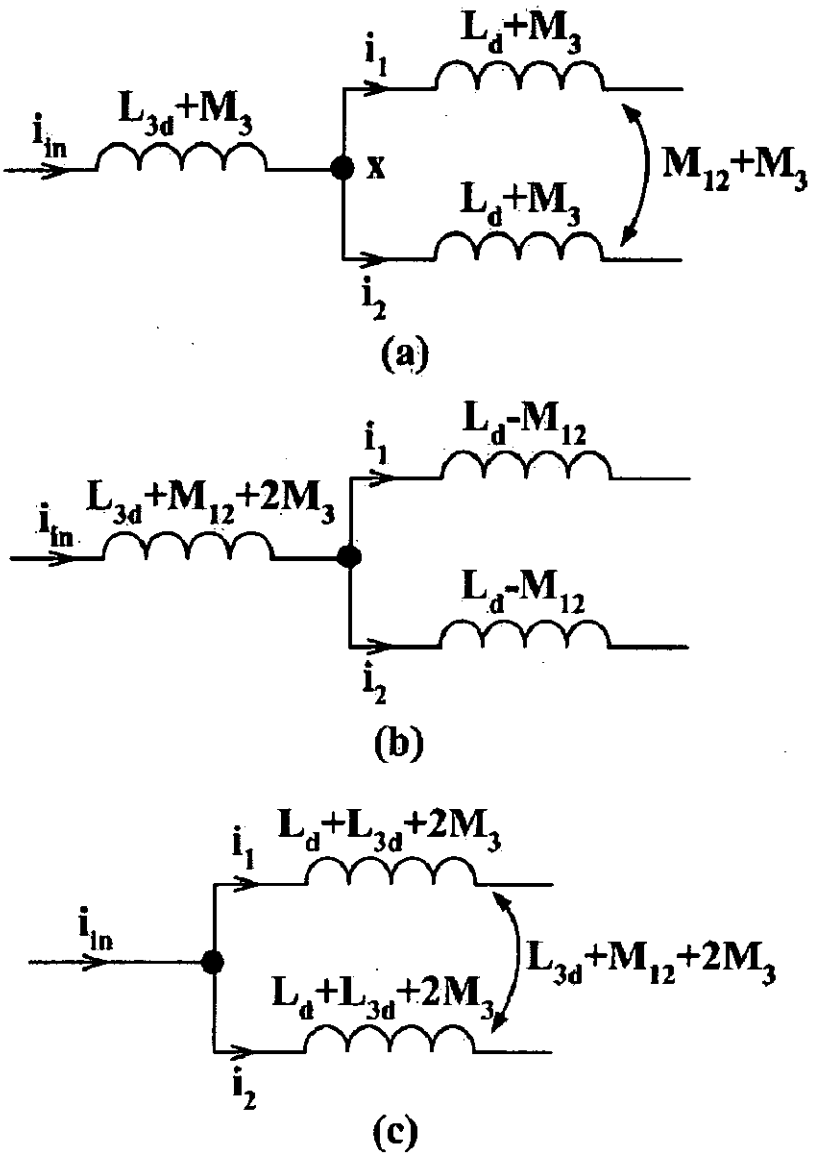


Fig. 4.7 Further simplification of the proposed structure.

By using (4-7), (4-8), and (4-10), the ratio between the overall equivalent inductance shown in Fig. 4.7(c) and the overall practical inductor inductance shown in Fig. 4.3 can be found as follows

$$\gamma = \frac{2(L_d + L_{3d} + 2M_3)}{2L_d + L_{3d}} = \frac{\frac{N^2}{r_C + 2} C(r_C + 1 + 2r_C r_N^2 + 2r_C r_N)}{\frac{N^2}{r_C + 2} C(r_C + 1 + r_C r_N^2)} \quad (4\text{-}24)$$

$$= \frac{r_C + 1 + 2r_C r_N^2 + 2r_C r_N}{r_C + 1 + r_C r_N^2}$$

Equation (4-24) is plotted in Fig. 4.8. From Fig. 4.8 we can see that γ increases as r_N increases. When $r_N = 0$, γ is equal to one. For $r_N > 0$, γ is always larger than one. A higher r_C will give a higher γ. Considering the simplest structure where all the air gaps have the same thickness, we have $r_C \approx 2.0$. For r_N changes from zero to two, γ also changes from one to almost 2.5. Larger γ refers to larger equivalent inductance. Therefore, for a certain value of equivalent inductance, larger γ is corresponding to smaller practical inductance.

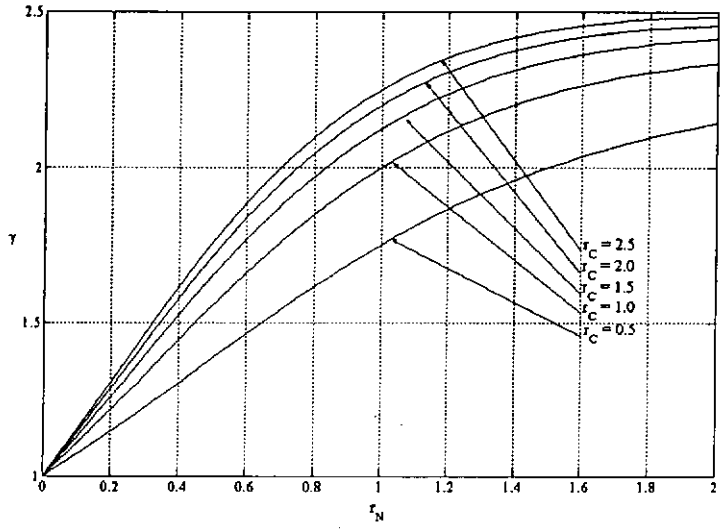


Fig. 4.8 γ as a function of r_N under different r_C.

From Fig. 4.7(c), the coupling coefficient of the equivalent electrical model can be found as (using (4-7) ~ (4-10))

$$\frac{L_{3d}+M_{12}+2M_3}{L_d+L_{3d}+2M_3}=\frac{\frac{N^2}{r_C+2}C(2r_C r_N^{\,2}-1+2r_C r_N)}{\frac{N^2}{r_C+2}C(r_C+1+2r_C r_N^{\,2}+2r_C r_N)}=\frac{2r_C r_N^{\,2}-1+2r_C r_N}{r_C+1+2r_C r_N^{\,2}+2r_C r_N} \quad (4\text{-}25)$$

The relationship between the coupling coefficient and r_N under different r_C is shown in Fig. 4.9. From Fig. 4.9 it can be seen that, the coupling coefficient can be positive or negative according to the combinations of r_C and r_N. For a given value of r_C, when r_N changes from zero to two, the coupling coefficient varies from a negative value which is corresponding to the inverse coupling, to a positive value which represents the direct coupling.

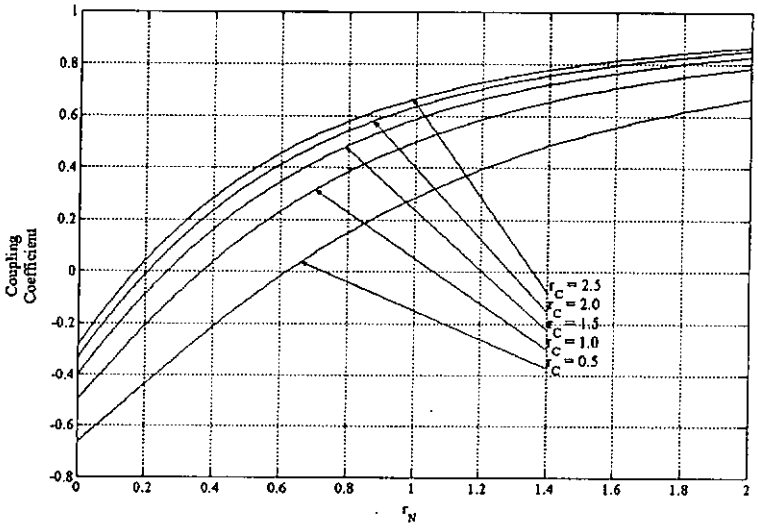
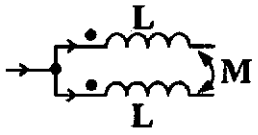
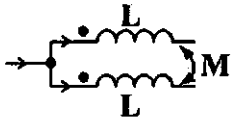
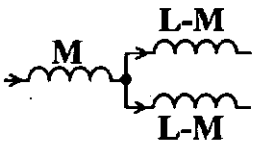
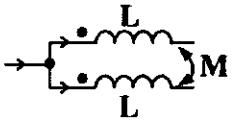
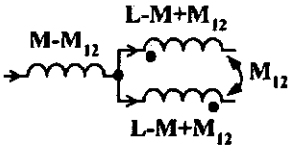
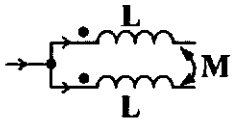
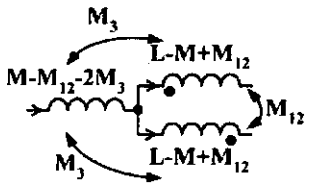
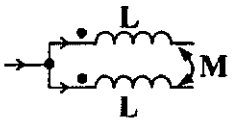


Fig. 4.9 Coupling coefficient as a function of r_N under different r_C.

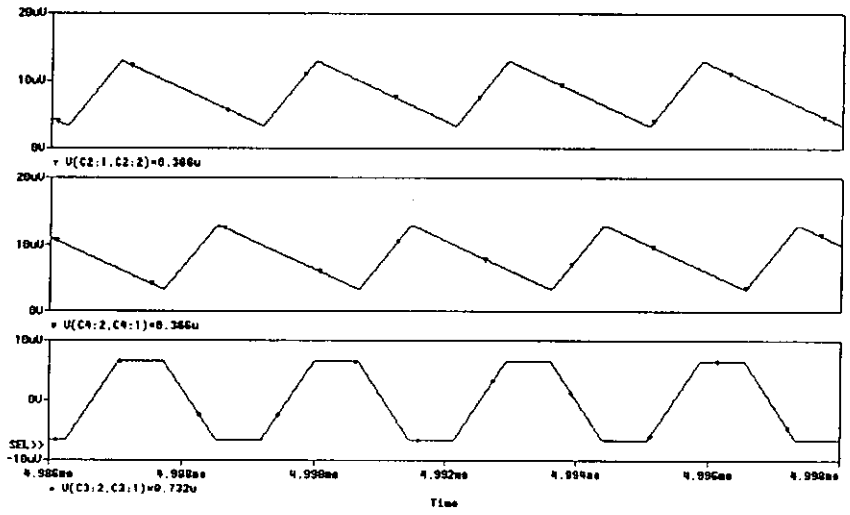
Table 4.3 Comparison of the overall practical inductances among different structures.

Different winding arrangements and core structures	Equivalent circuits (Supposing all the equivalent circuits are the same)	Overall practical inductances
		Normalized to 1 $(M > 0)$
		$1-\frac{M}{2L}$ $(M > 0)$
		$1-\frac{M}{2L}+\frac{M_{12}}{2L}$ $(M > 0,\ M_{12} < 0)$
		$1-\frac{M}{2L}+\frac{M_{12}}{2L}-\frac{M_3}{L}$ $(M > 0,\ M_{12} < 0,\ M_3 > 0)$

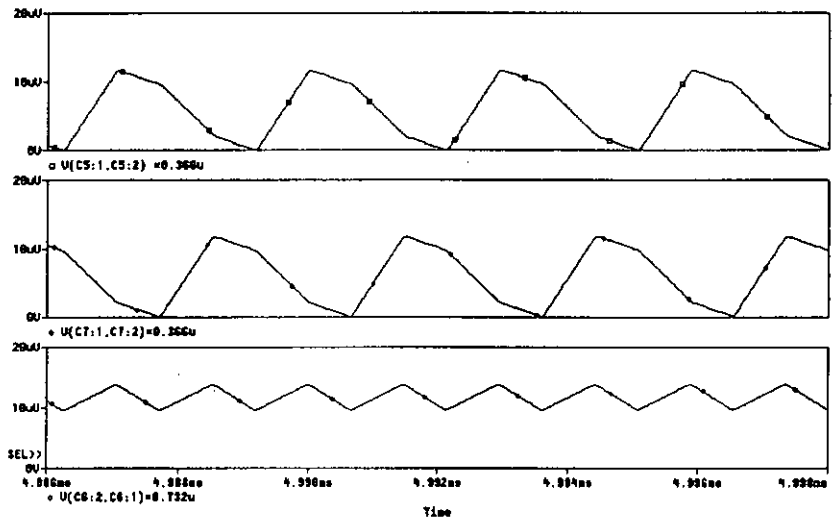
All the winding arrangements shown in Fig. 4.2 can be changed to the same equivalent circuit – a pair of coupled inductors. Supposing all the equivalent circuit models have the same inductor inductances and mutual inductances, a comparison of the overall practical inductance is illustrated in Table 4.3. From Table 4.3 it can be seen that, for the same equivalent circuit, different structures require different inductor inductances. Compared with

the other structures, the proposed integrated magnetics requires the minimum inductance. As a result, both the number of turns and the corresponding copper loss can be reduced with the proposed structure.

In the existing two-winding arrangement, AC fluxes of two outer legs are added in the center leg, which will cause large AC flux ripple. In the proposed integrated magnetics, two inductors L_{1d} and L_{2d} are inversely coupled. As the polarity is changed, the direction of the AC flux generated by the windings is changed correspondingly. As a result, the AC fluxes of two outer legs cancel each other in the center leg. The ripple of the AC flux is reduced so the proposed integrated magnetics will have a lower core loss in the center leg. Fig. 4.10 shows the flux simulation results.



(a) Flux simulation result of the two-winding integrated magnetics (Top trace and middle trace: flux in the outer legs; Bottom trace: flux in the center leg.)



(b) Flux simulation result of the proposed integrated magnetics (Top trace and middle trace: flux in the outer legs; Bottom trace: flux in the center leg.)

Fig. 4.10 Flux simulation results of two integrated magnetics.

4.4 Design Considerations

In order to facilitate the design of the converter, the duty cycle D, inductances of the proposed integrated magnetics and other design issues associated with the magnetic core will be discussed in this section.

4.4.1 Expression of Duty Cycle D

Because each channel operates in CRM and during the steady state, the voltage-second applied on the inductors should balance for each cycle, the duty cycle D can be found as follows:

$$D = 1 - \frac{v_{in}}{V_o} = 1 - \frac{V_{in,pk}}{V_o} \cdot \sin\theta, (\theta \in [0, \pi]) \qquad (4\text{-}26)$$

where $V_{in,pk}$ is the peak value of the input voltage.

4.4.2 Inductances of the Integrated Magnetics

The inductances of the integrated magnetics can be determined by the balance of the input power and the output power of the converter. The average combined input current, $I_{in,avg}$, should be found first. Because $I_{in,avg}$ is equal to the peak value of each inductor current for symmetric structure, basing on Fig. 4.6 and Table 4.1 and 4.2, the expression for $I_{in,avg}$ can be found as follows:

$$I_{in,avg} = \begin{cases} i_1(t_1) = \dfrac{v_x(t_0 \sim t_1)}{L_E} DT \\ \quad = \dfrac{v_{in}}{L_d + M_3} \cdot DT \cdot \dfrac{(1 - m + \dfrac{m+n}{1-D})}{(m+1+2n)(1-m)}, (D < 0.5) \\ i_1(t_3) = \dfrac{v_x(t_3 \sim t_4)}{L_E} (1-D)T \\ \quad = \dfrac{v_{in}}{L_d + M_3} \cdot DT \cdot \dfrac{(1 - m + \dfrac{m+n}{D})}{(m+1+2n)(1-m)}, (D > 0.5) \end{cases} \tag{4-27}$$

where $i_1(t_1)$, $i_1(t_3)$ are the values of i_1 at $t = t_1$ and $t = t_3$, respectively.

The expression of $I_{in,avg}$ can be written as

$$I_{in,avg} = \frac{v_{in}}{L_d + M_3} \cdot DT \cdot \frac{\left[1 - m + \dfrac{m+n}{\max(1-D, D)}\right]}{(m+1+2n)(1-m)} \tag{4-28}$$

Equation (4-28) tells us that to achieve unit power factor, the switching on-time can not be constant. This is different from the case of a single-channel boost converter operating in CRM.

Assuming the conversion efficiency of the converter is η, the balance between input power and output power can be expressed as follows:

$$\eta \cdot \frac{1}{\pi} \cdot \int_0^{\pi} v_{in} \cdot I_{in,avg} \cdot d\theta = \frac{V_O^2}{R_L} \tag{4-29}$$

where R_L is the load resistance.

Substituting (4-28) into (4-29), we have

$$\eta \cdot \frac{V_{in,pk}^2}{2} \cdot \frac{DT}{L_d + M_3} \cdot \frac{\left[1 - m + \frac{m+n}{\max(1-D, D)}\right]}{(m+1+2n)(1-m)} = \frac{V_O^2}{R_L} \tag{4-30}$$

$$L_d + M_3 = \eta \cdot \frac{R_L}{2} \cdot \frac{V_{in,pk}^2}{V_O^2} \cdot DT \cdot \frac{\left[1 - m + \frac{m+n}{\max(1-D, D)}\right]}{(m+1+2n)(1-m)} \tag{4-31}$$

For CRM operation, in order to find the inductance of the inductor, the maximum switching cycle T_{max} will be used. It occurs at the peak input voltage and the maximum output power. Once the maximum switching cycle T_{max} is found, the inductor can be determined by (4-31).

4.4.3 Other Design Issues with the Magnetic Core

All the windings should have the minimum number of turns to prevent the saturation of the core by limiting the $d\Phi/dt$. From Fig. 4.6, Table 4.1, and Table 4.2, we have:

For outer legs:

$$\begin{cases} N \geq \dfrac{v_x(t_0 \sim t_1)}{A_e \Delta B} DT = \dfrac{V_O D(1-D)T}{A_e \Delta B} \cdot \dfrac{m+1+\frac{n}{1-D}}{m+1+2n}, (D < 0.5) \\ N \geq \dfrac{V_O - v_x(t_3 \sim t_4)}{A_e \Delta B}(1-D)T = \dfrac{V_O D(1-D)T}{A_e \Delta B} \cdot \dfrac{m+1+\frac{n}{D}}{m+1+2n}, (D > 0.5) \end{cases} \tag{4-32}$$

For center leg:

$$\begin{cases} N \geq \dfrac{v_{in} - v_x(t_0 \sim t_1)}{2r_N A_e \Delta B} DT = \dfrac{V_O D(1-D)T}{2r_N A_e \Delta B} \cdot \dfrac{n(2 - \frac{1}{1-D})}{m+1+2n}, (D < 0.5) \\ N \geq \dfrac{v_x(t_3 \sim t_4) - v_{in}}{2r_N A_e \Delta B}(1-D)T = \dfrac{V_O D(1-D)T}{2r_N A_e \Delta B} \cdot \dfrac{n(2 - \frac{1}{D})}{m+1+2n}, (D > 0.5) \end{cases} \tag{4-33}$$

where A_e represents the cross-sectional area of the outer limbs of the core and ΔB denotes the flux excursion. It should be noted that the cross-sectional area of the center limb of the core is approximately two times A_e. Expressions (4-32) and (4-33) can be simplified into:

$$\text{For outer legs: } N \geq \frac{V_O D(1-D)T}{A_e \Delta B} \cdot \frac{m+1+\dfrac{n}{\max(1-D, D)}}{m+1+2n} \tag{4-34}$$

$$\text{For center leg: } N \geq \frac{V_O D(1-D)T}{2r_N A_e \Delta B} \cdot \frac{n\left[2 - \dfrac{1}{\max(1-D, D)}\right]}{m+1+2n} \tag{4-35}$$

The larger value between (4-34) and (4-35) should be chosen.

Air gaps are added to prevent saturation. In order to simplify the design, all the air gaps are assumed to have the same thickness, l_g. To find the expression of l_g, ΔB of the three limbs of the magnetic core should first be determined. From Fig. 4.4(b) and equations (4-1) ~ (4-3) we have

$$\begin{aligned} \Delta B_1 &= \frac{\Delta \Phi_1}{A_e} = \frac{C_1 \cdot v_{C1}}{A_e} = \frac{C_1 \cdot i_{C1}(s) \cdot \dfrac{1}{sC_1}}{A_e} \\ &\approx \frac{\mu_0}{l_g} \cdot \frac{N}{r_C + 2} \cdot \left[i_1 \cdot (r_C r_N + r_C + 1) + i_2 \cdot (r_C r_N - 1) \right] \end{aligned} \tag{4-36}$$

$$\Delta B_2 = \frac{\Delta\Phi_2}{A_e} = \frac{C_2 \cdot v_{C2}}{A_e} = \frac{C_2 \cdot i_{C2}(s) \cdot \frac{1}{sC_2}}{A_e} \approx \frac{\mu_0}{l_g} \cdot \frac{N}{r_C + 2} \cdot [i_1 \cdot (r_C r_N - 1) + i_2 \cdot (r_C r_N + r_C + 1)] \quad (4\text{-}37)$$

$$\Delta B_3 = \frac{\Delta\Phi_3}{2A_e} = \frac{C_3 \cdot v_{C3}}{2A_e} = \frac{C_3 \cdot i_{C3}(s) \cdot \frac{1}{sC_3}}{2A_e} \approx \frac{\mu_0}{l_g} \cdot \frac{N}{r_C + 2} \cdot \left[i_1 \cdot (r_C r_N + \frac{r_C}{2}) + i_2 \cdot (r_C r_N + \frac{r_C}{2}) \right] \quad (4\text{-}38)$$

where $\mu_0 = 4\pi \times 10^{-7}$.

From (4-36) ~ (4-38) l_g can be found as follows:

$$l_g \approx \frac{N}{r_C + 2} \cdot \frac{\mu_0}{\max(\Delta B)} \cdot \max \begin{Bmatrix} i_1 \cdot (r_C r_N + r_C + 1) + i_2 \cdot (r_C r_N - 1) \\ i_1 \cdot (r_C r_N - 1) + i_2 \cdot (r_C r_N + r_C + 1) \\ i_1 \cdot (r_C r_N + \frac{r_C}{2}) + i_2 \cdot (r_C r_N + \frac{r_C}{2}) \end{Bmatrix} \quad (4\text{-}39)$$

4.5 Experimental Results

Both the existing two-winding structure (shown in Fig. 4.2(a)) and the proposed integrated magnetics were evaluated by experimental work. The converter was designed to have the following parameters: (a) Input AC voltage v_{ac} = 150 ~ 250 V_{RMS}; (b) Output DC voltage V_O = 400 V; (c) Output power P_O = 500 W; (d) Minimum switching frequency $f_{s,min}$ = 50 kHz; (e) Switches S_1 and S_2: IRF840; (f) Output rectifiers D_1 and D_2: MUR460; (g) Output capacitor C_O = 560 uF/450 V; (h) Magnetic core: Planar OR44308; (i) Thickness of air gaps: 0.6 mm. Both the two-winding structure and the proposed integrated magnetics have the same core structure for fair comparison. For two-winding integrated magnetics, the

inductance of each inductor is 165.3 uH (25 turns of #38 AWG×64). For the proposed integrated magnetics, L_d = 82.65 uH (16 turns of #38 AWG×64) and L_{3d} = 27.55 uH (8 turns of #38 AWG×64). The controller IC is MC33262.

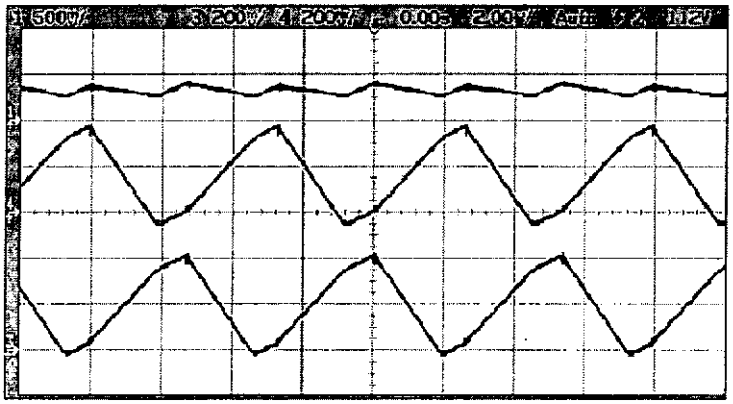


Fig. 4.11 Experimental inductor current waveforms for v_{in} = 150 VDC and P_O = 500 W. (From top to bottom: i_{in}, 5A/div; i_1, 2A/div; i_2, 2A/div. Time base: 2us/div.)

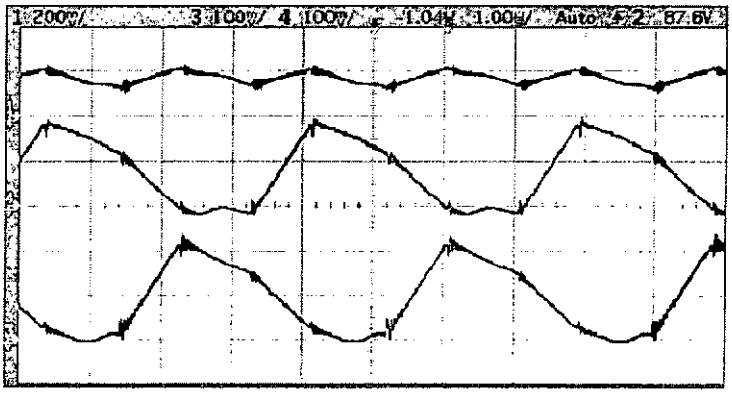


Fig. 4.12 Experimental inductor current waveforms for v_{in} = 300 VDC and P_O = 500 W. (From top to bottom: i_{in}, 2A/div; i_1, 1A/div; i_2, 1A/div. Time base: 1us/div.)

Before putting the circuit to an AC line test, the DC operation of the converter with the proposed integrated magnetics was first studied. Fig. 4.11 and Fig. 4.12 show the inductor current waveforms i_{in}, i_1, and i_2 when v_{in} = 150 VDC and v_{in} = 300 VDC, respectively (both the output powers are equal to 500 W). These waveforms agreed well with the theoretical predictions in Fig. 4.6, except a small dead time was added between the cross-zero of the inductor current and the turn-on of the switch, which was used to achieve reduced switch turn-on loss. As a result, i_1 and i_2 were practically in discontinuous conduction mode but very close to CRM operation. Both i_1 and i_2 had large current ripple. i_{in} was the combined input current and its ripple was quite small.

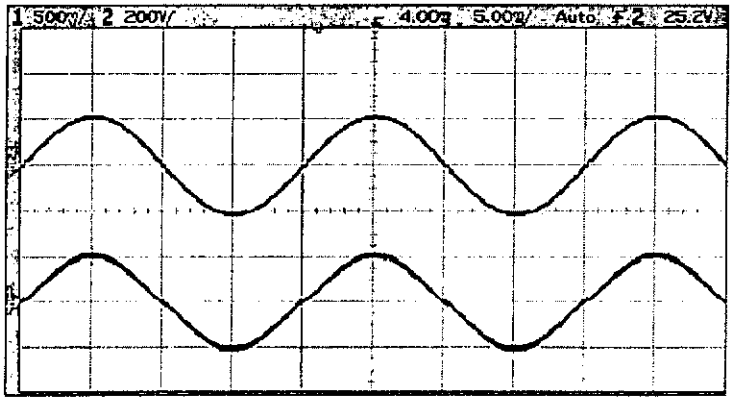


Fig. 4.13 Line voltage and line current waveforms for v_{ac} = 150 V_{RMS} and P_O = 500 W. (From top to bottom: Line voltage, 200V/div; Line current, 5A/div. Time base: 5ms/div.)

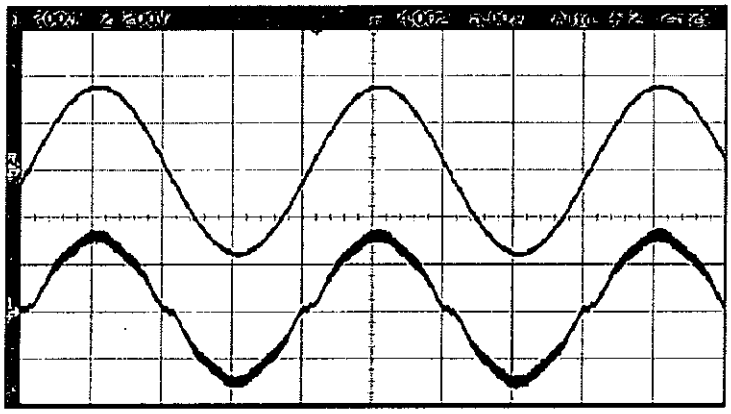


Fig. 4.14 Line voltage and line current waveforms for v_{ac} = 250 V_{RMS} and P_O = 500 W. (From top to bottom: Line voltage, 200V/div; Line current, 2A/div. Time base: 5ms/div.)

Fig. 4.13 (v_{ac} = 150 V_{RMS}, P_O = 500 W) and Fig. 4.14 (v_{ac} = 250 V_{RMS}, P_O = 500 W) show the waveforms of the line voltage and line current for the circuit with the proposed integrated magnetics. Power factors and THDs of line currents of the proposed structure at different input voltages are given in Fig. 4.15 and Fig. 4.16, respectively. Fig. 4.17 shows the comparison of the conversion efficiencies of the proposed structure and the two-winding structure. Both the structures had very high conversion efficiencies because of the alleviated rectifier reverse-recovery problem. From Fig. 4.17 it can be seen that the converter with the proposed integrated magnetics had higher conversion efficiencies than the converter with the two-winding structure. When input voltage is minimum, where the losses are the most significant, approximately 0.7% efficiency improvement was obtained, which accounted for about 3.5W loss reduction for 500W output power. Such efficiency improvement shows that the proposed integrated magnetics can dramatically reduce the copper loss and core loss.

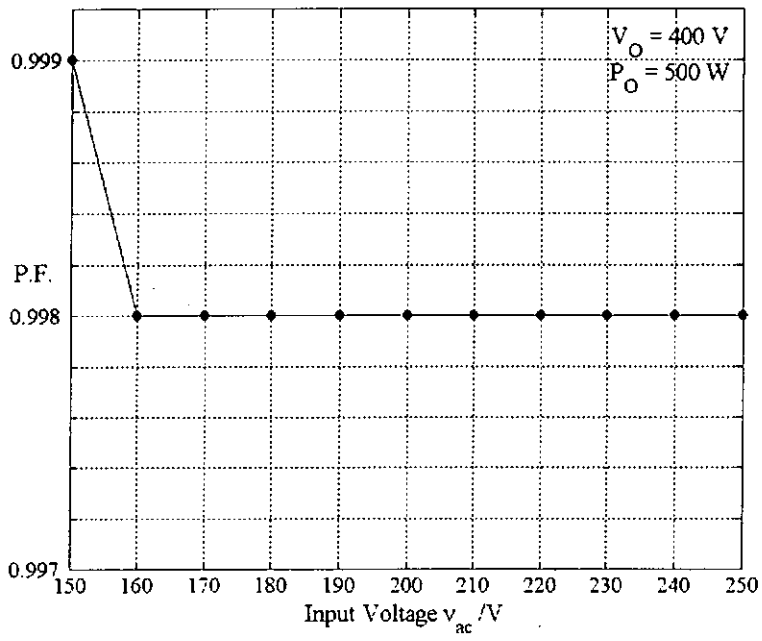


Fig. 4.15 Power factors of line current of the proposed structure at different input voltages v_{ac}.

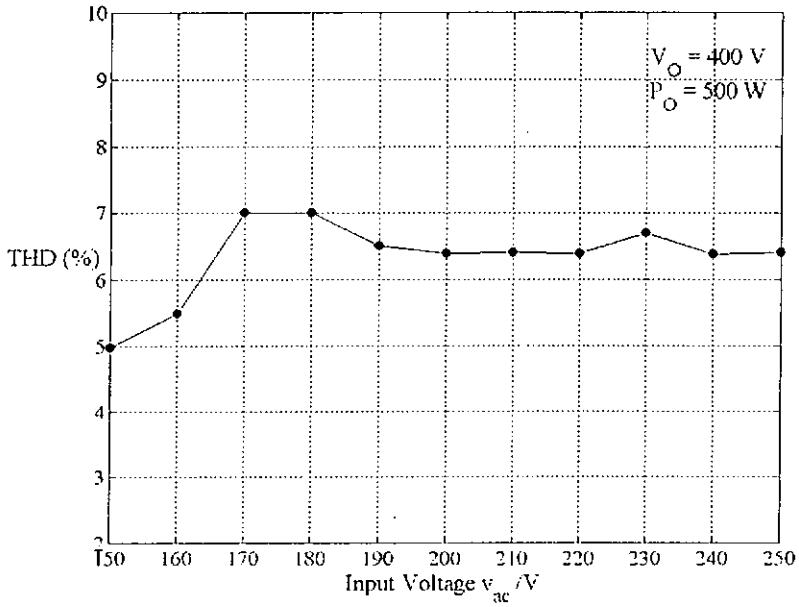


Fig. 4.16 THDs of line current of the proposed structure at different input voltages v_{ac}.

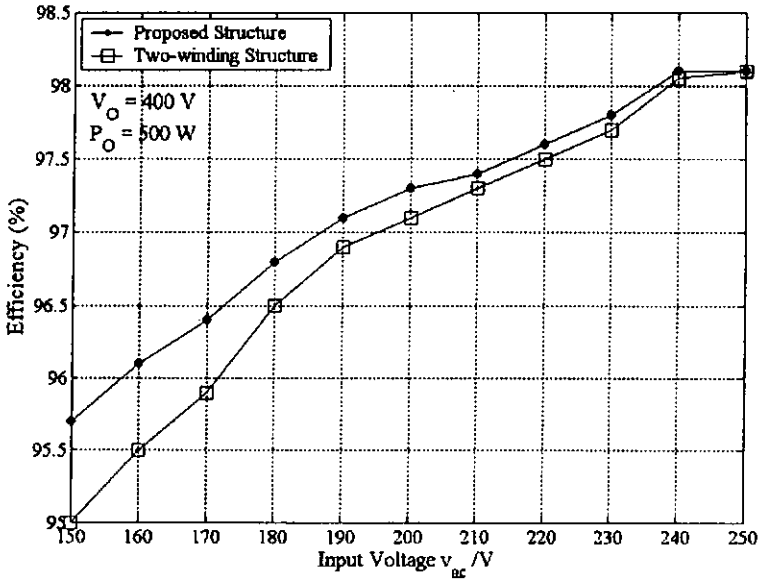


Fig. 4.17 Comparison of the conversion efficiencies of the proposed structure and the two-winding structure for the PFC converter.

4.6 Summary

A two-channel interleaved boost converter using an integrated magnetic component to reduce the core and copper losses has been proposed in this paper. With the proposed winding arrangement, inductors can be designed to have smaller inductances and lower copper losses. The windings on the two outer legs are inversely coupled and the AC flux ripple in the center leg is cancelled. The derivation and electrical circuit model of the proposed integrated magnetic component are discussed. Experimental results show the efficiency improvement due to the adoption of the proposed structure.

CHAPTER 5

A THREE-CHANNEL INTERLEAVED CCM BOOST CONVERTER WITH ZERO DIODE REVERSE-RECOVERY LOSS

5.1 Introduction

In Chapter 4, a two-channel interleaved boost converter is proposed to replace a single-channel boost converter operating in CCM for high power PFC applications. The output power is shared by two channels and a high efficiency can be attained. However, when the output power increases, the power to be processed in each channel maybe higher than its power-handling capability. Therefore, three or more channels need to be paralleled. In [83], four-channel flyback converter was constructed to provide 600 W output power. Article [84] used an eight-channel boost converter to provide 1.5 kW output power for office environment computer applications and high efficiencies were achieved (94% ~ 97%, including bias supply and EMI filter losses).

By increasing the number of interleaved channels, current stress for each channel can be reduced and the net ripple amplitude of both input and output current can be smaller. The effective ripple frequency of the overall converter can be raised without increasing the switching loss or device

stresses. In some cases where the ripple may already be small, for the same ripple amplitude, increasing the number of interleaved channels can help to reduce the switching frequency and/or reduce the inductance per channel, which can increase the conversion efficiency of the converter [84].

With the aim to further increase the power level while eliminating the reverse-recovery problem, a highly efficient, three-channel interleaved CCM boost converter is proposed in this chapter, which has the following features:

- An integrated magnetic component is used to control the $\frac{di}{dt}$ of output rectifiers.
- The circuit can be extended to any number of channels and is particularly suitable for large power applications.

The basic three-channel circuit topology and the principle of operation will first be explained. Design considerations will then be given. Finally, the simulation and experimental results, based on the analysis in the former sections, will be demonstrated.

5.2 Basic Circuit and Principle of Operation

The proposed three-channel interleaved CCM boost converter is shown in Fig. 5.1. L_m is the main boost converter inductor. The current through L_m, i_{Lm}, is continuous and has very small ripple. Compared to the conventional boost converter, the proposed converter has three channels: L_1, S_1, D_1 as Channel 1, L_2, S_2, D_2 as Channel 2, and L_3, S_3, D_3 as Channel 3. As will be shown later, with proper design, the current through each rectifier can be

decreased in steps and finally be reduced to zero before the switch in the same channel is turned on. L_1, L_2, and L_3 are small inductances when compared with L_m and they each can be utilized to control the decreasing rate of the current through the corresponding rectifier. C_O is the output capacitor.

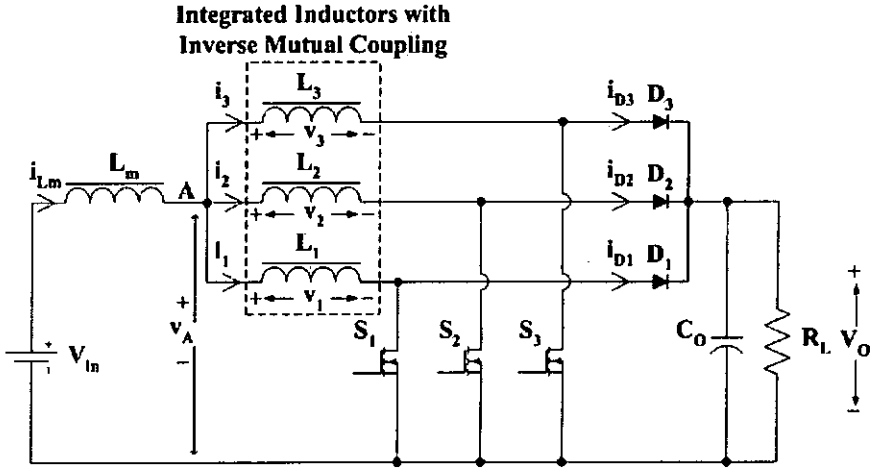


Fig. 5.1 The proposed three-channel interleaved CCM boost converter.

Instead of using three separate inductors, L_1, L_2, and L_3 are wound on a single magnetic core. The physical structure and practical winding arrangement of the integrated inductors are shown in Fig. 5.2(a), where P_1, P_2, and P_3 are the permeances of the corresponding limbs of the integrated inductors. Three inductors are wound on three limbs of the core respectively. N_1, N_2, and N_3 are the numbers of turns. Air gaps are added to prevent saturation of the magnetic core. Based on [20]-[27], the Z–parameter/gyrator model and the equivalent-circuit model of the integrated inductors are shown in Fig. 5.2(b) and Fig. 5.2(c), respectively. In Fig. 5.2(b), C_1, C_2, and C_3 are used to model P_1, P_2, and P_3, respectively. The

windings are modeled by the magnetomotive force (MMF) sources. In Fig. 5.2(c), L_{s1}, L_{s2}, and L_{s3} are used to modeled P_1, P_2, and P_3, respectively. Here numerically, $L_{s1} = C_1 = P_1$, $L_{s2} = C_2 = P_2$, and $L_{s3} = C_3 = P_3$. The circuits in the dashed-line boxes T_1, T_2, and T_3 are ideal transformers and the following equations can be found: $L_1 = N_1^2 L_{s1}$, $L_2 = N_2^2 L_{s2}$, and $L_3 = N_3^2 L_{s3}$.

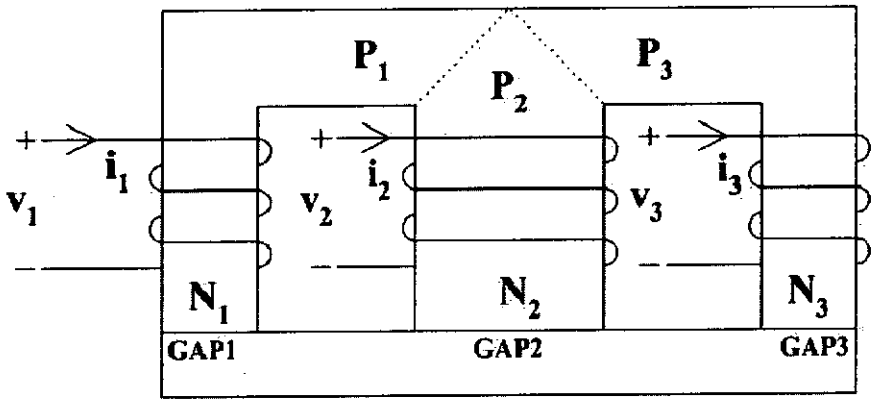


Fig. 5.2(a) Winding arrangement.

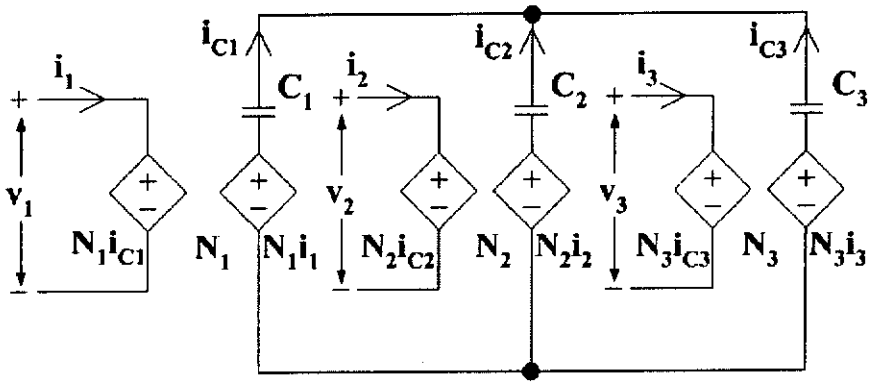


Fig. 5.2(b) Z–parameter/gyrator model.

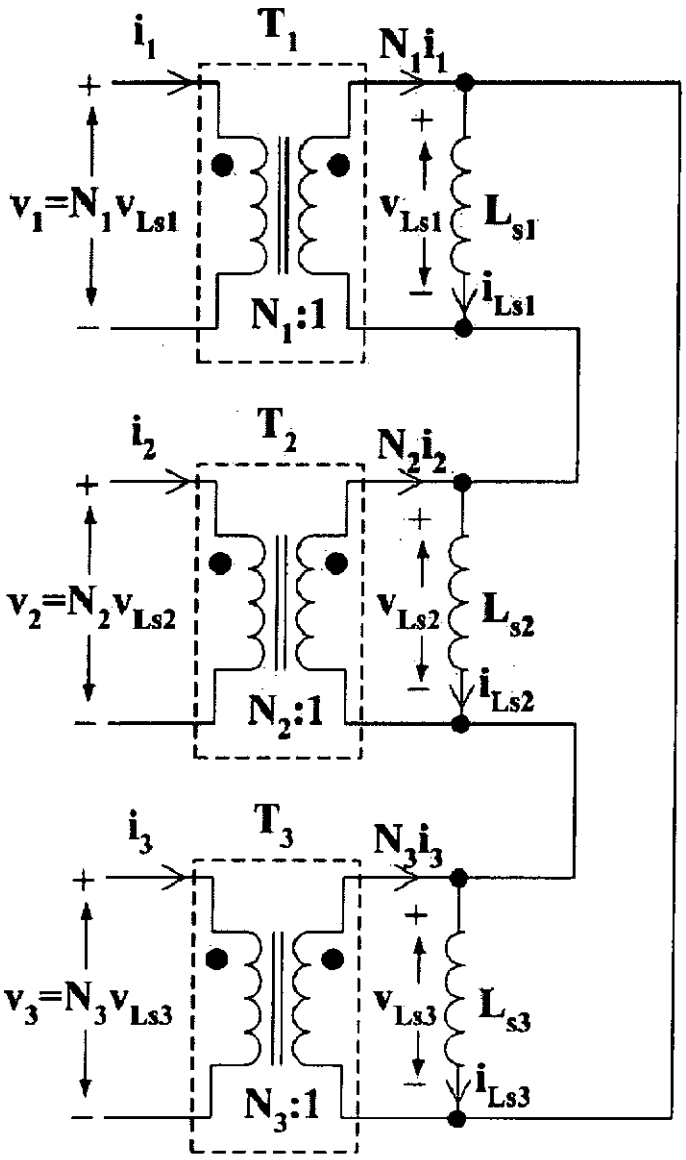


Fig. 5.2(c) Equivalent-circuit model.

Fig. 5.2 Winding arrangement, Z–parameter/gyrator model, and the equivalent-circuit model of three inversely-coupled integrated inductors.

It should be noted that the winding arrangement shown in Fig. 5.2(a) enables the magnetic flux to be inversely coupled between each pair of the coupled inductors. It is this mutually opposite-polarity coupling that

enhances the separation among different channels of the converter (which help achieve zero diode recovery loss).

The inverse coupling arrangement can be extended to any number of channels. Fig. 5.3 shows the arrangement of an integrated magnetic with five inversely coupled inductors.

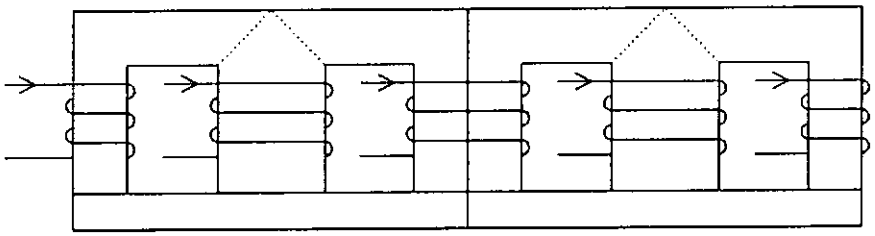


Fig. 5.3 Winding arrangement of five inversely-coupled integrated inductors.

To facilitate the analysis of circuit operation, the following assumptions are made:

1. The converter has reached its steady state and the main inductor current i_{Lm} is continuous.
2. The integrated inductors have zero leakage inductance.
3. Numerically, $L_1 = L_2 = L_3 = L$.
4. The output capacitor C_O is large enough to smooth out the switching output voltage ripples and V_O is essentially constant within a switching cycle.

With the aid of the waveforms shown in Fig. 5.4 and the current paths shown in Fig. 5.5 (where the thick lines indicate the conducting path), the operation of the converter can be explained as follows.

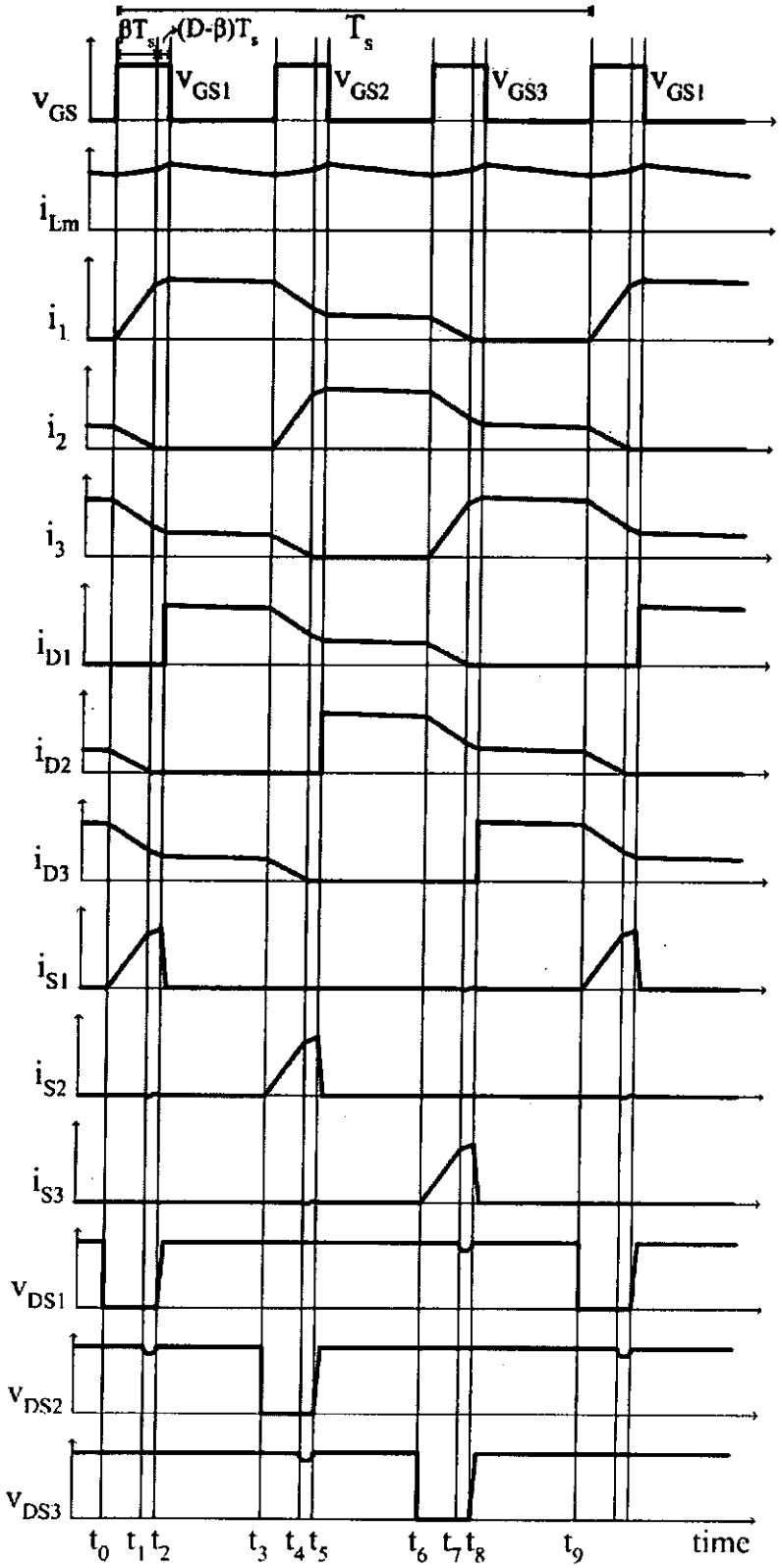


Fig. 5.4 Key voltage and current waveforms.

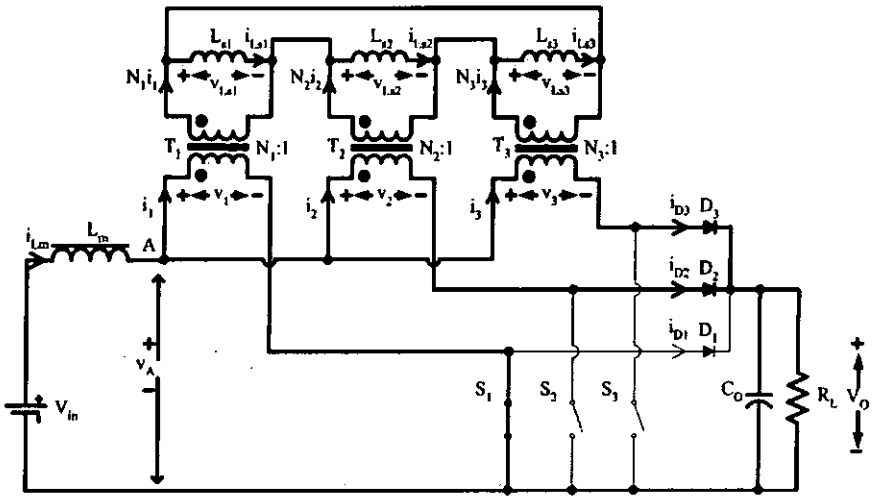


Fig. 5.5(a) Operation of the proposed converter: Stage 1 ($t_0 - t_1$).

Stage 1 ($t_0 - t_1$)(The working condition is shown in Fig. 5.5(a).): It is assumed that, before t_0, the current i_{D1} has been reduced to zero. At $t = t_0$, switch S_1 is turned on. The reverse voltage across D_1 equals the output voltage V_O. Rectifiers D_2 and D_3 are forward biased by inductive currents i_2 and i_3, respectively. The voltage across the primary of T_1 is v_A. The voltages across the primaries of T_2 and T_3 are both equal to ($v_A - V_O$). From the Appendix, v_A at this stage can be found as

$$v_A = \frac{2}{3} V_O \tag{5-1}$$

The current i_{Lm} (the sum of i_1, i_2, and i_3) will increase at the rate of

$$\frac{di_{Lm}}{dt} = \frac{V_{in} - v_A}{L_m} = \frac{V_{in} - 2V_O/3}{L_m} \tag{5-2}$$

i_1 will increase at the rate of (detailed derivation given in Appendix)

$$\frac{di_1}{dt} = \frac{1}{3}\left(\frac{V_{in} - 2V_O/3}{L_m} + \frac{2V_O}{L}\right) \tag{5-3}$$

Both i_2 and i_3 will decrease at the rate of

$$\frac{di_2}{dt} = \frac{di_3}{dt} = -\frac{1}{3}\left(-\frac{V_{in} - 2V_O/3}{L_m} + \frac{V_O}{L}\right) \qquad (5\text{-}4)$$

It should be noted that since the output current is shared by i_2 and i_3 at this stage, i_2 actually drops from relatively low amplitude. It means that the forward current before the rectifier turn-off is quite small.

This stage ends when i_2 drops to zero, which helps to reduce the reverse-recovery problem in later stages.

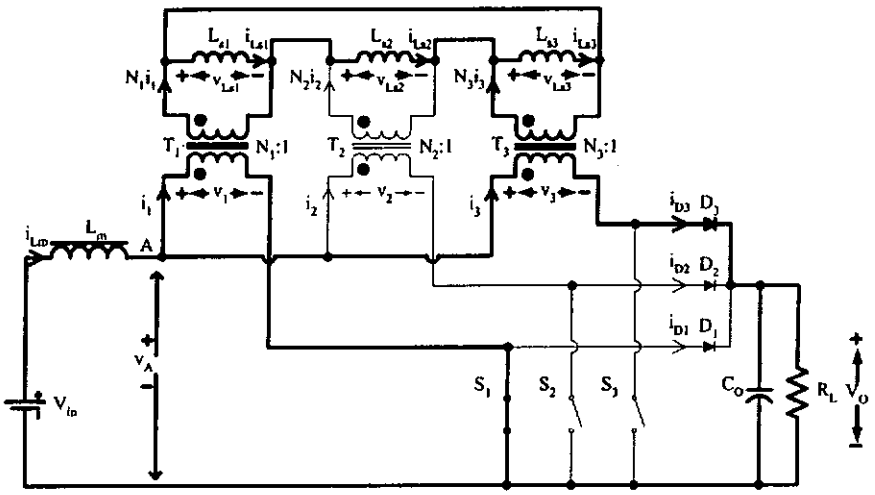


Fig. 5.5(b) Operation of the proposed converter: Stage 2 ($t_1 - t_2$).

Stage 2 ($t_1 - t_2$)(The working condition is shown in Fig. 5.5(b).): Since i_2 is zero, D_2 recovers to the blocking state naturally. The drain to source voltage of switch S_2 will have a slight damped oscillation due to the resonant tank formed by the parasitic capacitor of D_2 and the integrated inductors. v_A at this stage changes to

$$v_A = \frac{LV_{in} + 3L_m V_O}{L + 6L_m} \qquad (5\text{-}5)$$

The reverse voltage across D_2 can be found as

$$\text{Reverse voltage of } D_2 = (V_O - v_A) - (2v_A - V_O) = \frac{2LV_O - 3LV_{in} + 3L_m V_O}{L + 6L_m} \quad (5\text{-}6)$$

Since $L << L_m$, the reverse voltage applied to the rectifier D_2 during its turn-off is much smaller than the output voltage V_O. This would also help to reduce the reverse-recovery loss.

i_1 will increase at the rate of

$$\frac{di_1}{dt} = \frac{3LV_{in} - LV_O + 3L_m V_O}{L(L + 6L_m)} \quad (5\text{-}7)$$

i_3 will decrease at the rate of

$$\frac{di_3}{dt} = -\frac{2LV_O - 3LV_{in} + 3L_m V_O}{L(L + 6L_m)} \quad (5\text{-}8)$$

i_{Lm} (the sum of i_1 and i_3) will increase at the rate of

$$\frac{di_{Lm}}{dt} = \frac{d(i_1 + i_3)}{dt} = \frac{6V_{in} - 3V_O}{L + 6L_m} \quad (5\text{-}9)$$

Stage 3 ($t_2 - t_3$)(The working condition is shown in Fig. 5.5(c).): At the time $t = t_2$, switch S_1 is turned off. The current that flows through S_1 is delivered to charge up the output capacitor of S_1. Then D_1 is forward-biased and begins to conduct. At this stage, v_A is found as

$$v_A = \frac{LV_{in} + 6L_m V_O}{L + 6L_m} \quad (5\text{-}10)$$

The reverse voltage of D_2 is

$$\text{Reverse voltage of } D_2 = (V_O - v_A) - 2(v_A - V_O) = \frac{3L(V_O - V_{in})}{L + 6L_m} \quad (5\text{-}11)$$

Both i_1 and i_3 will decrease at the rate of

$$\frac{di_1}{dt} = \frac{di_3}{dt} = -\frac{3(V_O - V_{in})}{L + 6L_m} \tag{5-12}$$

i_{Lm} (the sum of i_1 and i_3) will decrease at the rate of

$$\frac{di_{Lm}}{dt} = \frac{d(i_1 + i_3)}{dt} = -\frac{6(V_O - V_{in})}{L + 6L_m} \tag{5-13}$$

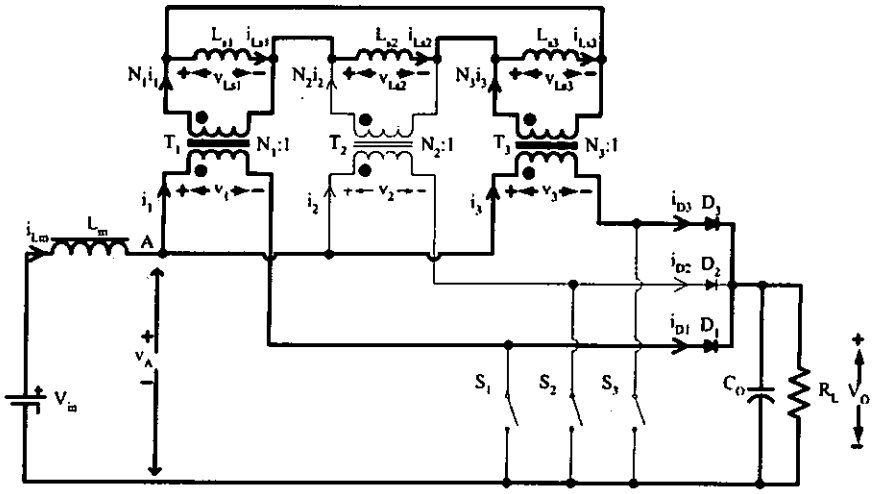


Fig. 5.5(c) Operation of the proposed converter: Stage 3 ($t_2 - t_3$).

Stage 4 ($t_3 - t_4$)(The working condition is shown in Fig. 5.5(d).): At $t = t_3$, switch S_2 is turned on. The reverse voltage across D_2 equals the output voltage V_O. v_2 is equal to v_A and both v_1 and v_3 are equal to ($v_A - V_O$). At this stage, v_A changes back to $\frac{2V_O}{3}$, so the increasing rate of i_{Lm} is the same as equation (5-2). Both i_1 and i_3 will decrease at the rate of

$$\frac{di_1}{dt} = \frac{di_3}{dt} = -\frac{1}{3}\left(-\frac{V_{in} - 2V_O/3}{L_m} + \frac{V_O}{L}\right) \tag{5-14}$$

i_2 starts to increase at the rate of

$$\frac{di_2}{dt} = \frac{1}{3}\left(\frac{V_{in} - 2V_O/3}{L_m} + \frac{2V_O}{L}\right) \tag{5-15}$$

This stage ends when i_3 drops to zero.

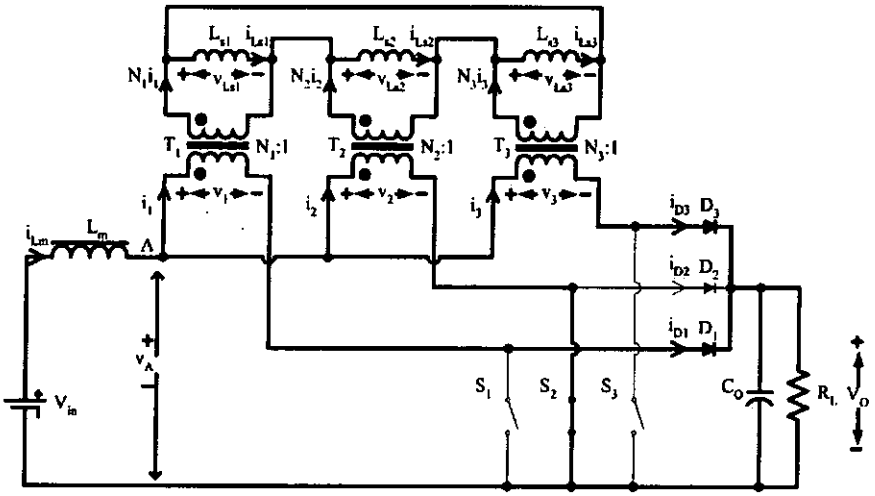


Fig. 5.5(d) Operation of the proposed converter: Stage 4 ($t_3 - t_4$).

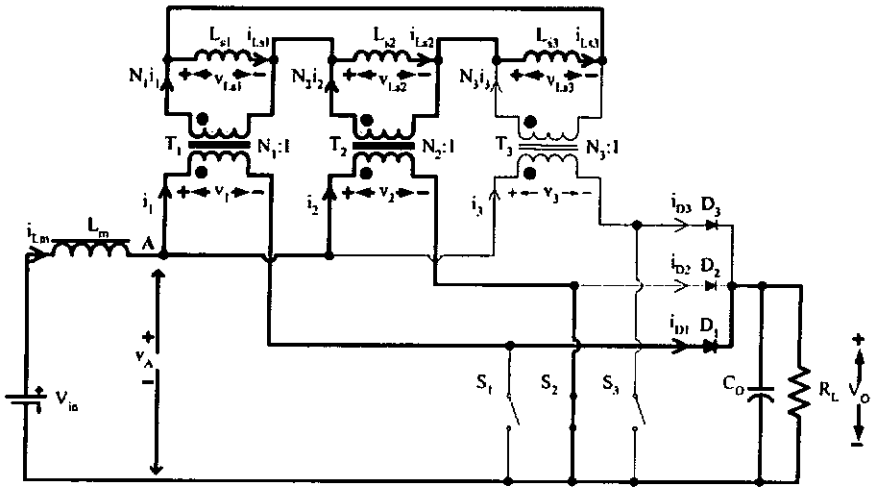


Fig. 5.5(e) Operation of the proposed converter: Stage 5 ($t_4 - t_5$).

Stage 5 ($t_4 - t_5$)(The working condition is shown in Fig. 5.5(e).): Since i_3 is zero, D_3 recovers to the blocking state naturally. The drain to source voltage of switch S_3 will have a slight damped oscillation due to the resonant tank formed by the parasitic capacitor of D_3 and the integrated

inductors. At this stage v_A and the reverse voltage across D_3 are the same as (5-5) and (5-6), respectively. i_1 will decrease at rate of

$$\frac{di_1}{dt} = -\frac{2LV_O - 3LV_{in} + 3L_m V_O}{L(L+6L_m)} \tag{5-16}$$

i_2 will continue to increase at the rate of

$$\frac{di_2}{dt} = \frac{3LV_{in} - LV_O + 3L_m V_O}{L(L+6L_m)} \tag{5-17}$$

The increasing rate of i_{Lm} (the sum of i_1 and i_2) is the same as (5-9).

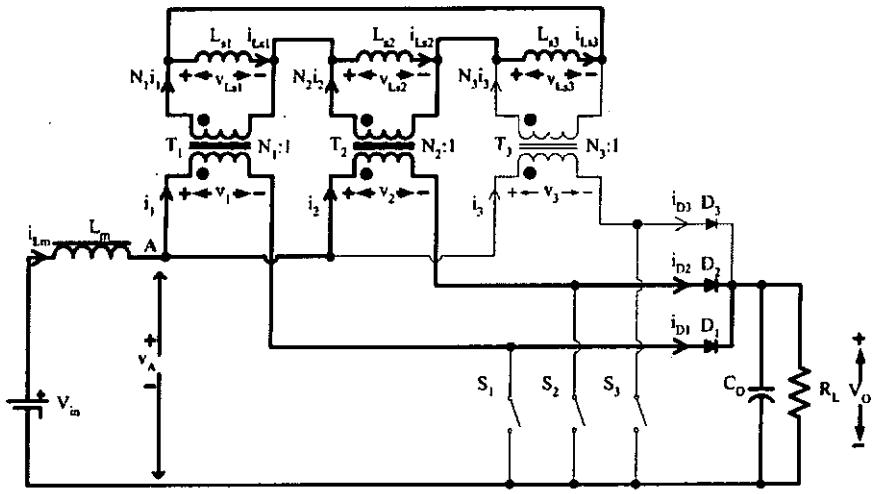


Fig. 5.5(f) Operation of the proposed converter: Stage 6 ($t_5 - t_6$).

Stage 6 ($t_5 - t_6$)(The working condition is shown in Fig. 5.5(f).): At the time $t = t_5$, switch S_2 is turned off. The output capacitor of S_2 is charged up by i_2 and then rectifier D_2 begins to conduct. The expressions of v_A and the reverse voltage across D_3 are the same as (5-10) and (5-11), respectively. Both i_1 and i_2 will decrease at the rate of

$$\frac{di_1}{dt} = \frac{di_2}{dt} = -\frac{3(V_O - V_{in})}{L+6L_m} \tag{5-18}$$

The decreasing rate of i_{Lm} (the sum of i_1 and i_2) is the same as (5-13).

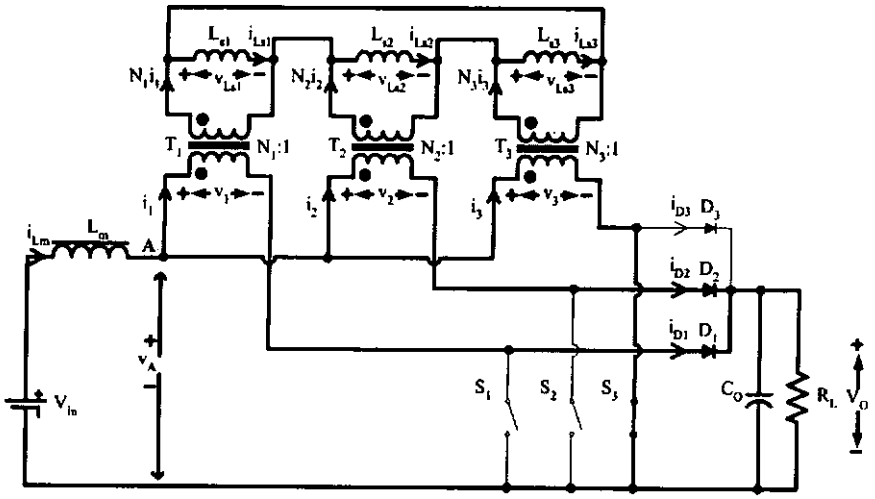


Fig. 5.5(g) Operation of the proposed converter: Stage 7 ($t_6 - t_7$).

Stage 7 ($t_6 - t_7$)(The working condition is shown in Fig. 5.5(g).): At $t = t_6$, switch S_3 is turned on. The reverse voltage across D_3 equals the output voltage V_O. v_3 is equal to v_A and both v_1 and v_2 are equal to ($v_A - V_O$). At this stage, v_A changes back to $\frac{2V_O}{3}$, so the increasing rate of i_{Lm} is the same as equation (5-2). Both i_1 and i_2 will decrease at the rate of

$$\frac{di_1}{dt} = \frac{di_2}{dt} = -\frac{1}{3}\left(-\frac{V_{in} - 2V_O/3}{L_m} + \frac{V_O}{L}\right) \qquad (5\text{-}19)$$

i_3 starts to increase at the rate of

$$\frac{di_3}{dt} = \frac{1}{3}\left(\frac{V_{in} - 2V_O/3}{L_m} + \frac{2V_O}{L}\right) \qquad (5\text{-}20)$$

This stage ends when i_1 drops to zero.

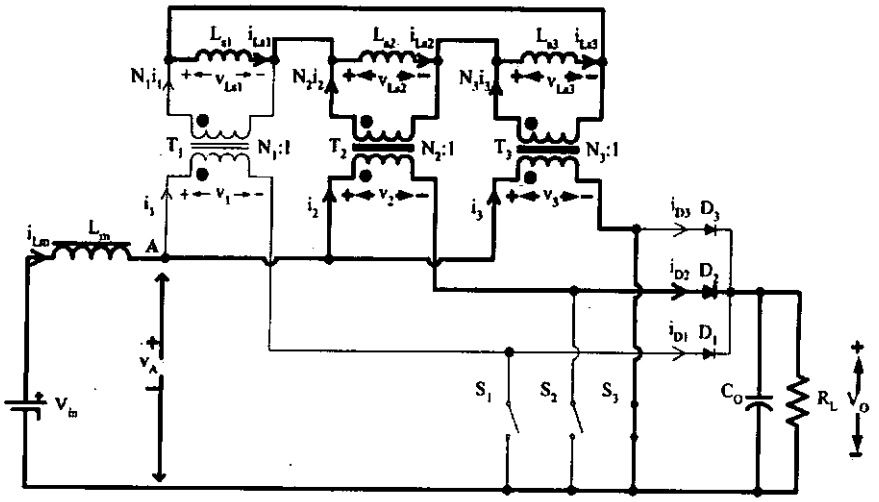


Fig. 5.5(h) Operation of the proposed converter: Stage 8 ($t_7 - t_8$).

Stage 8 ($t_7 - t_8$)(The working condition is shown in Fig. 5.5(h).): Since i_1 is zero, D_1 recovers to the blocking state naturally. The drain to source voltage of switch S_1 will have a slight damped oscillation due to the resonant tank formed by the parasitic capacitor of D_1 and the integrated inductors. At this stage v_A and the reverse voltage across D_1 are the same as (5-5) and (5-6), respectively. i_2 will decrease at rate of

$$\frac{di_2}{dt} = -\frac{2LV_O - 3LV_{in} + 3L_mV_O}{L(L+6L_m)} \tag{5-21}$$

i_3 will continue to increase at the rate of

$$\frac{di_3}{dt} = \frac{3LV_{in} - LV_O + 3L_mV_O}{L(L+6L_m)} \tag{5-22}$$

The increasing rate of i_{Lm} (the sum of i_2 and i_3) is the same as (5-9).

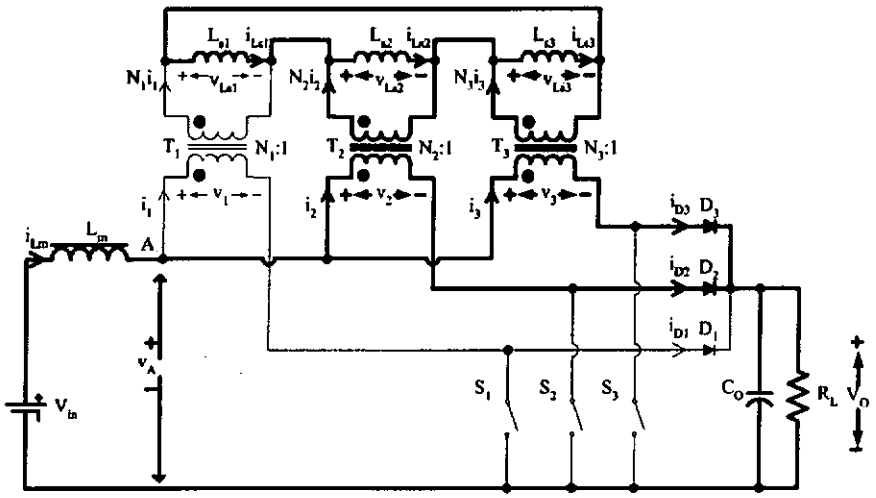


Fig. 5.5(i) Operation of the proposed converter: Stage 9 ($t_8 - t_9$).

Stage 9 ($t_8 - t_9$)(The working condition is shown in Fig. 5.5(i).): At the time $t = t_8$, switch S_3 is turned off. The output capacitor of S_3 is charged up by i_3 and then rectifier D_3 begins to conduct. The expressions of v_A and the reverse voltage across D_1 are the same as (5-10) and (5-11), respectively. Both i_2 and i_3 will decrease at the rate of

$$\frac{di_2}{dt} = \frac{di_3}{dt} = -\frac{3(V_O - V_{in})}{L + 6L_m} \tag{5-23}$$

The decreasing rate of i_{Lm} (the sum of i_2 and i_3) is the same as (5-13).

Once the switch S_1 is turned on again, the above operation stages will repeat. From the current waveforms shown in Fig. 5.4, it can be seen that the current of each output rectifier decreases in steps and finally reduces to zero before the switch in the same channel is turned on. Although the inductor current in each channel is discontinuous, the overall input current, i_{Lm}, is continuous and smooth.

5.3 Design Considerations

To facilitate the design of the proposed converter, the selection of the number of turns of the integrated inductors, the determination of inductance L_m, and the expression of output voltage V_O will be discussed in this section. A design example will also be given to illustrate the design procedure. Before the discussion, two parameters should first be defined:

$$M = \frac{V_O}{V_{in}} \tag{5-24}$$

$$r_L = \frac{L}{L_m} \tag{5-25}$$

M refers to the voltage conversion ratio and r_L is a design parameter.

5.3.1 Relationship between Duty Cycle D, r_L, and Voltage Conversion Ratio M

From the waveform of i_{Lm} in Fig. 5.4, it can be seen that the net change of i_{Lm} in each one third of the switching cycle is equal to zero. Therefore, from equations (5-2), (5-9), (5-13), (5-24), (5-25), and Fig. 5.6 we have

$$\frac{V_{in} - 2V_O/3}{L_m} \cdot \beta T_S + \frac{6V_{in} - 3V_O}{L + 6L_m} \cdot (D - \beta) T_S + \left[-\frac{6(V_O - V_{in})}{L + 6L_m} \right] \cdot (\frac{1}{3} - D) T_S = 0$$

$$(r_L - \frac{2}{3} r_L M - M)\beta + 3MD = 2(M - 1) \tag{5-26}$$

where T_s is the switching period, D is the duty cycle, and β is the ratio of the time period, starting at the turn-on of the switches and ending when the inductor currents are discharged to zero, to the switching cycle, as shown in Fig. 5.4.

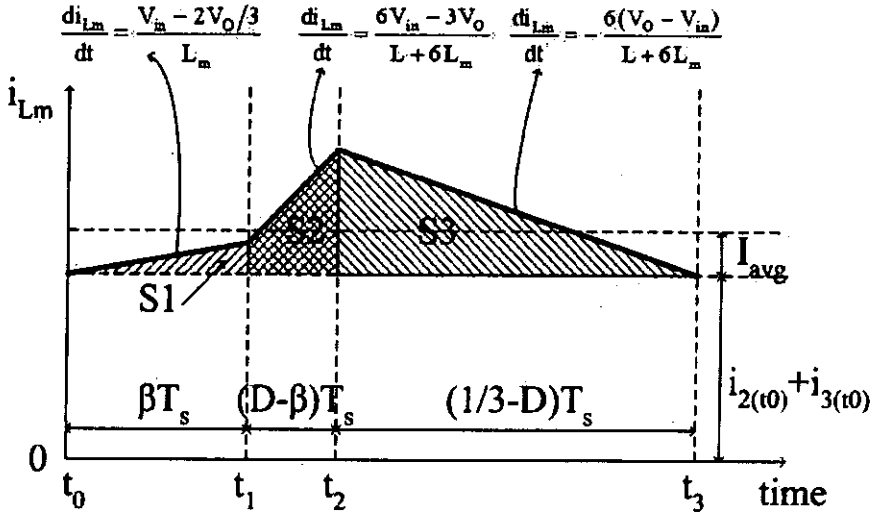


Fig. 5.6 Waveform of input current i_{Lm} in one third of the switching cycle.

It should be noted that, in order to make sure that the current of an output rectifier will be reduced to zero before the switch in the same channel is turned on, we need to have

$$\beta \le D \tag{5-27}$$

With the aim to better utilize the output rectifiers and to make the design simpler, we can choose

$$\beta = D \tag{5-28}$$

Substituting (5-28) into (5-26), we have

$$D = \frac{2M - 2}{r_L - 2r_L M/3 + 2M} \tag{5-29}$$

Fig. 5.7 shows the relationship between D and r_L under different values of M. From Fig. 5.7 it can be seen that the steady-state duty cycle D increases as the voltage conversion ratio M increases. For the same M, duty cycle D will slightly decrease as r_L changes from zero to one.

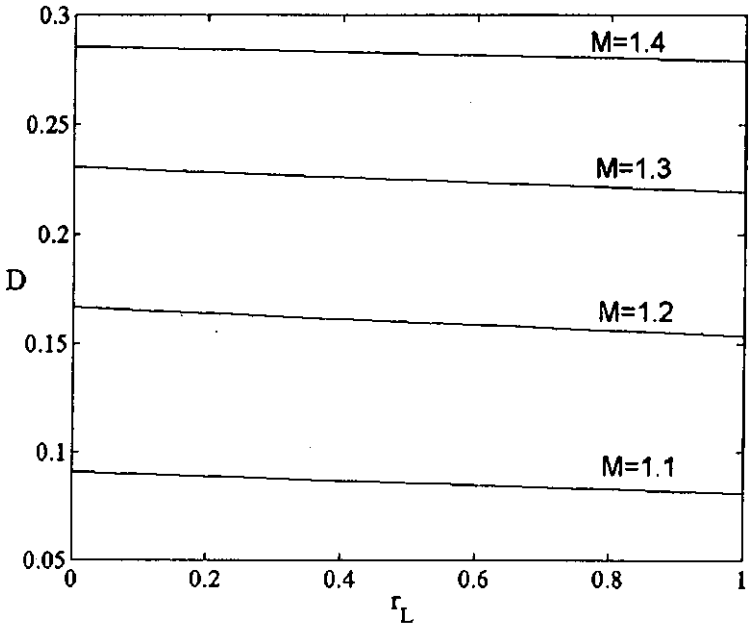


Fig. 5.7 Duty cycle D as a function of r_L under different M.

5.3.2 Limitation of r_L

In order to make the converter more cost effective and to achieve a smaller size, r_L should be chosen as small as possible. From the view of efficiency, since the inductor current in each channel is discontinuous, a smaller r_L will lead to smaller copper loss. However, if r_L is chosen too small, there is a tendency for all the rectifiers to conduct simultaneously at **Stage 3**, **6**, and **9** (Fig. 5.5(c), (f), and (i)). In order to prevent this from happening, the conducting two inductors should have a sufficiently large back EMF to reverse bias output rectifier connected to the third inductor. Consider **Stage 3** (Fig. 5.5(c)) as an example. Assuming that the forward voltage drop of the rectifier is V_F, v_A at this stage should be changed from (5-10) to

$$v_A = \frac{LV_{in} + 6L_m(V_O + V_F)}{L + 6L_m} \tag{5-30}$$

Therefore, the reverse voltage of D_2 is also changed from (5-11) to

$$\begin{aligned} \text{Reverse Voltage of } D_2 &= (V_O - v_A) - 2(v_A - V_O - V_F) \\ &= \frac{3L(V_O - V_{in}) - 18L_m V_F}{L + 6L_m} + 2V_F \end{aligned} \tag{5-31}$$

The value of equation (5-31) should be greater than or equal to one volt. Substituting (5-25) into (5-31), we have

$$\begin{aligned} \frac{3r_L(V_O - V_{in}) - 18V_F}{r_L + 6} + 2V_F &\geq 1 \\ r_L &\geq \frac{6 + 6V_F}{2V_F - 1 + 3(V_O - V_{in})} \end{aligned} \tag{5-32}$$

By assuming V_F = 1V, equation (5-32) is plotted in Fig. 5.8. Here r_L should be chosen from the shaded area in order to prevent the situation of all rectifiers conducting simultaneously. From Fig. 5.8, it can be seen that r_L can be less than 0.21 when $(V_O - V_{in}) \geq 20V$.

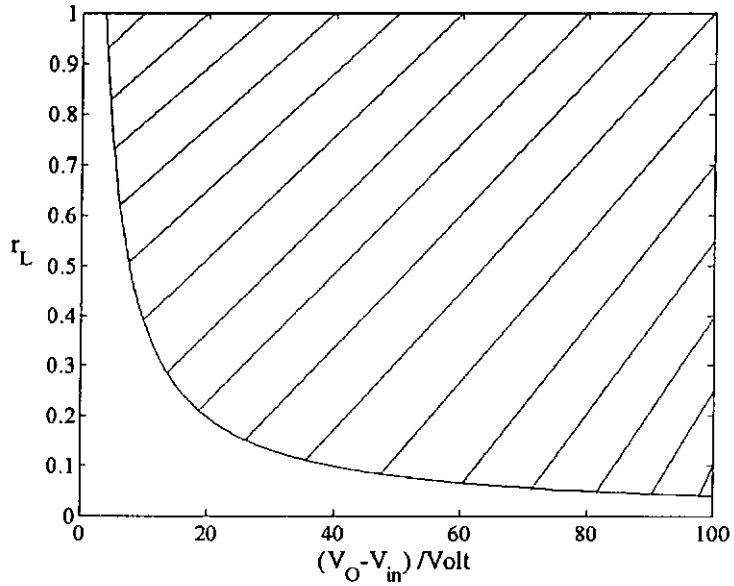


Fig. 5.8 r_L as a function of $(V_O - V_{in})$.

5.3.3 Determination of Inductance L_m

L_m can be determined by the balance of the input power and the output power of the converter. The average input inductor current, $I_{Lm,avg}$, should be found first. From Fig. 5.6, we have

$$I_{Lm,avg} = I_{avg} + i_{2(t0)} + i_{3(t0)} \tag{5-33}$$

where $i_{2(t0)}$ and $i_{3(t0)}$ are the values of i_2 and i_3 at the time $t = t_0$, respectively.

I_{avg} can be derived as follows:

$$\begin{aligned} I_{avg} &= \frac{S1+S2+S3}{\frac{T_S}{3}} \\ &= \frac{3}{T_S}\left\{\begin{aligned} &\frac{1}{2}(D-\beta)T_S\cdot\left[\frac{V_{in}-2V_O/3}{L_m}\beta T_S+\frac{6(V_O-V_{in})}{L+6L_m}(\frac{1}{3}-D)T_S\right] \\ &+\frac{6(V_O-V_{in})}{2(L+6L_m)}(\frac{1}{3}-D)^2T_S^{\,2}+\frac{V_{in}-2V_O/3}{2L_m}(\beta T_S)^2 \end{aligned}\right\} \end{aligned} \tag{5-34}$$

where S1, S2, and S3 refer to the shaded area in Fig. 5.6.

$i_{2(t0)}$ can be found from (5-4):

$$i_{2(t0)} = \frac{1}{3}(-\frac{V_{in}-2V_O/3}{L_m}+\frac{V_O}{L})\cdot\beta T_S \tag{5-35}$$

$i_{3(t0)}$ can be found from (5-4), (5-8), (5-12), and (5-14):

$$\begin{aligned} i_{3(t0)} = &\frac{1}{3}(-\frac{V_{in}-2V_O/3}{L_m}+\frac{V_O}{L})\beta T_S+\frac{2LV_O-3LV_{in}+3L_mV_O}{L(L+6L_m)}(D-\beta)T_S \\ &+\frac{3(V_O-V_{in})}{L+6L_m}(\frac{1}{3}-D)T_S+\frac{1}{3}(-\frac{V_{in}-2V_O/3}{L_m}+\frac{V_O}{L})\beta T_S \end{aligned} \tag{5-36}$$

Assuming that the conversion efficiency of the converter is η, we have

$$\eta V_{in}\cdot I_{Lm,avg} = \frac{V_O^2}{R_L} \tag{5-37}$$

where R_L is the load resistance.

Substituting (5-24), (5-25), (5-33), (5-34), (5-35), and (5-36) into (5-37) and using the relationship shown in (5-26), we get

$$(3-2M)D\beta+\frac{6(M-1)}{6+r_L}(-1+3D)\beta+\frac{2M\beta}{r_L}+\frac{6-2M+6M/r_L}{6+r_L}(D-\beta)=\frac{\alpha\cdot M^2}{\eta\cdot\pi} \tag{5-38}$$

where $\alpha=\frac{2\pi\cdot L_m}{T_S\cdot R_L}$.

Combining (5-28) and (5-38) we have

$$\alpha=\frac{\eta\cdot\pi}{M^2}\left[(3-2M)D^2+\frac{6(M-1)}{6+r_L}(-1+3D)D+\frac{2MD}{r_L}\right] \tag{5-39}$$

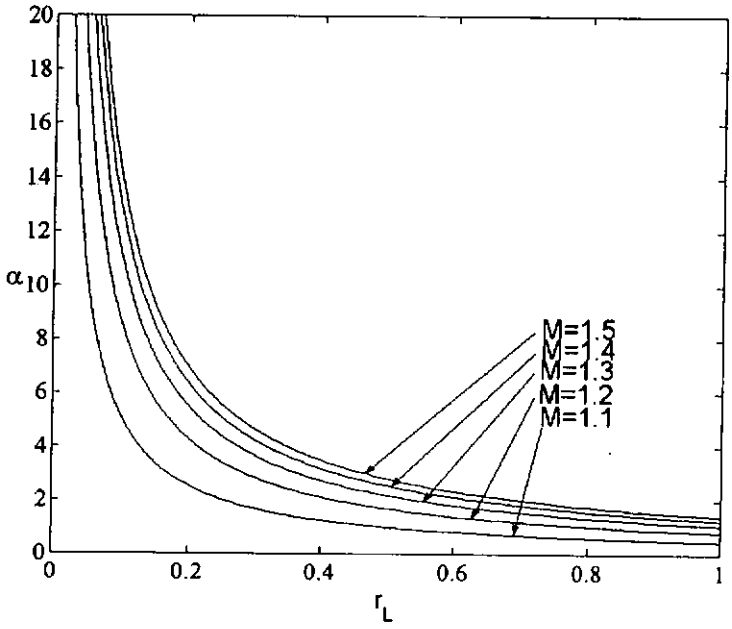


Fig. 5.9 α as a function of r_L under different M.

The relationships between α and r_L for different values of M are shown in Fig. 5.9. For a given r_L, a larger M means a larger α. If M is given, α will decrease as r_L increases. It should be noted that, as far as the efficiency and

the size of the converter are concerned, a smaller r_L would be better. However, a smaller r_L will need a larger α, which in turn will need a larger inductance L_m for the same $(T_S \cdot R_L)$. Although a larger L_m would help to reduce the ripples of input current, the size and the weight of inductor L_m maybe unacceptable. Therefore, on the selection of r_L, a trade-off should be made.

5.3.4 Expression of Output Voltage V_O

From (5-39) we can find the expression of the output voltage V_O. Equation (5-39) can be changed to:

$$\frac{\alpha M^2}{\pi}+\eta\cdot\left[2D^2-\frac{6(-1+3D)D}{6+r_L}-\frac{2D}{r_L}\right]\cdot M+\eta\cdot\left[\frac{6(-1+3D)D}{6+r_L}-3D^2\right]=0 \tag{5-40}$$

Then M is found as

$$M=\frac{-\eta\cdot\pi\cdot\left[2D^2-\frac{6(-1+3D)D}{6+r_L}-\frac{2D}{r_L}\right]+\sqrt{\eta^2\left[2D^2-\frac{6(-1+3D)D}{6+r_L}-\frac{2D}{r_L}\right]^2-\frac{4\alpha}{\pi}\left[\frac{6(-1+3D)D}{6+r_L}-3D^2\right]}}{2\alpha} \tag{5-41}$$

It should be noted that (5-41) is valid only when α is sufficiently small (that is, the load resistance R_L is sufficiently large) to make $M \geq 1$ for a boost converter. The condition is provided in (5-42).

$$\alpha \leq 2\pi\cdot\eta D\left(\frac{D}{2}+\frac{1}{r_L}\right) \tag{5-42.A}$$

Or

$$R_L \geq \frac{L_m}{\eta T_S D(\frac{D}{2}+\frac{1}{r_L})} \qquad (5\text{-}42.B)$$

If α is larger than the value given by (5-42.A) (or R_L is smaller than the value given by (5-42.B)), the inductor current in each channel will become continuous and the feature of zero reverse-recovery loss will be lost.

5.3.5 Design Example

Based on the analysis above, a simplified design example will be presented here to illustrate the design procedure. Suppose the input voltage of the converter $V_{in} = 100$ V and the output voltage $V_O = 120$ V. Output power $P_O = 236$ W ~ 600 W ($R_L = 61\ \Omega \sim 24\ \Omega$). The minimum switching frequency $f_{s,min} = 59$ kHz ($T_{s,max} = 17$ us).

From equation (5-24), we have

$$M = \frac{120}{100} = 1.2 \qquad (5\text{-}43)$$

Because the value of ($V_O - V_{in}$) is equal to 20 V, from Fig. 5.8 we can find $r_L \geq 0.21$. Here, the minimum value of r_L is chosen so $r_L = 0.21$. Therefore, the steady-state duty cycle $D = 0.164$ can be determined from Fig. 5.7. The corresponding value of α can be determined as $\alpha = 4.1$ from Fig. 5.9.

According to equations (5-29) and (5-39), the duty cycle is insensitive to load change while the switching frequency will vary according to the load change. The switching frequency will become minimum when the loading is maximum and the switching frequency will become maximum when the

loading is minimum. According to the definition of K, inductance L_m can be found

$$L_m = \alpha \cdot T_{s,max} R_{L,min} /(2\pi) = 265\ \text{uH} \tag{5-44}$$

The maximum switching frequency

$$f_{s,max} = f_{s,min} \cdot \frac{R_{L,max}}{R_{L,min}} = 150\ \text{kHz} \tag{5-45}$$

Assuming permeance $L_{s1} = L_{s2} = L_{s3} = 555\ \text{nH}$, the number of turns of integrated inductors is

$$N_1 = N_2 = N_3 = \sqrt{\frac{r_L \cdot L_m}{L_{s1}}} \approx 10 \tag{5-46}$$

Now, we can find the decreasing rate of the output rectifier current. As shown before, the current decreasing rate of the output rectifiers is governed by (5-4). Therefore, based on the data above, the decreasing rate of the output rectifier current can be calculated as 0.69 A/us. It can be seen that all the rectifiers are softly turned off and the reverse-recovery problem can be eliminated.

It should be noted that if the output power is below the design range (below 236 W), one could either increase the switching frequency or vary the duty cycle while keeping the switch frequency to regulate the output voltage. In the latter case, the output rectifier current will drop to zero earlier than in the optimal operation. The output rectifiers will be worse utilized but the reverse-recovery loss is still eliminated since switches are turned on under zero output rectifier currents. The conversion efficiency may drop a little bit for lower output power.

5.4 Simulation and Experimental Results

In this section, the proposed converter is evaluated by PSpice simulation with practical component values and experimental work. Similar to the design example, the converter was designed to have the following parameters:

(1) Input voltage: $V_{in} = 100\ V$;

(2) Output voltage: $V_O = 120\ V$;

(3) Output power: $P_O = 236\ W \sim 600\ W$;

(4) Switching frequency: $f_s = 59\ kHz \sim 150\ kHz$;

(5) Inductor $L_m = 265\ uH$;

(6) Switch S_1, S_2, and S_3: NTP15N40;

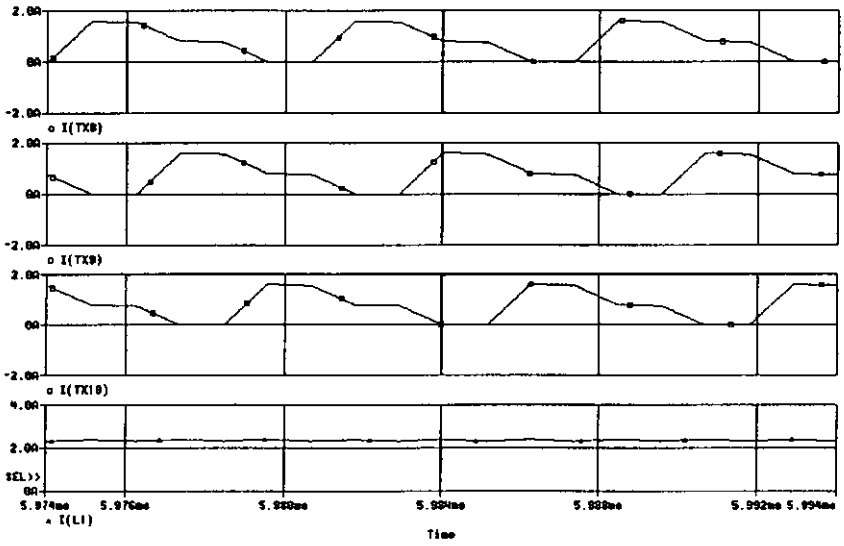
(7) Output rectifiers D_1, D_2, and D_3: MUR 820;

(8) Output capacitor $C_O = 2 \times 470\ uF / 200\ V$;

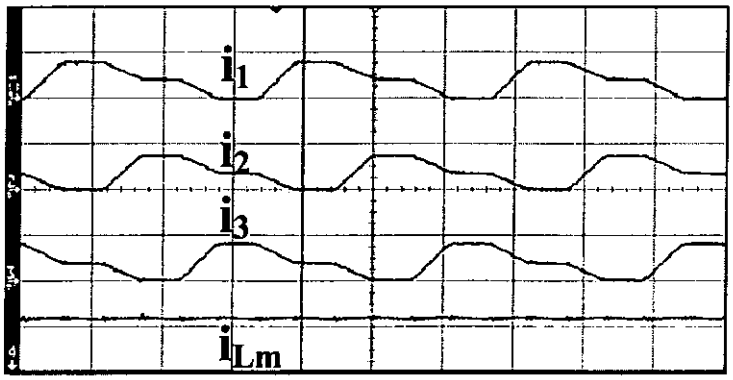
(9) Inversely-coupled integrated inductors:

Core: Planar OK43618; Turns of windings (N): 10 turns of #38 AWG × 64; Gap1: 0.2 mm; Gap2: 0.42 mm; Gap3: 0.2 mm; $L_1 = L_2 = L_3 = 555$ nH.

The results of simulation, using the equivalent-circuit model shown in Fig. 5.2(c), are presented in Fig. 5.10(a), Fig. 5.11(a), Fig. 5.12(a), and Fig. 5.13(a). The experimental waveforms are shown in Fig. 5.10(b), Fig. 5.11(b), Fig. 5.12(b), and Fig. 5.13(b). It can be seen that they agree well with each other.

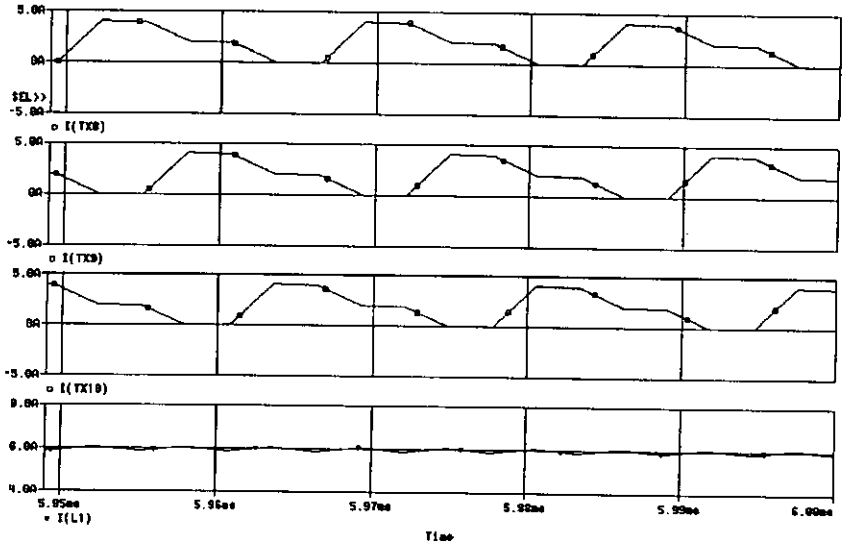


(a) Simulation waveforms (From top to bottom: i_1, i_2, i_3, and i_{Lm}).

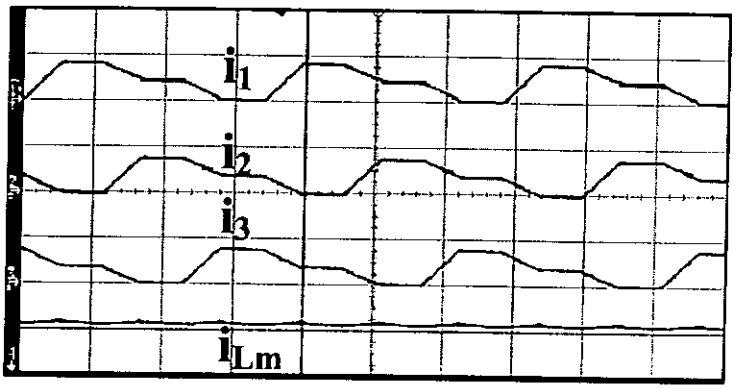


(b) Experimental waveforms (From top to bottom: i_1, 2A/div; i_2, 2A/div; i_3, 2A/div; i_{Lm}, 2A/div. Time base: 2μs/div).

Fig. 5.10 Simulation and experimental inductor current waveforms when output power is 236W.

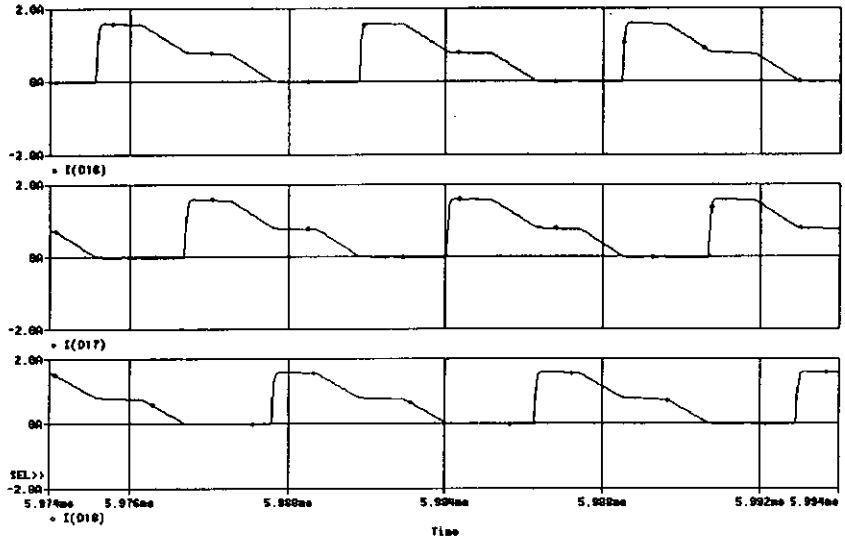


(a) Simulation waveforms (From top to bottom: i_1, i_2, i_3, and i_{Lm}).

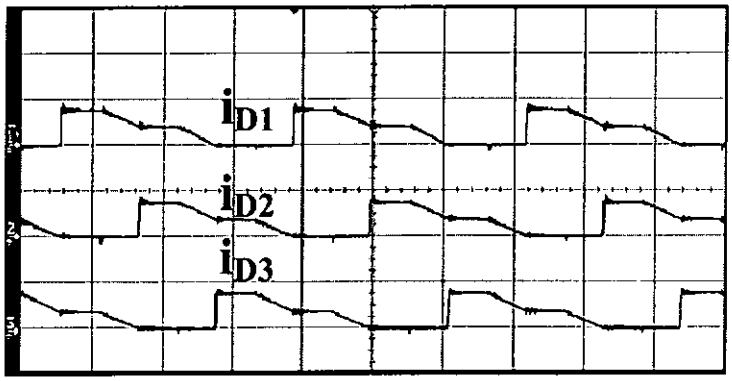


(b) Experimental waveforms (From top to bottom: i_1, 5A/div; i_2, 5A/div; i_3, 5A/div; i_{Lm}, 5A/div. Time base: 5μs/div).

Fig. 5.11 Simulation and experimental inductor current waveforms when output power is 600W.

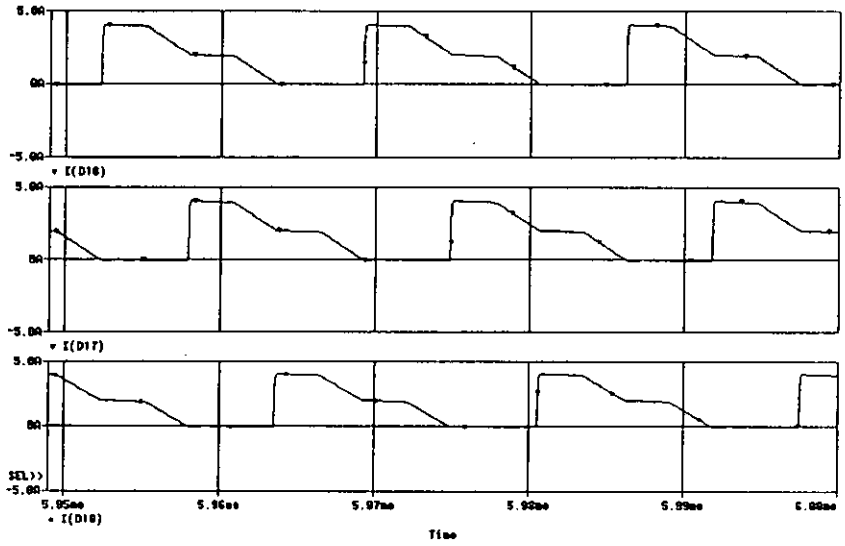


(a) Simulation waveforms (From top to bottom: i_{D1}, i_{D2}, and i_{D3}).

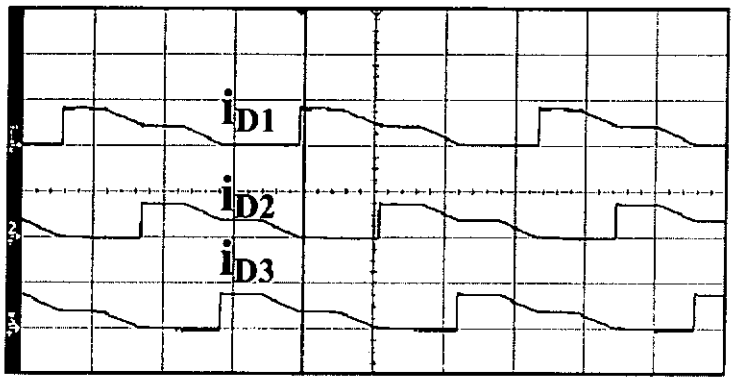


(b) Experimental waveforms (From top to bottom: i_{D1}, 2A/div; i_{D2}, 2A/div; i_{D3}, 2A/div. Time base: 2μs/div).

Fig. 5.12 Simulation and experimental output rectifier current waveforms when output power is 236W.

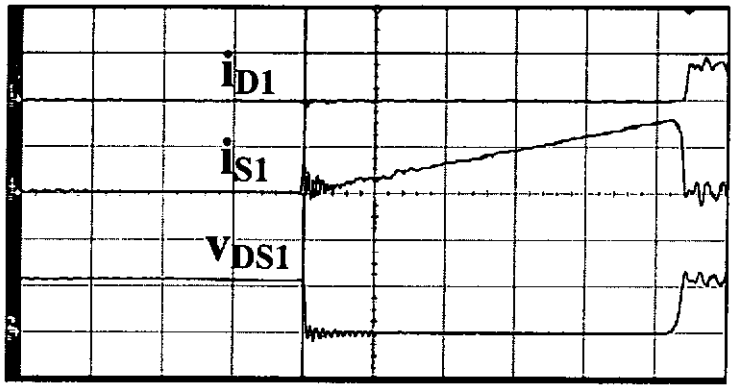


(a) Simulation waveforms (From top to bottom: i_{D1}, i_{D2}, and i_{D3}).

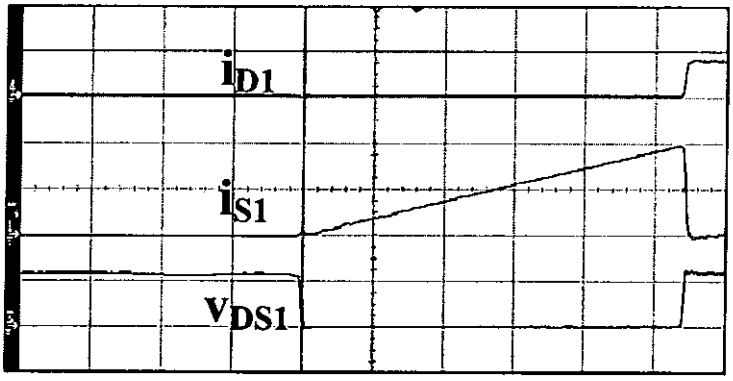


(b) Experimental waveforms (From top to bottom: i_{D1}, 5A/div; i_{D2}, 5A/div; i_{D3}, 5A/div. Time base: 5μs/div).

Fig. 5.13 Simulation and experimental output rectifier current waveforms when output power is 600W.



(a) Experimental waveforms (From top to bottom: i_{D1}, 2A/div; i_{S1}, 1A/div; v_{DS1}, 100V/div. Time base: 200ns/div).



(b) Experimental waveforms (From top to bottom: i_{D1}, 5A/div; i_{S1}, 2A/div; v_{DS1}, 100V/div. Time base: 500ns/div).

Fig. 5.14 Experimental waveforms ((a) output power: 236W; (b) output power: 600W).

From Fig. 5.10 and Fig. 5.11 we can find that although the current ripple in each single channel is large, the overall input current is continuous and very smooth. From Fig. 5.12 and Fig. 5.13 it can be seen that all the currents of output rectifiers are decreased in steps and finally reduced to zero before the corresponding switches are turned on. Fig. 5.14 shows the

detailed waveform of the rectifier current i_{D1} at the instant of S_1 turn-on. The current decreasing rate of output rectifier is controlled and no reverse recovery spikes appear in the current waveform of the rectifier at the turn-on instant of S_1. It proves that the reverse-recovery loss is eliminated. In addition, from Fig. 5.12 and Fig. 5.13 it can be seen that the output current is always shared by two output rectifiers. Therefore, the current stress of each channel is greatly reduced for the same power level. Fig. 5.15 shows the measured efficiency of the converter. It is found that the efficiency can be higher than 98.8% in a wide load range.

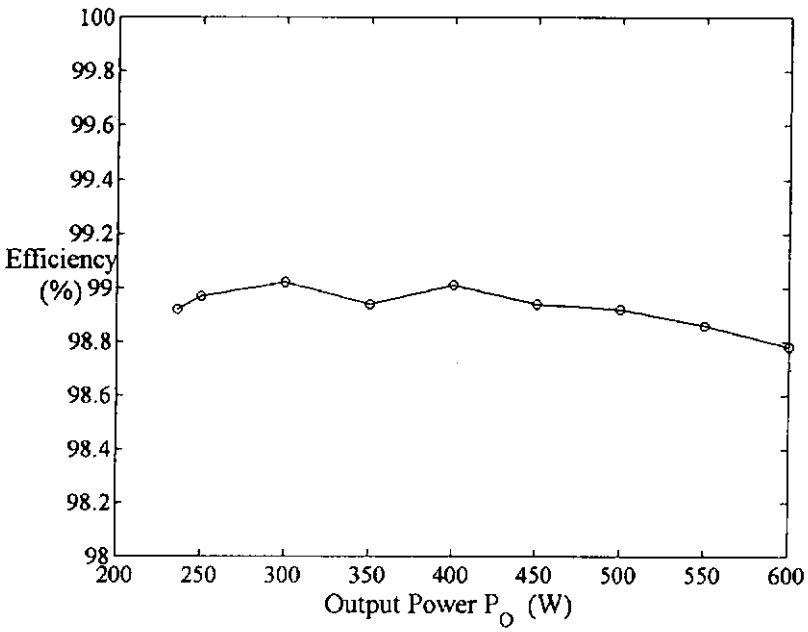


Fig. 5.15 Measured efficiency of the proposed converter for different output power.

5.5 Summary

A three-channel interleaved CCM boost converter using inversely-coupled integrated inductors is presented. The current of the output rectifiers

is decreased in steps and finally reduced to zero. The $\frac{di}{dt}$ of the rectifiers is controlled by the integrated inductors and all the rectifiers can be turned off softly. A very high efficiency is attained because the reverse-recovery loss is eliminated and the output power is shared among three channels. The winding arrangement of the inversely-coupled integrated inductors is discussed and the equivalent-circuit model is derived. The principle of operation of the converter and the design issues are also explained. The converter is verified by simulation and experimental setup and the results show good agreement with the theoretical predictions.

CHAPTER 6

CONCLUSIONS AND SUGGESTIONS FOR FUTURE RESEARCH

6.1 Conclusions

The harmonic reduction requirements imposed by regulatory agencies have accelerated interest in power factor corrected AC – DC rectifiers for switching mode power supplies. Passive power filters exhibit high efficiency and low cost, but they are very hard to optimize for universal line operation. In addition, they are bulky and heavy due to the size and weight of the inductors and capacitors. Therefore, passive approach is used only in low power and fixed line voltage applications. For higher power and universal line voltage applications, high switching frequency (typically over 30kHz) active techniques are used.

In this thesis, three novel converters are proposed. The first one is a single-switch high-power-factor regulator with near-zero output current ripple. The proposed converter employs a modified-boost converter as the input-current waveform shaper and a double-ended forward converter as the DC – DC converter. A clamping capacitor is utilized to clamp the voltage spike due to the transformer leakage inductance at the instant of turning off the switch. Zero output current ripple and high power factor are achieved. In this converter, integrated magnetics is utilized to reduce the number and the size of the magnetic components. The proposed converter will find

applications in low-cost low-power consumer products and it is especially suitable for low output voltage, high output current applications due to the feature of near zero output current ripple.

The second one is a two-channel interleaved boost converter with reduced core loss and copper loss. Each individual channel operates in CRM to eliminate the reverse-recovery problem. The overall input current is continuous and smooth, which will reduce the requirement for input filter. The existing inductor winding arrangement for two directly-coupled inductors is redesigned and a new winding arrangement is proposed. In the proposed structure, core loss can be reduced because the windings on the two outer legs are inversely coupled and as a result, the ripple of the AC flux in the center leg is greatly reduced. On the other hand, the proposed structure can increase the equivalent inductance of the coupled inductors so the practical inductors can be designed with smaller values. Since fewer turns are used, copper loss is reduced correspondingly. High power factors and efficiencies were attained in the experimental prototype. This circuit can be used as the front-end of high power PFC regulators.

The last one is a three-channel interleaved CCM boost converter with zero diode reverse-recovery loss. Three channels are used to further increase the power level. An inversely-coupled integrated inductor is utilized to control the decreasing rate of the rectifier current and as a result, all the rectifiers can be softly turned off. A very high efficiency is attained because the reverse-recovery loss is eliminated and the current stress for each channel is reduced. The overall input current is smooth although each channel operates in DCM, which will help to reduce the filtering

requirement. The circuit can be extended to any number of channels and is particularly suitable for large power applications.

The main contributions of this thesis can be summarized as follows:

- For low power applications (typically below 200 W), SSIPP is popular due to its low cost and simplicity. However, the voltage spike during the turn-off of the switch in a SSIPP will limit its applications. To solve this problem, costly or complex techniques should not be used. The single-switch high-power-factor regulator proposed in this thesis tackles this problem with the minimum components. At the same time, a good power factor and zero output current ripple can be achieved with the proposed converter.
- For large power applications, boost converters operating in CCM have been widely used because of lower input current ripple. However, CCM operation will present severe reverse-recovery problem, which will increase the losses in both the switch and the rectifier and generate EMI noise. From the experimental results in Chapter 4 and Chapter 5 it can be seen that, paralleling and interleaving two or more channels operating in DCM or CRM can be a good solution to eliminate the reverse-recovery problem while keeping the feature of low overall input current ripple.
- To further increase the power level, one can increase the number of channels for paralleling and interleaving. By doing so, the input and output current ripple can be further reduced and the conversion efficiency can be improved.

6.2 Suggestions for Future Research

A) Improve the PFC performance of a boost converter operating in DCM

As discussed in Chapter 2, a boost converter operating in DCM can achieve a relatively high power factor and low THD even without a current loop. However, considerable distortion still exists in the filtered line current, especially when the peak input voltage is close to the output voltage. Further distortion reduction can be attained by using frequency modulation [44][45][56] or by modifying pulse width modulation [51][85]. In the proposed converter in Chapter 3 and article [60], it is found that inserting a capacitor into the boost converter can help to improve the power factor due to the voltage offset of the capacitor. Therefore, further research can focus on the effect of such a modification of a conventional boost converter and on other possible structures that can help to improve the power factor without the need to change the control circuit.

B) Parallel operation for three-phase AC input

In this thesis, only a single-phase AC input is considered. For large power applications or three-phase AC input, single-phase rectifiers can be paralleled. Parallel operation can improve the reliability of the system by providing redundancy. Although each rectifier is corresponding to a single-phase input, the control circuit will be much more complicated. Current sharing scheme should be implemented to make sure that the loading current is shared equally between each phase. The system should be designed to allow further parallel operation of similar devices for future expansion.

APPENDIX

DERIVATION OF EQUATIONS FOR CHAPTER 5

The derivation of the voltage of point A (shown in Fig. 5.1), v_A and the rate of change of inductor currents will be carried out in this appendix.

Because the characteristic of interleaving, the first three stages of operation ($t_0 - t_3$ in Fig. 5.4) will be taken as an example. Equations in the other stages can be derived using the same method.

In order to simply the analysis, we assume that $N_1 = N_2 = N_3 = N$ and $L_{s1} = L_{s2} = L_{s3} = L_s$ in Fig. 5.2(c) and Fig. 5.5.

$t_0 - t_1$ (referring to Fig. 5.5(a)): Because switch S_1 is turned on and the output rectifiers D_2 and D_3 are forward-biased, we have

$$\begin{cases} v_1 = v_A \\ v_2 = v_3 = v_A - V_O \end{cases} \tag{A1}$$

From Fig. 5.2(c) one gets

$$v_{Ls1} + v_{Ls2} + v_{Ls3} = 0 \tag{A2}$$

Then, we have

$$v_1/N + v_2/N + v_3/N = 0$$

$$v_A = \frac{2V_O}{3} \tag{A3}$$

It can also be seen from Fig. 5.2(c) that

$$N\Delta i_1 - \Delta i_{Ls1} = N\Delta i_2 - \Delta i_{Ls2} = N\Delta i_3 - \Delta i_{Ls3} \qquad (A4)$$

Because $\Delta i_{Ls1} = \frac{v_1}{NL_s}\Delta t$, $\Delta i_{Ls2} = \frac{v_2}{NL_s}\Delta t$, and $\Delta i_{Ls3} = \frac{v_3}{NL_s}\Delta t$, from (A1) ~ (A4), one gets

$$\Delta i_1 = \Delta i_2 + \frac{V_O}{N^2 L_s}\Delta t = \Delta i_3 + \frac{V_O}{N^2 L_s}\Delta t \qquad (A5)$$

Due to the fact that $\Delta i_{Lm} = \Delta i_1 + \Delta i_2 + \Delta i_3$, from (4.2) and (A5) one obtains

$$\frac{di_1}{dt} = \frac{\Delta i_1}{\Delta t} = \frac{1}{3}\left(\frac{V_{in} - 2V_O/3}{L_m} + \frac{2V_O}{N^2 L_s}\right) = \frac{1}{3}\left(\frac{V_{in} - 2V_O/3}{L_m} + \frac{2V_O}{L}\right) \quad (A6)$$

$$\frac{di_2}{dt} = \frac{di_3}{dt} = \frac{\Delta i_2}{\Delta t} = -\frac{1}{3}\left(-\frac{V_{in} - 2V_O/3}{L_m} + \frac{V_O}{N^2 L_s}\right) = -\frac{1}{3}\left(-\frac{V_{in} - 2V_O/3}{L_m} + \frac{V_O}{L}\right) \qquad (A7)$$

$t_1 - t_2$ (referring to Fig. 5.5(b)): In this stage, $i_2 = 0$ and we have

$$\begin{cases} v_1 = v_A \\ v_3 = v_A - V_O \end{cases} \qquad (A8)$$

From (A2) and (A8), v_2 can be found as follows,

$$v_2 = V_O - 2v_A \qquad (A9)$$

Combining (A4), (A8), and (A9) we have

$$\Delta i_1 = \frac{3v_A - V_O}{N^2 L_s}\Delta t \qquad (A10)$$

$$\Delta i_3 = -\frac{-3v_A + 2V_O}{N^2 L_s}\Delta t \qquad (A11)$$

Because the rate of change of inductor current i_{Lm} can be written as

$$\Delta i_{Lm} = \frac{V_{in} - v_A}{L_m}\Delta t \qquad (A12)$$

Substituting (A10) ~ (A12) into equation $\Delta i_{Lm} = \Delta i_1 + \Delta i_2 + \Delta i_3$, one gets

$$v_A = \frac{N^2 L_s V_{in} + 3L_m V_O}{N^2 L_s + 6L_m} = \frac{LV_{in} + 3L_m V_O}{L + 6L_m} \tag{A13}$$

Substituting (A13) into (A10), (A11), and (A12) respectively, the following expressions can be attained

$$\frac{di_1}{dt} = \frac{3LV_{in} - LV_O + 3L_m V_O}{L(L + 6L_m)} \tag{A14}$$

$$\frac{di_3}{dt} = -\frac{2LV_O - 3LV_{in} + 3L_m V_O}{L(L + 6L_m)} \tag{A15}$$

$$\frac{di_{Lm}}{dt} = \frac{d(i_1 + i_3)}{dt} = \frac{6V_{in} - 3V_O}{L + 6L_m} \tag{A16}$$

$t_2 - t_3$ (referring to Fig. 5.5(c)): In this stage the switch S_1 is turned off and output rectifiers D_1 and D_3 are conducting. Therefore,

$$\begin{cases} v_1 = v_A - V_O \\ v_3 = v_A - V_O \end{cases} \tag{A17}$$

From (A2) and (A17), we have

$$v_2 = 2(V_O - v_A) \tag{A18}$$

Combining (A4), (A17), and (A18) one gets

$$\Delta i_1 = \Delta i_3 = -\frac{3(V_O - v_A)}{N^2 L_s} \Delta t \tag{A19}$$

Substituting (A12) and (A19) into equation $\Delta i_{Lm} = \Delta i_1 + \Delta i_2 + \Delta i_3$, one has

$$v_A = \frac{N^2 L_s V_{in} + 6L_m V_O}{N^2 L_s + 6L_m} = \frac{LV_{in} + 6L_m V_O}{L + 6L_m} \tag{A20}$$

Substituting (A20) into (A19) and (A12) respectively, the following expressions can be attained

$$\frac{di_1}{dt} = \frac{di_3}{dt} = -\frac{3(V_O - V_{in})}{L + 6L_m} \qquad (A21)$$

$$\frac{di_{Lm}}{dt} = \frac{d(i_1 + i_3)}{dt} = -\frac{6(V_O - V_{in})}{L + 6L_m} \qquad (A22)$$

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