The Hong Kong Polytechnic University

Department of Electronic and Information Engineering

Design of Power Supplies for Fast Load Transients

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A thesis submitted in partial fulfilment of

the requirements for the degree of

Doctor of Philosophy

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Certificate of Originality

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Abstract

This thesis aims to provide effective methodologies for designing power supplies with fast dynamic response. A strategy for low-cost and high-efficiency design is to employ an auxiliary circuit which only operates for feeding fast load transients. The design and practical applications of some auxiliary circuits are discussed, along with a proposed classification of auxiliary circuits that provides guidelines for choosing the appropriate type of auxiliary circuits for a given application.

The main contributions of this thesis are summarized as follows:

Firstly, a general classification of auxiliary circuits is discussed on the basis of circuit configuration, control and load information. Based on the classification, design and application principles of auxiliary circuits are given for various practical scenarios and requirements.

Secondly, a low loss bi-directional buck-boost circuit is proposed to work as an auxiliary circuit which is connected at the output port of the main converter. As no extra power source is required, the circuit employs a reservoir capacitor to draw or release energy, aiming to eliminate output voltage fluctuations during load transients. The capacitor may have a non-zero net input power and its voltage may become uncontrolled after many cycles of charging and discharging. A method to regulate the energy storage level within a specific range is proposed. The prototype is constructed to validate the proposed design.

Thirdly, a scheme to realize an auxiliary circuit that can cope with the trend of load-informed power management is proposed. The unconstrained sensor band-

width and the simplification of the control algorithm are the advantages of this method. The effectiveness of this method depends on the precision of transient predictions. A strategy for tackling inaccurate predictions is also proposed. Two specific implementations are given, along with experimental verification.

Publications

Journal papers

- **Z. Shan**, S. C. Tan, C. K. Tse, "Transient mitigation of dc–dc converters for high output current slew rate applications," *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2377–2388, May 2013.

- **Z. Shan**, C. K. Tse, S. C. Tan, "Pre-energized auxiliary circuits for very fast transient loads: coping with load-informed power management for computer loads," *IEEE Transactions on Circuits and Systems—I*, to appear.

- **Z. Shan**, C. K. Tse, S. C. Tan, "Classification of auxiliary circuit schemes for feeding fast load transients in switching power supplies," *IEEE Transactions on Circuits and Systems—I*, to appear.

Conference papers

- **Z. Shan**, S. C. Tan, C. K. Tse, "Transient mitigation of dc–dc converters using an auxiliary switching circuit," *IEEE Energy Conversion Congress and Exposition*, (ECCE 2011), Phoenix, Arizona, USA, pp. 1259–1264, Sep. 2011.

- **Z. Shan**, P. T. Krein, C. K. Tse, S. C. Tan "Pre-energized compact auxiliary circuit to buffer loads from fast transients with the goal of managing

load-informed power," *IEEE Workshops on Control and Modeling of Power Electronics (COMPEL 2013)*, Salt Lake City, Utah, USA, 2013.

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Chapter 1

Introduction

1.1 Background and Motivation

A power supply is an indispensable part of many electronic appliances. The fundamental function of a power supply is to deliver energy to the load in a stable, precise and efficient way. Several decades ago, electronic appliances consist of almost only analog and linear components. Therefore, such appliances never demand high slew-rate current from the power supply.

Any variation in the load current is normally handled by the feedback control loop of the power supply. Current methods are capable to address low-frequency interference and keep the output voltage nearly constant. However, since the 1980s, development in the electronics industry has made significant and continuous progress in digital electronics where transistors are operating as switches. Sophisticated and well designed power supplies are needed to feed current with very high slew-rate to digital integrated circuits.

Over the past decades, the integration density of integrated circuits has increased following the Moore's law [1, 2], as shown in Fig. 1.1. Inside a multi-core microprocessor, billions of transistors may switch synchronously with the system clock up to several GHz. The slew rate of fast transients generated by a mod-

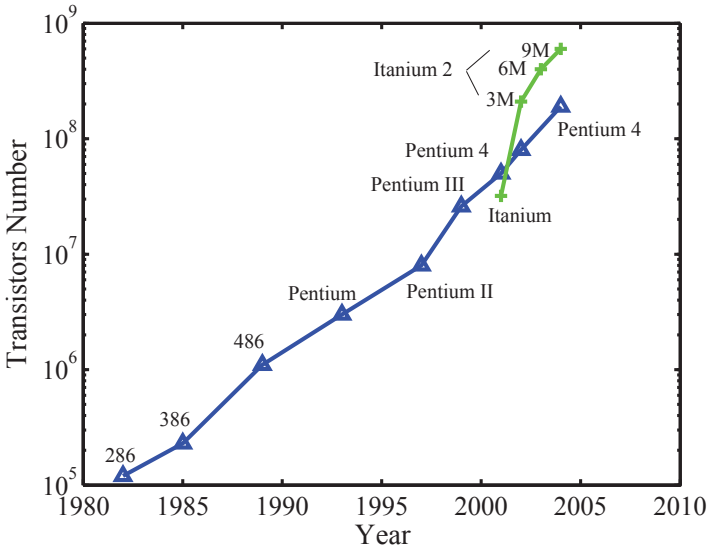


Figure 1.1: Moore's law continues—integration density of Intel microprocessors road map [2].

ern computer load may approach hundreds of A/μs [3, 4, 5, 6]. Furthermore, advanced manufacturing techniques allow microprocessor chips to lower the supply voltage down to under 1 V to reduce energy consumption, as illustrated in Fig. 1.2. In that case, small voltage fluctuations (e.g., several tens of mV) at power pins may lead to internal logic errors. Only small fluctuations in the supply voltage are allowed under all conditions [6].

In addition, modern computers can slow down the clocks smartly when the computational loads are light, or reversely speed up the clocks when the computational loads are heavy [7, 8, 9, 10]. Therefore, fast load transients may occur frequently and substantially affect the power supply performance. Besides, applications around portable devices can afford very limited space for power supplies while demanding very high conversion efficiency.

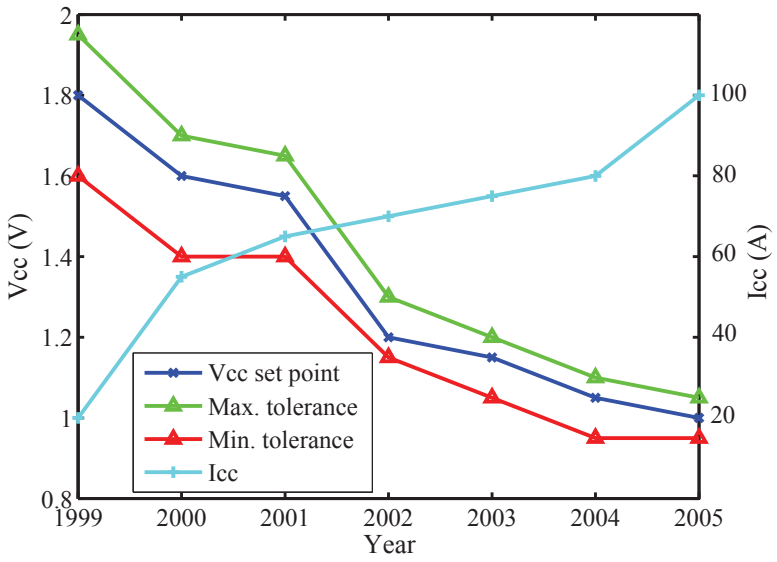


Figure 1.2: Intel microprocessors voltage and current requirement road map [5].

1.2 Objectives of the Thesis

The principal objective of this thesis is to study the design of auxiliary circuits for addressing very fast load transients. First we review the existing auxiliary circuits, and develop a systematic classification that would facilitate the design and selection of appropriate auxiliary circuits for the applications under consideration. The second aspect of our investigation is to find a low loss circuit that can feed very fast transient current. The corresponding control scheme for this circuit that cooperates with the main power supply is proposed. The third aspect of investigation is to develop a new auxiliary circuit and the associated control implementation taking advantage of load-informed power management.

1.3 Organization of the Thesis

This thesis is divided into two parts. The first part consists of Chapter 1 and Chapter 2, which will present a detailed discussion of the research background and an overview of existing methods for achieving fast transients using auxiliary circuits. In the second part, from Chapter 3 to Chapter 6, the original contribu-

tions of this research project will be described in detail.

Chapter 1 gives the motivations for designing power supplies that are capable of feeding fast load transient current. The objectives of this research work and the organization of this thesis are given in this chapter.

Chapter 2 gives an overview of power supply design schemes for feeding fast transient current. Firstly, four existing strategies for addressing the issue of fast load transients are reviewed. Then, some nonlinear control methods for generating minimum voltage overshoots and recovery time for a fixed topology are reviewed. Finally, the use of auxiliary circuits for extending the physical limits of minimum overshoots is discussed. Some existing implementations of auxiliary circuits are summarized.

Chapter 3 presents a general classification scheme for auxiliary circuits that deal with fast load transients in dc/dc converters. Each type of schemes is considered for specific applications. To identify the interaction mechanism of the auxiliary circuit and the main converter, the concept of intruding and non-intruding control is described. Finally, the design principles of auxiliary circuits for different application requirements are given.

Chapter 4 introduces the application of auxiliary circuits in addressing fast load transients based on the use of a bi-directional buck-boost converter circuit. Specific applications in three types of converters are described. The capacitor voltage control method is proposed to ensure the circuit stability.

Chapter 5 discusses the method of pre-energized auxiliary circuit to obtain null response under fast load transients. This method is specifically proposed for the application of load-informed power management, which means that the load is able to inform the power supply about information of the load transients. The information would include the exact times of load transients occurring and their magnitudes. Two candidate circuit implementations are given.

Chapter 6 gives the conclusion of this thesis. The first part is a reiteration

of the key contributions of the thesis. The second part offers a feasible direction for future development which includes the construction of a resonant circuit that achieves improved performance in certain aspects.

Chapter 2

Overview of Power Supply Design for Fast Transients

2.1 Introduction

In most applications, the power supply is responsible for providing a fixed voltage independently of the load current. To achieve this function, the power supply may employ a controllable current source to cope with the dynamic load current, as illustrated in Fig. 2.1.

In the conventional linear scheme, a high-power transistor operating in the

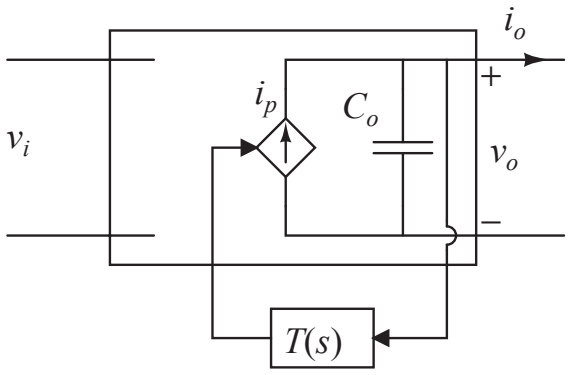


Figure 2.1: Basic mechanism of controlled current source feeding dynamic load current.

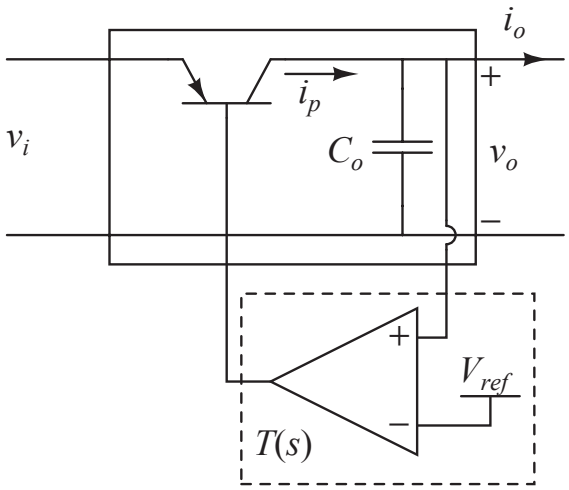


Figure 2.2: Basic structure of a linear voltage regulator.

active region is used to generate a controllable current source i_p. Fig. 2.2 shows that the magnitude of i_p is regulated by the bias current according to a comparator that compares the output voltage with a fixed reference. However, this is not an efficient voltage conversion scheme as the power transistor with non-zero voltage drop across it is always dissipating energy. Therefore, this so-called linear voltage regulator is only preferred for applications where the load is light or the desired voltage is close to the source voltage [11, 12, 13, 14].

Over the past few decades, more efficient schemes for providing a controllable i_p have been developed around switched-mode power circuits [15] where transistors are only operating as switches. The inductor current is regulated by varying the duty cycle of the switching transistor. To guarantee the stability of the system and sufficient precision of the output, the duty cycle signal is generated using a sophisticated feedback loop.

Since the switched-mode power circuit is nonlinear, the traditional feedback loop is designed based on a linear approximation model which is obtained via averaging and small-signal perturbation. Generally speaking, with a well designed feedback controller, the system may achieve the optimal bandwidth of $f_s/4$, where f_s is the switching frequency. The converter operating at hundreds of kHz is

impossible to feed fast load transients up to hundreds of A/μs without output voltage fluctuations. Increasing the size of C_o is a straight-forward solution to tackle this issue.

2.2 Strategies to Improve the Transient Response of Switched-Mode Power Supplies

As discussed before, a general switched-mode power supply which is designed based on a linear approximation model cannot provide satisfactory dynamic response to fast load transients. Four specific strategies to improve the transient response of switched-mode power supplies are discussed below.

2.2.1 Nonlinear Control

The first strategy is to use a nonlinear controller which is able to control the switch based on tracking the real-time trajectory in the state-space. Minimal recovery time and voltage fluctuation have been realized by the time-optimal control, which is shown in Fig. 2.3. When a fast transient occurs in a buck converter, the main switch can be immediately turned on or off (for positive or negative transient cases). Then, i_L may rise or fall at a maximum slew rate which is still much lower than the fast changing load current. Voltage overshoot or undershoot will appear due to the difference between i_L (i_p) and i_o. To suppress the voltage fluctuation, i_L needs to go beyond and then back to the destination steady-state point. In this way, both minimal voltage fluctuation and minimal settling time are achieved.

Many kinds of control schemes, e.g., boundary control [16, 17, 18], geometric control [19, 20, 21], sliding mode control [22], one-cycle control [23] and time optimal digital control [24, 25, 26, 27, 28], have been proposed to optimize the

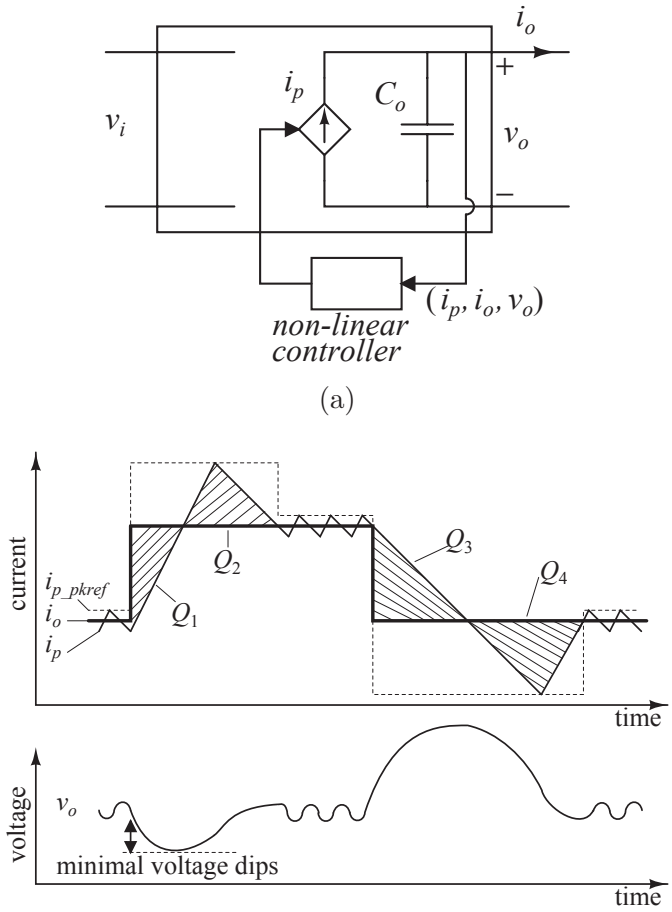


Figure 2.3: Power supply with nonlinear controller to achieve a minimum voltage fluctuation. (a) Block diagram of a power supply and (b) ideal waveform corresponding to time-optimal control scheme for fixed component parameters.

dynamic performance. However, regardless of the control method used, there is a minimum voltage fluctuation that cannot be overcome unless either a larger filter capacitor or a smaller inductor is used. This is the physical limitation of any converter of fixed topology.

With a smaller inductor (i.e., a higher current slew rate di/dt), the converter could respond more rapidly to a load change. However, a smaller inductor would also mean a larger current ripple, which will incur a higher current stress on the device, a higher ac power loss in the magnetics, and a larger output voltage ripple. Hence, it is often necessary to limit the inductor size of the converter. In

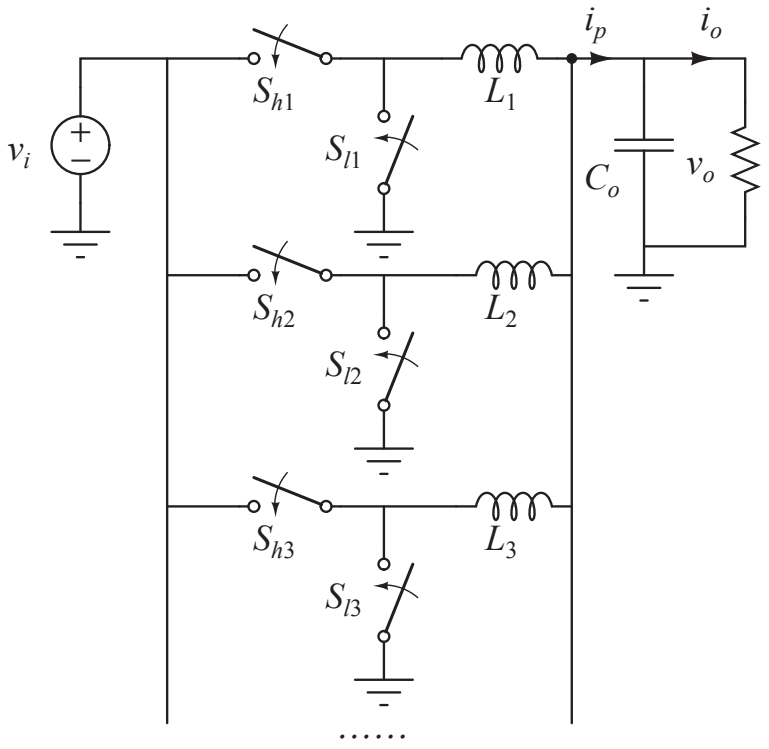


Figure 2.4: Multiphase topologies to achieve i_p coping with fast load transients.

most critical applications, a very large capacitance is typically used to achieve a satisfactory suppression of the output voltage overshoots. However, in practice, this may significantly increase the converter cost and size.

2.2.2 Multiphase Strategy

The multiphase structure shown in Fig. 2.4 has become an industry standard for the design of voltage regulator modules (VRM) for powering microprocessors [3], and is widely used in applications requiring low output voltage, high power and fast transient recovery. In this strategy, i_p is provided by several identical switching cells connected in parallel with appropriate control, as shown in Fig. 2.4. The N-phase structure can achieve a slew rate that is N time higher than the single-phase case, and reduce the ripple magnitude by N folds.

Based on the multiphase topology, a number of control methods for improving the dynamic response are proposed [29, 30]. A coupled multiphase converter that

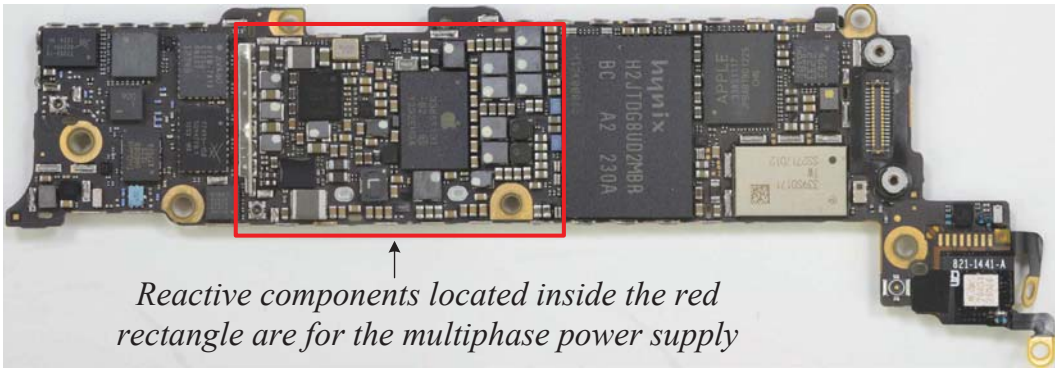


Figure 2.5: Bottom view of the iPhone5 main board where the power section occupies about 1/3 of the available space.

can provide fast load transients has been presented in [31]. More discussions on the efficiency and control performance of this scheme are given in [32, 33, 34].

However, the added phases will increase the control complexity, the components cost and the power supply module size. In some portable applications, the multiphase power supply occupies a substantial space of the main board, and presents serious limitation to accommodating further compact appliances (see Fig. 2.5).

2.2.3 Switched-Inductor Scheme

The third strategy is to instantly speed up the controllable current source i_p as illustrated in Fig. 2.6 where the fast current source is denoted as i_{pu}. The slew rate of the inductor current is proportional to the voltage drop across it and inversely proportional to the inductance value. Instantaneously reducing the inductance may speed up i_L to cope with the fast varying i_o. Fig. 2.6(b) and (c) show a practical method for realizing the strategy, which involves short-circuiting the main inductor and leaving a small leakage inductance.

Based on the above mechanism, an inductor switching method using a coupled inductor has been proposed to feed step-up fast transients [35]. A stepping inductance scheme which employs a coupled inductor has also been proposed to

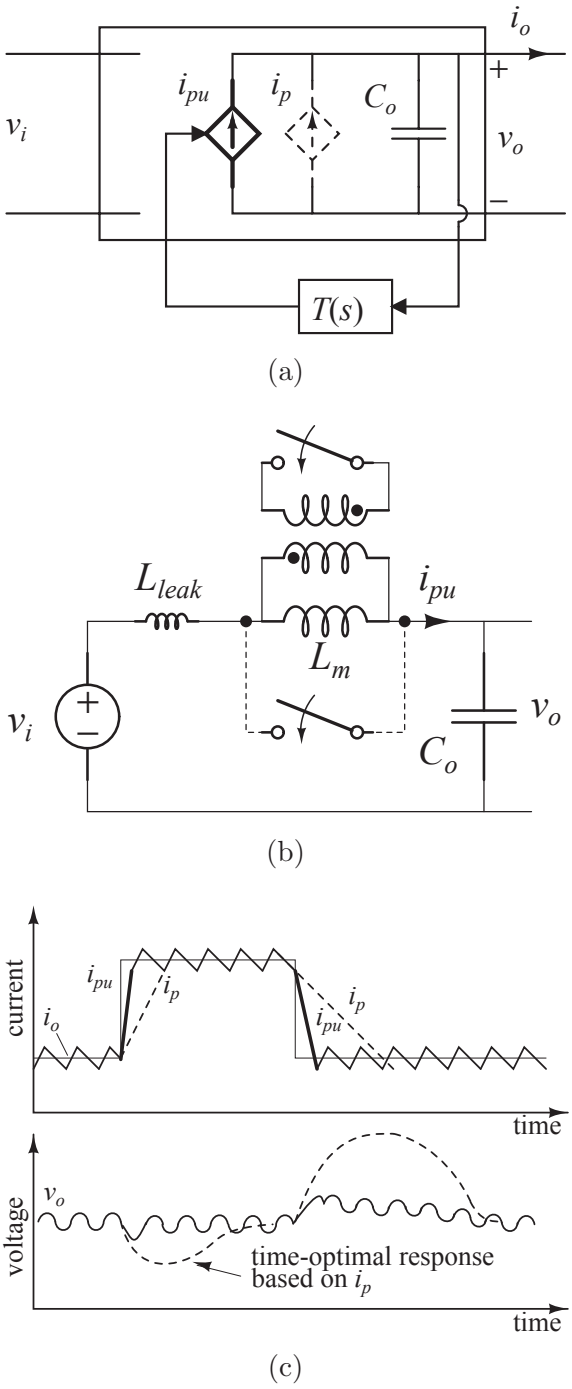


Figure 2.6: Operating principle of switched-inductor scheme. (a) Equivalent circuit model, (b) implementation using a coupled inductor, and (c) ideal waveforms.

feed both step-up and step-down transients [36]. Furthermore, a steered-inductor scheme has been used to realize ultra-fast step-down inductor current without using a coupled inductor [37]. Moreover, a flyback transformer scheme has been

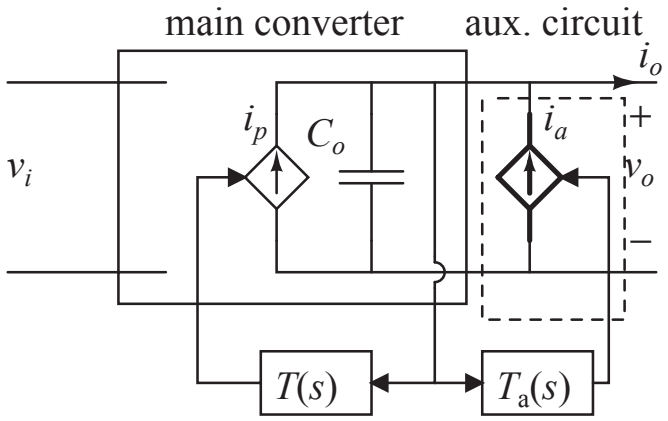


Figure 2.7: Auxiliary circuit strategy to feed fast load transients.

proposed to facilitate a digitally controlled buck converter to address the fast load transient problem [38].

The switched-inductor scheme is an effective strategy to lift the performance beyond the physical limit. However, the use of coupled inductors will increase the complexity of the system structure and cost. Moreover, the need for an extra switch which is connected in series to the inductor for catering a step-down load transient will also incur additional power loss [35, 37, 38].

2.2.4 Auxiliary Circuits to Compensate Fast Transients

The fourth strategy involves constructing an auxiliary circuit (i_a) to feed the fast transient current (see Fig. 2.7). In this scheme, the main converter is an ordinary power supply. From the viewpoint of the load, the combined use of an ordinary main converter and an auxiliary circuit provides an ultra-fast dynamic response to any transient disturbance that occurs at the load.

The basic principles for designing an auxiliary circuit are as follows.

1. Compared to the main converter, the auxiliary circuit must be capable of feeding ultra-fast transient current.

2. The auxiliary circuit is active during transient periods of the main converter

when fast stepping load current occurs.

3. When the main converter has recovered to its steady state, the auxiliary circuit operation will be suspended.

4. If the repetition rate of the transients is not high, the energy loss in the auxiliary circuit may not be significant comparing with that in the main converter.

5. The auxiliary circuit should occupy as little space as possible. The auxiliary circuit's operational current exceeding the components current ratings is allowed, since the auxiliary circuit is idle for most of the time. Components of low current rating and small size are suitable for the circuit.

2.3 Existing Schemes Using Auxiliary Circuits

2.3.1 Nullor Based Design of Compensator for Fast Transients

A theoretical formulation of auxiliary circuits for feeding fast transient currents has been proposed based on the use of nullators and norators which are two ideal components in circuit theory. The key idea is that the combination of the proposed auxiliary circuit and the practical load forms a "phantom" load which will remain slowly varying regardless of the occurrence of fast transients in the practical load [39].

The auxiliary circuit is performing as a "norator", as shown in Fig. 2.8. Then, the load is connected to the norator which supplies fast transient current to it so quickly that the main converter cannot feel the occurrence of fast transients in the load. On the other hand, the "norator" only provides the entire step current

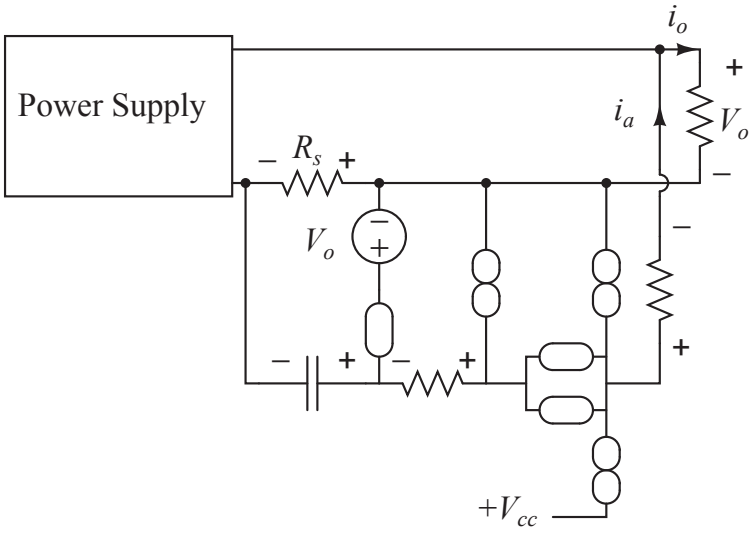


Figure 2.8: An auxiliary circuit based on the nullor model.

at the onset of the transient and then gradually decreases the current feeding level. Finally, the main converter will take over the entire load smoothly.

The proposed auxiliary circuit is realized by a set of push-pull power transistors that provide the required transient current. Details of the implementation are described in [40]. The cooperation of two control loops corresponding to the auxiliary circuit and the main converter have been studied and the operating principle of this control scheme has been proposed [41]. Moreover, the auxiliary circuit can be implemented in integrated forms due to the absence of reactive elements. Examples of on-chip schemes using this method are given in [42].

This method can significantly improve the dynamic response. However, its main drawback is that the auxiliary circuit needs extra power and thus reduces the efficiency overall.

2.3.2 Double Buck Converter Method

The parallel double buck converter has been proposed to improve the dynamic response to fast load transients [43]. This method is different from the multiphase method which employs several identical switching cells to feed fast transient cur-

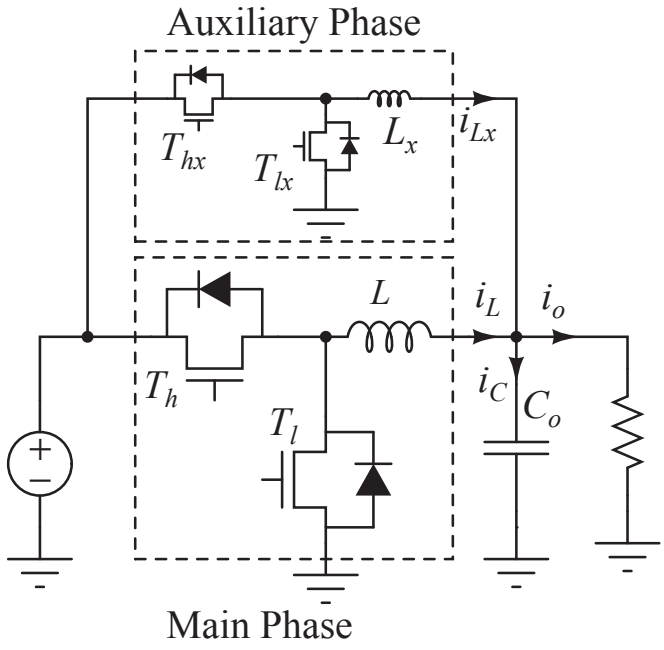


Figure 2.9: Double buck topology for improving the dynamic response to fast load transients.

rent. The topology of the double buck converter is shown in Fig. 2.9.

The main converter which is designed for power delivery at steady state uses components of higher power rating and operates at a lower switching frequency to improve the efficiency. The auxiliary converter which is designed for feeding fast transient current employs components with fast response characteristics and operates at a higher switching frequency. When v_o hits the preset threshold, i.e., when a fast load transient is detected, the auxiliary converter will operate to supply or absorb the needed energy to smooth v_o. When v_o is recovered to the normal band, the auxiliary converter will become idle.

The inductor of the auxiliary converter should be small to achieve a high slew rate current. In addition, all components only need to handle pulsating currents, and hence the size of inductors and MOSFETs can be reduced.

Before the concept of the double buck converter was proposed, an auxiliary converter had already been applied in isolated converters to address the fast transient requirement [44]. Moreover, a control scheme is needed for the auxiliary

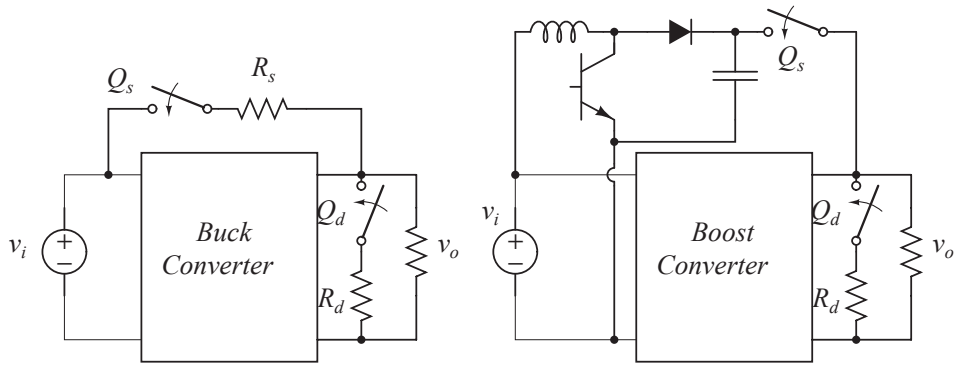


Figure 2.10: Augmentation method using resistance components to feed fast transient load.

converter, such as one that is based on the control of the capacitor current [45]. A digital control method has been proposed for an auxiliary converter [46, 47].

2.3.3 Resistance Augmentation Method

The short-term imbalance between the energy demanded by the load and that being available by the power supply is the main cause for failure to achieve null response to fast load transients in a traditional dc/dc converter with a fixed topology. Quantitative analysis of the energy imbalance for different topologies is given in [48, 49].

To address the above issue without imposing significant penalties on the cost, size and complexity of the system, the resistance augmentation method [50, 51] has been proposed and is illustrated in Fig. 2.10. Specifically, for a buck converter where the problem of fast load transients is prominent, discussions about the condition to achieve perfect response and a geometric control algorithm for the augmentation method have been given [52]. The resistance augmentation method would achieve fast load transients without the use of extra reactive components.

An example of an on-chip scheme realizing the augmentation by specific transistors is given in [53]. Since the augmented circuit will burn energy, the scheme is suitable for low power and portable applications.

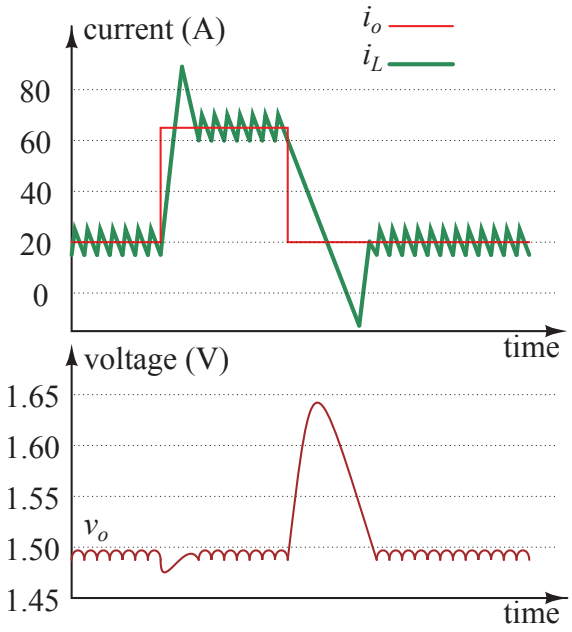


Figure 2.11: Responses to positive and negative transients on a buck converter with high voltage conversion ratio.

2.3.4 Auxiliary Circuits for Negative Transients

A practical application with fast load transients is a microprocessor power supply where the buck converter requires a rather high voltage conversion ratio [54, 55, 56, 57]. In this case, auxiliary circuits for negative load transients have been proposed to reduce the size, improve the efficiency and lower the cost.

The slew rate of the inductor current is proportional to the voltage drop across

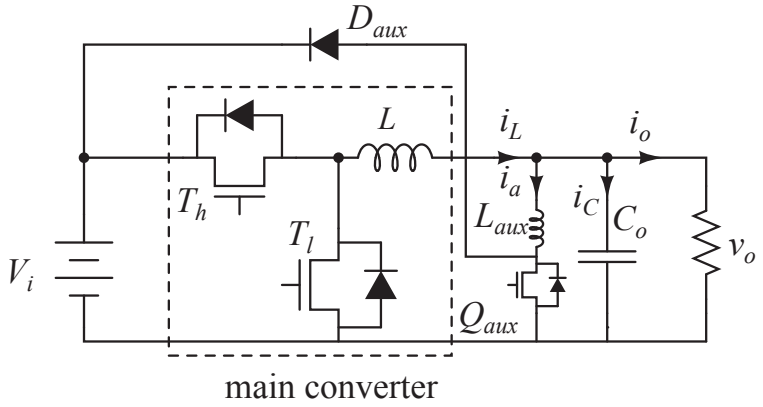


Figure 2.12: Auxiliary circuit topology for addressing negative transients.

the inductor. In a buck converter with a high V_i/V_o ratio, e.g., 12/1.5, when the positive switch is turned on, the voltage drop across the inductor is $V_i - V_o$. Conversely, when the positive switch is turned off, the voltage across on the inductor is $-V_o$, which is substantially less than $V_i - V_o$. Therefore, fluctuations on V_o induced by negative load transients are more significant compared to those by positive load transients (see Fig. 2.11).

An example of an auxiliary circuit for handling negative transients is shown in Fig. 2.12. Since it operates for negative load transients, only one switch control signal is needed. The control scheme could be simplified. Another advantage of this circuit is that the energy imbalance casing output voltage overshoots in the main converter can be re-circulated to the input terminal.

2.3.5 Auxiliary Circuits Taking Advantage of Power-Aware Computing

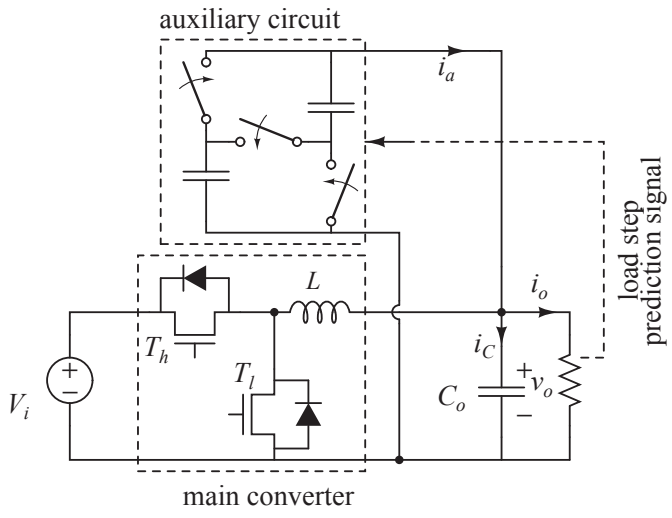


Figure 2.13: The switched capacitor scheme with load prediction to feed fast transients.

To obtain a perfect response by using auxiliary circuits, accurate and delay-free detections of load transients are needed. It is a big challenge to design such high-performance current sensors and related amplifier circuits. However, the

issue can be avoided if the load can communicate to the power supply about exact information of the transient times and magnitudes.

Modern computer loads are able to communicate with their power supplies and predict the occurrences of fast transients. Taking advantage of this capability of the load, a pre-charged switched capacitor circuit for feeding fast load transients has been proposed in [58] (see Fig. 2.13). When a fast load transient is expected, information about its amplitude and the time instant will be sent to the auxiliary circuit and the power supply. The capacitor will be pre-charged to an appropriate level. When the load transient occurs, the charged capacitor is connected to v_o. The acquired amount of energy will be transferred to or removed from the filter capacitor to reduce its voltage fluctuation.

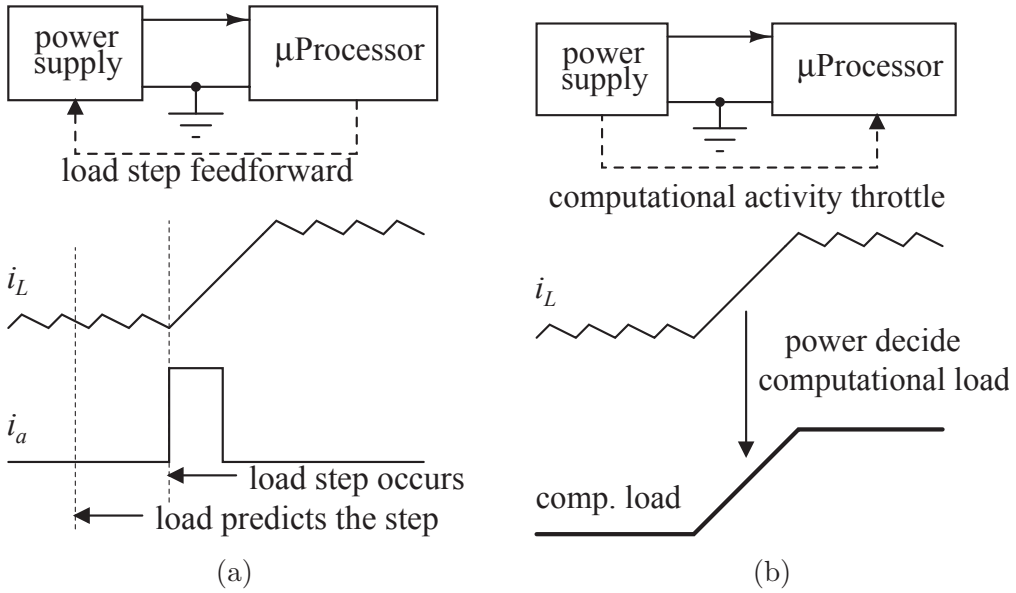


Figure 2.14: Power management achieved by power-aware computing. (a) The microprocessor informs the power supply when a load step will occur and how large the transient will be, and (b) the power supply controls the ramp rate of computational load.

Another example of power management arising from power-aware computing has been presented in [59]. Here, the power supply can get transient predictions from the microprocessor, thereby simplifying the control algorithm for the augmentation circuits to feed fast load transients. On the other side, the micro-

processor may also receive information about the status of the inductor current from the power supply to adjust the ramp rate of its computational load. When the slew rate of the inductor current matches the ramp rate of the load varying, output voltage deviations will be eliminated, as illustrated in Fig. 2.14.

2.4 Summary

Existing methods based on the use of auxiliary circuits are able to improve the dynamic response of dc/dc converters without having to increase the size and cost of the whole system. The design of auxiliary circuit has so far been following ad hoc procedures focusing on the specific application being considered. In the following chapters, a classification will be first presented to facilitate a more informed choice of circuit designs, control methods and connection schemes that would best suit a given application. Based on the proposed classification, some auxiliary circuits are proposed for specific applications.

Chapter 3

Classification of Auxiliary Circuit Schemes for Feeding Fast Load Transients in Switching Power Supplies

3.1 Introduction

Modern digital loads, such as microprocessors or digital signal processors (DSPs), impose challenging requirement for power supplies to feed high slew-rate transients [3, 4]. The main challenge in the power supply design is that after the occurrence of a transient, the power supply should keep its output voltage fluctuation within a short transition period and recover itself to a new operating point. If the converter can always keep its output voltage within a specified range around the reference point, e.g., $\pm 2\%$ of the reference value, the response of the power converter is said to produce a null-response to large-signal transients. The fundamental limitation for achieving null-response to large-signal transients is the size of the filter capacitor [48, 51, 52]. Many nonlinear control schemes

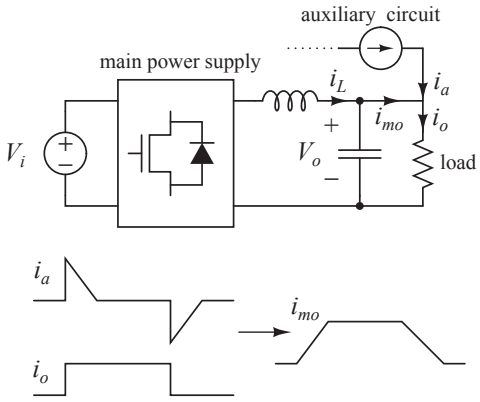


Figure 3.1: Equivalent model of auxiliary circuit for fast load transients.

have pushed the dynamic performance of a converter near to its physical limit [25, 24, 28, 21, 20, 27, 22, 16, 19]. To achieve further breakthrough without efficiency degradation, a number of methods utilizing auxiliary circuits have been proposed [48, 51, 52, 40, 39, 42, 41, 60, 44, 61, 62, 45, 47, 46, 43, 57, 56, 54, 55, 53, 58, 59]. Such auxiliary circuits operate as add-on current sources which will feed current with identical magnitude but in reverse direction to the transient to counteract the fast load change. An equivalent model of the auxiliary circuit is given in Fig. 3.1.

The use of auxiliary circuits has been proven effective for improving the dynamic response of the original converter. The increased complexity and efficiency reduction due to the use of the auxiliary circuit have been discussed for different practical situations. Specifically, the efficiency reduction has been studied previously in [48, 51, 52, 40, 39, 42, 41, 60, 44, 61, 62, 45, 47, 46, 43, 57, 56, 54, 55]. The problem of efficiency reduction in these schemes becomes significant because high-performance microprocessors operate with transients of huge magnitude and high repeating rate. To achieve optimal performance for specific applications, it is necessary to derive a common set of design principles for the application of auxiliary circuits. In this chapter, we propose a way to classify the existing schemes of auxiliary circuits. Through the process of classification study, we hope to provide

a systematic exposition of the design considerations of auxiliary circuits and to offer insights into the construction of suitable auxiliary circuits to satisfy specific requirements.

3.2 Overview of Classification

The earliest auxiliary circuits are achieved by linear circuits that may be a linear voltage regulator or power transistor pair [40, 39, 42, 41]. Resistance branches are added to create auxiliary current paths [48, 52, 51, 53, 59]. Such auxiliary circuits can be regarded as the *linear current-source style*, because the output current of the auxiliary circuit is provided by a linear regulator, i.e., the transistor is operating in the active region or the current-limiting resistors are in series with the output circuit. This type of auxiliary circuits gives an adequately fast transient but incurs significant power loss, especially when load transients occur more frequently. Moreover, the *linear current-source style* scheme uses no reactive components, and hence can be integrated on-chip. Therefore, in some low-power applications, this linear circuit scheme can be adopted to establish an on-chip solution of the power management [42, 53]. On the other hand, the use of *switching current-source style* constitutes a different type of auxiliary circuits in which the output current of the auxiliary circuit is controlled by regulating the duty cycle of a switching power circuit [60, 45, 44, 47, 46, 43, 57, 56, 54, 55, 61, 62] or the charge level of a switching capacitor [58]. Since the switching power circuit achieves a much higher efficiency than the linear voltage regulator, *switching current-source* based schemes are expected to enjoy a higher popularity.

In terms of connection style, auxiliary circuits can be classified into two categories, namely, the *shunt-output* style (or simply called *shunt* style) [40, 39, 42, 41, 60, 44, 61, 62, 58] and the *bridge-connection* style (or simply called *bridge* style) [48, 51, 52, 45, 47, 46, 43, 57, 56, 54, 55, 53, 59], as shown in Fig. 3.2. For

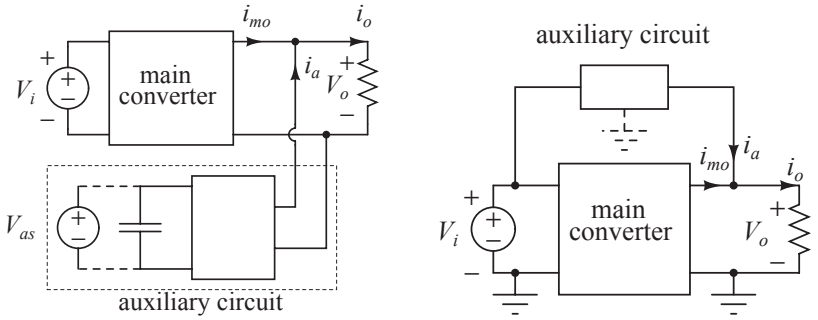


Figure 3.2: Classification of auxiliary circuits according to connection style. (a) Shunt-output style; (b) bridge-connection style.

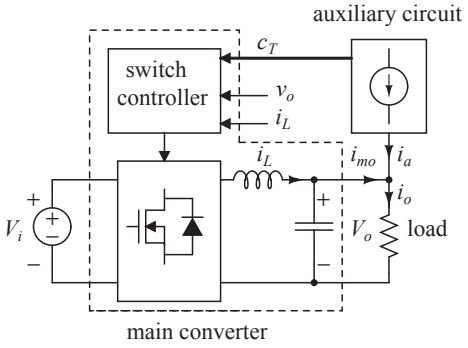


Figure 3.3: Classification of auxiliary circuits according to control loop interaction. Presence and absence of c_T signal defines an *intruding* scheme and *non-intruding* scheme, respectively.

the shunt style, the auxiliary circuit is plugged on to the output port of the power supply and hence can be used in isolated power supplies. Moreover, the auxiliary circuit must include sufficient capacity of energy storage elements or independent power source. For the bridge style, the auxiliary circuit is connected across the input and output ports of the power supply.

In terms of interaction style of control loops, classification can be performed according to the way in which the control loop of the auxiliary circuit interacts with that of the main power converter. Specifically, we can classify auxiliary circuits as *intruding style* [48, 51, 52, 41, 60, 61, 62, 58, 47, 46, 43, 57, 56, 54, 55, 59] or *non-intruding style* [40, 39, 42, 44, 45, 53], depending on whether the control loop of the main converter would be interrupted or affected during the transient

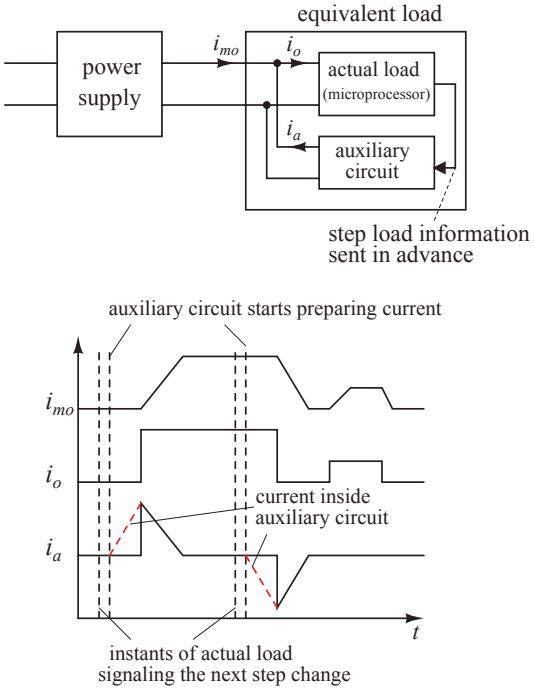


Figure 3.4: Illustration of i_a supplied by the auxiliary circuit to the converter with advance load information.

operation. In the intruding style, the auxiliary circuit control loop will affect the switching actions of the main converter, as shown in Fig. 3.3. Such auxiliary circuits can achieve the fastest change of the inductor current. On the other hand, in the non-intruding style, the auxiliary circuit does not interact with the main converter whose dynamics will be solely determined by its own feedback loop at all times. The auxiliary circuit effectively makes the original fast load transient appear as a slowly changing current slope that can be treated as a small-signal interference.

Recently, there has been rapid development in the availability of computer load information, resulting in a likely trend that the load profile including transient magnitude and time of occurrence can be accurately provided. Specifically, microprocessors, loads with fast transients, can predict the energy requirement and time of code executions quite accurately [63, 64, 65, 66, 67, 68]. A paradigm shift in power supply design may therefore be conceived that the design of power

converters may make use of the advance information about load changes [58, 59]. The impact of this paradigm shift on the design of auxiliary circuits is that communication is possible between the load and the auxiliary circuit, and hence load changes are no longer necessarily regarded as random or unpredictable processes. Thus, the load may pre-inform the auxiliary circuit before it steps up or down such that the switching frequency of the auxiliary circuit can be changed to avoid unwanted delays in transient detections. We refer to this type of auxiliary circuits as *load-informed style* as given in Fig. 3.4 and to others as *non-load-informed style*.

In the next section, we make a comparison of the *shunt-output* and the *bridge-connection* schemes. In Section 3.4, the development trend and implementations of the *intruding* scheme are discussed. In Section 3.5, the pros and cons of the *load-informed* auxiliary circuit schemes are discussed. Finally, in Section 3.6, we present some experimental measurements based on a buck converter to validate the various comparative properties under the proposed classification schemes.

3.3 Shunt-Output and Bridge-Connection Auxiliary Circuits

3.3.1 Power Loss

For the sake of comparison, we employ the bi-directional buck-boost converter as the auxiliary circuit for both shunt and bridge styles, as given in Fig. 3.5. Without the connection to V_i, the auxiliary circuit belongs to the shunt style. Here, V_{as} varies according to the choice of circuit parameters and the operation of the circuit [61]. Moreover, with the connection to V_i, the circuit assumes the bridge style and V_{as} becomes a constant.

The conduction power loss, switching loss and driver loss [69, 54] in the aux-

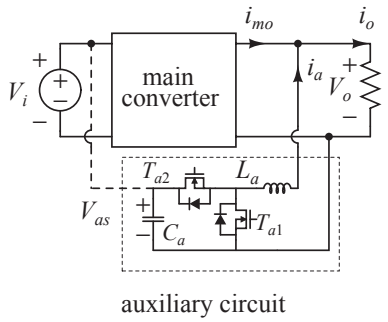


Figure 3.5: Auxiliary circuit scheme using a buck-boost converter.

iliary circuit can be expressed mathematically as respectively

$$P_{\text{con\_loss}} = \left(\frac{I_{\text{step}}^2}{3} + \frac{I_{pv}^2}{12}\right)(R_{\text{on}} + R_l), \tag{3.1}$$

$$\begin{aligned} P_{\text{sw\_loss}} &= P_{\text{sw\_on}} + P_{\text{sw\_off}} \\ P_{\text{sw\_on}} &= \frac{2}{3} C_{oss} V_{as}^2 f_s \\ P_{\text{sw\_off}} &= \frac{1}{4} V_{as} I_{\text{step}} t_f f_s \end{aligned} \tag{3.2}$$

and

$$P_{\text{gd\_loss}} = C_{iss} V_{gs}^2 f_s. \tag{3.3}$$

The meaning of the variables are explained in Table 3.1. Here, (3.1) indicates that the conduction loss is independent of V_{as}. From (3.2) and (3.3), it can be observed that for the required I_{step} and the given components, the switching and driving losses mainly depend on V_{as} and f_s.

When the auxiliary circuit is operating for a negative transient (i.e., step-down load current), T_{a1} is operating as an active switch, as shown in Fig. 3.6. Usually, m_1 (the slope of the falling edge), m_3 (the slope of mean i_a) and I_{pv} are specified by the application. It can be observed that f_s depends on V_{as}, i.e.,

$$m_3 = \frac{I_{\text{step}}}{T_{\text{tran}}} = m_2(1 - D_1) - m_1 D_1$$

Table 3.1: Variable Meaning of Power Loss Estimations

Variables	Meanings
I_{step}	Magnitude of load transients
I_{pv}	Peak-valley value of deviation referring to mean i_a in one switching cycle
R_{on}	On resistance of MOSFETs*
R_l	Winding resistance of the inductor
C_{oss}	Output capacitance of MOSFETs
C_{iss}	Input capacitance of MOSFETs
V_{gs}	Driver voltage of MOSFETs
V_{as}	Source voltage of the auxiliary circuit
f_s	Switching frequency
t_f	Turn off time of MOSFETs

*assuming that characteristics of the MOSFETs are identical

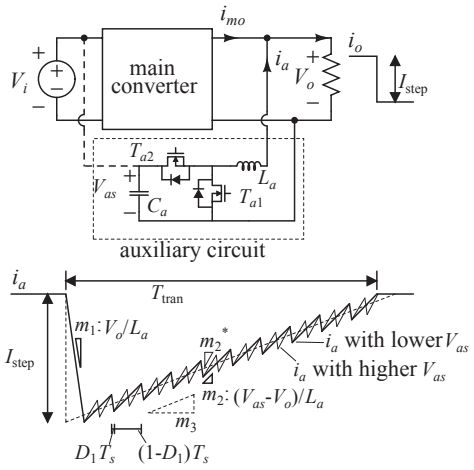


Figure 3.6: Operation under negative load transient, i.e., step-down load current.

$$= V_{as}m_1D_1/V_o - (V_{as} - V_o)/V_om_1, \tag{3.4}$$

$$D_1 = \frac{m_1(V_{as} - V_o)/V_o - m_3}{m_1V_{as}/V_o}$$

$$\approx 1 - \frac{V_o}{V_{as}} \quad (m_1 \gg m_3) \tag{3.5}$$

and

$$f_s = D_1/T_{\text{on}} \approx \frac{1}{T_{\text{on}}}\left(1 - \frac{V_o}{V_{as}}\right) \tag{3.6}$$

where T_{on} is a function of m_1, m_3 and I_{pv}. Substituting f_s in (3.2) and (3.3) by

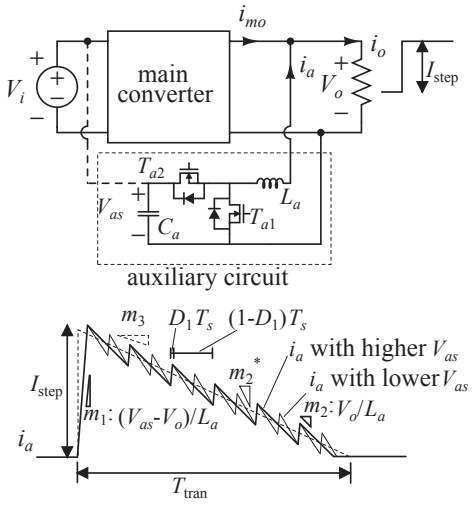


Figure 3.7: Operation under positive load transient, i.e., step-up load current.

(3.6), the sum of switching power loss and driver loss can be found as

$$\begin{aligned} P_{\text{sw\_loss}} + P_{\text{gd\_loss}} &= \frac{2}{3}\frac{C_{oss}}{T_{\text{on}}}V_{as}(V_{as}-V_o) \\ &+\frac{1}{4}I_{\text{step}}t_f\frac{V_{as}-V_o}{T_{\text{on}}} \\ &+C_{iss}V_{gs}^2\left(1-\frac{V_o}{V_{as}}\right)\frac{1}{T_{\text{on}}} \end{aligned} . \tag{3.7}$$

From the above equations, we clearly see that decreasing V_{as} will substantially reduce power loss.

The scenario of positive transient, i.e., step-up load current, is shown in Fig. 3.7. The power loss can be calculated in a likewise manner as for the case of negative transient above, i.e.,

$$\begin{aligned} m_3 &= \frac{I_{\text{step}}}{T_{\text{tran}}} = m_1D_1 - m_2(1-D_1) \\ &= m_1V_o/(V_{as}-V_o) - m_1D_1V_{as}/(V_{as}-V_o), \end{aligned} \tag{3.8}$$

$$\begin{aligned} D_1 &= \frac{m_1V_o/(V_{as}-V_o) - m_3}{m_1V_{as}/(V_{as}-V_o)} \\ &\approx \frac{V_o}{V_{as}} \quad (m_1 \gg m_3), \end{aligned} \tag{3.9}$$

$$f_s = D_1/T_{\text{on}} \approx \frac{V_o}{T_{\text{on}}V_{as}}. \tag{3.10}$$

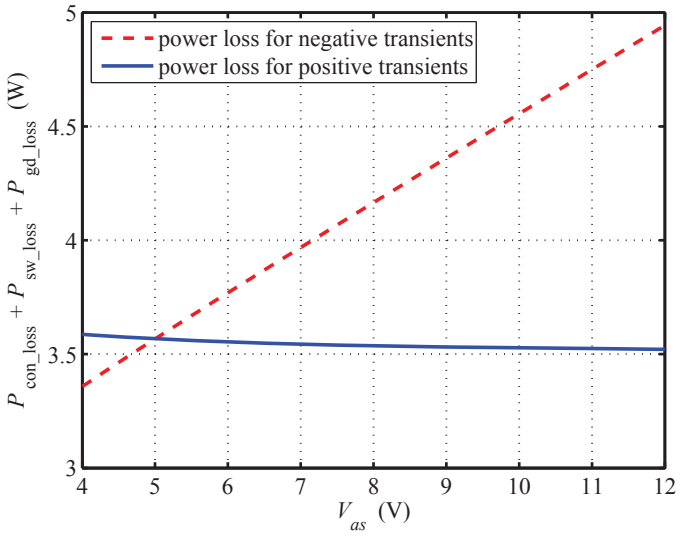


Figure 3.8: Power loss versus V_{as} during auxiliary circuit operation (V_i = 12 V, V_o = 2.5 V, C_{iss} = 460 pF, C_{oss} = 95 pF, t_f = 20 ns, V_{gs}= 12 V, I_{step} = 15 A, I_{pv} = 2 A, m_1 = 5 A/μs, T_{on} = 0.4 μs, R_{on} = 35 mΩ.

And finally, we get

$$P_{\text{sw\_loss}} + P_{\text{gd\_loss}} = \frac{2}{3}\frac{C_{oss}}{T_{\text{on}}}V_{as}V_o + \frac{1}{4}I_{\text{step}}t_f\frac{V_o}{T_{\text{on}}} + C_{iss}V_{gs}^2\frac{V_o}{T_{\text{on}}V_{as}}. \tag{3.11}$$

In this case, the minimal value of $P_{\text{sw\_loss}} + P_{\text{gd\_loss}}$ exists while $V_{as} = \sqrt{\frac{3C_{iss}}{2C_{oss}}}V_{gs}$. Since C_{iss} is usually a few times of C_{oss} and V_{gs} is 8 to 12 V for low V_o applications, variation in V_{as} will not quite affect (3.11), as compared to (3.7). Fig. 3.8 shows a plot of the total power loss versus V_{as}.

3.3.2 Choice of Applications

When the converter is operating at a high input-to-output ratio, e.g., V_i/V_o = 12/2.5 V/V. The auxiliary circuit only need to work for negative transients [57]. When the bridge-connection scheme is chosen, the auxiliary circuit will incur a high dissipation. This is because V_{as} is fixed and has the same voltage as V_i. However, when the shunt scheme is applied, V_{as} will be provided by C_a and

controlled by configuring the capacitance. In this case, a strategy for energy balance is necessary, and can be achieved by reservoir capacitor voltage control, which will incur power loss [61]. If this power loss is sufficiently small, the shunt scheme will still be more desirable.

On the other hand, when the converter is operating at a low input-to-output ratio, e.g., $V_i/V_o = 5/2$ V/V. The power loss of the circuit in the bridge-connection scheme will be naturally reduced. Thus, the simpler bridge scheme is preferred. Moreover, when isolation is required between the input and output, the shunt scheme will be the only choice.

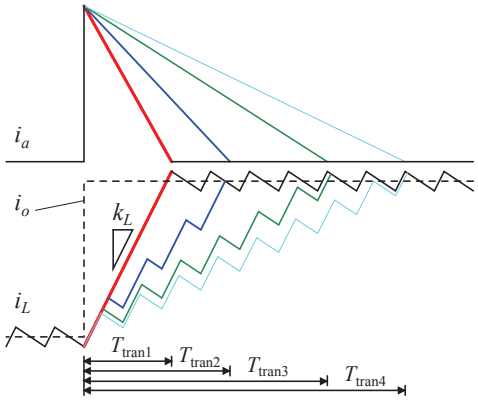


Figure 3.9: Operation time of the auxiliary circuit depends on the current slope of i_a but is limited by k_L.

3.4 Non-Intruding and Intruding Auxiliary Circuit Schemes

The purpose of using an auxiliary circuit is to make a large load fast transient "appear" as a slow transient load current so that any ordinary power supply would be able to handle the load change. Effectively, the auxiliary circuit and the load together present themselves as a composite smart load (whose transients are always slow) to the power supply. When the resulting slope of the transiting

current is relatively high, the operation time required of the auxiliary circuit is relatively short, as shown in Fig. 3.9. The intruding scheme provides the shortest operation time of the auxiliary circuit thus incurring less power loss, while the non-intruding scheme offers the advantage of design simplicity.

3.4.1 Non-intruding Schemes

Suppose the application of the auxiliary circuit makes the resulting load current change slowly, i.e., a relatively long T_{tran}. The resulting current thus becomes a small perturbation having most frequency components lying within the bandwidth of the control loop of the main converter. In this case, v_o can be tightly regulated. In this operation, the programmed i_a is well tracked by the main converter, as illustrated in Fig. 3.10.

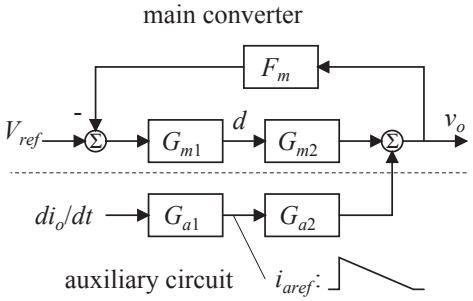


Figure 3.10: Non-intruding auxiliary circuit schemes are achieved by a closed-loop main converter and an open-loop auxiliary circuit.

The auxiliary circuit does not interact with the control loop of the main converter, and is referred to as a *non-intruding* auxiliary circuit scheme. The advantage is that two parts (main converter and auxiliary circuit) are almost operating independently. Using this scheme, an existing main converter might be enhanced in dynamic performance without modifications on its original circuit design to cater the scheme.

The simulation result is given in Fig. 3.11, where the main converter takes 500 μs (100 switching cycles) to relocate its operation point. The application of

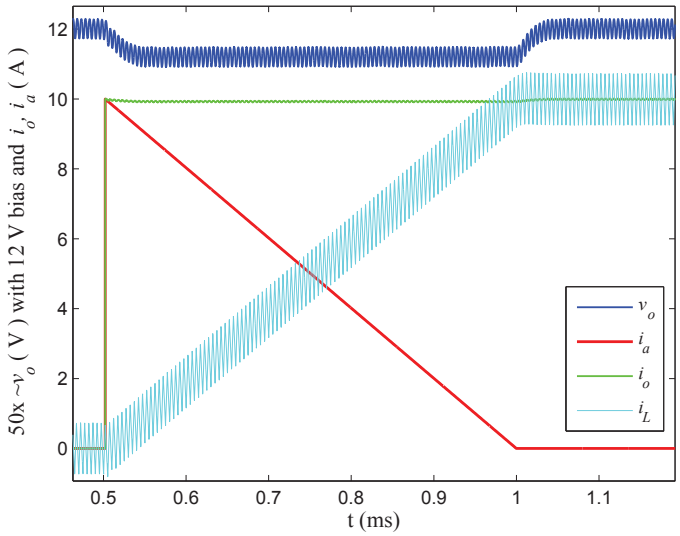


Figure 3.11: Simulation waveforms of non-intruding scheme for a 10 A positive transient, with $V_i/V_o = 12/2.5$ V/V, and switching frequency of main converter at 200 kHz. The auxiliary circuit provides a ripple-free i_a.

non-intruding schemes obviously have their drawback as they may incur a higher power loss due to the prolonged active period T_{tran}. Components with larger current and heat rating are thus needed. Hence, trade-off between size, efficiency and overshoot on v_o would need to be considered.

3.4.2 Intruding Schemes

To overcome the inherent deficiency of the non-intruding scheme, we need to shorten the active time, for example, by speeding up the rate of decline of i_a. The shortest possible active time of i_a is T_{tran1}, as shown in Fig. 3.9. However, the main converter may fail to follow i_a for such a fast trajectory, as controllers cannot have infinite control bandwidth [70]. The solution is to let the auxiliary circuit interact with the control loop of the main converter to achieve the fastest transition while the auxiliary circuit is following the state of i_L to provide the required current. Auxiliary circuits that interact with the main control loop are referred to as *intruding* auxiliary circuits.

In the mechanism described in Fig. 3.12, there is a circuit block to identify

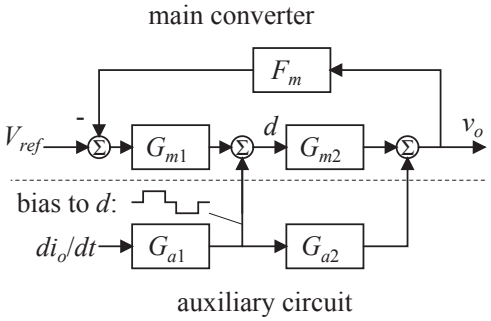


Figure 3.12: Intruding auxiliary circuit model.

the transient at i_o, intruding a biasing signal to change the duty cycle of the main converter. This obviously will increase the complexity of the control system. Only a few additional low power components need to be included in the existing PWM controller ICs. In practice, there are two ways to achieve the intruding function in PWM controllers.

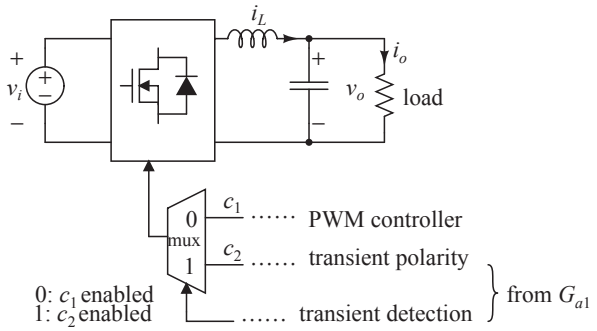


Figure 3.13: Schematics of the brute-force switch-signal switching in the intruding scheme.

1) Brute-force Switching of the Switch Signal

A multiplexer can be added to the switch controller of the main converter, as explained in Fig. 3.13. Normally, c_1 from the original feedback controller is enabled, while the auxiliary circuit is suspended. When an i_o transient is detected, c_2 from the auxiliary circuit is enabled to enforce a "100%" duty cycle for a positive transient or "0%" duty cycle for a negative transient. This method has been adopted in most auxiliary circuit schemes [60, 61, 58, 62, 47, 43, 57, 56, 54].

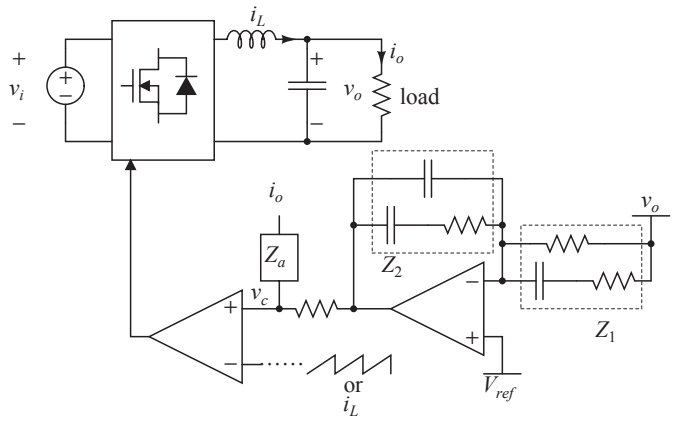


Figure 3.14: Schematics of the feedforward-signal injecting in the intruding scheme, where a signal corresponding to i_o is injected into feedback controller.

2) Injecting a Feedforward Signal

Another way to achieve intruding is shown in Fig. 3.14, where a feedforward signal dependent on i_o is injected to the feedback control through the network Z_a [48, 51, 52, 46]. In a conventional linear controller, the control signal v_c derived from v_o cannot follow i_o in the large-signal sense. When the feedforward signal is added to the feedback network, a fast transient at i_o will lead to a large increment or decrement in v_c, which can achieve a "100%" or "0%" duty cycle instantly.

Injecting a feedforward signal has an extra merit. When the auxiliary circuit is active, the operating point is allowed to shift at a large scale in a short time. However, under a linear feedback controller, the operating point can only move slowly at small-signal scale. Thus, the feedback controller cannot take v_c to the new steady-state point quickly enough following a rapid change in i_L. The feedforward signal not only switches the duty cycle to 1 or 0, but also pushes v_c to the new operating point without any overshoot in v_o. Fig. 3.15 shows the comparison of the brute-force switch-signal switching and the use of feedforward signal. It is noted that at instants of 1.0 ms and 1.5 ms, the load transients and voltage deviations have been addressed by the auxiliary circuit.

In Fig. 3.15(b), the duty cycle is switched to "0" or "1" by brute-force switch-

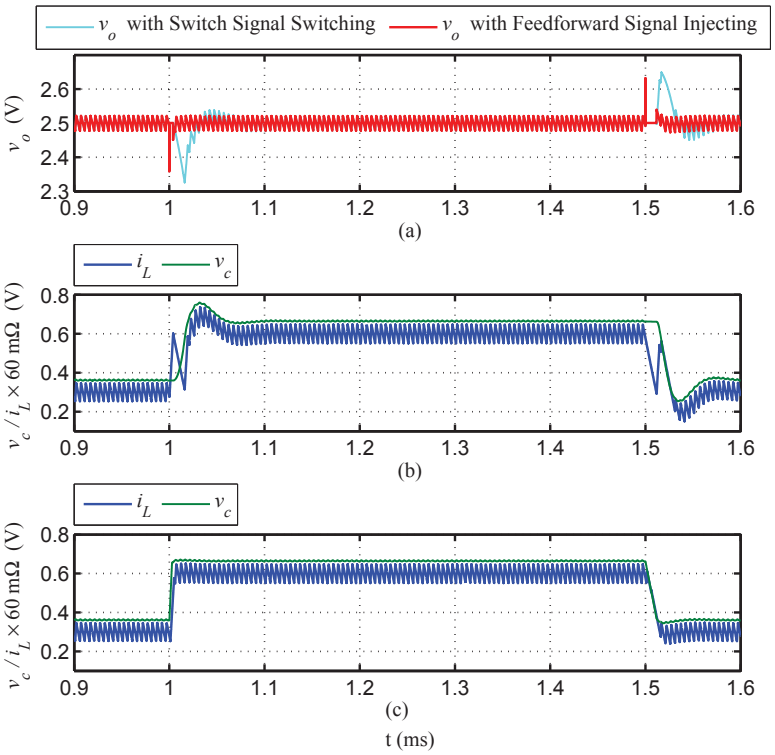


Figure 3.15: (a) Comparison of waveforms of output voltage. Waveforms of inductor current (i_L) and current reference (v_c) of the controller intruded by (b) brute-force switching of the switch-signal; (c) injecting a feedforward signal.

ing. It is clear that i_L initially is not tracked to v_c as the control loop is temporarily suspended, and after the transition (active period of the auxiliary circuit), i_L is re-tracked to v_c. In this process, a voltage deviation occurs. Moreover, in Fig. 3.15(c), v_c is influenced by the feedforward signal, causing i_L to react spontaneously during the transition.

3.5 Load-informed Auxiliary Circuits

As explained in Section 3.2, computer loads are capable of providing accurate load profile information, including the magnitudes and times of occurrence of load transients. Auxiliary circuits can thus be designed with the assumption of the availability of load information. Essentially, the load communicates with the auxiliary circuit about a future occurrence of a load transient, allowing the

auxiliary circuit to pre-charge its storage element appropriately and provide the necessary fast transient current at the time it occurs. This eliminates the limitation caused by sensing delays when the load transients occur at random times.

3.5.1 Benefits of Load-informed Schemes

The first obvious advantage of the load-informed scheme is the elimination of transient sensing circuits [58, 59]. Voltage deviations due to the sensing delays can thus be avoided.

In the previously described non-load-informed auxiliary circuit using a switching power circuit, the design involves trade-off consideration between efficiency and output voltage deviation. In the scenario of Figs. 3.6 and 3.7, to provide faster i_a to meet the high slew rate requirement, a small inductor should be employed, necessitating the use of a high switching frequency and incurring a high power dissipation.

With the load-informed auxiliary circuit, the load information including step time, magnitude and direction are known in advance. Thus, the auxiliary circuit can pre-energize its storage elements and to address the transient at the right synchronized time [58]. The auxiliary circuit can thus be designed to achieve a higher current slew rate at a lower switching frequency.

3.5.2 Limitations of Load-informed Schemes

The effectiveness of the load-informed scheme depends on the precision of loading prediction, and the effect of inaccurate load profile information remains fundamental. Since the loading prediction method of microprocessor or computer loads is based on execution models of the given codes, errors may be inevitable due to some unexpected events such as interrupts.

When the predicted magnitude of I_{step} has an error of i_{ae}, i_a may be adaptively

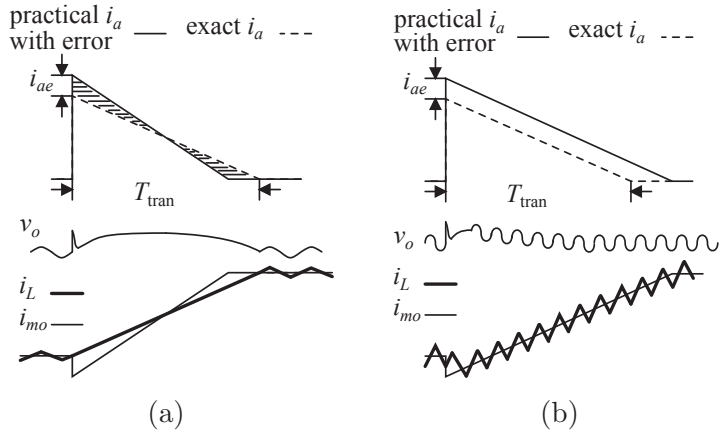


Figure 3.16: Prediction inaccuracy in the magnitude of transient for (a) intruding and (b) non-intruding schemes.

regulated, as depicted in Fig. 3.16(a) for the intruding scheme, to make sure the two hatched triangles have identical area. In this case, a current sensor will indicate the real value of I_{step}. Hence, i_L will not run beyond the needed scale. It is noted that this sensor does not require a wide bandwidth, while the active time of the auxiliary circuit is controlled by load information instead of transient detection. The voltage overshoot due to the inaccuracy of magnitude prediction can be estimated as

$$\Delta v_{oe} < \frac{T_{\text{tran}} i_{ae}}{4C_o}. \tag{3.12}$$

For the non-intruding scheme, as shown in Fig. 3.16(b), i_a can track the scheduled trajectory and the converter is able to follow i_{mo}. The voltage overshoot is caused by the main converter feeding a transient of i_{ae}. As long as the main converter can feed a small transient, i.e., i_{ae}, the scheme will allow a maximum prediction error of i_{ae}.

Furthermore, a sync signal indicating the time instant of a transient occurrence may be introduced to guarantee the synchronization of the action of the auxiliary circuit with the transient. Essentially, the auxiliary circuit may prepare itself with the received information, and the action of delivering i_a can be induced by the sync signal. See Fig. 3.17. Therefore, an inaccurate prediction in

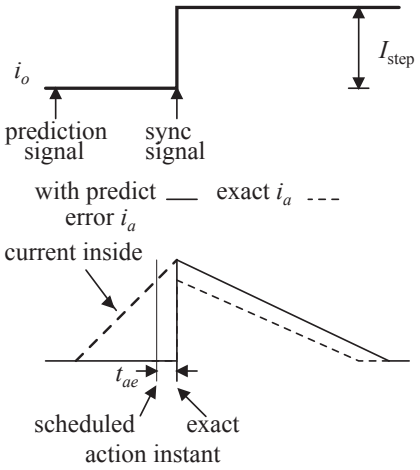


Figure 3.17: Prediction inaccuracy in the time of transient occurrence for non-intruding schemes.

the time of transient occurrence may be lumped on the magnitude error which can be handled readily.

3.6 Experimental Validation

3.6.1 Prototypes

To validate the above analysis, two sets of experimental prototypes are constructed. A buck converter (parameters given in Table 3.2) with an auxiliary circuit (parameters given in Table 3.3) operating in a shunt-output style or bridge-connection style is implemented. The schematic diagram is given in Fig. 3.18.

The switch K is for selecting the operation mode between the *shunt-output style* and the *bridge-connection style*. When K is on, V_{as} is duplicated from V_i, establishing a *bridge-connection* scheme. Conversely, when K is off, a *shunt-output* scheme is established. Here, V_{as} is controlled by the reservoir capacitor voltage [61]. For brevity, the function mode of the reservoir capacitor voltage control is not shown in Fig. 3.18. The dummy load is able to generate transients from 5 A to 10 A. The module M_1 is used to detect the transient at the load

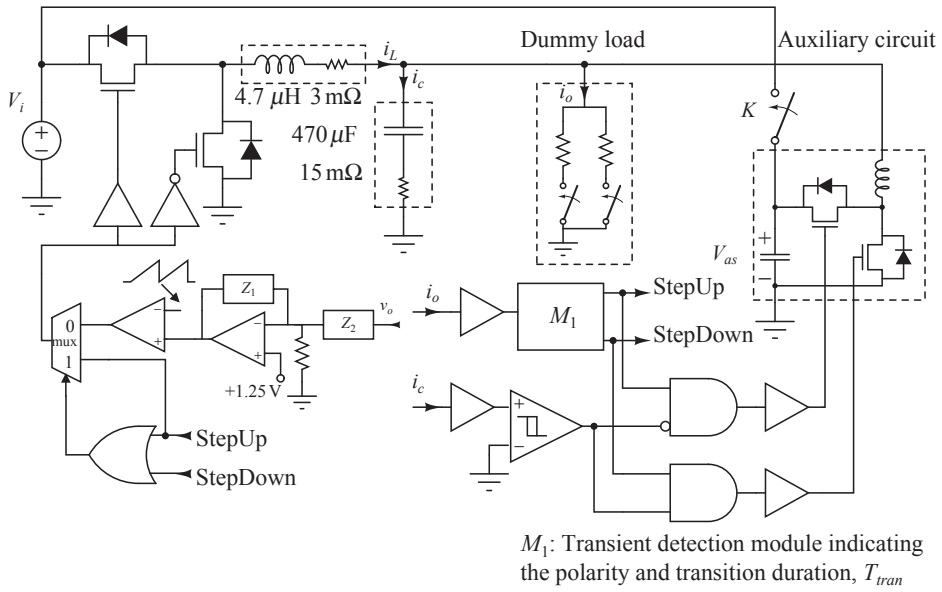


Figure 3.18: Schematic of the prototype for comparing bridge-connection and shunt-output schemes.

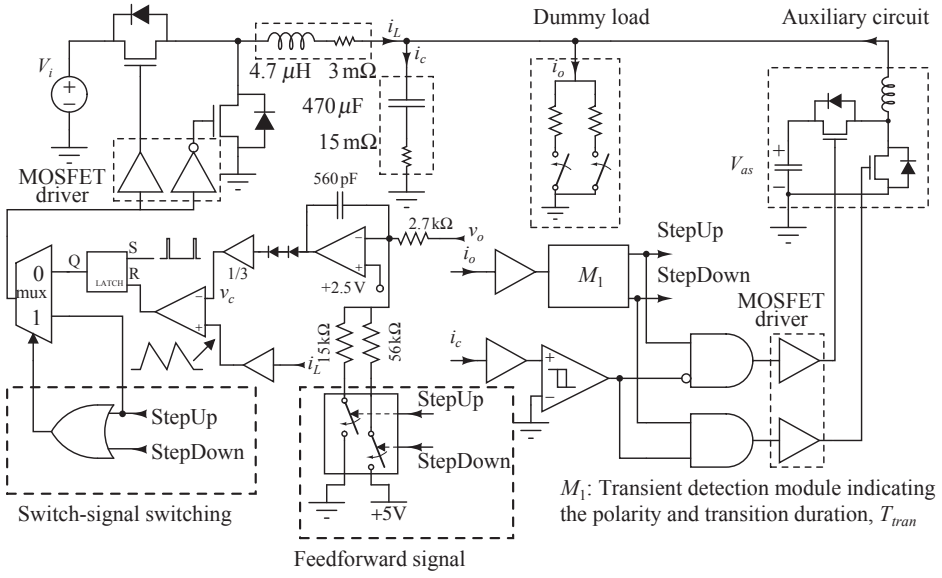


Figure 3.19: Schematic of the prototype demonstrating the effectiveness of the intruding scheme.

Table 3.2: Parameters of the buck converter for comparison of bridge-connection and shunt-output schemes

Parameter	Value
V_i	12 V—5 V
V_o	2.5 V
Controller	IRU3037
Control mode	voltage mode
f_s	200 kHz
L	4.7 μH, 3 mΩ
C	470 μF, 15 mΩ
MOSFETs	IRL3715
Load	1 A— 15 A
V_o deviation	$\leq$ 80 mV

Table 3.3: Parameters of auxiliary circuits

Parameter	Value
V_{as}	equal to V_i (bridge-connection) 4 V to 6 V (shunt-output)
T_{on}	0.3 μs
I_{pv}	2 A
m_1	$\geq$ 5 A/μs
Inductor	0.47 μH, 5 mΩ
MOSFETs	FW261 R_{on} = 35 mΩ C_{oss} = 95 pF C_{iss} = 460 pF V_{gs} = 12 V t_f = 20 ns
C_a	33 μF

side and generate an indication pulse ("StepUp" and "StepDown"), whose pulse width is proportional to the amplitude of the transient. Also, i_c is measured from the value of dv_o/dt by a differential circuit, and i_o is measured by a current sensor with current sensor amplifier ADM4073T.

Another buck converter (parameters given in Table 3.4) with an auxiliary circuit (parameters are same with Table 3.3) operating in the *intruding style* under the two implementation strategies described earlier is implemented. The schematic diagram is shown in Fig. 3.19. The transient detection and the control circuits are the same as the first prototype constructed for the shunt-output

Table 3.4: Parameters of the buck converter for studying the intruding scheme

Parameter	Value
V_i	12 V
V_o	2.5 V
Controller	UC3843
Control mode	current mode
Current sensor	3 mΩ (with 20 V/V amplifier, ADM4073T)
Bilateral switch	CD4066
f_s	200 kHz
L	4.7 μH, 3 mΩ
C	470 μF, 15 mΩ
MOSFETs	IRL3715
Load	5 A— 15 A
V_o deviation	$\leq$ 80 mV

scheme.

In the control circuit of the main converter, two functional blocks are employed to achieve the "intruding" scheme, which will facilitate generation of a fastest response under the two implementation approaches, namely, brute-force switching of the switch-signal and feedforwarding. The circuit serving the former is a multiplexer. When no transients occur, the channel 0 is selected and hence the traditional peak current control loop is formed. Either "StepUp" or "StepDown" signal is enabled, and the high-side switch is set as "1" or "0". The circuit serving for the latter is a bilateral switching resistors group, where bilateral switches are implemented by CD4066. When "StepUp" or "StepDown" is enabled, the corresponding switch will be turned on to vary v_c.

In these prototypes, the buck converter is controlled by a current-mode controller UC3843. A simple RC compensation network ($R = 2.7$ kΩ, $C = 560$ pF) maintains stability in the main converter. To achieve the appropriate feedforwarding in v_c, two 15 kΩ and 56 kΩ resistors are employed. Hence, when the negative terminal of the error amplifier is connected to 0 V through the 15 kΩ resistor, a 360 mV/μs v_c ramp-up is achieved. On the other case, when 5 V is

connected through the 56 kΩ resistor, a 96 mV/μs v_c ramp-down is achieved. The two implementations of the intruding scheme will be enabled separately.

3.6.2 Power Loss Comparison of Shunt-Output and Bridge-Connection Schemes

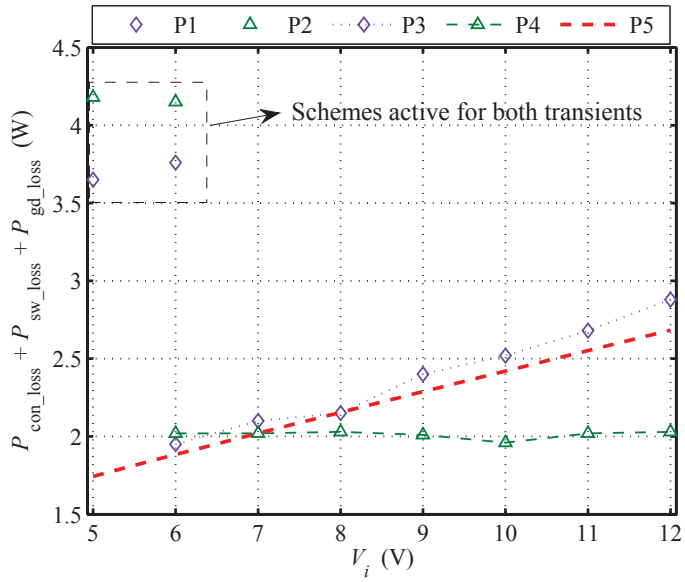


Figure 3.20: Power loss measurement comparison of the auxiliary circuit assisting a buck converter in various schemes with varying V_i. Lines P1 and P2 correspond, respectively, to bridge-connection scheme and shunt-output scheme for either step-up and step-down transients, Lines P3 and P4 correspond to step-down transients for the bridge-connection scheme and shunt-output scheme, respectively. Line P5 is ideal power loss for step-down transients in the bridge-connection scheme or the shunt-output scheme with V_{as} chosen in the range of 5 to 12 V.

When the load is undertaking a 10 A transient, the auxiliary circuit operates separately in the two schemes for different V_i. Power loss in these two cases are compared and given in Fig. 3.20. All measured values in the plots represent power loss of the auxiliary circuit during its normalized active period, i.e., 9.4 μs which is the active time of the auxiliary circuit for 5 A step-down transients. For the *shunt-output* scheme, the energy loss in the reservoir capacitor voltage regulation is also included in the total energy loss. Note that when V_i is high, the auxiliary

circuit is only active for step-down transients.

For the *bridge-connection* scheme, V_{as} is equal to V_i. Referring to Fig. 3.20, the loss in the bridge-connection scheme for step-down transients (line P3 in the figure) is close to the ideal loss (line P5), which displays a rising trend as V_i increases. Furthermore, for the *shunt-output* scheme, with a fixed range of V_{as} (4 V to 6 V), the auxiliary circuit is always pumping around 2 W power. The ideal power loss can be estimated as around 1.75 W, as labeled as dotted line P5 in Fig. 3.20. The absorbed energy will be discharged to the output slowly with dissipation. Thus, the real current power loss is higher than the ideal value.

From Fig. 3.20, we see that when V_i is around 6 V to 8 V, the power loss of the two schemes are very close. However, when V_i is higher, the power loss of *bridge-connection* style becomes significantly larger than that of the *shunt-output* style. This result verifies the analysis presented in Section 3.3.2.

When V_i drops to 6 V, the auxiliary circuit should be made to work to handle a step-up transient. Operating for a step-up transient incurs a higher power loss in the *shunt-output* scheme than the *bridge-connection* scheme. The reason is two-fold. First, the requirement of balanced bidirectional charging of the reservoir capacitor (only for *shunt-output* scheme) will incur more energy loss. Second, in the *bridge-connection* scheme, a lower V_i will reduce the energy loss in the auxiliary circuit for negative transients while the *shunt-output* scheme is still applying 4 to 6 V in V_{as}, incurring a constant energy loss. In this case, when V_i is lower than 6 V, the *bridge-connection* scheme is preferred.

3.6.3 Comparison of Intruding Auxiliary Circuits

For the purpose of testing, we apply step-up and step-down load transients of 5 A to a standard buck converter under current-mode control with and without an *intruding* auxiliary circuit. The transient waveforms of v_o and i_L of the regulated

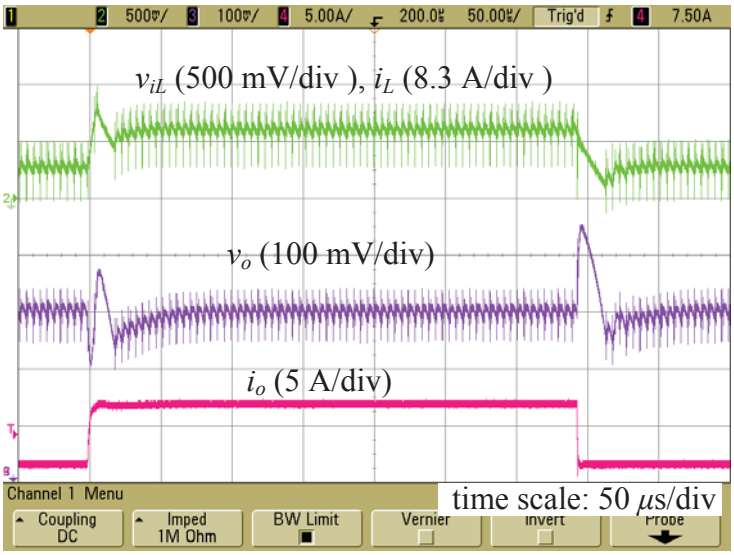
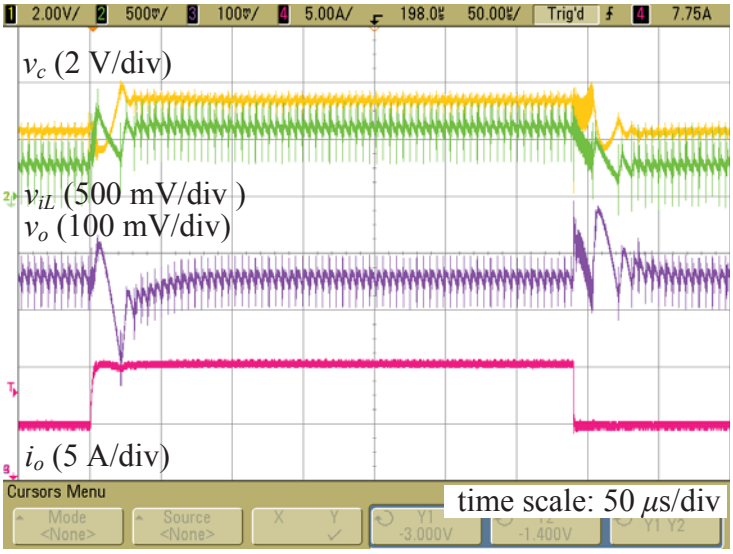


Figure 3.21: Response under application of 5 A load transients of buck converter without the auxiliary circuit.

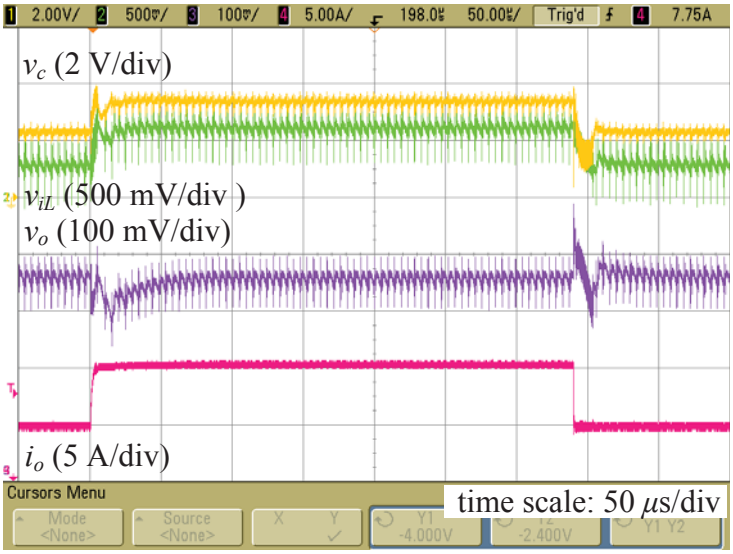
buck converter are shown in Fig. 3.21. A 160 mV fluctuation in v_o has been observed at the instant of application of a 5 A step-down transient. Auxiliary circuits using the two mentioned *intruding* schemes (as given in Section 3.4.2) are implemented, and the measured waveforms are given in Figs. 3.22 and 3.23. A reduced voltage fluctuation in v_o has been observed for these cases.

Moreover, when the intruding scheme is implemented by brute-force switching of the switch-signal, voltage overshoot can be suppressed only during the active period of the auxiliary circuit, but the switch control signal of the main PWM controller is still in the transition stage. Hence, a secondary transient occurs and is marked in Fig. 3.23(a), where the control signal v_c and the current signal v_{iL} are highlighted to illustrate this mechanism.

On the other hand, for the implementation using the feedforward scheme, we observe from Fig. 3.23(b) that v_c has been appropriately changed by the feedforward signal which results in i_L moving to the new operation point with an expected amount of voltage fluctuation. Hence, the feedforward scheme is suitable for tackling fast load transients in converters under current-mode control.

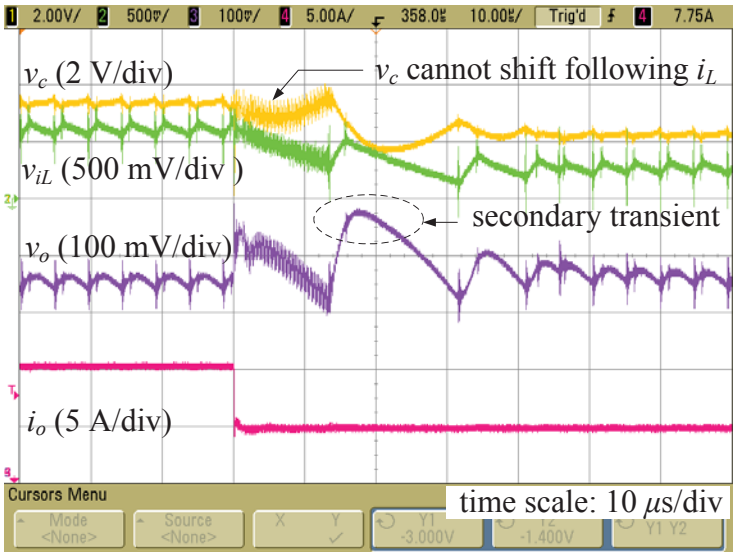


(a)

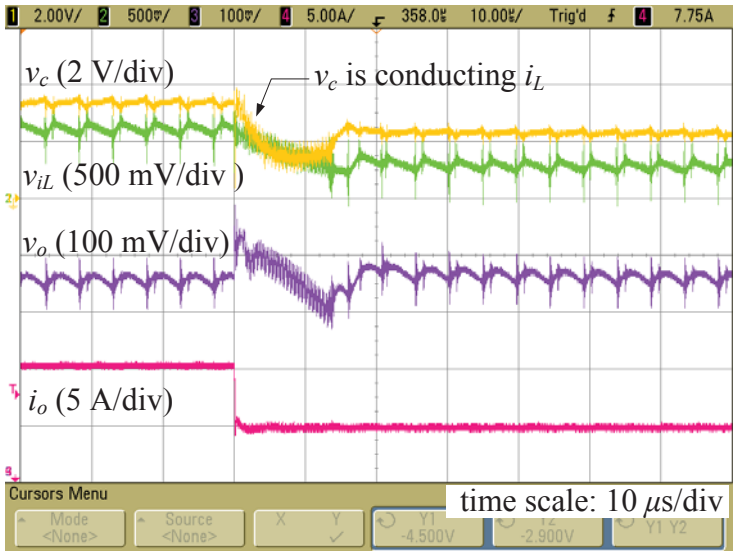


(b)

Figure 3.22: Waveforms under application of 5 A load transients for buck converter with the auxiliary circuit achieving intruding scheme by (a) switching of switch-signal and (b) feedforwarding



(a)



(b)

Figure 3.23: Enlarged control signals under application of 5 A load transients for buck converter with the auxiliary circuit achieving intruding scheme by (a) switching of switch-signal and (b) feedforwarding.

We omit the experimental validation of the load-informed schemes here, as a more detailed exposition will be provided in Chapter 5 and the experimental prototype would involve a substantially different setup in order to illustrate the advance provision of load information in such schemes.

3.7 Existing Circuits Under the Proposed Classification

The systematic classification of auxiliary circuits presented above provides a convenient framework for comparison of various types of auxiliary circuits. Specifically, it would be useful for circuit designers in deciding on the use of a specific circuit style or control method if the the various auxiliary circuits can be compared in terms of their efficiency, circuit and control complexity, possible applications, along with some existing implementations.

In Table 3.5, we provide a tabular comparison of the auxiliary circuits categorized under the proposed classification, i.e., types of power devices, connection styles, control methods, and load information availability, and make specific reference to their efficiency, complexity and possible applications. Our aim is to provide circuit designers a practical guideline for selecting auxiliary circuits and control methods for their specific applications. For instance, if a simple low-cost method is needed to enhance the transient response of a power supply feeding a non-computer load, a bridge-connected linear current source with non-intruding control would be adequate. On the other hand, a shunt-connected switching current source with an intruding control would be very desirable for a microprocessor load that can provide load profile information.

Table 3.5: Comparison of Auxiliary Circuits for Practical Design Applications

Classification	Types	Power loss	Complexity	Applications (load conditions)	Existing implementations (references)
Power devices used	linear current source	high	simple	• low transient current • low transient repetition rate • integrated on-chip	[40, 39, 42, 41, 48, 52, 51, 53]
	switching current source	low	complex	• high transient current • high transient repetition rate • based on discrete parts	[60, 45, 44, 47, 46, 43, 57, 56, 54, 55, 61, 62, 58]

Table 3.5 – Continued from the previous page

Classification	Types		Power loss	Complexity	Applications (load conditions)	Existing implementations (references)
Connection styles with the power supply and load	bridge connection		related to V_i/V_o	simple	• non-isolation applications • low V_i/V_o ratio	[40, 39, 42, 41, 60, 44, 61, 62, 58]
	shunt connection		low	complex	• isolation or non-isolation • high V_i/V_o ratio	[48, 51, 52, 45, 47, 46, 43, 57, 56, 54, 55]
Control methods	non-intruding		high	simple	• existing main power supply not modifiable	[40, 39, 42, 44, 45]
	intruding	brute-force switching of switch signal	low	complex	• main power supply with voltage mode control and modifiable switch driving	[60, 61, 58, 62] [47, 43, 57, 56, 54]
		injecting feedforward signal	low	complex	• main power supply with current mode control and non-modifiable switch driving	[48, 51, 52, 46]

Table 3.5 – Continued from the previous page

Classification	Types	Power loss	Complexity	Applications (load conditions)	Existing implementations (references)
Load information availability	available (load-informed)	low	simple	• computer or other intelligent loads with advance step change information	[58, 59]
	not available	high	complex	• no limitation on the load	[48, 51, 52, 40, 39, 42, 41, 60, 44, 61, 62, 45, 47, 46, 43, 57, 56, 54, 55, 53]

3.8 Summary

In the chapter, we present a classification of auxiliary circuit schemes for tackling fast load transients in switching power supplies. We first consider the construction of auxiliary circuits in terms of the way in which they are connected to the load and the main power supply, and also the interaction of the auxiliary circuit and the control loop of the main converter. Furthermore, we consider a classification based on a new design paradigm which has emerged from the recent research in load profile prediction in computer and microprocessor loads. Under this new paradigm, auxiliary circuits may receive advance load information and hence are able to tackle the transients by appropriately pre-energizing themselves. A comparison of the characteristics of the various schemes is discussed. Our study provides practical design pathways for selecting the appropriate kinds of auxiliary circuits for the applications concerned.

Chapter 4

Transients Mitigation by Using Auxiliary Circuits

4.1 Introduction

There is a growing demand for ultrafast-response dc/dc converters [3]. Many effective control solutions, such as the one-cycle control [23], sliding mode control [71], minimum-time geometric control [21], time-optimal control [25], boundary control [18], nonlinear control [27, 72, 73], etc., have been applied to dc/dc converters to meet such an objective. However, for a general-purpose converter operating under a large step load change (hundreds of A per microsecond), no effective control scheme can prevent voltage deviations from appearing at the output [62]. For most critical applications, a very large electrolytic capacitor is typically required to achieve a satisfactory suppression of the overshoots. This may significantly increase the cost and the size of the converter, and may also reduce its lifetime and reliability.

Different approaches of dealing with such kinds of load disturbance for the converters have been presented in references [35, 36, 37, 39, 40, 42, 48, 49, 52, 51, 45, 44, 47, 43, 57, 56, 55, 60, 74, 75]. One interesting approach is to instan-

taneously change the value of the storage inductance corresponding to a load change to achieve the necessary load current change which occurs at a high slew rate [35, 74, 36]. By varying the inductance, the output voltage overshoot can be alleviated when load disturbances occur. While high efficiency is achievable with the proposed method, the complicated transformer or tapped inductor design is the main drawback of this method [57].

Another approach of handling large transients is to parallel a linear controllable current source to the output port to compensate the transient current [39, 40, 42]. The transient overshoot is largely suppressed at the expense of reduced efficiency due to the use of a linear current source.

A third possible approach is through the use of circuit augmentation [48, 49, 52, 51], which provides an effective means of achieving ultrafast load transients. With this scheme, an extra energy path is directly added to the converter without altering the slew rate of the inductor. The combined use of geometric digital control and circuit augmentation enhances the converter's response so as to handle very fast load changes. But to deal with step load changes, resistors of small value and high power ratings are needed, resulting in inevitable power loss.

A fourth approach is to use specialized control strategy which includes a switching auxiliary circuit [60, 45, 44, 47, 43], in which energy can be flexibly transferred between the filter capacitor and the power source to regulate the output voltage. This is an effective way of dealing with both positive and negative load disturbances. Moreover, the power loss can be significantly reduced. In particular, when the converter operates with a low duty cycle, the overshoot caused by a positive load transient is insignificant. The approach which focuses on handling unloading transient is preferred for its high efficiency and low cost [57, 56, 55].

In this chapter, an effective active solution for suppressing transient overshoots for both positive and negative step changes in the load current, via the use of

a small low-cost auxiliary power circuit and a complementary control scheme, is proposed. With the auxiliary circuit operating as an energy buffer, a much improved transient response is achievable through the transfer of energy between its capacitor and the main dc/dc converter in the event of large load variations. Furthermore, comparing with previous methods, the features of the proposed method are:

- The auxiliary circuit is decoupled from the input and will not transfer energy from the load to the power source.
- There is no recirculation of the transient energy. Excess energy from the main converter is absorbed by the auxiliary circuit and stored in the capacitor. The energy is utilized for the positive disturbance. This is unlike previous methods where the excess energy is transferred from the output back to the input causing a recirculation of energy between the input and the output.
- The proposed method is generally applicable to all dc/dc converters because the topology is independent of the main converter. Moreover, it can be modified and applied to inverter systems.

4.2 Fast Transient Recovery Using Auxiliary Circuits

An essential idea of the proposed method of tackling fast load transients is the use of an auxiliary circuit. It includes an energy storage element which can provide bidirectional current flow to and from the load. Fig. 4.1 shows an overview of the concept. Here, the auxiliary circuit operates only when it is required, and the circuit is fully decoupled from the input terminal.

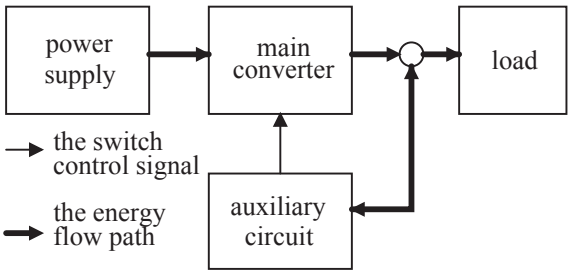


Figure 4.1: Converter with an auxiliary circuit.

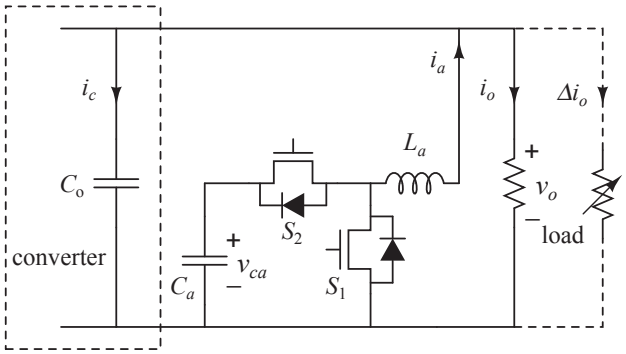


Figure 4.2: Schematic diagram of auxiliary circuit.

To achieve bidirectional energy buffering of the converter that can deal with both positive and negative transients, a bi-directional buck/boost converter [76] is adopted as the auxiliary circuit. It comprises two MOSFET switches, one inductor and one capacitor, as shown in Fig. 4.2. The power rating of all the components are dependent on the load step value and the frequency of the step changes since the circuit only operates in the event of a load step. Generally speaking, the current rating of the components is much lower than that of the main converter [46]. Therefore, low-power, low-cost components can be used.

When S_1 and S_2 are turned off, the auxiliary circuit has no effect on the converter. When S_1 is turned on and off alternately, the polarity of i_a will be negative and current will be pumped from the output port of the main converter into C_a, thereby increasing its stored charge. Conversely, when S_2 is activated, i_a will be positive which will release the charge from C_a to the load, thereby decreasing the energy storage level. Essentially, the auxiliary circuit will operate

only in the following two conditions.

1. When there is a difference between the load and the inductor current of the main converter during load transients, the auxiliary circuit will operate to control the output current, i_a, to provide/absorb the current deficit/surplus.

2. After each load disturbance, the auxiliary circuit needs to regulate the energy stored in its capacitor (C_a) to deal with all possible transients in future. In this case, the voltage of C_a will become the reference of the auxiliary circuit operation. The duty cycles of the two switches will be set very small to generate a small i_a so that there is minimum interference on the converter's steady-state operation. Note that the the main energy dissipation in the switches only occurs during transients.

4.3 Operating Mechanism of the Auxiliary Circuit

The proposed control method involves the control of the output current of the auxiliary circuit (i_a) and its reservoir capacitor voltage (v_{ca}) which represents the energy storage level. The first aspect of the control is to ensure that the voltage overshoot of the main converter is minimized and tight output voltage regulation is achieved. The second aspect is to ensure that the reservoir capacitor of the auxiliary circuit has sufficient storage energy as well as volume for any predictable load disturbances.

4.3.1 Output Current Control

Fig. 4.3 shows a set of normalized waveforms illustrating the key variables of the main converter and its auxiliary circuit. I_{os} and I_{ol} represent the desired steady-state levels of the load transients, with I_{os} being the lower level and I_{ol} the higher

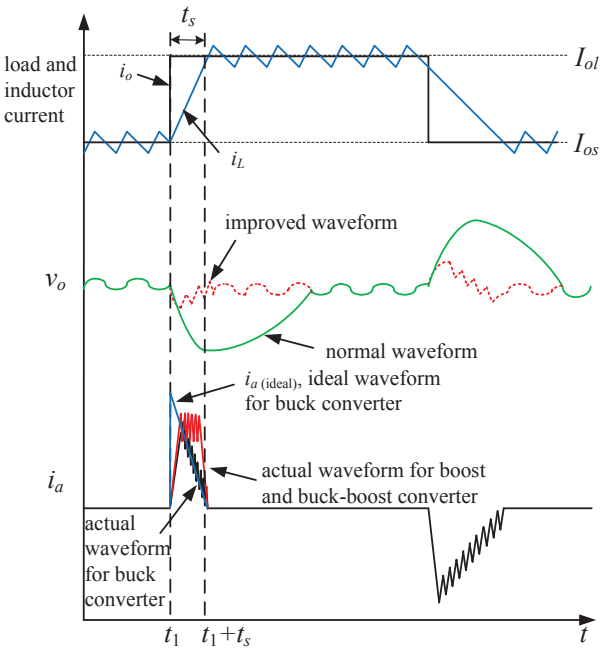


Figure 4.3: Normalized waveforms of key variables.

current level. When the load experiences a sudden step change from I_{os} to I_{ol} at time t_1, the fastest response is to lock the duty cycle at "1" making the inductor current rise to the new operating point in time duration t_s. Conversely, when the load drops, the duty cycle is locked at "0". Clearly, the change of the inductor current is much slower than the change of the load current. Hence, there is a momentary shortage of energy that can be delivered from the inductor to the load. The proposed strategy is to supply this transient shortage using energy from the reservoir capacitor of the auxiliary circuit during t_s. Specifically, a very small inductor and a high-speed switch are used to trace an "ideal" transient output current, denoted as $i_a(t)$, which is varying with time, according to the circuit parameters and transient specifications.

For example, when a load connecting to the buck converter increases from I_{os} to I_{ol} instantly at t_1, as shown in Fig. 4.3, the inductor current rises at a slew rate of $(V_i - V_o)/L$. In this time period, the inductor is unable to deliver current to the load at the required level. Hence, to eliminate the large voltage

dip at v_o, an extra current denoted conceptually as $i_{a(ideal)}$ as shown in Fig. 4.3 is needed. The expression of this current as a function of time is $i_{a(ideal)} = I_{ol} - [I_{os} + (t - t_1)(V_i - V_o)/L]$. Here, the actual current i_a is controlled by S_2 and it will track closely the ideal current $i_{a(\text{ideal})}$. A smaller L_a or a higher switching frequency can reduce the overshoot ripple of the output voltage.

For different converters undergoing step-up and step-down load changes, the value of i_a can be found using the formulas given in Table 4.1, under the condition that a step load appears at t_1. Here, i_a is only defined for the time duration $[t_1, t_1 + t_s]$, where t_s represents the transition time duration and it can be obtained from

$$t_s = \frac{(I_{ol} - I_{os})}{k_L}, \tag{4.1}$$

where k_L represents the current slew rate of the inductor and can be found using Table 4.1. To produce the expected i_a, the variables t_1, t_s and $i_{a(ideal)}$ must be known. Also, t_1 is detectable from the circuit and t_s is proportional to the step change of I_{ol} to I_{os}. If i_a is precisely equal to its ideal value, the current of the filter capacitor of the main converter, denoted as i_c, will be equal to zero. This means that i_c can be used as the error signal of i_a relative to its ideal value for the purpose of control.

4.3.2 Reservoir Capacitor Voltage Control

When the auxiliary circuit operates to deal with the load disturbances, the energy stored in C_a changes in a passive and uncontrollable manner, as shown by the dashed line in Fig. 4.4. Over time, the net input power of the reservoir capacitor may not be zero. It is necessary that the auxiliary circuit operates actively to regulate the reservoir capacitor voltage after handling each load disturbance, as shown by the solid blue line in Fig. 4.4. Otherwise, the storage energy or volume of the capacitor may not be sufficient to handle future disturbances.

Table 4.1: Ideal Calculation of i_a for Step-Up Load ($i_o = I_{os} \rightarrow I_{ol}$) and Step-Down Load ($i_o = I_{ol} \rightarrow I_{os}$)

Variable		Buck	Boost	Buck-boost
i_L	step-up load	$I_{os} \rightarrow I_{ol}$	$I_{os} \cdot \frac{1}{1-D} \rightarrow I_{ol} \cdot \frac{1}{1-D}$	$I_{os} \cdot \frac{1}{1-D} \rightarrow I_{ol} \cdot \frac{1}{1-D}$
	step-down load	$I_{ol} \rightarrow I_{os}$	$I_{ol} \cdot \frac{1}{1-D} \rightarrow I_{os} \cdot \frac{1}{1-D}$	$I_{ol} \cdot \frac{1}{1-D} \rightarrow I_{os} \cdot \frac{1}{1-D}$
k_L	step-up load	$\frac{V_i - V_o}{L}$	$\frac{V_i}{L}$	$\frac{V_i}{L}$
	step-down load	$\frac{-V_o}{L}$	$\frac{V_i - V_o}{L}$	$\frac{-V_o}{L}$
$i_{a(ideal)}$	step-up load	$I_{ol} - [I_{os} + k_L(t - t_1)]$	I_{ol}	I_{ol}
	step-down load	$I_{os} - [I_{ol} + k_L(t - t_1)]$	$I_{os} - \left[I_{ol} \cdot \frac{1}{1-D} + k_L(t - t_1)\right]$	$I_{os} - \left[I_{ol} \cdot \frac{1}{1-D} + k_L(t - t_1)\right]$

Table 4.2: Decremental/Incremental Energy Stored in the Capacitor of the Auxiliary Circuit for a Step Load Change

	ΔE_1 (Step up)	ΔE_2 (Step down)
Buck	$\frac{1}{2}\left(\frac{I_{ol}}{I_{os}} - 1\right)^2 I_{os}^2 \frac{LD}{1-D}$	$\frac{1}{2}\left(\frac{I_{ol}}{I_{os}} - 1\right)^2 I_{os}^2 L$
Boost	$\frac{I_{ol}}{I_{os}}\left(\frac{I_{ol}}{I_{os}} - 1\right)\frac{I_{os}^2 L}{(1-D)^2}$	$\frac{1}{2}\left[\left(\frac{I_{ol}}{I_{os}} + 1\right)\frac{1}{1-D} - 2\right]\left(\frac{I_{ol}}{I_{os}} - 1\right)\frac{I_{os}^2 L}{D(1-D)}$
Buck-boost	$\frac{I_{ol}}{I_{os}}\left(\frac{I_{ol}}{I_{os}} - 1\right)\frac{I_{os}^2 DL}{(1-D)^2}$	$\frac{1}{2}\left[\left(\frac{I_{ol}}{I_{os}} + 1\right)\frac{1}{1-D} - 2\right]\left(\frac{I_{ol}}{I_{os}} - 1\right)\frac{I_{os}^2 L}{1-D}$

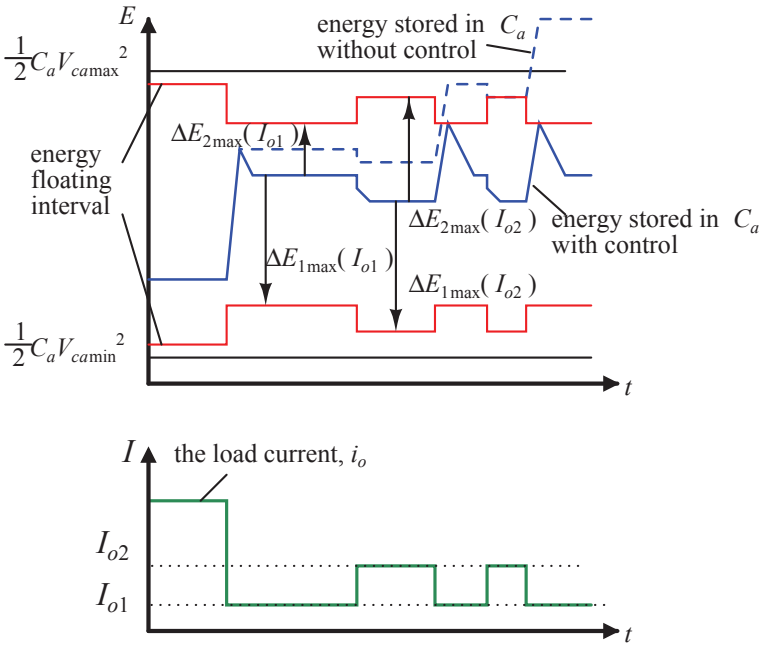


Figure 4.4: Reservoir capacitor voltage and the energy balance waveforms.

In other words, the capacitor must always be capable of satisfying the energy diverting requirement for all possible load disturbances. For any step load disturbance occurring at t_1, the energy change in C_a during t_s can be calculated as

$$\Delta E = \int_{t_1}^{t_1+t_s} V_o|i_a(t)|dt. \tag{4.2}$$

Correspondingly, ΔE_1 and ΔE_2 are used to represent the value of ΔE, when the auxiliary circuit is operating for a step-up (I_{os} to I_{ol}) or step-down (I_{ol} to I_{os}) load disturbance. After expanding (4.2) with the expression of $i_{a(ideal)}$ given in Table 4.1, ΔE_1 and ΔE_2 can be derived and are given in Table 4.2.

For any converter, there is a specified range of the output current, e.g., from $I_{o\min}$ to $I_{o\max}$. The converter can operate anywhere within this range and it is possible to shift from the current level, I_o, to a new level within $[I_{o\min}, I_{o\max}]$ anytime. Therefore, it is reasonable to assume that the maximal ΔE_1 or ΔE_2 will appear when the load current I_o steps to $I_{o\max}$ or $I_{o\min}$, and they can be defined as $\Delta E_{1\max}$ and $\Delta E_{2\max}$. Furthermore, the range of the operating voltage

of the reservoir capacitor can be specified as a lower bound, $V_{ca\,\min}$, which must not be less than v_o of the main converter, and an upper bound, $V_{ca\,\max}$, which must not exceed the voltage rating of the capacitor.

Hence, for every I_o, a suitable V_{ca} can be found. The energy released by the capacitor due to the change of V_{ca} to $V_{ca\,\min}$ will be able to facilitate the load transient of I_o stepping to $I_{o\,\max}$. Similarly, the energy storage volume gained by the capacitor from V_{ca} changing to $V_{ca\,\max}$ will be able to serve the load step of I_o changing to $I_{o\,\min}$. Hence, v_{ca} can be written as a function of i_o, i.e.,

$$v_{ca}(i_o) = \sqrt{\frac{(V_{ca\,\min}^2 + V_{ca\,\max}^2)}{2} + \frac{1}{2C_a}\left[(I_{o\,\max} - I_o)^2 \frac{LD}{1-D} - (I_o - I_{o\,\min})^2 L\right]}. \tag{4.3}$$

Details of the mathematical derivations and principles of v_{ca} control can be found in Appendix A.1.

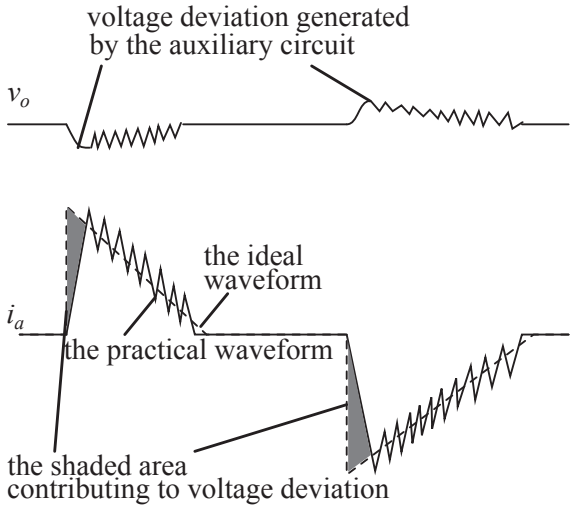


Figure 4.5: Current and voltage waveforms during load changes.

4.4 Performance Analysis and Design Guidelines

Due to the finite slew rate of i_a, it is not possible to achieve a perfect current step. There is always a small voltage deviation right after the onset of the load

disturbance, before the auxiliary current reaches the required level, as illustrated in Fig. 4.5. In this section, the voltage deviation with respect to the reference ($v_{t\text{aux}}$) will first be analyzed. Then, an analysis involving the switching frequency (f_{as}), ripple current ($I_{r\text{aux}}$), and voltage ($v_{r\text{aux}}$) of the auxiliary circuit, will be presented. A guideline for choosing the circuit components will be provided.

4.4.1 Possible Voltage Deviation

A practical auxiliary circuit cannot provide a current that exhibits the ideal waveform. By assuming that k_c is the slew rate of the inductor when it is being de-energized and k_{aux} represents the slew rate of i_a, the time period taken for the auxiliary circuit current to catch up with the load step is $\frac{I_{ol}-I_{os}}{k_c+k_{\text{aux}}}$. The shaded area in Fig. 4.5, which represents $v_{t\text{aux}}$, can be expressed as

$$\begin{aligned} v_{t\text{aux}} &= \frac{1}{C_o}\int_{t_1}^{t_1+\frac{I_{ol}-I_{os}}{k_c+k_{\text{aux}}}} |(k_c+k_{\text{aux}})(t-t_1)-i_a|\ dt \\ &= \frac{1}{2C_o(k_c+k_{\text{aux}})}(I_{ol}-I_{os})^2, \end{aligned} \tag{4.4}$$

where for a boost or buck-boost converter, when the load is undertaking a step-up change, the current flowing to the load from the inductor will always be zero. Hence, k_c is equal to 0. Otherwise, $k_c = k_L$, which is found in Table 4.1. Here, $k_{\text{aux}} = (v_{ca} - V_o)/L_a$ or $k_{\text{aux}} = -V_o/L_a$ is used in a step-up or step-down load operation. The inductance L_a affects the voltage deviation and can be determined from the overshoot limit, $v_{t\text{aux}\,\max}$.

Since the auxiliary circuit is a switching circuit, the maximum value of the switching frequency, $f_{as\,\max}$, is limited by the specification and also the size of the inductor, i.e.,

$$f_{as} \approx \left[I_{r\text{aux}}L_a\left(\frac{1}{V_{ca}-V_o}+\frac{1}{V_o}\right)\right]^{-1} = \frac{V_o(V_{ca}-V_o)}{I_{r\text{aux}}L_aV_{ca}}, \tag{4.5}$$

where $I_{r\text{aux}}$ is the ripple band selected by the designer. This ripple band induces a voltage ripple at the output port directly which can be expressed as

$$v_{r\text{aux}} = \frac{I_{r\text{aux}}}{8C_o f_{as}}. \tag{4.6}$$

4.4.2 Components Value and Guidelines

With the chosen $v_{t\text{aux}\max}$, $I_{r\text{aux}}$ and $f_{as\max}$, and using (4.4) and (4.5), we can derive the design conditions of the inductor as

$$\begin{cases} L_a \le \min\left\{ \dfrac{V_{ca\min} - V_o}{\dfrac{\Delta I_{o\max}^2}{2C_o v_{t\text{aux}\max}} - k_c}, \dfrac{V_o}{\dfrac{\Delta I_{o\max}^2}{2C_o v_{t\text{aux}\max}} + k_c} \right\} \\ L_a \ge \dfrac{V_o(V_{ca\max} - V_o)}{I_{r\text{aux}} f_{as\max} V_{ca\max}} \end{cases}. \tag{4.7}$$

Note that a larger inductance relates to a lower switching frequency, but a larger voltage deviation. If the design specification requires a very small power dissipation, the inductance should be as high as possible but within the upper limit.

The capacitance of the auxiliary circuit is governed by the required size of the energy storage and its voltage range. As presented above, the energy floating interval is a variable corresponding to $i_o \in [I_{o\min}, I_{o\max}]$. It must always be within the energy bound of the capacitor, i.e., less than $\frac{1}{2}C_a(V_{ca\max}^2 - V_{ca\min}^2)$. The capacitor requirement is given as

$$C_a \ge \max_{i_o \in [I_{o\min}, I_{o\max}]} \left\{ \frac{\Delta E_{1\max} + \Delta E_{2\max}}{\frac{1}{2}\left(V_{ca\max}^2 - V_{ca\min}^2\right)} \right\}, \tag{4.8}$$

from which it can be observed that there is a trade-off between the level of the capacitor voltage and its size. If a smaller capacitor is expected, V_{ca} must be sufficiently high, which will increase the leakage current and the voltage rating

of the relevant components. Conversely, the choice of a lower voltage rating will require the use of a larger capacitor.

4.5 Simulation and Experimental Verifications

The proposed scheme is validated through simulations and experiments on a synchronous buck converter. In this section, the experimental setup is described and the relevant results are reported.

4.5.1 Simulation Results

The specification of the buck converter for simulation and the experimental prototype is shown in Table 4.3. The switching frequency and the value of the inductor are chosen based on consideration of the current ripple. The capacitor value is selected based on the ripple requirement of 50 mV. A type III compensator with voltage-mode control is utilized in this converter. With a maximum converter's voltage deviation of 0.15 V, a maximum auxiliary circuit's switching frequency of 1.5 MHz, and a maximum auxiliary circuit's current ripple of 4 A, the parameters of the auxiliary circuit can be calculated from the design procedure as: $v_{ca} \in [8.5\ V, 10\ V]$, $L_a = 0.42\ \mu$H, $C_a = 40\ \mu$F, and the regulation formula as $v_{ca} = 0.19\sqrt{(i_o + 81.58)(32.74 - i_o)}$ by using (4.3). Using a load step interval of 10 ms, the permitted voltage ripple during v_{ca} regulation is 10 mV. Thus, t_{w} is set as 0.12 μs and the operation interval is set as 16 μs.

4.5.2 Simulation Results

The specification of the buck converter for simulation and the experimental prototype is shown in Table 4.3. The switching frequency and the value of the inductor are chosen based on consideration of the current ripple. The capacitor

Table 4.3: Design Specifications of Synchronous Buck Converter

Description	Parameter
Input voltage	12 V
Output voltage	5 V
Inductor value	10 μH
Capacitor value	47 μF
Switching frequency	200 kHz
Output current	1 A — 10 A
Controller chip	IRU3037 (voltage mode)

Table 4.4: Transfer Function of the Compensator in the Linear PWM Controller

C_o value	Transfer function of the compensator
47 μF	$H(s) = \frac{8.3 \times 10^6 (s + 3.5 \times 10^4)(s + 4.7 \times 10^4)}{s(s + 6.3 \times 10^5)(s + 2.3 \times 10^6)}$
470 μF	$H(s) = \frac{9.8 \times 10^6 (s + 1.0 \times 10^4)(s + 1.4 \times 10^4)}{s(s + 6.0 \times 10^5)(s + 8.1 \times 10^4)}$
1000 μF	$H(s) = \frac{10.5 \times 10^6 (s + 0.7 \times 10^4)(s + 1.0 \times 10^4)}{s(s + 6.0 \times 10^5)(s + 4.5 \times 10^4)}$
1500 μF	$H(s) = \frac{11.3 \times 10^6 (s + 0.6 \times 10^4)(s + 0.8 \times 10^4)}{s(s + 6.0 \times 10^5)(s + 3.0 \times 10^4)}$
3300 μF	$H(s) = \frac{13.5 \times 10^6 (s + 0.4 \times 10^4)(s + 0.5 \times 10^4)}{s(s + 6.0 \times 10^5)(s + 1.4 \times 10^4)}$

Table 4.5: Parameters of the Auxiliary Circuit

Description	Parameter
$f_{as\,\max}$	1.5 MHz
$I_{r\mathrm{aux}}$	4 A
v_{ca}	$[8.5\ V, 10\ V]$
L_a	0.42 μH
C_a	40 μF
v_{ca} regulation formula	$v_{ca} = 0.19\sqrt{(i_o + 81.58)(32.74 - i_o)}$

value is selected based on the ripple requirement of 50 mV. A type III compensator (parameters shown in Table 4.4) with voltage-mode control is utilized in this converter. The unity-gain bandwidth is set as 50 kHz. With a maximum

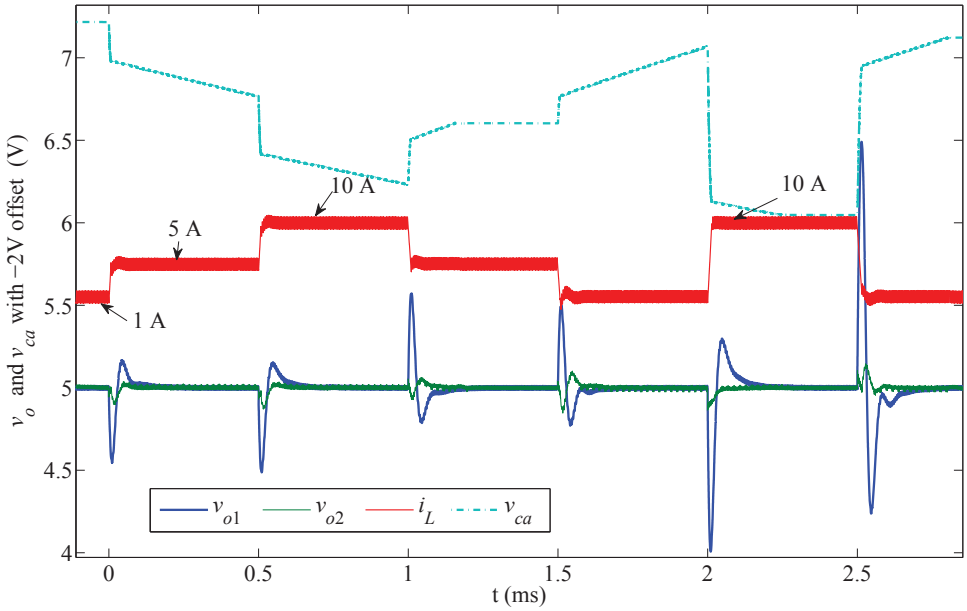


Figure 4.6: Simulated waveforms of the synchronous buck converter operating with the auxiliary circuit (V_{o2}, i_L and V_{ca}), comparing to that without the auxiliary circuit (V_{o1}).

converter's voltage deviation of 0.15 V, the parameters of the auxiliary circuit can be calculated from the design procedure and given in Table 4.5 (maximum auxiliary circuit's switching frequency and current ripple are arbitrarily chosen). Using a load step interval of 10 ms, the permitted voltage ripple during v_{ca} regulation is 10 mV. Thus, t_w (defined and explained in Appendix A.1) is set as 0.12 μs and the operation interval is set as 16 μs. To validate the effect of the proposed auxiliary circuit, two simulations (one with the auxiliary circuit and the other without the auxiliary circuit) have been performed with MATLAB simulink package, and the results are given in Fig. 4.6 for comparison. In the figure, v_{o1} is the output voltage of the converter without the auxiliary circuit and v_{o2} is that with the auxiliary circuit. The simulated waveforms illustrate that when load disturbances appear at 0 ms, 0.5 ms, 1.0 ms, etc., the transient voltage is greatly reduced (having a maximum reduction of 90%) with the use of the auxiliary circuit.

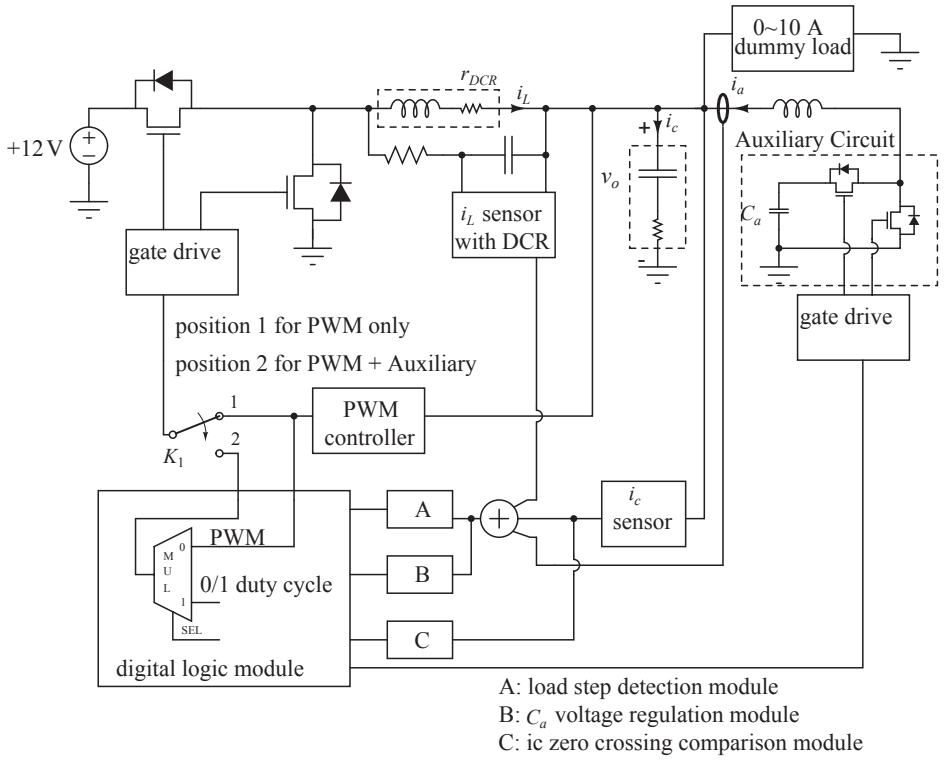


Figure 4.7: The block diagram of the whole prototype.

4.5.3 Experimental Prototype

The experimental prototype is constructed using the same converter and the auxiliary circuit design adopted in the simulation. The block diagram of the prototype is given in Fig. 4.7. The detailed schematic diagrams are given in Appendix A.2.

The inductor current is measured by its body DC resistance (DCR) and the related circuits [77]. There are no traditional resistor-sensors which will incur extra energy losses, while the inductor current is read from the DCR. The idea is to shunt a series RC network onto the inductor body. The time constant of the RC network should match that of the LR network of the inductor body (inductance and DCR). The signal representing i_L is constructed and labeled as "InducSens" in Fig. A.2.

The filter capacitor current (i_c) is sensed by a shunting RC network which

is placed alongside C_o. While a capacitor of 47 μF with an equivalent series resistance (ESR) of 4 mΩ is used, an RC network of 47 nF and 4 Ω is applied (see Fig. A.2). The voltage on the 4 Ω resistor is equal to that on the ESR of C_o. Then, the re-scaled and inverted voltage of the ESR of C_o is labeled as CapSens in Fig. A.2.

The sensed i_L, i_c and i_a are summed by the "Adding Unit Circuit" which is labeled in Fig. A.3. The "Adding Unit Circuit" output which is labeled as "LoadCurrentSens" represents the load current i_o and is fed into two blocks, denoted as "A" and "B" in Fig. 4.7.

Block A is used to detect load transients. The output signals of the block, "LoadStep-Up" or "LoadStep-Down", will synchronously generate a negative pulse, when a load transient occurs. The pulse width is equal to the acquired rising or dropping time of the main converter's i_L to approach its new level.

Block B generates "AuxE↑" or "AuxE↓" signals to indicate whether v_{ca} is higher, lower than or matching the reference which is the function of "LoadCurrentSens". The function realizes the regulation formula given in Table. 4.5. More details are shown in the "Reservoir Capacitor Voltage Regulation Circuits" part of Fig. A.3.

Block C is to detect the i_c zero crossing. When i_c exceeds the preset negative or positive thresholds, signals serving for step-down or step-up transients will be enabled, respectively. The above two digital signals are fed into the "Digital Logic Module". The control signals for S_1, S_2 and the main converter switch are given by the "Digital Logic Module" (see the operation principle details in Appendix A.2).

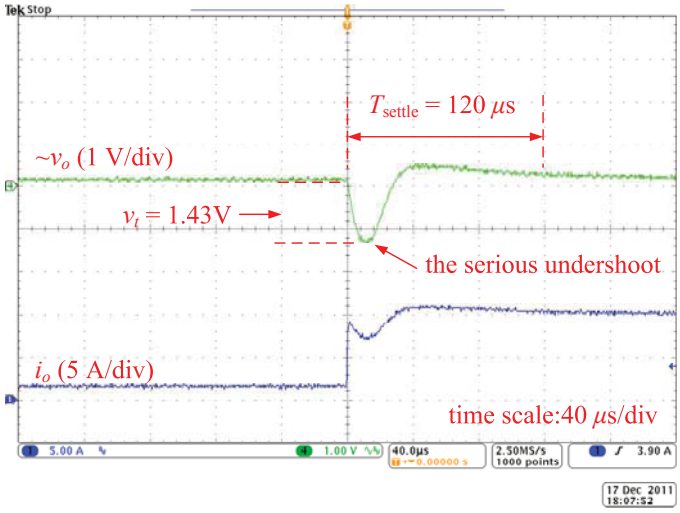
In Fig. 4.7, it can be seen that a switch K_1 has been included to switch between the choice of using or not using the auxiliary circuit. To validate the effectiveness of the proposed scheme, different values of the filter capacitance are used and the relevant compensation network parameters are optimally adjusted.

4.5.4 Experimental Results

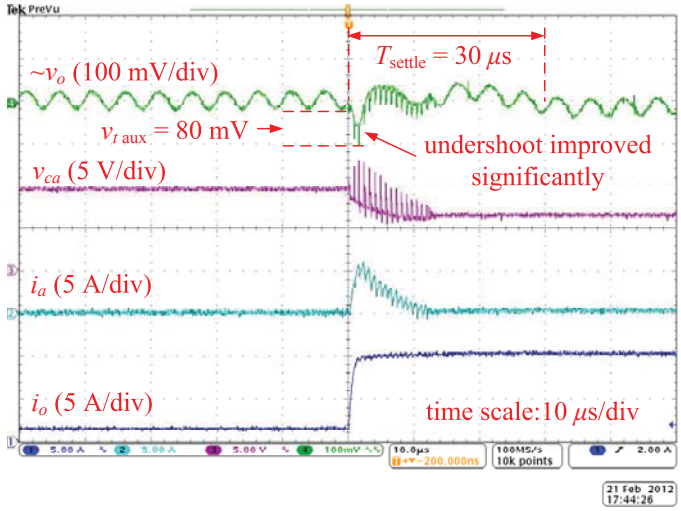
To validate the proposed solution, the synchronous buck converter is tested with different filter capacitance values. For each value of the capacitance, the compensation network is optimally tuned for the best transient performance.

Figs. 4.8 to 4.10 show the voltage and current waveforms of the buck converter with and without the auxiliary circuit for step load change between 1 A to 10 A. In Figs. 4.8(a) and 4.9(a), a large voltage overshoots of 1.4 V and 2.0 V, respectively, and long settling time of 120 μs can be observed. Comparatively, waveforms in Figs. 4.8(b) and 4.9(b) present an improved response of the synchronous buck converter using the auxiliary circuit. The voltage overshoot for step-up change is reduced to 80 mV and for step-down change to 324 mV. The settling times are 30 μs and 20 μs, respectively, for the step-up and step-down load changes. The reservoir capacitor voltage changes (between 7 V and 11 V) while the auxiliary circuit handles the transients. In Fig. 4.10, the enlarged waveforms of Figs. 4.8(b) and 4.9(b) are shown. In both cases, the switching frequency is around 1.25 MHz, which is kept within the maximum switching frequency design limit of 1.5 MHz. The current ripple at i_a is about 3 A, which is less than the specification of 4 A. The voltage overshoot is larger than the designed requirement of 0.15 V. This discrepancy can be attributed to the detection time delay (about 0.5 μs) of the load current step. The detection delays cannot be avoided, as the bandwidth of the transient detection circuit must be limited to eliminate the noise. Therefore, it still remains a technical challenge to achieve the transient detection without time delays.

To validate the effectiveness of the reservoir capacitor voltage control, a large-time-scale waveform of various transient operations is given in Fig. 4.11. In this test, the load is stepped up from 0 A to 5 A and then 10 A, and then stepped down to 5 A and back to 0 A. The process of regulating the reservoir capacitor

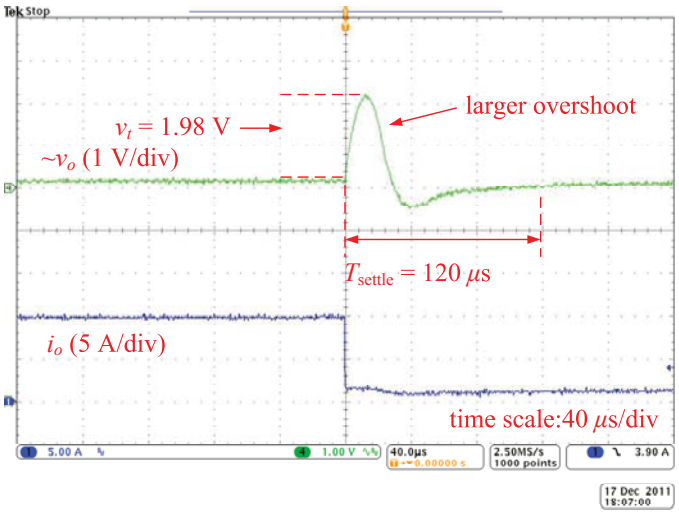


(a)

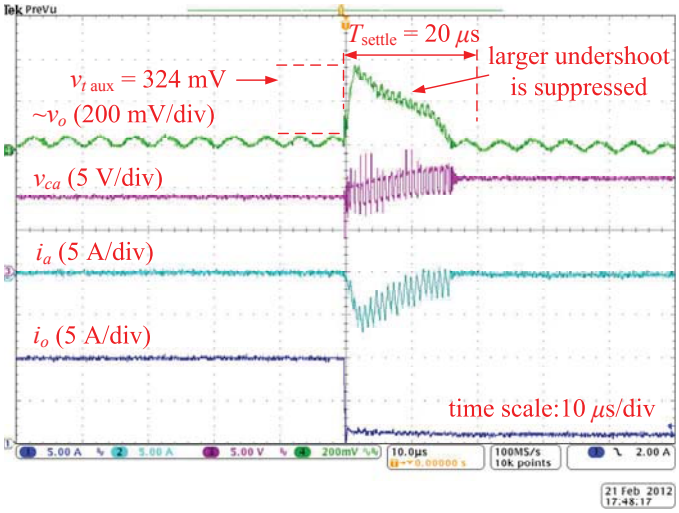


(b)

Figure 4.8: Waveforms of the buck converter using a 47 μF filter capacitor under step-up change from 1 A to 10 A (a) without the auxiliary circuit, and (b) with the auxiliary circuit.

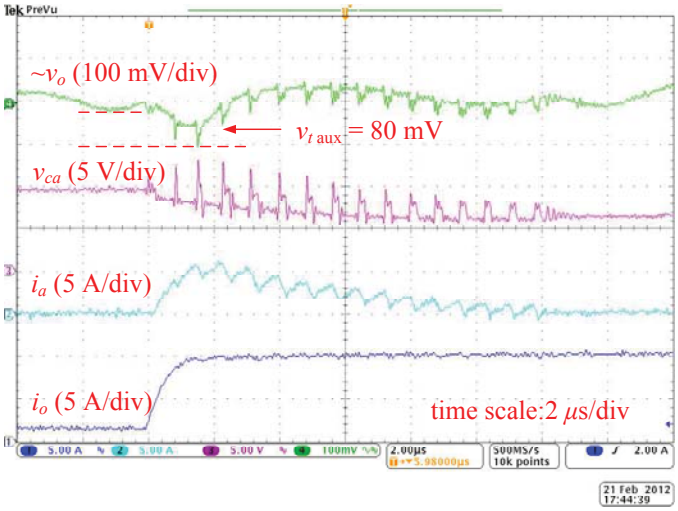


(a)

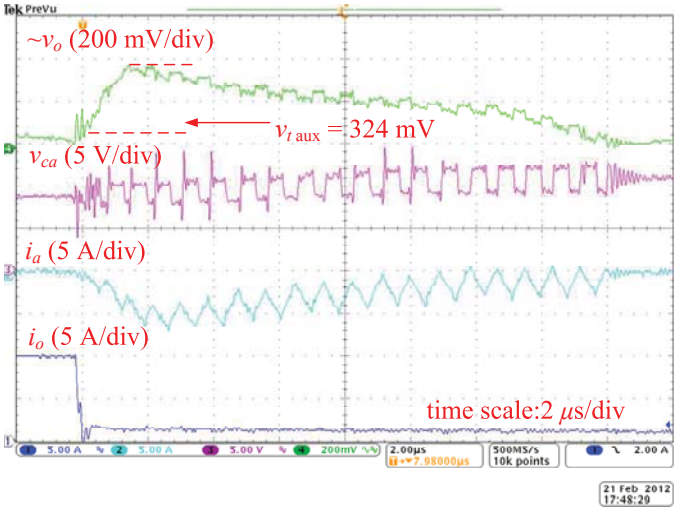


(b)

Figure 4.9: Waveforms of the buck converter using a 47 μF filter capacitor under step-down change from 10 A to 1 A (a) without the auxiliary circuit, and (b) with the auxiliary circuit.



(a)



(b)

Figure 4.10: Enlarged waveforms of the buck converter (using a 47 μF filter capacitor) for step load change between 1 A and 10 A with the auxiliary circuit in the case of, (a) step-up load, and (b) step-down load.

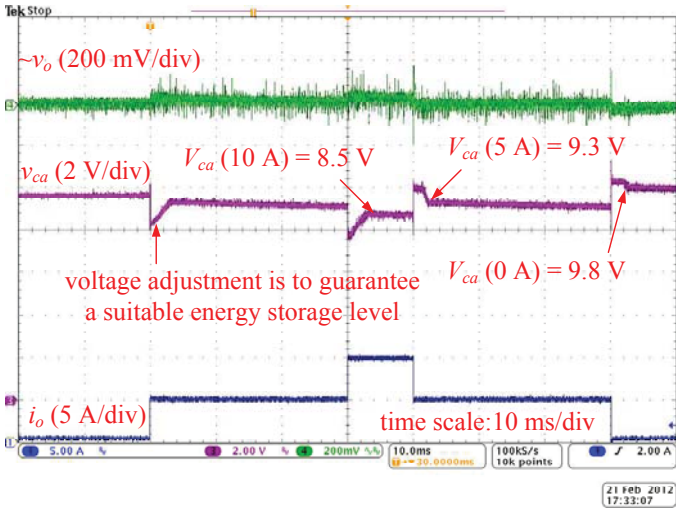


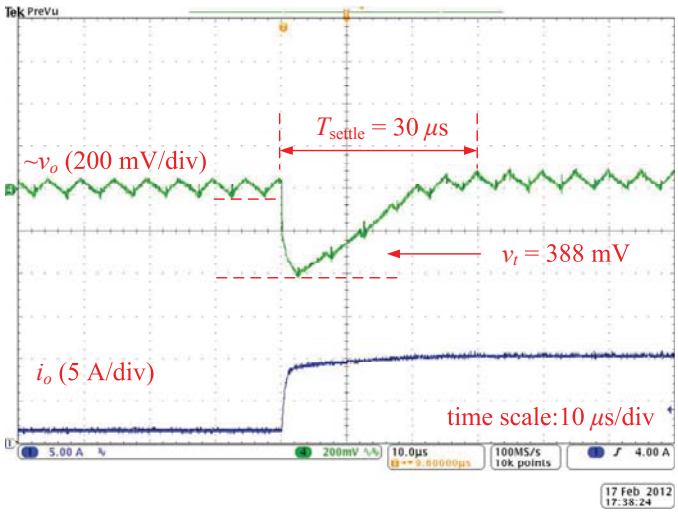
Figure 4.11: Waveform showing the effectiveness of the capacitor voltage regulation mechanism of the auxiliary circuit in maintaining energy balance of the capacitor and handling load transients.

energy can be found after the operation for each step load. The reservoir capacitor voltage is regulated to the expected value after each load changing cycle.

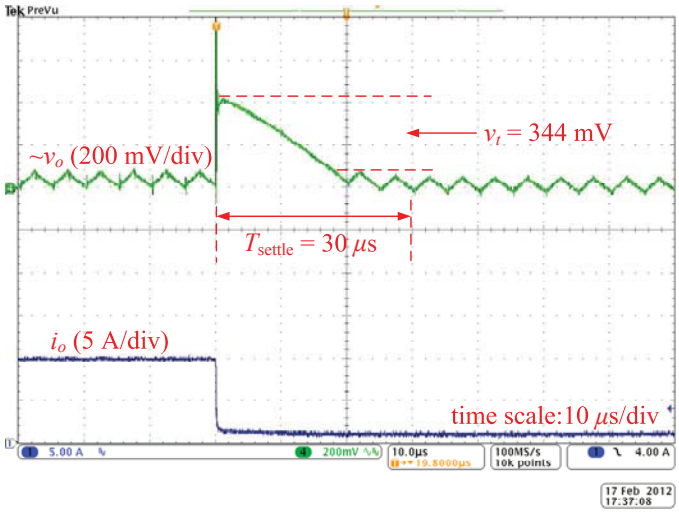
Table 4.6: Performance Comparison Between Converters with and without the Auxiliary Circuit for Different Filter Capacitance

*(load step-up: 1 A to 10 A; load step-down: 10 A to 1 A)

Prototype	Disturbance Polarity	Performance	
		Voltage Overshoot (V)	Settling Time (μs)
without auxiliary circuit	load step up	1.43	120
47 μF filter capacitor	load step down	1.98	120
with auxiliary circuit	load step up	0.080	30
47 μF filter capacitor	load step down	0.324	20
without auxiliary circuit	load step up	0.420	30
470 μF filter capacitor	load step down	0.492	30
without auxiliary circuit	load step up	0.388	30
1000 μF filter capacitor	load step down	0.344	30
without auxiliary circuit	load step up	0.214	30
1500 μF filter capacitor	load step down	0.226	32
without auxiliary circuit	load step up	0.208	32
3300 μF filter capacitor	load step down	0.240	30



(a)



(b)

Figure 4.12: Waveforms of the buck converter using a 1000 μF filter capacitor for step load change between 1 A and 10 A in the case of, (a) step-up load, and (b) step-down load.

Waveforms of the converter without the auxiliary circuit but with a 1000 μF filter capacitor are shown in Fig. 4.12. The voltage overshoots are larger and the settling times are longer than those of the converter using 47 μF capacitor with the auxiliary circuit. The experimental results of the transient voltage overshoot and settling time for all cases of capacitance values are tabulated in Table 4.6. From the table, it can be seen that for both step-up and step-down load changes, the dynamic responses are improved with the auxiliary circuit. The transient overshoot has been suppressed by at least 85% and the settling time shortened by 80%. In practice, a converter with a large voltage overshoot is not allowed. A typical practice is to increase the size of the capacitance to the point where the transient response is satisfactory. From the experimental results, it can be seen that even with an output filter capacitor of 3300 μF, the step-up overshoot is still much larger than the case of 47 μF with the auxiliary circuit. With an output filter capacitor of 1000 μF, the response of load step down is comparable to the proposed method. However, the total capacitance used with the auxiliary circuit is no more than 1/10 of 1000 μF. In the proposed method, only ceramic capacitors are used, which have a longer lifespan.

On the other hand, the auxiliary circuit controller which is implemented by discrete elements and low density ICs still occupies a relatively large amount of space. In terms of complexity and space, the traditional method of using a large C_o is more attractive than the proposed method. However, all the elements for control may be integrated into a silicon wafer with ease. Furthermore, the auxiliary circuit only operates intermittently as and when required. Hence, only the peak current value is considered for the design of the auxiliary circuit. If the load-step intervals are relatively long, thermal factors need not be considered. Then, the whole auxiliary circuit could be packaged into an integrated circuit.

Finally, an experiment on the power efficiency has been conducted with the following testing conditions:

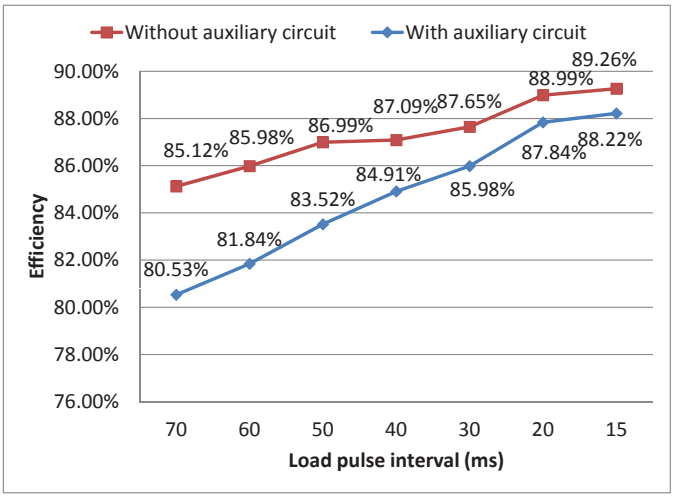


Figure 4.13: Plots of the data collected from the efficiency tests. (Power is defined as energy per unit time. The comparison of power efficiency is achieved by comparing the energy consumption which can be readily measured.)

- Load steps changing between 0 A and 10 A;
- Pulsewidth duration of the 10 A load is 10 ms;
- Pulse interval of the 10 A load varies between 15 ms to 70 ms;
- The filter capacitance of the prototype is fixed at 47 μF.

Two series of data have been collected and plotted as given in Fig. 4.13. It can be observed that with the auxiliary circuit, the efficiency is a few percent lower. This is the price to pay for an improved transient performance. It can also be observed that with a shorter pulse interval, the efficiency between the converter with and without the auxiliary circuit is closer (about 1%). This means that the amount of power loss is approximately the same. The reservoir capacitor leakage current and the driving circuits may be the main contribution to the power losses. Hence, it will become insignificant when the output power of the system is higher. Therefore, in applications where there is frequent load transients, the use of the auxiliary circuit does not incur efficiency degradation, since the frequent energy exchanges between the circuit and the main converter will not lead to an increase

in power loss.

4.6 Summary

This chapter proposes a method of incorporating an auxiliary switching circuit and a complementary control scheme for dc/dc converters to cope with very fast load disturbances. Large filter capacitors are no longer needed for suppressing excessive overshoots. Ceramic capacitors of longer lifetime can be used instead of electrolytic capacitors. The auxiliary circuit operates as an energy buffer that will decouple itself from the power source. The presented scheme of active energy storage adjustment guarantees that the residual energy storage and volume of the capacitor can always handle any predictable step load change. The method has been validated experimentally for a synchronous buck converter and the idea is generally applicable to other power converters.

Recently, the performance gain in dynamic response resulting from microprocessors providing information of the load dynamics to their power supplies has been discussed [59]. This is a new design direction to cope with very fast transient requirement through communication between the actual load and the power supply. For the case of microprocessor loads, a signal containing information of the occurrences of load transients can be communicated to the power supply so as to allow fast transient control to be applied almost synchronously without the need for sensing the onsets of the load transients. Thus, very fast transients can be achieved in dc/dc converters if information of the load dynamics is available and an appropriate fast transient control method is used. In the next chapter, this idea will be further explored and some practical auxiliary circuit schemes will be discussed.

Chapter 5

Pre-Energized Auxiliary Circuits for Very Fast Transient Loads: Coping with Load-Informed Power Management for Computer Loads

5.1 Introduction

The usual consideration of the dynamic performance of a power supply assumes that the load changes are not known, though the ranges of the extents of load changes are normally specified. In other words, the power supply is always trying to cope with a variable load having random behavior. In a power supply employing a standard voltage feedback controller, the fundamental principle of regulating the operating point is based on the measured information at the output. Time delays inevitably existing in the feedback network and the inductor

involved may lead to unacceptable fluctuations on the output voltage. As discussed in previous chapters, a large filter capacitor bank is able to smooth fast load transients and then suppress the voltage fluctuations. Nevertheless, we still need to decrease the volume of the capacitor bank, considering the size and cost of power supplies.

A number of methods have been proposed for tackling this problem. An auxiliary circuit that deals with fast transients has been considered, and its implementation involves connecting an extra energy transfer path to the load [39, 40, 43, 44, 45, 47, 48, 49, 51, 52, 55, 56, 57, 60], as shown in Fig. 5.1(a). This type of auxiliary circuits can significantly improve transient performance under high slew-rate output current conditions. On the other hand, for the auxiliary circuit to generate the necessary current, the occurrence of the load step, either up or down, must be precisely detected. However, it is difficult to implement an accurate detection of the current step change due to the effect of voltage delay and the finite bandwidth of amplifier circuits. Furthermore, when the auxiliary circuit is implemented using a switching circuit, it is impossible to generate an ideal step current to deal with very rapid transients [43, 44, 45, 47, 55, 56, 57, 60]. Clearly, linear circuits and resistors can be used to achieve very rapid current steps [39, 40, 48, 49, 51, 52], but the poor efficiency is often a price too high to pay.

A practical system where the above problem occurs is the power supply for microprocessors [3, 4]. Recently, a paradigm shift in the design of power supplies for microprocessors has begun to emerge as advance information about the load change may become available [58, 59], as illustrated in Fig. 5.1(b). Thus, we may conceive a new concept in the use of auxiliary circuits for providing very fast transient power, where the load may communicate with the power supply circuit about its future transient events. The auxiliary circuit will then prepare the output current and take an appropriate action to tackle the transient. In

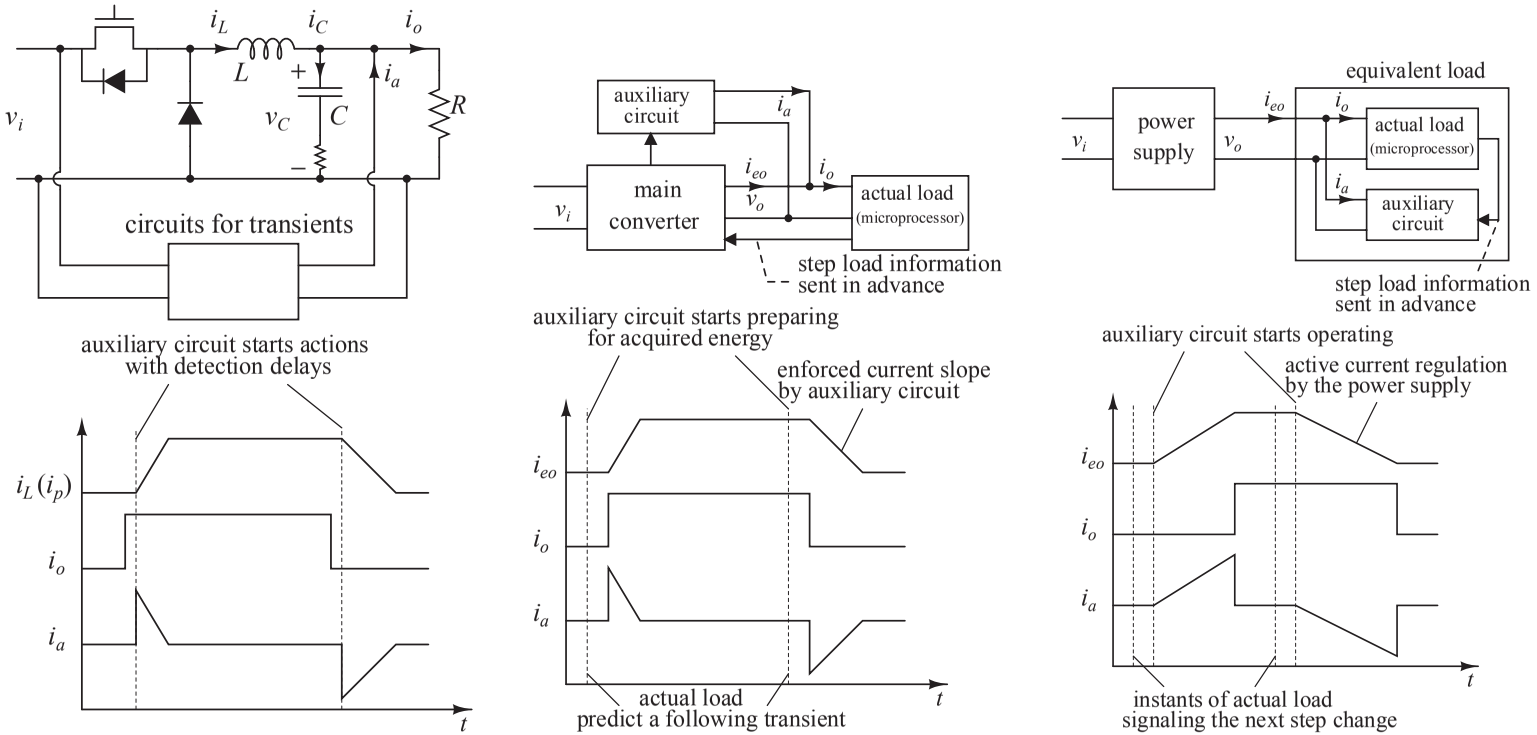


Figure 5.1: Summary of three auxiliary circuits. (a) Previous auxiliary circuit used in a buck converter to assist load transients, (b) illustration of the paradigm of the auxiliary circuit cooperating with a behavior predictive load, and (c) proposed pre-energized scheme of the auxiliary circuit with load-informed power.

this case, a switching capacitor or resistance augmentation is utilized to achieve the energy supply or sink. Comparing with the switching mode auxiliary circuits mentioned earlier, this method will offer very rapid current steps and generate perfect spike-free responses to fast load transients.

In this chapter, we examine this new auxiliary circuit design paradigm where advance loading information is utilized for achieving very fast load transient response. We propose a practical approach to implementing such auxiliary circuits. Specifically, the auxiliary circuit will start sinking or sourcing current at a slow rate to pre-energize the power supply before the load transient occurs. Since the time instant and magnitude of the load current change are known, the auxiliary circuit may schedule a suitable start time of the pre-energizing process. At the instant of the application of the load transient, the output current of the power supply is hitting the new level to which the load is heading. At the same time the auxiliary circuit will remove i_a, switching i_o to the load, as shown in Fig. 5.1(c). It should be noted that in the whole process the power supply is operating independently. Compared with other auxiliary-circuit-based methods, no interaction between the power supply and the auxiliary circuit is required, implying a lower complexity of the system. In addition, as the load provides a synchronized signal at the instant of the application of each transient, exact predictions or detections of the times of the transients are unnecessary, thus greatly simplifying the design of the system and enhancing the transient performance.

5.2 Application Scenarios

As mentioned earlier, a likely consequence of the development of load-informed power management is that the microprocessor can communicate with the auxiliary circuit about the occurrence of a large current load step before it actually applies the step. With the prior information, interactions between the micropro-

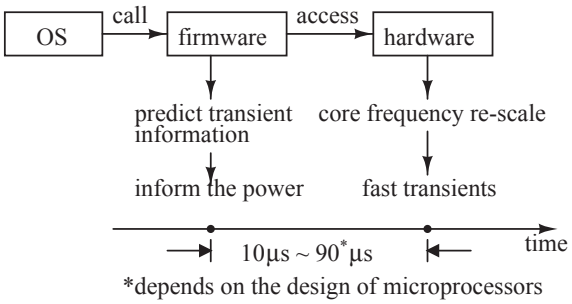


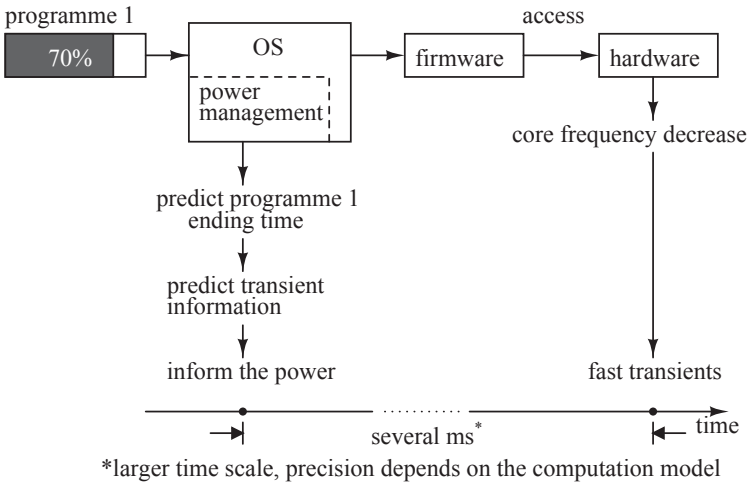
Figure 5.2: The process of core frequency scaling from OS calling the firmware to the hardware implementation and transient predictions in small time scale.

cessor and the auxiliary circuit would eliminate the requirement for fast transient capability of the power supply. The combined auxiliary circuit and load is then connected to an "ordinary" power supply which is capable of providing regulated voltage under small-signal perturbations.

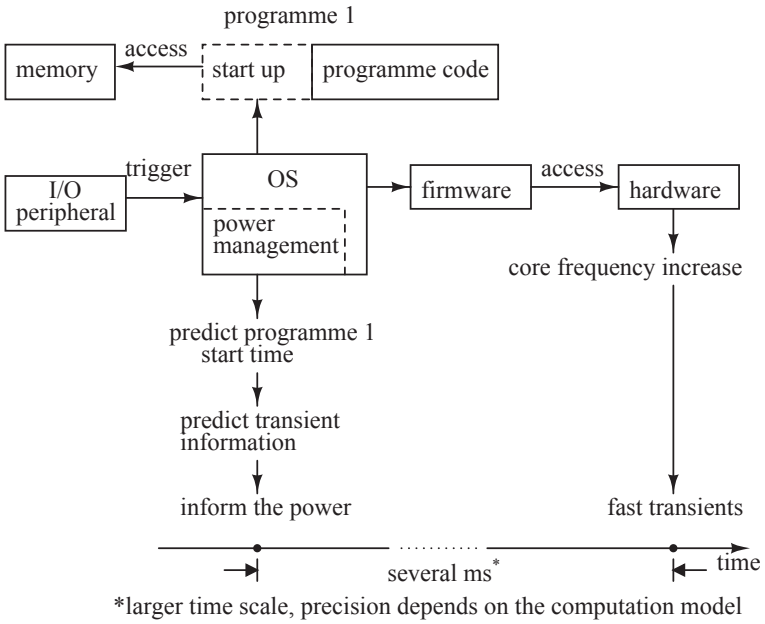
5.2.1 Possibility of Microprocessor Informing Auxiliary Circuit

Dynamic voltage and frequency scaling (DVFS) in practical microprocessor systems allows the clock frequency and supply voltage to vary dynamically in response to computational load requirements. Hence, a microprocessor is able to predict its energy cost and time duration before the completion of one section of the code execution [63, 64, 65, 66, 67, 68].

Specifically, the dynamic frequency scaling (DFS) is generally realized in three stages. First, the operation system (OS) would send out a command to re-scale the core frequency when the CPU usage has changed in a significant scale. Second, the firmware or BIOS (Basic Output Input System) will reconfigure the clock generator and related registers. Finally, it will take the hardware circuit several tens of microseconds to change the clock rate [78]. An illustration of the interactions among OS, firmware and hardware is shown in Fig. 5.2. It can be seen that the whole system needs some time to respond to the power changing



(a)



(b)

Figure 5.3: Predict the real (a) ending and (b) starting time of the programme to give the advance transients information in a large time scale.

requirement from the OS. Hence, the microprocessor is able to accurately provide the transient information prior to the occurrence of the transient in a small time scale.

Furthermore, the OS may predict the transients in a large time scale, as shown in Fig. 5.3. The ending time of program executions can be estimated by the OS with the corresponding computational profile of different applications, i.e.,

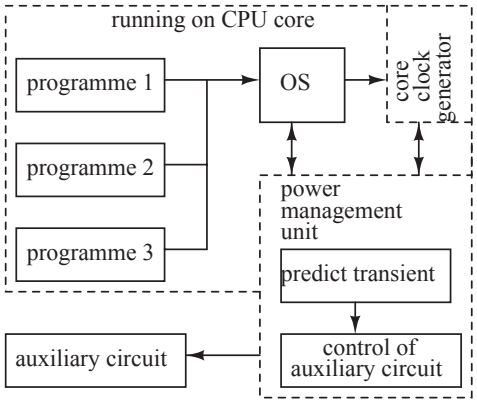


Figure 5.4: A power management unit operating for load-informing is integrated with CPU cores.

arithmetic calculations, media playing or file copying. When the heavy computational load is finished, the computer may immediately enter the idle/sleep mode. Therefore, the step-down load transients can be predicted. Likewise, a step load transient will appear after the application program is triggered by some input signals. In that case, the OS still needs to prepare for the start-up, e.g., assigning software or hardware resources, accessing the source data and regulating the core frequency. The transient prediction for power management may also be triggered by the same input signal. The information would be sent to the auxiliary circuit with minimum latency.

Observation and estimation of computational requirement for power management would occupy part of computational resource. To address this problem, a special unit may be integrated in one chip with CPU cores to realize the power management functions discussed above, as shown in Fig. 5.4. Also, the control function of the auxiliary circuit may also be integrated together. In this case, the communication for load-informed power can be implemented within one chip.

On the other hand, it is possible to reserve several pins for communication with auxiliary circuits. For a microprocessor, interaction signals for voltage identifications (VID) are assigned for dynamic voltage scaling (DVS) in the traditional power management system of microprocessors [79]. This mechanism will facili-

tate the power supply in suppressing overshoots. If the VID scheme is removed and replaced by a pre-energizing scheme to compensate the transients, the reference of power supply can be constantly set to the lowest voltage value and about 10% energy saving may be achieved, assuming an average of 50% loading [59]. Hence, the pins reserved for VID function can be used instead to transmit control signals for the auxiliary circuit, as given in Fig. 5.5. Null response to large-signal transients will be achieved by the operation of the auxiliary circuit [52].

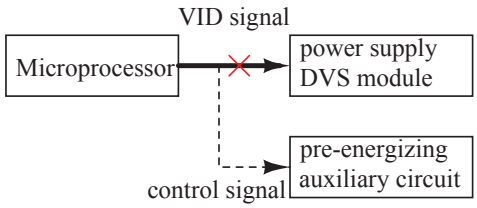


Figure 5.5: Microprocessor pins for VID signals can be used for load-informed power management.

5.2.2 Interaction of Actual Load and Auxiliary Circuit

The equivalent load contains the actual load and an auxiliary circuit, as shown in Fig. 5.1(c). The current of the actual load, i_o, may exhibit an ultra high slew rate but can be predicted before it is applied. As discussed before, a key feature of the equivalent load is that the actual load sends a signal to the auxiliary circuit in advance of each occurrence of large load steps. After receiving that signal, the auxiliary circuit will schedule its action by calculations.

The instant when the predictive signal is received is defined as the time origin. From the signal it can be learned that at the instant T_e the load transient with ΔI_o magnitude will occur. Here, the characteristic of i_a vs time is known and denoted as $i_a(t-t_{as})$, where t_{as} is the start point of circuit actions. When $i_a(T_e-t_{as}) = \Delta I_o$ is expected, then $t_{as} = T_e - T_a$ is obtained, where $T_a = i_a^{-1}(\Delta I_o)$. Hence, the auxiliary circuit starts its action at the time instant t_{as}, as given in Fig. 5.6. Also,

$T_e > T_a$ must be satisfied to give sufficient time for i_a to rise. Here, the time consumption on calculations for scheduling is omitted.

Prior to the application of the step current in i_o, the auxiliary circuit will begin to sink current (denoted as i_a) during T_a. The slew rate of i_a must not exceed the allowed limit, denoted as $k_{p\max}$. When the actual load current step occurs, the power supply continues to deliver the load current but the auxiliary circuit ceases to sink instantly, resulting in the delivery of a very fast transient current to the actual load. Likewise for the case of opposite polarity, before i_o steps to a lower magnitude, i_a goes negative gradually and then is cut off simultaneously as i_o steps down. In other words, the equivalent load connecting to the power supply is designed to sink/source a controllable slowly ramping current, making use of an energy buffer circuit which has prior information about when a rapid load change would occur.

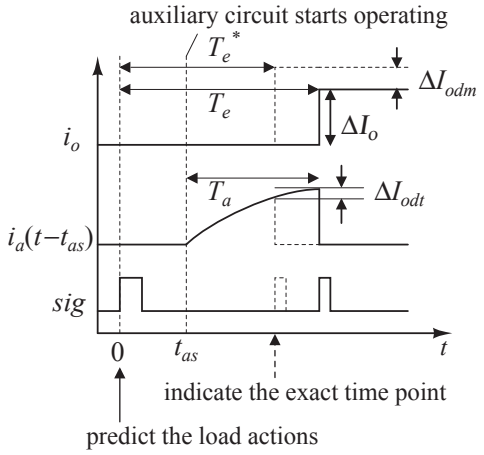


Figure 5.6: Scheduling and implementing the auxiliary circuit action by the signal predicting and indicating transients.

5.2.3 Synchronization Signal to Allow Inexact Prediction

In this prediction method, the actions of load transient and the auxiliary circuit must be aligned in time. A synchronization signal to indicate the occurrence of a load transient will allow inexact time prediction. The energy consumption

of microprocessors depends on the operation frequency which is dynamically scaled and implemented by the hardware. Hence, the hardware is able to indicate the instantaneous clock rates and naturally give a synchronous signal with the occurrence of transients.

Referring to Fig. 5.6, if the load generates a fast transient at T_e^* instead of T_e, the auxiliary circuit will be triggered by the synchronization signal to cut off i_a immediately. In this case, only residual transients, quantified as ΔI_{odt}, need to be taken care of by the power supply. Furthermore, letting the prediction inaccuracy of the magnitude be ΔI_{odm}, the load transient taken by the power supply becomes

$$\Delta I_{od} = \Delta I_{odt} + \Delta I_{odm} = -i_a(T_a + T_e^* - T_e) + \Delta I_o + \Delta I_{odm}. \qquad (5.1)$$

If $T_e^* - T_e \ll T_a$ is obtained, then $\Delta I_{odt} \ll \Delta I_o$. The power supply only needs to address a much smaller amount of transient ΔI_{od}, as compared to ΔI_o.

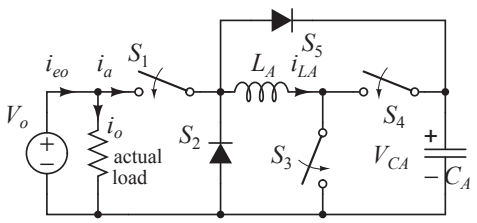


Figure 5.7: Schematic diagram of auxiliary circuit to provide prior slow sloping current.

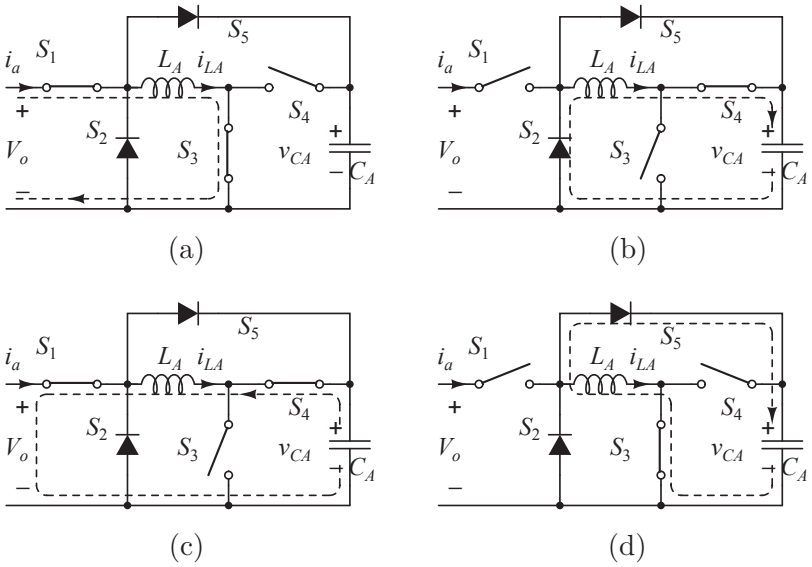


Figure 5.8: Switch topologies of the auxiliary circuit. (a) Stage P_1 and (b) stage P_2 are for step-up load currents, and (c) stage P_3 and (d) stage P_4 are for step-down load currents.

5.3 Implementation of Auxiliary Circuit for Supplying Pre-Energizing Current

5.3.1 Auxiliary Circuit Topology

Our design of the auxiliary circuit is shown in Fig. 5.7 which consists of five switches, an inductor and a capacitor. Here, S_1 is a bi-directional switch realized by a pair of back-to-back MOSFETs (two MOSFETs connected by jointing the drains and turned on/off synchronously); S_3 and S_4 are general MOSFETs; S_2 and S_5 are diodes which may incur small power loss during the energy recovery cycles. Four operation stages can be identified, i.e., P_1, P_2, P_3 and P_4, for the two types of load steps, as explained in Fig. 5.8. Detailed waveforms of the auxiliary circuit are given in Fig. 5.9. Stages P_1 and P_2 are employed for step-up load currents, whereas P_3 and P_4 are for step-down load currents.

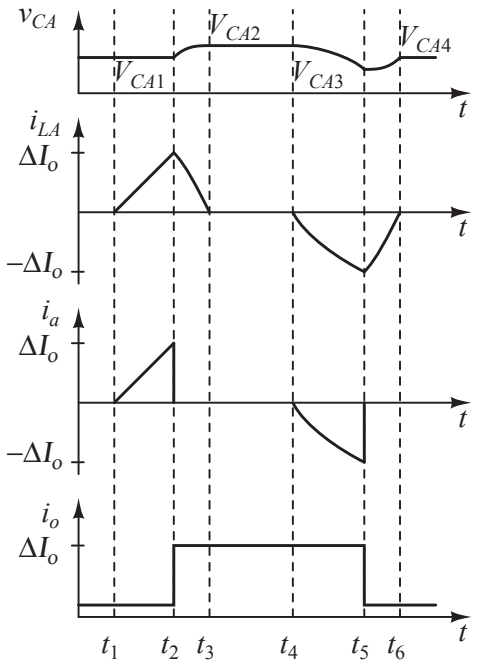


Figure 5.9: Waveforms of the auxiliary circuit for the four operating stages for ΔI_o stepping up at t_2 and down at t_5.

1) Stage $\mathbf{P}_1$ $[t_1, t_2]$

At t_1, the auxiliary circuit, turning on S_1 and S_3 at the same time, begins to sink current gradually from the power supply and stores energy in L_A. Hence, the slew rate of $i_{a/eo}$ is programmable by choosing the inductance of L_A.

2) Stage $\mathbf{P}_2$ $[t_2, t_3]$

When i_a catches up with the load step (ΔI_o) with the same amount of step appearing in i_o, the circuit enters stage P_2. At t_2, which is the beginning of P_2, i_a drops to zero immediately, canceling out the positive transient of ΔI_o at i_o. In this stage, the energy stored in L_A during P_1 is transferring to C_A through S_2 and S_4. This stage will end at t_3, when i_{LA} has declined to zero.

Table 5.1: Parameters of Power Supply and Load for Auxiliary Circuit Design

Symbols	Descriptions
V_o	Output voltage of the power supply
$\Delta I_{o\max}$	Maximum transient step of the actual load
$k_{U\max}$	Maximum slew rate of positive transient of the output current of power supply i_{eo} that does not cause output voltage fluctuation
$k_{D\max}$	Maximum slew rate (absolute value) of negative transient of output current of power supply i_{eo} that does not cause output voltage fluctuation
$k_{p\max}$	Maximum allowable slew rate of the varying i_{eo} that does not cause fluctuation of V_o exceeding $\pm 3\%$ reference value (see Fig. 5.10)

3) Stage $\mathbf{P}_3$ $[t_4, t_5]$

The start time of this stage, t_4, can be calculated once the microprocessor has provided the prior information of negative load step. Similar to P_1, when the circuit enters stage P_3, the auxiliary circuit generates an increasingly negative i_a, while releasing energy from C_A. Different from P_1, however, the trajectory of i_a will never be quasi-linear, but becomes quasi-sinusoidal as a result of an RLC oscillation. The slew rate of i_a depends on the values of L_A and C_A, and the initial voltage of C_A at t_4.

4) Stage $\mathbf{P}_4$ $[t_5, t_6]$

At the start of this stage, i_a has reached the level of $-\Delta I_o$. Switches S_1 and S_4 will be open to cut off i_a, and hence current in L_A will start to flow through the closed switch S_5 to C_A. Hence, the transients in i_a and i_o counteract each other at t_5. Then, i_{LA} will decline to zero at t_6, which is the end of this stage.

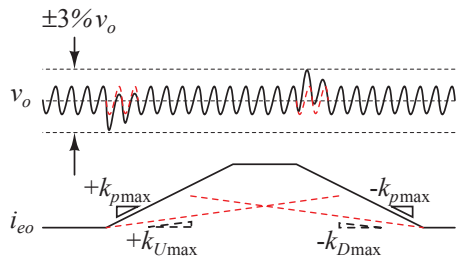


Figure 5.10: Allowed fluctuation of V_o, e.g. ±3% band, incurred by the i_{eo} with the slew rate of $k_{p\,\max}$.

5.3.2 Operating Principles

First, as presented in Section 5.3.1, in stage P_1, i_a is equal to i_{AL}, which is given as

$$i_{LA}(t) = V_o/R_{d1}\left[1 - e^{-R_{d1}/L_A(t-t_1)}\right] \quad (t_1 \le t \le t_2), \tag{5.2}$$

where R_{d1} is the dominant parasitic resistance in topology P_1 and equal to the sum of turn-on resistances of the two switches and the ESR of L_A. In stage P_3, i_{LA} flows through S_1 to the load giving a negative quasi-sinusoidal i_a, which is given by

$$\begin{aligned} i_{LA}(t) &= -i_{m3}\sin\omega_d(t-t_4) \\ &\approx -i_{m3}\sin\tfrac{t-t_4}{\sqrt{L_AC_A}} \quad (t_4 \le t \le t_5), \end{aligned} \tag{5.3}$$

where

$$i_{m3} = \frac{(V_{CA2} - V_o)\sqrt{C_A}}{\sqrt{L_A}} e^{\frac{-R_{d3}}{2L_A}(t-t_4)} \tag{5.4}$$

and R_{d3} is the dominant parasitic resistance in topology P_3. Since in P_3 the current starts from zero, $i_a(t)$ is in the phase range $[0, (t_5 - t_4)/\sqrt{L_AC_A}]$, as depicted in Fig. 5.11.

5.3.3 Parameters Constraints from $k_{U\,\max}$, $k_{D\,\max}$ and $\Delta I_{o\,\max}$

From the definitions of $k_{U\,\max}$ and $k_{D\,\max}$ shown in Table 5.1, in order to achieve a null response to large load current transients, the auxiliary circuit should be

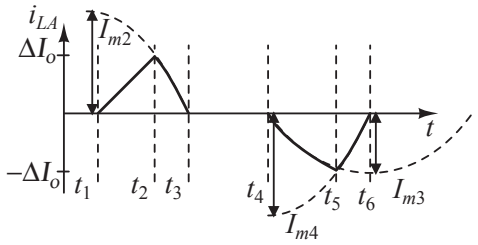


Figure 5.11: Sinusoidal inductor current in the auxiliary circuit starts and ends at certain phase angle with different magnitudes.

designed to satisfy

$$di_a/dt \leq k_{U\max} \tag{5.5}$$

and

$$di_a/dt \geq -k_{D\max} \tag{5.6}$$

in P_1 and P_3, respectively. When the auxiliary circuit is sinking current in P_1, the slew rate of i_a is given as

$$\frac{di_a}{dt} = (V_o/L_A)e^{-R_{d1}/L_A(t-t_1)} \leq V_o/L_A \leq k_{U\max}. \tag{5.7}$$

Thus, the inductance value should be limited as

$$L_A \geq V_o/k_{U\max}. \tag{5.8}$$

In P_3, releasing current to the load, the slew rate of i_a will take the form as

$$\begin{aligned} \frac{di_a}{dt} &= -\frac{V_{CA2}-V_o}{L_A}\cos\frac{t-t_4}{\sqrt{L_AC_A}}e^{-\frac{R_{d3}}{2L_A}(t-t_4)} \\ &+\frac{V_{CA2}-V_o}{L_A}\sin\frac{t-t_4}{\sqrt{L_AC_A}}\frac{R_{d3}}{2L_A}e^{-\frac{R_{d3}}{2L_A}(t-t_4)} \\ &\geq -k_{D\max} \quad (t_4 \leq t \leq t_5), \end{aligned} \tag{5.9}$$

from which the limitation for L_A can be derived as

$$-\frac{V_{CA2}-V_o}{L_A} \geq -k_{D\max} \tag{5.10}$$

and

$$L_A \geq (V_{CA2}-V_o)/k_{D\max}. \tag{5.11}$$

Moreover, considering $\Delta I_{o\max}$, (5.4) is limited as

$$I_{m3}=\frac{(V_{CA2}-V_o)\sqrt{C_A}}{\sqrt{L_A}}e^{-\frac{\pi R_{d3}\sqrt{C_A}}{4\sqrt{L_A}}} \geq \Delta I_{o\max}. \tag{5.12}$$

5.3.4 Determination of Parameters

First V_{CA2} can be chosen arbitrarily using the following procedure:

- V_{CA2} is basically higher than V_o. When the auxiliary circuit is operating, v_{CA} must always be higher than V_o. Otherwise, the auxiliary circuit cannot release current to the load.
- Lower V_{CA2} means flatter i_a slope that is observed from (5.9). Slow i_a will weaken the interference from i_a to the power supply. However, a lower V_{CA2} means that a larger capacitor is required, since in P_3, the energy requirement will be covered by the energy released by C_A, which is given as $C_A(V_{CA2}^2-V_{CA3}^2)/2$.

With V_{CA2} determined, (5.5) and (5.11) are used as the lower bound of L_A, i.e.,

$$L_A \geq \max\left\{\frac{V_{CA2}-V_o}{k_{D\max}}, \frac{V_o}{k_{U\max}}\right\}. \tag{5.13}$$

Furthermore, from (5.12), the constraint for C_A can be derived as

$$C_A \geq \frac{\Delta I_{o\max}^2 L_A}{(V_{CA2}-V_o)^2}e^{\frac{\pi R_{d3}\sqrt{C_A}}{2\sqrt{L_A}}}, \tag{5.14}$$

where R_{d3}/L_A needs to be sufficiently smaller than $1/\sqrt{L_A C_A}$ so as to make $e^{\frac{\pi R_{d3}\sqrt{C_A}}{2\sqrt{L_A}}}$ approach 1. To determine the time instants of the switching actions, we refer to Fig. 5.9. Specifically, the time instants t_2 and t_5 (duration being equivalent to T_e in Fig. 5.6) will be provided to the auxiliary circuit. The auxiliary circuit can readily calculate the switching time instant t_1 from (5.2) and t_4 from (5.3) (duration being equivalent to t_{as} in Fig. 5.6) using

$$t_1 = t_2 - \frac{L_A}{R_{d1}} \ln(\frac{V_o}{V_o - \Delta I_o R_{d1}}) \tag{5.15}$$

and

$$t_4 = t_5 - {i_{LA}}^{-1}(\Delta I_o), \tag{5.16}$$

where i_{LA}^{-1} represents the inverse function of $i_{LA}(t)$ in (5.3) which has no analytical solution. In practical applications, t_1 and t_4 can be obtained by using a look-up table that contains the off-line numerical calculation results of (5.2) and (5.3) to reduce the on-line calculations.

5.4 Alternative Practical Implementation

5.4.1 Practical Trade-offs

The proposed pre-energizing strategy and auxiliary circuit scheme aims to achieve null response in V_o to fast current transients. In practice, most applications allow some voltage fluctuation in V_o, while size, cost and efficiency remain the key considerations.

The solution presented in Section 5.3 requires a large inductor and a large capacitor in order to achieve an ideal performance. Smaller values of $k_{U\max}$ and $k_{D\max}$ require larger capacitors, as can be seen from Fig. 5.12. For applications involving 15 A current transients, for instance, increasing V_{CA2} to 12 V may

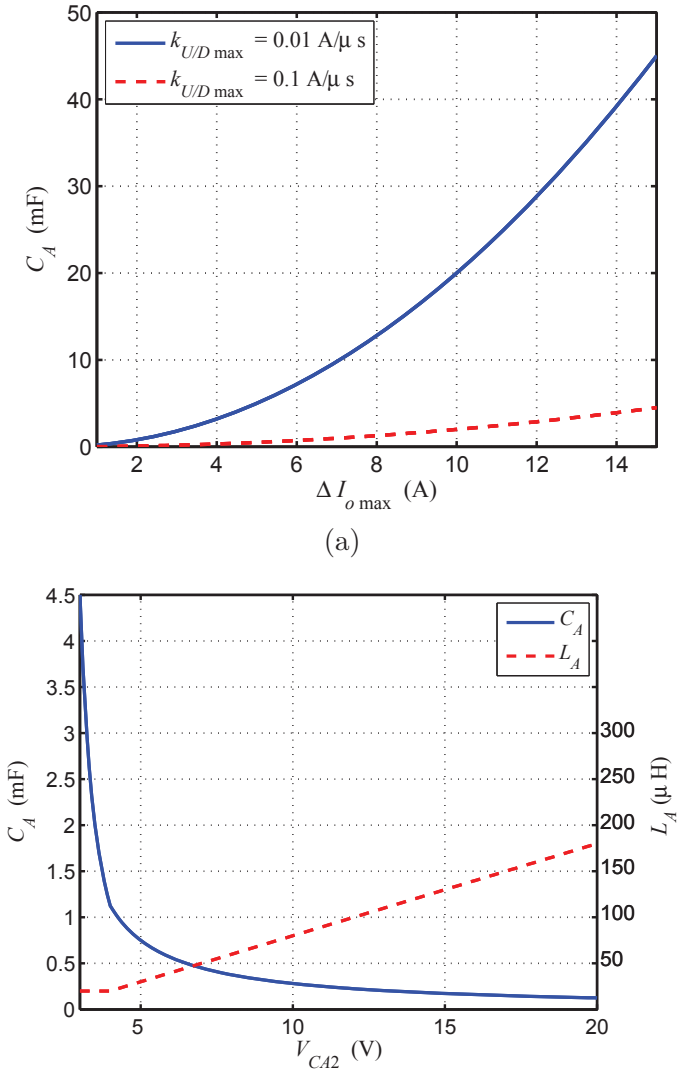


Figure 5.12: Value of C_a versus (a) $\Delta I_{o\,\max}$ in $V_o = 2$ V and $V_{CA2} = 3$ V or (b) V_{CA2} in $V_o = 2$ V, $\Delta I_{o\,\max} = 15$ A and $k_{U/D\,\max} = 0.1$ A/μs.

reduce the value of C_A to 0.3 mF, but it also increases L_A to 100 μH which would still take up a significant space. From (5.13), applying i_a with higher slew rates than $k_{U\,\max}$ and $k_{D\,\max}$ will necessitate a smaller inductance of L_A leading to an increase in the voltage deviation of v_o. Also, $k_{p\,\max}$ is used to define the fast load current which would control the maximum voltage deviation, as shown in Fig. 5.10. Moreover, applying a faster current slope (as determined by $k_{p\,\max}$) and increasing V_{CA2} may not decrease L_A to an accepted range.

To reduce the size of storage elements, a practical approach is to operate

the auxiliary circuit in switching mode, emulating the linear ramping currents in stages P_1 and P_3 with switching ramps, as illustrated in Fig. 5.13 [76, 80]. Specific arrangements are explained in the next subsection.

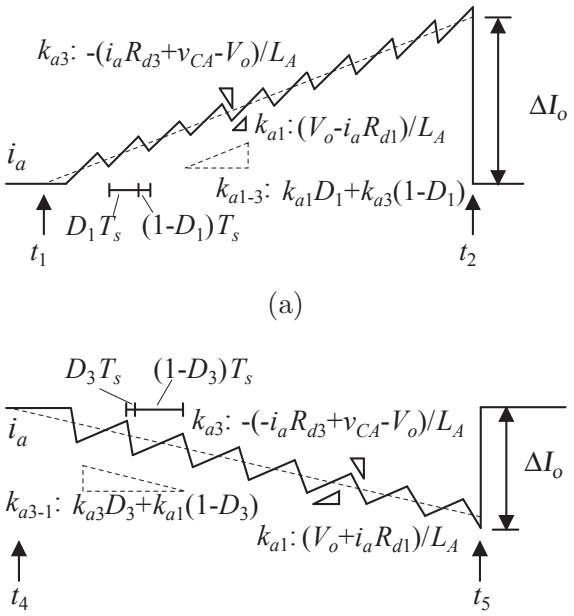


Figure 5.13: Waveforms of i_a during (a) $[t_1, t_2]$ and (b) $[t_4, t_5]$ using high-frequency switching mode implementation.

5.4.2 Alternative Switching Scheme

In the two time durations $[t_1,\ t_2]$ and $[t_4,\ t_5]$, i_a should be ramping up and down, respectively, at a sufficiently low rate. The strategy described in Section 5.3 employs two topologies corresponding to stages P_1 and P_3 to achieve the required function.

As discussed above, implementing stages P_1 and P_3 in switching mode would reduce the size of L_A significantly. Our approach is to switch between P_1 and P_3, and the required ramping current (up or down, as appropriate) can be achieved in the average sense by controlling the duty cycle, as illustrated in Fig. 5.13. To avoid confusion, we denote the ramp-up stage (originally P_1) as $P_{1\text{-}3}$, and the

ramp-down stage (originally P_3) as $P_{3\text{-}1}$. Also, for brevity, we denote di_a/dt given in (5.7) and (5.9) as k_{a1} and k_{a3}. It should be noted that even when k_{a1} and k_{a3} are much larger than what is required, the duty cycle (ratio of durations of P_1 and P_3) can be programmed to generate i_a with the needed slew rate of k_{a1-3} and k_{a3-1} for $P_{1\text{-}3}$ and $P_{3\text{-}1}$, as illustrated by the dash line in Fig. 5.13. The original time durations $[t_1, t_2]$ and $[t_4, t_5]$ will be replaced by the durations of stages $P_{1\text{-}3}$ and $P_{3\text{-}1}$, respectively.

During $P_{1\text{-}3}$ and $P_{3\text{-}1}$, the duty cycles of the auxiliary circuit, D_1 and D_3, can be derived as

$$D_1 = \frac{k_{a1\text{-}3} - k_{a3}}{k_{a1} - k_{a3}} \approx 1 - \frac{V_o - L_A k_{a1\text{-}3} - i_a R_{d3}}{v_{CA}} \tag{5.17}$$

and

$$D_3 = \frac{k_{a3\text{-}1} - k_{a1}}{k_{a3} - k_{a1}} \approx \frac{V_o - L_A k_{a3\text{-}1} - i_a R_{d1}}{v_{CA}}, \tag{5.18}$$

assuming that $R_{d1} \approx R_{d3}$ and i_a is approximately constant during a switching cycle.

5.4.3 Circuit Design

In this alternative implementation of the auxiliary circuit, L_A and C_A are determined by the upper limits of the switching ripples, $\Delta I_{o\max}$, v_{CA}, and the expected value of $k_{a1\text{-}3}$ and $k_{a3\text{-}1}$.

First of all, V_{CA2} is chosen as discussed in Section 5.3.4. Second, the switching frequency is chosen according to the driving technique and devices used, and is normally several hundreds of kHz to one MHz. Third, L_A can be designed by considering the ripple magnitude of i_a which should be limited by the ripple band of the main converter. Fourth, C_A is designed to store sufficient energy that is

released during $P_{3\text{-}1}$, i.e.,

$$\frac{1}{2}C_A(V_{CA2}^2 - V_{CA3}^2) \geq \frac{V_o{\Delta I_o}^2}{2k_{a3\text{-}1}} + \frac{1}{2}L_A{\Delta I_o}^2 + E_{\text{cond\_loss}}, \tag{5.19}$$

where $E_{\text{cond\_loss}} \approx \dfrac{R_{d1} + R_{d3}}{6k_{a3\text{-}1}}\Delta I_o^3$. This result is obtained based on the approximation of 50% duty ratio of P_1 and P_3, separately, over the $P_{3\text{-}1}$ period. In addition, we assume that the ripple current is much less than ΔI_o. Hence, C_A is given as

$$C_A \geq \frac{\dfrac{V_o{\Delta I_o}^2}{k_{a3\text{-}1}} + L_A{\Delta I_o}^2 + 2E_{\text{cond\_loss}}}{(V_{CA2}^2 - V_{CA3}^2)} \tag{5.20}$$

5.4.4 Voltage Control of C_A

As mentioned before, at the instant of t_4, the auxiliary circuit should guarantee that C_A is charged adequately for use in $P_{3\text{-}1}$. However, V_{CA3} is related to past operations of the auxiliary circuit. A worst case is that the load generates step-down transients and slow ramp-up currents. In that case, v_{CA} will get smaller due to operation for the step-down transients. Even in a general situation, the magnitudes of positive and negative fast transients are not always symmetrical, which would makes v_{CA} drift toward one direction. Applying P_1 or P_3 to generate small i_a is able to regulate v_{CA} to a suitable level, when the auxiliary circuit is not operating for transients. The suitable level for v_{CA} is related to the instantaneous load current. An effective scheme to set the suitable v_{CA} has been described in [61], and has been adopted in the prototype.

5.5 Experimental Validation

In this section, an experimental prototype is constructed to validate the proposed method. A low voltage and high current load (1.5 V and 20 A (max)) is selected

Table 5.2: Parameters of the Dc/Dc Synchronized Buck Converter (Which Serves as the External Power Supply to the Load)

Parameters/Components	Values
Input voltage	12 V
Output voltage	1.5 V
Inductance	0.47 μH
Output capacitance	2 $\times$ 100 μF
	2 $\times$ 330 μF
Maximum current	20 A
Switching frequency	300 kHz
Operation mode	Continuous mode
Control	Current mode control
$k_{U\,\max}$	8 A/ms
$k_{D\,\max}$	-8 A/ms
$k_{p\,\max}$	$\pm$100 A/ms

Table 5.3: Parameters of **Auxiliary Circuit I**

Parameters/Components	Values
L_A	200 μH/15 A (max)
C_A	1 F/5 V
v_{CA}	3.0 V—2.8 V
k_{a1}	8 A/ms
k_{a3}	-8 A/ms
MOSFETs ($S_{1,3,4}$)	IRLR7821, $R_{\mathrm{DS(ON)}}$=10 mΩ
Diodes ($S_{2,5}$)	1N5819, V_F = 0.55 V

to emulate a practical microprocessor load. The power supply is a synchronous dc/dc buck converter, whose circuit parameters are shown in Table 5.2. It is a high performance converter, and is capable of handling load current slew rates of up to $k_{U\,\max}$ = 8 A/ms and $k_{D\,\max}$ = –8 A/ms without voltage fluctuation, or $k_p = \pm$100 A/ms with voltage fluctuation within $\pm$3% of 1.5 V. In this study, the original implementation with ideal performance but large components (*Auxiliary Circuit I*) and the switching implementation with small components but limited voltage spikes (*Auxiliary Circuit II*) are constructed to validate the method.

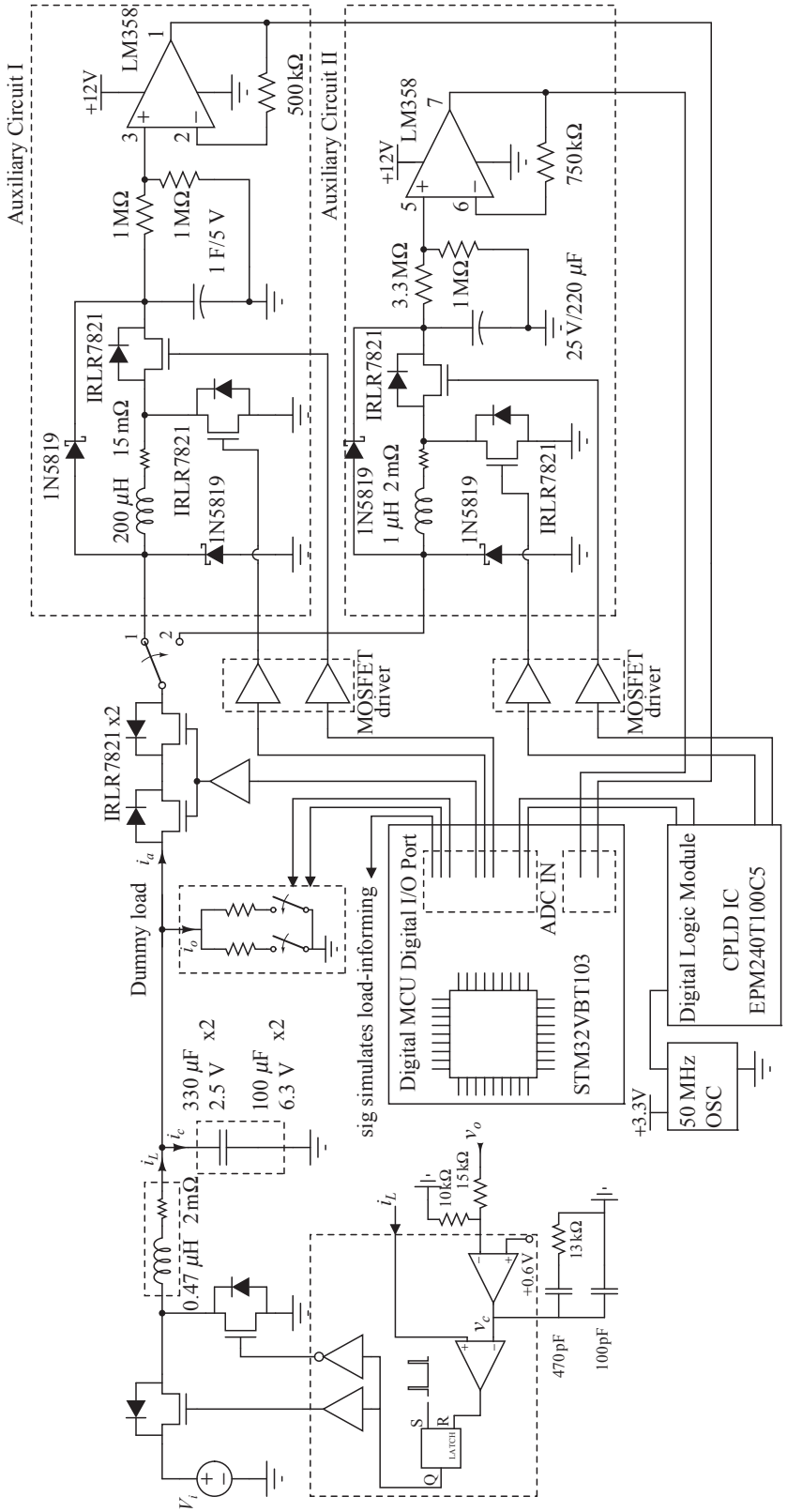


Figure 5.14: Schematic diagram of experimental prototype.

Table 5.4: Parameters of **Auxiliary Circuit II**

Parameters/Components	Values
L_A	1 μH/15 A (max)
C_A	220 μF
v_{CA}	9.5 V—4.5 V
k_{a1}	1500 A/ms
k_{a3}	-8000 A/ms
f_s	500 kHz for $P_{1\text{-}3}$ 1 MHz for $P_{3\text{-}1}$
$k_{a1\text{-}3}$,$k_{a3\text{-}1}$	$\pm$100 A/ms
ripple on i_a	1.5 A
MOSFETs ($S_{1,3,4}$)	IRLR7821, $R_{\text{DS(ON)}}$=10 mΩ
Diodes ($S_{2,5}$)	1N5819, V_F = 0.55 V

5.5.1 Prototype Design

The prototype comprises a general converter, a dummy load, and a digital controller to emulate a computer load, and it also performs as the proposed power management unit to provide advance loading information and control the auxiliary circuit. The schematic diagram is shown in Fig. 5.14.

A traditional type-II compensation strategy is utilized in this converter. The dummy load is capable of generating 0–15 A transients at 20 A/μs by a resister bank. Switching actions of the resister bank are controlled by the digital microcontroller. When the load prediction signal comes, the digital controller will schedule time instants t_1 or t_4. When the switching actions are taken at t_2 or t_5, the auxiliary circuit will operate synchronously, and another indication signal is generated to represent the information from the load. In this prototype, the dummy load and the auxiliary circuit are controlled by one controller which validates the idea in Fig. 5.4 for integrating the power management unit with the computer. It should be noted that the information signal in Figs. 5.15 (a) and (b) is used to demonstrate the load-informed power management and monitor the operation of the prototype.

Two auxiliary circuits are constructed. The parameters are given in Tables

5.3 and 5.4. In Auxiliary Circuit I, the minimum capacitor for $V_{CA2} = 3.0$ V is 0.02 F. To allow for conduction loss and current leakage, C_A is chosen as 1 F/5 V. Thus, the size of the capacitor is still very large. Hence, this solution remains illustrative but understandably impractical. The advantage for this circuit is that a high speed controller is not necessary, and the turn-on duration is several milliseconds for a 15 A transient. The driving loss is reduced but the conduction loss is increased due to the long operation time for a given transient.

In Auxiliary Circuit II, similar to Auxiliary Circuit I, the digital controller is responsible for providing S_1 and the enable signals of S_3 and S_4. The duty cycles in stages $P_{1\text{-}3}$ and $P_{3\text{-}1}$ are controlled by a digital logic module (CPLD in Fig. 5.14). Since v_{CA} is always varying during the above two stages, a strategy implemented within the digital logic module can be used to generate the incremental duty cycles, i.e., D_1 and D_3, during $P_{1\text{-}3}$ and $P_{3\text{-}1}$.

In either of the auxiliary circuits, the digital controller will sample the value of v_{CA}. When the auxiliary circuit is waiting for the next action and v_{CA} exceeds beyond the specified range, the voltage regulation will become active. In this scenario, S_1 will be turned on first, then ultra small duty cycle pulses will drive S_3 or S_4 to charge or discharge C_A. The strategy described in Appendix A.1 can be used to set the duty cycle for the regulation of v_{CA}, since the mechanism of it is almost the same as that of the reservoir capacitor voltage control described in Chapter 4.

5.5.2 Experimental Results

The effectiveness of Auxiliary Circuit I is illustrated in Fig. 5.15. The use of the auxiliary circuit can effectively suppress the voltage fluctuation, reducing the magnitude of the output voltage fluctuation from 200 mV to 60 mV.

When Auxiliary Circuit II is applied, the voltage fluctuation is increased, as

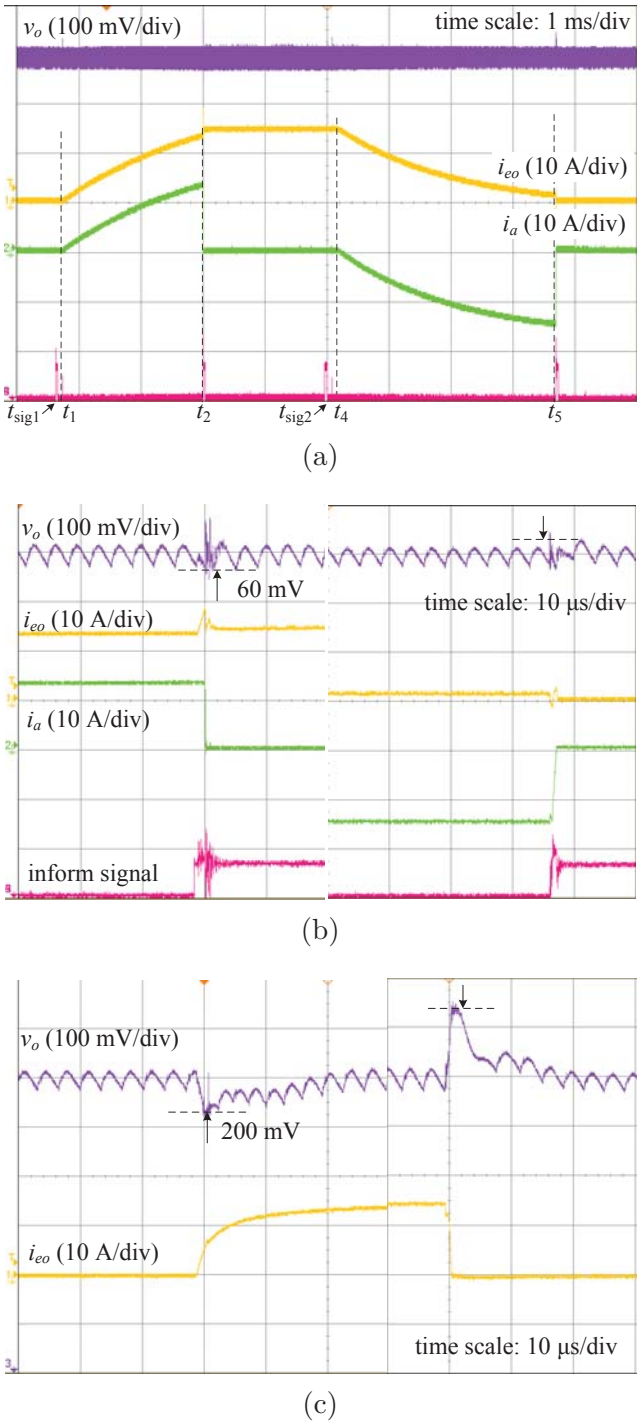
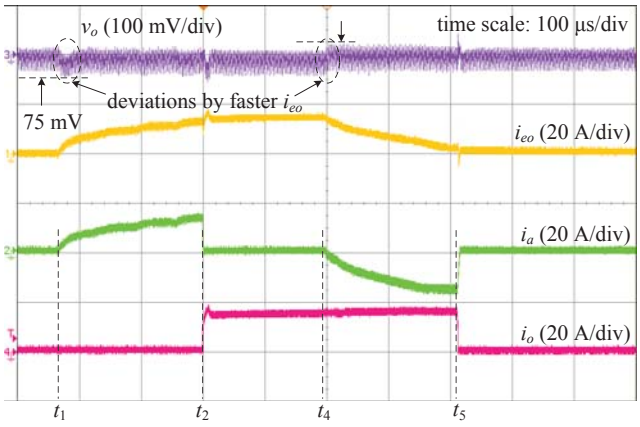
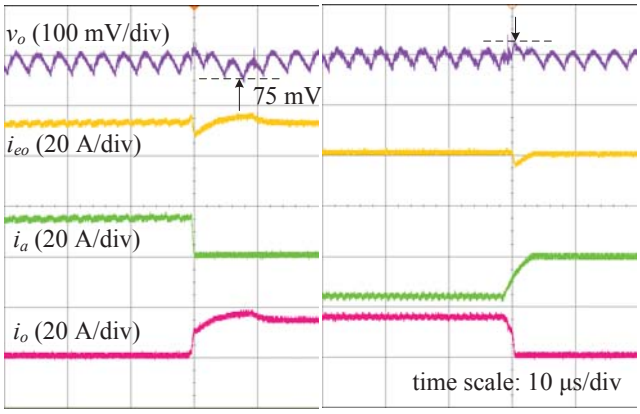


Figure 5.15: Response comparisons for a 10 A transient between the system with and without using the proposed method. (a) Waveforms of the system with Auxiliary Circuit I, (b) enlargement of (a) near t_2 and t_5, and (c) waveforms of the system without the method.

shown in Fig. 5.16. A faster rate of change in i_{eo}, both positive and negative, has been shown to cause about 15 mV of voltage fluctuation. In addition, the



(a)



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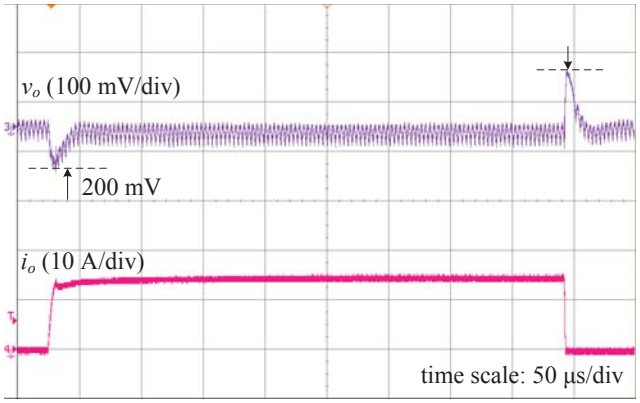

(c)

Figure 5.16: Response comparisons for a 15 A transient between the system with and without using the proposed method. (a) Waveforms of the system with Auxiliary Circuit II, (b) enlargement of (a) near t_2 and t_5, and (c) waveforms of the system without the method but with an additional 220 μF filter capacitor.

switching ripple of the auxiliary circuit generates very small voltage fluctuation in V_o. Here, Auxiliary Circuit II is able to suppress the magnitude of the output

voltage fluctuation from 200 mV to 75 mV.

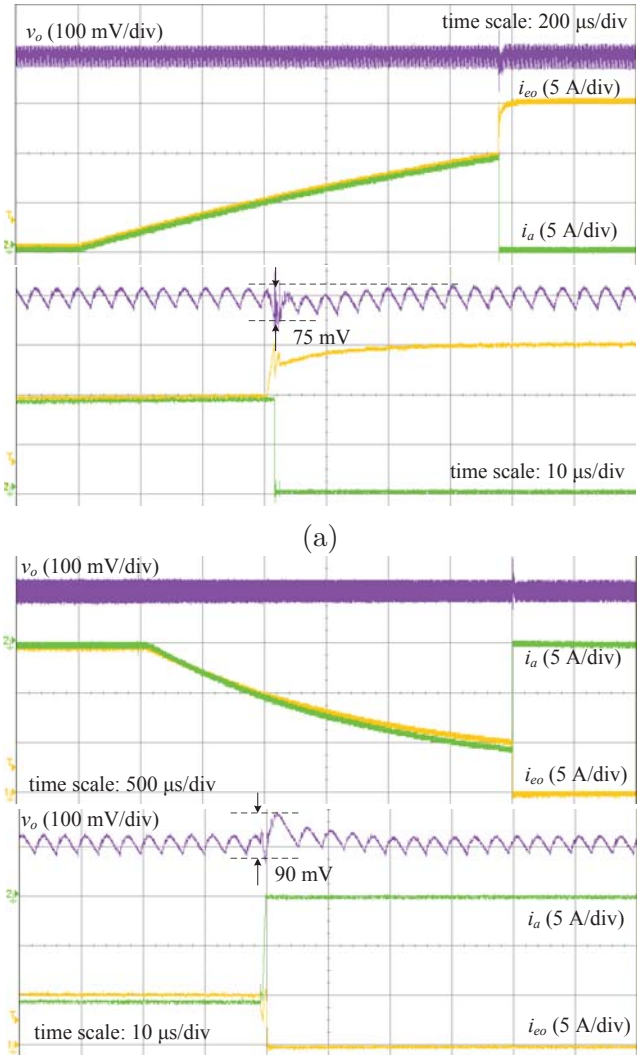

Figure 5.17: Effects of the auxiliary circuit generating a magnitude mismatched current for (a) step-up load current, and (b) step-down load current.

The analysis about the effect of inexact prediction has also been validated in this experiment. Specifically, we let the auxiliary circuit receive a prediction of 10 A step-up transient while a 15 A transient actually occurs. The same condition can be caused by a prediction error of the instant of the application of the transient, i.e., when the auxiliary circuit receives a prediction of 15 A transient while the transient occurs earlier than predicted, for instance, at the instant when i_a reaches 10 A. Therefore, in this case, a 5 A fast transient exists

at i_{eo}, as reported in Fig. 5.17(a). Likewise, we can emulate a prediction error in the step-down transient. The result shows a 5 A mismatch in i_a and i_o, as shown in Fig. 5.17(b). For both cases, an acceptable voltage fluctuation of less than 90 mV is measured.

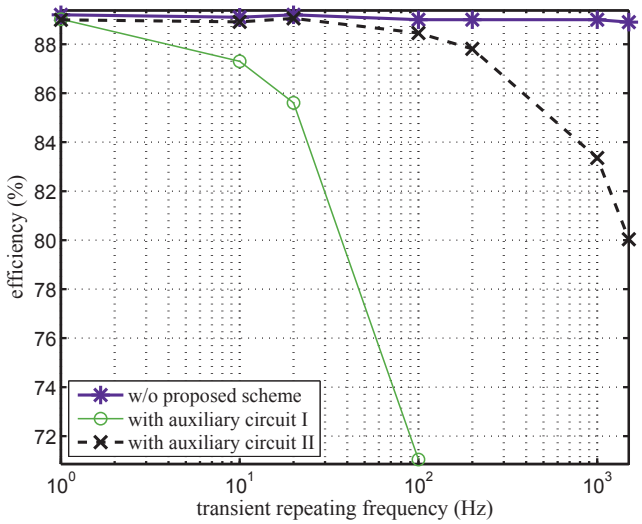

Figure 5.18: Experimental measurements of efficiency degradation in the proposed method using Auxiliary Circuit I and II, where the magnitude of transients is 15 A and the mean load current is 7.5 A.

As with other auxiliary circuit schemes, the proposed method leads to converter efficiency degradation, as shown in Fig. 5.18. When the transient repetition rate is high, Auxiliary Circuit I incurs significantly more loss than Auxiliary Circuit II. The power losses are mainly from the conduction loss in the former scheme and additionally from the switching loss and magnetic components' loss in the latter scheme. Since the operation duration of Auxiliary Circuit I is much longer than that of Auxiliary Circuit II, the former has a poor efficiency. To solve this problem, two strategies are given. One is to apply MOSFETs with lower $R_{\mathrm{DS(ON)}}$ which is proportional to the amount of dissipation and replace $S_{2,5}$ by two MOSFETs in Auxiliary Circuit I, where these two switches are turned on for a relatively long duration. The other strategy is to use a high-performance main converter that can cope with fast dynamic response, i.e., with higher $k_{p\max}$,

to reduce the operation duration of the auxiliary circuit.

In addition, we note that the power loss is independent of the mean load current level. For applications having a higher mean value of load current but same transient current, the effect on the efficiency degradation incurred by the auxiliary circuit would become insignificant.

In this experiment, although some characteristics (e.g., power and transient slew rate) of the prototype do not fully resemble the real microprocessor power system (e.g., hundreds of watts and hundreds of A/μs), the experimental result clearly validates the effectiveness of the proposed design in obtaining a response to large signal transients with insignificant voltage fluctuation.

Compared to existing schemes, the auxiliary circuit does not need a high bandwidth sensor to detect the load transient. There is also no interaction between the auxiliary circuit and the power supply. However, a capacitor and more switches are used to pre-energize the power supply. Therefore, the proposed auxiliary circuit occupies larger amount of space, compared to existing methods. Nevertheless, space occupation will not be a drawback of the proposed method as long as the auxiliary circuit is packaged in a chip.

5.6 Summary

A method using auxiliary circuit to achieve null response to fast transients in a power supply system has been discussed in this chapter. The idea has been inspired by a basic design paradigm shift requiring the load to provide real-time information about its power consumption dynamics. Then, the auxiliary circuit provides slowly rising current to pre-energize the power supply prior to actual load steps, cooperating with advance notice from the load. Such a development trend seems to be highly promising as the design of the associated power management circuits and systems can be desirably facilitated and the performance specifi-

cations can be more readily met. Thus, our idea transpires a possible future development of microprocessors which sees the inclusion of an auxiliary power circuit as a standard integrated part and the use of predictable load demand information for achieving the required power supply functions. In this chapter we have proposed two specific implementations of the method and demonstrated their feasibility in a practical environment.

Chapter 6

Conclusions and Suggestions for Future Research

This chapter summarizes the main contributions of this research project, and discusses some possible future direction for further development in this research area.

6.1 Contributions of the Thesis

Switched-mode power supplies (SMPS), due to their low cost, high efficiency and compact size, are widely used in power conversion applications. The drawback of SMPS is the slow dynamic response. For loads that exhibit very fast transients, the response of a SMPS can be enhanced by enlarging the filter capacitor or adopting a multiphase structure. These strategies will require more space or add extra cost to the power supply, weakening the advantages mentioned above. This thesis addresses the issue of fast load transients and has made the following contributions:

1. A classification of auxiliary circuit schemes for feeding fast load transients has been proposed.

In order to provide a systematic exposition of the design of auxiliary circuits, a classification has been proposed based on the implementation methods, the ways in which the auxiliary circuits are connected with the power supplies and loads, as well as the control methods. The efficiency, complexity and application constraints of different categories of schemes are analyzed. Suitable applications for specific schemes are given to help circuit designers make appropriate choice for their applications.

2. A bi-directional buck-boost converter operating as an auxiliary circuit to feed fast load transients has been studied.

The proposed auxiliary circuit might supply or sink energy to control the charge balance of the filter capacitor during load step-up or step-down transients. To avoid the charge imbalance of the reservoir capacitor caused by non-zero net input energy, an effective scheme to regulate the reservoir capacitor voltage has been proposed. The reservoir capacitor voltage will be set at a specific level according to the load level. Design guidelines of the auxiliary circuit have been given.

3. A pre-energized auxiliary circuit for feeding fast load transients based on load-informed power management has been proposed.

With the availability of load dynamics information through communication of the load with the power supply, the power management designed for intelligent loads can be optimized further. The proposed auxiliary circuit might pre-energize the power supply to shift its operating point prior to the occurrence of load transients. When a fast transient current occurs, the auxiliary circuit would buffer it. The power supply would never feel the occurrence of fast transients at the load and hence can be designed as an ordinary power supply for handling small-signal perturbations. The system structure would become simpler.

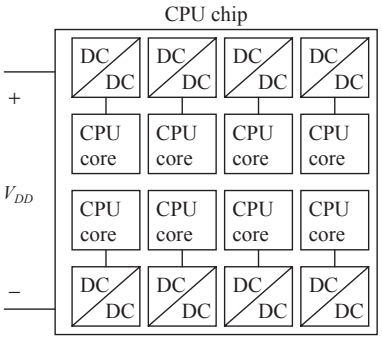

Figure 6.1: Distributed power supplies integrated with CPU chips.

6.2 Suggestions for Future Research

The strategy of feeding fast transients needs to be improved in view of the new development trend of loads and power supplies.

6.2.1 The Trend of Power Supply on-Chip

The microprocessor chip is the main application of a power supply designed for feeding fast load transients. A traditional power supply is designed to sit around the microprocessor chip on the mainboard to reduce power loss as far as possible. Nevertheless, the loss in the connection lines is still rising as the supply voltage is getting lower and the required current is getting higher.

To further improve the efficiency of power delivery, the trend of power supply design for microprocessors is to integrate the distributed sub-power supplies on the chip with CPU cores (see Fig. 6.1). The current level of each sub-power supplies might become as low as several amperes magnitude. Therefore, the auxiliary circuit for feeding fast transients needs to be integrated on the chip as well.

6.2.2 Resonant Auxiliary Circuit for Fast Transients

Existing auxiliary circuits that consist of transistors and resistors could be integrated on-chip. However, when the load voltage becomes lower, removing the extra energy on the filter capacitor for step-down load transients becomes difficult as it will occupy larger silicon space to realize ultra-low resistance switches. To solve the problem, a negative voltage source might be used to drain out the extra energy from the filter capacitor.

Another problem in constructing an on-chip auxiliary circuit including reactive components is the presence of a magnetic-core inductor which cannot be integrated. The solution is to decrease the inductance value and to operate the auxiliary circuit in resonant mode. When the inductance value becomes sufficiently small, e.g., around several tens of nano-henry scale, it becomes feasible to realize the inductor by coreless printed spiral winding (CPSW) and to integrate it on chip.

Finally, the circuit will eliminate the requirement of components on low ESR and magnetic-core, and therefore all components are able to be integrated on-chip. In addition, a resonant circuit may operate in ZCS or ZVS conditions that would reduce the switching loss and improve the efficiency.

Appendix A

Derivations and Experimental of Chapter 3

A.1 Derivation Details of Reservoir Capacitor Voltage Control

The limitation of v_{ca} is given as

$$\begin{cases} \frac{1}{2}C_a v_{ca}^2 - \Delta E_{1\,\max} \geq \frac{1}{2}C_a V_{ca\,\min}^2 \\ \\ \frac{1}{2}C_a v_{ca}^2 + \Delta E_{2\,\max} \leq \frac{1}{2}C_a V_{ca\,\max}^2 \end{cases}, \tag{A.1}$$

which can be combined as

$$\frac{1}{2}C_a V_{ca\,\min}^2 + \Delta E_{1\,\max} \leq \frac{1}{2}C_a v_{ca}^2 \leq \frac{1}{2}C_a V_{ca\,\max}^2 - \Delta E_{2\,\max}, \tag{A.2}$$

e.g., for a buck converter, where $\Delta E_{1\,\max} = \frac{1}{2}\left(\frac{I_{o\,\max}}{I_o} - 1\right)^2 I_o^2 \frac{LD}{1-D}$ and $\Delta E_{2\,\max} = \frac{1}{2}\left(\frac{I_o}{I_{o\,\min}} - 1\right)^2 I_{o\,\min}^2 L$. $\Delta E_{1\,\max} + \Delta E_{2\,\max}$ is defined as the energy floating interval. For a given i_o, if $\frac{1}{2}C_a v_{ca}^2$ does not fall within the inequalities given in (A.2), the auxiliary circuit may exceed the operating boundary in the next operation.

To prevent this from happening, the auxiliary circuit can be operated to charge or discharge some of its energy such that v_{ca} falls within the inequality in (A.2) before the occurrence of the next disturbance. This method of capacitor voltage control is illustrated in Fig. 4.4, where the normal energy range are depicted in black solid lines while the energy floating intervals are depicted in red lines. The dashed line in Fig. 4.4 corresponds to the case of v_{ca} exceeding the upper limit without the reservoir capacitor voltage control.

In practice, the midpoint of the interval defined by inequality (A.2) can be chosen as the optimal regulation reference for v_{ca}. This means that the energy floating interval will always be located at the center of the normal energy range of C_a. This can be mathematically expressed as

$$\frac{1}{2}C_a v_{ca}^2 = \frac{1}{2}\left[\frac{1}{2}C_a(V_{ca\,\min}^2 + V_{ca\,\max}^2) + (\Delta E_{1\,\max} - \Delta E_{2\,\max})\right] \tag{A.3}$$

and after simplification as

$$v_{ca}(i_o) = \sqrt{\frac{1}{2}(V_{ca\,\min}^2 + V_{ca\,\max}^2) + \frac{\Delta E_{1\,\max} - \Delta E_{2\,\max}}{C_a}}. \tag{A.4}$$

By substituting $\Delta E_{1\,\max}$ and $\Delta E_{2\,\max}$ into the buck column of Table 4.2, (4.3) is generated.

With knowledge of the output current i_o, the relevant reference of v_{ca} can be calculated using (A.4). If the actual v_{ca} is larger than the reference value, S_2 is driven by a series of short pulse signal (at a small duty ratio) to release some energy from the capacitor to the load at a relatively low speed. Through this process, excessive energy from the capacitor are released to the load. If v_{ca} is lower than the reference, S_1 is driven by a small duty ratio such that v_{ca} increases slowly until it reaches the reference value.

The turn-on time of switches, $t_{\rm w}$, and the turn-on interval, $t_{\rm int}$, should be

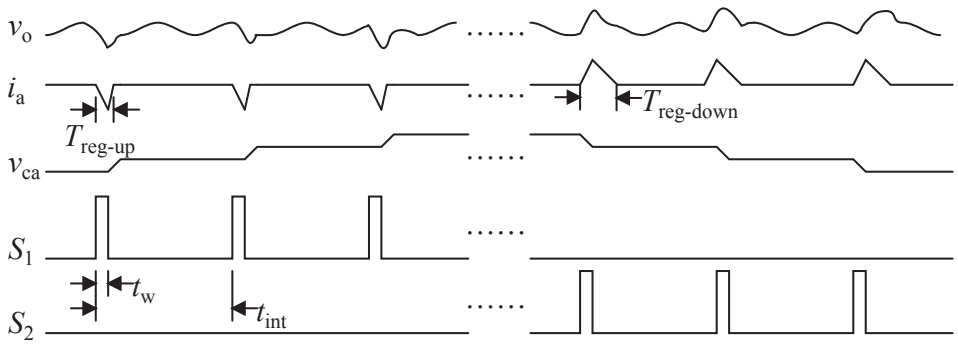

Figure A.1: Key waveforms of reservoir capacitor voltage regulation.

chosen following this principle. First, as such operations will induce a small voltage ripple at v_o, $t_{\rm w}$ should be sufficiently small to ensure the voltage ripple to be within the converters ripple band. On the other hand, $t_{\rm int}$ affects the response time of the voltage regulation and the stability of the converter. A shorter $t_{\rm int}$ gives a faster voltage regulation but induces a larger current flow in the main converter. Therefore, $t_{\rm int}$ should be as large as possible but is limited by the required response time of v_{ca}. The waveforms corresponding the reservoir capacitor voltage regulation process are shown in Fig. A.1.

When S_1 is operated to increase the value of v_{ca}, the ripple voltage at the converter's output will be

$$\begin{aligned} v_{r\rm reg} &= \frac{1}{C_o}\int\limits_{<T_{\rm reg\text{-}up}>} |i_a|dt \\ &= \frac{1}{2}\frac{V_o t_{\rm w}}{L_a}\left[t_{\rm w} + \frac{V_o t_{\rm w}}{C_o L_a}\left(\frac{V_{ca}-V_o}{L_a}\right)^{-1}\right] \\ &= \frac{1}{2}\frac{V_o t_{\rm w}^2}{C_o L_a}\frac{V_{ca}}{V_{ca}-V_o}, \end{aligned} \tag{A.5}$$

where v_o and v_{ca} become approximately constant. A maximum value of $v_{r\rm reg}$ will appear when $v_{ca} = V_{ca\,\rm min}$, i.e.,

$$v_{r\rm reg\,max} = \frac{1}{2}\frac{V_o t_{\rm w}^2}{C_o L_a}\frac{V_{ca\,\rm min}}{V_{ca\,\rm min}-V_o}. \tag{A.6}$$

Similarly, when S_2 is operated to decrease the value of v_{ca}, the ripple voltage can be derived as

$$v_{rreg} = \frac{1}{C_o} \int\limits_{<T_{\text{reg-down}}>} |i_a| dt = \frac{1}{2} \frac{(V_{ca} - V_o) t_{\text{w}}^2}{C_o L_a} \frac{V_{ca}}{V_o} \tag{A.7}$$

and its maximum as

$$v_{rreg\,\max} = \frac{1}{2} \frac{(V_{ca\,\max} - V_o) t_{\text{w}}^2}{C_o L_a} \frac{V_{ca\,\max}}{V_o}. \tag{A.8}$$

If the specified ripple band is $v_{rreg\,\max}$, to satisfy the specification, t_{w} is limited to

$$t_{\text{w}} \leq \min \left\{ \sqrt{\frac{2 v_{rreg\,\max} C_o L_a (V_{ca\,\min} - V_o)}{V_o V_{ca\,\min}}}, \sqrt{\frac{2 v_{rreg\,\max} C_o L_a V_o}{(V_{ca\,\max} - V_o) V_{ca\,\max}}} \right\}. \tag{A.9}$$

The energy change of C_a for a complete switching action of S_1 or S_2 is

$$\Delta E_{\text{S1/S2}} = \int\limits_{<T_{\text{reg-up}}/T_{\text{reg-down}}>} V_o |i_a| dt. \tag{A.10}$$

Under a reasonable approximation that v_{ca} is a constant, the approximate energy change of C_a for S_1 and S_2 are respectively

$$\Delta E_{\text{S1}} > \frac{1}{2} \frac{V_o^2 t_{\text{w}}^2}{L_a (V_{ca\,\max} - V_o)} V_{ca\,\max} \tag{A.11}$$

and

$$\Delta E_{\text{S2}} > \frac{1}{2} \frac{(V_{ca\,\min} - V_o) t_{\text{w}}^2}{L_a} V_{ca\,\min}. \tag{A.12}$$

Assuming the voltage regulation range of v_{ca} is from $V_{ca\,\min}$ to $V_{ca\,\max}$, the maximum number of switching cycles needed for the completion of the voltage adjust-

ment process is

$$N_{\text{switch max}} = \max\left\{\frac{\frac{1}{2}C_a(V_{ca\,\max}^2 - V_{ca\,\min}^2)}{\Delta E_{\text{S1}}}, \frac{\frac{1}{2}C_a(V_{ca\,\max}^2 - V_{ca\,\min}^2)}{\Delta E_{\text{S2}}}\right\}. \quad \text{(A.13)}$$

If the smallest load-step interval is $t_{\text{load min}}$, then $N_{\text{switch max}}$ times of cycles of S_1 or S_2 must be completed during $t_{\text{load min}}$. The switching interval can be derived as

$$t_{\text{int}} = \frac{t_{\text{load min}}}{N_{\text{switch max}}}. \quad \text{(A.14)}$$

A.2 Details of Experimental Setup

The schematic diagrams of the converter and the auxiliary circuit are given in Figs. A.2 and A.3, respectively. The mechanism of the auxiliary circuit and control is as follows. The top left corner of Fig. A.3 shows the adding unit circuit for the capacitor current, the inductor current, and the auxiliary current. The signal representing the load current step ("LoadStep-down" and "LoadStep-up") are generated by the step detection circuit at the top right corner. The capacitor voltage of this circuit is proportional to the steady state i_o signal value. Once a load step occurs, a constant charging (or discharging) current will let the capacitor voltage track a new reference which is synchronously changed with i_o. The active time of charging (or discharging) current is proportional with the load step size. The signal used to enable the charging (or discharging) current source is labeled as "LoadStep-up" (or "LoadStep-down").

The schematics inside "Filter Capacitor Current Zero Crossing Comparator" part of Fig. A.3 is responsible to give the state of i_c (positive or negative). The sensed filter capacitor current signal (bottom left of the figure) is fed into the zero-crossing comparator to generate "ZcCompStep-down" or "ZcCompStep-up" for a step-down or step-up load transient, respectively. When i_c exceeds the

preset negative or positive threshold "ZcCompStep-down" or "ZcCompStep-up" will be enabled (logic "0"), respectively.

The energy regulation signal "AuxE↑" and "AuxE↓" (middle right) provides the information as to whether the auxiliary circuit should increase or decrease v_{ca} with respect to the reference. Whenever v_{ca} exceeds the tolerance with respect to the reference, the comparators will enable either "AuxE↑" or "AuxE↓" signal which is fed into the "Digital Logic Module". The reference signal is generated by the external MCU controller using the sampled i_o and an i_o-to-v_{ca} software algorithm.

"Digital Logic Module" includes a complex programmable logic device (C-PLD) which functions as follows:

1. When output signals of "A" are both disabled, i.e., no fast load transients are detected, the PWM signal from the controller is directly transferred into the main converter switch. Sometimes signals with ultra-low duty cycle will drive S_1 or S_2 to regulate v_{ca}, while "AuxE↑" or "AuxE↓" signal is enabled, respectively. The duty cycle value depends on t_w and t_{int}.

2. When a fast load transient is detected, i.e., either an output signal of "A" is enabled, 100% or 0% duty ratio will be given to the main converter switch. The inductor current is changing to its new steady state, over the transition time determined by "A". In this duration, the auxiliary circuit will be active.

3. While the auxiliary circuit is active for fast load transients, the control of S_1 and S_2 is following hysteresis mechanism. The system will be naturally stable as delay time exists over the control loop. In a load step-down case, S_1 is turned on first. Once "ZcCompStep-down" becomes "0", i.e., i_c is exceeding its negative tolerance, S_1 will be off immediately until "ZcCompStep-down" recovers. Similarly, in a load step-up case, S_2 is turned on first. Once

"ZcCompStep-up" becomes "0", i.e., i_c is exceeding its positive tolerance, S_2 will be off immediately until "ZcCompStep-up" recovers.

The dummy load is realized by a resistor bank and MOSFETs. To emulate the real computer load profile (sharp current edges), fast response MOSFETs and drive ICs (MC33152) are used (see Fig. A.2).

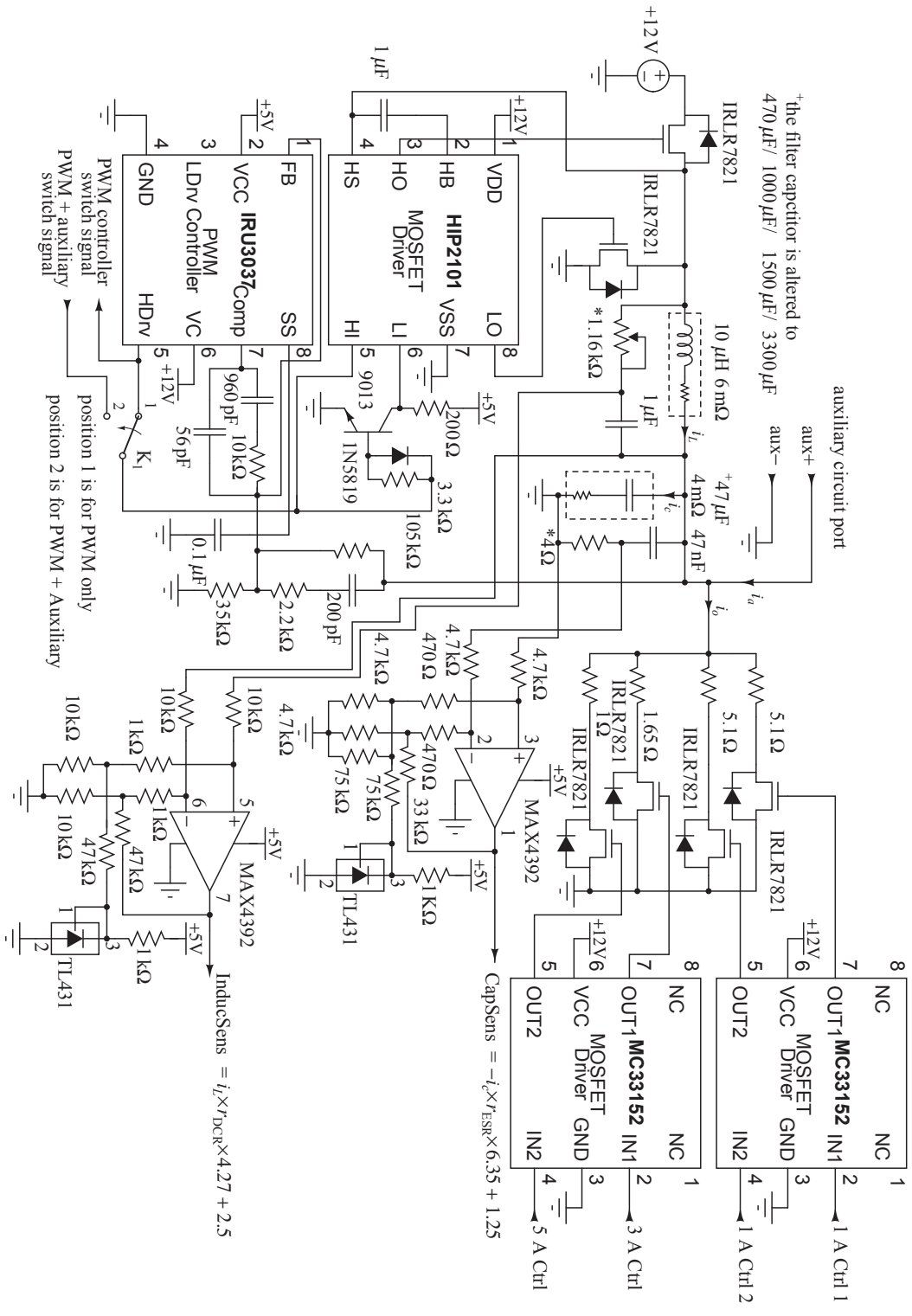

Figure A.2: The schematic diagram of the synchronous buck converter.

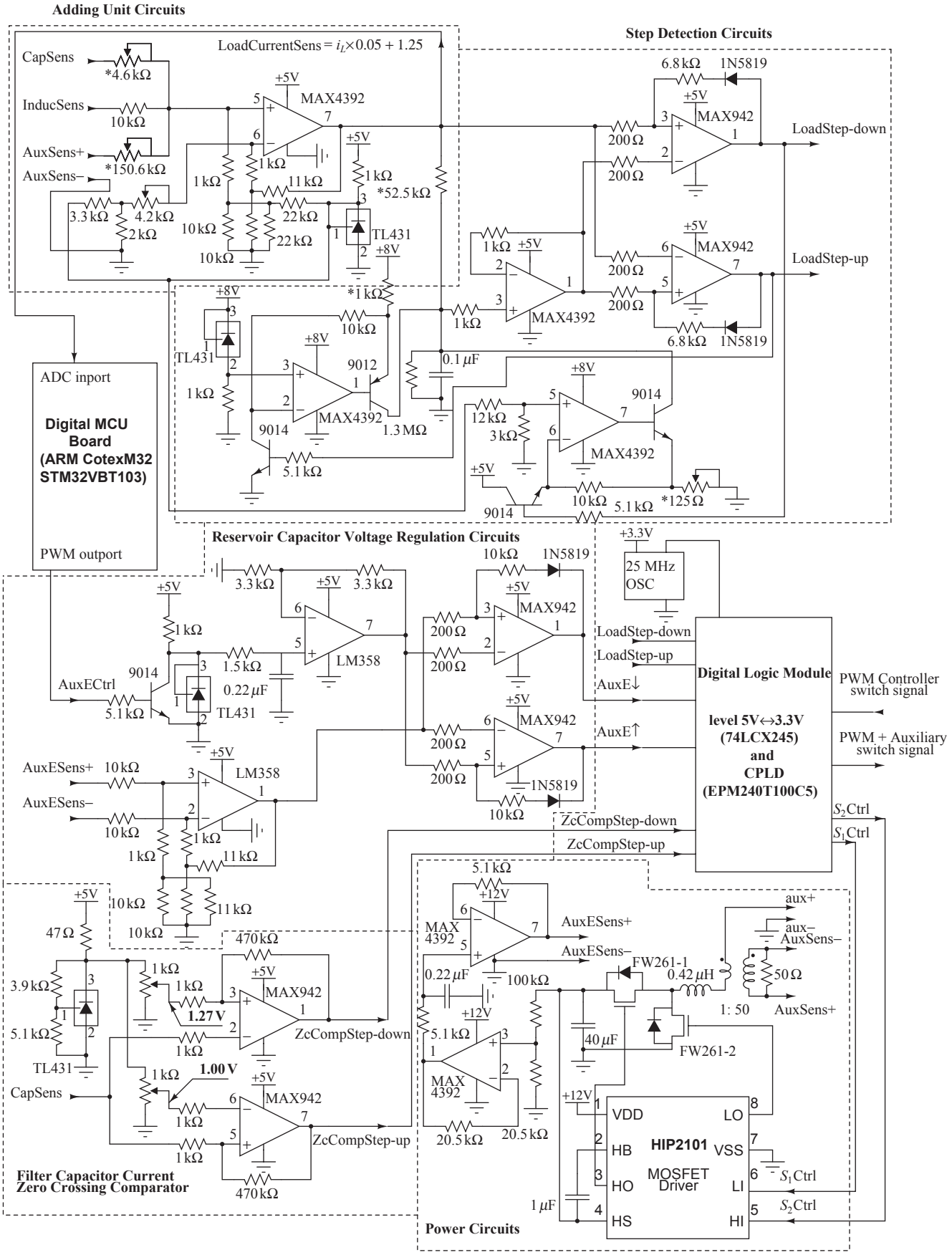

Figure A.3: The schematic diagram of the auxiliary circuit and its control.

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