Design and Practical Implementation of Efficient Power-Factor-Corrected Switching Regulators Based on Reduced Redundant Power Processing Principle

Martin Kin Ho CHEUNG

Department of Electronic and Information Engineering,
The Hong Kong Polytechnic University, Hung Hom, Hong Kong.

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To my parents

Abstract

Abstract of the thesis entitled 'Design and Practical Implementation of Efficient Power-Factor-Corrected Switching Regulators Based on Reduced Redundant Power Processing Principle' submitted by Martin Kin Ho CHEUNG for the degree of Master of Philosophy at The Hong Kong Polytechnic University in August 2002

Power-factor-corrected switching regulators effectively eliminate the current harmonic distortions of the AC mains, associated with large non-linear loads, capacitive loads, and inductive loads from the electric machinery and electronic systems. Switching regulators with power factor correction (PFC) and fast voltage regulation are constructed by two simple converters with an energy storage element. Simple and typical power-factor-corrected switching regulators are connected with their the converters and the storage element serially. The main drawback of this approach is that the efficiency of these arranged switching regulators is inevitably reduced by the two power processing stages, the two simple converters. To solve the efficiency problem, non-cascaded switching regulators are proposed. Unlike the typical power-factor-corrected switching regulators, the non-cascaded power-factor-corrected switching regulators allow part of the input power to be processed by only one power stage, thereby reducing the amount of power redundantly processed by the two constituent power stages. Unfortunately, industry has been slow to appreciate and exploit the considerable advantages of the non-cascaded power-factor-corrected switching regulators. There seem to be the reason for that: the lack of detail, systematic comparison, and practical information on the non-cascaded power-factor-corrected switching regulators. The objective of this study is to fill this gap by providing a well-organized compendium of useful information for

the switching regulator design engineers who want to understand the practical detail of the non-cascaded power-factor-corrected switching regulators for accomplishing an optimal in their designs. Two non-cascaded power-factor-corrected switching regulators have been constructed and tested for validating the reduced-redundant-power-processing (R^2P^2) principle. A rigorous and detail comparison of the switching regulators output power level, circuit complexity, components stress, and control methodological are reported.

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Chapter 1

Introduction

1.1 Motivation and Objectives

Huge non-linear loads generate an excessive distortion on the current of the power supplied to consumers through the power distribution system. Due to the rapid proliferation of electric machinery and electronic systems [1], the resulting distortion causes a drastic degradation in power quality of the power distribution system. Reported by Clemmensen [2], poor power quality leads to about $13.3 billion in damage per year in the United States. Improving the power distribution system power quality and current distortion becomes paramount issue of the switching regulator design engineers.

One of the most common switching regulators is the AC-DC regulator, which supplies a DC load with power drawn from the AC mains. Virtually all electronic systems, including equipment for instrumentation, communication, computer, and household electric appliances, require a DC voltage. In low-power applications, a simple rectifier bridge is usually followed by a DC-DC regulator to smooth and regulate the output voltage. At high-power applications, the phase controlled rectification provides a regulated DC output voltage using rugged semiconductor devices.

All of these methods for generating a DC voltage from the AC mains are simple and cost-effective solutions, however they also have the drawback resulting a poor input-current waveform, which imposes problems as follows:

1. Distortion of the line voltage affecting both the offending equipment and other equipment connected to the same power line.
2. Conducted and radiated electromagnetic interference resulting from harmonics currents drawn from the power source causing impaired performance of nearby electronic systems.
3. Poor utilization of the capacity of power source.
4. Higher losses and reactive voltage drops in the power distribution network.

Now several international standards, [3] and [4], require that the harmonics of the line-current of an electronic equipment stay below certain specified levels. The design engineers of a utility fed AC-DC switching regulator must now consider the effects of the regulator not only on the DC load, but also focus on the AC mains. In essence, the design has to consider the quality of the input current as well as the output voltage.

Cascaded power-factor-corrected switching regulators provide the low current harmonics distortion and fast voltage regulation. Inefficient operation is the major drawback in typical cascaded power-factor-corrected switching regulators. In this study, focus is put on the efficient and non-cascaded power-factor-corrected switching regulators, the idea of that regulators have been proposed recently [5]-[8]. However, a rigorous comparison of practical regulators and their design aspects are not yet available in the literature.

1.2 Literature Review

In the last decade, power factor correction have been seriously considered by the industrial and academic communities [9]-[14]. Figure 1.1 summarizes the power factor correction methods, that can be broadly classified as passive methods and active methods. An overview of both passive and active power factor correction circuitries are described by J. Sebastian et al. [15], W. G. Hurley [16], R. Redl [17], P. Jain et al. [18], and O. Garcia et al. [19].

Passive methods, input-inductor filters and tuned filters, give reliable solutions for reducing of harmonic currents. In 1981, Dewan [20] presented a

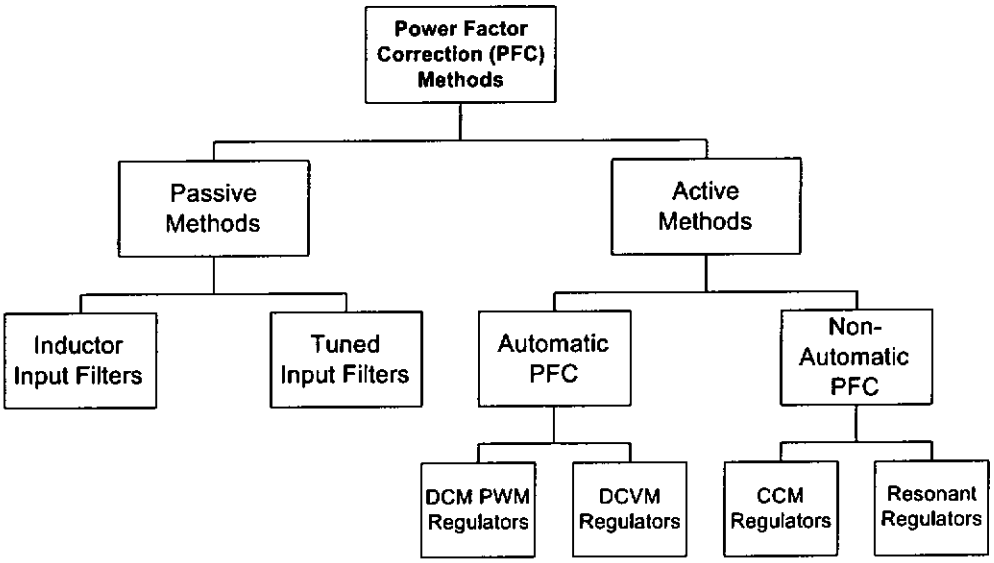


Figure 1.1: Classification of power factor correction methods.

paper mentioning optimum input-inductor filters design for single-phase rectifier power supplies. In 1989, Kelley and Yadusky [21] reported a quantitative computer-simulation-based analysis of single-phase and three-phase rectifier line-current harmonics and power factor as a function of the output filter inductor. But the bulky and heavy input-inductor filter is an unacceptable solution in modern electronic products. Merit of the tuned input filter compare with the input-inductor filter is that the size of the filter becomes smaller. In 1990 and 1992, Vorperian and Ridley [22], and Ignazio [23] proposed their series resonant filters respectively to achieve a high power factor with a sinusoidal input current. A novel passive method was proposed by Wolfle et al. [24] in 2000, there reported a new swinging inductor to implement adapted harmonic filtering over a wide power change range to overcome limited operating power range of the input-inductor filters and the tuned filters.

Active PFC methods can be classified as automatic PFC and non-automatic PFC. The output power level is a main consideration for using the automatic PFC and the non-automatic PFC [25]. It can be well understood [26]-[29] the basic converters operating in discontinuous conduction mode (DCM) offer automatic PFC due to their inherent resistive input impedance. In 1998, Chow et al. [30] proposed their boost DCM power factor correctors using both pulse

width modulation and frequency modulation for achieving high power factor, low bulk capacitor voltage, and fast voltage regulation. The DCM Ćuk converters for power factor correctors was reported by Brkovic et al. [31], and Simonetti et al. [32] in 1992, and 1997 respectively. In 1994, Peres et al. [33] reported a Zeta converter can also be used as an automatic PFC. Discontinuous capacitor voltage mode (DCVM) is that the voltage across a certain capacitor becomes zero for a portion of a switching period. DVCM can also provide automatic PFC that was reported by Tse and Chow [34], and Lin and Lee [35].

Non-automatic power factor correctors are based on the control of the input inductor current of converters for achieving high power factor. In 1987, Schlecht and Miwa [36] proposed their active power correction for switching power supplies applying boost converter with clamping circuit. An interesting comparison was reported by Drobnik [37] that a push-pull converter cascaded-connected with front-end boost converter for PFC is more efficient than that push-pull converter without PFC. A new PFC circuit using a buck converter and a boost converter characteristics is proposed by Jiang and Lee [38]. A low output power PFC circuit applying flyback converter is introduced by Tang et al. [39]. A 1-kW battery charger with front-end hard-switched boost converter for PFC is given by Canales et al. [40]. Resonant converters are also proposed as non-automatic PFC [41]-[44], however, the design and the circuits operation are more complicated when compared to any non-resonant PFC converters.

The above-mentioned literature of the non-automatic power factor correctors presented unregulated or cascaded power-factor-corrected switching regulators. Non-cascaded or parallel power-factor-corrected switching regulators, provide PFC and fast voltage regulation, concept was proposed at 1993 by Jiang et al. [45]. In 1994, Jiang and Lee [46] presented a practical parallel power factor corrected switching regulator. Simulation results for the two-transformer PFC switching regulator with parallel power processing were discussed by Srinivasan and Oruganti [47]. A systematical method for generating non-cascaded power factor switching regulators is discussed by [6]-[8].

1.3 Objectives of the Thesis

The primary objective of this thesis is, based on the reduced-redundant-power-processing (R^2P^2) principle, to design and implementation non-cascaded power-factor-corrected switching regulators that can achieve in high power factor, fast output voltage regulation, and their high efficiency are compared in terms of their features and specifications. The designed and implemented regulators can be used for providing a systematical record for switching regulator design engineers.

1.4 Outline of the Thesis

Chapter 2 briefly reviews the definition of power factor. Basic PFC principles and some techniques used for power-factor-corrected switching regulator are described. Then an introduction for cascaded power-factor-corrected switching regulator and non-cascaded power-factor-corrected switching regulators are provided. Finally, it discusses the benefits of the non-cascaded switching regulators and outlines two particular non-cascaded switching regulators.

Chapter 3 discusses an Input-Side Non-Cascaded Power-Factor-Corrected Switching-Regulator for low power applications. Design aspects of this switching regulator such as power transformer, voltage stress and current rating of switches and diodes, and controllers are given. Experimental results and waveforms are reported. Comparison with the theoretical results are made to verify the R^2P^2 function of this switching regulator.

Chapter 4 describes an Output-Side Non-Cascaded Power-Factor-Corrected Switching-Regulator for high power applications. Analysis of this particular switching regulator is given. Experimental results and waveforms are reported that are compared with the theoretical results to verify the principle of R^2P^2.

Chapter 5 gives a detailed comparison of these two particular switching regulators. Features and specification of the switching regulators are discussed. Issue related to output power levels, circuit complexity, components stress, and ease of control are elaborated.

Conclusions and further improvements are given in Chapter 6.

Chapter 2

Review of Power Factor and PFC Circuits and Techniques

This chapter reviews the definition of power factor and the existing control methods in terms of the non-automatic power-factor-corrected switching regulators. The basic requirements of the power-factor-corrected switching regulators with PFC and fast voltage regulation are discussed in detail. The outline of two non-cascaded power-factor-corrected switching regulators will be shown.

2.1 Power Factor

The term power factor is borrowed from elementary AC circuit theory. Power factor is one of the common measures of the line current quality. It is connecting both voltage and current components. In this section, power factor is analyzed from different avenues and important observation are made.

2.1.1 Time-Domain Interpretation

Consider a load drawing a current i_l from the AC mains with voltage v_l. Both i_l and v_l are sinusoidal waveforms with period T_l. The load draws the average power that is given by:

$$P_{\text{ave}} = \frac{1}{T_l}\int_0^{T_l} v_l i_l dt \tag{2.1}$$

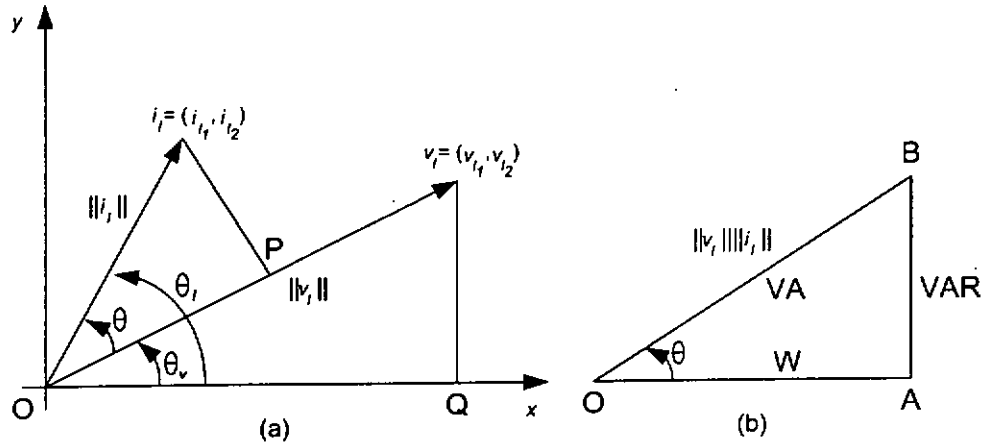


Figure 2.1: (a) The phasor diagram of the AC mains connecting with an capacitive load; (b) Power triangle.

where $\int_0^{T_l}$ represents the integral over any continuous interval of time length T_l. The power factor is defined by:

$$\text{Power Factor} = \frac{\text{P}_{\text{ave}}}{\text{V}_{\text{lrms}} \times \text{I}_{\text{lrms}}} \tag{2.2}$$

where V_{lrms} and I_{lrms} are presented by the R.M.S. line-voltage and line-current, are given by:

$$\text{V}_{\text{lrms}} = \sqrt{\frac{1}{T_l}\int_0^{T_l} v_l^2 dt} \tag{2.3}$$

$$\text{I}_{\text{lrms}} = \sqrt{\frac{1}{T_l}\int_0^{T_l} i_l^2 dt} \tag{2.4}$$

A set of afore-described equations is based on time-domain to represent power factor.

2.1.2 Vector-Algebra Interpretation

Figure 2.1 (a) and (b) show a phasor diagram and a power triangle of the AC mains. The phasor diagram shows that the AC mains connected to a capacitive load, because the current vector, i_l, is leading the voltage vector, v_l. From Figure 2.1(a), $\|v_l\|$ and $\|i_l\|$ are represented the fundamental components of the voltage and current. Also $\|v_l\|$ and $\|i_l\|$ denote respectively the length of the vector v_l and i_l. For example, $\|v_l\|$ is the hypotenuse of the triangle of

v_1OQ. θ indicates the phase difference between v_1 and i_1. Figure 2.1 (a) shows that:

$$\cos\theta = \cos(\theta_i - \theta_v) \tag{2.5}$$

$$= \cos\theta_i \cos\theta_v + \sin\theta_i \sin\theta_v \tag{2.6}$$

$$= \frac{v_{1_1} i_{1_1} + v_{1_2} i_{1_2}}{\|v_1\|\|i_1\|} \tag{2.7}$$

The power triangle shown in Figure 2.1 (b) indicates an information of the phasor diagram. The OA of Figure 2.1 (b), which is projection OP of i_1 onto vector v_1 in Figure 2.1 (a), is used to denote a real power of that capacitive load. A product of $\|v_1\|$ and $\|i_1\|$ is apparent power, OB, of the capacitive load. θ can be expressed by the power triangle as shown below:

$$\cos\theta = \frac{OA}{OB} \tag{2.8}$$

$$= \frac{\text{Real Power}}{\text{Apparent Power}} \tag{2.9}$$

From the mathematic point of view, the phasor diagram and power triangle also provide important information, that: the length of OA will be zero when $\|i_1\|$ is orthogonal with $\|v_1\|$, the maximum length of OA must be small or equal the length of the power triangle hypotenuse, OB. Furthermore, from the linear circuit theory, these observations give power factor $= \cos\theta \leq 1$, its means power factor can never be greater than unity. Power factor is the ratio of the real power to the apparent power ($\|v_l\|\|i_l\| = V_{lrms}I_{lrms}$ VA). The apparent power will be equal to the real power, if power factor is unity.

2.1.3 Power Factor for Sinusoidal Voltage

Power factor for sinusoidal voltage contains two parameters and they are called the displacement factor and the distortion factor. The displacement factor can be interpreted by vector-algebra easily, however, the distortion factor relates to the frequency-domain problem. A periodic distorted current signal, i_l, is represented by Fourier series with a fundamental angular frequency of ω as shown below:

$$i_l = I_l + \sum_{n=1}^{\infty} a_n \cos\omega nt + b_n \sin\omega nt \tag{2.10}$$

where a_n, b_n, and I_l are expressed below:

$$a_n = \frac{1}{\pi}\int_0^{2\pi} i_l \cos \omega n t dt \tag{2.11}$$

$$b_n = \frac{1}{\pi}\int_0^{2\pi} i_l \sin \omega n t dt \tag{2.12}$$

$$I_l = \frac{1}{2\pi}\int_0^{2\pi} i_l dt \tag{2.13}$$

When the current signal only contains the even function or the odd function, a_n is zero, the series becomes,

$$i_l = I_l + I_1 \sin \omega t + I_2 \sin 2\omega t + ... \tag{2.14}$$

where I_l is the DC component of the series and I_1 is the fundamental component of i_l. Because only the fundamental current can contribute to average power, according the definition of power factor from 2.2 and 2.9, an equation of power factor for sinusoidal voltage will be reconstructed to follow

$$\text{Power Factor} = \cos\theta \frac{I_1}{i_l} \tag{2.15}$$

where the $\frac{I_1}{i_l}$ is called the distortion factor. If i_l contains no a DC component, then the distortion factor can be written by

$$\frac{I_1}{i_l} = \frac{1}{\sqrt{1 + (\text{THD})^2}} \tag{2.16}$$

where THD denotes Total Harmonic Distortion, is defined by

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} {I_n}^2}}{I_1} \tag{2.17}$$

THD provides only the harmonic content but without provides the phase information. The displacement factor only contains the phase information of the fundamental components of the current and voltage.

In the case of the pure linear load, the line current contains only a fundamental component and power factor is solely determined by the displacement factor. On the other hand, the load is reactive, and nonlinear the input current can be both displaced, phase shift, and distorted. Fragmenting the power factor into two different factors is useful because these two problems require entirely different solutions. For example, if a power system is heavily loaded

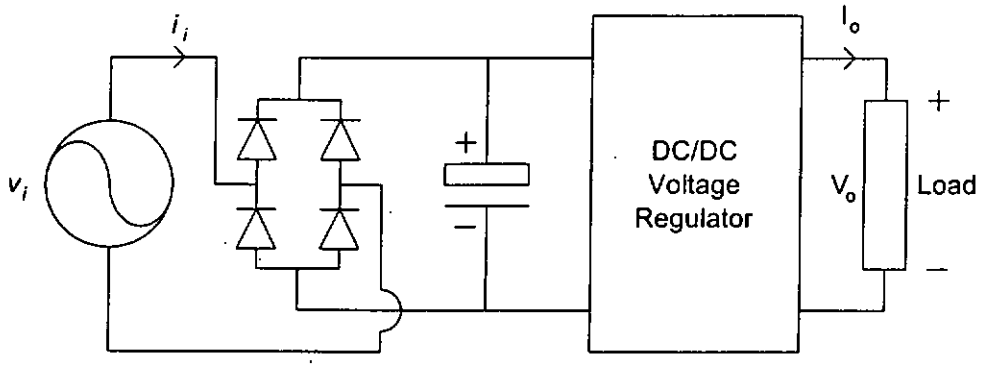


Figure 2.2: A simple input capacitor filter circuit for AC-DC power supply.

with an inductive load, it will be compensated by installing suitable parallel a capacitor to reduce the phase angle between the line voltage and the line current. However, a non-linear load requires a different solution as this becomes clear in Section 2.3.

2.2 Input Capacitor Filter

For low to medium power applications, the most common method to generating DC power from the AC mains uses an input capacitor filter circuit as shown in Figure 2.2. The circuit is a bridge rectifier followed by a filter capacitor for smoothing the rectified voltage. The filter capacitor voltage of the circuit should have a small ripple, which depends on the capacitor capacitance. The input capacitor filter is a cost-effective, simple, and rugged system which is often used with a post-regulator. The voltage regulation is provided by DC-DC converter for the well-regulated output voltage.

Unfortunately, the input capacitor filter suffers from a poor line current waveform. Since the output capacitor has large capacitance for maintaining a nearly constant voltage, the diode bridge turns on only for a narrow duration when the input voltage is close to its peak resulting in peaky input current pulses of the narrow duration as shown in Figure 2.3 (a). Although both Figures 2.3 (a) and (b) represent the same consumption of average power for any given resistance, the line current shown in Figure 2.3 (b) is smaller than that shown in Figure 2.3 (a). Compared to the pure resistive case, the input

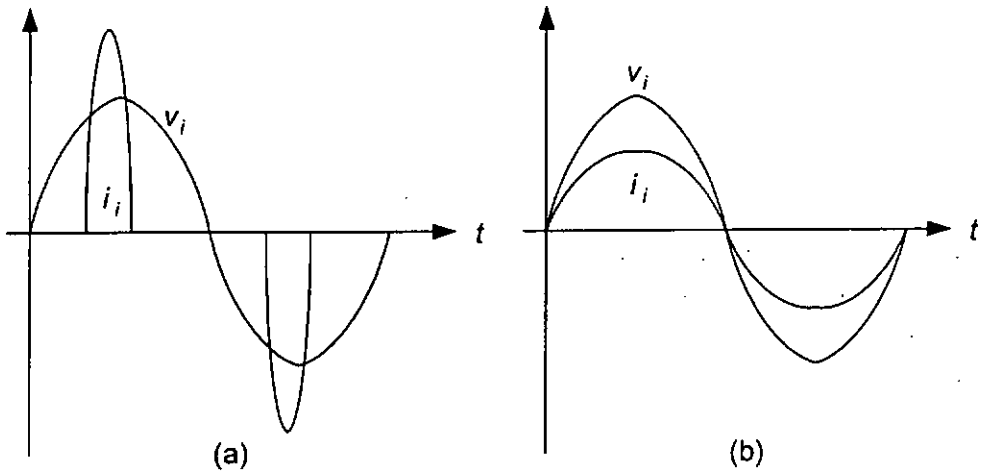


Figure 2.3: (a) A simple input capacitor filter circuit line voltage and line current waveforms; (b) The voltage and the current waveforms of the AC mains directly connect to a resistor.

capacitor filter circuit case shown in Figure 2.3 (a) demands a higher peak current and severe current harmonic distortion that impose a higher demand on the power generators, transformers, circuit breakers, and power transmission lines in order to supply the same amount of average power for the same loading. Hence, all the elements of a power distribution system should be designed for a higher rating, resulting in greater size, weight, and cost.

2.3 Active Power Factor Corrector

A typical active power factor corrector with an energy storage element is shown in Figure 2.4. This is a method for generating DC voltage from the AC mains. The corrector is constructed by a diode, a switch, and an inductor. The diode, D, is an ultra-fast diode, that is called a passive switch because the turn-on and turn-off time of that switch depends on the corrector switch. The switch, S, is an active switch, that should be operated at a high frequency, switching frequency, higher than the line frequency. In this particular power factor corrector, the input current is equal the inductor current, which is controlled by the active switch. A capacitor, C, is the energy storage element of the power factor corrector, its function will be discussed in next Section. The

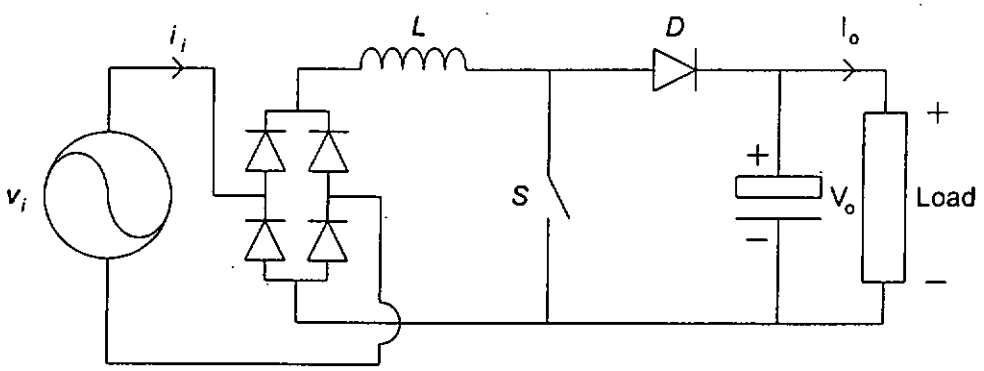


Figure 2.4: A typical active power factor corrector with an energy storage element.

output voltage of the power factor corrector should contain a ripple voltage and the ripple voltage frequency is twice of the line frequency, so the output terminal of power factor corrector always connects a DC-DC converter for providing the tightly regulated output voltage and the fast load transient response. Therefore all power factor correctors regardless of their employed circuit topology are also known as PFC pre-regulators.

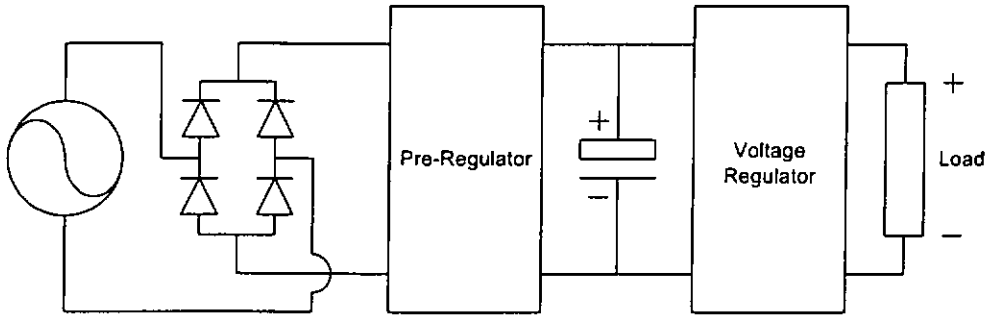


Figure 2.5: A block diagram of the common active power-factor-corrected switching regulator connection.

2.4 Basic Requirements of Active PFC Switching Regulators

Three basic stages, pre-regulator, voltage regulator, and energy storage element are essential components of the active power-factor-corrected switching regulators. A block diagram of the most of common active power-factor-corrected switching regulator is shown in Figure 2.5. A bridge rectifier is followed by a pre-regulator, then the pre-regulator output is connected to a capacitor which acts an energy storage element. The final stage of the switching regulator is voltage regulator.

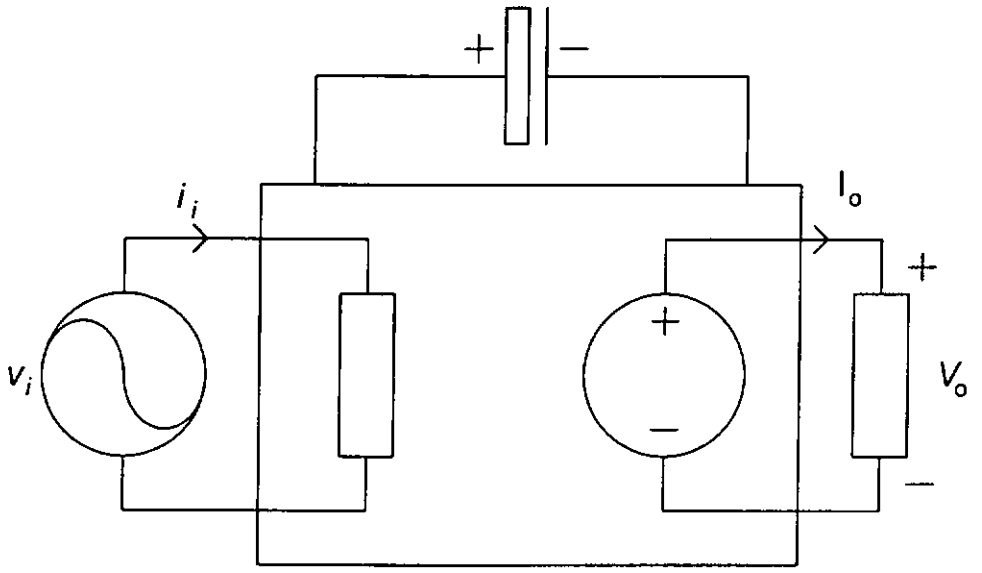


Figure 2.6: Three-port diagram for active power-factor-corrected switching regulator.

A three-port diagram is reported by [6], [7], and [48] as shown in Figure 2.6. The diagram presents the basic requirement of the active power-factor-corrected switching regulators. The input of the three-port diagram is a resistive load simulator. The simulator makes that the line current waveform is proportional to the line voltage. In the switching regulator, this property should be obtained by active control. An internal energy storage element is necessary to absorb and supply the difference between the instantaneous input

power and the constant output power. The internal energy storage element is also necessary to hold-up power for providing the output load during short-duration. For those reasons the internal energy storage element should have capability for storing the low frequency energy, therefore, a single electrolytic capacitor is invariably used to meet the requirements. A wide bandwidth regulated voltage source is provided by a switching converter for servicing the output load, because the simulator can be only provide unregulated voltage, which contain second harmonic ripple voltage. The regulated output voltage must not contain the second harmonic ripple voltage. Hence the voltage regulator is required and controlled by a feedback loop with wide bandwidth much greater than the second harmonic frequency.

2.4.1 Pre-Regulator

2.4.1.1 Buck Pre-Regulator

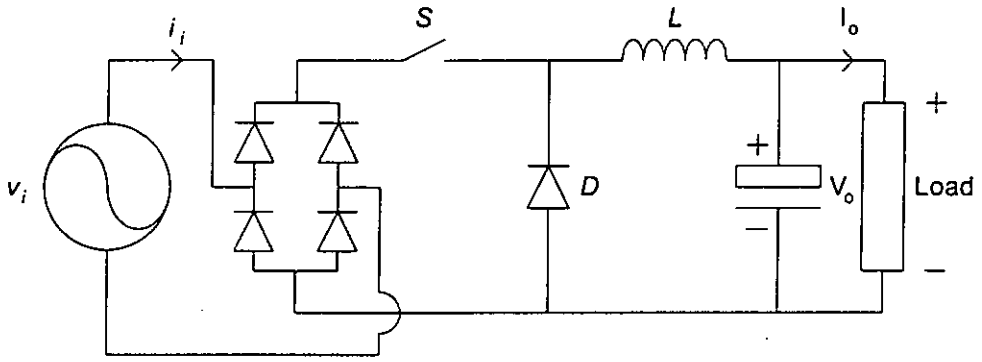


Figure 2.7: Buck pre-regulator.

Figure 2.7 and Figure 2.8 show a buck pre-regulator circuit and the typical line current waveform of the buck pre-regulator together with the AC mains voltage. A forward converter, an isolated buck converter, is discussed by Pereira et al. [49] and Nagao [50] for providing PFC. The line current becomes zero when the instantaneous line voltage is below than the output voltage. That leads a significant distortion of the line current. Furthermore, the buck pre-regulator input current is pulsating, an additional L-C filter is needed for smoothing the pulsating input current. The active switch driver is

an isolated gate drive circuit. Because the buck pre-regulator has about drawbacks, the buck converter are seldomly used for acting to PFC pre-regulator.

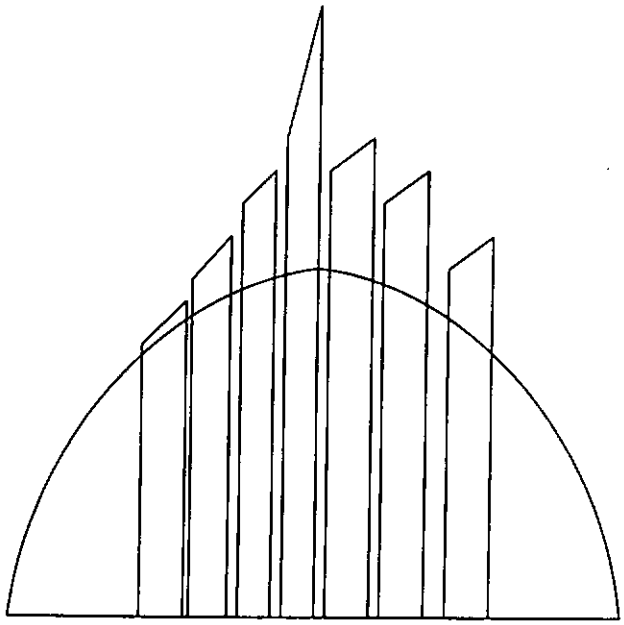


Figure 2.8: Switch current in buck pre-regulator.

2.4.1.2 Boost Pre-Regulator

The continuous conduction mode (CCM) boost converter is the most common topology for PFC pre-regulator applications [51]–[53]. The boost pre-regulator offers the best utilization of the active switch [54] such as lower average and peak current rating, and can be applied a non-isolated gate drive circuit for the active switch. However, the output voltage of the boost pre-regulator is always higher than the AC mains peak voltage, that is an inevitable drawback of the boost pre-regulator.

There are many boost variations pre-regulator [55, 56], depending on the number of the switches and the location of the inductor. However the most significant classification is based on the operating mode of the inductor current, because the operation mode dictates the method of control and their PFC performance.

For high power applications, boost pre-regulators always operate in CCM. That makes a reasonable current rating of that pre-regulators semiconductor

devices. However, the problem of the CCM boost pre-regulators is slow reverse recovery time of the power diode. This effect leads the serious power loss of the CCM boost pre-regulator and reduces reliability of that pre-regulator. Apart from employing the ultra-fast diode [57], the passive snubber circuit [58, 59], and the active clamping and soft switching [60]–[64] techniques can also be applied to reduce the associated power losses.

The discontinuous conduction mode (DCM) boost converter is popular topology for PFC pre-regulators producing a high power factor but with a substantial amount of harmonic distortion on the line current. Under constant-duty-cycle operation, the amount of line-current harmonics can be reduced at the expense of high conversion ratio [26]. The DCM boost pre-regulators are free from the problem of slow reverse recovery time at the power diode, but the DCM boost pre-regulator active switch suffers the high peak and R.M.S. current rating for a given output power level compared with CCM boost pre-regulator.

2.4.1.3 Buck-Boost Pre-regulator

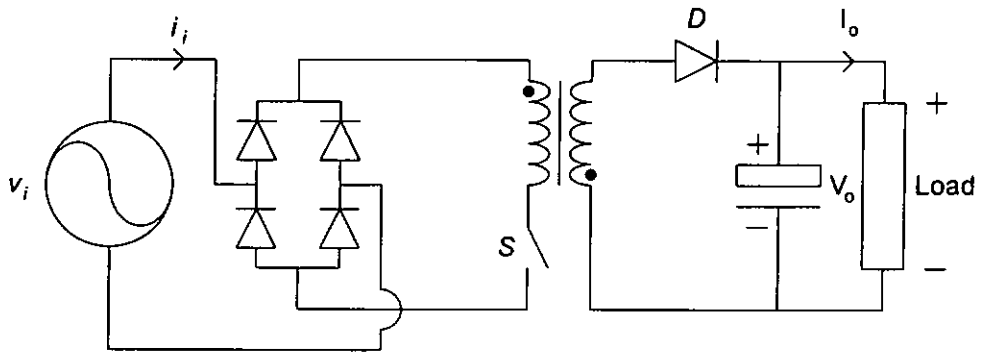


Figure 2.9: Flyback pre-regulator.

Figure 2.9 shows an isolated version buck-boost converter, flyback converter. The buck-boost pre-regulator has an output voltage step down and up capability, it can provide a wide input line voltage range for maintaining a low line-current distortion. This feature overcomes the buck and the boost pre-regulators drawbacks. Figure 2.10 shows the line current waveform together with the line voltage for the flyback PFC pre-regulator operated at CCM.

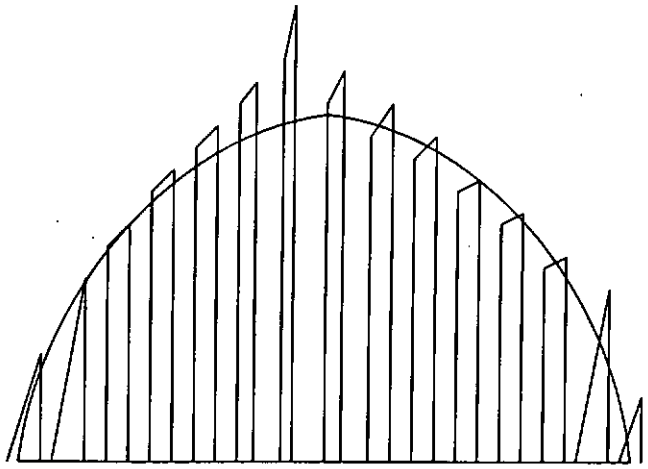


Figure 2.10: Switch current in flyback pre-regulator.

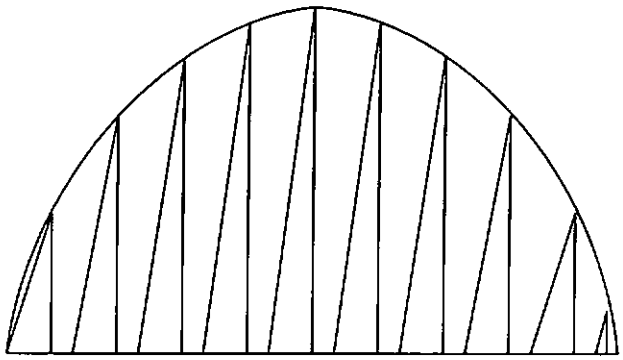


Figure 2.11: Switch current in flyback operated in DCM pre-regulator.

The flyback topology is usually furnishes for low power PFC pre-regulator applications, because it suffers serious voltage overshoot occurred at the active switch due to the energy stored in the leakage inductance of the isolating transformer. The voltage overshoot problem is solved by an effective clamping, which discusses in [65, 66].

The flyback converter can automatically simulates a resistor to get unity power factor without the harmonic current, when the converter is operated in DCM under constant duty-cycle and switching frequency operation [28]. This property can be easily understand because the averaged input line current is proportional to the line voltage along with the line period as shown in Figure

2.11. This feature leads that the DCM flyback converter provides a good solution for PFC at low power and cost applications.

2.4.2 Voltage Regulator

Voltage regulators provide fast voltage regulation to an output load. In a front-end boost power-factor-corrected switching regulator, the voltage regulator is providing the stepped-down voltage function and galvanic isolation. However, in the front-end flyback power-factor-corrected switching regulator, the voltage regulator is only providing voltage regulation. In essence any DC-DC converters can be voltage regulators.

2.4.3 Energy Storage Element

An energy storage element plays an important role in active power-factor-corrected switching regulators. Figure 2.12 shows power waveforms of the active power-factor-corrected switching regulator with unity power factor and perfect voltage regulation. For a constant load with the output power of P_{out}, the power drawn from the AC mains has a value of $P_{\text{out}}(1 - \sin 2\omega t)$ for an ideal active power factor corrector. The minimum stored energy necessary for unity-power-factor operation is the difference between the energy consumed by the constant-power load and the energy delivered by the AC mains during one-quarter of its period $\frac{\pi}{2\omega}$ starting with zero energy.

The energy consumed by the load, E_{dc}, during $0 < t < \frac{\pi}{2\omega}$ is

$$E_{\text{dc}} = P_{\text{out}} \frac{\pi}{2\omega} \tag{2.18}$$

The energy delivered by the line, E_{dc}, during $0 < t < \frac{\pi}{2\omega}$ is

$$\begin{aligned} E_{\text{ac}} &= \int_0^{\frac{\pi}{2\omega}} P_{\text{out}}(1 - \sin 2\omega t)dt \\ &= P_{\text{out}}(\frac{\pi}{2\omega} - \frac{1}{\omega}) \end{aligned} \tag{2.19}$$

The minimum stored energy is the difference between the two energies as given

$$\begin{aligned} E_{\text{min}} &= E_{\text{dc}} - E_{\text{ac}} \\ &= \frac{P_{\text{out}}}{\omega} \end{aligned} \tag{2.20}$$

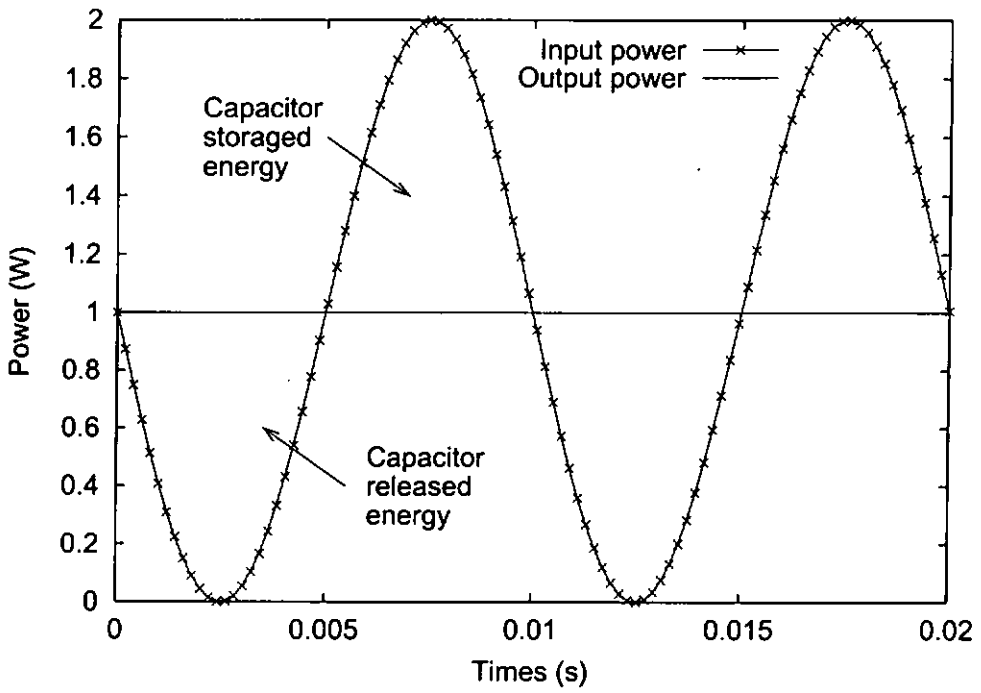


Figure 2.12: Power waveforms for ideal active power-factor-corrected switching regulator at line frequency equal 50 Hz.

If the storage elements is a capacitor C_s, the energy stored in the capacitor is

$$E_{C_s} = \frac{1}{2}C_s(v^2_{C_{s\max}} - v^2_{C_{s\min}}) \quad (2.21)$$

$$\text{or} = C_s V_{C_s}|\Delta v_{C_s}| \quad (2.22)$$

where E_{C_s} is the static value of v_{C_s}, and $|\Delta v_{C_s}|$ is the peak-to-peak variation of the v_{C_s}. Using equations (2.20) and (2.22)

$$|\Delta v_{C_s}| = \frac{P_{\text{out}}}{\omega C_s V_{C_s}} \quad (2.23)$$

Therefore, the amount of ripple voltage can be increased by adding an output load and can be reduced by a large capacitor under a high static stress.

In the case of a typical power-factor-corrected switching regulators, for maintaining the unity-power factor operation, the minimum capacitance can be obtained if the capacitor voltage is allowed to vary from zero to its peak value during each half of the AC mains period, such that $|\Delta v_{C_s}| = 2V_{C_s}$. The calculating minimum capacitance is

$$C_{s_{\min}} = \frac{2P_{\text{out}}}{\omega|\Delta v_{C_s}|^2} \quad (2.24)$$

2.5 Control Methods for Pre-Regulator

Figure 2.13 shows the simplify circuit diagram of a boost pre-regulator with active control of the line current and output voltage. Virtually the control circuit takes a rectified sinewave reference, synchronized to the line voltage, which provides a template for the line current controlling loop. The template level is multiplied by output feedback signal, the level of the output feedback signal depends on output voltage of the boost pre-regulator, via the electronic multiplier. Therefore the output voltage of the boost pre-regulator stays constant when the line voltage or load current varies.

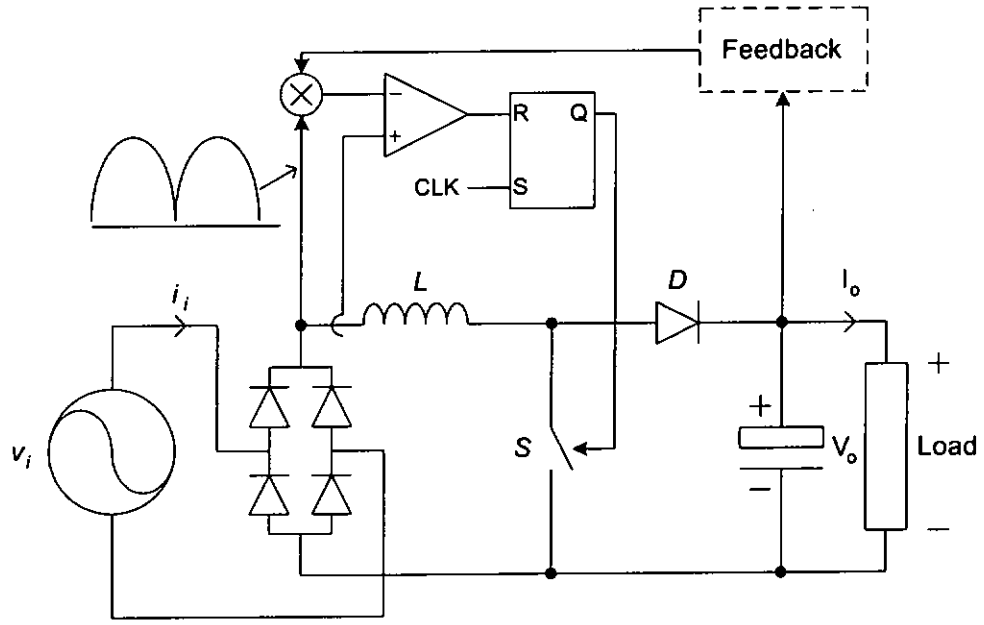


Figure 2.13: CCM boost pre-regulator under current-mode control simplify circuit.

The slow response time to a load change is major problem of the PFC pre-regulator. As mentioned in Section 2.4.3 due to the large line frequency ripple in output voltage, the crossover frequency of the voltage control loop of the pre-regulator must be kept below about half of the AC mains frequency. Excessive third-harmonic distortion is occurred by higher crossover frequency of the voltage control loop [67].

Feedforward of the line voltage can be used for reducing the response

times in the PFC pre-regulator without increasing the bandwidth of the loop gain. An example applies line voltage feedforward control for pre-regulator is shown in [68]. The result is that the output voltage is kept narrow variation based on the concept of the constant output power.

Several current-control methods are available for active control of the line current. Mahdavi et al. [69], gives consideration of their performances in terms of electromagnetic interference (EMI).

Average Current mode Control–The small line current distortion can achieved by an average current mode control. It is the most common method of the pre-regulators control. In essence, the average current mode control can be applied in any pre-regulator with different topological arrangement [70]. In a few switching cycle, inductor current of the pre-regulator is averaged for controlling the line current, so the average current tracks the line voltage with a high degree of accuracy. The additional advantage of this method is that the switching noise sensed by current sampling circuit can be effectively reduced by the effect of averaging. Figure 2.14 shows the boost pre-regulator line current waveform using average current mode control.

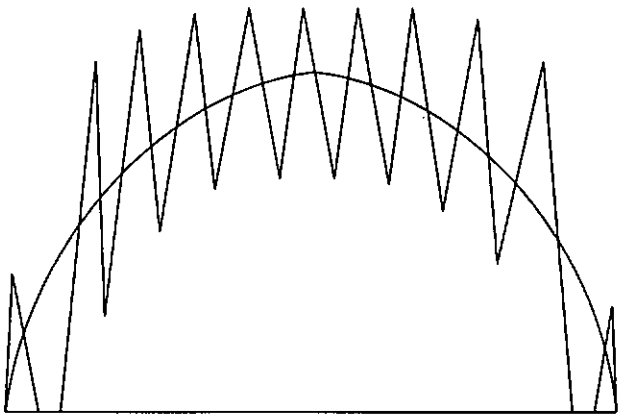


Figure 2.14: Boost pre-regulator line current waveform under average current mode control.

Peak Current mode Control–The simplest implementation is peak current

mode control [71] which has a cost-effective circuit. For the peak current mode control, the reference template plays an important role, that determines the line current shape and value. The active switch is turned off when the inductor current reaches the value governed by the controlled reference template, it is turned on again with constant frequency clock pulses. Figure 2.15 shows the line current waveform using peak current mode control applied at the boost pre-regulator. In the boost pre-regulator, the peak current mode control provides a very nice and low distortion input line current, because the peak inductor current value is as close as the averaged inductor current. However, in the buck-boost converter, the inductor current is not the input current, therefore the wrong current is controlled and leads distortion of the line current. Poor noise immunity is a disadvantage compared with average current mode control.

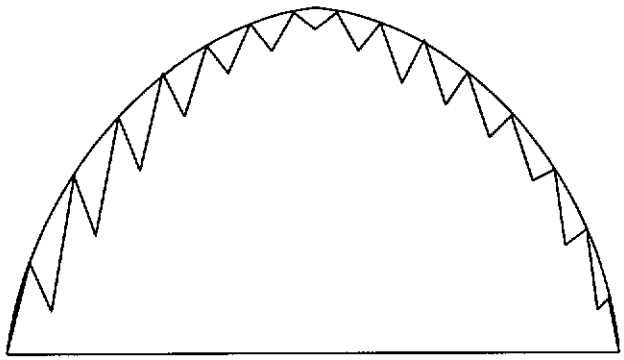


Figure 2.15: Boost pre-regulator line current waveform applies peak current mode control.

Hysteretic current mode control–Two reference templates, an upper reference and a lower reference, are determined the line current of the boost pre-regulator [72] as shown in Figure 2.16. The switch of the boost pre-regulator is turned off when the peak inductor current reaches the upper reference, on the other hand, the switch is turned on when the peak inductor current reaches the lower reference. The distortion of the boost pre-regulator line current depends on these two references. Without control loop, which reduces the control circuit

complexity, but the disadvantage of the hysteretic current mode control is that the switching frequency varies over the line period.

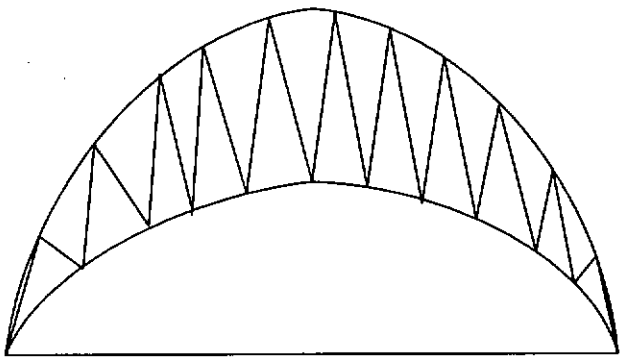


Figure 2.16: Boost pre-regulator line current waveform using variable hysteretic current mode control.

Borderline current mode control–Lower reference becomes the ground level, that is major difference between the borderline current mode control and the hysteretic current mode control. The boost pre-regulator operated in borderline current mode control is illustrated by Zhang et al. [73]. The boost pre-regulator enjoyably operates at borderline current mode control, because that inherent soft-switched property eliminates the losses associated with the power diode reverse recovery time and a borderline current mode control boost pre-regulator can serve for the front-end PFC pre-regulator for distributed power system. The main drawbacks of borderline current control are variable switching frequency and high differential mode EMI. However, the EMI problem can be solved by interleaving two boost pre-regulators with special switching sequence. Figure 2.17 shows line current waveform using borderline current mode control.

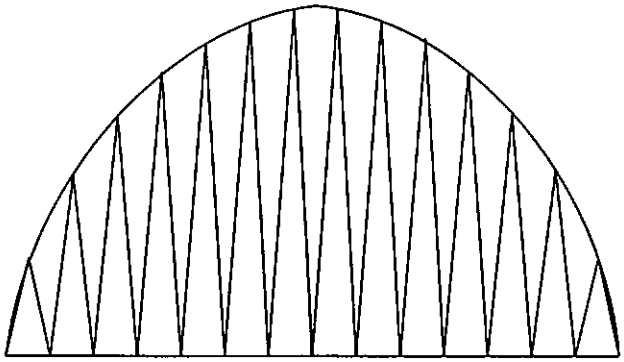


Figure 2.17: Boost pre-regulator line current waveform using borderline current mode control.

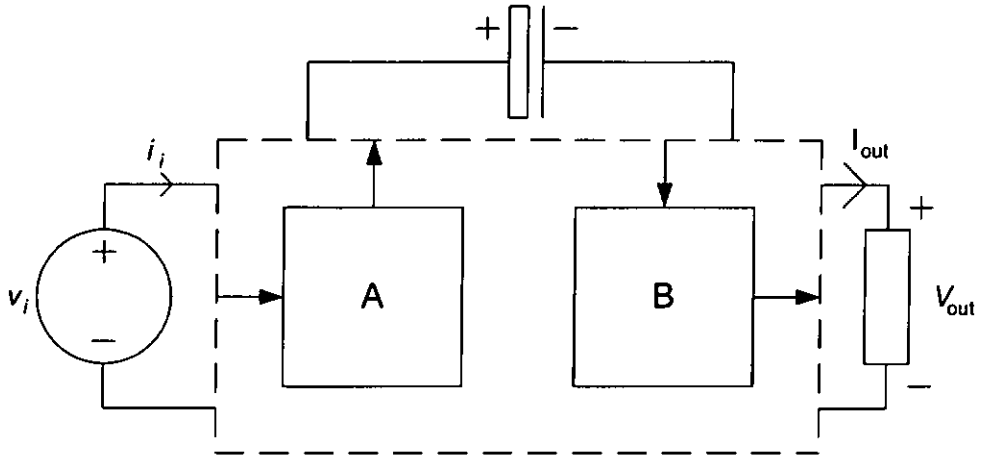


Figure 2.18: Power flow diagram for cascaded active power-factor-corrected switching regulator.

2.6 Non-Cascaded Active PFC Switching Regulators

Three port diagram, mentioned at Section 2.4, illustrates the switching regulators which must contain a pre-regulator, a voltage regulator, and an energy storage element for achieving the PFC and fast voltage regulation. The most straightforward way to design of an active power-factor-corrected switching regulator is to connect the regulators and the energy storage element serially. Efficiency is limited in this cascaded connection. For example, if the efficiency of pre-regulator is 80% and the voltage regulator also is 80%, the overall efficiency is 64% as shown in Figure 2.18. Non-cascaded active

power-factor-corrected switching regulators are allowed apart of input energy only processed by one power stage and this arrangement can increase overall efficiency of the PFC switching regulators.

Fifteen configurations of the non-cascaded active power-factor-corrected switching regulators are developed by [6]–[8]. In this fifteen configurations, the two particular configurations' power flow diagrams are shown in Figure 2.19 and Figure 2.20. They are named by Input-Side Non-Cascaded Power-Factor-Corrected Switching Regulator (ISPFC) and Output-Side Non-Cascaded Power-Factor-Corrected Switching Regulator (OSPFC).

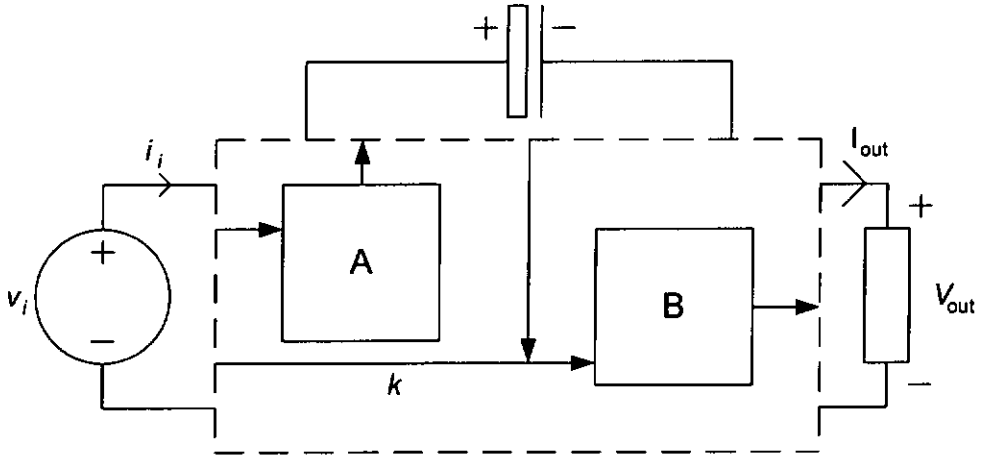


Figure 2.19: Power flow diagram for input-side non-cascaded power-factor-corrected switching regulator.

Theoretical efficiency of three switching regulators are shown below:

For the cascaded switching regulator shown in Figure 2.18, the efficiencies of the two converters are η_A and η_B, the overall efficiency is given by

$$\eta_{\text{cascaded}} = \eta_A \eta_B \tag{2.25}$$

For ISPFC shown in Figure 2.19, the efficiency equation is shown as follow

$$\begin{aligned} \eta_{\text{ISPFC}} &= (1-k)\eta_A\eta_B + k\eta_B \\ &= \eta_A\eta_B + k\eta_B(1-\eta_A) \\ &> \eta_A\eta_B \text{ for all } 0 < k < 1 \end{aligned} \tag{2.26}$$

where k is the ratio of the input power that is split between converter A and

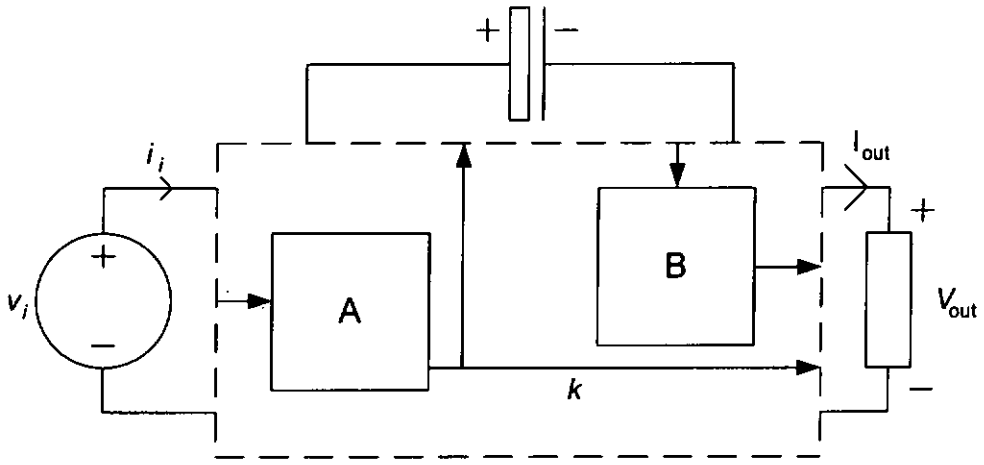


Figure 2.20: Power flow diagram for output-side non-cascaded power-factor-corrected switching regulator.

converter B, and η_A and η_B are the efficiency of the converter A and converter B, respectively.

For OSPFC shown in Figure 2.20, the efficiency equation is shown as follow

$$\begin{aligned} \eta_{OSPFC} &= (1-k)\eta_A\eta_B + k\eta_A \\ &= \eta_A\eta_B + k\eta_A(1-\eta_B) \\ &> \eta_A\eta_B \text{ for all } 0 < k < 1 \end{aligned} \tag{2.27}$$

where k is the ratio at which amount of input power is split at the output converter A to the output load.

As an observation of these equations, from Equation 2.26 and Equation 2.27, it is clear that ISPFC and OSPFC can achieve higher efficiency than the cascaded one. The efficiency gain of ISPFC and OSPFC are same, if the constituted converters have same efficiency.

2.7 Summary

This chapter gives detail definitions at time-domain interpretation and vector-algebra interpretation to explain power factor. A brief introduction describes the active power factor corrector. Basic requirements of active power-factor-corrected regulators is illustrated. In general, there are three basic components, a pre-regulator, a voltage regulator, and an energy storage element. Three-port diagram is used to explain the function of each component, such as the pre-regulator is a resistive load simulator, the voltage regulator provides a wide bandwidth regulated voltage source, and the energy storage element is a buffer for absorbing the difference between the instantaneous input power and the constant output power. The advantages and drawbacks of buck pre-regulators, boost pre-regulators, and buck-boost pre-regulators are described. The reasons why these pre-regulators cannot provide tight output voltage regulation and fast load transient response are also explained based on energy balance consideration. The existing control methods, average current mode control, peak current mode control, hysteretic current mode control, and borderline current mode control, for power-factor-corrector are shown and illustrated with their merits and disadvantages. Finally, this chapter explains the benefits, efficiency gain, of the non-cascaded active power-factor-corrected switching regulators.

Chapter 3

Input-Side Non-Cascaded PFC Switching Regulator

For off-line low-power applications, power-factor-corrected switching regulators are usually operated in DCM. It always uses a DCM flyback converter for automatic PFC and galvanic isolation, then the DCM flyback converter is followed by a DC-DC converter for voltage regulation. However, this approach leads that the semiconductor devices, active switch and power diode, of the DCM flyback converter suffer high voltage and current stress rating, which causes the inefficient cascaded power-factor-corrected switching regulators to become even more inefficient. While a number of non-cascaded DCM switching regulators with PFC capability are already being proposed for low power applications. Therefore, a new off-line input-side non-cascaded power-factor-corrected switching regulator for low power applications studies in this chapter. Especially the switching regulator is constructed by a CCM buck-boost and a CCM two-switch forward converter, that using non-cascaded arrangement provides more efficient operation. In essence, the switching regulator has potential to serve medium (below 500W) power applications. A completed design procedure for that particular switching regulator is discussed. An outline of this switching regulator specifications are described, and using the block diagram, as mentioned at Figure 2.19, realizes that practical non-cascaded switching regulator.

The original contribution of this chapter is to develop a completed proce-

dure and an analysis of this particular switching regulator. A discussion is included to show voltage and current rating of the active switch and power diode and practical issue such as power transformer, core reset path, and snubber circuit related the switching regulator. The measured results and experimental waveforms validate the switching regulator, which achieves PFC and fast voltage regulation, and high efficiency are also provided.

3.1 Reported Non-cascaded Input-Side Converter: "Zeta Converter"

From the power flow diagram point of view, zeta converter is a non-cascaded input-side converter. Zeta converter merges a buck-boost converter and a buck converter to share same switch for operation. Zeta converter for PFC is introduced by [33, 74]. Figure 3.1 is shown a non-isolated zeta converter, which is constructed by two inductors and capacitors, a power diode and an active switch.

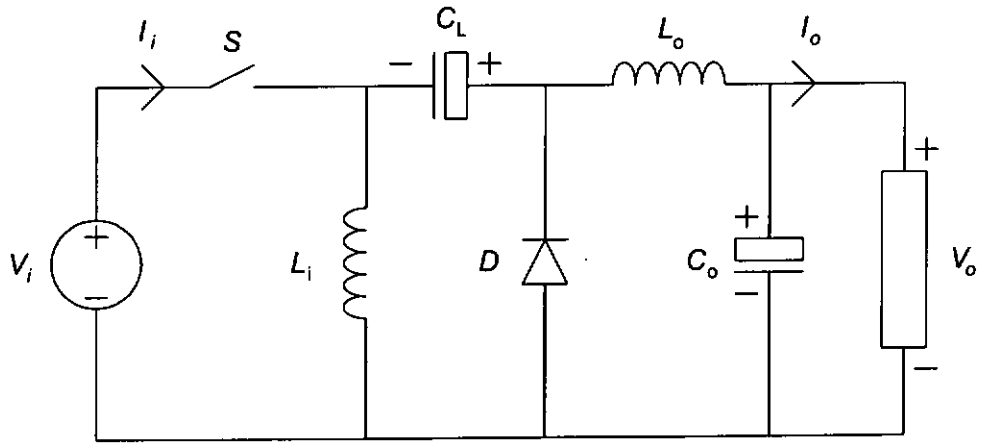


Figure 3.1: 'Non-isolated zeta converter'

The operation of zeta converter is split by two stages, switch turned-on and switch turned-off stages. When the active switch, S, is conducting, the input voltage source supplies energy to the input inductor, L_i. The energy available in the output inductor, L_o, comes from the line source and the capacitor, C_L. S is turned off and the diode, D, starts to conduct the energy

from L_i and L_o is transfered to C_L and the output capacitor, C_o, respectively. Zeta converter is named by input-side non-cascaded converter because it can allow part of the input voltage source energy directly transfered to load at the switch turned-on stage.

3.2 Specifications of ISPFC

The first step is that defines the specifications of input-side non-cascaded power-factor-corrected switching regulator (ISPFC) and according the specifications to implement a practical switching regulator. In the following discussion, the switching regulator provides output power at low power level, and the pre-regulator, buck-boost converter, and voltage regulator, two-switched forward converter, are operated in CCM. The output power range of the switching regulator is 25 W to 110 W. The input voltage is 110 V RMS and the output voltage is 24 V DC, and the storage element, capacitor, voltage level should be lower than 250 V. The switching regulator must provide galvanic isolation between the input port and the output port. The switching frequency of two converters are 100 kHz that optimizes the size and switching loss of the converters. For the simple circuitries reason, two converters should be operated at hard-switching. The power factor of the switching regulator should be able to meet international standard, IEC 61000-3-2 [3].

3.3 Realization of ISPFCs

As the name implies, the input-side non-cascaded power-factor-corrected switching regulator, that the switching regulator allows the AC mains power directly flowing to voltage regulator. The block diagram of ISPFC is shown in Figure 2.19. The square boxes denote a simple converter and the arrows denote power flow path and their direction. The next logical step for realization is to place a simple converter to the square boxes. Figure 3.2 is shown the equivalent circuit of ISPFC. The terminals X^+ and X^-, and Y^+ and Y^- represent the input port, and the output port of the simple converter respectively. The simple converter circuits are shown in Figure 3.3, which illustrates a short

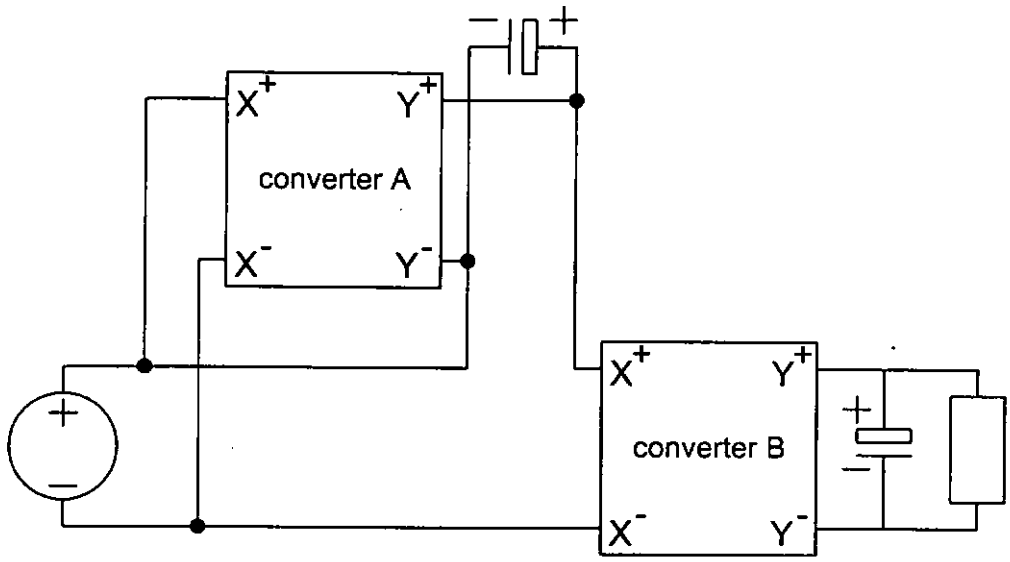


Figure 3.2: Equivalent circuit of ISPFC. Rectangular blocks denote converters.

circuit path of each converter. When places the simple converter into the square boxes, the care should be made to ensure that the short-circuit path imposed by the simple converters do not affect the intended connections.

For example, from Figure 3.2 at the converter A the negative input terminal, X^-, and the negative output terminal, Y^-, must be without connected path in normal operation of this switching regulator. Because if these two terminals provide a short-circuit path, it means that makes a short circuit path occurred in the AC mains. Therefore the converter A should be a buck-boost converter, but at the converter B it can be any simple converter. A possible solution for a non-isolated ISPFC using a buck-boost converter and a buck converter for converter A and converter B is shown in Figure 3.4. Using a buck converter places to converter B, because buck converter provides step down function for lower output voltage, which meets the specification discussed with previous section. Isolation is a compulsory requirement of the switching regulator. The next step is that changes the non-isolated ISPFC to become an isolated version. Because the AC mains has connected directly with the buck converter, the galvanic isolation transformer should be put on the converter B, buck converter. The isolated ISPFC is shown in Figure 3.5, the buck converter is replaced by forward converter for providing galvanic isolation.

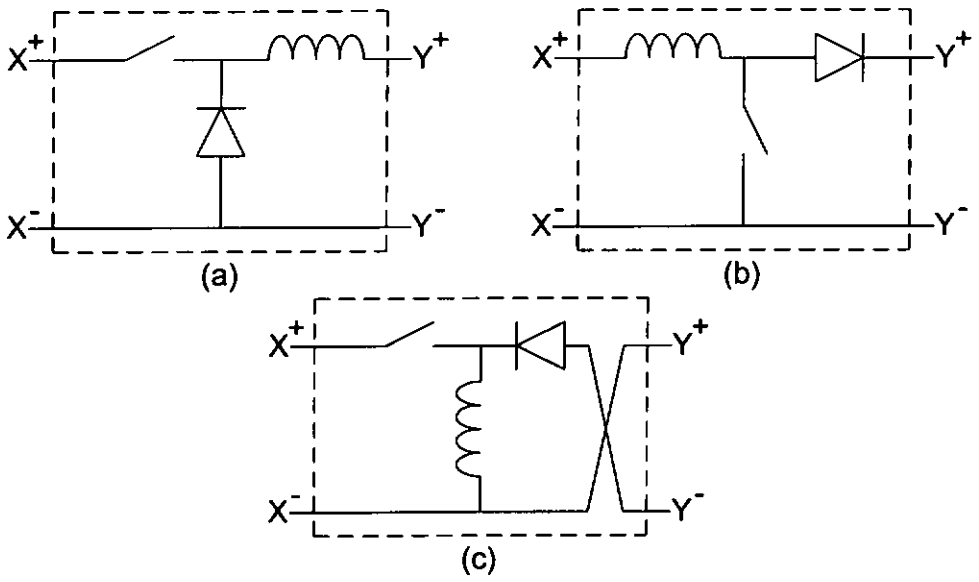


Figure 3.3: Basic voltage converter circuits (a) Buck; (b) Boost; (c) Buck-Boost.

3.4 Analysis of ISPFC

A detail numerical analysis is reported by Chow et al. [7]. Here describes the important aspects of this particular non-cascaded power-factor-corrected switching regulator in terms of circuit operation and control requirement. Figure 3.6 shows the average model of ISPFC, buck-boost converter and forward converter. It assumes that the storage element, C_L, voltage is constant, and the input of buck-boost converter is connected to a rectified sinusoidal voltage:

$$v(t) = \hat{v}|\sin\omega_m t| \tag{3.1}$$

The input to the forward converter is therefore given by

$$v_{\text{forward}} = V_L + \hat{v}|\sin\omega_m t| \tag{3.2}$$

where V_L is the capacitor voltage, ω_m is the AC mains frequency. Suppose that the output voltage is well regulated by the forward converter. In the steady state, assume that the forward converter efficiency is unity, therefore the input current of the forward converter is given by

$$i_{\text{forward}} = \frac{P_o}{V_L + \hat{v}|\sin\omega_m t|} \tag{3.3}$$

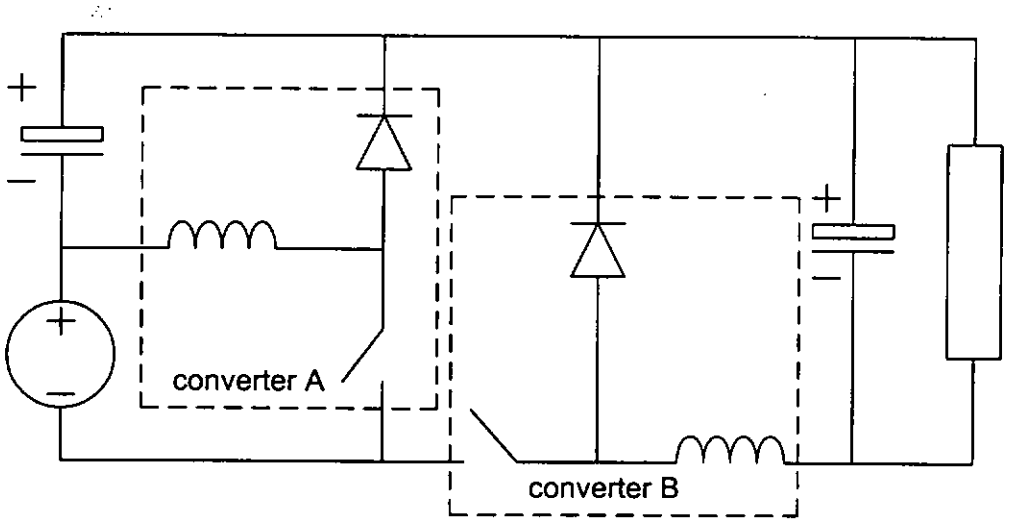


Figure 3.4: A possible solution for non-isolated ISPFC using a buck-boost converter and a buck converter for converter A and converter B.

where P_o is the output power drawn by the output load. Referring to Figure 3.6, the input current can be expressed as the sum of $d_1 i_{\text{buck-boost}}$, where d_1 is the duty cycle of the buck-boost converter, and the current drawn by the forward converter

$$i_i = d_1 i_{\text{buck-boost}} + i_{\text{forward}} \tag{3.4}$$

Assumed that the switching regulator can achieve unity power factor, i_i is proportional to the input voltage waveform, i_i is expressed by

$$i_i = \hat{i}_i |\sin \omega_m t| = \frac{2P_o}{\hat{v}} |\sin \omega_m t| \tag{3.5}$$

As an observation from Equation 3.4, $d_1 i_{\text{buck-boost}}$ should be contain negative value when i_i is close to zero-crossing of the AC mains line cycle. The negative value can be reduced by increasing the storage element voltage level. Thus, this illustrates that the power factor of this particular switching regulator is below unity and it has a bit high total harmonic distortion when i_{forward} is increased, because i_i contains the DC current component.

In order to maintain high power factor and voltage regulation, the duty cycles of two converters should be vary independently. d_1 and d_2 are denoted by the buck-boost converter and the forward converter duty cycles, respectively. d_2 can be interpreted by

$$d_2(t) = \frac{V_o}{V_L + \hat{v} |\sin \omega_m t|} \tag{3.6}$$

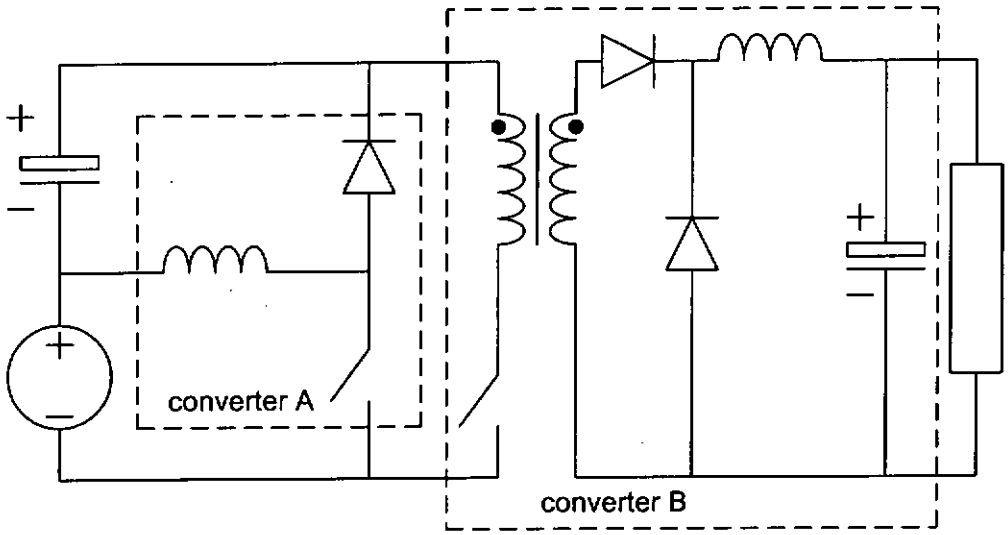


Figure 3.5: Isolated ISPFC using a buck-boost converter and a forward converter for converter A and converter B (Core reset arrangement omitted for brevity)

where V_o is the DC output voltage. Using Equations 3.3 and 3.4, the value of d_1 can be solved as follows

$$d_1(t) = \frac{2P_o|\sin\omega_m t|}{i_{buck-boost}(t)\hat{v}} - \frac{P_o}{i_{buck-boost}(t)(V_L + |\hat{v}\sin\omega_m t|)} \tag{3.7}$$

Based on the relationship between the current and voltage of an inductor, the current of inductor L_i can be related as

$$\frac{di_{buck-boost}(t)}{dt} = \frac{(V_L + \hat{v}|\sin\omega_m t|)d_1(t) - V_L}{L_i} \tag{3.8}$$

Thus, from Equations 3.7 and 3.8, $i_{buck-boost}$ is given by

$$\frac{di_{buck-boost}(t)}{dt} = \frac{P_o[2|\sin\omega_m t|(V_L + \hat{v}|\sin\omega_m t|) - \hat{v}]}{L_i\hat{v}i_{buck-boost}(t)} - \frac{V_L}{L_i} \tag{3.9}$$

The two duty cycles are represented by two Equations 3.6 and 3.7, therefore the two duty cycles could be operated independently.

3.4.1 Gain of Efficiency

The theoretical overall efficiency equation of ISPFC, as mentioned in last Chapter, is shown below:

$$\eta_{ISPFC} = \eta_A\eta_B + k\eta_B(1 - \eta_A) \tag{3.10}$$

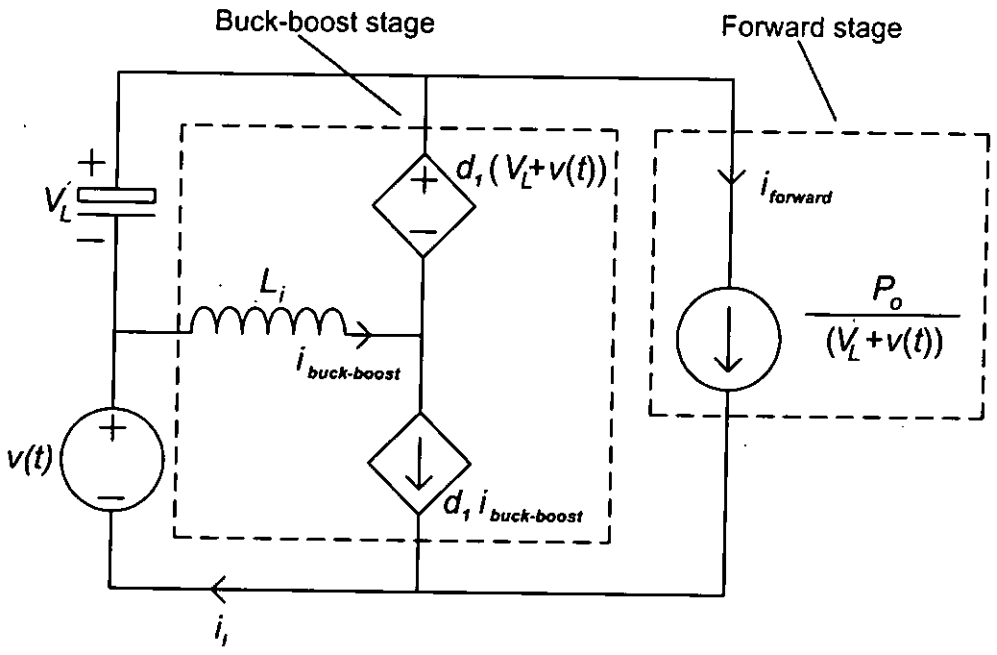


Figure 3.6: Average model for pre-regulator of the input-side non-cascaded power-factor-corrected switching regulator

In that equation, the factor k affects the efficiency gain of the switching regulator. η_A and η_B represent the efficiency of the buck-boost converter and the forward converter. It is useful if the factor k can be determined in terms of the circuit parameters of ISPFC. Based on Figure 3.6

$$P_o = i_{forward}(V_L + v(t)) \tag{3.11}$$

$$P_{direct} = i_{forward} v(t) \tag{3.12}$$

where P_{direct} is power directly transferred to the forward converter from the AC mains. Because $v(t)$ is equal to $\hat{v}|\sin\omega_m t|$, which value can be simplified by the following equation to become an average value.

$$V_{average} = \frac{2}{T}\int_0^{\frac{T}{2}} \hat{v}\sin\omega_m t d\omega_m t \tag{3.13}$$

where T is a period time of the AC mains line frequency.

Therefore, from Equations 3.11 and 3.13, the equation of P_{direct} can be re-arranged as

$$P_{direct} = \frac{v(t)}{V_L + v(t)} P_o$$

$$\text{or} \quad = \quad \frac{V_{\text{average}}}{V_{\text{L}} + V_{\text{average}}} P_{\text{o}} \tag{3.14}$$

In the foregoing analysis, the factor k can be determined by a ratio between the capacitor voltage and the averaged input line voltage.

$$k = \frac{V_{\text{average}}}{V_{\text{L}} + V_{\text{average}}} \tag{3.15}$$

Consideration based on a reverse power flow is shown in Figure 3.7 such that it is possible to show choosing which converter efficiency is the more important in ISPFC. The overall efficiency of ISPFC can be expressed by

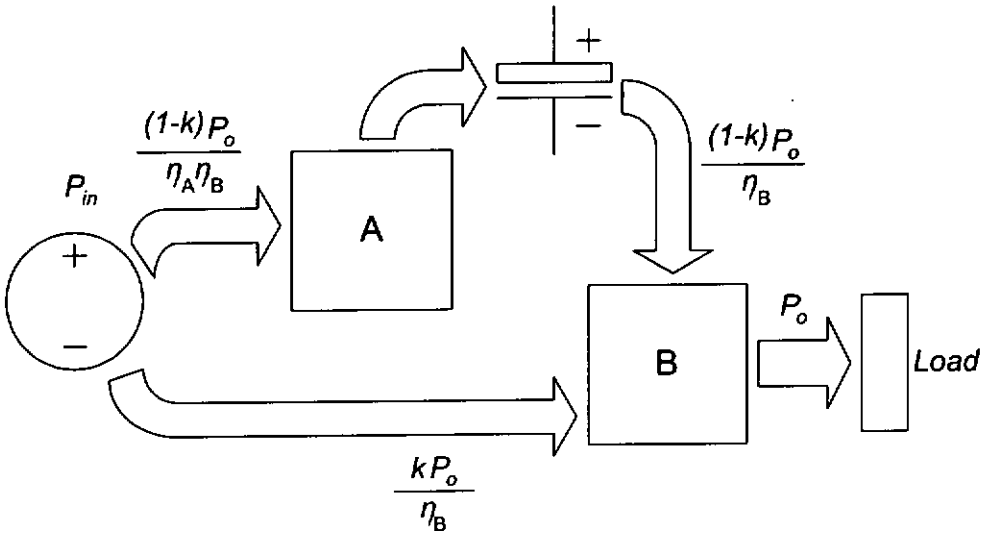


Figure 3.7: A schematic representation of the reverse power flow diagram in ISPFC

follow equations to become:

$$\begin{aligned} P_{\text{in}} &= \frac{P_{\text{o}}(1-k)}{\eta_{\Lambda}\eta_{\text{B}}} + \frac{kP_{\text{o}}}{\eta_{\text{B}}} \\ &= \frac{P_{\text{o}} - P_{\text{o}}k + kP_{\text{o}}\eta_{\Lambda}}{\eta_{\Lambda}\eta_{\text{B}}} \\ &= \frac{P_{\text{o}}(1-k(1-\eta_{\Lambda}))}{\eta_{\Lambda}\eta_{\text{B}}} \end{aligned} \tag{3.16}$$

$$\eta_{\text{ISPFC}} = \frac{P_{\text{o}}}{P_{\text{in}}} = \frac{\eta_{\Lambda}\eta_{\text{B}}}{(1-k(1-\eta_{\Lambda}))} \tag{3.17}$$

$$0 < k < 1$$

As shown in the result of this analysis, the forward converter efficiency, η_B, plays the most significant role in ISPFC. This is a reasonable result, because all power from input port must be processed by the forward converter.

3.4.2 Voltage and Current Rating of Semiconductor Devices

An important information for switching regulator designers to designing their input-side non-cascaded power-factor-corrected switching regulator is the voltage and current rating of semiconductor devices. In this particular switching regulator, because the pre-regulator has been chosen as a buck-boost converter, the minimum switch and power diode voltage stress of the pre-regulator should be equal to input line voltage adding with storage element voltage.

A two-switch forward converter is chosen for voltage regulator. The reason of using the two-switch forward converter is because a typical single-switch forward converter switch suffers twice of the input voltage stress, in this particular switching regulator, the input voltage of the voltage regulator is input line voltage plus storage element voltage, and this makes the single-switch forward converter undergoing an unreasonable high voltage stress and reduces the reliability of the voltage regulator. The switches of the two-switch forward converter voltage has only to tolerate the input voltage of the voltage regulator. This is the major reason for choosing the two-switch forward converter for voltage regulator at this particular switching regulator.

The maximum power of ISPFC is 110 W and the input line voltage is 110 RMS, therefore the input peak current is around 1.5 A. The current rating of semiconductor devices of the pre-regulator should be lower than 4 A. In the two-switch forward converter, the current rating of the switches must be lower than the input peak current, because the high input voltage of the voltage regulator. The output current of ISPFC is 4.6 A, then the current rating of the output diodes of the voltage regulator is around 5 A.

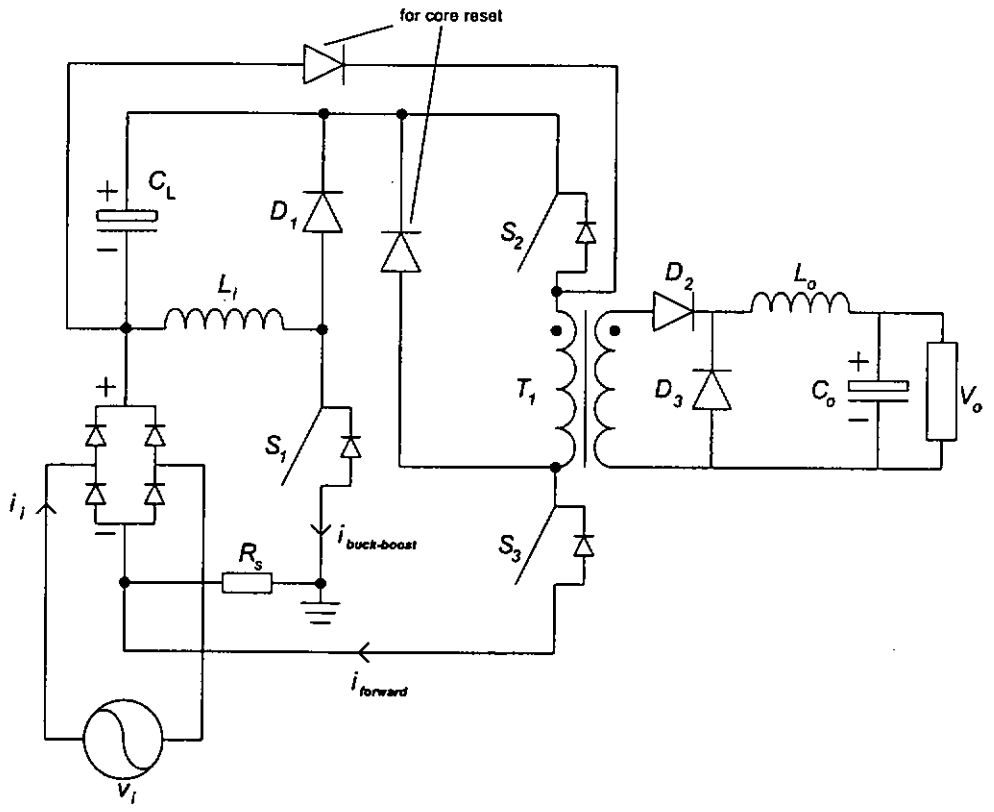


Figure 3.8: Simplified schematic circuit of ISPFC.

3.5 Circuit Implementation Overview

The simplified schematic of ISPFC, comprising of a non-cascaded connection the buck-boost converter and the two-switch forward converter, is shown in Figure 3.8. The two constituent converters have their independent active switches and control circuits. The AC mains is an input port of the buck-boost converter. The output terminal of the buck-boost converter is low frequency capacitive storage element, C_L.

A special arrangement on the two-switch forward converter input port is that the input voltage of the two-switch forward converter is the rectified line voltage superimposed with the voltage of C_L. Therefore part of power from the AC mains can directly transfer to load only via the voltage regulation stage. In the traditional two-switch forward converter, the magnetizing current of the transformer should have a reset path that flows through the input voltage source of that converter via two diodes. Therefore the reset arrangement for

ISPFC deserves some attention. Specifically the reset loop should avoid going through the AC mains where a bridge-rectifier prohibits current flow in the direction required by the reset. In Figure 3.8, the capacitive storage element voltage is used to reset the core during the switches turn-off time of the two-switch forward converter. In the practical point of view, the current return path of the two-switch forward converter is connected to the negative terminal of the bridge rectifier, because if the current return path is connected to the ground of the buck-boost converter, then the pulsating current generated by the two-switch forward converter merges with the switch current of the buck-boost converter, that confuses the current sense level of the PFC controller for providing PFC. The switch drivers of the two-switch forward converter must be floated with the buck-boost converter ground.

ISPFC can only be operated in low input line voltage, because the high input line voltage imposes an extremely high input voltage on the voltage regulator, furthermore, the pre-regulator switch and diode also suffering high voltage stress. A summary of the specifications of ISPFC is shown in Table 3.1. An experiment has been performed for validating the gain in efficiency by changing the voltage of the storage element from 160 V to 230 V. According to the average model analysis, the factor k is affected by the storage element voltage level and the input line voltage, and controls the gain in efficiency of ISPFC, therefore, this experiment clearly manifests the R^2P^2 function of ISPFC. The experimental results demonstrate once again that the voltage level of the storage element controls the current harmonic distortion and the efficiency gain of ISPFC. It is clear that the performance in current harmonic distortion can be improved by increasing the voltage level of the storage element at the expense of reduction in the efficiency gain.

3.6 Design Procedures

An average current mode control is used for achieving PFC in the buck-boost converter. The average current mode is a two-loop system. The buck-boost converter switch current is controlled by the inner loop, and the output voltage, capacitor voltage level, is monitored by the outer loop. A peak current mode control is applied for controlling the two-switch forward converter. A

Table 3.1: Specifications of the ISPFC

Specification	Value
Output power range	25-110 W
Input voltage	110 RMS
Output voltage	24 V DC
Storage element capacitor voltage range	160-230 V
Switching frequency	100 kHz

brief, step by step summary of the design procedure for ISPFC and control loops calculation are shown below.

3.6.1 Defining Component Values

Selection input inductance L_i:
The maximum peak line current is

$$\begin{aligned} I_{\text{pk}} &= \frac{\text{Output Power} \times \sqrt{2}}{\text{Input Voltage} \times \eta_{\text{ISPFC}}} \\ &= 1.76\text{A} \end{aligned} \tag{3.18}$$

where assume the η_{ISPFC} is 0.8.
Ripple current is defined by 30% of the maximum peak current.

$$\Delta I = 1.76 \times 0.3 = 0.528\ A \quad \text{,which is peak to peak value.} \tag{3.19}$$

Determine the duty cycle at peak current level where the input rectified voltage should be at peak level.

$$\begin{aligned} \frac{V_{\text{L}}}{V_{\text{peak}}} &= \frac{D}{1-D} \\ D &= \frac{V_{\text{L}}}{V_{\text{L}} + V_{\text{peak}}} \end{aligned} \tag{3.20}$$

At V_{L} equal 160 V, the duty cycle is 0.51, on the other hand, at V_{L} equal 230 V, the duty cycle is 0.60.
Calculate the inductance at a switching frequency of 100 kHz.

$$L_{\text{i}} = \frac{V_{\text{peak}} \times D}{\text{Switching Frequency} \times \Delta I} \tag{3.21}$$

The input inductance is 1.5 mH at the 160 V output voltage, and needs 1.76 mH at the 230 V output voltage. Because the purpose of ISPFC validates the R^2P^2 principle, for fair comparison, components of ISPFC must be same. The optimum inductance, 1.6 mH, is chosen.

Selection output capacitance, C_L:
Requirement of the output capacitor should have low equivalent series resistor (ESR) at both low and high frequency. The minimum capacitance can be calculated by using Equation 2.23 as shown follow

$$C_L = \frac{P_o}{\eta_{ISPFC} 2\pi V_L \times \text{Ripple Voltage}} \tag{3.22}$$

where the ripple voltage is defined by 5 V (peak to peak), therefore the capacitance of C_L is equal to 547 μF at output voltage of 160 V. At 230 V output voltage, the capacitance becomes 380 μF. The 470 μF low ESR capacitor is chosen for the storage element.

Selection of power transformer turn ratio:
The power transformer plays an important role in the switching regulator. In essence, as a typical two-switch forward converter, the duty cycle of that converter should be smaller than 0.5 for providing an enough time slot for resetting the magnetizing current of the power transformer and an enough voltage level for the output regulation. However, in this particular switching regulator, the consideration of the resetting time slot becomes more complicated, because the input voltage level of the converter varies with double line frequency of the AC mains, but the reset voltage source is the storage element voltage only. According this condition, the procedure for calculating the power transformer turn ratio is shown as follows:
Assuming the output voltage of the two-switch forward converter is 26 V (supposing the power diode and the copper wire have 2 V voltage drop), the maximum duty is 0.48, and the input voltage is 160 V, which means that the rectified line voltage closes to zero-crossing level. The turn ratio can be expressed by

$$V_o = V_{forward} \times D \times \frac{N_s}{N_p} \tag{3.23}$$

$$26 = 160 \times 0.48 \times \frac{N_s}{N_p}$$

$$\frac{N_s}{N_p} = 0.338 \tag{3.24}$$

where $V_{forward}$ denotes the input voltage of the two-switch forward converter, and the N_s and N_p represent the number of turn of secondary and primary of the power transformer respectively. At the afore-described case the transformer turn ratio, $N_p : N_s$ is around equal 3:1. The next logical step is to prove this turn ratio provides an enough time slot for release the magnetizing current. The worst case should be that the input voltage is $V_{peak} + V_L$ but the reset voltage is V_L. So the turn-off, T_{off}, time of the two-switch forward converter must be double or longer than turn-on time, T_{on}. Using Equation 3.23 to calculate the time slot for resetting magnetizing current is shown as follows:

$$\begin{aligned} T_{on} &\leq 2T_{off} \\ D &\leq 0.33 \\ 26 &= 320 \times D \times 0.333 \\ D &= 0.24 \end{aligned}$$

where the calculated result shows that the power transformer has enough time for the resetting, so the power transformer's turn ratio is 3:1. Table 3.2 shows the value of ISPFC.

Table 3.2: Summary for defining component values of ISPFC

Component	Value
Input inductance	1.6 mH
Output capacitance	470 μF
Output voltage	24 V DC
Power switches voltage stress	500 V
Diode of buck-boost converter voltage stress	500 V
Current rating of buck-boost converter	5 A
Power Transformer turn ratio	3:1

3.6.2 Control loop Parameters

An average current mode control based on Unitrode PFC controller UC3854 is employed in the buck-boost converter. The detail calculation the buck-boost converter gain and designing the optimum current control loop are shown in Dixon [70]. The testing stability procedures for power factor correction circuits applying average current mode control is reported by Venable [75]. A peak current mode control is applied in the two-switch forward converter. A common control chip, UC3845, is employed. The average current model control and peak current mode control are two-loop system. Here describes some important issues of that particular switching regulator.

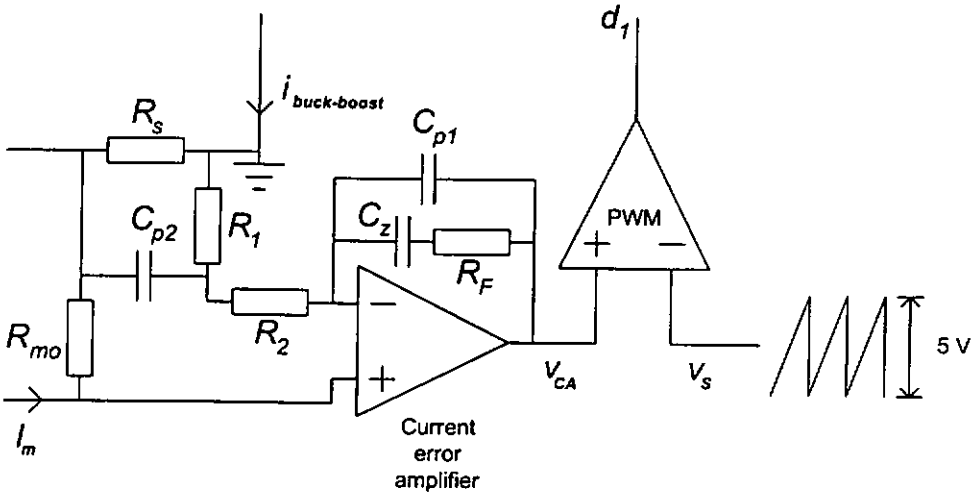


Figure 3.9: A simplified schematic current error amplifier circuit of the average current mode control for ISPFC

3.6.2.1 Current Error Amplifier of Buck-Boost Converter

Figure 3.9 shows current error amplifier circuit of the average current mode control for ISPFC. The large amplitude chopped current waveform of the buck-boost converter must be integrated by error current amplifier. The upslope of the integrated signal at the error current amplifier must not exceed the ramp signal of the PFC controller. The result causes lower crossover frequency, f_c, and the lower gain-bandwidth. The small-signal control-to-input

gain of the buck-boost converter current loop power circuit (from V_{CA} at the current error amplifier output, to v_{RS}, the voltage across R_s) is:

$$\frac{\hat{v}_{RS}}{\hat{v}_{CA}} = \frac{R_s}{V_s}(i_{buck-boost} + \frac{V_L}{sL_i}) \tag{3.25}$$

where R_s is equal 0.35 Ω. The minimum zero frequency can be calculated as:

$$\begin{aligned} f_z &= \frac{V_L}{2\pi L_i i_{buck-boost}} \\ &= 9 \text{ kHz} \end{aligned} \tag{3.26}$$

The minimum zero frequency is 9 kHz, and the gain above the minimum frequency is 0.12, which is around equal -18.4 dB. The average value of the chopped switch current is compared to the current program level across R_{mo} and amplified. Assumed that the C_{p2} and C_{cz} are open circuited. The current error amplifier gain at switching frequency, f_s, can be determined by integrator time constant $(R_1 + R_2)C_{p1}$. The optimum current error amplifier gain at switching frequency is the gain at which the maximum current error amplifier output upslope signal equals the upslope ramp signal. Because the R_{mo}, 2 kΩ, is fixed by the PFC controller current multiplier and the $(R_1 + R_2)$ must be equal to the R_{mo}, the C_{p1} is defined by

$$\begin{aligned} C_{p1} &= \frac{i_{buck-boost(pk)}R_s}{V_s f_s (R_1 + R_2)} \\ &= 592 \text{ pF} \end{aligned} \tag{3.27}$$

where V_s is peak to peak voltage level of the ramp signal. The current error amplifier integrator gain at high frequency can be calculated and entered in the bode plot:

$$G_p = \frac{1}{2\pi f (R_1 + R_2) C_{p1}} = \frac{134 \text{ kHz}}{f} \tag{3.28}$$

Figure 3.10 shows the buck-boost converter bode plot. The pole-zero pair is necessary to add the current error amplifier for providing high power factor and stable operation. The function of the zero is to increase the value of phase margin. The C_z of the current error amplifier is $4 \times C_{p1}$. The current error amplifier integrator gain at low frequency can be defined by

$$G_z = \frac{1}{2\pi f (R_1 + R_2)(C_{p1} + C_z)} = \frac{27 \text{ kHz}}{f} \tag{3.29}$$

The location of the flat portion of the current error amplifier gain is determined by R_F. Theoretically, the zero and pole should bracket the crossover frequency,

however, the crossover frequency is not at all critical. The loop response is really determined by the integrator gain below the zero curve. The crossover frequency in Figure 3.10 the error current amplifier in the flat portion is 15 dB. This is accomplished by

$$R_F = 5.6 \times (R_1 + R_2) = 11.2\ \text{k}\Omega \tag{3.30}$$

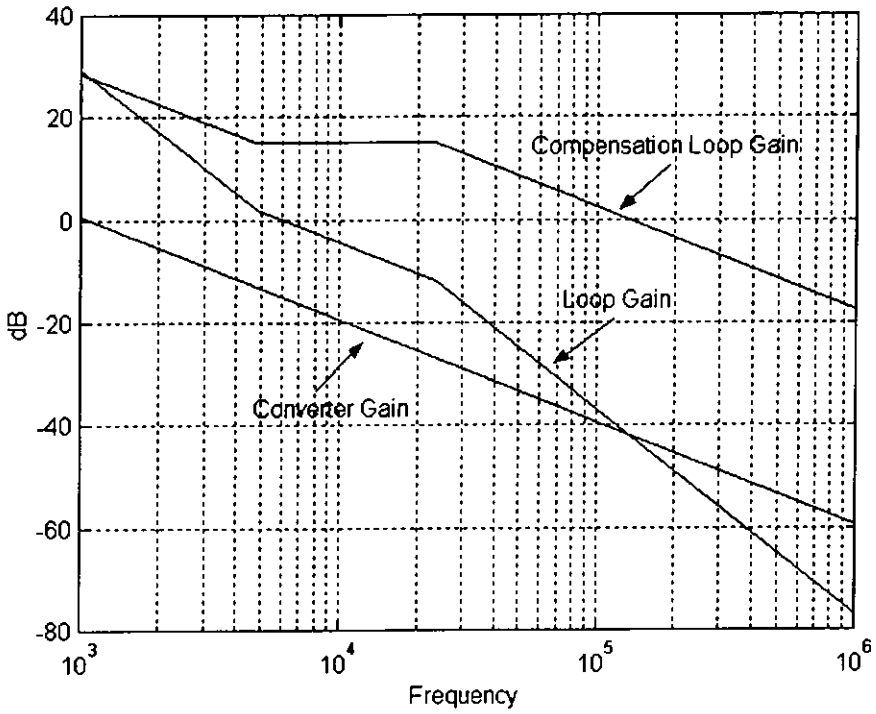


Figure 3.10: Buck-boost pre-regulator bode plot

Finally, an additional low pass filter, is constructed by R_1 and C_{p2}, is placed at switching frequency, 100 kHz, to filter out the noise spikes.

$$C_{p2} = \frac{1}{2\pi\ 100\ \text{kHz}\ 1\ \text{k}\Omega} = 1.6\ \text{nF} \tag{3.31}$$

3.6.2.2 Voltage Error Amplifier of Buck-Boost Converter

The PFC control chip, UC3854 provides feed-forward voltage mode control for monitoring the output voltage of the buck-boost converter. The advantage of the feed-forward voltage mode control is to speed up the response time

for regulation, however, it also has the chance to increase third harmonic distortion. Therefore feed-forward control pin of the PFC control chip is disabled by a DC voltage that do not affect the PFC function. Figure 3.11 shows a simplified circuit of the voltage regulation part for PFC controller. In essence, the voltage error amplifier input usually senses the output voltage of the buck-boost converter. In this ISPFC, the sampling resistor network is connected with capacitor positive terminal to the buck-boost converter ground, because the voltage control loop of the buck-boost converter uses a special and simple method for sampling the capacitor voltage, which is using an extreme low cut-off frequency one pole integrator to filter out the rectified line voltage. That integrator makes the input of voltage error amplifier only response with the DC voltage, capacitor voltage. This method effectively senses the output voltage of the buck-boost converter, and reduces the cost of ISPFC, because the sampling circuit does not need an external isolated circuit. The variable resistor in the sampling circuit adjust the capacitor voltage for measurement purposes.

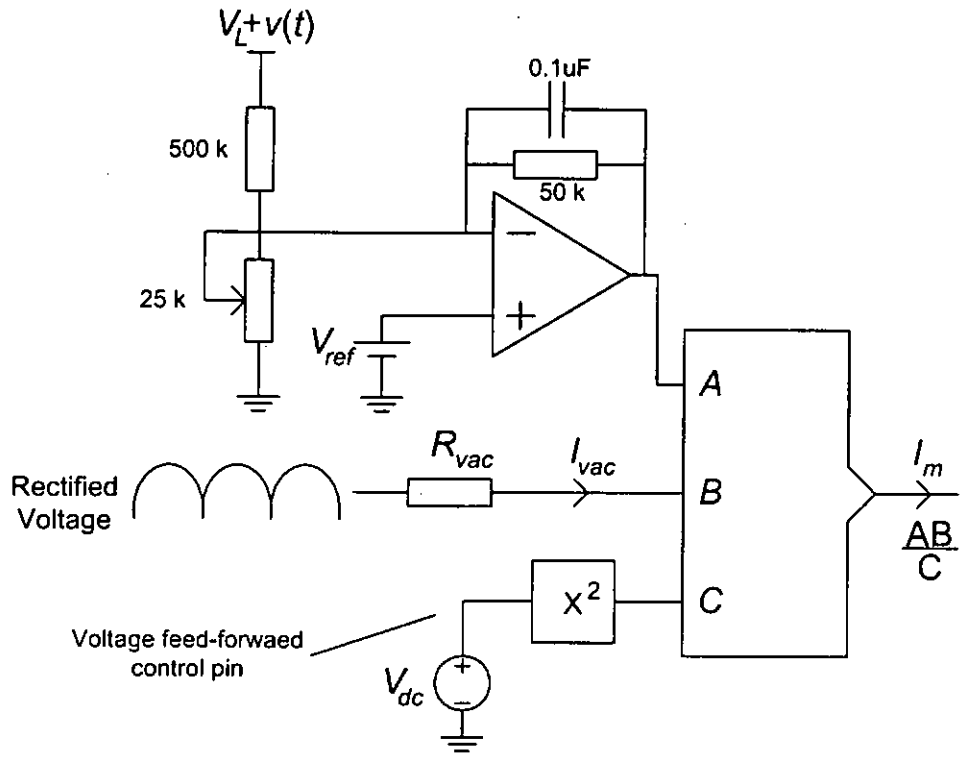


Figure 3.11: Simplified circuit of voltage error amplifier of the PFC controller

3.6.2.3 Control of Two-Switch Forward Converter

Theoretically, the most simplest control method, voltage mode control, can be applied in the two-switched forward converter, but in this particular switching regulator, the input voltage vary according to the AC mains line frequency, such that an additional feed-forward voltage loop control circuit is required in the voltage mode control for stable voltage regulation. For that reason, peak current mode control is employed to replace the voltage mode control. UC3845 is employed to control the two-switch forward converter, since that chip maximum duty cycle is limited to 0.5. Isolated gate drive circuits are needed.

3.6.3 Practical Issues for the ISPFC

According to the afore-description, the prototype of ISPFC component list and their specifications and completed practical ISPFC circuit are shown in Table 3.3 and Figure 3.12, respectively.

A turn-on snubber circuit for the buck-boost converter switch is shown in Figure 3.12. The reason of adding this extra snubber circuit is because the slow reverse recovery time problem occurs in the buck-boost converter power diode. When the switch is turned-on, the power diode needs a short time slot for turning off the conducted path. At this short time slot, the power diode suffers high voltage spikes. A solution for solving this problem is to reduce the speed of the switch turn-on time, since the turn-on snubber is applied in the switch. The power loss of the turn-on snubber circuit can be estimated by

$$\text{Power dissipation} = \frac{1}{2} L_s I^2 \times \text{Switching Frequency} \tag{3.32}$$

where I is the peak current in the input inductor, L_i, and it includes the power diode reverse recovery current. Power dissipation of the turn-on snubber circuit is proportional with L_s inductance and switching frequency. The inductor, L_s, functions normally when the switch turns on and the current only flows through the resistor, which is connected with power diode, when it is needed to dissipate the energy which is stored in the inductor. The power diode of the buck-boost converter is parallel connected with an R-C network circuit, which is passive method for compressing the voltage spikes.

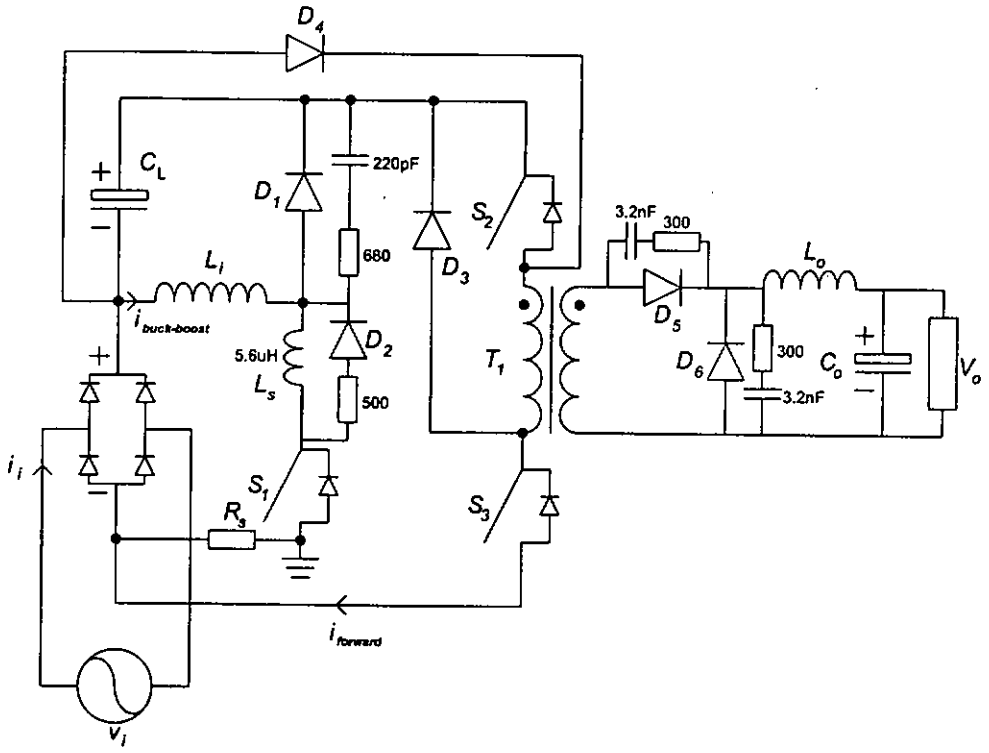


Figure 3.12: Completed circuit of ISPFC

Because switching voltage spikes of the two-switch forward converter switches are clamped by the capacitor voltage, V_L, via the reset path diodes, the switches do not need any snubber circuit for increasing their reliability. However, a leakage inductance, which is generated by imperfect coupling, in the power transformer affects the power diode of two-switched forward converter, R-C network circuits are connected in parallel with the power diodes.

Figure 3.13 shows the efficiency of ISPFC when the capacitor voltage is 160 V. The efficiency of the buck-boost converter and the two-switch forward converter are around 85%, which leads the overall efficiency of ISPFC at a low efficiency level, 75%. After an hour operation of ISPFC for testing, it is found that the power loss major occurred in the semiconductor devices, especially at power switches, and the snubber circuit resistors.

A modified ISPFC circuit is shown in Figure 3.14 to improve the efficiency of each converter. An L-C filter is added between the bridge rectifier and the input port of the buck-boost converter for prevention the high frequency switching noise to reduce power loss at the bridge rectifier. For reducing the

Table 3.3: Component list and their specifications

Component (part No.)	Specifications
Power switch (IRF840)	V_{DS}=500 V, $R_{DS(on)}$=0.85 Ω, I_D=8 A
Power diode D_1 – D_4 (MUR460)	V_{rr}=600 V, I_F=4 A, t_{rr}=75 ns
Power diode D_5 and D_6 (MUR820)	V_{rr}=200 V, I_F=8 A, t_{rr}=35 ns
Storage Capacitor C_L	V_{max}=400 V, $ESR_{low(100\ Hz)}$=250 mΩ,
470 μF (Philips:157-46471)	$ESZ_{high(10\ kHz)}$=210 mΩ
Output Capacitor C_o	V_{max}=35 V,
3300 μF (Panasonic:EEUFC1V332)	$ESZ_{high(100\ kHz)}$=15 mΩ
Power transformer ETD 49 (3C85)	Primary wire (4 AWG 26 lace up),
	No. of turns=39
	Secondary wire (10 AWG 26 lace up),
	No. of turns=13
Magnetizing inductance	3.39 mH
Input inductor L_i (Kool Mμ:77715A7)	1.6 mH,
	Wiring (4 AWG 26 lace up)
Output inductor L_o (Kool Mμ:77715A7)	300 μH,
	Wiring (10 AWG 26 lace up)
Snubber inductor L_s (Kool Mμ:77934AA7)	5.6 μH

conduction loss, all power switches are changed to a low conduction resistor switches, IRFP460. The turn-on snubber circuit is canceled. For increasing the reliability of ISPFC, two serially connected MUR460 are parallel with a rearranged R-C network and used as the buck-boost diode. The two-switch forward converter diodes are replaced by schottky diodes, MBR20200, to reduce the power loss occurred in the reverse recovery time. The specifications of two replaced semiconductor devices are illustrated in Table 3.4. The new rearranged buck-boost converter, two-switch forward converter, and ISPFC efficiency curves at 160 capacitor voltage are shown in Figure 3.15. The two converters efficiency are around 90%, which makes the overall efficiency of ISPFC to 84%.

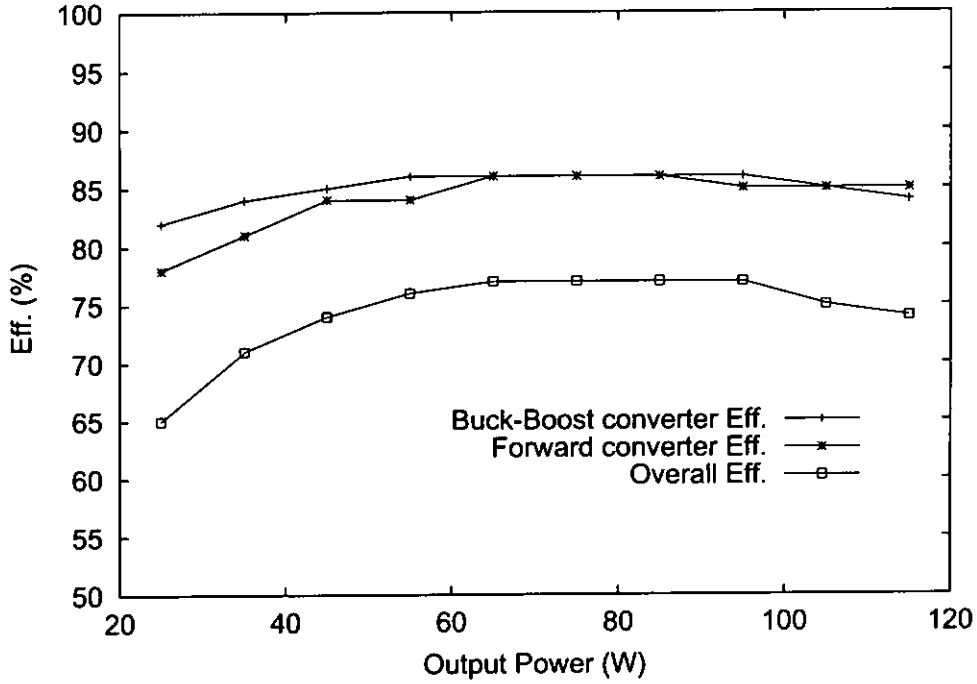


Figure 3.13: The efficiency curves for the buck-boost converter, the two-switch forward converter, and ISPFC at 160 V capacitor voltage.

3.7 Results for Validating R^2P^2 Principle and Experimental Waveforms

The section is attempted to demonstrate the advantage of the R^2P^2 principle of ISPFC experimentally. The rearranged circuit, shows in Figure 3.14, is tested over a power range from 25 W to 110 W. Since the prototype is to verify the function of the reduced redundant power processing, the measurements

Table 3.4: Comparison of semiconductor devices

Component	Part No.	Specifications
Power switch	IRF840	V_{DS}=500 V, $R_{DS(on)}$=0.85 Ω, I_D=8 A
	IRPF460	V_{DS}=500 V, $R_{DS(on)}$=0.27 Ω, I_D=20 A
Power diode	MUR820	V_{rr}=200 V, I_F=8 A, t_{rr}=35 ns
	MBR20200	V_{rr}=200 V, I_F=10 A

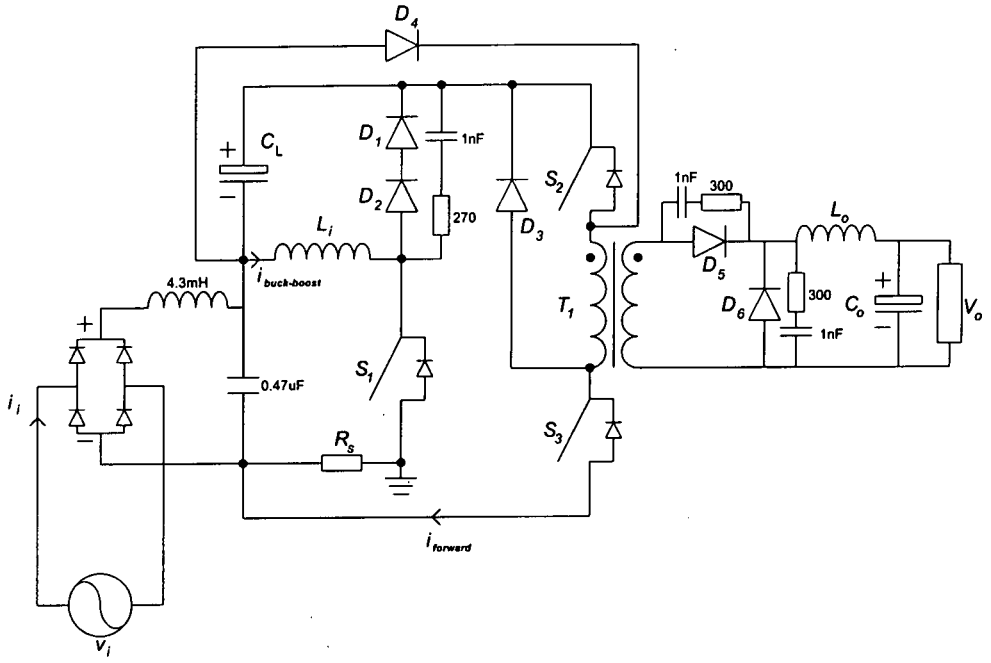


Figure 3.14: A new rearranged circuit of ISPFC for getting high efficiency

specifically take the efficiencies of the two constituent converters and compare their product with the measured overall efficiency, under the same k factor and input voltage level for each power level. For example, Figure 3.16 and Figure 3.17 compare the efficiencies for $V_{\rm L}$ from 160 V to 230 V, increasing 10 V per each measurement. Figure 3.18 shows a plot of efficiency versus $V_{\rm L}$ at 100 W output power. From Figures 3.16 and 3.17, the results show that the efficiency of ISPFC is generally improved over of a cascaded structure consisting of the same two constituent converters. Also, for a lower value of $V_{\rm L}$, the overall efficiency is higher, as shown in Figure 3.18. This agrees with the efficiency formulae given previously, i.e.

$$\eta_{\rm ISPFC} = \eta_{\rm A}\eta_{\rm B} + k\eta_{\rm B}(1-\eta_{\rm A}) \tag{3.33}$$

$$k = \frac{V_{\rm average}}{V_{\rm L} + V_{\rm average}} \tag{3.34}$$

Finally, to verify the PFC function, the harmonic distortion are measured for different $V_{\rm L}$ and output power level, shown in Figure 3.19, and some measured waveforms are shown in Figure 3.20. As a verification, the experimental results illustrate that the efficiency advantage gradually becomes less significant when $V_{\rm L}$ become large, as clearly shown from Figures 3.16 and 3.17. This

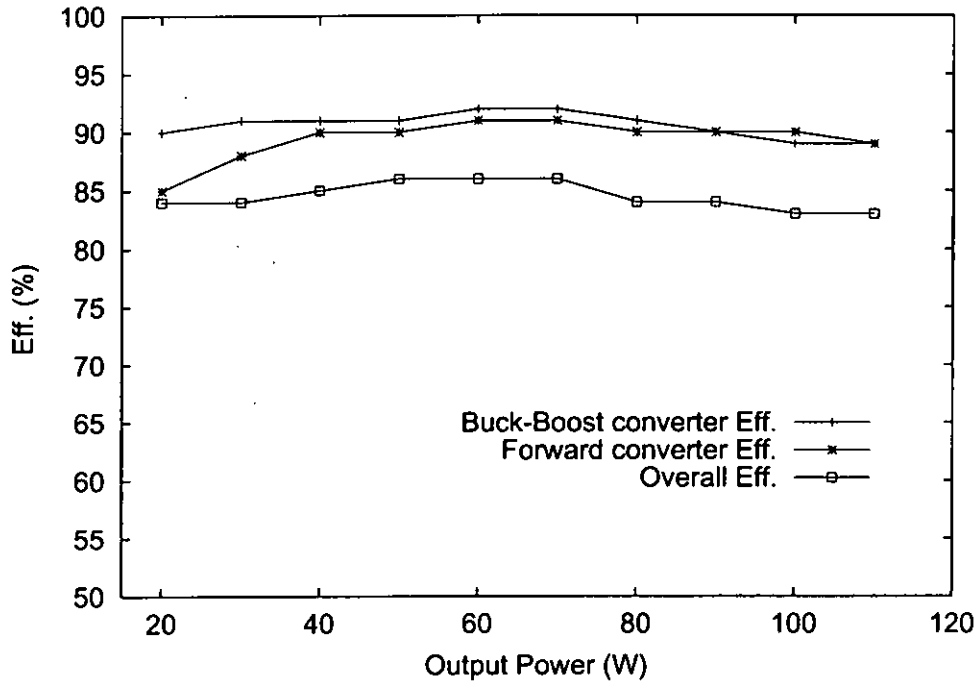
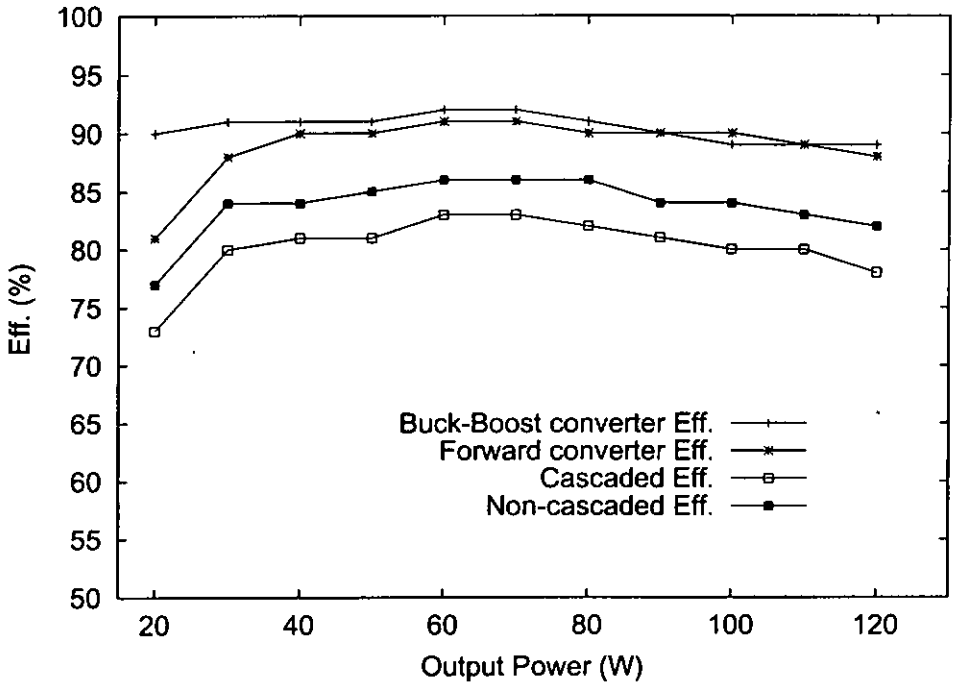
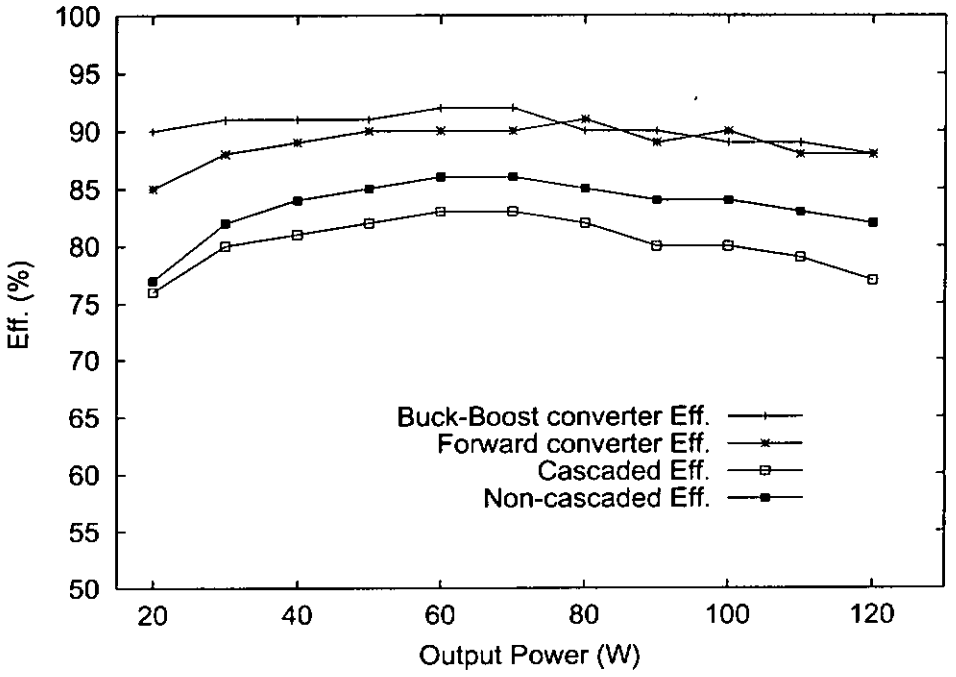


Figure 3.15: The new rearranged circuit efficiency curves for the buck-boost converter, the two-switch forward converter, and ISPFC at 160 V capacitor voltage.

can be easily understood because ISPFC is actually having more re-processing as V_L increase (k decrease). On the other hand, increasing in V_L leads to a reduction in the current total harmonic distortion of ISPFC and clearly this result agrees with the previous analysis.


100
95
90
85
80
75
70
65
60
55
50
Eff. (%)
20
40
60
80
100
120
Output Power (W)
Buck-Boost converter Eff.
Forward converter Eff.
Cascaded Eff.
Non-cascaded Eff.

(a) k=0.38


100
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80
75
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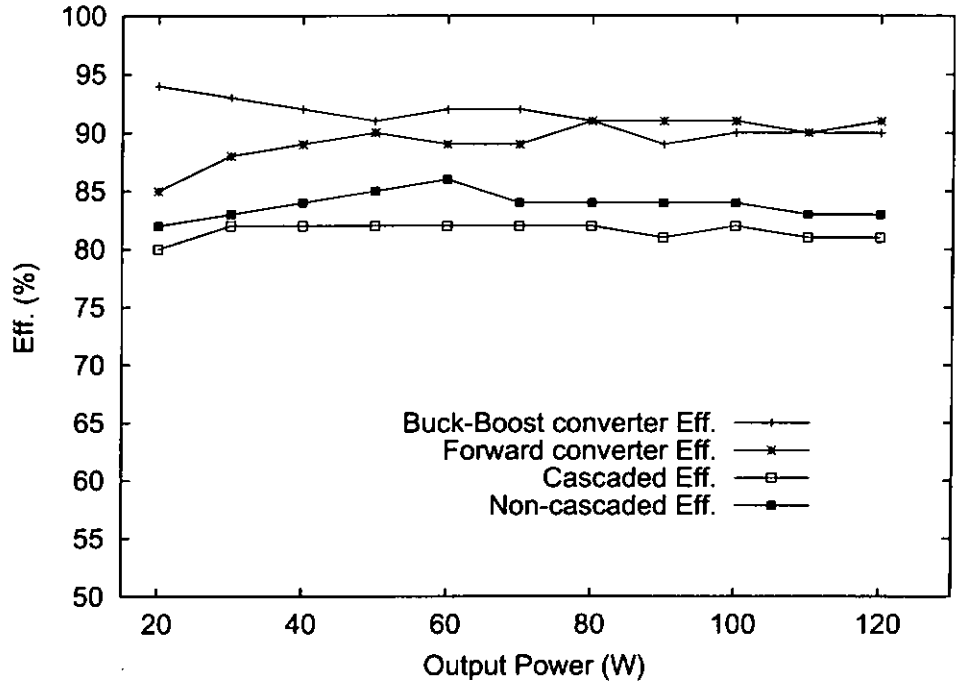
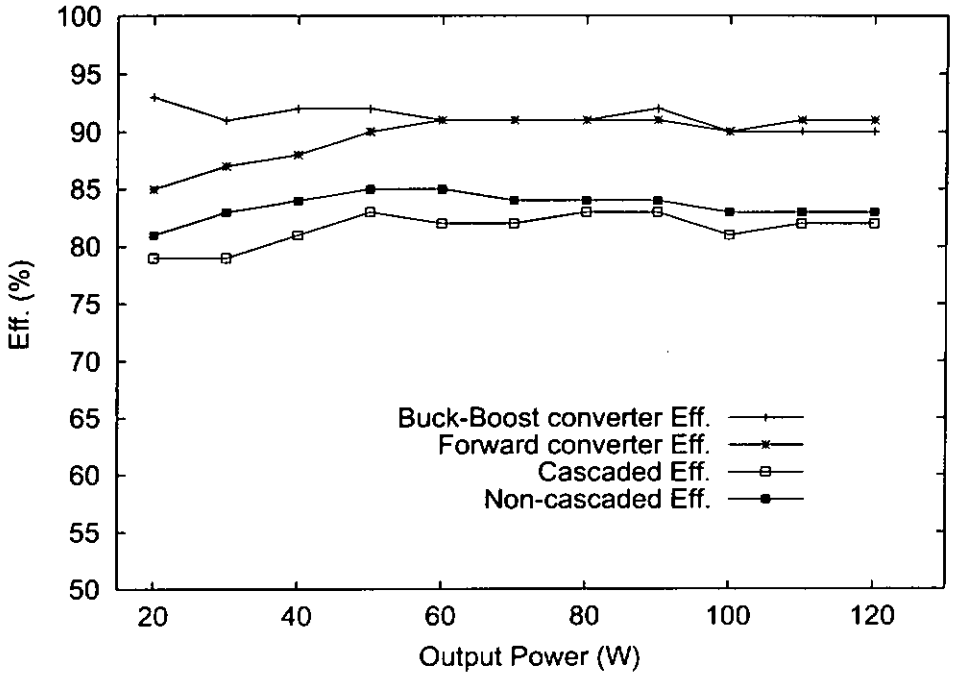
60
55
50
Eff. (%)
20
40
60
80
100
120
Output Power (W)
Buck-Boost converter Eff.
Forward converter Eff.
Cascaded Eff.
Non-cascaded Eff.

(b) k=0.37

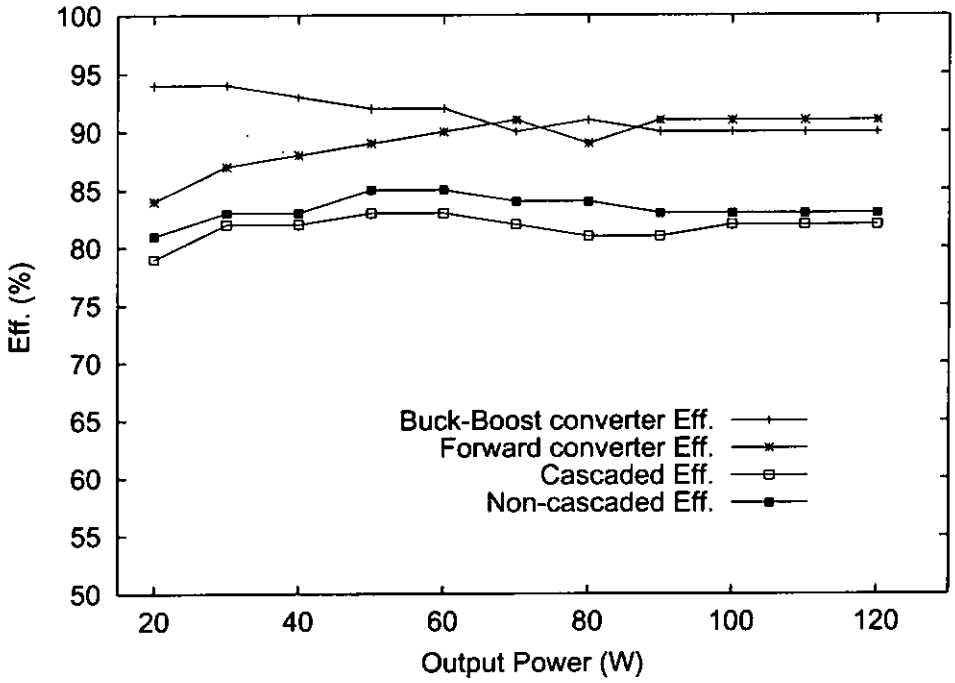


(c) k=0.35

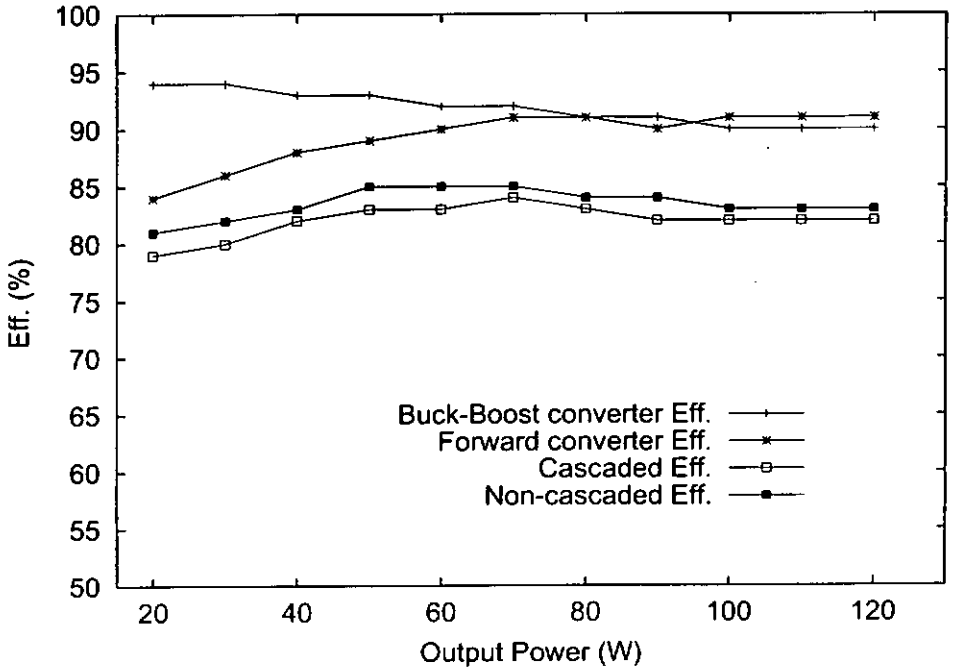


(d) k=0.34

Figure 3.16: Efficiency comparison of ISPFC, showing improved overall efficiency over a cascade structure for (a) V_L=160 V; (b) V_L=170 V; (c) V_L=180 V; (d) V_L=190 V.


100
95
90
85
80
75
70
65
60
55
50
Eff. (%)
20
40
60
80
100
120
Output Power (W)
Buck-Boost converter Eff.
Forward converter Eff.
Cascaded Eff.
Non-cascaded Eff.

(a) k=0.33


100
95
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50
Eff. (%)
20
40
60
80
100
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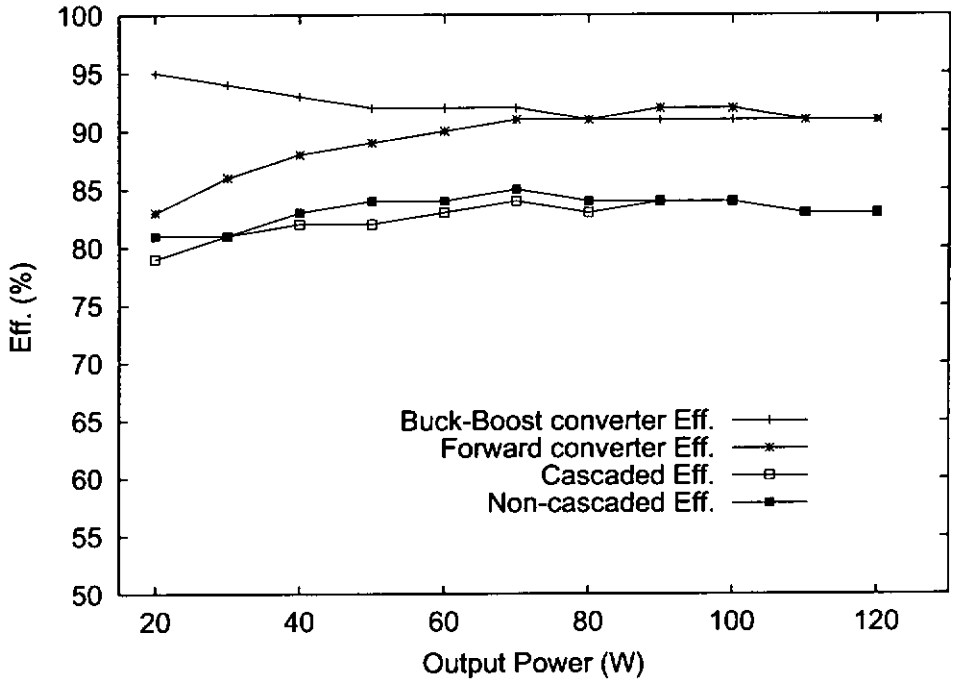
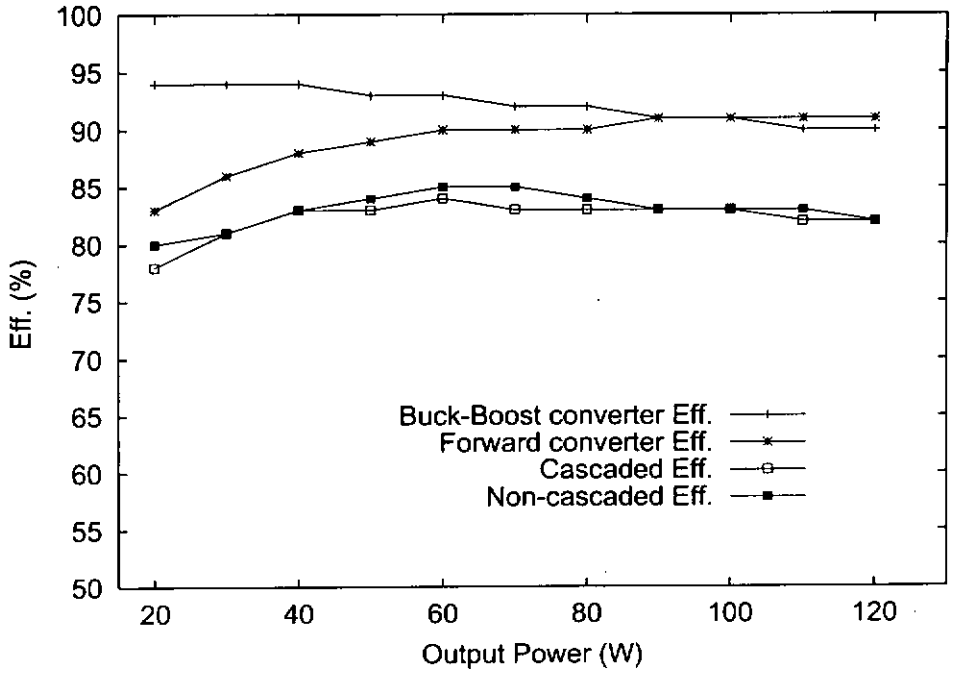
Output Power (W)
Buck-Boost converter Eff.
Forward converter Eff.
Cascaded Eff.
Non-cascaded Eff.

(b) k=0.32



(c) k=0.31



(d) k=0.30

Figure 3.17: Efficiency comparison of ISPFC, showing improved overall efficiency over a cascade structure for (a) V_L=200 V; (b) V_L=210 V; (c) V_L=220 V; (d) V_L=230 V.

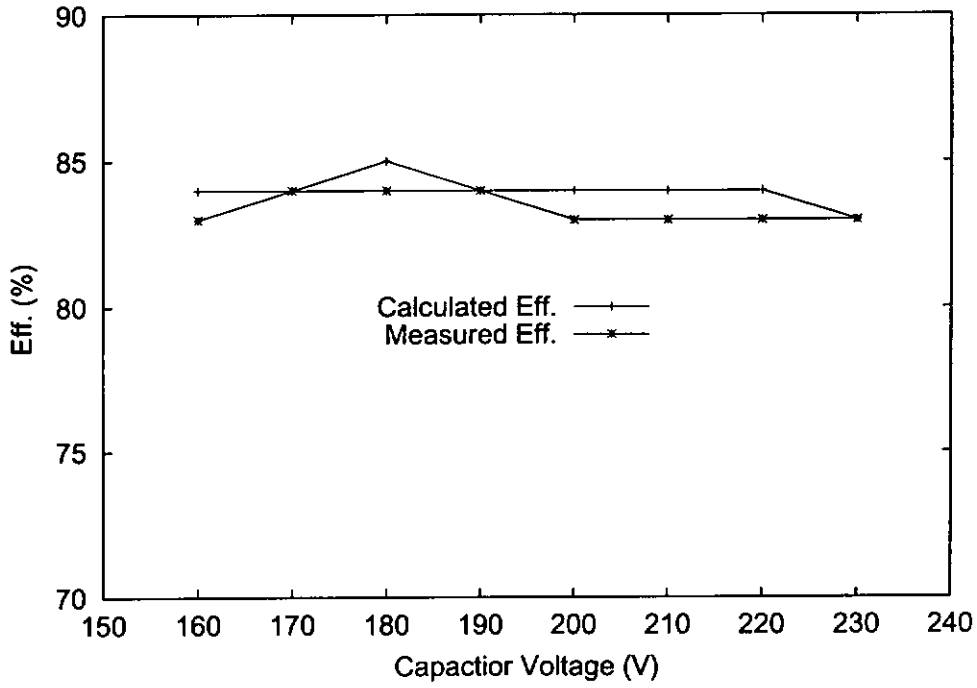


Figure 3.18: Efficiency versus V_L at 100 W of ISPFC, confirming the efficiency formula; calculated curve is based on efficiency formula and measured values of η_A and η_B; experimental curve is from direct measurement of the overall efficiency

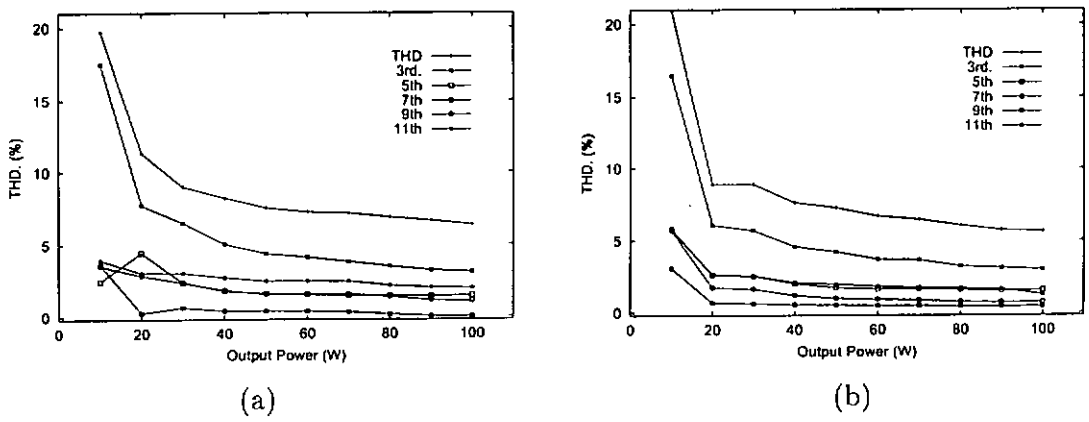
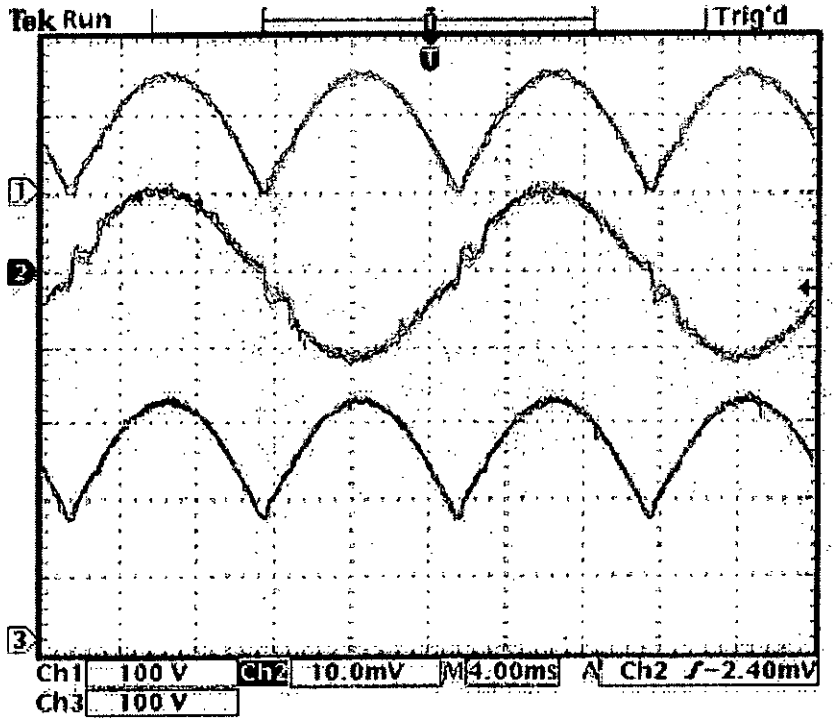
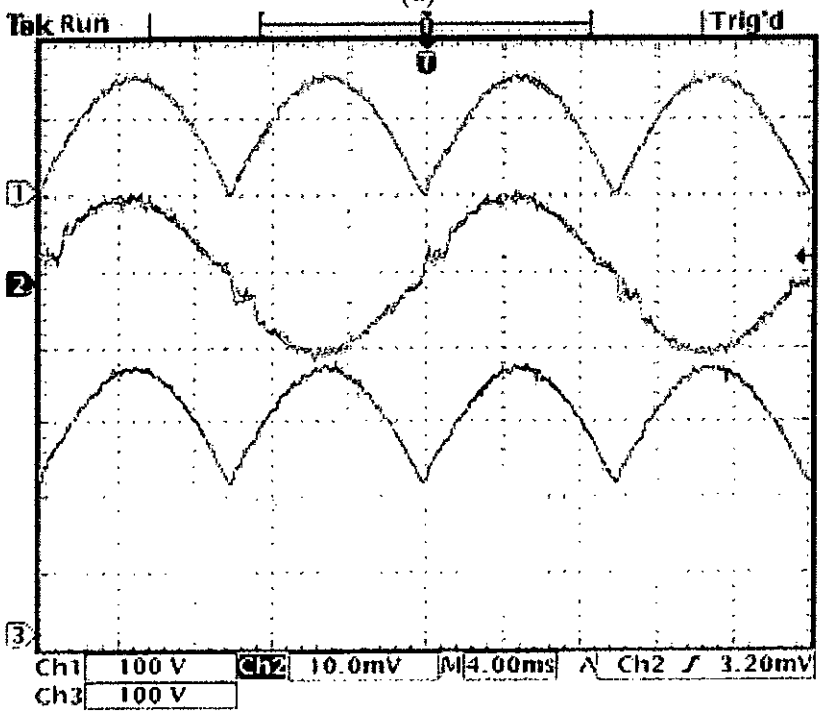


Figure 3.19: Measured current harmonic distortions versus output power. (a)V_L=160; (b)V_L=200.



(a)



(b)

Figure 3.20: Measured waveforms of input voltage (upper trace), input current (middle trace), input voltage of the two-switch forward converter (lower trace). (a) V_L=160 V; (b) V_L=200 V. Scale: 100 V/div, 1 A/div and 4 ms/div.

3.8 Summary

This chapter realizes a practical input-side non-cascaded power-factor-corrected switching regulator based on the power flow diagram. A detail analysis and clear design procedure for that particular switching regulator are reported. The essential element related to the control circuit for controlling ISPFC are also described. This information can be served as a reference of the switching regulator design engineers. By comparing the theoretical efficiencies and the practical results, the separated power process plays a crucial role in determining the overall efficiency of ISPFC. A particularly illuminating result, which turns out to be intuitive, is that the overall efficiency can be improved if the power processed by one converter is not re-processed totally by the other converter within ISPFC. This leads to the idea of reduced-redundant-power-processing power-factor-corrected switching regulator which has been the subject of this thesis. However, the switching regulator design engineers should make a trade-off between the efficiency and the current total harmonic distortions in ISPFC, which also is investigated by the analysis and verified by the experiment. It is hoped that this study will provide useful reference for engineers to practise and build their efficient PFC regulators.

Chapter 4

Output-Side Non-Cascaded PFC Switching Regulator

A 1-kW isolated non-cascaded boost buck-boost power-factor-corrected switching regulator based on reduced redundant power processing principle is elaborated in this chapter. In essence, boost converter is the most common converter for PFC in high power applications, however without isolation and high output voltage, boost converter output voltage must be higher than the input peak voltage and this is the major disadvantage of the boost converter. Noticeably the isolated boost converters merge boost converter and other simple converters, buck converter or buck-boost converter, sharing same switch to attain boost converter like function. An example found in Yang et al. [76] proposed a CCM isolated boost converter for front end power factor corrector to serve distributed power system. The isolated boost converter is merged by a boost converter and an half-bridge converter using same switches. This power factor corrector, can provide galvanic isolation and voltage stepped-down function, followed by a second switching regulation, e.g., a buck converter, which supplies regulated output voltage. The afore-described power-factor-corrected switching regulator is still connected in a low-efficiency approach–cascaded approach.

This chapter discusses a particular type of output-side non-cascaded power-factor-corrected switching regulator (OSPFC) that has been proposed by Garcia et al. [5] however their switching regulator employed a DCM flyback con-

verter for PFC and a DCM buck-boost converter for voltage regulation. Therefore the switching regulator is only suitable for low-power applications. The objective of this chapter is to develop an OSPFC, which not only provide high efficiency and power factor, and fast voltage regulation but also have potential for serving high power applications.

The original contributions of this chapter are, from switching regulator design engineers point of view, to illustrate and to verify experimentally that the OSPFC implemented on the chosen isolated boost converter for PFC can achieve a higher overall efficiency in comparison with the cascaded connection and it can also provide low harmonic input current characteristic and fast voltage regulation.

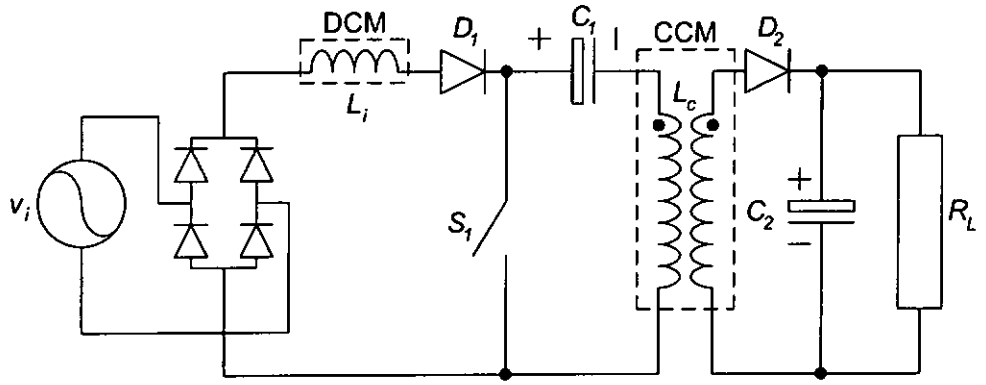


Figure 4.1: Boost converter integrated with flyback converter/Energy storage for PFC and voltage regulation

4.1 Operation Principle of OSPFCs

The BIFRED converter [48] is a boost converter merges flyback converter using the same active switch and it can also be regarded as an OSPFC. Because the input port energy passes through the pre-regulator and part of output energy of the pre-regulator directly go to output load. Figure 4.1 shows the BIFRED converter. L_i, D_1, and S_1 are components of the boost converter and the flyback converter is constructured by the coupled inductor, L_c, output diode, D_2, and the switch, S_1. It has the ability to provide PFC and voltage

regulation. The DCM boost converter is for simulating an input resistive characteristic, then the flyback converter can be operated in CCM and provides fast output voltage regulation. The low frequency storage element role should be played by the capacitor, C_1, between the boost converter and the flyback converter. The output port of the boost converter is connected with C_1 and L_c, since the output power can transfer to the output load, R_L, directly, when S_1 is turned-off. The operation of the BIFRED can be divided by three intervals. During the first interval S_1 and D_1 conduct and D_2 is reverse bias. In that interval, input and storage element energy transfer to L_i and L_c, respectively. During the second interval S_1 is turned-off, the energy stored in L_i releases to C_1 and L_c. Since D_2 is conducting, then the input inductor and coupled inductor currents transfer energy to the load via D_2. Because the input inductor is operated in DCM, the third interval is that the input inductor releases all stored energy and the current of the input inductor is maintained at a zero level. So D_2 current is only equal to the coupled inductor current in that interval.

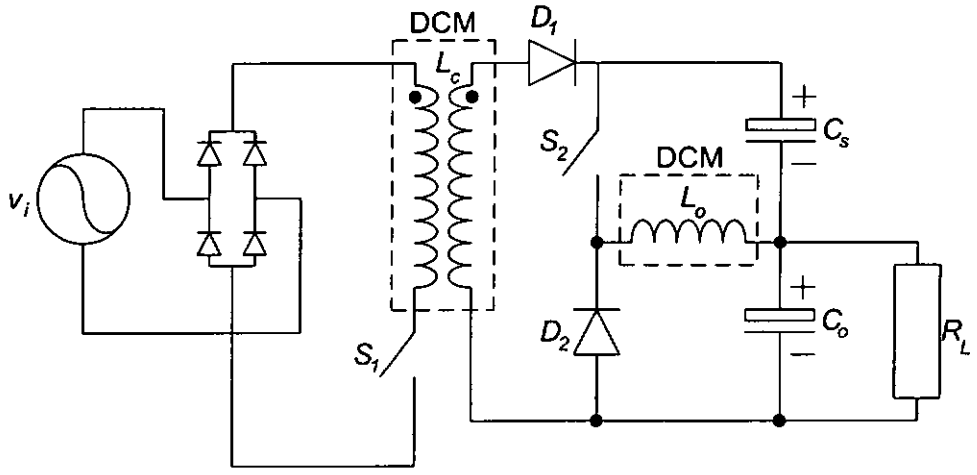


Figure 4.2: Two operated DCM buck-boost converter connected with non-cascaded configuration to make an OSPFC.

The afore-mentioned single-switch OSPFC is quite difficult to control because control of the single switch has to satisfy to two requirements that are PFC and voltage regulation. Garcia et al. [5] propose a family of topologies for two-switch OSPFC, which employs a power factor corrector switch and a

voltage regulator switch. These switches are controlled by independent control circuits according to difference parameters such as storage element voltage level, output voltage, and input current. Figure 4.2 shows one of Garcia proposed OSPFC circuits, which is built by a DCM flyback converter for automatic PFC and that converter is also followed by a DCM buck-boost converter for voltage regulation.

4.2 Specifications of the Proposed OSPFC

Afore-described OSPFCs are unsuitable high power applications, because those OSPFCs contain a pre-regulator operated in DCM. This operation leads to a high current rating on the active switches of the pre-regulators and the rating is usually higher than the double of the input average current. In the below described OSPFC, the switching regulator can provide 1-kW output power at an output voltage equal to 48 V, therefore all the converters of the switching regulator must be operated in CCM such that the switches and diodes of the converters can enjoy reasonable voltage and current ratings. The input voltage is 200 V R.M.S. The low frequency storage element voltage level should be lower than the peak value of the input voltage. The switching frequency of two converters are 50 kHz and the converters are operated at hard-switching. Power factor and input current harmonic distortion of this switching regulator should meet international standard, IEC 61000-3-2 [3]. The proposed OSPFC is built by an isolated-boost type converter and a buck-boost converter.

4.3 Circuit Overview

Figure 4.3 shows the equivalent circuit of the proposed OSPFC. From the equivalent circuit, at the converter B the negative input terminal, X^-, and the negative output terminal, Y^-, there must be without connecting path all the times. Because if these two terminals have a short circuit path, it means that the output terminal of the proposed OSPFC is shorted by that circuit path. If all the converters of the proposed OSPFC are isolated-type converters, this

Table 4.1: Specifications of the proposed OSPFC

Specification	Value
Output power range	200 W-1 kW
Input voltage	200 RMS
Output voltage	48 V DC
Storage element capacitor voltage	$\leq$ 150 V
Switching frequency	50 kHz
Pre-regulator	Isolated-boost type converter
Voltage regulator	Buck-boost converter

short-circuit path problem can be avoided. However, from the switching regulator design engineers point of view, isolated-type converters provide some practical problems such as core reset path, leakage inductance, increase in size and cost of the switching regulators. A converter placed at the proposed OSPFC converter B should have the ability to make a short circuit path between negative input terminal, X^-, and positive output terminal, Y^+, i.e., a buck-boost converter or Ćuk converter. From Figure 4.3, isolation transformer should be inserted to the converter A, and converter A could be any simple converter.

4.4 Connection of Proposed OSPFC

The block diagram of the proposed OSPFC, consisting a non-cascaded connection of an isolated-boost type converter and a buck-boost converter, is shown in Figure 4.4. Based on the principle of power balance, a low-frequency storage element is required to buffer the difference between the instantaneous input power and output power in the switching regulator with PFC and voltage regulation. Capacitor, C_L, serves as the storage element and is connected in series with the output capacitor, C_o. The series combination forms the loading for the isolated-boost type converter. Therefore a portion of the output energy from the isolated-boost type converter is transferred directly to the output because C_o is in parallel with the output load. The voltage of C_o should

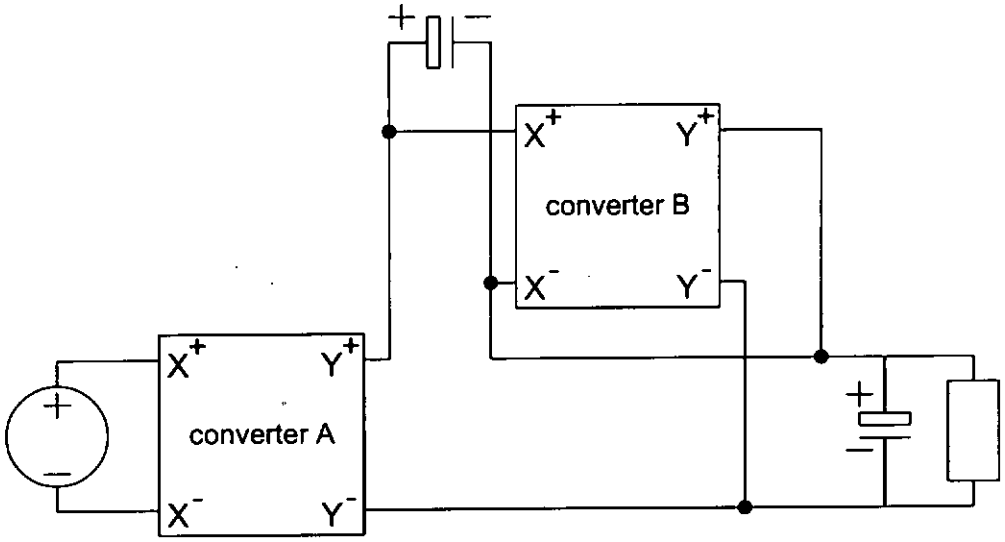


Figure 4.3: Equivalent circuit of the proposed OSPFC. Rectangular blocks denote converters.

be free of low-frequency voltage ripple because it is the actual output of the whole OSPFC. On the other hand, C_L has a low-frequency ripple voltage which is generated from the difference between the instantaneous input power and output power. The buck-boost converter takes energy from C_L and delivers the energy to the load.

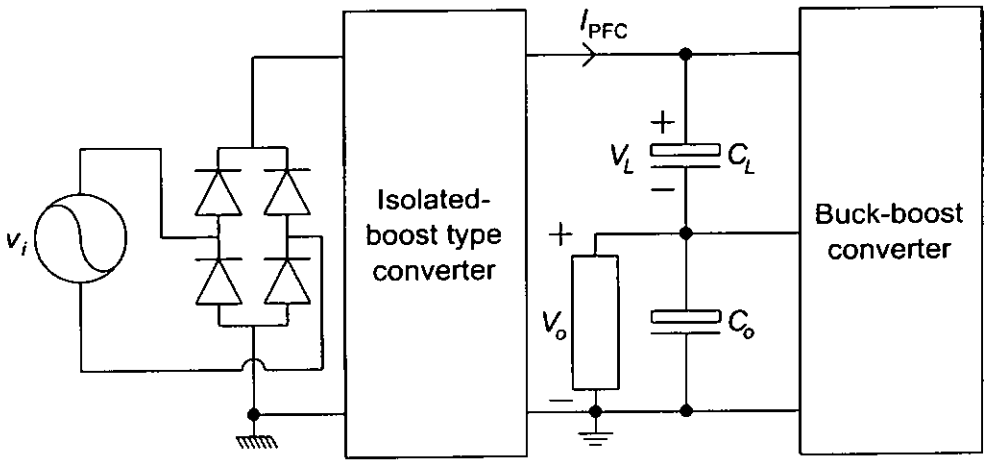


Figure 4.4: Proposed OSPFC with storage element connection block diagram

4.5 Maximum Efficiency Gain

The overall efficiency of the proposed OSPFC can be estimated by using Equation 2.27. Suppose again that the square box A and the square box B, which are shown in Figure 2.20, denote the isolated-boost type converter and buck-boost converter, respectively. Then the efficiency can be divided by

$$\eta_{\text{OSPFC}} = \eta_{\text{A}}\eta_{\text{B}} + k\eta_{\text{A}}(1 - \eta_{\text{B}}) \tag{4.1}$$

where k is the ratio at which the amount of the output power of isolated-boost type converter is split to reach the output load. The efficiency gain of the proposed OSPFC is $k\eta_{\text{A}}(1 - \eta_{\text{B}})$.

From the above discussion, the factor k affects the efficiency gain of the proposed OSPFC. It is more convenient to determine the factor k in terms of the circuit parameters of the proposed OSPFC. Based on Figure 4.4,

$$P_{\text{PFC}} = I_{\text{PFC}}(V_{\text{L}} + V_{\text{o}}) \tag{4.2}$$

$$P_{\text{direct}} = I_{\text{PFC}}V_{\text{o}} \tag{4.3}$$

From Equations 4.2 and 4.3, the factor can be interpreted by

$$P_{\text{direct}} = \frac{V_{\text{o}}}{V_{\text{L}} + V_{\text{o}}}P_{\text{PFC}} \tag{4.4}$$

where P_{PFC} and I_{PFC} are the output power and the output current of the isolated-boost type converter and P_{direct} denotes the amount of the output power of the isolated-boost type converter directly transferred to the output load. Therefore, the factor k can be determined in circuit parameters by

$$k = \frac{V_{\text{o}}}{V_{\text{L}} + V_{\text{o}}} \tag{4.5}$$

To increase the overall efficiency of the proposed OSPFC, it is clear that the factor k should be made as large as possible. On the other hand, the factor k should be kept small enough such that the buck-boost converter can provide a low-frequency ripple free output voltage while the isolated-boost type converter maintains a prefect PFC operation, i.e., the input current is proportional with input voltage, pure sinusoidal current.

With the afore-mentioned considerations, the theoretical maximum value of the factor k can be evaluated as follows. Consider the power flow waveforms

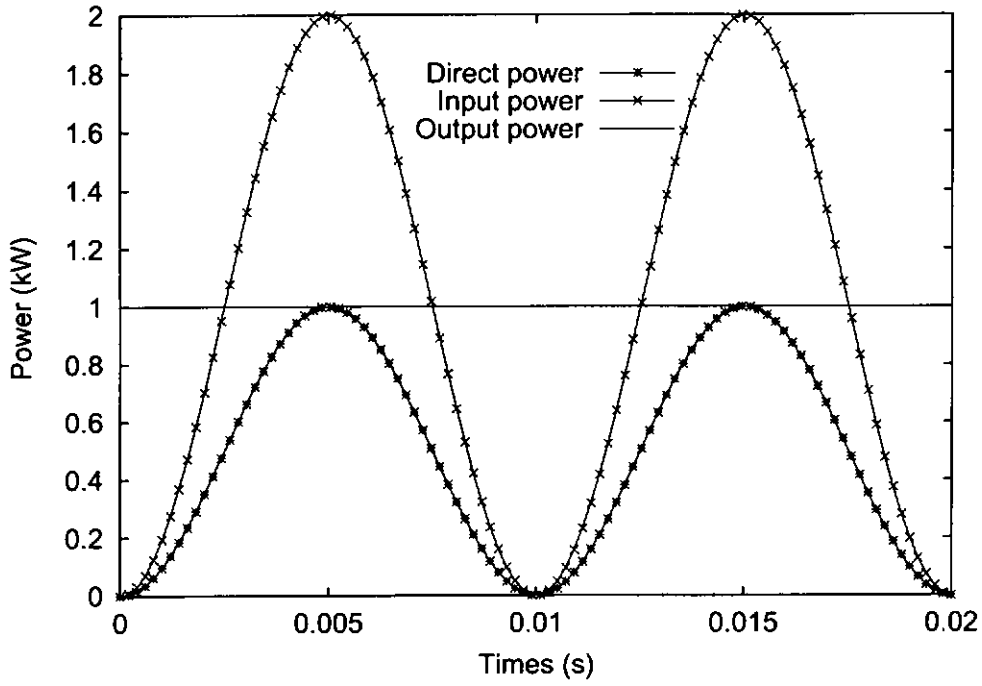


Figure 4.5: Ideal power waveforms of the proposed OSPFC

of the proposed OSPFC as shown in Figure 4.5. For a constant-power load condition, the output power is denoted by power waveform (Output power). In order to provide this output power, the input power waveform of the isolated-boost type converter, must be a pure shifted sinusoid with an average value of the waveform (Input power) if the isolated-boost type converter can provide perfect PFC operation and has an efficiency of unity. Note that the frequency of the shifted sinusoid is twice of that of the AC mains line frequency. The amount of power that is transferred directly from the isolated-boost type converter to output is denoted as the direct power waveform which has a waveform similar to the input power waveform. For maintaining a low-frequency ripple free output voltage, the peak value of the direct power must be less than the output power at all time. Since the direct power waveform has a sinusoidal waveform, this condition can be easily fulfilled if

$$P_{\text{direct}_{\text{peak}}} \leq P_{\text{out}} \tag{4.6}$$

The maximum value of P_{direct} can be related with P_{PFC} because P_{PFC} has an

average value of P_{out}. Therefore,

$$P_{\text{direct}_{max}} = \frac{1}{2} P_{PFC} \tag{4.7}$$

In other words, the maximum value of the factor k is equal to $\frac{1}{2}$, hence

$$\frac{1}{2} = \frac{V_o}{V_o + V_L} \tag{4.8}$$

Equation 4.8 shows that when V_L is equal to V_o, the proposed OSPFC can achieve its maximum efficiency.

4.6 Value of the Storage Element

In the case of the typical cascaded power-factor-corrected switching regulators, for maintaining the unity-power-factor operation, the minimum requirement of the capacitance are shown in Equation 2.24. Because the switching regulators allow that the variation of capacitor voltage is equal to the twice of the static voltage of the capacitor voltage, i.e., $|\Delta v_{C_s}|$ =2 V_{C_s}. However the proposed OSPFC, for maintaining the unity-power-factor operation, the minimum capacitance can be obtained if the output voltage of the isolated-boost type converter is allowed to vary from V_o to its peak value during each half of the AC mains periods because the output voltage of the isolated-boost type converter of the proposed OSPFC must contain a DC voltage which is larger or equal to output voltage. Figure 4.6 illustrates the condition of the maximum storage element capacitor voltage variation of the proposed OSPFC. The maximum ripple voltage of the output voltage of the isolated-boost type converter is equal to $2V_L$. Using Equation 2.22, the required minimum capacitance for energy storage is

$$C_{L_{min}} = \frac{P_o}{2\omega V_L (V_L + V_o)} \tag{4.9}$$

In general, the capacitance of the proposed OSPFC requires a larger value than that of the typical cascaded switching regulators because the allowable voltage ripple Δv_{C_s} is usually kept at a smaller value otherwise a large variation in the duty cycle of the buck-boost converter is required. However capacitor C_L of the proposed OSPFC clearly enjoys a lower voltage stress when compared with that of the typical cascaded power supplies as shown in Figure 2.5.

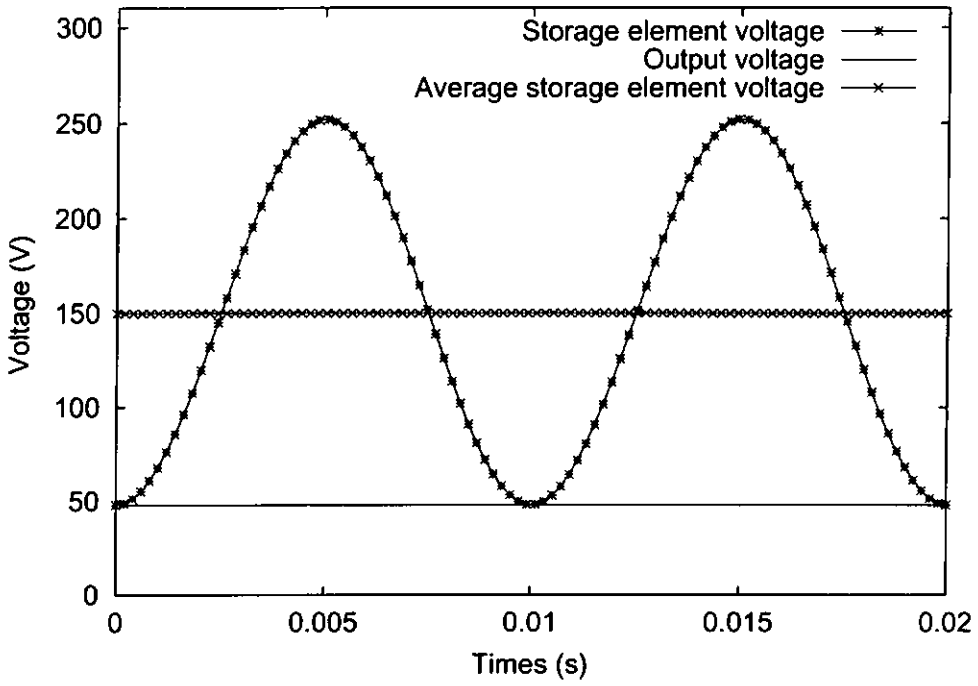


Figure 4.6: The proposed OSPFC of maximum voltage variation of the capacitor storage element waveforms

4.7 Pre-Regulator: Isolated-Boost Full-Bridge Converter

Isolated-boost type converters used for PFC in high power applications were reported recently in [45], [76]–[80]. Basically the isolated-boost type converter can be divided by two difference types, half-bridge converter or full-bridge converter follows a boost converter. The isolated-boost type converters share the common advantages with boost type converters for PFC pre-regulator, i.e., its input current is equal to inductor current that must be continuous current waveform and controlled by the active switches for achieving the required PFC action. Furthermore, the isolated-type converters can also offer a number of additional merits, for example, the size and the cost of the input boost inductor can be reduced due to its frequency-doubling effect; its transformer provides galvanic isolation and stepped down output voltage for reducing the voltage rating of the storage element capacitor. In terms of transformer core utilization, the isolated-boost type converters clearly provides

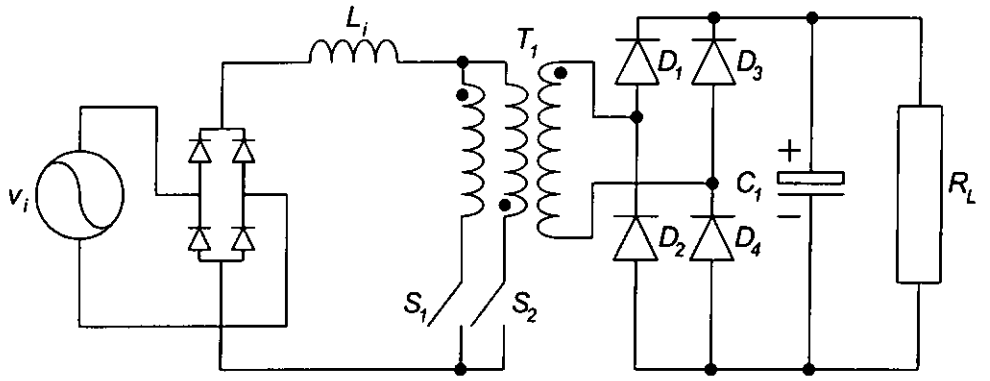


Figure 4.7: A typical isolated-boost half-bridge converter

better performance than that of flyback and forward converters. However two different type converters, full-bridge and half-bridge, also have their advantages and drawbacks. Figure 4.7 shows an isolated-boost half-bridge converter. Voltage stress of the switches of isolated-boost half-bridge converters is twice the reflected output voltage. From Yang et al. [76], the authors replaced the MOSFETs with IGBTs for withstanding 1-kV voltage stress and used an extra MOSFET for soft-switching to assist the IGBTs operation normally.

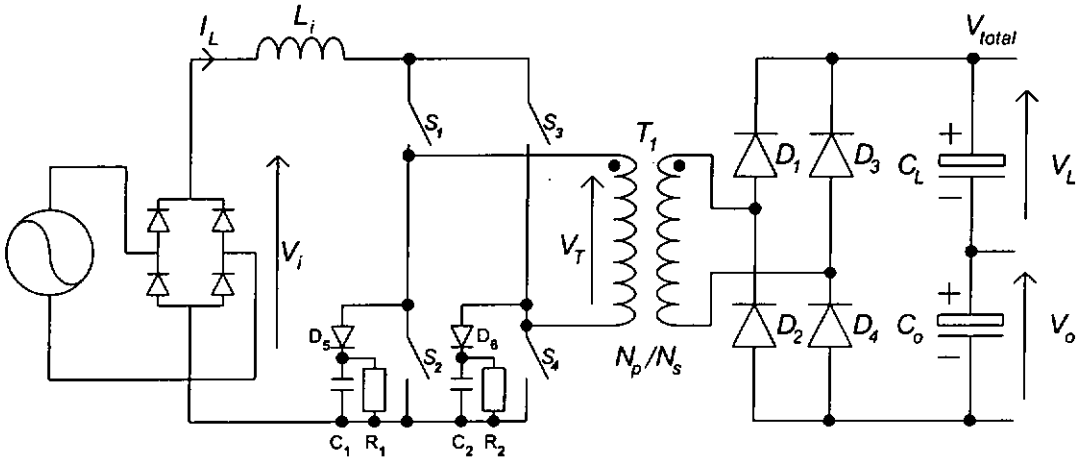


Figure 4.8: The isolated-boost full-bridge converter for the proposed OSPFC pre-regulator

The simplified circuit of the four-switch IBFB converter is shown in Figure 4.8 for the proposed OSPFC pre-regulator. The set of waveforms that relates

the ideal gate timing with the corresponding inductor current and transformer voltage is shown in Figure 4.9. It is easy to see that the operation of this converter resembles that of a typical boost converter. The duty ratio of the four active switches is fixed at 50%, by which the upper switches (S_1, S_3) and the lower switches (S_2, S_4) are clocked alternately, resulting in a simpler control circuitry compared with those reported in [77] and [78].

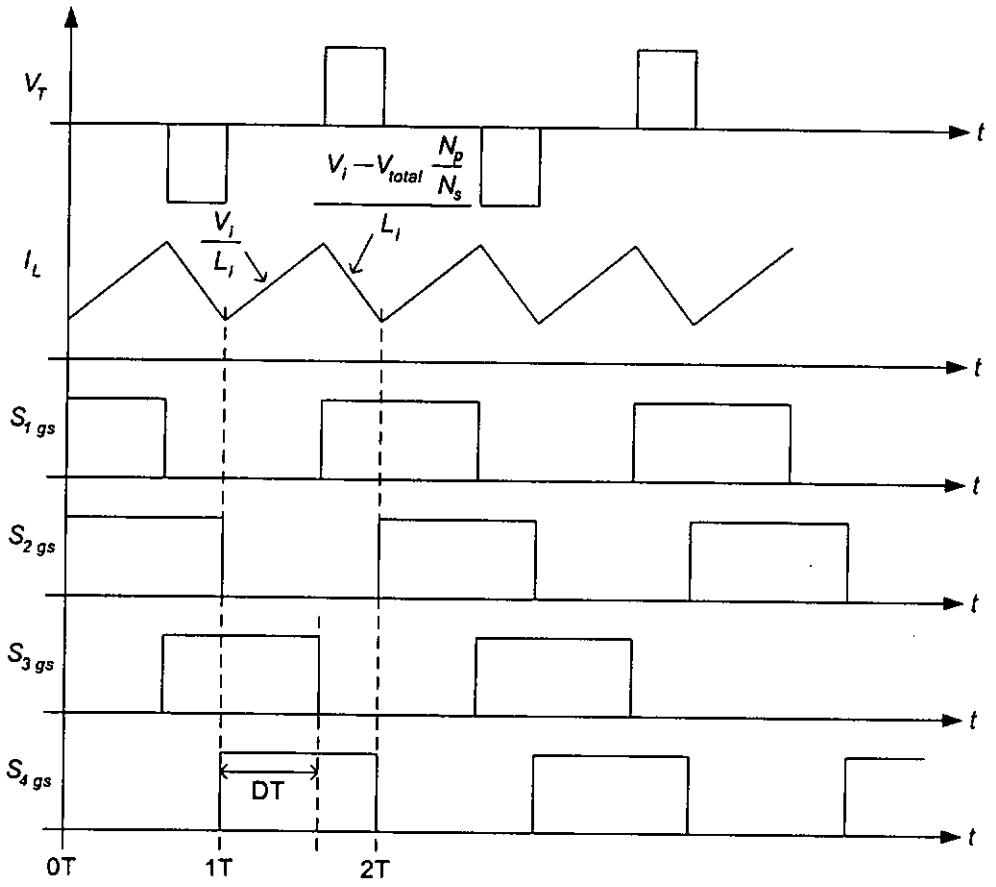


Figure 4.9: The ideal gate timing diagrams for the IBFB converter with the corresponding waveforms of the input inductor current and transformer voltage

Energizing intervals of L_i occur at the time when both S_1 and S_2, or S_3 and S_4 are turned on. De-energizing intervals of L_i occur at the time when both S_1 and S_3, or S_2 and S_4 turned on. The input energy is stored in L_i in the energizing intervals, and released through the transformer T_1 in the

de-energizing intervals. The conversion ratio of the IBFB converter can be easily derived for the IBFB converter by applying the principle of volt-second balance to the inductor current waveform, where

$$\frac{V_{\mathrm{i}}}{L_{\mathrm{i}}}DT = -(\frac{V_{\mathrm{i}} - V_{\mathrm{total}}\frac{N_{\mathrm{p}}}{N_{\mathrm{s}}}}{L_{\mathrm{i}}})(1-D)T \tag{4.10}$$

Thus, the conversion ratio equation can be simplified by

$$\frac{V_{\mathrm{total}}}{V_{\mathrm{i}}} = \frac{N_{\mathrm{s}}}{N_{\mathrm{p}}}\frac{1}{(1-D)} \tag{4.11}$$

which is similar to that of a typical boost converter conversion ratio with an additional factor of $\frac{N_{\mathrm{s}}}{N_{\mathrm{p}}}$ due to the transformer turns ratio.

In the circuit shown in Figure 4.8, two additional snubber circuits are added in the pre-regulator for compressing voltage spikes, which is generated by power transformer leakage inductance. Because the pre-regulator is employed an isolated-boost full-bridge converter, each switch of the pre-regulator has to tolerate the reflected voltage only. Table 4.2 shows the proposed OSPFC pre-regulator components and their value.

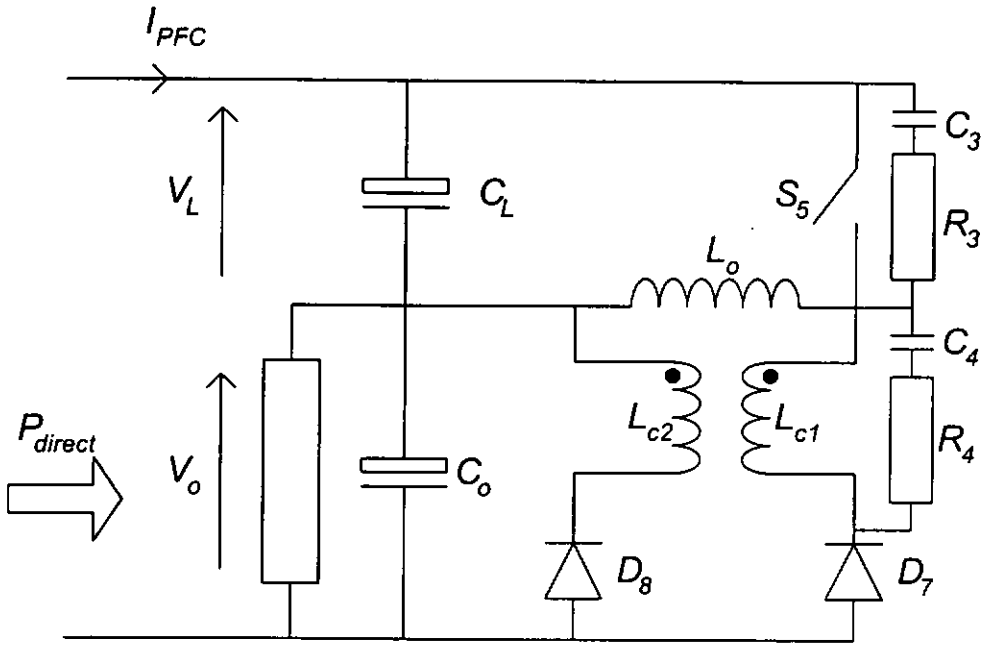


Figure 4.10: The buck-boost converter with low-loss turn-on snubber

Table 4.2: Components and their value/types for the proposed OSPFC pre-regulator

Parameters	Components / Value
L_i	560 μH
L_i core	Coilcraft: PVC-2-564-08
Bridge rectifier (BR)	20ETF10 × 4
Power switches (S_1-S_4)	APT 6025BVR
Output rectifier (D_1-D_4)	DESP 30-03A
Storage element	1200 μF × 4, V_{max}=250
Power transformer core	ETD 59 (3F3)
Primary wire	8 AWG 24 lace up
	No. of turns=50
Secondary wire	24 AWG 24 lace up
	No. of turns=18
Magnetizing inductance	13mH
Snubber resistor ($R_1 - R_2$)	100 Ω, 10 W
Snubber diode ($D_5 - D_6$)	MUR460
Snubber capacitor ($C_1 - C_2$)	2.2 nF, 1 kV

4.8 Voltage Regulator: Buck-Boost Converter

Based on the description in Section 4.5, the output voltage regulator processes only part of the total output power, therefore its power rating is less than 1 kW. A buck-boost converter is chosen as a voltage regulator of the proposed OSPFC power supply because the negative of its input terminal must be connected to the positive of its terminal according to Figure 4.4. In Section 4.3 a detail discussion is provided for that particular OSPFC arrangements.

The input voltage source of the buck-boost converter is the energy storage element, therefore the input voltage source of the buck-boost converter contains a DC voltage level superimposed with a low frequency ripple voltage. Since the low frequency ripple voltage level relates to the output power of OSPFC, as shown in Equation 2.22, the duty cycle variation of the buck-boost converter depends on the output power level of OSPFC.

The buck-boost converter with low-loss turn-on snubber is shown in Figure 4.10. The basic components of the buck-boost converter are S_5, D_7 and L_o. A simple RC snubber circuit consisting of (C_3, R_3) is used to compress the voltage spikes on S_5 when it is off. The power diode, D_5, with a slow reveres recovery time could impose a heavy loss on the converter at the moment when S_5 is being turned on. This problem is solved by employing the low-loss turn-on snubber [81] which consists of couple inductors (L_{c1}, L_{c2}) and an ultra fast diode, D_8. High frequency current spikes occur when the active switch is turned-on. At this moment current spikes energy is transferred from L_{c1} to L_{c2}. The current spikes energy can transfer to output load through the coupled inductors and is filtered by the output capacitor. D_8 controls the current flow direction of L_{c2}. C_4 and R_4 are used to compress the ringing voltage generated by the couple inductors.

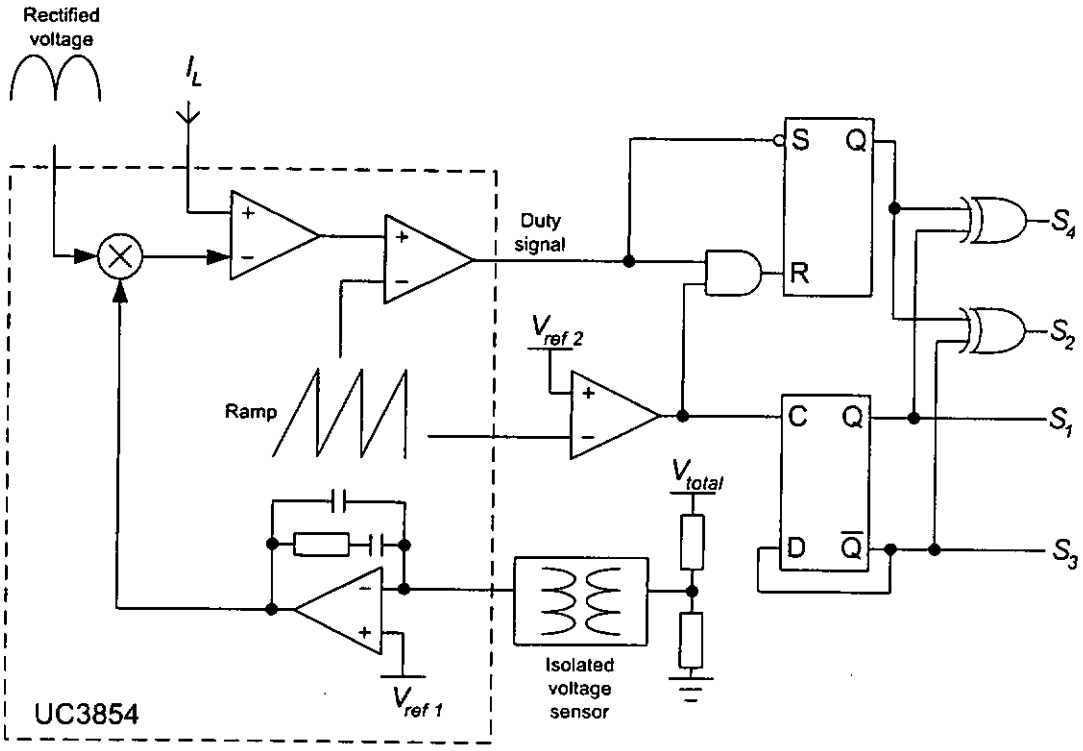


Figure 4.11: The simplified schematic circuit of the PFC controller.

4.9 Implementation

The average current mode control based on Unitrode PFC controller UC3854 is employed in the IBFB converter. There are four switches which are required to be controlled for realizing the PFC function, therefore additional logical circuits are required to generate required gating pulses according to Figure 4.9. The simplified schematic diagram of the PFC controller with the additional logic circuit is shown in Figure 4.11.

According to Figure 4.9, the duty ratio of all switches is 50% as S_1 and S_3, and S_2 and S_4 are anti-phase. The phase difference between S_3 and S_4 really controls the duty cycle of the IBFB converter. The functions of the additional logic circuits are to generate a phase difference between the S_3 and S_4 according to the duty signal of UC3854 and to provide 50% gate signals for all the active switches. The clock signal of UC3854 is not externally accessible, therefore it is extracted by means of a comparator connecting to the sawtooth signal generated by UC3854. The extracted clock signal is synchronized with the duty signal and used to trigger a D-type flip-flop for generating 50% gate signals for S_1 and S_3. Note that the gate signal are anti-phase with each other. According to the duty signal of UC3854 and gate signals of S_1 and S_3, gate signals of S_2 and S_4 are created by an R-S flipflop and two exclusive OR gates with a proper phase difference between S_3 and S_4.

Peak current mode control based on UC3843 is employed in the buck-boost converter. Because 40% of the output power goes to the load directly through the PFC stage, the maximum processing power of the buck-boost converter becomes 600 W for a total output power of 1 kW. Clearly the size and the component ratings of the voltage regulator in the proposed OSPFC are smaller and lower in comparison with its cascaded counterpart. Table 4.3 shows the components detail of the buck-boost converter.

4.10 Experimental Results

The proposed OSPFC is tested at a power level of 1 kW and with an input voltage of 200 V RMS. The input current waveform of the proposed OSPFC is shown in the Figure 4.16. The measured power factor is 0.995 and

Table 4.3: Components and their value/types for the proposed OSPFC voltage regulator

Parameters	Components/Values
L_o	130 μH
L_{c1}	7 μH
L_{c2}	7 μH
D_6, D_7	DESP 30-03A
S_5	IXFK 48N50
C_o	1200 μF $\times$ 3 63 V
C_3, C_4	1 nF 1 kV
R_3	35 Ω 2 W
R_4	100 Ω 2 W
L_o transformer core	ETD 59 (3F3)
L_o winding	Copper foil 25 turns with air gap
L_{c1}, L_{c2} transformer core	ETD 49 (3C90)
L_{c1}, L_{c2} winding	Copper foil 10 turns with air gap

the overall efficiency is 86%, which are shown in Figure 4.12 with the output power level from 250 W to 1 kW. The IBFB converter output voltage is 150 V and the buck-boost converter regulated output voltage is 48 V. The objective of this measurement is to verify the validity of the principle of reduced redundant power processing, therefore the measurement is specifically measured the efficiencies of the two constituent converters and compare their product with the measured overall efficiency, under the same efficiency gain ($k = \frac{48}{102+48}$) for an output power level from 250 W to 600 W. The results are plotted as a set of efficiency curves which are shown in Figure 4.13 and the measurements are performed at V_L of 150 V and V_o of 48 V, i.e., k=0.32. Figure 4.14 shows a comparison of the measured and calculated efficiencies and confirms the validity of the efficiency formulae 4.1 and 4.5. Finally, for showing the PFC performance, the harmonic distortions of the input current are measured for different power levels at the same factor k as shown in Figure 4.15. The photos of the experimental converters and the PFC controller are shown in Figures 4.17 and 4.18, and Figure 4.19 respectively.

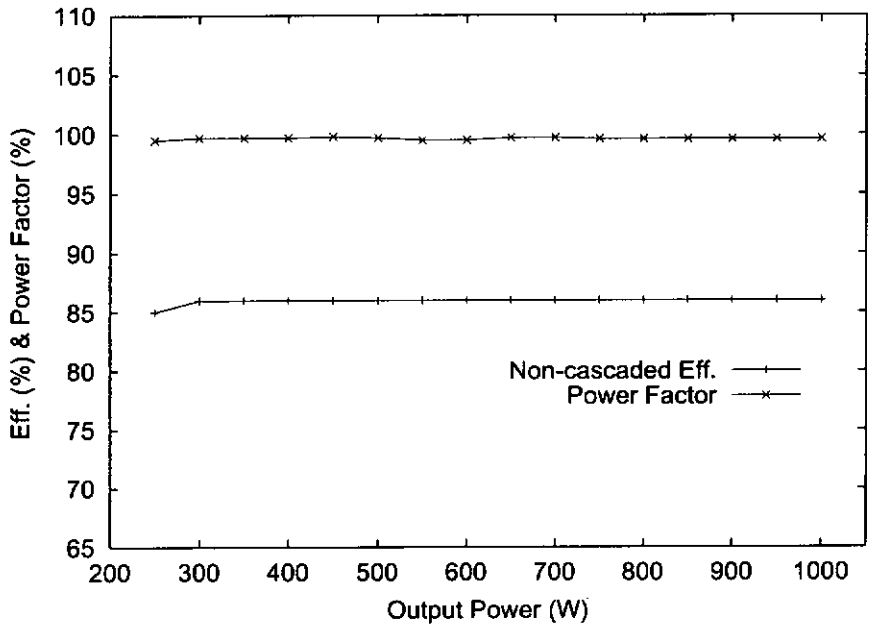


Figure 4.12: The measured overall efficiency and power factor for output power level from 250 W to 1 kW.

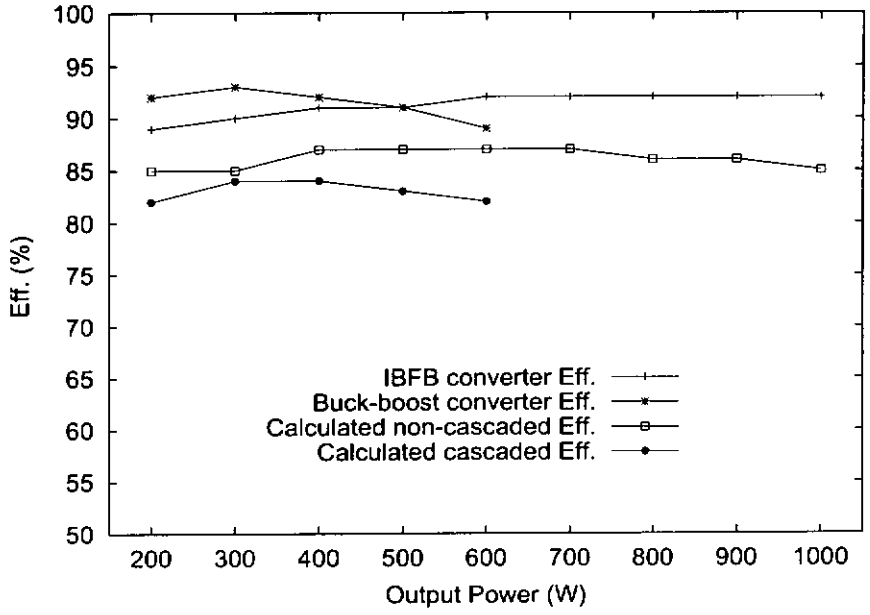


Figure 4.13: Efficiency comparison of the proposed OSPFC showing improved overall efficiency over a cascaded structure for k=0.32

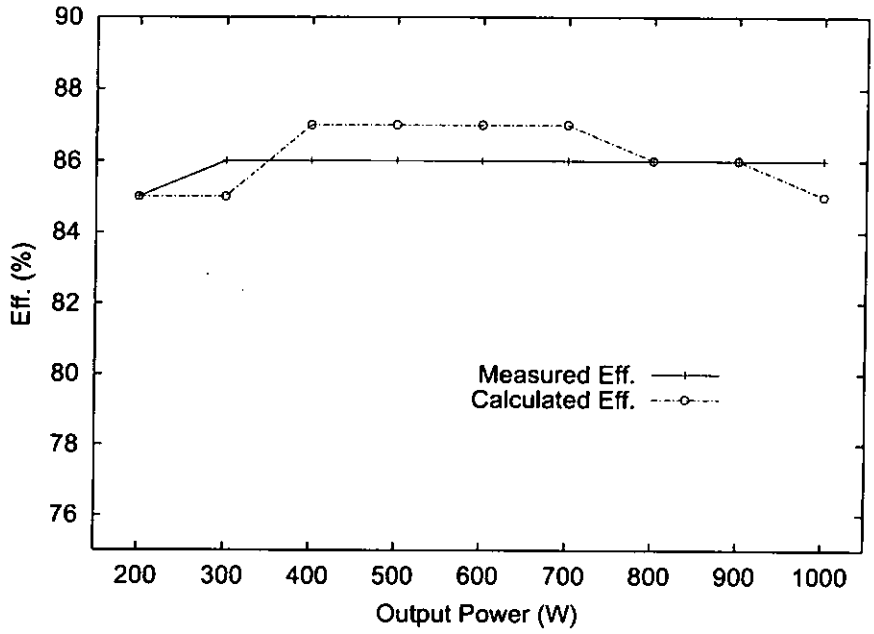


Figure 4.14: Confirming the efficiency formulae; calculated curve is based on the efficiency formula and measured efficiencies of the IBFB converter and buck-boost converter at k=0.32; experimental curve is from direct measurement of the overall efficiency.

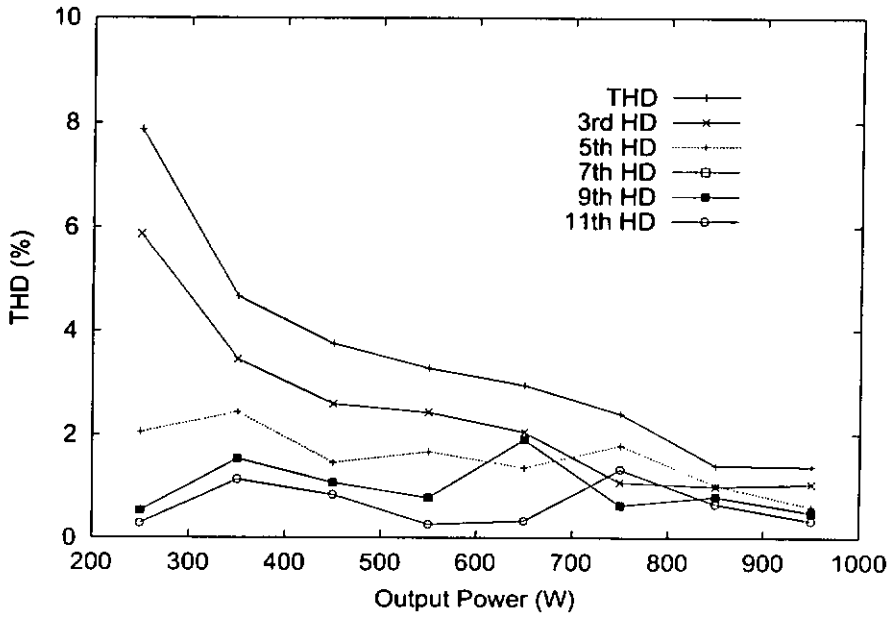


Figure 4.15: Measured harmonic distortions versus output power at k=0.32

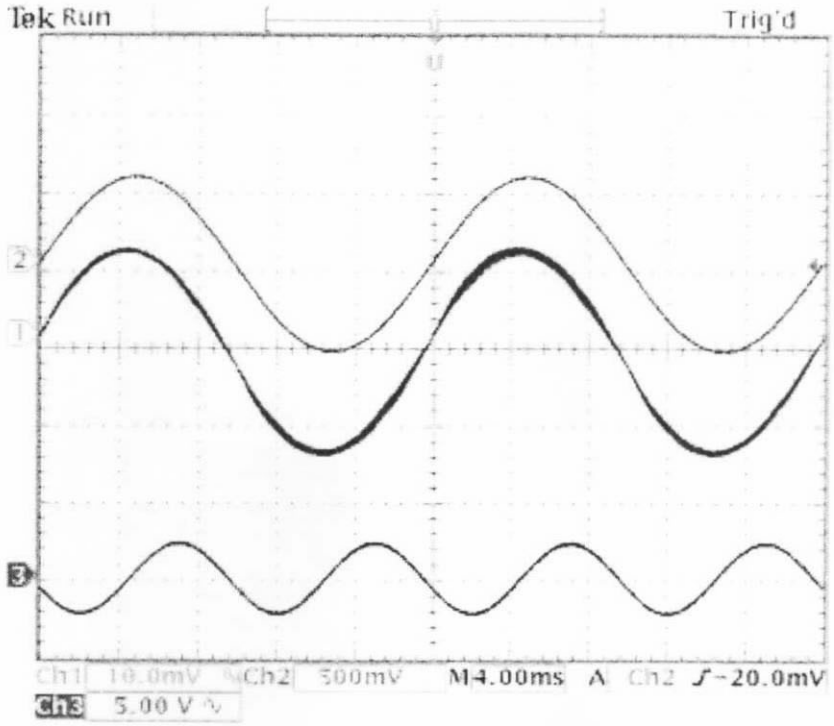


Figure 4.16: Measured waveforms of input current (Channel 1), input voltage (Channel 2), output ripple voltage (Channel 3) of the IBFB converter. Input voltage is 200 V RMS with an output power of 1 kW. Scale: Channel 1 5 A/div, Channel 2 250 V/div, Channel 3 5 V/div and time base 4 ms/div.

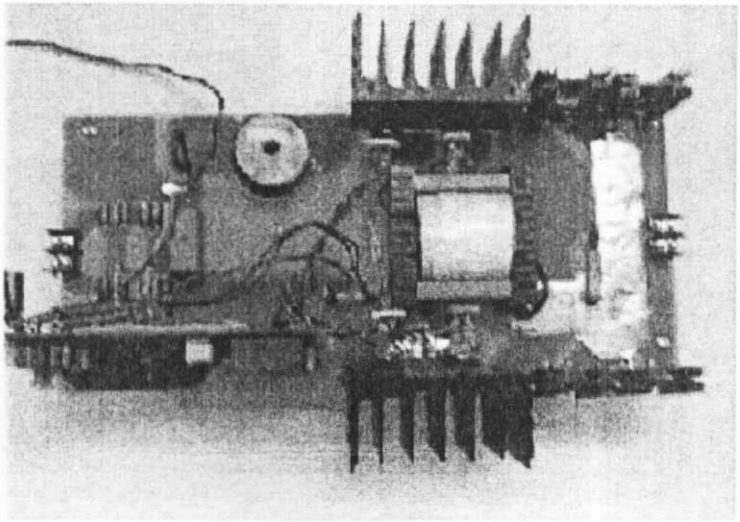


Figure 4.17: Photograph of 1 kW isolated-boost full-bridge converter

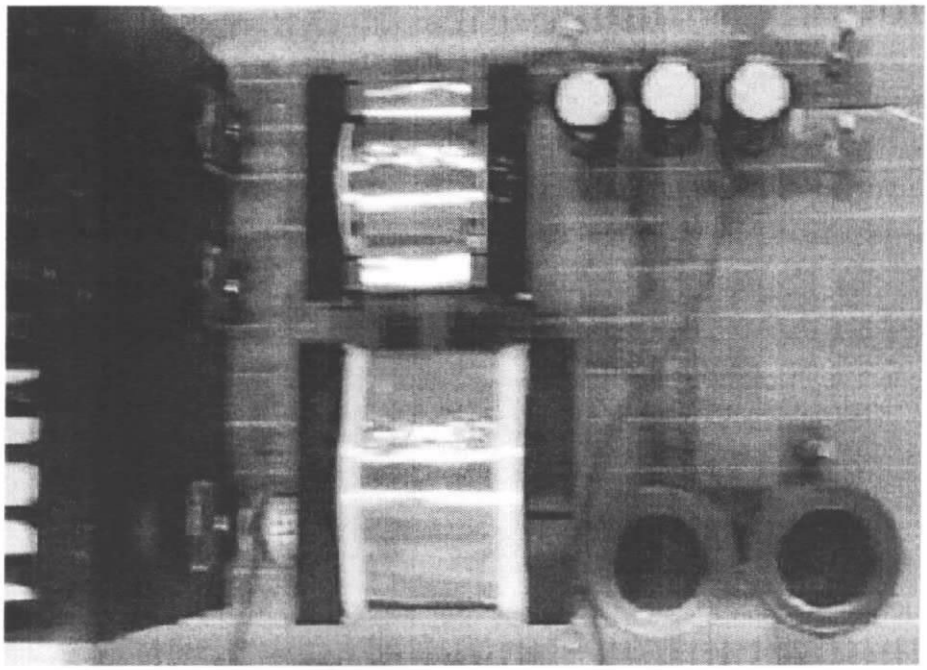


Figure 4.18: Photograph of 600 W buck-boost converter

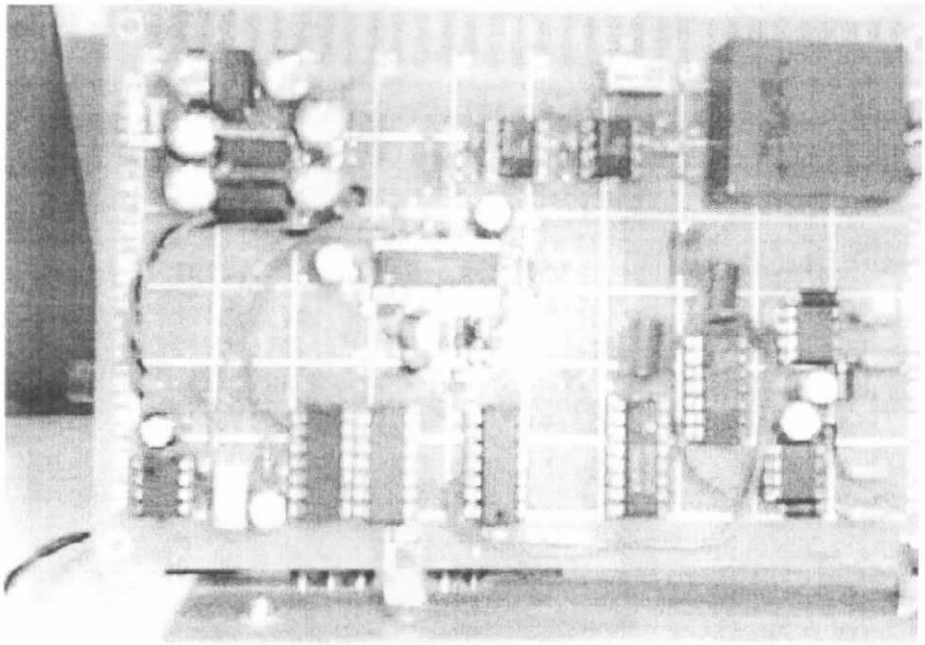


Figure 4.19: Photograph of the PFC controller

4.11 Summary

This chapter studies a particular OSPFC employing an isolated-boost full-bridge pre-regulator and a buck-boost voltage regulator, and the regulators are operated in CCM for 1-kW output power applications. This OSPFC can provide a reasonably high power factor when the regulators are connected with non-cascaded fashion. Substantial practical circuits for high efficiency PFC switching regulator applying reduced redundant power processing principle have been shown. This chapter derives an appropriate procedure for choosing each regulators in the OSPFCs. Quantitative analyses on the gain of the efficiency of the OSPFC and the voltage stress of on the energy storage capacitor are present. A comparison illustrates that the requirement on the energy storage capacitor capacitance of the OSPFC is higher than that of the case when the IBFB and buck-boost converters are connected in cascaded. According to the principle, the overall efficiency of the proposed OSPFC can be improved because part of the output power of the IBFB converter is transferred directly to the regulated output. A 1 kW experimental prototype has been built and tested, which can achieve high input power factor and tight output voltage regulation. The measured results validate the theoretical prediction on the improved efficiency for the proposed OSPFC in comparison with the cascaded operation. The chapter shows that the reduced redundant power processing (R^2P^2) principle not only work in low power applications PFC switching regulators but also can be applied into high power applications PFC switching regulators.

Chapter 5

Features of Non-Cascaded PFC Switching Regulators

By definition a non-cascaded power-factor-corrected switching regulator allows part of input energy without double processed by two converters or directly transfer input energy to output load and provides output voltage regulation and input power factor correction. In the last two chapters detailed design procedures and practical implementation information of two particular non-cascaded power-factor-corrected switching regulators, which are operated in both CCM pre-regulator and voltage regulator, are given. In essence, the non-cascaded power-factor-corrected switching regulators use the three-port power flow diagram to develop 15 configurations [6, 8]. On the other hand, only 8 configurations, are shown in Figure 5.1, have ability for providing galvanic isolation, that include the ISPFCs and OSPFCs. Derivation of practical circuit can be based on the configuration block diagrams from Figure 5.1 for creating non-cascaded power-factor-corrected switching regulators. For ease of presentation, each configurations are named by the authors [6, 8], for example Type I-IIA and Type I-IIIB are denoted the ISPFCs and OSPFCs respectively. Based on these configurations, the squares of block diagrams can be replaced by two simple converters for construction of actual circuits.

The original contribution of this chapter is point out the features of the non-cascaded power-factor-corrected switching regulators, especially based on reduced redundant power processing (R^2P^2) principle in designing switching

regulators. A completed comparison for the particular two regulators, ISPFC and OSPFC, are discussed.

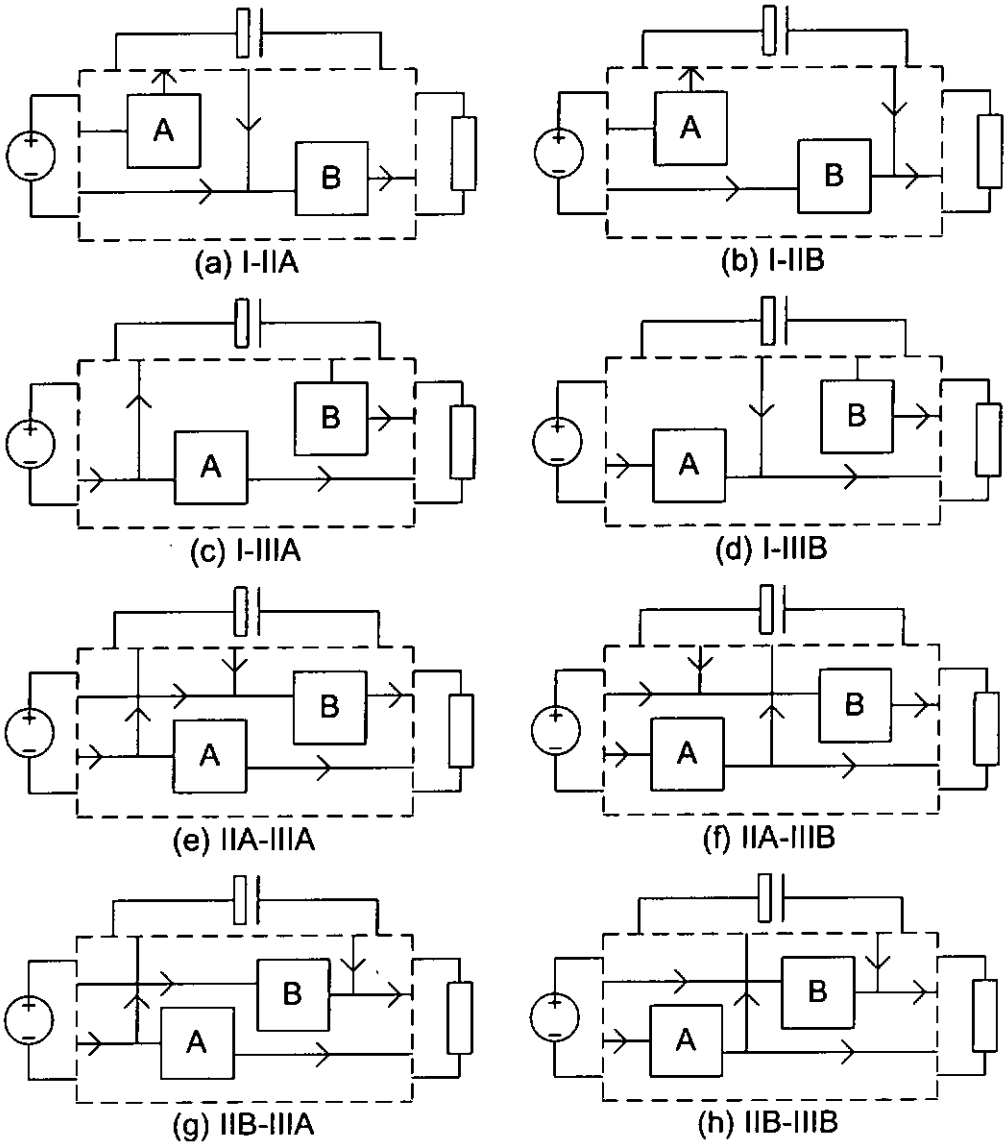


Figure 5.1: Configuration block diagrams of the non-cascaded power-factor-corrected switching regulators in terms of power flow paths

5.1 Summarization of Possible Non-Cascaded PFC Switching Regulators

Referring to Figure 5.1, the pre-regulator and voltage regulator are presented by the converter A and converter B, respectively. For ease of discussion, the type I-IIA, I-IIB, I-IIIA, and I-IIIB are chosen for the example to describe the procedure for constructing non-cascaded power-factor-corrected switching regulators. Figure 5.2 shows the equivalent circuits of these four types and rectangular blocks denote pre-regulator and voltage regulator. The next logical step is put a simple converter to the rectangular boxes. As mentioned in the previous chapter, the simple converters have short circuit path, for example, buck and boost converter short circuit path occur between their input negative terminal and output negative terminal, and buck-boost and Ćuk converter short path occur between their input negative terminal and output positive terminal. Clearly, in choosing a non-isolated basic converter for placement in an non-cascaded switching regulator, the designer are required to ensure that the simple converter short circuit path does not affect the non-cascaded switching regulators operation. Table 5.1 shows the possible choices of non-isolated converter for constructing the non-cascaded switching regulators, along with some previously reported circuits.

- For Configuration I-IIA, converter A can only be a buck-boost converter, and converter B can be any converter.
- For Configuration I-IIB, two cases are possible. If converter A is a buck or a boost converter, converter B can only be a buck-boost converter, on the other hand, if the converter A is a buck-boost converter, the converter B can be a buck or a boost converter.
- For Configuration I-IIIA, two cases are possible. Converter A can only is a buck-boost converter, when converter B is a buck or a boost converter. However, converter A can be a buck or a boost converter, converter B can only be a buck-boost converter.
- For Configuration I-IIIB, converter B can only be a buck-boost converter, and the converter A can be any converter.

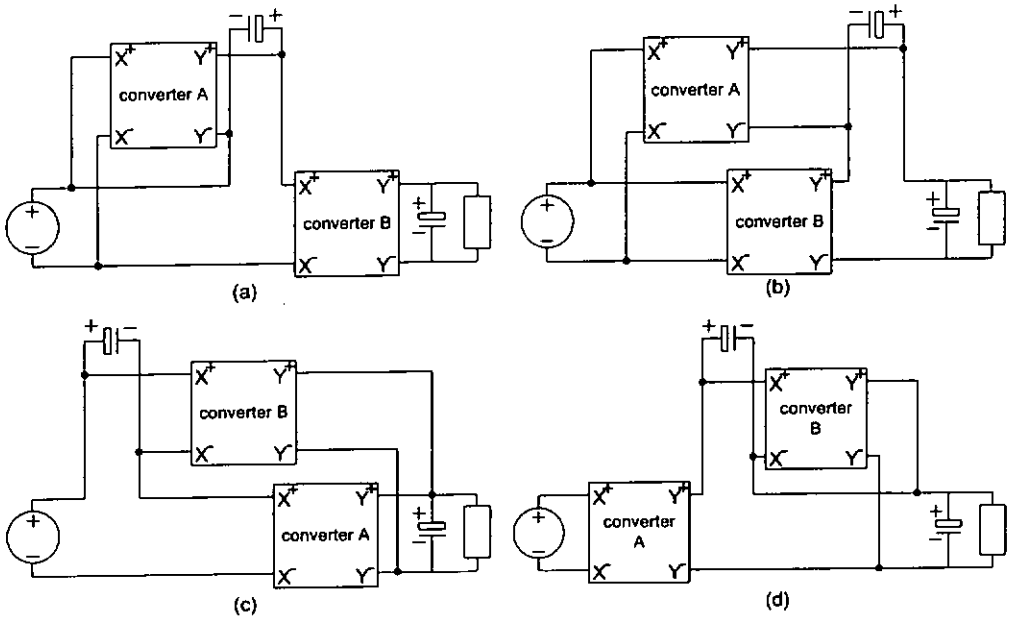


Figure 5.2: Equivalent circuits of the simplest reduced redundant power processing (R^2P^2) configurations: (a)I-IIA; (b)I-IIB; (c)I-IIIA; and (d)I-IIIB.

In the above-mentioned configurations, the non-cascaded switching regulator circuits are without galvanic isolation. The requirement of isolation between the input and load necessitates the use transformer-isolated converters for either or both constituent converters. The simplest implementation for Configuration I-IIA is to have only converter B isolated. In Configuration I-IIIB, the isolated converter should be implemented in converter A. Configurations I-IIB and I-IIIA would require transformer isolation for both converters A and B. Hence, this is major reason why only Configurations I-IIA and I-IIIB are chosen to implement practical non-cascaded switching regulators in this study.

5.2 Comparison of Two Non-Cascaded PFC Switching Regulators

The characteristics of three power-factor-corrected switching regulators are listed in Table 5.2 and Table 5.3. These are the proposed ISPFC, the proposed OSPFC, and a conventional power-factor-corrected switching regulator

Table 5.1: Possible choice of converter for non-isolated R^2P^2 power-factor-corrected switching regulator

Configuration	Converter A	Converter B	Reported
I-IIA	buck-boost	buck	Zeta and Chow et al. [7]
I-IIA	buck-boost	buck-boost	-
I-IIA	buck-boost	boost	-
I-IIB	buck	buck-boost	-
I-IIB	boost	buck-boost	-
I-IIB	buck-boost	buck	-
I-IIB	buck-boost	boost	-
I-IIIA	buck	buck-boost	-
I-IIIA	boost	buck-boost	-
I-IIIA	buck-boost	buck	-
I-IIIA	buck-boost	boost	-
I-IIIB	buck-boost	buck	-
I-IIIB	buck-boost	boost	SEPIC and BIFRED [48]
I-IIIB	buck-boost	buck-boost	Garcia et al. [5]

that is a boost pre-regulator and a single-switch forward converter connected in cascade.

5.2.1 Pre-Regulator Comparisons

Input current harmonics is a major concern for switching regulator design engineers. The conventional boost converter operating in CCM has been applied to power factor correction. It has a continuous input inductor current and generates less EMI problems. Buck-boost pre-regulator of the proposed ISPFC has trapezoidal and pulsating input current. This results in severe EMI problems and requires a significant input filter. Besides, the input filter may cause input current phase delay in PFC. The IBFB pre-regulator of the proposed OSPFC not only has continuous input current but also can provide the voltage step down and up function, which is provided by the power transformer turn ratio.

Table 5.2: Comparisons among conventional boost converter, buck-boost converter (ISPFC), and IBFB converter (OSPFC) for PFC

Converters	Boost	Buck-boost (ISPFC)	IBFB (OSPFC)
Voltage conversion	Step up	Step up / down	Step up / down
Component count	3 elements	3 elements	10 elements
Switch voltage stress	Output voltage	Rectified voltage +Output voltage	Reflected output voltage
Diode voltage stress	Output voltage	Rectified voltage +Output voltage	Output voltage
Switch and diode current (average)	Input current	Input+Output current	Input current
Input current	Continuous	Pulsating	Continuous
Input filter	No necessary	Necessary	No necessary
Output current (before filter)	Pulsating	Pulsating	Pulsating
Output filter	Required	Required	Required
Harmonic distortion	Little	Significant	Little
Input filter phase delay	No	Yes	No

The continuous input current in the conventional boost and the IBFB converter can decrease the harmonic distortion significantly and thus achieve good EMI performance. However the IBFB converter has a large component count compared with the conventional boost and the buck-boost converter, and volt-second balance problem of the IBFB converter transformer should be taken with good care by the engineers during implementation.

The output current of all pre-regulators are pulsating, so high quality, low ESR (equivalent series resistance) and ESZ (equivalent series impedance), capacitor is needed for filtering the pulsating current and buffer the difference between the instantaneous input power and output power in the power-factor-

corrected switching regulators.

To select proper circuit, the component voltage and current stresses are very important criteria. From Table 5.2, it can be seen that the IBFB converter retains the advantages of the conventional boost converter. The voltage stresses on the active switches and power diodes are the reflected output voltage only while that is the sum of input voltage and output voltage in the case of buck-boost. It can be seen that the conventional boost and the IBFB converter voltage stress is independence with input line voltage. The sum of the current flowing through the active switch and the power diode is the input current only for the case of the conventional boost and the IBFB converter while that is the sum of the input and output current in the case of the buck-boost converter.

Table 5.3: Comparisons among conventional forward converter, forward converter (ISPFC), and buck-boost converter (OSPFC) for voltage regulation

Converters	Single-switch forward	Two-switch forward (ISPFC)	Buck-boost (OSPFC)
Input voltage	DC (100 Hz ripple)	Rectified voltage +DC (100 Hz ripple)	DC (100 Hz ripple)
Voltage conversion	Step down	Step down	Step down / up
Component count	6 elements	8 elements	3 elements
Switch voltage stress	Double input voltage	Input voltage	Input+Output voltage
Diode voltage stress	Input+Output voltage	Input+Output voltage	Input+Output voltage
Input current	Pulsating	Pulsating	Pulsating
Output current	Continuous	Continuous	Pulsating
Current through output capacitor	Small	Small	Large
Diode current (R. M. S. and peak)	Low	Low	High

5.2.2 Voltage Regulator Comparisons

The conventional single-switch forward converter and the buck-boost converter (OSPFC) input voltage is a static voltage level containing a small amount of 100 Hz ripple voltage. Therefore the voltage regulation can be easily achieved by using the simplest control method in these converters. Because the input voltage of the two-switch forward converter is a rectified voltage superimposed on a DC voltage, the voltage regulation may not be easy to achieve without complicated control methods such as feedforward control and current mode control.

The inherently stable input voltage appearing in the single-switch forward and the buck-boost converter can provide significant improvement in the load regulation because the duty cycle of switches is more or less constant.

Since the ripple current through the output capacitor of two forward converters is small and the output current have a continuous waveform, the forward converters do not need high quality, low ESR and ESZ, capacitor for their output capacitor. Also the output capacitor will have a longer lifetime compared with the pulsating output current of buck-boost converter.

Table 5.3 shows that the diode voltage stress of all converters is equal to the input voltage superimposed by the output voltage. However the IBFB converter has step down voltage function, the active switch of the buck-boost converter operates at lower voltage stress compared with the switches of the forward converters. It is because the active switch of the single-switch forward converter to suffer a stress of a double input voltage, and in the case of the two-switch forward converter, the switches have to tolerate a stress of input voltage level. The buck-boost converter has an advantage in the component count compared with the two forward converters, because the buck-boost converter does not need to set an extra current path for resetting the magnetizing current of the power transformer. For given output current, the R. M. S. and the peak current of diodes of the two forward converters are lower than that of the buck-boost converter.

5.3 Features of Two Non-Cascaded PFC Switching Regulators

The features of the conventional cascaded configuration, consisting of a boost and a single-switch forward converter, the proposed ISPFC configuration, and the proposed OSPFC configuration used in power-factor-corrected switching regulator are listed in Table 5.4.

Table 5.4: Comments of ISPFC and OSPFC, and compared with the conventional cascaded configuration.

Configurations	Conventional	ISPFC	OSPFC
Input voltage range	Narrow and low	Narrow and low	Wide and high
Output voltage	Wide range	Wide range	Narrow range
Harmonic distortion	Low	High	Low
Power factor	Near perfect	Imperfect	Near perfect
Output power level	Low to high	Low to medium	Low to high
Storage element voltage level	High	Low	Low
Component count	9 elements	11 elements	13 elements
PFC control method	Average or peak current mode	Average current mode	Average or peak current mode
Voltage regulation control method	Voltage mode or peak current mode	Peak current mode	Peak current mode
Control circuits and complexity	Independent and ease	Independent and advanced	Independent and advanced
Overall efficiency	Low	High	High

5.3.1 Conventional Cascaded Configuration

Input voltage range of the conventional cascaded configuration usually operates at low line voltage level, because high input voltage leads to high voltage stress in the active switches and power diodes, then consequently this causes high voltage level imposed on the storage element. However, the configuration has nearly perfect power factor and low harmonic distortion. Additionally it can operate at low input line voltage and high output power applications, because the current rating of their converters only equal to their input current and output current. From the production cost point of view, the total number component count is the lowest in comparison with the ISPFC and the OSPFC configurations. The two independent control circuits, the simplest control methods, and the power switches with non-isolated driver circuits are employed by this configuration. The major disadvantage of the cascaded configuration is that two constituted converters are connected by cascaded configuration, which inevitably causes low efficiency operation.

5.3.2 Non-Cascaded ISPFC Configuration

The ISPFC can only be operated in low line voltage, owing to high line voltage provides extreme high input voltage of the voltage regulator. In addition, the pre-regulator active switch and power diode suffer high voltage stress. Therefore the ISPFC configuration is only suitable for the low and medium power applications. The storage element voltage level could be lower than the cascaded configuration and the level can be step up or down depends on the pre-regulator duty signal. Nevertheless, this configuration can only provide imperfect power factor and the harmonic distortion is a bit higher than the cascaded and OSPFC configurations. In the control circuit, the PFC controller should use average current mode control for improving accuracy in tracking of the input current. The voltage regulator is controlled by the peak current mode controller, because the input voltage is variable voltage. The driver circuit of the voltage regulator power switches must be isolated version. The merit of the ISPFC configuration is that part of the input power directly transfers to the voltage regulator. It has ability for improving efficiency due the reduction in power re-processing in the two constituted converters. The efficiency gain of

the ISPFC is affected by the voltage ratio between the storage element voltage and the input line voltage.

5.3.3 Non-Cascaded OSPFC Configuration

The OSPFC has advantages of the cascaded configuration and the ISPFC configuration. An IBFB converter for pre-regulator has nearly perfect power factor and low harmonic distortion. The storage element voltage level can be stepped down by the power transformer turn ratio. Owing to the OSPFC configuration has step up and down function, it can operate at wide input line voltage range. The configuration is suitable for low to high output power applications. But the IBFB converter power switches still suffer high voltage stress. In this configuration, only a buck-boost converter can be used in the voltage regulator and the peak current mode is employed by the voltage regulator controller to overcome the right-half plane zero problem. In the OSPFC, all switches drivers circuits are isolated. The main advantage of the OSPFC is that the output power of the pre-regulator directly transfers to the regulated load, therefore the voltage regulator is not required to processing all output power. Clearly, this reduces the cost and size of the voltage regulator and provides more efficient power conversion. The output voltage of the pre-regulator must contain output DC voltage that causes the capacitance of the storage capacitor larger than the cascaded configuration for given power output and ripple voltage level. Although the OSPFC is constructed with 13 basic elements that could be considered as an expensive solution by the switching regulator design engineers, the OSPFC has nearly perfect PFC and efficient power conversion as practising circuit in high power applications.

5.4 Summary

Complete sets of three configurations, the conventional cascaded configuration, the ISPFC configuration, and the OSPFC configuration, and their corresponding features are derived and compared in this chapter. The results are important in understanding for the applications of the configurations. In particular, it has shown that the ISPFC can operate in low line input voltage only. The OSPFC has the ability to operate at wide range input voltage and keeps the storage element voltage at low level due to the power transformer turn ratio. Moreover, this chapter illustrates that the major advantage of the ISPFC and the OSPFC configurations is to provide a highly efficient power conversion process than that of the cascaded configuration. In this chapter, it also provides a completed summary for creating a new non-cascaded power-factor-corrected switching regulators.

Chapter 6

Conclusion and Future Research

The delivery of electric power with a well regulated DC output voltage and in-phase sinusoidal input-current from the single-phase AC mains is an important technical area in power electronics. Serious current harmonic distortions are created by nonlinear loads such as line-fed rectifiers with smoothing capacitors, and it leads to poor utilization of the AC mains, reduction efficiency and creation of interference problems. Hence, a current waveform with unity power factor can offer a full utilization of the AC mains and reduce the interference problems.

Power factor correction fall into two categories: they are namely passive methods and active methods. Since the passive methods suffer from excessive size and weight, the active methods become commonly used in practice which can be classified as non-automatic and automatic PFC methods. Automatic power factor is based on DCM operation. These correctors draw proportional input current with sinusoidal input voltage when operating under fixed duty signal and switching frequency. This thesis focuses on non-automatic power factor correctors use a separate input current controller as in the buck-boost or boost PFC converters operating in CCM.

The essential requirements of power-factor-corrected switching regulators must contain three components, pre-regulator, voltage regulator, and low frequency storage element. The conventional power-factor-corrected switching regulators are connected in cascaded connection by these three components. In this approach, the voltage regulator is a simple DC-DC converter that main-

tains a regulated output while the preceding pre-regulator for power factor corrector ensures a high input power factor and low harmonic distortion. The storage element usually is connected between the pre-regulator and the voltage regulator. This type of combined circuits always has a lower efficiency, because the input power is processed by two power conversion stages before it can reach the output load. New arrangement, non-cascaded connection, for the power-factor-corrected switching regulators is proposed by [6]-[8]. In essence, a detail theory prove out that the non-cascaded power-factor-corrected switching regulators not only provide PFC and voltage regulation but also achieves higher efficiency compared with the cascaded connected switching regulators. Nevertheless, switching regulator design engineers has been slow to appreciate and exploit the considerable advantages of the non-cascaded connected switching regulators. This study provides completed practical implementation information for the engineers who want to fully understand the non-cascaded switching regulators.

6.1 Contributions of the Thesis

Due to its potential in the improvement of the overall efficiency of the power-factor-corrected switching regulators, two non-cascaded power-factor-corrected switching regulators based on reduced redundant power processing are studied in detail.

A practical input-side non-cascaded power-factor-corrected switching regulator provides a reasonably high power factor, which is achieved by the buck-boost converter. Because the return current path of the two-switch forward converter connects directly to the bridge rectifier, the switching regulator cannot provide prefect PFC. The line current harmonic distortion could be reduced at the expense of the double power processing at two power conversion stages. The overall efficiency of the ISPFC is controlled by the voltage ratio between the storage element voltage and the input line voltage. In order to simplify the design of the feedback control associated with power factor and voltage regulation, a detail average model proves that the two duty signals should operate independently. Thus two control methods, average current mode control and peak current mode control are applied in the pre-regulator and the voltage

regulator respectively. This thesis shows an ISPFC prototype for validating the efficiency equations and the amount of the power that is directly transfered to the output port. The measured results illustrate the prototype can operate at high overall efficiency compared that constituted converters connected in cascaded configuration.

A practical output-side non-cascaded power-factor-corrected switching regulator is also described in this thesis. This switching regulator is derived by reduced redundant power processing principle for achieving unity power factor, low storage element capacitor voltage stress, fast voltage regulation, and high overall efficiency. Unlike the input-side non-cascaded configuration arrangement, the input current can be fully controlled by the OSPFC pre-regulator. For reducing the re-processing power, part of the output power is directly transfered to the regulated output, in the other words the voltage regulator has to process a power less than the output power, so the voltage regulator becomes smaller in size and has a lower voltage and current stresses rating in saving of the production cost. This thesis is to explain the efficiency equations and the amount of power that is transfered directly to the output in terms of the circuit parameters. The maximum efficiency gain of the practical OSPFC is illustrated. The isolated-boost full-bridge pre-regulator is controlled by a common PFC controller chip, UC3854, with the additional logical circuits and a simple peak current mode control is employed by the buck-boost voltage regulator. The performance of the OSPFC with proposed non-cascaded connection is verified with experimental tests at high output power level.

This thesis also conducts a theoretical examination of the circuit requirements for achieving both high power quality and fast output regulation in switching regulators. The basic PFC switching regulator is modeled by a three-port network. According to the three-port network, the authors of [6, 8] are proposed a family of sixteen configurations that are derived based on the concept of power flow graphs. From switching regulator design engineers point of view, only eight configurations have potential to become a practical products. Four realization examples, including ISPFC and OSPFC, are described and the description starts from the three-port network to the choice of placing converters for realization a practical circuit. The study provides in insight into the features of ISPFC and OSPFC. A detail comparison points out the char-

acteristics of these two types of non-cascaded power-factor-corrected switching regulators.

6.2 Suggestions for Future Improvement

This thesis described two main prototypes. One is the low power application of ISPFC and the other is high power application of OSPFC. Both of them are operated in hard-switching. In the low power applications, the voltage and current stresses can be suppressed by passive snubber circuits, however at high power applications the passive snubber circuits power consumption can affect the overall efficiency of the switching regulators. For solving this problem, zero voltage and zero current switching may be applied into two non-cascaded power-factor-corrected switching regulators. At the ISPFC, the ideal place for applying the zero voltage and zero current switching should be in the sequence of control duty signals that drive the switches. A properly designed sequence will make semiconductor devices of the ISPFC pre-regulator operating at zero voltage or zero current switching.

At the high power application of the OSPFC, a low-loss snubber circuit is applied at the voltage regulator to solve slow reverse recovery problem of the power diodes. The switching loss problem associated with the four switches in the isolated-boost full-bridge pre-regulator should also be taken care. The soft-switching techniques of the full-bridge converter for PFC are proposed by [82]-[85], there are good references for applying soft-switching at the isolated-boost full-bridge pre-regulator of the OSPFC.

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Conference papers

1. Chi K. Tse, M. H. L. Chow, and M. K. H. Cheung "Reduced redundant power processing (R^2P^2) PFC voltage regulators: Circuit synthesis and control", in Record of the 31st Annual IEEE Power Electronics Specialists Conference, pp. 825–830, June 2000.

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