DESIGN OF ROBUST AND FAST CONTROLLER FOR HIGH-PERFORMANCE DC-DC CONVERTERS

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Design of Robust and Fast Controller for High-Performance DC-DC Converters

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Certificate of Originality

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_____(Signed)

__MAJID ALI__(Name of student)

To my parents

Abstract

To provide a well-regulated supply voltage for their operation, dc-dc power converters are widely used in computers, cell phones, telecommunication system, grid-connected energy storage systems, distributed generators, photovoltaic systems, and many others. Fast dynamic response performance is an essential requirement for these dc-dc power converters, and this is achievable with a well-designed feedback controller. Traditional methods for designing feedback controller are based on an accurate small-signal model of the power converter. However, model uncertainties and power converter's parameter variations due to, for example temperature or aging effects, will adversely affect the performance of the designed feedback controller. Another major disadvantage of the conventional feedback control approach is that the feedback controller is required to meet both stability and transient response performance requirements, and these two requirements usually cannot be met with one set of controller parameters. Hence, there is always a tradeoff between stability and dynamic response performance. These factors make the design of high-performance feedback controller a challenging task. To address these issues various adaptive and nonlinear control methods have been proposed. However, these methods are relatively complex and require high-performance microcontroller for there implementation. The principal focus of this work is to develop and implement a parameter insensitive, hardware-efficient and high-performance feedback controller for dc-dc power converters. For illustration, the feedback controller design for non-isolated dc-dc buck converter

commonly used for low power applications and the isolated dc-dc dual-active-bridge (DAB) converter commonly used for medium to high power level has been selected for this study.

A novel non-intrusive method for online estimation of power-stage parameters and autotuning of the feedback controller for buck converter is presented in the first part of this research work. The autotuning controller presented has been specially developed to handle wide-range variations in the resonant frequency of the L_oC_o output filter, equivalent series resistance (ESR) zero of the output capacitor, and input voltage. The proposed controller accurately estimates the resonant frequency ω_o and the ESR zero frequency ω_{ESR} by examining the converter's startup transient and by online measurement of output voltage ripple. As a result, the proposed method is non-intrusive and does not disturb the converter's normal operation or output voltage regulation. Based on these results, the digital compensator is automatically tuned based on some user-defined phase margin and crossover frequency to provide the desired transient response and output voltage regulation over wide-range variations of power-stage parameters and operating points. It has been demonstrated by experimental results that the presented controller can maintain absolute stability and consistent transient performance over a wide-range of power-stage parameters and operating points of the converter.

In the second part of this research work, in order to enhance the transient response of the front-end DAB converter and reduce the amplitude of the second-order ripple component in the dc-bus voltage of a cascaded converter system comprising a DAB dc-dc converter followed by a single-phase inverter, a disturbance observer based dc-bus voltage control has been proposed. In the proposed method, a disturbance observer is designed based on minimal plant information and is combined with a proportional controller to form a decoupled composite controller for dc-bus voltage control. The input to the disturbance observer is

the sensed dc-bus voltage and the control signal. Hence, the proposed solution does not require additional voltage or current sensor. Using this information, the disturbance observer can accurately estimate and compensate for the lumped disturbance which includes external disturbances, model uncertainties, and circuit parameter variations due to temperature and aging effects. With these disturbances accounted for and their effects compensated, superior control performance can always be achieved.

In the final part of this research work, in order to overcome the bandwidth limitation of conventional feedback control methods, an uncertainty and disturbance estimator (UDE) assisted sensorless load current feedforward control scheme for two-stage single-phase inverter system has been proposed. The proposed control method consists of a feedforward path, an UDE, and a voltage feedback loop. The load current is estimated from the estimated average current of the DAB's secondary bridge, and lossless sensing of the dc-link capacitor current is achieved using a digital filter, and the estimated load current is fed forward to achieve fast dynamic response. However, the estimation accuracy of the load current and calculation of the optimum feedforward gain depends on the values of circuit parameters which may be not known with high precision. Hence, an UDE is used to compensate for model uncertainties and parameters variations, and the voltage feedback loop is designed to ensure good converter's stability. As compared to traditional single-loop voltage-mode control or voltage-mode control with load current feedforward, the proposed UDE assisted current sensorless load current feedforward control scheme results in an improved dynamic response performance and reduced dc-bus voltage ripple.

Publications

Journal papers

1. **M. Ali**, M. Yaqoob, L. Cao, and K. H. Loo,"Disturbance Observer Based DC-Bus Voltage Control for Ripple Mitigation and Improved Dynamic Response in Two-Stage Single-Phase Inverter System," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 9, pp. 6836-6845, 2019.

2. **M. Ali**, K. H. Loo, and Y. M. Lai,"Non-Intrusive Parameter Estimation Method for Autotuned DC-DC Converter Based on Quasi-Impulse Response," *IET Power Electronics*, vol. 11, no. 12, pp. 2019–2028, 2018.

Conference papers

1. **M. Ali**, K. H. Loo, and Y. M. Lai,"Digital Autotuning Controller for Point-of-Load Converter Based on Non-Intrusive Start-up Transient Observer," in *8th Annual IEEE Energy Conversion Congress & Exposition (ECCE)*, Wisconsin, USA, 2016, pp. 1-8.

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Chapter 1

Introduction

1.1 Motivation and Objectives

Many applications such as computers, cell phones, telecommunication power supplies, solid-state-transformer (SST), photovoltaic systems, distributed generators, gird connected energy storage systems requires switch-mode dc-dc converters for there proper operation. The primary requirement for the dc-dc power converters in these applications is to provide accurate and reliable voltage during steady-state, fast dynamic response and absolute stability over wide range of converter's power-stage components values and operating points. A well-designed feedback controller is required to achieve these objectives. Conventionally a single-loop voltage-mode control or dual-loop current-mode control is employed to regulate the output voltage of the power converter. Frequency domain analysis such as Bode plot and root locus methods are used for the design and analysis of the feedback controller.

Conventional linear feedback controllers are designed based on the small-signal model of power converter. Thus an accurate small-signal model of the converter is needed for feedback controller design. Once a feedback controller is designed for a particular set of power-stage parameters, any changes in these parameters mainly

due to aging and temperature dependencies will have adverse effects on the performance of the designed feedback controller. Additionally, conventional feedback controller needs to meet both stability and transient response requirements, and these two are often in contradiction with each other. Hence, a compromise between stability and transient response performance is inevitable. Consequently, control methods that can improve the dynamic response without effecting stability needs to be employed. This motivates our research to investigate alternative control methods to improve the dynamic response performance of the converter without affecting its stability.

The main objective of this research work is to develop and implement a parameter insensitive, hardware-efficient and high-performance feedback controller for dc-dc power converters. For illustration, the feedback controller design for nonisolated dc-dc buck converter commonly used for low power applications and isolated dc-dc dual-active-bridge (DAB) converter commonly used for medium to high power level have been selected for this study.

1.2 Outline of the Thesis

The thesis is organized as follows:

In Chapter 2, the influences of variations in power-stage component values on closed-loop gain are investigated. In addition, various autotuning control methods presented in the literature are reviewed and there limitations are discussed.

In Chapter 3, a non-intrusive method for online estimation of power-stage components values and autotuning of feedback compensator for a digitally controlled dc-dc buck converter is presented. The presented autotuning controller can maintain a consistent transient response performance and stable operation over wide-range variations in the equivalent series resistance (ESR) zero of the output capacitor and the resonant frequency of the output filter. Experimental

results are presented to verify the effectiveness of the proposed control method.

In Chapter 4, the basic steady-state operating principle of a two-stage cascaded converter comprising of a front-end DAB dc-dc converter followed by a single-phase inverter is presented. Furthermore, a comprehensive review of various control methods proposed in the literature to enhance the transient response of the front-end DAB converter is presented.

In Chapter 5, a disturbance observer based control method is proposed to enhance the dynamic response performance of the frond-end DAB converter and to reduce the double-line frequency ripple in the dc-bus voltage of a two-stage single-phase inverter system. In the proposed method, all un-modeled effects including external disturbances and parameter variations are treated in the form of lumped disturbance which are estimated in real-time and compensated for in a feed-forward manner.

In Chapter 6, an uncertainty and disturbance estimator (UDE) assisted sensorless load current feedforward is proposed to achieve fast dynamic response and to reduce dc-bus ripple in a cascaded converter system comprising a front-end DAB dc-dc converter followed by single-phase inverter. In the proposed method load current feedforward is used to enhance the dynamic response of the front-end DAB converter while an UDE is used to compensate for any nonidealities arising from model uncertainties and error in load current estimation.

Concluding remarks and suggestions for future researches are provided in Chapter 7.

Chapter 2

Digital Autotuning Control Methods for DC-DC Power Converter

2.1 Introduction

Buck converter is commonly used to provide a well-regulated and reliable dc-output voltage. The applications of buck converter range from small hand-held devices such as mobile phones and tablets to large desktop and servers. To regulate the output voltage of a buck converter around a particular reference voltage a well-designed feedback controller is required [1–7]. The most commonly used control methods for feedback control design of buck converter is voltage-mode control or current-mode control. However, in conventional off-line feedback controller design, power-stage parameters are directly used [8–13], but uncertainty in the knowledge of power-stage component values due to manufacturing tolerance and aging can adversely affect the design accuracy and performance of the designed controller [14–18].

In this chapter, the influences of variations in power-stage parameters on loop-

gain design are investigated in detail. The design and implementation of some digital autotuning controllers for buck converter published in the literature will also be reviewed.

2.2 Influence of Power-Stage Parameters on Loop Gain

2.2.1 Voltage-Mode-Controlled Buck Converter

The schematic of a voltage-mode-controlled buck converter with a Type-III compensator is shown in Fig. 2.1. The control-to-output transfer function of a buck converter is a function of output filter's resonant frequency and output capacitor's ESR zero frequency, as given by equation (2.1) [19, 20].

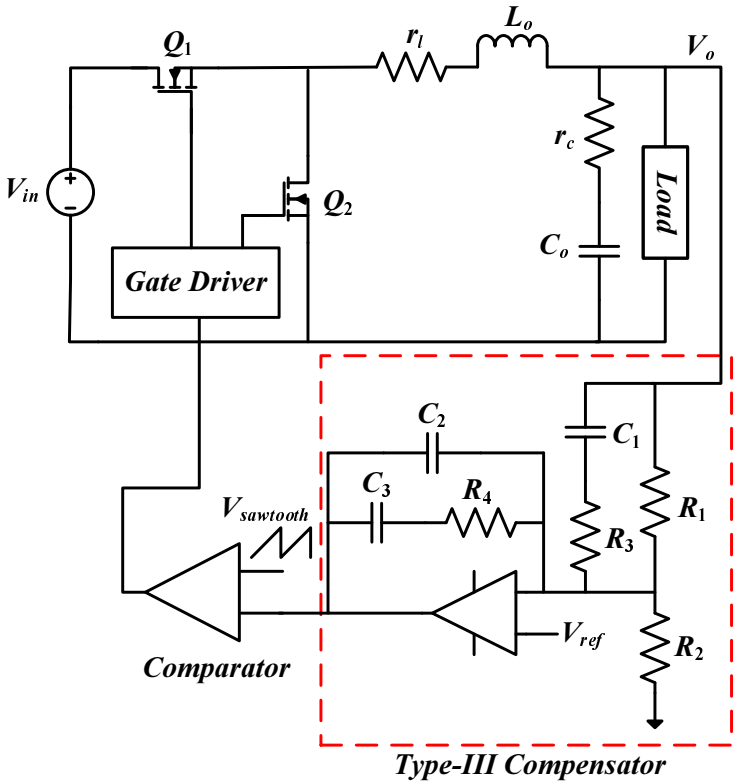


Figure 2.1: Voltage-mode-controlled buck converter with Type-III compensator.

$$G_{vd}(s) = \frac{v_o(s)}{d(s)} = V_{in}\frac{1+\frac{s}{\omega_{ESR}}}{1+2\frac{\zeta}{\omega_o}s+\frac{s^2}{\omega_o^2}} \tag{2.1}$$

where

$$\omega_o = \frac{1}{\sqrt{L_o C_o}} \tag{2.2}$$

$$\zeta = \frac{R_{dson}+r_l+r_c}{2}\sqrt{\frac{C_o}{L_o}} \tag{2.3}$$

$$\omega_{ESR} = \frac{1}{r_c \times C_o} \tag{2.4}$$

Generally, a Type-III compensator is used for realizing voltage-mode feedback control. The s-domain transfer function of a Type-III compensator has three poles and two zeros, as given by equation (2.5). Typically, compensating a converter to meet regulation objectives and stability criteria requires the placement of the first zero of the compensator (ω_{z1}) at low frequency to compensate for the phase lag of the pole at the origin. The second zero (ω_{z2}) is used to compensate for one of the power stage's double poles. The first pole (ω_{p1}) is used to cancel the output capacitor's ESR zero, and the second pole (ω_{p2}) is used to provide attenuation for frequencies above half of the switching frequency. The value of the integrator gain K is chosen such that the desired crossover frequency and phase margin are obtained [21, 22].

$$G_{com}(s) = \frac{K}{s}\frac{(1+\frac{s}{\omega_{z1}})(1+\frac{s}{\omega_{z2}})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})} \tag{2.5}$$

$$\omega_{z1} = 0.8\omega_o = 0.8\frac{1}{\sqrt{L_o C_o}} \tag{2.6}$$

$$\omega_{z2} = \omega_o = \frac{1}{\sqrt{L_o C_o}} \tag{2.7}$$

$$\omega_{p1} = \omega_{ESR} = \frac{1}{r_c \times C_o} \tag{2.8}$$

$$\omega_{p2} = \frac{\omega_s}{2} \tag{2.9}$$

$$K = \frac{\omega_{z1}\omega_{z2}\omega_c}{V_{in}\omega_o^2} \tag{2.10}$$

where ω_c is the desired closed-loop bandwidth. According to [23, 24], the fundamental upper limit for ω_c is $\frac{1}{3}$ of the switching frequency. For most practical designs the recommended value for ω_c is $\frac{1}{5}$ to $\frac{1}{10}$ of the switching frequency.

Based on the time-domain transfer function of an analog compensator, the z-domain representation of an equivalent digital controller can be obtained by bilinear transformation (equation 2.11) and the result is given by equation (2.12).

$$s = \frac{2}{T_s}\frac{(z-1)}{z+1} \tag{2.11}$$

where $T_s = \frac{1}{f_s}$ is the sampling frequency, which is equal to the converter's switching frequency.

$$G_{com}[z] = \frac{y[z]}{e[z]} = \frac{B_0 + B_1 z^{-1} + B_2 z^{-2} + B_3 z^{-3}}{1 + A_1 z^{-1} + A_2 z^{-2} + A_3 z^{-3}} \tag{2.12}$$

where $e[z]$ is the error signal which is the input to the digital controller and $y[z]$ is the value of duty cycle.

By applying the shifting property of z-transform, the coefficients of the digital controller expressed in terms of the locations of the converter's poles and zeros, sampling frequency T_s, and dc gain can be obtained as given by equations (2.13)-

(2.19).

$$A_1 = \frac{-12 + T_s^2\omega_{p1}\omega_{p2} - 2T_s^2(\omega_{p1} + \omega_{p2})}{(2 + T_s^2\omega_{p1})(2 + T_s^2\omega_{p2})} \tag{2.13}$$

$$A_2 = \frac{12 - T_s^2\omega_{p1}\omega_{p2} - 2T_s^2(\omega_{p1} + \omega_{p2})}{(2 + T_s^2\omega_{p1})(2 + T_s^2\omega_{p2})} \tag{2.14}$$

$$A_3 = \frac{(2 - T_s^2\omega_{p1})(-2 + T_s^2\omega_{p2})}{(2 + T_s^2\omega_{p1})(2 + T_s^2\omega_{p2})} \tag{2.15}$$

$$B_0 = \frac{T_s K\omega_{p1}\omega_{p2}(2 + T_s\omega_{z1})(2 + T_s\omega_{z2})}{2(2 + T_s\omega_{p1})(2 + T_s\omega_{p2})\omega_{z1}\omega_{z2}} \tag{2.16}$$

$$B_1 = \frac{T_s K\omega_{p1}\omega_{p2}[-4 + 3T_s^2\omega_{z1}\omega_{z2} + 2T_s(\omega_{z1} + \omega_{z2})]}{2(2 + T_s\omega_{p1})(2 + T_s\omega_{p2})\omega_{z1}\omega_{z2}} \tag{2.17}$$

$$B_2 = \frac{T_s K\omega_{p1}\omega_{p2}[-4 + 3T_s^2\omega_{z1}\omega_{z2} - 2T_s(\omega_{z1} + \omega_{z2})]}{2(2 + T_s\omega_{p1})(2 + T_s\omega_{p2})\omega_{z1}\omega_{z2}} \tag{2.18}$$

$$B_3 = \frac{T_s K\omega_{p1}\omega_{p2}(-2 + T_s\omega_{z1})(-2 + T_s\omega_{z2})}{2(2 + T_s\omega_{p1})(2 + T_s\omega_{p2})\omega_{z1}\omega_{z2}} \tag{2.19}$$

The corresponding linear difference equation of the digital controller is given by equation (2.20).

$$y[n] = B_0e[n]+B_1e[n-1]+B_2e[n-2]+B_3e[n-3]-[A_1y[n-1]+A_2y[n-2]+A_3y[n-3]] \tag{2.20}$$

By keeping the aforementioned guidelines in view, a digital compensator has been designed for a buck converter operating with V_{in} = 12 V, V_o = 1.5 V, f_s = 500 kHz, C_o = 1.1 mF, r_c = 6 mΩ and L_o = 1.2 μH. Fig. 2.2 and Fig. 2.3 shows the converter's loop gain for large variations in L_o and C_o respectively,

along with the nominal values for which the compensator has been designed. It can be seen that for a fixed compensator and an increase in the values of L_o and C_o, phase margin increases and crossover frequency decreases, which deteriorate the converter's transient response. Also, in the case of a substantial increase in the values of the power-stage parameters (L_o and C_o,), multiple crossover frequencies can exist which cause the system to suffer from conditional stability. For the case of a decrease in the values of L_o and C_o, crossover frequency increases and phase margin decreases, which can make the converter unstable.

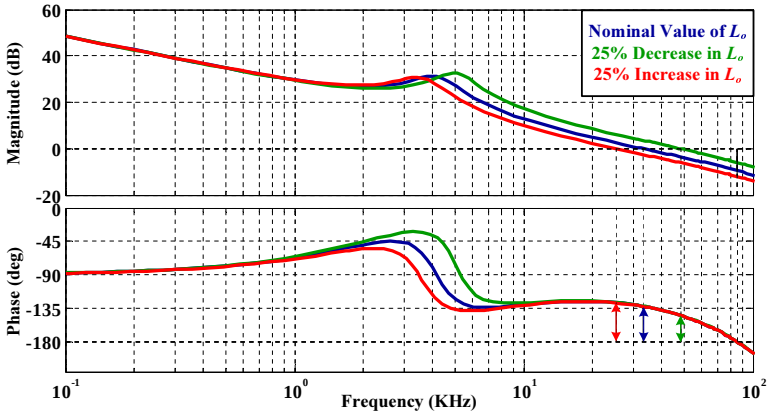


Figure 2.2: Open-loop gain with voltage-mode control for different values of L_o.

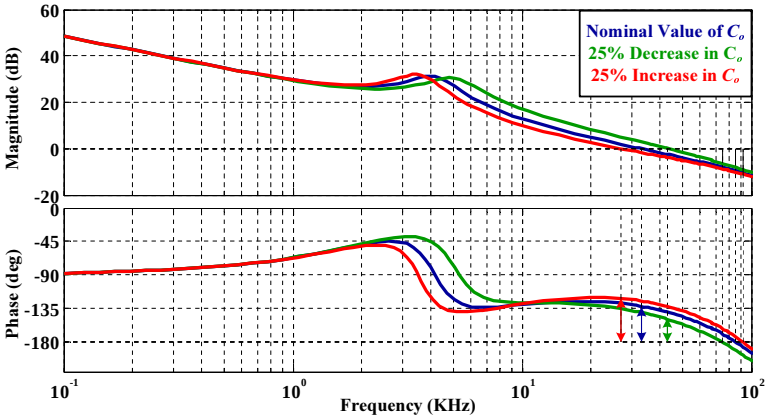


Figure 2.3: Open-loop gain with voltage-mode control for different values of C_o.

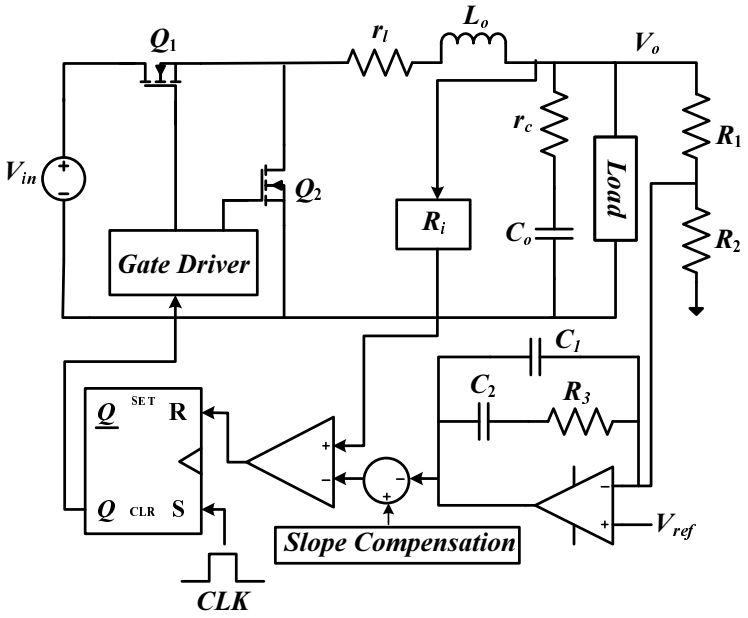


Figure 2.4: Peak-current-mode-controlled buck converter with Type-II compensator.

2.2.2 Peak-Current-Mode-Controlled Buck Converter

Fig. 2.4 show block diagram of a peak-current-mode-controlled buck converter with a Type-II compensator. Based on the multi-loop analysis method [25–27], the control-to-output-voltage and control-to-inductor-current transfer functions are given by equation (2.21) and (2.22) respectively.

$$G_{vd}(s) = \frac{v_o(s)}{d(s)} = V_{in}\frac{1+\frac{s}{\omega_{ESR}}}{1+2\frac{\zeta}{\omega_o}s+\frac{s^2}{\omega_o^2}} \tag{2.21}$$

$$G_{id}(s) = \frac{I_L(s)}{d(s)} = \frac{V_{in}}{R_{Load}}\frac{1+sR_{Load}C_o}{1+2\frac{\zeta}{\omega_o}s+\frac{s^2}{\omega_o^2}} \tag{2.22}$$

A simple compensation scheme is usually implemented for peak-current-mode control as compared to voltage-mode control. A Type-II compensator (with two poles and one zero) is normally used for this purpose [28]. A pole is placed at the origin to obtain zero steady-state error. The zero of the compensator (ω_z) is placed at low frequency to cancel the effect of the pole at the origin. The

second pole of the compensator (ω_p) is used to cancel the output capacitor's ESR zero. The value of the integrator gain K is chosen such that the desired crossover frequency and phase margin are obtained [22].

$$G_{com}(s) = \frac{K}{s}\frac{(1+\frac{s}{\omega_z})}{(1+\frac{s}{\omega_p})} \tag{2.23}$$

$$\omega_z = \omega_o = \frac{1}{\sqrt{L_o C_o}} \tag{2.24}$$

$$\omega_p = \omega_{ESR} = \frac{1}{r_c \times C_o} \tag{2.25}$$

$$K = \omega_z \omega_c R_i C_o \tag{2.26}$$

where ω_c is the desired closed-loop bandwidth and R_i is the current sensing gain.

By using bilinear transformation, i.e. equation (2.11), the s-domain transfer function of the analog Type-II compensator is transformed into z-domain, as given by equation (2.27).

$$G_{com}[z] = \frac{y[z]}{e[z]} = \frac{B_0 + B_1 z^{-1} + B_2 z^{-2}}{1 + A_1 z^{-1} + A_2 z^{-2}} \tag{2.27}$$

The corresponding linear difference equation of the digital controller is given by equation (2.28).

$$y[n] = B_0 e[n] + B_1 e[n-1] + B_2 e[n-2] - [A_1 y[n-1] + A_2 y[n-2]] \tag{2.28}$$

where

$$A_1 = -\frac{4}{2 + T_s\omega_p} \tag{2.29}$$

$$A_2 = \frac{2 - T_s\omega_p}{2 + T_s\omega_p} \tag{2.30}$$

$$B_0 = \frac{T_s K\omega_p(2 + T\omega_z)}{2(2 + T_s\omega_p)\omega_z} \tag{2.31}$$

$$B_1 = \frac{T_s K\omega_p}{2 + T_s\omega p} \tag{2.32}$$

$$B_2 = \frac{T_s K\omega_p(-2 + T\omega_z)}{2(2 + T_s\omega_p)\omega_z} \tag{2.33}$$

Fig. 2.5 and Fig. 2.6 shows the outer-loop gain, which determines the system's phase margin and bandwidth for different values of L_o and C_o along with the nominal values for which the compensator has been designed originally. It can be seen that the change in L_o have no effect on the outer-loop gain. This is because with peak-current-mode control the converter acts as a controlled current source [29]. However, with decreases in C_o its phase margin decreases and its

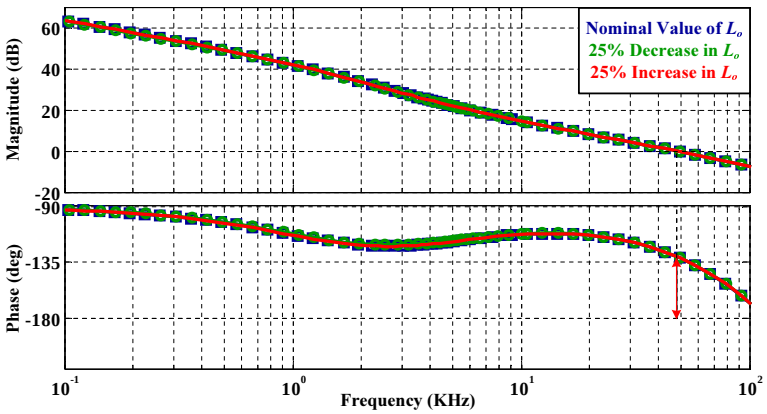


Figure 2.5: Outer-loop gain with peak-current-mode control for different values of L_o.

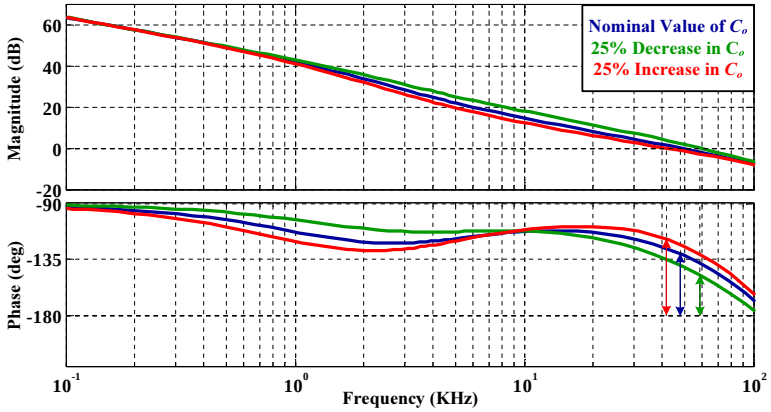


Figure 2.6: Outer-loop gain with peak-current-mode control for different values of C_o.

crossover frequency increases, hence the converter has the tendency to become unstable with a reduction in C_o and a fixed compensator.

2.3 Autotuning Control Methods for Power Converter

From the analysis in the previous section, it can be concluded that in order to maintain a stable transient response performance and unconditionally stable system over wide-range variations of power-stage parameters, the coefficients of the digital controller should be adjusted regularly according to the variations in power-stage component values. An autotuning controller that adjusts its coefficient to compensate for the variations in power-stage component values are widely employed to maintain a stable transient response performance and unconditionally stable system over wide-range variations of power-stage parameters. The autotuning controller for power converters can be broadly classified into two categories: parametric and non-parametric autotuning controller [30, 31]. For parametric approach, the values of the power converter's power-stage are estimated, and the controller coefficient is adjusted accordingly. While for non-parametric

approach the frequency response of the power converter is measured online and the controller is adjusted based on the measured frequency response to obtain the desired phase margin and crossover frequency [32].

2.3.1 Non-Parametric Digital Autotuning Controller

A non-parametric approach for online system identification based on cross-correlation method is presented and successfully applied to a forward converter in [33, 34]. A pseudo-random binary signal (PRBS) is digitally generated using a shift register and is injected as a perturbation into the system through its control input. The impulse response of the converter is then obtained by cross-correlation of the input signal and the converter output. The obtained impulse response of the converter is then converted into frequency response using a Discrete Fourier Transform (DFT). Based on the obtained frequency response data, frequency domain analysis can be used to design a suitable feedback controller. However, there are specific limitations of the proposed method: the controller needs to process a large amount of data which will require a significant amount of time and memory; the converter needs to operate in open-loop during the identification phase as such the method is not suitable for continuous controller tuning; the fidelity of system identification significantly depends on the ADC quantization effect and switching noise.

In [35] pre-emphasis and de-emphasis filters are introduced to improve the accuracy and reduce the effect of noise on the cross-correlation based system identification method. The generated PRBS data is passed through a pre-emphasis filter before injecting it into the system while the output of the converter is passed through a de-emphasis filter. In [36] a window function is applied to the data obtained from the cross-correlation of the input signal and the converter's output voltage to remove high frequency noise from it. This results in an improved

accuracy of the control-to-output voltage transfer function especially at high frequency. The achieved accuracy and removal of the high frequency noise depend on the selection of the width of the window function. In [37, 38] other types of signals are used as the perturbation signal instead of the PRBS to further improve the accuracy of the cross-correlation based system identification method. In [37] a discrete-interval binary signal (DIBS) is used as perturbation signal while in [38] inverse-repeat binary sequence (DRBS) is used as perturbation signal as these signals are less sensitive to distortion and noise and will result in an improved accuracy in noisy systems.

An autotuning controller based on online frequency-response measurement is presented in [39]. During identification phase, the output of the controller is held at its steady-state value and a signal is injected into the digital pulse-width modulator (DPWM) in addition to the controller's output. With the help of an identification block the open-loop frequency response of the converter is measured and stored in memory. Autotuning algorithm is then used to tune the controller for the desired crossover frequency and phase margin. In [40, 41], autotuning of controller is performed by continuous monitoring of the system's crossover frequency and phase margin. A small digital square wave is injected into the feedback loop and error signals are generated by subtracting the measured bandwidth and phase margin from the desired bandwidth and phase margin. Based on these error signals, a multi-input-multi-output controller is used to tune the coefficients of the digital PID compensator to nullify the errors. With signal injection into control loop, this method inevitably causes perturbations to the output voltage and affects load regulation. Moreover, the method is relatively complex as additional hardware resources including variable frequency signal generator, band-pass filters, multi-input-multi-output (MIMO) controller are required to map error signals to PID compensator's coefficients.

A model reference autotuning controller is presented in [42, 43]. In [42] the

model reference and the actual system are simultaneously perturbed through the application of a common excitation waveform and their outputs are compared to yield the tuning error. By means of a tuning algorithm the compensator's coefficients are adjusted until the tuning error is reduced to zero. In [43] the impulse response of the actual system is measured online then an error signal is generated by subtracting the measured impulse response from a reference impulse response. Based on the generated error signal the coefficient of the digital controller are altered in such away that the error signal is reduced to zero. In [44] an adaptive proportional derivative plus integral (PD+I) control method has been proposed and successfully applied to a buck converter. The proposed method consists of an adaptive PD controller plus a non-adaptive integral controller. The adaptive PD controller is implemented using finite impulse response (FIR) predictive error filter. A DCD-RLS algorithm is used to adjust the coefficient of the FIR filter in such away that the error converges to zero rapidly.

A gain-scheduling control scheme based on inductor current is presented in [45]. In the proposed method, linear controllers for different converter's operating points are designed offline and stored in a lookup table, and a particular set of controller coefficients are subsequently selected according to the sensed inductor current for a given operating point. An online closed-loop autotuning digital controller is presented in [46]. The presented method is based on tuning the closed loop controller parameters by observing the time-domain characteristics of the compensated error signal. A larger peak-to-peak value of the compensated error signal corresponds to a larger bandwidth. Thus, the parameters of the compensator such as gain, poles or zeros are altered in a direction that will increase the peak-to-peak amplitude of the compensated error signal.

2.3.2 Parametric Digital Autotuning Controller

A relay feedback based method for online estimation of power-stage parameters and autotuning of a feedback controller is presented in [47–49]. In the proposed method, a non-linear relay is introduced in the feedback loop. During the identification phase the non-linear relay causes the converter's output voltage to oscillate at the system's resonant frequency. Thus the zeros of the compensator are placed at the resonance frequency of the converter. Subsequently the poles and gain of the compensator is adjusted using iterative procedure to obtain the desired phase margin and crossover frequency. However, the proposed method causes the converter's output voltage to oscillate during the identification phase thus disturbing the converter's normal operation. Additionally, the poles and gain of the compensator is adjusted using an iterative procedure thus the complete identification and autotuning process require a significant amount of time. The complete identification and autotuning process takes approximately 27 ms at a sampling frequency of 200 kHz [49].

Instead of using a non-linear relay in the feedback loop, a limit-cycle-oscillations-based method for online estimation of power-stage parameters and autotuning of a feedback controller is proposed in [50, 51]. In the proposed method, oscillations known as limit-cycle-oscillations are introduced in the converter's output voltage by reducing the resolution of the DPWM as compared to the resolution of the ADC. The converter's parameters such as output filter resonant frequency and quality factor are then estimated by examining the amplitude and frequency of the intentionally introduced limit-cycle-oscillations. Once the converter's parameters are estimated a pole-zero cancellation method is adopted to tune the compensator's coefficients for achieving the desired crossover frequency and phase margin. The main drawback of this method is that it is based on intentionally introduced limit-cycle oscillations, which will affect the converter's normal op-

eration and output-voltage regulation during the identification and autotuning phase.

In [52], a time-domain method for estimating the open loop control-to-output voltage transfer function is proposed. In the proposed method, the system is perturbed by introducing a step change in the duty cycle. To improve the accuracy of the proposed method, the same step change in the duty cycle is applied for at least five times. The average input and output data is then collected and an iterative least square algorithm is applied to estimate the open-loop control-to-output voltage transfer function of the converter. However, there is a limitation of the proposed method. Any step change in the duty cycle will result in a change in the output voltage thus changing the converter's operating point.

Hammerstein model based black box modeling of dc-dc converter is presented in [53, 54]. The assumed Hammerstein-type mathematical model for the dc-dc converter consists of a static nonlinear model and a linear time-invariant (LTI) model. The model identification is a two-step procedure. In the first step the converter is supplied with a fixed input voltage and a variable duty cycle. The obtained input and output data for this operating mode is then utilized to obtain the static nonlinear model of the converter. In the second step the duty cycle is perturbed with a PRBS signal and the obtained input and output data for this operating mode is then utilized to obtain the LTI model of the converter. The proposed method will result in an improved model of the dc-dc converter as compared to conventional small-signal model. However, the proposed method is relatively complicated and not suitable for low-cost DSP implementation. A black box modeling approach based on analyzing the converter's transient response is presented in [55, 56]. A step change in load is introduced and the resulting dynamic response of the converter is captured. A Least square algorithm is then used to obtain the coefficients of the LTI system transfer function.

A method for estimating the parameters of converter is presented in [57–

59], which does not require any current sensor. In the proposed method, the conventional analog RC filter, used for lossless inductor current sensing is replaced by a first-order digital filter. During a short period of calibration phase a small precise current sink, connected in parallel to the load is activated. Then the gain and time constant of the digital filter are adjusted such that any change in load current exactly correspond to the change in the measured inductor current. The estimated parameters can be then used to autotune the digital controller. A non-intrusive, current-sensorless method for online identification of output capacitor's ESR and C_o is proposed in [60–63]. The values of ESR and C_o are estimated by sampling the output voltage twice in a switching period and using the information of steady-state duty cycle and sampling frequency from the digital pulse width modulator.

2.4 Conclusion

In this chapter, the influences of variations in the power-stage parameters on converter's loop-gain are investigated. From the analysis, it can be concluded that in the presence of variations in power-stage components values and fixed controller the crossover frequency and phase margin of converter changes, which could degrade the converter's transient response and its stability. To address this issue, various non-parametric and parametric autotuning control methods have been proposed in the literature. For non-parametric autotuning control methods, the frequency response of power converter is measured online and used to tune the feedback controller. However, these methods are relatively complicated as the DSP needs to process a large amount of data and as such is not suitable for low-cost DSP implementation. For parametric approach, converter's power-stage component values are estimated, and pole-zero cancellation method is applied to tune the feedback controller. The parametric methods are relatively easy to

implement. However, most of the presented methods are based on trial-and-error approach, or it is assumed that at least some of the converter's parameters are known with high precision and does not change over time.

Chapter 3

A Non-Intrusive Parameter Estimation Method for Autotuned DC-DC Converter Based on Quasi-Impulse Response

3.1 Introduction

In Chapter 2, various autotuning control methods for dc-dc converters have been reviewed to maintain consistent dynamic response performance and stability of converter despite variations in the converter's power-stage parameters. However, it is observed that with non-parametric autotuning methods the digital controller needs to process a large amount of data and as such these methods are relatively complicated and usually require a high-performance DSP for their implementation. In contrast, parametric autotuning control methods are rela-

tively easy to implement and are more suitable for low-cost DSP implementation. However, most of these methods are based on trial-and-error approach, or it is assumed that at least some of the converter power-stage parameters are known with high precision and does not change over time.

To address these limitations, a new method for online estimation of power-stage parameters along with a controller that can be autotuned is proposed in this chapter. With the proposed method, the resonant frequency ω_o and ESR zero frequency ω_{ESR} are estimated by analyzing the converter's quasi-impulse response during start-up transient and online measurement of steady-state output voltage ripple. Based on these estimated parameters, the coefficients of the digital controller are tuned to maintain constant crossover frequency and phase margin irrespective of variations in power-stage parameters. As a result, the proposed method offers the advantage of being free from trial-and-error and non-intrusive, hence it does not disturb the converter's normal operation. Moreover, the proposed method is hardware efficient since no additional hardware such as voltage and current sensors are required and can be implemented on a low-cost microcontroller.

3.2 Estimation of Power-Stage Parameters

The schematic diagram of the proposed autotuning digital compensator for voltage-mode and peak-current-mode control are shown in Fig. 3.1 and Fig. 3.2, respectively. The complete system consists of a power-stage, an identification block and an autotuning digital compensator. The identification block is used to perform online estimation of the resonant frequency of the output filter and ESR zero frequency of the output capacitor. It uses the digital values of the sampling frequency f_s, steady-state duty cycle D and output voltage v_o, and in the case of peak-current-mode control, the additional input is the sensed inductor current.

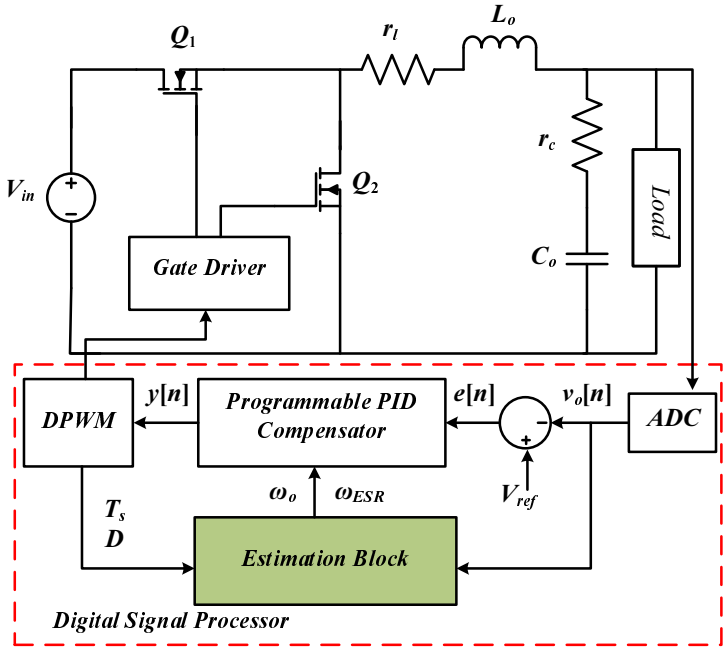


Figure 3.1: Digital voltage-mode-controlled buck converter with estimation block.

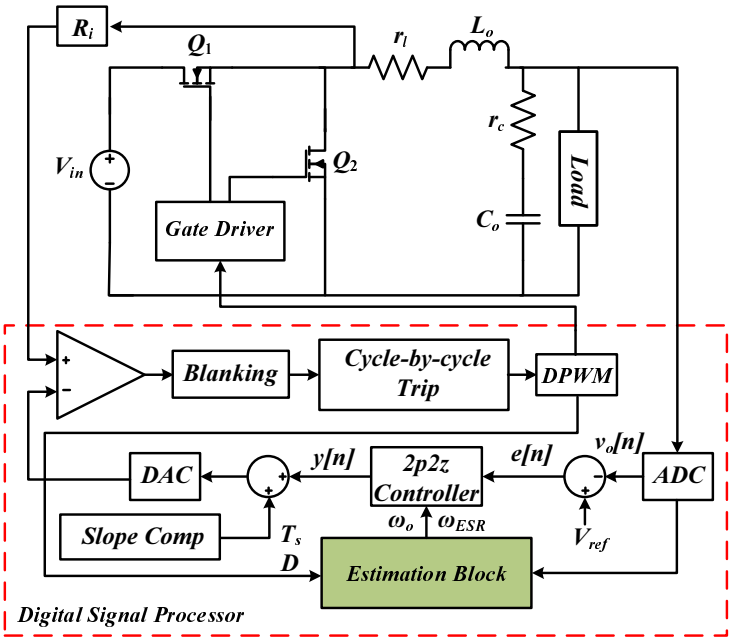


Figure 3.2: Digital peak-current-mode-controlled buck converter with estimation block.

In this work, the resonant frequency ω_o and ESR zero frequency ω_{ESR} are estimated by analyzing the converter's quasi-impulse response during startup and the measured output voltage ripple during steady-state operation, respectively.

The controller's coefficients are then adjusted accordingly to maintain a constant closed-loop bandwidth and phase margin of the converter over wide-range variations of L_o, C_o and ESR.

3.2.1 Resonant Frequency ω_o Estimation

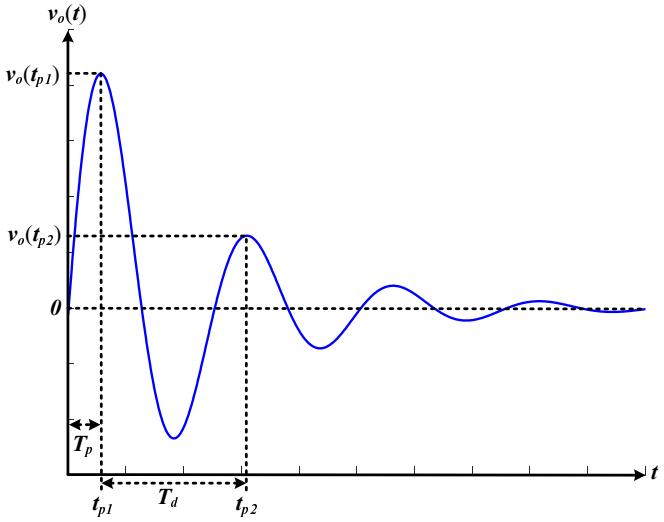
The resonant frequency ω_o of the L_oC_o output filter is estimated by analyzing the converter's response to a short rectangular pulse as a means to emulate the converter's open-loop impulse response. During the estimation phase, the main switch Q_1 is closed to provide a short pulse to the buck converter. The converter's output voltage response to a short pulse is shown in Fig. 3.3, similar to a second-order system [115]. The peak value of the output voltage can be adjusted by changing the on-time of the main switch in order to keep it within a predefined band to avoid excessive voltage stress on the load and to prevent unintentional triggering of over-voltage protection circuit. This approach has significant advantage compared to step excitation which subjects the load to a voltage significantly higher than the nominal value. Fig. 3.3c shows the quasi-impulse response of an underdamped buck converter's power-stage for different values of pulse width.

Underdamped response

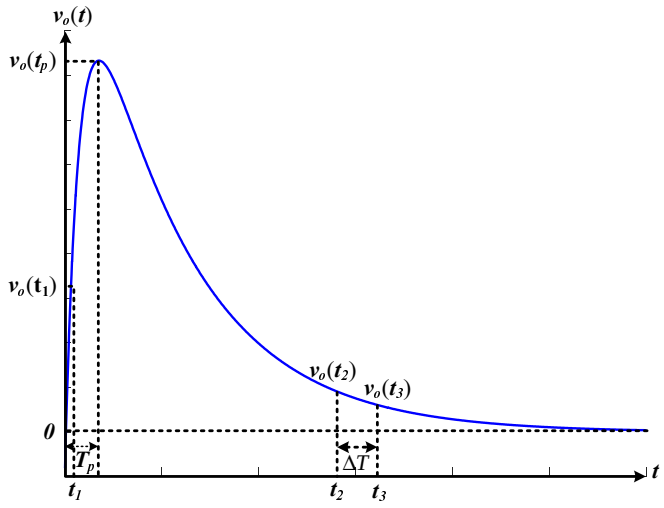
The response of an underdamped second-order system excited by short rectangular pulse of duration T_w is given by equation (3.1) and is shown in Fig. 3.3a.

$$v_o(t) = \frac{A_m e^{-\zeta\omega_o t}}{\sqrt{1-\zeta^2}} \Big[e^{-\zeta\omega_o T_w} \sin\left(\omega_o\sqrt{1-\zeta^2}\,(t-T_w)+\phi\right) - \sin\left(\omega_o\sqrt{1-\zeta^2}t+\phi\right)\Big] \quad (3.1)$$

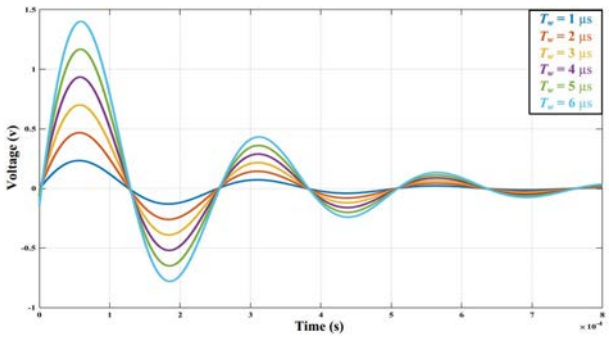
where A_m is the amplitude of input voltage, T_w is the main switch on-time, ω_o



(a)



(b)



(c)

Figure 3.3: (a) Underdamped (b) overdamped response of buck converter excited by short rectangular pulse and (c) quasi-impulse response of an underdamped buck converter's power-stage for different values of pulse width.

is the resonance frequency, ζ is the damping ratio and $\phi = \arccos(\zeta)$. Equation (3.1) can be simplified to equation (3.2), which implies that the response of a buck converter to short rectangular pulse is a scaled and phase shifted version of its impulse response.

$$v_o(t) = \frac{C\omega_o}{\sqrt{1-\zeta^2}} e^{-\zeta\omega_o t} \sin\left(\omega_o\sqrt{1-\zeta^2}t - \phi^{'}\right) \tag{3.2}$$

where C is a scaling constant and $\phi^{'}$ is given by equation (3.3).

$$\phi^{'} = \arctan\left[\frac{e^{\zeta\omega_o T_w}\sqrt{1-\zeta^2}\cos\left(\omega_o\sqrt{1-\zeta^2}T_w\right)}{e^{\zeta\omega_o T_w}\zeta\cos\left(\omega_o\sqrt{1-\zeta^2}T_w\right)} \frac{-e^{\zeta\omega_o T_w}\zeta sin\left(\omega_o\sqrt{1-\zeta^2}T_w\right) - \sqrt{1-\zeta^2}}{+e^{\zeta\omega_o T_w}\sqrt{1-\zeta^2}\sin\left(\omega_o\sqrt{1-\zeta^2}T_w\right) - \zeta}\right] \tag{3.3}$$

At peak time t=T_p, the derivative of the output voltage is zero. Hence,

$$0 = \cos\left(\omega_o\sqrt{1-\zeta^2}T_p - \phi^{'}\right) - \frac{\zeta\sin\left(\omega_o\sqrt{1-\zeta^2}T_p - \phi^{'}\right)}{\sqrt{1-\zeta^2}} \tag{3.4}$$

Solving for ω_o gives

$$\omega_o = \frac{\arccos(\zeta) + \phi^{'}}{T_p\sqrt{1-\zeta^2}} \tag{3.5}$$

For small pulse width T_w, $\phi^{'}$ is typically very small. Hence equation (3.5) can be approximated by equation (3.6)

$$\omega_o \approx \frac{\arccos(\zeta)}{T_p\sqrt{1-\zeta^2}} \tag{3.6}$$

$$\zeta = \frac{\ln\left(\frac{v_o(t_{p1})}{v_o(t_{p2})}\right)}{\sqrt{4\pi^2 + \left[\ln\left(\frac{v_o(t_{p1})}{v_o(t_{p2})}\right)\right]^2}} \tag{3.7}$$

Thus by measuring the ratio between two successive peaks and the time of the first output voltage peak T_p, the damping ratio and the resonance frequency of the L_oC_o output filter can be estimated using equation (3.7) and equation (3.6).

Overdamped response

The overdamped response is a superposition of two exponentially decaying functions as given by equation (3.8) and is shown in Fig. 3.3b.

$$v_o(t) = \frac{A_m\omega_o}{2\sqrt{\zeta^2-1}}\left[\frac{\left(1-e^{P_2T_w}\right)e^{-P_2t}}{P_2} - \frac{\left(1-e^{P_1T_w}\right)e^{-P_1t}}{P_1}\right] \tag{3.8}$$

where A_m is the amplitude of the excitation pulse, T_w is the main switch on-time, ω_o is the resonance frequency, ζ is the damping ratio, $P_1 = \zeta\omega_o + \omega_o\sqrt{\zeta^2-1}$ and $P_2 = \zeta\omega_o - \omega_o\sqrt{\zeta^2-1}$

Equation (3.8) can be written as equation (3.9), which implies that the response of a buck converter to a short rectangular pulse is a scaled version of its impulse response.

$$v_o(t) = \frac{C\omega_o}{2\sqrt{\zeta^2-1}}\left[e^{-P_2t} - e^{-P_1t}\right] \tag{3.9}$$

Since $P_1 > P_2$, the voltage response is dominated by P_2 near steady-state, i.e. $t >> T_p$. Hence equation (3.9) can be approximated by equation (3.10)

$$v_o(t) = \frac{C\omega_o}{2\sqrt{\zeta^2-1}}e^{-P_2t} \tag{3.10}$$

Hence, the output voltage at time t_2 and t_3 can be approximated by equation (3.11) and equation (3.12) respectively.

$$v_o(t_2) = \frac{C\omega_o}{2\sqrt{\zeta^2 - 1}} e^{-P_2 t_2} \tag{3.11}$$

$$v_o(t_3) = \frac{C\omega_o}{2\sqrt{\zeta^2 - 1}} e^{-P_2 t_3} \tag{3.12}$$

Dividing equation (3.11) by equation (3.12) and solving for P_2 gives

$$P_2 = \frac{1}{t_3 - t_2} \ln \left[\frac{v_o(t_2)}{v_o(t_3)} \right] \tag{3.13}$$

At t=t_1 the output voltage is given by

$$v_o(t_1) = \frac{C\omega_o}{2\sqrt{\zeta^2 - 1}} \left[e^{-P_2 t_1} - e^{-P_1 t_1} \right] \tag{3.14}$$

Solving for P_1 gives

$$P_1 = -\frac{1}{t_1} \ln \left[e^{-P_2 t_1} - \frac{v_o(t_1)}{A} \right] \tag{3.15}$$

where $A = \frac{C\omega_o}{2\sqrt{\zeta^2-1}} = \frac{v_o(t_2)}{e^{-P_2 t_2}}$

At peak time t=T_p, the derivative of equation (3.9) is zero.

$$0 = P_1 e^{-P_1 T_p} - P_2 e^{-P_2 T_p} \tag{3.16}$$

Substituting the values P_1 and P_2 and solving for ω_o gives

$$\omega_o = \frac{\ln \left[\frac{\zeta + \sqrt{\zeta^2-1}}{\zeta - \sqrt{\zeta^2-1}} \right]}{2T_p \sqrt{\zeta^2 - 2}} \tag{3.17}$$

$$\zeta = \frac{P_1 + P_2}{2\sqrt{P_1 P_2}} \tag{3.18}$$

The data points $v_o(t_2)$ and $v_o(t_3)$, given by 2% of $v_o(t_p)$ and 1% of $v_o(t_p)$

respectively, are used to calculate P_2, while the data point $v_o(t_1)$ selected close to the main switch-off time is used to calculate P_1. The resonance frequency ω_o and the damping ratio ζ is then given by equation (3.17) and equation (3.18), respectively.

In practical implementation, the system is considered to be underdamped if their exists multiple peaks. On the contrary, the system is considered to be overdamped if the output voltage settles to zero after the first peak.

The continuous sampling of the converter's output voltage is used to detect the output voltage peaks. The value $v_o[n-1]$ just before the sign change of $\Delta v_o[n]$ is regarded as peak, while data points $v_o(t_2)$ and $v_o(t_3)$ are sampled at 2% and 1% of $v_o(t_p)$ respectively.

$$\Delta v_0 = v_o[n] - v_o[n-1] \tag{3.19}$$

A timer, which increments at the clock frequency and is independent of the number of instructions is used to measure the time t_1, t_2, t_3 and the peak time T_p. At time $t = 0$, when the main switch is closed, the timer is started. The time t_1 is selected close to the main switch off-time. The detection of sign change from positive to negative of Δv_o gives the peak time T_p, while the time t_2 and t_3 is given by the time at which the output voltage reaches to 2% and 1% of $v_o(t_p)$, respectively.

3.2.2 ESR Zero Frequency ω_{ESR} Estimation

The measured steady-state output voltage ripple and the estimated resonant frequency ω_o are used to estimate the output capacitor's time constant. Equation (3.20) represents the total output voltage ripple of a buck converter.

$$\Delta V_{rip} = \Delta V_{r_c} + \Delta V_c \tag{3.20}$$

where ΔV_{r_c} is the component of the output voltage ripple developed across the ESR. ΔV_c is the contribution to the output voltage ripple due to variation in the stored charge of the output capacitor. The ratio of the two the output voltage ripple components can be given by (3.21).

$$\frac{\Delta V_{r_c}}{\Delta V_c} = 8 f_s r_c \times C_o = \frac{4 f_s}{\pi f_{ESR}} \tag{3.21}$$

From equation (3.21) the ratio $\frac{\Delta V_{r_C}}{\Delta V_c}$ will be larger than 1, provided that the switching frequency is considerably higher than f_{ESR}. Thus the peak-to-peak output voltage ripple is dominated by the output capacitor's ESR. This condition is easily satisfied in dc-dc converters, in which high switching frequency is typically used in order to achieve high power density and reduce the size of passive components. When the contribution of ESR to the peak-to-peak output voltage ripple is significantly larger compared to that due to variation in stored charge, equation (3.20) can be approximated by equation (3.22).

$$\Delta V_{rip} \approx \Delta V_{r_c} \tag{3.22}$$

Therefore, the time constant of the output capacitor's ESR zero can be given by (3.23). Furthermore, for peak-current-mode control the individual values of L_o and C_o can be calculated from the inductor current ripple information ΔI_L and the estimated resonance frequency ω_o as given by equation (3.24) and equation (3.25) respectively.

$$\omega_{ESR} = \frac{1}{r_c \times C_o} = \frac{V_o \omega_o^2 (1 - D) T_s}{\Delta V_{rip}} \tag{3.23}$$

$$L_o = \frac{V_o (1 - D)}{\Delta I_L f_s} \tag{3.24}$$

$$C_o = \frac{1}{\omega_o^2 L_o} \tag{3.25}$$

In DSP, the inductor current ripple and output voltage ripple information is obtained by capturing the sensed inductor current and the output voltage twice in a switching period as shown in Fig. 3.4. The internal trigger of the DPWM module is used to trigger the ADC when the counter is equal to zero, and when the counter is equal to DT_s. During the identification phase the switching frequency of the converter can be temporarily reduced for converters operating at high switching frequency, or for systems that do not have high sampling rate ADC. Fig. 3.5 shows the implementation flowchart of the entire system.

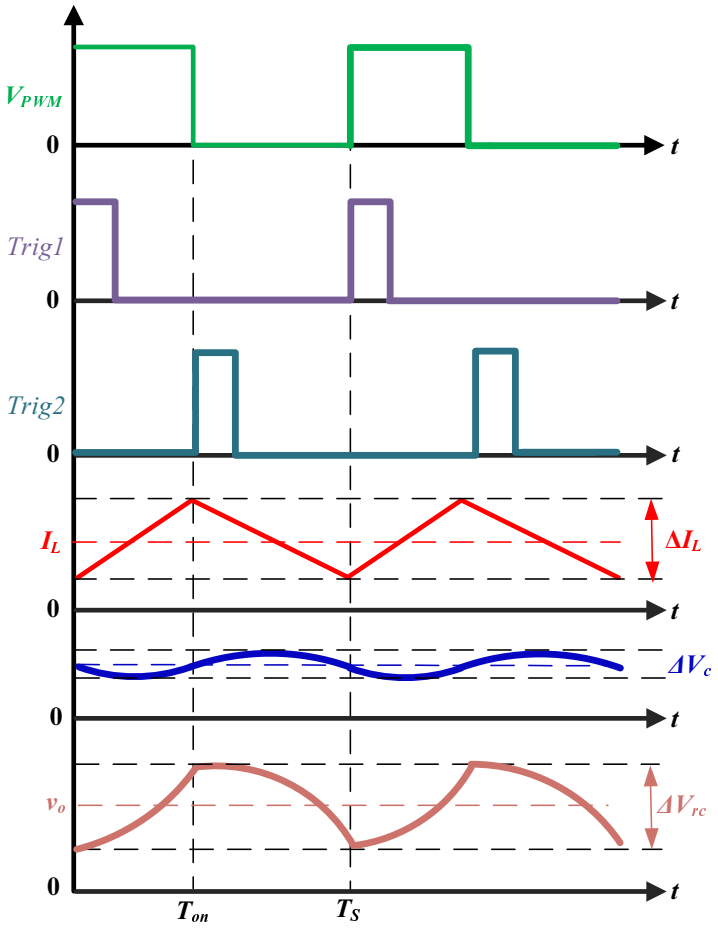


Figure 3.4: Output voltage and inductor current ripple measurement.

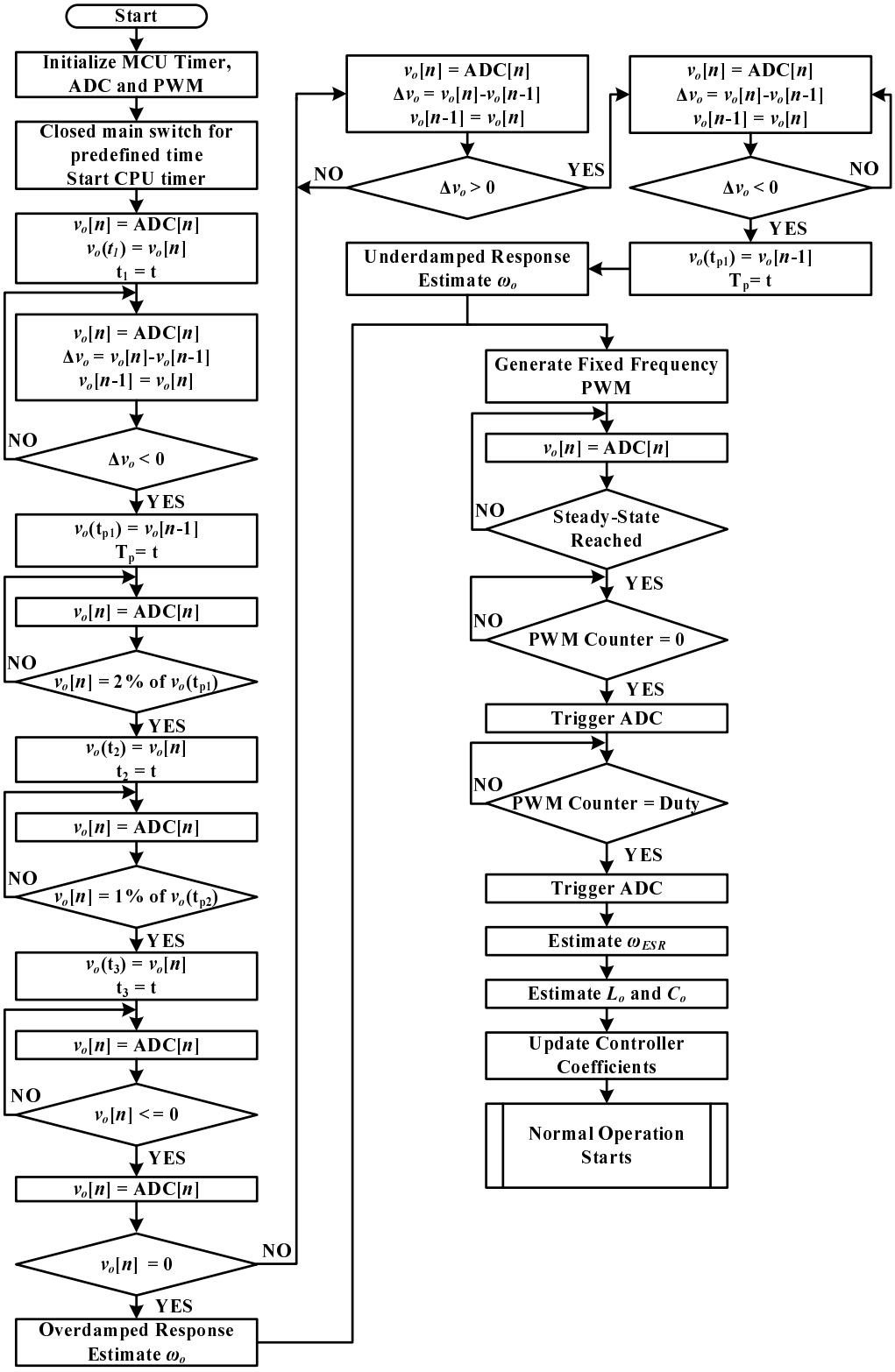


Figure 3.5: Flowchart representing the implementation of the autotuning controller with parameter estimation.

Table 3.1: Vales of L_o and C_o for three different power-stages

	Power− Stage 1 (reference)	Power− Stage 2	Power− Stage 3
$L_o(\mu\text{H})$	1.2	1.2	0.8
$C_o(\text{mF})$	1.1	0.81	1.1

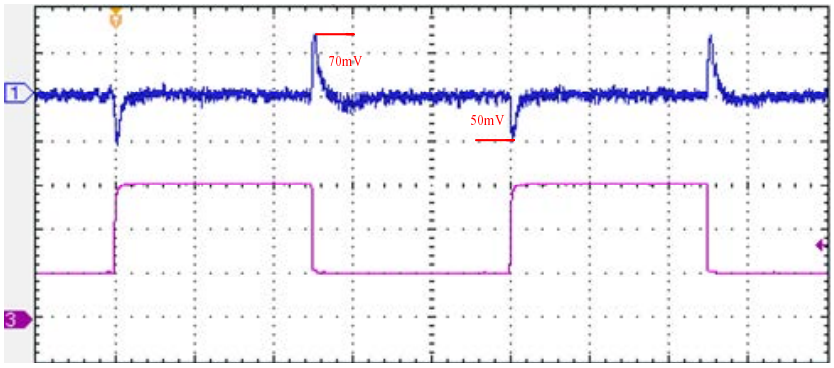
3.3 Experimental Results

The proposed autotuning algorithm has been applied to three different synchronous buck converter configurations with different power-stage component values . The specifications of the converter are input voltage of 12 V, output voltage of 1.5 V and output current of 15 A. The different values of the L_oC_o output filter for the three power-stages are given in Table 3.1. A digital fixed voltage-mode and peak-current-mode controller was designed using the nominal power-stage parameter values. Digital signal processor (TMS320F28377S) was used to implement the digital controller. For all cases, the load current's slew rate is 1.7 A/μs for step-up and 50 A/μs for step-down.

3.3.1 Voltage-Mode Control

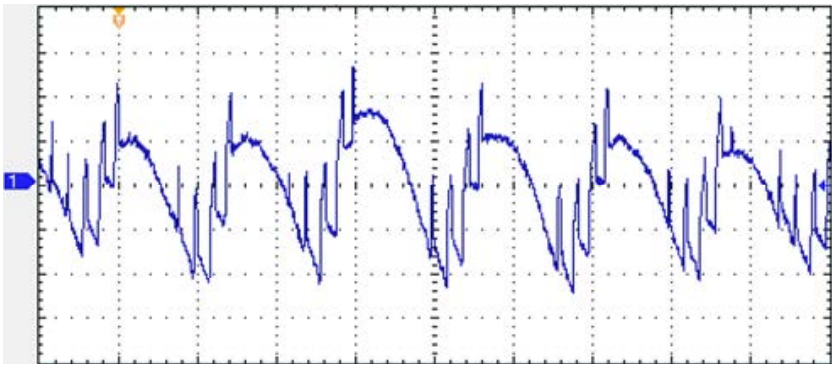
The dynamic response of the converter with the designed digital controller under step load changes is shown in Fig. 3.6. It can be observed that the converter is stable and the peak-to-peak overshoot is 120 mV for a load current step of 5A $\leftrightarrow$ 15A. For the case of fixed controller and reduced values of L_o and C_o, the results are given in Fig. 3.7 and Fig. 3.8 respectively. The waveform of the output voltage shows that the converter has become unstable due to reduced phase margin and increased crossover frequency.

With the proposed autotuning controller, the startup transient is used to determine the the resonant frequency ω_o of the output filter by calculating the



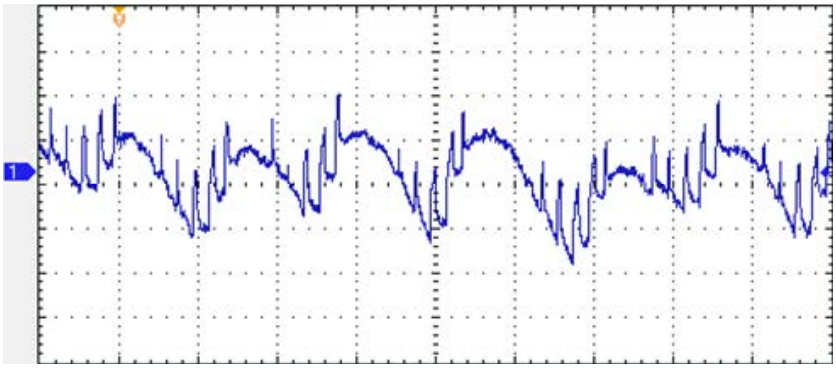
Time: 200µs/Div.
Top Trace (Output Voltage, AC Coupled): 50mV/Div.
Bottom Trace (Load Current): 5A/Div.

Figure 3.6: Measured transient response of the power converter during a load transient of 5A $\leftrightarrow$ 15A with fixed voltage-mode controller and nominal values of L_o and C_o.



Time: 10µs/Div.
Output Voltage, AC Coupled: 20mV/Div.

Figure 3.7: Measured steady-state output voltage waveform with $L_o = 0.8$ μH and fixed voltage-mode controller.



Time: 10µs/Div.
Output Voltage, AC Coupled: 20mV/Div.

Figure 3.8: Measured steady-state output voltage waveform with $C_o = 0.81$ mF and fixed voltage-mode controller.

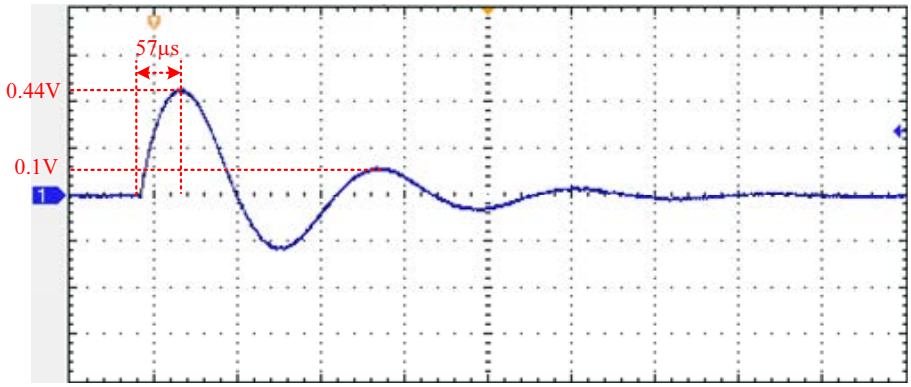
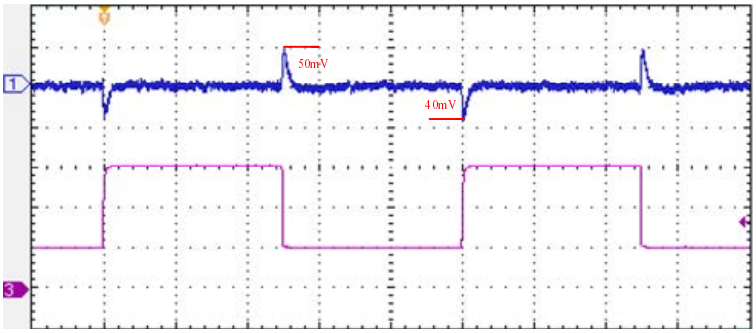


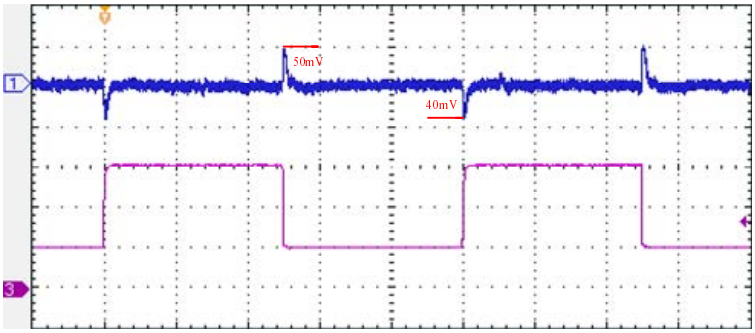
Figure 3.9: Measured start-up transient of buck converter.

time of the initial output voltage peak T_p and the ratio between two successive peaks as shown in Fig. 3.9. Using the measured output steady-state voltage ripple and the calculated ω_o, the ESR zero frequency is calculated. The coefficients of the digital controller are tuned on the basis of the estimated ω_o and ω_{ESR} in order to achieve the desired crossover frequency. Using $L_o = 1.2$ μH, $C_o = 1.1$ mF and autotuning controller, the dynamic response of the converter is shown in Fig. 3.10. The maximum peak-to-peak overshoot has been reduced from 120 mV to 90 mV with the proposed autotuning controller. The dynamic response of the converter with the autotuning controller and reduced values of L_o and C_o are shown in Fig. 3.11 and Fig. 3.12. It is evident from the results that the autotuning controller makes the operation of the converter stable for all three cases irrespective of variations in power-stage parameters. The settling time and maximum peak-to-peak overshoot are similar for all three cases; however there is a slight increase in the output voltage ripple with decreases in output filter component values. The autotuning controller ensures fixed phase margin and crossover frequency with variations in power-stage component values.



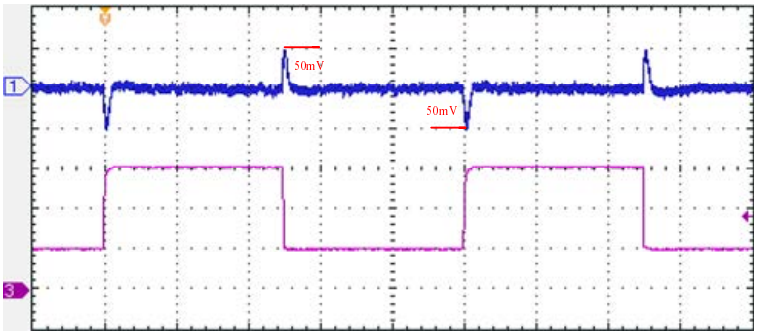
Time: 200µs/Div.
Top Trace (Output Voltage, AC Coupled): 50mV/Div.
Bottom Trace (Load Current): 5A/Div.

Figure 3.10: Measured transient response of the power converter during a load transient of 5A $\leftrightarrow$ 15A with autotuning voltage-mode controller and nominal values of L_o and C_o.



Time: 200µs/Div.
Top Trace (Output Voltage, AC Coupled): 50mV/Div.
Bottom Trace (Load Current): 5A/Div.

Figure 3.11: Measured transient response of the power converter during a load transient of 5A $\leftrightarrow$ 15A with $L_o = 0.8\ \mu$H and autotuning voltage-mode controller.

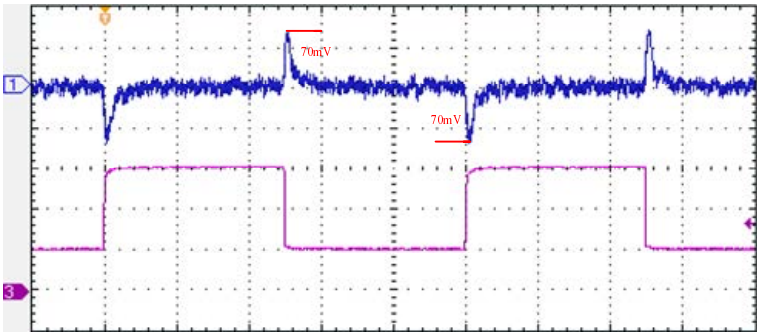


Time: 200µs/Div.
Top Trace (Output Voltage, AC Coupled): 50mV/Div.
Bottom Trace (Load Current): 5A/Div.

Figure 3.12: Measured transient response of the power converter during a load transient of 5A $\leftrightarrow$ 15A with $C_o = 0.81$ mF and autotuning voltage-mode controller.

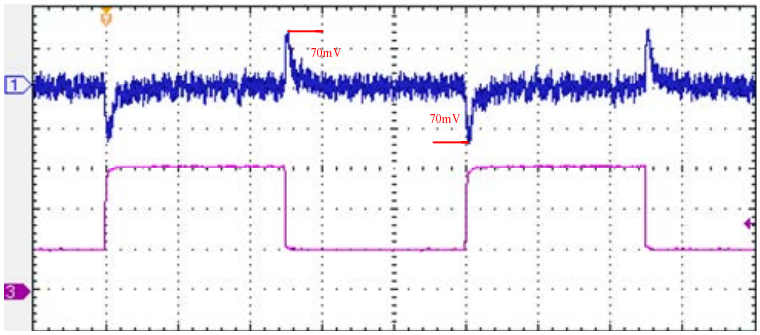
3.3.2 Peak-Current-Mode Control

For peak-current-mode control using $L_o = 0.8$ μH, 1.2 μH and a load current step of 5A $\leftrightarrow$ 15A, the transient response of the buck converter with a fixed controller is shown in Fig. 3.13 and Fig. 3.14. It is clear from the results that the converter is stable for both cases with approximately the same maximum peak-to-peak overshoot. For the case of a decrease in the value of C_o and fixed controller, the result of the transient response is given in Fig. 3.15. It is evident from the result that for fixed peak-current-mode control, a reduced value of C_o makes the converter unstable, and a degraded phase margin accounts for this instability. For an autotuning peak-current-mode controller, the dynamic response of the converter with nominal values of L_o and C_o is shown in Fig. 3.16. The peak-to-peak overshoot has been reduced from 140 mV to 120 mV with the proposed autotuning controller. Fig. 3.17 and Fig. 3.18 illustrates the converter's response with the autotuning controller and reduced L_o, C_o values. With the autotuning controller, the converter is stable for a similar decrease in C_o. This is because the coefficients of the autotuning controller are updated in accordance with the estimated power-stage component values. Table 3.2 and Table 3.3 enlists the measured and estimated values of resonant frequency ω_o and ESR zero frequency



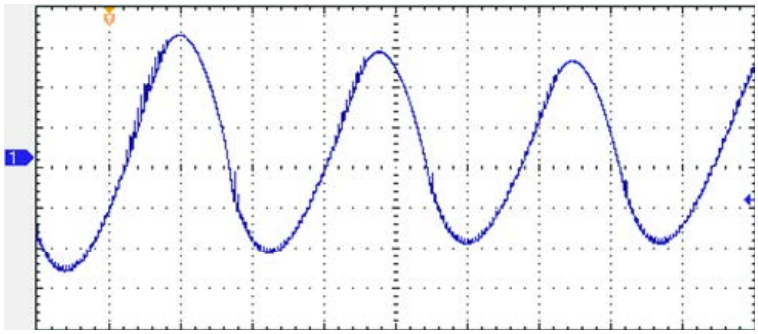
Time: 200µs/Div.
Top Trace (Output Voltage, AC Coupled): 50mV/Div.
Bottom Trace (Load Current): 5A/Div.

Figure 3.13: Measured transient response of the power converter during a load transient of 5A $\leftrightarrow$ 15A with fixed peak-current-mode controller and nominal values of L_o and C_o.



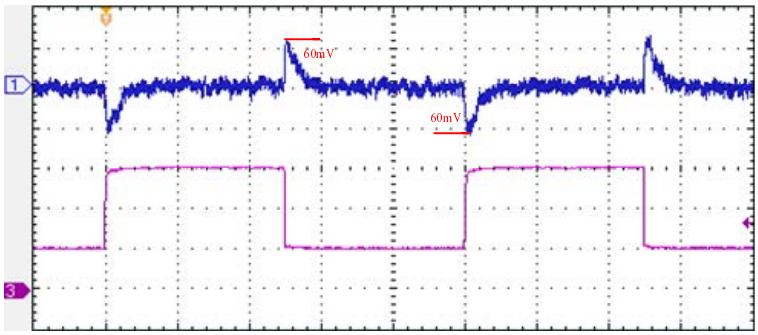
Time: 200µs/Div.
Top Trace (Output Voltage, AC Coupled): 50mV/Div.
Bottom Trace (Load Current): 5A/Div.

Figure 3.14: Measured transient response of the power converter during a load transient of 5A $\leftrightarrow$ 15A with $L_o = 0.8$ μH and fixed peak-current-mode controller.



Time: 40µs/Div.
Output Voltage, AC Coupled: 200mV/Div.

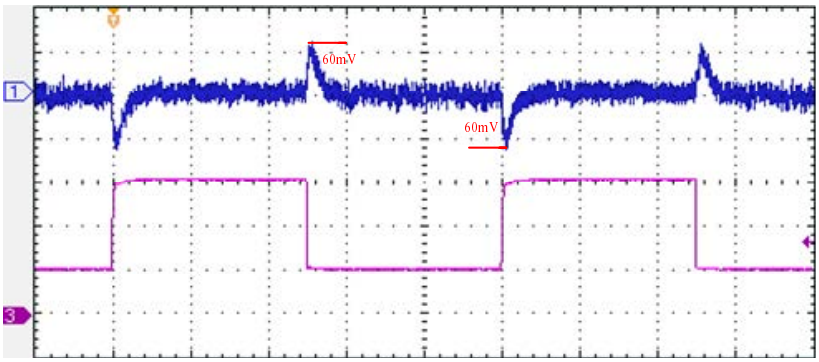
Figure 3.15: Measured steady-state output voltage waveform with $C_o = 0.81$ mF and fixed peak-current-mode controller.



Time: 200µs/Div.
Top Trace (Output Voltage, AC Coupled): 50mV/Div.
Bottom Trace (Load Current): 5A/Div.

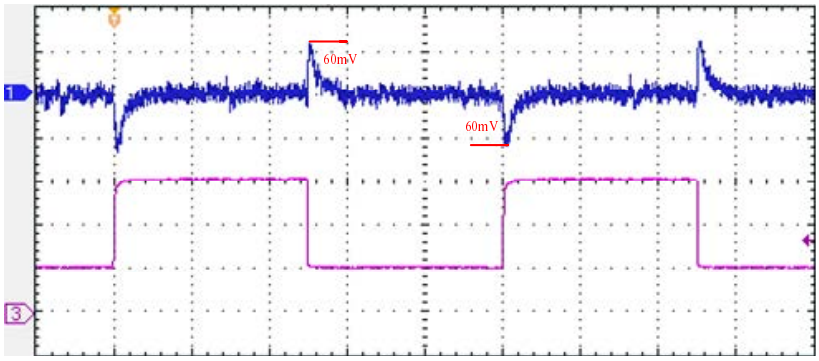
Figure 3.16: Measured transient response of the power converter during a load transient of 5A $\leftrightarrow$ 15A with autotuning peak-current-mode controller and nominal values of L_o and C_o.

ω_{ESR} for the three power-stages investigated. The percentage of error between the measured and estimated values is less than 5% in all cases.



Time: 200µs/Div.
Top Trace (Output Voltage, AC Coupled): 50mV/Div.
Bottom Trace (Load Current): 5A/Div.

Figure 3.17: Measured transient response of the power converter during a load transient of 5A $\leftrightarrow$ 15A with $L_o = 0.8\ \mu$H and autotuning peak-current-mode controller.



Time: 200µs/Div.
Top Trace (Output Voltage, AC Coupled): 50mV/Div.
Bottom Trace (Load Current): 5A/Div.

Figure 3.18: Measured transient response of the power converter during a load transient of 5A $\leftrightarrow$ 15A with $C_o = 0.81\ mF$ and autotuning peak-current-mode controller.

Table 3.2: Measured and estimated values of ω_o

	Measured ω_o (rad/sec)	Estimated ω_o (rad/sec)	Error (%)
Power – Stage 1	27277	27787	1.8
Power – Stage 2	33201	33760	1.6
Power – Stage 3	32075	32539	1.4

Table 3.3: Measured and estimated values of ω_{ESR}

	Measured ω_{ESR} (rad/sec)	Estimated ω_{ESR} (rad/sec)	Error (%)
Power – Stage 1	153050	149674	2.2
Power – Stage 2	155040	150173	3.1
Power – Stage 3	198410	202684	2.1

3.4 Comparison of the Proposed Method With Other Autotuning Methods

The online closed-loop autotuning method proposed in [46] uses the time-domain characteristics of the compensated error signal to tune the controller. Trial-and-error method is used to adjust the gain, poles, and zeros of the compensator in a manner that will increase the peak-to-peak amplitude of the compensated error signal. Since the poles and zeros are adjusted using a trial-and-error approach this may cause the system to become unstable during the tuning process. Moreover, with this method the phase margin of the system cannot be controlled.

The autotuning method presented in [47–51] uses intentionally introduced limit-cycle-oscillations to estimate the resonance frequency of the output filter. Hence, the zeros of the compensator can be accurately placed at the resonance frequency. After that an iterative procedure is used to adjust the compensator poles and gain in order to obtain the desired phase margin and crossover frequency. The main drawback of this method is that it is based on intentionally introduced limit-cycle-oscillations which will affect the converter's normal operation and output voltage regulation during the autotuning phase.

The autotuning schemes presented in [39–43] are based on the measurement of closed-loop frequency response. A test signal is injected into the feedback loop and the frequency response is measured online, based on which the digital com-

pensator coefficient is adjusted in a manner to obtain the desired phase margin and crossover frequency. Since these methods are based on online frequency response measurement they require more significant signal processing techniques such as high-performance microcontroller is usually required for their implementation. Moreover, with signal injection into control loop, this method inevitably causes perturbations to the output voltage and affects load regulation.

With the method proposed in this work, the resonant frequency ω_o and ESR zero frequency ω_{ESR} are estimated by analyzing converter's quasi-impulse response during start-up transient and online measurement of steady-state output voltage ripple. Based on these estimated parameters, the coefficients of the digital controller are tuned to maintain constant crossover frequency and phase margin irrespective of variations in power-stage parameters. As a result, the proposed method offers the advantage of being free from trial-and-error and is non-intrusive, hence it does not disturb a converter's normal operation. Moreover, the proposed method is hardware efficient since no additional hardware such as voltage and current sensors are required and can be implemented on low-cost microcontroller. The advantages and disadvantages of various autotuning methods are given in Table 3.4.

3.5 Conclusion

A simple method for online estimation of the power-stage parameters of a digitally controlled buck converter and its application in autotuning controller has been presented in this chapter. A quasi-impulse response of the converter's power-stage is generated by a short rectangular pulse during startup and is utilized to estimate the resonant frequency ω_o of the L_oC_o output filter. The ESR zero is accurately estimated by combining the estimated resonant frequency with the measured steady-state output voltage ripple. Online estimation of power-stage

Table 3.4: Comparison of various autotuning methods

	Advantages	Disadvantages
Online closed-loop autotuning digital controller [46]	• Does not affect converter's normal operation. • Suitable for continuous parameter tuning.	• Poles and zeros are adjusted using trial-and-error approach. • Can cause the system to become unstable during tuning phase. •Phase margin cannot be adjusted.
Autotuning controller based on relay feedback [47–49]	• Digital compensator zeros can be accurately placed at the resonance frequency. • Phase margin and crossover frequency can be adjusted.	• Affect converter's normal operation. • Not suitable for continuous parameter tuning. • Compensator poles are placed using iterative procedure. • Requires a non-linear relay.
Limit-cycle oscillation based autotuning [50, 51]	• Digital compensator zeros can be accurately placed at the resonance frequency. • Phase margin and crossover frequency can be adjusted.	• Affect converter's normal operation. • Not suitable for continuous parameter tuning. • Compensator poles are placed using iterative procedure.
Model reference-based autotuning [42, 43]	• Converter's phase margin and crossover frequency can be accurately adjusted. • Not based on trial-and-error approach.	• Affect converter's normal operation. • Not suitable for continuous parameter tuning.
Adaptive tuning system based on desired phase margin [40, 41]	• Converter's phase margin and crossover frequency can be accurately adjusted. • Not based on trial-and-error approach.	• Affect converter's normal operation. • Not suitable for continuous parameter tuning.
Autotuning controller based on online frequency response measurement [39]	• Converter's phase margin and crossover frequency can be accurately adjusted. • Not based on trial-and-error approach.	• Affect converter's normal operation. • Not suitable for continuous parameter tuning.
Quasi-impulse response based method (this work)	• Converter's phase margin and crossover frequency can be accurately adjusted. • Not based on trial-and-error approach. • Does not affect converter's normal operation.	• Not suitable for continuous parameter tuning.

parameters and adjustments of the coefficients of digital controller accordingly are able to ensure constant crossover frequency and phase-margin in the presence of wide-range variations in power-stage parameters. Experimental results for

both digital voltage-mode and peak-current-mode controlled buck converter are presented to validate the proposed method. The same approach can be applied to other converter topologies with minor adaptation.

Chapter 4

Cascaded Converter System: Analysis and Control

4.1 Introduction

Many applications such as uninterruptible power supplies (UPS), solid-state transformers (SST), grid-connected energy storage systems and grid-connected photovoltaic (PV) systems adopt cascaded converter structure [64–69]. A cascaded converter system for these applications typically consists of a dc-dc frond-end converter followed by a dc-ac inverter as shown in Fig. 4.1 [70–74]. The front-end dc-dc converter is used to provide a well-regulated and reliable dc-bus voltage. In addition, the dc-dc converter can be used to step-up or step-down the input dc-

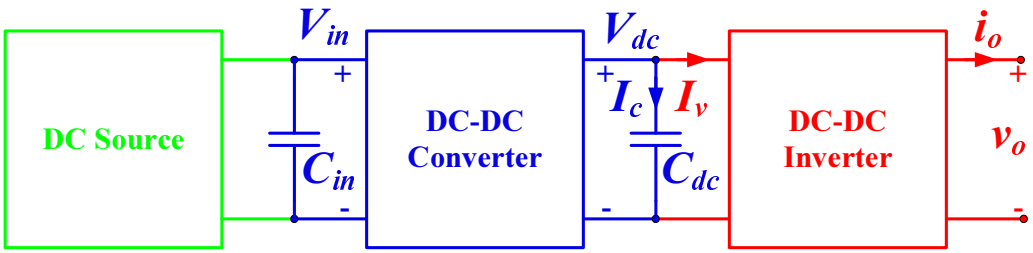


Figure 4.1: Typical cascaded converter system.

voltage and provide galvanic isolation between the input and output if required. The dc-ac inverter is used to generate an ac-voltage at the grid frequency and used to power ac-load or to feed ac-power into the grid. Dual-active-bridge (DAB) converter is the preferred candidate for the front-end dc-dc conversion stage due to its soft-switching operation, high efficiency, high frequency operation, bidirectional power-flow capability, ability to step-up or step-down the dc voltage using a high frequency transformer and provision of galvanic isolation [75–79].

In this chapter, the basic operating principle of a DAB based two-stage single-phase inverter system is presented in detail, followed by a thorough discussion of some recently proposed control methods to enhance the dynamic response of the front-end dc-dc converter and to reduce the amplitude of the second-order ripple component in the dc-bus voltage without significantly increasing the dc-bus capacitance.

4.2 Basic Operating Principle of Two-Stage Single-Phase Inverter System

4.2.1 Operating Principle of DAB DC-DC Converter

Fig. 4.2 depicts the topology of a DAB dc-dc converter. Referring to Fig. 4.2, V_{in} is the input voltage, V_{dc} is the dc-bus voltage, C_{in} is the input capacitor, C_{dc} is the dc-bus capacitor, $n = \frac{n_p}{n_s}$ is the transformer turns ratio and L is the energy transfer inductance. Switches $S_1 - S_4$ constitute the primary bridge while switches $Q_1 - Q_4$ constitute the secondary bridge of the DAB converter.

Single-phase-shift (SPS) modulation is the most commonly used modulation method to modulate the output power of DAB converter. The primary-and-secondary-side switches are operated with 50% duty ratio to generate two square wave voltages v_p and v_s, respectively. A phase-shift is introduced between the

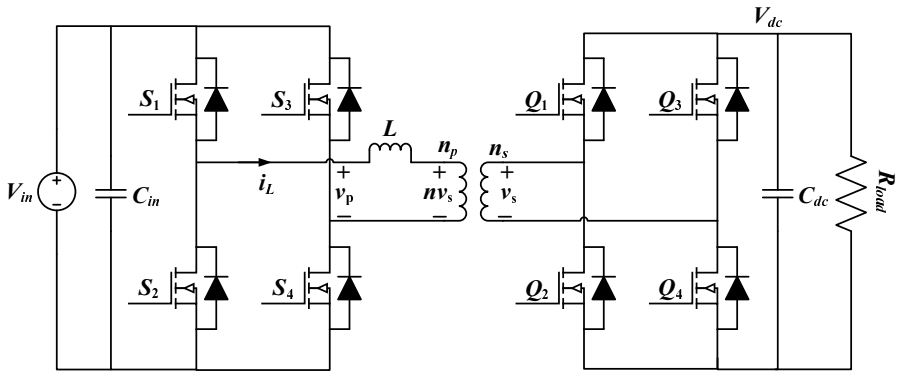


Figure 4.2: Front-end DAB dc-dc converter.

primary voltage v_p and the secondary voltage v_s, and power flows from the bridge having a leading phase to the bridge having a lagging phase.

The steady-state operating waveforms of a DAB dc-dc converter with SPS modulation in forward power flow made are given in Fig. 4.3a-c. From Fig. 4.3a it can be seen that during the time interval $t_o \rightarrow t_1$ the switches S_1 and S_4 of the primary bridge and the switches Q_2 and Q_3 of the secondary bridge are turned on thus creating a positive and a negative voltage across the transformer's primary and secondary windings, respectively. During this time interval, the inductor current is then described by

$$i_L(t_1) = \frac{(V_{in} + nV_{dc})dT}{2L} + i_L(t_0) \tag{4.1}$$

where V_{in} is the input voltage, V_{dc} is the dc-bus voltage, $n = \frac{n_p}{n_s}$ is the transformer turns-ratio, d is the phase-shift between v_p and v_s, $T = \frac{1}{f_s}$ is the switching period and L is the energy transfer inductance.

During the time interval $t_1 \rightarrow t_2$ the switches S_1 and S_4 of the primary bridge and switches Q_1 and Q_4 of the secondary bridge are turned on thus creating a positive voltage across both the transformer's primary and secondary windings. The inductor current during this interval is described by

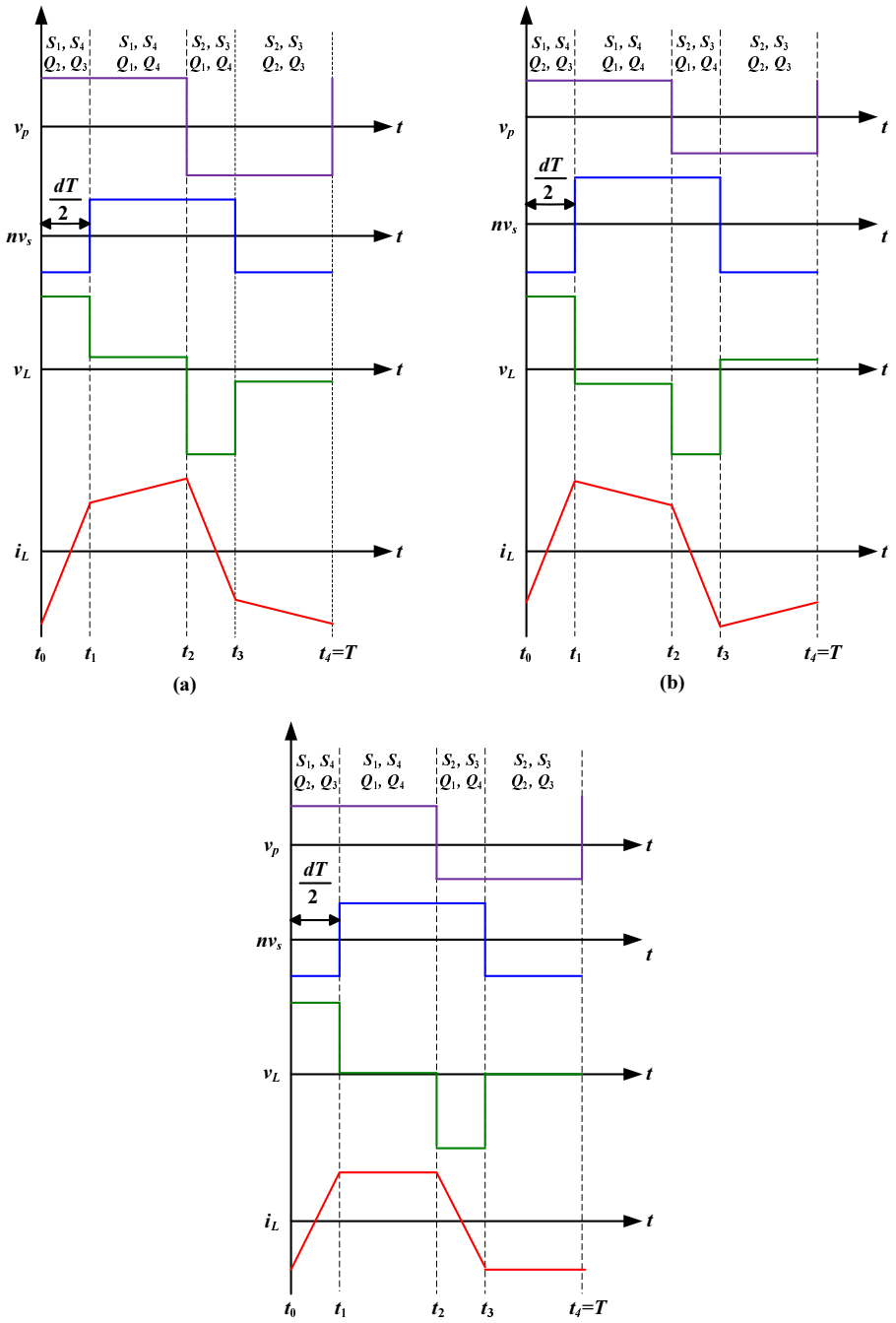


Figure 4.3: Steady state operating waveforms of DAB converter (a) $V_{in} > nV_{dc}$ (b) $V_{in} < nV_{dc}$ (a) $V_{in} = nV_{dc}$.

$$i_L(t_2) = \frac{(V_{in} + nV_{dc})(1-d)T}{2L} + i_L(t_1) \tag{4.2}$$

Due to symmetry, $i_L(t_2) = -i_L(t_0)$, thus the inductor current at time $t = t_o$

and $t = t_2$ can be calculated from equation (4.1) and equation (4.2) as follows:

$$i_L(t_0) = \frac{T}{4L}[(1-2d)nV_{dc} - V_{in}] \tag{4.3}$$

$$i_L(t_2) = \frac{T}{4L}[-(1-2d)nV_{dc} + V_{in}] \tag{4.4}$$

The average value of the inductor current I_L for half-switching cycle can be then calculated as follow

$$I_L = \langle i_L \rangle = \frac{1}{2T}[-(i_L(t_0) + i_L(t_1))dT + (i_L(t_1) + i_L(t_2))(1-d)T]$$

$$I_L = \langle i_L \rangle = \frac{V_{in}d(1-d)}{2f_sL} \tag{4.5}$$

Hence, the average power transferred to the load is given by

$$P = V_{in}I_L = \frac{nV_{in}V_{dc}d(1-d)}{2f_sL} \tag{4.6}$$

Assuming 100% converter's efficiency, the average value of the current flowing out of the secondary bridge I_{os} can be obtained as follows:

$$I_{os} = \langle i_{os} \rangle = \frac{nV_{in}d(1-d)}{2f_sL} \tag{4.7}$$

4.2.2 Operating Principle of Single-Phase Inverter

Fig .4.4 depicts the topology of a single-phase full-bridge inverter. Switches $T_1 - T_4$ constitute a full-bridge. Sinusoidal-pulse-width-modulation (SPWM) is used to generate the switching signals for the switches. As shown in Fig .4.5 the switching signal for the switch T_1 is generated by comparing a carrier signal to a sinusoidal modulation signal. When the modulation signal is higher than

the carrier signal switch T_1 is turned-on, and vice versa. Similarly the switching signal for switch T_3 is generated by comparing the same carrier signal to a phase-shifted modulation signal. Switch T_3 is turned-on when the modulation signal is larger than the carrier signal. The switching signals for T_2 and T_4 are the inverse

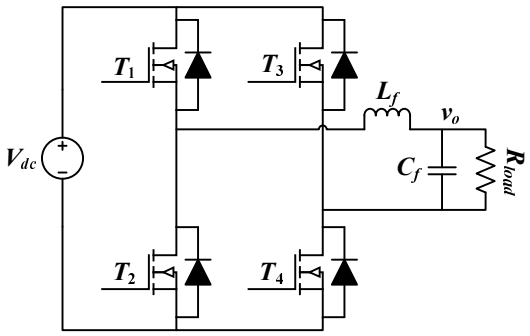


Figure 4.4: Single-phase inverter.

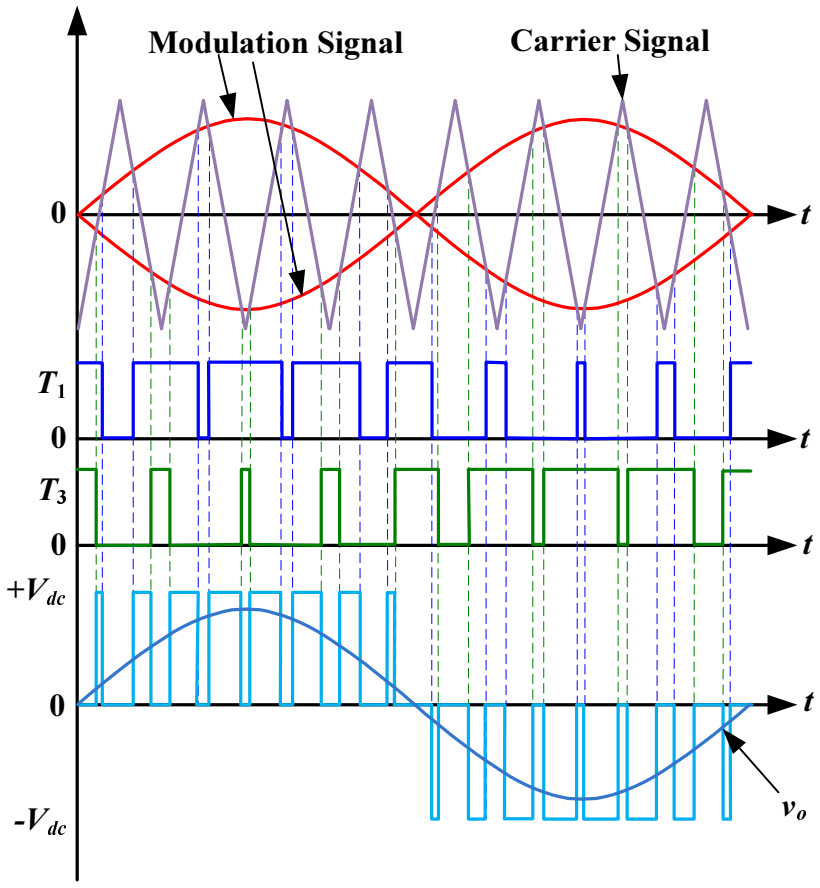


Figure 4.5: Steady state operating waveform of single-phase inverter with SPWM
.

of those for T_1 and T_3.

4.3 Control Methods for the Front-End DC-DC Converter in Cascaded Converter System

To provide a well regulated and reliable dc-bus voltage and to reduce the dc-bus capacitance, tight output voltage regulation and fast transient response of the front-end dc-dc converter is required. Furthermore, when inverter is connected as a load to the frond-end dc-dc converter there exists an ac-ripple component in the dc-bus voltage oscillating at twice the inverter's output frequency due to the pulsating instantaneous output power of the inverter. This double-line frequency ripple component can result in a reduced lifetime of the dc-bus capacitor and affects the inverter's output voltage quality. Therefore, it is necessary to reduce the amplitude of this double-line frequency ripple in the dc-bus voltage. To reduce the amplitude of the double line-frequency ripple on the dc-bus voltage, a large dc-bus capacitance is typically required which results in increased cost and reduced power density [80–83].

Conventionally, a single-loop voltage-mode or a dual-loop current-mode PI controller is employed to regulate the output voltage of DAB converter [84–86]. However, the main drawback associated with conventional PI controller is that it is challenging for the PI controller to meet both dynamic response performance and stability requirements satisfactorily, as they are often in contradiction with each other. Hence, there is always a tradeoff between dynamic response performance and stability with this approach. Moreover, the performance of the designed PI controller can be adversely affected by model uncertainties and variations in circuit parameters. Finite gain of the PI controller at the double-line frequency implies that it cannot effectively suppress the double-line frequency

ripple without resolving to the use of large and bulky dc-bus capacitance. In the literature, various control methods have been proposed to enhance the dynamic response of the frond-end dc-dc converter and to reduce the amplitude of the double-line frequency ripple component without increasing dc-bus capacitance.

To enhance the transient response of DAB converter to load current and reference voltage changes a lookup table based feedforward control method is proposed in [87, 88]. In the proposed method a first-order linearised dynamic model that relates the transient response of the converter to load current and reference voltage changes is derived. Based on the derived converter's model a lookup table is constructed. During each switching cycle, the converter parameters are used to estimate the load current. Based on the estimated load current, a feed-forward phase-shift term is obtained from the lookup-table and added to the output of PI controller. Since the lookup table and the estimated load current are computed based on nominal converter parameters, there might be discrepancies between the desired phase-shift and the commanded phase-shift.

To improve the dynamic response performance of DAB converter a dual-loop current-mode control is proposed in [89–95]. In [89], a feedforward-based peak-current-mode control is proposed to regulate the output voltage and enhance the dynamic response performance of DAB converter. With the proposed method the conventional PI controller in the outer voltage loop is replaced by a feedforward block. The feedforward block uses the converter's input and output voltages and the input power as the inputs to generate a peak-current reference signal for the inner current loop. For the implementation of the inner-current loop, the actual inductor current is sensed using a current sensor. The sensed inductor current is then compared to the calculated peak current reference signal to generate the switching signals for the secondary bridge of the DAB converter. However, the proposed control method requires additional voltage and current sensors and precise knowledge of the transformer's turns ratio.

In [90–92], a digital predictive current-mode control is presented, where instead of sampling the actual average inductor current which will require an analog-to-digital converter (ADC) with high sampling rate, the transformer current is sampled once at the beginning of each switching cycle and the required phase-shift for the next switching cycle is calculated using the nominal values of converter parameters. To further improve the performance of peak-current-mode control, a predictive valley-peak-current-mode control is proposed in [93]. Instead of controlling only the peak value of inductor current, both the peak and valley values of inductor current is actively controlled. A current-mode control method with load current feedforward is proposed in [94]. With the proposed method, linear and nonlinear load current feedforward formulas are derived based on which a feedforward term is added to the output of PI controller to enhance the dynamic response performance of DAB converter.

As an alternative to conventional PI control, a boundary control method for DAB converter is proposed in [96, 97]. The natural voltage-current trajectories of DAB converter are derived and used to produce the switching signals for the two active bridges. To eliminate the dc bias in inductor current and to improve the dynamic response performance of DAB converter during fast load change, a double-sided modulation strategy is proposed in [98, 99]. As opposed to single-sided modulation scheme where the switching signals for one of the bridges is fixed and the switching signals for the other bridges are phase shifted according to the control signal, the proposed double-sided modulation scheme distributes the required phase shift during transient events among the primary bridge and secondary bridge according to an optimized ratio. As an alternative to conventional PI control method, a Lyapunov-based control law is derived and successfully applied to a resonant dc-dc converter in [100] to enhance its transient response performance and regulate its output voltage.

A disturbance observer based nonlinear control method is proposed in [101,

102] for DAB converter, where a nonlinear disturbance observer is used to estimate the direct and quadrature components of inductor current. The two current components are used to control the active and reactive power of a DAB converter, respectively. However, the proposed control method requires an extra current sensor to sense the converter's input current. A virtual direct power control method is proposed in [103] to improve the dynamic response performance of DAB converter. With the proposed method, during each switching cycle, the desired phase shift value is calculated based on the sampled load current and input/output voltages and added to the output of PI controller. In [104, 105], a unified-phase-control with power balancing strategy is proposed to enhance the efficiency and to improve the dynamic response performance of DAB converter. One major disadvantage common to both virtual direct power control and unified-phase-control with power balancing is that they require the use of extra voltage and current sensors which will introduce additional losses and will increase the bulkiness of the converter.

In [106, 107], a proportional-integral-resonant (PI-R) controller is utilized to mitigate the double-line frequency oscillation and to regulate the output voltage of DAB converter. With the proposed method, the two poles of the resonant controller are placed at the double-line frequency in order to achieve a high loop gain at the frequency. However, the addition of extra poles will increase the system order and may result in degraded dynamic response and reduced phase margin at other frequencies. Another approach for reducing the double-line frequency ripple on the dc-bus voltage is by shaping the output impedance of converter. A virtual impedance based control method is proposed in [108, 109] to reduce the double-line frequency ripple in the dc-bus voltage, where a band-pass filter is incorporated in the inductor current's feedback path to increase its impedance. In [110] and [111], a method to shape the output impedance of the front-end DAB dc-dc converter is proposed. Instead of using a single-loop voltage-mode control,

a dual-loop voltage-mode control is proposed. A DAB converter will exhibit different closed-loop output-impedance characteristics depending on the feedback gain selected for the inner voltage-loop.

To reduce the second-order harmonic current in the front-end dc-dc converter, instead of using a constant dc-bus reference voltage, the dc-bus reference voltage is varied according to load current so the dc-bus capacitor nearly provides all the ripple [112, 113]. The proposed solution however, requires a large dc-bus capacitor and induces large fluctuations of dc-bus voltage which will have negative effect on inverter's output voltage quality. In [114], a disturbance observer based load current feed-forward control method is used to improve the transient response performance of DAB converter and to reduce the double-line frequency ripple on the dc-bus voltage. Instead of sensing the actual load current which will require an additional current sensor and will incur power loss, a nonlinear disturbance observer is used to estimate load current. However, the accuracy of the estimated load current strongly depends on the accuracy of the estimated converter parameters.

4.4 Conclusion

In this chapter, the steady-state operating principle of the front-end DAB converter and single-phase inverter are presented. When DAB converter is used to drive a single-phase inverter, there exists an ac-ripple component in the dc-bus voltage oscillating at twice the inverter's output frequency due to the pulsating instantaneous output power of the inverter. This double-line frequency ripple component can result in a reduced lifetime of the dc-bus capacitor and affects the inverter's output voltage quality. Therefore, it is necessary to minimize its amplitude in the dc-bus voltage. The problem is rooted in the controller design of the front-end dc-dc converter. To enhance the dynamic response performance of the

front-end DAB converter and to reduce the amplitude of the double-line frequency ripple in the dc-bus voltage, various control methods have been proposed in literature. However, most of these control methods are based on an ideal small-signal converter model where model uncertainties and variations in converter parameters are not taken into consideration. Maintaining superior closed-loop dynamic response performance in-spite of model uncertainties and parameter variations is still a problem that needs to be addressed.

Chapter 5

Disturbance Observer Based DC-Bus Voltage Control for Ripple Mitigation and Improved Dynamic Response in Two-Stage Single-Phase Inverter System

In Chapter 4, various control methods proposed in the literature for the enhancement of the dynamic response of front-end dc-dc converter are discussed. However, majority of these control methods can only deal with external disturbances such as load current and input voltage changes, while variations in circuit parameters and model uncertainties are not considered. In this chapter, a disturbance observer based control strategy for front-end DAB converter is proposed to enhance its dynamic response performance and to mitigate the double-line frequency ripple on the dc-bus voltage of a two-stage single-phase inverter system.

The proposed disturbance observer is designed based on the least amount of plant information and is combined with a proportional controller to form a de-

coupled composite controller [116–120]. The input to the disturbance observer is the sensed dc-bus voltage and control signal. Hence, the proposed solution does not require additional voltage or current sensor. By using this information, the disturbance observer can accurately estimate and compensate for the lumped disturbance which includes external disturbances, model uncertainties, and circuit parameter variations due to temperature and aging effects. With this disturbance sources accounted for and their effects compensated, superior control performance can be achieved over a wide range of operating conditions. Moreover, with the proposed solution, the output current of DAB converter can closely track the inverter's input current and therefore effectively minimizes the double-line frequency ripple on the dc-bus voltage without resolving to the use of large and bulky bus capacitance.

5.1 Analysis and Modeling of Two-Stage Single-Phase Inverter System

Fig. 5.1 shows a two-stage single-phase inverter system which consists of a DAB dc-dc converter driving a single-phase inverter. Single-phase-shift (SPS) modulation is by far the most widely used modulation scheme for controlling the output power of DAB converter. As shown in Fig. 5.2 a phase shift is introduced between the primary and the secondary bridge, and power flows from the bridge having a leading phase to the bridge having a lagging phase. The amount of power transferred from the leading bridge to the lagging bridge is given by equation (5.1) [121–126].

$$P = \frac{nV_{in}V_{dc}d(1-d)}{2f_sL} \tag{5.1}$$

where $n = \frac{n_p}{n_s}$ is the transformer turns ratio, V_{in} is the input voltage, V_{dc} is the

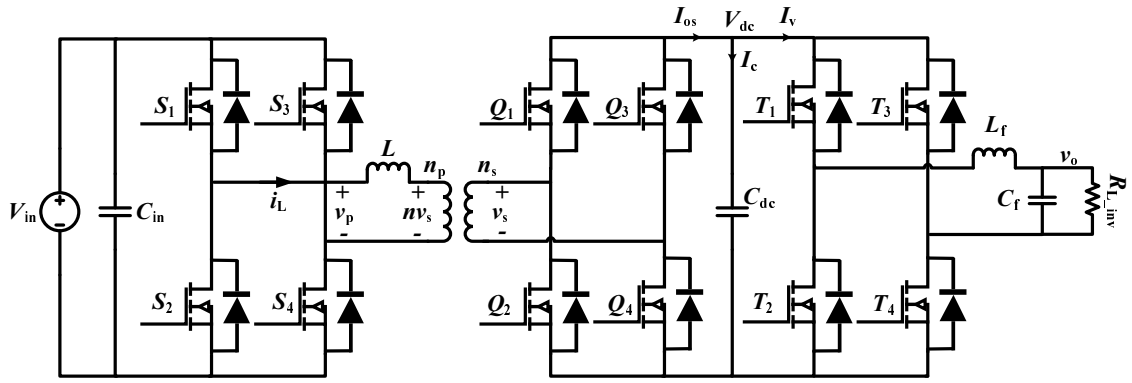


Figure 5.1: DAB dc-dc converter driving a single-phase inverter.

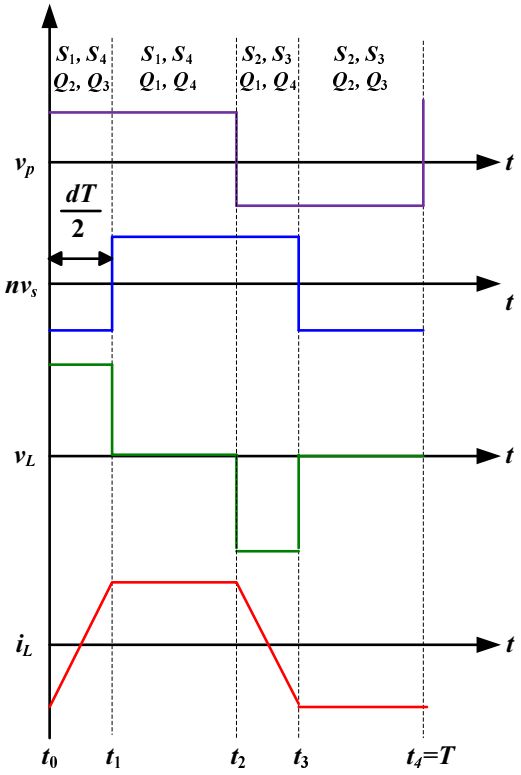


Figure 5.2: Operating waveforms of DAB converter under single-phase shift modulation.

dc-bus voltage, d is the phase shift between the primary and secondary bridge voltages, f_s is the switching frequency and L is the energy transfer inductance.

From the power equation of the DAB converter, the average current flowing out of the secondary bridge I_{os} can be calculated as follows:

$$I_{os} = \frac{nV_{in}d(1-d)}{2f_sL} \tag{5.2}$$

By taking the partial derivative of equation (5.2), the small-signal value of the output current of the secondary bridge can be obtained and is given by equation (5.3).

$$\tilde{i}_{os} = \frac{nV_{in}(1-2d)}{2f_sL}\tilde{d} \tag{5.3}$$

The single-phase inverter which is controlled by using sinusoidal pulse-width modulation (SPWM) scheme is connected as a load to the front-end dc-dc converter. From the viewpoint of the disturbance observer, the inverter load can be treated as an equivalent dc resistance given by equation (5.4), calculated based on the average inverter's input power [127–131], while the double-line frequency ripple is regarded as a form of disturbance which will be estimated and compensated by the disturbance observer.

$$R_{in\_eq} = \frac{V_{dc}^2 R_{L\_inv}}{V_{o\_rms}^2} \tag{5.4}$$

where V_{dc} is the dc-bus voltage, V_{o_rms} is the inverter's rms output voltage, and R_{L_inv} is the inverter's load resistance.

Based on equation (5.3) and equation (5.4), the small-signal average model of the DAB converter driving a single-phase inverter is shown in Fig. 5.3, where $\tilde{i}_v$

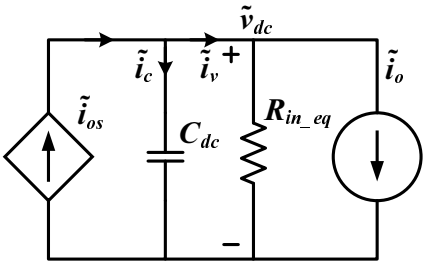


Figure 5.3: Small-signal model of DAB converter driving an inverter load.

and $\tilde{i}_o$ is the small-signal load current and small-signal perturbation to the load current, respectively.

5.2 Disturbance Observer Design

In order to achieve a fast transient response and to suppress the double-line frequency ripple on the dc-bus voltage, a disturbance observer is designed to estimate the total disturbances affecting the dc-bus voltage and the observer's output is added to the control signal for compensating these disturbances. Fig. 5.4 shows the block diagram of the proposed controller which consists of a disturbance observer and a feedback controller. Here, the feedback controller is designed to achieve the required phase margin and cross-over frequency, while the disturbance observer is used to estimate and compensate for the lumped disturbance which includes model uncertainties and circuit parameter variations. Based on the average model of the two-stage single-phase inverter system (since disturbance observer is designed based on nominal plant's information, the perturbation to load current is set to zero, i.e. $\tilde{i}_o$=0), and applying Kirchhoff's current law, the differential equation describing the dc-bus capacitor dynamics can be written as follows:

$$\frac{\mathrm{d}\tilde{v}_{dc}}{\mathrm{d}t} = -\frac{\tilde{v}_{dc}}{R_{in\_eq}C_{dc}} + \frac{nV_{in}(1-2d)}{2f_sLC_{dc}}\tilde{d} \tag{5.5}$$

Equation (5.5) can be rearranged as equation (5.6)

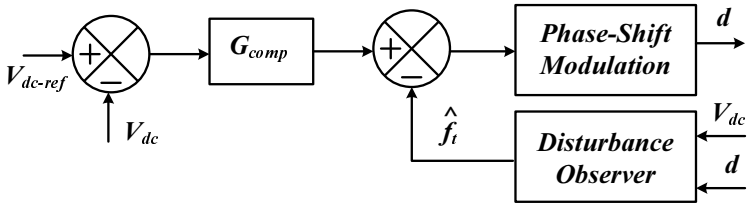


Figure 5.4: Block diagram of disturbance observer based voltage-mode control.

$$\dot{\tilde{v}}_{dc} = f_t(\tilde{v}_{dc},\ \tilde{\mu}) + b_o\tilde{\mu} \tag{5.6}$$

where $f_t(\tilde{v}_{dc},\ \tilde{\mu}) = a\tilde{v}_{dc} + (b - b_o)\tilde{\mu}$ is the lumped disturbance which includes external disturbances, circuit parameter variations and model uncertainties, with

$$a = -\frac{1}{R_{in\_eq}C_{dc}} \qquad b = \frac{nV_{in}(1-2d)}{2f_sLC_{dc}}$$

$$b_o = \frac{nV_{in0}(1-2d_0)}{2f_sL_0C_{dc0}} \qquad \tilde{\mu} = \tilde{d}$$

where V_{in0}, L_0 and C_{dc0} represents the nominal values of the input voltage, inductor, and bus capacitor, respectively.

The disturbance observer for this system can be designed using equations (5.7) and (5.8) [132, 133].

$$\hat{\dot{\tilde{v}}}_{dc} = \hat{f}_t + \beta_1(\tilde{v}_{dc} - \hat{\tilde{v}}_{dc}) + b_o\tilde{\mu} \tag{5.7}$$

$$\hat{\dot{f}}_t = \beta_2(\tilde{v}_{dc} - \hat{\tilde{v}}_{dc}) \tag{5.8}$$

where $\hat{\tilde{v}}_{dc}$ is estimated value of the dc-bus voltage $\tilde{v}_{dc}$, $\hat{f}_t$ is the estimated value of the lumped disturbance and β_1, β_2 are the observer gains.

Defining the estimation errors as $e_1 = \tilde{v}_{dc} - \hat{\tilde{v}}_{dc}$ and $e_2 = f_t(\tilde{v}_{dc},\ \tilde{\mu}) - \hat{f}_t$, the following equation can be obtained.

$$\dot{e}_1 = \dot{\tilde{v}}_{dc} - \hat{\dot{\tilde{v}}}_{dc} = e_2 - \beta_1 e_1 \tag{5.9}$$

$$\dot{e}_2 = \dot{f}_{\mathrm{t}}(\tilde{v}_{\mathrm{dc}},\ \tilde{\mu}) - \hat{\dot{f}}_{\mathrm{t}} = \dot{f}_{\mathrm{t}}(\tilde{v}_{\mathrm{dc}},\ \tilde{\mu}) - \beta_2 e_1 \tag{5.10}$$

Equation (5.9) and equation (5.10) can be rearranged as equation (5.11).

$$\dot{\mathbf{e}} = \mathbf{A_e}\mathbf{e} + \mathbf{\Phi} \tag{5.11}$$

with

$$\mathbf{e} = \begin{bmatrix} e_1 \\ e_2 \end{bmatrix} \quad \mathbf{A_e} = \begin{bmatrix} -\beta_1 & 1 \\ -\beta_2 & 0 \end{bmatrix} \quad \mathbf{\Phi} = \begin{bmatrix} 0 \\ \dot{f}_{\mathrm{t}}(\tilde{v}_{\mathrm{dc}},\ \tilde{\mu}) \end{bmatrix}$$

If β_1 and β_2 are strictly positive, the roots of the characteristic polynomial of $\mathbf{A_e}$ will exist on the left-half of the s-plane, in which case $\mathbf{A_e}$ will be Hurwitz stable and the estimation error will converge exponentially to zero. In other words, the estimated states will converge to the actual states. The time-domain solution of equation (5.11) is given by,

$$\mathbf{e(t)} = e^{\mathbf{A_e}(t-t_o)}\mathbf{e(t_o)} + \int_{t_o}^{t} e^{\mathbf{A_e}(t-\tau)}\mathbf{\Phi}(\tau)d\tau \tag{5.12}$$

If $\mathbf{A_e}$ is Hurwitz stable, there exists a constant $c > 0$ such that $\parallel e^{\mathbf{A_e}(t-t_o)} \parallel \leq ce^{\frac{\lambda(\mathbf{A_e})}{2}(t-t_o)}$ [134–137]. It can therefore be concluded from equation (5.13) that the error dynamics is bounded in a finite time T_o, *i.e.* $\parallel \mathbf{e(t)} \parallel \leq \epsilon$, $\forall t \geq T_o > 0$, where ϵ is a small positive constant. For small estimation error, $\lambda(\mathbf{A_e})$ should be chosen to be sufficiently large.

$$\parallel \mathbf{e(t)} \parallel \leq\ ce^{\frac{\lambda(\mathbf{A_e})}{2}(t-t_o)} \parallel \mathbf{e(t_o)} \parallel + \int_{t_o}^{t} ce^{\frac{\lambda(\mathbf{A_e})}{2}(t-\tau)} \parallel \mathbf{\Phi}(\tau) \parallel d\tau$$

$$\leq ce^{\frac{\lambda(\mathbf{A_e})}{2}(t-t_o)} \parallel \mathbf{e(t_o)} \parallel - \frac{2c}{\lambda(\mathbf{A_e})} \underset{t_o \leq \tau \leq t}{\mathrm{sub}} \parallel \Phi(\tau) \parallel \tag{5.13}$$

For different values of β_1 and β_2, it is expected that the disturbance observer, and hence the DAB converter, will exhibit different transient response character-

istics, therefore a careful design of the observer gains is mandatory and will be discussed next.

5.3 Parameter Selection and Controller Design

In this section, the disturbance observer gains are selected based on a frequency domain analysis of the estimation error dynamics. Based on the selected observer gains and the resulting converter's loop gain, a feedback controller will be designed for the DAB converter.

5.3.1 Selection of Disturbance Observer Gains

Let β_1 and β_2 be $2\zeta\omega_n$ and ω_n^2, respectively, where ζ and ω_n represents the damping ratio and the undamped natural frequency of the closed-loop error estimation system. Substituting the value of β_1 and β_2, equation (5.7) and equation (5.8) can be rearranged as follows:

$$\dot{\mathbf{X}} = \mathbf{A}\mathbf{X} + \mathbf{B}\mathbf{U} \tag{5.14}$$

with

$$\mathbf{A} = \begin{bmatrix} -2\zeta\omega_n & 1 \\ -\omega_n^2 & 0 \end{bmatrix} \quad \mathbf{X} = \begin{bmatrix} \widehat{\tilde{v}}_{\mathrm{dc}} \\ \hat{f}_{\mathrm{t}} \end{bmatrix} \quad \mathbf{B} = \begin{bmatrix} b_{\mathrm{o}} & 2\zeta\omega_n \\ 0 & \omega_n^2 \end{bmatrix} \quad \mathbf{U} = \begin{bmatrix} \tilde{\mu} \\ \tilde{v}_{\mathrm{dc}} \end{bmatrix}$$

The input to the disturbance observer is the control signal $\tilde{\mu}$ and the sensed bus voltage $\tilde{v}_{dc}$, while the output of the disturbance observer is the lumped disturbance $\hat{f}_t$. The s-domain transfer function from the control signal $\tilde{\mu}$ to the lumped disturbance $\hat{f}_t$ with $\tilde{v}_{dc} = 0$ and from the bus voltage $\tilde{v}_{dc}$ to the lumped disturbance $\hat{f}_t$ with $\tilde{\mu} = 0$ is given by equation (5.15) and equation (5.16), re-

spectively.

$$G_{f\mu} = \frac{\hat{f}_{\mathrm{t}}(s)}{\tilde{\mu}(s)} = \begin{bmatrix} 0 & 1 \end{bmatrix} [sI - A]^{-1} \begin{bmatrix} b_o \\ 0 \end{bmatrix}$$

$$= \frac{-\omega_n^2 b_o}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{5.15}$$

$$G_{fv_{\mathrm{dc}}} = \frac{\hat{f}_{\mathrm{t}}(s)}{\tilde{v}_{\mathrm{dc}}(s)} = \begin{bmatrix} 0 & 1 \end{bmatrix} [sI - A]^{-1} \begin{bmatrix} 2\zeta\omega_n \\ \omega_n^2 \end{bmatrix}$$

$$= \frac{\omega_n^2 s}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{5.16}$$

The small-signal open-loop, control-to-bus voltage and load current-to-bus voltage transfer function can be obtained from Fig. 5.3, and is given by equation (5.17) and equation (5.18), respectively. Fig. 5.5 shows the small-signal block diagram of the DAB converter under disturbance observer based voltage-mode control. The transfer function from the compensated error signal $\tilde{v}_c$ to the dc-bus voltage $\tilde{v}_{dc}$ is given by equation (5.19).

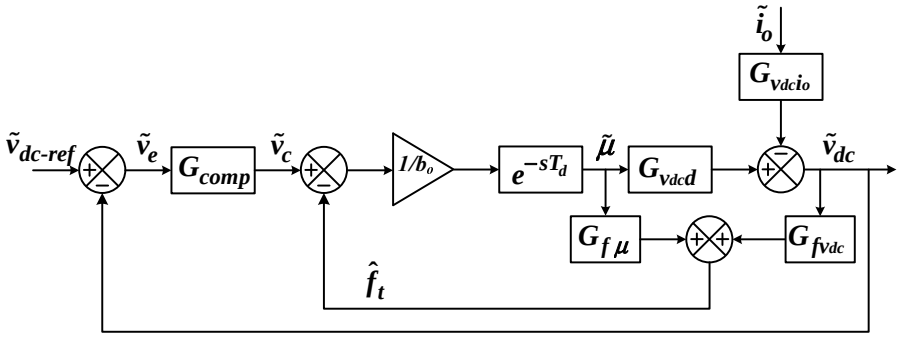


Figure 5.5: Small-signal block diagram of disturbance observer based voltage-mode controller for DAB converter.

$$G_{v_{dc}d} = \frac{\tilde{v}_{dc}}{\tilde{d}} = \frac{nV_{in}R_{in\_eq}(1-2d)}{2f_sL(1+sR_{in\_eq}C_{dc})} \tag{5.17}$$

$$G_{v_{dc}i_o} = \frac{\tilde{v}_{dc}}{-\tilde{i}_o} = \frac{R_{in\_eq}}{1+sR_{in\_eq}C_{dc}} \tag{5.18}$$

$$G_{v_{dc}v_c} = \frac{\tilde{v}_{dc}}{\tilde{v}_c} = \frac{G_{v_{dc}d}b_o^{-1}e^{-sT_d}}{1+G_{v_{dc}d}b_o^{-1}e^{-sT_d}(G_{f\mu}G_{v_{dc}d}^{-1}+G_{fv_{dc}})} \tag{5.19}$$

Fig. 5.6 shows the pole-zero map of $G_{v_{dc}v_c}$ for different values of ω_n and a damping ratio of 1. As ω_n increases, the poles move towards infinity on the left-half of the s-plane. The higher the value of ω_n the faster will be the transient response of the system. However, a higher value of ω_n will introduce more high-frequency noise to the system. Thus, there is a trade-off between the transient response performance and the noise level of the system.

5.3.2 Controller Design

The closed-loop transfer function of the DAB converter, *i.e.* from $\tilde{v}_{dc-ref}$ to $\tilde{v}_{dc}$, is given by equation (5.20).

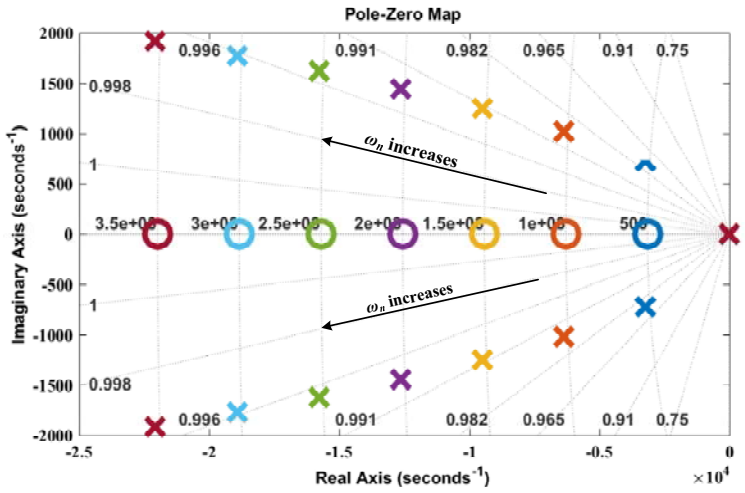


Figure 5.6: Location of poles and zeros of $G_{v_{dc}v_c}$ as a function of ω_n.

$$G_{v_{\mathrm{dc}}v_{\mathrm{dc-ref}}} = \frac{\tilde{v}_{\mathrm{dc}}}{\tilde{v}_{\mathrm{dc\_ref}}} = \frac{G_{\mathrm{comp}}G_{v_{\mathrm{dc}}v_{\mathrm{c}}}}{1 + G_{\mathrm{comp}}G_{v_{\mathrm{dc}}v_{\mathrm{c}}}} \tag{5.20}$$

where G_{comp} is the feedback controller to be designed and $G_{v_{dc}v_c}$ is given by equation (5.19). The low- and high-frequency response of $G_{v_{dc}v_c}$ can be approximated, respectively, as:

$$G_{v_{dc}v_c} \approx \begin{cases} \frac{1}{s} & \omega \ll \omega_n \\ G_{v_{dc}d} b_o^{-1} e^{-sT_d} & \omega \gg \omega_n \end{cases} \tag{5.21}$$

From equation (5.21), it can be observed that, at frequencies much lower than the observer's bandwidth, the uncompensated plant can be approximated as an integrator. Thus, a simple proportional (P) or proportional-derivative (PD) controller can be used as feedback controller to obtain zero steady-state error and the desired phase margin. Fig. 5.7 shows the bode plot of the compensated converter's loop gain with a proportional controller, which is designed to have a crossover frequency of 500 Hz with a phase margin of 87°.

It should be emphasized that, provided that the crossover frequency is significantly below ω_n, the compensated loop gain is insensitive to variations in ω_n, hence ω_n can be selected independently to meet certain transient response requirements without affecting the converter's stability condition.

5.3.3 Closed-Loop Output Impedance

From the control block diagram depicted in Fig. 5.5, the closed-loop output impedance of the DAB converter can be derived as given by equation (5.22) and plotted in Fig. 5.8 with ω_n as parameter. The closed-loop output impedance of the DAB converter under PI control with the same crossover frequency is included on the same plot for comparison.

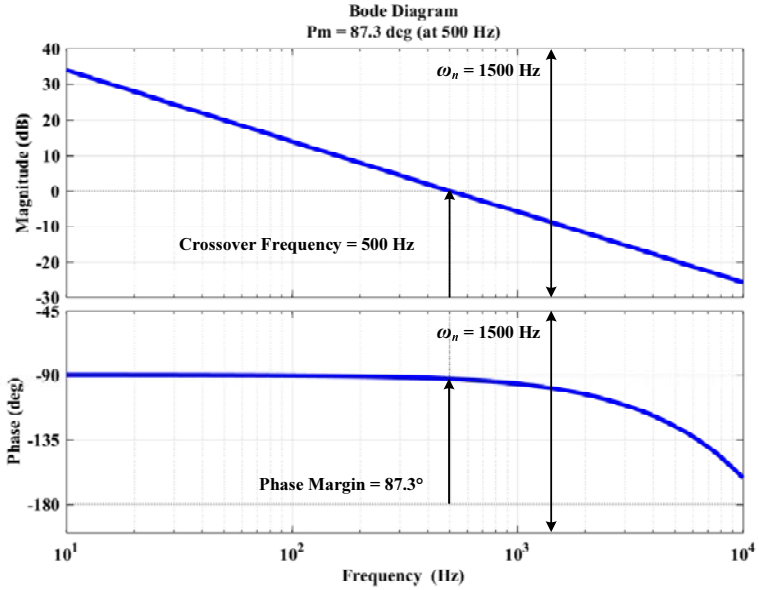


Figure 5.7: Bode plot of DAB converter's loop gain with proportional control and disturbance observer included.

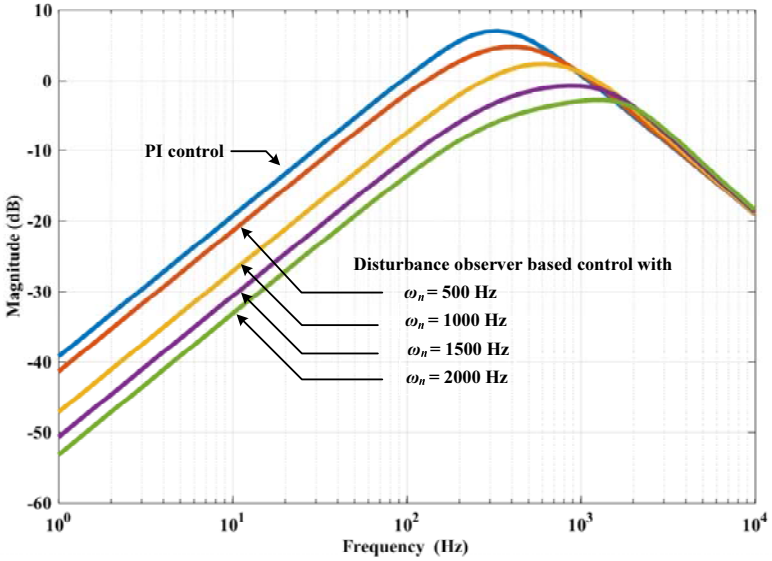


Figure 5.8: Closed-loop output impedance of the DAB converter with disturbance observer based control.

$$Z_{ocl} = \frac{\tilde{v}_{dc}}{-\tilde{i}_o} = \frac{G_{v_{dc}i_o}}{1 + \frac{(G_{fv_{dc}} + G_{comp})G_{v_{dc}d}e^{-sT_d}}{G_{f\mu}e^{-sT_d} + b_o}} \tag{5.22}$$

It can be seen that, despite having the same crossover frequency, the DAB converter under disturbance observer based control exhibits a lower closed-loop

output impedance than that under PI control at frequencies below the crossover frequency. In addition, a higher ω_n has a stronger attenuation effect on the closed-loop output impedance and its variation does not alter the crossover frequency, and hence the stability design, of the DAB converter appreciably. As a result, disturbance observer with a higher ω_n is expected to be more effective in mitigating the double-line frequency ripple on the dc-bus voltage.

5.3.4 Digital Implementation of the Proposed Control Method

For practical implementation on digital signal processor (DSP) the proposed disturbance observer designed in the s-domain is mapped to the z-domain by applying bilinear transformation (equation 5.23) to equation (5.15) and equation (5.16) and the result is given by equation (5.24) and equation (5.25).

$$s = \frac{2}{T_s}\frac{(z-1)}{z+1} \tag{5.23}$$

where $T_s = \frac{1}{f_s}$ is the sampling frequency, which is equal to the converter's switching frequency.

$$G_{f\mu}(z) = \frac{\hat{f}_t(z)}{\tilde{\mu}(z)} = \frac{B_0 + B_1 z^{-1} + B_2 z^{-2}}{1 + A_1 z^{-1} + A_2 z^{-2}} \tag{5.24}$$

$$G_{fv_{dc}}(z) = \frac{\hat{f}_t(z)}{\tilde{v}_{dc}(z)} = \frac{D_0 + D_1 z^{-1} + D_2 z^{-2}}{1 + C_1 z^{-1} + C_2 z^{-2}} \tag{5.25}$$

where $\tilde{\mu}(z)$ and $\tilde{v}_{dc}(z)$ is the input to the disturbance observer and $\hat{f}_t(z)$ is the output of the disturbance observer.

By applying the shifting property of the z-transform to equation (5.24) and equation (5.25) the linear difference equation for digital implementation can be obtained and is given by equation (5.26) and equation (5.27), where the coefficients of the difference equations in terms of the disturbance observer bandwidth,

damping ration and sampling frequency is given by equations (5.28)-(5.37) .

$$\hat{f}_t[n] = B_0\tilde{\mu}[n] + B_1\tilde{\mu}[n-1] + B_2\tilde{\mu}[n-2] - A_1\hat{f}_t[n-1] - A_2\hat{f}_t[n-2] \quad (5.26)$$

$$\hat{f}_t[n] = D_0\tilde{v}_{dc}[n] + D_1\tilde{v}_{dc}[n-1] + D_2\tilde{v}_{dc}[n-2] - C_1\hat{f}_t[n-1] - C_2\hat{f}_t[n-2] \quad (5.27)$$

$$B_0 = -\frac{T_s^2\ \omega_n^2\ b_o}{T_s^2\ \omega_n^2 + 4\zeta T_s\ \omega_n + 4} \quad (5.28)$$

$$B_1 = -\frac{2T_s^2\ \omega_n^2\ b_o}{T_s^2\ \omega_n^2 + 4\zeta T_s\ \omega_n + 4} \quad (5.29)$$

$$B_2 = -\frac{T_s^2\ \omega_n^2\ b_o}{T_s^2\ \omega_n^2 + 4\zeta T_s\ \omega_n + 4} \quad (5.30)$$

$$A_1 = \frac{2(T_s^2\ \omega_n^2 - 4)}{T_s^2\ \omega_n^2 + 4\zeta T_s\ \omega_n + 4} \quad (5.31)$$

$$A_2 = \frac{T_s^2\ \omega_n^2 - 4\zeta T_s\ \omega_n + 4}{T_s^2\ \omega_n^2 + 4\zeta T_s\ \omega_n + 4} \quad (5.32)$$

$$D_0 = \frac{2T_s\omega_n^2}{T_s^2\ \omega_n^2 + 4\zeta T_s\ \omega_n + 4} \quad (5.33)$$

$$D_1 = 0 \quad (5.34)$$

$$D_2 = -\frac{2T_s\omega_n^2}{T_s^2\ \omega_n^2 + 4\zeta T_s\ \omega_n + 4} \quad (5.35)$$

$$C_1 = \frac{2(T_s^2\ \omega_n^2 - 4)}{T_s^2\ \omega_n^2 + 4\zeta T_s\ \omega_n + 4} \tag{5.36}$$

$$C_2 = \frac{T_s^2\ \omega_n^2 - 4\zeta T_s\ \omega_n + 4}{T_s^2\ \omega_n^2 + 4\zeta T_s\ \omega_n + 4} \tag{5.37}$$

5.4 Experimental Results

To demonstrate the effectiveness of the designed controller, a DAB dc-dc converter prototype was designed and tested under two sets of experimental conditions. In the first experiment, a resistive load is connected to the DAB converter and step load changes are applied, while in the second experiment, the DAB converter is used to drive a single-phase inverter. Fig. 5.9 shows the photo of the experimental prototype, where the specifications of the DAB converter and the inverter are given in Table I. The output voltage of the DAB converter is sam-

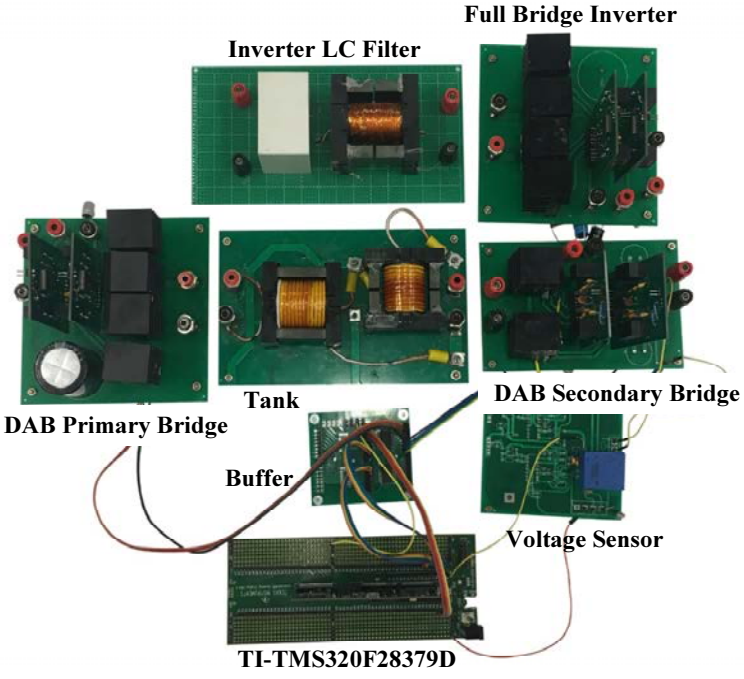


Figure 5.9: Photo of the experimental prototype.

Table 5.1: Specifications for the experimental prototype.

DAB Converter	
Input Voltage V_{in}	200 V
dc-bus Voltage V_{dc}	100 V
Rated Output Power P_{o}	250 W
Switching Frequency f_{s}	50 kHz
Turns Ratio N	2 : 1
Inductance L	160 μH
dc-bus Electrolytic Capacitor	150 μF
Controller	TI TMS320F28339D
Inverter	
Output Voltage V_o	50 V_{rms}
Modulator Frequency f_{m}	50 Hz
Carrier Frequency f_{c}	50 kHz
Filter Inductor L_{f}	500 μH
Filter Capacitor C_{f}	20 μF

pled using an isolated voltage sensor. The sensed analogue voltage signal is then converted to digital signal using the on-chip analogue-to-digital converter (ADC) of the TMS320F28379 digital signal processor (DSP). The algorithms for the PI controller and the disturbance observer are executed in the interrupt service routine at a fixed frequency, equal to the switching frequency of the converter. The output of the controller is fed to the on-chip digital-pulse-width modulator (PWM) to generate the switching signals for the primary and secondary bridges.

5.4.1 Experiment 1: Response to Step Load Change

Fig. 5.11a shows the transient response of the DAB converter under step load increase of 0.5A $\rightarrow$ 2.5A and a well-tuned PI controller with a crossover frequency of 500 Hz and a phase margin of 66° (c.f., Fig. 5.10). The peak voltage undershoot is 2.5 V and the settling time is approximately 1.6 ms. The transient response of

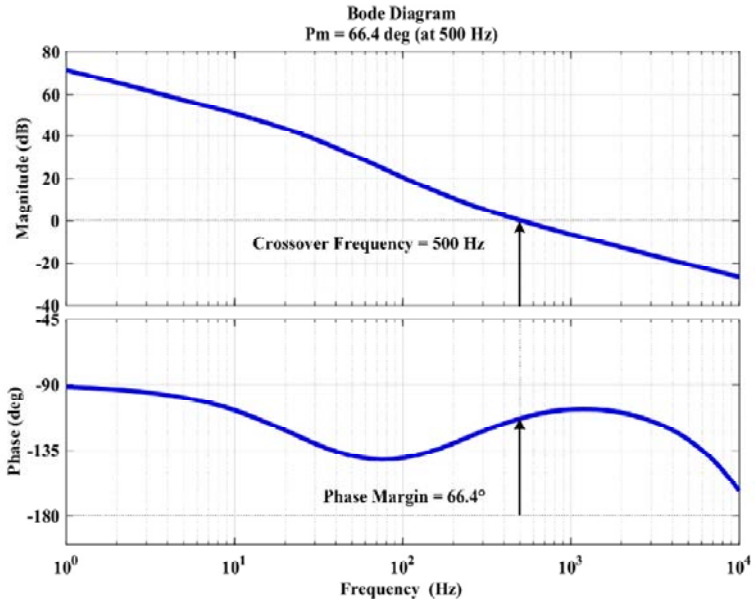
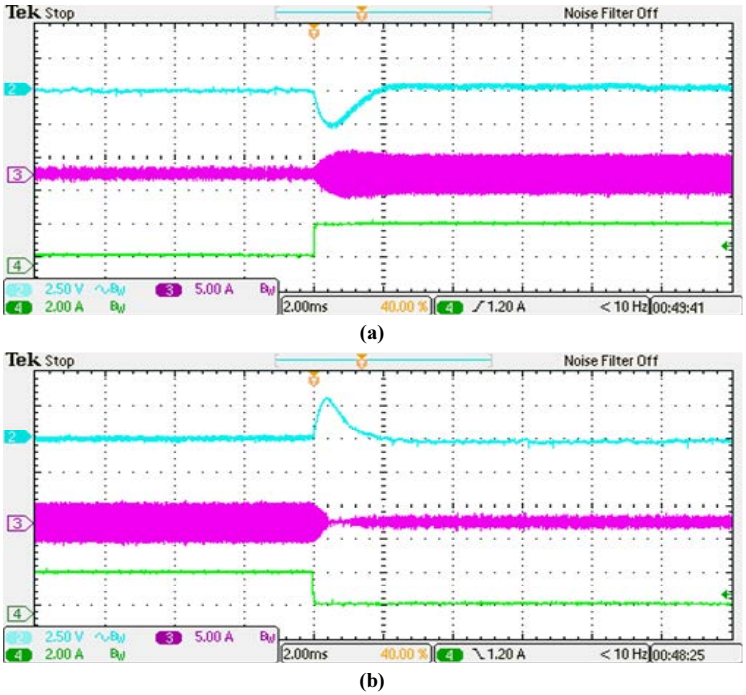


Figure 5.10: Bode plot of DAB converter's loop gain with PI control.

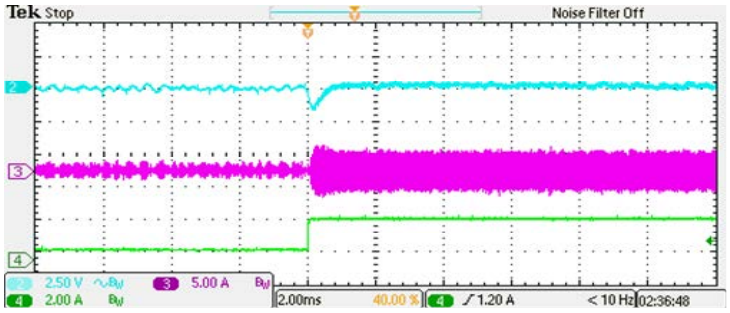


Time: 2ms/Div.
Top Trace (DC-bus voltage V_{dc}, AC coupled): 2.5V/Div.
Middle Trace (Inductor current I_L): 5A/Div.
Bottom Trace (Load current I_o): 2A/Div.

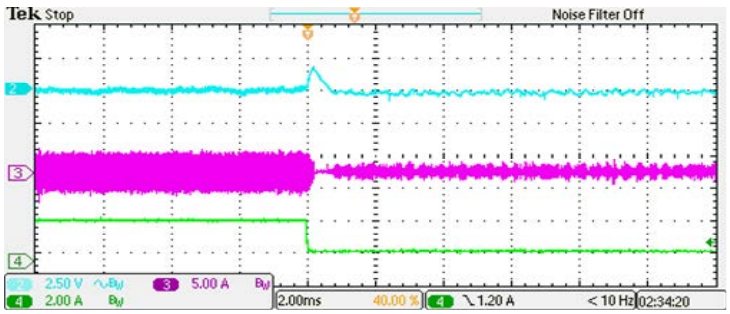
Figure 5.11: Measured transient response of the DAB converter to a step load change of 0.5A $\leftrightarrow$ 2.5A under PI control.

the DAB converter under step load decrease of 2.5A → 0.5A with the same PI controller is shown in Fig. 5.11b. The settling time is approximately 2 ms and the peak voltage overshoot is 3 V.

When disturbance observer based voltage-mode control is implemented on the DAB converter, the corresponding transient response under step load increase of 0.5A → 2.5A is shown in Fig. 5.12a with an observed voltage undershoot of only 1.5 V, which is reduced by 40% compared to the case with PI controller, and the settling time is reduced by 75% to 0.4 ms. A similar degree of improvement is observed in the transient response of the DAB converter under step load decrease of 2.5A → 0.5A, shown in Fig. 5.12b, from which a voltage overshoot of 2 V and a settling time of approximately 0.8 ms have been measured. Hence, the dynamic response of the DAB converter has been improved significantly with disturbance



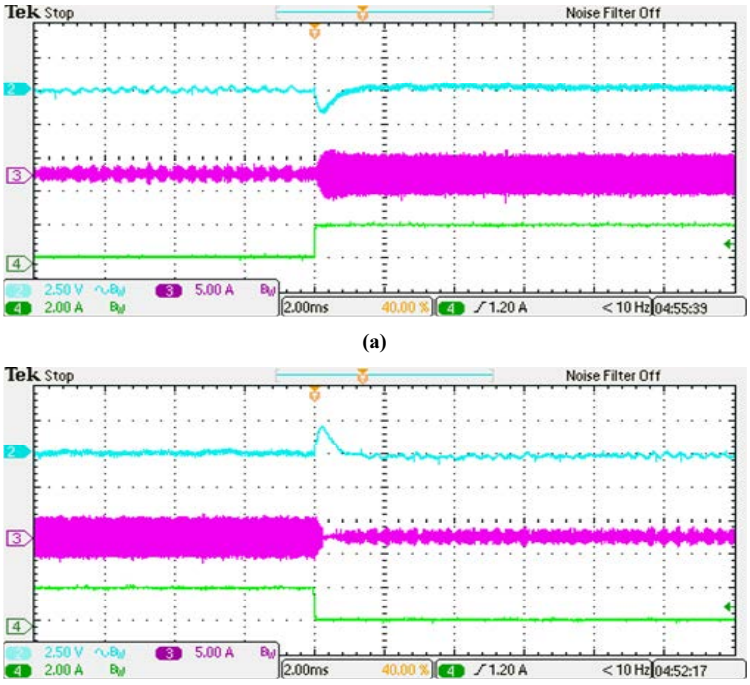
(a)



(b)

Time: 2ms/Div.
Top Trace (DC-bus voltage V_{dc}, AC coupled): 2.5V/Div.
Middle Trace (Inductor current I_L): 5A/Div.
Bottom Trace (Load current I_o): 2A/Div.

Figure 5.12: Measured transient response of the DAB converter to a step load change of 0.5A ↔ 2.5A under disturbance observer based voltage-mode control.



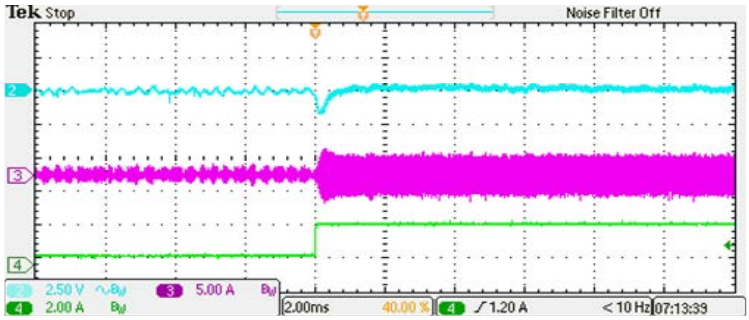
Time: 2ms/Div.
Top Trace (DC-bus voltage V_{dc}, AC coupled): 2.5V/Div.
Middle Trace (Inductor current I_L): 5A/Div.
Bottom Trace (Load current I_o): 2A/Div.

Figure 5.13: Measured transient response of the DAB converter to a step load change of 0.5A $\leftrightarrow$ 2.5A under disturbance observer based voltage-mode control and reduced controller's bandwidth.

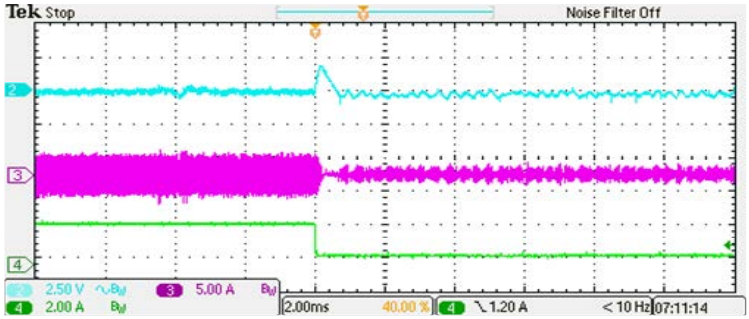
observer based control.

Fig. 5.13a and Fig. 5.13b show the step-up and step-down transient responses of the DAB converter with a step load change of 0.5A $\leftrightarrow$ 2.5A and 50% decrease in closed-loop bandwidth. It can be observed that in-spite of a 50% reduction in the closed-loop bandwidth, the DAB converter still exhibits similar undershoot and overshoot in output voltage during step load changes with very slight increase in settling time. This verifies the decoupling between the action of the proportional feedback control and that of the disturbance observer which is a form of feed-forward compensation. As a result, the feedback controller can be designed for stability by achieving certain specified phase margin and crossover frequency, while the disturbance observer is mainly employed to handle fast transient events.

Fig. 5.14 and Fig. 5.15 shows the transient responses of the DAB converter to a sequence of step load change 0.5A ↔ 2.5A with 20% decrease and increase in dc-bus capacitance respectively. It can be seen from the results that despite the large variation in the dc-bus capacitance the resulting undershoot and overshoot in output voltage remains essentially unchanged. Similarly from Fig. 5.16 it can be observed that with 20% decrease in input voltage and disturbance observer based control the transient response of the DAB converter virtually remains the same. These results confirm that the DAB converter's dynamic response is not sensitive to variations in converter's power-stage parameters and operating points under disturbance observer based control.



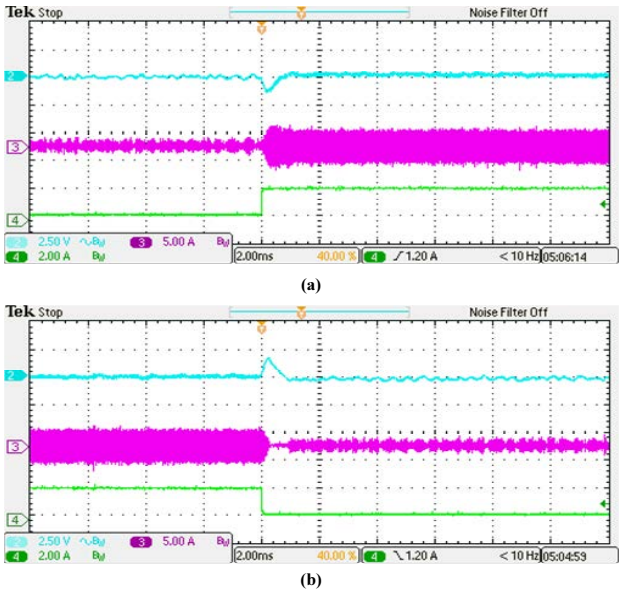
(a)



(b)

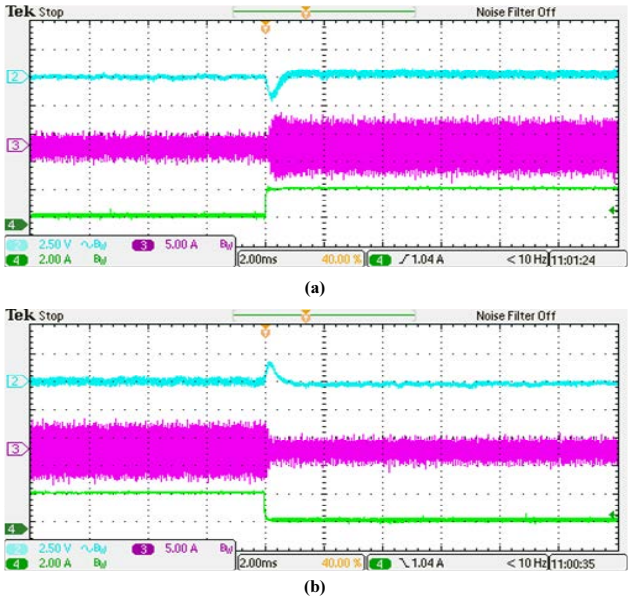
Time: 2ms/Div.
Top Trace (DC-bus voltage V_{dc}, AC coupled): 2.5V/Div.
Middle Trace (Inductor current I_L): 5A/Div.
Bottom Trace (Load current I_o): 2A/Div.

Figure 5.14: Measured transient response of the DAB converter to a step load change of 0.5A ↔ 2.5A under disturbance observer based voltage-mode control and 20% decrease in dc-bus capacitance.



Time: 2ms/Div.
Top Trace (DC-bus voltage V_{dc}, AC coupled): 2.5V/Div.
Middle Trace (Inductor current I_L): 5A/Div.
Bottom Trace (Load current I_o): 2A/Div.

Figure 5.15: Measured transient response of the DAB converter to a step load change of 0.5A ↔ 2.5A under disturbance observer based voltage-mode control and 20% increase in dc-bus capacitance.

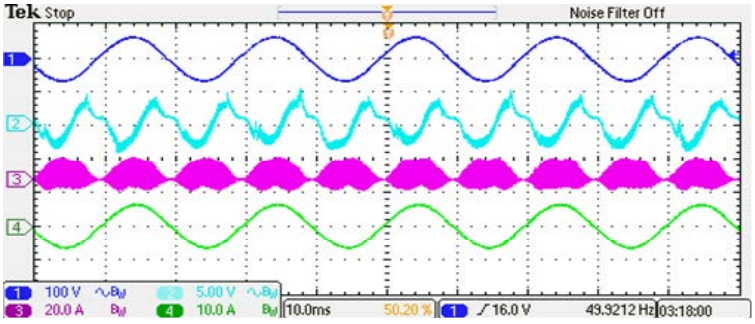


Time: 2ms/Div.
Top Trace (DC-bus voltage V_{dc}, AC coupled): 2.5V/Div.
Middle Trace (Inductor current I_L): 5A/Div.
Bottom Trace (Load current I_o): 2A/Div.

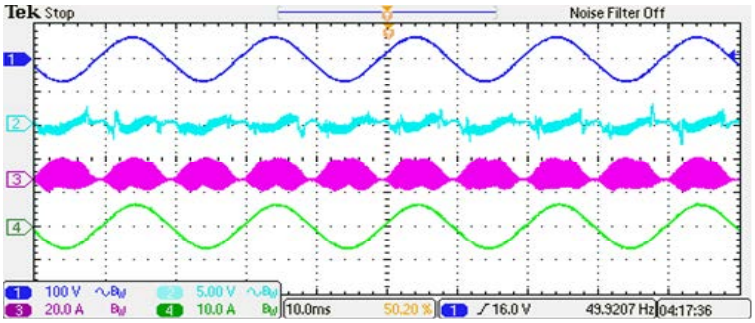
Figure 5.16: Measured transient response of the DAB converter to a step load change of 0.5A ↔ 2.5A under disturbance observer based voltage-mode control and 20% increase in input voltage.

5.4.2 Experiment 2: DAB Converter Driving a Single-Phase Inverter

In this experiment, a single-phase inverter is connected to the output of the DAB converter, and a resistive load of 10 Ω is connected to the output of the inverter. The steady-state waveforms of the DAB converter driving an inverter when its output voltage is regulated using a PI controller and a disturbance observer based voltage-mode controller is shown in Fig. 5.17a and Fig. 5.17b, respectively. In both figures, the top trace is the inverter's output voltage, the 2nd trace is the dc-bus voltage, the 3rd is the inverter's input current, and the bottom trace is the inverter's output current.



(a)



(b)

Time: 10ms/Div.
Top Trance(Inverter's output voltage, AC coupled): 100V/Div.
2nd Trace (DC-bus voltage, AC coupled): 5V/Div.
3rd Trace (Inverter's input current): 20A/Div.
Bottom Trace (Inverter's output current): 10A/Div.

Figure 5.17: Steady-state waveforms of DAB converter driving an inverter load when the dc-bus voltage is regulated by (a) PI control (b) disturbance observer based control.

It can be seen from Fig. 5.17a that, when the inverter is connected to the output of the DAB converter with its output voltage regulated by PI controller, there exists a significant double-line frequency ripple on the dc-bus voltage. The size of the ripple voltage on the dc-bus is closely correlated to the design of the PI controller which has to be designed to meet both stability and transient response requirements, hence some trade-offs in design are typically inevitable. On the contrary, with the implementation of disturbance observer based voltage-mode control, the double-line frequency ripple is effectively suppressed without additional hardware, as shown in Fig 5.17b. The reduction in the double-line frequency ripple on the dc-bus voltage can be more clearly visualized from the Fast Fourier Transform (FFT) analysis of the dc-bus voltage. Fig. 5.18a and Fig. 5.18b shows the FFT of the dc-bus voltage under PI control and disturbance observer based control, respectively. The effectiveness of the disturbance observer based control is verified by the over 50% reduction in the double-line frequency

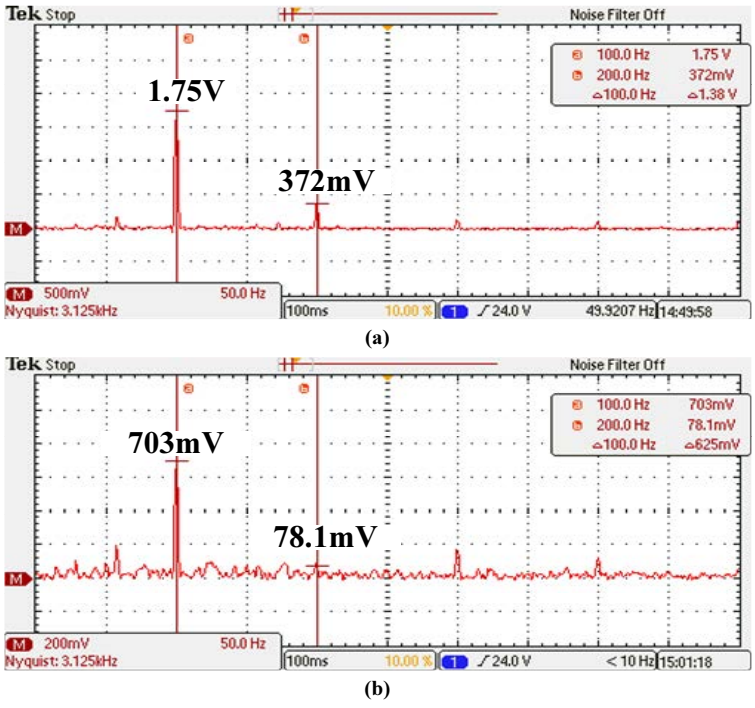
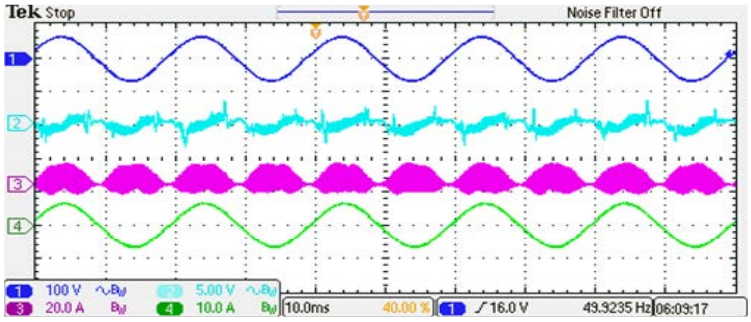


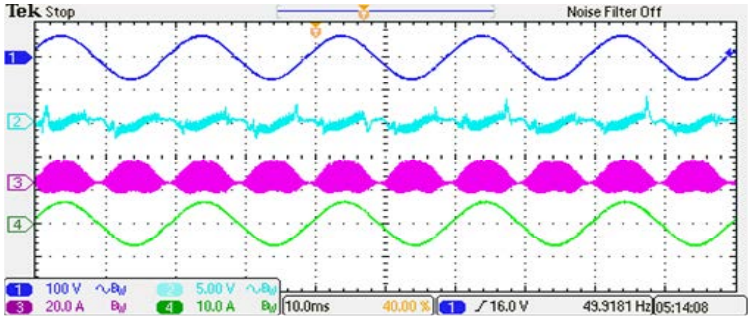
Figure 5.18: FFT spectrum of dc-bus voltage when the dc-bus voltage is regulated by (a) PI control (b) disturbance observer based control.

component compared to the case of PI control. Fig. 5.19a and Fig. 5.19b shows the steady-state waveforms of the DAB converter driving an inverter when the dc-bus voltage is regulated using a disturbance observer based voltage-mode controller with 20% decrease and increase in dc-bus capacitance, respectively. It can be seen from the results that despite variations in the dc-bus capacitance the dc-bus voltage ripple remains essentially unchanged.

Finally, Fig. 5.20a and Fig. 5.20b compare the FFT of the inverter's output voltage when the dc-bus voltage is regulated by PI control and disturbance observer based control, respectively. As expected, since there exists a significant double-line frequency component on the dc-bus voltage when it is regulated by PI control alone, it follows that a larger third-order frequency component arising



(a)



(b)

Time: 10ms/Div.
Top Trance(Inverter's output voltage, AC coupled): 100V/Div.
2nd Trace (DC-bus voltage, AC coupled): 5V/Div.
3rd Trace (Inverter's input current): 20A/Div.
Bottom Trace (Inverter's output current): 10A/Div.

Figure 5.19: Steady-state waveforms of DAB converter driving an inverter load when the dc-bus voltage is regulated by disturbance observer based control and variation in dc-bus capacitance (a) 20% decrease in dc-bus capacitance (b) 20% increase in dc-bus capacitance

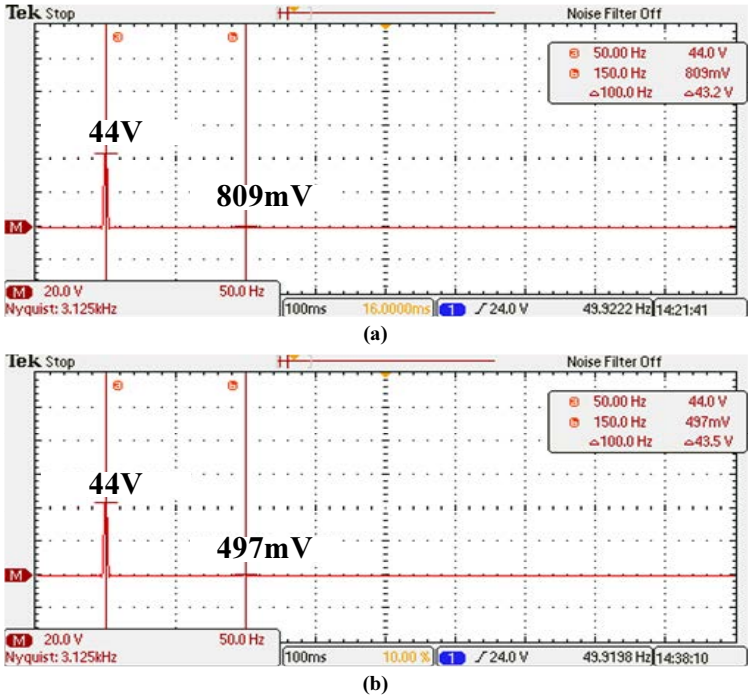


Figure 5.20: FFT spectrum of inverter's output voltage when the dc-bus voltage is regulated by (a) PI control (b) disturbance observer based control.

from the intermodulation of the fundamental component of the inverters output voltage and the double-line frequency ripple component in the DC-bus voltage also exists at the inverter's output voltage compared to the case of disturbance observer based control. In the latter case, the third-order frequency component has been reduced by more than 35%, in agreement with a similar level of reduction of the double-line frequency component on the dc-bus voltage when it is regulated by disturbance observer based control.

5.5 Conclusion

The problem of mitigating the double-line frequency ripple on the dc-bus voltage of a two-stage single-phase inverter system is addressed by means of disturbance observer based control. Specifically, a two-stage single-phase inverter system consisting of a DAB dc-dc converter driving a single-phase inverter is

studied. A disturbance observer is formulated by treating the lumped disturbance of the system as an extended state which is estimated and compensated in a feed-forward manner. With this control approach, the stability and transient response performance of the DAB converter can be optimized by designing its feedback and feed-forward (realized by disturbance observer) compensation independently of each other. The performance of disturbance observer based control is compared with that of conventional PI control, and it is experimentally verified that the former is capable of suppressing transient voltage overshoot/undershoot by 40% under step load changes and attenuating the double-line frequency ripple on the dc-bus voltage by over 50% under the experimental conditions studied.

Chapter 6

Enhancement of DC-Bus Voltage Regulation in Cascaded Converter System by a New Sensorless Load Current Feedforward Control Scheme

In Chapter 4, various control methods proposed in the literature for the enhancement of dynamic response of the front-end dc-dc converter are discussed. However, most of these control methods are based on the use of ideal small-signal converter model where model uncertainties and variations in converter's parameters are not taken into consideration. To address this drawback, a UDE-based dc-bus voltage control with current sensorless load current feedforward for a two-stage single-phase inverter system is proposed in this chapter. The proposed control method consists of a feedforward path, a UDE and a voltage feedback loop. The load current is estimated from the average current of the DAB's secondary bridge and lossless sensing of capacitor current is achieved using a digital

filter and the estimated load current is fed forward to achieve fast dynamic response. However, the estimation accuracy of the load current and calculation of the optimum feedforward gain depends on the values of circuit parameters which may be not known with high precision. Thus an UDE is used to compensate for model uncertainties and parameters variations, and the voltage feedback loop is designed to ensure good converter's stability. As compared to traditional single-loop voltage-mode control or voltage-mode control with load current feedforward, the proposed UDE-assisted current sensorless load current feedforward control results in an improved dynamic response performance and reduced dc-bus voltage ripple.

6.1 Analysis and Modeling of Two-Stage Single-Phase Inverter System

Fig. 6.1 depicts the circuit diagram of a two-stage single-phase inverter system comprising a DAB dc-dc converter and a single-phase inverter. Single-phase-shift (SPS) modulation (c.f., Fig. 6.2) is by far the most commonly used modulation method to modulate the output power of DAB converter. It can be seen from Fig. 6.2 that the primary (v_p) and the secondary (v_s) bridge voltages are phase shifted, and power flows from the bridge with a leading phase to the bridge with a lagging phase, and vice versa. The output power transferred from the leading bridge to the lagging bridge of a DAB converter is given by equation (6.1) [121–126].

$$P = \frac{nV_{in}V_{dc}d(1-d)}{2f_sL} \tag{6.1}$$

where V_{in} is the input voltage, V_{dc} is the dc-bus voltage, $n = \frac{n_p}{n_s}$ is the transformer's turns ratio, d is the phase-shift between v_p and v_s, L is the energy transfer inductance and f_s is the switching frequency. From equation (6.1), the

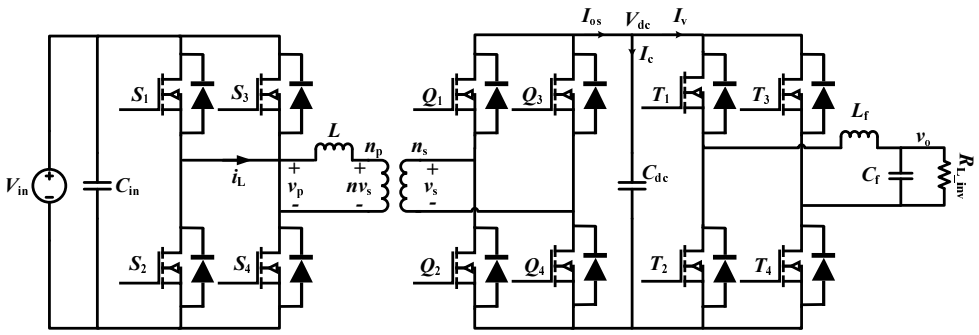


Figure 6.1: DAB dc-dc converter driving a single-phase inverter.

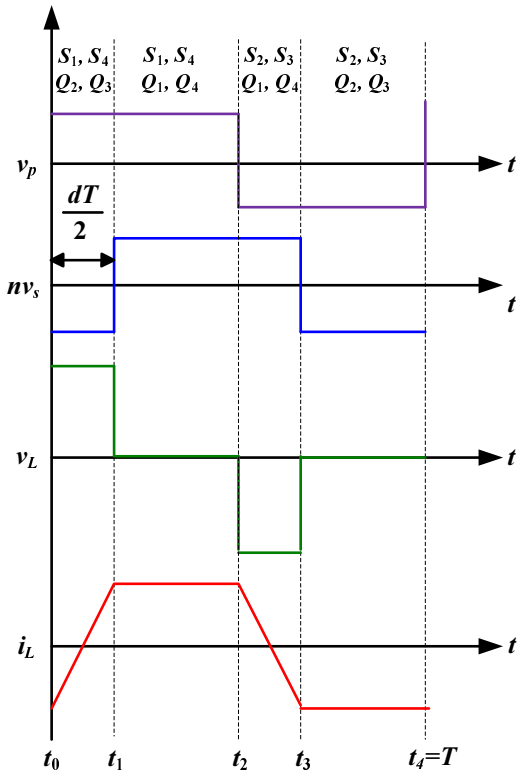


Figure 6.2: Operating waveforms of DAB converter under single-phase-shift modulation.

average output current I_{os} of the DAB converter secondary bridge is given by:

$$I_{os} = \langle i_{os} \rangle = \frac{nV_{in}d(1-d)}{2f_sL} \tag{6.2}$$

where $\langle\ \rangle$ denotes switching-frequency-averaged value.

The small-signal variation of $\langle i_{os} \rangle$, with respect to variation in d is derived by

taking the partial derivative of equation (6.2) with respect to d and the result is given by equation (6.3).

$$G_{i_{\mathrm{os}}d} = \frac{\tilde{i}_{\mathrm{os}}}{\tilde{d}} = \frac{nV_{\mathrm{in}}(1-2d)}{2f_sL} \tag{6.3}$$

The single-phase inverter shown in Fig. 6.1 is modulated by sinusoidal pulse-width modulation (SPWM) method and acts as load to the front-end DAB converter. From the viewpoint of UDE, the inverter load can be treated as an equivalent dc resistance R_{in_eq} given by equation (6.4) while the double-line frequency power fluctuation is regarded as a form of disturbance which will be estimated and compensated by the disturbance estimator to be discussed in Section 6.3.

$$R_{in\_eq} = \frac{V_{dc}^2 R_{L\_inv}}{V_{o\_rms}^2} \tag{6.4}$$

where V_{dc} is the dc-bus voltage, R_{L_inv} is the inverter's load resistance, and V_{o_rms} is the rms value of the inverter's output voltage.

From equation (6.3) and equation (6.4), the small-signal average model of the DAB converter driving a single-phase inverter can be obtained as shown in Fig. 6.3, where C_{dc} is the dc-bus capacitor, $\tilde{i}_{os}$ is the small-signal value of the output bridge current, $\tilde{i}_v$ and $\tilde{i}_o$ is the small-signal load current and small-signal perturbation to the load current, respectively. The small-signal open-loop control-to-bus voltage and output current-to-bus voltage transfer functions are derived from Fig. 6.3 and the results are given by equation (6.5) and equation (6.6), respectively.

$$G_{v_{dc}d} = \frac{\tilde{v}_{dc}}{\tilde{d}} = \frac{nV_{in}R_{in\_eq}(1-2d)}{2f_sL(1+sR_{in\_eq}C_{dc})} \tag{6.5}$$

$$G_{v_{dc}i_o} = \frac{\tilde{v}_{dc}}{-\tilde{i}_o} = \frac{R_{in\_eq}}{1+sR_{in\_eq}C_{dc}} \tag{6.6}$$

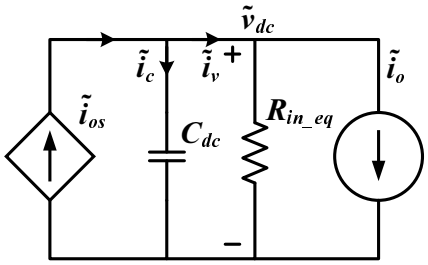


Figure 6.3: Small-signal model of DAB converter driving an inverter load.

6.2 Current Sensorless Load Current Feedforward

In conventional voltage-mode control, a PI controller is required to meet both dynamic response and stability requirements and it is challenging to optimize the design of PI controller for meeting these objectives simultaneously with one set of design parameters. Hence, there is always a trade-off between stability and dynamic response performance when PI control is used alone. To enhance the dynamic response performance of power converter to fast load transients without affecting stability, feedforward control has been proven to be an effective method. Fig. 6.4 shows the small-signal block diagram of a DAB converter with load current feedforward. Referring to Fig. 6.4, G_{comp} is the transfer function of the feedback compensator, e^{-sT_d} represents the delay due to digital implementation of the control algorithm, $G_{v_{dc}d}$ is the control-to-dc-bus voltage transfer function, $G_{v_{dc}i_o}$ is the load current-to-dc-bus voltage transfer function, $G_{i_{os}d}$ is the control-to-output bridge current transfer function, $G_{i_cv_{dc}}$ is the dc-bus voltage-to-capacitor current transfer function and K_{ff} is the load current feedforward gain.

From Fig. 6.4, the closed-loop output impedance of the DAB converter (i.e. the transfer function from $\tilde{i}_o$ to $\tilde{v}_{dc}$) can be derived as given by equation (6.7).

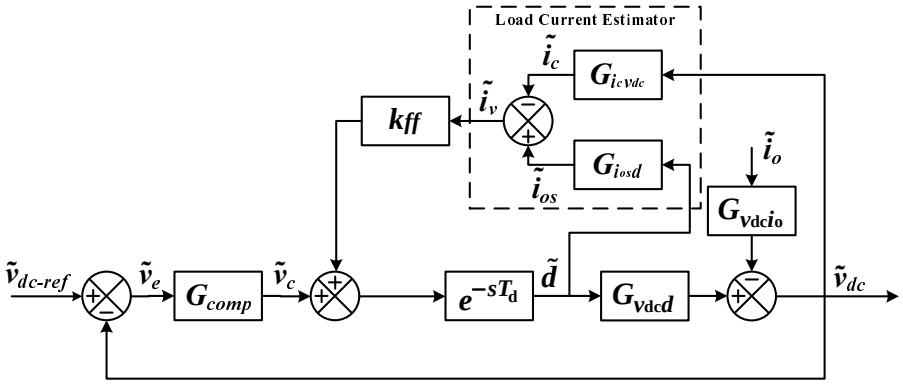


Figure 6.4: Closed-loop Small-signal block diagram of DAB converter driving an inverter load with load current feedforward.

$$Z_{oc} = \frac{\tilde{v}_{dc}}{-\tilde{i}_o} = \frac{G_{v_{dc}i_o}}{1 + \frac{(G_{comp}+k_{ff}G_{i_c v_{dc}})G_{v_{dc}d}e^{-sT_d}}{1-K_{ff}G_{i_{os}d}e^{-sT_d}}} \tag{6.7}$$

By setting the closed-loop output impedance of the DAB converter equal to zero, the optimal feedforward gain can be obtained as

$$k_{ff} = \frac{1}{e^{-sT_d}G_{i_{os}d}} \tag{6.8}$$

Substituting the transfer functions $G_{i_{os}d}$ from equation (6.3) into equation (6.8), and ignoring the delay term for $\omega T_d \ll 1$, the optimal feedforward gain can be obtained as follows:

$$k_{ff} = \frac{2f_s L}{nV_{in}(1-2d)} \tag{6.9}$$

It can be seen from equation (6.9) that the optimal load current feedforward gain for the DAB converter requires the values of the energy transfer inductance, input voltage, and transformer turns ratio.

To implement load current feedforward control, information of the load current is required. The most direct method to obtain load current information is by using a current-sense resistor or a Hall-effect sensor. However, the former

will incur additional losses while the latter will require an extra current sensor which increases cost and bulkiness. An alternative method to obtain load current information without using additional sensor, and therefore does not incur additional losses, is to estimate the load current from the output bridge current and capacitor current according to equation (6.10).

$$\tilde{i}_v = \tilde{i}_{os} - \tilde{i}_c \tag{6.10}$$

where $\tilde{i}_v$ is the average load current, $\tilde{i}_c$ is the average capacitor current and $\tilde{i}_{os}$ is the average output current of the DAB converter's secondary bridge and is given by equation (6.3).

To estimate the capacitor current without current sensor, the method shown in Fig. 6.5 based on the well-known impedance matching principle is applied [57,138–140]. For the R_sC_s network shown in Fig. 6.5a, the following relationship can be obtained.

$$\tilde{v}_{RS} = \tilde{i}_c R_{c_{dc}} \left(\frac{1 + \frac{1}{sR_{c_{dc}}C_{dc}}}{1 + \frac{1}{sR_sC_s}} \right) \tag{6.11}$$

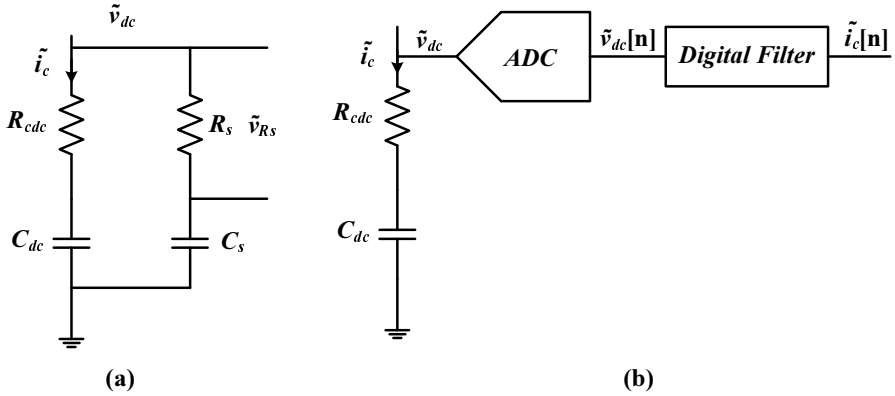


Figure 6.5: Current sensorless capacitor current sensing.

$$G_{i_c v_{dc}} = \frac{\tilde{i}_c}{\tilde{v}_{dc}} = \frac{1}{R_{c_{dc}}(1 + \frac{1}{sC_{dc}R_{cdc}})} \tag{6.12}$$

From equation (6.11), it can be deduced that if the time constant of the dc-bus capacitor matches the time constant of the sensing network, the voltage across the sense resistor $\tilde{v}_{RS}$ becomes a scaled version of the capacitor current. However, it is not practically feasible to know the time constant of the dc-bus capacitor with high precision (e.g. both capacitance and ESR are sensitive to operating temperature), and therefore such a current sense method is always prone to error. In this paper, this error is estimated and compensated by an UDE which is used to enhance the robustness of the proposed control scheme, and its design and implementation will be discussed in the next section.

In digital implementation, the analog R_sC_s filter is replaced by a digital filter as shown in Fig. 6.5b and the dc-bus voltage is sensed and passed through a digital filter having a time constant equal to that of the dc-bus capacitor. By applying bilinear-transformation to equation (6.12), the "sensed" capacitor current can be expressed as follows:

$$\tilde{i}_c[n] = C_1\tilde{i}_c[n-1] + C_2(\tilde{v}_{dc}[n] - \tilde{v}_{dc}[n-1]) \tag{6.13}$$

with

$$C_1 = \frac{(2R_{c_{dc}}C_{dc} - T_s)}{(2R_{c_{dc}}C_{dc} + T_s)} \qquad C_2 = \frac{2C_{dc}}{(2R_{c_{dc}}C_{dc} + T_s)}$$

6.3 UDE Assisted Sensorless Load Current Feedforward for DC-Bus Voltage Regulation

The performance of load current feedforward control is expected to be optimal when the feedforward gain is optimal and the "sensed" load current information is accurate. However, the optimality of the selected feedforward gain is not always guaranteed due to parameter variations and model uncertainties such as the effects of un-modeled parasitic components. For this reason, in this work, an UDE-assisted sensorless load current feedforward control method for DAB converter driving an inverter is proposed to enhance the DAB converter's dynamic response performance and reduce the amplitude of the double-line frequency ripple component in the dc-bus voltage. The block diagram of the proposed UDE-assisted sensorless load current feedforward control is shown in Fig. 6.6 where the load current is estimated using equation (6.10) and equation (6.13), and a feedforward control signal is added to the output of the voltage loop's feedback compensator. In addition to this, an UDE is used to estimate the total lumped disturbance due to model uncertainties and parameter variations with the aim to achieve a robust and tight control of the dc-bus voltage. From Fig. 6.3, the dc-bus capacitor dynamics can be expressed as follows using Kirchhoff's current law:

$$\frac{\mathrm{d}\tilde{v}_{dc}}{\mathrm{d}t} = -\frac{\tilde{v}_{dc}}{R_{in\_eq}C_{dc}} + \frac{nV_{in}(1-2d)}{2f_sLC_{dc}}\tilde{d} \tag{6.14}$$

which can be rearranged as equation (6.15)

$$\dot{\tilde{v}}_{dc} = a\tilde{v}_{dc} + b\tilde{d} \tag{6.15}$$

where

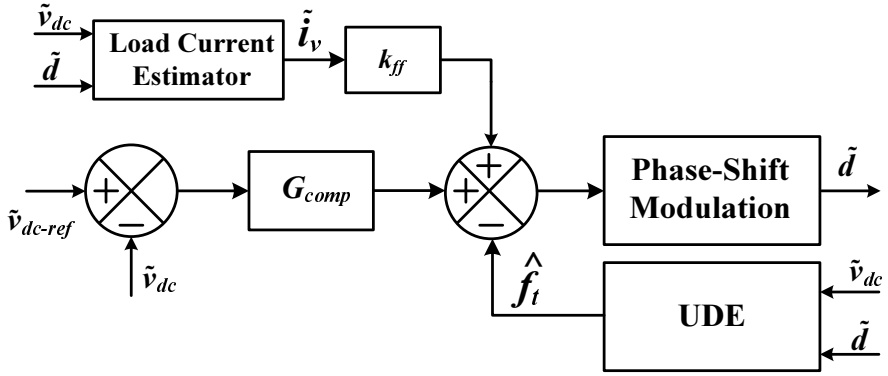


Figure 6.6: Block diagram of UDE-assisted sensorless load feedforward for dc-bus voltage regulation.

$$a = -\frac{1}{R_{in\_eq}C_{dc}} \qquad b = \frac{nV_{in}(1-2d)}{2f_sLC_{dc}}$$

Equation (6.15) can be amended to include the effects of disturbance by adding a lumped disturbance term f_t.

$$\dot{\tilde{v}}_{dc} = a\tilde{v}_{dc} + b\tilde{d} + f_t \tag{6.16}$$

where $f_t = \Delta a\tilde{v}_{dc} + \Delta b\tilde{d}$. Hence, the total lumped uncertainty and disturbance can be estimated from equation (6.16) as follows [141–143]:

$$f_t = \dot{\tilde{v}}_{dc} - a\tilde{v}_{dc} - b\tilde{d} \tag{6.17}$$

However, the derivative state variable $\dot{\tilde{v}}_{dc}$ cannot be measured directly, hence it is estimated using an UDE represented by equation (6.18).

$$\hat{f}_t = f_t \star g_f \tag{6.18}$$

where $\star$ is the convolution operator and g_f is the impulse response of a low-pass filter $G_f(s)$ given by equation (6.19).

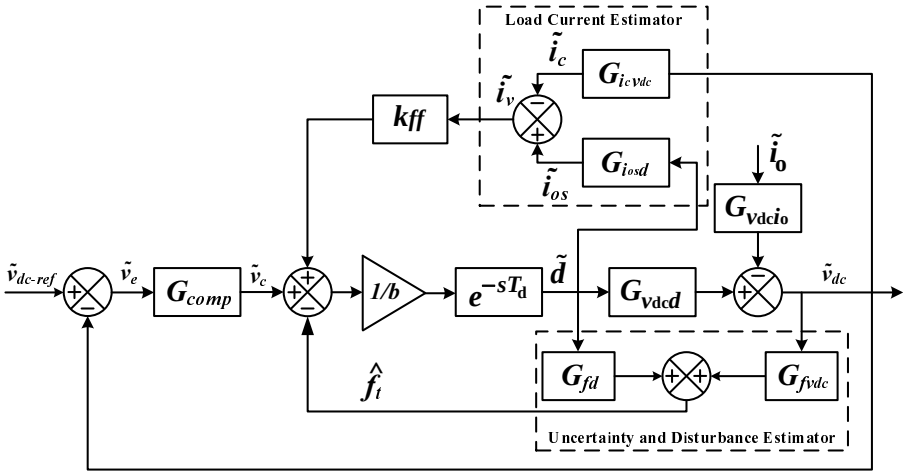


Figure 6.7: Small-signal block diagram of UDE-based dc-bus voltage control with estimated load current feedforward.

$$G_f(s) = \frac{1}{1 + \frac{s}{\omega_{fc}}} \tag{6.19}$$

Taking the Laplace transform of equation (6.18) gives

$$\hat{f}_t(s) = \frac{(s-a)}{1 + \frac{s}{\omega_{fc}}}\tilde{v}_{dc} - \frac{b}{1 + \frac{s}{\omega_{fc}}}\tilde{d} = G_{fv_{dc}}\tilde{v}_{dc} + G_{fd}\tilde{d} \tag{6.20}$$

Based on equation (6.20), the small-signal block diagram of the DAB converter with UDE-assisted sensorless load current feedforward control is shown in Fig. 6.7.

6.3.1 Feedback Controller Design

The feedback controller of the DAB converter is designed in this section in frequency domain. The UDE estimates the total lumped disturbances by using the sensed dc-bus voltage $\tilde{v}_{dc}$ and the phase-shift $\tilde{d}$ as inputs. From equation (6.20), the s-domain transfer function from the control signal $\tilde{d}$ to the estimated lumped disturbances $\hat{f}_t$ and from the dc-bus voltage $\tilde{v}_{dc}$ to the estimated lumped disturbances $\hat{f}_t$ can be derived as given by equation (6.21) and equation (6.22), respectively. From the small-signal control block diagram of the DAB converter

depicted in Fig. 6.7, the transfer function from the control signal $\tilde{v}_c$ to the dc-bus voltage $\tilde{v}_{dc}$ is given by equation (6.23).

$$G_{fd} = \frac{\hat{f}_t}{\tilde{d}} = -\frac{b}{1+\frac{s}{\omega_{fc}}} \tag{6.21}$$

$$G_{fv_{dc}} = \frac{\hat{f}_t}{\tilde{v}_{dc}} = \frac{(s-a)}{1+\frac{s}{\omega_{fc}}} \tag{6.22}$$

$$G_{v_{dc}v_c} = \frac{\tilde{v}_{dc}}{\tilde{v}_c} = \frac{G_{v_{dc}d}b^{-1}e^{-sT_d}}{1+G_{v_{dc}d}b^{-1}e^{-sT_d}(G_{fd}G_{v_{dc}d}^{-1}+G_{fv_{dc}})} \tag{6.23}$$

Substituting the transfer functions G_{fd} and $G_{fv_{dc}}$ from equation (6.21) and equation (6.22) into equation (6.23) gives

$$G_{v_{dc}v_c} = \frac{\tilde{v}_{dc}}{\tilde{v}_c} = \frac{G_{v_{dc}d}b^{-1}e^{-sT_d}}{1-\frac{e^{-sT_d}}{1+\frac{s}{\omega_{fc}}}+\frac{(s-a)}{1+\frac{s}{\omega_{fc}}}(G_{v_{dc}d}b^{-1}e^{-sT_d})} \tag{6.24}$$

For $\omega \ll \omega_{fc}$, equation (6.24) can be approximated as follows (ω_{fc} is selected to be 5 times of the compensated loop gain's crossover frequency)

$$G_{v_{dc}v_c} = \frac{\tilde{v}_{dc}}{\tilde{v}_c} \approx \frac{1}{(s-a)} \tag{6.25}$$

From equation (6.25) it can be concluded that the modified plant has a dominant pole open-loop characteristics, thus a simple PI controller can be used to obtain the desired phase margin and zero steady-state error. Fig. 6.8 shows the compensated loop-gain with a phase margin of 69° and a crossover frequency of 200Hz.

6.3.2 Closed-Loop Output Impedance

In this section, the effect of the UDE-assisted sensorless load current feedforward control on the closed-loop output impedance of the front-end DAB dc-dc

converter is investigated. Based on the small-signal block diagram of Fig. 6.7, the DAB converter's closed-loop output impedance can be derived as given by equation (6.26). Fig. 6.9 shows the calculated DAB converter closed-loop output impedance under different control schemes. For a fair comparison, the same PI controller's parameters are used in all cases. From the figure, it can be seen that when the dc-bus voltage is regulated by the proposed control scheme, the DAB converter's closed-loop output impedance has been attenuated significantly and is consistently the lowest at all frequencies among all the control schemes considered. Next, the proposed control scheme is validated experimentally on hardware prototype.

$$Z_{ocl} = \frac{\tilde{v}_{dc}}{-\tilde{i}_o} = \frac{G_{v_{dc}i_o}}{1 + \frac{(G_{comp}+G_{fv_{dc}}+G_{ic}v_{dc}k_{ff})G_{v_{dc}d}e^{-sT_d}}{b+G_{fd}e^{-sT_d}-G_{iosd}k_{ff}e^{-sT_d}}} \tag{6.26}$$

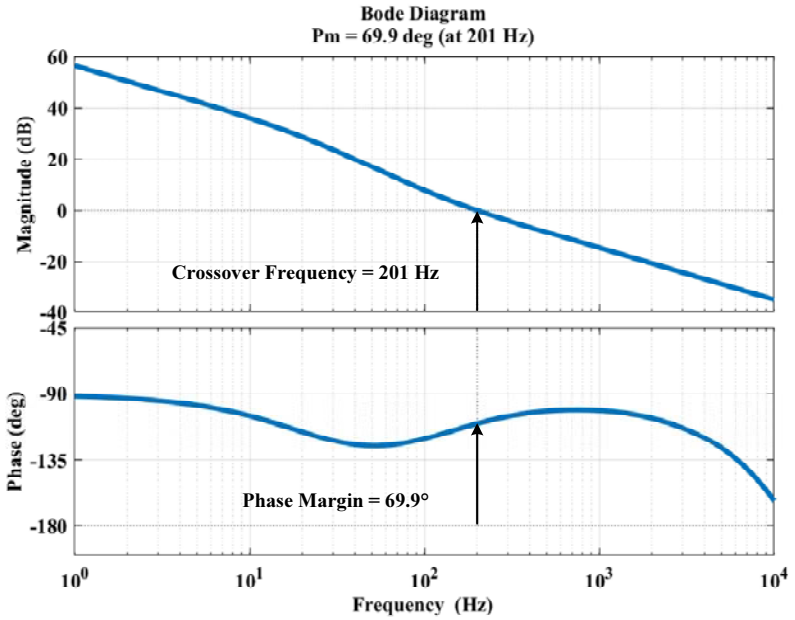


Figure 6.8: Bode plot of converter's loop gain with UDE-assisted sensorless load current feedforward control.

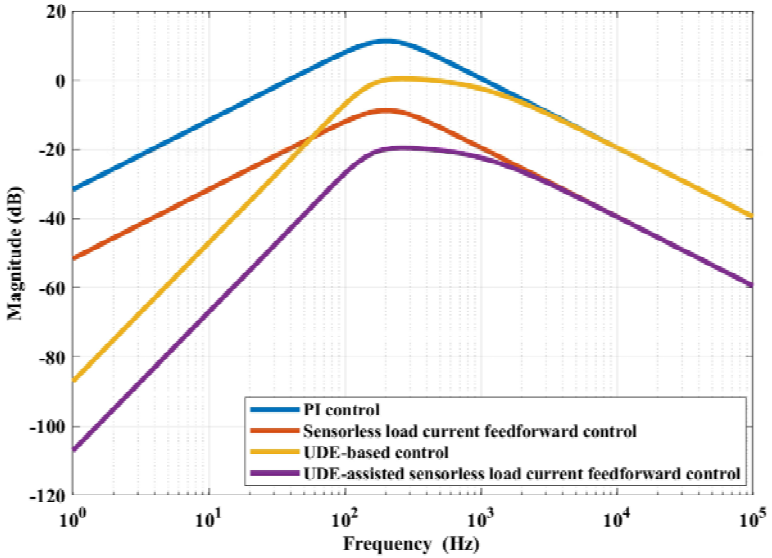


Figure 6.9: Closed-loop output impedance of DAB converter under different control schemes.

6.3.3 Digital Implementation of the Proposed Control Method

The uncertainty and disturbance estimator (UDE) designed in frequency domain can be implemented on digital signal processor (DSP) by applying bilinear-transformation (equation 6.27) to equation (6.21) and equation (6.22) and the result is given by equation (6.28) and equation (6.29).

$$s = \frac{2}{T_s}\frac{(z-1)}{z+1} \tag{6.27}$$

where $T_s = \frac{1}{f_s}$ is the sampling frequency, which is equal to the converter's switching frequency.

$$G_{fd}(z) = \frac{\hat{f}_t(z)}{\tilde{d}(z)} = \frac{B_0 + B_1 z^{-1}}{1 + A_1 z^{-1}} \tag{6.28}$$

$$G_{fv_{dc}}(z) = \frac{\hat{f}_t(z)}{\tilde{v}_{dc}(z)} = \frac{D_0 + D_1 z^{-1}}{1 + C_1 z^{-1}} \tag{6.29}$$

where $\tilde{d}(z)$ and $\tilde{v}_{dc}(z)$ is the input to the UDE and $\hat{f}_t(z)$ is the output of the

UDE.

By applying the shifting property of the z-transform to equation (6.28) and equation (6.29) the linear difference equation for digital implementation can be obtained and is given by equation (6.30) and equation (6.31), where the coefficients of the difference equations is given by equations (6.32)-(6.37) .

$$\hat{f}_t[n] = B_0\tilde{d}[n] + B_1\tilde{d}[n-1] - A_1\hat{f}_t[n-1] \tag{6.30}$$

$$\hat{f}_t[n] = D_0\tilde{v}_{dc}[n] + D_1\tilde{v}_{dc}[n-1] - C_1\hat{f}_t[n-1] \tag{6.31}$$

$$B_0 = -\frac{T_s\omega_{fc}b}{T_s\omega_{fc}+2} \tag{6.32}$$

$$B_1 = -\frac{T_s\omega_{fc}b}{T_s\omega_{fc}+2} \tag{6.33}$$

$$A_1 = \frac{T_s\omega_{fc}-2}{T_s\omega_{fc}+2} \tag{6.34}$$

$$D_0 = \frac{2\omega_{fc}-T_s\omega_{fc}a}{T_s\omega_{fc}+2} \tag{6.35}$$

$$D_1 = -\frac{(2\omega_{fc}+T_s\omega_{fc}a)}{T_s\omega_{fc}+2} \tag{6.36}$$

$$C_1 = \frac{T_s\omega_{fc}-2}{T_s\omega_{fc}+2} \tag{6.37}$$

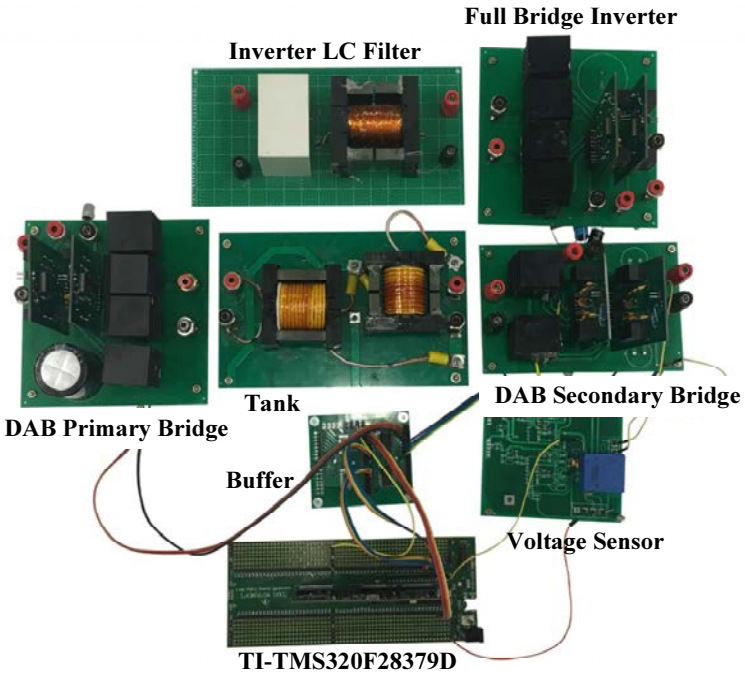


Figure 6.10: Hardware prototype of a two-stage single-phase inverter system.

6.4 Experimental Results

The proposed control scheme is implemented on a DAB dc-dc converter in two different configurations to validate its effectiveness. In the first configuration, a resistive load is directly connected at the output of the DAB converter, while in the second configuration a single-phase inverter is connected as a load at the output of the DAB converter. The nominal parameters of the DAB dc-dc converter and the single-phase inverter are listed in Table 6.1. The control algorithm is implemented digitally on a digital signal processor (DSP) (TMS320F28339D). The DSP has an on-chip analog-to-digital (ADC) and a pulse-width modulator (PWM). The dc-bus voltage is sampled using an analog voltage sensor and is converted to a digital signal using the on-chip ADC of the DSP. The control algorithm is then executed at a fixed frequency in the interrupt service routine. Based on the output of the control algorithm, the on-chip PWM is used to generate the switching signals for the DAB converter's MOSFETs.

Table 6.1: Specifications of experimental prototype.

DAB Converter	
Input Voltage V_{in}	200 V
DC-bus Voltage V_{dc}	100 V
Rated Output Power P_{o}	250 W
Switching Frequency f_{s}	50 kHz
Turns Ratio n	2 : 1
Inductance L	160 μH
DC-bus Electrolytic Capacitor	150 μF
Controller	TI TMS320F28339D
Inverter	
Output Voltage V_o	50 V_{rms}
Modulator Frequency f_{m}	50 Hz
Carrier Frequency f_{c}	50 kHz
Filter Inductor L_{f}	500 μH
Filter Capacitor C_{f}	20 μF

6.4.1 Dynamic Response Performance to Step Load Change

Fig. 6.12a and Fig. 6.12b shows the step-down and step-up dynamic responses of the DAB converter when the dc-bus voltage is regulated by using a well-tuned PI controller with a crossover frequency of 200 Hz and phase margin of

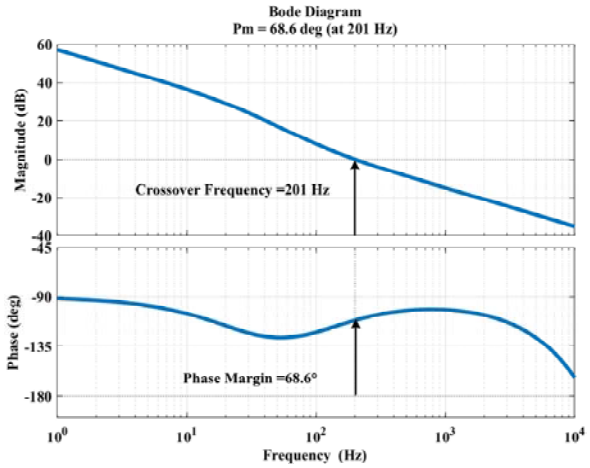
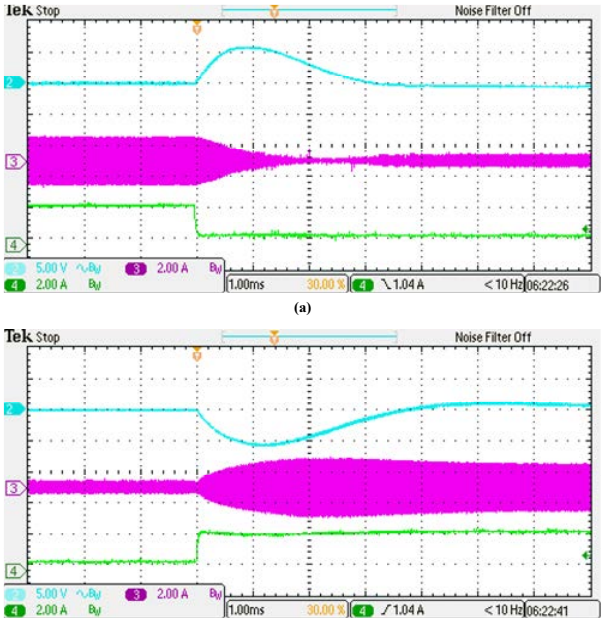
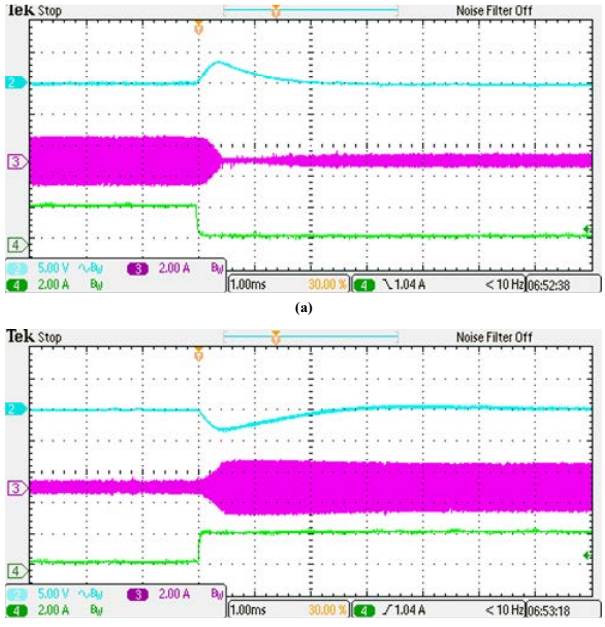


Figure 6.11: Bode plot of DAB converter's loop gain with PI control.



Time: 1ms/Div.
Top Trace (DC-bus Voltage, AC Coupled): 5V/Div.
Middle Trace (Inductor Current): 2A/Div.
Bottom Trace (Load Current): 2A/Div.

Figure 6.12: Step response of DAB converter with PI control.



Time: 1ms/Div.
Top Trace (DC-bus Voltage, AC Coupled): 5V/Div.
Middle Trace (Inductor Current): 2A/Div.
Bottom Trace (Load Current): 2A/Div.

Figure 6.13: Step response of DAB converter with sensorless load current feedforward.

68° (c.f., Fig. 6.11). The maximum overshoot and undershoot of the dc-bus voltage is approximately 6 V with a settling time of approximately 3 ms. The dynamic response of the DAB converter to a step load change of 0.5A $\leftrightarrow$ 2.5A with sensorless load current feedforward control only is shown in Fig. 6.13, where the maximum overshoot and undershoot of the dc-bus voltage is reduced to 4 V and the settling time is reduced to 2 ms. Fig. 6.14 shows the dynamic response of the DAB converter when the dc-bus voltage is regulated using UDE-based control alone (i.e. without load current feedforward). The DAB converter's dynamic response is improved as compared to that of the previous two cases in term of voltage overshoot/undershoot and settling time.

The dynamic response of the DAB converter is further improved when UDE-based control is combined with current sensorless load current feedforward as shown in Fig. 6.15. The maximum overshoot and undershoot of the dc-bus voltage is reduced to 2 V with a settling time of only 0.6 ms, or 1/5 of that resulted

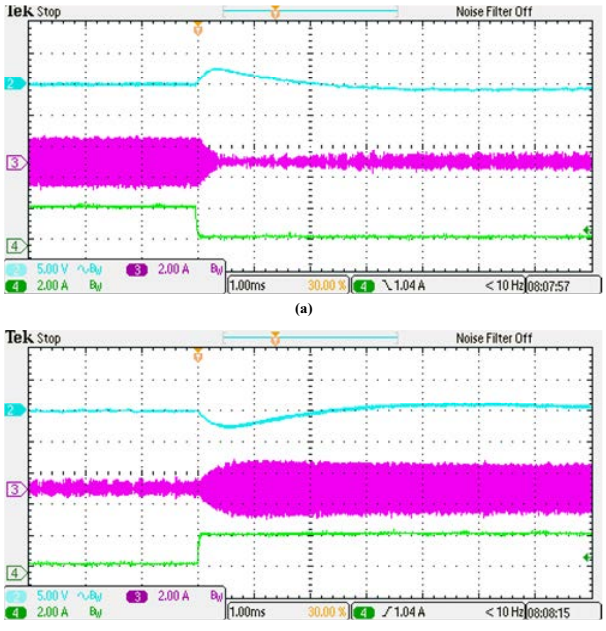


Figure 6.14: Step response of DAB converter with UDE-based control only.

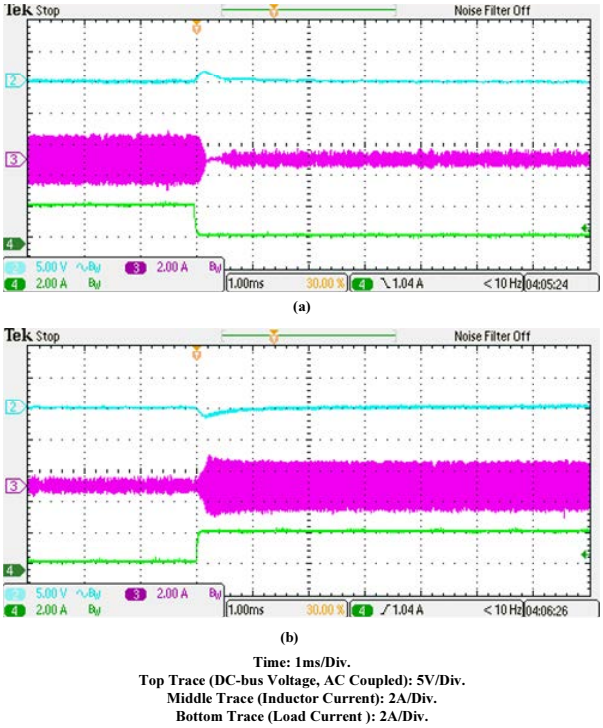


Figure 6.15: Step response of DAB converter with UDE-assisted sensorless load current feedforward control.

from PI control. From these results, it can be concluded that the DAB converter has the most sluggish dynamic response performance when the dc-bus voltage is regulated by using conventional PI control. The DAB converter exhibits improved dynamic response when either or both of the sensorless load current feedforward control and UDE-based control are implemented. However, the best dynamic response performance is exhibited by the combined effect of these two control schemes. The reasons for this is that any nonidealities that may affect the effectiveness of load current feedforward control are compensated in large part by the compensative actions of the UDE, making it approach the performance of an optimal feedforward controller.

Fig. 6.16 and Fig. 6.17 shows the transient waveforms of the DAB converter when the dc-bus voltage is regulated by using UDE-assisted sensorless load current feedforward control and 20% decrease in L and C_{dc}, respectively. From these waveforms, it can be seen that in spite of large variations in converter's pa-

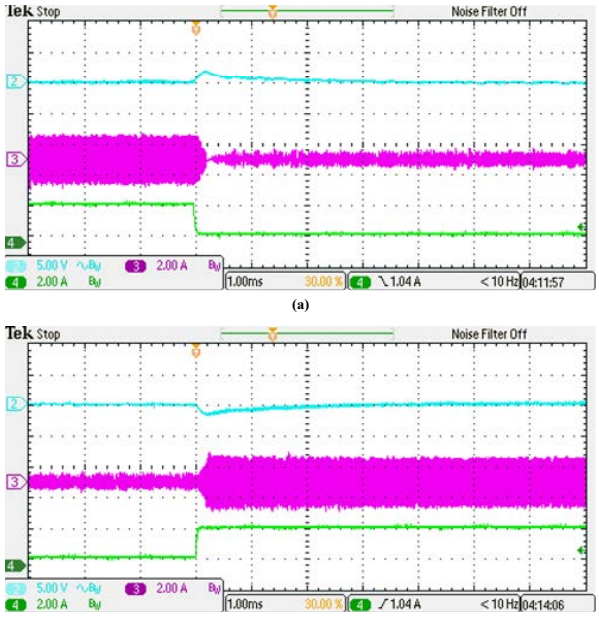


Figure 6.16: Step response of DAB converter with UDE-assisted sensorless load current feedforward control and 20% decrease in the value of L.

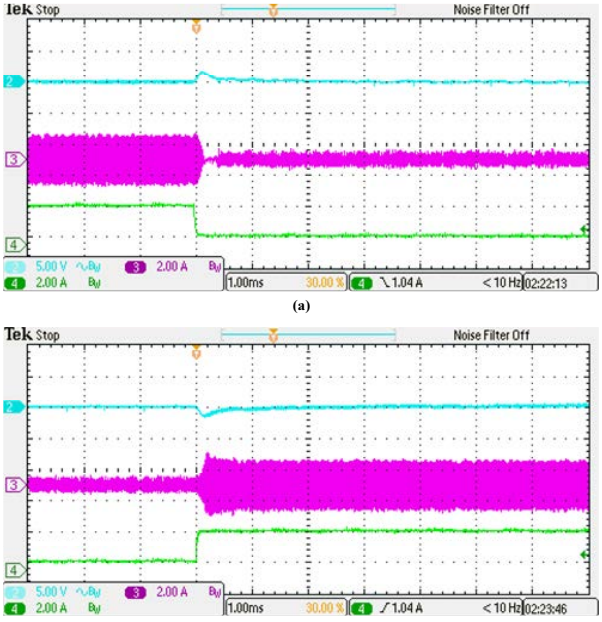


Figure 6.17: Step response of DAB converter with UDE-assisted sensorless load current feedforward control and 20% decrease in C_{dc}.

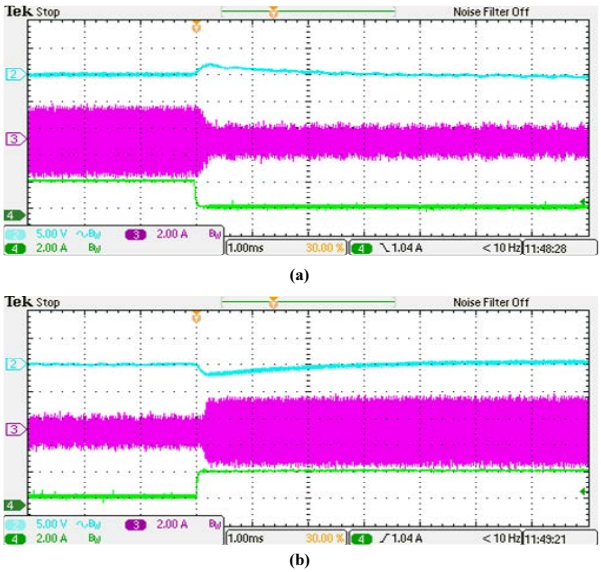
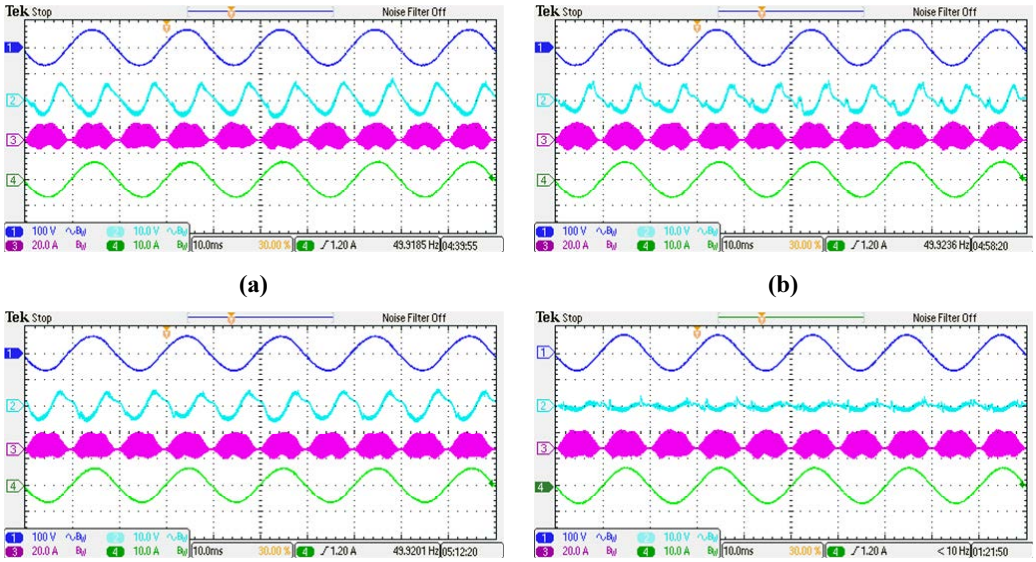


Figure 6.18: Step response of DAB converter with UDE-assisted sensorless load current feedforward control and 20% decrease in input voltage.

rameters, the maximum overshoot and undershoot remains essentially unchanged with only a slight increase in the settling time with decreased L. Similarly from Fig. 6.18 it can be observed that with 20% decrease in input voltage and UDE-assisted sensorless load current feedforward the transient response of the DAB converter virtually remains the same. From these results it can be concluded that the proposed control method can maintain a consistently fast transient response performance in spite of variations in converter's parameters.

6.4.2 DAB Converter Driving an Inverter

In this configuration, the DAB converter is used to drive a single-phase inverter. Fig. 6.19 shows the steady-state waveforms of the DAB converter driving the inverter. The top trace shows the inverter's output voltage, the second trace shows the dc-bus voltage, the third trace is the inverter's input current (i.e. DAB converter's output current), and the bottom trace is the inverter's output current.



Time: 10ms/Div.
Top Trance(Inverter's output voltage, AC coupled): 100V/Div.
2nd Trace (DC-bus voltage, AC coupled): 10V/Div.
3rd Trace (Inverter's input current): 20A/Div.
Bottom Trace (Inverter's output current): 10A/Div.

Figure 6.19: Steady-state waveform of DAB converter driving a single phase inverter (a) PI control (b) sensorless load current feedforward (c) UDE-based control (d) UDE-assisted sensorless load current feedforward.

It can be seen from Fig. 6.19a that, when the dc-bus voltage is regulated using a PI controller, there is a large double-line frequency component present in the dc-bus voltage. Fig. 6.19b and Fig. 6.19c show that the dc-bus voltage ripple has been reduced (by 23.1% and 11.7% respectively) when the dc-bus voltage is regulated using sensorless load current feedforward or UDE-based control. When sensorless load current feedforward control is enhanced by the UDE as shown in Fig. 6.19d, the dc-bus voltage ripple is further reduced by 69.1–73.1% giving a smooth dc-bus voltage.

The reduction in the dc-bus voltage ripple and its effect on the inverter's output voltage can be more clearly visualized from the Fast-Fourier-Transform (FFT) spectrum of the dc-bus voltage and inverter's output voltage. Fig. 6.20 and Fig. 6.21 shows the FFT spectrum of the dc-bus voltage and inverter's out-

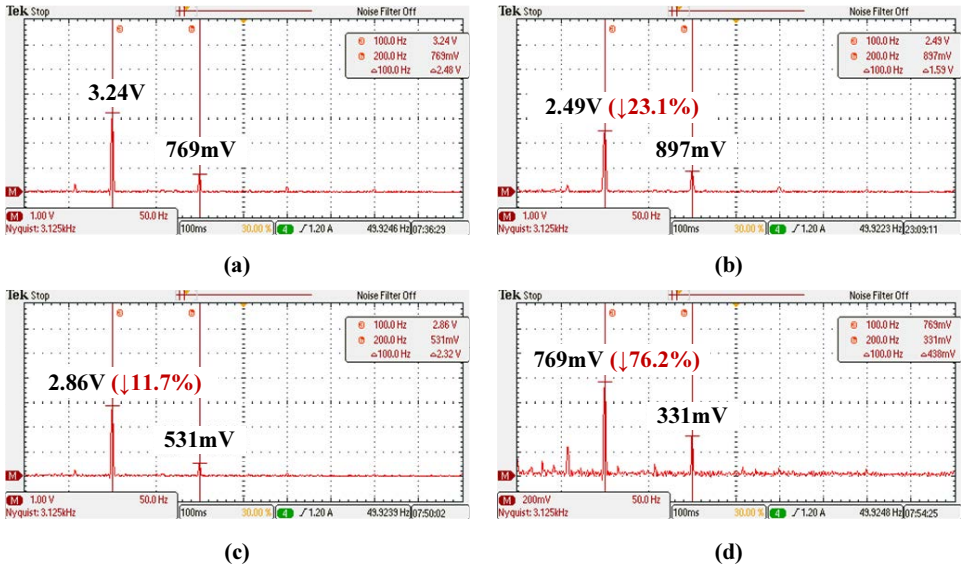


Figure 6.20: FFT spectrum of dc-bus voltage (a) PI control (b) sensorless load current feedforward (c) UDE-based control (d) UDE-assisted sensorless load current feedforward.

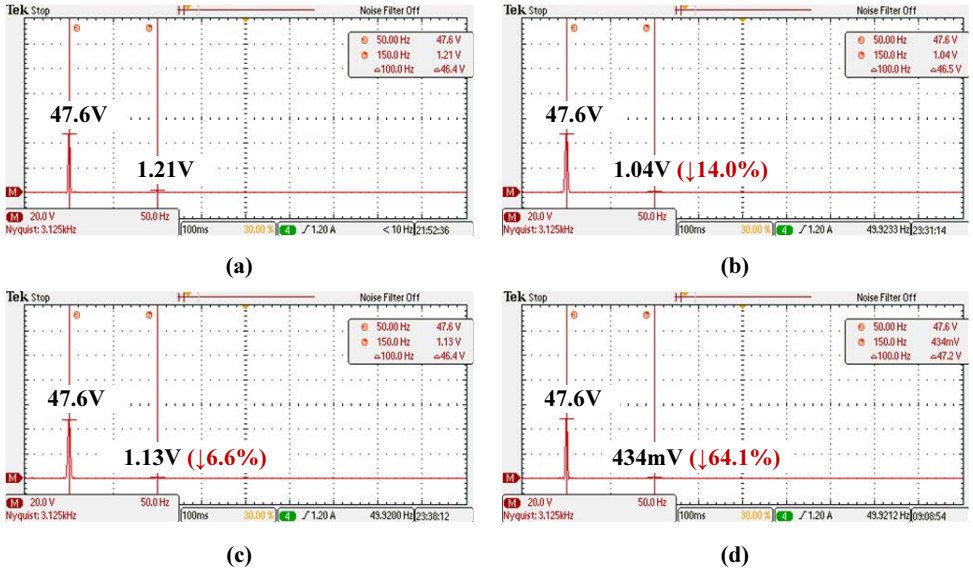


Figure 6.21: FFT spectrum of inverter's output voltage (a) PI control (b) sensorless load current feedforward (c) UDE-based control (d) UDE-assisted sensorless load current feedforward.

put voltage under different control schemes. It can be seen from Fig. 6.20a that, when the dc-bus voltage is regulated using PI control there is a large double-line frequency ripple component in the dc-bus voltage leading to a large third-order harmonic component in the inverter's output voltage due to intermodulation be-

tween the inverter's fundamental frequency (50 Hz) and the double-line frequency present in the dc-bus voltage, as evident from Fig. 6.21a. On the other hand, when the dc-bus voltage is regulated by UDE-assisted sensorless load current feedforward, the double-line frequency ripple component on the dc-bus voltage is significantly attenuated which results in a decrement of the third-order harmonic component in the inverter's output voltage, and thus improved inverter's output voltage quality.

6.5 Conclusion

In this chapter, a new sensorless load current feedforward control method is proposed to achieve improved dc-bus voltage regulation in a cascaded converter system comprising a DAB dc-dc front-end converter and a single-phase inverter. Without using sensor, the load current is estimated from the calculated DAB's output bridge current and lossless sensing (with digital filter) of the dc-bus capacitor current. The effects of any nonidealities on load current estimation are compensated by an UDE, thus making the proposed control scheme robust against uncertainties in circuit parameters and other un-modeled effects. It has been verified experimentally that the dynamic response performance of the DAB dc-dc converter has been significantly enhanced by the proposed control scheme in comparison with conventional PI control and the case when load current feedforward or UDE-based control is used alone. When subjected to step load change, it has led to 66.6% reduction in output voltage overshoot/undershoot and 80% reduction in settling time compared to conventional PI control. When cascaded with a single-phase inverter, the double-line frequency ripple component in the dc-bus voltage is reduced by 64.1% compared to conventional PI control, confirming the effectiveness of the proposed control scheme.

Chapter 7

Conclusion and Suggestions for Future Research Work

In this thesis, various robust and fast control methods for dc-dc converter have been proposed. Compared to traditional feedback control methods, the proposed control schemes are hardware efficient, parameter insensitive and result in improved transient response performance. In this chapter the main contributions of this thesis are summarized, along with some suggestions for possible future research directions.

7.1 Main Contributions of the Thesis

The main contributions of this thesis are summarized as follows:

1. In order to achieve good dynamic response performance and absolute stability in spite of wide range variations in power-stage component values, a non-intrusive and hardware-efficient method for online estimation of power-stage parameters and an autotuning controller is proposed for a digitally controlled buck converter. With the proposed method, and for an underdamped response, the time of the first output voltage peak T_p and the ratio

between two successive peaks are used to estimate the resonant frequency of the L_oC_o output filter, where as for an overdamped response, the resonance frequency ω_o is estimated from the time of the first output voltage peak T_p and the time constants of the output voltage's exponential decay. Following this, the time constant of the output capacitor's ESR zero is estimated from the previously obtained resonant frequency and the measured output voltage ripple under steady-state operation. On the basis of these estimated parameters, the coefficients of the digital controller are tuned to maintain a constant crossover frequency and phase margin irrespective of variations in power-stage parameters. As a result, the proposed method offers the advantage of being free from trial-and-error and non-intrusive; hence, it does not disturb the converter's normal operation. Moreover, the proposed method is hardware efficient since no additional hardware such as voltage and current sensors are required and can be implemented on a low-cost microcontroller.

2. To enhance the transient response of the front-end DAB converter and to reduce the amplitude of the double-line frequency voltage ripple in the dc-bus voltage, a disturbance observer based dc-bus voltage control for two-stage single-phase inverter system is proposed. In the proposed method a disturbance observer is designed by treating the lumped disturbance of the system as an extended state, which is estimated and compensated by the disturbance observer in real time. The major advantage of this control solution is that only minimal plant information is needed for controller design and that a decoupled composite controller can be realized, where the feedback compensator is designed to meet certain stability criteria while the disturbance observer based feed-forward compensator is designed to handle fast transient events. Furthermore, the inputs required for the disturbance

observer to estimate the total lumped disturbance is the sensed dc-bus voltage and control signal, and as such the proposed control scheme does not require any extra voltage or current sensor.

3. To achieve fast dynamic response and to reduce the amplitude of the double-line frequency voltage ripple in the dc-bus voltage without resolving to the computational complexity of an extended state, a new UDE-assisted sensorless load current feedforward control for two-stage single-phase inverter system is proposed. The proposed control method consists of a feedforward path, a UDE and a voltage feedback loop. The load current is estimated from the average current of the DAB's secondary bridge and lossless sensing of capacitor current is achieved using a digital filter, and the estimated load current is fed forward to achieve fast dynamic response. With this implementation, since the estimation accuracy of the load current and calculation of the optimum feedforward gain depends on the values of circuit parameters, which may be not known with high precision, an UDE is used to compensate for any model uncertainties and parameters variations, so that the design of the voltage feedback loop is aimed at ensuring good converter's stability. As compared to traditional single-loop voltage-mode control or voltage-mode control with load-current feedforward, the proposed UDE-assisted current sensorless load-current feedforward control results in an improved dynamic response performance and reduced dc-bus voltage ripple. While bringing about the benefit of low computational complexity.

7.2 Suggestions for Future Research Work

An autotuning controller based on the analysis of converter's start-up transient and measurement of steady-state output voltage ripple for buck-type con-

verter is presented in Chapter 3. However, many other topologies are used to provide well-regulated dc output voltage. One obvious future work is to apply the proposed method to other power converter topologies.

As an example, boost converter is commonly used in battery operated device to provide a higher output voltage. Due to the presence of a moving right half plane (RHP) zero in the control-to-output voltage transfer function (equation 7.1), its controller design is more challenging. Generally, a pole of the compensator is used to cancel the effect of the RHP zero. However, due to the moving nature of the RHP zero the converter has the tendency to become unstable with fixed controller.

$$G_{vd}(s) = \frac{v_o(s)}{d(s)} = \frac{v_{in}}{(1-D)^2} \frac{(1 - \frac{s}{\omega_{RHP}})(1 + \frac{s}{\omega_{ESR}})}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}} \tag{7.1}$$

where

$$\omega_{RHP} = \frac{(1-D)^2 R_{load}}{L_o} \tag{7.2}$$

$$\omega_{ESR} = \frac{1}{r_C \times C_o} \tag{7.3}$$

$$\omega_o = \frac{(1-D)}{\sqrt{L_o C_o}} \tag{7.4}$$

$$Q = (1-D)^2 R_{load} \sqrt{\frac{C_o}{L_o}} \tag{7.5}$$

In Chapter 5, a disturbance observer based dc-bus voltage control for two-stage single-phase inverter system is proposed in order to enhance the transient response of the front-end DAB converter. It is well known that the transient response of the converter can be improved by using a dual-loop current-mode

control. However, with traditional dual-loop control the PI controller in both the outer voltage-loop and inner current-loop are designed based on an accurate small-signal model of the converter. As such the traditional dual-loop current-mode control may not achieve the optimal dynamic response performance in the presence of model uncertainties and converter power-stage parameters variations. In order to retain the dynamic response performance and control the inductor current despite of model uncertainties and converter's parameter variations, a nested disturbance observer current-mode control of a two-stage single-phase inverter system can be used.

To enhance the transient response of the front-end DAB converter a new UDE-assisted sensorless load current feedforward control scheme for a two-stage single-phase inverter system is proposed in Chapter 6. In the proposed method a low-pass filter $G_f(s)$ is used to estimate the total lumped uncertainty and disturbance. However, for different transfer function selected for $G_f(s)$ the DAB converter will exhibit different closed-loop output impedance characteristics and hence different transient response performances. Hence it will be interesting to further investigate the dynamic and steady-state performances of a DAB converter when different transfer functions are selected for $G_f(s)$.

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