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CHARACTERIZATION OF 2D HETEROSTRUCTURES

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MPhil

The Hong Kong Polytechnic University

2019

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Department of Applied Physics

Characterization of 2D Heterostructures

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A thesis submitted in partial fulfilment of the

requirements for the Degree of Master of Philosophy

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Certificate of originality

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Abstract

Up to now, A great effort has been used to study the field of two dimensional (2D) materials. Reduced crystal symmetry existing in 2D materials when they are scaled down from bulk to monolayer leads to the change of their band structures. Graphene was the most widely 2D material in last decade because of its distinctive physical properties. A lot of devices based on graphene have been reported. However, the absence of a bandgap for graphene has limited its applications in electronics and optoelectronics. Taking advantages of reduced crystal symmetry, transition metal dichalcogenides (TMDs) have various advantages such as high electron mobilities, high ON/OFF ratio current ratio and excellent bendability, which are suitable for next generation low-power consumption and flexible electronic devices. Laterally, TMDs have strong covalent bonds which provide a great in-plane stability. Vertically, the van der Waals force allow TMDs to stack on other materials to form a 2D hybrid van der Waals (vdW) heterostructures without the need for considering the lattice mismatch of the two different materials. As a result, it opens the opportunities for developing novel device applications in the future. Recently, p-n junctions based on organic and two-dimensional (2D) materials have been recognized as the easiest way to fabricate hybrid 2D van der Waals heterojunction devices for electronic and optoelectronic applications. General speaking, organic materials on 2D materials is usually fabricated by thermal evaporation with the presence of high voltage and vacuum systems. In this thesis, we introduce a simple way to fabricate p-organic/n-2D heterostructure, where Pedot:PSS was chosen to be the p-organic material due to its high conductivity,

excellent film forming ability and good stability, while MoS_2 and WS_2 were chosen as the n-2D material due to their well-known properties. We demonstrate that simple technique introduced in our fabrication of organic/2D van der Waals heterojunction could extend to include other organics and 2D materials.

List of publications

1. **K.H. Chan**, S.M. Ng, H.F. Wong, C.W. Leung, C.L. Mak, Rectify Effect of Pedot:PSS/WS_2 Heterostructure, physica status solidi (a)

2. K.K. Lam, **K.H. Chan**, S.M. Ng, H.F. Wong, Y.K. Liu, C.W. Leung, C.L. Mak, Fabrication and Characterization of Epitaxial Gd-Doped SBN Thin Films, physica status solidi (a)

3. H.F. Wong, S.M. Ng, Y.K. Liu, K.K. Lam, **K.H. Chan**, W.F. Cheng, D.v. Nordheim, C.L. Mak, B. Ploss, C.W. Leung, Gate-Controlled Transport Properties in Dilute Magnetic Semiconductor (Zn, Mn)O Thin Films, IEEE Transactions on Magnetics

4. Y.K. Liu, H.F. Wong, K.K. Lam, **K.H. Chan**, C.L. Mak, C.W. Leung, Anomalous Hall effect in Pt/$Tb_3Fe_5O_{12}$ heterostructure: Effect of compensation point, Journal of Magnetism and Magnetic Materials

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The Structure of the Thesis

In this project, we have synthesized MoS_2 and WS_2 layered materials. Their structural and optical properties were characterized. Furthermore, MoS_2- and WS_2- based field effect transistors and their heterostructures had been fabricated and their electrical properties were measured. The structure of the thesis is divided into seven chapters.

Chapter 1. Introduction. The brief background of 2D materials is described, including the structural, optical and electrical properties of 2D materials as well as their heterostructures.

Chapter 2. Experimental Details. In this chapter, all the experimental techniques and the fabrication procedures used for fabricating 2D van der Waals heterostructure devices are described. The basic theories of the equipment used in this thesis are also included.

Chapter 3. Material Characterization. In this chapter, the electrical characterization of different materials, including MoS_2, WS_2 and Pedot:PSS, are described. The FETs and sheet resistance measurement of these materials are discussed.

Chapter 4. Electrical characterization of Pedot:PSS/WS_2 heterostructure. In this chapter, the typical I-V measurements of p-n diodes are discussed. Also, gate dependenct and temperature dependent measurements of the devices have been investigated. The result are discussed in this chapter.

Chapter 5. Electrical characterization of Pedot:PSS/SiO_2/n-2D heterostructures. In this chapter, the MoS_2 and WS_2 are chosen to be the n-2D materials of our p-i-n junction devices. The performance of the two devices are discussed.

Chapter 6. Electrical characterization of Pedot:PSS/SiO_2/MoS_2 heterostructures with different conductivity of Pedot:PSS. In this chapter, different ratios of Pedot:PSS (Al4083) and Pedot:PSS (PH500) are mixed to study the effects of conductivity of the p-organic material on the performance of the devices. It aims to optimize a suitable conductivity of p-organic in fabricating Pedot:PSS/SiO_2/MoS_2 heterostructure devices.

Chapter 7. Conclusion and future work. In this chapter, the results of the MoS2 and WS2 based heterostructures are summarized and a conclusion is made. Furthermore, future work of these devices is suggested.

Chapter 1 Introduction

1.1 Background of two-dimensional materials

1.1.1 Graphene

In 2004, Andre Geim and Konstantin Novoselov published the first article about the synthesis of graphene by the method called mechanical exfoliation method, and its field effect transistor characteristics, which has opened a new research direction for future study.[1] Graphene is an allotrope of carbon in the form of an atomic layer. It has hexagonal carbon rings structure and each carbon atom has a covalent bonding with other neighbor atoms by sp^2 hybridization.[2]

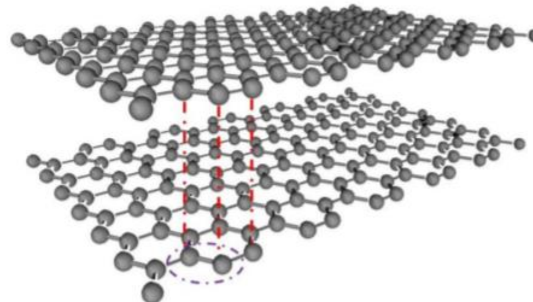


Figure 1-1 Schematic diagram of graphene with honey comb lattice structure

Figure 1-1 shows the atomic structure of graphene. The carbon-carbon bond length is about 0.14 nm. Each graphene layer is attracted by the weak van der Waals force, which is much weaker than the carbon-carbon bond in the horizontal direction, with other graphene layer. Therefore, we can obtain few graphene layers from bulk graphite easily by the mechanical exfoliation.

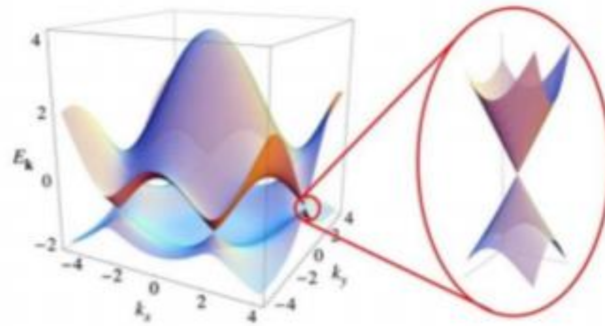


Figure 1-2 The electronic dispersion of graphene in reciprocal space. One of Dirac cone is zone in.[3]

Figure 1-2 shows the electron dispersion of graphene in reciprocal space. The dispersion relation of graphene at K points in the reciprocal space is linear which leads to the zero-effective mass for electrons and holes in graphene. Carriers in graphene can move freely with little interference between the conduction band and valence band. As a result, the carrier in graphene has an ultra-high mobility of 2×10^5 $cm^2V^{-1}s^{-1}$ which is around 140 times of the carrier mobility of silicon[3]. However, the minimum of the conduction band in graphene touch the maximum of the valence band which leads to no bandgap for graphene.

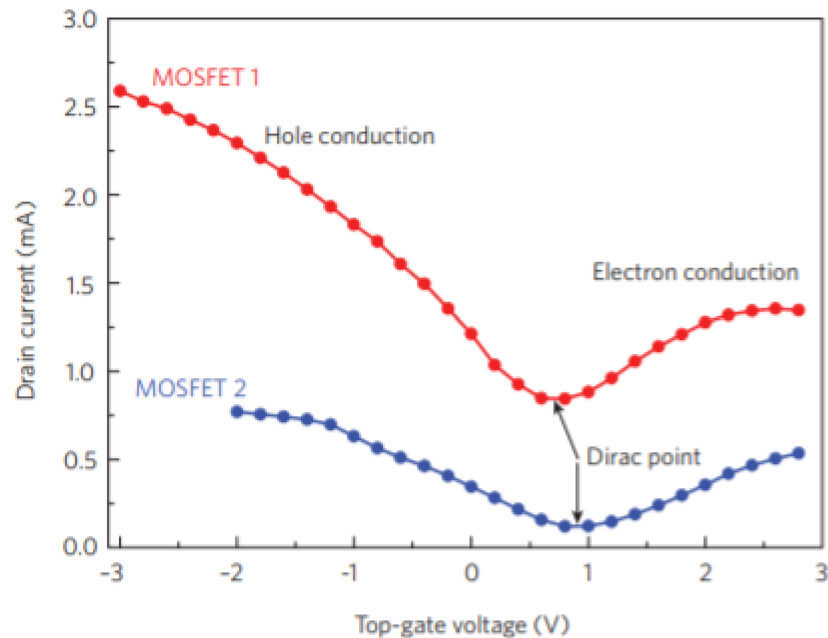


Figure 1-3 Typical transfer characteristics for two MOSFETs with large-area-graphene channels[4]

Figure 1-3 shows the typical transfer characteristics of two graphene MOSFETs. The ON/OFF ratio of MOSFET1 and MOSFET2 are around 3 and 7 respectively. For graphene transistors, it has a very special transfer characteristic that the carrier density and the type of carrier of the FET channel can be tuned by gate voltage. With increasing positive gate voltage, electrons will accumulate in the channel (n-type channel). In contrast, large negative voltage will lead to p-type channel. The turning point of these two transfer characteristics is called Dirac point. The position of this turning point depends on the difference between the gate work function and graphene, interface effect and doping concentration of graphene.[4] Based on the results, it was found that the ON/OFF ratios of graphene FETs at room temperature were around 2-20 which are far lower than conventional silicon devices value of ~1000. This limits graphene's

applications in electronics and optoelectronics.

Besides graphene, other 2D materials, such as transition-metal dichalcogenides (TMDs) also exhibit many interesting properties when they are scaled down from bulk to nanoscale.

1.1.2 Transition Metal Dichalcogenides

Due to the limitation of graphene, some researchers have been turning their focus on other graphene-like 2D materials. Among all 2D materials, transition metal dichalcogenides (TMDs) have been intensely studied because of their high carrier mobility, indirect-direct bandgap transition, strong spin-orbit coupling and good chemical stability[5], which are suitable for next-generation flexible nanoelectronics and nano-optoelectronics applications.

TMDs typically can be described by formula MX_2, where M stands for transition metal (for example Ti, Zr, Hf, V, Nb, Ta, Mo, W, Tc, Re, Co,Rh,Ir, Ni, Pd, Pt) and X stands for chalcogenide atom (such as S, Se, Te).[6] Combining with different elements, TMDs could result in semiconducting, metallic or superconducting behavior. In the introduction section of this thesis, we start with the most widely studied and air stable semiconducting MoS_2 as a typical example for 2D materials.

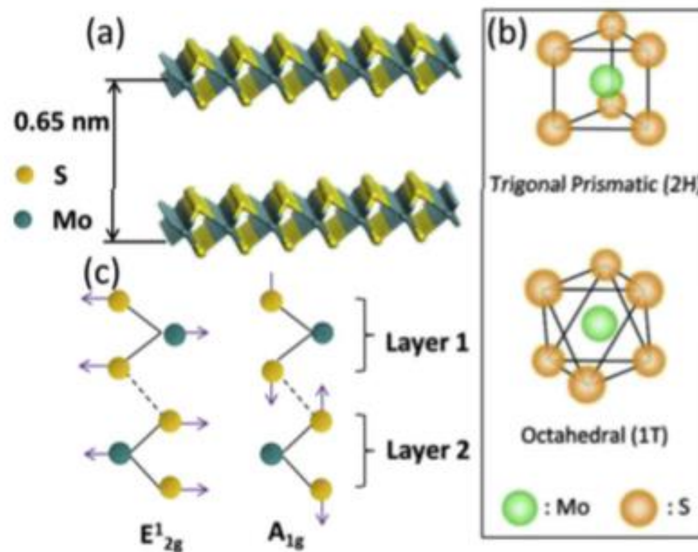
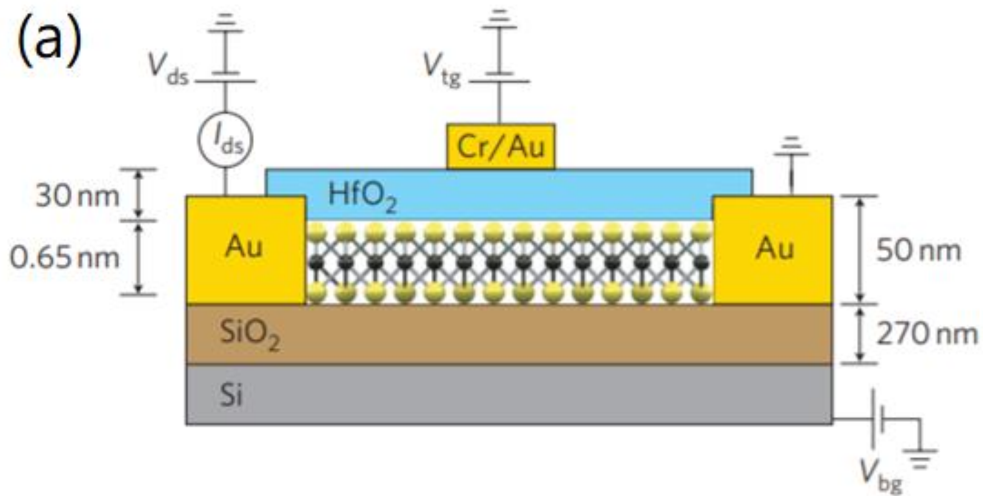
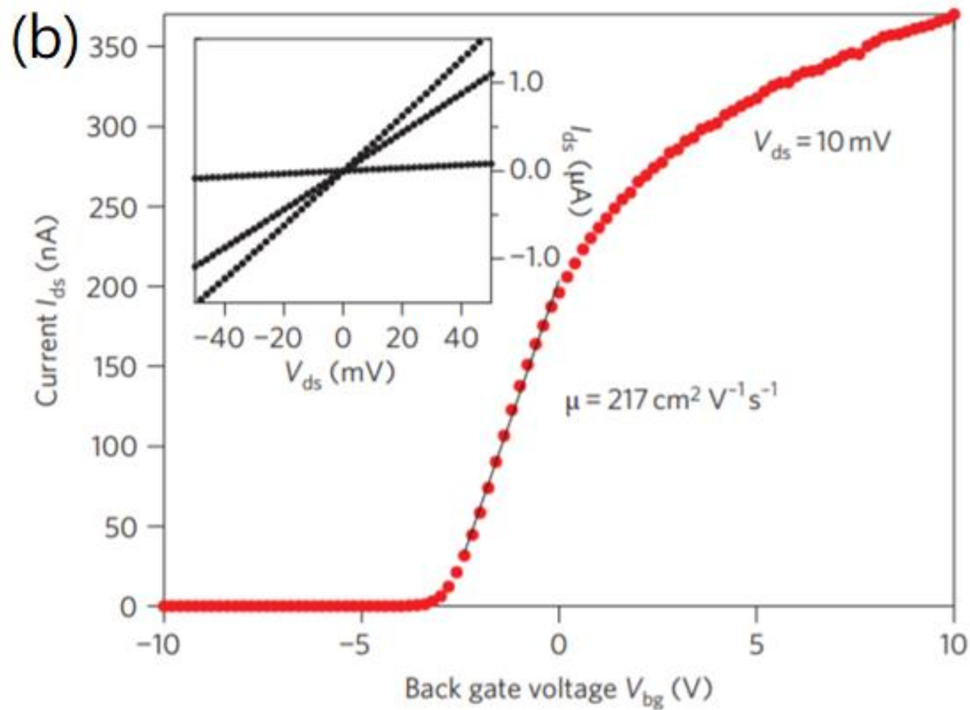


Figure 1-4 (a) Chemical structure of two MoS_2 layer. (b) Two polytypes of single layer MoS_2: trigonal prismatic (2H) and octahedral (1T). (c) Schematic illustrations of the two typical Raman-active phonon mode (E^1_{2g}, A^1_g).[7]

Figure 1-4 (a) shows the chemical structure of two MoS_2 layers. We can see that Mo (+4) and S (-2) atoms are formed in a sandwich structure by the strong covalent bonds in a sequence of S-Mo-S.[8] Like graphene, each layer is also attracted by the weak van der Waals forces. Each layer has a theoretical thickness of 0.65 nm. Figure 1-4 (b) shows two configurations of MoS_2 which are trigonal prismatic polytype (2H) and octahedral crystal symmetry (1T). MoS_2 with 2H structure exhibits semiconducting behavior and 1T structure exhibits the metallic behavior.[9] Figure 1-4 (c) is the schematic illustrations of two typical Raman-active phonon modes (E^1_{2g} and A^1_g). E^1_{2g} is corresponding to in-plane vibration modes of S atoms and A^1_g is corresponding to out-of-plane vibration modes of S atoms.[10] From bulk to monolayer, the Raman peak frequency difference between E^1_{2g} and A^1_g shows a clear decreasing trend.[10] Therefore, researchers always use this Raman technique to confirm the thickness of

MoS_2 samples.[10]





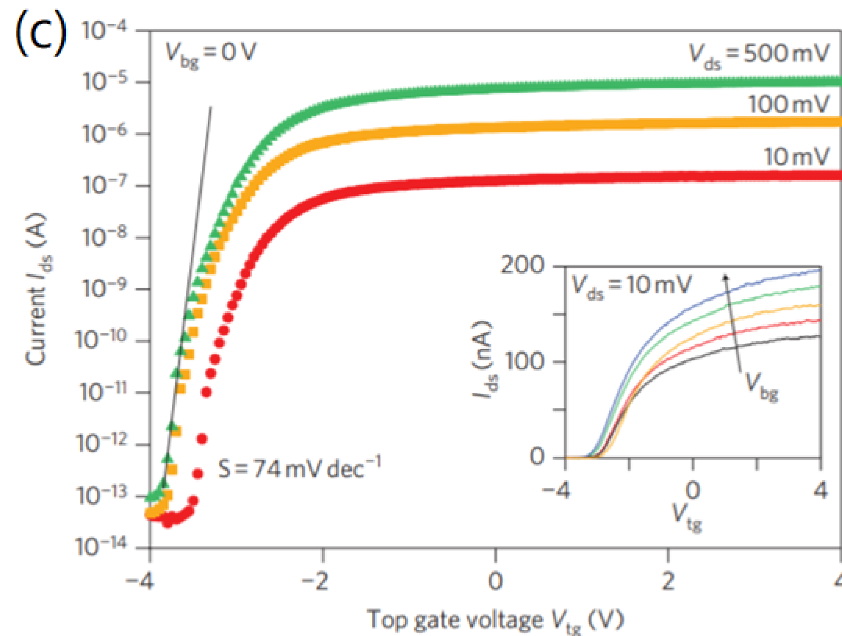


Figure 1-5 (a) Cross-sectional view of the structure of a monolayer MoS_2 FET together with electrical connections used to characterize the device. (b) Room-temperature transfer characteristics for the FET with 10 mV applied bias voltage V_{ds}. Back gate voltage V_{bg} is applied to the substrate and the top gate is disconnected. (c) I_{ds}-V_{tg} curve recorded for a bias voltage ranging from 10 mV to 500 mV. Measurements were performed at room temperature with the back gate grounded.[11]

The most widely studied 2D materials is graphene due to its high mobility. Unfortunately, graphene has no bandgap, a property which is hindered its applications for electronics and optoelectronics devices. Therefore, researchers have been looking for other 2D materials for better application potentials. Figure 1-5 (a-c) show a report using a hafnium oxide gate dielectric to demonstrate a MoS_2 transistor with a room-temperature mobility of above 200 $cm^2V^{-1}S^{-1}$ and current ON/OFF ratio of 10^8.[11]

Lots of excellent properties have been found in monolayer MoS_2. The relatively high

carrier mobility of ~200 $cm^2V^{-1}s^{-1}$ at room temperature, the incredible ON/OFF ratio value up to 10^8 and most importantly, indirect bandgap (1.2 eV) to direct bandgap (1.8 eV) transition scaled down from bulk to monolayer. All these excellent properties show that TMDs can be a promising complementary 2D materials of graphene.

1.2 Two major advantages compared with bulk counterparts

The first advantage is no need to consider the screening effect. For typical silicon-based transistors, the thickness of the semiconductor materials must be designed to be as thin as possible to minimize the electrostatic screening effect in the transistors. 2D materials are so thin that just one atomic layer which can be served as the best candidate to minimize the electrostatic screening effects.[12]

$$\lambda = \sqrt{\frac{\varepsilon_s d_s d_{ox}}{\varepsilon_{ox}}} \tag{1}$$

Equation 1 states the formula of Debye length, where ε_s is the dielectric constant of the semiconductor, d_s is the thickness of the semiconductor, ε_{ox} is the dielectric constant of the dielectric oxide and d_{ox} is the thickness of the dielectric oxide. Based on this formula, it is noticed that the Debye length can be minimized by reducing the thickness of the semiconductor. Therefore, 2D materials are the best materials that can be used in device applications.

The second advantage is based on the quantum capacitance limit. 2D materials can operate beyond the quantum capacitance limit (QCL)[13] which can minimize the energy consumption for switching.

1.3 Background of Pedot:PSS

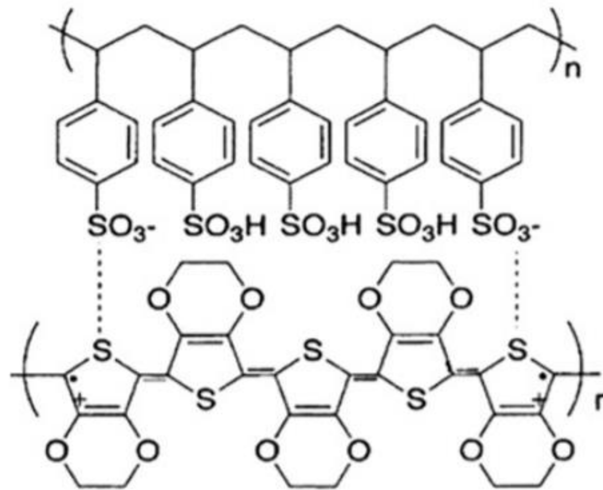


Figure 1-6 Schematic of the molecular structure of Pedot:PSS[14]

Pedot:PSS (poly(3,4-ethylenedioxythiophene) : polystyrene sulfonate) is a p-type transparent conducting polymer which consists of a mixture of two ionomers. Based on its advantages of conductivity, transparency, ductility and simple processing ability[15], it has become one of the most widely used organic materials in thin film fabrication. The π -conjugated system shown in Figure 1-6 is responsible for the hole transport in Pedot.[14] Researchers usually use it as a hole transporting layer in organic light emitting diode devices, organic photovoltaic devices and perovskite photovoltaic devices.[16]

1.4 p-n junction based on 2D materials

Combining p-type semiconductor with n-type 2D material to form a 2D vdW heterostructures has been demonstrated in a wide range of applications such as

rectifying diodes, light emitters, photo-detector and photovoltaic solar cells.

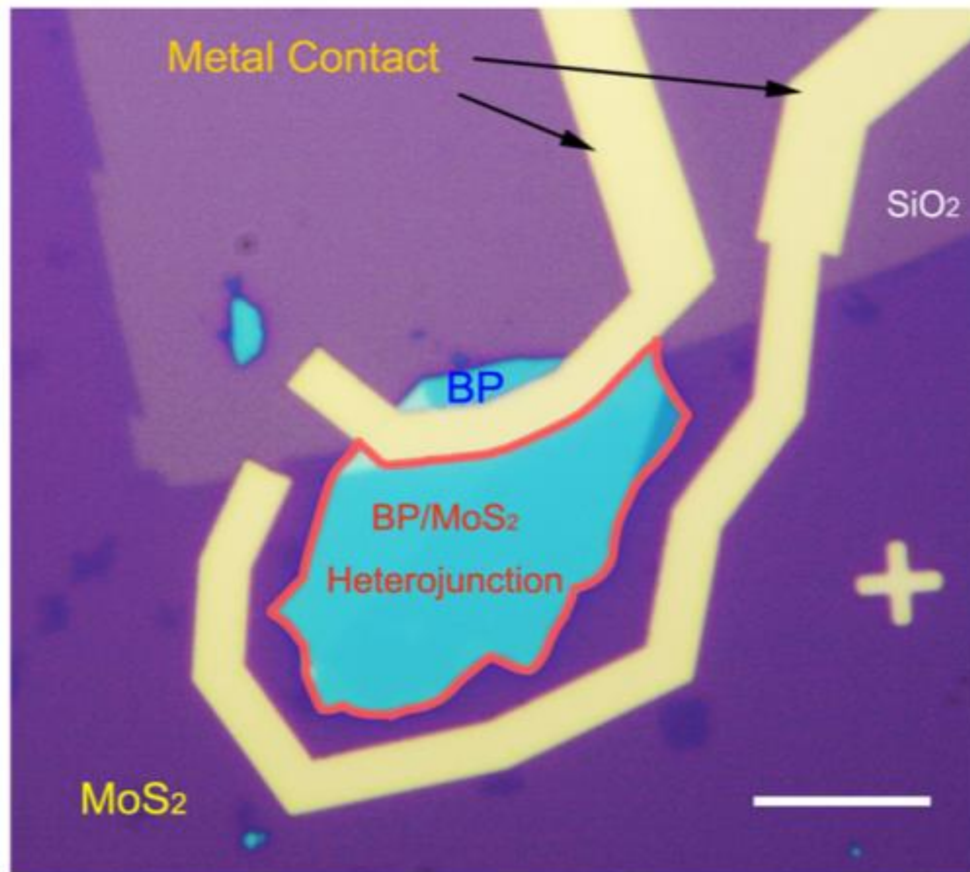


Figure 1-7 Optical image of the p-Black phosphorus/n-2D MoS_2 heterojunction[17]

In 2014, Deng's group used the mechanical exfoliation technique to combine p-Phosphorus/n-2D MoS_2 to fabricate a photodetector device.[17] Under illumination, the device reached a maximum photodetection responsivity of 418 mA/W for a 633 nm light source and photovoltaic energy conversion with an external quantum efficiency of 0.3% which showed 2D materials can be further explored in broadband photodetection and solar energy harvesting.

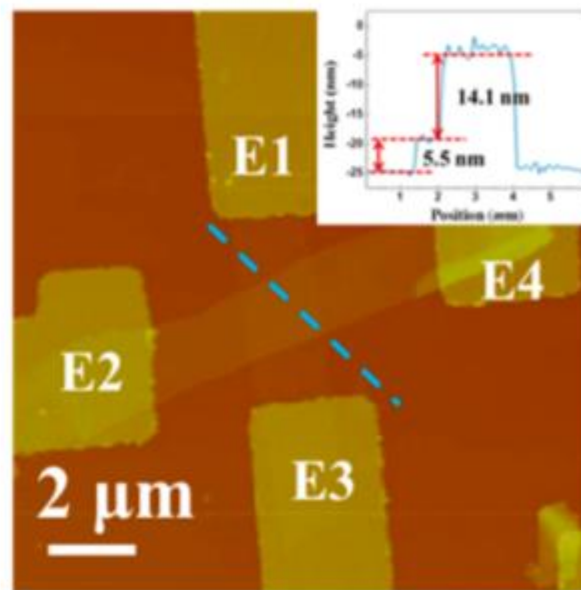


Figure 1-8 AFM image of the p-GaTe/n-MoS_2 device. The four electrodes are marked as E1, E2, E3 and E4.[18]

Following Deng's work, Wang's group reported that they used the same technique of mechanical exfoliation to produce the combination of p-GaTe/n-MoS_2 vdW heterostructure.[18] The device showed a high photovoltaic and photo-detecting performance. The rectification ratio, external quantum efficiency, and photoresponsivity were $4x10^5$, 61.68 %, and 21.83 AW^{-1} respectively. Especially a detectivity up to $8.4x10^{13}$ J was obtained, which is higher than those of the commercial Si and InGaAs photodetectors.

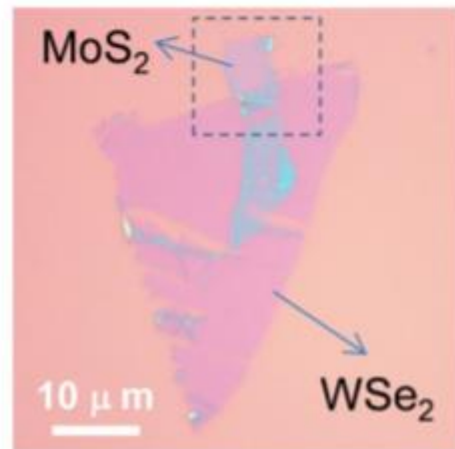


Figure 1-9 Optical microscope image of the MoS_2/WSe_2 heterojunction.[19]

By using similar technique of mechanical exfoliation, Peng's group successfully demonstrated the exciton dissociation and charge transfer in MoS_2/WSe_2 vdW heterostructure.[19] Their results showed that the electron transfer from WSe_2 to MoS_2 was just 470 fs upon optical excitation with nearly 100% charge transfer efficiency.

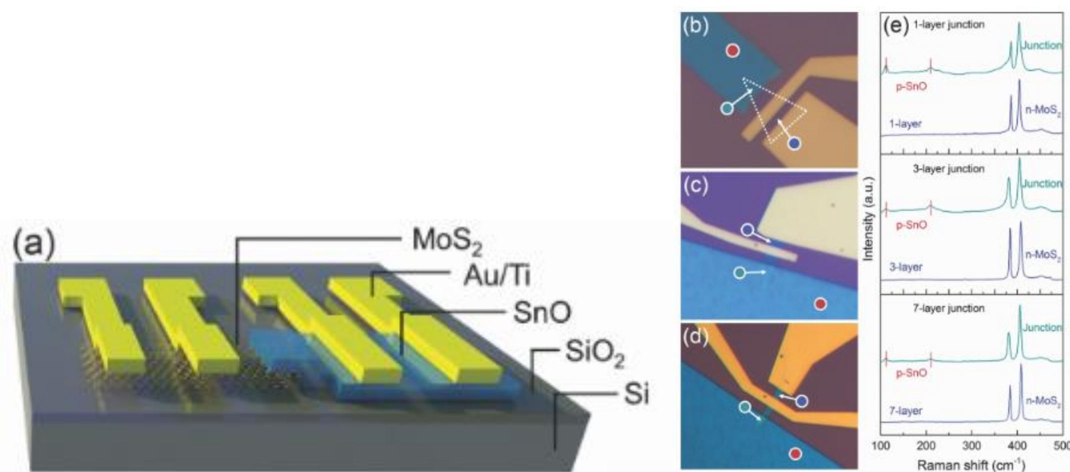


Figure 1-10 (a) Schematic illustration for the hybrid vdW heterojunction (b-d) Optical images for the 1-layer(b), 3-layer(c), 7-layer(d) junctions. The laser focus for Raman spectroscopy is specified, red: SnO; blue: MoS_2; green: junction. (e) Raman spectra

of the junction devices and n-MoS_2 layers.[20]

To simplify the whole process, Wang et.al reported a heterojunction of combining a p-SnO and an n-MoS_2.[20] Figure 1-10 (a) is the schematic of the devices. Figure 1-10 (b-d) are the optical images for the 1 layer, 3 layers and 7 layers devices respectively. The devices showed a high rectification ratio up to 10^4 and ideality factor of 2. Figure 1-10 (e) shows their corresponding Raman spectra.

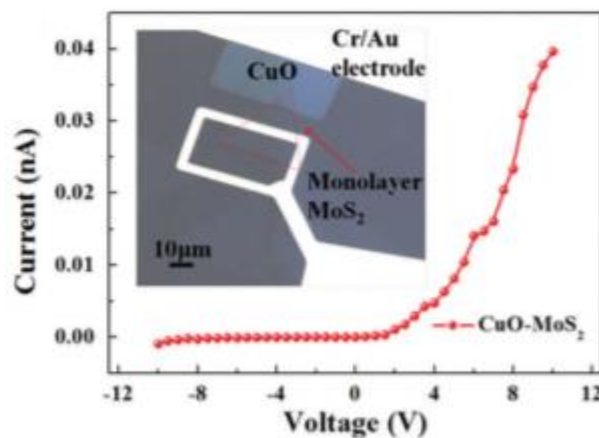


Figure 1-11 Optical image and I-V curve of the p-CuO/n-MoS_2 device[21]

In 2017, Zhang's group developed a flexible photodetector based on p-CuO/n-MoS_2 heterojunction.[21] The p-CuO film was deposited by magnetron sputtering and the monolayer MoS_2 was grown by chemical vapor deposition. Under a tensile strain of 0.65 % and 532 nm illumination, the device reached 27 times of photocurrent compared with the strain free conditions and the detection sensitivity could reach up to 3.27×10^8 Jones.

All the above-mentioned devices have been fabricated by the mechanical exfoliation

technique and/or physical deposition technique for p-type semi-conducting materials. However, mechanical exfoliation cannot ensure the production yield, while physical deposition techniques need to spend a lot of time in finding the optimal growing conditions. Therefore, in this thesis, p-type organic semiconductors were employed in 2D devices fabrication, due to the advantages of relatively simple growing process, low cost and flexibility obtained in organic semiconductors.

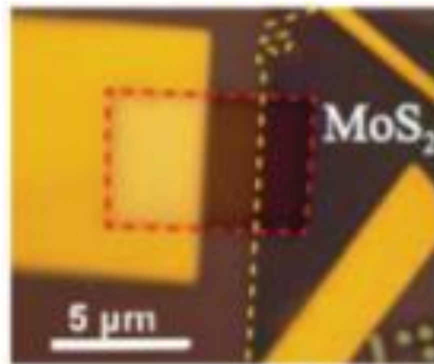


Figure 1-12 Optical micrograph of a representative CuPC/MoS_2 device.[22]

The first p-organic material introduced in 2D vdW heterostructures was Cu-phthalocyanine (CuPc). Saül Vélez's group demonstrated the integration of CuPc with 2D MoS_2 to hybrid p-n junction with both gate tunable diode characteristics and photovoltaic effect.[22] The device showed properties with a diode rectifying factor of 10^3, an external quantum efficiency of ~11 %, an open circuit voltages up to 0.6 V and a power conversion efficiency of 0.7 %.

However, depositing organic materials on 2D materials to form 2D vdW heterostructures is usually demonstrated by thermal evaporation where high voltage and vacuum systems are needed.[22, 23] In this thesis, we present a simpler way to

fabricate p-organic/n-2D heterostructures. We believe that our study is of interest to researchers who are working on 2D vdW heterostructures. This simple technique for fabricating organic/2D van der Waals heterojunction could extend to include other organics and 2D materials.

Chapter 2 **Experimental Details**

2.1 Synthesis of TMD materials

2.1.1 Mechanical Exfoliation

The first successfully fabricated 2D material, graphene, was discovered by Geim et al. Researchers always use mechanical exfoliation method to explore new 2D materials because this method can produce 2D materials with high quality. In this thesis, the 2D materials of p-organic/n-2D heterojunction were firstly fabricated by mechanical exfoliation. The schematic diagram below summarizes the step of mechanical exfoliation of the 2D material.

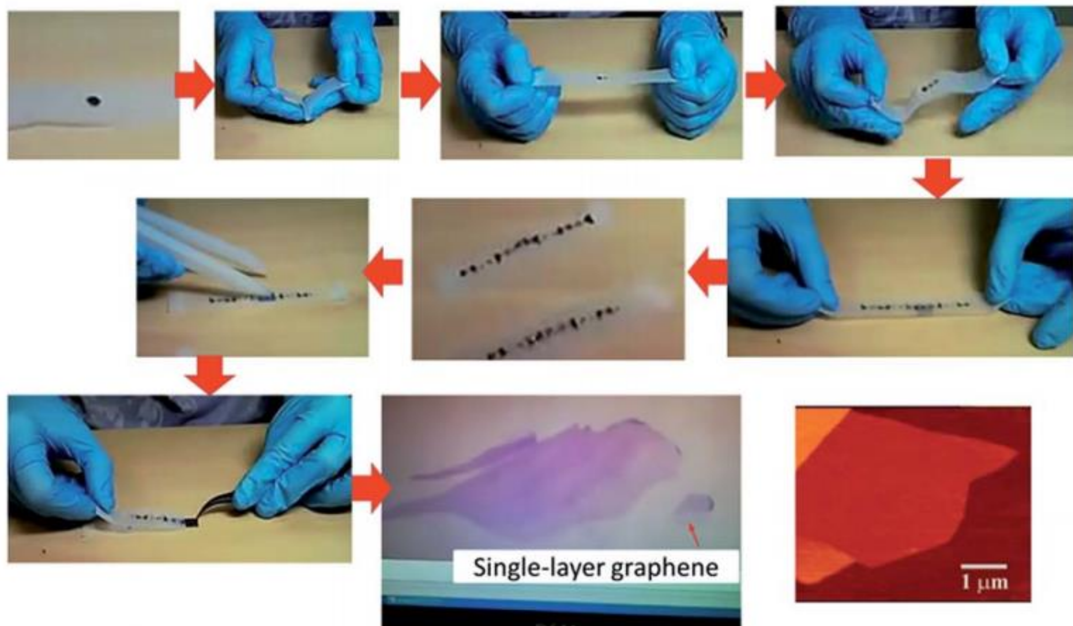


Figure 2-1 An illustrative procedure of the Scotch-tape based micromechanical exfoliation of graphene.[24]

Typically, a small piece of 2D crystals was placed onto a scotch tape. Then, folded the tape several times to make more 2D flakes on the scotch tape until the color of the 2D

flakes changed from metallic shiny to gray. Then, the tape with 2D flakes was placed onto a silicon wafer. Before that, the silicon wafer with 300 nm thick SiO_2 had been cleaned by the standard cleaning procedures, i.e. using acetone, ethanol and deionized water to clean the surface. Pressed the tape onto the silicon wafer for several times, the tape was then peeled off slowly. Due to the help of van der Waals force, 2D flakes could be produced on the substrate. However, the yield of this method to obtain a monolayer was very low which is not suitable for manufacturing of devices. With the help of a high color contrast optical microscope, 2D flakes of different thickness could be distinguished. Silicon wafer with 300 nm thick SiO_2 was found to be the most suitable thickness to distinguish different 2D layers.[25, 26] Figure 2-2 shows a few layers MoS_2 produced by mechanical exfoliation compared with a bulk MoS_2.

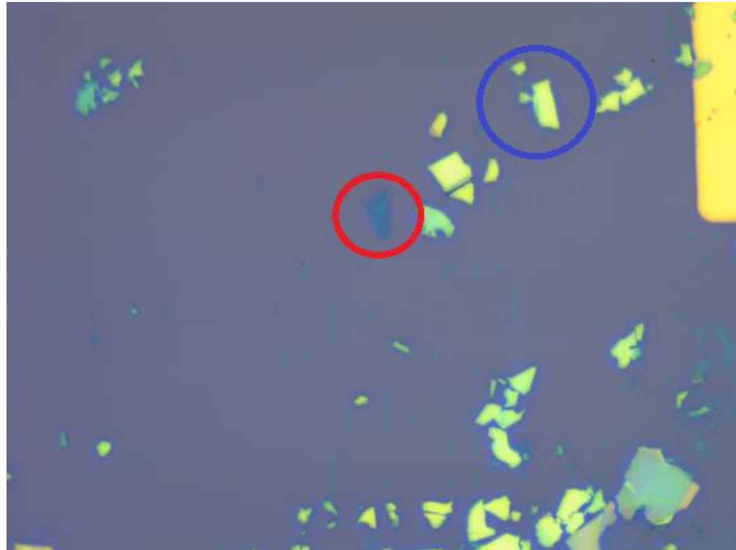


Figure 2-2 Optical images of a thin MoS_2 (red circle) and bulk MoS_2 (blue circle) on silicon substrate by mechanical exfoliation.

The color of the few layer MoS_2 was quite similar to the background color. On the other hand, the shiny yellow color was from the bulk MoS_2 flake. Through comparing the

color of various MoS_2 flakes, few layer MoS_2 was found. To confirm whether the material is 2D flake or glue residual, Raman spectroscopy was conducted. Raman spectroscopy is a fast and non-destructive technique to identify the number of layers of 2D materials.[27] This technique is discussed later.

2.1.2 Chemical Vapor Deposition

In order to have a better control of the 2D materials used for the heterostructures. Chemical vapor deposition was employed in this thesis.

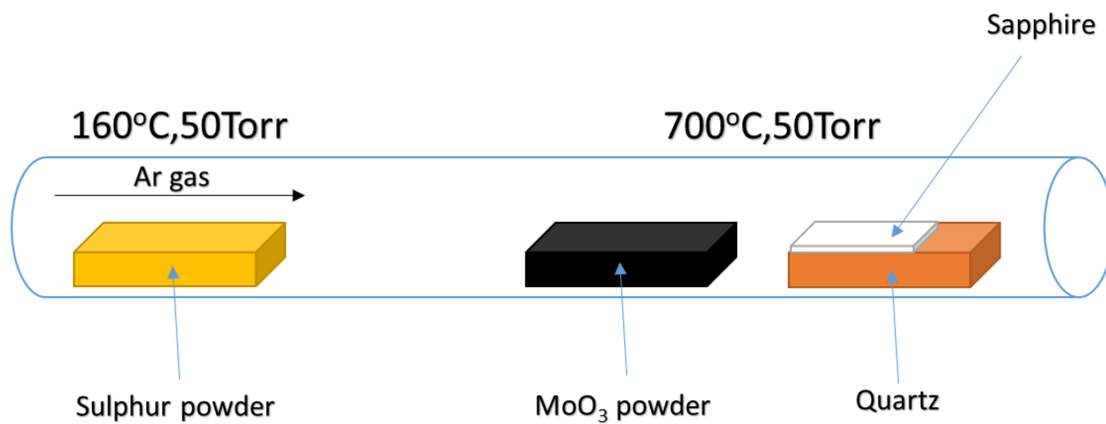


Figure 2-3 Schematic diagram of CVD process for growth of MoS_2

The CVD growing process are summarized as below:

i) Loaded the quartz holder with sapphire substrate (500 µm thick, 1 cm x 4 cm), MoO_3 powder and sulphur powder in order as shown in Figure 2.3.

ii) The MoO_3 powder was pre heated up to 550°C, then the Sulphur was started to heat up. So that, the final temperature of Sulphur powder and MoO_3 powder were 160°C and 700°C respectively

iii) The sapphire substrate was heated up to 700 °C for 30 min with Ar gas flowing at a flow rate of 50 sccm

iv) After the reaction, the temperature was cooled down naturally under the same flow of Ar gas

Table 1 The optical images of CVD grown MoS_2 with different working temperatures.

Temperature (^oC)	Optical image
650	
660	
670	
680	
690	
700	

To investigate the influence of substrate temperature on the growth of MoS_2. Here, the amount of the MoO_3 powder and working pressure were kept at 5 mg and 50 Torr respectively. The temperature was varied at the range of 650°C – 700°C. Table 1 shows the surface morphology of the sapphire substrates after the CVD growth. With increased temperature, the amount of the MoS_2 flakes increased. However, when it came to 700°C or higher, right hand side of the sapphire substrates which were putting close to MoO_3 powder became dark in color which was probably due to the evaporated MoO_3 powder.

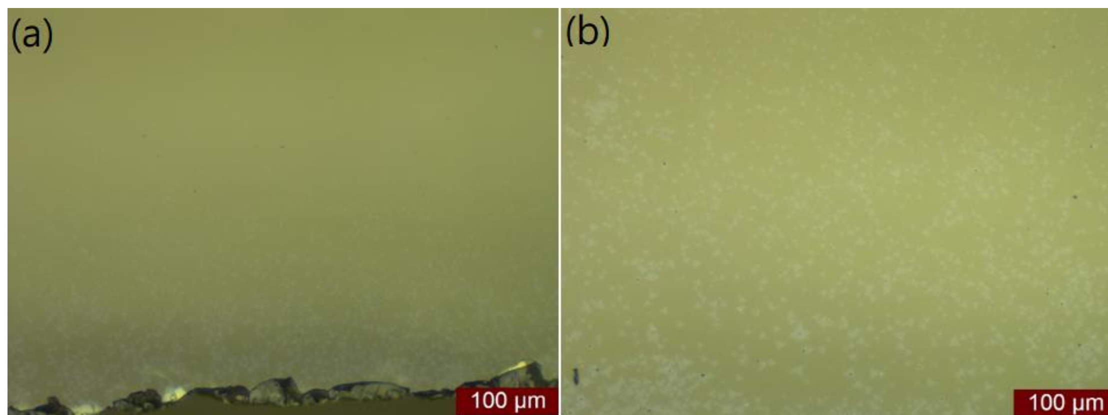


Figure 2-4 Optical microscope images of MoS_2 flakes grown with 5mg MoO_3 powder at 690°C (a) and 700°C (b).

Figure 2-4 are the optical microscopic images of MoS_2 flakes grown with 5 mg MoO_3 powder at 690 °C and 700 °C. With increased temperature, the lateral dimension of MoS_2 flakes became larger. Under 700°C growth temperature, the dimensional of ~10 μm MoS_2 flakes were successfully synthesized which were big enough for our devices fabrication. The qualities of the synthesized MoS_2 flakes are discussed at the next chapter.

2.2 Characterization methods

2.2.1 Raman Spectroscopy

A lot of information such as material's band structure, composition of material, stress/strain state, crystal symmetry, quality of crystal and amount of material can be obtained using Raman spectroscopy.[28]

Basic components of a Raman system include:

(i) A laser source

(ii) Excitation delivery optics

(iii) Samples

(iv) Collection optics

(v) A wavelength separation device (Spectrometer/grating)

(vi) A detector and associated electronics (CCD)

(vii) A recording device (Computer)

<u>Process involved in collecting data</u>

When light is incident on to a sample, the light is scattered and collected by collection optics. The notch filter is usually used to block most of the elastic scattered light to avoid the overwhelming of the weak sign from the inelastically scattered photons. The Raman scattered light is dispersed corresponding to its wavelength by grating and/or spectrometer and detected by a CCD. Finally, the signal is enlarged by an amplifier and recorded by a computer.

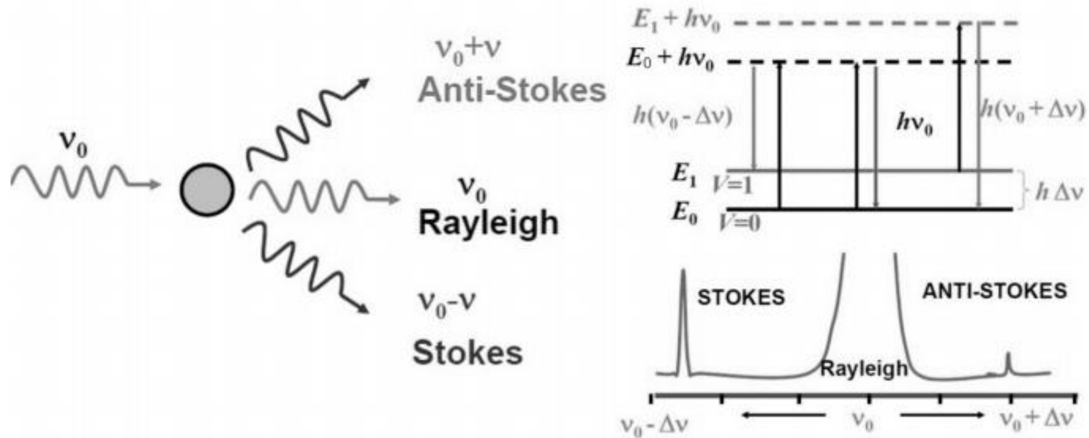


Figure 2-5 The schematic diagram of Raman scattering. V_o is the frequency of incident light, V_o+V and V_o-V represents the frequencies of scattered light.

Raman spectroscopy relies on inelastic scattering (Raman scattering) between an incident light and molecules to obtain Raman shift spectrum. Phonon exchange energy to the molecules when the light is incident and therefore the frequency of the scattered light will be different from the incident light. There are two transitions of Raman scattering. If the frequency of scattered light is lower than the incident light that means some energy is transferred to the molecules and the corresponding Raman spectra is called Stokes. On the other hand, it is called anti-Stocks.[29] The Raman shift in wavenumber (cm^{-1}) is calculated by

$$\text{Raman shift} = \frac{1}{\text{wavelength of incident photon}} - \frac{1}{wavelength\ of\ scattered\ photon} \quad (2)$$

The Stokes and anti-Stokes are symmetrical distributed in two side of Rayleigh line. The intensity of the anti-Stokes peaks is far lower than the Stokes peaks because of the Boltzmann distribution, i.e. the numbers of electron on the ground state are far more than the numbers of electron on the vibrational level.[30]

Figure 2-6 Front view of Horiba Jobin Yvon HR-800 Confocal Raman system.

A Horiba Jobin Yvon HR-800 Raman spectroscopy was employed in our measurement. Figure 2-6 shows the experimental setup of the Horiba Jobin Yvon HR-800 Raman spectroscopy. For our measurement, a cyan 488 nm laser was used as the exciting laser. The model of the laser source is Spectra-Physics PC14584 and its output power is 50 mW.

There were two sets of grating (1800 grooves/mm and 3000 grooves/mm) that we could choose in the measurement. Moreover, a neutral filter, which could adjust the intensity of laser from 50 mW to 5 μW to prevent damage of the samples, was used.

2.2.2 Photoluminescence

2D materials exhibit an indirect-direct bandgap transition when they are scaled down from bulk to monolayer. In a typical photoluminescence experiment, the 2D materials are excited with a light source providing photon energy larger than the bandgap of the 2D materials. Photon with enough energy (>= the bandgap) will produce electron-hole pairs in the conduction and valence band. The excitations will then undergo recombination with the release of photon possessing energy equals to the bandgap minimum.[31] In the recombination, the recombination of free carriers and free excitons dominates the signal of the PL spectra. The bandgap is calculated by

$$E_g = \frac{hc}{\lambda} \quad (3)$$

, where E_g is bandgap of semiconductor, h is Planck's constant, c is speed of light and λ is wavelength of light.[32]

In this thesis, the PL spectra was measured by the Horiba Jobin Yvon HR-800 system. The excited laser was 488nm cyan laser. The intensity of laser was decreased from 50 mW to 5 μW to prevent damage of samples during PL measurement.

2.2.3 Atomic Force Microscopy

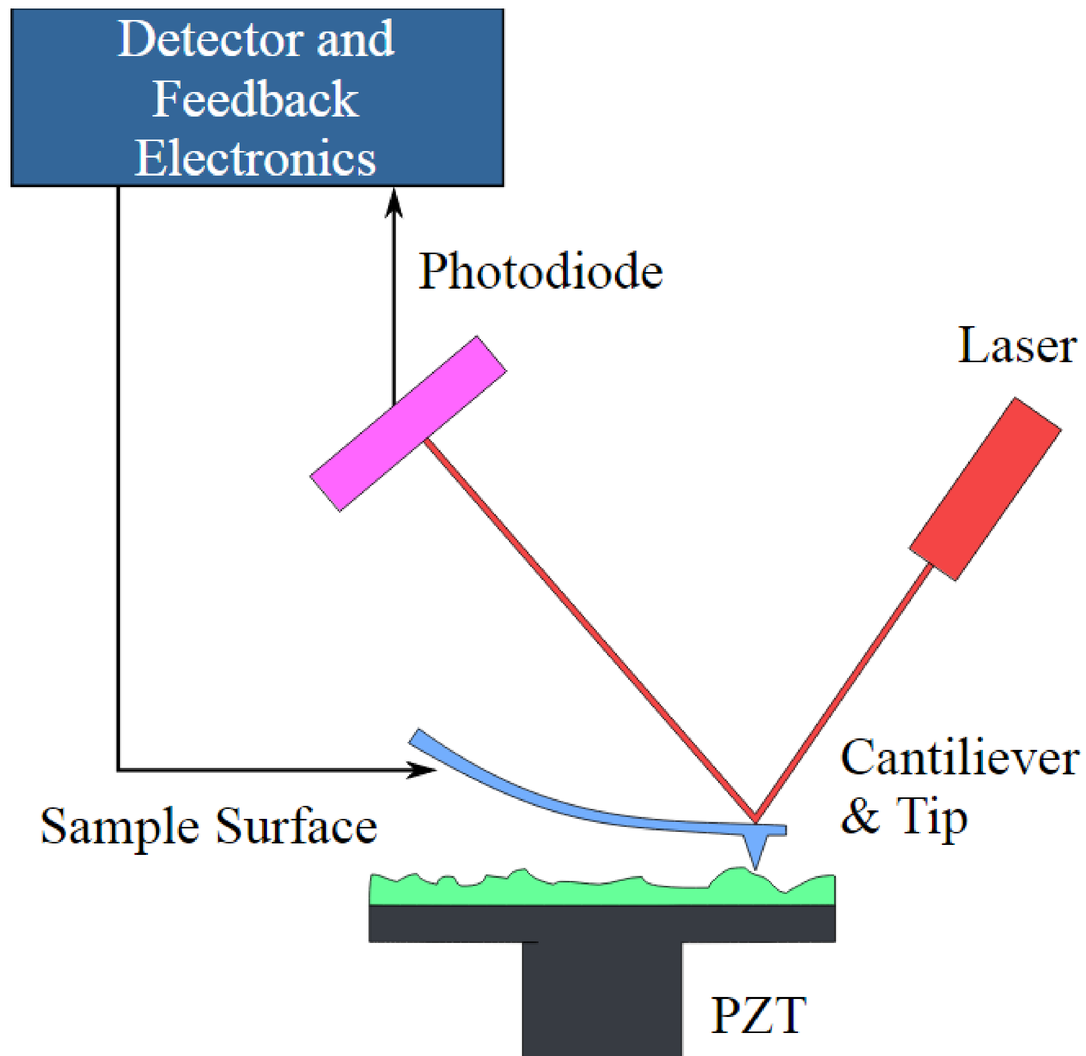


Figure 2-7 Block diagram of AFM using beam deflection detection.

Atomic force microscopy (AFM) uses a sharp tip scan through the sample. The variation of the force between the tip and sample surfaces allows us to obtain the morphology of the samples. The tip is mounted on the end of a cantilever. When the tip scans the sample feature, the force between the tip and sample will bend the cantilever, and there is a detector sensing the deflection of the cantilever. A feedback electronics is connected to the cantilever to keep the distance between the tip and sample

constantly. The feedback signal is then transferred to a computer to output an image of the sample surface.[33]

There are three basic modes of AFM, namely, contact mode, tapping mode and non-contact mode. For contact mode, the tip is directly contact across the surface of the samples. The force between the tip and surface sample can be described by the Hooke's law, f=-kx, where k is force constant of the cantilever and x is the displacement. This mode leads to a quite strong repulsive van der Waals force among the tip and sample surface, and may damage the surface of 2D materials. For non-contact mode, the tip oscillates outside of the repulsive regime. This mode eliminates the strong frictional force between the tip and surface, but the resolution of the imager is quite bad. Tapping mode takes the advantages of both the contact mode and non-contact mode, it oscillates at a resonant frequency and contacts the sample surfaces periodically in an extremely short time. The scanning speed of this mode is much faster than contact mode and non-contact mode, and is suitable for our measurements.

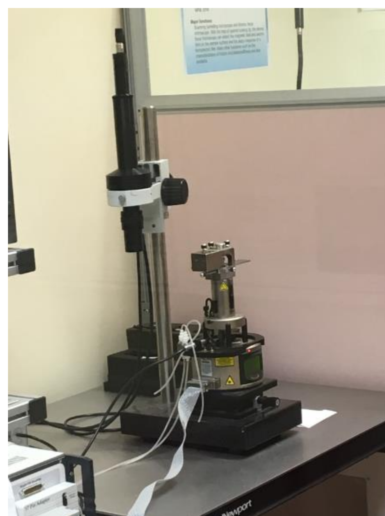


Figure 2-8 Bruker NanoScope 8

2.3 Transfer process

Due to the limited applicability of insulating substrates in electron beam lithography (EBL), transferring WS_2 from sapphire to SiO_2/Si can simplify the process in electron beam lithography.

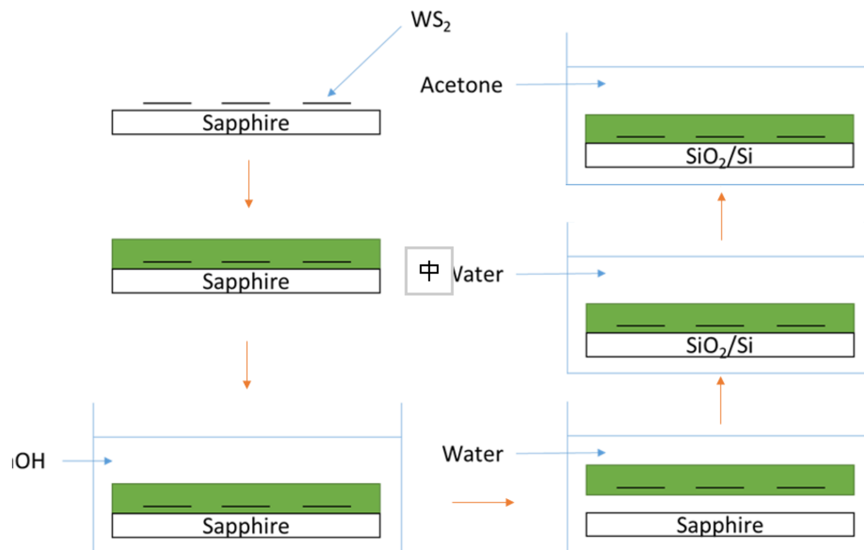


Figure 2-9 Schematic diagram of wet transfer process.

The transfer process is summarized as below:

(i) Spin-coat a layer of PMMA on the WS_2 films and bake it for 1 min at 160 °C at 10 min

(ii) Put the sample into aqueous solution of sodium hydroxide (NaOH) with a concentration of 2 M for 3 min at 100 °C

(iii) Soak the sample into de-ionized water for few seconds. The PMMA coated WS_2 films will be detached

(iv) Transfer the PMMA coated WS_2 to SiO_2/Si substrate in de-ionized water. Bake it 10 min to increase its adhesion

(v) Place the sample into acetone for 24 h to remove the remained PMMA layer

2.4 Patterning of Substrate Marking

2.4.1 Photolithography

General speaking, for fabricating electronic devices, it contains many steps of photolithography. In modern semiconductor manufacturing, this photolithography technique is typically used in microfabrication of pattern on thin films or substrates. The patterned features are accomplished by spin-coating an ultraviolet (UV) light sensitive chemical on substrates, which are then exposure to the UV light through a photomask. For a positive photoresist, the light increases the solubility of the resist, so the resist can then be dissolved by a developer. The minimum feature size is around ~1 μm. This limitation is due to the diffraction limit of light.

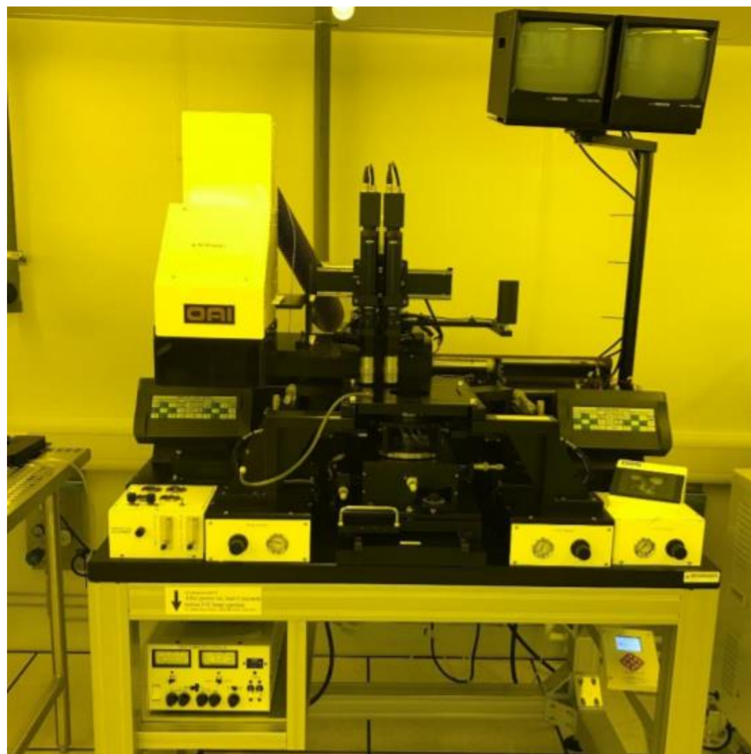


Figure 2-10 UV contact alignment

The steps for photolithography are summarized as below:

(i) Substrate surface cleaning

(ii) Spin-coating photoresist

(iii) Baking

(iv) Mask alignment

(v) Exposure to UV light

(vi) Development

2.4.2 Sputtering

Sputtering is a physical vapor deposition method that a target is eroded by high energy ions within a gaseous plasma, and the released atoms will then be deposited onto a substrate to form a thin film.[34]

Figure 2-11 Experimental setup of a D.C. magnetron sputtering system.

Before depositing the thin film onto the substrate, the chamber's pressure needs to first be pumped down to high vacuum (~10^{-6} Torr) to avoid any potential contaminants. When the required high vacuum is reached, sputtering gas is introduced, and the pressure is fixed in millitorr range. A high voltage is then applied between the cathode (located behind the target) and anode (connected to the chamber as electrical ground) to produce a gaseous plasma. The positive ions are accelerated towards the cathode so that the collisions cause the deposition of thin film onto the substrate.[35] To increase the deposition rate, a high molecular weight gas such as argon is typically

chosen and by using strong magnets which can confine the electrons near the target surface.

The advantages of sputtering are stated as below:

i) No limitation of target materials, and

ii) Similar composition between the target material and the grown film will be maintained

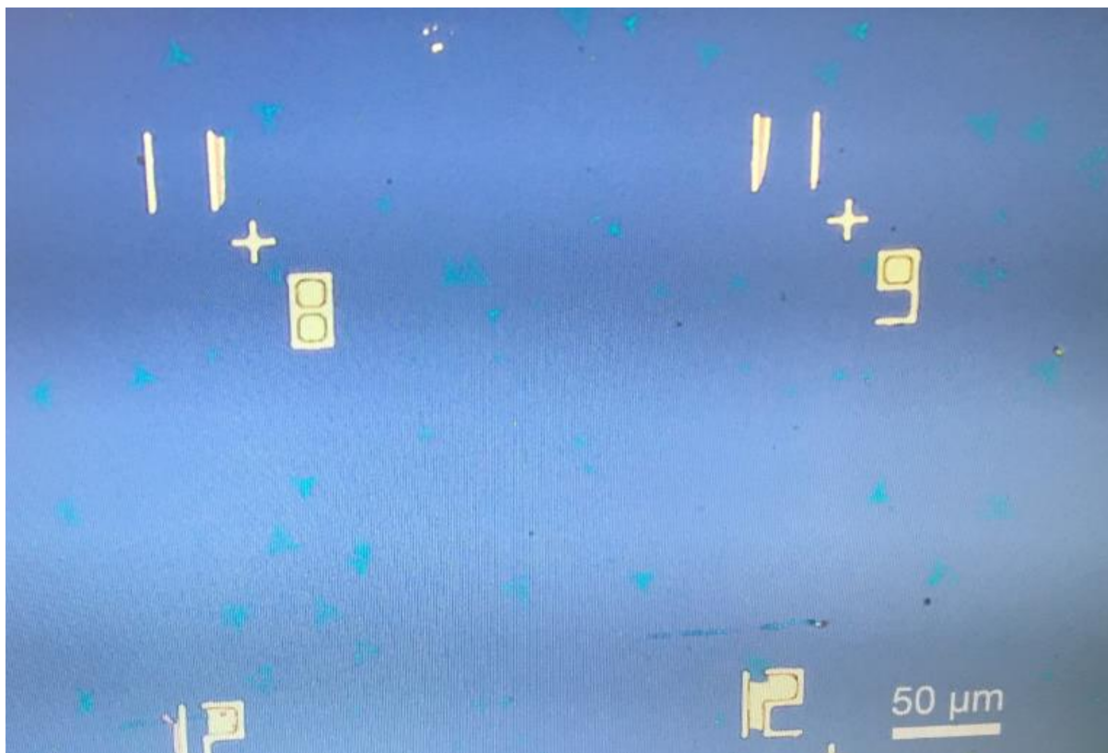


Figure 2-12 Alignment mark on a silicon substrate after gold deposition by magnetron sputtering

2.5 Electrodes Deposition

2.5.1 Electron beam lithography

A Jeol JIB multi beam system was used to produce pattern of any types on arbitrary substrates for our p-n junction and p-i-n junction patterning.

Due to the extremely small wavelength of electrons, whereas photolithography is limited by the wavelength of light source, Electron Beam Lithography (EBL) is a useful technique for creating nano-structures that cannot be fabricated by photolithography. A high-quality EBL system can even achieve resolutions of a few nanometers.

Figure 2-13 JEOL JIB-4501 scanning electron microscope equipped with the module of nano-pattern generation system.

For EBL, the system makes use of a scanning electron microscope, a pattern generator and a beam blanker to control which areas are needed to be exposed. During the process, a highly focused electron beam is exposed to a resist. It significantly changes the solubility of the resist. After the exposure, the resist is developed in a solvent (Isopropyl alcohol: Methyl isobutyl ketone: 3:1). Similar with photolithography, the

electron beam resist either dissolved or presence, is also depended on which type of electron beam resist is being used. The solvent will then either dissolve or remain presence in the exposed areas of the electron beam resist.

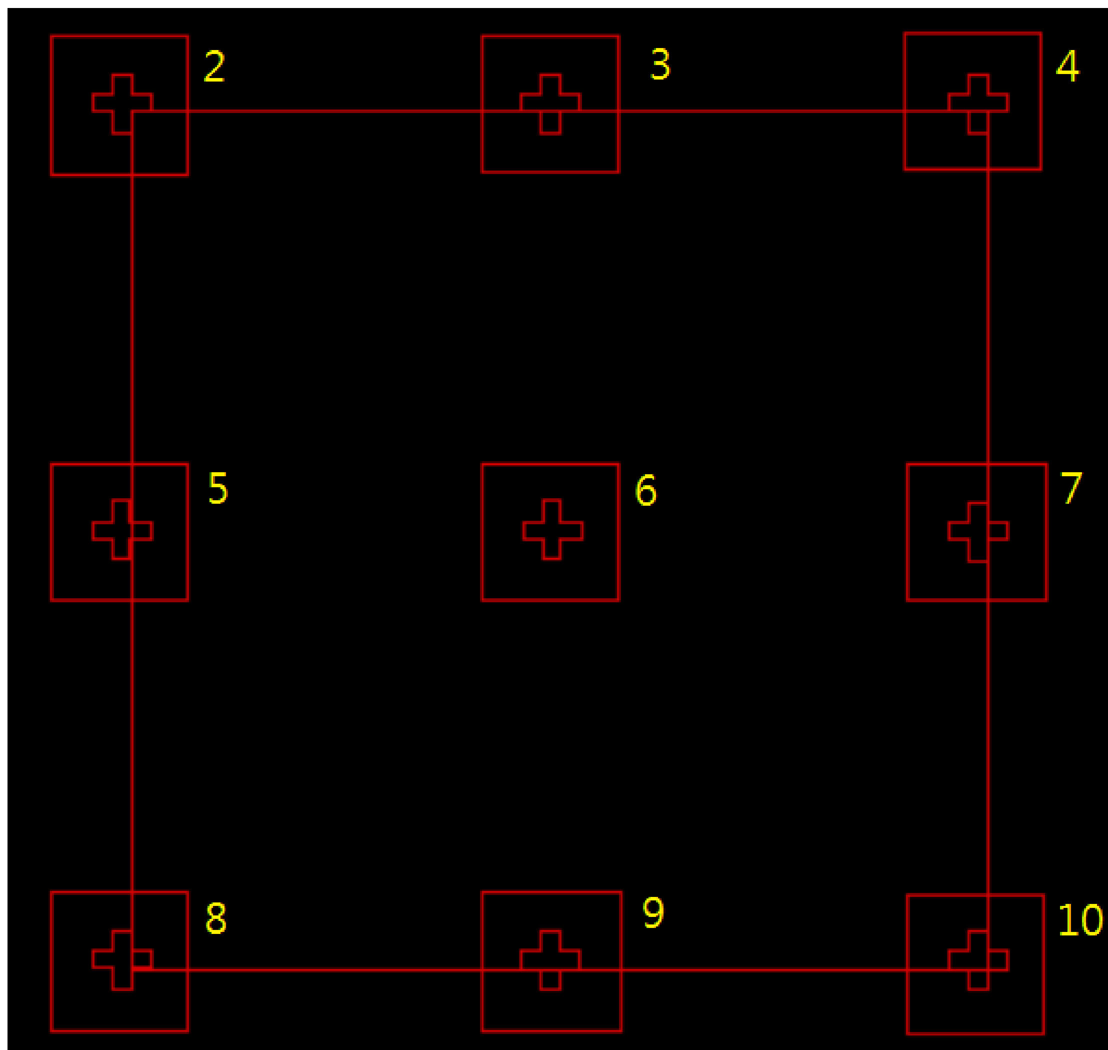


Figure 2-14 DesignCad program for pattering in electron beam lithography.

Figure 2-14 shows the designed pattern for alignment using electron beam lithography. Each of the alignment was separated by 125 μm. For a sample which did not require a precise pattern, we chose three out of four alignment marks (No. 2, 4, 8, 10) for the

alignment. Otherwise, three out of four alignment marks (No. 6, 7, 9, 10) for the alignment are needed.

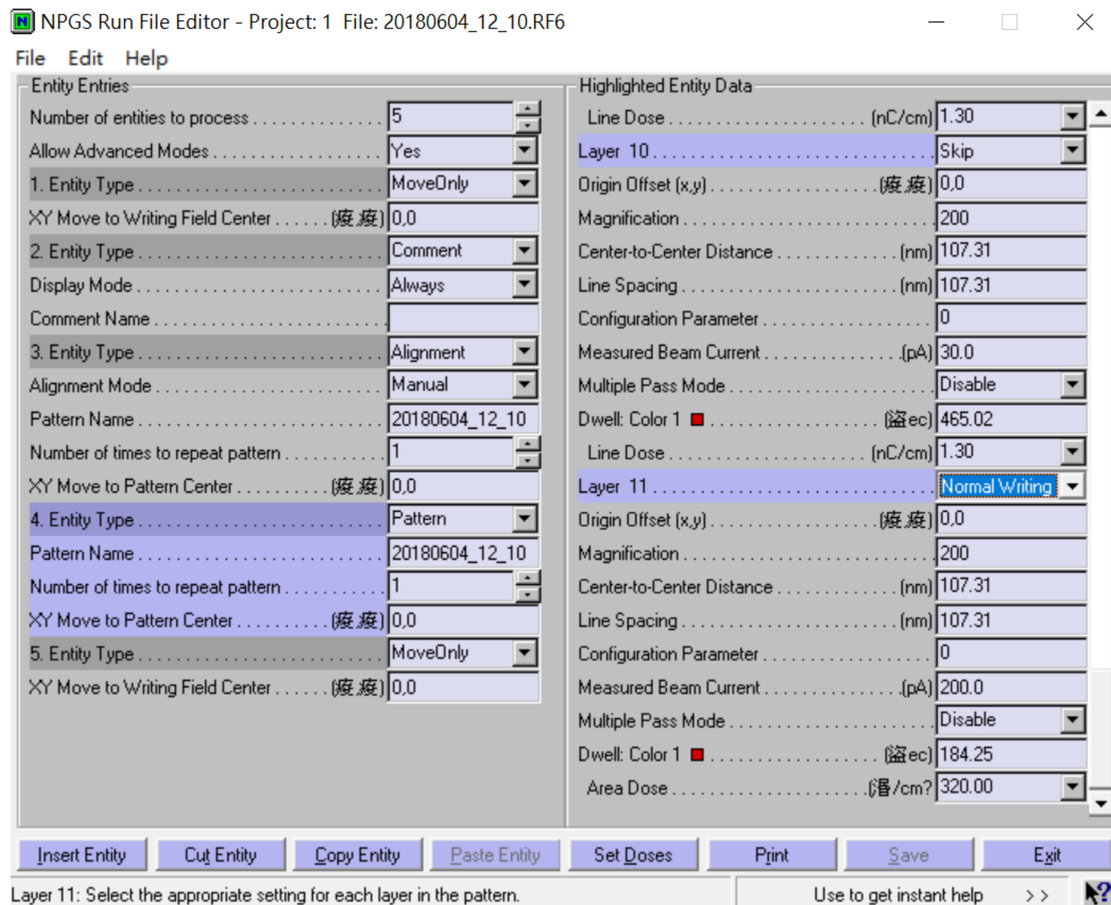


Figure 2-15 Setting in EBL

Figure 2-15 shows the optimized conditions for the electron beam lithography. The optimized beam current and area dose were 200 pA and 320 μC/cm^2 respectively. Too small beam current would lead to PMMA residue remained on 2D materials, while too large beam current would damage the 2D materials and might lead to significantly low mobility of the device. [36-39]

2.5.2 Electron beam evaporation

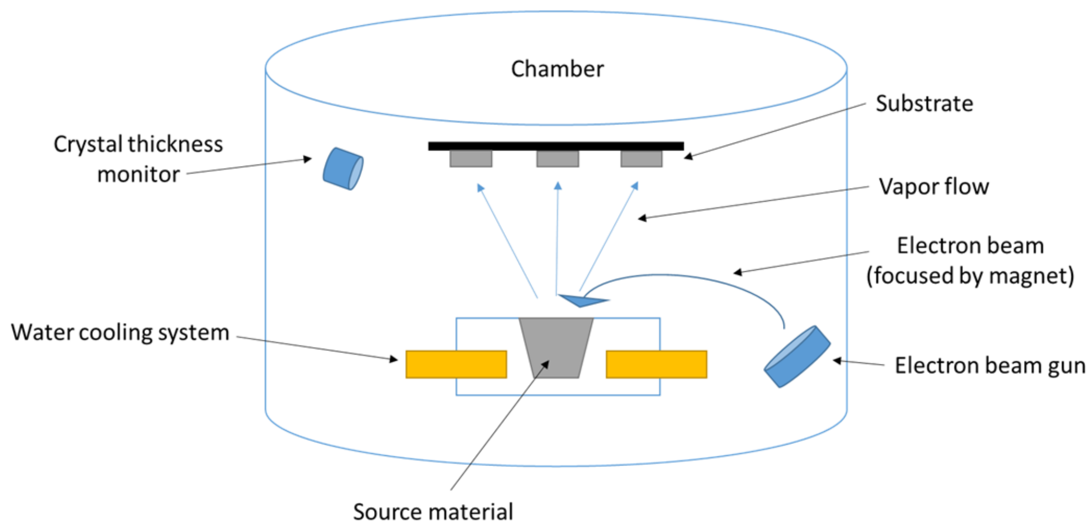


Figure 2-16 Schematic diagram of an electron beam evaporator.

Same as sputtering, electron beam evaporation is a very common type of physical vapor deposition technique. It is a thermal evaporation process that electron beam is exposed to targets providing a large amount of thermal energy. This beam can evaporate metals or dielectric materials to form films even though the materials have very high melting temperatures. To generate an electron beam, a current is passing through a filament locating outside the deposition zone to avoid any contamination during the deposition. The heated filament will generate thermionic emission of electrons which are then focused by the magnetic field to make the electron beam directly injecting to the target. Table 2 lists the deposition conditions of our devices.

Table 2 Deposition parameters in electron beam evaporation

Materials	Density(g/cm^3)	Impedance(10^5gcm^{-2}s^{-1})	Deposition rate(Á/s)	Thickness(nm)
Titanium	4.5	14.05	0.2	5

Gold	19.3	23.17	0.3	50
SiO_2	2.65	1.00	0.1	2

2.6 Mechanism of the formation of the Schottky barrier

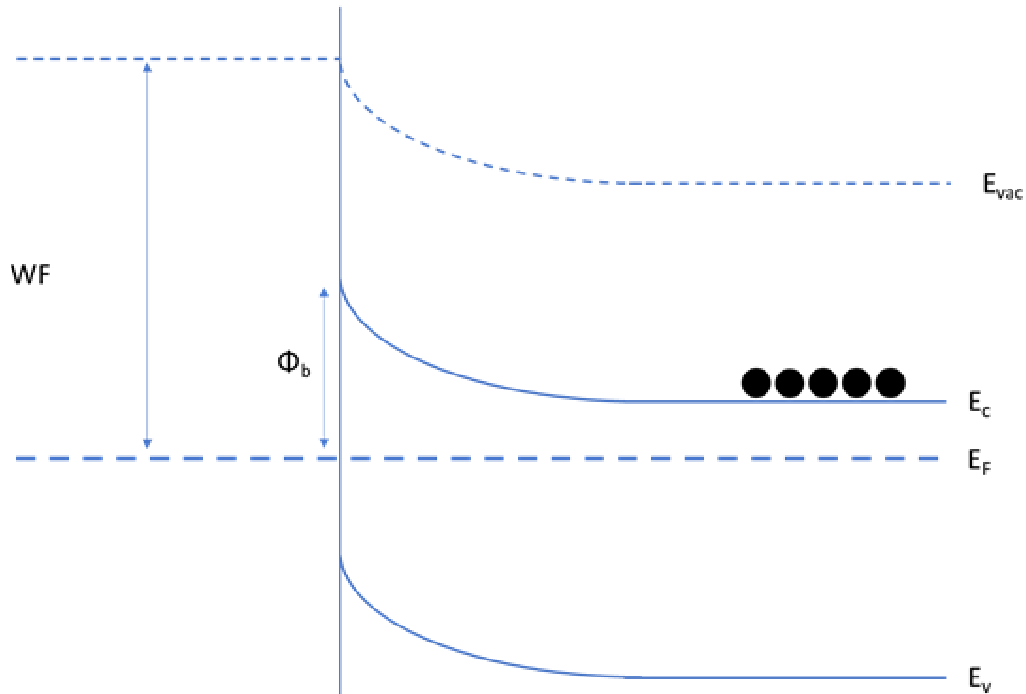


Figure 2-17 Schematic band diagram of a p-type conducting polymer and n-type semiconductor, where Φ is the work function, Evac is the vacuum level, E_c is the conduction band of n-type semiconductor and E_v is the valence band of n-type semiconductor.

The formation of the Schottky barrier is explained by Figure 2-17. When a p-type conducting polymer and n-type 2D materials are in contact, the band bends so that electrons flow from n-type and enters into the LUMO level of p-type conducting polymer, forming a Schottky barrier.[40] The barrier height depends on the work

function of p-type conducting polymer and the surface states on n-type 2D material.[41] When positive gate voltage was applied, the charge density of n-type 2D material increased which causes the upward shift of Fermi level in n-type 2D material. The upward shift of Fermi level in n-type 2D material result in a lowering of Schottky barrier. The lower potential barrier that more electrons will diffuse towards the p-type conducting polymer so $I_{forward}$ increase.

Due to the thermal activation at high temperature, the charge density of n-type 2D material was increased significantly that also causing the upward shift of Fermi level, resulting in a lower potential barrier. In contrast, due to the inhibition of the thermal activation at low temperatures, the charge density was reduced and became the limiting factor of $I_{forward}$.

2.7 Electrical Characterization

2.7.1 Probe station with 4200 semiconductor analyzer

For p-n diodes, the rectifying properties could be revealed by measuring its current-voltage characteristics. For our devices, current of pico-amperes to nano-amperes was expected to pass through the p-n junction. In our studies, the currents were measured by a LAKESHORE_Low Temperature IV probe station with a Keithley 4200 semiconductor analyzer. Keithley 4200 is a multi-source meter that can be served as either a power source, voltage source or current source. The resolution of this equipment reached up to 0.1 fA. During measurement, the system's pressure was pumped down to 10^{-6} Torr to avoid any interference during the measurement. Furthermore, this system was also connected to a cold compressor such that the samples could be measured at various temperature.

Figure 2-18 A typical current-voltage characteristics of a conventional semiconducting diode.

2.7.2 The Transmission Line Method

Beside measuring the I-V characteristics, the probe station was also used to measure the conductivity and contact resistance of our samples.

1. Junction preparation

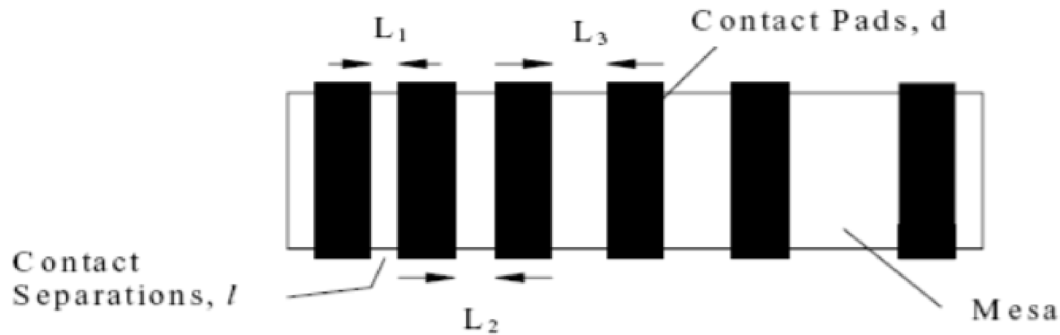


Figure 2-19 A typical arrangement for a TLM test pattern

To measure the contact resistance of a metal-semiconductor junction, a specific metal electrode pattern was deposited on the semiconductor. Figure 2-19 shows the metal pattern in our measurements. The metal-semiconductor contacts were formed on the sample and the electrodes were separated by a distance L_i. All the electrodes on the semiconductor had the same width (W) and length (d) and were separated in different distances.

The resistance between two contacts R_i is equal to

$$R_i = 2R_c + R_{sh}\frac{l_i}{W} \tag{4}$$

, where R_c is the contact resistance of the semiconductor, R_{sh} is the sheet resistance of the semiconductor, L_i is the separated distance and W is the width of the electrodes.[42]

2. I-V measurement

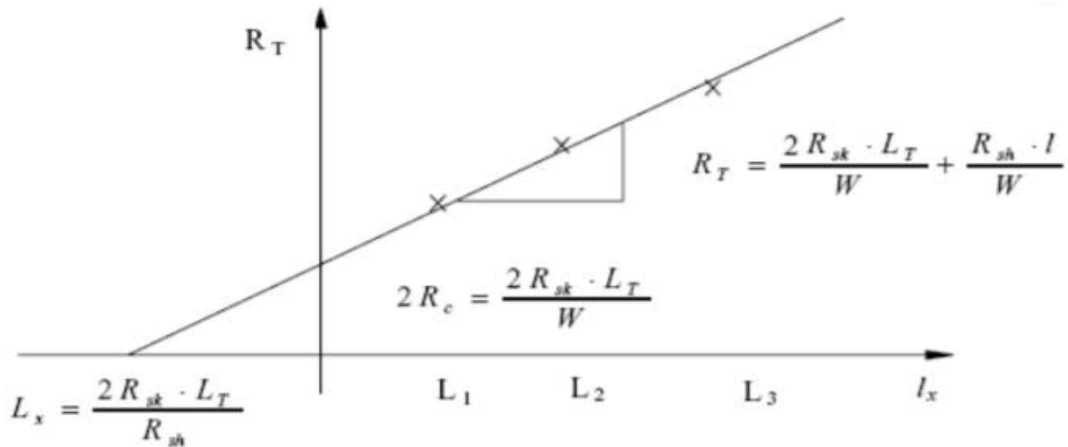


Figure 2-20 Plots of total resistance versus contact spacing

The measurements are just required simple I-V measurement. By using the probe station and semiconductor analyzer, the resistance between two electrodes R_i can be obtained. By plotting the R_i to L_i curve, a straight line will be obtained. The slope of the straight line represents the value of R_{sh}/W and the y intercept of the straight line gives the value of 2 times of contact resistance. [42]

Chapter 3 **Materials characterization**

3.1 WS_2

3.1.1 Raman and PL spectra of WS_2

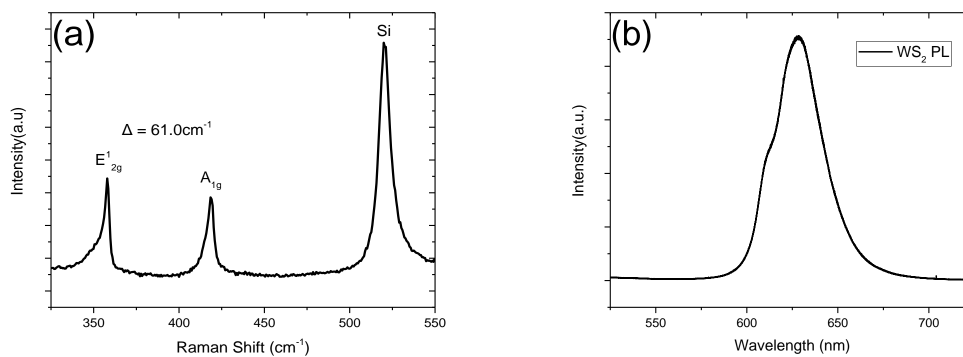


Figure 3-1 (a) The Raman spectrum of the CVD grown WS_2 on a SiO_2/Si substrate. (b) The photoluminescence spectrum of the CVD grown monolayer WS_2. The excitation laser was 488 nm.

Figure 3-1 (a) and (b) are the Raman and photoluminescence (PL) spectra of WS_2 flake. The Raman mode difference between the A_{1g} mode and E^1_{2g} mode was 61.0 cm^{-1} which confirmed the identity and monolayer nature of the WS_2.[43] The strong PL peak obtained at the 630 nm (2.0 eV) responded to the direct bandgap nature of WS_2.

3.1.2 Electrical characterization of WS_2

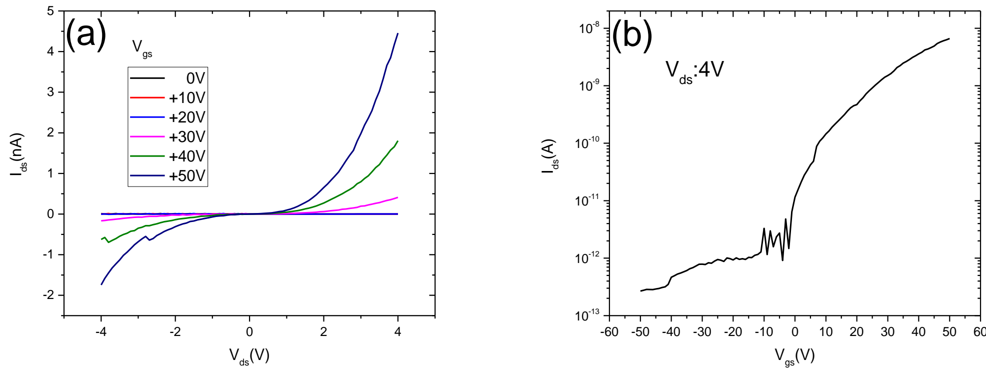


Figure 3-2 Drain-source current (I_{ds}) versus drain-source voltage (V_{ds}) of WS_2 FET for various back-gate voltage bias (V_{gs}) taken in vacuum. (b) Transfer characteristics of WS_2 FET.

WS_2 is a n-type semiconductor, its conductivity is expected to be exponentially increasing when a positive gate voltage bias is applied as shown in Figure 3-2.

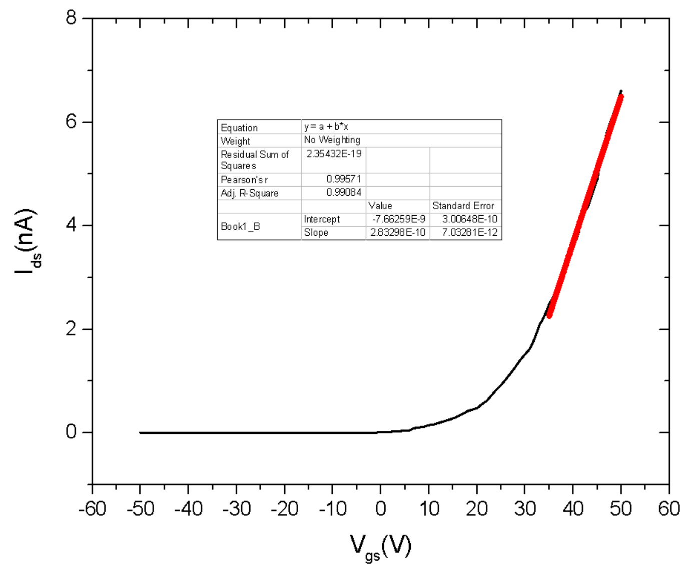


Figure 3-3 Room-temperature transfer characteristics for the WS_2 FET with 4V

applied bias voltage V_{ds}.

From the presented Figure 3-3, by using the Equation 5,

$$\text{mobility } \mu = \frac{dI}{dV} \text{x} \frac{L}{WCV} \quad (5)$$

, where in our measurement L is the channel length = 1 μm, W is the channel width = 5 μm and C is the capacitance between the channel and the back gate per unit area = 1.17 x 10^{-4} F m^{-2} (C = $\varepsilon_o \varepsilon_r/d$; ε_r = 3.9; d = 300 nm). [11] As a result, we extracted the field effect mobility of WS_2 to be 0.5 $cm^2V^{-1}S^{-1}$. The relatively low mobility might be due to the interfacial charged impurities[44-46] and the remained PMMA residue on WS_2 after the wet transfer. The rectification ratio of WS_2 FET is about 10^5 which is comparable with value reported in literature.[47]

3.2 MoS_2

3.2.1 Raman and PL spectra of MoS_2

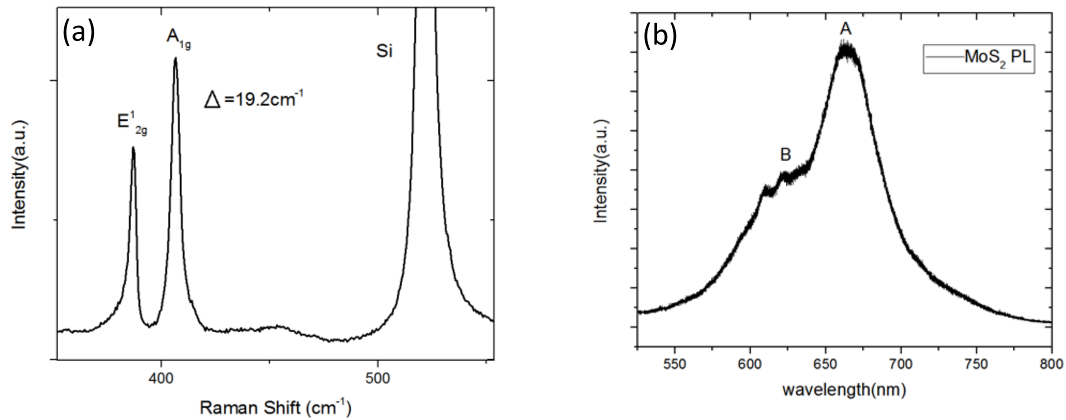


Figure 3-4 (a) The Raman spectrum of the CVD grown MoS_2 on the SiO_2/Si substrate. (b) The photoluminescence spectrum of the CVD grown monolayer MoS_2. The excitation laser was 488 nm.

Figure 3-4 (a) and (b) are the Raman and photoluminescence (PL) spectra of MoS_2 flake. The Raman mode difference between the A_{1g} mode and E^1_{2g} mode was 19.2 cm^{-1} which confirmed the identity and monolayer nature of the MoS_2.[48, 49] The strong PL peak obtained at the 620 nm (2.0 eV) and 670 nm (1.85 eV) responded to the A and B optical transition of MoS_2.[50]

3.2.2 Electrical characterization of MoS_2

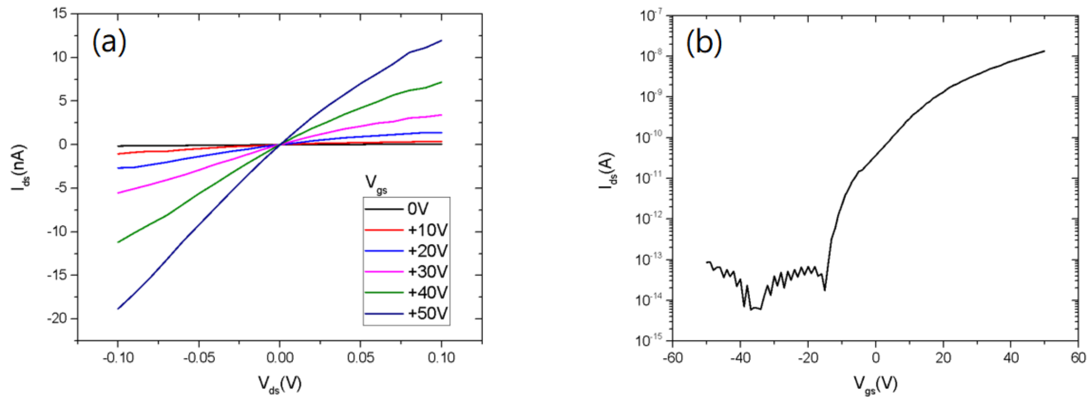


Figure 3-5 (a) Drain-source current (I_{ds}) versus drain-source voltage (V_{ds}) of MoS_2 FET for various back-gate voltage bias (V_{gs}) taken in vacuum. (b) Transfer characteristics of MoS_2 FET.

MoS_2 is also a n-type semi-conductor, its conductivity is expected to be exponentially increasing when positive gate voltage bias is applied as shown in Figure 3-5.

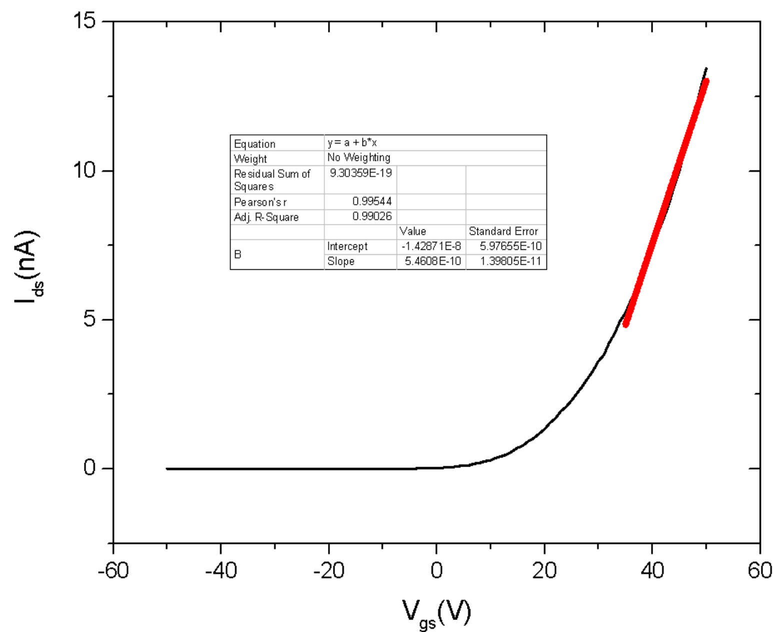


Figure 3-6 Room-temperature transfer characteristics for the MoS_2 FET with 4V applied bias voltage V_{ds}

From Figure 3-6, using the Equation 5 again,

$$\text{mobility } \mu = \frac{dI}{dV} \text{x} \frac{L}{WCV}$$

the obtained field effect mobility of MoS_2 was 15 $cm^2V^{-1}S^{-1}$ and the rectification ratio of MoS_2 FET was about 10^6. This mobility is a little bit lower than the value reported in the literature. [11] The reason may be due to the 2D materials grown by CVD method. General speaking, large area of monolayer MoS_2 have been successfully synthesized by CVD method which is known to be the most practical method of synthesizing large area and high quality monolayer MoS_2. However, studies showed that devices based on these polycrystalline MoS_2 films are still not as good as their exfoliated counterparts.

One of the possible reasons may be due to the detrimental effects of the grain boundaries.[51]

3.3 Pedot:PSS

3.3.1 Raman spectrum of Pedot:PSS

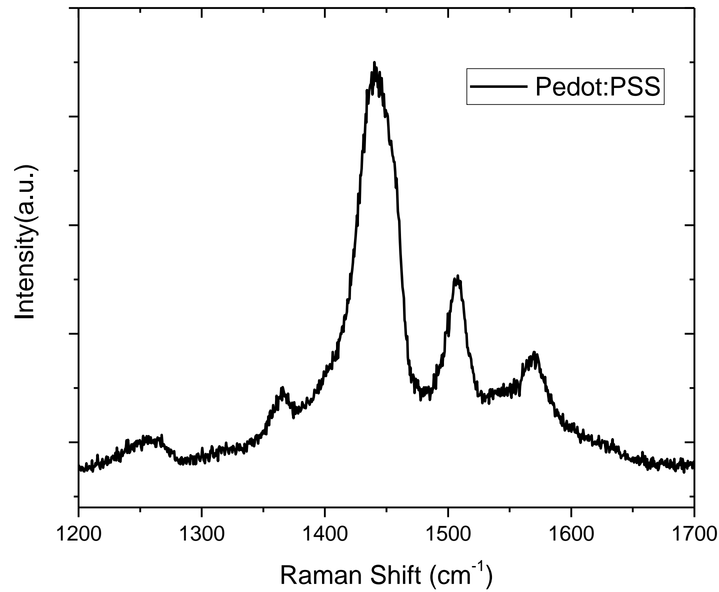


Figure 3-7 The Raman spectrum of Pedot:PSS (Al4083). The excitation laser was 488 nm.

Figure 3-7 shows the Raman spectrum of Pedot:PSS after deposition which proves that Pedot:PSS has excellent quality that can be used to fabricate our devices.[52]

3.3.2 Electrical characterization of Pedot:PSS

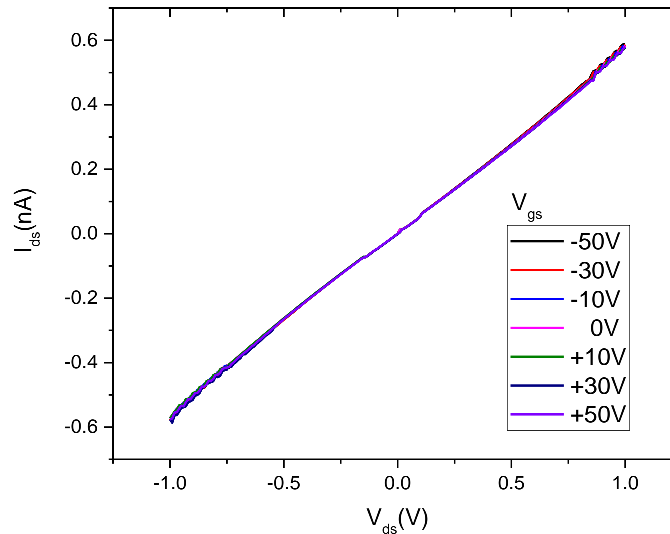


Figure 3-8 Current-voltage (I_{ds}-V_{ds}) curve for Pedot:PSS connected in a FET configuration in vacuum under various back-gate voltage bias from -50 V to +50 V

Figure 3-8 shows the current-voltage characteristics of Pedot:PSS film. When the Pedot:PSS was connected in the FET configuration, the slope of I-V curve was linear and did not show any change even if the back gate voltage bias varied between -50V and 50V. This behavior might be due to the high charge carrier density in the conducting polymer and the external electric field was screened on an atomic scale, so it followed the ohmic conductor at low voltage bias. [40]

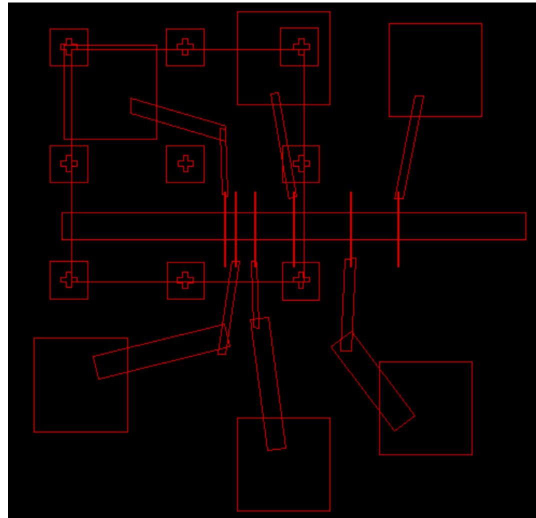


Figure 3-9 The DesignCad pattern of measuring Pedot:PSS sheet resistance using transmission line method

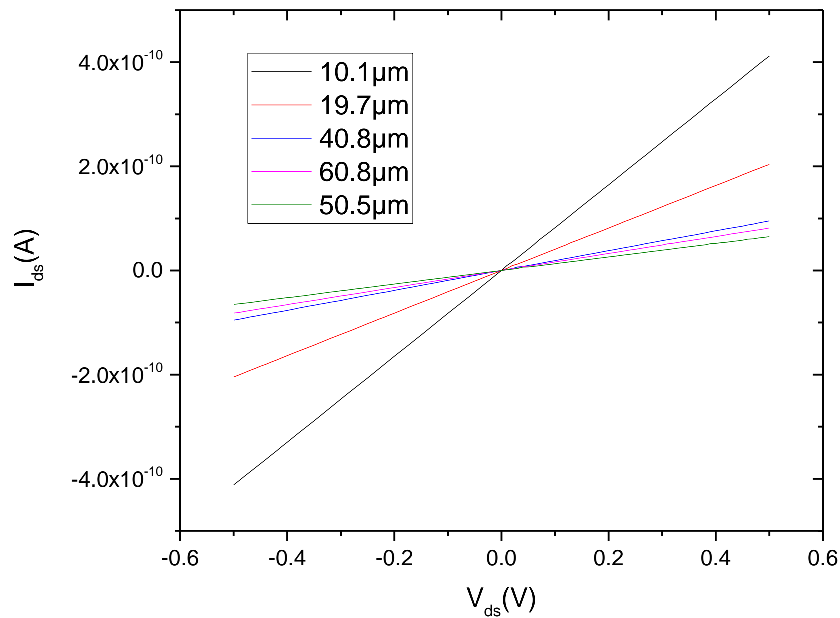


Figure 3-10 Current-voltage (I_{ds}-V_{ds}) curve for Pedot:PSS(Al4083) with various distance separations.

A series of Au/Ti electrodes with various distance separations (10.1 μm, 19.7 μm, 40.8 μm, 50.5 μm and 60.8 μm) were deposited on SiO_2/Si substrates before spin-coating of

Pedot:PSS(Al 4083). After spin-coating Pedot:PSS(Al4083) on the electrodes, I-V measurements were made between different pairs of electrodes. Figure 3-10 shows the I-V curve of the Pedot:PSS(Al4083) with different electrodes separation. For lengths of 10.1 μm, 19.7 μm, 40.8 μm, 50.5 μm and 60.8 μm, resistances of 1.21×10^9 Ω, 2.45×10^9 Ω, 4.66×10^9 Ω, 6.11×10^9 Ω and 7.67×10^9 Ω were obtained respectively.

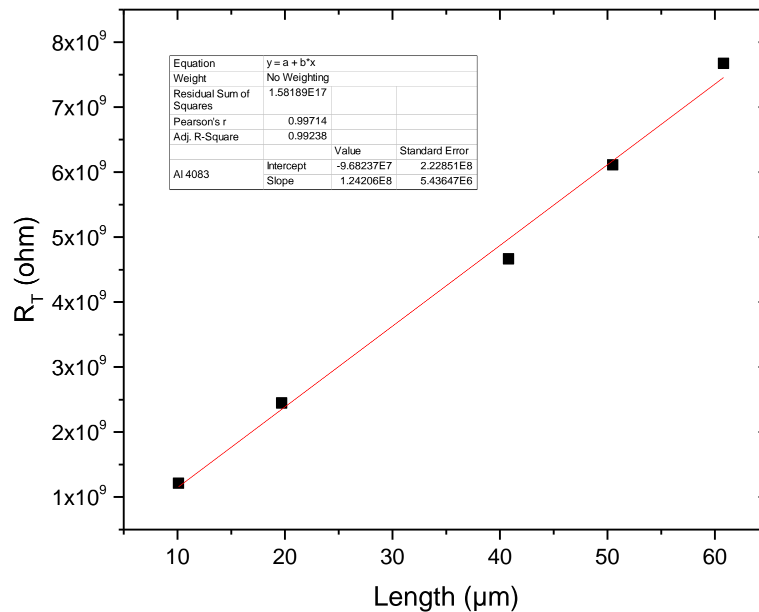


Figure 3-11 Total resistance for Pedot:PSS (Al4083) with various contact separation.

By plotting resistance versus contact separation graph, the information of contact resistance and sheet resistance were obtained. First, the best fit line based on least square method was plotted. Then, the intercept of the line with the y-axis was two times of the contact resistance. Theoretically, the data points should be lied on a straight line, and the slope of the line is the sheet resistance. However, our data points(Figure 3-11) cannot connect into a straight line. This might probably due to the

unstable electron beam current during the EBL experiment. Although the electron and area dose for the patterning were set as 200 pA and 320 μC/cm^2 respectively, electron beam was quite unstable that the current value varied a lot during the experiment. For example, too small beam current would lead to PMMA residue remained on 2D materials which resulted in a large contact resistance for a specific electrode. The fitting slope of the line was 1.24x10^8 Ω/μm. By the Equation 6,

$$\mathrm{m} = \frac{R_{sh}}{\mathrm{W}} \tag{6}$$

, where R_{sh} is the sheet resistance and W is the width of the electrodes, it is found that R_{sh} of Pedot:PSS (Al4083) is around 3.63x10^9 Ω/sq.

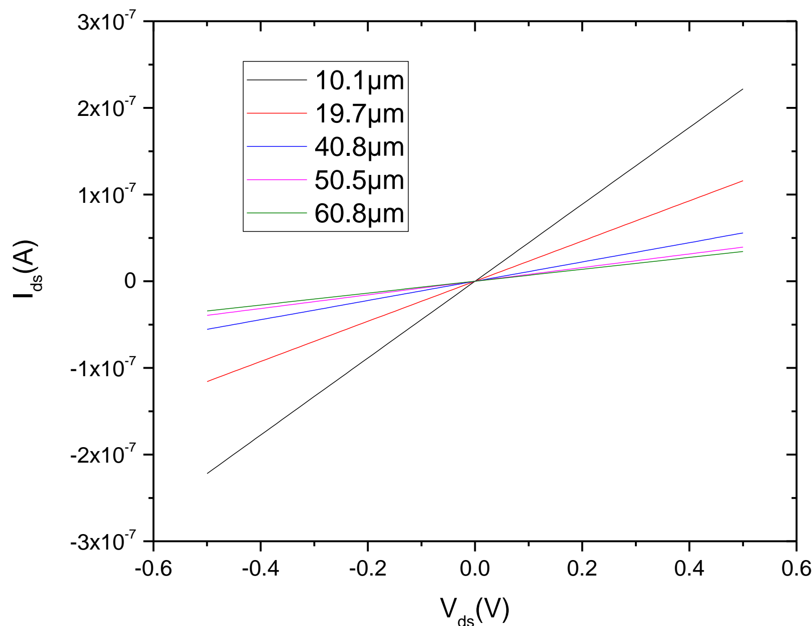


Figure 3-12 Current-voltage (Ids-Vds) curve for Pedot:PSS (AlPH500) with various

distance separations.

Another series of Au/Ti electrodes with various distances separation (10.1 μm, 19.7 μm, 40.8 μm, 50.5 μm and 60.8 μm) were also deposited on the SiO_2/Si substrate before spin-coating of Pedot:PSS(PH500). After spin-coating Pedot:PSS(PH500) on the electrodes, I-V measurements were also made between different pairs of electrodes. Figure 3-12 shows the I-V curve of the Pedot:PSS(PH500) with different electrodes separation. For lengths of 10.1 μm, 19.7 μm, 40.8 μm, 50.5 μm and 60.8 μm, resistances of 2.25×10^6 ohm, 4.32×10^6 ohm, 8.99×10^6 ohm, 1.27×10^7 ohm and 1.46×10^7 ohm were obtained respectively.

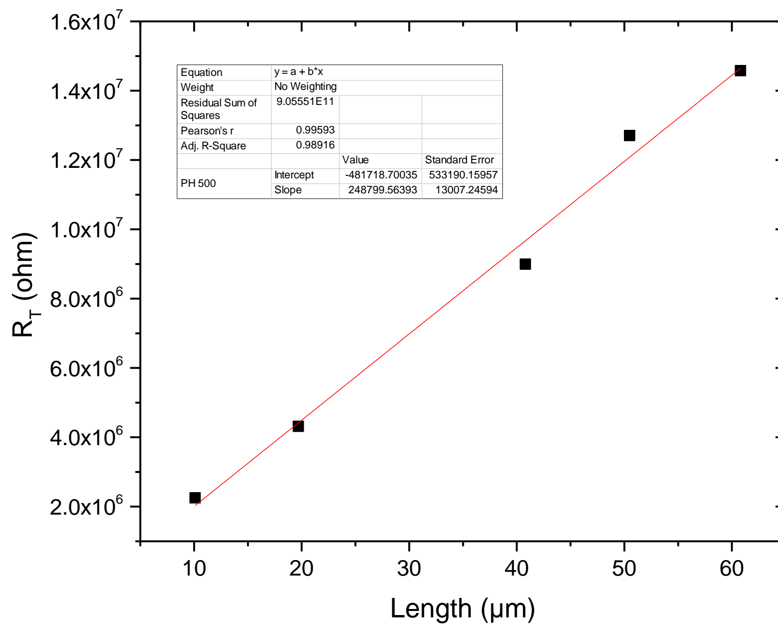


Figure 3-13 Total resistance for Pedot:PSS (PH500) with various contact separation.

Figure 3-13 is the Pedot:PSS(PH 500) resistance versus contact separation graph. By simply fitting the slope of R_T-length curve, the slope of this curve equals to 2.49×10^5 Ω/μm. Similarly, using the formula

$$\mathrm{m} = \frac{R_{sh}}{\mathrm{W}}$$

it was found that R_{sh} of Pedot:PSS (PH500) was around 7.46×10^6 Ω/sq. i.e., Pedot:PSS (PH500) is more conductive than Pedot:PSS (Al 4083).

Chapter 4 Fabrication of Pedot:PSS/WS_2 heterostructures

4.1 Fabrication procedures of Pedot:PSS/WS_2 heterojunction.

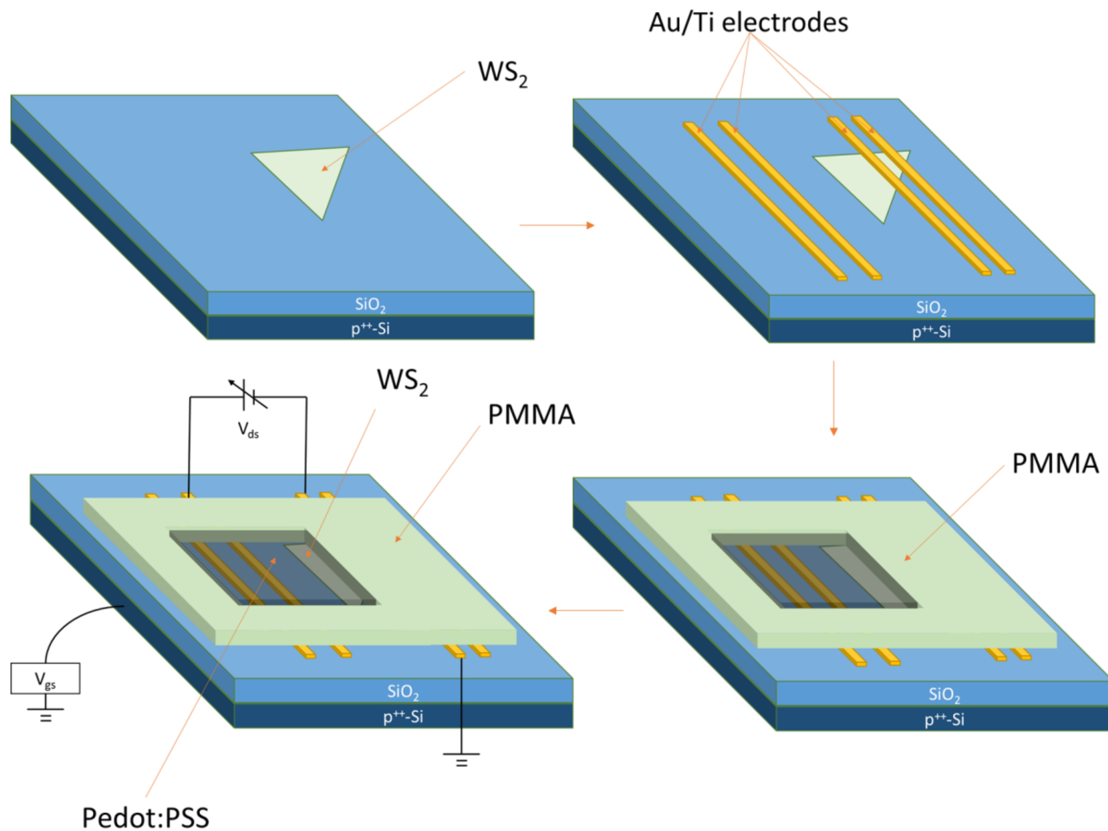


Figure 4-1 Fabrication procedures of Pedot:PSS/WS_2 pn junction devices.

The fabrication process of the Pedot:PSS/WS_2 hetero-junction are summarized as Figure 4-1. Firstly, mono-layer WS_2 flakes were grown on sapphire by chemical vapor deposition (CVD). Then, the flakes were transferred by PMMA wet transfer technique onto p-doped silicon substrates with a 300 nm SiO_2 layer. Secondly, Au(50nm)/Ti(5nm) electrodes were deposited on WS_2 and SiO_2 using e-beam lithography. Here, two

electrodes were deposited partially on top of WS_2 and partially on SiO_2, then another two electrodes were totally on SiO_2 near WS_2. Afterwards, PMMA was spin-coated on the whole device. Another e-beam lithography step was used to remove the PMMA (as shown in Figure 4-1) in order to open a window to allow deposition of Pedot:PSS on WS_2 to produce a hetero-junction. Before spin-coating at 2500 rpm into the PMMA window, the Pedot:PSS aqueous solution (Al4083) was filtered through a 0.45 µm syringe filter. Pedot:PSS (Al 4083) was purchased from Ossila and the ratio of Pedot:PSS (Al4083) used was 1:6 which is one of the most commonly used formulations in thin film electronic devices. The device was then thermal annealed on a hot plate at 150°C for 10 min to enhance the crystallinity of Pedot:PSS. As shown in Figure 4.1, our device consisted of WS_2 field effect transistor (FET), Pedot:PSS/WS_2 hetero-junction, and a Pedot:PSS FET in series. Each part of our device can be electrically characterized independently.

4.2 I-V measurement of Pedot:PSS/WS_2 at room temperature

More than ten Pedot:PSS/WS_2 devices were fabricated and characterized using different monolayer WS_2 flakes. All those devices showed similar electronic properties. In the following chapter, the properties of a typical device is selected to be presented. All the characterizations were measured at vacuum and dark environments to avoid any unwanted situation.

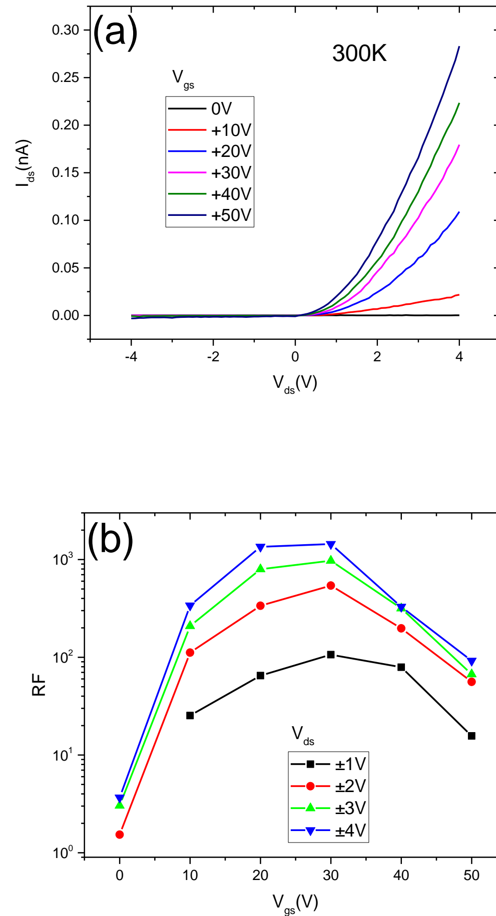


Figure 4-2 (a) Drain current-voltage characteristics at various gate voltage bias in the dark and RT condition. (b) RF curves of Pedot:PSS/WS_2 device measured at different ±Vds various back-gate voltage bias.

The drain current-voltage characteristics of the Pedot:PSS/WS_2 hetero-junction Schottky diode at various gate voltages in the dark and RT condition are plot in Figure 4-2(a). The rectification ratio at V_{ds} = ± 4V was ~5 and the device turn on voltages under various gate voltage bias were around 2V. The I-V characteristics of the Pedot:PSS/WS_2 hetero-junction were also investigated with various gate voltage bias and temperature conditions. Applying a back-gate bias voltage can tune the carrier

density in the WS_2, and therefore can change the barrier height of the heterojunction. As shown in Figure 4-2 (a), our device demonstrates that the device performance was tuned by applying different gate voltage bias. When the gate voltage bias increased from + 10 V to +30 V, the OFF state current magnitude increased insignificantly at around 10^{-13} A and the ON state current magnitude increased slightly from around 10^{-11} to 10^{-10} A. However, when the gate voltage bias increased from +30 to +50 V, the OFF state current magnitude increased from $1.2x10^{-13}$ A to $3.1x10^{-12}$ A, but the ON state kept around 10^{-10} A. As a result, the ON/OFF ratio increased with increasing gate voltage bias from +10 V to +30 V but decreased with increasing gate voltage bias from +40 V to +50 V. Figure 4-2 (b) shows the rectification ratio curves of Pedot:PSS/WS_2 device measured at different drain-source voltage at various back gate voltages. Drain-source voltage from ± 1V to ± 4V also showed similar trend that the ON/OFF ratio increased from 0 V to +30 V but decreased from +40 V to +50 V. A remarkable ON/OFF ratio about 10^3 was reached at V_{ds}: ±4 V and gate voltage bias between +20 and +30 V, which was comparable with the reported value in 2D vdW hetero-structure devices. [17-22] Under +30 V gate voltage bias and ±4 V forward voltage bias, we observed that the device had a very low dark current of ~0.12 pA at the reverse voltage bias and became exponentially increasing at forward bias and the maximum measured rectification ratio of about ~10^3.

4.3 Temperature dependent characterization of Pedot:PSS/WS_2

4.3.1 I-V measurement

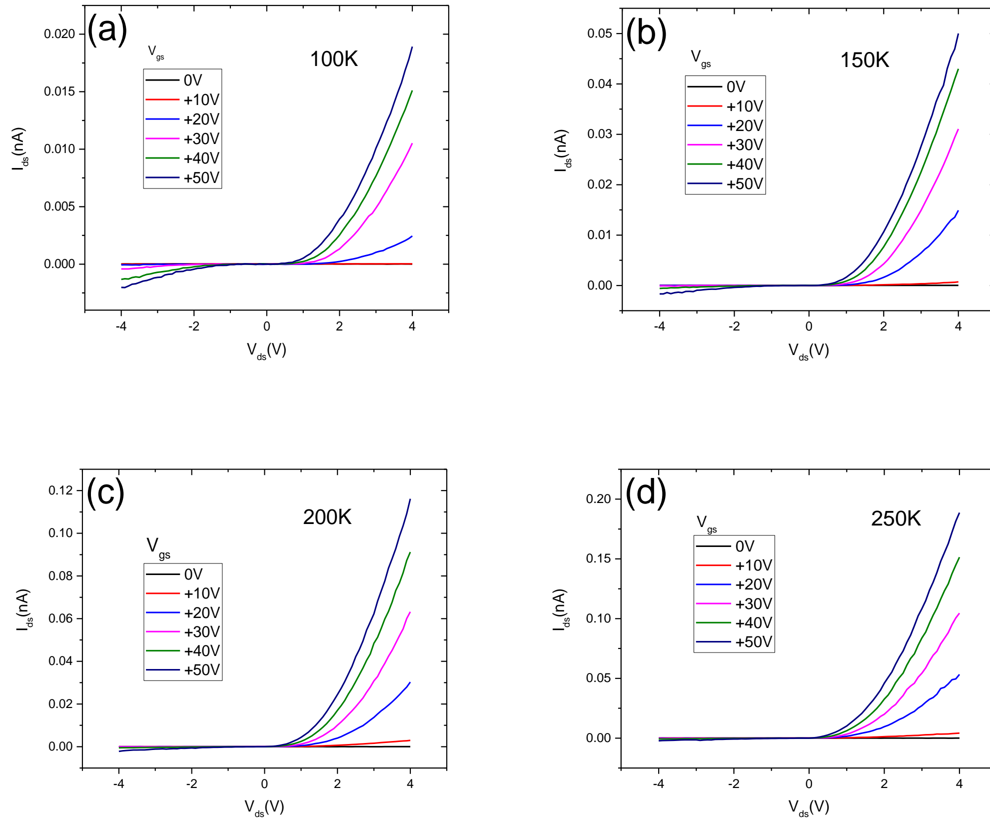


Figure 4-3 Drain current-voltage characteristics at various back-gate voltages at (a) 100K, (b) 150K, (c) 200K and (d) 250K, respectively in the dark and RT conditions.

Figure 4-3 (a-d) shows the current-voltage (I_{ds} – V_{ds}) curves as a function of the gate voltage (V_{gs}) measured at 100, 150, 200 and 250K, respectively. At all temperatures, our device showed a diode-like behavior. In addition, atomically thin WS_2 allows our device to be strongly tuned by V_{gs}.

4.3.2 Relationships between rectification ratio and back-gate bias at different temperature

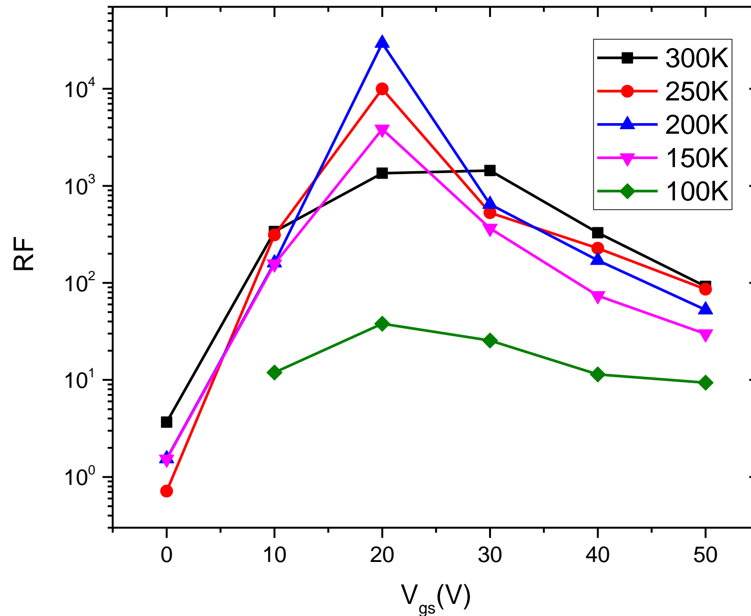


Figure 4-4 Relationships between the rectification ratio (defined as RF = $I_{forwad}/I_{reverse}$) and the back-gate voltage at different temperatures

By defining rectification ratio (RF) = $I_{forward}/I_{reverse}$, a similar trend that RF reached a maximum at V_{gs} = 20 V for all temperature. The highest RF of $4x10^4$ was obtained at 200 K, V_{gs} = 20 V, and V_{ds} from -4 to 4 V. However, a relative low RF was observed at RT, which was owing to the large $I_{reverse}$ at RT. Due to the thermal activation at high temperature, the charge density of WS_2 was increased significantly and became the dominant factor of diffusion ($I_{reverse}$). For T between 100K and 250K, due to the inhibition of the thermal activation at low temperatures, the charge density was reduced and became the limiting factor of $I_{reverse}$.

4.3.3 Relationships between the threshold voltage and temperatures

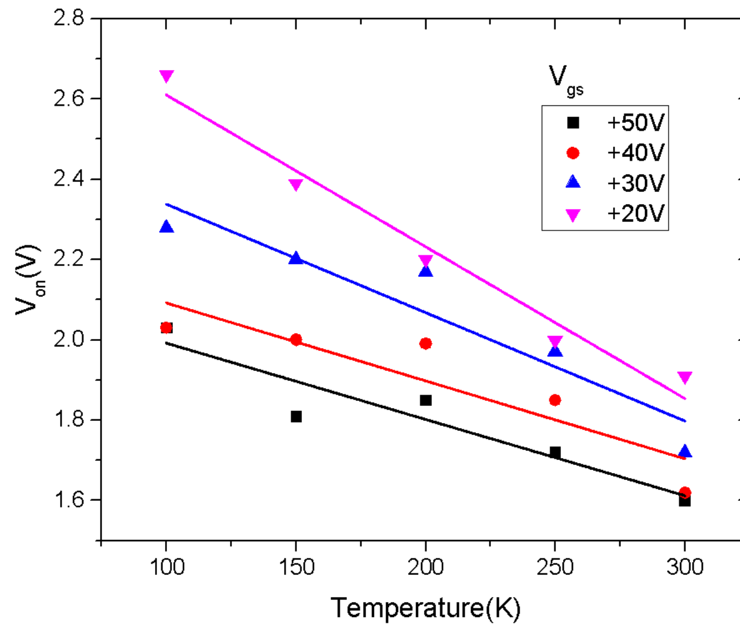


Figure 4-5 Plot of threshold voltage against temperatures.

The turn on voltage of the diode at various back-gate voltage bias ranging from +20 V to +50V under different temperature is shown in Figure 4-5. It was noticed that the turn on voltage of the diode increased with decreasing back-gate voltage bias and temperature. Indeed, the slope of the curves did not change much with different V_{gs} applied. Given that the Pedot:PSS didn't show a field effect but WS_2 did (as demonstrated in chapter 3), the back gating effect is simply explained as the resistance of WS_2 in our device was changed by the back-gate voltage bias, leading to the variation of the diode current.

4.3.4 Relationships between ideality factor, back-gate voltage bias and temperature

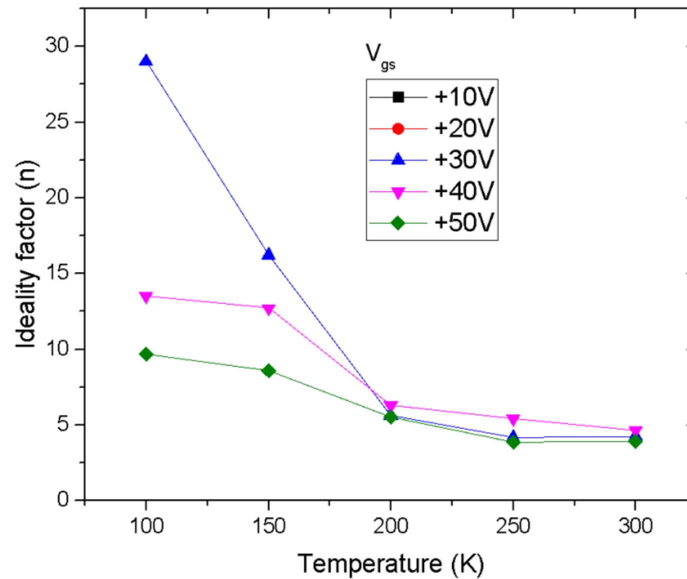


Figure 4-6 The ideality factor with different back-gate voltage bias as a function of temperature.

The ideality factors of the Pedot:PSS/WS_2 diode under various back-gate voltage bias are shown in Figure 4-6.The ideality factors were found to rise when the temperature dropped. Large value of ideality factors was obtained when the temperature was equal to 100K. By the Equation 7,

$$n = \frac{q}{KT} \text{x} \frac{V}{\ln \frac{I}{I_o}} \tag{7}$$

, where q is the charge of electron = $1.6 \text{x} 10^{-19}$C, K is the Boltzmann's constant = $1.38 \text{x} 10^{-23}$ J/K, T is temperature in the unit of Kelvin, V is the voltage across the diode, I is the current through the diode and I_o is the dark saturation current.

The parameters q, K and T is known. From the Figure 4.3, we can obtain the $\ln(I/I_o)$-V curve. In a small forward bias voltage region, ideality factors were calculated and plot in Figure 4-6.

On the basis of this equation, ideality factor is inversely proportional to the junction temperature, and from Figure 4-6, a similar trend is observed. The quite large ideality factor may be due to the high series resistance between the contacts of Pedot:PSS and WS_2 and recombination site.

Chapter 5 Fabrication of Pedot:PSS/SiO_2 /n-2D heterostructures

5.1 I-V measurement of Pedot:PSS/SiO_2/WS_2 at room temperature

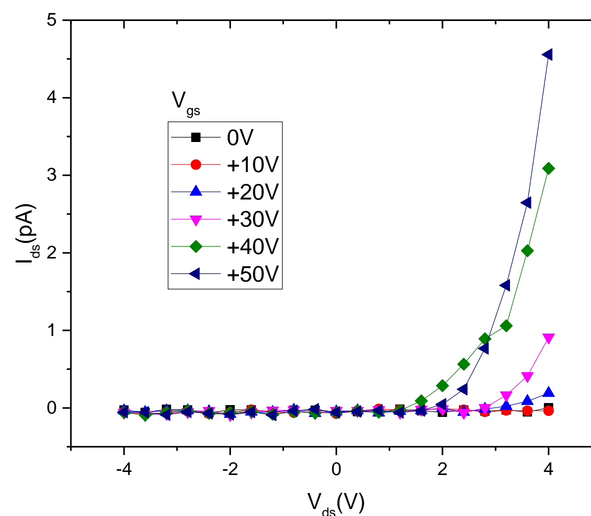


Figure 5-1 Drain current-voltage characteristics of Pedot:PSS/SiO_2/WS_2 at various back-gate voltage in the dark and RT conditions.

Figure 5-1 shows the drain current- voltage characteristics of the Pedot:PSS/SiO_2/WS_2 heterojunction Schottky diode at various gate voltages in dark and RT conditions. Based on the graph, it is observed that the On state current of the dioide decreased a lot which was just one tenth of value of the Pedot:PSS/WS_2 diode under the same drain source and back-gate voltage (Figure 4-2) obtained before.

5.2 I-V measurement of Pedot:PSS/MoS_2 at room temperature

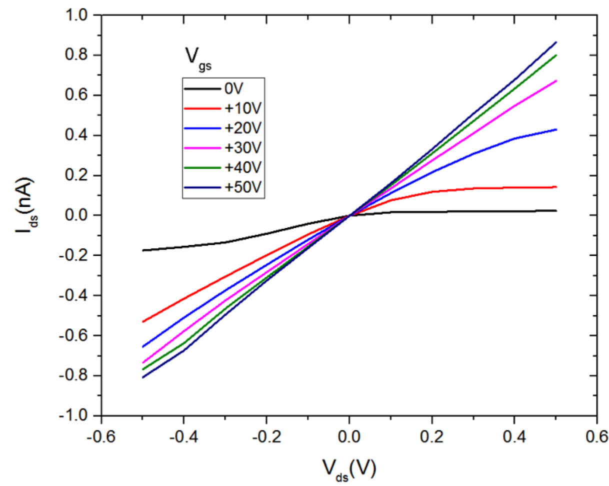


Figure 5-2 Drain current-voltage characteristics of Pedot:PSS/MoS_2 at various back-gate voltages in the dark and RT conditions.

Figure 5-2 shows the I-V characteristics of Pedot:PSS(Al 4083)/MoS_2 at various back gate voltages, and the I-V curves showed that Pedot:PSS(Al 4083)/MoS_2 device did not follow the Schottky diode equation and the curve was symmetric. This might be due to the easy electron injection from Pedot:PSS to MoS_2 at a reverse voltage bias. Therefore, an insulating SiO_2 buffer of thickness about 2 nm in between Pedot:PSS and MoS_2 was introduced in order to eliminate the electron injection.

5.3 Temperature dependence of I-V measurement of Pedot:PSS/SiO_2/MoS_2

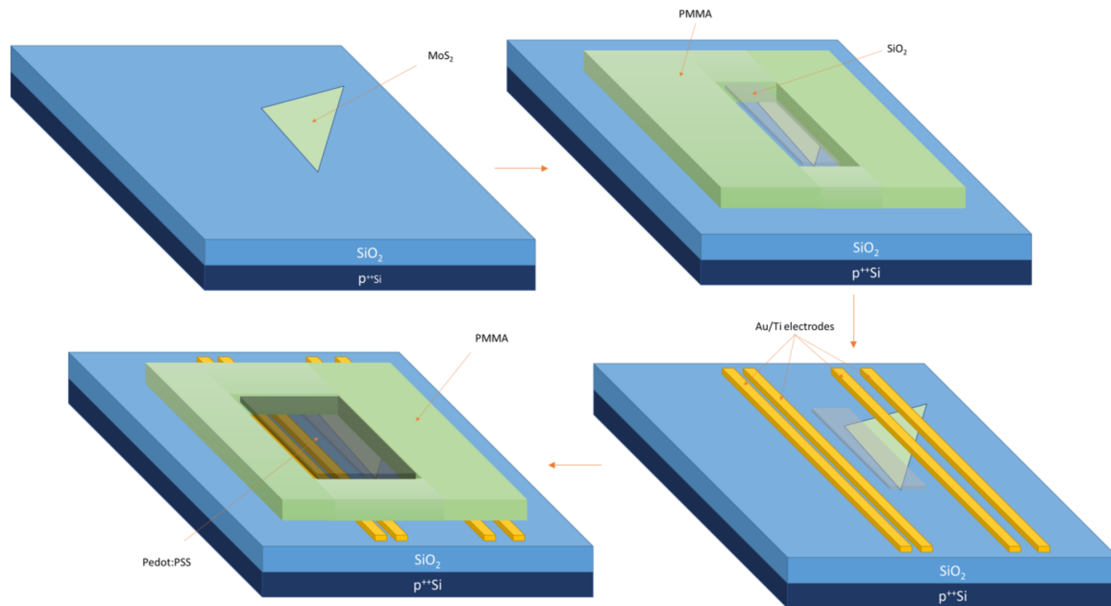
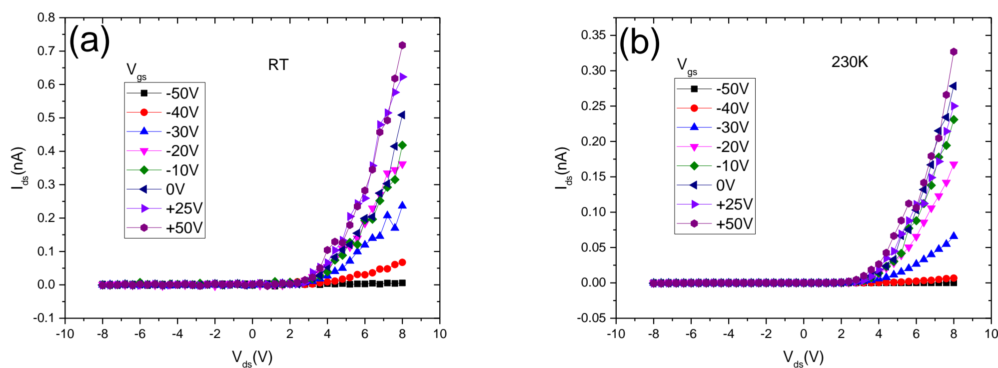


Figure 5-3 Fabrication procedures of Pedot:PSS/SiO_2/MoS_2 junction devices.

The fabrication process of the Pedot:PSS/SiO_2/MoS_2 hetero-junction are summarized as Figure 4-15-3. The fabrication process contains one more step of e-beam lithography compare with the Pedot:PSS/WS_2 hetero-junction to allow the deposition of 2 nm SiO_2 on MoS_2.



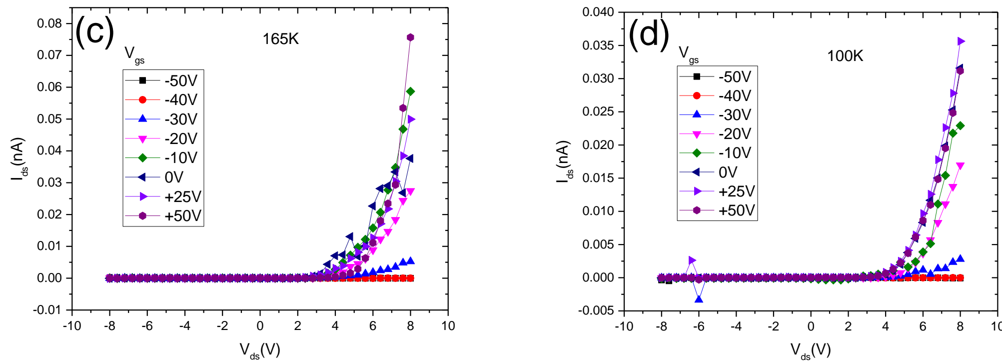


Figure 5-4 Drain current-voltage characteristics of Pedot:PSS/SiO_2/MoS_2 at various back-gate voltage bias at (a) RT, (b) 230K, (c) 165K and (d) 100K, respectively in the dark and RT conditions.

After inserting the SiO_2 insulating layer in between the Pedot:PSS and MoS_2, diode exhibits an improved rectify effect similar to a Schottky diode.

Figure 5-4 (a-d) shows the current-voltage ($I_{ds} – V_{ds}$) curves of Pedot:PSS/SiO_2/MoS_2 as a function of the gate voltage (V_{gs}) measured at 100, 165, 230 and 300K, respectively. At all temperatures, the device showed a diode-like behavior compared to the symmetric curve without the SiO_2 layer. In addition, atomically thin MoS_2 also allowed the device to be strongly tuned by V_{gs}.

5.4 Comparison of the performance of Pedot:PSS/WS_2 and Pedot:PSS/SiO_2/WS_2 at room temperature

Table 3 ON state and OFF state current of Pedot:PSS/WS_2 and Pedot:PSS/SiO_2/WS_2 with ±4 V drain-source voltage bias

Pedot:PSS/WS_2			Pedot:PSS/SiO_2/WS_2		
V_{gs}	I_{on} (A)	I_{off} (A)	V_{gs}	I_{on} (A)	I_{off} (A)
0	1.10×10^{-13}	3.00×10^{-14}	0	1.96×10^{-15}	2.64×10^{-14}
10	2.17×10^{-11}	6.42×10^{-14}	10	3.64×10^{-14}	4.93×10^{-14}
20	1.09×10^{-10}	8.09×10^{-14}	20	1.90×10^{-13}	3.42×10^{-14}
30	1.80×10^{-10}	1.25×10^{-13}	30	9.12×10^{-13}	5.88×10^{-14}
40	2.24×10^{-10}	6.82×10^{-13}	40	3.09×10^{-12}	5.98×10^{-14}
50	2.83×10^{-10}	3.08×10^{-12}	50	4.56×10^{-12}	5.55×10^{-14}

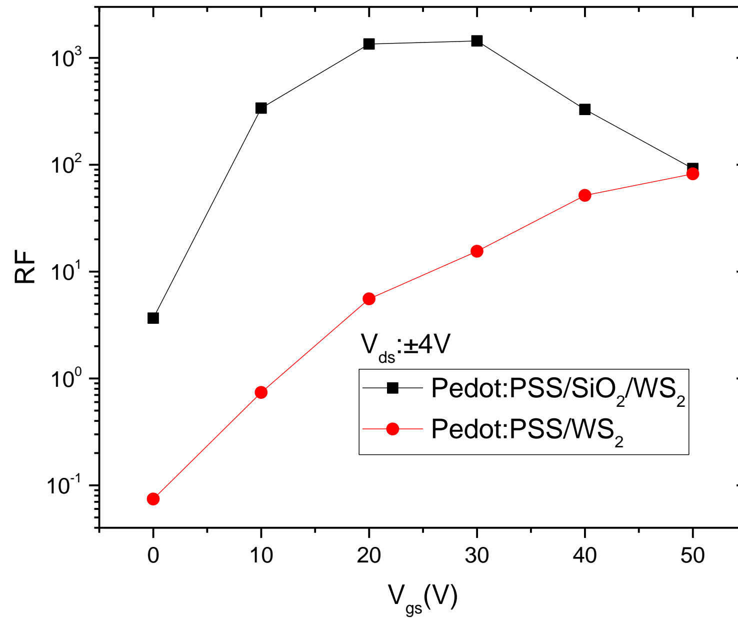


Figure 5-5 The RF ratio of Pedot:PSS/WS_2 and Pedot:PSS/SiO_2/WS_2 with various back-gate voltage bias.

The rectification ratio curves of Pedot:PSS/WS_2 and Pedot:PSS/SiO_2/WS_2 devices are compared in Figure 5-5. Two measurements of the two devices were measured at $\pm$4 V drain-source voltages at various back-gate voltages from 0 V to +50 V. Two RF curves showed a different trend that the ON/OFF ratio of Pedot:PSS/WS_2 device increased with back-gate voltage from 0 V to +30 V but decreased from +30 V to +50 V, and the ON/OFF ratio of Pedot:PSS /SiO_2/WS_2 device kept increasing with back-gate voltage bias from 0 V to +50 V. When the back-gate voltage bias increased from 0 V to +30 V, the Off state current magnitude of Pedot:PSS/WS_2 increased insignificantly at around 10^{-14} A and 10^{-13} A and the ON state current magnitude increased slightly from around 10^{-13} A to 10^{-10} A. However, when the back-gate voltage bias increases from +30 V to +50 V, the OFF state current magnitude increased from 1.25x10^{-13} A to 3.08x10^{-12} A,

but the ON state kept around 10^{-10} A. On the other hand, the Off state current magnitude of Pedot:PSS/SiO_2/WS_2 device remained the value at around 10^{-14} A when the back-gate voltage bias increased from 0 V to +50 V, and the ON state current at V_{gs} = +50 V increased more than 100 times than 0 V. As a result, the ON/OFF ratio of Pedot:PSS/WS_2 device increased with back-gate voltage bias increasing from +10 V to 30 V but decreased with back-gate voltage bias increasing from +30 V to +50 V, and the ON/OFF ratio of Pedot:PSS/SiO_2/WS_2 device kept increasing with back-gate voltage bias from 0 V to +50 V, as shown in Figure 5-5.

By comparing the maximum ON/OFF ratio of the two devices, Pedot:PSS/WS_2 showed a better rectification performance than Pedot:PSS/SiO_2/WS_2 due to a much lower ON state current of Pedot:PSS/SiO_2/WS_2 device. The lower ON state current is probably due to the inserted SiO_2 insulating layer in between the Pedot:PSS and WS_2. Before inserting the SiO_2 insulating layer, the range of the ON state current with back-gate voltage bias from +10 V to +50 V was 2.17×10^{-11} A to 2.83×10^{-10} A. After inserting the SiO_2 insulating layer, the range of the ON state current with the same range of back-gate voltage bias decreased to the range of 3.64×10^{-14} A to 4.56×10^{-12} A. At their maximum ON/OFF ratio, both devices had a very low dark current with the reverse voltage bias which was 1.25×10^{-13} A and 5.55×10^{-14} A for Pedot:PSS/WS_2 and Pedot:PSS/SiO_2/WS_2 respectively. The two maximum measured rectification ratios were 10^3 and 10^2 respectively. It is worth to notice that the device based on Pedot:PSS/SiO_2/WS_2 gave an ultra-low dark current of 4.6 pA even under 4V forward and +50V back-gate voltage bias which may be advantageous for high performance optical sensing.

5.5 Comparison of the performance of Pedot:PSS/MoS_2 and Pedot:PSS/SiO2/MoS_2 at room temperature

Table 4 ON state and OFF state current of Pedot:PSS/SiO_2/MoS_2 and Pedot:PSS/MoS_2 with ±8 V and ±0.5 V drain-source voltage bias

Pedot:PSS(Al 4083)/SiO_2/MoS_2			Pedot:PSS(Al 4083)/MoS_2		
V_{gs}	I_{on} (A)	I_{off} (A)	V_{gs}	I_{on} (A)	I_{off} (A)
-50	5.66×10^{-12}	2.19×10^{-12}	0	2.44×10^{-11}	1.74×10^{-10}
-40	6.74×10^{-11}	3.93×10^{-13}	10	1.43×10^{-10}	5.29×10^{-10}
-30	2.36×10^{-10}	3.56×10^{-13}	20	4.30×10^{-10}	6.54×10^{-10}
-20	3.62×10^{-10}	8.49×10^{-13}	30	6.73×10^{-10}	7.34×10^{-10}
-10	4.18×10^{-10}	6.37×10^{-13}	40	8.01×10^{-10}	7.67×10^{-10}
0	5.09×10^{-10}	4.98×10^{-13}	50	8.66×10^{-10}	8.06×10^{-10}
25	6.23×10^{-10}	9.79×10^{-13}			
50	7.17×10^{-10}	1.31×10^{-12}			

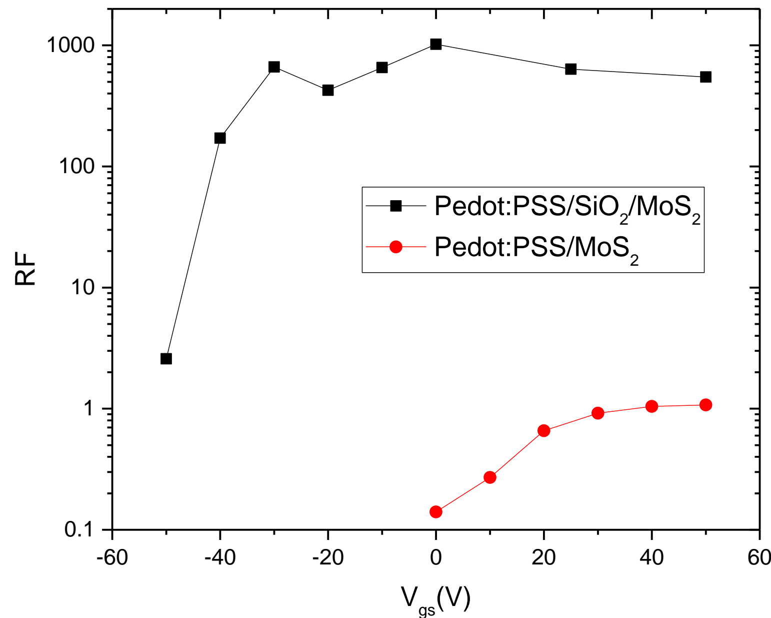


Figure 5-6 The RF ratio of Pedot:PSS/MoS_2 and Pedot:PSS/SiO_2/MoS_2 with various back-gate voltage bias.

The rectification ratio curves of Pedot:PSS/MoS_2 and Pedot:PSS/SiO_2/MoS_2 devices are compared in Figure 5-6. Both devices were measured at their optimized drain-source voltage at various back-gate voltages. However, the two RF curves showed different ON/OFF ratio levels. The ON/OFF ratio of Pedot:PSS/MoS_2 device remained at a value equal or below 1 whatever the back-gate voltage was increased from 0 V to + 50V. On the other hand, the ON/OFF ratio of Pedot:PSS /SiO_2/MoS_2 device kept around $5x10^2$ with back-gate voltage bias from -30 V to +50 V.

For Pedot:PSS/MoS_2 heterojunction without SiO_2 insulating buffer layer, the reverse dark current was around 0.2 nA at just -0.5 V reverse drain-source voltage bias. Indeed, the rectification ratio was about 0.1, no matter whenever back-gate voltage bias was applied or not. This kind of heterojunction with a poor rectifying property is probably

due to an unacceptable leakage current which is not suitable for practical application. Fortunately, an effective way to decrease the OFF state current for the Pedot:PSS/MoS_2 heterojunctions is by introducing a SiO_2 buffer layer. It is observed that the value of OFF state current decreased from 0.8 nA to 1.3 pA even under +50 V back-gate voltage bias. This improvement indicated that the SiO_2 buffer layer could be a good insulator and effectively prevent the electron injection from Pedot:PSS to MoS_2 at a reverse voltage bias.

5.6 Comparison of the performance of Pedot:PSS/SiO_2/MoS_2 and Pedot:PSS/SiO_2/WS_2 at room temperature

Table 5 ON state and OFF state current of Pedot:PSS/SiO_2/MoS_2 and Pedot:PSS/SiO_2/WS_2 with ±8 V drain-source voltage bias

Pedot:PSS(Al 4083)/SiO_2/MoS_2			Pedot:PSS(Al 4083)/SiO_2/WS_2		
V_{gs}	I_{on} (A)	I_{off} (A)	V_{gs}	I_{on} (A)	I_{off} (A)
-50	5.66 x10^{-12}	2.19 x10^{-12}	0	6.32 x10^{-14}	4.06 x10^{-15}
-40	6.74 x10^{-11}	3.93 x10^{-13}	10	5.62 x10^{-13}	1.42 x10^{-14}
-30	2.36 x10^{-10}	3.56 x10^{-13}	20	1.02 x10^{-11}	5.23 x10^{-14}
-20	3.62 x10^{-10}	8.49 x10^{-13}	30	6.82 x10^{-11}	5.46 x10^{-14}
-10	4.18 x10^{-10}	6.37 x10^{-13}	40	1.30 x10^{-10}	1.32 x10^{-13}
0	5.09 x10^{-10}	4.98 x10^{-13}	50	1.90 x10^{-10}	2.20 x10^{-13}
25	6.23 x10^{-10}	9.79 x10^{-13}			
50	7.17 x10^{-10}	1.31 x10^{-12}			

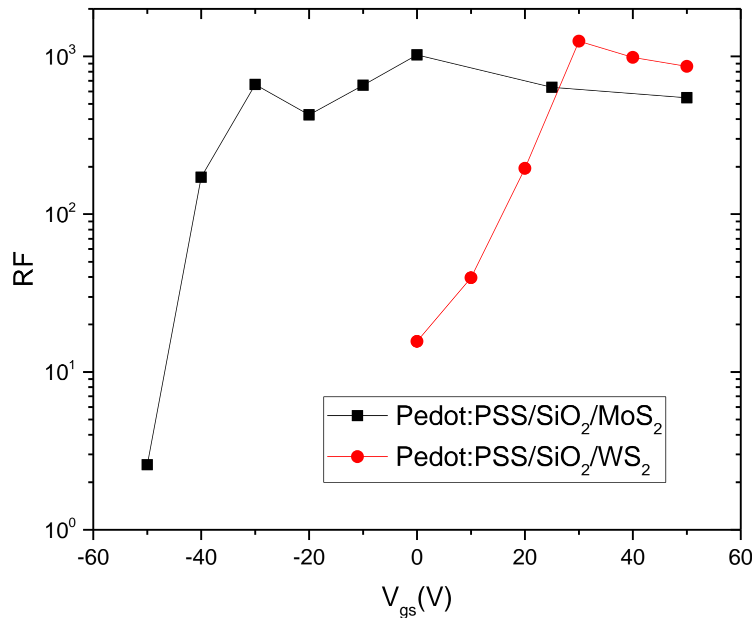


Figure 5-7 The RF ratio of Pedot:PSS/SiO_2/MoS_2 and Pedot:PSS/SiO_2/WS_2 with various back-gate voltage bias.

The rectification ratio curves of Pedot:PSS/SiO_2/MoS_2 and Pedot:PSS/SiO_2/WS_2 devices are compared in Figure 5-7. Both devices were measured at their optimized drain-source voltage at various back-gate voltages. On the basis of our results, it was found that the ON/OFF ratio of Pedot:PSS/SiO_2/MoS_2 device remained around ~$5x10^2$ when the back-gate voltage was in the range of +30 V to +50 V. For Pedot:PSS/SiO_2/WS_2, the ON/OFF ratio of the device increased with back-gate voltage from 0 V to +30 V but decreased a little from +30 V to +50 V. When the back-gate voltage bias increased from 0 V to +30 V, the Off state current magnitude increased insignificantly at around 10^{-14} A and the ON state current magnitude increased a lot from $6.32x10^{-14}$ A to $6.82x10^{-11}$ A. When the back-gate voltage bias increased from +30 V to +50 V, the OFF state current magnitude increased from $5.46x10^{-14}$ A to $2.20x10^{-13}$ A, and the ON state

current increased from $6.82x10^{-11}$ A to $1.90x10^{-10}$ A. As a result, the ON/OFF ratio of Pedot:PSS/SiO_2/WS_2 device increased with back-gate voltage bias increased from +10 V to 30 V but decreased a little with back-gate voltage bias increased from +30 V to +50 V. Pedot:PSS/SiO2/WS_2 still performs badly in the -ve voltage region is simply due to the low conductivity of WS_2 in the -ve voltage region.

By comparing the maximum ON/OFF ratio of the two devices, Pedot:PSS/SiO_2/WS_2 exhibited a little higher ON/OFF ratio than Pedot:PSS/SiO_2/MoS_2 but it is worth to notice that Pedot:PSS/SiO_2/MoS_2 device can reach to its maximum ON/OFF ratio without applying back-gate voltage which consumes less energy consumption under the operation.

By comparing the forward and reverse dark current of the two devices at their maximum ON/OFF ratio operating condition, the ON state current of Pedot:PSS/SiO_2/MoS_2 without back-gate voltage bias was $5.09x10^{-10}$ A and the ON state current of Pedot:PSS/SiO_2/WS_2 with +30 V back-gate voltage bias was $6.82x10^{-11}$A. On the other hand, the reverse dark current of Pedot:PSS/SiO_2/MoS_2 without voltage bias was $4.98x10^{-13}$ A and the OFF state current of Pedot:PSS/SiO_2/WS_2 with +30 V back-gate voltage bias was $5.546x10^{-14}$A. It is concluded that the ON/OFF state current of Pedot:PSS/SiO_2/MoS_2 at their maximum ON/OFF ratio operating condition were also 10 times higher than that of Pedot:PSS/SiO_2/WS_2.

Chapter 6 Fabrication of Pedot:PSS/SiO_2/ MoS_2 heterostructures with different conductivity of Pedot:PSS

6.1 Comparison performance of Pedot:PSS/SiO_2/MoS_2 heterostructures with different Pedot:PSS compositions of different conductivities

6.1.1 The I-V curves of different conductivities of Pedot:PSS at room temperature

In this part, the effects of the conductivity of Pedot:PSS on the electrical properties of Pedot:PSS/SiO_2/MoS_2 heterostructures were investigated. The performances of 4 Pedot:PSS types with volume ratio of (100% Al4083), (75% Al4083+25% PH500), (50%Al4083+50%PH500) and (100% PH500) were compared. General speaking, Al4083 has a lower conductivity than that of PH500 as shown in chapter 3. It was observed that the device employing (75%Al4083+25% PH500), (50% Al4083+50% PH500) and (100% PH500) both exhibited larger ON/OFF state current at Vds =±8 V compared with the device employing Pedot:PPS(Al 4083).

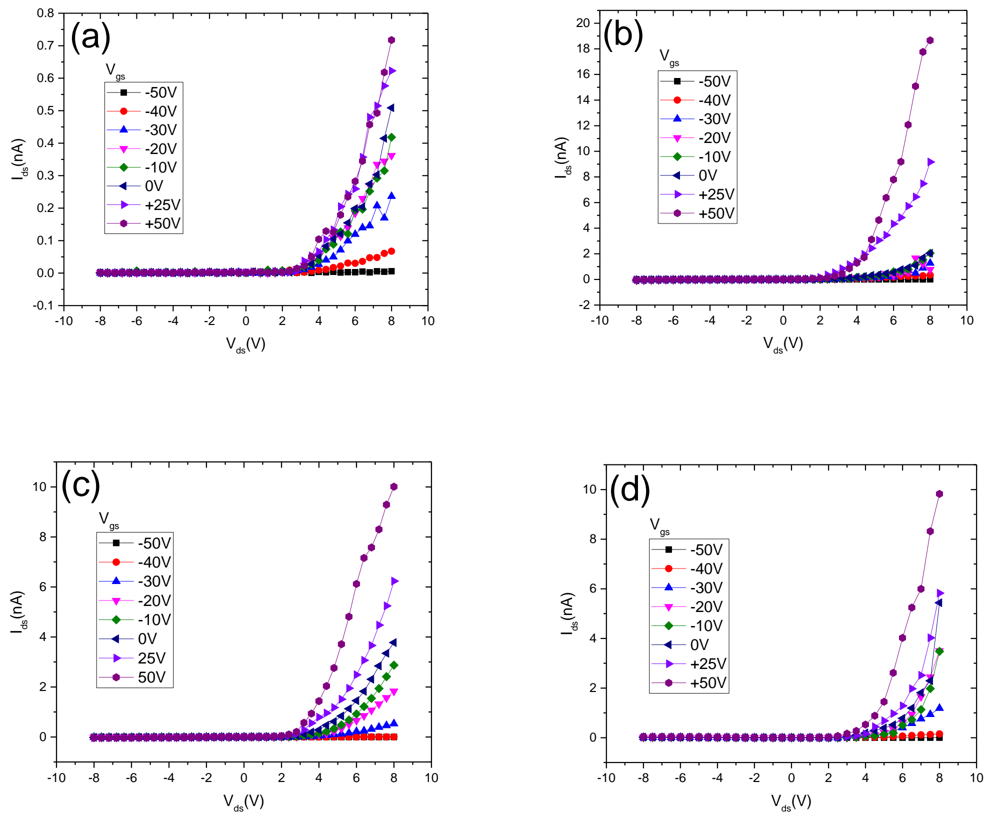


Figure 6-1 Drain current-voltage characteristics at various back-gate voltage with (a) Pedot:PSS(Al4083), (b) Pedot:PSS(75% Al4083+25% PH500), (c) Pedot:PSS(50% Al4083+50% PH500) and (d) Pedot:PSS(PH500)

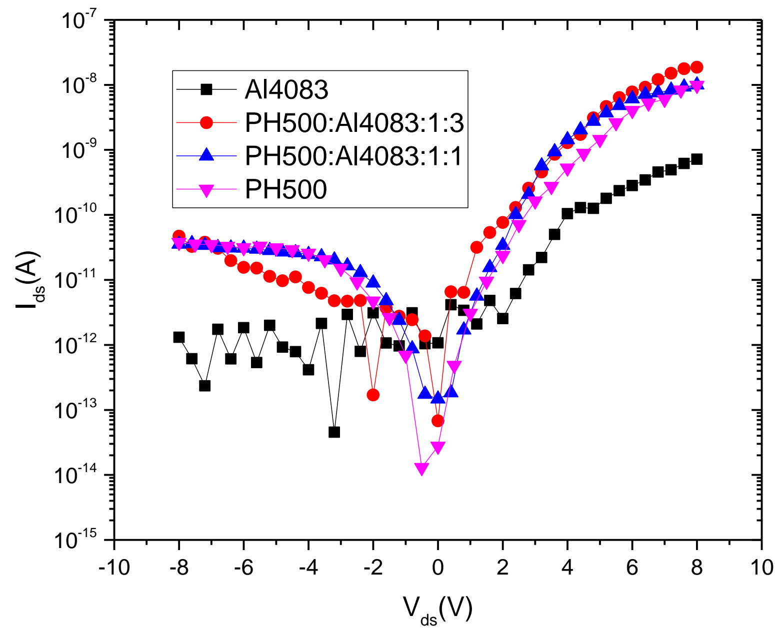


Figure 6-2 The drain current-voltage characteristics with different conductivities at V_{gs} = +50 V in semilogarithmic scale

6.1.2 I_{on} and I_{off} with different conductivities of Pedot:PSS

Table 6 ON state and OFF state current of Pedot:PSS/SiO_2/MoS_2 with different conductivities of Pedot:PSS at +8/-8 V drain-source voltage bias

I_{on}
I_{on} I_{ds}(A) 10^{-8} 10^{-9} 10^{-10} V_{gs}: -30V, -20V, -10V, 0V, 25V, 50V Pedot:PSS(Al 4083) · Pedot:PSS(Al 40 83+PH 500)(3:1) · Pedot:PSS(Al 40 83+PH 500)(1:1) · Pedot:PSS(PH 500)
I_{off}
I_{off} I_{ds}(A) 10^{-11} 10^{-12} V_{gs}: -30V, -20V, -10V, 0V, 25V, 50V Pedot:PSS(Al 4083) · Pedot:PSS(Al 40 83+PH 500)(3:1) · Pedot:PSS(Al 40 83+PH 500)(1:1) · Pedot:PSS(PH 500)

The ON/OFF state current of the 4 devices with back-gate voltage bias from -30 V to 50 V are summarized in Table 6. In the aspect of each device, it is found that the ON/OFF state current of each device generally increased as the back-gate voltage bias increased from -30 V to 50 V. Based on our measurements of both MoS_2 and Pedot:PSS FETs, we have proved that the conductivity of MoS_2 increased exponentially when positive back-gate voltage bias increased and the conductivity of the Pedot:PSS remained the same magnitude whenever different back-gate voltages were applied. Due to the forward current solely depends on the conductivity of p-type and n-type semiconductors, increasing the back-gate voltage bias from -30 V to 50 V keeps the conductivity of Pedot:PSS to be constant and increases the conductivity of MoS_2 exponentially, this will therefore increase the ON state current of each device.

By comparing the performance of the 4 devices with different Pedot:PSS compositions, it is found that the device of volume ratio of (100% Al4083) exhibited a quite different performance with (75% Al4083+25% PH500), (50%Al4083+50%PH500) and (100% PH500). The ON state current of Pedot:PSS(100% Al4083) was in the range of 10^{-10} A with the back-gate voltage bias increased from -30 V to +50 V. However, the ON state current of other 3 devices: (75% Al4083+25% PH500), (50%Al4083+50%PH500), and (100% PH500) both were in the range of 10^{-9} A to 10^{-8} A with the back-gate voltage bias increased from -30 V to +50 V. This situation also happened for the OFF state current. For example, the OFF state current of Pedot:PSS(100% Al 4083) was in the range of 10^{-13}A to 10^{-12} A but the OFF state of other three devices were in the range of 10^{-11} A.

By introducing Pedot:PSS(PH 500) to mixed with Pedot:PSS (Al 4083), we have

fabricated 4 different Pedot:PSS devices (4 different levels of conductivity). We expected that the four devices will exhibit their own current level including ON state and OFF state current. Unfortunately, on the basis of our result, we did not see any big difference between the three devices, namely, (75% Al4083+25% PH500), (50%Al4083+50%PH500) and (100% PH500) when we compared their current levels. This may be due to the fact that Pedot:PSS(PH 500) dominates in the charge transport of the p-n junctions. Although there is only 25% of Pedot:PSS (PH500), it is high enough to reach the ON state current of 10^{-9} A to 10^{-8} A and OFF state current of 10^{-11} A.

6.1.3 RF ratio with different conductivities of Pedot:PSS

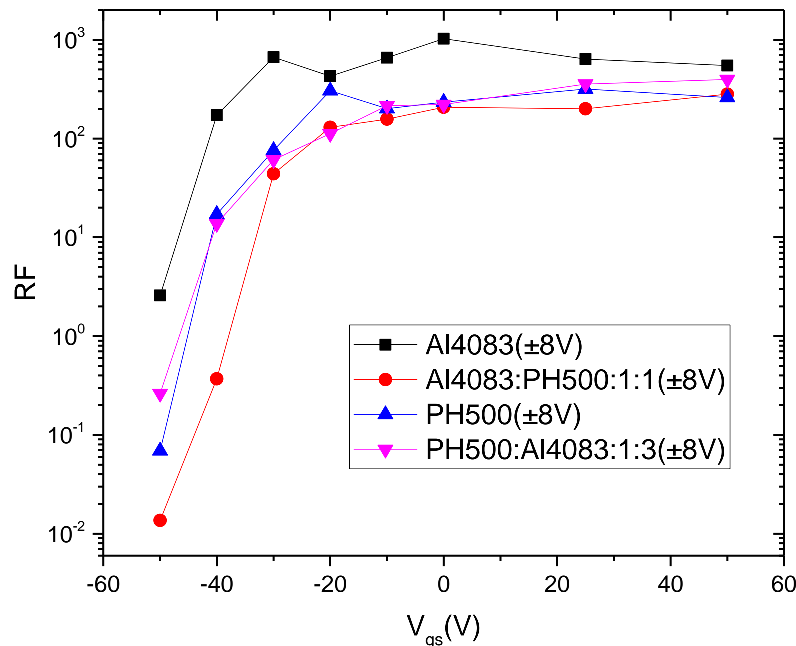


Figure 6-3 The RF ratio at various back-gate voltage bias with different conductivities of Pedot:PSS

The RF ratio as a function of the back-gate voltage bias curves for the four devices are

shown in Figure 6-3. Since the domination of Pedot:PSS(PH 500) in the charge transport of the p-n junctions, the other 3 Pedot:PSS devices (75% Al4083+25% PH500, 50%Al4083+50%PH500, and 100% PH500) exhibited similar ON/OFF ratio trends. Although the device with Pedot:PSS (Al 4083) had the lowest ON and OFF state current, it exhibited a slightly higher ON/OFF ratio as compared to the others, which was about 10^3 operating at +8/-8 drain-source voltage bias.

Chapter 7 **Conclusion and Future work**

In conclusion, this thesis aims to study the electrical properties of 2D vdW heterostructures. Several materials, Pedot:PSS, SiO_2, MoS_2 and WS_2 were combined to fabricate the 2D vdW heterojunction devices.

On the basis of our results, we found that the Pedot:PSS/WS_2 device showed a large rectification ratio up to 10^3 at room temperature with 30 V back-gate voltage bias. Under the temperature range of 150 K to room temperature, the device still worked well, and the rectification ratio increased from 10^3 to 10^4. This device can be used in a logic circuit.

On the other hand, it was observed that the SiO_2 buffer layer could be a good insulator and effectively prevent the electron injection from p-organic to n-2D at a reverse bias of up to -4 V. Also, the device based on Pedot:PSS/SiO_2/WS_2 gave an ultra-low dark current of 4.6 pA even under 4 V forward and +50 V back-gate voltage bias which may be advantageous for high performance optical sensing.

By mixing Pedot:PSS(PH 500) with Pedot:PSS (Al 4083), we have fabricated 4 devices with different conductivities of Pedot:PSS. However, it seems that Pedot:PSS(PH 500) dominated in the charge transport of the p-n junctions. As a result, we did not see any trend when we compared their current levels. Although there was only 25% of Pedot:PSS (PH500), it was enough to obtain the ON state current up to 10^{-8} A and OFF state current of 10^{-11} A.

Based on these results, several suggestions are made. Firstly, the device based on Pedot:PSS/SiO_2/WS_2 showed an advantageous for high performance optical sensing.

Therefore, we may study the light power, back-gate voltage bias, and temperature-tunable photovoltaic effect of the vdW heterojunction in the future.

Secondly, no study has demonstrated a doped-2D material to combine with p-type semiconductors to form a 2D vdW heterostructure. Therefore, it is worth to investigate the doping effect of n-type 2D in vdW heterostructures in the future also.

Chapter 8 **Appendix**

Table 7 Summary of all device performances (ON/OFF ratio) obtained in this thesis

Devices	Performance in room temperature (On/Off ratio)
Pedot:PSS(Al4083)/WS_2(Vds:±4V)	~10^3
Pedot:PSS(Al4083)/MoS_2	~1
Pedot:PSS(Al4083)/SiO_2/MoS_2(Vds:±8V)	~10^3
Pedot:PSS(Al4083)/SiO_2/WS_2(Vds:±8V)	~10^3
Pedot:PSS(Al4083:PH500:3:1)/SiO_2/MoS_2 (Vds:±8V)	~5x10^2
Pedot:PSS(Al4083:PH500:1:1)/SiO_2/MoS_2 (Vds:±8V)	~5x10^2
Pedot:PSS(PH500)/SiO_2/MoS_2(Vds:±8V)	~5x10^2

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