ELECTROCHEMICAL REPLICATION AND TRANSFER: PRINCIPLE, FABRICATION, AND APPLICATIONS

LU XI

PhD

The Hong Kong Polytechnic University

2020

The Hong Kong Polytechnic University

Institute of Textiles and Clothing

Electrochemical Replication and Transfer: Principle, Fabrication, and Applications

LU Xi

A thesis submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy

August 2019

Certificate of Originality

I hereby declare that this thesis is my own work and that, to the best of my knowledge and belief, it reproduces no material previously published or written, nor material that has been accepted for the award of any other degree or diploma, except where due acknowledgement has been made in the text.

_____(Signed)

LU Xi

August 2019

Abstract

Patterning technique can generate arbitrary micro- and nanopatterns on substrates of choice, which is a fundamental step in a wide range of applications. A wide variety of patterning techniques are used nowadays, such as photolithography, electron beam lithography (EBL), nanoimprint lithography (NIL), inkjet printing, screen printing, etc. High resolution, high throughput, and low cost are three basic requirements for an advanced patterning technique. Photolithography, EBL, and NIL can fabricate high-resolution patterns with nanoscales. However, these high-resolution patterning techniques suffer from limitations of either expensive equipment or low throughput. Inkjet and screen printings can achieve high throughput with relatively low cost. But their resolutions are seriously poor at micrometer scale. A big challenge for existing patterning techniques is the critical tradeoff among the resolution, throughput, and cost. Therefore, it is still of great significance to develop an alternative patterning technique that can achieve high resolution, high throughput, and low cost simultaneously. To address this challenge, an alternative patterning technique, termed electrochemical replication and transfer (ERT), is developed in this thesis.

Firstly, ERT process only consists of two steps: 1) electrochemical replication of target materials on pre-patterned template and 2) transfer of replicated pattern onto target substrate. The parallel patterning on large-area substrate allows ERT to fabricate multi-scale patterns with resolutions spanning from sub-100 nm to many cm, which overcomes the tradeoff between resolution and throughput. On the other hand, the cost of ERT is ultralow own to its all-solution process based on ultralow-cost equipment and the nature of additive manufacturing. Furthermore, ERT is

suitable for fabricating various materials including metals, semiconductors, metal oxides, and polymers with arbitrary geometric shapes on various flexible substrates including plastics, papers, and textiles.

Secondly, the mechanism of ERT process was analyzed. In the step of electrochemical replication, two necessary conditions are the rational structure of Au-patterned template and optimization of current density, which both control the electrodeposited materials to be confined on the region of Au patterns. The success of transfer step is attributed to the surface modification of self-assembled monolayers (SAMs) on template and the use of photo-curable polymer as binder. The SAMs, pre-modified on Au surface, act as the anti-adhesive layers, which not only facilitate the peeling off of target materials, but also improve the reusability of template. The use of photo-curable adhesive as binder could make the transfer easy through its strong interaction with target materials.

Thirdly, the applications of ERT technique were demonstrated. ERT technique was used to fabricate three types of typical electrodes (flexible transparent electrodes (FTEs), source/drain (S/D) electrodes, and interdigital electrodes (IDEs)), which were further integrated in the electronic devices. The FTEs show excellent electrical and optical properties, mechanical flexibility, and environmental stability, which were further used in optoelectronic devices, i.e., flexible transparent electrodes, touch screen panels, and organic light-emitting diodes. Furthermore, ERT was used to fabricate S/D electrodes and IDEs, which were successfully integrated in organic electrochemical transistors (OECTs) and micro-supercapacitors (MSCs), respectively.

In conclusion, as an alternative patterning technique, ERT combines the advantages of high resolution, high throughput, and low cost. It can fabricate arbitrary geometric patterns with various materials on various flexible/wearable substrates. The mechanism of ERT process are relevant to the template structure, electrodeposition parameter, surface modification, and photo-curable binder. The applications of ERT for demonstration include flexible transparent electrodes, source/drain electrodes, and interdigital electrodes and their integrations in the electronic devices.

Publications Arising from the Thesis

Journal Publications

1. Wang, D.; Zhang, Y.; **Lu, X.**; Ma, Z.; Xie, C.; Zheng, Z., Chemical formation of soft metal electrodes for flexible and wearable electronics. *Chem. Soc. Rev.* 2018, 47 (12), 4611-4641.
2. Zheng, Z.; Chen, L.; Li, P.; **Lu, X.**; Wang, S., Binary Polymer Brush Patterns from Facile Initiator-Stickiness for Cell Culturing. *Faraday Discuss.* 2019, 219, 189-202.
3. Zhang, Y.; Ng, S.-W.; **Lu, X.**; Zheng, Z., Solution-Processed Transparent Electrodes for Emerging Thin-film Solar Cells. *Chem. Rev.* 2020, 120 (4), 2049-2122.

Papers in Preparation

1. **Lu, X.**; Wang, H.; Wang, W.; Wang, D.; Chang, J.; Ng, S.-W.; Rong, M.; Li, P.; Huang, Q.; Zheng, Z., Electrochemical Replication and Transfer. (to be submitted)
2. **Lu, X.**; Wang, D.; Chang, J.; Zhang, Y.; Chen, D.; Chen, L.; Ng, S.-W.; Li, P.; Wu, Z.; Ma, Z.; Zheng, Z., Resist-Free Electrochemical Replication and Transfer (ERT) Strategy for High-Performance Flexible and Smooth Metal Meshes. (to be submitted)
3. **Lu, X.**; Zheng, Z., Metal-based flexible transparent electrodes: challenges and recent advances. (to be submitted to *Adv. Electron. Mater.*)

Patent

Zheng, Z.; **Lu, X.,** Low-Cost and Facile Fabrication of Embedded Metal Mesh-based Flexible Transparent Electrodes. 2018. *China Patent* (application number: 201910072960.1)

Conference Presentations

Oral presentations

1. **Lu, X.,** Low-Cost and Facile Fabrication for High-Performance Metal Mesh-Based Flexible Transparent Electrodes. *E-MRS 2019 Spring Meeting*, 27 - 31 May 2019, Nice, France
2. **Lu, X.,** Electrochemical Replication and Transfer (ERT): A Low-Cost and High-Resolution Patterning Technique for Flexible Electronics. *10th International Conference on Materials for Advanced Technologies (ICMAT 2019)*, 23 - 28 June 2019, Singapore

Acknowledgements

First of all, I would like to express my sincere gratitude to my supervisor Prof. Zheng Zijian for offering me the chance for PhD study in the research group and the long-term academic guidance in the past four years. His strong responsibility, rigorous attitude and critical analysis on scientific research, are impressive and always motivating me. The research skills for academic presentation, literature reading, and paper writing which he emphasizes are practically helpful to my PhD study. What I learned from my supervisor have brought me great progress in the past four years and will be powerful tools in my future research.

I would also like to thank all the members in Zheng's group for their help and company during my PhD study, especially Prof. Wang Dongrui, Dr. Chang Jian, Dr. Xie Zhuang, Dr. Niu Liyong, Dr. Chen Lina, Dr. Ng Sze-wing, Dr. Zhang Yaokang, Dr. Huang Qiyao, Dr. Yu You, Dr. Yang Yu, Dr. Guo Ruisheng, Dr. Chen Dongdong, Dr. Wu Zhongwei, Dr. Liu Guoqiang, Dr. Gan Qi, Dr. Wang Wenshuo, Dr. Zhang Yiqi, Dr. Hu Hong, Dr. Gao Yuan, Dr. Lin Zhiqiang, Dr. Li Dongdong, Mr. Li Peng, Mr. Shang Jian, Mr. Xie Chuan, Ms. Yan Ka Chi, Ms. Wang Younseon, Ms. Wang Huixin, Ms. Zhuang Qiuna, Ms. Rong Mingming, and Ms. Guo Qianyi. In the meantime, I would like to show my acknowledgement to Prof. Lee Chun-sing's group in City University of Hong Kong, Dr. Wing-Cheung Roy Law's group in The Hong Kong Polytechnic University, Prof. Zhou Xuechang's group in Shenzhen University, and Prof. Deng Yonghong's group in Southern University of Science and Technology for the cooperative experiments to support my research.

My thanks are also expressed to the scientific officers and technical staff at The Hong Kong Polytechnic University, especially Ms. Lemona Kong, Ms. Mow-Nin Sun, Mr. Patrick Pang in Institute of Textile and Clothing, and Ms. Joyce Ho, Dr. Pai Wong, Dr. Wei Lu in University Research Facility in Materials Characterization and Device Fabrication, for their patient guidance and help without any discrimination during my PhD study. I also gratefully acknowledge the financial support from the Hong Kong Polytechnic University (RUAV, ZVGH, K-ZR24).

Finally, I would like to thank my family members for their understanding and support on my PhD study.

Table of Contents

List of Figures

List of Tables

Chapter 1: Introduction

1.1 Background and Challenges

Patterning technique can generate arbitrary patterns of materials with feature sizes ranging from a few nanometers up to tens of millimeters on substrates of choice. It is the fundamental technique for a wide range of applications in the field of electronics, photonics, biological research, medical study, etc.[1-6] In the history of science and technology, people have developed a wide variety of patterning techniques to meet different requirements. Among them, some patterning techniques have been mature and widely used in the academic research and industrial application, such as photolithography, electron beam lithography (EBL), nanoimprint lithography (NIL), inkjet printing, screen printing, etc.

To meet the requirement of high-volume manufacturing (HVM) in the industry, high resolution, high throughput, and low cost are three basic factors which are required for a perfect patterning technique. Photolithography have been deeply studied and developed in the past decades because of its high resolution and high integration in the semiconductor industry.[7-8] However, the costs of equipment and fabrication process for nanoscale patterns in photolithography are generally ultrahigh. The high cost is acceptable for chip fabrication, while limited in other kinds of applications where low cost and high resolution are both necessary. The resolutions of electron beam lithography and nanoimprint lithography also can reach nanoscales.[9-10] Similarly, they also face the challenge of poor throughput

and/or high cost. The conventional printings, such as inkjet printing and screen printing, can meet the requirements of low cost and high throughput simultaneously. However, they are limited seriously to their poor resolution at tens of micrometers.[11]

Based on the review and summary, a big challenge for existing patterning techniques is a critical tradeoff among their resolution, throughput, and cost. These three factors are dependent to each other. Therefore, it is still of great significance to develop an alternative patterning technique that can balance high resolution, high throughput, and low cost. To address this challenge, an alternative patterning technique, termed electrochemical replication and transfer (ERT), is developed in this research project. The additive and parallel patterning attributes of ERT allow to fabricate multi-scale patterns with resolutions spanning from sub-100 nanometer to many centimeters simultaneously, which overcomes the tradeoff between resolution and throughput of conventional patterning techniques. On the other hand, the cost of ERT technique is ultralow owning to its all-solution process in ambient condition and the nature of additive manufacturing. Furthermore, ERT is suitable for fabricating a wide variety of materials including metals, semiconductors, metal oxides, and polymers into arbitrary shapes on a wide variety of flexible substrates including plastics, papers, and textiles.

1.2 Research Objectives

To address the challenge that is stated above, this research project focuses on developing an alternative pattering technique, named as electrochemical replication and transfer (ERT), which is expected to achieve high resolution, high

throughput, and low cost simultaneously. The research objectives of this research are listed in detail as following:

(1) To develop an alternative patterning technique, named as electrochemical replication and transfer (ERT).

(2) To study and illustrate the resolution, throughput, and cost of ERT technique and to compare it with other typical patterning techniques.

(3) To investigate the applicability of ERT method in a wide variety of target materials and flexible substrates.

(4) To study the mechanism of ERT process.

(5) To demonstrate the applications of ERT technique.

1.3 Research Originality

Pattern generation is a basic requirement in a wide range of research and industrial fields. This research develops a new patterning technique, termed electrochemical replication and transfer (ERT), which can create high-resolution and large-area functional material patterns via a facile and low-cost way. As an alternative patterning technique, ERT bridges the research gap of tradeoff among the resolution, throughput, and cost in the conventional patterning technique.

On one hand, the mechanism of ERT process allows to fabricate arbitrary patterns with different feature sizes spanning from sub-100 nm to micrometer scale on a large area within minutes. The pattern resolution is only limited to the pre-made template and the throughput of ERT can reach 10-10^2 m^2/h regardless of the feature

size. On the other hand, the entire process is lithography-free and purely additive manufacturing. The use of electrodeposition equipment ensures the ultra-low cost of the patterning process. Furthermore, the ERT method can readily fabricate patterns of a wide variety of material including metals, semiconductors, metal oxides, and polymers on a wide variety of flexible substrates including plastics, papers and textiles.

1.4 Outlines of the Thesis

The thesis is organized as following:

Chapter 1, Introduction, gives a brief introduction of the background and challenges in the field of conventional patterning techniques. Then the objective and originality of this research project are stated.

Chapter 2, Literature Review, reviews comprehensively on the mechanism and fabrication process of typical conventional patterning techniques. Then the strategies towards high resolution, high throughput, and low cost for patterning techniques are discussed and summarized. After the comprehensive comparison and summary of patterning techniques in terms of resolution, throughput, and cost, the research gap is pointed out at the end.

Chapter 3, Methodology, describes the methodologies for this study, including materials, equipment, fabrication processes, and characterization techniques.

Chapter 4, Electrochemical Replication and Transfer (ERT), introduces the fabrication process of ERT method and its applicability to a wide variety of geometric patterns, target materials, and flexible substrate. The comparison of ERT with typical conventional patterning techniques is also illustrated.

Chapter 5, Mechanism Analysis of ERT Process, discusses the mechanism of ERT process, including the rational structure of template and optimization of electrodeposition parameters in the step of electrochemical replication and the functions of surface modification and UV-curable binder in the step of transfer.

Chapter 6, Applications of ERT Method, demonstrates flexible electronic devices based on ERT method, including flexible transparent electrodes for flexible transparent heaters (FTHs), organic light-emitting diodes (OLEDs), and touch screen panels (TSPs), source/drain electrode for organic electrochemical transistors (OECTs), and interdigital electrode for micro-supercapacitors (MSCs).

Chapter 7, Conclusions and Suggestions for Future Research, shows the conclusions of this study and discusses the outlooks and suggestions for this new patterning technique.

Chapter 2: Literature Review

Patterning technique can generate arbitrary patterns with feature sizes ranging from a few nanometers up to tens of millimeters on substrates of choice, which is the fundamental step to fabricate electronic, photonic, biological and medical devices for a wide range of applications in modern science and technology (as shown in Figure 1).[1-6] Frequently used patterning techniques include two main categories: lithography and printing. Lithography uses light, mechanical force, or electron beam to transfer a geometric pattern from a premade mask to a resist layer.[8] The patterned resist acts as a protective layer in subsequent etching or lift-off process to generate pattern of target material on the substrate. Generally, the pattern fabricated by lithography belongs to subtractive manufacturing, which is also called as top-down process. Lithography techniques are usually finished in an as-called parallel replication, which shows excellent throughput. Printing is direct-write patterning technique. In printing process, pattern is generated by serially scanning a patterning element across a substrate. The serial mode of printing process usually limits its throughput. However, some printing processes (such as inkjet printing) are additive manufacturing. This bottom-up process can significantly reduce the cost of material consumption.

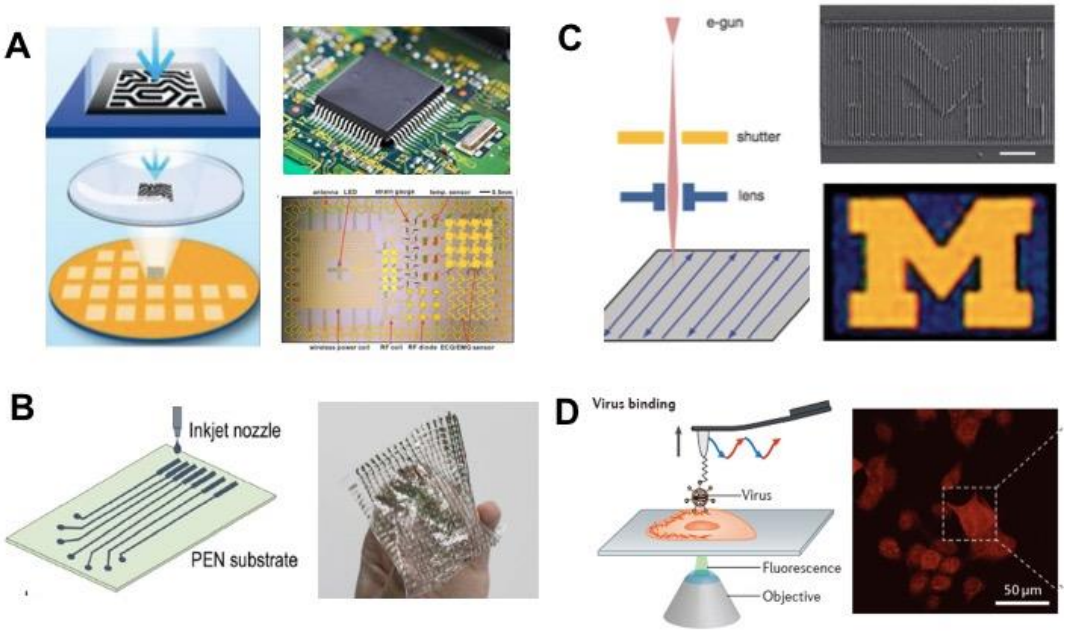


Figure 1. A wide range of applications of various patterning techniques: (A) photolithography for traditional rigid electronics and emerging flexible electronics, (B) inkjet printing for printed electronics, (C) electron beam lithography and ion beam lithography for photoelectronics, (D) scanning probe lithography for biological research, etc.[1, 12-16]

In the following sections, several typical patterning techniques, including photolithography, electron beam lithography (EBL), nanoimprinting lithography (NIL), printing techniques (inkjet, screen, flexographic, and gravure printings), and other emerging patterning techniques, will be introduced in terms of principle, fabrication process, resolution, throughput, cost, etc. Particularly, the strategies to optimize the resolution, throughput and cost of patterning techniques will be discussed respectively. Subsequently, a comprehensive comparison in terms of resolution, throughput and cost of several typical patterning techniques will be analyzed. Finally, the research gap for this research project will be highlighted

after the comprehensive review on the patterning techniques.

2.1 General Introduction of Patterning Techniques

2.1.1 Photolithography

Photolithography, also known as optical lithography, is the most widely used lithography process in the fabrication and mass production of integrated circuits in the semiconductor industry in the past decades. It has been the main workhorse to push the Moore's law.[7-8, 17-18] Photolithography is a photon-based patterning technique. It uses light, usually ultraviolet (UV) light, to transfer geometric pattern from a photomask to a photoresist (light-sensitive polymer) layer on a substrate of choice. The mechanism of pattern formation in the photoresist is the UV light induced chemical reactions on the photoresists. There are two kinds of chemical reactions for two types of photoresists during the UV exposure, i.e., scissoring in positive photoresist and crosslinking in negative photoresist. This patterning of photoresist process generally consists of coating of photoresist on the substrate, pre-baking of photoresist, UV-exposure of photoresist covered with photomask, post-baking of photoresist, and developing (selectively dissolving photoresist to generate pattern).[5, 8, 19] A schematic illustration of photolithography is shown in Figure 2. The patterned photoresist layer is acted as a mask and subsequently the pattern in the target material is formed underneath the photoresist through a series of steps, including deposition of target material, etching or lift-off, and stripping of photoresist. Two fabrication routes, etching and lift-off, for patterning target material based on photolithography are shown in Figure 3. Generally, the etching route uses positive resist, in which the exposed regions are removed during

developing step. The lift-off route uses negative resist, in which the unexposed regions are removed.[20]

During the whole process of patterning target material, the photolithography is only used to pattern the photoresist. However, it is the fundamentally important step for the whole process. These two fabrication routes, etching and lift-off, for patterning target material are not only combined with photolithography, but also applicable to other kinds of lithography processes, such as electron beam lithography (EBL), nanoimprint lithography (NIL), etc.[5]

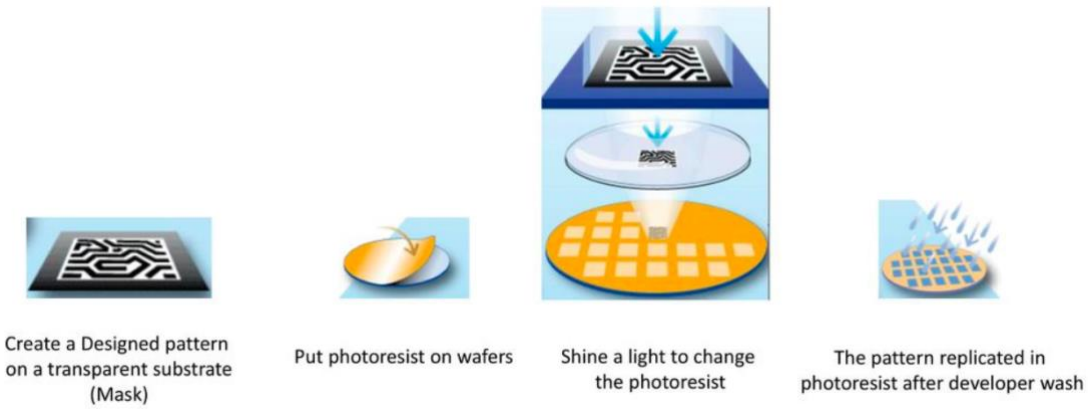


Figure 2. Schematic illustration of photolithography process: design of photomask, coating of photoresist on wafer, exposure of photoresist covered with photomask, and developing to obtain pattern replicated in photoresist (scheme taken from presentation slide of ASML company, a leading manufacturer of photolithography systems).

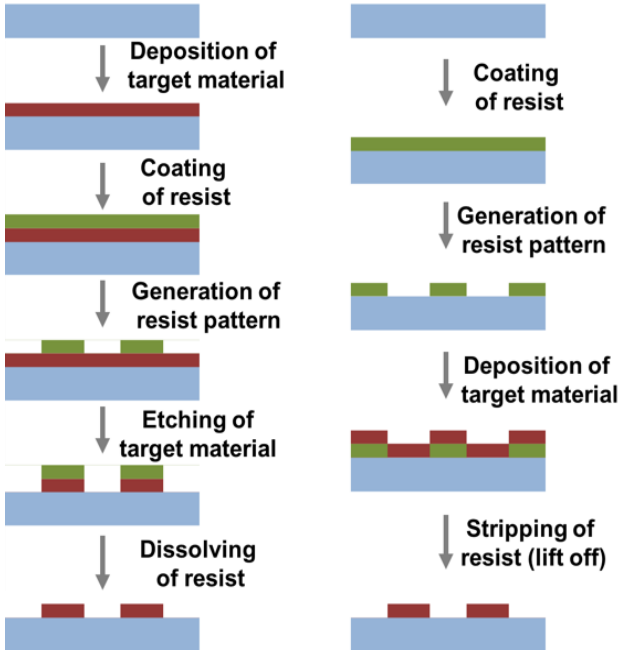


Figure 3. Two typical fabrication routes for patterning target material based on lithography: etching (left) and lift-off (right). Generally, positive resist is used in etching route, while negative resist used in lift-off route. For positive resist, the exposed regions are removed during developing step, while for negative resist, the unexposed regions are removed.[20]

2.1.2 Electron Beam Lithography (EBL)

Electron beam lithography (EBL) utilizes electron beam to scan across the surface of electron-sensitive resist to make an exposure for generation of patterns. This electron beam is focused with diameter as small as a few of nanometers and controlled by computer to scan on the surface of resist in a point-by-point mode (serial writing) to generate a pattern.[20] Figure 4 shows a schematic illustration of electron beam lithography.[5] The exposure of resist under electron beam indicates chemical reaction of resist caused by electron-electron collision, i.e., scissoring in

the case of a positive resist and crosslinking in the case of a negative resist.[19, 21] After the resist is selectively exposed under electron beam, the developing step can selectively remove unnecessary regions, i.e., for positive resist, the electron beam exposed regions are removed, while for negative resist, the unexposed regions are removed.[20] This phenomenon is similar with that in photolithography. However, there is no mask in this process and the pattern is generated in a low-speed serial writing mode. The electron beam lithography only generates the pattern in the resist layer. For further patterning in the target material, etching or lift-off route is needed to implement step by step.

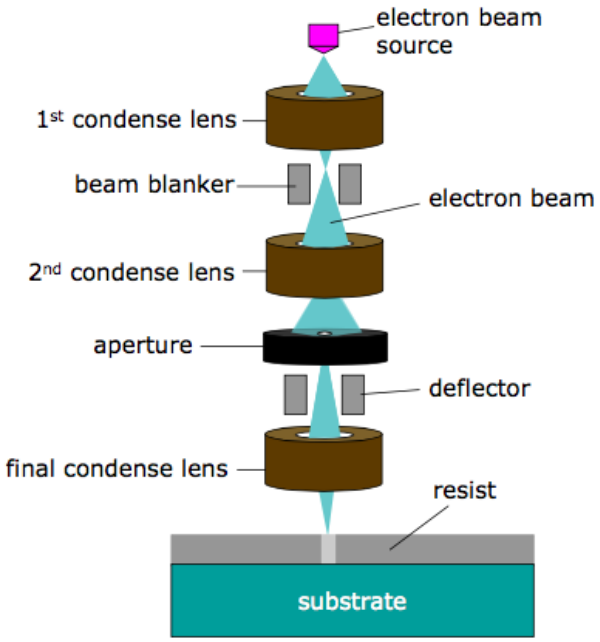


Figure 4. Schematic illustration of electron beam lithography. Electron beam is focused as small as nanoscale and scans on the resist for exposure to generate the pattern by a serial writing mode.[5]

2.1.3 Nanoimprint Lithography (NIL)

Nanoimprint lithography (NIL) is an emerging nanopatterning technique, which creates patterns by mechanical deformation of a deformable material using a pre-made hard mold to replicate the patterns on the surface of resist.[22-24] Photolithography and e-beam lithography employ radiation (photons and electrons) to change the local chemical properties of resists and realize the generation of patterns. On the other hand, for nanoimprint lithography, the pattern in resist is formed by mechanical deformation with a pre-patterned mold. Therefore, its fundamental physical principle enables its resolution not to be limited to diffraction which is common in the radiation-based nanolithography techniques.[24] The typical process of nanoimprint lithography is shown in Figure 5, mainly including pressing mold and solidifying resist, removing mold, and removing residual resist by reactive ion etching (RIE) to transfer pattern.[5] The resists can be thermoplastic resists or UV curable polymers. Correspondingly, there are two main categories: thermal nanoimprint lithography (T-NIL, or hot embossing) and UV curable nanoimprint lithography (UV-NIL).[25]

Nanoimprint lithography was firstly introduced and developed by Stephen Y. Chou in 1995.[22] The parallel manner enables this nanopatterning technique to achieve high throughput with a relatively facile route. Therefore, nanoimprint lithography quickly became an advantage alternative nanopatterning technique and a serious contender of photolithography and e-beam lithography because of its high resolution and high throughput with a relatively low cost.[5, 10]

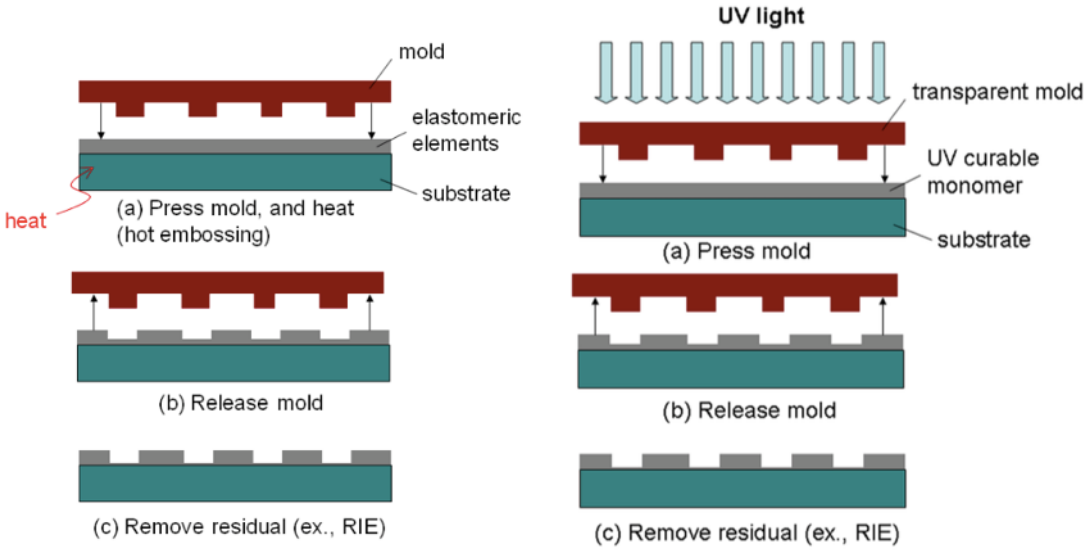


Figure 5. Schematic diagrams of nanoimprint lithography (NIL). Left, thermal nanoimprint lithography (T-NIL). Right, UV curable nanoimprint lithography (UV-NIL).[5]

2.1.4 Printing Techniques: Inkjet, Screen, Flexographic, and Gravure Printings

Conventional printing techniques, such as inkjet, screen, flexographic, gravure printings (as shown in Figure 6), are mass-patterning strategies and widely used in the low-cost flexible printed electronics where high resolution and high performance are not required critically. These printing techniques are usually integrated in the continuous, roll-to-roll process and achieve ultrahigh throughput with relatively low cost of fabrication.

Inkjet printing creates patterns through a mode as called printing on demand. This

direct printing technique is flexible, versatile, and can be set up with relatively low cost and effort.[26] During the process of inkjet printing, the functional liquid (ink) is transferred from the nozzle to the substrate (as shown in Figure 6D). This process can be divided into five steps: ejection from the nozzle, flight, impact on the substrate, ink spreading, and drying of the solvent.[11, 27-28] Based on the different mechanism of droplet forming at the nozzle, there are three types of inkjet printings, i.e., thermal inkjet, piezoelectric inkjet, and continuous inkjet. In thermal inkjet, a small electrical heater heats up the ink in the cavity and a bubble is formed to push the ink out of the nozzle. In piezoelectric inkjet, an electric pulse changes the shape of the piezoelectric element, which further induces a mechanical pressure on the ink. In continuous inkjet, the ink is applied by a constant pressure and forms a continuous flow.[26, 29] The sizes of droplets created by these mechanisms are usually at tens of micrometer scale, which is directly determine the resolution of inkjet printing.

Screen printing, also called as stencil printing, uses a squeegee to press inks to print on the substrate through a screen with porous mesh (as shown in Figure 6C).[30] The thickness of pattern fabricated by screen printing is typically higher than ~0.5 μm. The resolution of screen printing is also limited (~50 μm). Because of its high thickness and poor resolution, screen printing is not appropriate for high-resolution printed electronics.[11, 30] During the research in academic lab, there is one kind of screen printing, also called as evaporation printing, using a shadow mask (stencil) with designed porous to cover on the substrate, which further enables material to be deposited selectively on the substrate through thermal evaporation, e-beam deposition, sputtering, etc.

Flexographic printing can be considered as a relief printing process, where a cylinder with a positive relief structure to print inks (as shown in Figure 6A).[31] The printing process is complemented by attaching inks to the printing cylinder and then allowing the cylinder to roll over the surface of target substrate, transferring the inks. The advantage of flexographic printing compared with other kinds of printing techniques is that it is applicable to a wide range of inks, not only oil-based inks, but also water-based inks.[29] The printing speed is high enough for its capability in the high-volume manufacturing (HVM). However, the normal resolution of flexographic printing is about 100 μm, which is difficult to meet the requirement of high resolution.[31-33]

Gravure printing uses gravure roller with engraved pattern on surface to print ink (as shown Figure 6B). The process of gravure printing consists of three successive steps: (1) filling the cells engraved on the surface of gravure roller with inks, (2) wiping excess inks on the surface of roller by a doctor blade, and (3) transferring the remaining inks in the engraved cells to the target substrate.[11, 31, 34] Gravure printing is widely used in the flexible printed electronics. The advantages of gravure printing are the high printing speed and throughput own to its continuous, roll-to-roll fabrication.[11, 33] However, the printing resolution is typically ~50 μm, which is not superior than other patterning techniques. The very high cost of gravure rollers and roll-to-roll system indicate that gravure printing is more suitable used in the high-volume production in the factory rather than in the academic lab.[35]

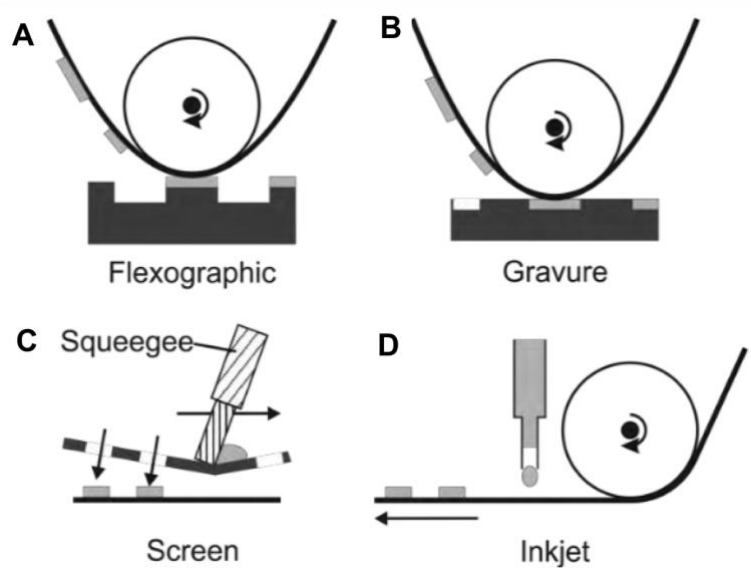


Figure 6. Schematic illustration of four typical printing techniques: flexographic, gravure, screen, and inkjet printings.[36-37]

2.1.5 Other Emerging Patterning Techniques

In addition to the aforementioned patterning techniques, people have developed a wide variety of patterning techniques in the past decades. The targets mainly focus on the high-resolution, high-throughput, and cost-efficient pattering techniques. In this section, three typical kinds of emerging patterning techniques, i.e., microcontact printing (μCP), dip-pen nanolithography (DPN), and nanotransfer printing (nTP), will be briefly introduced. Even through these emerging patterning techniques are not mature enough for practical application in the industry, they have been widely studied and used in the academic research in the past decades.

Microcontact Printing (μCP)

During 1990s, the Whitesides group in Harvard University firstly introduced and developed an alternative, non-photolithographic set of microfabrication method soft lithography, which uses a patterned elastomer as the stamp (or mold, mask) to generates micropatterns or microstructures by contact printing, embossing, and replica molding. They have reported six types of such techniques: microcontact printing (μCP), replica molding (REM), microtransfer molding (μTM), micromolding in capillaries (MIMIC), solvent-assisted micromolding (SAMIM), and phase-shift photolithography.[38-39] The powerful patterning capability and experimental simplicity make soft lithography achieve widespread use in the academic research for applications in fields ranging from electronics, photonics, biotechnology, to microfluidics. Among these techniques, microcontact printing (μCP) was firstly reported and is probably the best known soft lithographic patterning technique,[30] which is used as a typical example for illustration in this section.

The concept and process of microcontact printing (μCP) are straightforward. It uses a soft elastomeric stamp with relief structure to form pattern of self-assembled monolayers (SAMs) on the surface of substrate by contact. As shown in Figure 7A, poly(dimethylsiloxane) (PDMS) stamp with relief pattern is inked with alkanethiol solution and contacts on the surface of Au. The reaction between alkanethiol and Au with loss of dihydrogen forms a pattern of alkanethiol layer on Au surface. This patterned alkanethiol layer is used as resist for etching or deposition in the following steps. The minimum feature size fabricated by microcontact printing was reported with several tens of nanometer.[39] However, the surface diffusion of molecular inks and disorder at the edges of printed SAMs limit its practical resolution at around 100 – 200 nm.[40]

Nanotransfer Printing (nTP)

Nanotransfer printing (nTP) was developed by Rogers, J. A., *et al*.[41-47] The fabrication process of nanotransfer printing is very similar to that of microcontact printing. In nanotransfer printing, the ink is solid target material, but not liquid phase that used in microcontact printing. Therefore, nanotransfer printing does not suffer from the surface diffusion, edge disorder in inks, and post-steps to produce patterns of target materials.[41] As shown in Figure 7B, the PDMS stamp with relief surface is deposited with target material Au and then covered on the substrate which is modified with thiol-group SAMs. The reaction between Au and thiol group realizes the transfer of Au from the relief of stamp to the surface of substrate.[42] Nanotransfer printing allows to transfer functional materials to a wide range of substrates, which makes it a useful approach in the emerging field of flexible and stretchable electronics.[30]

Dip-Pen Nanolithography (DPN)

Dip-pen nanolithography (DPN) was reported by Mirkin's group in 1999.[48] The process mechanism of dip-pen lithography is shown in Figure 7C. An atomic force microscope (AFM) tip is used as a pen and inked with alkanethiols. The inked tip writes nanopatterns on the substrate directly by the molecular transport from the tip to the substrate. The significant advantage of DPN is that it is a simple and powerful method to generate nanopatterns with high resolutions (30 nm at the first report) comparable to those achieved with much more expensive patterning techniques, such as photolithography, electron beam lithography. However, as a serial writing technique, the relatively low throughput limits it for practical applications in the industry. After DPN was reported, there have been a number of

variants of DPN by using novel multifunctional tips, such as thermal DPN (tDPN),[49] eletro pen nanolithography (EPN),[50] nano fountain pen (NFP).[51-52]

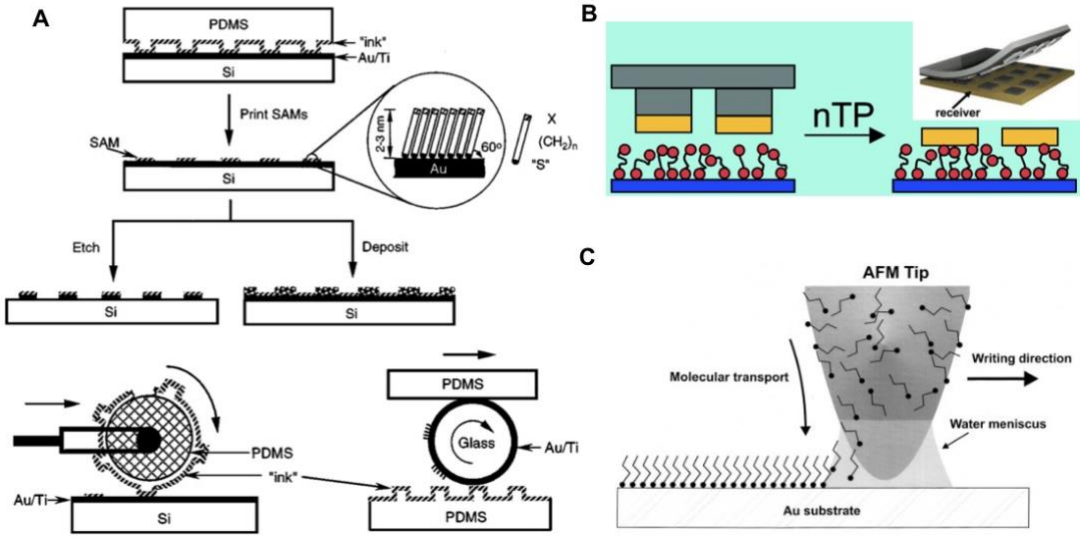


Figure 7. Schematic illustration of three typical emerging patterning techniques. (A) Microcontact printing (μCP): the alkanethiol inked on the elastomeric stamp is printed on the surface of Au substrate. Top, printing on a planar surface with a planar stamp. Bottom left, printing on a planar surface with a rolling stamp. Bottom right, printing on a nonplanar surface with a planar stamp.[38-39] (B) Nanotransfer printing (nTP): the target material inked on the surface of mold is printed on the substrate directly.[42, 46]. (C) Dip-pen nanolithography (DPN): an atomic force microscope (AFM) tip is used to write alkanethiol on a Au surface.[48]

2.2 Towards High Resolution

Resolution is a fundamental measure of the capability of a patterning technique. The definition of resolution is perfectly general: the smallest feature of a given

type which can be printed with a specified depth of focus. For depth of focus (DOF), it is defined as the range of focus that keeps a given feature in all specifications (linewidth, sidewall angle, and resist loss). There are two types of resolutions in patterning technique: the smallest pitch (or half-pitch, pitch resolution) and the smallest feature size (or critical dimension, feature resolution) (shown in Figure 8).[53-54]

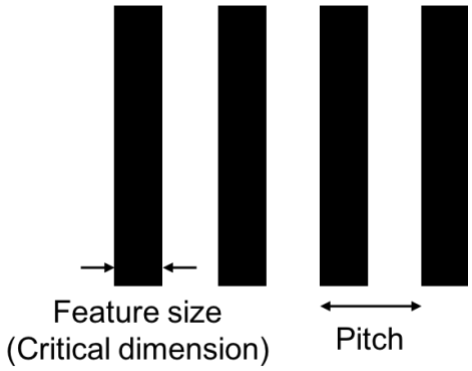


Figure 8. Two distinct resolutions in patterning technique: the smallest pitch (pitch resolution) and the smallest feature (feature resolution).[54]

The resolution of one patterning technique is fundamentally relevant to the mechanism of fabrication process. The strategies to enhance resolution for patterning techniques are usually associated with the improvement and upgradation of fabrication tools. In the past years, resolution enhancement is usually achieved by upgrading patterning equipment or optimizing fabrication condition base on considering the fundamental mechanism of patterning process. In this section, an introduction on resolution enhancement for typical patterning techniques will be given.

In the semiconductor industry, Moore's law describes the long-term trend in the integrated electronics that the number of transistors on an integrated circuit doubles approximately every 2 years.[55] This trend still continues today. The higher and higher resolution of nanofabrication technique, especially photolithography, is the fundamental factor to pushing Moore's law. The history of photolithography is a continuous effort to enhance the resolution of photolithography tools.[56] The resolution of photolithography is largely determined by the well-known Rayleigh's equation. The resolution *R* (half-pitch) can be described by the following equation:

$$R = k_1 \frac{\lambda}{NA}$$

where k_1 is the Rayleigh coefficient, λ is the optical wavelength, and *NA* is the numerical aperture of the optical system. k_1 is constant and determined by the processing conditions, such as illumination and the photoresist properties. Considering the optical perspective and periodic structures, the lower limit of k_1 is 0.25.[17] *NA* is determined by the optical lens and medium used in the optical system, which is given by the following equation:

$$NA = n \sin \theta$$

where *n* is the index of refraction of the medium between the lens and the image plane and θ is the angular aperture of the lens.

According Rayleigh equation shown above, to obtain higher resolution, there are two primary strategies: using shorter wavelength light (λ) and lens systems with larger numerical apertures (*NA*).[7-8] The optical wavelength for photolithography

has evolved from visible 436-nm g-line, ultraviolet 365-nm i-line, to deep ultraviolet (DUV) 248-nm KrF and 193-nm ArF excimer lasers, and to extreme ultraviolet (EUV, wavelength of 10 nm – 120 nm) with 13.5-nm wavelength (as shown in Figure 9).[56-61]

The later strategy to enhance resolution by increasing *NA* value is realized by immersion technology. Water shows higher refractive index (n = 1.44) than that of air (n = 1) and is adapted in the semiconductor industry to produce water-immersion lithography tools. The *NA*s can reach 1.35.[62] As shown in Figure 10, 193-nm ArF immersion lithography shows a resolution with 38 nm (half pitch), where k_1 and *NA* are optimized to 0.265 and 1.35, respectively.[63]

Extreme ultraviolet (EUV) lithography is a strong candidate to enhance the resolution to sub-10 nm. However, since almost all materials absorb energy at 13.5-nm wavelength of EUV, the system of EUV lithography is different from that of previous optical lithography (as shown in Figure 11).[64] The entire optical path must be controlled in a vacuum condition. The photomask in EUV lithography is a reflective mask instead of transmissive mask.[56, 64-67] The systems of EUV becomes much more complicated and costlier than those of traditional optical lithography. Based on EUV technique, the resolution in semiconductor industry has been improved significantly in the past years and ensures Moore's law to continue. The sub-10 nm patterns have been achieved from lab research to industry application.[60, 63, 68-72] In April 2019, Taiwan Semiconductor Manufacturing Company (TSMC) began commercial production of their own 5 nm process based on newly developed technique of EUV lithography.[73]

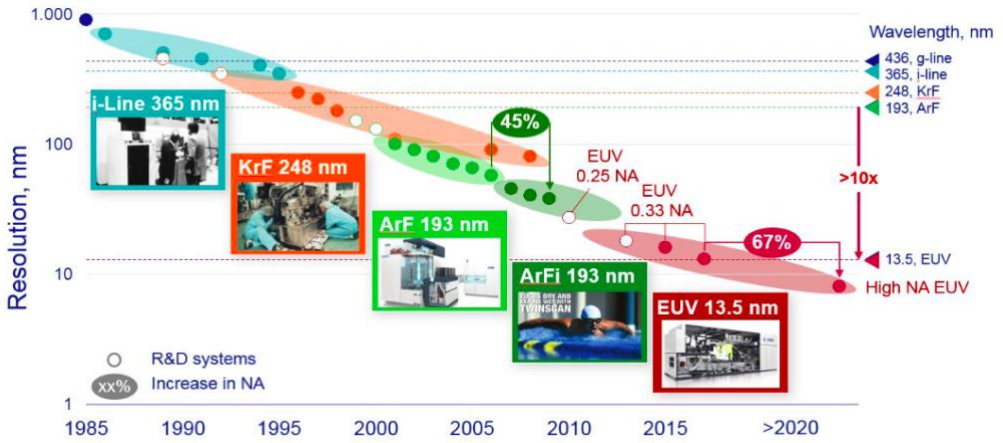


Figure 9. Roadmap of optical lithography: 436-nm g-line, 365-nm i-line, 248-nm KrF, 193-nm ArF excimer lasers, and to extreme ultraviolet (EUV) with 13.5-nm wavelength. Wavelength reduction and larger *NA* enhance the resoluiton.[60]

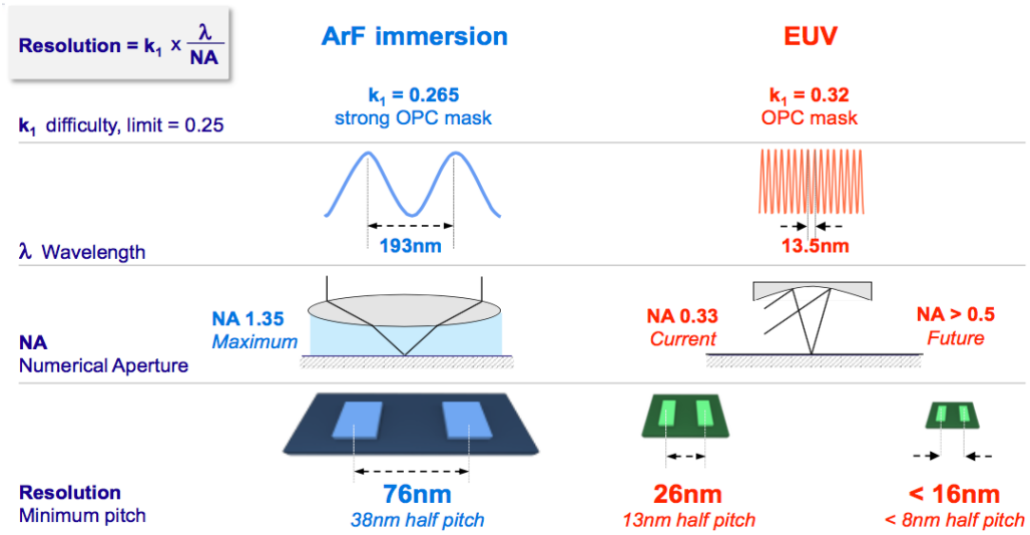


Figure 10. Strategies to enhance the resolution of photolithography: shorter wavelength λ and larger numerical aperture *NA*. Left, 193-nm ArF immersion lithography. Right, 13.5-nm EUV lithography.[63]

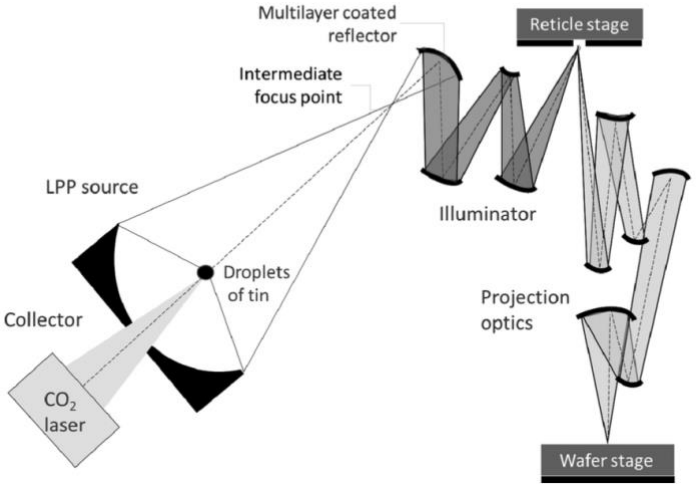


Figure 11. Schematic diagram of an EUV lithography system. Laser-produced plasma source (LPP) produces EUV light with wavelength of 13.5 nm. A collector mirror focuses the EUV light into a reflection optical system, as called illuminator. The mask with pattern (called as reticle) receives the light from illuminator and reflects it through a projection optics. The light is focused by the projcetion optics and transfers the pattern on the photoresist on wafer substrate.[64, 74]

Electron beam lithography can reach a high resolution of nanoscale pattern with a much simpler way, while compared with photolithography. The resolution of electron beam lithography is fundamentally relevant to the probe size of electron beam on the electron beam tool. The electron beam can be focused down to very small sizes, about 1 nm in the case of a typical scanning electron microscope (SEM). For better quality of SEM with high energy (30 kV), the probe size of electron beam can reach 0.5 nm or even much smaller.[20, 75] However, the final minimum feature sizes of pattern fabricated by electron beam lithography usually

are bigger than the probe size of focused beam. The secondary electrons are one major obstacle that limits the resolution of electron beam lithography. A large part of exposure with a range of 2 - 3 nm on resist is caused by the forward and backward scattering of secondary electrons (Figure 12). The exposed resist is not only limited to the location defined by incoming electron beam.[20, 76-77] On the other hand, the flatness of the substrate should be good enough and ensure the electron beam is focused on the resist.[20] Silicon substrate is suitable in the process of electron beam lithography. But for high-roughness polymers substrates for emerging flexible electronics, there will be a significant loss in resolution. Furthermore, it is a big challenge for direct writing on dielectric substrates because charge accumulation on the isolated substrate causes beam reflection and produces distorted patterns.[78-79] By using high energy (~100 kV) of electron beam, the resolution can reach sub-10 nm. There are several reports of dots/lines with ~5-nm resolution.[9, 80-83]

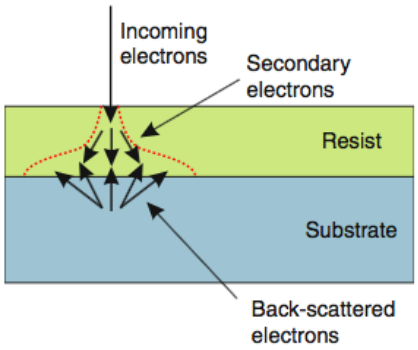


Figure 12. Illustration of infuence of secondary electrons on the resolution of electron beam lithography. Extra exposure on resist is caused by the scattering electrons, not limited to the location defined by the incoming electron beam.[76]

The fabrication process of nanoimprint lithography is the mechanical deformation. Therefore, its resolution is related to the surface topology of the mold, which is not limited to the wave diffraction, scattering and interference in the resist in the cases of photolithography or electron beam lithography. However, the molds for nanoimprint lithography are needed to be fabricated by other patterning techniques, such as conventional photolithography, EUV lithography, electron beam lithography.[22-23, 84] In other words, the minimum feature sizes on the mold are limited by the other patterning techniques and the resolution of nanoimprint lithography should not exceed that of the techniques used to fabricate the molds. Since Chou, S. Y. firstly reported nanoimprint lithography with 25-nm feature size in 1995,[22] the resolution of nanoimprint lithography has been enhanced to 10 nm or even more.[25, 85-86]

The resolutions of the four typical printing techniques (inkjet, screen, flexographic, and gravure) are much poorer than the three lithography techniques introduced above. Their resolutions are usually at the tens of micrometer (μm) scale. For example, the resolution of inkjet printing is limited to 20 to 100 μm. The main reason is fundamentally relevant to its fabrication process. The size of droplet cannot be small enough. Furthermore, after the droplets released from the nozzle, the statistical variations of the flight direction and diffusion on the substrate increase the feature size of printed patterns.[30, 87] Even though a resolution-enhanced printing technique, named as electrohydrodynamic (EHD) jet printing, is developed based on traditional inkjet printing, its resolution is still limited at micrometer or sub-micrometer scales and the throughput is sacrificed greatly at the same time.[88-92] The other kinds of printing techniques are also limited in poor resolution at tens of micrometers.[11, 32-33, 93] The advantages of these printing

techniques are the high throughput and low cost, which will be introduced in the following sections.

2.3 Towards High Throughput

The throughput is defined the patterning speed of a patterning technique forming patterns. Patterning area per unit time (square meter per hour, m^2/h, or wafer per hour, WPH) or patterning length per unit time (meter per second, m/s) is usually used for measuring the patterning throughput.[11] It is obvious that high throughput indicates the ability of mass production and reasonable fabrication cost for a patterning technique applicable in the practical industry. It is generally accepted that the high-volume-production techniques show throughput of more than 100 wafers per hour (WPH, 36 s for 1 wafer) corresponding to >1 m^2/h (10^{12} $\mu m^2/h$).[94] In general, parallel process shows much higher throughput than that of serial writing process. The integration of roll-to-roll strategy in the patterning process can significantly improve the throughput by orders of magnitude. In this section, a discussion on increasing throughput based on these two strategies will be illustrated.

Serial Writing VS. Parallel Replication

Patterning techniques based on serial process show relatively low speed and throughput, because the patterns are created by direct-writing in a point-by-point mode. Typical pattern techniques based on serial mode include electron beam

lithography, focused ion beam lithography, scanning probe lithography, etc. These serial nanolithography shows relatively low throughput of 10^6 $\mu m^2/h$ or even smaller (as shown in Figure 13).[94-95]

The main advantage of electron beam lithography over photolithography is generation of higher-resolution and versatile patterns in a much easier way. However, it is a time-consuming serial process, which seriously limits its throughput. In order to improve its throughput, people have tried to develop parallel-mode electron beam lithography, such as projection electron beam lithography, multiple beam system, and variable shaped beam tools.[7, 96-101] The challenge for all of these emerging technologies for increasing throughput is to sacrifice its high resolution. Therefore, the single Gaussian beam direct writing still plays the major role among the electron beam lithography. Its applications focus on research, mask making, prototyping, and small volume products.[21]

Dip-pen nanolithography (DPN), introduced by Mirkin's group in 1999, can direct write sub-50 nm pattern in the ambient environment.[48] However, the nature of serial writing limits its throughput. In order to improve the writing speed, parallelization DPN technique should be the effective strategy.[102] Mirkin's group successively developed massively parallel dip-pen lithography,[103-105] polymer pen lithography (PPL),[106] beam pen lithography,[107] hard-tip, soft-spring lithography (HSL).[108] This improvement by integration of parallel strategy significantly increases the throughput of scanning probe-based lithography. However, there is a drop of resolution while increasing the throughput by the parallel strategy.[106, 109]

In contrast, photolithography and nanoimprint lithography are typical parallel replication of patterns and show relatively high throughput in a range of 10^{10} to 10^{12} μm²/h (as shown in Figure 13).[94-95] High throughput enables photolithography to be the main workhorse in the semiconductor industry.

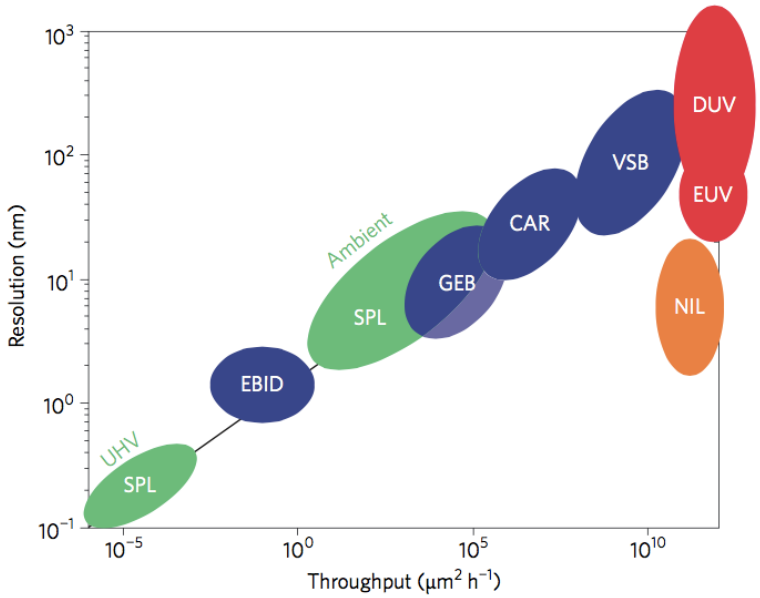


Figure 13. Throughput and resolution in nanolithography. Parallel-mode lithography shows high throughput in the range of 10^{10} to 10^{12} μm²/h. Red shapes: deep ultraviolet (DUV) lithography, extreme ultraviolet (EUV) lithography. Orange shape: nanoimprint lithography (NIL). Serial-mode lithography has much lower throughput (10^{-6} – 10^{6} μm²/h) compared with parallel-mode technique. Blue shapes: maskless electron beam lithography (EBL). EBID, electron-beam-induced deposition; GEB, Gaussian beam lithography; CAR, chemically amplified resists; VSB, variable shaped beam. Green shapes: scannning probe lithography (SPL).[94-95]

Roll-to-Roll Process

Roll-to-roll (R2R) process is a continuous, low-cost, and environment friendly manufacturing method and widely used in various industrial sites.[110-111] While integrated in the patterning technique, its continuity can drastically increase the throughput by orders of magnitude. As shown in Figure 6, these conventional printing techniques are intrinsically integrated with roll-to-roll process. Their throughput can reach an ultrahigh level (~10^3 m^2/h or even higher, as shown in Figure 14), much higher than those of normal parallel mode.[31, 33, 35]

The integration of roll-to-roll process is not applicable in all patterning techniques, especially those vacuum-based techniques (such as electron beam lithography). For those ambient technique, such as nanoimprint lithography, people have researched on the integration of roll-to-roll strategy to improve the throughput. Guo's group reported a continuous roll-to-roll nanoimprint lithography (R2RNIL) process (as shown in Figure 15).[112] This roll-to-roll mode greatly improves the throughput of nanoimprint lithography by continuously producing large-area, high-speed patterns.[113-116] However, there is a trade-off between throughput and resolution. While the roll-to-roll strategy increases the throughput into a high value (~1 m^2/h or more), the as-printed patterns cannot maintain high resolution as that fabricated by precise traditional nanoimprint lithography (~10 nm). The resolution of R2RNIL may go down to sub-micrometer or micrometer scale.[35, 112]

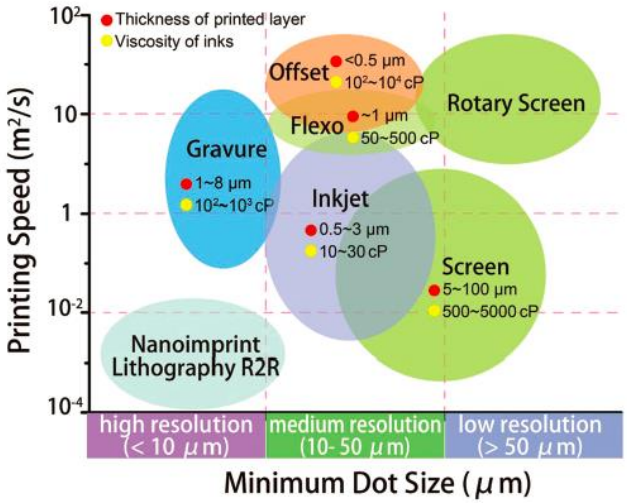


Figure 14. Throughput (printing speed) and resolution of typical printing techniques.[35]

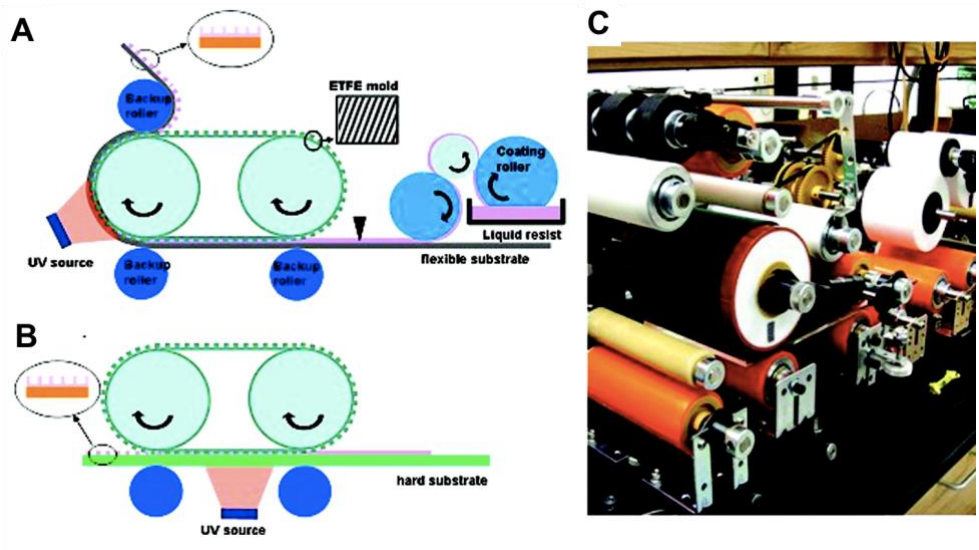


Figure 15. Schematic illustration of roll-to-roll nanoimprint lithrography: (A) roll-to-roll nanoimprint lithrography (R2RNIL) on on flexible web; (B) roll-to-plate nanoimprint lithography (R2PNIL) on rigid substrate. (C) Photography of R2R/R2PNIL apparatus.[112]

2.4 Towards Low Cost

In addition to high throughput, cost effectiveness is one important factor for one patterning technique to ensure its potential for high-volume manufacturing (HVM). The cost of patterning process involves many factors, including the cost of capital equipment, related facility, fabrication environment, material consuming, power consuming, etc. Taking photolithography as an example, the cost of a EUV system reaches 100 million US$ (ASML's EUV system).[117-119] The overall cost of the entire production line is even billions of US$.[120] The fabrication process of photolithography needs to be implemented in critical clean-room environment. The deposition of materials on substrates or resist-patterned substrates usually relies on vacuum-based physical deposition technique (such as thermal evaporation, electron-beam deposition, magnetron sputtering, etc.). The cost of running the production line is more than millions of US$ per year. In this section, the discussion on the cost in various patterning processes will be illustrated from the following consideration: the cost of capital equipment, the requirement of fabrication condition (vacuum or solution process), and material deposition mode (subtractive or additive).

Cost of Capital Equipment

The capital equipment is usually the bottleneck of the whole process of patterning and holds the big percentage of overall cost, such as UV-exposure system in photolithography, electron beam system in electron beam lithography. As

mentioned above, the price of commercial system for EUV lithography reaches 100 million $ or even higher. For chip production, it is cost effective. Old generations of exposure systems have lower prices (still at million level).[101] However, their relatively lower resolutions (sub-micrometer or micrometer) cannot meet the requirement in the semiconductor industry nowadays. These low-resolution exposure systems are used by academic institutions, who are able to suffer relatively low price. Obviously, there is a trade-off between the resolution and price of these UV exposure systems (as shown in Figure 16).[121]

The capital equipment for electron beam lithography is much lower than that of photolithography. However, the price of these vacuum-based equipment still as high as million US$. Furthermore, the throughput of single beam lithography is ultralow, which cannot meet the requirement of high-volume manufacturing. Multiple-electron-beam (MEB) lithography is expected to improve the throughput by orders of magnitude.[122] However, there is still a lot of research to be done for making this technique become mature. The estimated price of MEB system is ~50 million US$, much higher than normal electron beam system.[101]

The non-vacuum-based patterning techniques, such as nanoimprint lithography and inkjet printing, do not require equipment with ultrahigh cost. The nanoimprint tools cost about 0.5M – 5 M US$, which is much lower than that of photolithography system.[123] However, the fabrication of mold with nanoscale structure and removing residue resist by RIE involve expensive equipment.[124] The price of one inkjet printer for the academic lab is only thousands of US$. However, during practical production process, those printing techniques (i.e., inkjet,

flexographic, gravure, screen, etc.) are usually integrated with the continuous, roll-to-roll process. The cost of equipment to realize the whole production line becomes much higher than that in the lab level.

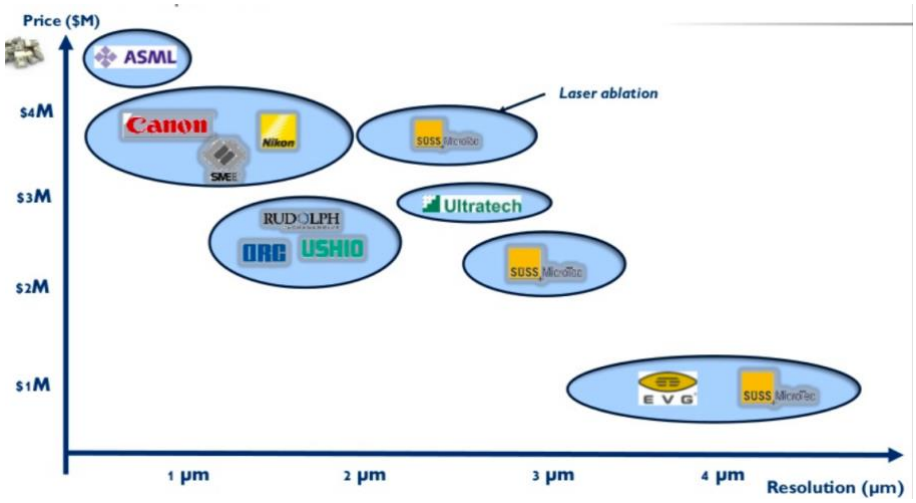


Figure 16. Price (US$ million) VS. resolution capabilities of exposure systems (captured from report by Yole Development).[121] There is a trade-off between the resolution and cost of exposure tools: higher resolution needs higher cost of equipment.

Vacuum Based-Process VS. All Solution-Based Process

The vacuum-based process generally refers to the deposition of materials on the substrates or resist-patterned substrates. These vacuum-based deposition techniques can offer high quality in terms of pattern resolution, surface smoothness, and device performance. However, the vacuum-based process complicates the fabrication process and requires high-cost equipment (as shown in Table 1).[110, 125]

The deposition of materials by non-vacuum-based, all-solution-process can significantly simplify the fabrication process and decrease the cost in terms of equipment and materials consumption.[126] Corresponding to vacuum-based physical deposition (such as thermal evaporation, sputtering), all-solution chemical deposition usually refers to electrodeposition (ED) and electroless deposition (ELD).[126-130] These all-solution deposition technique can be implemented in ambient condition and without requirement of high-cost equipment. A low-cost direct current (DC) power source can run a setup of electrodeposition process (as shown in Figure 17).[131] Electroless deposition can be carried out in chemical bath, without any specific equipment.

Table 1. Capital cost and annual depreciation of vacuum-based deposition (unit: US$ million).[125]

	Sputter, in-line	Sputter, roll	PECVD, in-line	PECVD, roll
Total capital	8.1	6.6	8.3	6.8
Annual depreciation	0.81	0.66	0.83	0.68

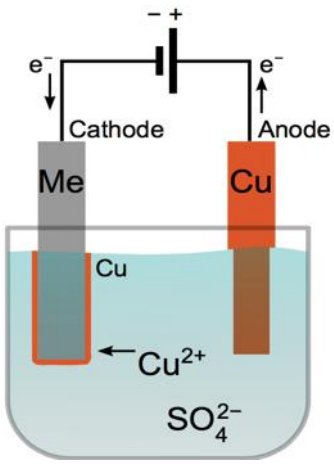


Figure 17. Electrodeposition setup for copper (Cu) deposition in a copper sulfate ($CuSO_4$) bath, equipped with a DC power source.[131]

Subtractive Manufacturing VS. Additive Manufacturing

Reduction of material consumption is one effective solution to decrease the cost of fabrication. In most fabrication routes based on lithography (photolithography, electron beam lithography, nanoimprint lithography, etc.), the target material patterned on substrates is realized by subtractive mode. As shown in Figure 3, material is generally deposited on the whole substrate firstly and the unwanted part is selectively removed away by etching or lift-off process. This subtractive manufacturing results in serious waste of materials and increases the cost of fabrication. In contrast, the strategy of additive manufacturing can effectively avoid the waste of materials. Additive manufacturing has been developed in a high speed in the past decades because it can directly fabricate complex three-dimensional structure and it is advantageous in material and energy consumptions.[132-133] Inkjet printing is additive-type patterning technique, which can print on demand.[134-135] However, the resolution of inkjet printing is still limited

at tens of micrometer scale. Some other additive-type patterning techniques, such as electrohydrodynamic (EHD) printing, dip-pen nanolithography, focused ion beam, etc., can fabricate nanoscale patterns. But their throughput is still relatively low because of their intrinsic property of serial writing.[48, 117, 133, 136]

2.5 Comprehensive Comparison of Patterning Techniques in Terms of Resolution, Throughput, and Cost

Based on the introduction of several typical patterning techniques and the strategies towards high resolution, high throughput, and low cost, a comprehensive summary and comparison of typical patterning techniques in terms of resolution, throughput, and cost will be illustrated, which is directly helpful to point out the research gap of this field.

Based on the data introduced above and summary from references,[5, 33, 93-95, 101, 117, 137-139] Table 2 and Figure 18 show a comprehensive analysis and comparison of five typical patterning techniques (photolithography, electron beam lithography, nanoimprint lithography, inkjet printing and screen printing) in terms of resolution, throughput and capital cost of equipment. In order to meet the requirement of high-volume manufacturing, a perfect patterning technique should show advantages of high resolution, high throughput, and low cost. The data shown in Table 2 and Figure 18 indicate that there is a tradeoff among the resolution, throughput, and cost. Photolithography shows high resolution and high throughput, while the cost of capital equipment and others is ultrahigh. The cost of inkjet printing is relatively low and it can achieve high throughput. But it is seriously limited to its poor

resolution. These tradeoff and challenge also exist in other kinds of patterning techniques. The resolution, throughput, and cost are generally dependent on each other. It is a big challenge for a patterning technique to achieve high resolution, high throughput, and low cost simultaneously.

Table 2. Comparison of typical patterning techniques in terms of resolution, throughput, and capital cost of equipment.[5, 33, 93-95, 101, 117, 137-139]

Patterning technique	Resolution (μm)	Throughput (m^2/h)	Capital cost of equipment ($)
Photolithography	0.007-10	10^{-2}-1	1M-100M
E-beam lithography (EBL)	0.005-0.1	10^{-6}-10^{-3}	1M-5M
Nanoimprint lithography (NIL)	0.01-1	10^{-5}-1	500k-5M
Inkjet printing	20-100	10^{-2}-10	10k-50k
Screen printing	30-100	1-10^3	1k-1M

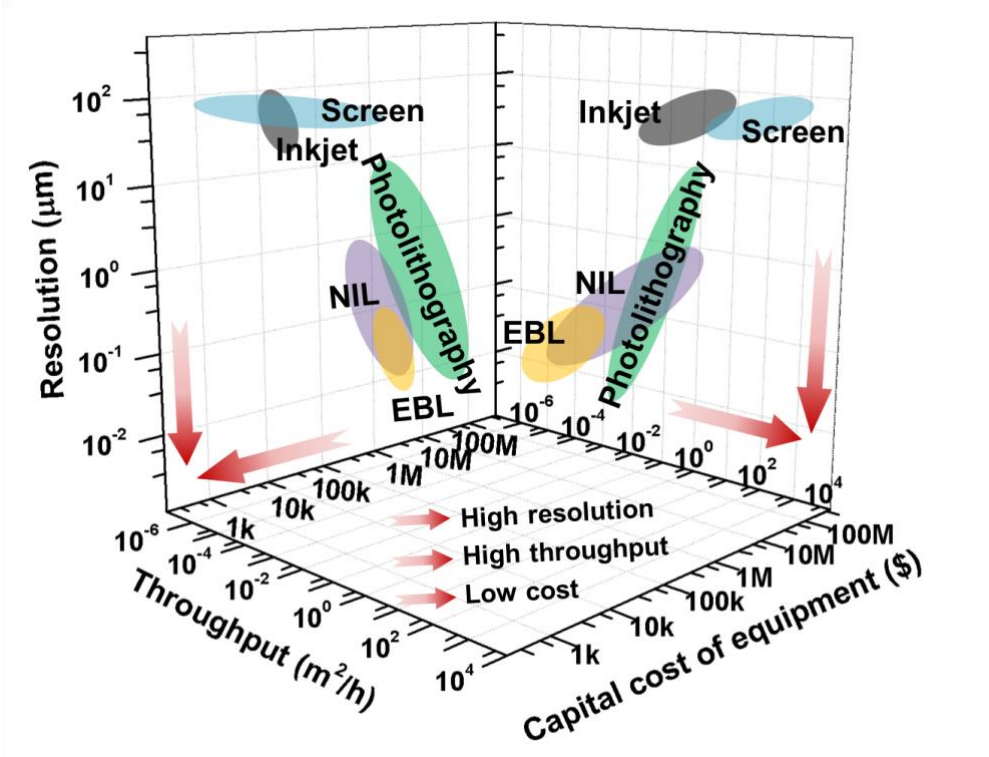


Figure 18. Comparison of typical patterning techniques in terms of resolution, throughput, and capital cost of equipment, based on the data in Table 2. There is trade-off among the resolution, throughput, and cost. Higher resolution generally needs high cost technique, and corresponding throughput is relatively low.

2.6 Conclusions and Summary of Research Gaps

Patterning technique is the fundamental process to generate arbitrary patterns to fabricate electronic, photonic, biological and medical devices for a wide range of applications. In this section, fabrication mechanisms and processes of several typical patterning techniques have been introduced, including photolithography, electron beam lithography, nanoimprint lithography, inkjet, screen, gravure, and flexographic printings, and emerging patterning techniques. To meet the

requirement of high-volume manufacturing in the practical applications, the patterning technique should show high resolution, high throughput, and low cost. The strategies towards high resolution, high throughput, and low cost for conventional patterning techniques have been discussed and summarized. Minimum feature size of one patterning technique is fundamentally relative to its fabrication mechanism and tools. High throughput can be realized by strategy of parallel patterning and integration with continuous, roll-to-roll process. Low cost can be achieved by decreasing the cost of equipment, using all-solution process and strategy of additive manufacturing process.

Photolithography, electron beam lithography, and nanoimprint lithography can reach high resolution with nanoscale, but their throughputs are not good enough or their costs are ultrahigh. Inkjet, screen, flexographic, and gravure printings show high throughput and relatively low cost, while they are all limited to poor resolution with microscale. It is concluded that there is commonly a trade-off among the resolution, throughput, and cost. High-resolution patterning technique is generally accompanied with low throughput and high cost. The resolution, throughput, and cost are dependent to each other. Therefore, it is still a big challenge to develop an alternative patterning technique with the advantages of high resolution, high throughput, and low cost.

Chapter 3: Methodology

3.1 Materials

Pure gold (Au, 99.999%, China New Metal), pure chromium (Cr, 99.9%, China New Metal, China), doped silicon wafer (Si, <100>, Suzhou Crystal Silicon Electronic & Technology CO., Ltd, China), Si wafer with silicon oxide layer (SiO_2, 300 nm, Suzhou Crystal Silicon Electronic & Technology CO., Ltd, China), positive photoresist (AZ 5214E, Microchemicals GmbH, Germany), developer for AZ 5214E (AZ 300 MIF, Microchemicals GmbH, Germany), negative photoresist (NR9-1500P, Futurrex, Inc., USA), developer for NR9-1500P (DR6, Futurrex, Inc., USA), Au etchant (Transene Company, Inc.), methyl isobutyl ketone (99.5%, Sigma-Aldrich), chemicals for electron beam lithography: resist ZEP520A, developer ZED-N50, remover ZDMAC (Tokyo Zairyo Co., LTD.), acetone (99.9%, Sigma-Aldrich), ethanol (99.5%, Sigma-Aldrich), isopropanol (99.5%, Sigma-Aldrich), 1H,1H,2H,2H-Perfluorodecanethiol (PFDT, 97%, Sigma-Aldrich), commercial copper / gold / nickel / zinc plating solutions (Plug N Plate Cu Solution, Plug N Plate Au Solution, Plug N Plate Ni Solution, Plug N Plate Zn Solution, Caswell Inc., USA), cadmium nitrate tetrahydrate ($Cd(NO_3)_2 \cdot 4H_2O$, 99%, Uni-chem), sodium thiosulfate pentahydrate ($Na_2S_2O_3 \cdot 5H_2O$, 99.5%, Sigma-Aldrich), hydrochloric acid (HCl, >37%, Sigma-Aldrich), manganese(II) acetate tetrahydrate ($Mn(CH_3COO)_2 \cdot 4H_2O$, 99%, Sigma-Aldrich), sodium sulfate (Na_2SO_4, 99%, Acros), pyrrole (98%, Sigma-Aldrich), potassium nitrate (KNO_3, 99%, Uni-chem), aniline (99.5%, Acros), sulfuric acid (H_2SO_4, 99%, Sigma-Aldrich), Norland Optical Adhesive 63 / 65 / 68 (NOA 63, NOA 65, NOA

68, Norland Products Inc., USA), methyl methacrylate (MMA, 99%, Sigma-Aldrich), 2,2′-azobis(2-methylpropionitrile) (AIBN, 99%, Sigma-Aldrich), 4-hydroxybenzophenone (4-HOBP, 98%, Sigma-Aldrich), ethylene glycol (EG, 99.8%, Sigma-Aldrich), N,N′-di(1-naphthyl)-N,N′-diphenyl-(1,1′-biphenyl)-4,4′-diamine (NPB, 99%, Sigma-Aldrich), tris(8-hydroxyquinolinato)-aluminium (Alq3, 99.995%, Sigma-Aldrich) lithium fluoride (LiF, 99.99%, Sigma-Aldrich), sodium chloride (NaCl, 99.5%, Sigma-Aldrich), polyvinyl alcohol (PVA, Mw 89,000-98,000, 99+% hydrolyzed, Sigma-Aldrich), lithium chloride (LiCl, 99%, Sigma-Aldrich), polyethylene terephthalate (PET, Suzhou Dawan Plastic Electronics Co. Ltd., China), ITO/PET (ITO-M1015, Zhuhai Kaivo Optoelectronic Technology Co., Ldt., China), adhesive tape (3M 810 Scotch Tape), commercial weighting paper, cotton cloth and nylon cloth, poly(3,4-ethylenedioxythiophene)-poly(styrenesulfonate) (PEDOT:PSS, Clevios™ PH 1000, Heraeous Epurio, Germany).

3.2 Fabrication of Templates for Electrodeposition

3.2.1 Fabrication of Templates through Photolithography

a) Etching Route

A 5-nm thickness of adhesive Cr layer and 25-nm Au layer were deposited by thermal evaporation on Si or SiO_2 substrate. Positive photoresist AZ 5214 was spin coated on the Au-coated substrate at 4000 rpm for 30 s. It was then pre-baked on a hotplate at 110 ℃ for 3 min. The photoresist was covered with as-designed photomask and exposed under UV light with dose of 40 mJ/cm^2 on a mask aligner

(MA6, SUSS MicroTec, Germany). It was then post-baked at 90℃ for 1 min. The photoresist was then developed in AZ 300 MIF developer for 70-80 s. The uncovered Au was then etched away in a mixed solution of pristine Au etchant and water at a 1:5 ratio for 60-120 s. The Au-pattern template was finally obtained after the photoresist was rinsed in acetone and ethanol and dried with compressed N_2.

b) Lift-off Route

The bare Si or SiO_2 substrate was spin coated with negative photoresist NR9-1500P at 4000 rpm for 40 s. It was then pre-baked on a hotplate at 155 ℃ for 1 min. The photoresist was covered with as-designed photomask and exposed under UV light with dose of 170 mJ/cm_2 on the mask aligner MA6. It was then post-baked at 105℃ for 3 min. The photoresist was then developed in DR6 developer for 10-15 s. The sample was rinsed in DI water and dried with compressed N_2. Subsequently, it was deposited with a 5-nm thickness of adhesive Cr layer and 25-nm Au layer by thermal evaporation. Finally, the photoresist and redundant deposited metals were washed away by acetone and ethanol.

3.2.2 Fabrication of Templates through Electron Beam Lithography

A bare Si substrate was spin coated with resist ZEP520A at 5200 rpm for 2 min. The patterning on resist was performed on EBL writer (JBX-9500FS Electron Beam Lithography System, JEOL Ltd., Japan). After post-baked at 180 ℃ for 3 min, the resist was developed in developer solution ZED-N50 for ~60 s. Subsequently, the sample was deposited with a 5-nm thickness of adhesive Cr layer

and 25-nm Au layer by thermal evaporation. Finally, the resist and redundant deposited metals were washed away by remover ZDMAC.

3.3 Electrochemical Replication and Transfer (ERT)

The as-fabricated Au-pattern template was immersed in 5 mM PFDT ethanol solution for 10-15 min to form a self-assembled monolayer on Au surface. The electrodeposition process could be carried out by two-electrode setup on source meter (Keithley 2400, Tektronix, Inc., USA) or three-electrode setup on electrochemical workstation (CHI 600e, CH Instruments, Inc., China). The surface modified Au-pattern template was used as working electrode. The counter electrode could be the dissolvable pure target material (such as Cu foil, Ni foil, or Zn foil) or noble platinum (Pt) foil. Ag/AgCl electrode was reference electrode. The details of electrodeposition solutions are listed in Table 3. After target material deposited on the template, it was rinsed by DI wafer and dried under compressed air.

The UV-curable polymers as binders used in the transfer step included NOA 63, NOA 65, NOA 68, and PMMA. For NOA 63, NOA 65 and NOA 68, these commercial products could be cast on the template directly and cured under 365-nm UV light with dose of more than 4,500 mJ/cm2. For PMMA, the liquid solution was mixed with MMA monomer, thermal initiator AIBN (0.2 wt.%) and photoinitiator 4-HOBP (0.2 wt.%). The mixed solution was firstly kept at 85 ℃ for 20 min to form a viscous oligomer liquid. This viscous oligomer liquid was then cast on the template and cured under UV light with dose of about 40, 000 mJ/cm2. Before the adhesive polymer was cured, a transparent PET layer was

covered on the top, which could help the adhesive polymer to be spread over the whole template by pressing and peel off the target material pattern from the template. After the target material pattern was transfer, the Au-pattern template was rinsed with DI water and ethanol for reuse.

Table 3. The electrodeposition solutions of eight target materials fabricated by ERT method.

Deposited material	Electrodeposition solution
Cu	Commercial Cu plating solution (Caswell, USA), mainly $CuSO_4$
Au	Commercial Au plating solution (Caswell, USA)
Ni	Commercial Ni plating solution (Caswell, USA), mainly $NiSO_4$
Zn	Commercial Zn plating solution (Caswell, USA), mainly $ZnCl_2$
Ag	Commercial Ag plating solution (Caswell, USA), mainly $AgNO_3$
CdS [140]	$Cd(NO_3)_2$, 0.05 M; $Na_2S_2O_3$, 0.025 M; pH~2 (HCl)
MnO_2 [141]	$Mn(CH_3COO)_2$, 0.01 M; Na_2SO_4, 0.02 M
PPy [142]	Pyrrole, 0.1 M; KNO_3, 0.3 M
PANi [143]	Aniline, 0.5 M; H_2SO_4, 1 M

The main components in Caswell plating solution were referred to the corresponding material safety data sheet (MSDS). The specific names and components in Au plating solution have been withheld as a trade secret. (https://www.caswellcanada.ca/MSDS.html)

3.4 Fabrication of Devices

Flexible Transparent Heaters (FTHs)

Metal (Cu) mesh was fabricated by ERT process on a template with size of 6.5 cm × 4.0 cm. The current density for electrodeposition was 2.0 mA/cm2 and deposition time was 20 min. The as-made Cu-mesh was a flexible transparent heater which could be heated up by voltage applied. The voltage on the two edges of Cu-mesh FTH was tuned by a DC power source and the temperature distribution of FTH was mapped by an infrared (IR) camera.

Touch Screen Panels (TSPs)

A Cu mesh with size of 6.5 cm × 4.0 cm was fabricated by ERT process with parameters of 2.0 mA/cm2 current density and 5 min deposition time. The touch screen panel (TSP) device for demonstration was assembled by using as-made Cu mesh-based FTE to replace the ITO@PET layer of a commercial TSP product. Four wire leads connected a controller to two edges of Cu mesh in vertical direction and two edges of ITO film in horizontal direction. The controller was connected to the personal computer. The commercial ITO-based TSP (TP177A, Siemens, Germany) and corresponding controller (STP-4500UG-G, Shenzhen Huiheng, China) were purchased online (www.taobao.com).

Organic Light-Emitting Diodes (OLEDs)

The structure of the organic light-emitting diodes (OLED) was: ERT-based Ni mesh/ PEDOT:PSS (120 nm) (anode)/ N,N′-di(1-naphthyl)-N,N′-diphenyl-(1,1′-biphenyl)-4,4′-diamine (NPB, 60 nm) (hole transport layer, HTL)/tris(8-hydroxyquinolinato)-aluminium (Alq3, 60 nm) (emitting layer and electron transport layer, EL&ETL)/lithium fluoride (LiF, 1 nm) /aluminium (Al, 100 nm)

(LiF/Al, cathode). Firstly, a Ni mesh was fabricated by ERT process with parameters of 2.0 mA/cm2 current density and 20 min deposition time. The Ni mesh was coated by the PEDOT:PSS (Clevios™ PH 1000) mixed with 5 wt.% ethylene glycol (EG) solution by spin coating with 3000 rpm for 60s. After annealed at 90 ℃ for 10 min, Ni mesh with PEDOT:PSS was used as hybrid electrode for OLED device. All the other layers (NPB, Alq3, LiF and Al) were deposited on the electrode by thermal evaporation.

Organic Electrochemical Transistors (OECTs)

Firstly, the gold source/drain electrodes were fabricated by ERT process. The Au electrode was coated by the PEDOT:PSS (Clevios™ PH 1000) solution (mixed with 5 wt.% ethylene glycol (EG)) by spin coating with 3000 rpm for 60s. After annealed at 120 ℃ for 30 min, a drop of 0.9 wt.% NaCl aqueous solution was dipped on the electrode, which was the electrolyte of the OECT device. Platinum (Pt) probe was gate electrode and stabbed in the electrolyte.

Micro-Supercapacitors (MSCs)

Firstly, a thin layer of Cu was electrodeposited on a template with Au interdigital electrode pattern under key parameters of 2.0 mA/cm2 current density and 2 min deposition time. Then a layer of Au was electrodeposited on top of deposited Cu layer with key parameters of 0.5 mA/cm2 current density and 20 min deposition time. The Cu/Au bilayer was transferred to PET substrate with binder NOA63. The thin Cu layer was on top of Au layer after transfer. A treatment with oxygen plamsa for oxidation on Cu layer was executed for ~5 min. Electrolyte was aqueous

solution of 10 wt.% PVA and 20 wt.% LiCl, which was cast on Cu/Au interdigital electrode and dried in the air.

3.5 Characterization and Techniques

Optical microscopic (OM) images were obtained on an optical microscope (Eclipse 80i, Nikon, Japan) with magnifications from 50× to 1000×.

Scanning electron microscopy (SEM) images were acquired on a field emission scanning electron microscope (FE-SEM, JSM-6335F, JEOL, Japan).

Atom force microscope (AFM, XE-100, Park Systems, Korea**)** was used to characterize the topography (line width, thickness, 3D view morphology, and surface roughness) of patterns.

X-ray diffraction (XRD) patterns were collected on an X-ray diffractometer (Rigaku SmartLab 9 kW, Japan) with a Cu Kα X-ray source.

Raman spectra were recorded on Raman microscope (Nomadic™ 3-in-1, BaySpec, USA), using 532 nm laser.

Fourier transform infrared (FTIR) spectra were obtained on a FTIR spectrometer (Spectrum 100, PerkinElmer, USA).

X-ray photoelectron spectroscopy (XPS) data were collected on X-ray photoelectron spectrometer (ESCALAB 250, Thermo Scientific, USA).

Contact angle (CA) was characterized on an optical contact angle measuring device (SDC-350, Dynetech, Inc., China) by dropping DI water on sample surface.

Force vs. extension curve was recorded on a tensile strength tester (Instron 4411, Lab World Group, USA).

Sheet resistance (R_s) was tested by four-probe method using a source meter (Keithley 2400 SourceMeter, Tektronix, Inc., USA).

Optical transmittance (T) was recorded on a UV-vis spectrometer (Cary 300, Varian, USA).

Bending tests were conducted on a stepper motor linear stage (TSA50-C, Zolix, China).

Adhesion tests were performed by using commercial tape (3M Scotch Magic, USA).

Temperature and IR images were recorded on an IR camera (E4, FLIR, USA).

The current density-voltage-luminance (J-V-L) characteristics of OLED was performed on a Keithley 2400 SourceMeter and a spectroradiometer (SpectraScan® PR-650, Photo Research, USA).

The transfer and output characteristics of organic electrochemical transistor (OECT) were recorded on a four-probe station with analyzer (Micromanipulator Probe station 450PM-B with Keithley 4200-SCS Semiconductor Parameter Analyzer, USA).

Electrochemical performance of micro-supercapacitor was characterized on an electrochemical workstation (CHI 600e, CH Instruments, Inc., China).

Chapter 4: Electrochemical Replication and Transfer (ERT)

In this chapter, a new patterning technique, termed electrochemical replication and transfer (ERT) will be introduced in detail on its fabrication process. Then the results based on this alternative patterning technique will show on its applicability to a wide variety of geometric patterns, target materials, and flexible substrate. The comparison of ERT with typical conventional patterning techniques (in terms of resolution, throughput, and cost) is also illustrated at the end.

4.1 Fabrication Process of ERT Method

The detailed fabrication process of ERT is schematically illustrated in Figure 19 and Figure 20. The reusable template was pre-made with traditional lithography routes such as photolithography and electron beam lithography (EBL). As a proof-of-concept, we demonstrated the ERT process using a 4-inch Au-patterned Si template (25 nm thick Au with a 5 nm of Cr as the adhesive layer, as characterized by AFM in Figure 20A), which was comprised of multiple patterns of different shapes and sizes (Figure 19B). A self-assembled monolayer (SAM) of 1H,1H,2H,2H-perfluorodecanethiol (PFDT) was modified on the surface of Au, which serves as the anti-adhesive release layer to facilitate the transfer of materials at the final step and to improves the reusability of the Au template. The SAM-modified Au-patterned template was immersed in the specific electrodeposition solution to execute the electrochemical replication of target material (target

material is Cu in Figure 19C and Figure 20B). It is the difference of conductive property between conductive Au layer and semiconducting Si substrate that enables the target material to be site-selectively electrodeposited on the region of Au pattern. Subsequently, a layer of flexible substrate (poly(ethylene terephthalate), PET) with photo-curable binder (Norland Optical Adhesive 63, NOA 63) was covered on the whole template. After the binder was cured under UV light, the as-deposited target material pattern was peeled off and attached on the target flexible substrate (top in Figure 19D and Figure 20C), leaving the Au-patterned template for reuse in the following many fabrication cycles (bottom in Figure 19D). The Cu pattern is embedded in the target substrate. This embedded structure significantly decreases the surface roughness of this kind of material, which is advantageous to be integrated in some practical devices, such as solar cell, organic light-emitting diode, etc.

Based on the results characterized by AFM, the minimum linewidth of Au line fabricated by photolithography route can research ~400 nm through deep developing and excessive etching (Figure 20A). After electrochemical repletion, Cu material was deposited on the Au pattern. The minimum linewidth of Cu line was ~500 nm. The growth thickness of Cu line was ~50 nm. We can infer that the reason of the increasing of linewidth is the isotropic phenomenon during electrodeposition. The minimum half pitch of pattern on the template obtained by lab-level photolithography system is 2 μm. Therefore, the half pitch of pattern fabricated by ERT based on this template is limited at 2 μm. To further investigate the higher resolution of ERT technique, templates with higher resolution can be prepared through other patterning techniques, such as electron beam lithography (EBL).

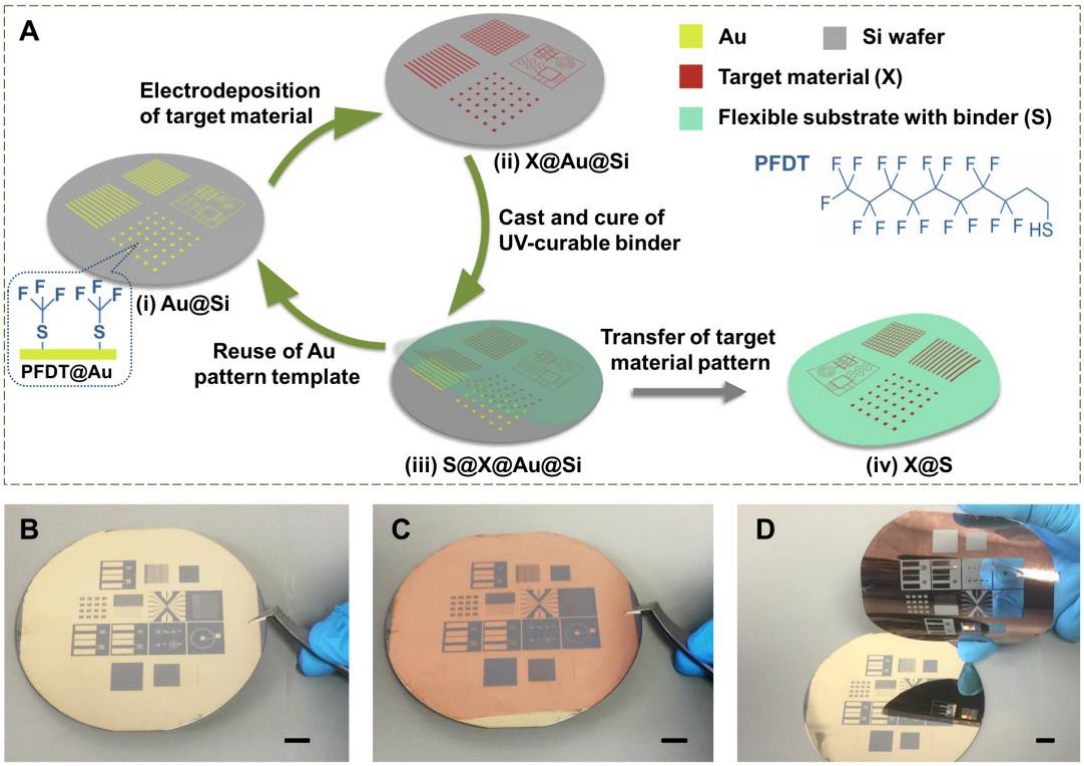


Figure 19. Fabrication process of electrochemical replication and transfer (ERT) method. (A) Schematic diagram of ERT method. (B-D) Wafer-scale demonstration of copper (Cu) pattern fabricated by ERT process. (B) Thin gold (Au) pattern on silicon (Si) wafer used as reusable template in ERT method. (C) Cu pattern obtained through electrochemical replication step, where Cu selectively electrodeposited on Au pattern. (D) Cu pattern transferred into flexible substrate PET with UV-curable binder (NOA 63), and the undamaged Au-pattern template reused for next fabrication cycle. Scale bars, 1 cm.

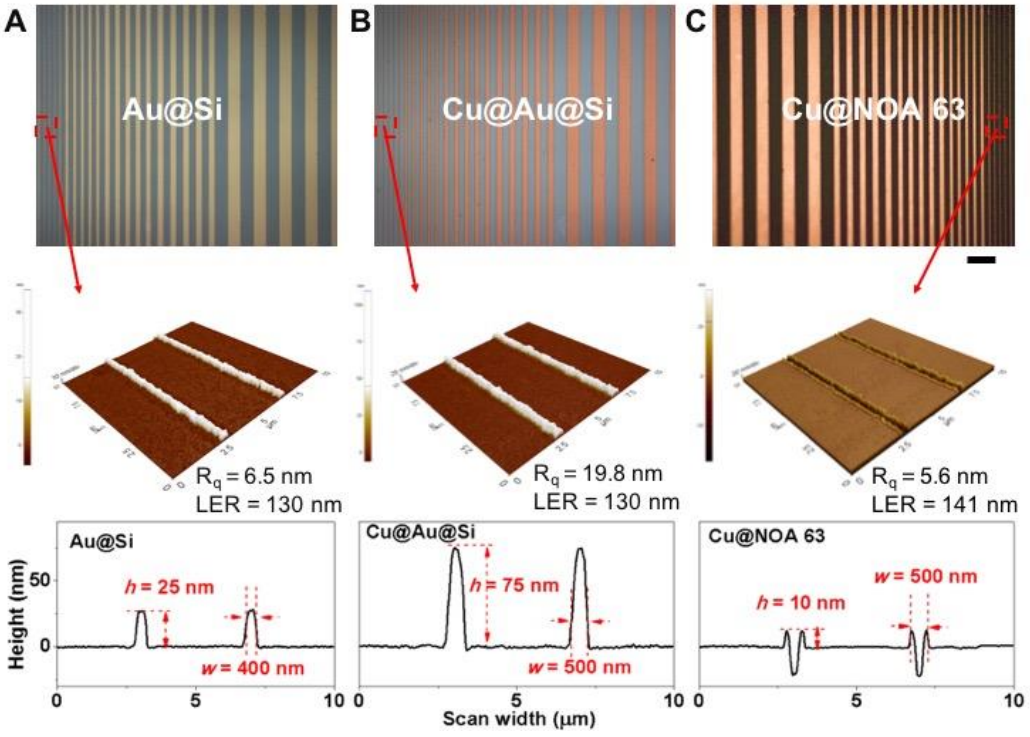


Figure 20. Characterization of ERT process based on the parallel-line patterns with differernt linewidths. Top, optical microscopic images. Middle, 3D images of topographic images characterized by AFM. Bottom, the profiles of pattern lines during ERT process. (A) Au-pattern template (Au@Si). Height of Au is about 25 nm. Linewidth is about 400 nm. (B) Cu deposited on Au-pattern template (Cu@Au@Si). Thickness of deposited Cu is about 50 nm (by subtracting 25-nm thickness of Au layer from the overall 75-nm thickness). Minimum linewidth is about 500 nm. Current density, 2 mA/cm2. electrodeposition time, 1 min. (C) Cu pattern transferred into the NOA 63 binder on PET substrate (Cu@NOA 63). Height of transferred Cu line based on the NOA 63 surface is about 10 nm (mostly embedded in the NOA 63). Linewidth is about 500 nm. The phenomenon of Cu embedded in the NOA 63 can significantly reduce the surface roughness, where root-mean-square roughness (R_q) is reduced to 5.6 nm from 19.8 nm. Line edge roughness (LER) is one of the key issues in patterning techniques. The LER of pattern fabricated by ERT is almost comparable to that fabricated by

photolithography. The increasing of LER in ERT is mainly because of the Cu growth at the directions of the sidewalls. Scale bar, 20 μm.

For the fabrication of Au pattern on template, in principle all the conventional lithography or printing strategies can be used to achieve this requirement. In addition to the above data based on the templates fabricated by photolithography, the results shown in Figure 21and Figure 22 indicate that EBL route can be used to fabricate the Au-patterned templates for the ERT process. We can EBL process to fabricate high-resolution nanoscale Au-patterns for the ERT-method and further use ERT process to prepare high-resolution ERT-based patterns. As shown in Figure 21 and Figure 22, the half pitches of dot arrays and parallel lines on the templates are all 250 nm. The half pitches of Cu patterns fabricated by ERT are also confined at 250 nm. By tuning the parameters of electrodeposition, the minimum diameter of Cu dot can reach about 200 nm (Figure 21) and the minimum linewidth and gap between the parallel lines can achieve 200 nm and 50 nm respectively (Figure 22, B-F). These ERT-based nanoscale patterns fabricated based on EBL-based templates further indicate that ERT method is a high-resolution patterning technique.

Since the Au-patterned template can be reused for many times in the ERT process, these tedious patterning processes for Au patterns on templates by photolithography or electron beam lithography only need to be executed for one time. The ERT process only consists of two facile steps, which are accomplished in ambient condition with ultralow cost. It significantly simplifies the generation of high-resolution pattern. Therefore, we can conclude that ERT is a cost-efficient patterning technique for high-resolution patterns with large scale.

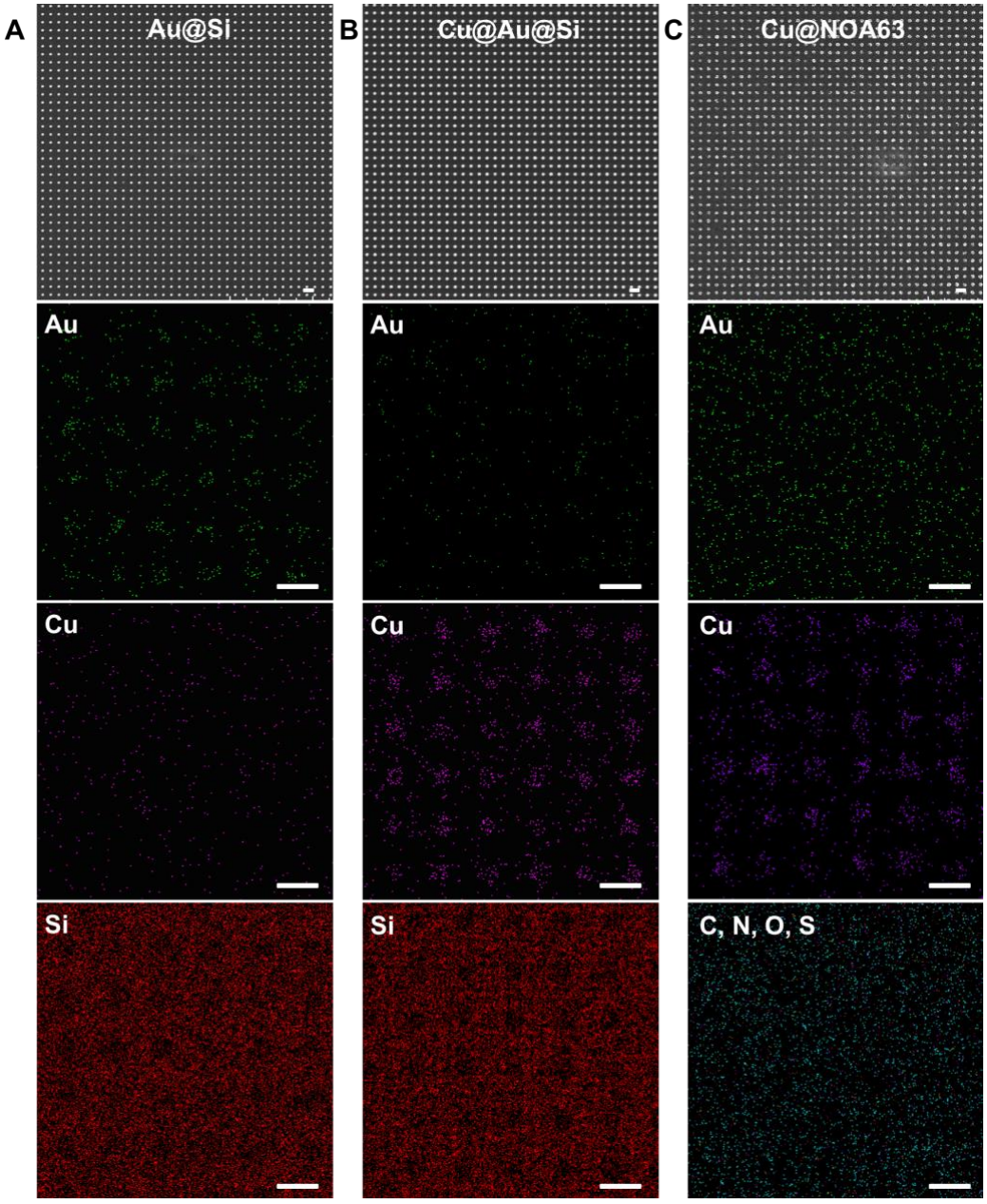


Figure 21. High-resolution dot-array patterns fabricated by ERT process. Nanoscale Au-patterned templates prepared by EBL process and the ERT-based Cu patterns fabricated on these templates. Left, Au-patterned templates prepared by EBL process. (A) SEM images and EDS analysis of Au-patterned template prepared by standard EBL process. Diameter of Au dot, 150 nm. Pitch of dot array,

500 nm. (B) Electrochemical replication of Cu nanodot array on EBL-based template. EDS result indicates that Cu materials are site-selectively electrodeposited on the Au-pattern regions. Current density, 1.5 mA/cm2. Deposition time, 30 s. Diameter of electrochemically-replicated Cu dot, 200 nm. (C) Transfer of Cu dot-array pattern on the PET/NOA 63 substrate. SEM image and EDS result show that Cu nanodot array is transferred successfully into the NOA 63. The EDS signal of Au becomes strong, because a thin layer of Au was deposited on the sample surface for SEM observation. Diameter of transferred Cu dot, 200 nm. Scale bar (pitch of dot array): 500 nm.

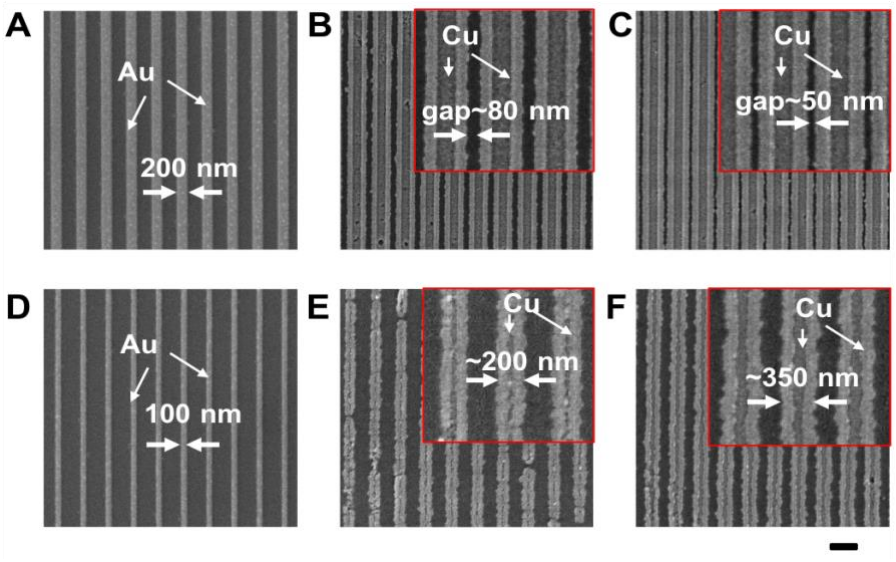


Figure 22. High-resolution parallel-line patterns fabricated by ERT process. Nanoscale Au-patterned templates prepared by EBL process. Left, Au-patterned templates prepared by EBL process. Linewidth of Au line, (A) 200 nm; (D) 100 nm. Middle and right, ERT-based Cu patterns obtained through different current densities. (B and E), 1.6 mA/cm2. (C and F) 1.7 mA/cm2. Electrodeposition time, 1 min. The minimum linewidth of Cu is about 200 nm. The minimum gap between Cu lines is about 50 nm. Half pitch in all patterns, 250 nm. Scale bar, 500 nm.

ERT process fabricates pattern of target material directly within two steps, which is superior than conventional lithography with multiple steps (Figure 23). In conventional lithography process, either etching or lift-off route, the pattern is generated on a layer of resist firstly. Then pattern on the resist layer is transferred to the target material. Target materials are deposited on the whole substrate firstly and then removed the unwanted regions to achieve the pattern. This subtractive process involves multiple and tedious steps, resulting in a lot of consumption of materials and time. In contrast, ERT process creates patterns of target materials directly through additive manufacturing, which significantly simplifies the fabrication steps and decreases the cost.

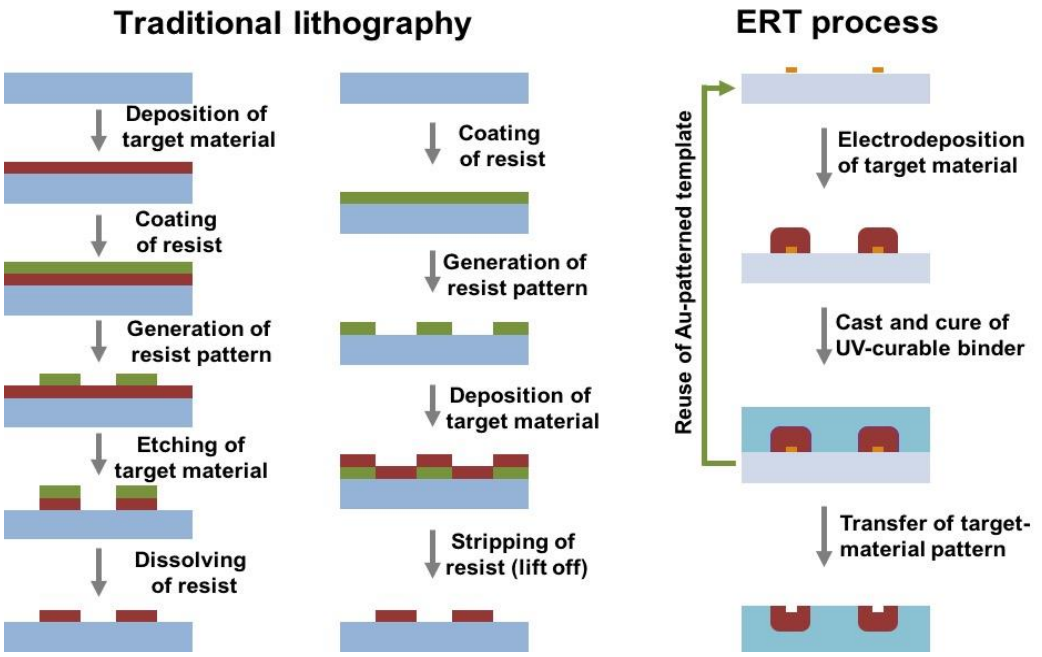


Figure 23. Comparison of traditional lithography and ERT process. In traditional lithography, the pattern of target material cannot be obtained directly. A pattern of resist is formed firstly. Then the target material pattern is transferred from the

pattern on resist layer through etching or lift off process. In ERT process, the pattern of target material is replicated on the template directly, without resist assistance and redundant material.

4.2 The Wide Applicability of ERT Method

As a proof-of-concept, the above samples demonstrate ERT process based on parallel-line pattern of Cu material on PET substrate. In principle, ERT method is widely applicable to a wide variety of geometric patterns, target materials, and target substrates. The following results will prove the wide applicability of ERT method.

4.2.1 ERT Method Applicable to Various Geometric Patterns

As aforementioned, we demonstrated the ERT process by fabricating a 4-inch Cu-patterned sample which was comprised of multiple patterns of different shapes and sizes. The morphology of each pattern on this wafer-scale Cu sample is shown in Figure 24. Pattern 1 and pattern 2 are percolation meshes, which can be used as flexible transparent electrodes (FTEs). Pattern 3 is spiral line, which is the basic structure of radio frequency identification (RFID) for wireless communication in the Internet of Things (IoT). Pattern 4, pattern 5, and pattern 6 are interdigital electrodes with different linewidths and gaps. These interdigital electrodes show a wide variety of applications, such as micro-supercapacitor, sensor, etc. Pattern 7 and pattern 8 are interconnection circuits, which are comprised of straight lines, serpentine lines, squares, circles, spiral lines, interdigital electrodes, etc. Pattern 9

and pattern 10 are positive and negative patterns with different linewidths and gaps, which are usually used to investigate the resolution. Pattern 11 is serial electrodes separated by gaps, which can be used as source/drain electrodes in the structures of various transistors. Pattern 12, pattern 13, and pattern 16 are typical isolated shapes, such as triangle, pentagram, logo of The Hong Kong Polytechnic University, letter of Cu, etc. Pattern 14 and pattern 15 are parallel lines with different linewidths and gaps.

Since the electrochemical replication on the template is a parallel process, it is remarkable that all these patterns, with different shapes, different linewidths and different gaps, can be fabricated on one substrate simultaneously. In other words, ERT can fabricate large-scale patterns with resolution ranging from several hundred nanometer to several centimeter through the same facile process. The resolution, throughput, and cost of this patterning technique are independent to each other.

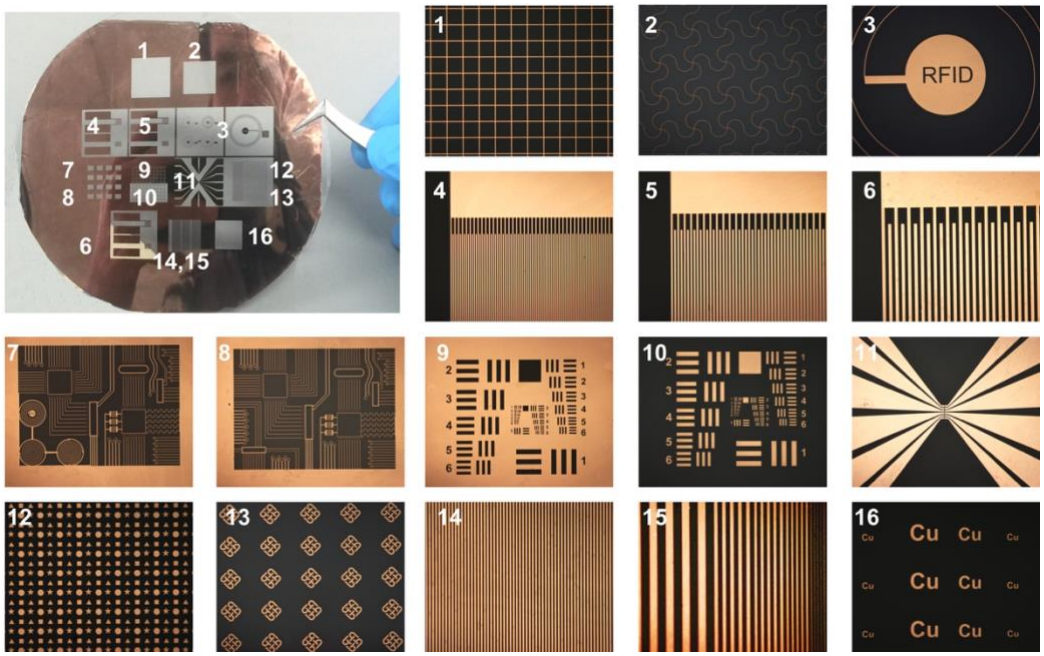


Figure 24. ERT method applicable to various geometric patterns. Top left corner, the digital image of a 4-inch wafer-scale Cu pattern fabricated by ERT method. Others, optical microscopic images of morphologies of each pattern marked on the digitial image.

4.2.2 ERT Method Applicable to Various Materials

On the other hand, ERT is applicable to a wide variety of materials. The basic principle of electrochemical replication is the conventional electrochemical deposition. Therefore, as long as the material can be synthesized by electrochemical deposition (such as electroplating, electropolymerization), it can be integrated in the ERT process. We herein demonstrated the ERT method applicable to eight typical materials, including metals (Cu, Au, Ni, and Zn), metal oxide (MnO_2), metal sulfide (CdS, semiconductor material), and polymers (PPy, PANi, conductive polymers), whose shapes are shown by their own chemical

names, respectively (Figure 25). Through ERT method, these eight materials could be successfully electrochemical replicated on the pre-prepared Au-patterned templates and transferred to target substrates, respectively. The electrodeposition parameters were referred to those typical routes (Table 3). The corresponding chemical characterization (including XRD, FTIR and Raman spectrum) of these eight materials further confirmed their synthesizing success based on ERT method (as shown in Figure 26). The XRD data indicate that these electrodeposited materials are polycrystals. The applicability of ERT method to a wide variety of materials indicates the wide potential applications based on this new patterning technique.

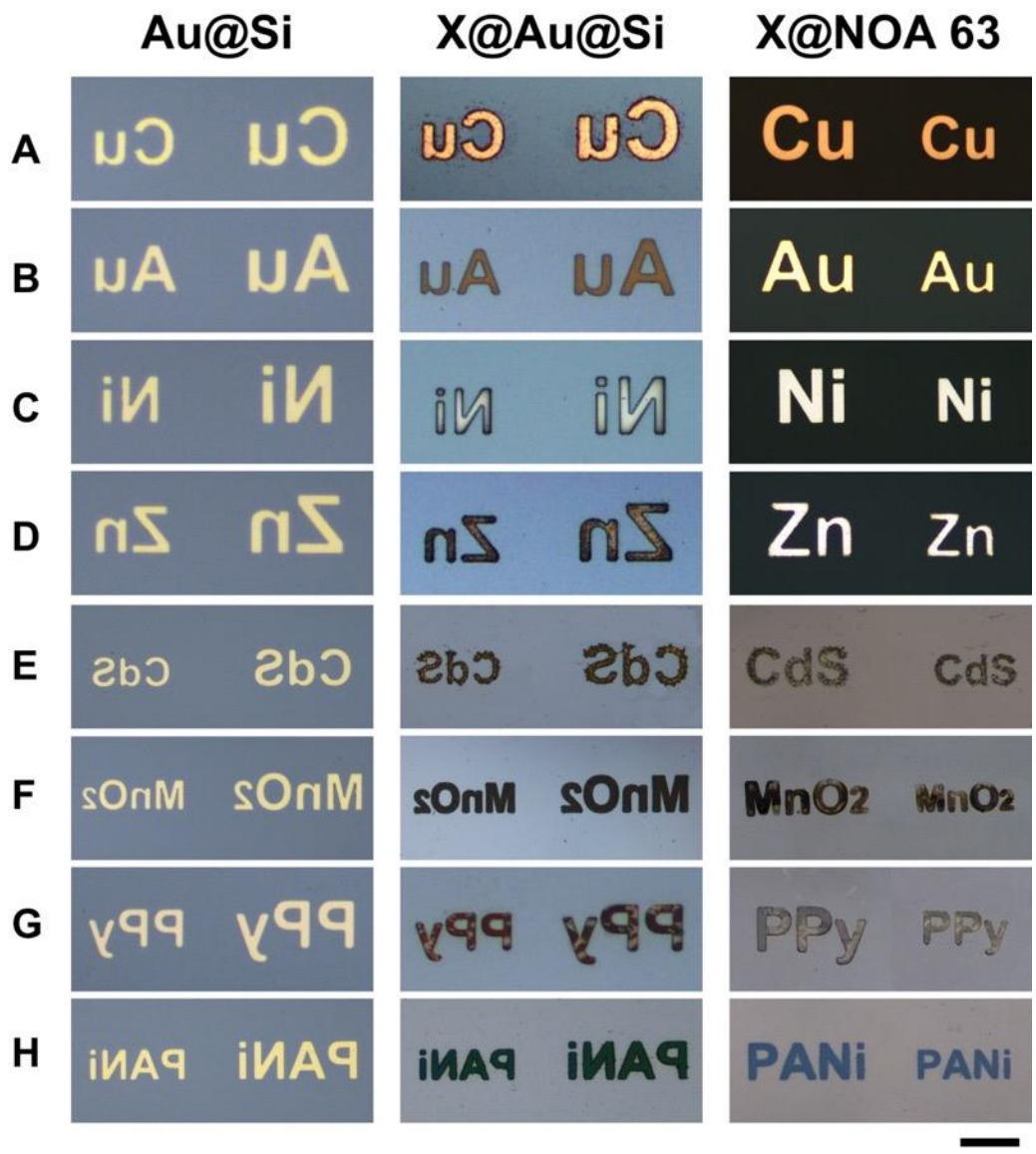


Figure 25. Optical microscopic images of different patterns based on eight materials during ERT process. Left, Au-patternd templates (Au@Si). Middle, different target materials deposited on the Au-patterned templates (X@Au@Si). Right, different target material patterns transferred into the NOA 63 binder (X@NOA 63). (A) Cu, (B) Au, (C) Ni, (D) Zn, (E) CdS, (F) MnO_2, (G) PPy, (H) PANi. Scale bar, 100 μm.

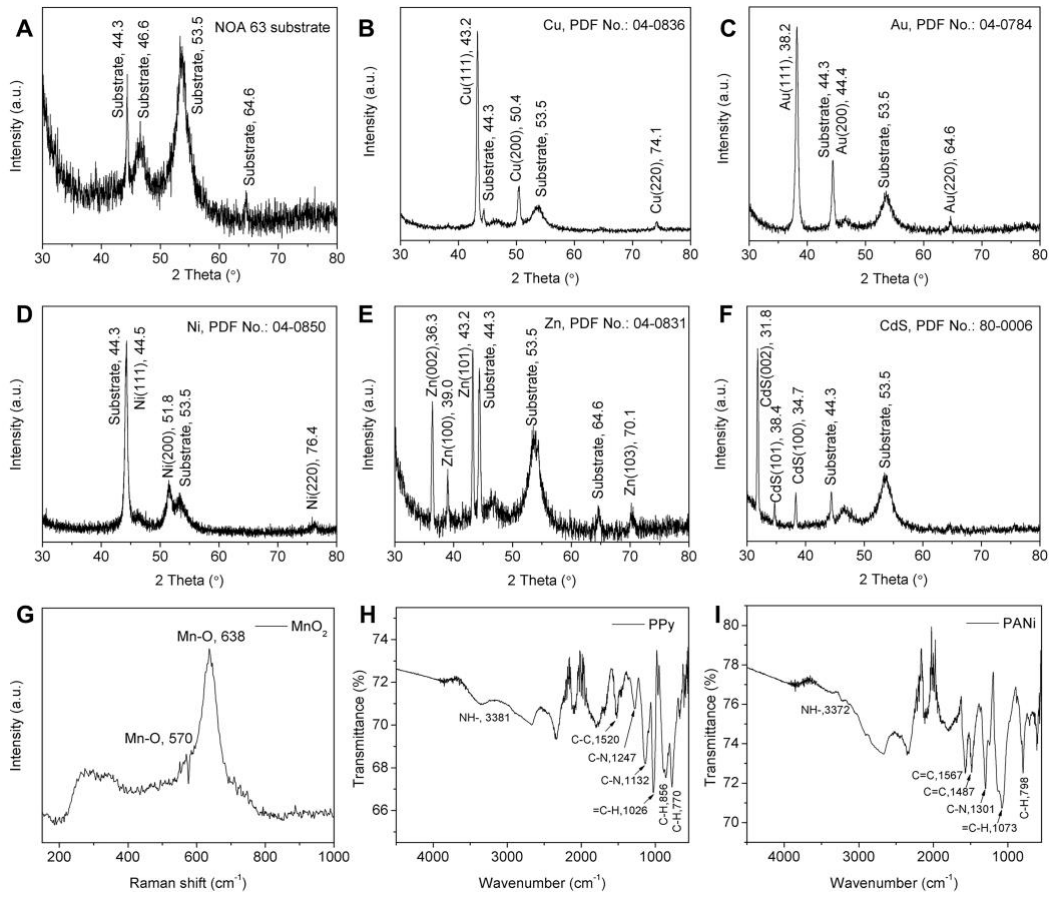


Figure 26. Characterization of eight materials fabricated by ERT method. XRD patterns of (A) NOA 63, (B) Cu, (C) Au, (D) Ni, (E) Zn and (F) CdS. Raman spectrum of (G) MnO_2. FTIR spectra of (H) PPy and (I) PANi.

4.2.3 ERT Method Applicable to Various Substrates

More importantly, patterns based on ERT process could be transferred on a wide variety of substrates. As a proof-of-concept, four typical substrates, i.e., PET, paper, cotton and nylon clothes (as shown in Figure 27), are used as the target substrates in the ERT process. By controlling other parameters, including the same Cu as deposited material, current density, deposition time, and NOA 63 as binder, four

groups of experiments with different target substrates are all successful to implement the ERT process. The successful integration of different flexible and wearable substrates in ERT process indicates the widely potential applications in flexible and wearable devices based on this alternative patterning technique.

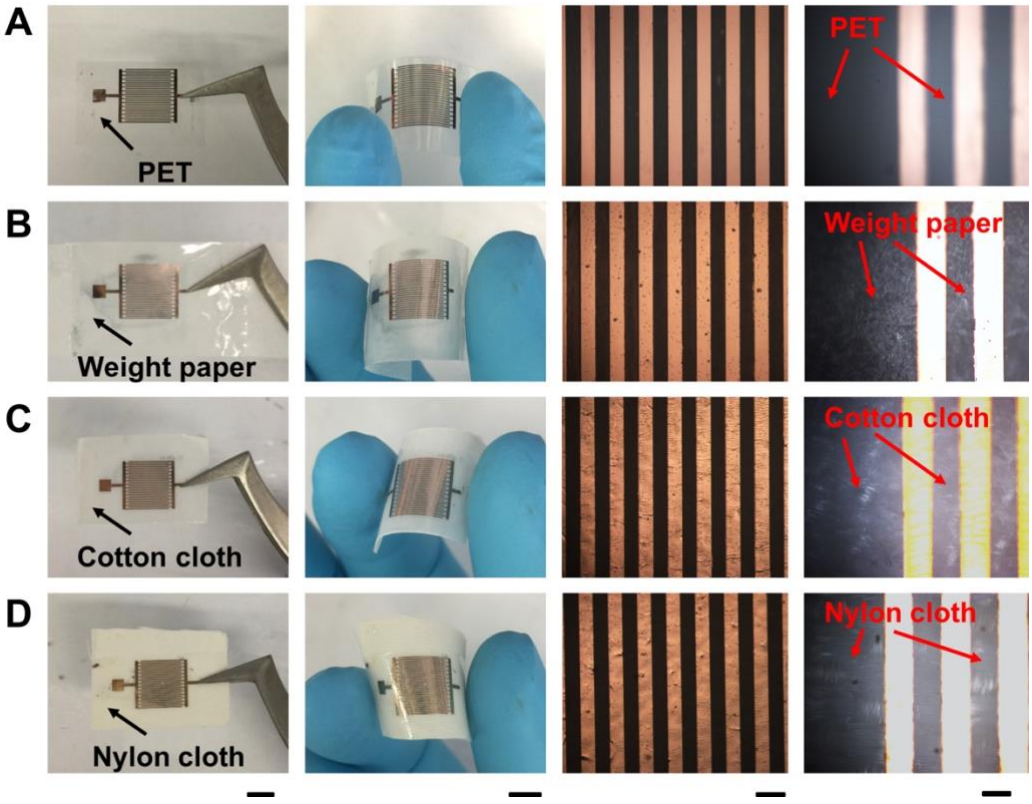


Figure 27. ERT method applicable to various flexible and wearable substrates: (A) PET, (B) paper, (C) cotton cloth, and (D) nylon cloth. UV-curable binder for four cases are all NOA 63. Current density, 2 mA/cm2. Electrodeposition time, 10 min. The first column: flat state. Scale bar, 5 mm. The second column: bending state. Scale bar, 5 mm. The third column: optical microscopic images of Cu pattern on different flexible substrates. Scale bar, 300 μm. The fourth column: optical microscopic images focusing on the surfaces of four flexible substrates. Scale bar, 150 μm.

4.3 Comparison of ERT Method with Conventional Patterning Techniques

Based on the literature review (especially data in Table 2 and Figure 18) and the results of ERT, a comprehensive summary and comparison of ERT method with typical conventional patterning techniques are illustrated in this section. ERT as an alternative patterning technique can fabricate arbitrary multiple patterns with different feature sizes spanning from sub-100 nm to μm on the wafer-scale flexible substrate within minutes with ultra-low cost. As shown in Table 4, the data of resolution of 7 nm for photolithography and 5 nm for electron beam lithography are obtained from the rigid Si electronics. Direct photolithography on flexible plastic substrates cannot reach such high resolution. Because of charge accumulation on isolating substrate, the resolution of EBL is also limited on flexible substrates. In the flexible electronics, the resolutions based on these patterning techniques are still lower than those on rigid substrates. In 2018, K. Myny proposed the concept of a Moore's law for flexible electronics, with minimum feature size of 200 nm.[144]

For throughput, it is generally accepted that the high-volume-manufacturing techniques show throughput of more than 100 wafers per hour (WPH, 36 s for 1 wafer) corresponding to >1 m^2/h.[94] In photolithography, only the bottleneck step, i.e. UV exposure step, is taken in account for calculation of its throughput. For ERT process, the bottleneck step is electrodeposition. To calculate its throughput, 1-2 min can finish 1 wafer (30-60 WPH) in 1 electrodeposition bath. Since the equipment cost and power consumption (mA scale current and 0.5-5 V voltage) are ultralow in ERT process, the practical production line can consist of 10-100 or

even more clustered, parallel electrodeposition baths. A conservative estimate of maximum throughput of ERT can reach 10^2 m^2/h.

The cost of patterning process involves the cost of capital equipment, fabrication environment, material consuming, power consuming, etc. As the capital cost is an easily-quantified factor, the capital cost of patterning equipment is used for comparison in term of cost. According to the introduction of equipment costs in Chapter 2, these five typical patterning techniques (photolithography, EBL, NIL, inkjet, and screen printings) all require high-cost tools, especially the exposure system for EUV lithography (~100M $). In contrast, the capital equipment of ERT process is the ordinary direct current (DC) power supply. In our experiment, we carried out electrodeposition on a source meter (Keithley 2400, Tektronix, Inc., USA), with cost of ~3k $. In practical production, the cost of DC power equipment can be much lower.

The consumptions of materials in ERT process mainly involve the target materials, electrodeposition solutions, and photo-curable binders. Taking the deposition of Cu as the example, pure Cu foil is used as the counter electrode and its cost is ultralow (<1 $ for 0.01 × mm × 100 mm × 1 m pure Cu foil, purchased on taobao.com). Since the counter electrode Cu will dissolve in the plating solution during electroplating process, the commercial Cu plating solution will keep constant according to the law of charge conservation, indicating the plating solution will be reused for a long time. For the amount of photo-curable binders used in ERT process, as long as the thickness of binder layer is higher than that of the layer of as-deposited target materials, it will be enough to facilitate the transfer

step. Considering the binder layer with 10-μm thickness, which is thicker than those of most deposited materials, 10-cm^3 binder is able to cover on 1-m^2 surface of substrate. The commercial binder NOA 63 with 30 cm^3 purchased on norlandprod.com is 37 $, which can be used to fabricate ~3 m^2 of ERT samples. Compared with the cost of consumptions used in photolithography (such as photoresist, developer, target materials, etc.), the cost of ERT is much lower. Furthermore, this all-solution, resist-free patterning technique generates patterns by additive mode within two facile steps, which further decreases the cost in terms of consumptions of materials and time.

More importantly, the resolution, throughput, and cost of ERT are independent to each other. Patterns with feature sizes of either sub-100 nm or micrometer scale can be all finished on small or large size substrates. There is no significant difference in terms of equipment requirement and fabrication conditions to fabricate different types of patterns. The achievement of high resolution does not result in low throughput or high cost. In contrast, for the five typical conventional patterning techniques, the high resolution is usually accompanied with relatively low throughput or high cost. Figure 28 describes this difference by using titled ellipses for the dependent phenomenon in traditional patterning techniques and un-titled ellipses for the independent phenomenon in ERT.

In summary, ERT is a high-resolution, high-throughput, and low-cost patterning technique, which bridges the research gap in the field of conventional patterning techniques. Remarkably, the resolution, throughput, and cost of ERT are independent to each other.

Table 4. Comparion of ERT method with typical conventional patterning techniques.

Patterning technique	Resolution (μm)	Throughput (m^2/h)	Capital cost of equipment ($)
Photolithography	0.007-10	10^{-2}-1	1M-100M
E-beam lithography (EBL)	0.005-0.1	10^{-6}-10^{-3}	1M-5M
Nanoimprint lithography (NIL)	0.01-1	10^{-5}-1	500k-5M
Inkjet printing	20-100	10^{-2}-10	10k-50k
Screen printing	30-100	1-10^{3}	1k-1M
Electrochemical replication and transfer (ERT)	**0.05-100**	**10^{-1}-10^{2}**	**1k-10k**

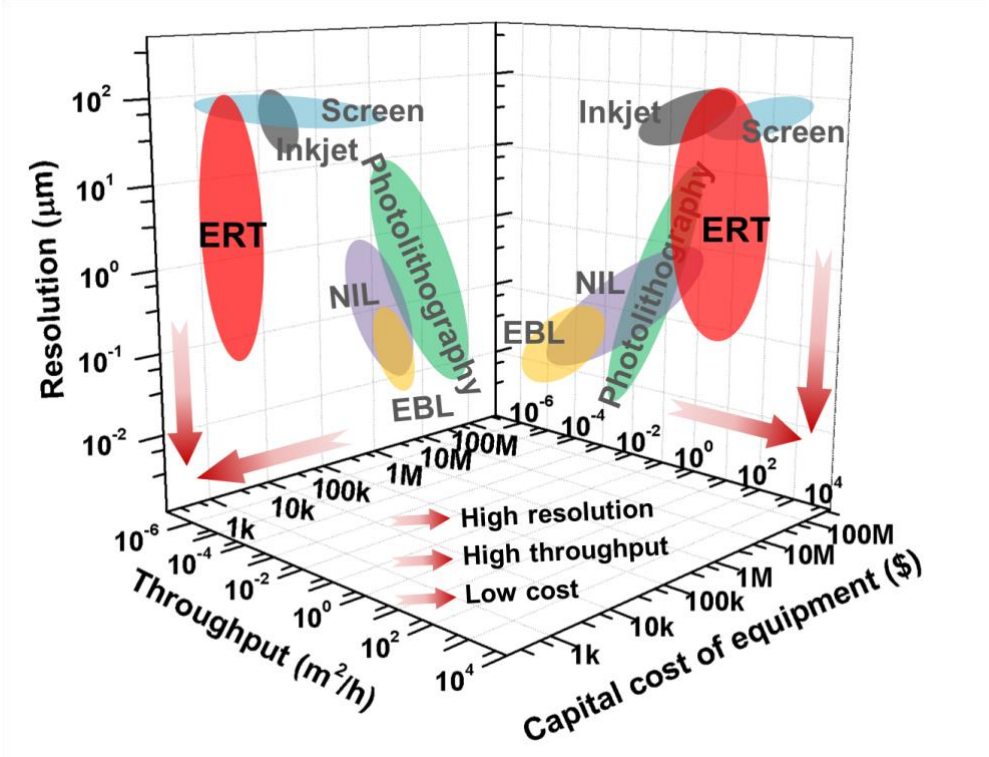


Figure 28. Comparion of ERT method with typical conventional patterning techniques (based on the data in Table 4). ERT bridges the research gap on the high resolution, high throughput, and low cost in the field of conventional patterning techniques. Titled ellipses for the dependent phenomenon in traditional patterning techniques and un-titled ellipses for the independent phenomenon in ERT.

4.4 Conclusions

Electrochemical replication and transfer (ERT) as a new patterning technique has been developed successfully. This alternative patterning technique fabricates multi-scale patterns by two facile steps, i.e., selective electrodeposition of target materials on a pre-defined template (first step: electrochemical replication), and subsequent transfer of the electrodeposited materials to a flexible substrate with a

photo-curable binder (second step: transfer). The additive and parallel patterning attribute of ERT allows to fabricate multi-scale patterns with resolutions spanning from sub-100 nm to micrometer scale simultaneously, which overcomes the tradeoff among the resolution, throughput and cost of conventional patterning techniques. Furthermore, ERT shows the wide applicability in terms of geometric patterns (arbitrary patterns), target materials (metals, metal oxides, semiconductors, conductive polymers), and flexible substrates (plastics, papers, textiles).

Chapter 5: Mechanism Analysis of ERT Process

Electrochemical replication and transfer (ERT) method only consists of two main steps: (1) electrochemical replication and (2) transfer. In this chapter, the mechanism of ERT process will be analyzed based on the strategies towards the success of these two steps respectively. When the original idea of ERT was created, the rational structure of template and optimization of electrodeposition parameters were two essential factors in the step of electrochemical replication and the functions of surface modification and UV-curable binder played important roles in the step of transfer.

5.1 Electrochemical Replication

5.1.1 Rational Structure of Au-Patterned Template

The structure of Au-patterned template is rationally designed to achieve the purpose of selective electrodeposition. Generally, the structure of template is a thin conductive Au layer deposited on the semiconductor substrate. This conductive-semiconductor architecture enables the target materials to be deposited selectively on the Au pattern region only.

In order to prove the hypothesis above, four kinds of templates were designed and used in the ERT processes (Figure 29). In these four kinds of templates, Au layers

are all the same in terms of pattern shape, size, and thickness (~25 nm, characterized by AFM in Figure 30). Si is semiconductor substrate and SiO_2 is non-conductive substrate. A thin chrome (Cr) layer is usually used as the adhesive layer to enhance the adhesion between the upper layer and substrate. On the other hand, Cr is easily oxidized in the air on its surface (Figure 31),[145] which makes Cr layer become a semiconductor layer (explanation in Table 5 and Table 6). Therefore, Cr layer is also acted as the semiconductor layer either on Si or SiO_2 substrate in this research.

Si and Cr with oxidation layer show semiconductor property. We evaluated three kinds of substrates with semiconductor materials for the ERT-templates: i) Si wafer, ii) Cr/Si, and iii) Cr/SiO_2 (Cr layer with native oxidation surface). The sheet resistances (R_s) of these semiconductor layers show at least two order higher than that of conductive Au layer (as shown in Table 6). The R_s difference between semiconductor substrate and conductive Au layer can ensure the success of selective electrodeposition on the region of Au pattern. As shown in Figure 29, Cu materials are all successfully electrodeposited on the Au patterns and transferred into NOA 63. The non-conductive SiO_2 substrate is used as the control group. As shown in Figure 29, Cu materials are not seen on the Au-pattern template after electrodeposition performed, because the SiO_2 with isolated Au pattern results in an open circuit which makes the electrodeposition impossible.

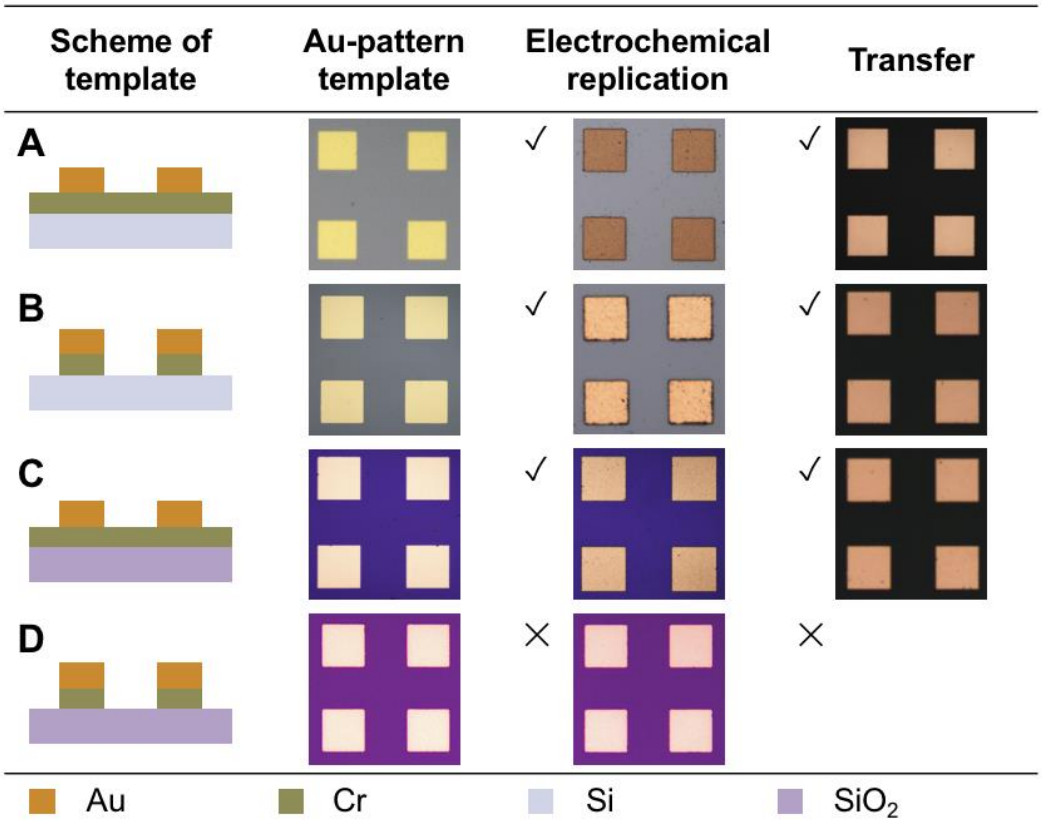


Figure 29. Four typical Au-pattern templates used for ERT method and the corresponding as-made Cu patterns. Semiconductor materials used as substrates of the Au-pattern templates: (A) Cr/Si; (B) Si; (C) Cr/SiO_2. Cu materials can be site-selectively electrodeposited on these kinds of Au-pattern templates and transferred to the NOA 63. As the control group, non-conductive material as the substrate of the Au-pattern template: (D) SiO_2. Cu material cannot be deposited on this kind of template. Templates in (A) and (C) fabricated by etching stategy. Templates in (B) and (D) fabricated by lift-off process. Current density, 2.0 mA/cm^2. Electrodeposition time, 5 min.

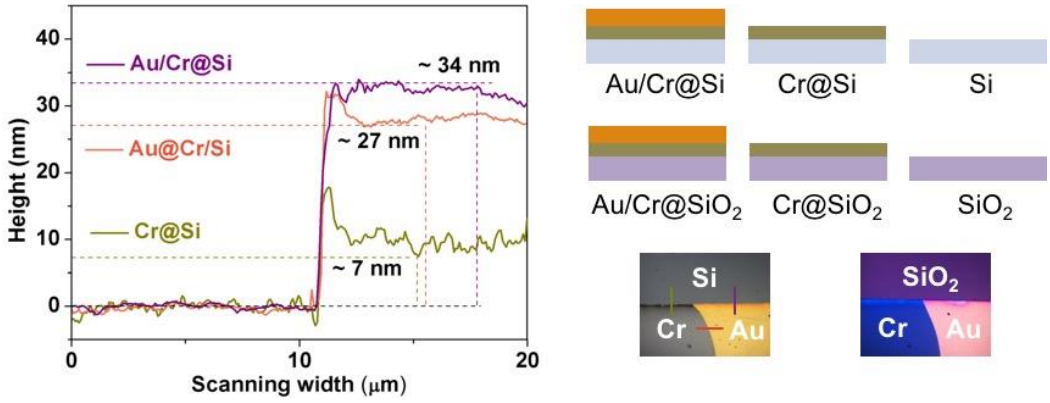


Figure 30. AFM characterization of the thickness of thermal evaporated Au and Cr layers. Left, AFM characterization of the thickness of Au and Cr layers on the Si or SiO_2 substrate. Top right, the schematic illustration of Au/Cr and Cr layers on the Si and SiO_2 substrates, respectively. Bottom right, the optical microscopic images of Au/Cr and Cr layers on the Si and SiO_2 substrates, respectively.

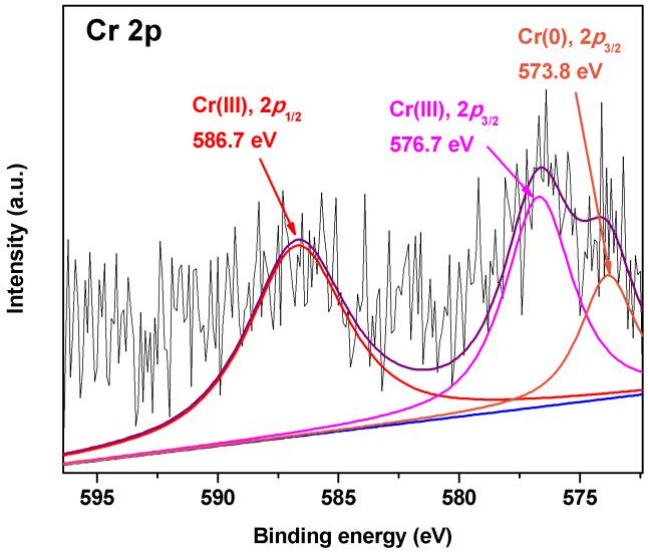


Figure 31. XPS characterization of the phenomenon of native oxidation on Cr surface.[145]

Table 5. The resistivities (ρ) of materials involved in the templates used in ERT process.

	Au	Cr	Cr_2O_3	Si	SiO_2
ρ (Ω·m)	2.4×10^{-8}	13×10^{-8}	3×10^{4}	10^{-3}-10^{1}	10^{12}-10^{14}

Table 6. The thicknesses (t) and sheet resistances (R_s) of different material layers involved in the templates used in ERT process.

	Au/Cr/Si	Cr/Si	Si	Au/Cr/SiO_2	Cr/SiO_2	SiO_2
t (nm)	$25/5/5\times10^{5}$	$5/5\times10^{5}$	5×10^{5}	25/5/300	5/300	300
R_s (Ω/sq)	0.94	441	74227	1.33	803	∞

For Cr layer with thickness of 5-10 nm, the theoretical value of sheet resistance is 13-26 Ω/sq. However, the measured values of Cr layer on Si and SiO_2 are 441 Ω/sq and 803 Ω/sq, respectively. These results further prove the phenomenon of native oxidation on Cr surface.

5.1.2 Optimization of Electrodeposition Parameters

In addition to the rational structure of template, the parameter of electrodeposition is another important factor to the success of electrochemical replication. The optimization of the current density for electrochemical replication is determined from the results shown in Figure 32. We tuned the current densities by every 0.5 mA/cm^2 from 0.5 to 6.0 mA/cm^2 to perform electrodeposition processes on the same template. When current density is small (≤0.5 mA/cm^2), Cu materials cannot totally cover on the region of Au pattern (Figure 32A). When the current densities

are controlled between 1.0 mA/cm2 and 2.0 mA/cm2, the Cu materials are site-selectively deposited on the region of Au patterns effectively (Figure 32, B-E). If the current densities are further increased (≥2.5 mA/cm2), the Cu materials cannot be defined on the region of Au pattern only, but also are deposited on the surface of template substrate as well, which cannot replicate the pattern on the template successfully.

Therefore, the optimized current densities for electrochemical replication are controlled at the range of 1.0 - 2.0 mA/cm2. Relatively low or high values of current densities may result in failure of pattern replication during electrochemical replication.

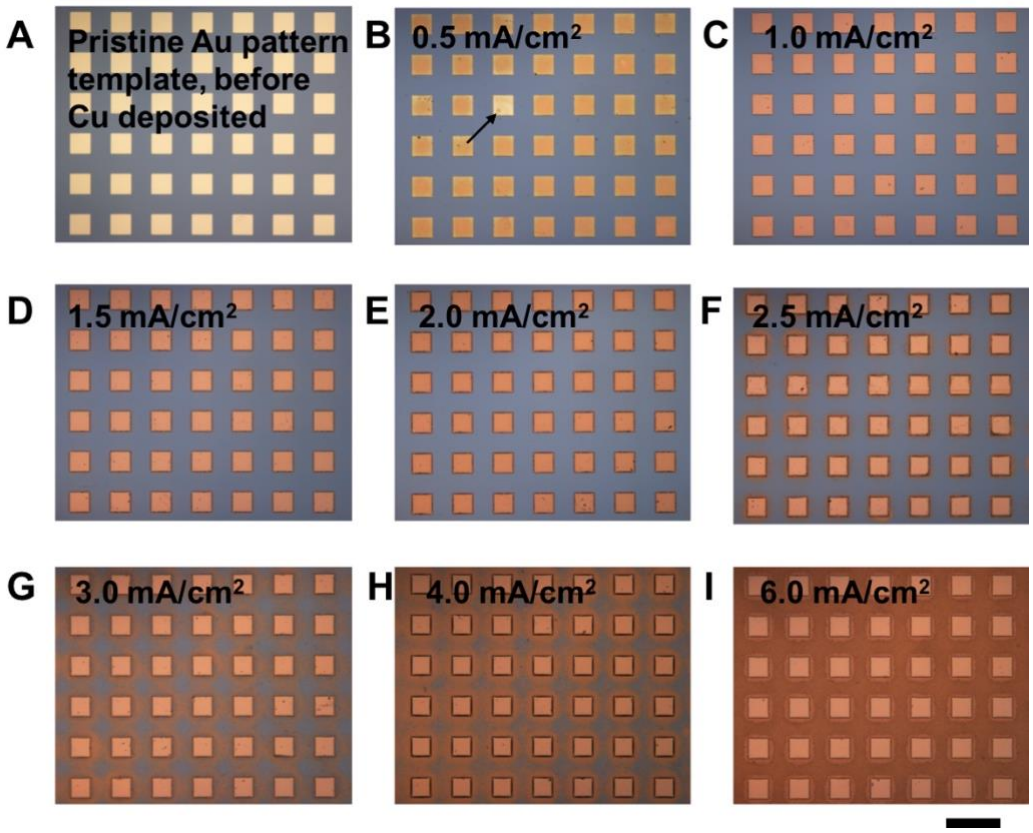


Figure 32. Optical microscopic images of Cu deposited on Au-pattern template under different current densities. The current density (mA/cm2) is calculated by dividing the current (mA) by the area (cm2) of the Au pattern. (A) Pristine Au-pattern template, before Cu materials deposited. (B) For small current density (≤0.5 mA/cm2), Cu materials cannot totally cover on the Au pattern region (as the arrow indicating). (C-E) The optimized current densities for effectively site-selective electrodeposition are 1.0 mA/cm2 to 2.0 mA/cm2. (F-I) For relatively big current density (≥2.5 mA/cm2), the Cu materials cannot be defined on the region of Au pattern, i.e., Cu is deposited on the surface of template substrate as well, which cannot replicate the pattern successfully. The current density (mA/cm2) is calculated by dividing the current (mA) by the area (cm2) of Au pattern (but not the area of the whole template). Electrodeposition time, 5 min. Scale bar, 100 μm.

To summarize the mechanism of the step of electrochemical replication, the schematic illustrations for typical cases are shown in Figure 33. A complete circuit is the necessary condition to perform electrochemical deposition. Material is deposited at the site where charge carriers travel through on the working electrode. Semiconductor and/or conductor (only Au as channel for charge carriers in Figure 33D) can be used as conductive mediums for charge carriers to go through and implement the electrodeposition process. In the setups of electrodeposition in Figure 33 A, B and D, working electrodes are made of semiconductor and/or conductor materials, the electrodeposition process can be implemented. If the circuit is cut off by dielectric materials (such as SiO_2 in Figure 33C), there will be no materials deposited on the working electrode.

Optimized current density is another necessary condition for selective electrodeposition on the Au-patterned template. Conductive Au is prior channel for the charge carriers, which realizes the prior deposition of Cu materials on the region of Au pattern (Figure 33A). Relatively big current density will result in unwanted deposition of materials beyond the region of Au pattern and fail in replication of patterns, because some charge carriers travel through the semiconductor substrate directly (Figure 33B).

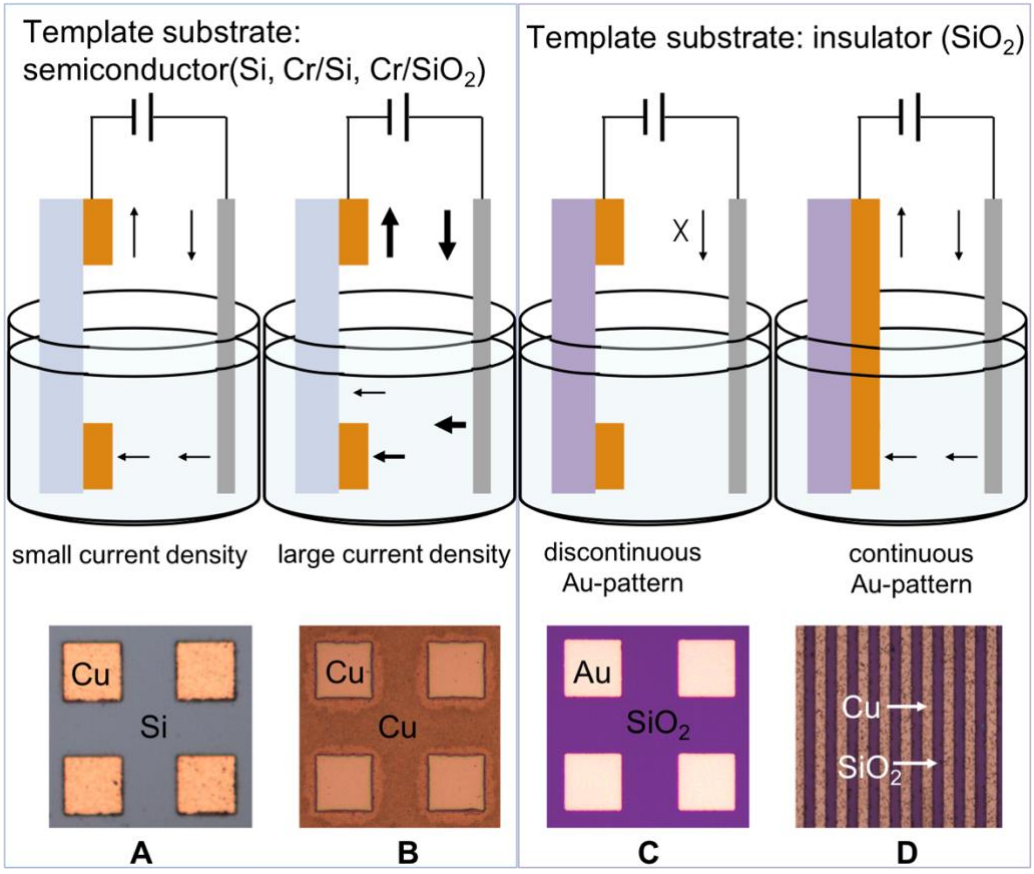


Figure 33. Schematic illustration of electrochemical replication process on different kinds of Au-patterned templates and by different values of current densities. For the templates using semiconductor materials as substrates (Si, Cr/Si, or Cr/SiO_2), target material can be site-selectively deposited on the Au pattern and form high quality pattern under optimized current density (A), while cannot form pattern effectively under relatively large current density (B). For the template using non-conductive material as substrate (SiO_2), the target material cannot be deposited on the isolated pattern (C), while can be deposited on the continuous pattern, where Au is the conductive medium for transporting the charge carriers to execute the electrodeposition process (D).

5.2 Transfer

The transfer of deposited material from the template to the target substrate is realized by mechanical peeling off process. The basic principle for successful transfer process is the adhesion between target material and target substrate is stronger than that between target material and original substrate. Based on this consideration, two strategies are applied in the ERT process (as shown in Figure 34): i) pre-treatment of self-assembled monolayers (SAMs) on the surface of Au pattern (surface modification) to decrease the adhesion between Au and deposited Cu, and ii) using adhesive polymer as binder to enhance the interaction with Cu. In this section, the mechanism analysis for the step of transfer will be discussed on these two strategies: the functions of surface modification and the binders used in transfer.

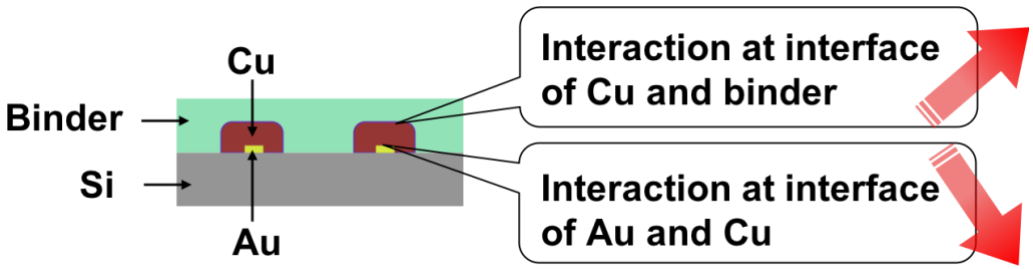


Figure 34. Schematic diagram of strategies to ensure the success of transfer: i) decreasing the interaction at the interface of Au and deposited Cu and ii) increasing the interaction at the interface of deposited Cu and binder.

5.2.1 Functions of Surface Modification

The surface modification with 1H,1H,2H,2H-Perfluorodecanethiol (PFDT) for

Au-patterned template as pre-treatment is significantly important in the ERT process (Figure 35). The first function of PFDT modification is to decrease the interaction between as-deposited material layer with the Au-pattern layer, ensuring the target material pattern could be peeled off successfully from the template. PFDT molecules can form self-assembled monolayers (SAMs) on the Au surface through the thiol groups at the chain terminals (gold-sulfur bonds).[146-147] This process is indicated by the change of wettability on Au surface, because fluorine (F) atoms on the carbon chain make the Au surface hydrophobic (Figure 35A).[148-149] The SAMs is used as the anti-adhesive layer, which can significantly decrease the force of peeling off deposited materials from the substrate (Figure 35, B, D-E).

The second function of PFDT modification is to protect the Au pattern from damage during the mechanical transfer step. Herein we demonstrated one Au-pattern template reused for 100 fabrication cycles of ERT process. While we used the same Au-patterned template with PDFT modification to repeat the ERT process for 100 times, no damage phenomenon was observed obviously on the Au pattern, which was confirmed by AFM and SEM characterizations (Figure 35, C and F). We listed all the 100 transparent Cu mesh samples fabricated by 1 single Au-patterned template in Figure 35H. The Au-patterned template without surface modification is used as control group. The force of peeling off target materials from the template of control group is much larger than that on template with surface modification (Figure 35B). Furthermore, the deposited Cu mesh cannot be transferred successfully (Figure 35E) and the Au mesh on the template is damaged seriously during the mechanical process of peeling off (Figure 35G).

Since the template is reusable, i.e., one template can be reused to fabricate many

ERT copies (Figure 34H). No matter by photolithography or EBL, we only need to perform the fabrication of template for once and then carry out the ERT process independently. Therefore, we can ignore the cost of the template in the whole ERT process. In other words, the reusability of the template makes ERT process as one new patterning technique. It should be highlighted that the reusability of Au-patterned template enables the ERT process showing the ability of scale-up production in the practical industry applications.

The thiol groups are prior self-assembled on the surface of Au, but not on the surface of Si substrate (or oxidized Cr surface).[150] Even though Si substrate (or oxidized Cr surface) is not protected by SAM layer, it is stable enough during the mechanical transfer process and the adhesive with binders is weak, because no residues from the substrate are detected on the transferred samples.

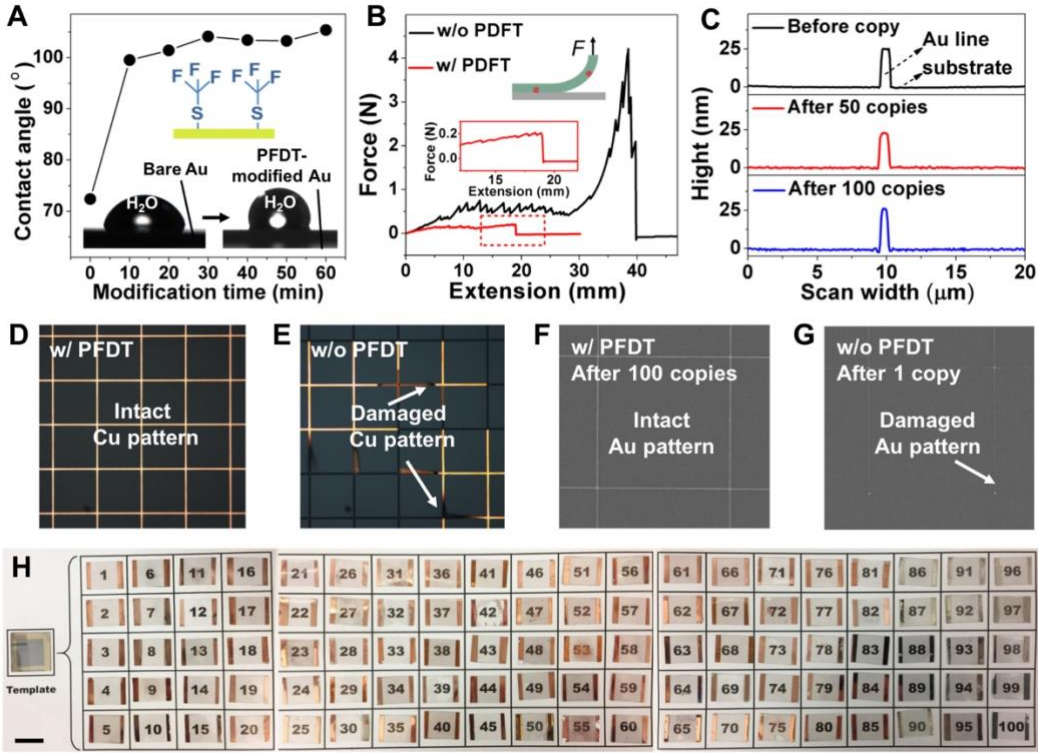


Figure 35. Functions of surface modification of self-assembled monolayer for ERT method. (A) Contact angles of Au film surface after modified by 1H,1H,2H,2H-Perfluorodecanethiol (PFDT) for different modification times. (B) The forces of peeling off as-deposited Cu patterns from the Au-patterned templates with and without the PFDT modification. (C) AFM characterization of the profiles on Au lines on template before and after 50 and 100 ERT processes. (D) With PFDT modified on Au-pattern template, as-deposited Cu pattern kept intact during transfer process. (E) Without PFDT modification, Cu pattern damaged seriously during the transfer process. (F) With PFDT modification, Au pattern kept intact after 100 copies. (G) Without PFDT protection, Au pattern damaged during the mechanical peeling off process. (D-G) Pitch size, 100 μm. (H) 100 transparent Cu mesh samples fabricated by a single Au-patterned template. Scale bar, 1 cm.

5.2.2. Rational Selection of Photo-Curable Binders

Photo-curable polymers used as adhesive binders can achieve high interaction with deposited materials and successfully transfer them during ERT process. The alternative photo-curable polymers as binders are varied. As a proof-of-concept, four kinds of UV-curable polymers, i.e., NOA serial products (NOA 63, NOA 65, NOA 68, Figure 36, A-C) and poly(methyl methacrylate) (PMMA, Figure 36D), are evaluated and used to peel off as-deposited materials from the Au-patterned template, respectively (Figure 36). The main components shown in Table 7 indicate there are thiol groups (mercapto) in the NOA products, which may be the key role for the adhesive functions. PMMA consists of acrylic group (Table 7), which is well known as acrylic adhesive in many commercial products. Acrylic adhesives are very strong and efficient at bonding different objects together.[151-152] PMMA as a binder used in ERT process effectively transfers the deposited materials from template to target substrate (Figure 36D).

To summarize the mechanism of the step of transfer, PFDT modified on Au surface is acted as anti-adhesive layer which weakens the interaction between deposited materials with Au layer on the template. On the other hand, the photo-curable adhesive polymer is used as the binder to peel off the deposited materials from the template effectively. The schematic diagram in Figure 34 shows that there are two other kinds of interactions, i.e., interaction between template substrate (Si) and binder, and interaction between Si and deposited Cu. However, the interactions at these two interfaces should be tiny because of the smoothness of Si surface. According to the results of the experiments, the combination of surface modification and the use of binders is already effective enough to ensure the success of the step of transfer.

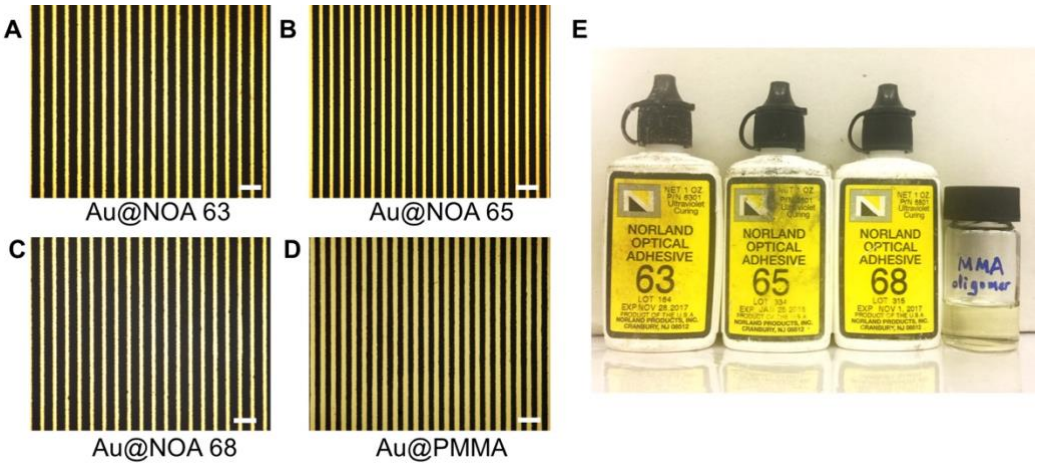
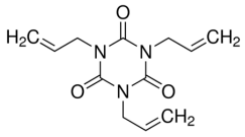
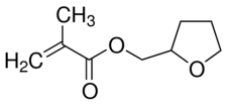
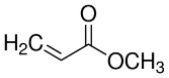
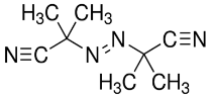
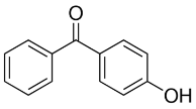


Figure 36. Alternative UV-curable binders used for the step of transfer in ERT process. Optical microscopic images of ERT-based Au patterns on (A) NOA 63, (B) NOA 65, (C) NOA 68, and (D) PMMA, respectively. Scale bar, 20 μm. For electrochemical replication of Au materials on template, current density: 0.5 mA/cm2, deposition time: 10 min. (E) Digital image of these four kinds of UV-curable binders. Their main components are listed in Table 7.

Table 7. The main components in the four UV-curable polymers used as binders in ERT method.

UV-curable binders	Main components
NOA 63	Triallyl Isocyanurate (15-40%)  Mercapto-ester* (30-50%) Mercapto-ester* (35-60%)
NOA 65	Mercapto-ester* (30-50%) Mercapto-ester* (35-60%)
NOA 68	Tetrahydrofurfuryl (15-25%)  Mercapto-ester* (30-50%) Mercapto-ester* (35-60%)
PMMA	Methyl acrylate (monomer)  Azobisisobutyronitrile (thermal initiator, 0.2%)  4-Hydroxybenzophenone (photoinitiator, 0.2%) 

The main components of NOA products were referred to the corresponding material safety data sheet (MSDS). * The specific chemical identity and concentration were withheld from this data sheet as a trade secret. (https://www.norlandprod.com/adhesiveindex2.html)

5.3 Conclusions

Electrochemical replication and transfer (ERT) process contains two main steps: (1) electrochemical replication and (2) transfer. In the electrochemical replication, the rational structure of template (i.e., conductive Au pattern on semiconductor substrate) and optimization of electrodeposition parameters are both necessary conditions, which together determine the success of selective electrodeposition. The success of transfer step is attributed to both the surface modification on Au-patterned template before the deposition of target material and the use of photo-curable polymers as the binder. The self-assembled monolayers (SAMs) modified on the surface of Au pattern not only serve as the anti-adhesive release layer to facilitate the transfer of materials, but also improve the reusability of the Au template.

Chapter 6: Applications of ERT Method

Generation of pattern is a fundamental step in a wide variety of applications, especially the electronic devices. In this chapter, the applications of ERT are demonstrated by fabricating various electrodes with different patterns based on ERT process and further integrating them in the electronic devices, including flexible transparent electrodes (FTEs) for flexible transparent heaters (FTHs), organic light-emitting diodes (OLEDs), and touch screen panels (TSPs), source/drain (S/D) electrodes for organic electrochemical transistors (OECTs), and interdigital electrodes (IDEs) for micro-supercapacitors (MSCs).

6.1 Flexible Transparent Electrodes (FTEs) Based on ERT Method

6.1.1 Background of FTEs

Flexible transparent electrodes (FTEs) are prerequisite components for emerging flexible and wearable optoelectronic devices, such as flexible transparent heaters (FTHs), light-emitting diodes (LEDs), solar cells (SCs), touch screen panels (TSPs), photodetectors, human-machine interaction apparatus, etc. Besides the two basic elements for rigid transparent electrodes, i.e. satisfactory electrical conductivity and optical transparency, excellent mechanical flexibility is an essential requirement for the new-generation FTEs.[126, 153-156] Indium tin oxide (ITO), as the current dominating material for transparent electrodes, combines low sheet resistance (R_s) and excellent transmittance (T), simultaneously.[157] However,

to be further served in flexible optoelectronic devices, ITO is hindered by some severe limitations, such as inherent brittleness of oxide film, increasing cost of indium source, infeasible high-temperature annealing on flexible polymeric substrates, etc.[158]

During the past decade, significant efforts have been focused on developing alternative materials of ITO. Promising candidates include conductive polymers (such as poly(3,4-ethylenedioxythiophene):poly(styrene sulfonate) (PEDOT:PSS)),[159-160] carbon-based materials (carbon nanotubes and graphene),[161-162] and metal-based materials (ultrathin metal film, metal nanowires and metal mesh, as shown in).[163-167] The mechanical flexibility of FTEs based on these emerging alternative materials is much superior to that of ITO. However, for conductive polymers, carbon-based materials, and ultrathin metal films, the overall optoelectronic properties, i.e. R_s and T, still cannot fully compete with ITO ($R_s \sim 10\ \Omega\ sq^{-1}$, $T \sim 90\%$).[157] On the other hand, the high-cost fabrication processes (such as vacuum-based thermal evaporation, sputtering, chemical vapor deposition, etc.) are considerable barriers to their widely practical applications. The all-solution process by using metal nanowire inks achieves the low-cost fabrication of FTEs. However, metal nanowire-based FTEs are also hindered by some drawbacks, such as significant contact resistances between wire-wire junctions, high surface roughness, unsatisfactory chemical stability, etc.[153-154, 156, 168]

Metal meshes, as one of the most promising candidates for FTEs, possess the advantage in balancing the trade-off between R_s and T. The overall electro-optical performance of metal mesh can be managed effectively due to the highly tunable geometric parameters (such as line width, thickness, and pitch). The R_s and T of

metal mesh-based FTEs can reach or even over the level of ITO. A large number of patterning techniques have been developed to fabricate metal meshes, ranging from conventional processes (such as photolithography,[169-171] e-beam lithography,[172] nanoimprinting,[166, 173-176] inkjet printing,[127, 167, 177] laser writing,[178-180] etc.) to emerging strategies (such as self-forming crack lithography,[181] nanosphere lithography,[182-183] grain boundary lithography,[184] coffee-ring lithography,[185-186] electrospun-fiber template,[187-188] bio-inspired template,[189-190] etc.). All these lithography/printing techniques can effectively pattern highly aligned metal meshes and realize satisfactory optoelectronic performances. However, the patterning metallic materials based on these techniques are generally complicated and practically time-consuming. Additionally, some extraordinarily expensive and material-consuming processes, such as the vacuum-based depositions, liftoff or etching of redundant metal materials, etc., are frequently employed in the fabrication processes of metal meshes.

Therefore, it is still a big challenge to develop an alternative cost- and time-saving patterning technique for the fabrication of metal mesh-based FTEs. The ERT strategy developed in this research is a high-resolution, high-throughput, and low-cost patterning technique, which shows high potential in the fabrication of high-performance metal mesh-based FTEs. In this section, ERT technique is used to fabricate metal meshes firstly. Then the opto-electrical performance, mechanical flexibility, and environmental stability of as-made metal meshes are characterized. Finally, metal mesh-based FTEs are integrated in the optoelectronic devices, including flexible transparent heaters (FTHs), touch screen panels (TSPs), and organic light-emitting diodes (OLEDs).

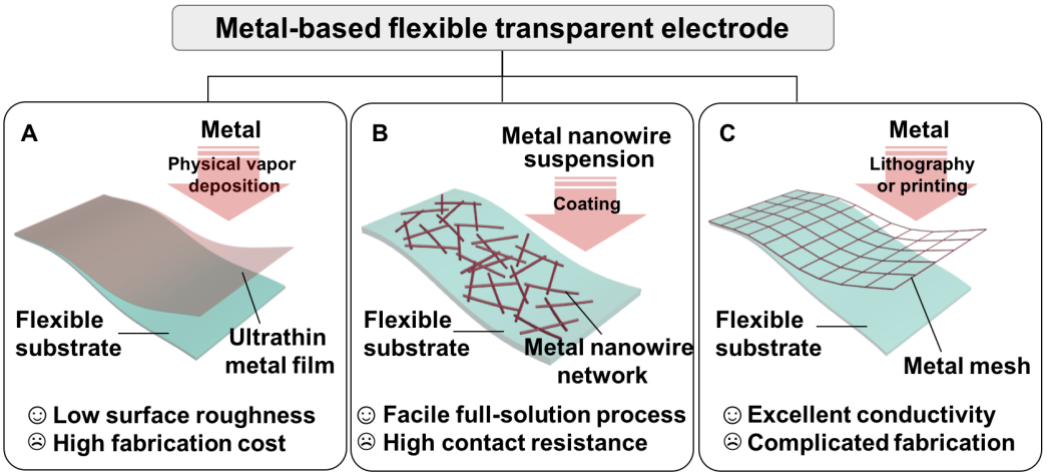


Figure 37. Schematic structures, fabrication technologies, major advantages and disadvantages of metal-based flexible transparent electrodes: (A) ultrathin metal film, (B) metal nanowire network and (C) metal mesh.

6.1.2 Fabrication of Metal Meshes for FTEs

As a proof-of-concept, we used a square pattern with 100-μm pitch (p) to implement the ERT process for the fabrication of metal meshes. The process of fabricating metal meshes based on ERT is characterized by optical microscope (OM), scanning electron microscope (SEM), and atom force microscope (AFM) in Figure 38. OM images indicate the high-aligned patterns during the fabrication process. The inserted digital photographs show the large-area size (6.5 cm × 4 cm) of as-made metal mesh. SEM images show the metal meshes at tilted and cross-section views, especially the transfer of out-of-plane Cu mesh to embedded Cu mesh in binder. AFM was used to characterize the topographies of metal meshes in terms of linewidth (w), height (h), and surface roughness (R_q).

The linewidth (w) of Au pattern was designed as sub-micron (~ 800 nm), which can be invisible to bare eyes for special optoelectronic applications, such as display and touch screen. Cu was selectively deposited on Au pattern to form well-patterned Cu mesh, while bare Si region was kept clean. Because of highly-effective deposition of electroplating, the thickness of Cu mesh could reach micrometer scale, which could remarkably enhance the electrical conductivity of final FTEs. The out-of-plane Cu mesh on Si substrate was peeled off and embedded in the NOA63 binder in the step of transfer. The strategy of embedded structure for metal mesh with high thickness could ingeniously achieve high electrical conductivity and low surface roughness, simultaneously. The morphological characterization indicated that the embedded Cu mesh-based FTEs were successfully fabricated through ERT process.

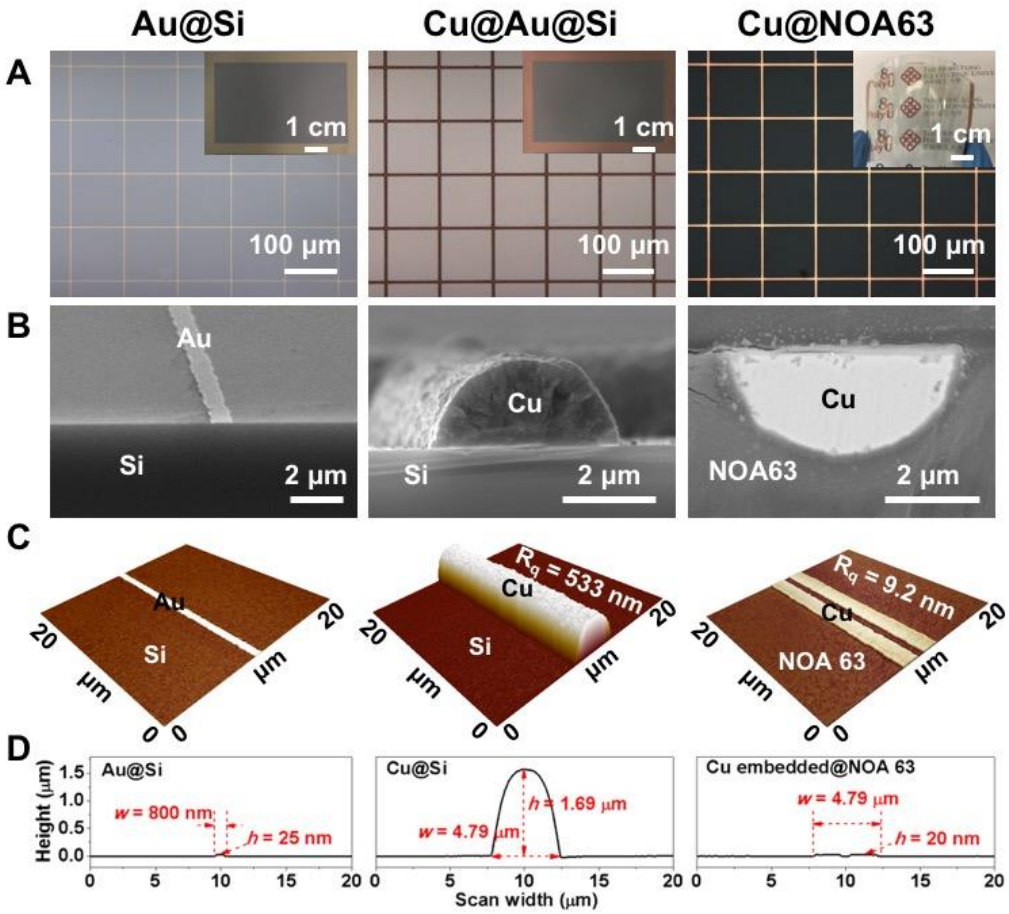


Figure 38. Morphological characterization of metal meshes at different fabrication steps: Au@Si, Au mesh prepared on Si wafer substrate as template; Cu@Au@Si, Cu mesh selectively electrodeposited on Au-patterned template; Cu@NOA63, Cu mesh transferred on the target substrate with binder NOA63. (A) Optical microscopic (OM) images and corresponding digital photographs inserted with size of 6.5 cm × 4 cm. (B) Scanning electron microscope (SEM) images at tilted and cross-section views. (C) 3D-view images characterized by atom force microscope (AFM). Surface roughness of embedded Cu (R_q = 9.2 nm) is significally smaller than that on Si substrate (R_q = 533 nm). (D) Linewidth (w) and height (h) of Au line on template and Cu line before and after transfer.

6.1.3 Electrical and Optical Performance of FTEs

Two templates with different linewidths, 0.8 μm and 4.0 μm, were used to fabricate metal meshes and study the corresponding morphology and opto-electrical property. For a fixed template, the line thickness (*t*) and width (*w*) (characterized by AFM) of electroplated Cu lines are controlled by electroplating time under the optimized current density (2 mA/cm2). Under a constant current density, both of *t* and *w* of deposited Cu meshes increased near-linearly with the deposition time (Figure 39, Figure 40A, Figure 41, Figure 42A). For the requirement of invisible line for some special optoelectronic devices, the line width can be controlled to less than 5 μm by tuning electroplating time (such as ≤35 min in the case of 0.8-μm Au mesh template).

The electrical conductivity of metal mesh is determined by the mass loading of deposited Cu for a certain pattern. Increasing the electrodeposition time and mass loading of Cu (linewidth and thickness increasing) can effectively improve the electrical conductance (Figure 40B and Figure 42B). For the case based on 0.8-μm Au mesh template, sheet resistance R_s decreased from 26.19 Ω sq-1 to 0.055 Ω sq-1 as the increasing of electroplating time (from 5 min to 100 min) and Cu line thickness (from 0.23 μm to 4.04 μm). Particularly, when the thickness was more than 1 μm, the R_s decreases to less than 1 Ω sq-1, and the smallest value even reached 0.055 Ω sq-1 (insert in Figure 40B).

As a percolation structure, optical transmittance (*T*) of metal mesh is mainly determined by the coverage percentage of Cu mesh, i.e., larger line width of Cu mesh results in lower *T* (Figure 40C and Figure 42C). For the case based on 0.8-μm Au mesh template, when the *w* of Cu mesh increased from 1.07 μm to 12.07

μm, the transmittance of FTEs at the wavelength of 550 nm decreased from 97.1% to 77.7%. It should be noted that the R_s and T of our embedded Cu meshes could both surpass the level of ITO (10 Ω sq^{-1}, 90%), such as (2.79 Ω sq^{-1}, 96.8%), (1.33 Ω sq^{-1}, 95.1%), (0.77 Ω sq^{-1}, 93.5%), (0.53 Ω sq^{-1}, 91.8%) that listed in Figure 40. For the case based on 4.0-μm Au mesh template, the sheet resistance could reach ultralow values (<0.1 Ω sq^{-1}) when the electrodeposition time was increased (Figure 42B). However, since the pristine linewidth of Au mesh was ~4.0 μm, which bigger than 0.8 μm in the above case, the transmittances were generally at the range of 80% to 90% (Figure 42C).

The tradeoff between R_s and T is a common issue among various transparent electrodes. Therefore, the overall performance of transparent electrodes is usually evaluated by the figure of merit (*FoM*). The *FoM* value was calculated based on the measured R_s and T according to the following widely accepted equation:[126, 154, 191-192]

$$FoM = \frac{188.5}{R_s(\frac{1}{\sqrt{T}} - 1)}$$

The increasing of Cu line thickness could achieve the sharp increasing of *FoM* value (Figure 40D). Even through the increase of linewidth caused a linear loss of transmittance, thicker linewidth and thickness of Cu mesh improved the electrical property much more significantly. The ultralow sheet resistances (~ 0.1 Ω sq^{-1}) shows notably positive impacts on the values of *FoM*. For the case based on 0.8-μm Au mesh template, while the plating times were 80 min and 100 min, the sheet resistances and transmittances were 0.11 Ω sq^{-1} and 85.0%, 0.055 Ω sq^{-1} and 77.7%, respectively. The corresponding values of *FoM* reached ~20,000 and ~25,000, respectively (Figure 40D). For the case based on 4.0-μm Au mesh template, the

maximum value of *FoM* was also large at ~18,000 (Figure 42D).

In order to study the influent of different geometrical shapes on the performance of metal meshes, a random pattern was designed for the template and corresponding ERT-based Cu meshes were fabricated and characterized (Figure 43). This random-pattern Cu mesh shows sheet resistance of 0.52 Ω sq^{-1}, transmittance of 86.3% and *FoM* of 4742. Compared with the data on the cases of square patterns, we cannot conclude which geometrical shape for the pattern is superior in this fabrication process. However, since electrodeposition process can reach high thickness of Cu pattern and excellent electrical property, we can infer that geometrical shape is not an important factor to decrease the sheet resistance while the thickness of deposited metal mesh plays the main role to improve the electrical property.

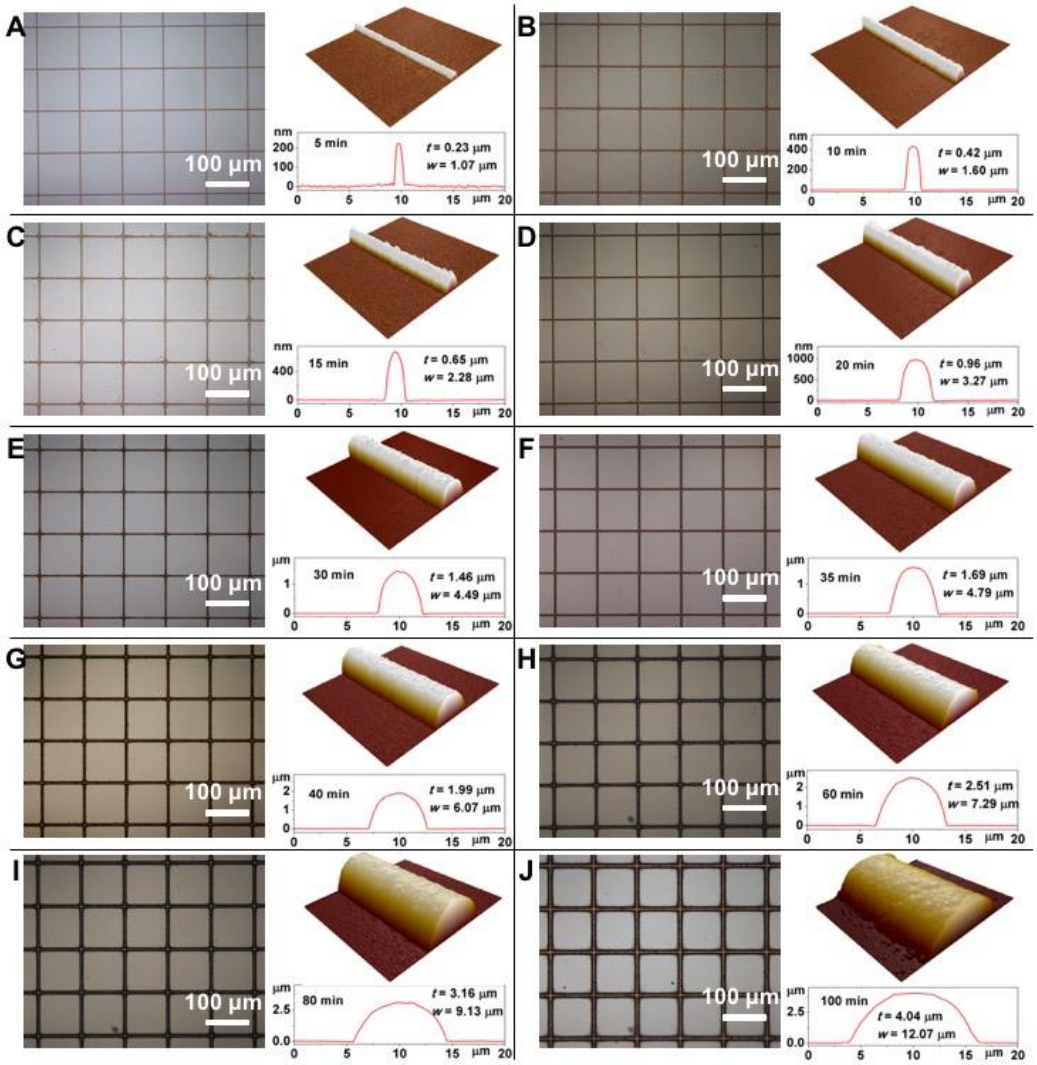


Figure 39. Based on 0.8-μm Au mesh template: morphological characterization of Cu mesh deposited on Si substrate with different electroplating times: (A) 5 min, (B) 10 min, (C) 15 min, (D) 20 min, (E) 30 min, (F) 35 min, (G) 40min, (H) 60min, (I) 80 min, and (J) 100 min. In each set of figures: left, optical microscope image; top right, 3D view image by AFM; bottom right, measurement of Cu line thickness (*t*) and width (*w*) by AFM.

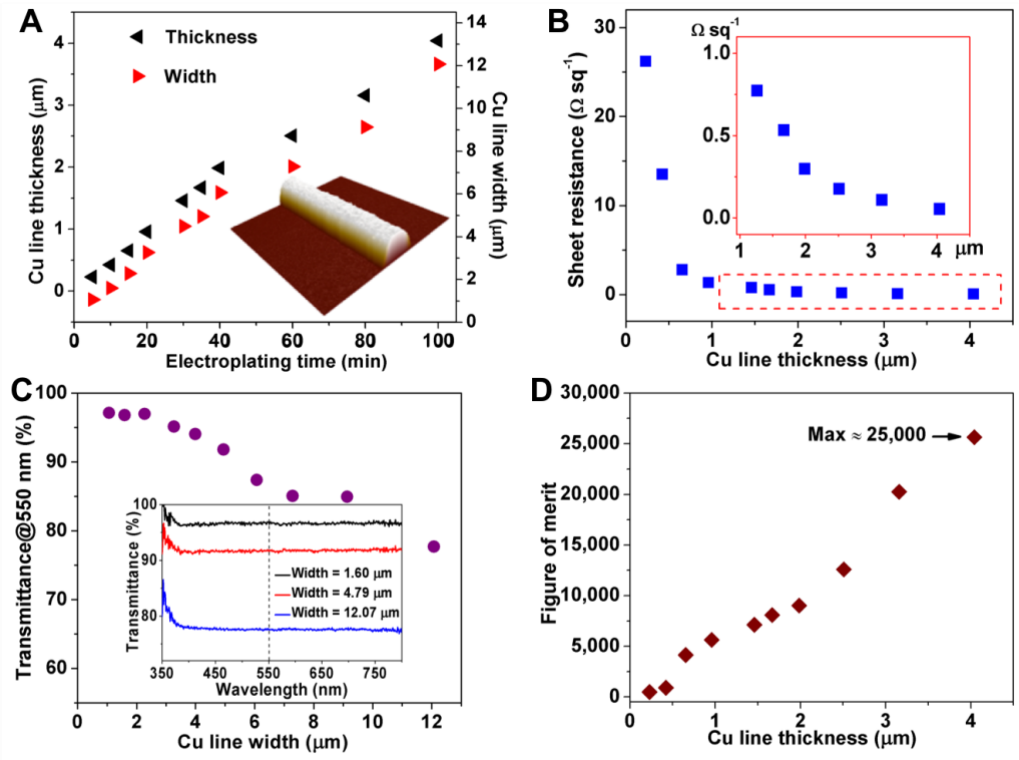


Figure 40. Based on 0.8-μm Au mesh template: (A) Line thickness and width of Cu mesh versus electrodeposition time (insert: AFM image of Cu mesh on Si substrate). The thickness and linewidth both increase linearly with the electrodeposition time. Optoelectronic performance characterization of embedded Cu mesh-based FTEs: (B) sheet resistance (R_s), (C) optical transmittance (T, insert, transmittance vs. wavelength), and (D) figure of merit (FoM) of embedded Cu mesh-based FTEs.

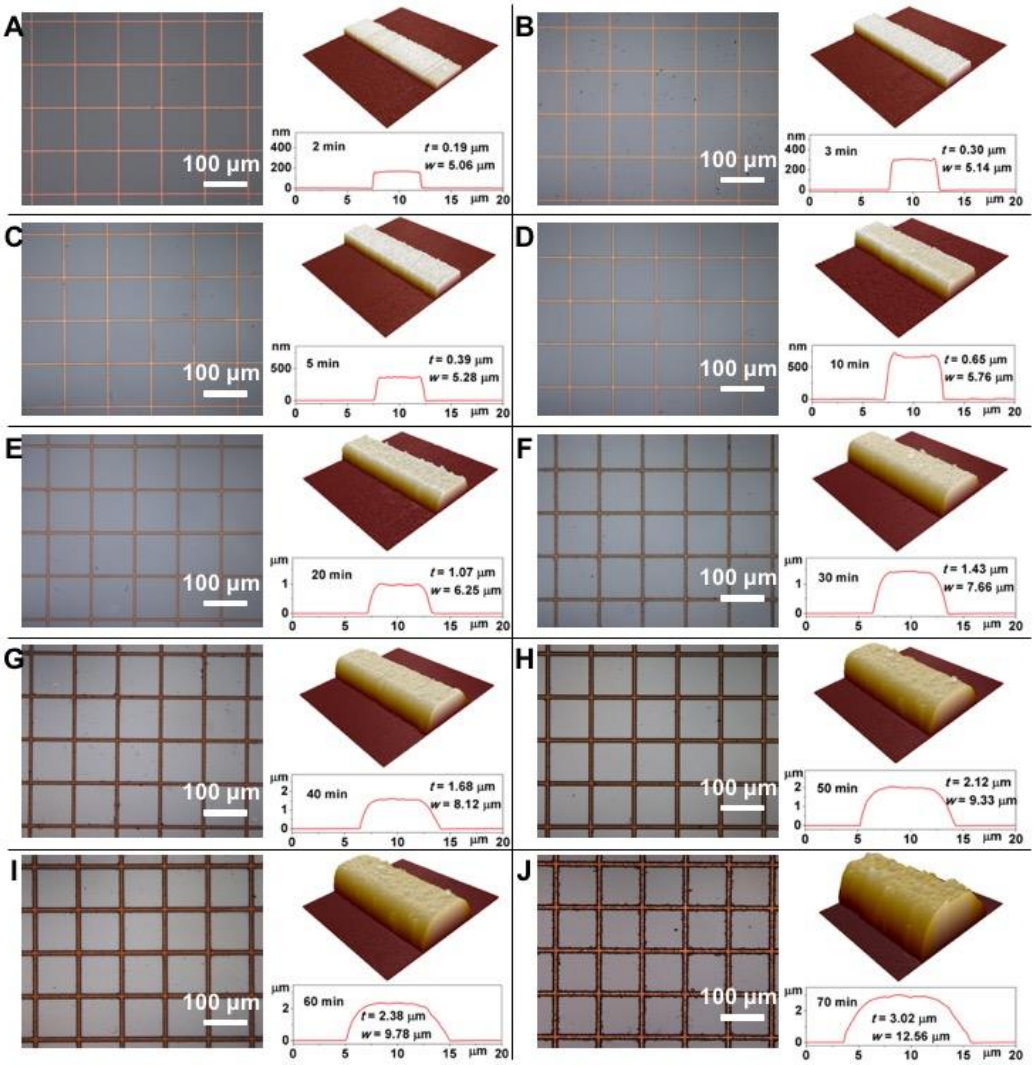


Figure 41. Based on 4.0-μm Au mesh template: morphological characterization of Cu mesh deposited on Si substrate with different electroplating times: (A) 2 min, (B) 3 min, (C) 5 min, (D) 10 min, (E) 20 min, (F) 30 min, (G) 40min, (H) 50min, (I) 60 min, and (J) 70 min. In each set of figures: left, optical microscope image; top right, 3D view image by AFM; bottom right, measurement of Cu line thickness (*t*) and width (*w*) by AFM.

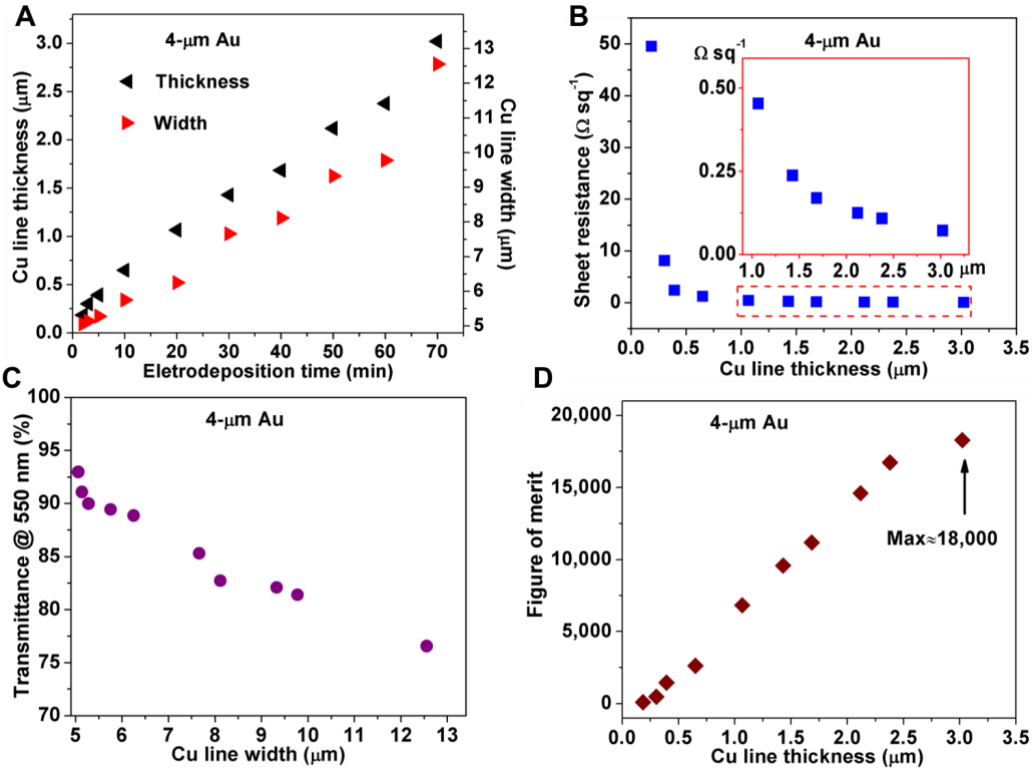


Figure 42. Based on 4.0-μm Au mesh template: (A) Line thickness and width of Cu mesh versus electrodeposition time (insert: AFM image of Cu mesh on Si substrate). Optoelectronic performance characterization of embedded Cu mesh-based FTEs: (B) sheet resistance (R_s), (C) optical transmittance (T), and (D) figure of merit (FoM) of embedded Cu mesh-based FTEs.

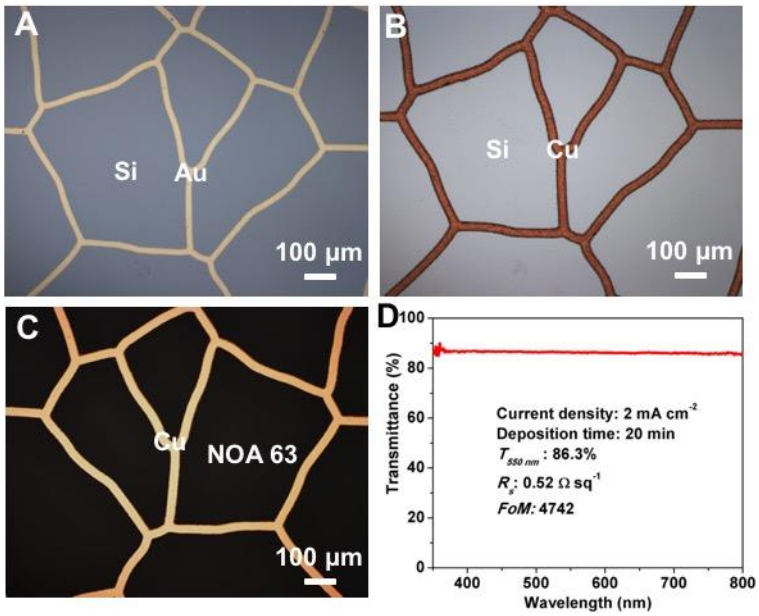


Figure 43. Based on random pattern Au mesh template: characterization of morphology and electro-optical performance. A) Au@Si; B) Cu@Au@Si; C) Cu@NOA 63; D) opto-electrical performance: sheet resistance (R_s), transmittance (T), and figure of merit (FoM).

A comprehensive comparison of transparent electrode materials on the electro-optical performances is shown in Figure 44. The R_s and T of typical transparent electrode materials, covering metal-based materials (metal meshes, metal nanowire networks and electrospun fiber networks),[165-167, 171, 193-194] carbon-based materials (CNT and graphene),[161-162] conductive polymers (PEDOT:PSS),[159-160] and transparent conductive oxides (ITO),[157] are summarized and compared with our embedded metal mesh-based FTEs. In principle, lower sheet resistance and higher transmittance indicate better optoelectronic performance of transparent electrodes. The data presented in Figure 44 obviously indicated that FoMs of our embedded metal meshes occupy at the leading positions among the various transparent electrode materials.

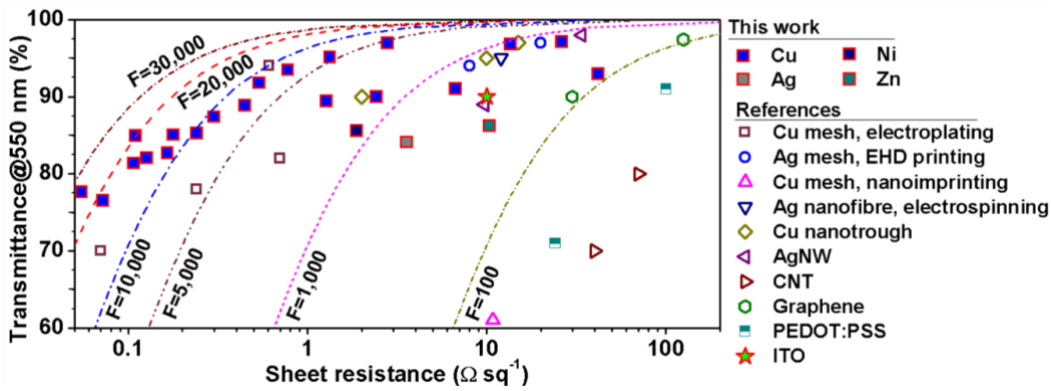


Figure 44. Comparison of optoelectronic performance of our embedded Cu mesh-based FTEs with other typical TEs published previously, including metal meshes fabricated by electroplating,[171] electrohydrodynamic (EHD) printing[167] and nanoimprinting,[166] metal nanofiber/nanotrough networks,[193-194] Silver nanowire networks,[165] carbon nanotube (CNT) networks,[161] graphene,[162] PEDOT:PSS,[159-160] and ITO films.[157]

6.1.4 Mechanical and Environmental Stability of FTEs

In addition to the remarkable electro-optical performances, the metal mesh-based FTEs showed excellent mechanical flexibility and environmental stability (Figure 45). Mechanical flexibility of FTEs is investigated through the typical bending tests (as shown in the inset of Figure 45A). The normalized resistance (R/R_0) recorded during bending test remains relatively stable at different curvature radii ranging for 1 mm to 15 mm (Figure 45A). ITO film sputtered on polyethylene terephthalate (PET) substrate (ITO@PET) is tested under the same conditions and compared as the control group. As shown in Figure 45A, the resistance of ITO@PET increases sharply when bending radius reduced to 2 mm. Furthermore,

after 1000 cycles of bending fatigue test, the resistance of metal meshes still shows little change, which is superior than the behavior of ITO@PET (Figure 45B). The superior mechanical flexibility of Cu mesh should be partially attributed to excellent ductility of metals. Even though some broken lines on Cu meshes are observed after 1,000 bending cycles (Figure 46, A-B), the surrounding undamaged lines still ensure current delivery effectively. By comparison, the inherent brittleness of ITO results in serious cracks during mechanical deformation (Figure 46C), and further impacts negatively on its conductivity, which is one of important drawbacks for its integration in flexible electronics.

The mechanical robustness is also characterized by testing the adhesion between embedded Cu mesh and NOA 63. A tape peeling test is applied on the embedded Cu mesh to check its adhesion with the substrate (insert in Figure 45C). Because of the embedded structure and the strong interaction caused by binder, the adhesion between Cu mesh and substrate is strong enough to ensure the excellent mechanical robustness. The resistance and morphology of as-tested Cu mesh are virtually unchanged after 100 times of tape peeling tests (Figure 45C and Figure 46D).

Furthermore, the Cu meshes show excellent environmental stability. The resistances and morphologies of Cu meshes were monitored for 7 days in four typical environments, including air, water, ethanol, and high-temperature/high-humidity (85℃/85%) conditions (Figure 45D and Figure 47). The resistances keep stable during the 7-day environmental tests. It is well known that Cu is easily oxidized while exposed in oxygen-water condition. Oxidation layers could be observed on the Cu meshes after 7-days environment tests, especially in the water

and high-temperature/high-humidity conditions (as shown in Figure 47, C-D). However, the impact of surface oxidation on the conductivity of embedded Cu mesh is extremely slight, indicated by the stable resistance during the environmental tests. It should be attributed to the high thickness of Cu mesh and the embedded structure. Since the overall thickness of Cu mesh is in micrometer scale, the surface oxidation layer is too thin to affect the overall electrical performance. One the other hand, the embedded structure could protect most of the Cu surface from the contact with oxygen-water environment.

The performances, including electrical and optical properties, mechanical flexibility, and environmental stability, of metal mesh-based FTEs are studied comprehensively. The relevant results indicate metal meshes fabricated by ERT are excellent candidate materials for flexible transparent electrodes. Based on the excellent performances, the low-cost metal meshes are promising to be integrated in the optoelectronic devices.

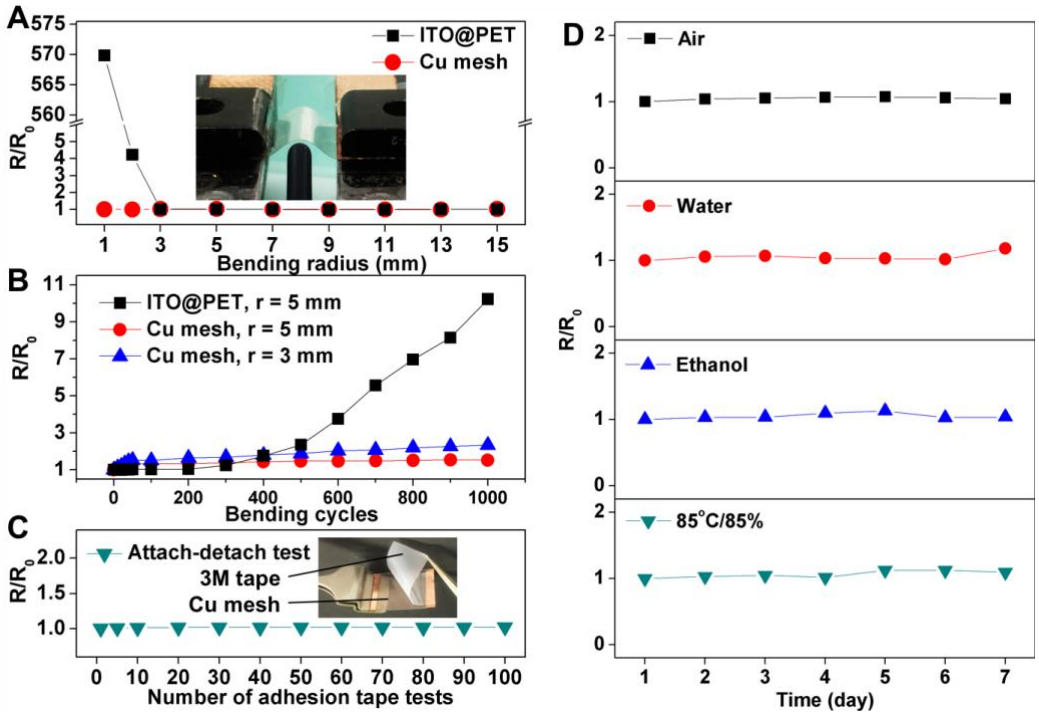


Figure 45. Mechanical flexibility and environmental stability. Resistance variations of embedded Cu mesh-based FTEs and ITO film deposited on PET substrate (ITO@PET, control group) bended at (A) different radii and (B) bending cycles. (C) Normalized resistance of embedded Cu mesh-based FTE during 100-cycle attach-detach tests for investigation of adhesion between Cu mesh and NOA 63 substrate. (D) Normalized resistance of embedded Cu mesh-based FTEs in four typical environments for 7 days, including air, water, ethanol, and high-temperature/high-humidity (85℃/85%) conditions.

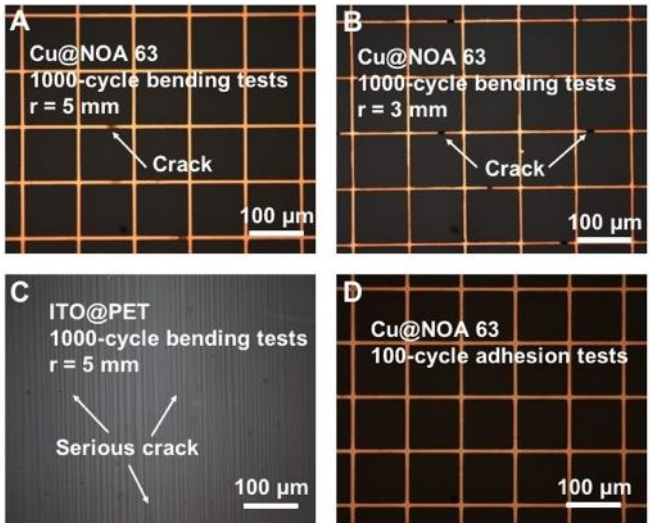


Figure 46. Morphologies of embedded Cu mesh-based FTEs after 1000-cycle bending tests at (A) 5-mm and (B) 3-mm bending radii. (C) Morphology of ITO@PET after 1000-cycle bending tests at 5-mm bending radius. (D) Morphology of embedded Cu mesh-based FTE after 100-cycle adhesion tests.

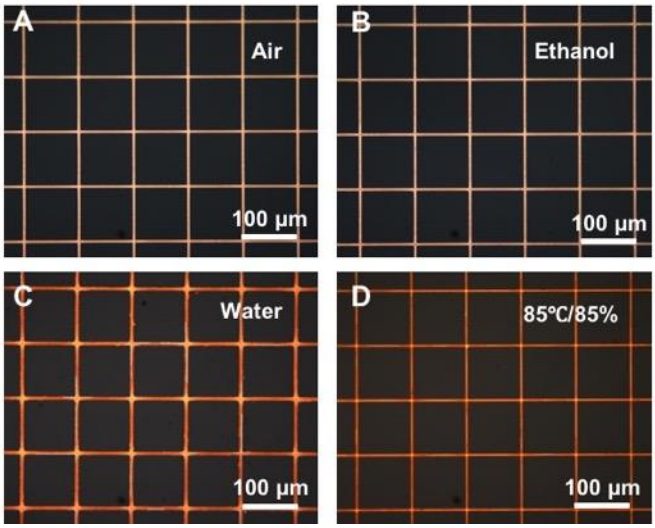


Figure 47. Optical microscope images of embedded Cu mesh-based FTEs in four typical environments after 7 days, including in (A) air, (B) ethanol, (C) water, and (D) high-temperature/high-humidity (85℃/85%) conditions.

6.1.5 Demonstrations of Optoelectronic Devices Based on FTEs

Flexible Transparent Heaters (FTHs)

Transparent heaters (THs) can be used to control the temperature by joule heating while applying voltage on the transparent conductors. This simple optoelectronic device exploits its applications in broad areas, such as defoggers in vehicles (displays, windshields and headlights), deicers, dehumidification for painting conservation, wearable electronic devices for personal thermal management or healthcare purposes, etc. Low sheet resistance and high optical transmittance are prerequisites for low-voltage transparent heaters. The basic requirements for flexible transparent heaters are fast heating and cooling rates at low input voltage or power, uniform and stable temperature distribution and even at flexible state.[171, 195-196]

One flexible transparent heater (FTH) based on the ETR-based Cu mesh is demonstrated and characterized in Figure 48. Direct current (DC) is applied on the two ends of a 6.5 × 4.0 cm^2 Cu mesh with the resistance of about 0.4 Ω. The saturation temperature increases linearly as the function of power density (Figure 48A). The saturation temperature could reach about 130 ℃ with ultra-low applied voltage (1.9 V) and power density (0.33 W cm^{-2}). The power efficiency is the slope of temperature to the power density, which is generally used as a performance comparison factor for transparent heaters. The power efficiency of our FTH with ~334 ℃ cm^2 W^{-1} is much superior than that of ITO-based heater (~88 ℃ cm^2 W^{-1}).[195-196] The IR image indicates that the temperature distribution

is homogeneous through such large-area device (inserted image in Figure 48A). When applied different value of voltages, the temperatures of FTH increase to the peak rapidly within ~50 s and keep stable at the platforms. The temperatures cool down to room temperature within ~50 s after power is turned off (Figure 48B). As a flexible device, the FTH is demonstrated to be bent at different bending radii (from 15 mm to 3 mm) during operation state. The stable temperature indicates the excellent flexibility of FTH device (Figure 48C).

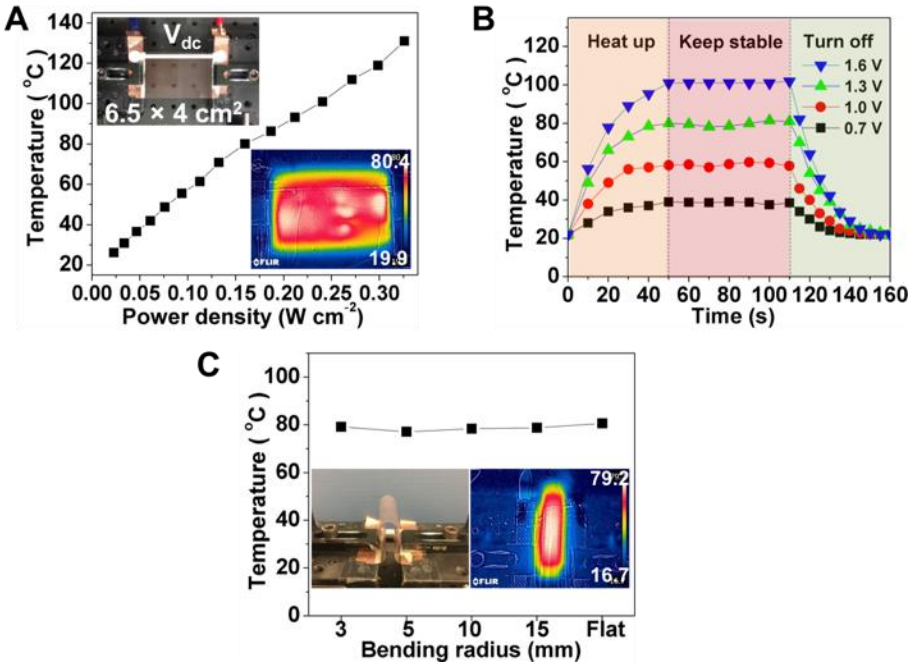


Figure 48. Demonstration of flexible transparent heater (FTH) based on flexible transparent electrode (FTE). (A) Maximum temperature of FTH at different supplied power density. Insert: digital and IR images of FTH. Size of transparent electrode: 6.5 cm × 4 cm. (B) Temperature profile of FTH versus time at different voltage applied. (C) Temperature variation of flexible transparent heater (FTH) at a constant input voltage (1.3 V) while bended at different radii.

Touch Screen Panels (TSPs)

A four-wire resistive touch screen panel (TSP) is successfully assembled by as-made metal mesh-based FTE. The demonstrated TSP consists of a top electrode of flexible metal mesh, and a bottom electrode of glass substrate coated with ITO and spacer array. Four copper tapes are used to connect these two electrodes to a touch screen controller (Figure 49, A-B). The top metal mesh and bottom ITO layer are separated to each other by spacer array when there is no pressure applied. The controller can record the position of pressure point and shows it at the corresponding position on the screen of computer. We tested the function of TSP by writing letters and Arabic numbers. The as-assembled device operates very well (Figure 49C).

However, the TSP fabricated here is just a rough demonstration, and the suggestion for further research is to enhance the resolution of this device. Since the pitch of metal mesh used in this TSP is 100 μm, which affected its resolution. To enhance the resolution of TSP, the metal mesh with small pitch can be used, or a conductive polymer (such as PEDOT:PSS) can be coated on the metal mesh to achieve a hybrid transparent electrode.

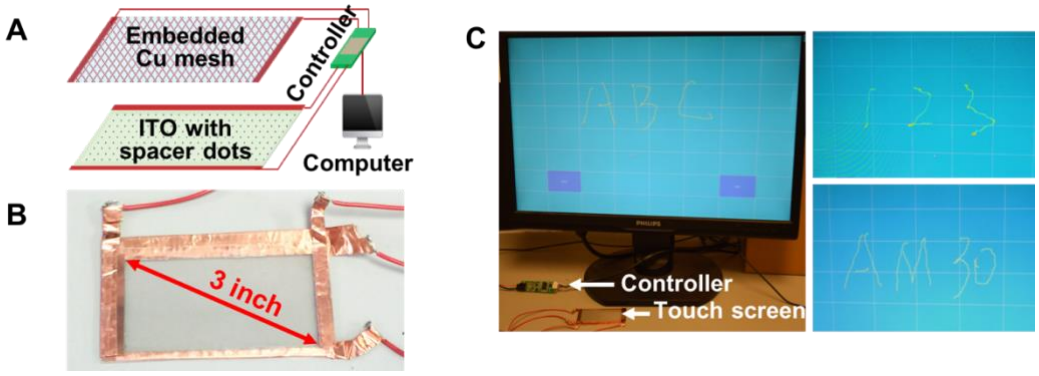


Figure 49. Demonstration of touch screen panel (TSP) based on flexible transparent electrode (FTE). (A) Schematic illustration of TSP using a top electrode of embedded Cu mesh and a bottom electrode of ITO with spacer array. (B) Photography of assembled TSP with 3-inch area. (C) Demonstration of assembled TSP by writing letters ABC (left), numbers 123 (top right), and AM 30 (30_{th} anniversary of Advanced Materials, bottom right).

Organic Light-Emitting Diodes (OLEDs)

A green organic light-emitting diode (OLED) was fabricated based on the ERT-based metal mesh. As shown in Figure 50A, the structure of the green OLED was: Ni mesh/ PEDOT:PSS (120 nm) (anode)/ N,N′-di(1-naphthyl)-N,N′-diphenyl-(1,1′-biphenyl)-4,4′-diamine (NPB, 60 nm) (HTL)/tris(8-hydroxyquinolinato)-aluminium (Alq_3, 60 nm) (EL & ETL)/lithium fluoride (LiF, 1 nm)/aluminium (Al, 100 nm) (cathode). The functions of PEDOT:PSS layer were current distribution uniformity and work function adjustment. The NPB, LiF, and Al layers are generally used in this kind of OLED device. The green OLED device based on the metal mesh could work well, even under the bending state (Figure 50B). This primary result indicated that the metal meshes show highly potential application

in the emerging flexible light-emitting devices. However, the performances (current density, luminance, etc.) of this metal mesh-based OLED device cannot comparable with those of ITO-based OLED device. Further research for optimization of performances needs to be carried out in the future.

There kinds of optoelectronic devices (flexible transparent heaters, touch screen panels, and organic light-emitting diodes) have been fabricated and work well based on the above results. The successful integration in the optoelectronic devices indicate that the metal mesh-based FTEs fabricated by ERT have an enormous potential for next-generation optoelectronics.

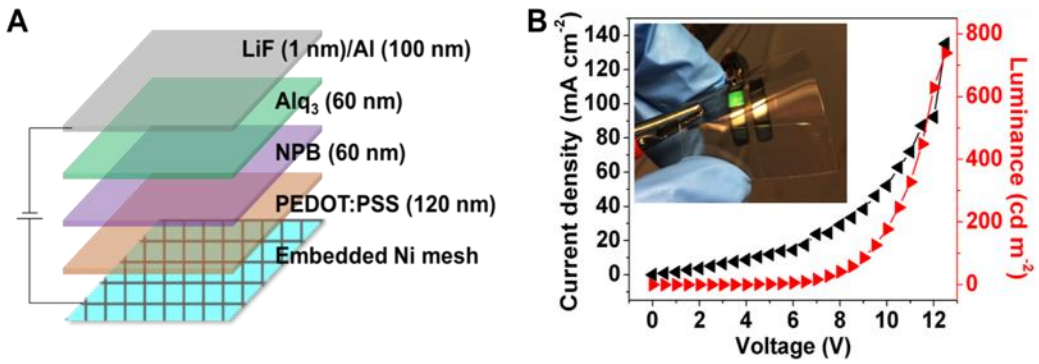


Figure 50. Demonstration of flexible organic light-emitting diode (OLED) based on flexible transparent electrode (FTE). (A) Schematic illustration of green OLED device with Ni mesh-based FTEs. (B) Characterization of current density and luminance of OLED device. Insert, OLED device operation under bending state.

6.2 Organic Electrochemical Transistors (OECTs) Based on ERT Method

6.2.1 Background of OECTs

Organic electrochemical transistors (OECTs) have been widely studied recently because their potential applications as the candidates of chemical and biological sensors. The advantages of OECTs include facile fabrication, simple structure, good biocompatibility, low cost, and mechanical flexibility, which make people consider OECTs can be used as disposable devices in the field healthcare.[197-199]

For the fabrication of metal source/drain electrodes, inkjet printing or screen printing is widely applied for the purpose of low cost and high throughput.[200-201] However, the resolutions of these printing techniques are limited, which cannot fabricate narrow channel for OECT devices and further affect negative on their performances. High-resolution photolithography is also used to pattern the source/drain electrodes.[202-203] However, this high-cost patterning process cannot meet the requirement of these low-cost, disposable devices. Therefore, as an alternative patterning technique, the high-resolution, high-throughput, low-cost ERT method show high potential to be applied in the fabrication of source/drain electrodes for OECT devices.

6.2.2 Fabrication of OECTs

The fabrication of OECT device was started from the fabrication of Au-based source/drain electrodes through ERT process. As shown in Figure 51A, the gap between source and drain electrodes (channel length) is about 2 μm. This patterning process was implemented through low-cost, all-solution ERT process. The structure of OECT device is schematically illustrated in Figure 51B. A layer

of PEDOT:PSS (p-type) was spin-coated on as-made Au electrodes and used as semiconductor layer. Electrolyte was 0.9 wt.% NaCl aqueous solution (saline solution), which was dropped on the top of semiconductor layer. Platinum (Pt) immersed in the electrolyte was the gate electrode.

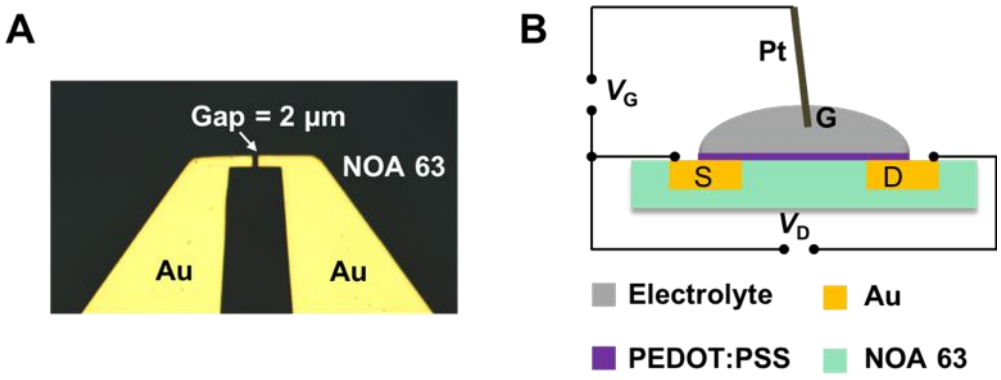


Figure 51. (A) Au source/drain electrodes with 2-μm gap fabricated by ERT method. (B) Schematic illustration of the structure of organic electrochemical transistor (OECT).

6.2.3 Characterization of OECTs

The output and transfer characteristics of as-assembled OECT device is shown in Figure 52. In this PEDOT:PSS-based OECT device works in the depletion mode. This p-type semiconductor film is controlled by the gate voltage. While a positive gate bias applied (V_G), cations in the electrolyte are injected into the semiconductor layer and the anions are compensated. This dedoping process decreases the conductivity of semiconductor layer, which results in the drop of the drain current (I_D).[204] The output and transfer characteristics shown in Figure 52 indicate that the

as-made OECT device can operate very well.

The transconductance (g_m) of OECT is defined by following equation:

$$g_m = \frac{\Delta I_D}{\Delta V_G}$$

Transconductance (g_m) is obviously the slope of I_D-V_G curve, which expresses the conversion of a modulation in the gate voltage ΔV_G to a modulation in the drain current ΔI_D. Transconductance is used as the figure of merit of OECT device.[203] The transconductance of as-made OECT device is ~15 mS (Figure 52C), which is superior than those results in previous reports.[203]

Furthermore, mechanical bending test was carried out on the as-made OECT device. The comparison of its output and transfer characteristics before and after bending test indicated the good mechanical flexibility of the device (Figure 52, A-B). Its transconductance also keeps at a high value (Figure 52C).

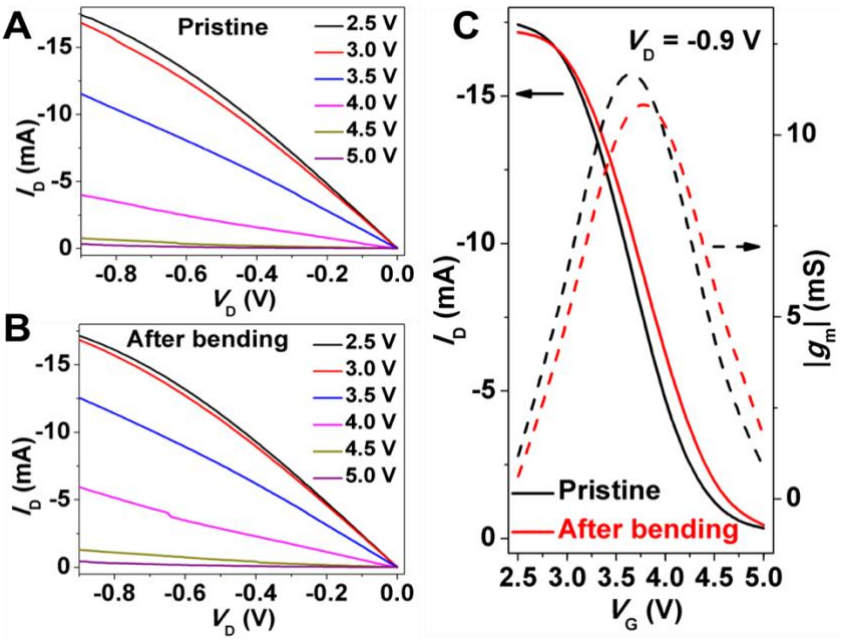


Figure 52. Output characteristics of as-assembled organic eletrochemical transistor (OECT) device (A) before and (B) after mechanical bending. (C) transfer characteristics and associated transconductances of OECT device before and after mechanical bending.

6.3 Micro-Supercapacitors (MSCs) Based on ERT Method

6.3.1 Background of MSCs

Micro-supercapacitors (MSCs) have attracted more and more attentions in recently years because of their potential applications in the miniaturized electronics and flexible/wearable on-chip microsystems.[205-206] There are two types of configurations for micro-supercapacitors, i.e., small-size sandwich (stacked) supercapacitor and in-plane interdigital micro-supercapacitor. Compared with the sandwich type, in-plane interdigital MSCs are preferred to be integrated in on-chip

electronic system.[207-209]

One of the big challenges in the micro-supercapacitors is to develop a reliable fabrication technique for patterning the interdigital electrodes (current collectors), depositing active materials, and integrating these components in the microelectronic systems.[206] In previous reports on fabrication of micro-supercapacitors, the conventional patterning techniques, such as photolithography, inkjet printing, etc., have been widely used.[206-207, 210-212] However, based on the aforementioned discussion and summary, these patterning techniques are either complicated or high cost. As a facile and low-cost patterning technique, ERT is a promising to be applied in the fabrication of micro-supercapacitors. In this section, the strategy of fabrication based on ERT and characterization of electrochemical performance of micro-supercapacitors were studied.

6.3.2 Fabrication of MSCs

The fabrication of micro-supercapacitors shows that ERT method can fabricate bilayer materials on one electrode. The fabrication process is shown in Figure 53A. Firstly, Cu and Au were subsequently electrochemically replicated on a template with interdigital electrode pattern. Then the Cu/Au bilayer pattern was transferred together on the flexible substrate (Figure 53B). This is the first time we demonstrate ERT method is applicable for fabricating patterns with bilayer materials in this research. After transferred on the flexible substrate, the bottom Au layer was acted as current collector. The top Cu layer was in-situ oxidized by the oxygen plasma (Cu_xO), which was used as active material for the micro-supercapacitor (Figure 53C).[213-214] Finally, the electrolyte (20 wt.% LiCl and 10%

wt.% PVA in H_2O) was coated on the surface of interdigital electrode.

Cu_xO was used in this research to demonstrate the applicability of ERT in fabricating bilayer patterns and the application in micro-supercapacitor. In principle, other kinds of active materials for micro-supercapacitors, such as NiO, PPy, PANi, MnO_2, etc., are also able to be integrated in the ERT process and demonstrate the applications in the area of energy storage, which are suggested to be studied systematically in the future research.

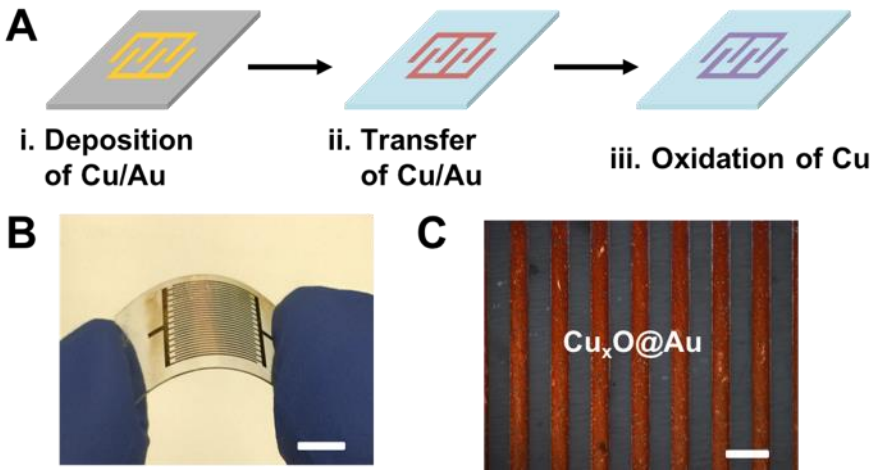


Figure 53. (A) Fabrication process of micro-supercapacitor (MSC) based on ERT method: i) Au and Cu electrodeposited subsequently on the interdigital Au-patterned template; ii) Au/Cu interdigital pattern transferred into the NOA 63; iii) in-situ oxidation of Cu to form copper oxide as active material for micro-supercapacitor, the Au layer acted as current collector. (B) Digital image of micro-supercapacitor at bending state. Scale bar, 5 mm. (C) Optical microscopic image of micro-supercapacitor. Bilayer, copper oxide (Cu_xO, top)/Au (bottom). Scale bar, 200 μm.

6.3.3 Characterization of MSCs

The electrochemical performance of as-made micro-supercapacitor is shown in Figure 54. The cyclic voltammetry (CV) curves indicated the micro-supercapacitor device can work well. The areal capacitances tested at different scanning rates were about 1 mF/cm2 (Figure 54B). The mechanical flexibility of micro-supercapacitor was studied (as shown in Figure 54C). The CV curves tested before and after mechanical bending test indicated its stability. It should be noted that the capacitance of as-made micro-supercapacitor is relatively low, mainly because of

the low mass-loading of active materials. The optimization study for enhancement of performance is suggested to carry out in the future research.

The demonstration of micro-supercapacitor not only shows the application of ERT technique in the field of micro energy storage, but also indicates that ERT method can fabricate bilayer or multilayer patterns. The latter significance indicates that ERT is promising for more potential applications in the future research.

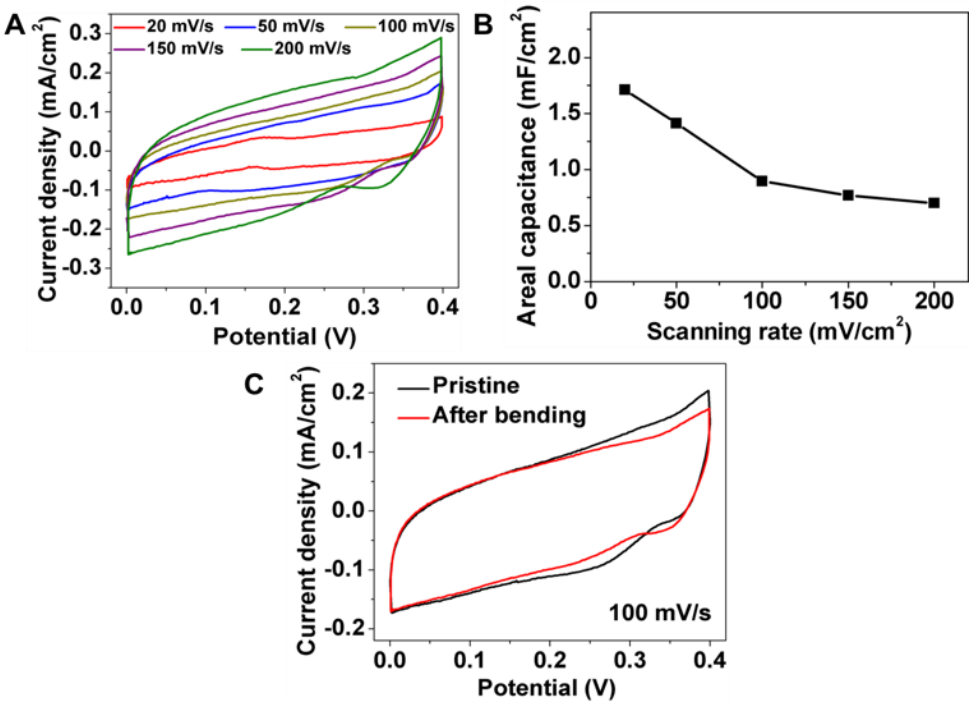


Figure 54. (A) CV curves of micro-supercapacitor (MSC) at different scanning rate: 20, 50, 100, 150, and 200 mV/s. (B) Specific capacitance of micro-supercapacitor. (C) CV curves of micro-supercapacitor before and after mechanical bending. Areal capacitances before and after bending are 0.90 mF/cm2 and 0.83 mF/cm2, repsectively. Scanning rate, 100 mV/s.

6.4 Conclusions

Generation of pattern is a fundamental step in the micro/nanofabrication processes. Patterning techniques are widely applied in the academic and industrial fields. ERT, as an advanced patterning technique firstly developed in this research, showed tremendous potential applications in a wide variety of fields. As a proof-of-concept, several typical electrodes with different patterns were fabricated by ERT process and integrated in the electronic devices. Flexible transparent electrode (FTE) as a typical demonstration of the application of ERT has been systematically studied in terms of fabrication parameters, performance, and integration in the optoelectronic devices. The metal mesh-based FTEs fabricated by ERT possessed the attributes of high thickness of metal layer and embedded structure, which allowed as-made FTEs to achieve excellent electrical and optical performance, mechanical flexibility, and environmental stability. Three kinds of optoelectronic devices, flexible transparent electrodes, touch screen panels, and organic light-emitting diodes, were successfully assembled based on the ERT-based metal meshes. Source/drain (S/D) electrodes and interdigital electrodes (IDEs) were both fabricated by ERT processes for demonstration of the applications in organic electrochemical transistors and micro-supercapacitors. Even though the performances of these two devices are still to be optimized, the preliminary results indicated that both two types of devices could operate smoothly and ERT is an effective patterning technique to fabricate microstructures in these fields.

Chapter 7: Conclusions and Suggestions for Future Research

7.1 Conclusions

In this thesis, electrochemical replication and transfer (ERT) has been developed as an alternative patterning technique. Its ability to fabricate arbitrary geometric shapes of patterns with a wide variety of materials on various flexible/wearable substrates was investigated. The mechanism of ERT process, i.e., electrochemical replication and transfer was analyzed comprehensively. Furthermore, the applications of ERT technique were demonstrated by fabricating typical electrodes with corresponding patterns based on ERT process and then integrating them in the electronic devices. The main achievement in each chapter is summarized as following.

In chapter 4, the fabrication process, resolution, throughput, and cost of ERT technique were illustrated and discussed. ERT as an alternative patterning technique, only consists of two facile steps: 1) selective electrodeposition of target materials on a pre-made Au template (electrochemical replication), and 2) transfer of the patterned materials from the Au template to the flexible substrate with a photo-curable binder, while the Au template is reused for the next patterning process. The minimum feature sizes of patterns based on this all-solution process were 200 nm of linewidth, 50 nm of gap, and 50 nm of thickness. Particularly, the additive, parallel patterning mode of all-solution ERT process allows to fabricate

multi-scale patterns on one large-scale substrate simultaneously, which overcomes the tradeoff among the resolution, throughput and cost of conventional patterning techniques. Furthermore, ERT is applicable to arbitrary geometric patterns and a wide variety of target materials (metals, metal oxides, semiconductors, conductive polymers), and flexible substrates (plastics, papers, textiles).

In chapter 5, the mechanism analysis of electrochemical replication and transfer (ERT) process was discussed in detail. In the step of electrochemical replication, the two necessary conditions are the rational structure of template and optimization of current density. The structure of template is a conductive Au pattern on a semiconductor substrate, where target materials are preferred to be deposited on the region of Au pattern. Optimized current density is controlled at the range of 1.0 – 2.0 mA/cm2. Either relatively low or relatively high current density may result in the failure of electrochemical replication of target material on Au template. The success of transfer step is attributed to the surface modification of self-assembled monolayers (SAMs) on Au-patterned template and the use of photo-curable polymer as the binder. The self-assembled monolayers (SAMs), modified on the surface of Au pattern before the deposition of target materials, act as the anti-adhesive layers to decrease the interaction at the interface of Au and target materials, which not only facilitate the mechanical peeling off of target materials, but also improve the reusability of the Au template. The use of photo-curable polymer as binder could make the transfer easy through its strong interaction with target materials because of its adhesive property.

In chapter 6, the applications of electrochemical replication and transfer (ERT) technique were demonstrated. ERT technique was used to fabricate three types of

typical electrodes (flexible transparent electrodes (FTEs), source/drain (S/D) electrodes, and interdigital electrodes (IDEs)), which were further integrated in the electronic devices. The metal mesh-based FTEs fabricated by ERT showed excellent electrical and optical properties, which were better than those of commercial ITO and other reported transparent electrodes. On the other hand, as-made FTEs showed superior mechanical flexibility and environmental stability. Three kinds of optoelectronic devices, i.e., flexible transparent electrodes, touch screen panels, and organic light-emitting diodes, are successfully assembled based on the metal mesh-based FTEs. Furthermore, ERT was used to fabricate source/drain (S/D) electrodes and interdigital electrodes (IDEs), which were basic components in organic electrochemical transistors (OECTs) and micro-supercapacitors (MSCs), respectively. The preliminary results indicated that OECTs and MSCs both operated smoothly and ERT is an effective patterning technique to fabricate microstructures in the fields of sensor and energy storage.

To be brief, electrochemical replication and transfer (ERT) has been developed as an alternative patterning technique with the advantages of high resolution, high throughput, and low cost. It could fabricate arbitrary geometric shapes of patterns with a wide variety of materials on various flexible/wearable substrates. The mechanism of ERT process are relevant to the rational structure of template, optimized current density, surface modification, and photo-curable binders. The applications of ERT technique demonstrated in this thesis included flexible transparent electrodes, source/drain electrodes, and interdigital electrodes and their integrations in the electronic devices.

7.2 Suggestions for Future Research

Electrochemical replication and transfer (ERT) as a new patterning technique is firstly developed in this research. There are still a lot of expanded research in the future.

Firstly, it is suggested that research on the optimization of some aforementioned devices should be carried out. In the chapter 6, flexible organic light-emitting diodes (OLEDs), organic electrochemical transistors (OECTs), and micro-supercapacitors (MSCs) have been successfully fabricated. However, their performances are still to be optimized.

Secondly, more other applications based on ERT techniques should be studied. The ERT-based flexible transparent electrodes show excellent opto-electrical performance and ultralow surface roughness, which are promising for the application in the energy harvest, especially the emerging, low-cost organic and perovskite solar cells.[215-217] On the other hand, ERT technique is promising to be used in the field of plasmonics. In previous reports, plasmonic devices with sub-micrometer or nanometer patterns were usually fabricated by electron beam lithography and nanoimprint lithography with expensive equipment and tedious processes.[218-220] These challenges are expected to be overcome by the low-cost and facile ERT patterning technique. Furthermore, Au and PMMA are both biocompatible and the Au patterns on PMMA fabricated by ERT are promising for the application in the biological research, such as study of controlling cell behaviors.[4, 221]

Thirdly, ERT process should extend its applicability to stretchable substrates. In the aforementioned results, target materials are all transferred to the flexible substrates, which cannot mechanically stretch. As an emerging research field, stretchable electronics shows more advantages than flexible/bendable electronics on the applications of wearable healthcare devices.[155, 222-224] Therefore, it is of great significance to develop ERT process on stretchable substrates, which will further extend its applications.

References

1. Kim, D. H.; Lu, N. S.; Ma, R.; Kim, Y. S.; Kim, R. H.; Wang, S. D.; Wu, J.; Won, S. M.; Tao, H.; Islam, A.; Yu, K. J.; Kim, T. I.; Chowdhury, R.; Ying, M.; Xu, L. Z.; Li, M.; Chung, H. J.; Keum, H.; McCormick, M.; Liu, P.; Zhang, Y. W.; Omenetto, F. G.; Huang, Y. G.; Coleman, T.; Rogers, J. A., Epidermal Electronics. *Science* **2011,** *333* (6044), 838-843.

2. Zhang, H.; Rogers, J. A., Recent Advances in Flexible Inorganic Light Emitting Diodes: From Materials Design to Integrated Optoelectronic Platforms. *Adv. Opt. Mater.* **2019,** *7* (2), 1800936.

3. Rosi, N. L.; Mirkin, C. A., Nanostructures in Biodiagnostics. *Chem. Rev.* **2005,** *105* (4), 1547-1562.

4. Chen, L.; Yan, C.; Zheng, Z., Functional Polymer Surfaces for Controlling Cell Behaviors. *Mater. Today* **2018,** *21* (1), 38-59.

5. Pimpin, A.; Srituravanich, W., Review on Micro- and Nanolithography Techniques and Their Applications. *Eng. J.* **2012,** *16* (1), 37-56.

6. Lee, H. E.; Park, J. H.; Kim, T. J.; Im, D.; Shin, J. H.; Kim, D. H.; Mohammad, B.; Kang, I.-S.; Lee, K. J., Novel Electronics for Flexible and Neuromorphic Computing. *Adv. Funct. Mater.* **2018,** *28* (32), 1801690.

7. Ito, T.; Okazaki, S., Pushing the limits of lithography. *Nature* **2000,** *406* (6799), 1027-1031.

8. Li, L.; Liu, X.; Pal, S.; Wang, S.; Ober, C. K.; Giannelis, E. P., Extreme ultraviolet resist materials for sub-7 nm patterning. *Chem. Soc. Rev.* **2017,** *46* (16), 4855-4866.

9. Manfrinato, V. R.; Zhang, L.; Su, D.; Duan, H.; Hobbs, R. G.; Stach, E. A.; Berggren, K. K., Resolution Limits of Electron-Beam Lithography toward the Atomic Scale. *Nano Lett.* **2013,** *13* (4), 1555-1558.

10. Pease, R. F.; Chou, S. Y., Lithography and other patterning techniques for future electronics. *Proc. IEEE* **2008,** *96* (2), 248-270.

11. Fukuda, K.; Someya, T., Recent Progress in the Development of Printed Thin-Film Transistors and Circuits with High-Resolution Printing Technology. *Adv. Mater.* **2017,** *29* (25).

12. Fukuda, K.; Takeda, Y.; Yoshimura, Y.; Shiwaku, R.; Tran, L. T.; Sekine, T.; Mizukami, M.; Kumaki, D.; Tokito, S., Fully-printed high-performance organic thin-film transistors and circuitry on one-micron-thick polymer films. *Nat. Commun.* **2014,** *5*.

13. Xu, T.; Wu, Y. K.; Luo, X. G.; Guo, L. J., Plasmonic nanoresonators for high-resolution colour filtering and spectral imaging. *Nat. Commun.* **2010,** *1*.

14. Alsteens, D.; Gaub, H. E.; Newton, R.; Pfreundschuh, M.; Gerber, C.; Muller, D. J., Atomic force microscopy-based characterization and design of biointerfaces. *Nat. Rev. Mater.* **2017,** *2* (5).

15. Pala, N.; Karabiyik, M., Electron Beam Lithography (EBL). In *Encyclopedia of Nanotechnology*, Bhushan, B., Ed. Springer Netherlands: Dordrecht, 2016; pp 1033-1057.

16. Khan, Y.; Pavinatto, F. J.; Lin, M. C.; Liao, A.; Swisher, S. L.; Mann, K.; Subramanian, V.; Maharbiz, M. M.; Arias, A. C., Inkjet-Printed Flexible Gold Electrode Arrays for Bioelectronic Interfaces. *Adv. Funct. Mater.* **2016,** *26* (7), 1004-1013.

17. Naulleau, P., Optical Lithography. In *Nanofabrication handbook*, S Cabrini, S. K., Ed. CRC Press: 2012; pp 127-139.

18. Ziaie, B.; Baldi, A.; Atashbar, M. Z., Introduction to Micro-/Nanofabrication. In *Springer Handbook of Nanotechnology*, Bhushan, B., Ed. Springer Berlin Heidelberg: Berlin, Heidelberg, 2010; pp 231-269.

19. van Assenbergh, P.; Meinders, E.; Geraedts, J.; Dodou, D., Nanostructure and Microstructure Fabrication: From Desired Properties to Suitable Processes. *Small* **2018,** *14* (20), 1703401.

20. Thoms, S., Electron Beam Lithography. In *Nanofabrication handbook*, S Cabrini, S. K., Ed. CRC Press: 2012; pp 9-40.

21. Tseng, A. A.; Kuan, C.; Chen, C. D.; Ma, K. J., Electron beam lithography in nanoscale fabrication: recent development. *IEEE Transactions on Electronics Packaging Manufacturing* **2003,** *26* (2), 141-149.

22. Chou, S. Y.; Krauss, P. R.; Renstrom, P. J., Imprint of sub‐25 nm vias and trenches in polymers. *Appl. Phys. Lett.* **1995,** *67* (21), 3114-3116.

23. Chou, S. Y.; Krauss, P. R.; Renstrom, P. J., Imprint Lithography with 25-Nanometer Resolution. *Science* **1996,** *272* (5258), 85-87.

24. Chou, S. Y., Nanoimprint Lithography. In *Nanofabrication handbook*, S Cabrini, S. K., Ed. CRC Press: 2012; pp 187-206.

25. Schift, H.; Kristensen, A., Nanoimprint Lithography – Patterning of Resists Using Molding. In *Springer Handbook of Nanotechnology*, Bhushan, B., Ed. Springer Berlin Heidelberg: Berlin, Heidelberg, 2010; pp 271-312.

26. Parashkov, R.; Becker, E.; Riedl, T.; Johannes, H.; Kowalsky, W., Large Area Electronics Using Printing Methods. *Proc. IEEE* **2005,** *93* (7), 1321-1329.

27. Kang, B.; Lee, W. H.; Cho, K., Recent Advances in Organic Transistor Printing Processes. *ACS Appl. Mater. Interfaces* **2013,** *5* (7), 2302-2315.

28. Subramanian, V.; Cen, J.; Vornbrock, A. d. l. F.; Grau, G.; Kang, H.; Kitsomboonloha, R.; Soltman, D.; Tseng, H., High-Speed Printing of Transistors: From Inks to Devices. *Proc. IEEE*

2015, *103* (4), 567-582.

29. Coatanéa, E.; Kantola, V.; Kulovesi, J.; Lahti, L.; Lin, R.; Zavodchikova, M., Printed electronics, now and future. *Bit Bang–Rays to the Future* **2009**, 63-102.

30. Moonen, P. F.; Yakimets, I.; Huskens, J., Fabrication of Transistors on Flexible Substrates: from Mass-Printing to High-Resolution Alternative Lithography Strategies. *Adv. Mater.* **2012,** *24* (41), 5526-5541.

31. Hu, G.; Kang, J.; Ng, L. W.; Zhu, X.; Howe, R. C.; Jones, C. G.; Hersam, M. C.; Hasan, T., Functional Inks and Printing of Two-dimensional Materials. *Chem. Soc. Rev.* **2018,** *47* (9), 3265-3300.

32. Khan, S.; Lorenzelli, L.; Dahiya, R. S., Technologies for printing sensors and electronics over large flexible substrates: a review. *IEEE Sens. J.* **2015,** *15* (6), 3164-3185.

33. Suganuma, K., *Introduction to Printed Electronics*. Springer Science & Business Media: 2014; Vol. 74.

34. Cen, J.; Kitsomboonloha, R.; Subramanian, V., Cell Filling in Gravure Printing for Printed Electronics. *Langmuir* **2014,** *30* (45), 13716-13726.

35. Wu, W., Inorganic Nanomaterials for Printed Electronics: a Review. *Nanoscale* **2017,** *9* (22), 7342-7372.

36. Vollmann, H. W., Neue Technologien zur filmlosen Herstellung von Druckformen. *Angew. Chem.* **1980,** *92* (2), 95-106.

37. Moonen, P. *Alternative lithography strategies for flexible electronics*. PhD, University of Twente, Enschede, 2012.

38. Xia, Y. N.; Whitesides, G. M., Soft lithography. *Angew. Chem. Int. Ed.* **1998,** *37* (5), 550-575.

39. Xia, Y. N.; Whitesides, G. M., Soft Lithography. *Annu. Rev. Mater. Sci.* **1998,** *28*, 153-184.

40. Rogers, J. A.; Nuzzo, R. G., Recent progress in soft lithography. *Mater. Today* **2005,** *8* (2), 50-56.

41. Loo, Y.-L.; Willett, R. L.; Baldwin, K. W.; Rogers, J. A., Interfacial Chemistries for Nanoscale Transfer Printing. *J. Am. Chem. Soc.* **2002,** *124* (26), 7654-7655.

42. Loo, Y.-L.; Lang, D. V.; Rogers, J. A.; Hsu, J. W. P., Electrical Contacts to Molecular Layers by Nanotransfer Printing. *Nano Lett.* **2003,** *3* (7), 913-917.

43. Menard, E.; Bilhaut, L.; Zaumseil, J.; Rogers, J. A., Improved Surface Chemistries, Thin Film Deposition Techniques, and Stamp Designs for Nanotransfer Printing. *Langmuir* **2004,** *20* (16), 6871-6878.

44. Chanda, D.; Shigeta, K.; Gupta, S.; Cain, T.; Carlson, A.; Mihi, A.; Baca, A. J.; Bogart, G. R.;

Braun, P.; Rogers, J. A., Large-area flexible 3D optical negative index metamaterial formed by nanotransfer printing. *Nat. Nanotechnol.* **2011,** *6*, 402.

45. Meitl, M. A.; Zhu, Z.-T.; Kumar, V.; Lee, K. J.; Feng, X.; Huang, Y. Y.; Adesida, I.; Nuzzo, R. G.; Rogers, J. A., Transfer printing by kinetic control of adhesion to an elastomeric stamp. *Nat. Mater.* **2005,** *5*, 33.

46. Carlson, A.; Bowen, A. M.; Huang, Y.; Nuzzo, R. G.; Rogers, J. A., Transfer printing techniques for materials assembly and micro/nanodevice fabrication. *Adv. Mater.* **2012,** *24* (39), 5284-5318.

47. Loo, Y.-L.; Willett, R. L.; Baldwin, K. W.; Rogers, J. A., Additive, nanoscale patterning of metal films with a stamp and a surface chemistry mediated transfer process: Applications in plastic electronics. *Appl. Phys. Lett.* **2002,** *81* (3), 562-564.

48. Piner, R. D.; Zhu, J.; Xu, F.; Hong, S. H.; Mirkin, C. A., "Dip-pen" nanolithography. *Science* **1999,** *283* (5402), 661-663.

49. Nelson, B. A.; King, W. P.; Laracuente, A. R.; Sheehan, P. E.; Whitman, L. J., Direct deposition of continuous metal nanostructures by thermal dip-pen nanolithography. *Appl. Phys. Lett.* **2006,** *88* (3), 033104.

50. Cai, Y.; Ocko, B. M., Electro Pen Nanolithography. *J. Am. Chem. Soc.* **2005,** *127* (46), 16287-16291.

51. Kim, K.-H.; Moldovan, N.; Espinosa, H. D., A Nanofountain Probe with Sub-100 nm Molecular Writing Resolution. *Small* **2005,** *1* (6), 632-635.

52. Salaita, K.; Wang, Y. H.; Mirkin, C. A., Applications of dip-pen nanolithography. *Nat. Nanotechnol.* **2007,** *2* (3), 145-155.

53. Mack, C. A., Field guide to optical lithography. In *Field Guides*, Grievenkamp, J., Ed. SPIE Press: Bellingham, WA, 2006; Vol. 6.

54. Mack, C., Resolution Enhancement Technologies. In *Fundamental Principles of Optical Lithography*, Mack, C., Ed. 2007; pp 411-456.

55. Moore, G. E., Cramming more components onto integrated circuits. McGraw-Hill New York, NY, USA:: 1965.

56. Wagner, C.; Harned, N., Lithography gets extreme. *Nat. Photonics* **2010,** *4*, 24.

57. Levinson, H. J. In *Overview of lithography: challenges and metrologies*, AIP Conf. Proc., AIP: 2003; pp 365-370.

58. Li, L.; Liu, X.; Pal, S.; Wang, S. L.; Ober, C. K.; Giannelis, E. P., Extreme ultraviolet resist materials for sub-7 nm patterning. *Chem. Soc. Rev.* **2017,** *46* (16), 4855-4866.

59. Bordonaro, G. J., DUV Photolithography and Materials. *Encyclopedia of Nanotechnology*

2012, 590-604.

60. Jürgens, D. In *EUV Lithography Optics: Status and Outlook*, SEMICON EUROPA 2018, München, München, 2018.

61. Lawson, R. A.; Robinson, A. P. G., Chapter 1 - Overview of materials and processes for lithography. In *Frontiers of Nanoscience*, Robinson, A.; Lawson, R., Eds. Elsevier: 2016; Vol. 11, pp 1-90.

62. Owa, S.; Nagasaka, H., *Immersion lithography: its potential performance and issues*. SPIE: 2003; Vol. 5040.

63. Young, C. D. In *EUV lithography drives Moore's law well into the next decade*, BAML 2018 APAC TMT Conference, Taipei, Taiwan, Taipei, Taiwan, 2018.

64. De Simone, D.; Vesters, Y.; Vandenberghe, G., Photoresists in extreme ultraviolet lithography (EUVL). *Adv. Opt. Techn.* **2017,** *6* (3-4), 163-172.

65. Inoue, S.; Amano, T.; Itani, T.; Watanabe, H.; Mori, I.; Watanabe, T.; Kinoshita, H.; Miyai, H.; Hatakeyama, M., Development of core technologies on EUV mask and resist for sub-20-nm half pitch generation. *Adv. Opt. Techn.* **2012,** *1* (4), 269-278.

66. Silverman, P. J., Extreme ultraviolet lithography: overview and development status. *J. Microlith., Microfab., Microsyst.* **2005,** *4* (1), 1-5, 5.

67. Rastegar, A.; Eichenlaub, S.; Kadaksham, A. J.; Lee, B.; House, M.; Huh, S.; Cha, B.; Yun, H.; Mochi, I.; Goldberg, K., *Particle removal challenges of EUV patterned masks for the sub-22nm HP node*. SPIE: 2010; Vol. 7636.

68. Mojarad, N.; Gobrecht, J.; Ekinci, Y., Interference lithography at EUV and soft X-ray wavelengths: Principles, methods, and applications. *Microelectron. Eng.* **2015,** *143*, 55-63.

69. Barnola, S.; Posseme, N.; Landis, S.; Darnon, M., 3 - Patterning Challenges in Microelectronics. In *Plasma Etching Processes for CMOS Devices Realization*, Posseme, N., Ed. Elsevier: 2017; pp 59-94.

70. Schuegraf, K.; Abraham, M. C.; Brand, A.; Naik, M.; Thakur, R., Semiconductor Logic Technology Innovation to Achieve Sub-10 nm Manufacturing. *IEEE Journal of the Electron Devices Society* **2013,** *1* (3), 66-75.

71. Schoot, J. v.; Schenau, K. v. I.; Valentin, C.; Migura, S., *EUV lithography scanner for sub-8nm resolution*. SPIE: 2015; Vol. 9422.

72. Fan, D.; Ekinci, Y., Photolithography reaches 6 nm half-pitch using extreme ultraviolet light. *J. Microlith., Microfab., Microsyst.* **2016,** *15* (3), 1-7, 7.

73. TSMC, TSMC and OIP Ecosystem Partners Deliver Industry's First Complete Design

Infrastructure for 5nm Process Technology. TSMC, Ed. Hsinchu, Taiwan, 2019.

74. Hecht, J., EUV lithography has yet to find its way into the fab. *Laser Focus World* **2013,** *49* (5), 55-59.

75. Groves, T. R., Electron beam lithography. In *Nanolithography*, Feldman, M., Ed. Woodhead Publishing: 2014; pp 80-115.

76. Hubenthal, F., Noble Metal Nanoparticles: Synthesis and Optical Properties. In *Comprehensive Nanoscience and Technology*, Andrews, D. L.; Scholes, G. D.; Wiederrecht, G. P., Eds. Academic Press: Amsterdam, 2011; pp 375-435.

77. Chapter 5 - Manipulation and Patterning of Surfaces (Nanolithography). In *Fundamentals and Applications of Nano Silicon in Plasmonics and Fullerines*, Nayfeh, M., Ed. Elsevier: 2018; pp 89-137.

78. Nagaraj, K. S.; Sangeeth, K.; Hegde, G. M., *Nanostructure patterning on flexible substrates using electron beam lithography*. SPIE: 2014; Vol. 9234.

79. Joo, J.; Chow, B. Y.; Jacobson, J. M., Nanoscale Patterning on Insulating Substrates by Critical Energy Electron Beam Lithography. *Nano Lett.* **2006,** *6* (9), 2021-2025.

80. Grigorescu, A. E.; Krogt, M. C. v. d.; Hagen, C. W., *Sub-10-nm structures written in ultra-thin HSQ resist layers using electron-beam lithography*. SPIE: 2007; Vol. 6519.

81. Duan, H.; Manfrinato, V. R.; Yang, J. K. W.; Winston, D.; Cord, B. M.; Berggren, K. K., Metrology for electron-beam lithography and resist contrast at the sub-10 nm scale. *J. Vac. Sci. Technol. B* **2010,** *28* (6), C6H11-C6H17.

82. Chen, W.; Ahmed, H., Fabrication of 5 – 7 nm wide etched lines in silicon using 100 keV electron - beam lithography and polymethylmethacrylate resist. *Appl. Phys. Lett.* **1993,** *62* (13), 1499-1501.

83. Yang, J. K. W.; Berggren, K. K., Using high-contrast salty development of hydrogen silsesquioxane for sub-10 - nm half-pitch lithography. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* **2007,** *25* (6), 2025-2029.

84. Guo, L. J., Nanoimprint Lithography: Methods and Material Requirements. *Adv. Mater.* **2007,** *19* (4), 495-513.

85. Chou, S. Y.; Krauss, P. R.; Zhang, W.; Guo, L.; Zhuang, L., Sub-10 nm imprint lithography and applications. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena* **1997,** *15* (6), 2897-2904.

86. Austin, M. D.; Ge, H.; Wu, W.; Li, M.; Yu, Z.; Wasserman, D.; Lyon, S. A.; Chou, S. Y., Fabrication of 5nm linewidth and 14nm pitch features by nanoimprint lithography. *Appl. Phys. Lett.* **2004,** *84* (26), 5299-5301.

87. Sirringhaus, H.; Kawase, T.; Friend, R. H.; Shimoda, T.; Inbasekaran, M.; Wu, W.; Woo, E.

P., High-Resolution Inkjet Printing of All-Polymer Transistor Circuits. *Science* **2000,** *290* (5499), 2123-2126.

88. Park, J. U.; Hardy, M.; Kang, S. J.; Barton, K.; Adair, K.; Mukhopadhyay, D. K.; Lee, C. Y.; Strano, M. S.; Alleyne, A. G.; Georgiadis, J. G.; Ferreira, P. M.; Rogers, J. A., High-resolution electrohydrodynamic jet printing. *Nat. Mater.* **2007,** *6* (10), 782-789.

89. Richner, P.; Kress, S. J. P.; Norris, D. J.; Poulikakos, D., Charge effects and nanoparticle pattern formation in electrohydrodynamic NanoDrip printing of colloids. *Nanoscale* **2016,** *8* (11), 6028-6034.

90. Zhang, B.; He, J. K.; Li, X.; Xu, F. Y.; Li, D. C., Micro/nanoscale electrohydrodynamic printing: from 2D to 3D. *Nanoscale* **2016,** *8* (34), 15376-15388.

91. An, B. W.; Kim, K.; Lee, H.; Kim, S.-Y.; Shim, Y.; Lee, D.-Y.; Song, J. Y.; Park, J.-U., High-Resolution Printing of 3D Structures Using an Electrohydrodynamic Inkjet with Multiple Functional Inks. *Adv. Mater.* **2015,** *27* (29), 4322-4328.

92. Galliker, P.; Schneider, J.; Eghlidi, H.; Kress, S.; Sandoghdar, V.; Poulikakos, D., Direct printing of nanostructures by electrostatic autofocussing of ink nanodroplets. *Nat. Commun.* **2012,** *3*.

93. Kim, S.; Sojoudi, H.; Zhao, H.; Mariappan, D.; McKinley, G. H.; Gleason, K. K.; Hart, A. J., Ultrathin High-Resolution Flexographic Printing Using Nanoporous Stamps. *Sci. Adv.* **2016,** *2* (12).

94. Garcia, R.; Knoll, A. W.; Riedo, E., Advanced scanning probe lithography. *Nat. Nanotechnol.* **2014,** *9*, 577.

95. Tennant, D. M., Limits of Conventional Lithography. In *Nanotechnology*, Springer: 1999; pp 161-205.

96. Pfeiffer, H. C., *Advanced e-beam systems for manufacturing*. SPIE: 1992; Vol. 1671.

97. Waskiewicz, W. K.; Biddick, C. J.; Blakey, M. I.; Brady, K. J.; Camarda, R. M.; Connelly, W. F.; Crorken, A. H.; Custy, J. P.; DeMarco, R.; Farrow, R. C.; Felker, J. A.; Fetter, L. A.; Freeman, R. R.; Harriott, L. R.; Hopkins, L. C.; Huggins, H. A.; Kasica, R. J.; Knurek, C. S.; Kraus, J. S.; Liddle, J. A.; Mkrtchyan, M. M.; Novembre, A. E.; Jr., M. L. P.; Rutberg, L.; Wade, H. H.; Watson, P. G.; Werder, K. S.; Windt, D. L.; Tarascon-Auriol, R. G.; Berger, S. D.; Bowler, S. W., *SCALPEL proof-of-concept system: preliminary lithography results*. SPIE: 1997; Vol. 3048.

98. Harriott, L. R. In *SCALPEL: projection electron beam lithography*, Proceedings of the 1999 Particle Accelerator Conference (Cat. No.99CH36366), 27 March-2 April 1999; 1999; pp 595-599 vol.1.

99. Berger, S. D.; Gibson, J. M.; Camarda, R. M.; Farrow, R. C.; Huggins, H. A.; Kraus, J. S.; Liddle, J. A., Projection electron‐beam lithography: A new approach. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and*

Phenomena **1991,** *9* (6), 2996-2999.

100. Boer, G. d.; Dansberg, M. P.; Jager, R.; Peijster, J. J. M.; Slot, E.; Steenbrink, S. W. H. K.; Wieland, M. J., *MAPPER: progress toward a high-volume manufacturing system*. SPIE: 2013; Vol. 8680.

101. Hoefflinger, B., Nanolithographies. In *CHIPS 2020 VOL. 2: New Vistas in Nanoelectronics*, Höfflinger, B., Ed. Springer International Publishing: Cham, 2016; pp 149-163.

102. Ginger, D. S.; Zhang, H.; Mirkin, C. A., The Evolution of Dip-Pen Nanolithography. *Angew. Chem. Int. Ed.* **2004,** *43* (1), 30-45.

103. Hong, S.; Mirkin, C. A., A Nanoplotter with Both Parallel and Serial Writing Capabilities. *Science* **2000,** *288* (5472), 1808-1811.

104. Salaita, K.; Lee, S. W.; Wang, X.; Huang, L.; Dellinger, T. M.; Liu, C.; Mirkin, C. A., Sub-100 nm, Centimeter-Scale, Parallel Dip-Pen Nanolithography. *Small* **2005,** *1* (10), 940-945.

105. Salaita, K.; Wang, Y.; Fragala, J.; Vega, R. A.; Liu, C.; Mirkin, C. A., Massively Parallel Dip–Pen Nanolithography with 55 000-Pen Two-Dimensional Arrays. *Angew. Chem. Int. Ed.* **2006,** *45* (43), 7220-7223.

106. Huo, F. W.; Zheng, Z. J.; Zheng, G. F.; Giam, L. R.; Zhang, H.; Mirkin, C. A., Polymer pen lithography. *Science* **2008,** *321* (5896), 1658-1660.

107. Huo, F. W.; Zheng, G. F.; Liao, X.; Giam, L. R.; Chai, J. A.; Chen, X. D.; Shim, W. Y.; Mirkin, C. A., Beam pen lithography. *Nat. Nanotechnol.* **2010,** *5* (9), 637-640.

108. Shim, W.; Braunschweig, A. B.; Liao, X.; Chai, J.; Lim, J. K.; Zheng, G.; Mirkin, C. A., Hard-tip, soft-spring lithography. *Nature* **2011,** *469*, 516.

109. He, Q.; Tan, C.; Zhang, H., Recent Advances in Cantilever-Free Scanning Probe Lithography: High-Throughput, Space-Confined Synthesis of Nanostructures and Beyond. *ACS Nano* **2017,** *11* (5), 4381-4386.

110. Abbel, R.; Galagan, Y.; Groen, P., Roll-to-Roll Fabrication of Solution Processed Electronics. *Adv. Eng. Mater.* **2018,** *20* (8), 1701190.

111. Park, J.; Shin, K.; Lee, C., Roll-to-Roll Coating Technology and Its Applications: A Review. *Int. J. Precis. Eng. Man.* **2016,** *17* (4), 537-550.

112. Ahn, S. H.; Guo, L. J., Large-Area Roll-to-Roll and Roll-to-Plate Nanoimprint Lithography: A Step toward High-Throughput Application of Continuous Nanoimprinting. *ACS Nano* **2009,** *3* (8), 2304-2310.

113. Ahn, S. H.; Guo, L. J., High-Speed Roll-to-Roll Nanoimprint Lithography on Flexible Plastic Substrates. *Adv. Mater.* **2008,** *20* (11), 2044-2049.

114. Kooy, N.; Mohamed, K.; Pin, L. T.; Guan, O. S., A review of roll-to-roll nanoimprint

lithography. *Nanoscale Res. Lett.* **2014,** *9* (1), 320.

115. Lan, S.; Lee, H.; Ni, J.; Lee, S.; Lee, M. In *Survey on Roller-type Nanoimprint Lithography (RNIL) Process*, 2008 International Conference on Smart Manufacturing Application, 9-11 April 2008; 2008; pp 371-376.

116. Liddle, J. A.; Gallatin, G. M., Nanomanufacturing: A Perspective. *ACS Nano* **2016,** *10* (3), 2995-3014.

117. Engstrom, D. S.; Porter, B.; Pacios, M.; Bhaskaran, H., Additive Nanomanufacturing – A Review. *J. Mater. Res.* **2014,** *29* (17), 1792-1816.

118. Tyson, M., ASML claims elusive EUV lithography milestone. https://hexus.net/tech/news/industry/108067-asml-claims-elusive-euv-lithography-milestone/.

119. Hutcheson, G. D. In *Moore's Law, Lithography, and How Optics Drive the Semiconductor Industry*, Extreme Ultraviolet (EUV) Lithography IX, International Society for Optics and Photonics: 2018; p 1058303.

120. Intel Invests $4.1 Billion In ASML 450mm & EUV Lithography. https://siliconsemiconductor.net/article/75571/Intel_Invests_41_billion_In_ASML_450mm_and_EUV_Lithography.

121. Developpement, Y. *Photolithography Equipment and Materials for Advanced Packaging, MEMS and LED Applications*; Yole Developpement: 2015.

122. Lin, B. In *Limits of optical lithography and status of EUV*, IEEE International Electron Devices Meeting (IEDM), 2009.

123. Simprintnanotech, About Nanoimprint lithography. http://simprintnanotech.com/pg/about.

124. Wu, D.; S Rajput, N.; Luo, X., Nanoimprint lithography-the past, the present and the future. *Curr. Nanosci.* **2016,** *12* (6), 712-724.

125. Garg, D.; Henderson, P. B.; Hollingsworth, R. E.; Jensen, D. G., An economic analysis of the deposition of electrochromic WO3 via sputtering or plasma enhanced chemical vapor deposition. *Mater. Sci. Eng. B* **2005,** *119* (3), 224-231.

126. Wang, D.; Zhang, Y.; Lu, X.; Ma, Z.; Xie, C.; Zheng, Z., Chemical formation of soft metal electrodes for flexible and wearable electronics. *Chem. Soc. Rev.* **2018,** *47* (12), 4611-4641.

127. Yu, Y.; Xiao, X.; Zhang, Y.; Li, K.; Yan, C.; Wei, X.; Chen, L.; Zhen, H.; Zhou, H.; Zhang, S.; Zheng, Z., Photoreactive and Metal-Platable Copolymer Inks for High-Throughput, Room-Temperature Printing of Flexible Metal Electrodes for Thin-Film Electronics. *Adv. Mater.* **2016,** *28* (24), 4926-34.

128. Yu, Y.; Yan, C.; Zheng, Z. J., Polymer-Assisted Metal Deposition (PAMD): A Full-Solution Strategy for Flexible, Stretchable, Compressible, and Wearable Metal Conductors. *Adv. Mater.*

2014, *26* (31), 5508-5516.

129. Li, K.; Zhen, H. Y.; Niu, L. Y.; Fang, X.; Zhang, Y. K.; Guo, R. S.; Yu, Y.; Yan, F.; Li, H. F.; Zheng, Z. J., Full-Solution Processed Flexible Organic Solar Cells Using Low-Cost Printable Copper Electrodes. *Adv. Mater.* **2014,** *26* (42), 7271-7278.

130. Liu, X. Q.; Zhou, X. C.; Li, Y.; Zheng, Z. J., Surface-Grafted Polymer-Assisted Electroless Deposition of Metals for Flexible and Stretchable Electronics. *Chemistry-an Asian Journal* **2012,** *7* (5), 862-870.

131. Henning, T., Copper electroplating principle. https://commons.wikimedia.org/wiki/File:Copper_electroplating_principle_(multilingual).svg.

132. Zhakeyev, A.; Wang, P. F.; Zhang, L.; Shu, W. M.; Wang, H. Z.; Xuan, J., Additive Manufacturing: Unlocking the Evolution of Energy Materials. *Adv. Sci.* **2017,** *4* (10).

133. Hirt, L.; Reiser, A.; Spolenak, R.; Zambelli, T., Additive Manufacturing of Metal Structures at the Micrometer Scale. *Adv. Mater.* **2017,** *29* (17).

134. Gysling, H. J., Nanoinks in inkjet metallization - Evolution of simple additive-type metal patterning. *Curr. Opin. Colloid Interface Sci.* **2014,** *19* (2), 155-162.

135. Vaezi, M.; Seitz, H.; Yang, S. F., A review on 3D micro-additive manufacturing technologies. *Int. J. Adv. Manuf. Tech.* **2013,** *67* (5-8), 1721-1754.

136. Khare, H. S.; Gosvami, N. N.; Lahouij, I.; Milne, Z. B.; McClimon, J. B.; Carpick, R. W., Nanotribological Printing: A Nanoscale Additive Manufacturing Method. *Nano Lett.* **2018,** *18* (11), 6756-6763.

137. Haaheim, J.; Nafday, O.; Levesque, T.; Fragala, J.; Shile, R. In *MEMS-enabled Dip Pen Nanolithography for directed nanoscale deposition and high-throughput nanofabrication*, Microfluidics, BioMEMS, and Medical Microsystems VII, International Society for Optics and Photonics: 2009; p 720706.

138. Tennant, D., Limits of conventional lithography. In *Nanotechnology*, Springer: 1999; pp 161-205.

139. He, Q.; Zhang, H., Nanoscale patterning hots up. *Nature Electronics* **2019,** *2* (1), 13-14.

140. Sasikala, G.; Dhanasekaran, R.; Subramanian, C., Electrodeposition and optical characterisation of CdS thin films on ITO-coated glass. *Thin Solid Films* **1997,** *302* (1), 71-76.

141. Chou, S.; Cheng, F.; Chen, J., Electrodeposition synthesis and electrochemical properties of nanostructured γ-MnO2 films. *J. Power Sources* **2006,** *162* (1), 727-734.

142. Wei, H.; Wang, Y.; Guo, J.; Yan, X.; O'Connor, R.; Zhang, X.; Shen, N. Z.; Weeks, B. L.; Huang, X.; Wei, S., Electropolymerized polypyrrole nanocoatings on carbon paper for electrochemical energy storage. *ChemElectroChem* **2015,** *2* (1), 119-126.

143. Zhong, Y.; Chai, Z. S.; Liang, Z. M.; Sun, P.; Xie, W. G.; Zhao, C. X.; Mai, W. J., Electrochromic Asymmetric Supercapacitor Windows Enable Direct Determination of Energy Status by the Naked Eye. *ACS Appl. Mater. Interfaces* **2017,** *9* (39), 34085-34092.

144. Myny, K., The development of flexible integrated circuits based on thin-film transistors. *Nature Electronics* **2018,** *1* (1), 30-39.

145. Hassel, M.; Hemmerich, I.; Kuhlenbeck, H.; Freund, H.-J., High resolution XPS study of a thin Cr2O3 (111) film grown on Cr (110). *Surf. Sci. Spectra* **1996,** *4* (3), 246-252.

146. Yourdshahyan, Y.; Zhang, H. K.; Rappe, A. M., n-alkyl thiol head-group interactions with the Au(111) surface. *Phys. Rev. B* **2001,** *63* (8), 081405.

147. Häkkinen, H., The gold–sulfur interface at the nanoscale. *Nat Chem* **2012,** *4* (6), 443-455.

148. Notsu, H.; Kubo, W.; Shitanda, I.; Tatsuma, T., Super-hydrophobic/super-hydrophilic patterning of gold surfaces by photocatalytic lithography. *J. Mater. Chem.* **2005,** *15* (15), 1523-1527.

149. Nicosia, C.; Huskens, J., Reactive self-assembled monolayers: from surface functionalization to gradient formation. *Mater. Horiz.* **2014,** *1* (1), 32-45.

150. Ben Haddada, M.; Blanchard, J.; Casale, S.; Krafft, J.-M.; Vallée, A.; Méthivier, C.; Boujday, S., Optimizing the immobilization of gold nanoparticles on functionalized silicon surfaces: amine- vs thiol-terminated silane. *Gold Bulletin* **2013,** *46* (4), 335-341.

151. TECH-FAQ, Acrylic Adhesives. http://www.tech-faq.com/acrylic-adhesives.html.

152. 3M, Acrylic Adhesives. https://www.3m.com/3M/en_US/bonding-and-assembly-us/structural-adhesives/acrylic-adhesives/.

153. Hecht, D. S.; Hu, L. B.; Irvin, G., Emerging Transparent Electrodes Based on Thin Films of Carbon Nanotubes, Graphene, and Metallic Nanostructures. *Adv. Mater.* **2011,** *23* (13), 1482-1513.

154. Ellmer, K., Past achievements and future challenges in the development of optically transparent electrodes. *Nat. Photonics* **2012,** *6* (12), 808-816.

155. Rogers, J. A.; Someya, T.; Huang, Y. G., Materials and Mechanics for Stretchable Electronics. *Science* **2010,** *327* (5973), 1603-1607.

156. Li, D.; Lai, W. Y.; Zhang, Y. Z.; Huang, W., Printable Transparent Conductive Films for Flexible Electronics. *Adv. Mater.* **2018,** *30* (10), 1704738.

157. Kim, H.; Gilmore, C.; Pique, A.; Horwitz, J.; Mattoussi, H.; Murata, H.; Kafafi, Z.; Chrisey, D., Electrical, optical, and structural properties of indium–tin–oxide thin films for organic light-emitting devices. *J. Appl. Phys.* **1999,** *86* (11), 6451-6461.

158. Park, S.; Vosguerichian, M.; Bao, Z., A review of fabrication and applications of carbon nanotube film-based flexible electronics. *Nanoscale* **2013,** *5* (5), 1727-52.

159. Tait, J. G.; Worfolk, B. J.; Maloney, S. A.; Hauger, T. C.; Elias, A. L.; Buriak, J. M.; Harris, K. D., Spray coated high-conductivity PEDOT:PSS transparent electrodes for stretchable and mechanically-robust organic solar cells. *Sol. Energy Mater. Sol. Cells* **2013,** *110*, 98-106.

160. Elschner, A.; Lovenich, W., Solution-deposited PEDOT for transparent conductive applications. *MRS Bull.* **2011,** *36* (10), 794-798.

161. Geng, H. Z.; Kim, K. K.; So, K. P.; Lee, Y. S.; Chang, Y.; Lee, Y. H., Effect of acid treatment on carbon nanotube-based flexible transparent conducting films. *J. Am. Chem. Soc.* **2007,** *129* (25), 7758-9.

162. Bae, S.; Kim, H.; Lee, Y.; Xu, X. F.; Park, J. S.; Zheng, Y.; Balakrishnan, J.; Lei, T.; Kim, H. R.; Song, Y. I.; Kim, Y. J.; Kim, K. S.; Ozyilmaz, B.; Ahn, J. H.; Hong, B. H.; Iijima, S., Roll-to-roll production of 30-inch graphene films for transparent electrodes. *Nat. Nanotechnol.* **2010,** *5* (8), 574-578.

163. Kang, H.; Jung, S.; Jeong, S.; Kim, G.; Lee, K., Polymer-metal hybrid transparent electrodes for flexible electronics. *Nat. Commun.* **2015,** *6*.

164. Zhang, C.; Zhao, D. W.; Gu, D. E.; Kim, H.; Ling, T.; Wu, Y. K. R.; Guo, L. J., An Ultrathin, Smooth, and Low-Loss Al-Doped Ag Film and Its Application as a Transparent Electrode in Organic Photovoltaics. *Adv. Mater.* **2014,** *26* (32), 5696-5701.

165. Leem, D. S.; Edwards, A.; Faist, M.; Nelson, J.; Bradley, D. D.; de Mello, J. C., Efficient organic solar cells with solution-processed silver nanowire electrodes. *Adv. Mater.* **2011,** *23* (38), 4371-5.

166. Kang, M. G.; Guo, L. J., Nanoimprinted semitransparent metal electrodes and their application in organic light-emitting diodes. *Adv. Mater.* **2007,** *19* (10), 1391-1396.

167. Schneider, J.; Rohner, P.; Thureja, D.; Schmid, M.; Galliker, P.; Poulikakos, D., Electrohydrodynamic NanoDrip Printing of High Aspect Ratio Metal Grid Transparent Electrodes. *Adv. Funct. Mater.* **2016,** *26* (6), 833-840.

168. Hu, L. B.; Wu, H.; Cui, Y., Metal nanogrids, nanowires, and nanofibers for transparent electrodes. *MRS Bull.* **2011,** *36* (10), 760-765.

169. Ghosh, D. S.; Chen, T. L.; Pruneri, V., High figure-of-merit ultrathin metal transparent electrodes incorporating a conductive grid. *Appl. Phys. Lett.* **2010,** *96* (4).

170. Kim, W. K.; Lee, S.; Lee, D. H.; Park, I. H.; Bae, J. S.; Lee, T. W.; Kim, J. Y.; Park, J. H.; Cho, Y. C.; Cho, C. R.; Jeong, S. Y., Cu Mesh for Flexible Transparent Conductive Electrodes. *Sci. Rep.* **2015,** *5*.

171. Khan, A.; Lee, S.; Jang, T.; Xiong, Z.; Zhang, C. P.; Tang, J. Y.; Guo, L. J.; Li, W. D., High-Performance Flexible Transparent Electrode with an Embedded Metal Mesh Fabricated by Cost-Effective Solution Process. *Small* **2016,** *12* (22), 3021-3030.

172. van de Groep, J. V.; Spinelli, P.; Polman, A., Transparent Conducting Silver Nanowire Networks. *Nano Lett.* **2012,** *12* (6), 3138-3144.

173. Li, Y. W.; Mao, L.; Gao, Y. L.; Zhang, P.; Li, C.; Ma, C. Q.; Tu, Y. F.; Cui, Z.; Chen, L. W., ITO-free photovoltaic cell utilizing a high-resolution silver grid current collecting layer. *Sol. Energy Mater. Sol. Cells* **2013,** *113*, 85-89.

174. Zhou, L.; Xiang, H. Y.; Shen, S.; Li, Y. Q.; De Chen, J.; Xie, H. J.; Goldthorpe, I. A.; Chen, L. S.; Lee, S. T.; Tang, J. X., High-Performance Flexible Organic Light-Emitting Diodes Using Embedded Silver Network Transparent Electrodes. *ACS Nano* **2014,** *8* (12), 12796-12805.

175. Maurer, J. H. M.; Gonzalez-Garcia, L.; Reiser, B.; Kanelidis, I.; Kraus, T., Templated Self-Assembly of Ultrathin Gold Nanowires by Nanoimprinting for Transparent Flexible Electronics. *Nano Lett.* **2016,** *16* (5), 2921-2925.

176. Yu, S.; Han, H. J.; Kim, J. M.; Yim, S.; Sim, D. M.; Lim, H.; Lee, J. H.; Park, W. I.; Park, J. H.; Kim, K. H.; Jung, Y. S., Area-Selective Lift-Off Mechanism Based on Dual-Triggered Interfacial Adhesion Switching: Highly Facile Fabrication of Flexible Nanomesh Electrode. *ACS Nano* **2017,** *11* (4), 3506-3516.

177. Lee, Y.; Min, S. Y.; Kim, T. S.; Jeong, S. H.; Won, J. Y.; Kim, H.; Xu, W.; Jeong, J. K.; Lee, T. W., Versatile Metal Nanowiring Platform for Large-Scale Nano- and Opto-Electronic Devices. *Adv. Mater.* **2016,** *28* (41), 9109-9116.

178. Paeng, D.; Yoo, J. H.; Yeo, J.; Lee, D.; Kim, E.; Ko, S. H.; Grigoropoulos, C. P., Low-cost facile fabrication of flexible transparent copper electrodes by nanosecond laser ablation. *Adv. Mater.* **2015,** *27* (17), 2762-7.

179. Liu, Y. H.; Xu, J. L.; Shen, S.; Cai, X. L.; Chen, L. S.; Wang, S. D., High-performance, ultra-flexible and transparent embedded metallic mesh electrodes by selective electrodeposition for all-solid-state supercapacitor applications. *J. Mater. Chem. A* **2017,** *5* (19), 9032-9041.

180. Pan, C.; Kumar, K.; Li, J.; Markvicka, E. J.; Herman, P. R.; Majidi, C., Visually Imperceptible Liquid-Metal Circuits for Transparent, Stretchable Electronics with Direct Laser Writing. *Adv. Mater.* **2018,** *30* (12), 1706937.

181. Han, B.; Pei, K.; Huang, Y. L.; Zhang, X. J.; Rong, Q. K.; Lin, Q. G.; Guo, Y. F.; Sun, T. Y.; Guo, C. F.; Carnahan, D.; Giersig, M.; Wang, Y.; Gao, J. W.; Ren, Z. F.; Kempa, K., Uniform Self-Forming Metallic Network as a High-Performance Transparent Conductive Electrode. *Adv. Mater.* **2014,** *26* (6), 873-877.

182. Kwon, N.; Kim, K.; Sung, S.; Yi, I.; Chung, I., Highly conductive and transparent Ag honeycomb mesh fabricated using a monolayer of polystyrene spheres. *Nanotechnology* **2013,** *24* (23).

183. Gao, T. C.; Wang, B. M.; Ding, B.; Lee, J. K.; Leu, P. W., Uniform and Ordered Copper Nanomeshes by Microsphere Lithography for Transparent Electrodes. *Nano Lett.* **2014,** *14* (4),

2105-2110.

184. Guo, C. F.; Sun, T.; Liu, Q.; Suo, Z.; Ren, Z., Highly stretchable and transparent nanomesh electrodes made by grain boundary lithography. *Nat. Commun.* **2014,** *5*, 3121.

185. Layani, M.; Gruchko, M.; Milo, O.; Balberg, I.; Azulay, D.; Magdassi, S., Transparent Conductive Coatings by Printing coffee Ring Arrays Obtained at Room Temperature. *ACS Nano* **2009,** *3* (11), 3537-3542.

186. Zhang, Z. L.; Zhang, X. Y.; Xin, Z. Q.; Deng, M. M.; Wen, Y. Q.; Song, Y. L., Controlled Inkjetting of a Conductive Pattern of Silver Nanoparticles Based on the Coffee-Ring Effect. *Adv. Mater.* **2013,** *25* (46), 6714-6718.

187. He, T. D.; Xie, A. Z.; Reneker, D. H.; Zhu, Y., A Tough and High-Performance Transparent Electrode from a Scalable and Transfer-Free Method. *ACS Nano* **2014,** *8* (5), 4782-4789.

188. Hong, K.; Ham, J.; Kim, B. J.; Park, J. Y.; Lim, D. C.; Lee, J. Y.; Lee, J. L., Continuous 1D-Metallic Microfibers Web for Flexible Organic Solar Cells. *ACS Appl. Mater. Interfaces* **2015,** *7* (49), 27397-27404.

189. Han, B.; Huang, Y. L.; Li, R. P.; Peng, Q.; Luo, J. Y.; Pei, K.; Herczynski, A.; Kempa, K.; Ren, Z. F.; Gao, J. W., Bio-inspired networks for optoelectronic applications. *Nat. Commun.* **2014,** *5*.

190. Yu, Y.; Zhang, Y. K.; Li, K.; Yan, C.; Zheng, Z. J., Bio-Inspired Chemical Fabrication of Stretchable Transparent Electrodes. *Small* **2015,** *11* (28), 3444-3449.

191. Dressel, M. G.; G. Gruner, *Electrodynamics of solids: Optical properties of electrons in matter*. Cambridge University Press: Cambridge, 2002.

192. Hu, L.; Hecht, D. S.; Gruner, G., Percolation in transparent and conducting carbon nanotube networks. *Nano Lett.* **2004,** *4* (12), 2513-2517.

193. Lin, S.; Bai, X.; Wang, H.; Wang, H.; Song, J.; Huang, K.; Wang, C.; Wang, N.; Li, B.; Lei, M.; Wu, H., Roll-to-Roll Production of Transparent Silver-Nanofiber-Network Electrodes for Flexible Electrochromic Smart Windows. *Adv. Mater.* **2017,** *29* (41), 1703238.

194. Wu, H.; Kong, D. S.; Ruan, Z. C.; Hsu, P. C.; Wang, S.; Yu, Z. F.; Carney, T. J.; Hu, L. B.; Fan, S. H.; Cui, Y., A transparent electrode based on a metal nanotrough network. *Nat. Nanotechnol.* **2013,** *8* (6), 421-425.

195. Ji, S. L.; He, W. W.; Wang, K.; Ran, Y. X.; Ye, C. H., Thermal Response of Transparent Silver Nanowire/PEDOT:PSS Film Heaters. *Small* **2014,** *10* (23), 4951-4960.

196. Yoshikawa, R.; Tenjimbayashi, M.; Matsubayashi, T.; Manabe, K.; Magagnin, L.; Monnai, Y.; Shiratori, S., Designing a Flexible and Transparent Ultrarapid Electrothermogenic Film Based on Thermal Loss Suppression Effect: A Self-Fused Cu/Ni Composite Junctionless Nanonetwork for Effective Deicing Heater. *ACS Appl. Nano Mater.* **2018,** *1* (2), 860-868.

197. Bihar, E.; Deng, Y.; Miyake, T.; Saadaoui, M.; Malliaras, G. G.; Rolandi, M., A Disposable paper breathalyzer with an alcohol sensing organic electrochemical transistor. *Sci. Rep.* **2016,** *6*, 27582.

198. Kim, S.-M.; Kim, C.-H.; Kim, Y.; Kim, N.; Lee, W.-J.; Lee, E.-H.; Kim, D.; Park, S.; Lee, K.; Rivnay, J.; Yoon, M.-H., Influence of PEDOT:PSS crystallinity and composition on electrochemical transistor performance and long-term stability. *Nat. Commun.* **2018,** *9* (1), 3858.

199. Friedlein, J. T.; Donahue, M. J.; Shaheen, S. E.; Malliaras, G. G.; McLeod, R. R., Microsecond Response in Organic Electrochemical Transistors: Exceeding the Ionic Speed Limit. *Adv. Mater.* **2016,** *28* (38), 8398-8404.

200. Basiricò, L.; Cosseddu, P.; Scidà, A.; Fraboni, B.; Malliaras, G. G.; Bonfiglio, A., Electrical characteristics of ink-jet printed, all-polymer electrochemical transistors. *Org. Electron.* **2012,** *13* (2), 244-248.

201. Lin, P.; Yan, F.; Chan, H. L. W., Ion-Sensitive Properties of Organic Electrochemical Transistors. *ACS Appl. Mater. Interfaces* **2010,** *2* (6), 1637-1641.

202. Kergoat, L.; Herlogsson, L.; Braga, D.; Piro, B.; Pham, M. C.; Crispin, X.; Berggren, M.; Horowitz, G., A Water-Gate Organic Field-Effect Transistor. *Adv. Mater.* **2010,** *22* (23), 2565-2569.

203. Khodagholy, D.; Rivnay, J.; Sessolo, M.; Gurfinkel, M.; Leleux, P.; Jimison, L. H.; Stavrinidou, E.; Herve, T.; Sanaur, S.; Owens, R. M.; Malliaras, G. G., High transconductance organic electrochemical transistors. *Nat. Commun.* **2013,** *4*, 2133.

204. Rivnay, J.; Inal, S.; Salleo, A.; Owens, R. M.; Berggren, M.; Malliaras, G. G., Organic electrochemical transistors. *Nat. Rev. Mater.* **2018,** *3*, 17086.

205. Li, H.; Liang, J., Recent Development of Printed Micro-Supercapacitors: Printable Materials, Printing Technologies, and Perspectives. *Adv. Mater. 0* (0), 1805864.

206. Wang, J.; Li, F.; Zhu, F.; Schmidt, O. G., Recent Progress in Micro-Supercapacitor Design, Integration, and Functionalization. *Small Methods 0* (0), 1800367.

207. Qi, D.; Liu, Y.; Liu, Z.; Zhang, L.; Chen, X., Design of Architectures and Materials in In-Plane Micro-supercapacitors: Current Status and Future Challenges. *Adv. Mater.* **2017,** *29* (5), 1602802.

208. Guo, R. S.; Chen, J. T.; Yang, B. J.; Liu, L. Y.; Su, L. J.; Shen, B. S.; Yan, X. B., In-Plane Micro-Supercapacitors for an Integrated Device on One Piece of Paper. *Adv. Funct. Mater.* **2017,** *27* (43).

209. Zhang, Y.-Z.; Wang, Y.; Cheng, T.; Lai, W.-Y.; Pang, H.; Huang, W., Flexible supercapacitors based on paper substrates: a new paradigm for low-cost energy storage. *Chem. Soc. Rev.* **2015,** *44* (15), 5181-5199.

210. Kyerematen, N. A.; Brousse, T.; Pech, D., Microsupercapacitors as miniaturized energy-

storage components for on-chip electronics. *Nat. Nanotechnol.* **2017,** *12* (1), 7-15.

211. Shen, C. W.; Xu, S. X.; Xie, Y. X.; Sanghadasa, M.; Wang, X. H.; Lin, L. W., A Review of On-Chip Micro Supercapacitors for Integrated Self-Powering Systems. *J. Microelectromech. S.* **2017,** *26* (5), 949-965.

212. Huang, T. T.; Jiang, K.; Chen, D.; Shen, G. Z., Recent progress and perspectives of metal oxides based on-chip microsupercapacitors. *Chin. Chem. Lett.* **2018,** *29* (4), 553-563.

213. Li, Y.; Chang, S.; Liu, X.; Huang, J.; Yin, J.; Wang, G.; Cao, D., Nanostructured CuO directly grown on copper foam and their supercapacitance performance. *Electrochim. Acta* **2012,** *85*, 393-398.

214. Singh, B. K.; Shaikh, A.; Badrayyana, S.; Mohapatra, D.; Dusane, R. O.; Parida, S., Nanoporous gold–copper oxide based all-solid-state micro-supercapacitors. *RSC Adv.* **2016,** *6* (102), 100467-100475.

215. Kim, W.; Kim, S.; Kang, I.; Jung, M. S.; Kim, S. J.; Kim, J. K.; Cho, S. M.; Kim, J. H.; Park, J. H., Hybrid Silver Mesh Electrode for ITO-Free Flexible Polymer Solar Cells with Good Mechanical Stability. *Chemsuschem* **2016,** *9* (9), 1042-1049.

216. Kang, M. G.; Park, H. J.; Ahn, S. H.; Guo, L. J., Transparent Cu nanowire mesh electrode on flexible substrates fabricated by transfer printing and its application in organic solar cells. *Sol. Energy Mater. Sol. Cells* **2010,** *94* (6), 1179-1184.

217. Yu, J. S.; Jung, G. H.; Jo, J.; Kim, J. S.; Kim, J. W.; Kwak, S. W.; Lee, J. L.; Kim, I.; Kim, D., Transparent conductive film with printable embedded patterns for organic solar cells. *Sol. Energy Mater. Sol. Cells* **2013,** *109*, 142-147.

218. Duan, H.; Hu, H.; Kumar, K.; Shen, Z.; Yang, J. K. W., Direct and Reliable Patterning of Plasmonic Nanostructures with Sub-10-nm Gaps. *ACS Nano* **2011,** *5* (9), 7593-7600.

219. Nagel, R. D.; Filser, S.; Zhang, T.; Manzi, A.; Schonleber, K.; Lindsly, J.; Zimmermann, J.; Maier, T. L.; Scarpa, G.; Krischer, K.; Lugli, P., Nanoimprint methods for the fabrication of macroscopic plasmonically active metal nanostructures. *J. Appl. Phys.* **2017,** *121* (8).

220. Hsiao, H. H.; Chu, C. H.; Tsai, D. P., Fundamentals and Applications of Metasurfaces. *Small Methods* **2017,** *1* (4).

221. Chen, L.; Xie, Z.; Gan, T.; Wang, Y.; Zhang, G.; Mirkin, C. A.; Zheng, Z., Biomimicking Nano‐Micro Binary Polymer Brushes for Smart Cell Orientation and Adhesion Control. *Small* **2016**.

222. Wagner, S.; Bauer, S., Materials for stretchable electronics. *MRS Bull.* **2012,** *37* (03), 207-213.

223. Sekitani, T.; Someya, T., Stretchable, Large-area Organic Electronics. *Adv. Mater.* **2010,** *22* (20), 2228-2246.

224. Kim, D. H.; Rogers, J. A., Stretchable Electronics: Materials Strategies and Devices. *Adv. Mater.* **2008,** *20* (24), 4887-4892.