ELEMENTAL TWO-DIMENSIONAL MATERIALS FOR NANOELECTRONICS APPLICATIONS

LIN ZIYUAN

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The Hong Kong Polytechnic University
Department of Applied Physics

Elemental Two-Dimensional Materials for Nanoelectronics Applications

LIN Ziyuan

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Abstracts

Elemental two-dimensional (2D) materials stand out for their simple compositions and excellent electrical properties, showing the great potential for nanoelectronics applications. In this thesis, we study the carrier transport of emerging elemental 2D materials: black phosphorous (BP) and tellurene (Te), which develops the understanding on transport behaviours and benefits the improvement of electronics devices based on 2D BP and Te. In addition, we develop a thinning method for few-layer Te, which allows local thinning with thickness control. This thinning process is compatible with device fabrication process, facilitating the further applications of few-layer Te in nanoelectronics.

We first demonstrate the *n*-type field-effect transistors (FETs) based on few-layer BP achieved by contact engineering. The copper (Cu) is chosen as contact metals for theoretical Ohmic contact and *n*-type doping effect. With detailed investigation on the interface between BP and Cu, it is found that highly diffusive Cu atoms migrate into BP and intercalate between BP layers without changing the crystal structure of BP. The BP with interstitial Cu is theoretically predicted to have smaller band gap than pristine BP. The Fermi level is greatly

shifted towards conduction band after the Cu penetration. Through this interstitial Cu-doped edge contact, *n*-type dominant BP transistors are achieved with high electron mobility of ~ 138 $cm^2V^{-1}s^{-1}$ and on/off ratio of ~ 100 at room temperature. The current density can reach 58 μA/μm. The Schottky barrier height for electron is negligibly low. This *n*-type transport property is attributed to *n*-doping induced by the penetration of highly-mobile Cu atoms at the contact region. The penetrated Cu in BP also changes the electrical property of BP to metallic-like behavior, bringing low contact resistance.

Afterwards, we study the transport property of few-layer Te and fabricate high-performance *p*-type FETs based on 2D Te with high-work-function contact metals, platinum (Pt) and palladium (Pd). The work functions of Pt and Pd are lying far below the valence band maximum (VBM) of 2D Te, facilitating the hole transport in Te. The devices exhibit unipolar *p*-type transport property with hole mobility reaching 700 $cm^2V^{-1}s^{-1}$ and on/off ratio up to 10^4. The current density can reach 0.17 mA/μm. The hole concentration is measured to be 3×10^{18} cm^{-3}, which is comparable with 2D BP. The contact resistance can be as low as 400 Ω•μm, indicating the excellent contact between 2D Te and contact metals. The remarkable *p*-type transport property results from the well-match band alignment between few-layer Te and high-work-function contact metals, which prompts the hole transport in Te. The high density of states of Te near Fermi level also facilitates the current injection from contact metals, bringing large sheet conductivity at the contact region.

Lastly, a local thinning process for few-layer Te involving Pt metal is developed. Under light illumination, few-layer Te near Pt contacts experiences thinning process in water. The thickness can be reduced by ~ 3 nm with 10 min process. Due to the small bandgap of few-layer Te, the electron-hole pairs can be easily generated under white light. The photogenerated electrons will transfer to Pt metal and react with H^+ in water producing H_2 with Pt catalyst. The left OH^- change the pH value near Pt and etch the few-layer Te, resulting thickness reduction of Te near Pt. This local thinning process is compatible with device fabrication process, providing feasible approach to few-layer Te with desirable thickness for various kinds of electronic devices.

In conclusion, the transport properties in 2D BP and Te receive detailed study to implement high-performance FET devices. Contact engineering is the focus of this study for the improvement of device performance. A local thinning method is also developed for few-layer Te to extend the applications of emerging 2D Te.

List of Publications

Journal

1. **Ziyuan Lin**, Jingli Wang, Jiewei Chen, Cong Wang, Jidong Liu, Wenjing Zhang, and Yang Chai, Two-dimensional tellurene transistors with low contact resistance and self-aligned catalytic thinning process, *Advanced electronic materials*, *submitted.*

2. **Ziyuan Lin**, Cong Wang, and Yang Chai, Emerging group-VI elemental 2D materials: preparations, properties, and device applications, *Small*, **2020**, 2003319.

3. **Ziyuan Lin**, Jingli Wang, Xuyun Guo, Jiewei Chen, Chao Xu, Mingqiang Liu, Bilu Liu, Ye Zhu, and Yang Chai, Interstitial copper-doped edge contact for n-type carrier transport in black phosphorus, *InfoMat*, **2019**, 1(2), 242.

4. Lejuan Cai, **Ziyuan Lin**, Mengye Wang, Feng Pan, Jiewei Chen, Yi Wang, Xinpeng Shen, and Yang Chai, Improved interfacial H_2O supply by surface hydroxyl groups for enhanced alkaline hydrogen evolution, *Journal of materials chemistry A*, **2017**, 5(46), 24091.

5. Lejuan Cai, Bocheng Qiu, **Ziyuan Lin**, Yang Wang, Sainan Ma, Mengye Wang, Yuen Hong Tsang, and Yang Chai, Active site engineering of Fe-and Ni-sites for highly efficient electrochemical

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6. Kang Xu, Yuda Zhao, **Ziyuan Lin**, Yan Long, Yi Wang, Mansun Chan, and Yang Chai, Doping of two-dimensional MoS_2 by high energy ion implantation, *Semiconductor Science and Technology*, **2017**, 32(12), 124002.

7. Bocheng Qiu, Lejuan Cai, Yang Wang, **Ziyuan Lin**, Yunpeng Zuo, Mengye Wang, and Yang Chai, Fabrication of nickel-cobalt bimetal phosphide nanocages for enhanced oxygen evolution catalysis, *Advanced Functional Materials*, **2018**, 28(17), 1706008.

8. Jingli Wang, Jingsi Qiao, Kang Xu, Jiewei Chen, Yuda Zhao, Bocheng Qiu, **Ziyuan Lin**, Wei Ji, and Yang Chai, Quasi one-dimensional van der Waals gold selenide with strong interchain interaction and giant magnetoresistance, *Science Bulletin*, **2020**, 65, 1451.

9. Chao Xu, Yancong Chen, Xiangbin Cai, Arno Meingast, Xuyun Guo, Fakun Wang, **Ziyuan Lin**, Tsz Wing Lo, Christian Maunders, Sorin Lazar, Ning Wang, Dangyuan Lei, Yang Chai, Tianyou Zhai, Xin Luo and Ye Zhu, Two-Dimensional Antiferroelectricity in Nanostripe-Ordered In_2Se_3, *Physical Review Letters*, **2020**, 125(4), 047601.

Conference

1. **Ziyuan Lin**, Jingli Wang, Jiewei Chen, Xuyun Guo, Chao Xu, Mingqiang Liu, Bilu Liu, Ye Zhu and Yang Chai, The 2019 Spring Meeting of the European Materials Research Society, **Oral**, 27 to 31 May 2019, Nice, France.

2. **Ziyuan Lin** and Yang Chai, The 2017 MRS Spring Meeting & Exhibit, **Oral**, 17 to 21 April 2017, Phoenix, American.

3. **Ziyuan Lin**, Jingli Wang, Cong Wang, Linfei Zhang, Wenjing Zhang and Yang Chai, The 2nd international symposium on Low Dimensional Materials for Optoelectronics, **Poster**, 12 to 15 December 2019, Shenzhen, China.

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Chapter 1 Introduction

1.1 Background

Since the successful preparation of the "first" two-dimensional (2D) material graphene by mechanical exfoliation in 2005,[1] 2D materials have received tremendous research efforts in the past decade.[1-16] Explosive research breakthroughs have been made on graphene and graphene-like ultrathin 2D materials. The family of 2D materials is greatly enriched and becomes a large material catalogue consisting of graphene,[1-3] hexagonal boron nitride (h-BN),[4-6] transition metal dichalcogenides (TMDs),[7-10] black phosphorous (BP),[11-13] silicene,[14] MXene,[15] recently discovered tellurene (Te),[16] *etc*. These 2D materials all have a layered or sheet-like structure with a thickness ranging from tenths of a nanometer (single atomic thickness) to tens of nanometer while the lateral size can be up to micrometers or larger. With different compositions and crystal structures, these 2D materials differ from each other in properties, which offers a wide material choice for different functionalities.[3, 4, 7, 9, 10, 13, 14] Apart from the enrichment of 2D material family, the preparation of various 2D materials is also well developed and roughly divided into top-down and bottom-up methods. Exfoliation is the main top-down method. Mechanical exfoliation can prepare high-quality 2D materials for fundamental characterizations and high-performance device fabrication, but it is limited by the small size and the low yield.[17-19] Liquid exfoliation has high yield of production, but the quality and the size of exfoliated 2D materials are still far from satisfactory.[20-22] Bottom-up methods contain vapor deposition and solution synthesis.[16, 23-25] Vapor deposition including chemical vapor deposition (CVD) and physical vapor deposition (PVD) now can synthesize several kinds of 2D materials with large size and relatively high quality.[23-25] The improvement of vapor deposition method is still ongoing, benefiting not only the availability of 2D materials with large size, but also the introduction of 2D materials into industry. The past decade has witnessed the great enrichment of 2D material family and the continuous improvement of preparation approaches, which allows the achievement of various applications based on 2D materials.

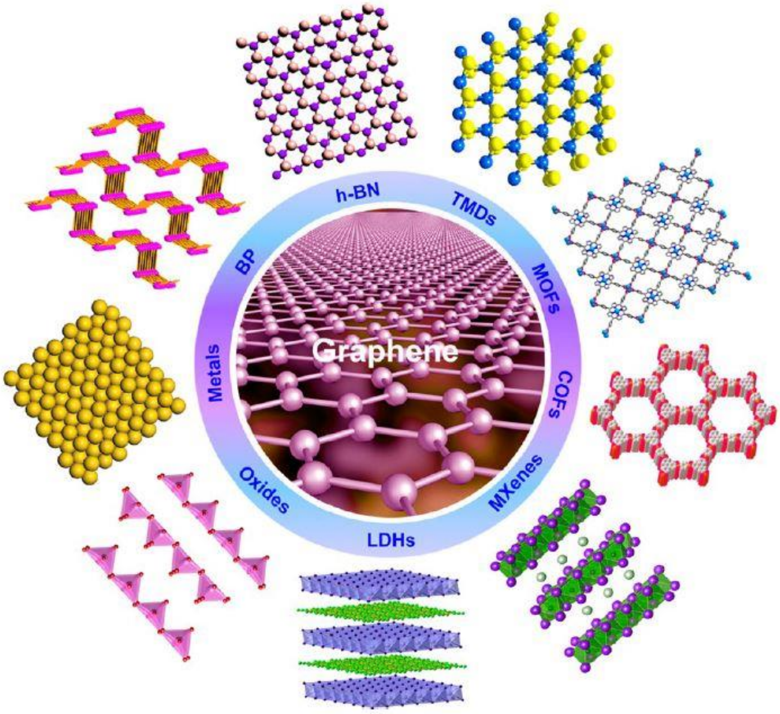

Figure 1.1 Illustration of different kinds of ultrathin 2D materials.[26]

Different from the bulk counterpart, 2D materials with atomic thickness have strikingly fascinating physical, chemical, electronic and optical properties, making themselves extremely promising in fundamental studies and a wide range of applications including electronics, catalysis, energy storage and sensors.[27-35] The numerous applications of 2D materials result from the diverse 2D materials with different compositions, atomic structures and crystal phases. Here in this thesis, we will focus on exploring the potential of 2D materials on future nanoelectronics.

Since the 1960s, the Moore's law, stating that the number of transistors on a chip will double every 18 months or 24 months, has been guiding the technology revolution of semiconductor industry and sustaining until now. However, in 2016, the worldwide semiconductor industry has acknowledged that the Moore's law is closing to the end.[36] One of the reasons is that scaling of silicon (Si) transistors will theoretically fail with gate lengths below five-nanometer.[37-39] This scaling limit results from the severe short channel effect. As Si transistors approach their scaling limit, the direct source-to-drain tunneling and the loss of gate electrostatic control on the channel will increase the off-state leakage currents, raise power dissipation, and thus severely degrade the performance of Si transistors.[39] Because of this scaling limit of Si transistors, exploration of new channel materials is of vital importance for future nanoelectronics.

Due to the unique 2D nature, the emerging 2D materials are promising candidates for next-generation semiconductor devices. The diversity of 2D materials provides broad choices of metals (*e.g.* graphene), insulators (*e.g.* h-BN) and semiconductors (*e.g.* TMDs, BP, Te).[3, 6, 9, 10, 13, 16, 19, 28] The 2D semiconductors with layer or thickness dependent bandgaps have been regarded as potential channel materials for replacing Si. A major advantage of 2D semiconductors over Si is the atomically thin and uniform thickness, as shown in Figure 1.2(A).[40] The layered nature of 2D semiconductors allows consistent thickness control with atomic precision down to the monolayer limit, leading to enhanced electrostatic control of the gate and further scaling of transistors. Also, the pristine surfaces of 2D semiconductors even down to monolayer limit are free of dangling bonds as illustrated in Figure 1.2(B).[40] The pristine surfaces give rise to low density of interface trap states and subsequently reduce the charge scattering. Taking TMDs as an example, molybdenum disulfide (MoS_2), one of the most widely studied 2D semiconductors, has a layer dependent bandgap ranging from 1.8 eV for monolayer to 1.3 eV for bulk, which is a potential replacement for Si.[9] Based on theoretical calculation (Figure 1.3), MoS_2 is predicted to have a direct source-to-drain tunneling leakage current ($I_{SD\text{-}LEAK}$) two orders of magnitude smaller than that of Si.[39] For monolayer MoS_2, the leakage current will not limit the scaling of transistors down to one-nanometer gate length, which is superior to Si with a sub-five-nanometer scaling limit.[39] With unique layer nature, 2D semiconductors alleviate the severe short channel effect in transistor scaling. Because of these features, 2D semiconductors have been regarded as potential options for transistors with ultimate thin channel.

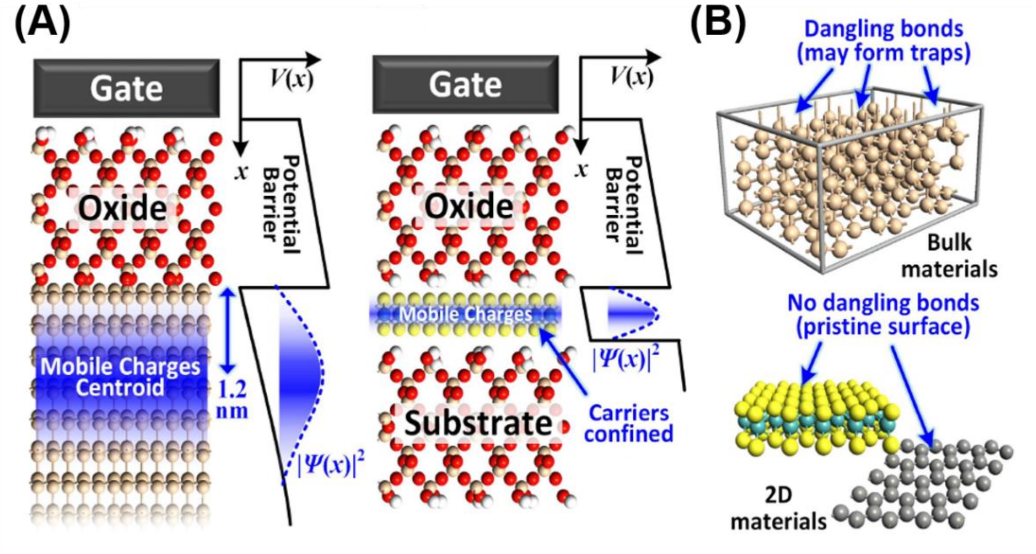

Figure 1.2 Advantages of 2D materials. (A) Charge distribution in 3D and 2D crystals as channel materials. Atomically thin thickness allows better electrostatic control. (B) Surface of 3D and 2D materials. Pristine surface reduces interface trap states.[40]

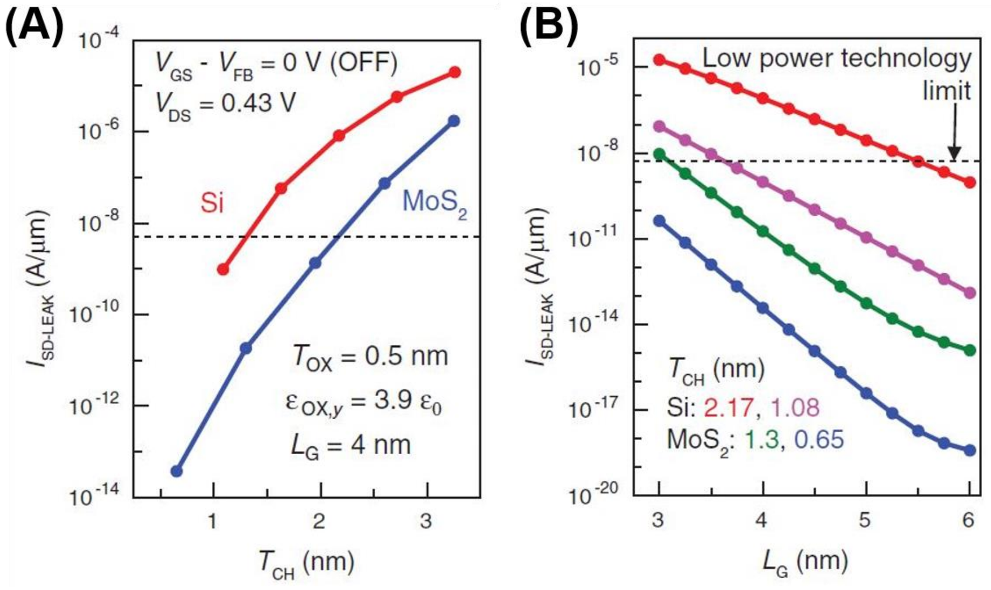

Figure 1.3 (A) The relationship between theoretical direct source-to-drain tunneling leakage current $I_{SD\text{-}LEAK}$ and channel thickness T_{CH} for Si and MoS_2 in the off state. (B) $I_{SD\text{-}LEAK}$ as a function of channel length L_G for Si and MoS_2 with

different T_{CH} in the off state.[39]

After realizing advantages of 2D semiconductors over Si, numerous research studies focus on searching for 2D semiconductors with high carrier mobility and preferably with a direct band gap and exploring their usage in future nanoelectronics.[9, 13, 27, 28] Elemental 2D semiconductors, such as BP and Te, stand out for their simple compositions and high carrier mobilities.[41, 42] Black phosphorus (BP), also called phosphorene for monolayer, is predicted to be a direct-bandgap semiconductor from monolayer to few-layer with an exceptionally high hole mobility of 10^4 $cm^2V^{-1}s^{-1}$.[41] Extensive research works demonstrate BP applications in field-effect transistors (FETs) and other devices.[11, 13] Recently, the few-layer form of tellurium (Te), also called tellurene, is successfully synthesized by solution approach.[16] Theoretical studies predict the hole mobility of Te higher than 10^5 $cm^2V^{-1}s^{-1}$.[42] Preliminary electrical characterization confirms Te another potential 2D semiconductor for future nanoelectronics. Although the field-effect mobility values of devices based on these two elemental 2D material are lower than predicted values because of contacts or interfaces, BP and Te transistors exhibit higher performance than TMDs transistors, which distinguishes BP and Te from popular 2D TMDs semiconductors.[10, 43, 44] Therefore, we focus our research study on these two elemental 2D materials, BP and Te.

1.2 Introduction to Black Phosphorus

Black phosphorus (BP) is a rare allotrope of phosphorus, which was discovered a century ago.[45] Compared with other allotropes like red phosphorus and white phosphorus, bulk BP exhibits semiconducting property.[46] It did not receive much attention until the discovery of graphene in 2004. Due to its layered structure BP was rediscovered and single-layer BP, also known as phosphorene, is the second elemental monolayer material after graphene. Because of its direct bandgap and high carrier mobility, BP is now attracting worldwide attention and being considered as one of potential options for future electronics.[13, 41, 46]

Monolayer and few-layer BP can be attained by exfoliation methods.[13, 47-50] Although some studies claim successful large-area vapor deposition of BP, high-quality monolayer or few-layer BP for electronic devices is solely prepared by mechanical exfoliation, which is one of bottlenecks for wide applications of BP.[13, 51, 52] Despite the low yield of preparation methods, there have been tremendous research works done theoretically and experimentally to understand carrier transport behavior in single-layer and few-layer BP and improve device performance in FETs and optoelectronic devices based on exfoliated BP flakes.[11, 13, 53, 54]

1.2.1 Crystal and Electronic Structure of BP

Thorough understanding on the crystal and electronic structures of BP is necessary before the successful application of BP in nanoelectronics. Resembling graphite, bulk BP has a layered structure with puckered honeycomb lattice in orthorhombic crystal structure, shown in Figure 1.4.[41, 55] Individual layers of phosphorus atoms are stacked in AB-stacking order by van der Waals force, which allows mechanical exfoliation to attain ultrathin BP flakes from a bulk crystal. A single layer of BP consists of two planes of phosphorus atoms. Every phosphorus atom is bonded with three neighboring atoms, two of which are in the same plane. The *x* and *y* directions of each BP layer correspond to the armchair (AM) and zigzag (ZZ) directions, along which the strong in-plane anisotropy is observed.[41, 56] The crystal structure is experimentally visualized by scanning transmission electron microscopy (STEM) with analytical aberration correction. Wu *et al.* reported the annular dark-field STEM (ADF-STEM) images of few-layer exfoliated BP flakes with atomic resolution (Figure 1.5).[57]

The recorded ADF-STEM images along different crystallographic directions, [001] (top view), [101] and [100] (side view) zone axes present exact positions of the atomic columns as high intensity spots. The image interpretation permits not only direct determination of lattice parameters but also confirmation of AB-stacking order. The theoretical prediction and atomic resolution STEM images provide accurate crystal structure of BP, with which we can predict the electronic properties of BP.

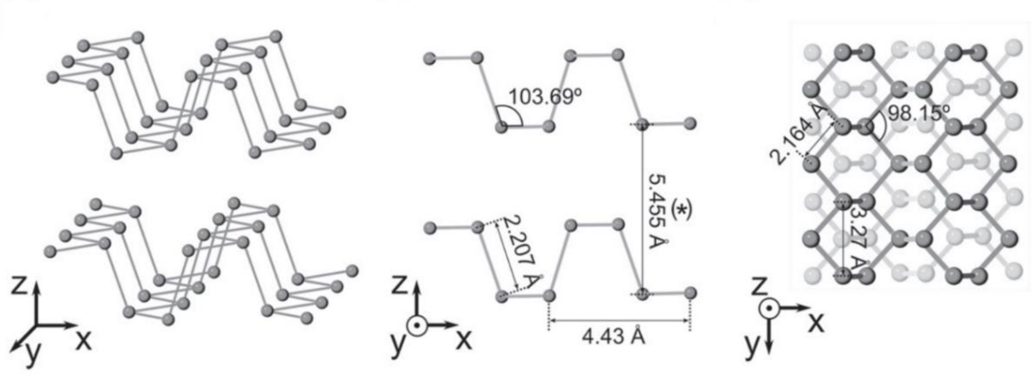

Figure 1.4 Schematic of the BP layer structure.[55]

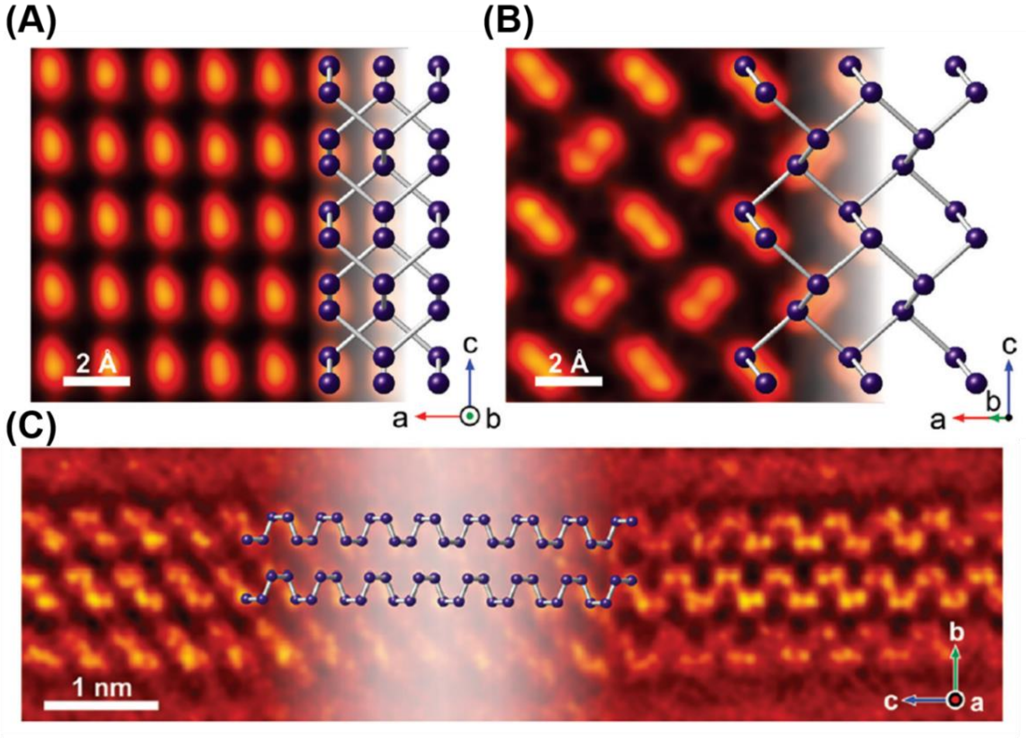

Figure 1.5 ADF-STEM images of BP crystal structure along (A) [001] (top view) and (B) [101] and (C) [100] (side view) zone axes.[57]

Electronic structure prediction by density functional theory (DFT) calculations based on crystal structure has been one of methods for searching 2D materials with appropriate bandgap and carrier mobility. Wei Ji's group conducted detailed calculations on electronic structure of monolayer and few-layer BP.[41] They have shown theoretically the phosphorene is a 2D semiconductor with a direct bandgap of 1.51 eV obtained at the G point. With different functionals for structural optimization, same reduction trends in bandgap are observed as the layer number increases (Figure 1.6). As individual layers of phosphorus are stacked together and the layer number increases, the interlayer interaction grows stronger, which introduces larger band dispersions of valence bands and conduction bands and consequently results in smaller bandgap. The bandgaps of BP are direct and reduced from ~ 1.5 eV for monolayer to ~ 0.3 eV for bulk, which covers visible red to mid-infrared light. This layer-dependent direct-bandgap structure of BP is of great importance for applications such as solar energy harvesting and optical sensing.[53] In addition to band structure, device performance is affected by carrier mobility in a large extent. Phosphorene is predicted to have exceptionally high carrier mobility values for both electron (~ 10^3 $cm^2V^{-1}s^{-1}$) and hole (~ 10^4 $cm^2V^{-1}s^{-1}$).[41] As for few-layer BP which is more frequently used to demonstrate devices, the predicted electron and hole mobility can reach ~ 900 and ~ 4400 $cm^2V^{-1}s^{-1}$, respectively. Also, the mobility shows strong in-plane anisotropy. The carrier mobility values for the AM direction are nearly twice the values for holes and four times for electrons along ZZ direction. Although the predicted intrinsic carrier mobility of BP is pretty high, the field-effect mobility extracted from devices will be inevitably lower than predicted values because of contacts and interfaces.[13] However, both the theoretical and experimental mobilities of BP are higher than TMDs, one of the most widely studied 2D semiconductors, which makes BP attractive in FET applications.[9, 10,44] Based on theoretical study on electronic structure of BP, the direct bandgap from monolayer to bulk and the remarkably high hole mobility distinguish BP from other popular 2D semiconductors and facilitate its applications including FET and optoelectronic devices.

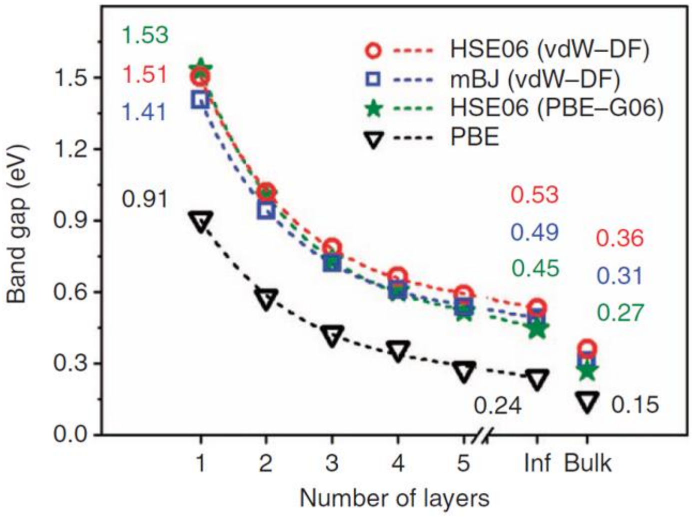

Figure 1.6 The direct bandgaps of BP as a function of the thickness.[41]

1.2.2 Device Applications of BP

Carrier mobility and on/off ratio are two main figures of merit for electronic devices (*e.g.* FETs). Since few-layer BP was rediscovered, interests on device applications of BP have been growing because the transport property of BP fills the gap between graphene and 2D TMDs.[53, 54, 58] The on/off ratio is much larger than graphene while the mobility is higher than TMD materials. These features are technologically important for device applications of BP.

1.2.2.1 Field-Effect Transistors

One of the best device applications of BP is FETs. The very first demonstration of few-layer BP for FET devices is reported by Li *et al.*[13] The FETs were fabricated with below-10-nm-thick few-layer BP as channel, 90 nm SiO_2 as gate dielectric and chromium (Cr) as metal contacts. The transfer property exhibits an on/off ratio of $\sim 10^5$ and a hole mobility reaching 984 $cm^2V^{-1}s^{-1}$ (Figure 1.7(A)). The current modulation (10^5) of BP is four orders of magnitude larger than that of graphene. The mobility, although still lower than that of graphene, is competitive compared with MoS_2 devices and much higher than that of commercially available Si-based devices (~ 500 $cm^2V^{-1}s^{-1}$). The output curve (Figure 1.7(B)) shows linearity at low drain biases suggesting Ohmic contacts and well-behaved saturation at high drain biases which is important to achieve high power gains in radio frequency (RF) FETs. The subthreshold swing (SS) determined from the transfer curve is 5 V/dec, much larger than that of commercial Si-based devices (~ 70 mV/dec), which can be enhanced by adoption of high-κ gate dielectric without compromising other parameters. Some research works utilize thin hafnium dioxide (HfO_2) film by atomic layer deposition (ALD) as high-κ gate dielectric and improve the SS to a nearly ideal value of ~66 mV/dec with the hole mobility maintaining at 536 $cm^2V^{-1}s^{-1}$.[59, 60] The improvement of SS indicates the high-κ gate dielectric can provide excellent gate control over the source-to-drain current and achieve better electrostatics control for BP FETs. To further enhance the performance including mobility and on/off ratio of BP FETs, interface engineering is important because the presence of high-density trapped charges and defects will increase the phonon scattering and degrade the performance.[61] When 2D semiconductors contact with 3D oxide dielectric, the high density of dangling bonds at the surface of 3D dielectric will introduce interfacial charge traps which scatter carriers and lower carrier mobility.[40] Thermal treatment, in some extent, can enhance 2D semiconductors/dielectric interface by passivation of dangling bonds.[59] In addition, when BP is under atmosphere conditions, the oxidation by O_2 and H_2O will further introduce charge impurities and degrade the quality of few-layer BP flakes.[62] Passivation by oxides on the top can protect BP from atmosphere, but BP cannot maintain its pristine surface. To make full use of 2D nature of BP, Chen *et al.* demonstrates FET devices based on few-layer BP sandwiched between two thin layers of h-BN.[63] Thin h-BN layers is an insulating 2D material with excellent air stability, which can serve as not only gate dielectric but also protection layers. The h-BN/BP/h-BN heterostructure is formed by van der Waals interaction with interfaces free of dangling bonds. Encapsulating BP between h-BN layers reduces the density of charge traps at semiconductor/dielectric interface and further avoid the degradation of BP caused by oxidation in the atmosphere. The realization of ultra-clean interfaces diminishes charge trap density and benefits high performance of BP FET devices. The as-fabrication devices with sandwiched heterostructure exhibit a high field-effect mobility of ~ 1350 $cm^2V^{-1}s^{-1}$ and an on/off ratio exceeding 10^5 without significant hysteresis and performance degradation (Figure 1.8). The extensively reported BP FET devices suggest BP a promising *p*-type channel material with high hole mobility for nanoelectronics.[13, 59, 60, 62, 63] The hole transport behavior is experimentally clarified in FET devices. Development of novel device geometry and fabrication process continuously enhances the device performance, fulfilling the great potential of BP in nanoelectronics.

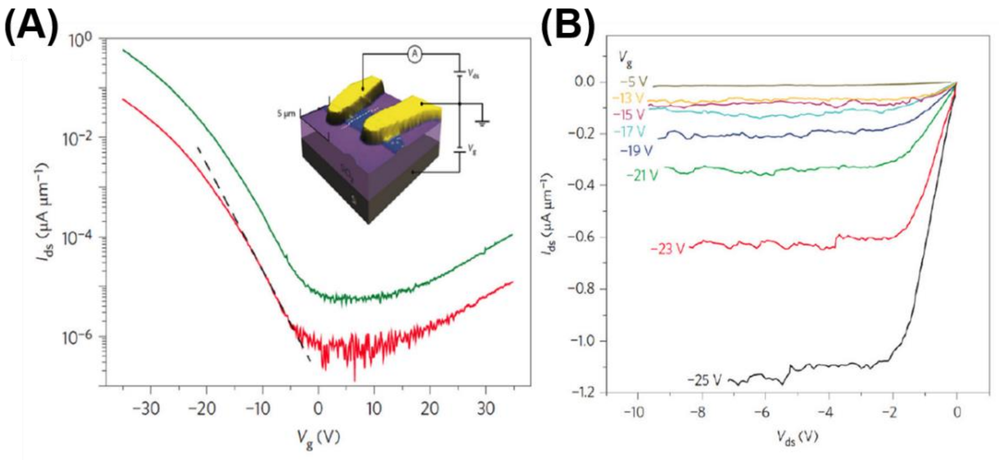

Figure 1.7 The (A) transfer curves and (B) output curves of the very first reported BP FETs.[13]

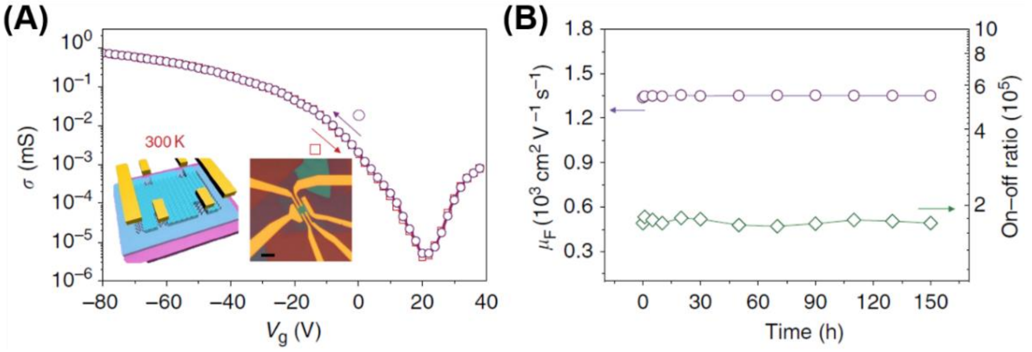

Figure 1.8 The performance of devices with h-BN/BP/h-BN sandwiched structures. (A) Transfer curve of the as-fabricated device. Inserted are the schematic of device structure and optical image of device. (B) The duration of mobility and on/off ratio.[63]

Although the pristine BP has no dominant preference for carrier type, the extensively reported BP FETs exhibit *p*-type dominant transport property due to the Fermi level pinning at the contacts and the suppressed electron transport caused by oxygen and moisture exposure.[64] To realize low-power complementary circuits, it is important to fabricate both *p*-type and *n*-type FETs with same channel materials. Contact engineering and surface doping have been applied to modulate the carrier type and achieve *n*-type BP FETs. Contact engineering by utilizing low-work-function metals such aluminum (Al), scandium (Sc) and erbium (Er) as contacts has been reported to successfully fabricate unipolar *n*-type BP transistors.[64, 65] David J. Perello *et al.* chose Al as contact metals due to its low work function (Φ_M ~ 4.0 – 4.3 eV) which matches well with the conduction band minimum (E_C) of few-layer BP.[64] With Al contacts, the 3-nm-thick BP channel shows a high on/off ratio higher than 10^5 and an electron mobility of 275 $cm^2V^{-1}s^{-1}$ at room temperature (Figure 1.9(A)). Al is a good *n*-type contact for BP FETs with all thicknesses as the E_C of BP weakly depends on BP thickness. The well match between E_C of BP and work function of Al introduces small Schottky barrier for electron, which benefits the electron transport in BP. As the layer number of BP increases, BP FETs with Al contacts experience transition from unipolar *n*-type to ambipolar. The transition results from the reduction of the Schottky barrier for hole, as presented in Figure 1.9(B). The large Schottky barrier for hole existing for ultrathin BP with Al contacts will decrease for thicker samples because of the reduction of bandgap. Other low-work-function metals, Sc and Er, are also demonstrated for high-performance unipolar *n*-type BP transistors (Figure 1.9(C) and 1.9(D)).[65] The fabricated BP transistors with Sc and Er contacts are reported to have the highest *n*-type current (125 μA/μm and 200 μA/μm for BP devices with 4.5 and 6.5 nm thickness, respectively) with a 10^4 on/off ratio. The easy oxidation of Sc at contact interfaces also helps Fermi level depinning and enhances *n*-type polarity. Surface doping is another way to achieve *n*-type BP FETs, which has been widely used to manipulate the electronic properties of 2D materials.[66-68] Surface transfer doping requires interfacial charge transfer between surface dopant and host 2D materials without introducing significant defects at the surface of 2D materials. Caesium carbonate (Cs_2CO_3) is found to strongly *n*-dope BP owing to the large work function difference.[66] The *p*-type dominant transport property can be gradually changed to ambipolar and finally to *n*-type dominant as the Cs_2CO_3 thickness grows. After Cs_2CO_3 decoration, the electron mobility of BP FETs increases from 1 $cm^2V^{-1}s^{-1}$ to 27 $cm^2V^{-1}s^{-1}$. As the surface charge transfer from Cs_2CO_3 may suffer from the low mobility and poor effectiveness of electron transfer into BP, metal adatom doping is proposed for its effective electron transfer. Copper (Cu) adatoms and Al adatoms are both reported to be electron donors that greatly shift Fermi level of BP into conduction band (Figure 1.10).[67, 68] These adatoms have great *n*-doping effect on pristine BP, altering the *p*-type BP FETs to *n*-type polarity. The electron mobilities of BP with Cu adatoms and Al adatoms can reach 380 $cm^2V^{-1}s^{-1}$ at room temperature and 1400 $cm^2V^{-1}s^{-1}$ at 260 K, respectively. These feasible approaches to *n*-type BP FETs facilitates the achievement of complementary circuits based on BP, showing the promising future of BP in nanoelectronics.

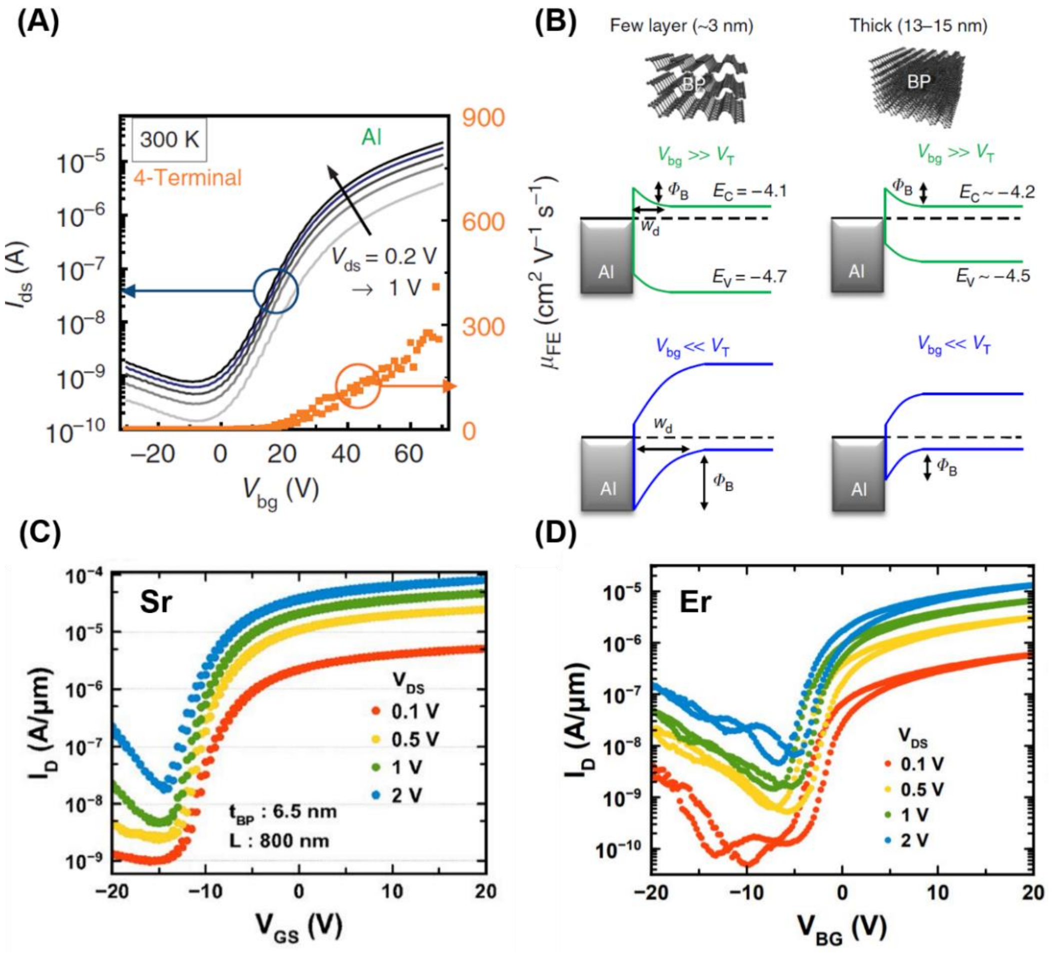

Figure 1.9 (A) Transfer curve of BP FETs with Al contact, exhibiting *n*-type transport property. (B) Schematic band diagrams for thin and thick BP flakes with Al contact.[64] (C) and (D) Transfer curves of BP FETs with (C) Sr and (D) Er contacts.[65]

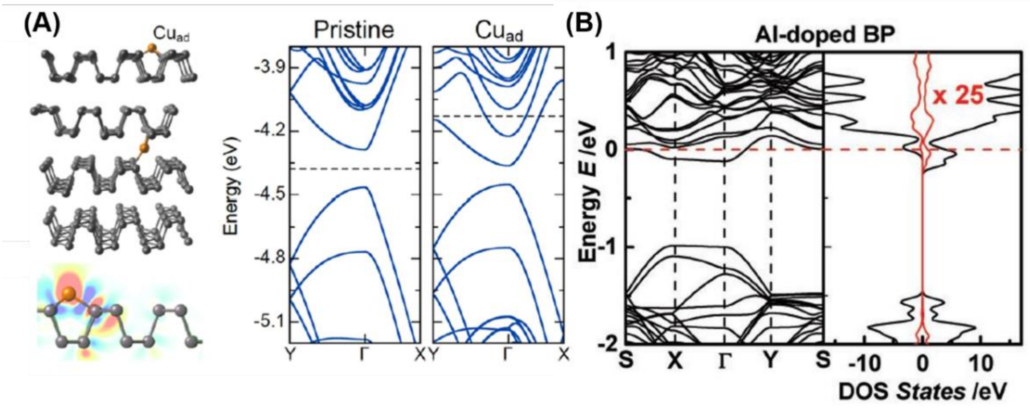

Figure 1.10 (A) DFT calculation of bandgaps of pristine and Cu-doped BP.[67] (B) DFT calculation of bandgap of Al-doped BP. The Cu-doped and Al-doped BP both show the great shift of Fermi level into conduction band.[68]

BP is also an excellent candidate for the applications in high frequency electronics.[69] The applications of 2D materials in high frequency electronics began with graphene FETs for the high carrier mobility of graphene.[70] However, graphene RF transistors are fundamentally limited because zero-bandgap nature of graphene cause the lack of current saturation, which restricts high frequency performance. The advantages of BP transistors over graphene transistors for high frequency electronics is the finite bandgap and relatively high carrier mobility of BP, for which BP FETs exhibit good current saturation behavior. Wang *et al.* first demonstrated the BP FETs operated in the gigahertz frequency range.[69] They chose few-layer BP with 6−10 nm thickness for device fabrication, which has balanced on/off ratio and hole mobility for RF applications. The as-fabricated devices with 300 nm channel exhibit a short-circuit current gain cut-off frequency f_T of 12 GHz and a maximum oscillation frequency f_{max} of 20 GHz. The high frequency performance of BP is comparable with graphene in terms of f_T but exceeds in terms of f_{max}. The operation of BP FETs in GHz range reveals the potential of BP transistors as power and voltage amplifiers in GHz frequency analogue.

BP FETs, as one of the beat device applications of BP, have made great progress with intensive research interests. The thorough understanding on transport behavior offers numerous approaches including interface engineering, contact engineering and surface transfer doping to improve device performance and achieve *p*/*n*-type polarity with same BP channel, which benefits high-performance complementary circuits. BP also shows its excellency in high frequency devices. These features are showing BP a promising 2D semiconductor with great potential in future nanoelectronics.

1.2.2.2 Optoelectronic Devices

Optoelectronic devices based on 2D materials have been investigated since the exploration of 2D materials.[53, 71] Graphene photodetectors are limited due to the nature of zero-bandgap of graphene.[72] Although 2D TMDs shows some interesting optoelectronic properties, their relatively large bandgaps confine the usage in visible range.[73-75] BP has a relatively small layer-dependent direct bandgap covering a broad range from the visible to the infrared in electromagnetic spectrum, which facilitates its application in photodetectors.[41] Michele Buscema *et al.* reported fabrication of 8-nm-thick BP FETs and study its optoelectronic properties as photodetectors.[11] As shown in Figure 1.11(A) and (B), the photo response to wavelengths from 640 nm to 940 nm was observed and the cutoff wavelength (λ_{cutoff}) was estimated up to 997 nm (1.24 eV), indicating the small-bandgap few-layer BP is appropriate for broadband photodetection. The responsivities (R) up to 4.8 mA/W was measured with small V_{ds} bias (200 mV). The BP FETs also show remarkably fast photo response with 1 ms for rise time (τ_{rise}) and 4 ms for fall time (τ_{fall}). Different from photodiodes which separate photo generated electron-hole pairs by internal electric field of *p*-*n* junction, the BP phototransistors extract carriers by external bias. The fast photo response time can be ascribed to the fast band-to-band recombination of the separated electron hole pairs. The broadband detection, sizeable responsivity and fast response make few-layer BP promising for photodetection. Wu *et al.* further extended the photodetection of BP to ultraviolet (UV) range.[76] They fabricated BP phototransistors with same configuration, which exhibits comparable optoelectronic properties in the visible-NIR range. For the first time, they demonstrated BP FETs as excellent UV photodetectors which shows different properties from visible-NIR detectors. Figure 1.11(C) presents a longer response time of ~ 200 s was recorded while the photocurrent was increased by 2 orders of magnitude larger than that of visible-NIR BP phototransistors. Instead of conventional band-to-band recombination, the electron-hole pairs excited by high energy recombine through trap centers from defects and charge impurities. As the excitation energy rises, increasing number of carriers from lower valence band are excited to the upper conduction band, making excited electron-hole pairs much more difficult to recombine. The excited carriers will circulate in the circuit many times until they recombine with their trapped counterparts, which leads to longer response time and larger photocurrent. The UV responsibility can reach four orders of magnitude larger than visible-NIR responsibility of BP, as presented in Figure 1.11(D). This value is also much higher than that of other 2D materials. The broadband detection from UV to NIR resulting from the small direct bandgap of few-layer BP shows superior optoelectronic properties of BP and its great potential in photodetectors.

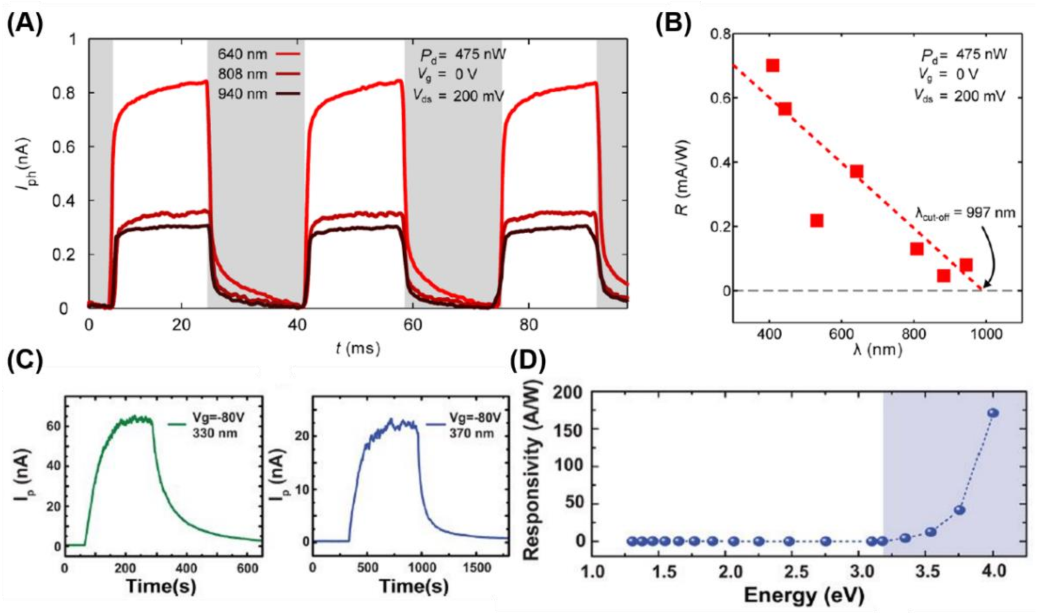

Figure 1.11 (A) Photocurrent of BP phototransistors under light excitation (~20 Hz) with different wavelengths. (B) The relationship between responsivity and excitation wavelength at constant power.[11] (C) Photocurrent response of BP phototransistors under wavelength 330 and 370 nm. (D) Photoresponsivity of BP phototransistors under light excitation within the energy range 1 ~ 4 eV.[76]

BP also allows polarization-sensitive photodetection owing to its anisotropic properties. Optical linear dichroism is expected along *x* (AM) direction and *y* (ZZ) direction with anisotropic crystal structure.[41] Theoretical calculation in Figure 1.12 presents that for polarized light parallel the *x* direction of BP, the band edge of first absorption peak is at the bandgap. This peak will greatly decrease from 1.55 eV to 0.46 eV as the thickness grows from monolayer to bulk. By contrast, with *y*-polarized light, this peak is located at 3.14 eV for monolayer BP and changes slightly as BP becomes thicker, which remains at 2.76 eV in bulk BP. This optical linear dichroism results from the anisotropic electronic structure of BP and have been experimentally investigated. Yuan *et al.* performed polarization-dependent absorption and reflection measurements.[77] In infrared range, the reflection spectrum experiences a sudden drop for incident light that has larger photon energy than the bandgap of BP and polarization direction parallel the x axis of BP crystal. By contrast, the reflection of y-polarized light exhibits no decrease near the band edge. This suggests that more photons are absorbed with x-polarized incident light than with y-polarized incident light. The photocurrent of as-fabricated BP photodetectors simultaneously shows peak value with x-polarized light and a minimum with y-polarized light. In the wavelength range from 400 nm to 1700 nm, the photo responsivity is much higher with x-polarized incident light, further confirming the optical linear dichroism and the resulting polarization-dependent photocurrent generation. The polarization-sensitive photodetection brings BP new functionalities and great potential in novel optoelectronic device applications.

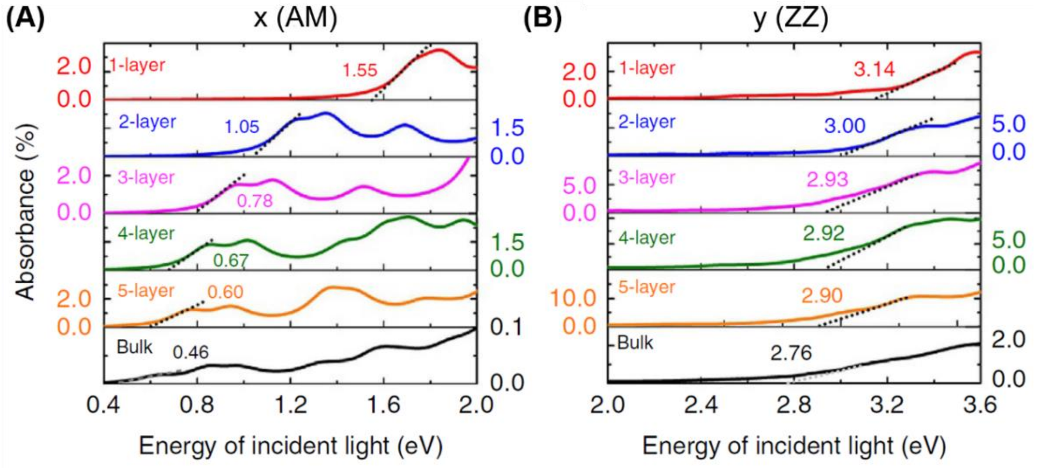

Figure 1.12 Theoretical calculation on optical absorption spectra of few-layer BP for light polarized along AM and ZZ directions.[41]

In addition, high speed optical communication benefits from the feasible applications of BP. Youngblood *et al.* studied the response of BP photodetectors to optical signal with a wide frequency range from 10 Hz to 10 GHz.[78] When devices are gated at low doping regime, a fast response was observed with a roll-off frequency of 2.8 GHz. The photocurrent generation is dominated by photovoltaic mechanism at low doping regime, which is limited by carrier recombination time in BP. In contrast, when it is gated at high doping regime, the photocurrent generation is dominated by bolometric effect which is limited by low thermal conductivity of BP, resulting for the slower response with a lower roll-off frequency of 0.2 MHz.

BP has shown its great potential in optoelectronic devices. The great advantage of BP is its small tunable direct bandgap covering a wide range of wavelength from the visible to the infrared. The broadband detection provides BP feasibility of photodetector applications. In the visible to the infrared range, the photocurrent generation is governed by photovoltaic mechanism which allows fast band-to-band recombination of photogenerated electron-hole pairs and successively offers fast response to incident light. The detection range is further widened by different photocurrent generation mechanism, extending the photodetector applications of BP. The optical linear dichroism of BP resulting from anisotropic electronic structure also allows polarization-dependent photodetection, which facilitates BP applications in novel optoelectronic devices. The performance of BP based phototransistors can be enhanced by multiple approaches including contact and interface engineering.[53, 61] Apart from the phototransistor configuration for photodetectors, the *p*-type BP can also form *p*-*n* junction heterostructure with other *n*-type 2D materials, achieving photodetection by photodiodes.[79, 80]

In this section, the understanding on crystal and electronic structure of BP is first introduced, showing BP a promising 2D semiconductor with tunable direct band gap and high carrier mobility. The excellent electronic properties of BP facilitate the device applications including FETs and photodetectors. High-performance devices based on few-layer BP are demonstrated and continuously enhanced by various approaches like contact engineering and interface engineering. Although BP suffers from difficulty of large-area preparation and instability in atmosphere condition, BP still attracts intensive research interests which helps BP fulfill its potential in future nanoelectronics.

1.3 Introduction to Tellurium

Although few-layer BP possesses striking electronic properties and fascinating device applications, a huge challenge for BP is the high-efficiency and large-area preparation of BP with controllable thickness. The fabrication of high-performance BP devices still relies on mechanical exfoliation for BP channel. The bottom-up synthesis of high-quality few-layer BP has yet to be achieved. Considering this, researchers call for an alternative material that succeeds outstanding electronic properties of few-layer BP and has reliable preparation approaches. Because of this, tellurium (Te) in its 2D or few-layer form is discovered recently.[16, 81] The reported tellurene (Te), few-layer form of Te is prepared by solution synthesis with large-area and high-yield production. The preliminary electrical measurement shows its excellent semiconducting properties. Owing to the discovery, Te as the newest member of 2D materials rapidly attracts extensive research interests on fundamental study and technical applications.[42, 82, 83]

Bulk and few-layer Te share the same trigonal crystal structure (Figure 1.13) in which individual helical chains of covalently bound Te atoms are parallel-aligned and oriented along the [001] direction.[42] These chains are stacked together by weak interaction. The crystal structure of Te with weak interaction in two directions is quite different from that of conventional 2D materials including graphene, TMDs and BP in which only interlayer bonding is van der Waals interaction. Due to the different structure anisotropy, Te prefers one-dimensional (1D) nanostructurs like nanowires, nanotubes and nanobelts.[84, 85] The successful preparation of 2D structure opens new opportunities for Te and extends the applications of Te in nanoelectronics. Several theoretical predictions and experimental works have demonstrated 2D Te a promising 2D semiconductors with intriguing electronic properties including high carrier mobility and high optical absorption.[16, 42, 84]

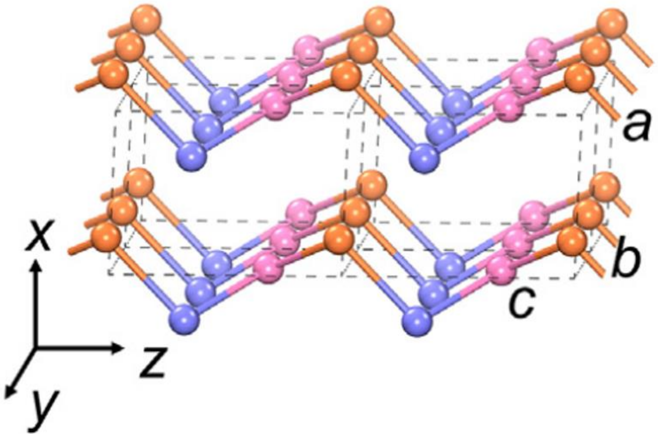

Figure 1.13 Crystal structure of few-layer Te.[42]

1.3.1 Preparation of Te Nanomaterial

To realize various applications of 2D Te, a reliable preparation approach to large-area, high-yield and high-quality 2D Te samples is greatly important for experimental research and industry. As the structure anisotropy of Te gives itself a strong trend toward 1D growth, the very early research works provide multiple approaches to 1D structure of Te, which can be references to 2D structure growth. In the last century, vapor deposition has been reported to produce Te whiskers with a few micrometers' length by direct sublimation of solid Te.[86] The morphology of Te whiskers is controlled by the substrate temperature. As the substrate temperature rises, the shape of Te whiskers changes from spines to filaments and finally to needles. It is also found that the high temperature reduces the dislocation in Te whiskers. Similar PVD is proposed by Li *et al.* years after.[87] Te tubes in a shape of hexagonal prisms with diameters ranging from ten to several hundred micrometers and length up to several centimeters are synthesized by simple evaporation of Te powder, which are greatly influenced by the reaction temperature and flow rate. The nucleation and growth processes with thermodynamic effect dominate the formation mechanism of Te tubes growths. The anisotropic structure is the primary reason for the formation of Te tubes and the thermodynamic effect prefers exposed crystal facet with lowest surface free energy. The combination of both effects leads to the growth of Te tubes with hexagonal cross section. Except physical vapor deposition, chemical vapor deposition for Te is also demonstrated using Al_2Te_3 solid and H_2O vapor as precursors through chemical reaction in Ar atmosphere at 500 °C.[88] The as-prepared single-crystalline Te nanobelts have a thickness of about 10 to 20 nm, a width of 50 to 300 nm and a length up to tens of micrometers.

Vapor deposition is always an important preparation method for large-area and high-quality nanomaterials. However, the relatively high temperature limits the choice of growth substrates and some applications. Solution synthesis offers feasible routes to free-standing Te nanomaterials with large scale and much lower reaction temperature. Xia and colleagues reported the reduction of orthotelluric acid or tellurium dioxide by hydrazine at various refluxing temperatures (90 ℃ to 200 ℃) to synthesize 1D structure of Te including spines, filaments, needles and tubular structures.[89] The morphology control is achieved by refluxing temperature. Mo *et al.* subsequently proposed a hydrothermal route by the disproportionation of sodium tellurite in aqueous ammonia at 180 ℃.[90] The as-synthesized Te nanobelts have an average thickness of 8 nm and a width of 30 to 500 nm. The hydrothermal process can also be assisted by polymer surfactant poly(vinyl pyrrolidone) (PVP) to prepare uniform Te nanowires with a diameter of 4-9 nm and nanobelts with a width of 250-800 nm.[91] The reaction parameters in the hydrothermal process including temperature, pressure, surfactant and precursor concentration have received detailed investigation and are revealed to dictate the formation of 1D structure of Te, which achieves the control over shape, thickness, width and length of Te nanomaterials. Vapor deposition and solution synthesis for Te in the early works offer great inspiration for the preparation of 2D Te.

With the basis of early works on 1D Te growth, vapor deposition and solution process have been extended to attain 2D Te including Te films, Te plates and Te flakes. Atomically flat Te thin films are reported to be van der Walls epitaxially grown on graphene/6H-SiC(0001) substrates and highly oriented pyrolytic graphite (HOPG) by molecular beam epitaxy (MBE), as shown in Figure 1.14(A).[92, 93] The few-layer films are formed with helical Te chains horizontally aligned. MBE provides high-quality production and atomic scale precise control on the thickness. Monolayer Te films are successfully MBE-deposit on HOPG by delicate control of reacting time, which is found to form different phase from few-layer and bulk Te. Although MBE combined with scanning tunneling microscopy (STM) can prepare and in-situ characterize pristine Te films, it suffers from the high cost, low efficiency and substrate limitation. Wang *et al.* demonstrated the PVD methods for hexagonal Te plates on the mica sheets.[94] The obtained single-crystalline Te plates as shown in Figure 1.14(B) have a thickness ranging from 30 to 80 nm with a few micrometers lateral size. The growth substrates, mica sheets have a surface free of dangling bond and resulting weak van der Waals interaction with Te, which promotes the migration of Te adatoms during deposition and facilitates the growth of Te plates without strict lattice mismatch. The growth of Te plates simply follows the Volmer-Weber model involving formation of Te nanoparticle, diffusion of Te adatoms and mergence into hexagonal structure. The Te plates are distinguished from other reported 2D Te because of the vertically aligned Te chains in plates, which may be related to the vertical sharp tips of Te nanoparticles at the initial growth. PVD also can realize growth of Te thin films with growth substrates at cryogenic temperatures.[95] Te thin films with thickness varying from 8 to 30 nm and micro-size domains, as presented in Figure 1.14(C), are attained with a substrate temperature of -80 °C. The film quality is significantly influenced by the substrate temperatures. The domain size is decreased from 25 μm^2 to 3 μm^2 as the substrate temperature rises from -60 °C to -10 °C. The film will lose its uniformity and consist of small particles when the growth substrates are at room temperature.

Another important growth method, solution synthesis is also presented to successfully prepare Te flakes. Wenzhuo Wu’s group shows the fabrication of Te thin flakes through the reduction of sodium tellurite by hydrazine hydrate assisted with PVP in an alkaline solution at 160 to 200 °C.[16] The micro-size Te flakes (Figure 1.14(D)) have a thickness from 10 to 100 nm. In the proposed solution process, PVP concentration is of great importance to 2D growth of Te. The medium level of PVP as surfactant in growth can well adjust the growth rate at width and thickness direction, changing initial 1D growth to sequent 2D growth. The thickness of Te flakes can be further reduced below

10 nm after a solvent-assisted post-growth thinning process. By controlling the pH of dispersion solution in this process, monolayer, bilayer and trilayer Te can be obtained.

With intensive research efforts, bottom-up methods including vapor deposition and solution synthesis are successful to prepare 2D Te, although these methods are still underdeveloped compared with the growth of graphene and 2D TMDs. Solution synthesis can prepare large-area, high-quality, free-standing and single-crystalline Te thin flakes, which is suitable for high-performance device demonstration. The substrate-free growth also facilitates some applications like flexible electronics with Te. However, the thickness variation limits large-scale applications, which can be further enhanced by delicate control of reaction parameters. The failure for wafer scale Te samples also hampers the application of solution synthesis in industry. Although vapor deposition is possible for wafer scale samples, the state-of-art is far from satisfactory. The obtained single-crystalline Te plates and polycrystalline Te thin film both have relatively low quality. Without detailed investigation on deposition parameters, the feasible and high-efficiency vapor deposition for large-scale, high-quality and single-crystalline 2D Te have not yet achieved, which is worth future exploration.

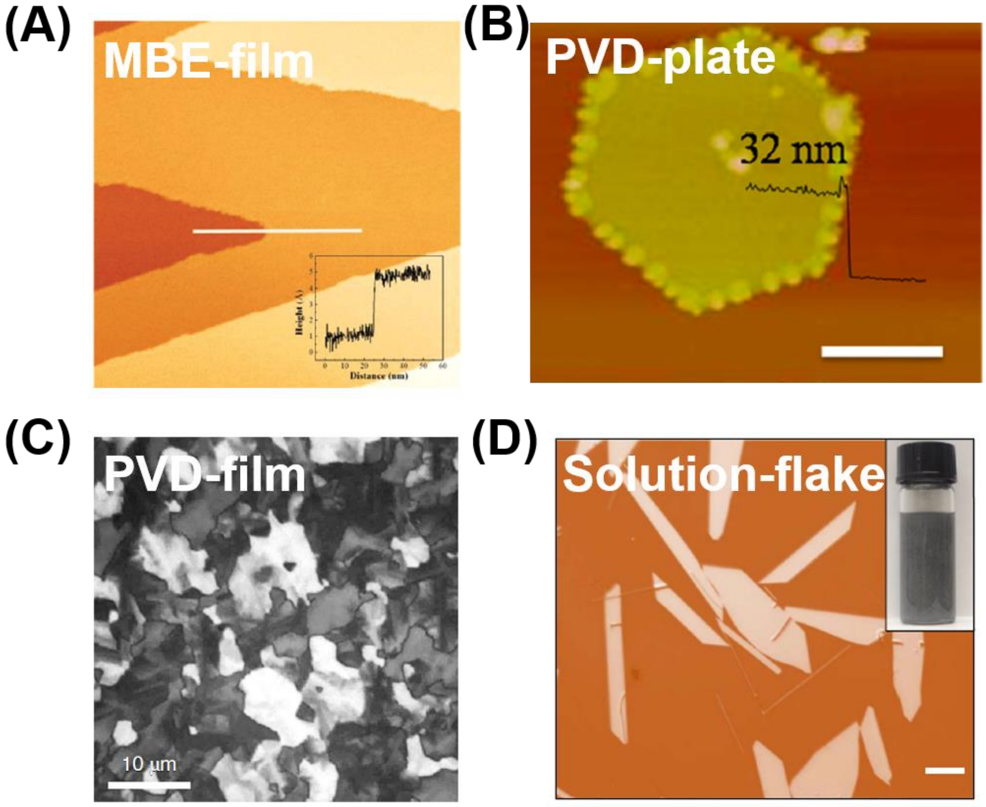

Figure 1.14 (A) Topographic image of MBE-grown Te film.[93] (B) AFM image of Te hexagonal plate by PVD.[94] (C) Polarized light microscopy image of PVD-grown Te film.[95] (D) Optical image of Te flakes by solution synthesis.[16]

Apart from bottom-up methods, top-down methods also succeed in preparing 2D Te. Mechanical exfoliation by sliding a freshly cleaved facet of Te on SiO_2 substrates is shown,[96] but the exfoliated Te with 15-nm thickness only has a width of 1-2 μm. As the Te chains in bulk are bonded by weak interaction, they will break away from bulk vertically and laterally, forming thin and narrow belt-like structure, unlike other mechanical exfoliated 2D materials (graphene and TMDs) with large flat surface. Liquid exfoliation is another top-down method.

The reported 5-nm-thick Te nanosheets by liquid exfoliation have very small lateral size in a range from 41.5 to 177.5 nm.[97] Although exfoliation methods offer routes to Te nanomaterials, the size of obtained Te is quite small, which is extremely inappropriate for electronic device.

1.3.2 Physical Properties of Te

Before exploration of device applications of Te, thorough understanding on the physical properties especially electronic properties is of great importance. As an emerging member of 2D materials, 2D Te has received only a few theoretical predictions and experimental studies. Wei Ji's group reported detailed theoretical calculations on the crystal phases and electronic structures of 2D Te.[42] Under normal condition, the α-phase Te with same crystal structure as bulk Te is the most stable phase for few-layer thickness (Figure 1.15 (A) and (B)). When the thickness is reduced to monolayer, the α-phase will transfer without a barrier to more stable β-phase, in which a Te helical chain moves towards the adjacent chain and forms an addition mirror symmetry (Figure 1.15 (C) and (D)). This different monolayer phase is experimentally confirmed by the MBE-grown monolayer Te on HOPG, of which the topographic STM image shows its in-plane lattice consistent with the predicted β-phase.[93] Although α-phase is more stable beyond monolayer thickness, the small energy difference (Figure 1.15(E)) between *α*- and *β*-phase and geometrical similarity may result in reversible phase transition *α*-*β* by strain or doping engineering.[42] Due to limiting research investigation, the physical properties of *β*-phase Te and the phase transition *α*-*β* are undisclosed, which still needs further exploration. Here, we will focus on the physical properties and device applications of few-layer *α*-phase Te owing to its feasible preparation.

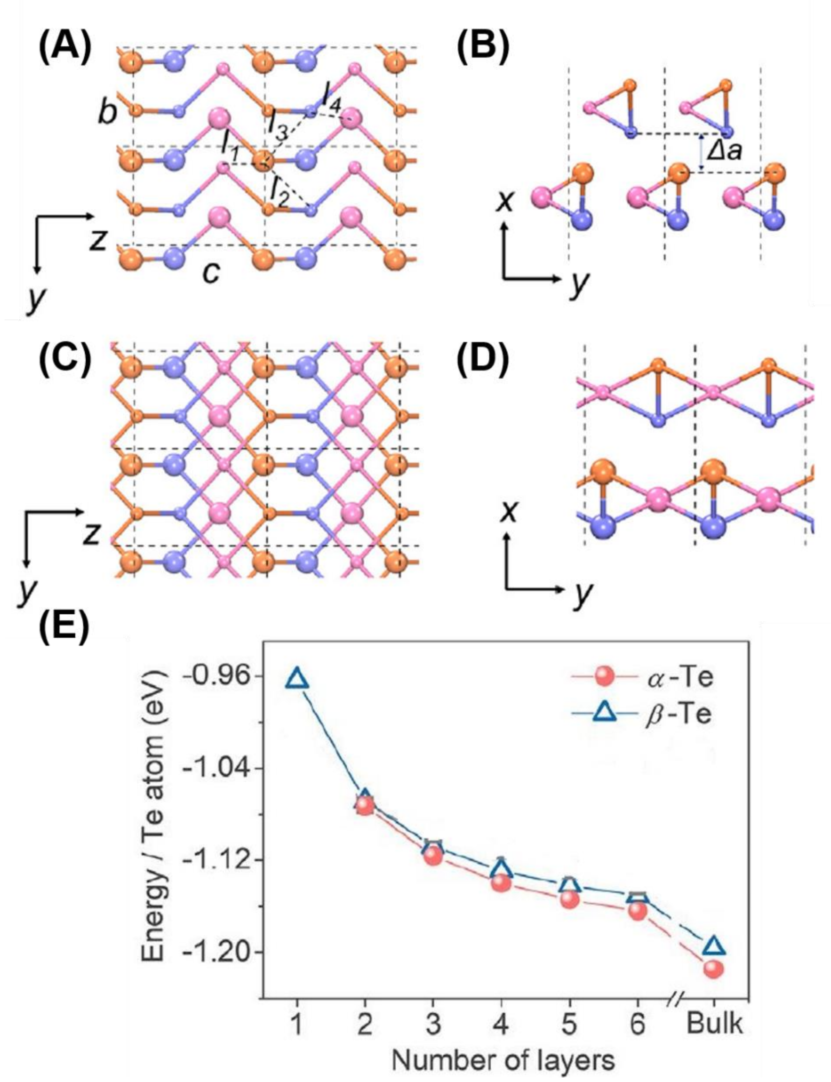

Figure 1.15 (A) and (B) Crystal structure of α-Te in the (A) top-view and (B) side-view. (C) and (D) Crystal structure of β-Te in the (C) top-view and (D) side-view. (E) Thickness-dependent energy stability of α-Te and β-Te.[42]

Few-layer α-phase Te is predicted to exhibit excellent semiconducting properties. In DFT calculation (Figure 1.16), bulk Te is found to have a nearly direct bandgap of 0.31 eV and the bandgap is expected to increase as thickness reduction.[42] The thinnest bilayer α-Te (monolayer Te is β-Te) have a predicted indirect bandgap of 0.9 eV. The prediction also shows the significant change of valence band maximum (VBM) from -4.98 to -4.35 eV and slight change of conduction band minimum (CBM) as thickness increases, suggesting *p*-type contact of bilayer α-Te with most metals. The thickness-dependent bandgap of 2D Te is also experimentally revealed by scanning tunneling spectroscopy (STS).[92] MBE offers high-quality epitaxial Te films with precise control on layer number. The bandgaps are determined by STS for monolayer (0.92 eV), bilayer (0.85 eV), trilayer (0.74 eV) and 13-layer (0.49 eV) Te, in agreement with the DFT calculations.[42] In addition to bandgap covering mid-infrared to red range, the extraordinarily large carrier mobility is expected 10^4-10^6 $cm^2V^{-1}s^{-1}$ for hole and 10^3-10^4 $cm^2V^{-1}s^{-1}$ for electron in 2D Te, appreciably larger than that of 2D TMDs and few-layer BP.[42] The structure anisotropy of Te suggests an anisotropy in carrier mobility. The mobilities along the *y* direction are generally larger than those along the *z* direction, which is related to interchain covalent-like quasi-bonding (CLQB) bonding. The layer-dependent bandgap and extremely large carrier mobility make 2D Te a promising 2D semiconducting channel and facilitate its applications in FET devices.

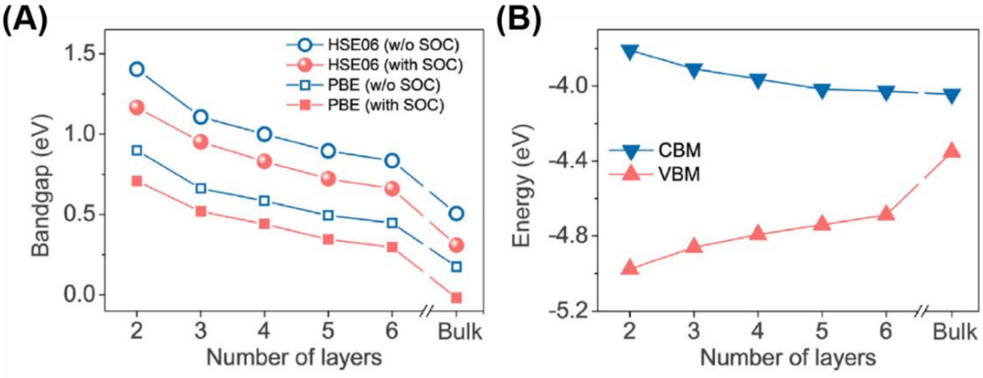

Figure 1.16 (A) and (B) Theoretical calculation on the thickness-dependent bandgaps, positions of CBM and VBM.[42]

To evaluating the possibility of Te application in photodetectors, it is vital to establish the understanding on optoelectronic properties of 2D Te. DFT calculation presents the relatively high absorbance for normal incident light (~ 9% at 3.2 eV), which is larger than that of BP.[42] It is interesting to notice that the light absorption exhibits near isotropy with bilayer to 5-layer thickness (Figure 1.17(A)) despite of the structure anisotropy and restores anisotropy at 6-layer or thicker Te (Figure 1.17(B)). The energy of absorption edge is about 0.2 eV larger than the predicted bandgap, suggesting inter-band transition and carrier transfer in 2D Te. These predicted features indicate great potential of Te in optical applications, which still requires detailed experimental investigation. For infrared light, Te offers another photo response mechanism owing to its excellent thermoelectric property.[98, 99] Thermoelectric effect enables a direct conversion between heat and electricity, which has always been one of working mechanisms for infrared detectors. As shown in Figure 1.17(C), with local heating by infrared laser, the carrier concentration in thermoelectric materials will change and induce a diffusion current, achieving photodetection based on thermoelectric effect.[98] The figure of merit zT determining the performance of a thermoelectric material is measured to be ~ 1.0 for Te, higher than other element-based thermoelectric materials, which indicates the potential of Te in photothermal detectors.[99] Owing to the photovoltaic and thermoelectric effects discovered in Te, 2D Te is greatly promising for photodetection in infrared range.

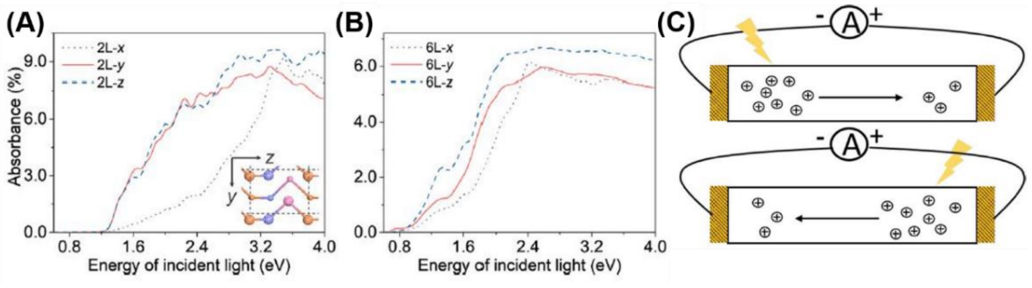

Figure 1.17 (A) and (B) Predicted absorbance of (A) bilayer and (B) 6-layer Te

under incident light with the polarization direction along *x*, *y* and *z*.[42] (C) Schematic of photothermal effect in Te.[98]

Compared with few-layer BP which is limiting in device applications due to its environmental instability, few-layer Te shows its superiority in great air-stability.[42] The prediction reported the sufficient reaction energy barrier (0.85~0.94 eV) to prevent the oxidation of Te at atmosphere, suggesting the environmental stability of Te. The stability is also experimentally confirmed by the performance retention of Te FETs exposed to air. The excellent environmental stability of Te is critical for the fundamental studies and realization of various applications in industry.

1.3.3 Device Applications of Te

Excellent semiconducting properties of 2D Te have attracted intensive research interests in exploration of device applications. FETs are one of typical device applications for most 2D materials. Wang *et al.* demonstrated the very first FET based on few-layer Te prepared by solution synthesis.[16] As shown in Figure 1.18 (A), the device with Pd contacts and 7.5-nm-thick 2D Te channel exhibits outstanding *p*-type characteristic with high on/off ratio of 10^5 and large drain current of 300 mA/mm. The *p*-type characteristic results from the high level of

VBM of Te as predicted. The thickness-dependent field-effect mobility (Figure 1.18(B)) is also studied, showing a peak value of 700 $cm^2V^{-1}s^{-1}$ for 16-nm-thick Te flakes at room temperature. The drain current can reach record-high value of 1 A/mm by scaling down the channel length to 300 nm and utilizing ALD-grown high-κ dielectric. The demonstration of high-performance Te FETs opens up opportunities for Te applications in future electronics. However, the large-scale or wafer-scale deposition of high-quality Te still limits the application in industry. Figure 1.18 (C) to (E) shows the device performance of *p*-type FET fabricated with vapor-deposited Te film as channel, which is recently reported Zhao *et al.*[95] The device structure consists of Ni metal contacts and 5-nm ZrO_2 gate dielectric. The typical FET device exhibits on/off ratio of ~10^4, an effective hole mobility of ~35 $cm^2V^{-1}s^{-1}$ and SS of 108 mV/dec at room temperature. Compared with figures of merit of FET based on solution synthesized Te, the poorer performance of Te film suggests the low quality of vapor-grown Te film, which is attributed to the polycrystallinity of Te film and the relatively small crystal size. The device performance can be enhanced with availability of vapor deposition for high-quality Te, which still need further investigation.

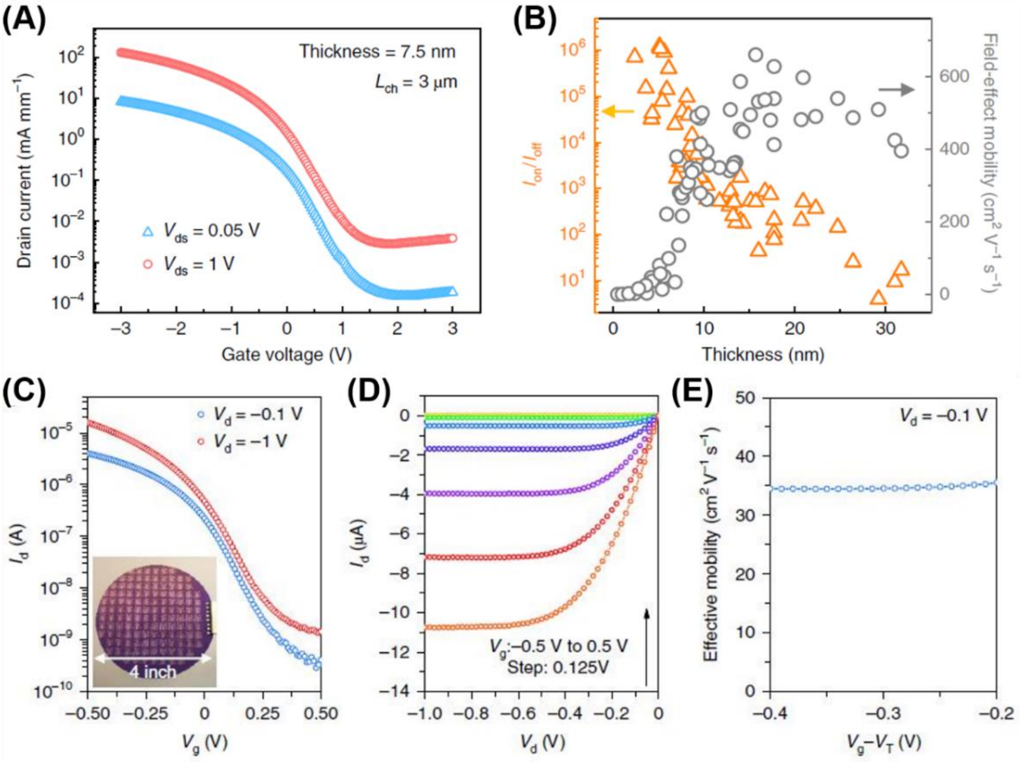

Figure 1.18 (A) Transfer curve of a typical FET with 7.5-nm-thick solution-Te as channel. (B) Thickness-dependent on/off ratio and field-effect mobility of solution-Te.[16] (C) and (D) Transfer curves and output curves of FETs with 8-nm-thick PVD-Te films as channel. (E) Field-effect mobility of PVD-Te derived from transfer curves.[95]

Photodetectors are another potential device application for few-layer Te with photovoltaic and thermoelectric effects. Amani *et al.* presented short-wave infrared (SWIR) photodetectors with solution synthesized Te flakes as channel.[100] By utilizing an optical cavity with optically thick Au and Al_2O_3 dielectric spacer layer (Figure 1.19(A)), the device exhibits a peak responsivity of 16 A/W with positive gate voltage (Figure 1.19(B)). A peak specific detectivity of 2.9×10^9

cmHz$^{1/2}$W^{-1} is measured and the Hz-dependent rise/fall time is observed. These figures of merit suggest the 2D Te flakes promising materials for high-performance optoelectronic devices. The successive research work demonstrated the Te-based photodetectors also possess a high gain up to 3.15×10^4 at 3.39 μm wavelength due to the photogating effect. A large bandwidth of 37 MHz is shown at the communication wavelength (1.55 μm). In addition, photocurrent can be generated by thermoelectric effect of Te. Qiu *et al.* studied the thermoelectrical current in Te flakes stimulated by local laser heating.[98] Figure 1.19(C) shows the schematic of device structure and Figure 1.17 (C) indicates the photocurrent generation. It is found that the high-work-function metals can more efficiently collect thermoelectrically generated carriers due to the accumulation-type contacts, which achieves photocurrent at μA range (Figure 1.19(D)). The thermoelectric effect of Te facilitates its applications not only in photothermal detectors but also micro energy harvesting systems, indicating the great potential of Te.

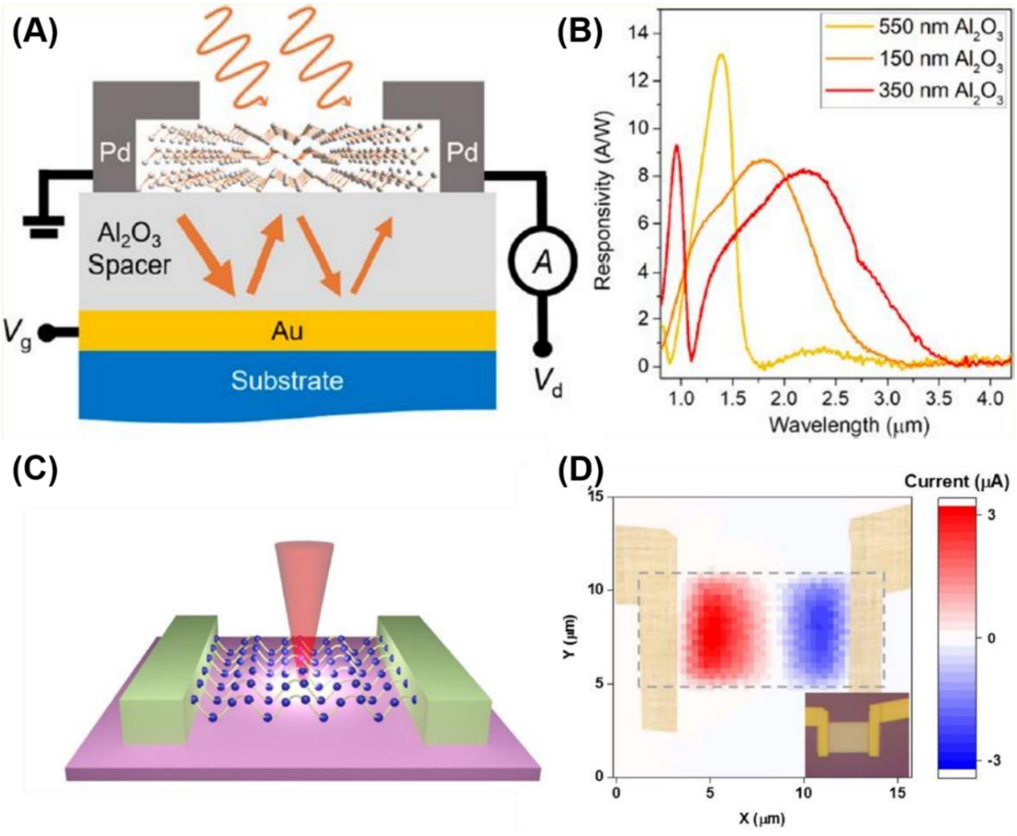

Figure 1.19 (A) Schematic of SWIR photodetector based on 2D Te. (B) Measured responsivities of 2D Te.[100] (C) Device structure of Te photodetector based on photothermal effect. (D) The current mapping image of photothermal detectors with Te channel.[98]

In this section, the feasible preparation methods of few-layer Te are first introduced. Based on thorough investigation on growth of 1D Te, the synthesis of 2D Te is developed and high-quality Te thin flakes are obtained by solution synthesis. However, the large-scale or wafer-scale vapor deposition of Te still needs more research efforts for high-quality Te film. After successful preparation of 2D Te, the physical properties including crystal phases, electrical properties, optical properties and stability receive theoretical calculations and experimental studies, suggesting Te promising in nanoelectronics.[16, 42, 84, 100] Pioneering device applications of Te are demonstrated recently.[16, 84, 100] The high-performance FETs and optoelectronic devices present air stable Te is excellent compared with BP, suggesting the great potential of Te in future nanoelectronics.

1.4 Research Objectives

1.4.1 Contact Engineering on BP

For low-power complementary circuits, it is important to fabricate both *p*-type and *n*-type transistors with same channel materials. Due to the Fermi level pinning at the contacts and the suppressed electron transport caused by oxygen and moisture exposure, the BP transistors usually exhibit *p*-type dominant transport property. Surface doping and contact engineering have been applied to modulate the carrier type and achieve *n*-type BP transistors. However, surface doping is not compatible with integrated circuit industry. The utilization of low-work-function metals, although compatible with industry, suffers from Fermi level pinning effect, which may change the polarity of devices. It has been reported BP FETs with Sc contacts can exhibit both *n*-type and *p*-type transport property. Therefore, it is worth finding another reliable solution to achievement of *n*-type BP FETs.

In theory, metal Cu is proposed to make excellent contact with BP. Also, Cu adatoms can act as electron donor and *n*-dope BP, which greatly shifts the Fermi level of BP towards conduction band and modulates the polarity of BP channel from *p*-type to *n*-type. The Cu contact for BP FETs has not been experimentally demonstrated. In addition, the contact doping effect from Cu is also not studied theoretically, which requires further investigation.

1.4.2 Transport property of Te

The 2D semiconductors are promising candidates replacing convention Si channel due to the ultrathin thickness and dangling-bond-free surface of 2D materials. The application of 2D semiconductors can alleviate the severe short channel effect in continuously downward scaling. The 2D materials with high carrier mobility and an appropriate band gap are desired in future nanoelectronics. Recently, the semiconducting 2D Te is rediscovered since it possesses outstanding physical properties including higher carrier mobility than TMDs and much better air stability than BP, which shows the great potential of 2D Te in future electronics.

As one of the newest members of 2D materials, 2D Te only received a few theoretical studies and experimental works presenting excellent electrical properties and some appealing applications (*e.g.* FETs, optoelectronic devices and thermoelectric devices). Although the reported works have shown the promising applications of 2D Te in nanoelectronics, the carrier dynamic and transport property have not yet received thorough understanding compared to other popular 2D materials. Metal contact is one of critical factors influencing the carrier transport in 2D material. It is predicted that metals including Cu, Ni, Ag, Pt and Pd can form lateral *p*-type Schottky contact with 2D Te due to Fermi level pinning. The limited research studies on contact engineering of 2D Te require further investigation to develop transport understanding and enhance device performances.

1.4.3 Thinning of few-layer Te

Few-layer Te has shown its promising applications in future nanoelectronics for its excellent electrical properties. Before the exploration of various applications of 2D Te, preparation for large-area, single-crystalline and high-quality samples is necessary. The precise thickness control of few-layer Te is important because the thickness-dependent properties greatly determine the performance of devices. There are some reported growth methods for Te samples including vapor deposition and solution synthesis. Despite the success of few-layer Te preparation, the quality and thickness control of as-grown samples are still beyond satisfactory.

Thinning is another approach to 2D materials with desired thickness, which has succeeded in other popular 2D materials. The thinning processes include local laser thinning, plasma treatment, thermal annealing and chemical reaction in solution. As an emerging 2D material, 2D Te does not have received adequate research works on thinning process. Solvent-assisted process using alkaline solution with acetone is one of reported thinning methods for 2D Te. Although this method can thin few-layer Te down to monolayer, the precise thickness control and local etching of 2D Te remains challenges. The thinning methods for Te can not only benefit the studies on thickness-dependent properties but also achieve devices based on 2D Te with desired thickness, which is worth future investigation.

1.5 Structure of Thesis

The chapters of this thesis are organized as follows:

Chapter 1: Introduction. In this chapter, the diversity of 2D materials and continuously developing preparation methods are presented, which facilitates various applications based on 2D materials. The applications of 2D semiconductors in nanoelectronics are focused. This chapter will first introduce the great advantages of 2D semiconductors over commercial Si, which are the atomically thin and uniform thickness resulting from 2D nature. Among various 2D semiconductors, we will focus on elemental 2D materials, BP and Te. For BP that was rediscovered several years ago, the electronic structure of BP is first shown, which is the fundamental for applications of few-layer BP. FET devices and optoelectronic devices are two cases introduced to illustrate BP a promising 2D semiconductor for nanoelectronics. As for Te which was demonstrated recently, the preparation methods are first reviewed, followed by theoretical studies and some experimental works on the properties of Te. Afterwards, some demonstrations on devices based on few-layer Te are introduced, indicating great potential of Te.

Chapter 2: Interstitial Copper-Doped Edge Contact for *n*-type Carrier Transport in Black Phosphorus. In this chapter, the *n*-type dominant BP transistors are demonstrated achieved by contact engineering. The interface between Cu contacts and few-layer BP will be first investigated. The Cu-doped BP edge contact is theoretically studied and experimentally characterized, which is found to facilitate the electron transport in BP. The detailed electric characterizations on BP transistors are conducted, suggesting high-performance *n*-type BP FET devices with Cu contacts.

Chapter 3: High-Performance Tellurium Field-Effect Transistors with High-Work-Function Metal Contacts. In this chapter, the high-performance unipolar *p*-type Te FETs with high-work-function metal contacts are demonstrated. The electrical properties and device performance are carefully characterized. The *p*-type characteristic is attributed to the well-match band alignment between few-layer Te and metal contacts (Pt and Pd). The detailed contact resistance measurement and low-temperature characterization suggest the excellent contacts resulting in the high-performance devices.

Chapter 4: Local Thinning Method for Few-layer Tellurium with Platinum Catalysis. In this chapter, a thinning method is developed for few-layer Te with Pt catalysis. The thinning process involves Te FETs with Pt contacts. The Te near Pt contacts experience thinning in water under light illumination. This process can be explained by the photo-oxidation of few-layer Te with Pt catalysis. The thickness change is recorded by Raman, AFM and electrical measurement. This method provides a feasible approach to few-layer Te with desired thickness.

Chapter 5: Conclusions and Outlooks.

Chapter 2 Interstitial Copper-Doped Edge Contact for *n*-type Carrier Transport in Black Phosphorus

2.1 Introduction

Two dimensional (2D) layered semiconductors have shown great promise for future nanoelectronics due to their ultrathin body thickness, dangling-bond-free surface and reasonably good carrier mobility.[10, 54, 101-103] Among the monoelemental 2D materials, black phosphorus (BP), also referred as phosphorene, received significant attentions for its atomic scale smoothness, widely tunable direct band gap (ranging from 0.35 eV for bulk to 2.0 eV for monolayer), and high hole mobility (10^2-10^3 $cm^2V^{-1}s^{-1}$) at room temperature.[13, 41, 104] The BP field-effect transistors (FETs) exhibit an on/off ratio about 10^5 and hole mobility up to 10^3 $cm^2V^{-1}s^{-1}$.[13] In contrast to molybdemun disulfide (one of the most studied 2D semiconductors), BP is predicted to have higher carrier mobility for both electrons and holes, which facilitates its application for complementary logic circuits.[41] Although the pristine BP has no dominant preference for carrier type, the extensively reported BP transistors exhibit *p*-type dominant transport property due to the Fermi level pinning at the contacts and the suppressed electron transport caused by oxygen and moisture exposure.[104-106] To realize low-power complementary circuits, it is important to fabricate both *p*-type and *n*-type transistors with same channel materials.[61]

Contact engineering and surface doping have been applied to modulate the carrier type and achieve *n*-type BP transistors.[64-67, 107] In recent studies, *n*-type BP transistors were fabricated by utilizing contact metals with low work function, such as aluminum (Al) and scandium (Sc).[64, 65] The *n*-type characteristic is mainly attributed to the energy level match between the conduction band of few-layer BP (E_c ~ 4.1 eV) and the work function of contact metal electrodes (Φ_{Al} ~ 4.0 eV, Φ_{Sc} ~ 3.5 eV). These low-work-function metal contacts hold the BP Fermi level close to the conduction band minimum with low Schottky barrier height (SBH) for electrons. Except utilizing low-work-function metals, surface charge transfer offers another way for modulation doping.[66, 67, 107-109] Surface functionalization with caesium carbonate (Cs_2CO_3) is reported to strongly electron dope BP, where the BP FETs exhibit transition from ambipolar to *n*-type transport property with the increase of the thickness of Cs_2CO_3.[66] Copper (Cu) adatoms can also act as electron donor and *n*-dope BP, which greatly shifts the Fermi level of BP towards conduction band and modulates the polarity of BP channel from *p*-type to *n*-type.[67] Also, metal Cu is proposed to make excellent contact with BP.[110] However, the Cu contact for BP FET has not been experimentally demonstrated. In addition, the contact doping effect from Cu is also not studied theoretically, which requires further investigation.

In this chapter, we will first investigate the interface between BP and Cu. Highly diffusive Cu atoms migrate into BP and intercalate between BP layers without changing the crystal structure of BP. The BP with interstitial Cu (Cu_{int}) is theoretically predicted to have smaller band gap than pristine BP. The Fermi level is greatly shifted towards conduction band after the Cu penetration. Through this interstitial Cu-doped edge contact, we demonstrate *n*-type dominant BP transistors with high electron mobility of ~ 138 $cm^2V^{-1}s^{-1}$ and on/off ratio of ~ 100 at room temperature. The current density can reach 58 μA/μm. This *n*-type transport property is attributed to *n*-doping induced by the penetration of highly-mobile Cu atoms at the contact region.

2.2 Methods

2.2.1 Cross-section TEM sample preparation and characterization

The BP flake was mechanically exfoliated on silicon substrates with 300-nm-thick SiO_2. 30 nm Cu and 30 nm Au were then deposited onto the BP flakes by thermal evaporator. Afterwards, the cross-section sample was prepared by dual beam multi-system FIB (JEOL Model JIB-4501) equipped with platinum (Pt) deposition cartridge: (1) Pt is deposited on selected area for protection from ion beam; (2) ion beam thins the sample down to electron transparency (< 50 nm); (3) the thin lamella is transferred to the Cu grid. The sample on Cu grid was characterized by field emission electron microscope STEM (JEOL Model JEM-2100F).

2.2.2 Device fabrication and electrical measurement

We fabricated back-gated FETs based on few-layer BP flakes. The BP flakes were first mechanically exfoliated onto 300 nm SiO_2 dielectric on highly doped Si substrates, and then coated with poly(methyl methacrylate) resist (PMMA) for lithography process. The source and drain electrodes were patterned by electron-beam lithography. Afterwards, 15 nm Cu and 40 nm Au were deposited using a thermal evaporator with a base pressure of 1×10^{-6} Torr. The devices were fabricated after lift-off process. The electrical measurements on these devices were conducted in a probe station (Lakeshore low temperature IV probe station).

2.3 Results and discussion

2.3.1 Cu diffusion in BP

Figure 2.1 shows the cross-section schematic of the BP FET near the contact region. The contact between metal and semiconductor greatly affects the contact resistance and carrier type of devices.[61] As the highly diffusive Cu may change the contact with BP, it is important to understand the interface between BP and Cu. The Raman spectrum of the BP flake in Figure 2.2 shows three sharp peaks at 361 cm^{-1}, 438 cm^{-1} and 466 cm^{-1}, corresponding to A^1_g, B_{2g} and A^2_g vibration modes. These values are consistent with the previous studies, confirming the nature of the BP flake.[104, 111, 112] To facilitate the cross-section scanning transmission electron microscopy (STEM) characterization, we chose the BP flake with a relatively large thickness. Figure 2.3 presents the cross-section STEM image of a BP flake covered with 30-nm-thick Cu layer and 30-nm-thick Au layer, which shows clear interface between the Au/Cu/BP/SiO_2 stacks. The electron energy loss spectroscopy (EELS) mapping of element Au, Cu and P qualitatively reveals the chemical distribution and provides detailed sight of the BP/Cu interface. As shown in the EELS elemental mapping, the Cu greatly penetrates the BP flakes and exhibit homogeneous distribution.

The corresponding line scan of EELS mapping in Figure 2.4 presents the slight decrease of Cu signal as the increase of penetration depth inside BP, indicating the Cu amount is gradually decreased beneath the contact.

There are substitutional and interstitial dopant atoms in the bulk crystal. To identify the existence configuration of Cu atoms, we performed detail characterization on the crystal structure of the Cu-penetrated BP. Figure 2.5(A) presents selected area electron diffraction (SAED) of the Cu-penetrated BP flake. The well-indexed diffraction pattern is in accordance with the pristine BP crystal (ICDD-PDF No. 76-1963), indicating the BP flake maintains its orthorhombic crystal structure after the Cu penetration. The high-resolution TEM (HRTEM) image in Figure 2.5(B) also clearly shows the interlayer lattice of the BP flake. The interlayer distance of BP with Cu dopant is 0.52 nm, which is still consistent with the reported values of pure BP.[113] The inserted fast Fourier transform (FFT) pattern is identical with that of pristine BP shown in Figure 2.6. The unchanged crystal structure of the BP flake after the Cu penetration indicates the Cu dopant atoms act as interstitial atoms in the BP crystal. The atom size of Cu ($r_{\mathrm{Cu}} \sim 0.14$ nm) is smaller than the interlayer distance (0.52 nm) of BP flakes and larger than “pore” size (< 0.1 nm) of BP plane, which suggests the Cu atoms are intercalated between the BP layers. We deduce that the Cu diffusion begins at the edge sites or surface defects of the BP flake and goes along the interlayer between BP planes, which results in BP with Cu_{int} between BP layers.

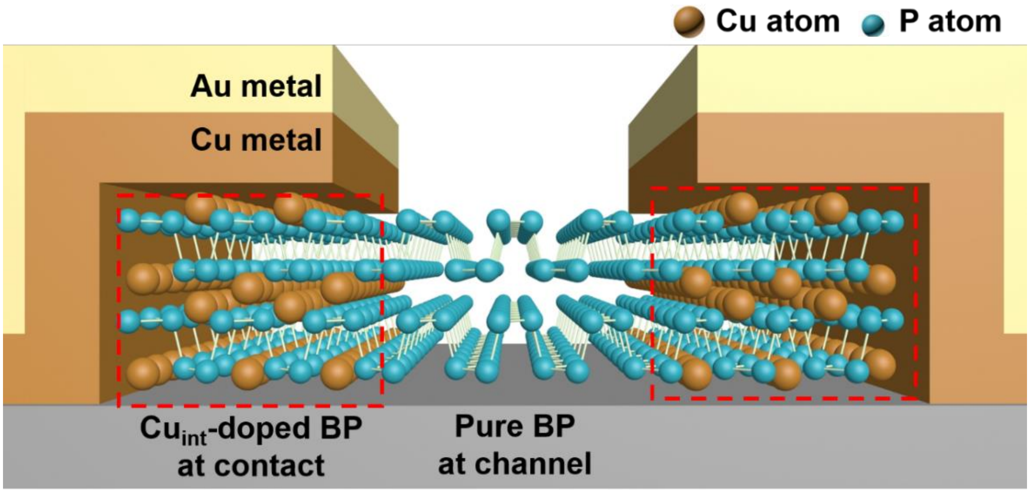

Figure 2.1 Cross-sectional schematic of Cu_{int}-doped contact of BP FETs.

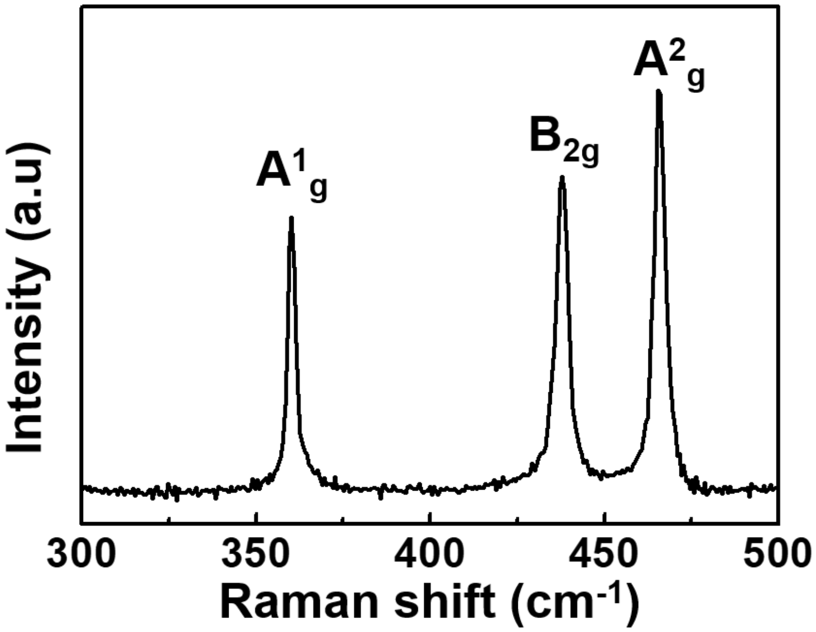

Figure 2.2 Raman spectrum of BP flakes.

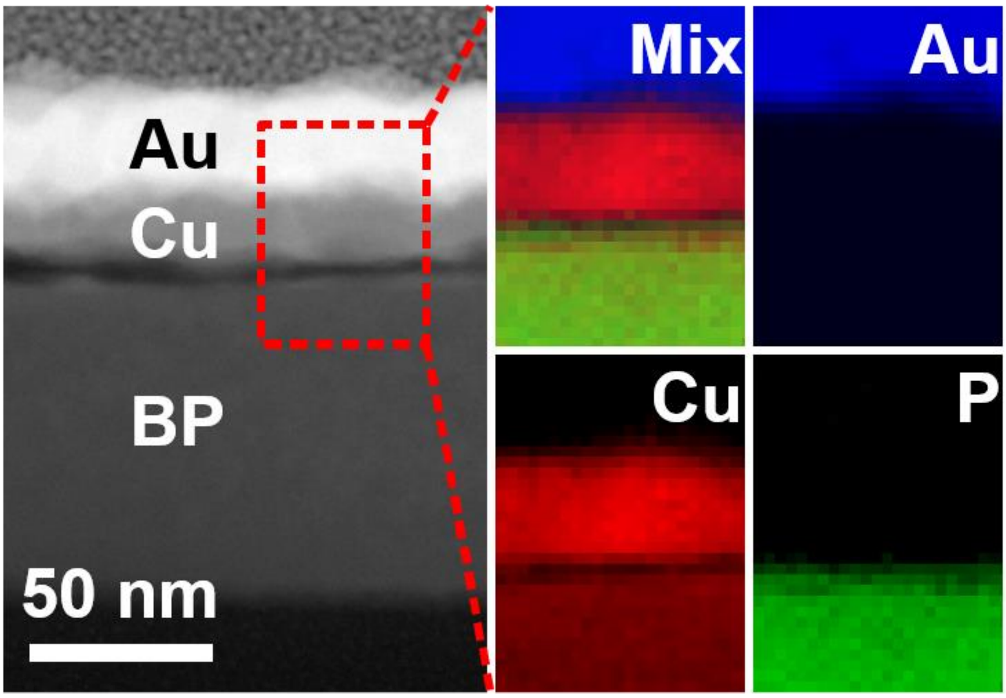

Figure 2.3 Cross-sectional STEM of Au/Cu/BP flake and corresponding elemental mapping images.

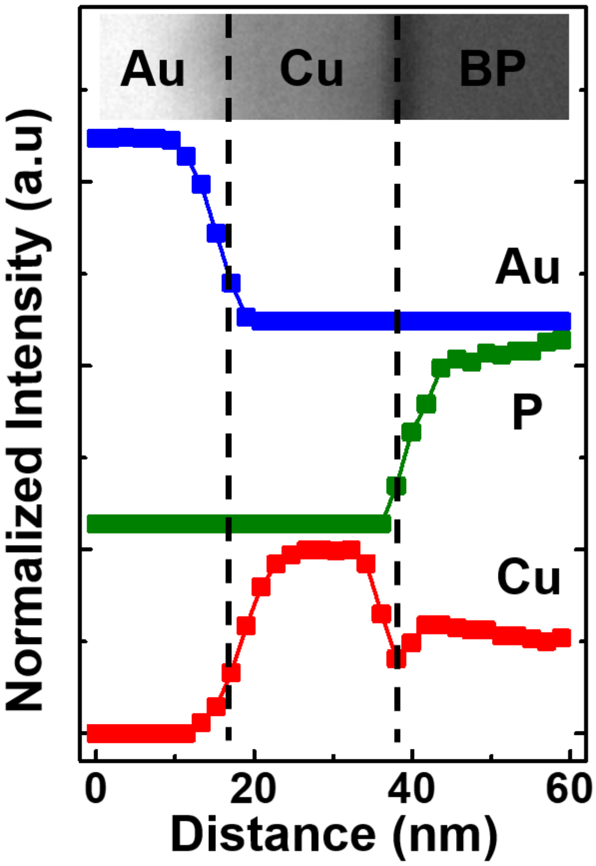

Figure 2.4 Line scan of EELS element analysis.

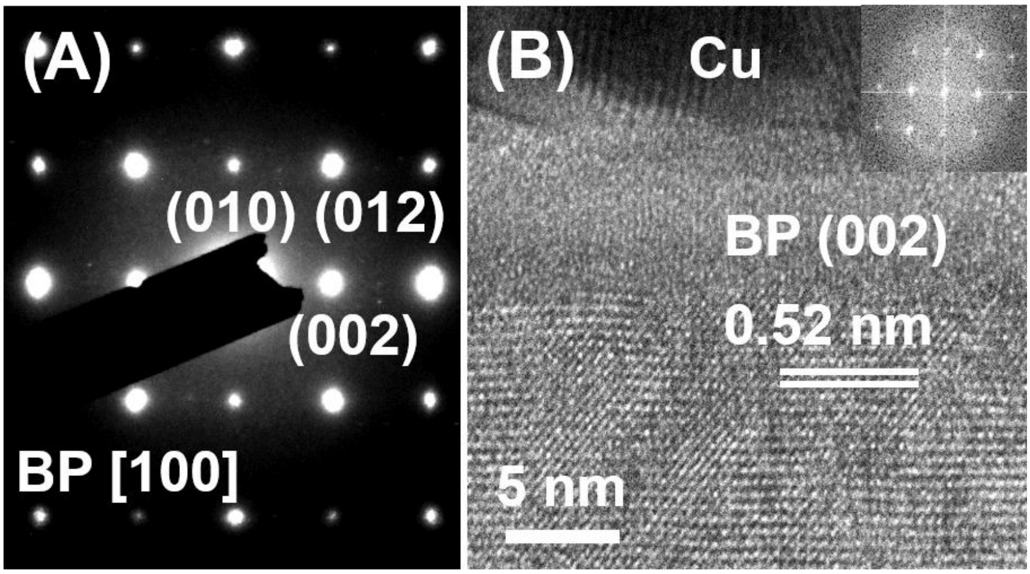

Figure 2.5 (A) SAED pattern of the Cu_{int}-doped BP flake. (B) HRTEM image of the Cu_{int}-doped BP. Inserted is the corresponding FFT pattern.

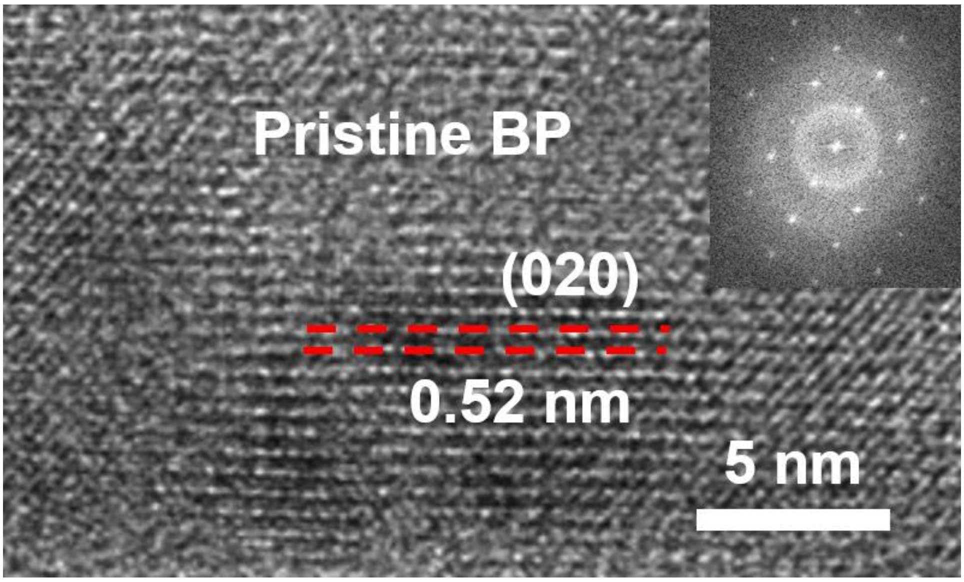

Figure 2.6 HRTEM image of pristine BP. Inserted is the FFT pattern.

Figure 2.7(A) and (B) present the XPS spectra of BP without and with Cu coating. Pristine BP shows a strong peak at 134.2 eV, corresponding to the P-O bonds, which indicates oxidization of BP. In contrast, the peak at 133.7 eV observed from BP with Cu coating can be attributed to the interaction between Cu and BP, indicating the Cu-P bonds at the surface and interlayer.[107] In each layer of BP, the lone pair electrons of phosphorus atoms interact with each other, forming conjugated π bond at the surface and interlayer. During the metal evaporation, the evaporated Cu atoms have negative formation energy with the conjugated π bond of BP, indicating the spontaneous electron interaction between Cu and BP at the surface and interlayer.

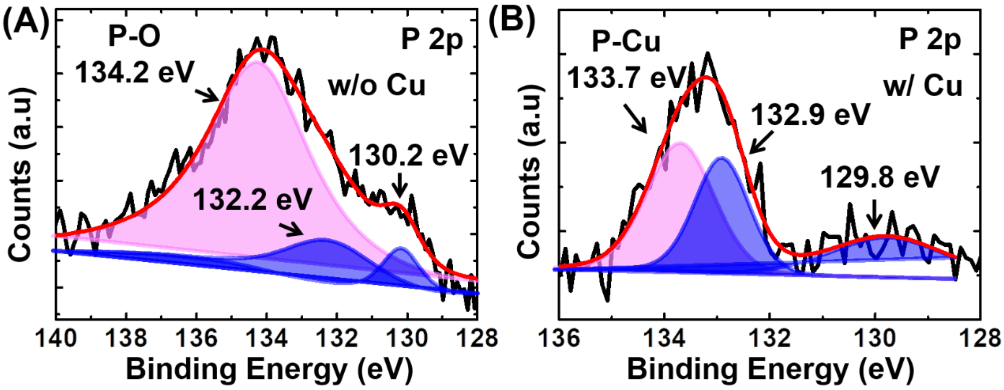

Figure 2.7 (A) and (B) XPS spectra of BP flakes without and with Cu coating.

Although the $\mathrm{Cu_{int}}$ dopant negligibly changes the crystal structure of BP flakes, it greatly affects the electrical property of few-layer BP. We studied the effect of $\mathrm{Cu_{int}}$ on the band structure of few-layer BP based on density functional theory (DFT). Figure 2.8(A) and 2.8(B) show the atomic configurations of pristine BP and $\mathrm{Cu_{int}}$-doped BP. For pristine BP, the band structure in Figure 2.8(C) clearly shows the Fermi level lies in middle of the bandgap. In contrast, Figure 2.8(D) shows that the Fermi level of BP with Cu_{int} is greatly shifted towards the conduction band, which is in agreement with *n*-doping effect of Cu adatom.[67] The Cu atom donates one electron from outmost shell, which induces the *n*-doping effect of Cu_{int}. In addition, the bandgap of BP with Cu_{int} is smaller than the pristine BP, indicating the transition from semiconductor to semi-metal of BP after Cu penetration.

As illustrated in Figure 2.1, the BP beneath the Cu contact experiences great *n*-doping effect of Cu from metal electrode. The Cu atoms at the contact region diffuse from the edge sites of BP flakes and bond with P atoms at the surface and interlayer during metal evaporation process. Theses penetrated Cu atoms act as interstitial and maintain the crystal structure of BP at contacts, which allows excellent edge contact with pure BP at channel. In addition, although the Cu_{int}-doped BP does not change its orthorhombic structure, the electrical structure is greatly changed. The bandgap of Cu_{int}-doped BP is narrowed while the Fermi level is shifted towards conduction band, which results in small barrier height for electron and promotes the electron transport in BP. The achievement of *n*-type BP FETs is attributed to the Cu_{int}-doped BP edge contact, providing another carrier type control rather than low-work-function metal contact and surface doping.

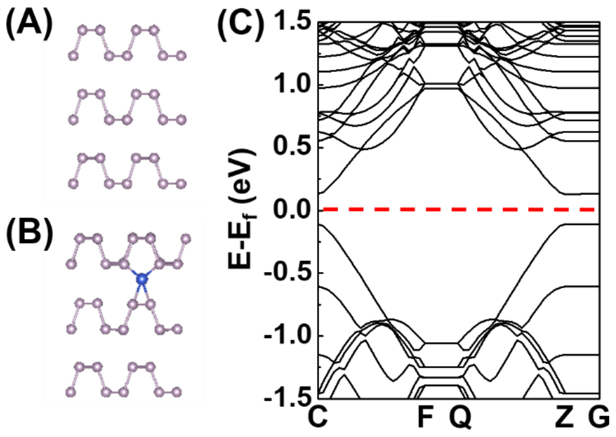

Figure 2.8 (A) and (B) Atomic configurations of pure BP and Cu_{int}-doped BP. (C) and (D) Calculated band structures of pure BP and Cu_{int}-doped BP.

2.3.2 BP FETs with Cu contact

We further studied the electrical characteristics of BP transistors with Cu contact electrodes prepared by thermal evaporation. Figure 2.9(A) presents the transfer curve of a typical BP transistor with 8-nm-thickness, which exhibits *n*-type dominant transport behavior with an on/off ratio in the order of 100 and a high electron mobility of ~138 $cm^2V^{-1}s^{-1}$ at room temperature. The current density can reach 58 µA/µm as shown in the output curve in Figure 2.9(B). For most FETs fabricated based on BP with thickness less than 10 nm in this work, the statistical analysis (Figure 2.10) indicates the on/off ratio is around 100 and the average electron mobility is ~ 70 $cm^2V^{-1}s^{-1}$. The *n*-type dominant transport property in BP FET with Cu contact reveals the

Note: box covers panels A–D.

great *n*-doping effect induced by the Cu_{int}-doped BP edge contact and the small SBH for electron. Figure 2.11 presents the thickness dependent transfer curves of BP transistors. The on/off ratio is reduced to 10 as the increase of BP thickness. As the thickness of BP increases, the *n*-branch current change slightly, suggesting the SBH for electron is small and nearly independent on BP thickness. The *p*-branch current dramatically increases by 10 times, indicating the considerable SBH for hole is reduced when bandgap is narrowed as increased BP thickness. The different change of *p*/*n*-branch current results in the transition of devices from *n*-type unipolar to *n*-type dominant ambipolar. The simplified band diagram of Cu_{int}-doped BP edge contact is presented in Figure 2.9(C). The Cu_{int}-doped BP has a Fermi level lying above the conduction band, which makes it act as metal. For $V_{gs} > V_T$ (threshold voltage), the Cu_{int}-doped BP edge contact has a small SBH for electron as the energy level match between Cu_{int}-doped BP and pristine BP. When $V_{gs} < V_T$, a large SBH for hole hinders the hole transport in BP. The Cu_{int}-doped BP edge contact achieves the *n*-type transport property of BP FET by providing small SBH for electron, which is benefited from the great *n*-doping effect of Cu_{int}.

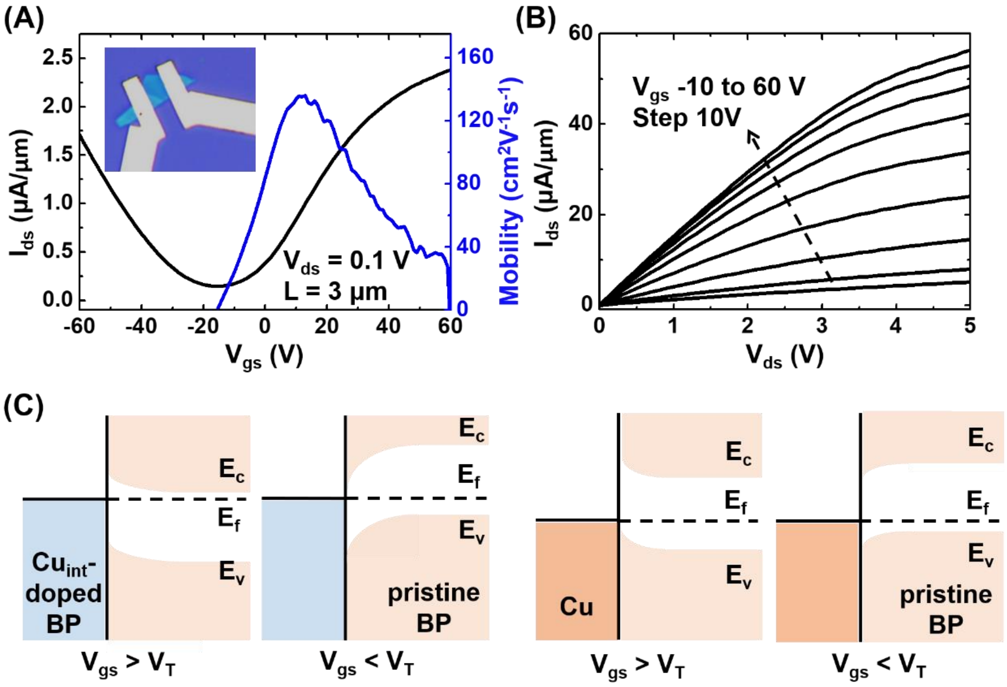

Figure 2.9 (A) Transfer curve of a typical BP FET with Cu contact exhibiting strong *n*-type transport property. The inserted is the corresponding optical image. (B) Output curve of the *n*-type BP FET. (C) Simplified band diagram of Cu_{int}-doped BP edge contact and pure Cu.

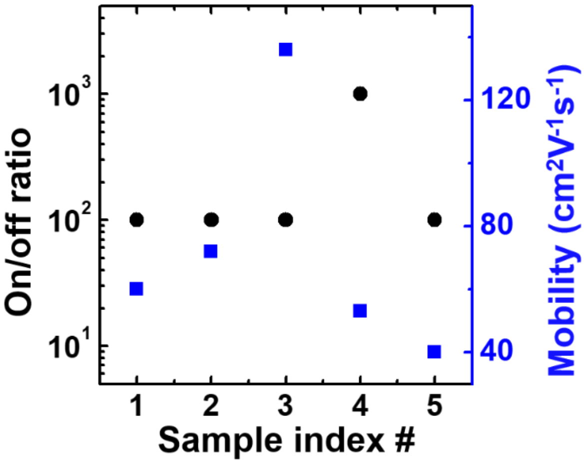

Figure 2.10 Statistical analysis of performance of BP FETs with Cu contact.

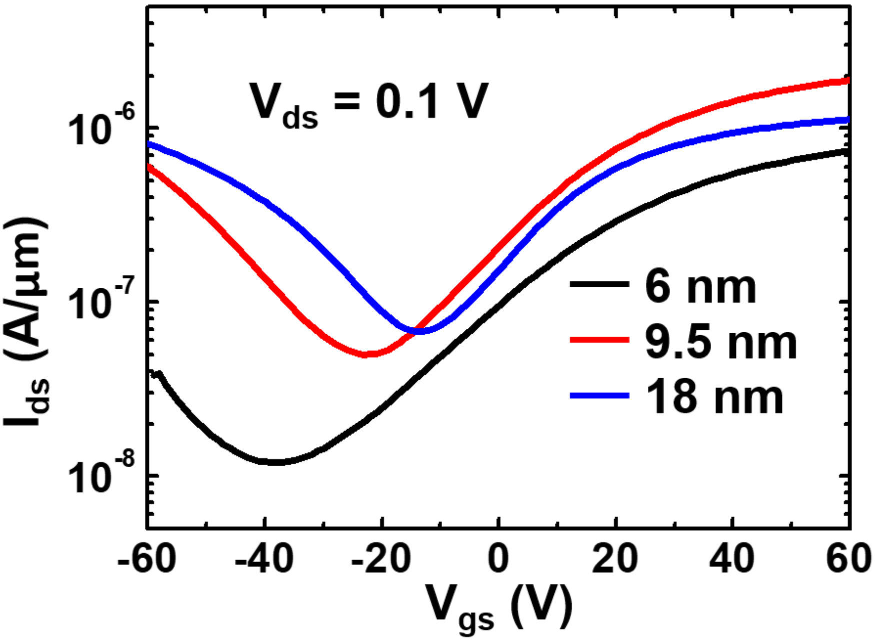

Figure 2.11 Thickness-dependent transfer curves of BP FET with Cu contact.

We also performed temperature dependent characterization of the devices to understand the barrier height at the contact region. Figure 2.12(A) shows the transfer curves of the BP transistor at various temperatures. The *n*-branch current of ambipolar BP FET exhibits negligible temperature dependence, which indicates a small Schottky barrier for electrons. In contrast, the *p*-branch current exhibits relatively large temperature dependence. With the decrease of the temperature, the *p*-branch current is decreased, revealing a larger Schottky barrier for holes.[105] Figure 2.12(B) presents the temperature dependent mobility. As the temperature decreases from 250 to 50 K, the mobility of BP is increased from 58 $cm^2V^{-1}s^{-1}$ to 89 $cm^2V^{-1}s^{-1}$, which is attributed to the reduced phonon scattering at low temperature.

In the phonon scattering region, the mobility fits the expression $\mu \sim T^{-\gamma}$ and the exponent γ was extracted to be 0.37 for the devices. The output curves at different temperatures are also shown in Figure 2.13(A) (300 K) and Figure 2.13(B) (50 K). The current density exhibits great increase from 41 μA/μm to 52 μA/μm as temperature decreases, confirming the reduced phonon scattering at low temperature.

We further tried to extract the SBH for electron of BP-Cu contact from temperature-dependent performance as reported work.[102] The Arrhenius plots in Figure 2.12(C) were obtained from the temperature-dependent transfer curves. The slope is associated with the barrier height at various back-gate voltages. According to the thermionic theory, when the back-gate voltage is below flat-band voltage (V_{FB}), the thermionic emission current dominates the drain current. The barrier height shows a linear relationship as a function of the gate voltage. When the back-gate voltage is larger than V_{FB}, thermally assisted tunneling current contributes to the drain current, which results in the nonlinear behavior between barrier height and gate voltage. At the turning point (the back-gate voltage equals to V_{FB}), the relationship between barrier height and the back-gate voltage changes from linear to nonlinear. SBH can be extracted when the back-gate voltage equals to V_{FB}, because thermally assisted tunneling does not contribute to the current. As shown in Figure 2.12(D), the barrier height maintains linear relationship as a function of the gate voltage without turning point, where the curve changes to nonlinear. The linear relationship without turning point suggests the negligible SBH, which is attributed to Cu_{int}-doped BP edge contact.

As presented in Figure 2.1, during the Cu/Au metal evaporation, the Cu metal will penetrate into BP through edge. The penetration results in the formation Cu_{int}-doped BP edge contact without changing the crystal structure, which suggests the well contact between Cu_{int}-doped BP at the contact and pure BP at the channel as they share same crystal structure. In addition, the Cu_{int} narrows the bandgap of BP, making the Cu_{int}-doped BP edge contact act as semi-metal. The Cu_{int} also donates electron and greatly shifts the Fermi level of BP into conduction band, causing the *n*-doping effect of BP. The Cu_{int}-doped BP electrode - pristine BP channel forms excellent contact due to the unique properties of Cu_{int}-doped BP edge contact including same crystal structure as pure BP and smaller bandgap, which induces the negligible SBH for electron.

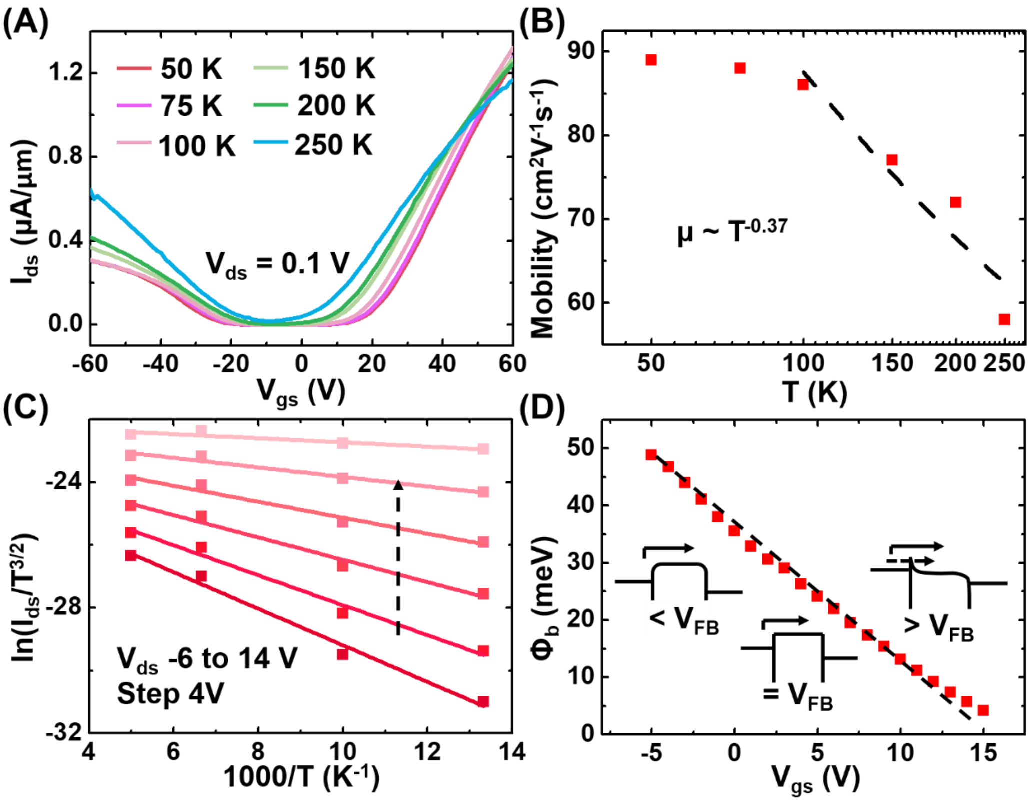

Figure 2.12 (A) Temperature dependent transfer curves. (B) Temperature dependent mobility of BP FET. (C) The Arrhenius plots for different back-gate voltages. (D) The extracted Schottky barrier heights for different back-gate voltages.

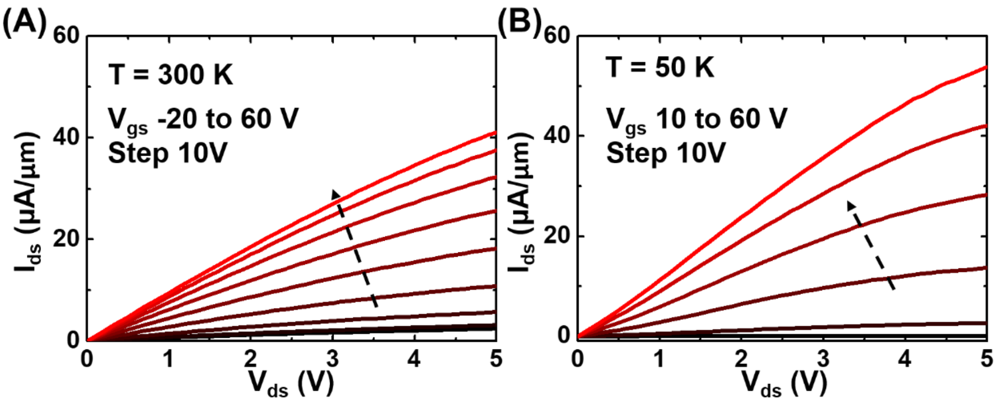

Figure 2.13 (A) and (B) Output curves of BP FET with Cu contact at 300 K and 50 K, respectively.

In addition to providing small SBH for electron in BP, the Cu_{int}-doped BP also forms Ohmic contact with metal electrodes. Figure 2.14(A) shows the I-V curve of Cu/BP/Au vertical junction. The current exhibits linear relationship as a function of the applied voltage with the current density of 158 $\mu A/\mu m^2$, about 100 times larger than that of Au/BP/Au vertical junction (1.70 $\mu A/\mu m^2$). The linear I-V curve of Cu/BP/Au indicates the metallic characteristics of the junction, while the nonlinear IV relationship of Au/BP/Au suggests non-Ohmic contact. The linear relationship and high current density of Cu/BP/Au is resulted from the Cu_{int}-doping during metal evaporation process. The penetrated Cu in BP changes the electrical property of BP to metallic-like behavior, which is consistent with our DFT calculation. The Ohmic contact between Cu_{int}-doped BP and metal electrodes benefits *n*-type BP FET with low contact resistance.

Transfer length method (TLM) is usually utilized to measure the contact resistance. Figure 2.14(B) presents the transfer curves of BP FETs with different channel lengths, showing similar off-state voltage for different channel lengths. The inserted image shows the 10-nm-thick BP device for TLM measurement. The total resistance can be calculated from the transfer curves with different channel lengths and gate voltages. Figure 2.14(C) shows the relationship between the total resistance and channel length at different gate voltages. The contact resistance can be extracted from the intercept of relationship between total resistance and channel length. The extracted contact resistance is about 5 kΩ•μm at a gate voltage of 60 V, which is comparable with that of *p*-type FET based on BP (7.5 kΩ•μm) and that of *n*-type FETs based on other 2D materials (like MoS_2, 1 kΩ•μm).[114, 115] After the contact resistance is excluded, we re-plot the transfer curve in Figure 2.14(D). The current is increased and the effective electron mobility calculated from the new transfer curve is 148 $cm^2V^{-1}s^{-1}$, higher than the previous value (72 $cm^2V^{-1}s^{-1}$) without excluding contact resistance. The relatively low contact resistance of Cu-BP contact benefits from the Cu_{int}-doped BP edge contact. The Cu_{int} greatly shifts the Fermi level and narrows the bandgap of BP, which produces negligibly low barrier high at the contact. The Cu_{int}-doped BP also have same crystal structure with the pure BP at the channel, forming edge contact with the channel. The Cu_{int}-doped BP edge contact results in the relatively low contact resistance of BP FET with Cu contact.

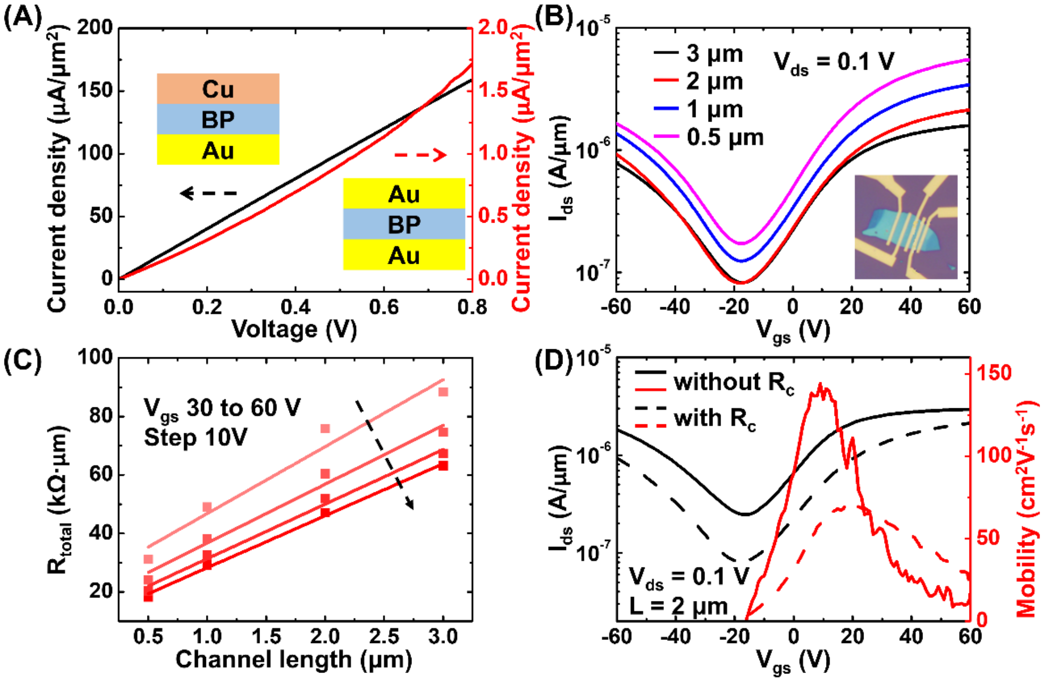

Figure 2.14 (A) Current density of vertical junction Cu/BP/Au and Au/BP/Au. (B) Transfer curves of BP FET with different channel lengths. (C) Total resistance versus channel length at different gate voltages. (D) Transfer curve and mobility with and without contact resistance.

2.3.3 *p*-*n* diode by asymmetric contact engineering

We compared with the performance of BP transistors with chromium (Cr) contact. As the band alignment in Figure 2.15(A) shows, the Cr metal has a work function of 4.6 eV, close to that of Cu metal (4.65 eV). The transfer curve in Figure 2.15(B) indicates the strongly unipolar *p*-type characteristics of BP transistors with Cr contact, which is consistent with the band alignment of Cr-BP. The *p*-type BP FET with Cr contact exhibits an on/off ratio of 10^3 and a high hole mobility of 180 $cm^2V^{-1}s^{-1}$. In comparison, the BP FET with Cu contact exhibits *n*-type transport property with same channel length. As compared in Figure 2.15(B), the BP transistors with Cr and Cu contact metals exhibit different types of carrier transport in spite of their similar work functions, suggesting different carrier type control mechanisms. The *p*-type BP FET with Cr contact is attributed to the band alignment of Cr-BP and Fermi level pinning effect. On the other hand, the work function of Cu is about 4.65 eV and much higher than that of Al (4.0 eV) and Sc (3.5 eV) utilized as metal contact for reported *n*-type BP FETs. The work function value of Cu cannot match well with the conduction band edge for few-layer BP flakes (4.1 eV), but is close to the value of Cr. The *n*-type characteristics of BP FETs with Cu contact is likely to be associated with the *n*-doping due to the highly-mobile Cu metal instead of the band alignment of Cu-BP. As illustrated in Figure 2.1, the interlayers of BP are occupied with interstitial Cu atoms, which causes great *n*-doping effect. The contact doping promotes electron transport due to the excellent edge contact between the highly *n*-doped BP with Cu_{int} and pristine BP, which gives rise to small SBH for electron.

Based on contact engineering, we further constructed a *p*-*n* junction with asymmetric contact (Au and Cu electrodes on two sides) on the same BP flake. The BP transistors with Au electrodes have *p*-type characteristics,[116] which allows to form *p*-*n* junction with Cu electrodes. Figure 2.15(C) shows the optical image of the *p*-*n* junction based on BP with Au and Cu contacts. The Cu electrode as source was patterned by electron-beam lithography while the Au electrode as drain was transferred and aligned on the BP flake.[117] Figure 2.15(D) presents the output curve of the *p*-*n* junction. The device shows rectification behavior, with a rectification ratio of about 100.

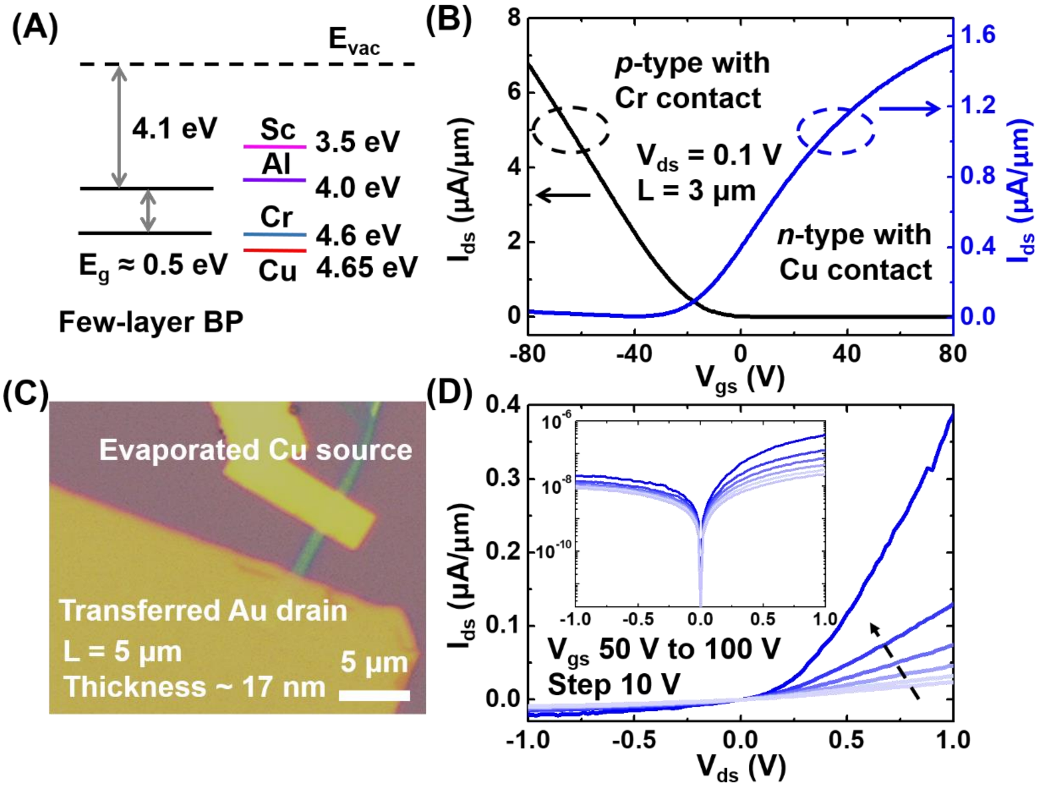

Figure 2.15 (A) Band alignment between few-layer BP and different metals. (B) Transfer curves of BP FET with evaporated Cr contact and Cu contact. (C) Optical image of BP *p*-*n* junction with asymmetric contact. (D) Output curve of BP *p*-*n*

junction. Inserted is output curve in semilogarithmic scale.

2.4 Summary

In this chapter, *n*-type dominant BP transistors with Cu contact are demonstrated. The interface between Cu and BP is contributed to the *n*-type transport property of BP FET. The contact metal Cu experiences penetration to BP flakes during metal evaporation, resulting in BP with interstitial Cu at the contact region. The Cu_{int} *n*-dopes the BP and narrow the bandgap of BP without changing the crystal structure of BP, which benefits the excellent Cu_{int}-doped BP edge contact with channel pure BP. The BP transistors with Cu contact exhibit *n*-type dominant transport characteristics although the Cu has a relatively large work function. The devices exhibit high electron mobility of ~ 138 $cm^2V^{-1}s^{-1}$ (average 70 $cm^2V^{-1}s^{-1}$) and on/off ratio of ~ 100 with a negligibly low SBH for electron. Although this work focuses on the Cu contact on BP, due to the highly-mobile Cu atoms, other new emerging 2D material, like tellurene, may have similar respond to Cu contact and exhibit different transport property rather than judging from band alignment.

Although few-layer BP possesses excellent electronic properties, the high-efficiency and large-area preparation of BP with controllable thickness remains a challenge. In addition, the poor air-stability further hampers the device applications of few-layer BP. Considering this, an alternative *p*-type 2D semiconductor is desired.

Chapter 3 High-Performance Tellurium Field-Effect Transistors with High-Work-Function Metal Contacts

3.1 Introduction

As the continuous scaling of convention silicon (Si) transistors, the short-channel effect become severe, which leads to increase of leakage current and degradation of device performance.[36-39] Two-dimensional (2D) semiconductors are reported promising candidates replacing convention Si channel due to the ultrathin thickness and dangling-bond-free surface of 2D materials.[40, 82, 118] The layered nature of 2D materials allows precise and consistent thickness control on 2D channels down to single-layer limit, which provides enhanced electrostatic control of the gate and further scaling of transistors. It has been reported that the short channel effect will not limit the scaling of transistors with 2D MoS_2 channels down to one-nanometer gate length, which is superior to the sub-five-nanometer scaling limit of Si transistors.[39] The application of 2D semiconductors can greatly alleviate the severe short channel effect in continuously downward scaling of transistors. Therefore, intensive research attentions are attracted on the 2D materials with high carrier mobility and an appropriate band gap for future nanoelectronics.

Recently, the semiconducting tellurium (Te) is rediscovered since it possesses outstanding physical properties including higher carrier mobility than transition metal dichalcogenides (TMDs) and much better air stability than black phosphorus (BP), which shows the great potential of 2D Te in future electronics.[82, 118] There are a few theoretical studies and experimental works presenting the electrical properties and some appealing applications (*e.g.* FETs, optoelectronic devices and thermoelectric devices) of 2D Te.[16, 42, 95] The prediction indicates the thickness-dependent bandgap of few-layer Te, which changes from nearly direct bandgap of 0.31 eV in bulk to indirect bandgap of ~ 0.9 eV in bilayer.[42] The extraordinarily high hole mobility in 2D Te is also expected 10^4-10^6 $cm^2V^{-1}s^{-1}$, appreciably larger than that of 2D TMDs and BP.[9, 41] Wang *et al.* demonstrated the very first FETs based on 2D Te, which exhibits *p*-type transport property with on/off ratio of 10^5 and a maximum hole mobility of 700 $cm^2V^{-1}s^{-1}$.[16] Zhao *et al.* also achieved integrated circuits with Te thin films prepared by vapor deposition.[95] The realization of full-adder, multiplier circuits and 3D invertors suggest the great potential of 2D Te applications in nanoelectronics.

As one of the newest members of 2D materials, 2D Te only received a few research interests. The carrier dynamic and transport property have not yet received thorough understanding compared to other popular 2D materials. Metal contact is one of critical factors influencing the carrier transport in 2D material.[61] It is predicted that metals including Cu, Ni, Ag, Pt and Pd can form lateral *p*-type Schottky contact with 2D Te due to Fermi level pinning.[119] The limited research studies on contact engineering of 2D Te require further investigation to develop transport understanding and enhance device performances.

In this chapter, we will demonstrate the *p*-type Te FETs with Pt and Pd contacts and study the carrier transport in 2D Te. The metals Pt and Pd are chosen as contact metals for their high work function (5.65 eV and 5.12 eV, respectively), which are lying far below the valance band maximum (VBM) of few-layer Te (4.35 eV). The well-match band alignment between metals and Te suggests small Schottky barrier height (SBH) for hole, which facilitates the hole transport and current injection. The Te FETs with Pt contact exhibit excellent *p*-type transport property with on/off ratio larger than 10^4 and field-effect hole mobility reaching 420 $cm^2V^{-1}s^{-1}$. The contact resistance is 400 Ω•μm, which is attributed to small SBH for hole and high density of states

(DoS) for Te beneath the contact. The excellent contact and outstanding performance of Te devices are realized by contact engineering, which is important for future application of 2D Te in nanoelectronics.

3.2 Methods

3.2.1 Device fabrication

Back-gated FETs with Pt/Pd contact were first fabricated with few-layer Te flakes on 300 nm SiO_2 dielectric on highly doped Si substrates. The substrates with Te flakes were coated with poly(methyl methacrylate) resist (PMMA) for lithography. The source and drain electrodes were patterned by electron beam lithography. Afterwards, 15 nm Pt/Pd and 30 nm Au were deposited as contact metals, using an electron beam evaporator. The devices were fabricated after lift-off process.

3.2.2 Characterization and electrical measurement

The Raman measurement was conducted using a Horiba Jobin Yvon LabRAM HR System with a laser wavelength of 488 nm. The laser spot size is ~1 μm. The AFM images were taken by Bruker NanoScope. The electrical measurements on the devices were conducted in a Lakeshore low temperature IV probe station.

3.3 Results and discussion

3.3.1 Basic characterizations

Few-layer Te for channel was prepared by solution synthesis.[16] The Raman spectra of few-layer Te in Figure 3.1(A) presents three Raman-active modes located at 90 cm^{-1}(E_1 mode), 119 cm^{-1}(A_1 mode) and 138 cm^{-1} (E_2 mode), indicating the nature of Te flake, as shown in the inserted image of Figure 3.1(A). Figure 3.1(B) shows the atomic force microscopy (AFM) image of a typical Te sample used for device fabrication, which has a thickness of ~15 nm. The AFM characterization confirms that few-layer Te flakes for device fabrication all have a thickness ranging from 10 nm to 30 nm to minimize the effect of interface scattering on mobility reduction. Figure 3.1(C) displays the schematic of back-gated field-effect transistors (FETs) structure with Te channel. Platinum (Pt) and palladium (Pd) were chosen as contact metals due to their high work functions. Figure 3.1(D) presents the band diagram between few-layer Te and metal contacts. Few-layer Te is predicted to possess a VBM of about 4.35 eV.[42] The work functions of Pt (5.65 eV) and Pd (5.12 eV) are lying far below the VBM of few-layer Te, suggesting small SBH for hole and facilitating the hole transport in Te.

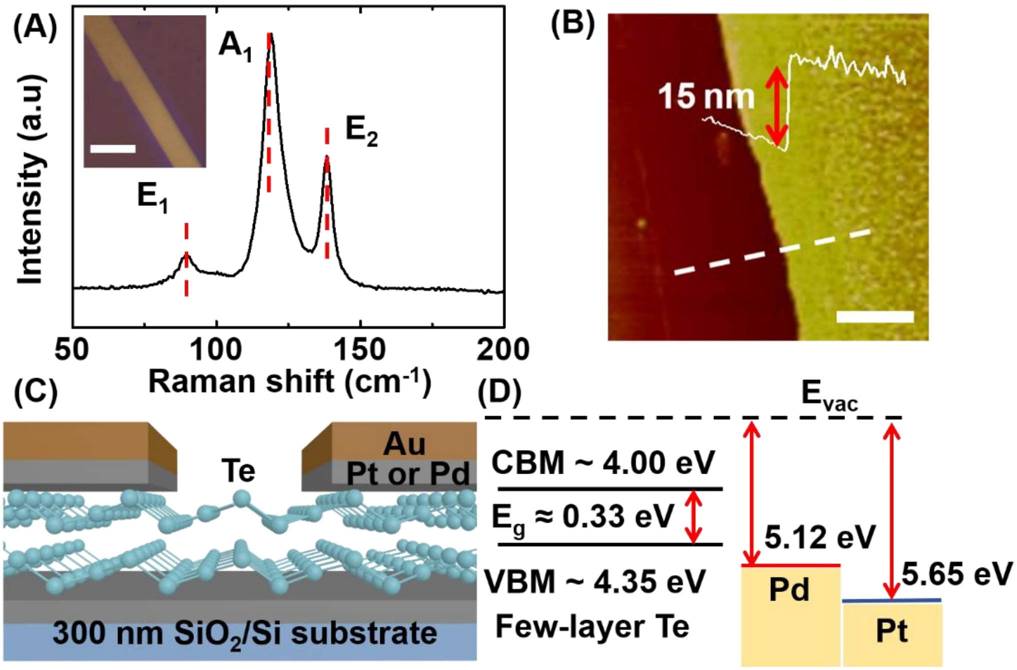

Figure 3.1 (A) Raman spectra of a Te flake on SiO_2 substrate. The inserted is the corresponding optical image. The scale bar is 10 μm. (B) AFM image of a typical Te sample for device fabrication. The scale bar is 2 μm. (C) Schematic of back-gated FETs structure with channel Te. (D) Band diagram between few-layer Te and metal contacts including Pt and Pd.

3.3.2 Electrical characterizations on Te FETs

We first studied the basic electrical characteristics of Te FETs with Pt contact. Figure 3.2(A) presents the transfer curve of a typical Te FET with 0.6 μm channel length. The device exhibits unipolar *p*-type transport property with on/off ratio larger than 10^4 and hole mobility reaching 420 $cm^2V^{-1}s^{-1}$. The output curves in Figure 3.2(B) shows the large current density as high as 0.17 mA/μm. The relationship among the drain current (I_{ds}), gate voltage (V_{gs}) and drain voltage (V_{ds}) of Te FETs can be described by the conventional model for metal oxide semiconductor field effect transistors (MOSFETs) using a formula as below:[120]

$$I_{ds}=\frac{\mu_{eff}WC_{ox}}{L}\left[\left(V_{gs}-V_{th}\right)V_{ds}-\frac{V_{ds}^{2}}{2}\right]\text{.................}(1)$$

where μ_{eff} is the field-effect mobility, W and L are the channel width and length, C_{ox} is the capacitance of gate insulator, and V_{th} is the threshold voltage, respectively. This equation is valid only for linear regime when $|V_{ds}| < |V_{gs}-V_{th}|$. The field-effect mobility of FETs can be calculated when V_{ds} is constant:

$$\mu_{eff}=\frac{L}{WC_{ox}V_{ds}}\frac{dI_{ds}}{dV_{gs}}=\frac{Lg_m}{WC_{ox}V_{ds}}\text{.................}(2)$$

The carrier concentration n_h can be further calculated with field-effect mobility:

$$n_h=\frac{1}{e\rho\mu_{eff}}\text{.................}(3)$$

where e is elementary charge and ρ is the resistivity of Te channel. The hole concentration of Te at $V_g = 0V$ is estimated to be 2.6×10^{18} cm^{-3}, which is comparable with reported values of MoS_2 and BP.[121, 122]

Considering the two-terminal configuration of source and drain electrodes which is widely adopted in FETs based on 2D materials, the drain current and field-effect mobility are often underestimated compared with the intrinsic property of channel materials due to the contact resistance between electrode metal and 2D materials. To extract the intrinsic mobility μ_0, Y-function method is proposed.[120] In this method, equation (1) is modified as:

$$I_{ds}=\frac{WC_{ox}}{L}\frac{\mu_0}{[1+\eta(V_{gs}\text{-}V_{th})]}(V_{gs}\text{-}V_{th})V_{ds}\ldots\ldots\ldots\ldots\ldots\ldots(4)$$

where η is the mobility reduction coefficient. The coefficient is related with contact resistance (R_C) and phonon scattering:

$$\eta=\frac{W}{L}\mu_0C_{ox}R_C+\eta_0\ldots\ldots\ldots\ldots\ldots\ldots(5)$$

where η_0 reflects the mobility reduction induced by interface scattering which can be ignored compared with the effect of contact resistance. Therefore, the transconductance g_m is expressed as below:

$$g_m=\frac{dI_{ds}}{dV_{gs}}=\frac{WC_{ox}}{L}\frac{\mu_0}{[1+\eta(V_{gs}\text{-}V_{th})]^2}V_{ds}\ldots\ldots\ldots\ldots\ldots\ldots(6)$$

The Y-function is mathematically created by combining equation (4) and (5) to eliminate the η:

$$Y=\frac{I_{ds}}{\sqrt{g_m}}=\sqrt{\frac{WC_{ox}}{L}\mu_0 V_{ds}(V_{gs}\text{-}V_{th})}\text{..................}(7)$$

The intrinsic mobility μ_0 can be attained from the slope of the Y-V_{gs} curve:

$$\mu_0=\frac{L(\text{slope})^2}{WC_{ox}V_{ds}}\text{..................}(8)$$

Figure 3.2(C) shows the relationship between Y function and V_{gs}. The intrinsic mobility μ_0 is extracted to be 504 $cm^2V^{-1}s^{-1}$, higher than the field-effect mobility μ_{eff} calculated from the transfer curve. Although the larger value of intrinsic mobility μ_0 indicates the existence of contact resistance, the small increment suggests the unremarkable influence of contact resistance on transport property of Te FETs resulting from the small contact resistance.

Afterwards, we measured the contact resistance of Te FETs with Pt contacts by utilizing transfer length method (TLM). Figure 3.2(D) presents the transfer curves of the devices with different channel lengths, exhibiting similar transport property. The FET with 23-nm-thick Te for TLM measurement is shown in the inserted image. The total resistance can be calculated from the transfer curves. The total resistance R_{total} between two contacts is a linear combination of the contact resistance R_c and the length-dependent channel resistance

$R_{ch}(L)$, which can be expressed as below:

$$R_{total}=2R_c+R_{ch}(L)\ldots\ldots\ldots\ldots\ldots\ldots(9)$$

Figure 3.2(E) shows the total resistance as a function of channel length at different gate voltages. Corresponding to equation (8), the contact resistance can be extracted from the intercept of relationship between total resistance and channel length. The extracted contact resistance is as low as 400 Ω•μm at -80 V gate voltage. This value is much lower than those of FETs based on other 2D materials.[114, 115] Figure 3.3 presents the contact resistance dependent on gate voltage, which is increased from 400 Ω•μm at V_{gs} = -80 V to 1.8 kΩ•μm at V_{gs} = 0 V. The negative gate voltage can increase the hole concentration and lower the sheet resistance of Te beneath the metal contacts, resulting in lower contact resistance. After excluding the contact resistance, we re-plot the transfer curves in Figure 3.2(F). The drain current increases as expected. The effective hole mobility extracted from the re-plotted transfer curve is 148 $cm^2V^{-1}s^{-1}$, higher than the field-effect mobility of 106 $cm^2V^{-1}s^{-1}$. The increase of hole mobility suggests the influence of contact resistance on carrier transport. The small contact resistance suggests the excellent contact between metal Pt and Te. Figure 3.4 compares the contact resistance of FETs with Pt contact based on Te with different channel thicknesses. The contact resistance gradually declines in devices based on thicker Te. Due to the Fermi level pinning effect, the Fermi level of Pt/Te interface is pinned close to the valance band of 2D Te. Theoretical calculation has shown that the VBM of 2D Te changes from 4.35 to 4.98 eV with the thickness reduction.[42] The change of VBM in thinner Te results in larger barrier height for hole at Pt/Te interface, which brings higher contact resistance. In addition, the increasing carrier density in thicker Te also facilitates the current injection by lowering the ρc and sheet resistance beneath the metal. The low carrier density in thin Te contributes to larger contact resistance of Te FETs.

The Te FETs with Pt contact exhibit particularly high performance including high on/off ratio of 10^4, large drain current density of 0.17 mA/μm, high field-effect/intrinsic hole mobility of 420/504 $cm^2V^{-1}s^{-1}$, large hole concentration of 2.6×10^{18} cm^{-3} and small contact resistance of 400 Ω•μm. Except the excellent intrinsic electrical property of Te channel, the Pt contact are also important for high-performance devices. The high work function of Pt metal lying far below the VBM of 2D Te ensures small Schottky barrier between Pt and Te, which faciliates hole transport and current injection and results in small contact resistance. In TLM model, the extracted contact resistance consists of three parts: the sheet resistance of metal, the specific contact resistivity and the sheet resistance of semiconductor beneath the metal.[123] In Te FET with Pt contact, the sheet resistance of metal can be ignored compared to the other two parts. The large hole concentration and high hole mobility of 2D Te can bring small sheet resistance under the contacts. The specific contact resistivity is associated with current injection from metal to semiconduction, which is affected by Schottky barrier at the interface. The small contact resistance suggests small SBH between Pt and Te. The high-work-function Pt metal forms excellent contact with 2D Te channel, leading to high-performance devices.

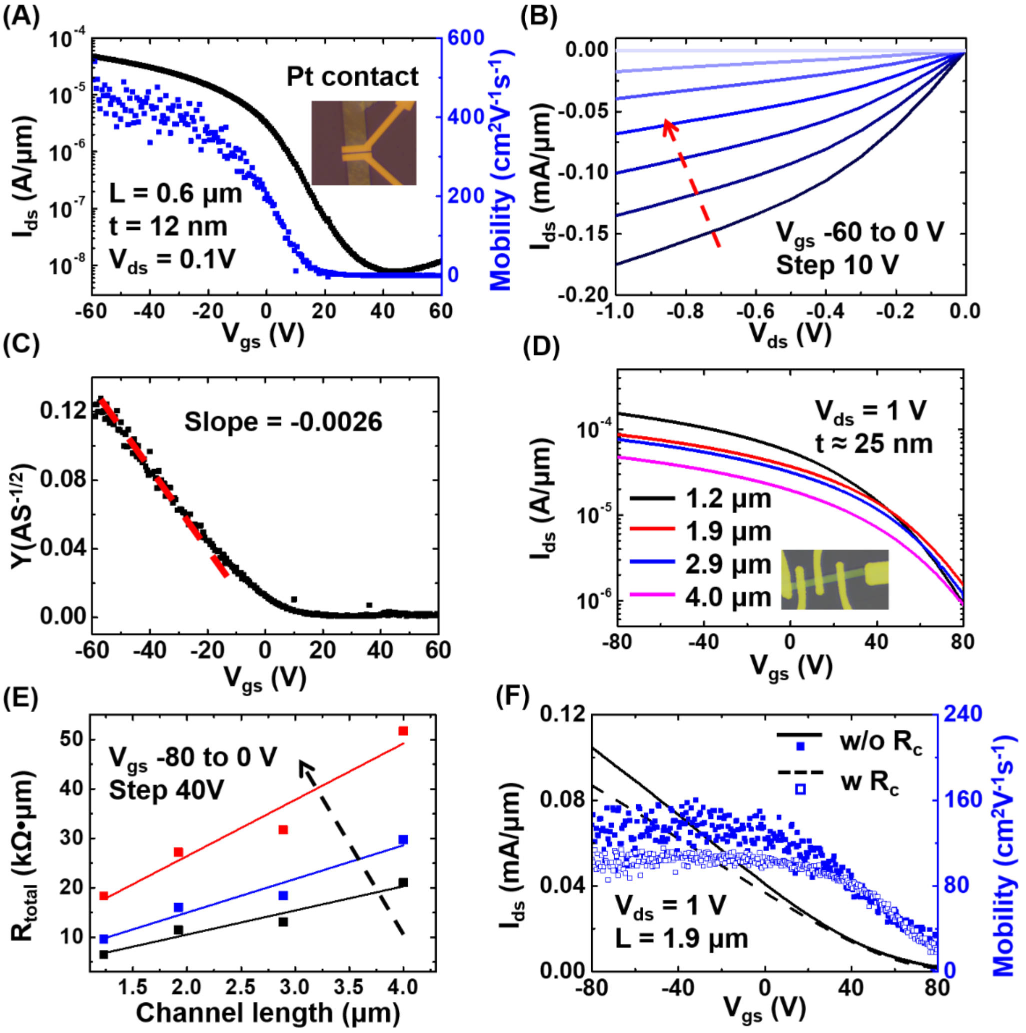

Figure 3.2 (A) Transfer curves and (B) output curves of a typical FET based on 2D Te with Pt contact. The inserted is optical image of the device. The thickness of Te channel is 12 nm. (C) Y-function derived from transfer curve for extraction of intrinsic mobility. (D) Transfer curves of Te FETs with different channel lengths. The inserted is optical image of the devices for TLM measurement. The thickness of Te channel is 25 nm. (E) Total resistance versus channel length at different gate voltages. (F) Transfer curve and hole mobility with and without contact resistance.

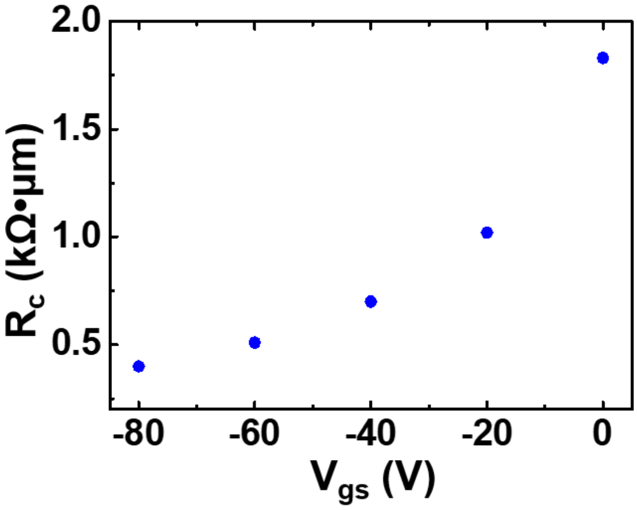

Figure 3.3 The contact resistance dependent on gate voltage.

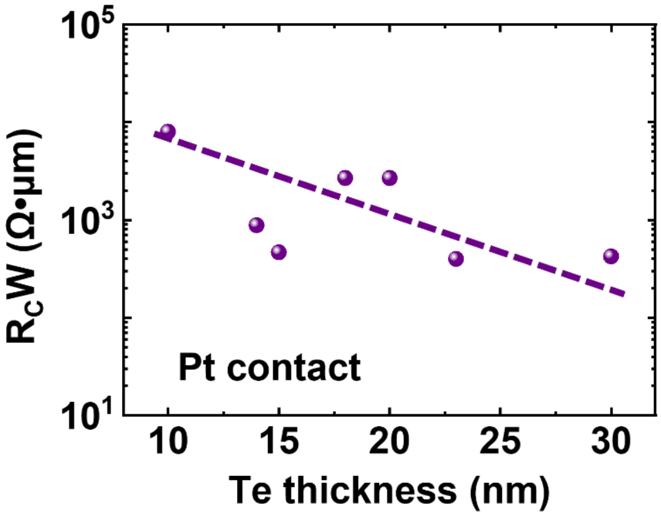

Figure 3.4 The contact resistance of Te FETs with Pt contact based on Te channels with different thicknesses.

The metal Pd has similar high work function with Pt, which indicates the well-match band diagram between Pd and Te. Figure 3.5 (A) presents the transfer curve of the Te FET with Pd contact. The device with 9.7-μm channel length has unipolar *p*-type transport property with on/off ratio larger than 10^4 and field-effect hole mobility reaching 601 $cm^2V^{-1}s^{-1}$. With Y-function method, the intrinsic hole mobility is extracted to be 625 $cm^2V^{-1}s^{-1}$. The output curve in Figure 3.5(B) also shows large current density of 0.13 mA/μm at V_{ds} = 3V. TLM method is also utilized for contact resistance of Te FET with Pd contact. Figure 3.5(C) displays transfer curves of FETs with different channel lengths. The relationship between the total resistance and channel length is illustrated in Figure 3.5(D). The contact resistance is estimated to be 880 Ω•μm, which is comparable with the value of FETs with Pt contact. The comparable performance of Te FETs with Pd contact indicates the excellent contact formed between 2D Te and metal Pd, similar with metal Pt. The metals Pt and Pd both have great contact with 2D Te and benefit hole transport and current injection in Te, suggesting the high work function of these metals contributes to high-performance *p*-type devices based on Te.

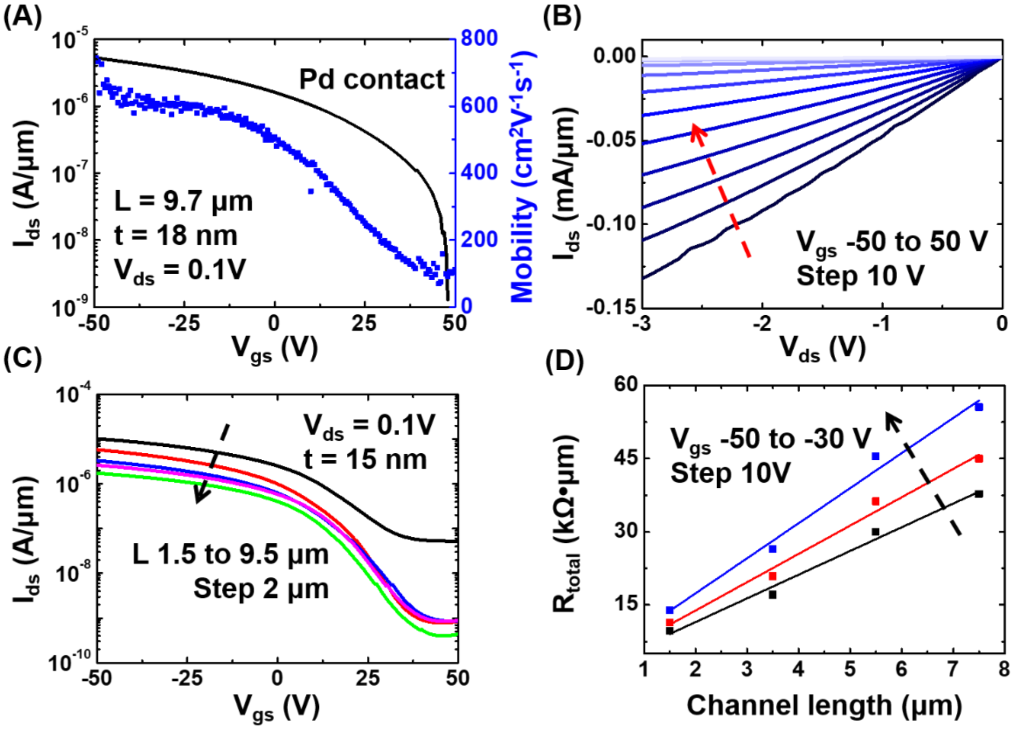

Figure 3.5 (A) Transfer curves and (B) output curves of a typical FET based on 2D Te with Pd contact. The thickness of Te channel is 18 nm. (C) Transfer curves of Te FETs with different channel lengths. The thickness of Te channel is 15 nm. (E) Total resistance versus channel length at different gate voltages of Te FETs with Pd contact.

3.3.3 Temperature-dependent properties of Te FETs

The electrical measurement is conducted at different temperatures on the Te devices with Pt contact to comprehend the temperature-dependent transport property of 2D Te. Figure 3.6(A) shows the transfer curves of the FET based on the 20-nm-thick Te flake at various temperature. As the temperature decreases, the on/off ratio of the device increases from 10^3 to 10^8. The on-state or *p*-branch current of Te FET exhibits negligible temperature dependence, which suggests a small Schottky barrier for hole. In the meantime, the off-state current is gradually reduced as the temperature decreases, which results in larger on/off ratio at low temperature. Figure 3.6(B) summarizes the mobility of the device at different temperatures. As presented, the field-effect hole mobility of Te is increased from ~290 $cm^2V^{-1}s^{-1}$ to ~680 $cm^2V^{-1}s^{-1}$ as the temperature decreases from 300 K to 150 K, which is attributed to the reduced phonon scattering at low temperature. The field-effect mobility experiences abrupt decrease to ~540 $cm^2V^{-1}s^{-1}$ at 100 K, which results from increased contact resistance at low temperature. Considering the two-terminal configuration adopted in devices for temperature-dependent measurement, the field-effect mobility is underestimated due to the contact resistance. As temperature decreases, phonon scattering is reduced at low temperature, resulting in higher hole mobility. However, the contact resistance is also grown at low temperature and has more considerable influence on underestimation on extraction of field-effect mobility. To exclude the effect of contact resistance, the Y-function method is applied for intrinsic hole mobility. The temperature-dependent intrinsic hole mobility exhibits progressive increase from 390 cm^2V^-

$^{1}s^{-1}$ to 750 $cm^2V^{-1}s^{-1}$ as temperature reduced, confirming the influence of reduced phonon scattering during temperature reduction. Figure 3.6(C) and 3.6(D) show the output curves of the FET at 100 K and 300 K, respectively. The current density is increased from 0.15 mA/μm at room temperature to 0.25 mA/μm at 100 K, which is also attributed to the reduced phonon scattering at low temperature.

According to the thermionic theory, the temperature-dependent drain current can be expressed as:[102]

$$I_{ds}=A_{2d}^{*}T^{\frac{3}{2}}\exp\left(\frac{e\phi_B}{k_BT}\right)[1\text{-}\exp(-\frac{eV_{ds}}{k_BT})] \text{ ………………(9)}$$

where A^{*}_{2d} is the 2D equivalent Richardson constant, T is the absolute temperature, Φ_B is the barrier height, and k_B is the Boltzmann constant. For *p*-type Te FET with Pt contact, this equation is only valid when the flat-band voltage (V_{FB}) is below back gate voltage. The Arrhenius plots in Figure 3.6(E) were first obtained from the temperature-dependent transfer curves for the extraction the SBH for hole of FETs with Pt contact. The slope is associated with the barrier height for hole at various back-gate voltages. When the back-gate voltage is larger than flat-band voltage (V_{FB}), the thermionic emission current dominates the drain current. The barrier height has a linear relationship with the gate voltage. When the back-gate voltage is below V_{FB}, thermally assisted tunneling current contributes to the drain current, which results in the nonlinear behavior between barrier height and gate voltage. At the turning point (the back-gate voltage equals to V_{FB}), the relationship between barrier height and the back-gate voltage changes from linear to nonlinear. SBH can be extracted when the back-gate voltage equals to V_{FB}, because thermally assisted tunneling does not contribute to the current. The barrier heights for different back-gate voltages are recorded in Figure 3.6(F). The SBH for hole can be extracted to be 65 meV. The small SBH for hole results from the high work function of Pt contact matching well with the VBM of few-layer Te.

Similar temperature-dependent measurement is also conducted on Te FETs with Pd contact. Figure 3.7(A) presents the transfer curves of Te device with Pd contact at various temperatures. The larger on/off ratio is observed at low temperature, which increases from 10^3 at 250 K to 10^5 at 80K. The temperature-dependent hole mobility summarized in Figure 3.7(B) exhibits same tendency as values for Te FETs with Pt contact. The field-effect mobility is grown from 280 $cm^2V^{-1}s^{-1}$ at 250 K to 384 $cm^2V^{-1}s^{-1}$ at 100 K and then is slightly reduced to 377 $cm^2V^{-1}s^{-1}$ at 80 K. The rise of field-effect hole mobility can be explained by reduced phonon scattering at low temperature while the decline is attributed to the increased contact resistance. The intrinsic hole mobility extracted by Y-function method can exclude the effect of contact resistance, showing gradual increase from as temperature reduction. Figure 3.8 records the barrier heights for different back-gate voltages, which is obtained from Arrhenius plots for extraction of SBH. The barrier height for hole in the Te FET with Pd contact is estimated to be 13 meV.

The temperature-dependent characterizations on Te FETs with Pt and Pd contact have shown the excellent contact formed between metals and 2D Te. The small SBH for hole facilitates the carrier transport and current injection, benefiting the high-performance *p*-type devices based on 2D Te. The small SBH is mainly attributed to the high work functions of Pt and Pd which are far below the VBM of Te, which provides the well-match band alignment. The band diagram between metals (Pt and Pd) and 2D Te is fundamental for high-performance devices.

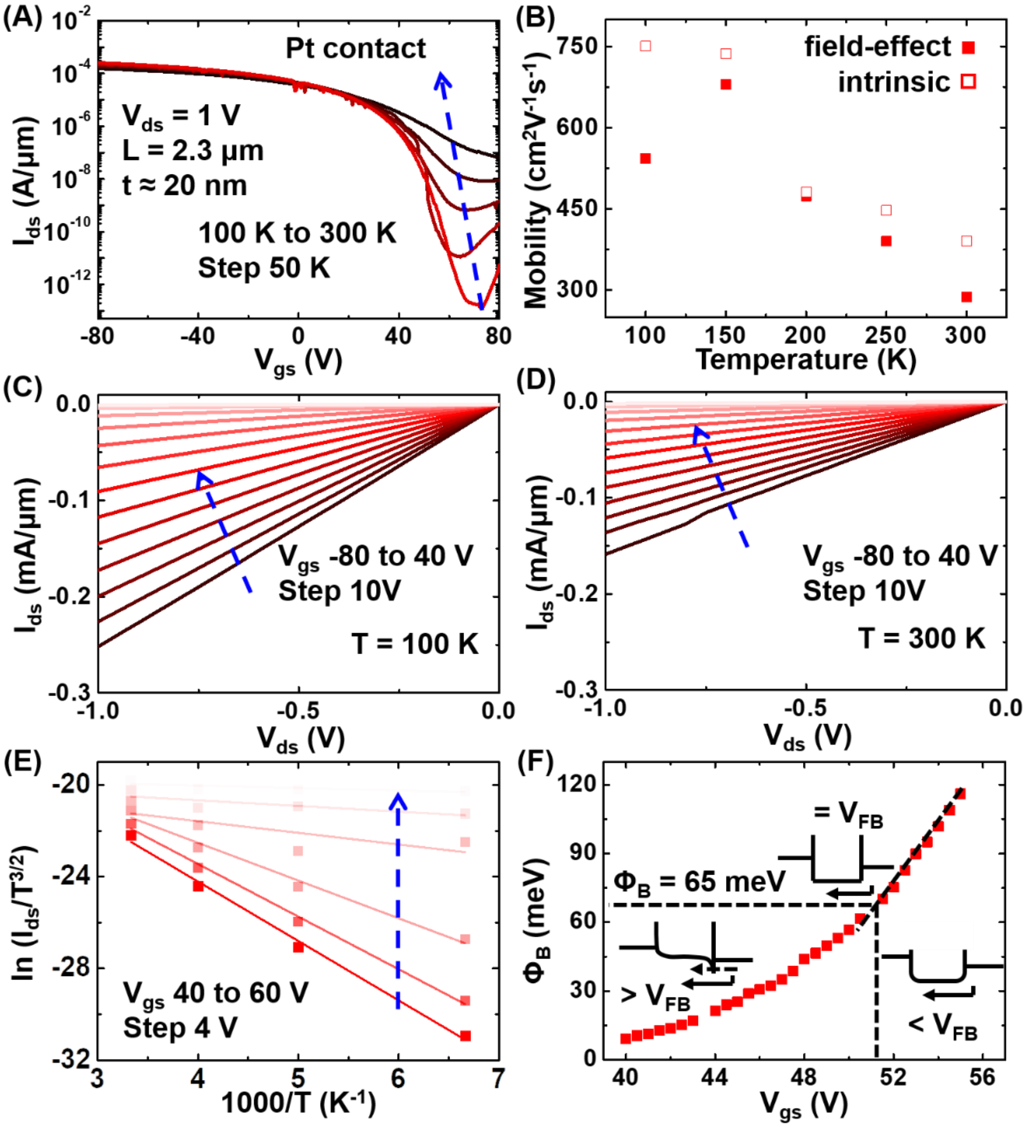

Figure 3.6 (A) Temperature dependent transfer curves of Te FETs with Pt connect. The thickness of Te channel is 20 nm. (B) Temperature dependent field-effect and intrinsic mobility of the Te FET. (C) and (D) Output curves of Te FET with Pt contact at 100 K and 300 K, respectively. (E) The Arrhenius plots for different back-gate voltages. (F) The extracted Schottky barrier heights for different back-gate voltages.

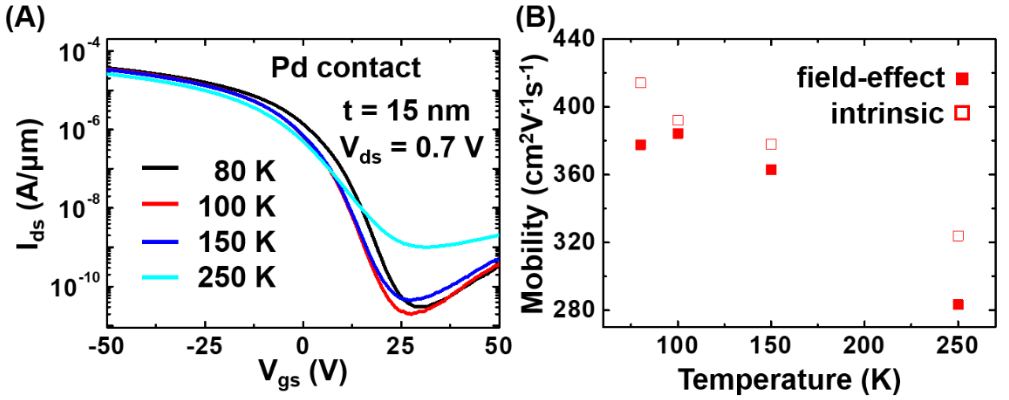

Figure 3.7 (A) Temperature dependent transfer curves of Te FETs with Pd connect. The thickness of Te channel is 15 nm. (B) Temperature dependent field-effect and intrinsic mobility of the Te FET with Pd contact.

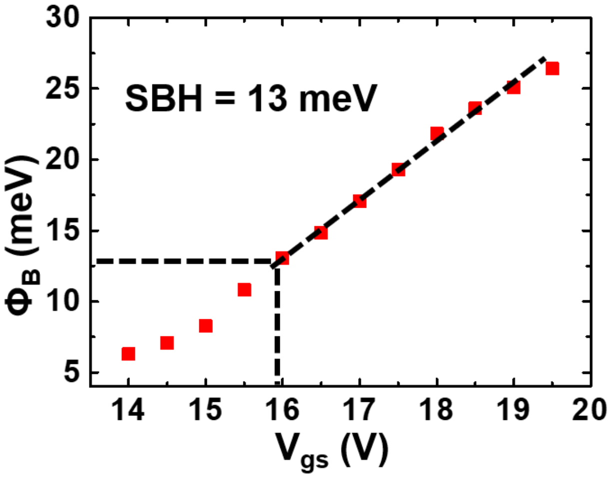

Figure 3.8 The extracted Schottky barrier heights for different back-gate voltages of Te FET with Pd contact.

Contact for electronic device is one of key factors that greatly influences the device performance. Since the application of 2D materials in nanoelectronics, contact engineering is increasingly important for performance improvement. The contact resistance is the performance killer for most electronic devices based on 2D materials. Figure 3.9(A) presents the schematic of TLM model for metal Pt/Te contact. In Te FETs with Pt contact, the negligible sheet resistance of metal contact ($R_{c\text{-}Pt}$), the specific contact resistivity ($R_{c\text{-}c}$) and the sheet resistance of Te beneath the contact within transfer length ($R_{c\text{-}Te}$) compose the contact resistance between Pt metal and Te. The 2D Te is experimentally confirmed to possess large carrier concentration and high carrier mobility, which can alleviate the influence of $R_{c\text{-}Te}$ on contact resistance. The $R_{c\text{-}c}$ is associated with carrier transport between metal and Te. The small SBH for hole derived from the well-match band alignment between Pt and Te is beneficial for hole transport and current injection, which helps to decrease $R_{c\text{-}c}$. The $R_{c\text{-}c}$ can also be improved by the high DoS of Te beneath the contact. It has been reported that small DoS for graphene suppresses current injection from metal to graphene.[123] Low contact resistance can be achieved in metal/graphene contact with high-work function metals, resulting from the increase of DoS for graphene induced by the charge transfer. Figure 3.9(B) theoretically compares the DoS near Fermi level of 2D Te and BP. The high DoS of Te shortens the screening length and promotes the current injection. The small SBH and high DoS for Te bring small $R_{c\text{-}c}$ and sequentially give rise to low contact resistance. The 2D Te as an outstanding *p*-type 2D semiconductor realizes excellent contact with high-work-function metals Pt and Pd. The low contact resistance provides basics for high-performance FETs, which also benefits other novel applications of 2D Te.

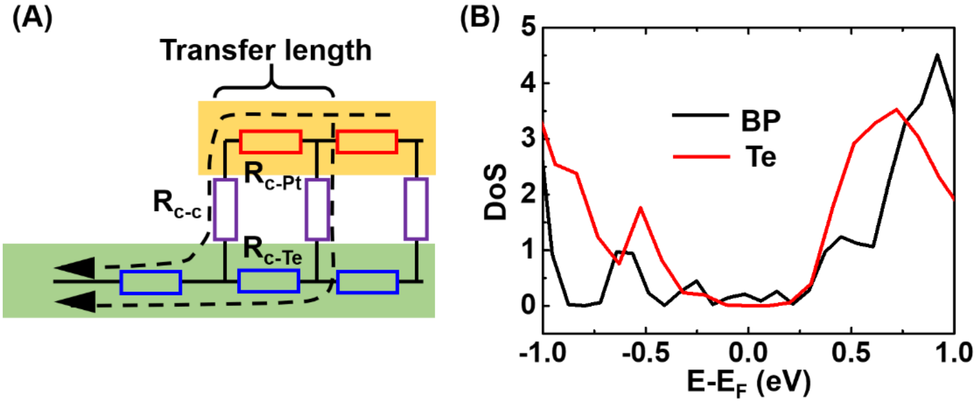

Figure 3.9 (A) Schematic of TLM model for metal Pt/Te contact. (B) DoS comparison between 2D Te and BP.

3.4 Summary

In this chapter, high-performance *p*-type FETs based on 2D Te with Pt or Pd contacts are demonstrated. The metal Pt and Pd have large work functions of 5.65 eV and 5.12 eV, respectively, which are far below the VBM of few-layer Te (4.35 eV). The devices with Pt contact exhibit excellent performance including high on/off ratio of 10^4 and high field-effect/intrinsic hole mobility of 420/504 $cm^2V^{-1}s^{-1}$. The contact resistance can be as low as 400 Ω•μm with small SBH for hole of 65 meV. Comparable figures of metric are attained in devices with Pd contact. The low contact resistance of Pt/Te contact has a great contribution to the high-performance device. The low contact resistance is attributed to small SBH and high DoS for Te. The small SBH is derived from the well-match band alignment between high-work-function metals and Te, which facilitates the hole transport. The high DoS of Te beneath the contacts shortens the screening length and promotes the current injection from metal to Te. The contact engineering by utilizing metals with high work function as contact for Te FETs realizes excellent contact and outstanding performance of Te device, which is beneficial for future application of 2D Te in nanoelectronics.

Chapter 4 Local Thinning Method for Few-layer Tellurium with Pt Catalysis

4.1 Introduction

Two-dimensional (2D) layered materials have received tremendous attentions for their unique physical properties and great potential for future electronics.[28, 53, 61, 82, 84] Recently, emerging group-VI elemental 2D material, tellurene (Te) stands out for its simple composition and excellent properties, *e.g.*, higher carrier mobility than transition metal dichalcogenides (TMDs) and better air stability than black phosphorus (BP).[16, 42] The 2D Te is theoretically predicted to have thickness-dependent bandgap ranging from 0.9 eV for bilayer to 0.3 eV for bulk with extraordinarily large hole mobility reaching 10^4-10^6 $cm^2V^{-1}s^{-1}$.[42] Wang *et al.* demonstrated unipolar *p*-type field-effect transistors (FETs) based on few-layer Te, exhibiting high on/off ratio of 10^5, large drain current of 300 mA/mm and outstanding hole mobility of 700 $cm^2V^{-1}s^{-1}$.[16] There are several theoretical and experimental research works which have shown 2D Te a promising semiconductor replacing conventional silicon channels.[82, 94, 95] Before exploring various applications of 2D Te, it is necessary to prepare large-area, high-quality and single-crystalline samples with thickness control. It has been reported that vapor deposition and solution synthesis successfully grew large-area few-layer Te samples.[16, 94, 95] However, the thickness variation of prepared samples is still beyond satisfactory, which hinders the application of Te with desirable thickness. To attain 2D Te with required thickness for the study of thickness-dependent properties as well as for specific applications, sample thinning is a feasible and controllable approach, which has succeeded in other 2D materials including TMDs and BP.

Thinning for 2D materials with thickness control is basically an etching process, which can be classified as dry-etching and wet-etching. The reported dry-etching methods include plasma treatment,[124] thermal annealing,[125] UV/ozone treatment,[126] and local laser thinning.[127, 128] Among these methods, some thinning processes utilize high-energy laser or plasma to directly sublimate top-layer atoms of 2D materials.[124, 127] Meanwhile, some approaches involve chemical oxidation and oxide evaporation triggered by relatively-high energy including laser, heating and UV irradiation.[125, 126, 128] The dry-etching methods have achieved selective patterning and layer-by-layer thinning of popular 2D materials (*e.g.* TMDs and BP) with delicate adjustment of process parameters. However, the high energy applied to samples in dry-etching can easily damage the bottom layers, which results in defects or disorders in the 2D materials after thinning. Wet-etching is another feasible approach involving chemical reaction in solution at lower temperature. Fan *et al.* demonstrated a solution-based method implementing BP thinning by chemical reaction between BP and solution of two electron-deficient organic reagents (tetramethylpiperidinyl-N-oxyl and triphenylcarbenium tetrafluorobor).[129] Wild *et al.* also presented an aqueous thinning process for exfoliated BP flakes by controllable oxidative degradation of top layers, with water as solubilizing agent.[130] The thinning of BP flakes consists of oxidation of top layers, removal of surface oxidized species by distilled water and termination of etching by non-covalent functionalization procedure. As an emerging 2D material, 2D Te has not received intensive efforts on its thinning process. Solvent-assisted process using alkaline solution with acetone is a reported thinning process for 2D Te.[16] Although this method achieves thinning of Te down to monolayer, the precise thickness control and local etching of 2D Te remains challenges. Therefore, it is vital to develop a feasible thinning process for 2D Te and attain Te with desirable thickness for further device fabrication.

In this chapter, we develop a local thinning method for few-layer Te flakes. Under white light illumination, the few-layer Te experiences controllable thinning with platinum (Pt) catalysis in water. The thickness is reduced by 3 nm with 10-min treatment, which occurs locally near the Pt metal. The thinning process can be explained by photo-oxidation of Te with Pt catalysis, involving electron-hole pairs generation, carrier transfer, Pt catalyzed water-splitting reaction and etching of Te. The Pt metal can also serve as contact metal for high-performance Te FETs, allowing simultaneous measurement of the electrical property of Te with different thicknesses. This local thinning method provides a feasible approach to Te with desirable thickness and presents excellent compatibility with device fabrication process, indicating its great potential in future applications of 2D Te.

4.2 Methods

4.2.1 Te sample preparation

The Te solution dispersion was first prepared by hydrothermal process as the reported work.[16] The Te flakes spread in water were then spin coated onto 300 nm SiO_2 dielectric on highly doped Si substrates.

4.2.2 Device fabrication

Back-gated FETs with Pt contact were first fabricated based on few-layer Te flakes. The substrates with Te flakes were coated with poly(methyl methacrylate) resist (PMMA) for lithography. The source and drain electrodes were patterned by photolithography. Afterwards, 15 nm Pt and 30 nm Au were deposited as contact metals, using an electron beam evaporator. The devices were fabricated after lift-off process. The electrical measurements on these devices were conducted in a probe station (Lakeshore low temperature IV probe station).

4.3 Results and discussion

4.3.1 Local thinning of Te flakes

Figure 4.1(A) schematically presents the thickness reduction of Te flakes near Pt contact after immersion in water under white light. The thinning of few-layer Te occurs in conjunction with multiple factors including Pt contact, light illumination and water immersion. Figure 4.1(B) shows the pristine Te flake covered by Pt/Au contact metals on one side. The metals were patterned and deposit through typical FET fabrication process. After immersion in water with white light exposure for 10 min, the Te flake near the contact metals is obviously thinned according to the contrast change in optical image of the thinned sample, shown in Figure 4.1(C). Interestingly, anisotropy behavior is presented during the thinning of Te flakes. The etching edge is vertical to the chain direction of Te instead of parallel to the edge of Pt metal, which is attributed to much higher etching rate along the Te chains. The AFM image of etching edge in Figure 4.1(D) indicates the thickness change after thinning treatment. The thickness is reduced by about 3.2 nm after 10-min treatment, which is measured from the step between thinned region (~7.7 nm) and unaffected region (~11.2 nm). The thickness change is also confirmed by the Raman spectra in Figure 4.1(E). Three sharp peaks at 89.4 cm^{-1}, 118.8 cm^{-1} and 138.3 cm^{-1}, corresponding to E_1, A_1 and E_2 vibration modes are identified in the Raman spectrum of pristine Te with 11.2-nm thickness, which agree with previous research works.[16, 42] As the thickness is thinned down to 7.7 nm, significant blueshifts for A_1 and E_2 modes are observed, which shift to 120.8 cm^{-1} and 139.1 cm^{-1}, correspondingly. The E_1 mode presents degeneracy with peak broadening in the thinned sample, probably because of the intrachain atomic displacement and the band structure change affected by the thickness reduction.[16] The AFM and thickness-dependent Raman spectra have verified the successful thinning of few-layer Te flakes with Pt contact. The Pt metal does not only form excellent contact with Te for high-performance devices, but also serves as catalyst for local thinning of Te flakes. The local thinning process involving low energy (white light exposure) and environmentally-friendly etchant (water) shows great compatibility with device fabrication and its potential in future applications.

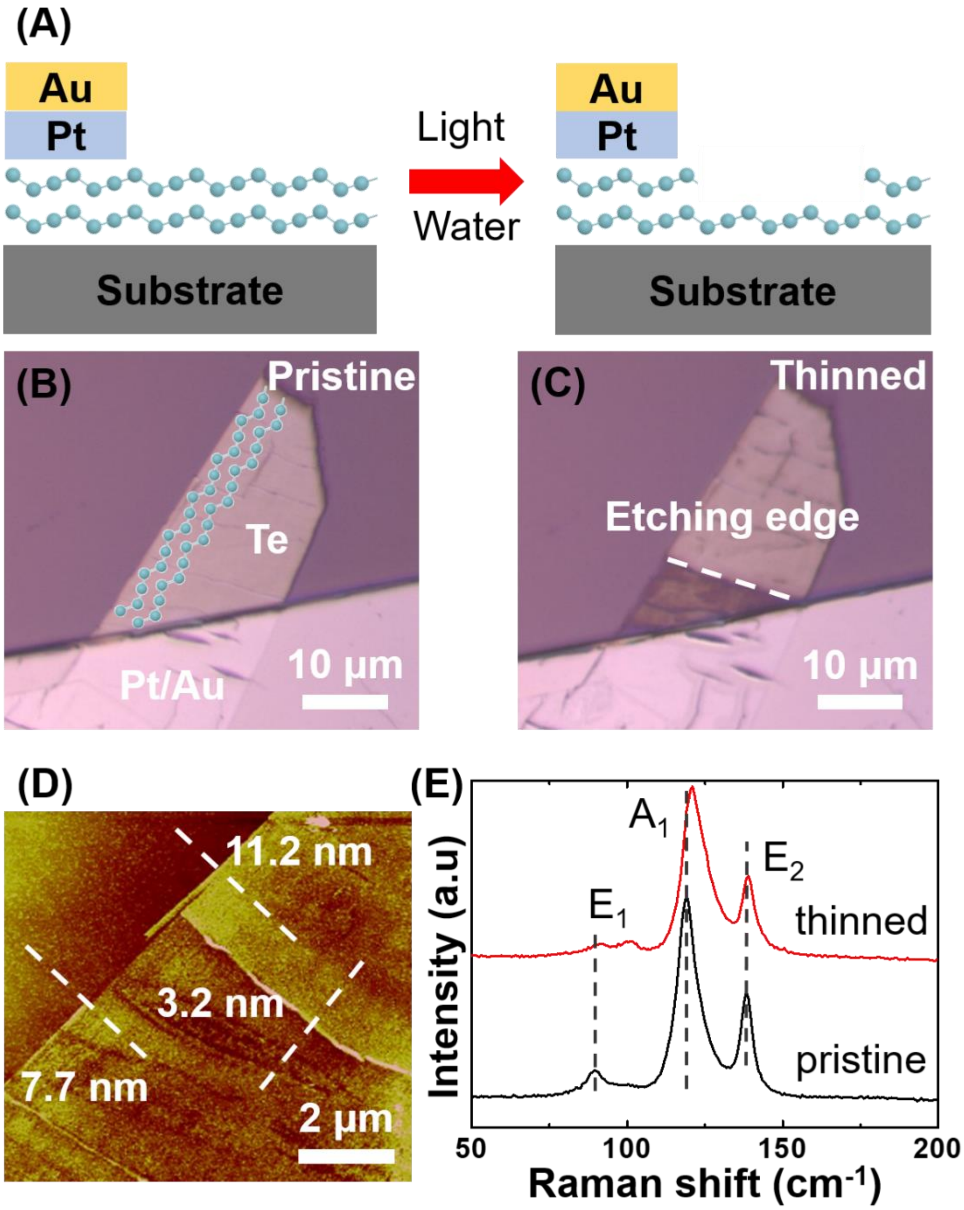

Figure 4.1 (A) Brief schematic of Te thinning involving Pt contact, light exposure and water immersion. (B) Optical image of pristine Te before thinning. (C) Optical image of the Te after thinning. (D) AFM image of thinned Te flakes around the

etching edge. (E) Raman spectra of pristine Te and thinned Te.

The thinning of Te can be explained by photo-oxidation of Te catalyzed by Pt metal. Figure 4.2 shows the schematic of the thinning process, which can be roughly divided by electron-hole pairs generation under light illumination, charge transfer due to work function differences, water-splitting reaction catalyzed by Pt, and etching of Te near Pt metal. Few-layer Te is theoretically and experimentally assured to have a nearly direct band gap covering mid-infrared to red range (0.74 eV for trilayer, 0.49 eV for 13-layer, and 0.3 eV for bulk).[42, 92] The small direct band gap allows the generation of electron-hole pairs in Te under white light illumination. The generated charges will separate and transfer due to the different work functions between Te and Pt. The Pt metal has a high work function of 5.65 eV lying far below the valance band maximum (VBM) of few-layer Te (4.35 eV), which prompts the photo-generated electrons to transfer from few-layer Te to Pt metal. The transferred electrons trigger the reaction with water catalyzed by Pt as below:

$$2H_2O + 2e^- \overset{Pt}{\rightarrow} H_2 + 2OH^-$$

The produced OH^- changes the pH value near the Pt metal and etches the few-layer Te following the reaction as below:

$$Te + 2OH^- + 2h^+ \rightarrow TeO_2 + H_2$$

The total reaction can be summarized:

$$Te + 2H_2O \xrightarrow{Pt,Light} TeO_2 + 2H_2$$

The oxidation species can be rinsed with water leading to fresh and thinned Te flakes. This top-down chemical method for Te thinning benefits from the appropriate optoelectronic property of few-layer Te and band alignment between Te and Pt. The catalyst Pt can be patterned and deposit by device fabrication procedure, which can serve as excellent metal contact after thinning without additional treatment. This thinning technique provides a feasible approach for few-layer Te with desired thickness, with advantages of low-energy requirement, environmental friendliness and compatibility with device fabrication.

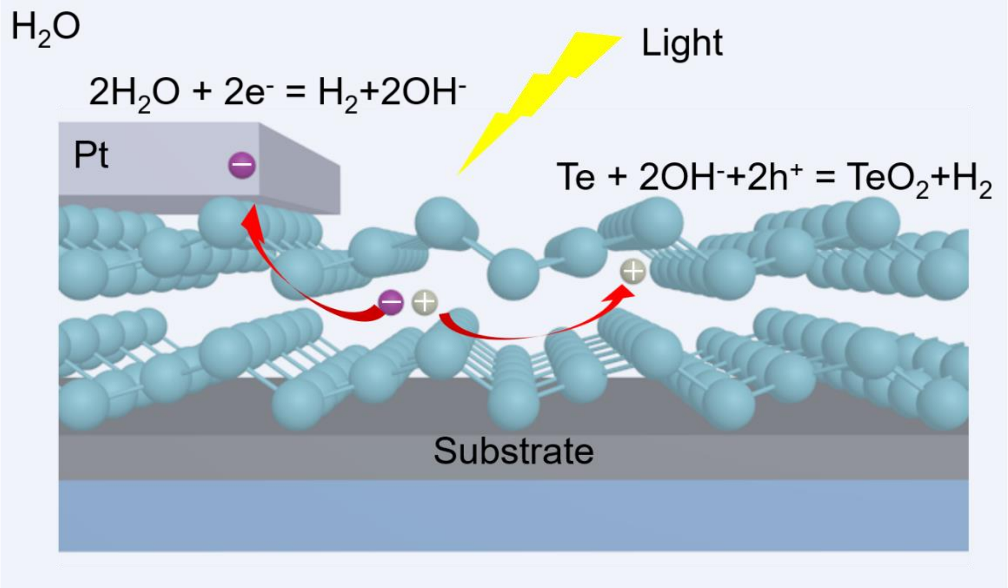

Figure 4.2 Schematic of thinning process for few-layer Te involving electron-hole

pair generation, charge transfer, Pt catalyzed reaction and etching of Te.

To confirm the influence of light illumination and water on thinning process, we performed several control experiments. We first examined the effect of white light illumination. Figure 4.3(A) displays the graphic of thinning process without white light. In Figure 4.3(B), a typical Te flake with 60-μm length and 40-nm thickness were chosen. After deposition of Pt electrodes, the Te was immersed in dark for 30 min. There is no significant change of optical contrast observed in the treated Te, indicating thickness reduction cannot be triggered without light. The same sample was then immersed in water again but under light illumination for 30 min. The treated Te flake is obviously thinned, which is revealed by the contrast change in the optical image. The comparison has confirmed the great importance of light illumination, without which the thickness reduction of Te will not happen. White light illumination is a low energy source allowing the trigger of photo-oxidation of Te, which is attributed to the small band gap of few-layer Te. The nearly direct bang gap of few-layer Te permits generation of electron-hole pairs excited by white light illumination. The photo-generated charges prompt the water-splitting reaction and the following etching of Te. It is presented that light illumination is of vital in the thinning process of 2D Te.

We also attempted to figure out the effect of water, which is related to water splitting, hydrogen production and Te etching by the left OH^-. As depicted in Figure 4.3(C), the pure water was changed to 1 mol/L silver nitrate ($AgNO_3$) solution for immersion of Te with Pt contact, which is often utilized in water splitting reaction as oxidizing reagent.[131] The presence of redox reagent Ag^+ changes the half reactions of water splitting and sequentially affects the thinning process for Te. The supposed reactions with redox reagent Ag^+ are as below:

reduction:

$$Ag^+ + e^- \xrightarrow{Pt} Ag$$

oxidation:

$$2H_2O + 4h^+ \rightarrow 4H^+ + O_2$$

total:

$$4Ag^+ + 2H_2O \xrightarrow{Pt,Light} 4Ag + 4H^+ + O_2$$

Figure 4.3(D) presents the pristine Te and the identical Te with Pt contact treated by immersion with $AgNO_3$ solution under white light for 30 min. The treated Te is found to become thicker covered by black solid which should be Ag solid produced in the photocatalytic reaction. The Ag^+ reagent changes the water-splitting reaction, hindering the production of OH^- and allowing Te not to be etched. The Te flake was covered by Ag instead of etched by OH^- with the existence of oxidizing reagent. The Ag products manifest the occurrence of water-splitting reaction involving photo-excited charges in Te semiconductor.

The thinning by photo-oxidation of Te can be considered as etching process via water-splitting reaction with photo-semiconductor catalysis. The process proceeds according to several steps as reported photochemical water splitting:[131](1) light absorption and electron-hole pairs generation; (2) charge separation and transfer; (3) reducing reaction between photo-generated electrons and H_2O and oxidizing reaction between holes and Te. The Te flakes are etched and thinned during the oxidizing reaction. Light illumination is the beginning of the thinning process. Because of the small band gap of few-layer Te in the near infrared (NIR) range, white light can stimulate electrons in the conduction band and create electron-hole pairs in Te, without which the etching reaction cannot be triggered. The Pt metal plays an important role in the subsequent steps. As an excellent catalyst, Pt also benefits the separation and transfer of photo-generated charges due to its high work function (5.65 eV) lying far below the VBM of few-layer Te (~4.35 eV). The band structure of Te with Pt contact prompts the charge separation and effective electron transfer from Te to Pt, facilitating the water-splitting reaction near Pt contact. In the region far from Pt, the electron-hole pairs will recombine quickly before transfer, resulting in maintenance of Te in this region. This feature permits the local thinning of Te by patterning Pt contact. The thinning method for Te is basically an etching process by photo-oxidation of Te, taking advantage of water splitting with photo-semiconductor catalysis.

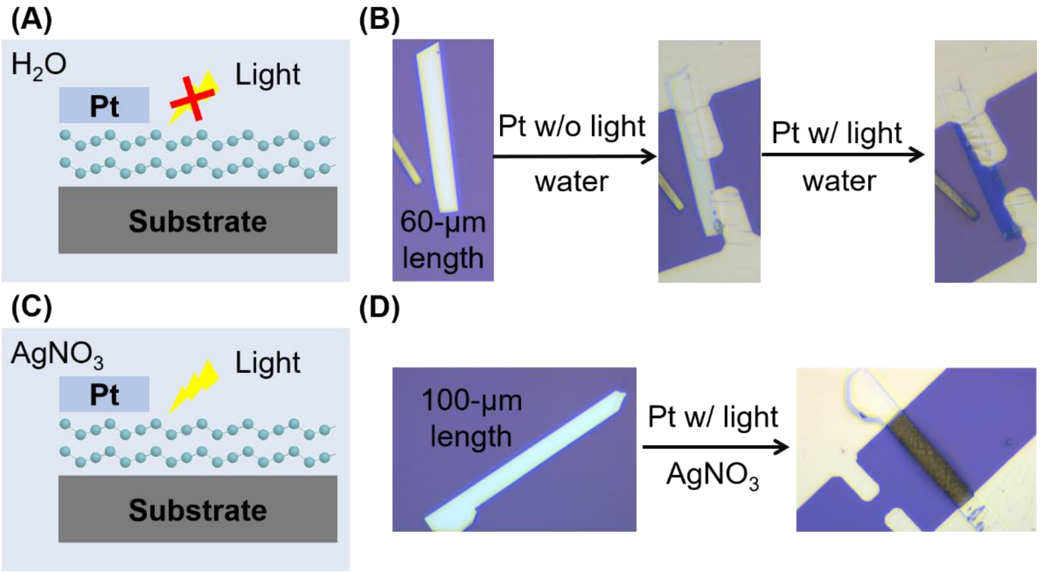

Figure 4.3 (A) Schematic of thinning process without light illumination. (B) Optical images of the pristine Te, the treated Te immersed with water in dark and the Te immersed with water under white light. (C) Schematic of thinning process utilizing $AgNO_3$ solution to replace water. (D) Optical images of the pristine Te and the treated Te immersed with $AgNO_3$ solution under white light.

4.3.2 Thickness-dependent electrical property

Except serving as catalyst in thinning process, the Pt metal forms excellent contact with Te for *p*-type FETs, which enables the electrical measurement for an identical Te FET during thickness reduction. Figure 4.4(A) records the optical images of a typical Te FET with 9-μm channel length and 9-μm width at different time-points in 30-min thinning treatment. The optical contrast change suggests the thickness reduction of Te in the channel. Figure 4.4(B) presents the transfer curves of Te FET during the thinning process. The pristine Te FET exhibits a high on/off ratio of 5×10^3, which is increased to 10^4 after 30-min thinning process. The enhanced on/off ratio is attributed to the better gate electrostatic control in thinner Te. As the thickness of Te continuously decreases, the sheet resistance of Te channel will increase and cause lower current density, which has been observed in the reported works on Te and other 2D materials.[16, 95, 105] However, in the first 30s, the thinning treatment will increase the drain current of Te FET, which is presented in the transfer curves in linear scale in Figure 4.4(C). The drain current is then decreased as expected when the thinning continues for 1 min or longer. In Figure 4.4(D), the output curves of Te FET treated with different time durations also show the distinguishing current tendency. With 50 V gate voltage and 1 V drain voltage, the drain current is increased from 94 μA to 136 μA in the first 30 s treatment and then gradually declined to 24 μA as the thinning continues. The increase of drain current benefits from the reduction of charge traps at surface which is etched at the early stage of thinning process. The charge traps like Te cluster and impurities at surface can attract photo-generated charges and trigger etching reaction before the host Te channel, smoothing the surface of Te channel. The surface improvement at the early stage of thinning reduces charge scattering in Te channel and consequently increases the drain current. After the etching of surface impurities and improvement of Te surface, the thickness reduction begins sequentially, which increases the channel sheet resistance and lowers the drain current. The surface smoothing is further indicated by the thinning-time-dependent hole mobility in Figure 4.4(E). The hole mobility of FET based on pristine Te is about 289 $cm^2V^{-1}s^{-1}$. After very short thinning treatment (< 1min), the mobility of the device is improved to 306 $cm^2V^{-1}s^{-1}$. The enhancement of hole mobility is because of the surface smoothing and reduction of charge scattering. As the thinning continues, the effect of thickness reduction is dominant, resulting the decline of mobility as the reported work.[16] Thinner Te is more susceptible to impurities at the interface and charge scattering, which can explain the decline of mobility as thickness reduction.

The compatible thinning method involving Pt metal enables the electrical measurement as thinning processes. The successful thickness reduction is indicated by the lower drain current, higher on/off ratio and lower hole mobility after thinning treatment, which follows the same trend of thinner Te in the reported works.[16] It is also found that the very short thinning treatment can smooth Te surface and reduce charge impurities at the surface, which can alleviate the charge scattering in Te and improve the performance of FETs. This suggests that this method can be a pre-treatment of Te FETs with Pt contact for performance improvement before device application.

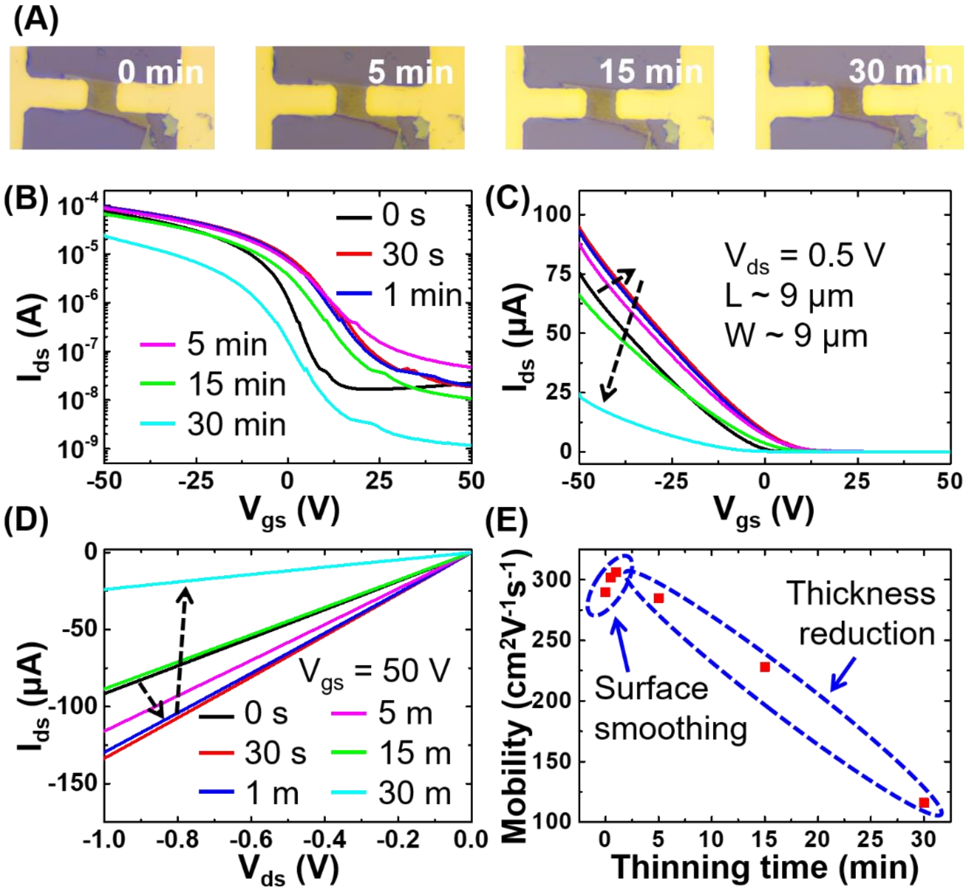

Figure 4.4 (A) Optical images of an identical Te FET treated by thinning method

with different time durations. (B) and (C) Transfer curves in (B) log scale and (C) linear scale of the Te FET thinned for 0s, 30s, 1min, 5min, 15min, and 30min. (D) Output curves of the Te FET treated for 0s, 30s, 1min, 5min, 15min, and 30min. (E) Hole mobility of the Te FET treated with different time durations.

4.4 Summary

In this chapter, we develop a thinning method for Te with Pt contact. This technique takes advantages of photo-oxidation of Te, which is achieved by water-splitting reaction with catalysis. The process involves several steps including: (1) light illumination and electron-hole pairs generation in Te; (2) charge separation and transfer by different work functions of Te and Pt; (3) water-splitting reaction; (4) etching of Te by oxidizing reaction between holes and Te. The thickness of Te is measured to reduce by 3 nm with 10-min treatment. The Pt metal facilitates charge separation and catalyzes water-splitting reaction, which limits the etching reaction of Te occurring near Pt and realizes local thinning. This thinning approach is also compatible with device fabrication and measurement. The electrical characterization during thinning reveals that very short treatment can improve device performance by smoothing the Te surface while thickness reduction dominates for process with longer time duration. This thinning method provides a feasible approach for few-layer Te with desired thickness, which is distinguished for its low-energy requirement, environmental friendliness and great compatibility with device fabrication and measurement. The thinning process allows wafer-scale treatment of devices based on few-layer Te.

Chapter 5 Conclusions and Outlooks

5.1 Conclusions

In conclusion, this thesis develops the understanding on the carrier transport behaviors of 2D BP and Te, which are of great importance for future applications in nanoelectronics. The study focuses on contact engineering, one of critical factors influencing the carrier transport in 2D materials.

For few-layer BP, the *n*-type FETs are demonstrated with Cu contact which is chosen because of the *n*-type doping effect and theoretical Ohmic contact formed between BP and Cu. The cross-section TEM characterizations on the interface between BP and Cu indicate that highly diffusive Cu atoms migrate into BP and intercalate between BP layers without changing the crystal structure. In theory, the interstitial Cu-doped BP has a smaller band gap than pristine BP and the Fermi level is shifted towards conduction band after Cu diffusion. The interstitial Cu-doped BP edge contact achieves *n*-type dominant FETs, which exhibit high electron mobility of ~ 138 $cm^2V^{-1}s^{-1}$ and on/off ratio of ~ 100 at room temperature. The current density can reach 58 μA/μm with negligibly low Schottky barrier height for electron. The metallic-like electrical property of interstitial Cu-doped

BP edge contact also results in low contact resistance (5 kΩ•µm). The *n*-type transport property of BP FETs with Cu contact is attributed to *n*-doping induced by the diffusion of highly-mobile Cu atoms at the contact region. The penetration of Cu metal also changes the electrical property of BP beneath contact metal, leading to the excellent edge contact between Cu-doped BP and pristine BP.

For few-layer Te, high-performance *p*-type FETs with high-work-function contact metals (Pt and Pd) are fabricated and characterized to study the transport property of few-layer Te. The Te FETs with Pt contacts exhibit unipolar *p*-type transport property with field-effect hole mobility reaching 420 $cm^2V^{-1}s^{-1}$ and on/off ratio up to 10^4. The intrinsic hole mobility is estimated to be 504 $cm^2V^{-1}s^{-1}$. The current density can reach 0.17 mA/µm with Schottky barrier height for hole of 65 meV. The contact resistance can be as low as 400 Ω•µm, indicating the excellent contact between few-layer Te and contact metals. Comparable performance is also exhibited in the Te FETs with Pd contact. The remarkable *p*-type transport property of Te FETs results from the well-match band alignment between few-layer Te and high-work-function contact metals. The work functions of Pt and Pd are lying far below the VBM of few-layer Te, which facilitates the hole transport in Te. The small SBH for hole and the high DoS of Te near

Fermi level promote carrier transport and facilitates the current injection from contact metals to Te, which brings low contact resistance and benefits the high-performance of Te FETs.

After investigation on transport property of 2D BP and Te, we demonstrate a thinning method for Te because of the limited study on thickness control of few-layer Te. A local thinning process for few-layer Te involving Pt metal is developed. The thickness of few-layer Te near Pt contact experiences thinning in water under white light illumination. The thickness is reduced by ~ 3 nm with 10 min process. The thickness reduction involves electron-hole pair generation, charge transfer, water-splitting reaction catalyzed by Pt and etching reaction of Te. Due to the small bandgap of few-layer Te, the electron-hole pairs can be easily generated under white light. The photogenerated electrons will transfer to Pt metal with high work function. The transferred electrons will react with water producing H_2 with Pt catalyst. The left OH^- in water change the pH value near Pt and etch the few-layer Te, resulting thickness reduction of Te near Pt. This local thinning process is compatible with device fabrication process, providing feasible approach to few-layer Te with desirable thickness for various kinds of electronic devices with the advantages of low-energy requirement and environmental friendliness.

As emerging elemental 2D materials, BP and Te still require thorough understandings to fulfill their great potential in future nanoelectronics. This thesis studies the carrier transport behaviors of 2D BP and Te with contact engineering. The thickness control of few-layer Te is also demonstrated. The study helps to deepen the understanding on 2D BP and Te, which benefits the various applications in nanoelectronics.

5.2 Outlooks

The BP and Te representing typical elemental 2D semiconductors have attracted intensive research interests for their extraordinary electrical properties and great technological potential. The recent studies have open up new opportunities and brought some challenges for development of 2D BP and Te.

Preparation of large-area and high-quality samples is one of the most challenging problems before industrial applications of BP and Te. For 2D BP, the high-quality samples for device applications are mainly prepared by mechanical exfoliation. The low yield and small size of attained BP samples limit the large-area applications like integrated circuits. Although with some trials of vapor deposition for 2D BP, the development of large-area deposition for high-quality BP is greatly hampered due to the instability of BP. For 2D Te, solution synthesis can prepare 2D samples for high-performance devices. However, the thickness variation of solution-synthesized samples is one of problems influencing the uniformity of device performance. Also, the reported vapor deposition methods are beyond satisfactory. The qualities including purity, crystallinity and surface smoothness of Te samples still require necessary enhancement for further applications of 2D Te in large-scale nanoelectronics. Therefore, the reliable and large-area preparation methods for high-quality 2D BP and Te are worth future research investigation before wafer-scale industrial applications of BP and Te.

Considering various applications of few-layer BP, air- and water-stability are other critical issues that hinder the development of electronic devices based on 2D BP. Long-term exposure of BP to air or water will change the composition and properties of BP and consequently degrade the device performance. Capping layers have been developed to protect BP from air and water, which successfully enhances the stability of BP. The protection strategy still remains a challenge to simultaneously prevent reaction between BP and atmosphere and maintain the pristine properties of BP. The compatibility with industrial processes is also important for large-scale applications of BP.

As one of the newest 2D materials, few-layer Te has not received enough research efforts compared with BP. The 2D Te is a promising *p*-type semiconductor with excellent electrical properties and stability, distinguishing itself from 2D BP. The research on 2D Te is at a very early stage. The reported FETs based on 2D Te mostly exhibit *p*-type transport property because of the high level of VBM of Te and the Fermi level pinning effect at the contact. However, complementary circuits require same channel materials for both *p*-type and *n*-type devices. Before further application of 2D Te in nanoelectronics, the carrier dynamic and transport behaviors in 2D Te remain obscure and require thorough understanding, which are basic to modulate carrier transport and control device polarity. The modulation approaches including contact, doping and interface engineering are worth investigating to achieve polarity control, improve device performance and extend novel applications of 2D Te. In particular, the Cu contact realizing *n*-type BP FETs is worth investing in achievement of *n*-type Te FETs due to the similar *n*-doping effect of Cu in Te. The diffusion of Cu in 2D Te and the corresponding influence on device performance can promote the understanding of contact engineering on few-layer Te.

The 2D heterostructures by stacking different 2D materials sequentially have been appealing research interest since the discovery of 2D materials, which offers unprecedented possibilities for novel applications. The properties of 2D heterostructures are determined by band alignments and charge transfer at the interfaces. Although some theoretical works predicted the properties of the heterostructures between few-layer Te and other 2D materials, the demonstration of heterostructures with 2D Te are rarely reported in experiment. The research investigation on heterostructures with 2D Te can further extend the applications of Te to other fields such as heterojunction solar cells.

In summary, 2D elemental semiconductors BP and Te have shown their great potential in future nanoelectronics. To fulfill the potential, the in-depth understanding on sample preparation, carrier dynamic, device performance enhancement, *etc* is of vital importance and worth future research investigation, which greatly benefits the realization of various applications in nanoelectronics.

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