STUDY OF SNSE AND SRTIO3 THIN FILMS FOR MEMRISTOR DEVICES

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Study of SnSe and SrTiO3 Thin Films for Memristor Devices

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CERTIFICATE OF ORIGINALITY

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Abstract

Due to the bottleneck limitation of von Neumann architecture-based hardware, the current Artificial Intelligence (AI) needs a large and complicated structure and a huge number of energy and memory accessing time to support the learning and thinking operation. Inspired by the operation of human brain, neuromorphic computing system built with circuit elements to mimic the neurobiological activities is a good concept to meet the challenge. Toward this application, resistive random-access memory (RRAM) has attracted great interest for non-volatile, low-power consumption, non-destructive readout, and high-density memories. In this work, RRAM devices based on SnSe and $SiTrO_3$ (STO) thin films and their heterostructures with Ag and Cu electrodes are fabricated by pulsed-laser deposition, and their different structures and memory characteristics are investigated.

Growth temperature-dependent microstructural study reveals that, the SnSe thin films grown at 300℃ on a Pt-coated silicon substrate possesses crystallized structure with better multi-level switching and endurance memory characteristics compared to that of the lower temperature grown film. With the STO buffer layer, the SnSe/STO heterostructure device shows much better performance on reliability test.

Multi-level switching studies reveal that the Cu/SnSe/STO/Pt heterostructure device can present 6 resistance states and the Ag/SnSe/STO/Pt device presents 8 resistance states; all states remain stable after 10000 seconds, suggesting very good

retention property. These results suggest that the Ag/SnSe/STO/Pt heterostructure device may function well in traditional multilevel memory applications. The memristive performance of SnSe/STO heterostructure suggests that these heterostructure devices are promising for applications in neuromorphic computing as a synaptic device.

List of Publications

Journal Articles

1. Lyapunov, N., Zheng, X. D., Yang, K., Liu, H. M., Zhou, K., Cai, S. H., Ho, T. L., Suen, C. H., Yang, M., Zhao, J., Zhou, X., Dai, J.-Y., A Bifunctional Memristor Enables Multiple Neuromorphic Computing Applications. Adv. Electron. Mater. 2022, 2101235.
2. Lyapunov, N.; Suen, C.H.; Wong, C.M.; Tang, X.; Ho, T.L.; Zhou, K.; Chen, X.X.; Liu, H.M.; Zhou, X.; Dai, J.Y. Ultralow Switching Voltage and Power Consumption of GeS2 Thin Film Resistive Switching Memory. *J. Adv. Dielect*. 2021, 11, 2150004.
3. Ho, T.L.; Ding, K.; Lyapunov, N.; Suen, C.-H.; Wong, L.-W.; Zhao, J.; Yang, M.; Zhou, X.; Dai, J.-Y. Multi-Level Resistive Switching in SnSe/SrTiO3 Heterostructure Based Memristor Device. *Nanomaterials* 2022, 12, 2128.

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Finally, I want to give my special love and appreciation to my parents and little sister, for their understanding, forever love, and endless care for me. I would like to give my highest praise to the Lord, the holy, faithful, and gracious creator. 'For from him and through him and to him are all things. To him be the glory forever! Amen!

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Chapter 1 Introduction

Due to the rapid growth of Information Technology (IT), human society has entered into a new era of big data and the Internet of Things (IoT). However, this development brings a great challenge and demand to computers for data processing. As the demand for high-performance computers increases, the traditional Von Neumann architecture computer becomes less efficient since it separates the memory and calculation modules, so current computers need large and complicated hardware and numerous of energy and memory accessing time to support the operation. To address this problem and cope with the demands from IT market, new memory devices need to be developed with higher storage density, faster operation speed, and lower power consumption.

Device size has decreased steadily as memory technology has evolved, while for conventional charge storage systems like capacitor-based Dynamic Random Access Memory (DRAM) and floating-gate flash memory, the aggressive scaling has provoked critical issues. Construction of small footprint capacitors with sufficient capacitance to store identifiable data for modern DRAM is becoming more and more challenging. Low endurance, sluggish speed, and high write voltage are problems for flash memory. Future generations of flash memory may need complex and expensive advancements like charge trap [1] or 3D stacking [2] to provide products that satisfy client demands.

Owing to the higher storage density, faster response, higher endurance, non-volatile characteristics and continuous conductance change property, many potential technologies are being developed such as magneto-resistive RAM (MRAM),

ferroelectric RAM (FeRAM) and electrical resistance switching RAM. In the group of electrical resistance switching RAM (RRAM), there are valence change memory (OxRAM), phase-change memory (PCRAM), and conductive bridge memory (CBRAM). Among them, CBARM is considered as one of the most desirable devices for emerging computer architecture to solve the challenges in integrating memristor chips and is also the topic of this thesis work.

1.1 Historical development of Memristor

In 1971, beyond three types of basic passive circuit components of resistor, capacitor, and inductor, Leon Chua hypothesized the existence of the fourth fundamental passive circuit element “memristor”. As shown in Figure 1.1, the term memristor, as a combination of the word’s "memory" and "resistor," refers to the fourth element. The link between these key circuit variables can be described by a set of equations which may be utilized to account for the correlation between the magnetic flux Φ and charge q [3]. Among them, the definition of memristance M is given as:

$$\mathrm{d}\Phi = \mathrm{M}\mathrm{d}q \tag{1.1}$$

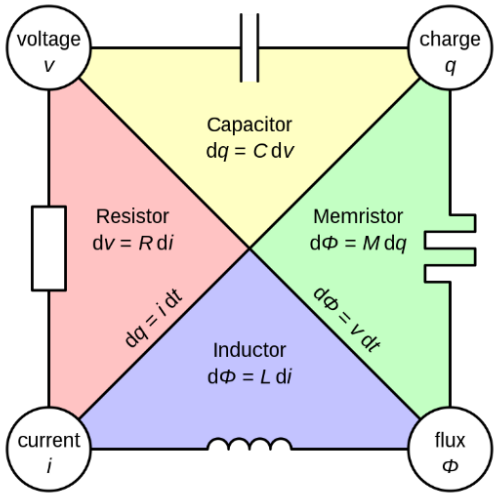

Figure 1.1. Relations between the four fundamental electronic variables and devices that implement these relations. [3]

Stanley Williams and colleagues from Hewlett-Packard Labs made a connection between this theory and a practical memristor prototype in 2008, i.e., memristors are two-terminal devices that are sometimes referred to as resistive random-access memory (RRAM). They employed a linked variable-resistor model to explain the internal mechanism during the memristor switching, where mobile dopants result in resistance change when influenced by an electric field [4]. In this model, by assuming that the memristor has two regions, i.e., a doped low resistance region, and an undoped high resistance region, the boundary between these two zones can be moved by an external bias *v(t)* causing the charged dopants to drift. This process can be described as:

$$v(t) = \left(R_{\mathrm{ON}} \frac{w(t)}{D} + R_{\mathrm{OFF}} \left(1 - \frac{w(t)}{D} \right) \right) i(t) \qquad (1.2)$$

where $w(t)$ is the width of the doped area and D is the width of the entire region. R_{ON} and R_{OFF} represent the resistance of a fully doped device and an undoped device,

respectively.

1.2 General working principles of RRAM

As shown in Figure 1.2 [5], the majority of memristive/resistive switching devices have either unipolar or bipolar switching. A memristive device changes from its high resistance state (HRS) to its low resistance state (LRS) through a process known as SET process. In addition, the action of switching a device from the LRS back to the HRS is known as the RESET process. Before they can demonstrate "typical" resistive switching, the majority of reported memristors need to undergo some sort of electroforming process. A higher voltage is needed for the electroforming process or FORMING, i.e., the first switching process from the HRS to LRS. Some devices require this FORMING (or electroforming) process because, in contrast to RESET and SET which will only rupture or restore a portion of the filament, building a complete filament from the pristine state of a dielectric film requires a higher voltage or more time (for a given voltage stimulus). Dielectric memristive materials such as oxides or nitrides, which function by modifying native dopants (such as oxygen or nitrogen vacancies), involve electrically creating native dopants during the electroforming process, while the native dopants are primarily moved during the RESET and SET processes. Bipolar switching denotes that SET and RESET occur at opposite polarities, whereas unipolar switching refers to switching when SET and RESET occur at the same polarity of applied voltages. A device is categorized as a nonpolar memristor if it can be switched to either its HRS or its LRS at one polarity but can be switched back

to its initial resistance state at either polarity. By including dopants or partially conducting routes into the switching film during the fabrication process, electroforming could be avoided [6].

Technologies for resistive memory are created utilizing a metal-insulator-metal (MIM) framework. It is possible to modify the device's resistance by applying a voltage. To prevent the device's resistance state from changing, low potential detection is necessary. There are essentially three competing technologies that fall under this fundamental framework and are at various degrees of manufacturing development. Those three technologies are valence change memory (OxRAM), phase-change memory (PCRAM), and conductive bridge memory (CBRAM) which is the topic of this work.

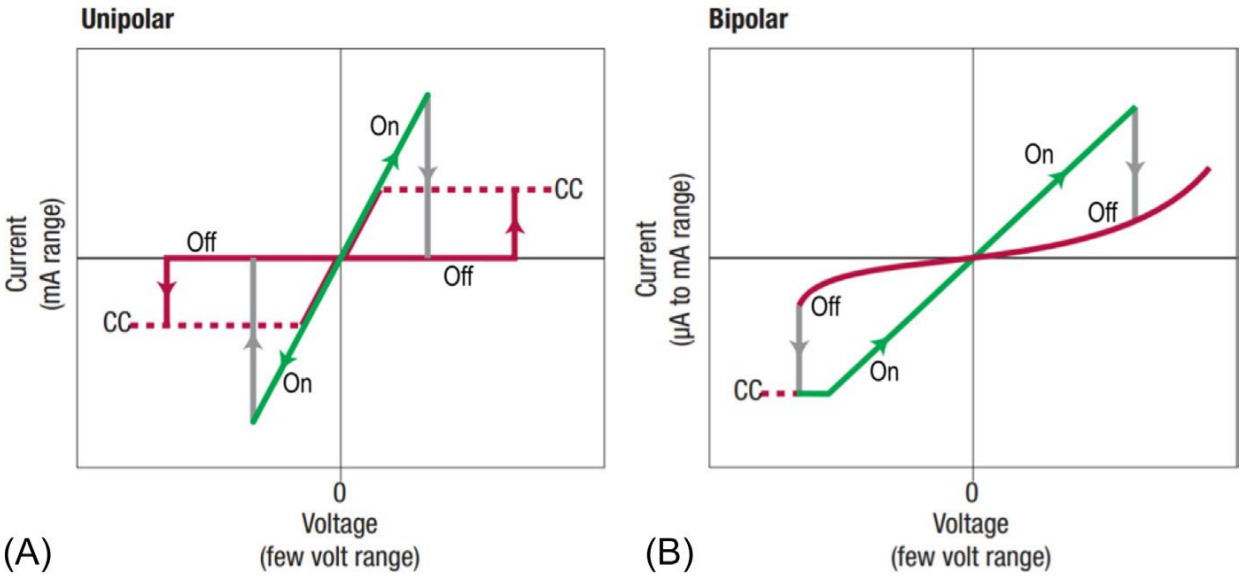

Figure 1.2. Two basic operation modes of a memristive device. (A) Unipolar (or nonpolar) and (B) bipolar. CC denotes compliance current controlled by external circuit. [5]

1.2.1 Valence Change Memory (OxRAM)

The migration of oxygen vacancies causes filament formation and rupture in OxRAM. The displacement of oxygen vacancies occurs in transition metal oxide (HfO_2, Ta_2O_5, NiO [7]–[9]) sandwiched by two electrodes, where an oxygen vacancy provider is required which can be a specific oxidizable electrode (such as Hf, Ta, Ti) or a specific resistive layer depleted in oxygen [8], [10], [11]. So far, there are two strategies to explain a switching mechanism based on oxygen vacancy displacements. One is that the oxygen vacancies already exist in the resistive layer, and when enough oxygen vacancies form a conducting channel in the oxide, it results in the formation of a filament, i.e., a Forming process. This process brings the cell into a low resistance state, and oxygen vacancies are responsible for electrical conduction. The rupture of this filament is called Reset which brings the cell back to the original high-resistance state. Another strategy relies on the generation and eradication of oxygen vacancies [12] during each cycle, not just during Forming. During SET or RESET, local redox reactions of the resistive layer might change the concentration of vacancies.

The difference in voltage favoring either metal oxidation or oxide reduction explains why the switching mechanism is bipolar. If the RESET process is merely thermally driven, a unipolar switching is furthermore feasible. A diagram of these two hypotheses is presented in Figure 1.3.

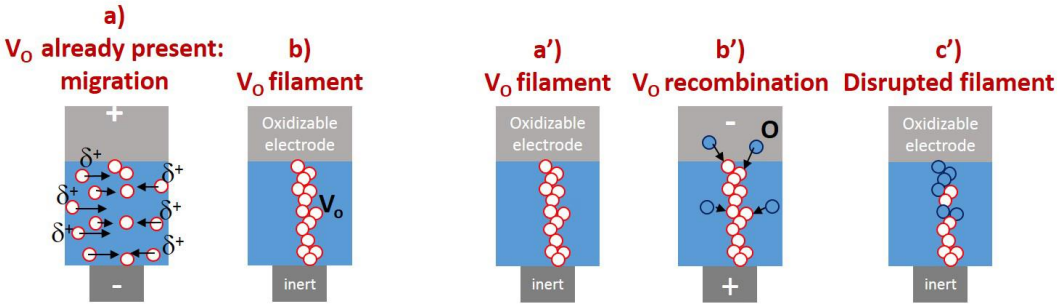

Figure 1.3. Schemas of oxygen vacancies (V_O) displacement at the heart of OxRAM technologies: (a) and (b) oxygen vacancies redistribution in the resistive layer. (a'), (b') and (c') oxygen vacancies recombination. [9]

1.2.2 Conductive Bridge Memory (CBRAM)

Conductive bridge memory (CBRAM), also referred to electrochemical metallization memory (ECM) and programmable metallization cell (PMC), is a possible option for next-generation memory. In the memory cell, an easily oxidizable metal, such as silver (Ag) or copper (Cu), is usually used to serve as the anode, and in order to create a metal-insulator-metal structured device, the cathode is built with a non-oxidizable metal, such as tungsten (W) or platinum (Pt). In 1976, Hirose and Hirose [13] published the first report on the memory where a reversible electrical resistance switching was performed using an Ag anode, a Pt cathode, and Ag photodoped arsenic trisulfide (As_2S_3) as an ion-conducting memory layer. The anode-chalcogenide interface undergoes an electrochemical process that produces silver ions when an electric field is applied. The ions penetrate the chalcogenide memory layer due to the electric field before being reduced at the tungsten cathode. The cathode and anode of

the device are connected by a metal filament, which finally shorts the circuit. Figure 1.4 [13] depicts a bridging device from the Hirose and Hirose study. In this device, when the gap is filled, the device's resistance decreases from high to low. The silver filament melts when the electric field is reversed; while some silver is left in the memory layer, and the majority returns to the anode. The device then exhibits high resistance once more.

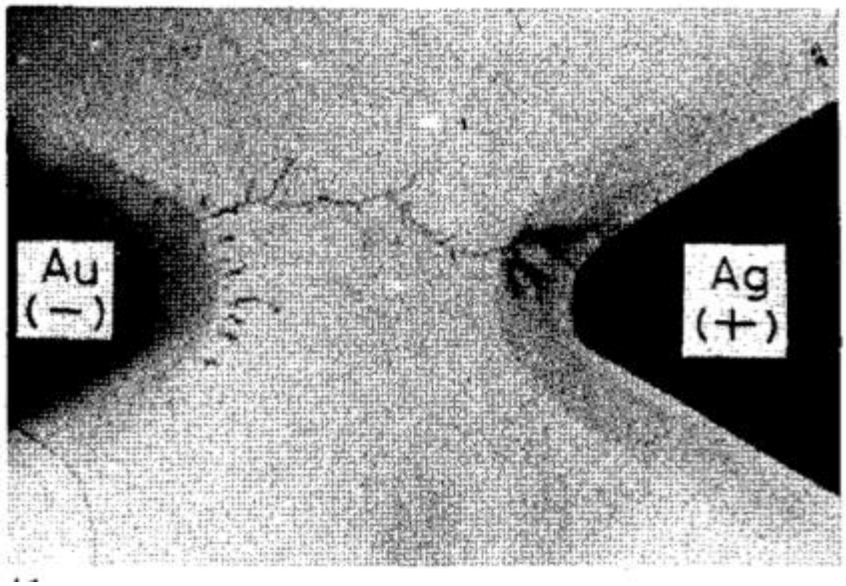

Figure 1.4. TEM image of a formed Ag filaments in resistive switching device between the anode and cathode [13].

The operation of the ion conducting memory device is schematically shown in Figure 1.5 [14]. The voltage rises starting with (A), i.e., the write operation. During this process, at the anode, silver oxidizes before moving through the electric field and reducing at the cathode; while on the cathode, a silver filament starts to form and fills the gap as the applied voltage rises. Since the filament offers a significantly reduced

resistance path between the two electrodes, current flow rises right away. Now the information (0 of 1) is written to ON state as shown in (B). The maximum compliance current in Figure 1.5 is set to 25 μA.

When the applied voltage sweeps back, current-voltage response linearly since the filament is operating like a resistor now. During this period, Ag starts to migrate back toward the Ag anode and oxidize from the filament when a negative voltage is introduced. As soon as a gap develops in the filament, the current immediately decreases and Ag no longer connects the electrodes, i.e., process (C). The majority of the silver returns to the anode when the voltage is increased more negatively, and the device is completely erased as illustrated in (D). The device can function as memory because the resistance of the erased state is typically many orders of magnitude higher than the resistance of the written state.

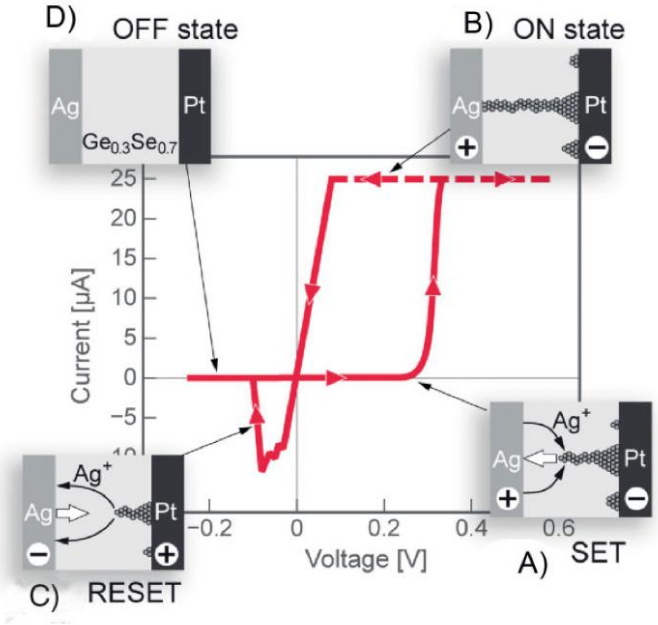

Figure 1.5. Schematic of operation of CBRAM device (A) SET process and (B) CBRAM device is in ON state. (C) RESET process and (D) CBRAM device is in OFF state [14].

1.3 Figures of Merit for Resistive Switching

1.3.1 Retention

"Retention" is the length of time a memory device can hold its programmed resistance state at a particular temperature. For applications involving nonvolatile memory, it is especially crucial. Nonvolatile memory must be retained for a minimum of ten years at a temperature of 85 °C. Retention is typically tested at high stress temperatures in order to be completed within a reasonable amount of time and to extract the activation energy for ion motion in the device because the degradation time complies with the Arrhenius dependence on temperature.

Electronic memristors have relatively shorter retention times than filament-based memristors, which generally have longer retention times [15]. The following describes one of the potential explanations. The modulation of the electron barrier height caused by trapped charge is what causes an electronic device to switch. When temperatures are the same, charge carriers can trap and detrap electrons more easily than migrating ions [16]. As shown in Figure 1.6, unintentional migration of oxygen or metal ions is the cause of the retention failure in filament-based memristors [17]. The device could stop maintaining its LRS if oxygen vacancies or metal ions move from the filament site to another location. When testing temperature is raised, it has been noticed that LRS failure typically occurs before HRS failure, indicating that LRS retention is typically a more delicate issue [18]. Limiting ion migration during

retention tests is one of the common ways to extend retention time in a filament-based memristor. In HfO_2-based RRAM, an improvement in retention had been made after the addition of a Hf capping layer. The additional capping layer slows down the recombination process and lowers the amount of oxygen that is available [19].

It is important to keep in mind that decreasing ion mobility could result in SET/RESET failure or a rise in switching energy. For particular applications, a trade-off between retention and endurance must be made. Additionally, varying electrical conditions can boost some performance parameters while making others worse. Based on the needs of the application, it is crucial to optimize both parameters in a balanced manner [20].

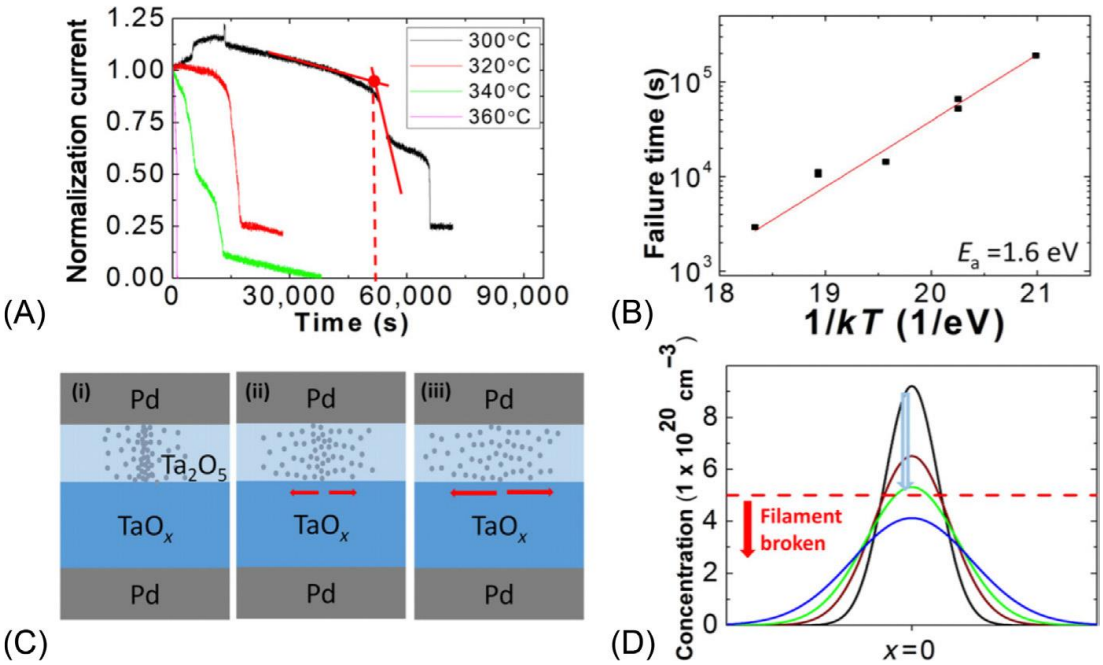

Figure 1.6. (A) $Pd/Ta_2O_5/TaO_x/Pd$ memristor retention at 300°C, 320°C, 340°C, and 360°C. (B) Fitted temperature dependence of the characteristic retention failure time following Arrhenius law. (C) Diagram showing the distribution of oxygen vacancies at the LRS (i), after they diffused (ii), and the filament ruptured (iii). (D) A time-dependent prediction of the profile of vacancy concentration. [17]

1.3.2 Uniformity

The uniformity of a memristor is another important indicator of its quality. How easily a memristor can be integrated into a large-scale, multipurpose circuit will depend on the uniformity of operating voltage, speed, resistance in HRS and LRS, and a few other parameters. Cycle-to-cycle variation can result from a variety of factors, such as randomness in ion migration, gradual changes in the morphology of a filament or switching interface, current overshoot, and more. The limitations of fabrication conditions can also lead to variation between devices.

The uniformity issue has been solved using a dual approach. One is electrical operation-oriented, while the other is material-oriented. To make the filament easier to rupture or restore under a reasonable amplitude of applied voltages, one idea for the material-oriented method is to use doping methods to lower the formation energy and the migration barrier of oxygen vacancies [21]. Depositing a capping layer between the electrode and the resistive switching layer is another successful strategy. The capping layer's duties may vary depending on the material stack. A GST ($Ge_2Sb_2Te_5$) layer was added by Lv et al. to a Cu_xO-based memristor [22]. As part of the forming process, a conductive path is created in the GST layer, and the filament is typically contained within a small area. Buffer oxide layers with high oxygen migration barriers were used by Yu et al. to prevent the filament from easily rupturing. The over-RESET issue can be reduced with the help of the buffer layer: the filament is typically partially ruptured during reset, leaving a small gap; however, if an excessive voltage is applied, the gap enlarges. This makes the HRS more uniform [23].

Electrical-oriented approaches can improve uniformity in a different way. Generally, the voltage used to power the device must be carefully balanced. A voltage that is too low could result in a weak or unstable filament, while a voltage that is too high might produce unwanted filaments and excessive Joule heating. The uniformity may also be impacted by electrical stimuli. In a previous study, current sweeping mode showed greater uniformity than voltage sweeping mode. This might be due to the fact that current sweeping could stop the growth of new filaments after the device has been SET [24].

1.3.3 Endurance

The "endurance" of a device refers to how many times it can be programmed and erased before failing. The durability of a device can be impacted by a variety of factors. The components of the memristor and the electrical operation schemes are the main determinants. When a device is switched on and off repeatedly, the switching material at the device's active region undergoes an irreversible change, which causes the device to become stuck in either its HRS or LRS state.

Three primary mechanisms of endurance degradation in TMO-based VCM RRAM were discussed in a study by Chen et al [25]. According to one of the proposed theories, oxygen vacancies can interact with an electrode to form a metal oxide layer, which creates a highly resistive area and prevents the device from performing a successful SET. According to the second proposed states, an excessive amount of oxygen vacancies may cause the filament to become too thick to rupture,

resulting in a RESET failure. In line with the proposed hypothesis, oxygen species have a tendency to move away from the filament site as a result of the combined effects of a continuously applied electric field and joule heating. As a result, there is also a RESET failure because there is not enough oxygen available to recombine with the oxygen vacancies.

In most cases, the reason for endurance degradation in CBRAM is the change in the distribution of metal. The material evolution following repeated SET and RESET is depicted in Figure 1.7 [26]. In the CBRAM device, a layer of HfO_x is sandwiched between the active electrode (Cu) and bottom electrode (Pt). The device switches for a specific number of cycles, and then according to TEM observations and energy dispersive X-ray spectroscopy (EDS) characterizations, Cu accumulates on the Pt electrode. As a result, the space between the electrode and the filament edge gets smaller and is easier for electron tunneling; this keeps the device stuck in the ON state.

The valence change type memristor has the best endurance performance, according to the 2015 International Technology Roadmap for Semiconductors (ITRS). A thermodynamically stable filament is a crucial requirement for the high endurance. For example, in TaO_x, even at high temperatures, the conductive Ta filament will not react with Ta_2O_5 [27]. Similar to the Hf-O system, which only permits two thermodynamically stable phases within the operating temperature range inside the device, the HfO_x-based memristor has also demonstrated high endurance [28].

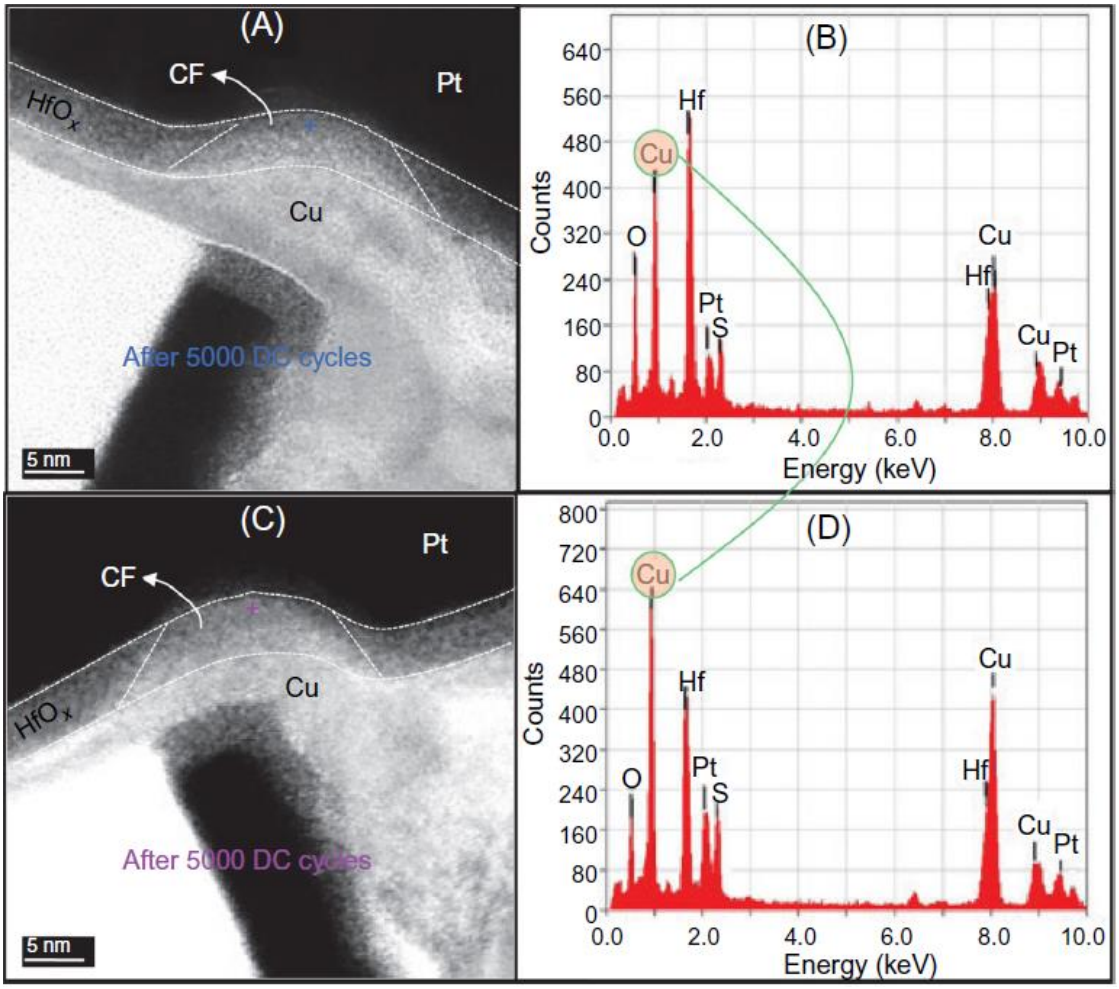

Figure 1.7. (A) TEM image of switching region after 500 cycles of current sweeping. (B) EDS profile of the switching region after 500 cycles of current sweeping. (C) TEM image of switching region after 5000 cycles of current sweeping. (D) EDS profile of the switching region after 5000 cycles of current sweeping. [26]

1.3.4 Switching speed

The reading and writing speed of a memory is one of its most significant performances. FLASH memory is slower than static random-access memory (SRAM) because the floating gate must be slowly charged via electron tunneling across a substantial

electronic barrier. SRAM is expensive and has a large area footprint even though it is much faster. However, memristors have demonstrated sub-100 ps switching [29], which is more than adequate for the majority of anticipated applications in the near future.

Memristors' switching mechanism and, consequently, the elements that affect how quickly they switch are up for debate, however, there are some known contributing factors; the mobility of mobile ions is one of them. As discussed in Section 1.2, the majority of resistive switching is related to the migration of oxygen (or nitrogen) anions or metal cations where Equation 2.1 and 2.2 can be used to explain the ion migration. Driven by electric force under an electric field, the ions can cross the energy barrier and move to the next nearby site that is most energy-beneficial if the electric force is strong enough, and the mobility of the ions can be exponentially increased in a strong electric field. Thus, the ion transport process is influenced by both the materials chosen and the applied voltage. A complex relationship exists between temperature and the switching process, both in terms of ion migration and the formation of chemical bonds. Although it is generally true that a device can switch exponentially faster when a higher voltage is applied [30], this process may have unfavorable effects on the device's reliability and power consumption.

Encouraging speed performances has been reported recently by Choi et al as shown in Figure 1.8, where 85 ps switching in a TiN/AlN/Pt device was achieved [29]. The zoomed-in image of the switching pulses is shown in the insets to Figure 1.8 (A) and (B). In this study, the migration species is nitride vacancies rather than oxygen vacancies. The justification for this decision is that +3 valence nitride vacancies, as

opposed to +2 valence oxygen vacancies, may be subjected to a stronger electric force. Pickett et al. noted in a previous paper that the switching site is located in a very small volume of the dielectric. Sub-nanosecond switching is produced by phase change brought on by joule heating [31]. A longer switching time is also a result of the fact that CBRAM switching involves a number of processes, such as oxidation, ion transport, attaching ions to the other electrode, detaching ions from one electrode, and reduction. However, as shown experimentally [32], such switching can still happen in nanoseconds.

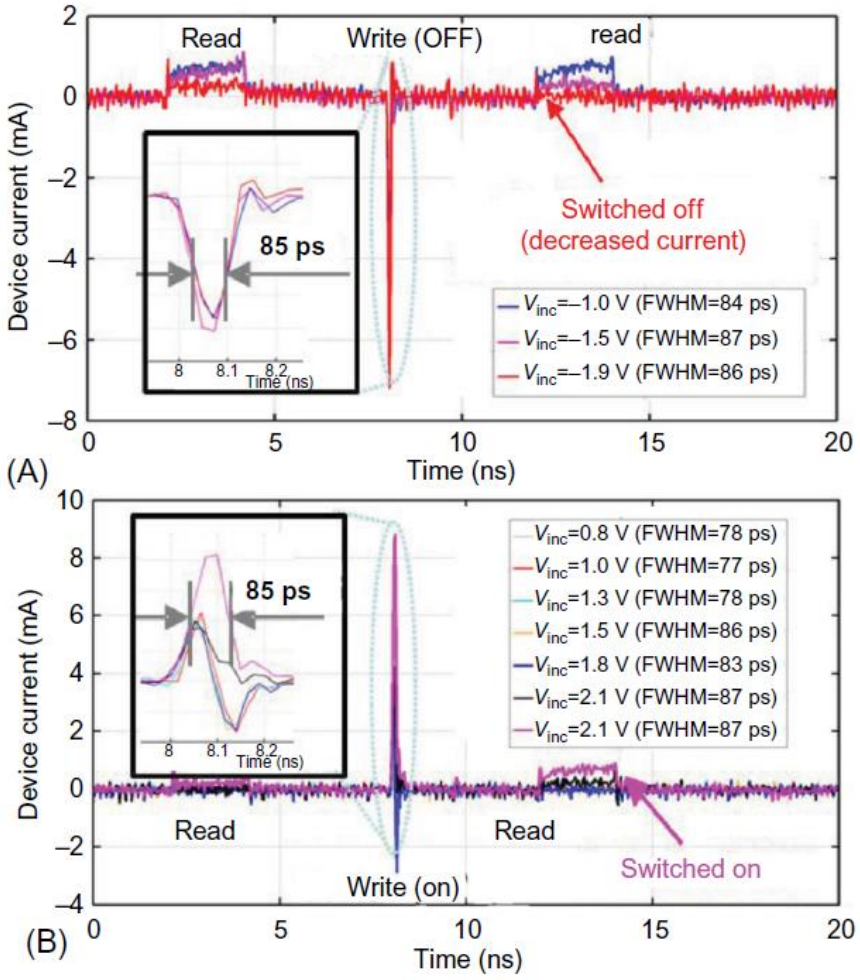

Figure 1.8. (A) 85-ps voltage pulse OFF switching. (B) 85-ps voltage pulse ON switching. [29]

1.4 Applications of memristive device

Beyond memristive properties, memristors also have inherent analog characteristics [33], so they can be used as the basic building blocks of a wide variety of networks by taking advantage of their rich properties. Spiking neural networks require more complex memristor dynamics and threshold switching to operate than artificial neural networks or level-based computing, which heavily depends on precise tuning of weights or conductance. This section reviews the community's efforts to create effective neuromorphic systems using memristors. The discussion is divided into two parts, starting with a more accurate replication of biological systems, namely the bio inspired approach and the adaptable computation-oriented approach, namely neural networks.

1.4.1 Bio-inspired approach

Chemical synapses function as junctions between neurons and can modify the transmission of neural signals through their synaptic weights, which can be modified through processes known as "plasticity." Synaptic functions have long been implemented using transistors [33]–[39]. Due to their simplicity and efficiency in terms of power consumption [40]–[48], two-terminal circuit components like memristors have recently been used for this purpose in neuromorphic architectures

[49]–[51].

The realization of neuronal functions such as short-term synaptic plasticity (STP) [40], [47], short-term plasticity to long-term plasticity transition (LTP) [42], [46], [52], and spike-timing-dependent plasticity (STDP) [42], [46] has been reported to involve the volatility of resistive switching in Ag-based ECM threshold switches. A Pt/Vac/Ag_2S/Ag system was reported to be short-term facilitated by Ohno et al. A biological synapse's short-term facilitation of transmission weight relaxation was mimicked by the system's high conductance upon stimulation of each input pulse (80 mV/0.5 s) and decay to the low conductance state during a relatively long (e.g., 20 s) interval between pulses [42] as shown in Figure 1.9 (A). Ohno et al. discovered long-term facilitation, or persistent conductance increment, in the Pt/Vac/Ag_2S/Ag system as shown in Figure 1.9 (B). After seven spikes using an increased stimulation frequency which is 2 second elapsed times between each pulse. According to Wang et al., similar Ag dynamics in a Pt/SiO_xN_y:Ag/Pt threshold switch led to both short-term facilitation and depression depending on the time interval between spikes (denoted as t_{zero}), sharing strong analogy with the Ca^{2+} dynamics of chemical synapses as shown in Figure 1.9 (C). Low-frequency stimulation resulted in a slower conductance increase or even a decrease (short-term depression) from the same initial conductance, whereas high-frequency stimulation increased the threshold switch's conductance from its initial ON state conductance [53]. Another crucial characteristic of chemical synapses is that they undergo a transition from early facilitation to eventual depression during high-frequency stimulation [54]–[56], which is shown in Figure 1.9 (D) [53]. This transition is caused by prolonged or excessive electrical spikes. When low-

frequency (196 Hz) spikes were applied to the device, it initially displayed depression. This was followed by facilitation at 5000 Hz simulation, which turned depression into depression with subsequent low-frequency (196 Hz) pulses, which eventually restored the device's initial ON state conductance [53], as shown in Figure 1.9 (D).

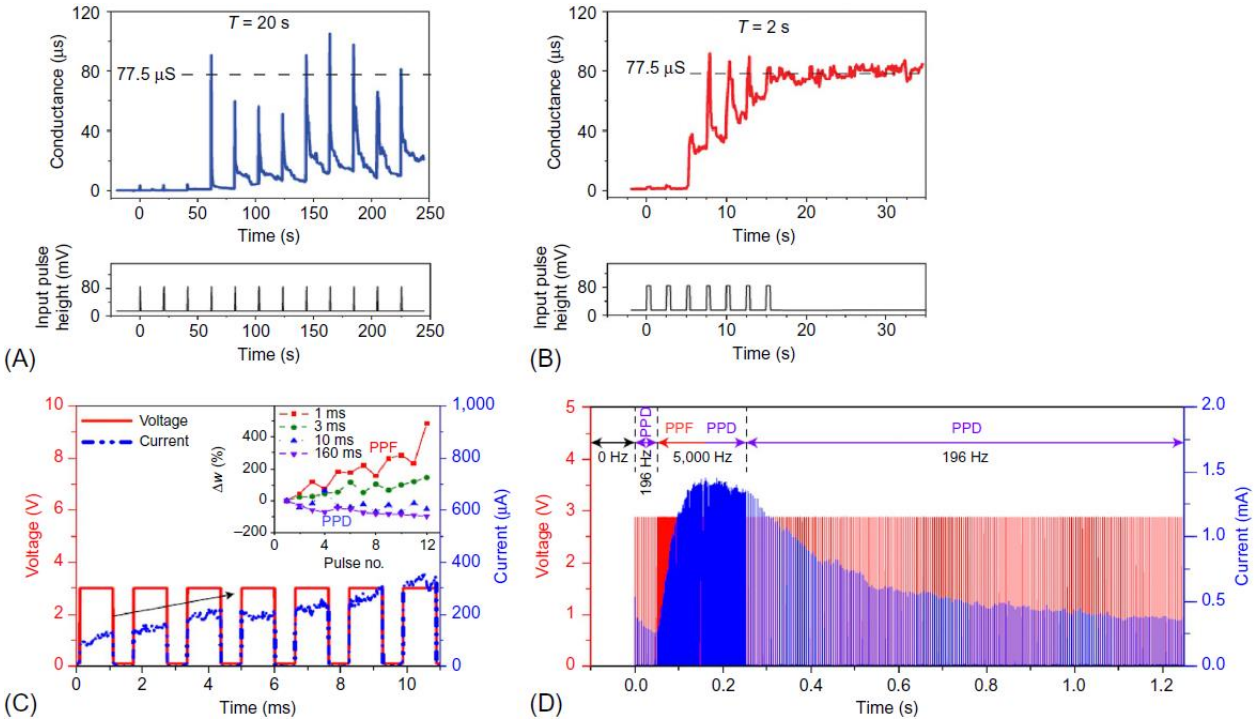

Figure 1.9. Synaptic applications with threshold switches. (A) short-term facilitation and (B) long-term facilitation of a Pt/Vac/Ag_2S/Ag system. (C) Short-term facilitation and depression of a Pt/SiO_xN_y:Ag/Pt threshold switch. (D) Long-term spike-rate-dependent potentiation (SRDP)and bio-realistic spike-timing-dependent plasticity (true STDP) behavior of a combined device consisting of a diffusive and a drift memristor. [42]

The Pt/SiO_xN_y:Ag/Pt threshold switch was able to demonstrate LTP-based [57] learning protocols, including the spike-rate-dependent potentiation [58] and STDP [56], [59], [60], as shown in Figure 1.10 (A), when paired with a nonvolatile Pt/TaO_x/Ta/Pt drift memristor. As exhibited in Figure 1.10 (B), Wang et al. revealed the rate-dependent potentiation in which the drift memristor weight (resistance)

variation was a function of the applied pulse frequency [53]. Insufficient time was allowed for the Pt/SiO_xN_y:Ag/Pt threshold switch to relax back to its HRS due to a higher frequency or shorter t_{zero}. According to the voltage division between the drift and diffusive memristors, a greater voltage would drop across the drift memristor as a result. In the drift memristor, this led to a bigger resistance change that was similar to the LTP. Moreover, a longer t_{zero} and a lower stimulation spike frequency gave the threshold switch enough time to return to its HRS, which resulted in a smaller voltage drop across the drift memristor and insignificant resistance change of the drift memristor [53].

Wang *et al*. used nonoverlapping electrical pulses to similarly illustrate the STDP learning rule on the combined device in Figure 1.10 (C). For the integrated device, an intrinsic timing mechanism was provided by the synaptic dynamics of the threshold switch. The initial spike turned on the threshold switch and started the timer without impacting the drift memristors [53]. The diffusive memristor's resistance gradually began to return, acting as a timed switch [53]. The time (Δt) between two pulses determined whether or not the second spike could program the drift memristor [53]. As illustrated in Figure 1.10 (D), a smaller diffusive memristor resistance and a greater resistance change in the drift memristor correlate to a narrower interval t, and vice versa [53]. The drift memristor was SET by the post-spike (i.e., potentiation) if the pre-spike appeared before the post-spike [53]. Depression would result if the pre-spike came after the post-spike because the pre-spike RESET the drift memristor, which spontaneously complied with the STDP rule seen in chemical synapses [53] without the use of artificially created overlapping spikes.

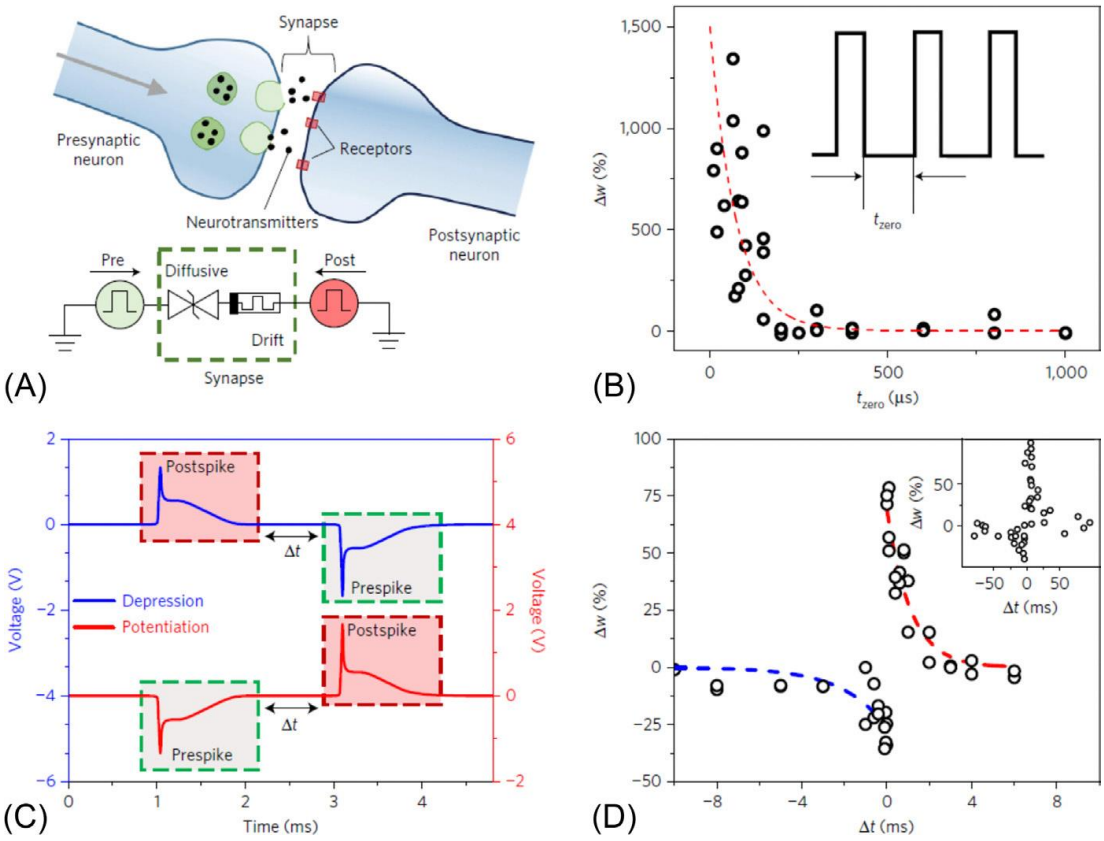

Figure 1.10. (A) Illustration of a biological synaptic junction and a circuit diagram of the electronic counterpart consisting of a memristor. (B) Spike-rate-dependent potentiation of the combined device in (A). (C) Schematic representation of the pulses applied to the combined device in (A) for STDP demonstration. (D) STDP of the combined device in (A). [53]

1.4.2 Neural networks

Human's nerve system and brain are made up of complex networks of synaptically coupled nerve cells, or neurons, which are connected to each another. In an effort to compute similarly to the nervous system, neural networks have been developed using a sophisticated network of interconnected artificial neurons (or nodes). Artificial synapses can be given a weight to modify the strength of an input received by a neuron

being connected to other neurons, [61]so that the incoming stimulus may be processed and an appropriate output can be produced. In order to facilitate data processing, neural networks are typically arranged into layers, such as an input layer, intermediate hidden layers, and an output layer. There have been numerous attempts recently to use memristive device arrays to create neural networks. Some recent developments in this area are introduced in this section.

- Pattern classification using passive memristor array

The first single perceptron in a passive memristor crossbar array was recently demonstrated by researchers at UCSB [47]. As shown in Figure 1.11 (A) and (B), they created an integrated 12 x 12 arrays of memristors with Al_2O_3 and TiO_{2-x} bilayers, where the current-voltage characteristics of those memristors were uniform enough. A single layer classifier with 10 inputs and 3 outputs that are fully coupled with 30 synaptic weights was implemented using the crossbar, as shown in Figure 1.11 (C). Figure 1.11 (D) illustrates the classification of three classes of 3 x 3 pixel black and white images using this network, where the nine network inputs, each corresponds to a pixel value, representing the images. As shown in Figure 1.11 (E), these patterns feature the letters z, v, and n as well as three sets of nine noisier variations of each letter that are produced by inverting one of the pixels in the original image.

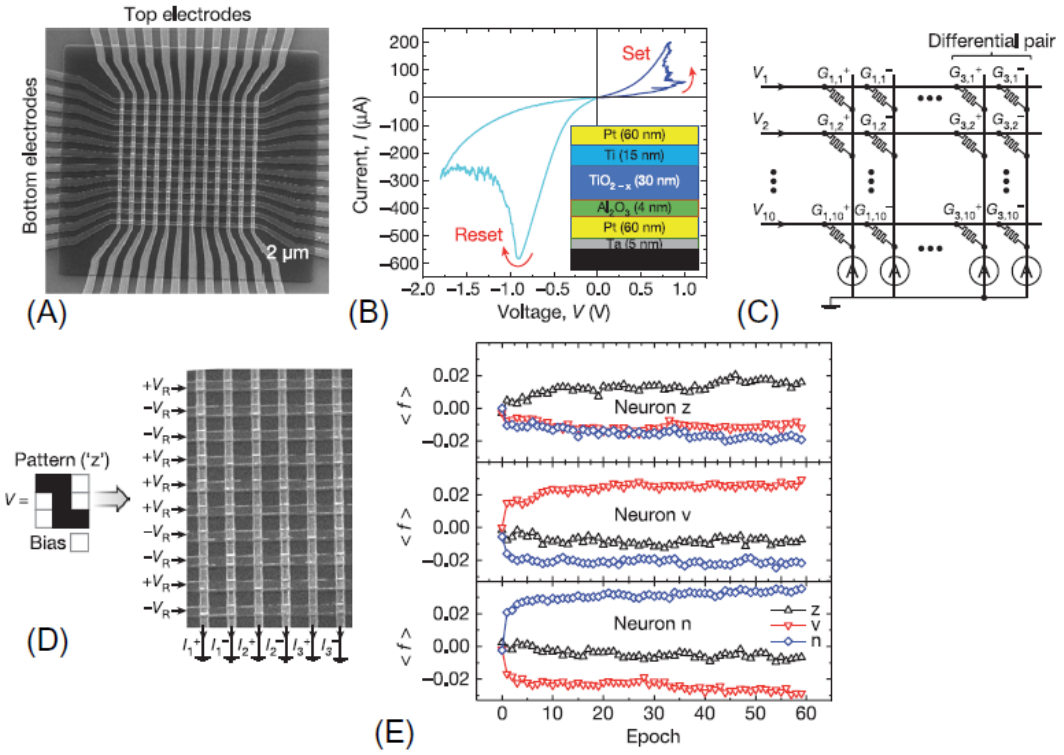

Figure 1.11. (A) Integrated 12 x 12 crossbar with an Al_2O_3/TiO_{2-x} memristor at each cross point. (B) A typical current-voltage curve of a formed memristor. (C) An implementation of a single-layer perceptron using a 10 x 6 fragment of the memristive crossbar. (D) An example of the classification operation for a specific input pattern with the crossbar input signals equal to $+V_R$ or $-V_R$, depending on the pixel color. (E) The evolution of output signals, averaged over all patterns of a specific class. [47]

- Fully memristive neural network

In comparison to conventional computational methods, artificial neurons and synapses may open the way for a more effective implementation of neural network algorithms. Using conventional CMOS-based hardware, there were various attempts at neuromorphic computing [62], [63]. Despite being effective at performing complex cognitive applications, they have had a very poor power consumption efficiency. For neuromorphic computing, searching for alternative technologies like memristors is the way to go.

There were some reports of memristor-based artificial neurons, but they had nothing in the way of bio-realistic dynamics and didn't interact directly with the fabricated synapses in an integrated system [64]–[67]. Recently, Wang et al. [68] built neural emulators that can demonstrate stochastic leaky integrate and fire dynamics with an adjustable integration time using Ag-based diffusive memristors. The authors then combined these neurons with non-volatile memristive synapses to create an artificial neural network that is entirely memristive. Using the aforementioned integrated system, the results showed unsupervised learning.

A diffusive memristor neuron, as seen in Figure 1.12 (A), has physically and functionally imitated a real neuron. Figure 1.12 (B)-(E) contrasts the results of physics-based simulations with experimentally obtained data. By giving the artificial neuron a single super-threshold voltage pulse followed by a series of low-voltage pulses, the temporal behavior of the cell was studied. The rise of a distinct delay period (τ_d) between the entry of the voltage pulse and the rise of the output current was caused by the interaction of the circuit's RC time constant and the internal Ag dynamics of the memristor. The RC time constant, which predominates the delay time when a large circuit capacitance is selected, is also high. As illustrated in Figure 1.12, as the capacitance decreases, the RC time shortens as well as the internal Ag dynamics of the memristor take control of the delay time and subsequent integrate-and-fire behavior.

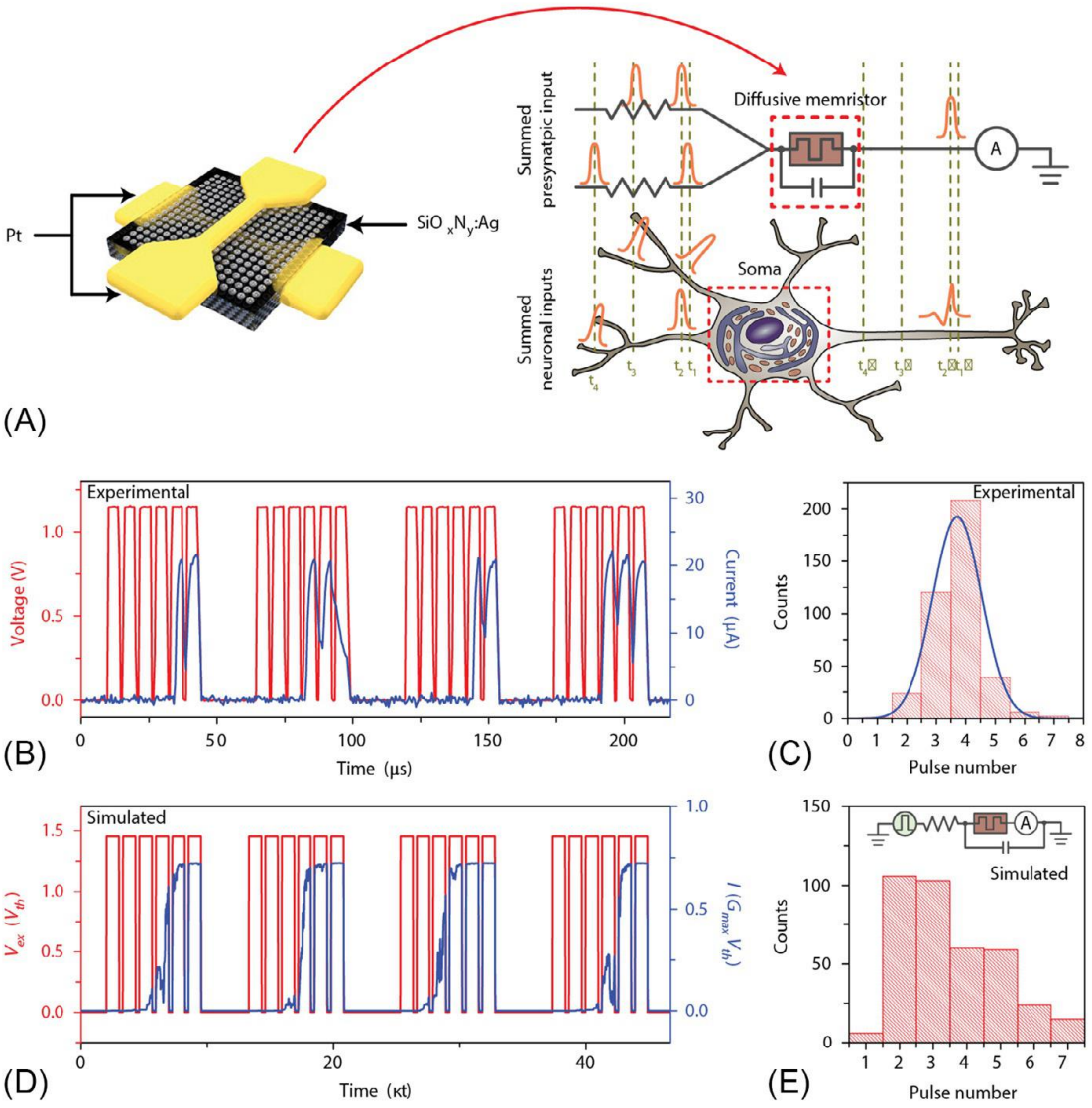

Figure 1.12. Diffusive memristor artificial neuron. (A) A cross point diffusive memristor is shown schematically as a SiO_xN_y:Ag layer sandwiched between two Pt electrodes. Presynaptic inputs are delivered to the artificial neuron by a pulsed voltage source and an analogous synaptic resistor, which are then software-summed. (B) Experimental behavior of the system in the presence of several subthreshold voltage pulses, followed by a 200μs rest time (C) A comparison between a Gaussian distribution in blue line and a histogram of the numbers of subthreshold voltage spikes in red color needed to successfully fire an artificial neuron (D) Simulation of the device's reaction to several subthreshold voltage pulses. (E) Switching statistics were simulated with respect to pulse counts. [68]

1.5 Motivation of this work

Recently, it was found that, beyond those active metals, semiconductors can be used as a buffer layer between the metal electrode and the insulating layer in the memory devices, leading to interesting switching performance [36], [48], [69]–[72]. The performance of such complicated heterostructures may significantly change the memory characteristics such as operation voltage, resistance ratio, and multilevel storage performance etc., especially when choosing unconventional materials such as perovskite oxides $SrTiO_3$ (STO) and $BaTiO_3$ (BTO) as switching layers [73]–[78].

STO is a potential candidate for next generation of high-*k* gate dielectric materials due to its large dielectric constant, low dielectric loss and potentially ferroelectricity under strain [79]–[81]. For RRAMs with STO thin films epitaxially grown on silicon, or a heterostructure of doped STO films on Nb-doped STO substrate, their resistance on/off ratios are only in the range between 1 and 100 [74]. These low resistance ratios may be increased by stacking with a semiconducting buffer layer forming a heterojunction structure. A heterostructure may also make the device achieve a much higher resistance ratio and even multilevel resistive switching.

In order to explore the switching mechanism and induce multilevel resistance states in the STO thin film-based device stacking with other semiconductor materials and different top electrodes, in this work, we study a SnSe/STO heterostructure-based memristor devices where the SnSe thin film is constructed in the metal-insulator-metal (MIM) sandwich structures with Ag and Cu as top electrodes.

1.6 Scope of the thesis

We are using pulsed laser deposition technique to fabricate polycrystalline SnSe and STO thin films, characterization of the films is also conducted. In chapter 1, we introduce the background and recent studies of memristor. In chapter 2, the instrumentation and experimental methods on growing thin films are described. Methods involved in structural and electrical characterizations of thin films are also introduced. Chapter 3 presents the results and discussion of polycrystalline SnSe thin films device in fabrication and electrical characterization. Results and discussions of SnSe/STO heterostructure in electrical characterization and the density-function theory (DFT) calculations are covered in chapter 4. Finally, a brief conclusion and possible further works are given in chapter 5.

Chapter 2 Introduction of Experimental Methods

2.1 Thin films deposition

A thin film is a layer of solid material that is adhered to a solid support, also known as a substrate. Surface and interface characteristics have a significant impact on thin film properties, so the thin film may experience stress due to the lattice mismatch and the difference in thermal expansion between the thin film and substrate. Throughout the deposition process, a thin film material usually goes through three phases: emission of species such as atoms, ions, and clusters from the source; transit through the vacuum chamber; and condensation on the substrate. Figure 2.1 depicts the schematic creation of a thin film. When the material loses enough kinetic energy provided by the emission process, it impinges on the surface of the substrate and adheres there. Adatoms are the particles that have been adsorbed on the surface of the substrate. Since the adatoms are indeed thermodynamically unstable at this point, they tend to desorb and migrate over the surface until they come into contact with one another and interact to create a bigger cluster. Because the clusters are less mobile, they stay where they are produced, interact with moving adatoms, and eventually develop into a sizable island. As the islands expand, they merge together to form a thin film.

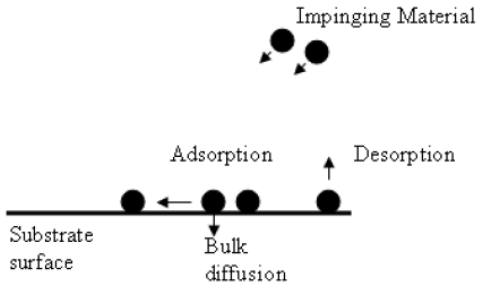

Figure 2.1. Formation of a thin film.

2.1.1 Pulsed laser deposition (PLD)

PLD is a method frequently used to deposit high-quality thin films. During laser ablation process, a target is initially hit by high-energy laser pulses causing the atoms on the target surface to vaporize. There are several ablation processes working in PLD, including thermal, mechanical, and electrical excitations, each of them creates a unique energy species, such as atoms, ions, clusters, and particulates. Together, those ablated atoms migrate to the substrate and create a glowing plasma known as a plume. When the energetic species reach the substrate, they collide with it, condense on the surface, and promote the formation of the film. Nucleation and thin film growth mechanisms may be divided into three categories. They result from the interaction of several factors, including substrate temperature, species density and energy, physical-chemical characteristics of the substrates, etc.: (1) Two-dimensional complete monolayer growth with three-dimensional islands growth (Frank-van der Merwe). (2) Three-dimensional island growth (Volmer-Weber). (3) Two-dimensional full monolayer growth (Stransk-Kastinov) [82], [83].

The PLD technique's primary benefit is the strong stoichiometric control, which is challenging to obtain using conventional deposition techniques. All of the constituents of the target surface can be vaporized using a high-energy laser as an excitation source, making it possible to produce thin films of any material in theory. Additionally, in-situ development of composites or multilayers made of various materials is possible under various ambient gas conditions by utilizing flanges that can handle several targets. PLD does have some drawbacks, though. Due to the problem of uneven film thickness, there are restrictions on the size of the substrate that may be employed. The film thickness is largest just under the plume's core and progressively gets thinner as you get further away from it. The deposition region is constrained to around 1 cm^2 just underneath the plume's center in order to produce a thin sheet that is comparatively uniform. One further significant issue with PLD is the production of particles. Due to the high laser power, all species, as well as contaminants and big particles, are deposited onto the substrate, which causes the formed films to have a rough surface.

2.1.2 Thin film deposition process by PLD

The design of the PLD system utilized in the research is shown in Figure 2.2. A pressure sensor, rotary pump, fused-silica glass window, substrate and target holders are all installed to the vacuum chamber. Substrates were cleaned with acetone and ethanol in succession in an ultrasonic bath for at least five minutes prior to the thin film deposition procedure. Targets were mechanically fixed onto target holders, and

after pre-ablation to remove surface imperfections, the targets are ablated by the pulsed laser. Usually, silver paint was used to attach the cleaned substrates to the substrate holder. The chamber was pumped for at least 30 minutes in order to reach a base pressure of 0.01 Pa or lower. The substrate holder was then heated to the necessary temperature, and once the substrate temperature was attained, oxygen gas was introduced into the chamber. The distance between the substrate and the target, the temperature of the substrate and the laser power should be well controlled since they all have a big impact on PLD deposition rate and film quality.

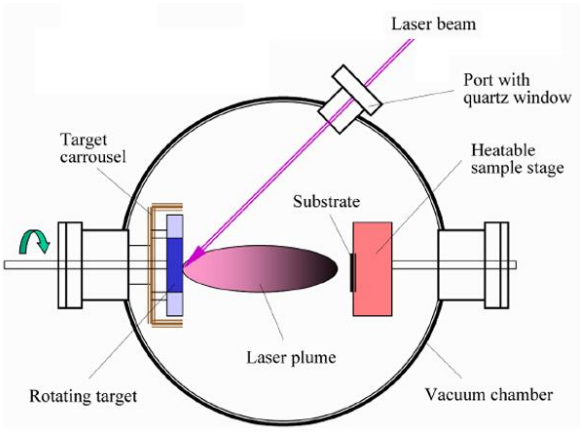

Figure 2.2. Schematic showing the setup of pulsed laser deposition.

2.1.3 Magnetron sputtering

The memory devices are required to have top and bottom electrodes which are deposited by sputter deposition. As illustrated in Figure 2.3, the intense argon (Ar) ions bombard the target and cause the target atoms to be expelled by transferring their kinetic energies and momentum to the target atoms during the bombardment. When these atoms condense on the substrate, they create a thin layer. This method

keeps the concentration of Ar ions in the plasma by venting the chamber with Ar gas. The concentration and energy of the gas ions, the distance between the target and substrate, and the intensity of the electric field are factors that impact the yield of sputtering.

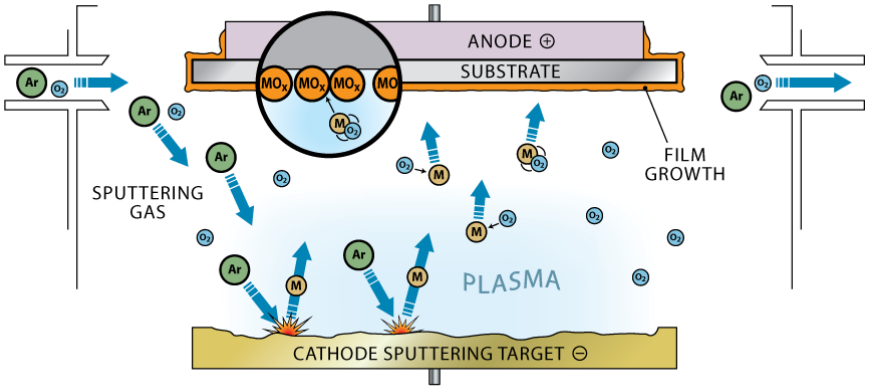

Figure 2.3. Schematic showing the process of sputtering.

2.2 Structural characteristics of the thin films

2.2.1 X-ray diffraction (XRD)

Characterizing the crystal structure of bulk and thin film materials using XRD is a non-destructive approach. When an X-ray beam incident into a crystal, it will be diffracted by the crystal lattice. According to Bragg's law, constructive interference occurs with crystal planes at specific incidence angles θ:

$$2d \sin\theta = n\lambda, \quad n = 1,2,\ldots \tag{2.1}$$

where d is the distance between the atomic planes, θ is the angle of the incident beam,

and λ is the wavelength of the X-ray source, if known, it is possible to compute the lattice parameters of unit cells a, b, and c from the peaks seen in the diffraction pattern. A Rigaku SmartLab x-ray diffractometer was employed in this experiment. There were three primary types of measurements: the phi- (ϕ) scan, the rocking curve (ω-scan), and the θ-2θ scan. Utilized was Cu $K_{\alpha 1}$ X-ray radiation with λ = 1.541Å.

First, θ-2θ scans were carried out, in which a 2:1 angular speed ratio was used to spin both the detector and the sample. By applying the Bragg's equation to the θ-2θ scan, the out-of-plane lattice parameters can be calculated. After that, measurements of the rocking curve were used to determine the film's crystallinity level. During the rocking curve measurement, the sample was rotated (or rocked) around the ω-axis while the X-ray source and detector were fixed for a certain angle proportional to the atomic plane spacing. The full width at half-maximum (FWHM), a measurement of the distribution of crystallite alignment, can be found in a peak, and a smaller FWHM is an indication of preferential alignment of crystallites in a certain direction. The ϕ scan was carried out in order to figure out the epitaxial relationship between the thin film and the substrate. The detector was positioned such that it could detect the thin film's reflection signals coming from a certain plane. In order to quantify the matching peak, the sample was additionally tilted at a comparable angle across the x-axis. This was followed by scanning along the ϕ-axis. Figure 2.4 displays a schematic of the X-ray measuring geometry.

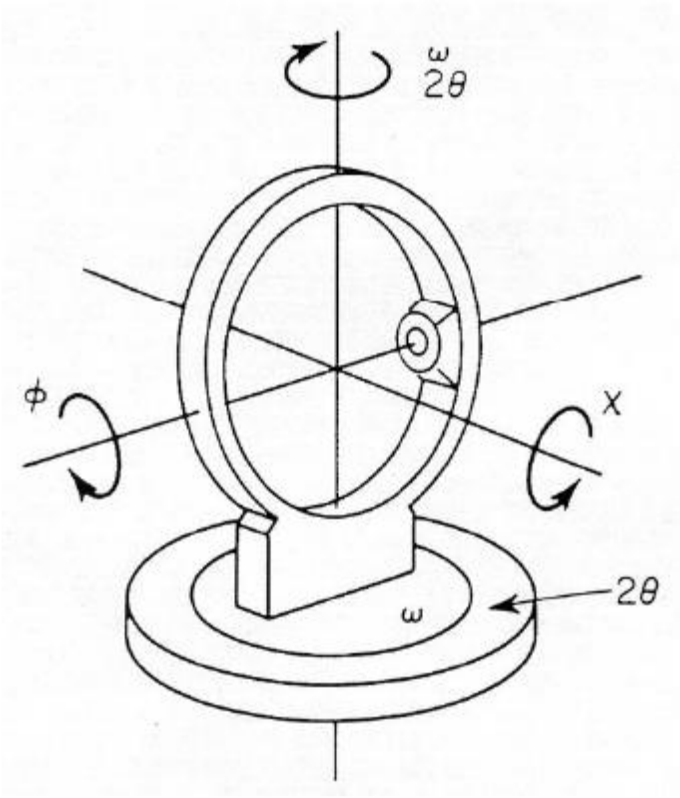

Figure 2.4. Schematic of four axis X-ray diffractometer geometry.

2.2.2 Scanning electron microscopy (SEM) and energy dispersive X-ray (EDX) spectroscopy

Thickness and surface quality of thin films can be measured using a SEM. In a SEM, an electron beam is launched, accelerated and concentrated by electromagnetic lenses. Inelastic electron scattering occurs when electrons incident to a sample's surface, and secondary electrons, backscattered electrons, Auger electrons, cathodoluminescence, and X-rays can be produced as a result of the interaction between the electron beam and the sample. By accumulating the secondary electrons released from the sample's exposed positions, the SEM obtains its images. Additionally, EDX are frequently

included in SEM systems which can be utilized to characterize chemical composition. The experiment employed EDX to describe the thin films' chemical composition.

2.2.3 Transmission Electron Microscopy (TEM)

Transmission electron microscopy (TEM), as opposed to optical microscopy, uses an electron beam instead of a light beam that is pointed at the object. An extremely high voltage (for instance, 200 kV) is introduced to a filament placed at the top of the device, an electron beam is fired to the sample. The electromagnetic lenses employed in the microscope are used to focus the electron beam on a specific area. In this study, the structural information of thin film samples is examined using a scanning transmission electron microscope (STEM), model number Jeol JEM-2100F.

2.2.4 Sample preparation using grinding tool and ion milling for TEM

The procedures in preparing thin film cross-section samples are as follow (Steps 3-5 only for plane-view):

1. Using an appropriate amount of M-bond, adhere the sample to a clean substrate face to face as indicated in figure 2.5.
2. Wax the sample and attach it to the grinding tool. Begin grinding the sample until one side is consistent and well-polished.

3. Use M-bond to adhere the well-polished side of sample to the copper grid. For plane-view's sample, adhere the thin film side.
4. Wax is used to adhere the sample to the grinding tool. Sandpaper and diamond past are then used to mechanically grind the specimen till $t < 20\mu m$, after which it is polished using polishing paper.
5. Argon ions are frequently employed in ion milling, which is accelerated by 3 to 6 kV and mills out the atom in the specimen as illustrated in figure 2.6, to further thin the specimen.

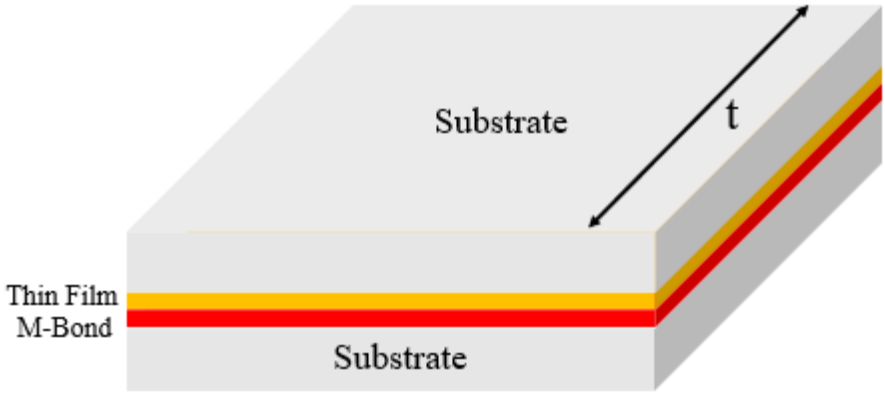

Figure 2.5. Schematic representation of a TEM sample in cross-section.

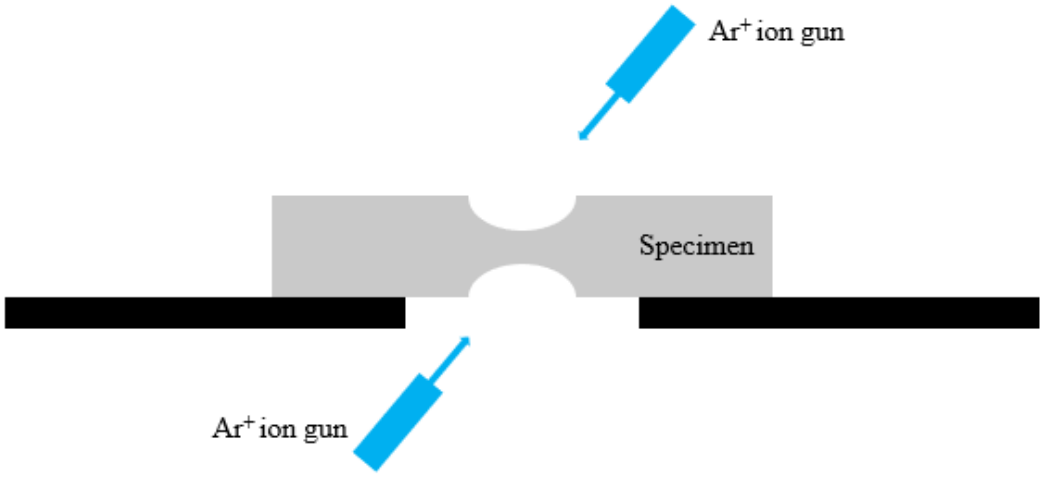

Figure 2.6. Diagram of an ion milling schematic.

2.3 Electrical characterizations

The resistance of the sample is normally measured using a two-point system. Figure 2.7 displays a schematic representation of the experimental setup. The simplest method for measuring resistance is a two-point measurement, which can be done regardless of the sample shape. In this work, a commercial memristor characterization platform called ArC ONE (ArC Instruments) was used to undertake electrical characterization of the memory device.

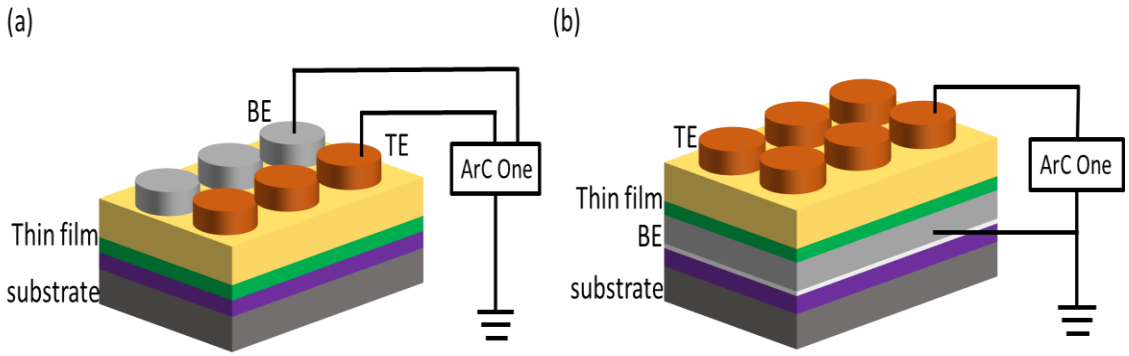

Figure 2.7. Schematics of electrical measurement configurations for measuring I-V and resistive switching characteristics by ArC ONE with (a) in-plane and (b) out-of-plane device geometry.

When a voltage is applied between the memory device's electrodes during the measurement, the current flowing through the memory device is measured, and the memory device's resistance is determined. Voltage pulses progressively increase in amplitude from 0V to V_{max} positive, then to V_{max} negative, and finally return to 0V. Since the highest currents that flow through the memory device under application of positive V_{max} and negative V_{max} are low, there is no need to apply positive and negative

current cut-off values during the electrical characterization to prevent the dielectric breakdown of the memory device. R-V characteristics and I-V characteristics are provided through electrical characterization. The switching voltage of the memory device may be determined from the R-V characteristics, as well as the value of the memory window. Both the amount of current flowing through the memory device and the switching voltage of the memory device can be determined from I-V characteristics.

A commercial memristor characterization platform called ArC ONE was also used to investigate the memory device's data retention and endurance characteristics (ArC Instruments). Pulses for writing and reading should be introduced first. Writing pulses are voltage pulses that, when applied to a memory device, causing that device's resistance to change from HRS to LRS or vice versa. In other words, the SET voltages and RESET voltages of the device are equal to or greater than the amplitude of writing pulses. Thus, the memory device's resistance state changes when a writing pulse is applied, but its value is not revealed. Reading pulses are pulses that do not alter the resistance of the memory device when applied. In other words, the SET voltages and RESET voltages of the memory device are greater than the amplitude of reading voltages. As a result, when a reading pulse is applied to a memory device, its resistance state is not altered; instead, its value is revealed. The amplitude of reading voltages typically falls between 0.01 and 0.1V.

The measurement of data retention offers information on the length of time that a memory device can keep binary data, which are represented by the memory device's resistance states either HRS or LRS. The memory device is subjected to reading pulses for a period of time with equal intervals in between after switching from HRS to LRS

or from LRS to HRS, respectively. Usually, the memory device's resistance state is read every one to ten seconds. A single writing pulse is followed by a series of reading pulses to test data retention.

The maximum number of the memory device switch between 0 and 1 is shown by the endurance measurement. In other words, it demonstrates how many successive sets and resets the memory device is capable of performing. The cycle used to test endurance includes a writing pulse to SET the memory device, a reading pulse to confirm that the SET process was successful, a writing pulse to RESET the memory device, and a reading pulse to confirm that the RESET process was successful. The memory device should be capable of doing more cycles in a row.

Figure 2.8 (A) shows the memristor characterization platform ArC ONE from ArC Instruments. As shown in Figure 2.8 (B), a memory device in crossbar array can be packaged in PLCC and used internally for electrical characterization, while individual memory devices can be used externally. In the second scenario, ArC ONE is linked to the probe station with probes and its external connections. Typically, one probe is put onto the bottom electrode for ground, with the other probe be put onto the top electrode of the sample for applying voltage bias as illustrated in Figure 2.8 (C).

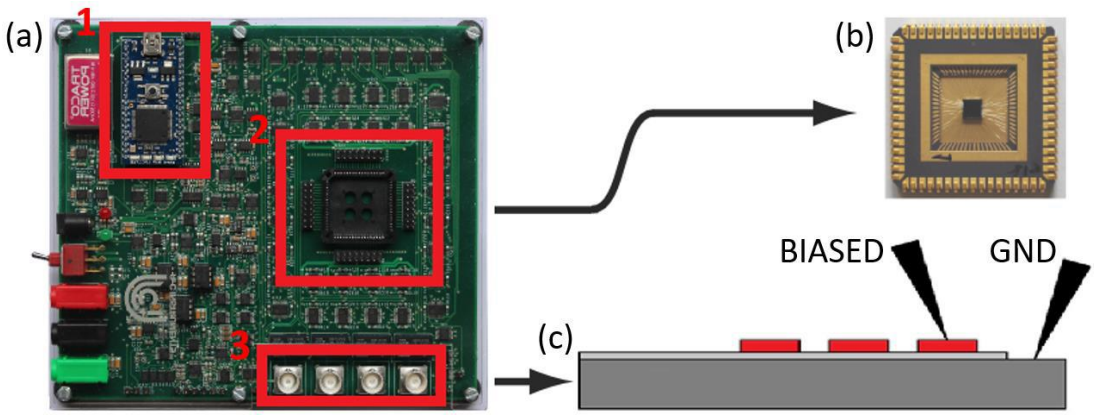

Figure 2.8. (A) Appearance of Memristor characterization platform ArC ONE from ArC Instruments where 1, 2, and 3 are labeled to the microcontroller, PLCC socket and external connections respectively. (B) Memristor devices in crossbar array packaged in PLCC chips holder. (C) Illustration of externally carried out electrical characterization of a memory device by probs.

Chapter 3 Characterization and non-volatile resistive switching behavior in SnSe-based memristor devices

Stoichiometric SnSe is a narrow band gap semiconductor at 0.9-1.3 eV, with relatively high resistance and low-density of intrinsic defects [84]. These properties may make SnSe memory device multifunctional by the integration of light sensitivity[85], [86] and ability to harvest energy from heat [87], [88]. Our previous results showed that SnSe is a good candidate for ultralow switching and multimode memristor [89]. In this work, for the first time, we demonstrate multilevel switching performance and resistive switching characteristics by inserting SnSe film on STO thin film to form a double layer heterostructure memristor device. We also study the switching mechanism and compare the performance between using Ag and Cu as active electrodes. Furthermore, multilevel storage is achieved, and its outstanding performance as a memristor device makes it a great candidate to be promoted to a practical application in neuromorphic computing.

3.1 Introduction of tin selenide (SnSe)

As illustrated in Figure 4.1, SnSe has a simple layered orthorhombic crystal structure with lattice parameters a =1.149 nm, b = 0.444 nm, and c = 0.4135 nm, while the two-

atoms-thick SnSe slabs are along their b-c plane. Although the connection between SnSe slab layers is weak along the a-axis, it is strong within the slab plane. In the severely deformed SnSe [90] coordination polyhedral, there are three short and four long Sn-Se bonds in its structure. The low-symmetry SnSe phase of the *Pnma* (#62) space group undergoes a second order displacive phase transition into the high-symmetry phase known as the *Cmcm* (#63) [91] space group until the temperature reaches 807 K, at which point the lattice will expand by 2.5%.

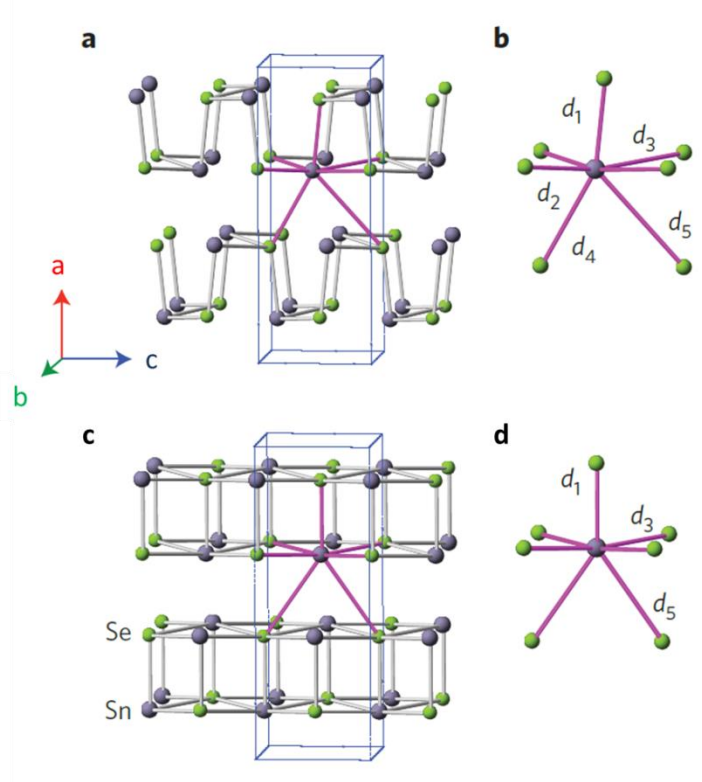

Figure 3.1. (a) Crystal structure of SnSe in *Pnma* phase space. (b) Sn coordination polyhedron corresponding to SnSe in *Pnma* phase space. (c) Crystal structure of SnSe in *Cmcm* phase space. (d) Sn coordination polyhedron corresponding to SnSe in *Cmcm* phase space. All Sn atoms are surrounded by seven Se atoms in SnSe. [91]

Moreover, the energy bandgap of SnSe is narrow as 0.86 eV, and the hole concentration of SnSe is within the range of 10^{17} – 10^{18} cm^{-3}. Room temperature

electrical resistivity of SnSe is about 10^1 – 10^5 Ωcm^{-1} with large optical absorption coefficient [92]. Due to the high optical absorption coefficient and electrical resistivity, 2D-layered SnSe structure entered to researcher's sight as a potential candidate of memristor recently. SnSe has been studied for applications in thermoelectric devices, supercapacitors and photo detectors [93]–[97]. Stoichiometric SnSe has a low density of intrinsic defects and a high resistance. These characteristics combine light sensitivity and the capacity to harvest energy from heat to create a multipurpose SnSe-based memory device.

3.2 Film Deposition

Investigating the growth of SnSe thin films at various temperatures is the primary objective of this chapter. Pulsed-laser deposition was used to prepare SnSe thin films. The krypton fluoride (KrF) laser used in this study has a wavelength of 248 nm and is a coherent excimer laser. SnSe thin films were deposited at temperatures of 250, 310, 330, and 350 ℃ with a laser repetition rate of 10 Hz; the distance between the substrate and the target was 30 mm. Base deposition pressure ranged from 5.0 x 10^{-5} Pa to 5.5 x 10^{-5} Pa. The effect of deposition time and substrate temperature will be covered in more detail in the following sections with the help of cross-sectional SEM image analysis and X-ray diffraction (XRD) analysis.

As shown in Figure 3.2, silicon (Si) substrate with a top layer of 300 nm SiO_2 that served as an electrical insulator between the Si substrate and the bottom electrode was used for memory device fabrication. Pt was chosen as the bottom electrode of the

memory device, a 150 nm Pt layer and a 20 nm titanium adhesion layer was deposited on top of SiO_2. Prior to thin film deposition, the substrates were subsequently cleaned with acetone and ethanol in an ultrasonic bath for at least five minutes.

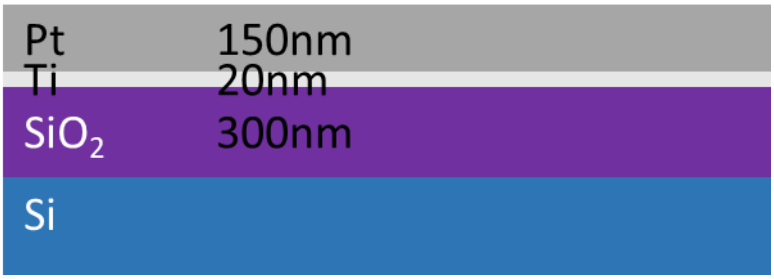

Figure 3.2. Schematic diagram of the Pt-coated Si substrate with SiO_2 as insulator.

3.3 Structural characterization of SnSe films

XRD analyses on SnSe films deposited on Pt-coated Si substrates at 250, 310, 330, and 350 °C were carried out, and the results are shown in Figure 3.3. The 2θ diffraction peaks at 15.4°, 31.1° and 64.8° are indexed, respectively, as orthorhombic (200), (400), and (800) atomic planes of SnSe (a = 1.149 nm, b = 0.4153 nm, and c = 0.444 nm, JCPDS #48-1224). The dominance of {200} peaks suggests that a-axis is the preferred growth direction of the layer-structured SnSe films at various temperatures. It is also apparent that when the deposition temperature reaches 350 °C, the diffraction peaks of (200) and (800) become much weaker compared to the films grown at relatively lower temperatures. However, at much lower growth temperature of 250 °C, the SnSe film presents additional peaks of (302) and (122) beyond the {200} peaks, suggesting that the optimal deposition temperature for SnSe thin films is close to 330 °C.

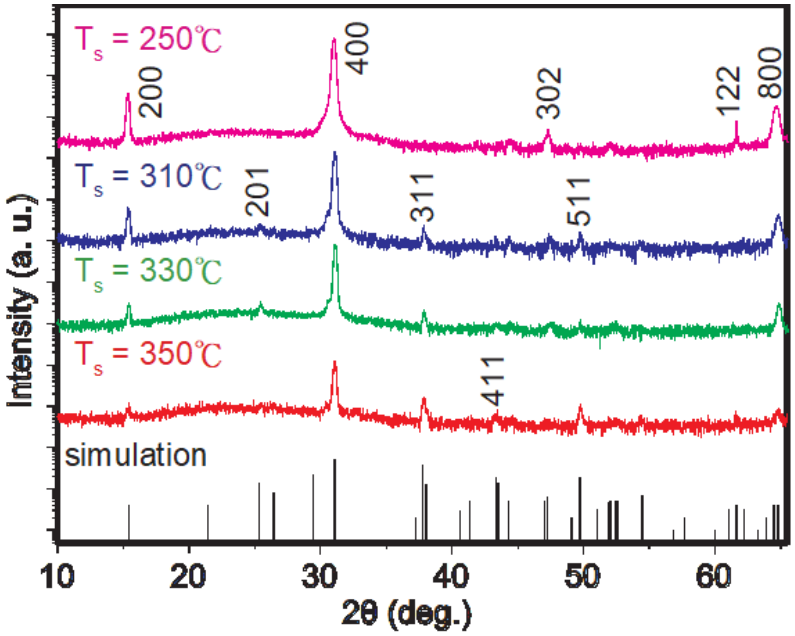

Figure 3.3. X-ray diffraction pattern of SnSe thin films deposited at T_s = 250 °C, 310 °C, 330 °C, and 350 °C compared to the simulation pattern of SnSe (JCPDS #48-1224).

Microstructure of the 330 °C-deposited SnSe thin film was examined by means of high-resolution TEM (HRTEM), and the cross-sectional image are shown in Figure 3.4 (a). One can see that the film presents polycrystalline structure which is also demonstrated by the ring-type of selected area electron diffraction (SAED) pattern shown in Figure 3.4 (b), where the corresponding SnSe atomic planes of (111), (122) and (311) with d-spacings of 3.44, 4.24, and 6.68 nm, respectively, can be indexed. These results correspond to diffraction peaks found in the XRD pattern.

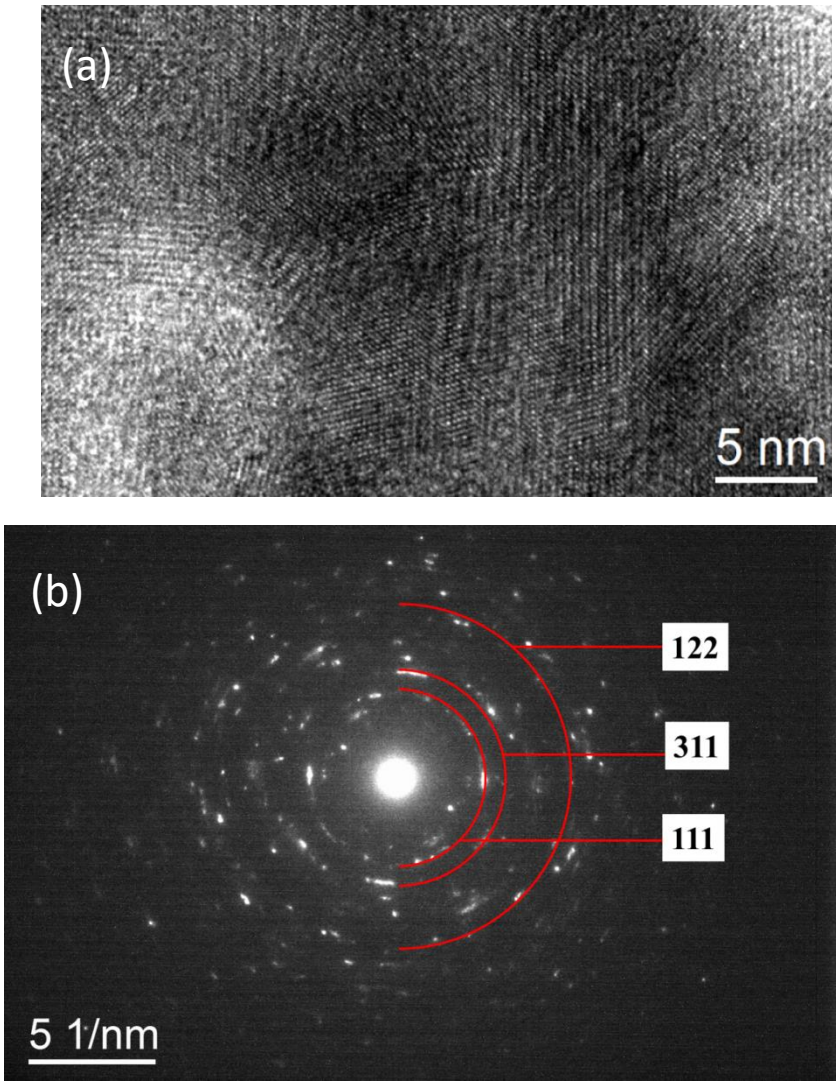

Figure 3.4. (a) HRTEM image of polycrystalline structure of the film and (b) a selected area diffraction pattern.

Figure 3.5 (a) displays a HRTEM image of a region of the SnSe thin film. The measured lattice plane angles and distances in the figure match with the orthorhombic SnSe structure (a = 1.149 nm, b = 0.4153 nm, and c = 0.444 nm), which are also consistent with the XRD results given before. The quantitative EDX analysis shows that the composition of Sn and Se is approximately 1:1, indicating the formation of the

SnSe compound. The composition of Sn and Se is shown by the EDX pattern displayed in Figure 3.5 (b) (notice that the Cu peak belongs to the copper grid).

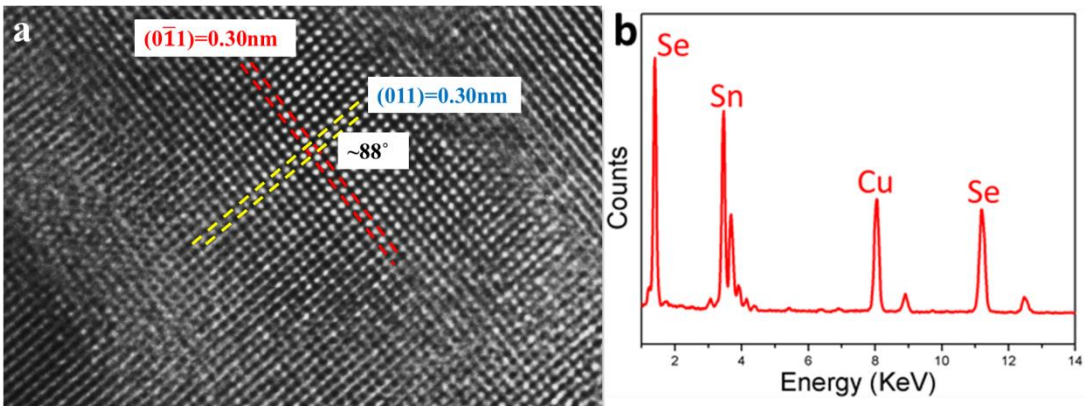

Figure 3.5. (a) HRTEM image showing (011) and (0$\bar{1}$1) planes with 88 ° between the planes and (b) EDX spectrum of SnSe thin film deposited at T_s = 330 ℃.

3.4 Electrical characterization of SnSe-based device

In order to explore the switching mechanism and induce the multi-level resistance states in the polycrystalline SnSe thin film-based device with different electrodes, we investigated the SnSe-based memristor devices where the SnSe thin film is constructed in the metal-insulator-metal (MIM) sandwiched structure with Ag and Cu as active electrode. We also studied the switching mechanism and compared the performance difference between Ag and Cu as active electrode.

Electrical characterization of memory devices of Cu/SnSe/Pt and Ag/SnSe/Pt were conducted in the commercial memristor characterization platform ArC ONE from Arc Instruments. During the measurement, when a voltage sweeping was applied between the top and bottom electrode of the memory device, the current flowing

through the memory device was measured and the resistance of the device is calculated. Figures 3.6 (a) and (b) show the results of I-V curve measurements. Generally, the device typically transits from the high resistance state (HRS) to the low resistance state (LRS) by gradually raising the positive voltage applied to it from 0 V to a certain positive value, which is known as the "SET" process. The "RESET" procedure, on the other hand, happens when the device switches from LRS to HRS by applying a voltage from 0 V to negative voltage. It should be noted that we established a current compliance of 1.3 mA while performing the voltage sweeping on the device for both Cu and Ag top electrode devices in order to safeguard it from irreversible resistive switching or damage.

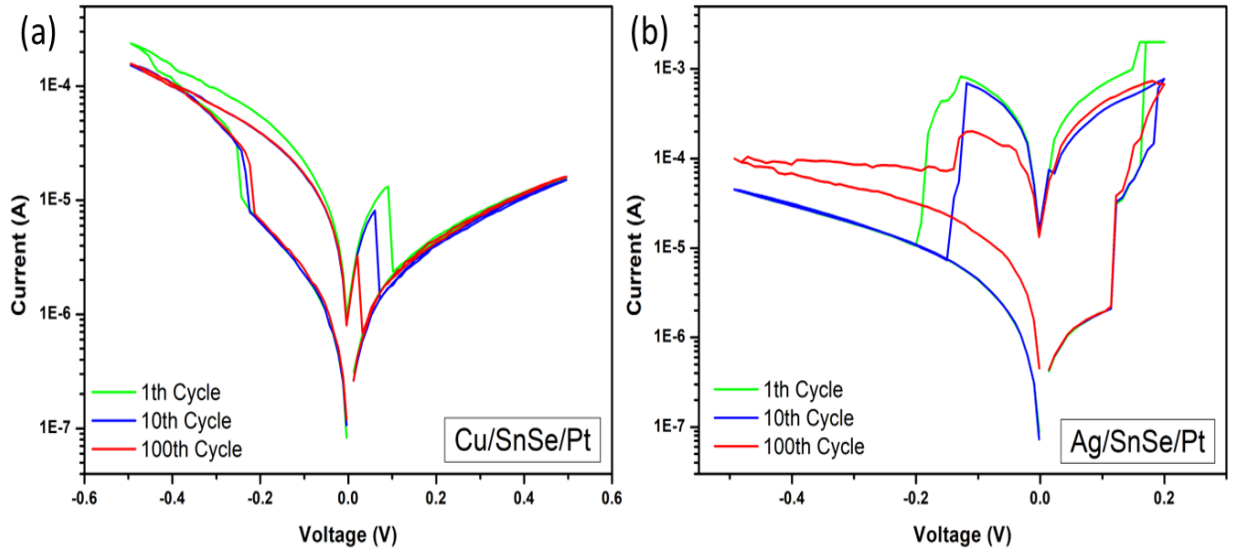

Figure 3.6. (a) I-V curves of the Cu/SnSe/Pt device and (b) the Ag/SnSe/Pt device at 100th applied voltages sweeping

As seen in Figure 3.6(a), the switching voltage is roughly at 0.1 V to SET the device from HRS to LRS. This can be seen by changing the magnitude of voltage applied sweeping on Cu electrode from 0 V to 0.5 V with 0.01 V step voltage increase.

The device was then reset using a negative voltage sweep from 0 V to -0.5 V with a 0.01 V step voltage reduction applied to the Cu electrode. To RESET the device from LRS to HRS, the first RESET voltage was roughly at -0.25 V. We used a voltage sweep from 0V→0.5V→0V→-0.5V→0V with 0.01V step voltage for 100 times in order to examine its reliability. The on/off resistance ratio of the Cu/SnSe/Pt device maintained a high of roughly 10 after 100 times of switching, according to the 1st, 10th, and 100th recorded I-V curves. Figure 3.6 (b) displays the I-V characteristics of the Ag/SnSe/Pt device as measured using the same technique. First, for the switching operation, we applied a positive voltage sweep on the Ag electrode from 0 V to 0.2 V using a 0.01 V step voltage, and we can observe that the device is switched ON at roughly 0.13V. The device was then reset using a negative voltage sweep from 0 V to -0.5 V with 0.01 V step voltage provided to the Ag electrode, turning it back off at about -0.2 V. To investigate the reliability, we also carried out the switching procedure on the Ag/SnSe/Pt device 100 times. The outcome demonstrates that the on/off resistance ratio remains at roughly 80 after 100 switching cycles.

Figure 3.7 presents the findings of an investigation on the memory device's data retention and durability characteristics, respectively. One can see that the memory device has good durability after 100 cycles and good data retention after 10,000 seconds, with essentially no degradation of either LRS or HRS as time approaches the end of the examined region. This could be explained by the resistance state reading pulses' cumulative disruption of the resistance state as a result of the memory device's ultralow switching voltage. In general, the memory device's data retention and endurance characteristics suggest that it might function well in traditional memory

applications.

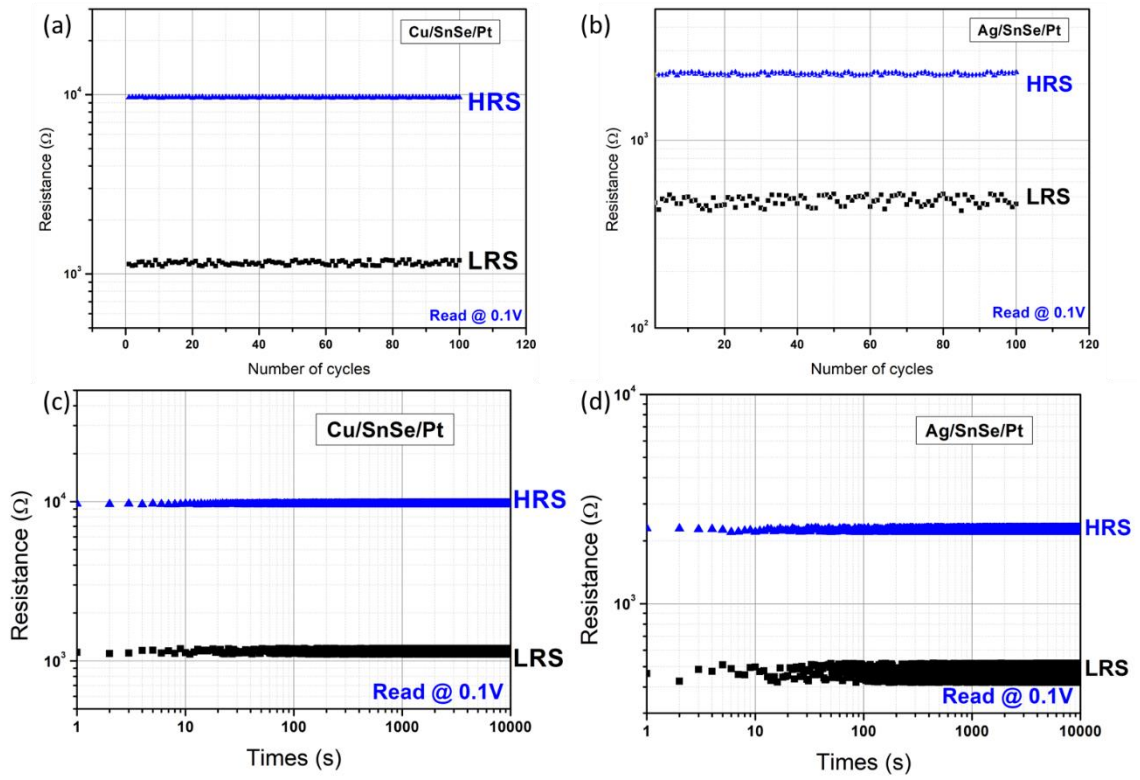

Figure 3.7. (a) Endurance characteristics of LRS and HRS of Cu/SnSe /Pt device and (b) Ag/SnSe/Pt device for 100 cycles each; retention characteristics of LRS and multilevel HRS under different RESET negative voltage pulses of (c) Cu/SnSe /Pt device and (d) Ag/SnSe/Pt device for 10^4 s.

3.5 Summary

Polycrystalline SnSe thin films on Pt-coated SiO_2/Si substrates have been characterized for their structural and electrical properties using Ag and Cu as the active electrodes, respectively. The findings demonstrate that the optimal deposition temperature for stoichiometric SnSe film is 330 °C. In electrical characterization, the SnSe films deposited between Ag or Cu active electrode and Pt bottom electrode in

M-I-M structure exhibit a resistive switching behavior where these devices are SET by positive voltage sweeping and RESET by negative voltage sweeping. For Cu/SnSe/Pt structured device, the ON/OFF ratio between LRS and HRS retains at about 10 after 100 cycles. While for Ag/SnSe/Pt structured device, the ON/OFF ratio between LRS and HRS retains at about 80 after 100 cycles, which is slightly higher than the Cu/SnSe/Pt structured device. Moreover, endurance and retention characteristics of both devices have been investigated. The result shows that polycrystalline SnSe thin film could perform well in traditional memory application.

Chapter 4 Characterization of STO thin films and heterostructure thin film composed of SnSe and STO

4.1 Introduction of strontium titanate (STO)

Strontium titanate ($SrTiO_3$) has an ABO_3 cubic perovskite structure with the space group of $Pm\bar{3}m$ (#221). Figure 4.1 (a) illustrates the unit cell of STO with a lattice constant of 0.39 nm and density of $\rho = 5.12 g/cm^3$. While the O^{2-} ions coordinate six times with the Ti^{4+} ions, and the Sr^{2+} ions are each surrounded by four TiO_6 octahedra. As a result, there are totally 12 O^{2-} ions coordinate with each Sr^{2+} ions. While the O-2p states and Ti-3d states hybridize within the TiO_6 octahedra, resulting in a strong covalent connection. Sr^{2+} and O^{2-} ions exhibit ionic bonding within the TiO_6 octahedra, whereas a hybridization of the O-2p states with the Ti-3d states results in a pronounced covalent bonding giving $SrTiO_3$ mixed ionic and covalent bonding properties. STO is a model electronic material due to its unique structure resulted from the chemical bonding. Figures 4.1 (b)-(d) show the arrangements of atoms for (100), (110), and (111) respectively, where the Ti layer is the terminating layer in all three major crystals cut directions.

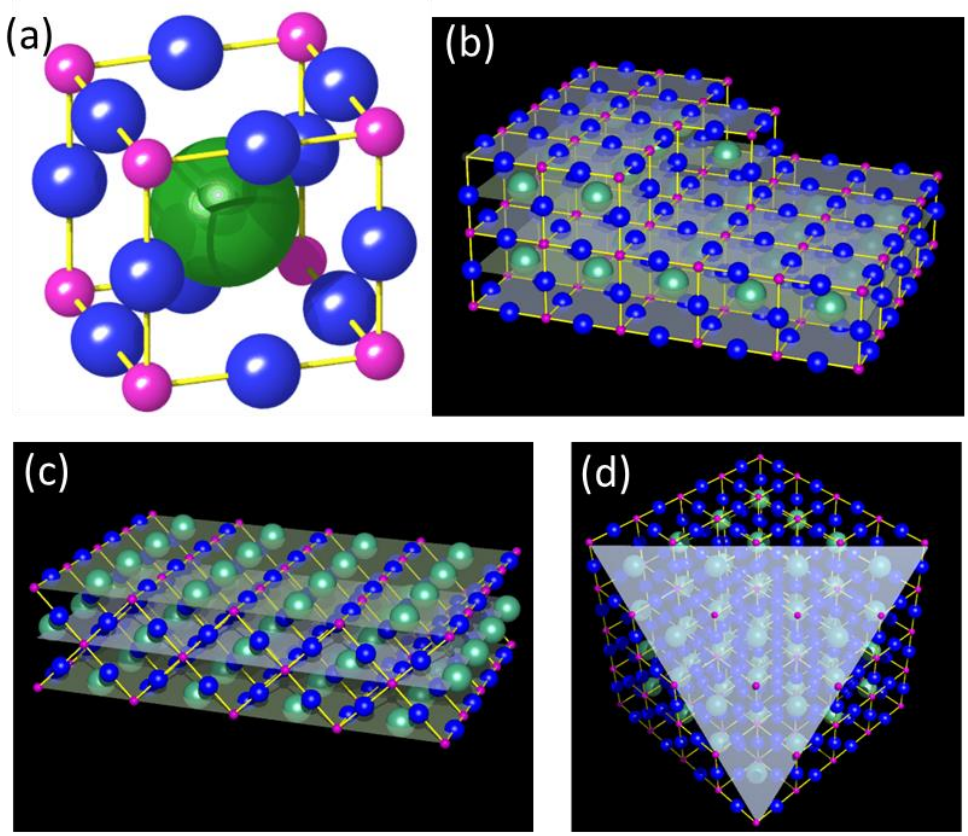

Figure 4.1. (a) Unit cell of $SrTiO_3$ where the violet, green, and blue spheres indicate Ti^{4+} cations, Sr^{2+} cations, and oxygens respectively. Crystal cut directions of $SrTiO_3$ at (b) (100) surface is cubic, (c) (110) surface is tetragonal, and (d) (111) surface has 6-fold symmetry.

STO is a potential candidate for next generation high-*k* gate dielectric materials due to its large dielectric constant, low dielectric loss and potentially ferroelectricity under strain [79], [81], [98]. For RRAMs with STO thin films epitaxially grown on silicon, or a heterostructure of doped STO films on Nb-doped STO substrate, their resistance on/off ratios are only in the range between 1 and 100 [74] as shown in Table 1. These low resistance ratios may be increased by stacking with a semiconducting buffer layer forming a heterojunction structure. A heterostructure may also make the device achieve a much higher resistance ratio and even multilevel resistive switching.

Table 1 Comparison of the devices with polycrystalline/crystalline STO film

Device	Crystalline STO film	Top electrode	SET voltage	RESET voltage	Resistance ratio	Resistance state	Ref.
Fe:STO/Nb:STO	Yes	Pt	~2.5V	~-2.5V	60	2	[74]
STO/SRO	Yes	Pt	~2V	~-2V	~100	2	[99]
STO/SRO	Yes	-	>-4V	>-4V	~10000	2	[100]
Ba:STO/SRO	Yes	Pt	>-3V	>4V	~3	2	[101]
STO/Pt	Yes	Ag	~1V	~-3V	~100000	4	[79]

4.2 Experimental Details

Firstly, a 30 nm-thick STO film was deposited by laser molecular beam epitaxy (LMBE) at 625°C on a 15 mm x 15 mm Pt/SiO_2/Si (HF-Kejing, China) substrate. After reaching a base vacuum of 2×10^{-5} Pa, high-purity oxygen (O_2:99.99%) was flowed into the chamber during the deposition. For STO thin film deposition, oxygen partial pressure of 5 Pa was maintained which is an important factor for the property control. After finishing the deposition of STO film, the sample was cooled down from 625°C to room temperature in 1000 Pa oxygen pressure. Subsequently, the based vacuum of 2×10^{-5} Pa was resumed, and a 90 nm-thick SnSe film was *in situ* deposited at room temperature on the STO film to form a SnSe/STO heterostructure. In order to compare the efficiencies of the different electrodes, Ag and Cu top electrodes were selected and deposited on the SnSe film by direct current (DC) magnetron sputtering at room temperature through a shadow mask from 80 to 500 μm in diameter. The thicknesses of Ag and Cu top electrodes are about 80 and 180 nm, respectively. Figure 4.2 (a) shows the schematic diagram of the fabricated SnSe/STO heterostructure-based memristor for electrical characterizations performed at room temperature in air using

an ArC-ONE memristor characterization instrument connected to a probe station. The microstructure of the heterostructure was characterized by means of transmission electron microscope (TEM) (JEOL 2100F).

All the first-principles calculations were performed using the Vienna Ab initio Simulation Package (VASP.5.4.4.18) with generalized gradient approximation of the Perdew-Burke-Ernzerhof functional (GGA-PBE) and projector augmented wave (PAW) potentials [102]–[104]. DFT-D3 method was used in SnSe bulk to correct van der Waals interaction [105]. PBE+U method was applied in STO bulk to describe the strong correlation of electrons on the Ti 3*d* orbital (U = 4.2 eV) [106], [107]. The cutoff energy was set to be 400 eV and The first Brillouin zones of SnSe and STO were sampled by $2 \times 6 \times 6$ and $6 \times 6 \times 6$ Monkhorst-Pack grids, respectively [108]. Energy convergence criterion was set to be 10^{-4} eV and force convergence criterion 0.05 eV/Å. The optimized unit cells of SnSe (a = 11.491 Å, b = 4.177 Å, c = 4.503 Å) and STO (a = b = c = 3.936 Å) were adopted to construct supercells ($1 \times 2 \times 2$ and a $2 \times 2 \times 2$) for calculating the diffusion barrier of Ag and Cu atom using nudged elastic band (NEB) method [109] , respectively.

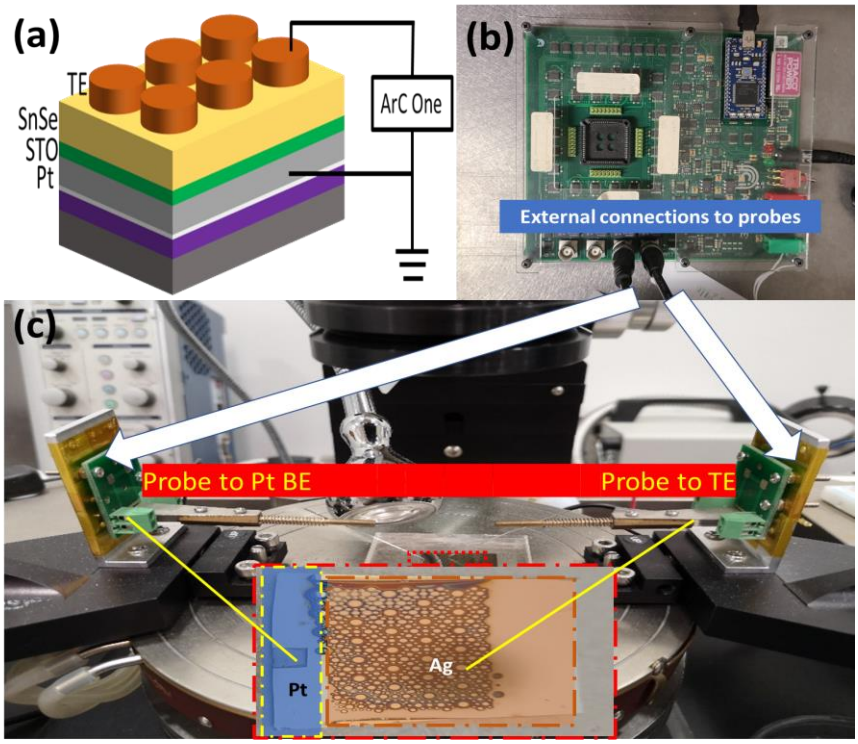

Figure 4.2. (a) Schematic of TE/SnSe/STO/Pt memristor device with Cu or Ag top electrode (TE) connected to ArC-One measurement instrument, (b) appearance of ArC-One measurement instrument, and (c) the probe station and the measured devices.

4.3 Structural characterization of SnSe/STO heterostructure films

Microstructure of the SnSe/STO/Pt heterostructure was characterized by cross-sectional TEM study and the results are shown in Figure 4.3. The contrast in Figure 4.3 (a) suggests that both the SnSe and STO layers are polycrystalline in microstructure, and the thicknesses of the SnSe and STO layers are determined to be about 90 and 30 nm, respectively. It is apparent that the $SrTiO_3$ (STO) layer is of perovskite structure as shown in Figure 4.3 (b), where the unit cell of STO can be identified and lattice

constant a = 0.39 nm can be determined. Some areas of the polycrystalline SnSe layer present a [010] preferred growth direction, and Figures 4.3 (c) and (d) depict typical HRTEM image and electron diffraction pattern along a zone axis close to [101] direction. Electron dispersive x-ray (EDX) spectra (not shown) of both layers reveal nearly 1:1 ratio of Sr:Ti and Sn:Se, suggesting stoichiometry of the deposited STO and SnSe layers.

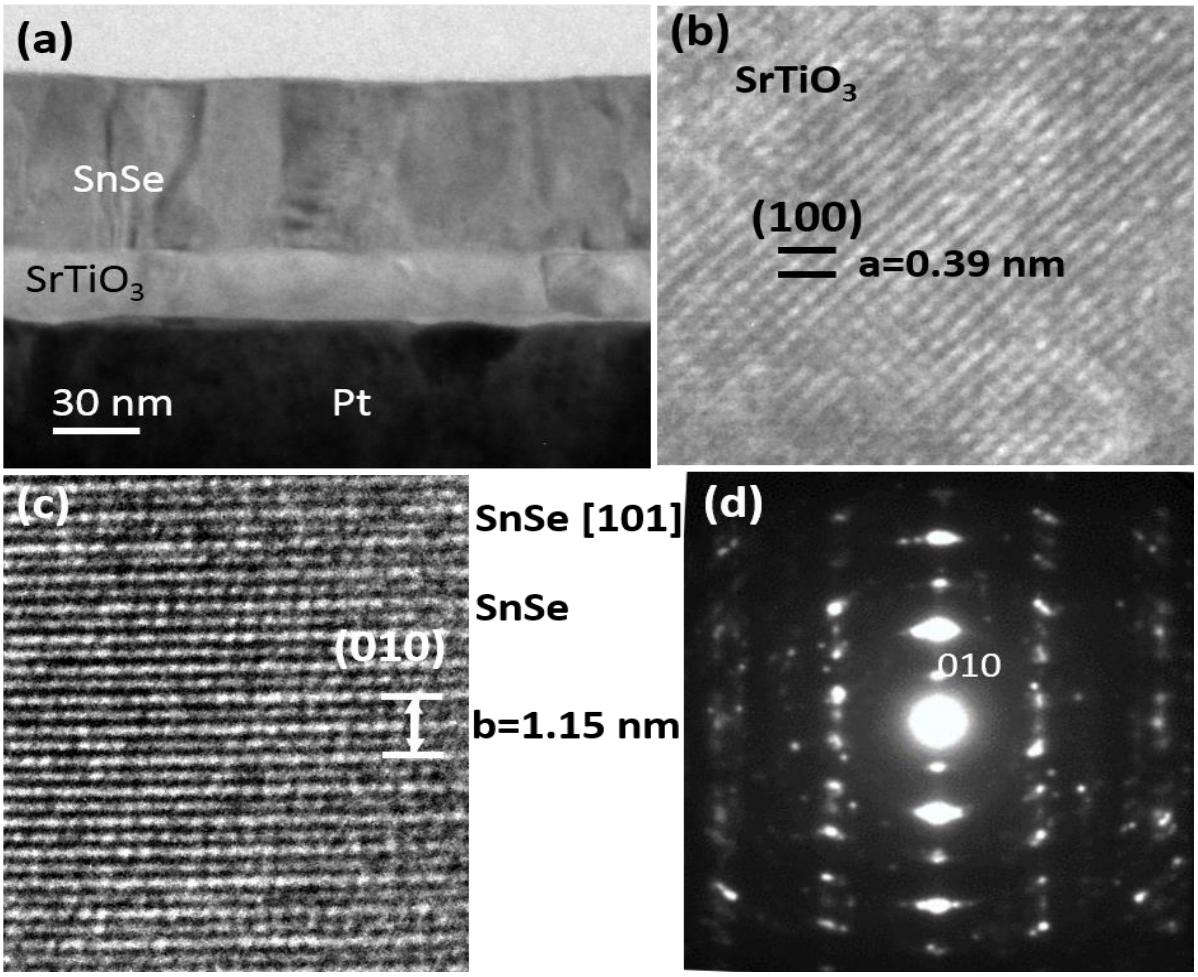

Figure 4.3. (a) Cross-sectional TEM image of a heterostructure device where the SnSe and STO layer can be clearly identified. (b) HRTEM image showing crystalized structure of STO, HRTEM image (c) and diffraction pattern (d) of the SnSe layer viewed along [101] direction.

4.4 Electrical characterization of SnSe/STO heterostructure-based device

Resistive switching characteristics of the Cu/SnSe/STO/Pt and Ag/SnSe/STO/Pt memory cells were investigated by voltage sweeping I-V curve measurements and the results are shown in Figures 4.4 (a) and (b). Generally, by steadily increasing the positive voltage imposed on the device from 0 V to a certain positive voltage, the device changes from high resistance state (HRS) to low resistance state (LRS), i.e., the "SET" process. On the other hand, the "RESET" process happens when the device changes from LRS to HRS by imposing the voltage from 0 V to negative voltage. As shown in Figure 4.4 (a), an electroforming process is required to activate the device to present the rectifying and hysteretic I-V characteristics which is the indicator of resistive switching. For both Cu and Ag top electrode devices, a forming process is necessary for activating the memory effect. It should be pointed out that, to protect the device from irreversible resistive switching or damage, we set a current compliance at 1.3 mA when applying the voltage sweeping on the device.

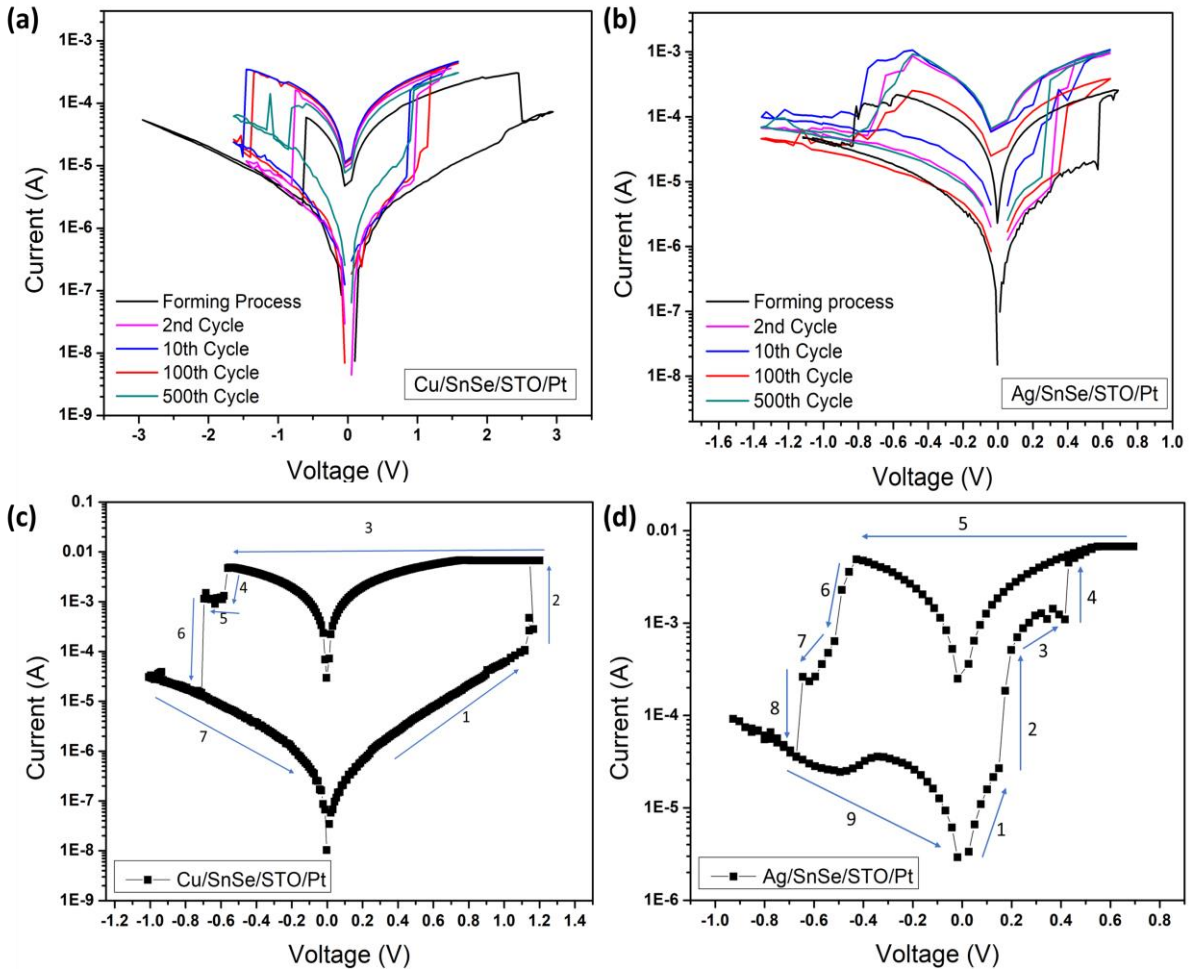

Figure 4.4. (a) I-V curves of the Cu/SnSe/STO/Pt device and (b) the Ag/SnSe/STO/Pt device at 500th applied voltages sweeping. The SET process and RESET process of (c) the Cu/SnSe/STO/Pt device, and (d) the Ag/SnSe/STO/Pt device.

As shown in Figure 4.4 (a), by controlling the amplitude of positive voltage swept on Cu electrode from 0V → 3V → 0V with 0.05 V step voltage increase for the forming process, we can see that the switching voltage is approximately at 2.5 V to SET the device from initial state to LRS. After the forming process, the Cu/SnSe/STO/Pt device stays at ON state. Then a reset process of negative voltage swept from 0 V → -3 V → 0 V with 0.05 V step voltage decrease was applied on the Cu electrode to switch the device back to OFF state. The first RESET voltage is approximately at -0.6 V to

RESET the device from LRS to HRS. In order to study the reliability, we applied a voltage sweep form 0 V → 1.6 V → 0 V → -1.65 V → 0 V with 0.05 V step voltage for one thousand times. The 2^{nd}, 10^{th}, 100^{th} and 500^{th} measured I-V curves of Cu/SnSe/STO/Pt device show that, after five hundred times of switching, the on/off resistance ratio retains high of about 10. The I-V characteristics of Ag/SnSe/STO/Pt device measured by the same method are shown in Figure 4.4 (b). Firstly, we applied positive voltage swept on Ag electrode from 0 V → 0.7 V → 0 V with 0.05 V step voltage for the forming process, and we can see that the device is switched ON at approximately 0.6 V. Then, a reset process of negative voltage swept from 0 V → -1.1 V → 0 V with 0.05 V step voltage was applied on the Ag electrode to switch the device back to OFF state at approximately -0.8 V. We also repeated the switching process for one thousand times on the Ag/SnSe/STO/Pt device to study the reliability. The result shows that, after five hundred times of switching, the on/off resistance ratio retains at about 10.

To analyze the switching mechanism, I-V curves of switching process of both Cu and Ag devices were measured and the results are shown in Figures 4.4 (c) and (d). It is apparent that the switching process of Cu/SnSe/STO/Pt device can be divided into seven steps. However, the switching process of Ag/SnSe/STO/Pt device is much more complicated, and it contains nine steps. According to reference reports, an important aspect of metal oxide materials is the migration of oxygen vacancies (or oxygen ions) under an applied electrical field. Based on the investigations from former reports, the switching mechanism in our devices should be mediated by forming and rupture of conductive filament. This active medium is actually much smaller than the cell size

which allowing a potential of scaling. When the positive voltage sweep is applied on both Cu and Ag-electrode devices, oxidation occurs on Ag and Cu top electrode since both are of electrochemically active metal. Therefore, volatile Cu^{+} and Ag^{+} cations could form as Cu → $Cu^{2+} + 2e^{-}$ and as Ag → $Ag^{+} + e^{-}$. These volatile cations migrate toward Pt electrode through the SnSe layer and STO layer and are finally reduced by electrons flowing from cathode, i.e., $Cu^{2+} + 2e^{-}$ → Cu and $Ag^{+} + e^{-}$ → Ag. Meanwhile, when negative voltage sweeps are applied, Cu ions and Ag ions can migrate back to the top electrode in the same way.

However, because of the different electrochemical activities of Cu and Ag, the forming voltage of Cu filament is relatively higher, and the switching time is relatively longer compared to Ag filament formation [110], [111]. The migration processes of Cu filament and Ag filament in the SnSe layer and STO layer are different. In the Cu/SnSe/STO/Pt device, the 2nd step of switching process shows that the Cu filament evolutes from unstable state to stable state in the whole heterostructure. Before the Cu filament forming stably between Cu top electrode and Pt bottom electrode, Cu ions firstly diffuse into SnSe layer. After the Cu filament is stabilized in SnSe layer between Cu top electrode and STO layer, it keeps migrating to Pt bottom electrode in the STO layer and finally changes the device to LRS. When the device is switched back from LRS to HRS in 4th to 6th step, the Cu filament ruptures and reduces back to Cu top electrode. The filament first reduces in STO layer and breaks from Pt bottom electrode, then it keeps reducing in STO layer as shown in the 5th step. After the whole filament is reduced and broken in STO layer, it starts reducing at SnSe layer and finally RESET to HRS as shown in 6th step. The switching process is very similar for the

Ag/SnSe/STO/Pt device, but one can see that the 2nd to 4th steps as shown in Figure 4.4 (d) present a more complicated process when Ag filament migrates between SnSe layer and STO layer to switch the device to ON state. Moreover, the RESET process of the Ag/SnSe/STO/Pt device in the 6th step shows a significant decrease of resistance, but the decreasing speed of resistance slows down at 7th step. It suggests that Ag ions migrate back from STO layer to SnSe layer and shows a multistate characteristic between the HRS and LRS. Finally, as the RESET voltage decreases, Ag ions migrate back to the electrode and the device returns to HRS. All these switching processes show that these two devices may result in different resistance states, implying multilevel data storage and application in neuromorphic computing.

Multilevel resistance states depending on different SET and RESET processes were investigated to find out the influence of positive and negative voltage pulses on the filament evolution in the resistive layers. As shown in Figure 4.5 (a), the LRS of Cu/SnSe/STO/Pt device is achieved by positive voltage pulses, while the other HRS are achieved by negative voltage pulses. In the multistate test of the Cu/SnSe/STO/Pt device, a positive sweeping voltage from 0 to 2 V without current compliance is first applied to reach the LRS (state '5'), then a negative voltage pulse of -2.2V is applied to reach the first HRS (state '4'). With the gradual increase of negative voltage pulses to -6 V, the Cu/SnSe/STO/Pt device shows up to 6 resistance states. We also carried out a similar test to investigate the multistate characteristics of the Ag/SnSe/STO/Pt device and the results are shown in Figure 4.5 (b). One can see that, the Ag/SnSe/STO/Pt device also switches from initial state to LRS (state '7') by positive voltage sweeping from 0 to 2 V, but its first HRS (state '6') is achieved by a negative

voltage pulse of -1.7 V which is slightly lower than the Cu/SnSe/STO/Pt device. With the gradual increase of negative voltage pulses to -6.6 V, the Ag/SnSe/STO/Pt device presents up to 8 resistance states, i.e., two more states than the Cu/SnSe/STO/Pt device. Normally, a device with more resistance states should perform better when applied in neuromorphic computing.

The stability of different resistance states was confirmed by endurance test for 25 cycles of positive voltage sweeping and negative voltage pulses to SET and RESET the devices as shown in Figure 4.5 (a). For the Cu/SnSe/STO/Pt device, five high resistance states are found to be 1.12, 5.33, 9.65, 21.54, 43.37 and 87.72 kΩ at RESET voltage pulse when sweeping from -2.2 V to -6 V. While for the Ag/SnSe/STO/Pt device shown in Figure 4.5 (b), there are seven high resistance states from 1.05, 2.26, 5.53, 9.92, 23.55, 45.72 to 92.63 kΩ at RESET voltage pulses from -1.7 to -6.6 V. Retention properties of the multistate memory cells for both devices were also investigated for the different resistance states which were set by the former processes. As shown in Figures 4.5 (c) and (d), for both devices read at 0.1 V, all the resistance states can last for 10^4 s without obvious change from the beginning to the end of the test. From these endurance and retention tests, we conclude that the Cu/SnSe/STO/Pt and Ag/SnSe/STO/Pt memory devices are suitable for high-density storage and multilevel RRAM and memristor applications.

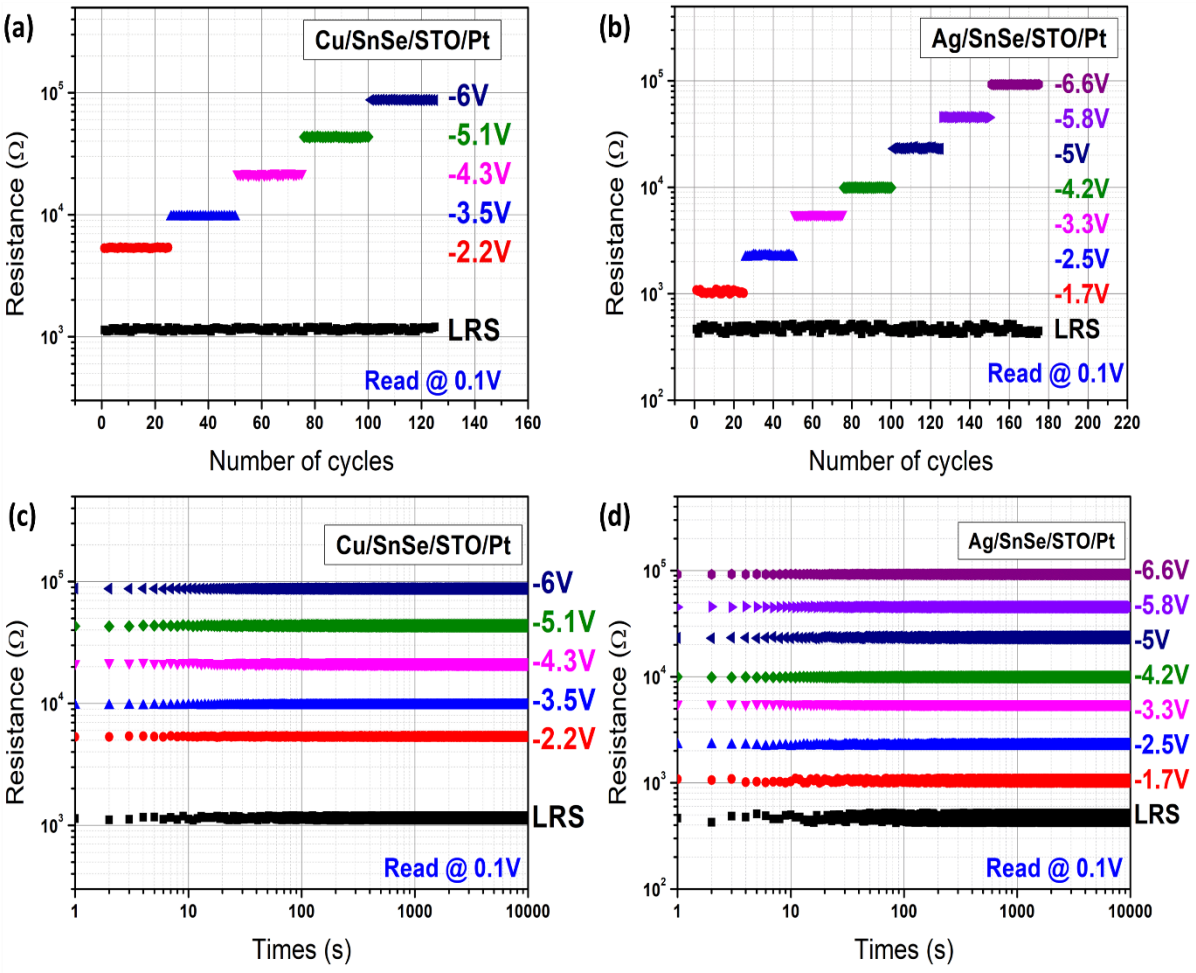

Figure 4.5. (a) Endurance characteristics of LRS and multilevel HRS under different RESET negative voltage pulses of Cu/SnSe/STO/Pt device and (b) Ag/SnSe/STO/Pt device for 25 cycles each; (c) multi-level retention characteristics of LRS and multilevel HRS under different RESET negative voltage pulses of Cu/SnSe/STO/Pt device and (d) Ag/SnSe/STO/Pt device for 10^4 s.

4.5 Study of the diffusion mechanism for copper and silver ions in SnSe/STO heterostructure films

We also created double logarithmic plots of I–V curves in both positive and negative voltage sweeps as shown in Figure 4.6. One can see that during the SET process, as shown in Figures 4.6 (a) and (c), thermally generated carriers are dominant over electrode-injected carriers in the ohmic conduction regime ($I \propto V$) at low voltage. Then the slope increases to the second regime ($I \propto V^3$) when the traps in SnSe/STO are all filled out by carriers due to the further increase of the voltage. There are two distinctive regimes with different slopes in the SET process for both Ag and Cu TE devices, which can be explained by the space charge limited conduction (SCLC) model. After the SET process, both devices are switched from HRS to LRS. As shown in Figures 4.6 (b) and (d), the double logarithmic plots of I–V curves in the RESET process of both Ag and Cu TE devices are also well-fitted with slope of about 1, suggesting an ohmic conduction behavior. This good fit indicates that Ag ion-based bridge filaments and Cu ion-based bridge filaments are formed in the SnSe/STO heterostructure switching medium, where the current path generated by filaments are metallic.

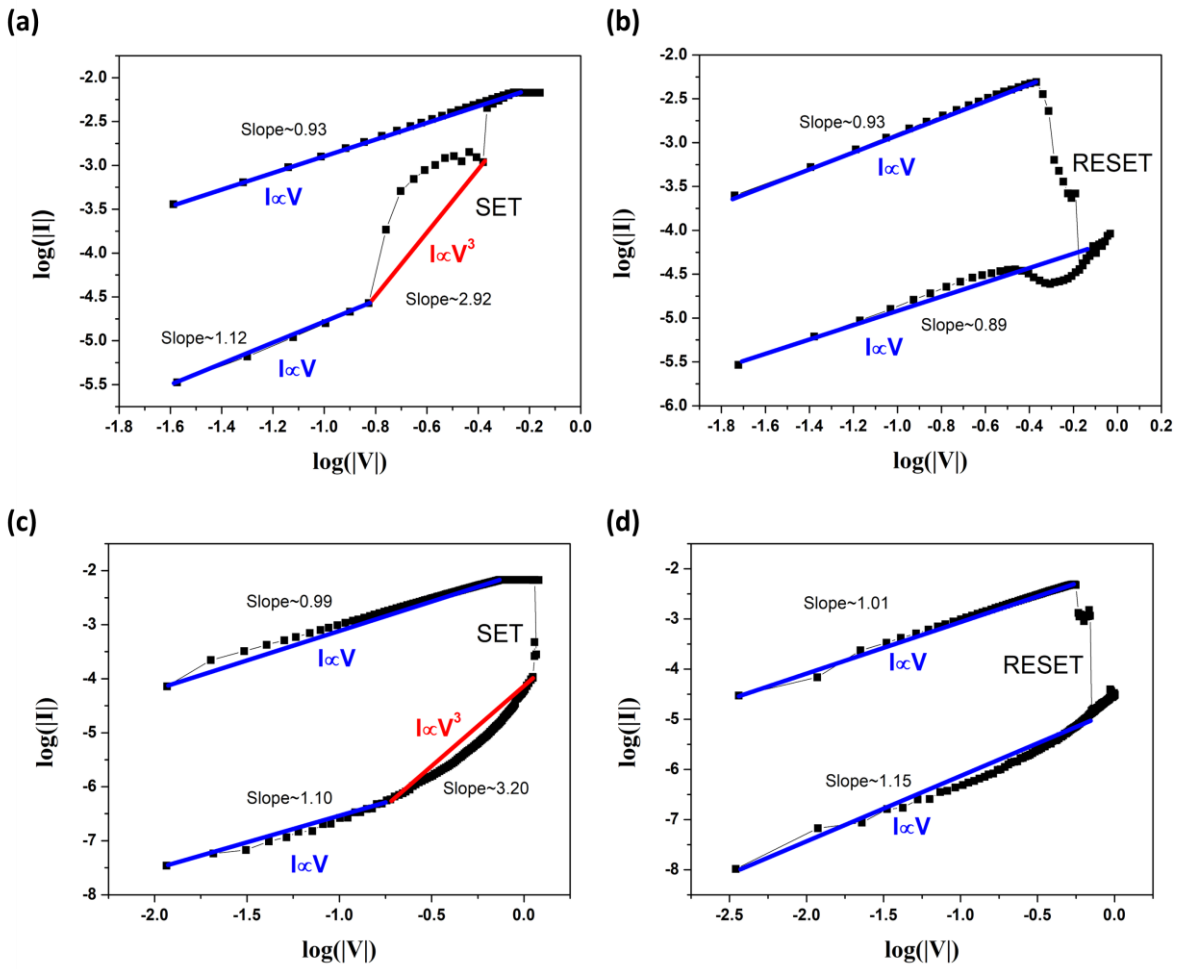

Figure 4.6. (a) Log(I)-Log(V) plots of the device with Ag TE under positive voltage sweeps and (b) under negative voltage sweeps. (c) Log(I)-Log(V) plots of the device with Cu TE under positive voltage sweeps and (d) under negative voltage sweeps.

To better understand the diffusion path and the energy barrier for Cu and Ag ions into the SnSe and STO layers, density-function theory (DFT) calculations were carried out. As shown in Figures 4.7(a) and (b), SnSe provides a faster diffusion channel for both Cu and Ag ions, as the energy barriers are 0.46 eV for Cu ions and 0.38 eV for Ag ions, respectively, which are much lower compared to that in STO. The energy barrier for Ag ion diffusion in STO layer is 1.21 eV, which is relatively higher

than that of the energy barrier for Cu ion which is 0.99 eV as shown in Figures 4.7(c) and (d). This result supports the fact that Ag as top electrode can archive more resistance states in the SnSe/STO heterostructure because the relatively higher energy barrier in STO helps to stabilize the intermediate states by delaying the filament rapture process. Since the LRS of devices is the initial state to achieve multistate and the time it takes for a voltage pulse to reach the middle state is approximately 1–5 μs [79], the filament in the SnSe layer and STO layer cannot migrate back to the top electrode completely in such a short time [112]–[115]. The filament rapture process is continuous at the SnSe/STO interface under increased negative voltage pulses on top electrode, leading to further change of resistance state of the device. Therefore, this delayed process increases the possibility of forming more resistance states when negative voltage pluses are applied on the device to rapture the filament. Figure 4.7(e) depicts the potential switching mechanisms of formation and rapture of conductive filament for the Cu and Ag-electrode devices [116], [117]. These intermediate states demonstrate that the devices are both resistive switching memories and memristors.

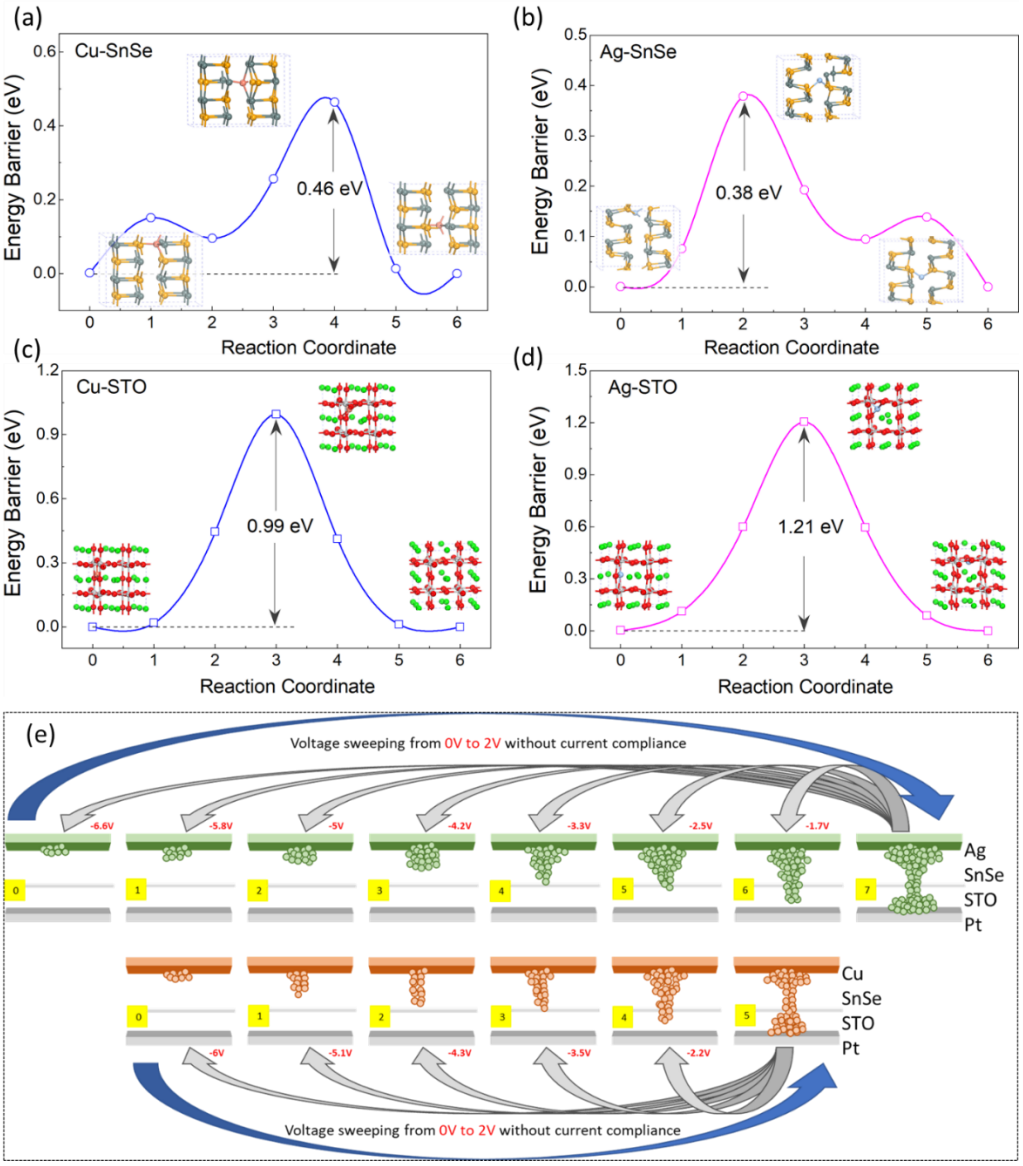

Figure 4.7. (a) The diffusion path and the energy barrier for Cu ions and (b) Ag ions diffused from the top electrode into SnSe; (c) The diffusion path and the energy barrier for Cu ions and (d) Ag ions diffused from the SnSe/STO interface into STO; (e) The switching mechanism of Cu/SnSe/STO/Pt device and Ag/SnSe/STO/Pt device. The blue arrows indicate that both devices are switched from HRS to LRS by voltage sweeping without current compliance, and the gray arrow indicate that the multi-states can be achieved by negative voltage pulse in different values.

4.6 Summary

In summary, we have fabricated and characterized SnSe/STO heterostructure-based memristors with different top electrodes. It was found that the resistance states of memory cells with Cu top electrode and Ag top electrode can achieve 6 and 8 resistance states, respectively; and the formation and destruction of Cu and Ag filaments in SnSe and STO layers under voltage sweeping and voltage pulses are believed to be responsible for these characteristics. These multilevel states are reliable during 10^3 SET and RESET reliability tests and are stable after 10^4 s retention tests. These results suggest that the SnSe/STO heterostructure-based memristors may have a great potential for synaptic device.

Chapter 5 Conclusions

The research work in this thesis including the fabrication and characterization of SnSe and STO thin films as well as their heterostructure on Pt-coated SiO_2/Si substrates as the switching medium in memristor devices. Different active top electrodes of Ag and Cu are compared for the performance of memory. The following conclusions are obtained:

1. Polycrystalline SnSe thin film memory devices with Ag and Cu as active top electrodes are found to have bipolar resistive switching behavior. Reliability test on both the Cu/SnSe/Pt and Ag/SnSe/Pt devices reveal that both devices remain their stable on/off ratios, i.e. 10 for Cu/SnSe/Pt and 80 for Ag/SnSe/Pt devices. Moreover, results of endurance and retention tests reveal that both devices possess good durability on 10000 seconds and good reproducibility up to 100 cycles.

2. With the STO buffer layer, the SnSe/STO heterostructure device shows much better performance on reliability test, the ON/OFF ratio for both Cu/SnSe/STO/Pt and Ag/SnSe/STO/Pt devices after 1000 cycles remain on 10.

3. Moreover, multi-level switching studies had been done on both devices. Electrical measurement shows that Cu/SnSe/STO/Pt can present 6 resistance states and Ag/SnSe/STO/Pt presents 8 resistance states. Multi-level retention

characteristics for both devices are studied, and it reveals that all states remain stable after 10000 seconds. These results suggest that the Ag/SnSe/STO/Pt heterostructure device may function well in traditional multilevel memory applications.

5.1 Directions for Future Work

Although this work has successfully demonstrated a memristor device with multi-level resistance states by stacking SnSe and STO to form a heterojunction, the studies can go further.

Firstly, the switching speed between Ag and Cu electrode on SnSe/STO/Pt device can be investigated because one of the merits of memristor device is the switching speed. The energy needed to switch the device between SET and RESET states can also be studied as lower energy consumption is better for an electronic device.

Last but not least, the bio-inspired application of SnSe/STO heterostructure device can be further investigated as it has stable performance on endurance and retention of multi-level resistance state.

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