P-TYPE SEMICONDUCTOR TELLURIUM GROWTH AND HIGH-PERFORMANCE P-TYPE FIELD EFFECT TRANSISTOR FABRICATION

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P-type semiconductor Tellurium growth and high-performance P-type field effect transistor fabrication

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CERTIFICATE OF ORIGINALITY

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_____(Signed)

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Abstract

Complementary n- and p-type field effect transistors (FET) are the foundation of modern semiconductor electronics. Researchers have synthesized many kinds of n-type semiconductors to fabricate high performance n-type FETs. An elemental p-type two-dimensional (2D) material (e.g., tellurene (Te)) has uncommon crystal structures and properties. Nevertheless, there are still many great challenges to grow high crystalline and large size Te by using conventional vapor deposition method.

Firstly, we design a Copper foil assisted alloy-buffer-controlled method to achieve the aligned, single crystalline Te with thickness thin to < 10 nm on mica substrate. The most significant role in this method is to form the Copper- Tellurene (Cu-Te) alloy. This alloy formation achieves the precursor distribution uniform both spatially and temporally which cannot be controlled in conventional vapor growth process. From transmission electron microscopy (TEM) characterization and theoretical calculations, we find that Te grows in the [110] direction along the [600] direction of mica substrate. This alignment growth is due to the lattice mismatch of Te and mica substrate is small to 0.15 % and their strong binding energy. The as-grown Te flakes shows smooth surface and high uniformity. This method successfully achieves the controlled growth of 2D Te.

Next in this thesis, we demonstrate a strategy to fabricate high performance p-type FETs. As the device size decreases down to nanoscale, the contact resistance becomes a dominant factor of device performance. Researchers have shown ultralow contact

resistance for n-type two-dimensional (2D) semiconductors with indium, bismuth, and antimony. However, the low-resistance electrical contact to p-type 2D semiconductors proves to be very challenging, which makes it difficult to construct complementary devices. Here we introduce an ultrathin (1.2 nm) Selenium (Se) interfacial layer at the contact region. Se has the highest work function in the periodic table of elements, which greatly reduces the Schottky barrier height (SBH) with p-type semiconductors. The semiconducting characteristics of Se can also mitigate the gap states induced by common metal electrodes. With the Se interfacial layer of p-type WSe_2 transistors, the saturated current density increases from 17.78 μA μm-1 to 124.62 μA μm-1; and the contact resistance decreases from 10.2 kΩ·μm to 2.2 kΩ·μm. Lastly, we extended our Se interfacial layer contact methodology to other p-type semiconductors (black phosphorus (BP), semiconducting carbon tubes (CNT)), providing a reliable method to establish low-resistance electrical contact to nanoscale p-type semiconductors. The Se interfacial layer contact can also be applied to dry transfer method to fabricate p-type FETs, that has comparable device performances compared to transistors fabricated by Se interfacial layer deposition. Our results provide a great opportunity to fabricate p-type FETs array with easy implemented way.

In conclusion, we demonstrate a vapor deposition method by using a Cu-Te intermediate to successfully grow aligned Te with high crystalline. This method provides great potential for growing high quality and single crystalline Te flakes. We present a reliable method to reduce the contact resistance of p-type 2D transistors using

standard laboratory technology. By adopting the ultrathin Se interfacial layer with semiconducting characteristics and the highest work function, we successfully suppress the metal-induced gap states and substantially reduce the Schottky barrier height.

List of Publications

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Chapter 1 Introduction

1.1 Background

The discovery of graphene and other two-dimensional (2D) materials have been a significant cornerstone in next-generation nano-electronics for semiconductor scaling down to nano-scale due to their layered structure and unique properties. The increasing trend of 2D research are reported[13]. These 2D materials play significant role in future nanoelectronics, optoelectronics and ultra-thin flexible devices. However, zero band gap quite limits its applications. In that case, the graphene-like 2D transition metal dichalcogenides (TMDS) like molybdenum disulphide (MoS_2), tungsten disulphide (WS_2) etc come into the researcher's field of vision. TMDs with the formula MX_2 (where M = transition metal and X = chalcogen), such as MoS_2, WS_2, and WSe_2, have recently attracted many interests due to their wide-ranging applications in electronics, optoelectronics and electrocatalytic, which is because their semiconducting properties can be tailored and their layer-dependent band gap properties[13, 16, 29-43].

The 2D layered materials could be synthesized through top-down and bottom-up methods. Among top-down method, mechanically exfoliation is one of the most widely used method to get few layer films from bulk phase[44-48]. From this method, the graphene has firstly been discovered in 2004 by Geim and his student Novoselov who were both won the Noble prize in 2010 because of the discovery of graphene[33]. After the discovery of graphene, many other graphene-like 2D materials have been also

searched and studied like MoS_2, $MoSe_2$, WSe_2 etc. Mechanical exfoliation is widely used because this method is much easier than other methods to acquire the thin flake, but the thickness and size are random which limit the applications of such 2D layered materials. Regarding to bottom-up synthesis method, there are two methods usually used which is hydrothermal synthesis and vapor phase deposition process respectively. In traditional hydrothermal reaction process, MoS_2 is often synthesized in a Teflon-coated autoclave from different Mo and S precursors with deionized water as solvent. The generally used Mo precursors are $(NH_4)_6Mo_7O_{24}$, MoO_3, and Na_2MoO_4, and S precursors include NH_2CSNH_2, elemental sulfur, KSCN, $Na_2S_2O_3$ etc. After hydrothermal reaction, the nanostructure MoS_2 (nanosheet, nanoflower, nanoparticles etc) can be successfully synthesized from all these precursors mentioned but the topography and thickness are both difficult to be well controlled[49-54]. Another inevitable shortcoming is that these as-synthesized nano materials have poor crystallinity and large number of defects which show poor properties that greatly affect the applications of the as-synthesized nanomaterials. Intercalation method is another top-down process to get 2D TMDS because they have weak vdW interlayer interactions to be intercalated[55-58]. There are many intercalation methods like gaseous, non-electrochemical solution and electrochemical methods. For gaseous intercalation methods, alkali metal, halogen compounds, and some organic molecular are usually to be intercalated into these layered materials at different temperature regarding to both non-electrochemical solution and electrochemical methods, there would be chemical

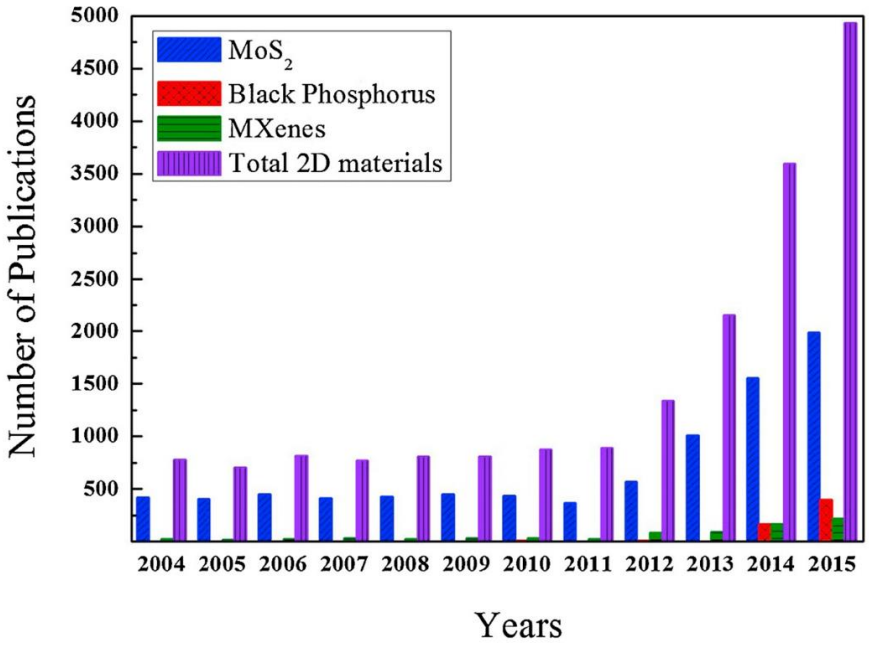

Figure 1.1 The number of publications about 2D materials in recent years[13].

reaction during the intercalation which will introduce strong doping in the layer or between the two sandwiches layer. These shortcomings greatly limit the device applications of these materials from intercalation methods. Nevertheless, vapor phase deposition is a common way to grow large scale, high quality and thickness-tunable layers. Many research groups have reported the vapor phase deposition to synthesize the library of TMCDS, especially for Liu Zheng's group. They demonstrated a general growth process to grow hundreds of TMDS. The salt (NaCl, KCl) was introduced to the growth system aims to decrease the melting point of the metal precursors due to the formation of the metal oxychlorides which has lower melting point comparing to the pure metal or metal oxide. This universal salt-assisted chemical vapor deposition method not only can grow TMDS, but also their heterostructures with high crystallinity

and less defects, which quite meaningful for exploring emerging materials and their applications[43]. However, the as synthesized library of TMDS do not have large scale. The reason may be the growth conditions are difficult to be controlled because there are many impact parameters (growth temperature, growth time, carrier gas, gas flow, system pressure etc) during the material grow process[59-63]. Hence, the wafer scale synthesis and thickness-tunable synthesis of such 2D layered materials are still challenging. To explore new and universal material synthesis methodology is urgent for next generation integrate circuit applications. Apart from these TMDs, emerging elemental two-dimensional materials joined two-dimensional world such as stanene, phosphorene, borophene, tellurene which have attracted great attention[64-84].

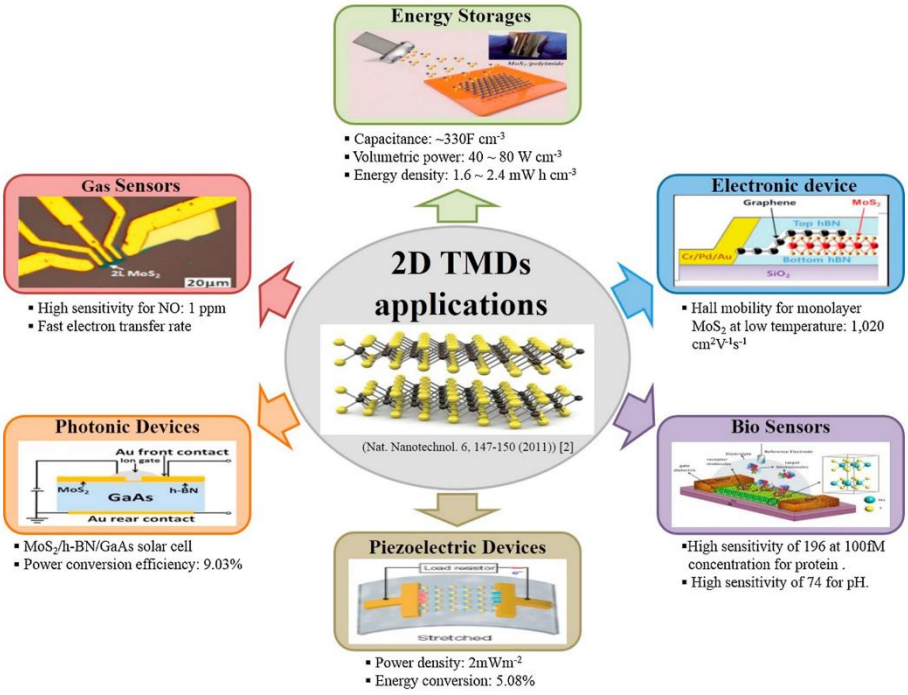

Figure 1.2 The device applications based on 2D TMDs materials[16].

2D materials are considered attractive for multiple applications, including high performance electronics, photonics, sensing, energy devices, topological insulator and neuromorphic computing applications[85-88]. These applications are inspired by their unique properties such as mechanical strength, tunable electronic structures, optical transparency, sensor sensitivities etc. Field effect transistor (FET) is one of the most important devices applications of TMDS in modern integrated circuits and chips[89-93]. A traditional FET device has four main parts, source, drain, gate and channel materials[94]. The working mechanism is that the current flowing from source to the drain is controlling by the gate voltage. Usually, two main figures are used to illustrate the performances of a FET device, which are transfer curve and output curve. Transfer curve (Id-Vg) is detecting the source drain current by applying a gate voltage bias and output curve is the relationship between the source-drain current and the source-drain voltage at various gate voltage. From these two curves, the basis properties could be analyzed, like the on-off ratio, subthreshold slope, threshold voltage, carrier mobility. On-off ratio is the current ratio between the on-state current and off-state current. The larger on-off ratio, the better device regulation. The subthreshold slope is the slope in the subthreshold region. The threshold voltage is the value of the gate voltage when the device transfers from off state to on state. Carrier mobility is another important factor to estimate the electrical properties of a transistor. A field effect transistor fabrication process is following. The most easily fabricated FET is back-gate transistor, which is just to deposit the source and drain onto the material on a dielectric layered deposited

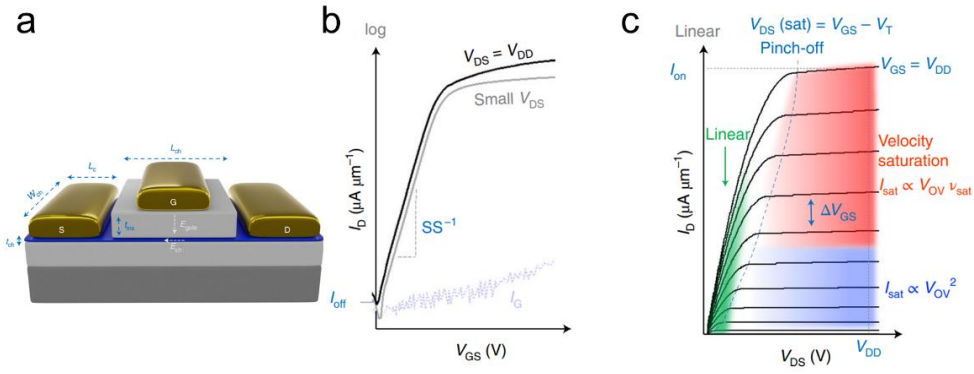

Figure 1.3 Basic device structure of FETs and typical electrical characteristic. (a) The diagram of typical 2D materials-based FETs, highlighting the counterparts of the device. (b) The transfer curve of n-type FET under different gate bias. The subthreshold regime is marked. (c) The output curves of the device with three regimes.

semiconductor substrate. Another common structure of transistor is top-gate transistor, which is just deposit the dielectric layer on the top of the channel material, rather than on the bottom of the channel[95-100]. These two structures of transistors are most fabricated and reported in recent papers. Electrical contact plays a dominant role in determining the performance of nanoscale devices. To establish low-resistance electrical contact to n-type two-dimensional (2D) semiconductors, researchers have adopted semimetal electrodes with low carrier density near their Fermi level and low work function[101, 102], including Bismuth (Bi)[103], Antimony (Sb)[17, 104]. However, it is still quite challenging to achieve low-resistance contact to p-type 2D semiconductors. Therefore, we focus our research on high performance p-type FET fabrications.

1.2 Introduction to p-type Tellurium

Among all the two-dimensional materials, the two-dimensional materials with the simplest elements are the most attractive. As an emerging two-dimensional single-layer material of group VIA elements, tellurene (Te) exhibits many exciting fundamental properties compared with phosphorene, graphene, and molybdenum disulfide, such as chemical and mechanical stability, band gap, and high carrier mobility. In addition, in further exploration, it was found that tellurene or tellurene based devices have excellent thermoelectric properties, piezoelectric properties, quantum Hall effect, and excellent optical properties, especially nonlinear optical properties, etc. The properties of tellurene can be tuned by strain, defect, edge and heterojunction effects[105-112]. Given so many unique properties, tellurene has attracted great interest since it was successfully predicted and prepared[113-115].

1.2.1 Properties of Te

Compared to its bulk counterparts, the 2D tellurium shows unique electronic and optical properties. Te is hexagonal crystal structure with helical chains along c-axis by the covalent bonding. It is easier for tellurium to form one dimensional chains and thick layers due to its unique crystal structure and strong interlayer force. Through the combination of DFT calculations and experiments, it is found that 2D Tellurium has a three-phase (α-, γ-Te) and tetragonal (β-Te) structure[115]. The formation mechanism of different phase is determined by the multivalency of Te. The α-Te and γ-Te phases

exhibit triplet and sixfold coordination structures, respectively. However, the β-Te phase has three-fold and four- fold coordination structures, and these findings suggest that Te has a variety of bond structures. Among these different crystal structures of Te, α-Te is confirmed as the most stable phase, and we focus on this phase study.

Te consists of chains of atoms in a triangular helix that is stacked together by van der Waals forces in a hexagonal array and has a 1D crystal structure instead of a layered 2D van der Waals structure. Furthermore, Te atoms only form covalent bonds with the two nearest neighbor Te atoms in the helical chain has a layered structure with strong

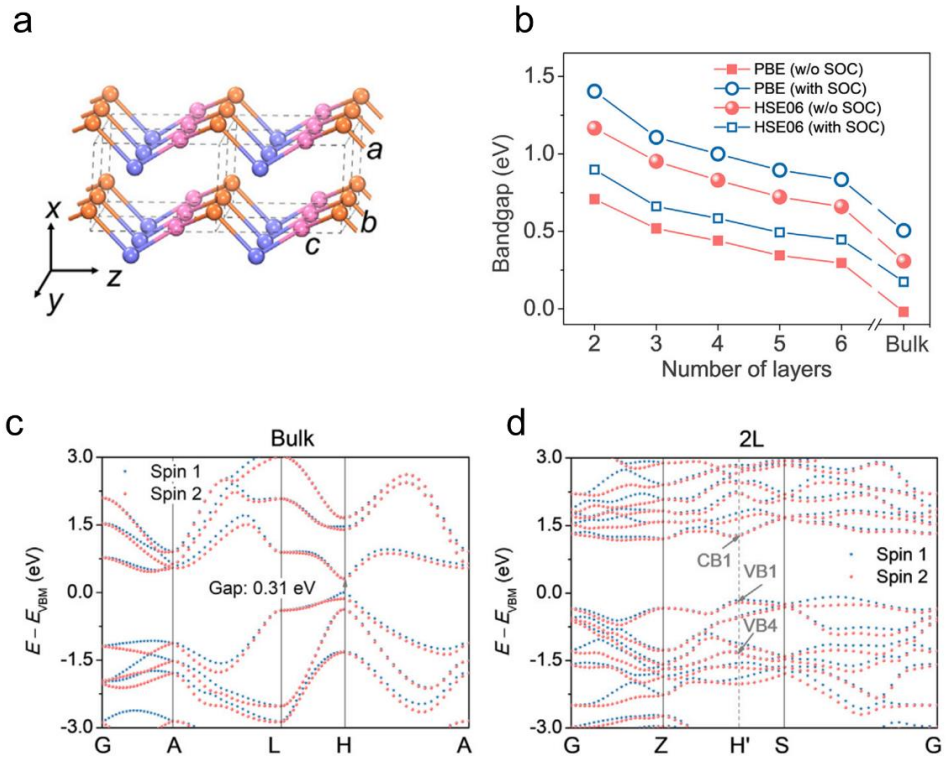

Figure 1.4 Crystal structure and electronic structure of Te (a) side view of Te structure. (b) The indirect band gap of Te with different number of layers. (c) The band structure of bulk Te with a gap of 0.31 eV. (d) The band gap of bilayer Te.

chemical bonds within the layers. When viewed along the x-axis, the sawtooth layers can be seen to stack together to form a three-dimensional structure through van der Waals forces.

1.2.2 Device applications of Te

2D tellurium has great application potential in high-performance 2D material-based electronic and optoelectronic devices[28, 116-122]. Thermally synthesized, environmentally stable quasi-two-dimensional tellurium nanofilms have been applied in mid-infrared photodetectors[123]. Prof Peter Ye's team introduced a high-performance field-effect transistor based on a solution synthesis method to prepare two-dimensional tellurium nanosheets. When the channel length is 3 μm, the drain current exceeds 300 mA/mm, and the on off ratio is about 10^5. When the sample thickness is about ~15 nm, the field effect mobility at room temperature is about 700 $cm^2/V/s$. At the same time, the two-dimensional tellurium exhibited excellent air stability, and the leakage current changed slightly after 55 days of exposure to the air without any encapsulation treatment. Maximum drain current exceeding 1.06 A/mm achieved by further reducing the channel length[12]. Other research teams also introduced the use of Au/Al_2O_3 optical cavity substrate to further enhance the absorption of the device. In addition, by adjusting the thickness of the Al_2O_3 spacer layer, the photo response wavelength of the device can be tuned from 1.4 μm (13 A/W) to 2.4 μm (8 A/W), and the non-zero photoresponsivity is as high as 3.4 μm. The responsivity as a function of various laser

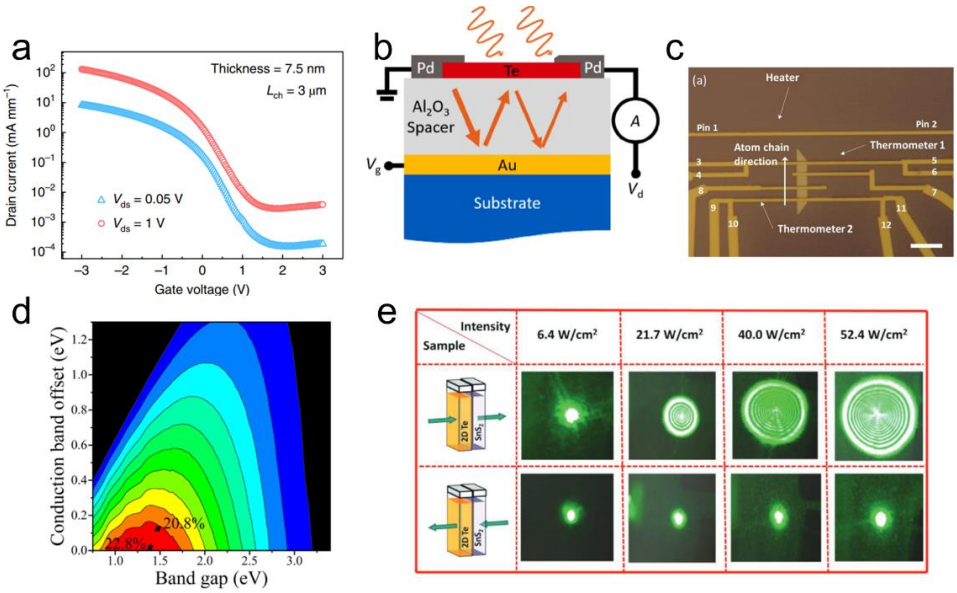

Figure 1.5 The device applications of Te. (a) The transfer curve of p-type Te FTEs[12]. (b) The Te-based near-infrared photodetector[18]. (c) The Te-based device structure and pin-out diagram[24]. (d) Power conversion efficiency of Te-based solar cell[27]. (e) Images of the diffraction rings of Te-based photodiode[28].

wavelengths was measured at temperatures of 78 K and 297 K. The responsivity peaked at λ=1.7 μm, which was 27 A/W (78 K) and 16 A/W (297 K), respectively. The corresponding calculated specific detectives are 2.6×10^{11} and 2.9×10^{9} at 78 and 297 K, respectively. The increase in specific detectivity at 78 K is due to more effective suppression of noise currents than at room temperature, which is inversely proportional to specific detectivity[18]. These results demonstrate that the solution fabricated 2D-Te nanosheets are suitable for high-performance photodetection covering the entire near-infrared band. A metal-tellurene-metal terahertz photodetector was also prepared, realizing light detection under millimeter-terahertz waves. The results show that the

terahertz photodetector based on logarithmic antenna tellurene has a high photoresponsivity (40 mA/W, 0.12 THz) at zero bias, a response time of 8 μs, and noise equivalent power (NEP) is 4 $pW \cdot Hz^{-0.5}$. The research results provide a new development path for high-performance room temperature terahertz light detection. Field-effect transistors based on two-dimensional tellurium have high uniformity, making it possible to be further applied to logic gates and circuits. The author's team introduced a logic gate and circuit based on a p-type two-dimensional tellurium field effect transistor. The gains obtained under Vdd=1 and 2 V are 22 and 38, respectively. Furthermore, as the number of FETs in the loop increases from 35 to 39, the maximum output voltage loss decreases from 6 % to 3 %. Many experimental and theoretical studies have shown that two-dimensional tellurium has superior thermoelectric properties, which is conducive to the further development of a new generation of thermoelectric devices based on two-dimensional tellurium. Some research introduced a thermoelectric device based on two-dimensional tellurium. When the incident light power is 3 mW, the current generated by the thermoelectric device is as high as 3 μA, which is much larger than previous reports[24]. In addition, 2D tellurium can also be applied to solar cells and achieve a high energy conversion efficiency of 20.8 %[27]. Due to the strong interaction between light and matter from the visible to infrared range, unique 2D Te-based nonlinear photonic devices with room temperature stability can be applied as photonic diodes and all-optical switches. These photonic diodes can be used in nonreciprocal optics propagation of telecommunications or integrated photonics. For

all-optical switching operation, the "ON" and "OFF" modes can be successfully realized in 2D Te-based light-modulating optical devices[28]. Due to the apparent two-photon absorption behavior with large energy excitation in the visible light range, tellurene can be used as an optical limit material to protect sensitive optical devices and human eyes[124].

1.2.3 Recent progress of Te growth

To expand the device applications of Te, develop high crystalline and large size of Te film is necessary. As mentioned, due to the unique crystal structure of Te, it is usually to form the 1D structure and 2D structure growth is still challenging.

1.2.3.1 1D structure of Te growth

Solution synthesis method is commonly used to synthesize nano materials. Mayers team reduced orthotelluric acid or tellurium dioxide using hydrazine. This process was carried out at a range of temperatures from 90 to 200 °C[19]. This method can form 1D structures, exhibiting various morphologies (spines, filaments, needles and tubular structures) by different temperatures. Another hydrothermal process was also reported to form Te nanobelts[14]. By disproportionation of sodium tellurite in aqueous ammonia with a temperature of 180 °C, the thickness of the as-synthesized Te nanobelts thin to 8 nm with width of 30 to 500 nm. During the hydrothermal process, the polymer surfactant such as poly (vinyl pyrrolidone) (PVP) and poly (vinyl alcohol) (PVA) has been as assistant. With the assistance of these polymers, the 1D Te morphology can be

modulated by amount of the polymer assistance. The solution method is usually used because of its low reaction temperature and easier modulation process. However, there are many parameters like precursor concentrations, reaction temperature, pressure, polymer surfactant and amount etc can affect the final morphology of the results. In addition, the residues after hydrothermal process can also affect the material quality and characteristics.

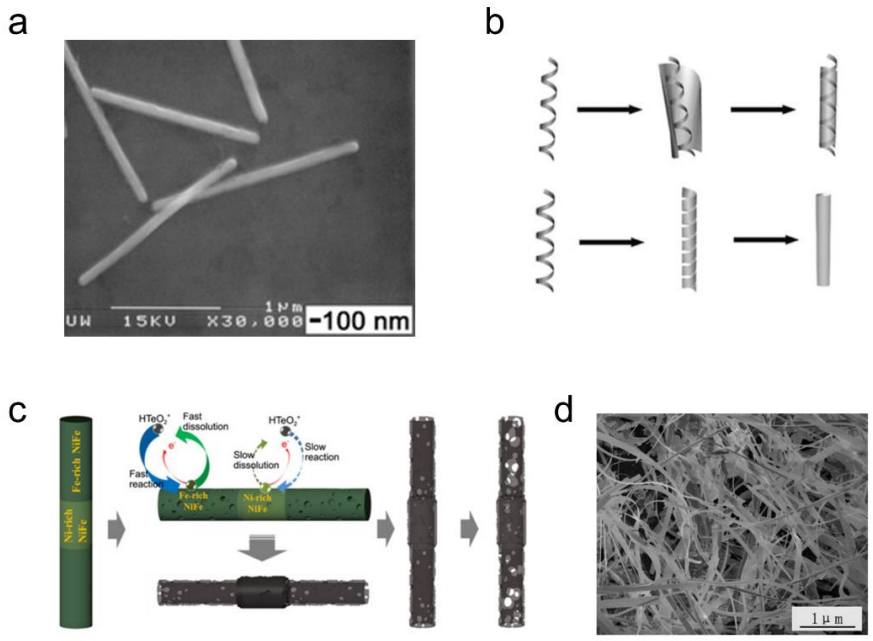

Figure 1.6 One-dimensional Te samples prepared by solution and vapor methods. (a) The 1D Te morphology prepared by hydrothermal method by polymer assistance under different PH value[14]. (b) The growth mechanism of Te nanobelts with orthotelluric acid reduction[19] (c) The Te nanotubes growth mechanism[22]. (d) The morphology of Te nanobelts from H_2O and Al_2Te_3 reaction[25].

Vapor deposition is another method to grow 1D materials. Due to the unique of quasi 1D structure of Te, one early research reported that by sublimation of solid Te precursor, the Te whiskers can be achieved by controlling the temperature of the growth substrate[125]. Another similar work also reported the Te microtubes by Te powder evaporation. The Te chains pack together then form the tube morphology, with the diameters of hundred micrometers and length of centimeter scale[22]. Chemical vapor deposition (CVD) method to grow Te nanobelts with thickness of 10-20 nm has also been demonstrated using H_2O and Al_2Te_3[25]. This reaction temperature is 500°C using Ar as carrier gas.

The conventional hydrothermal process and vapor deposition method have been successfully used to grow 1D Te. The morphology of the Te products is influenced by many parameters, such as growth temperature, precursor, carrier gas etc. In addition, the products of Te samples are usually limited to 1D structures, that limit the development of 2D Te growth and applications.

1.2.3.2. Growth of 2D Te

After realizing that 1D Te is difficult to controlled growth, several research works focus on solve this problem. Wang's group demonstrated a solution method by using hydrazine hydrate assisted with PVP ligand in alkaline solution through a reduction of sodium tellurite at temperature ant the range of 160 to 200 °C[12]. This method has successfully achieved large size, high-quality 2D Te flakes. The thickness of the as-grown Te flakes is around 10 nm. By adjusting the PH value of reaction solution, the

thickness of Te products can be further reduced. In this method the PVP amount is essential to the product of the Te morphology. A suitable level of PVP concentration can control the growth rate, promoting the 1D Te to 2D growth. The 1D growth of Te is dominated by the kinetic effect, while the 2D growth is the balance of both thermodynamic and kinetics. A well-controlled of kinetic and thermodynamic growth Te finally make Te shows 2D morphology.

The conventional hydrothermal method successfully synthesizes the 2D Te flakes. The complicated growth process and the products with limited size still limit the large-scale Te growth. Vapor deposition method may have more potential to grow large scale

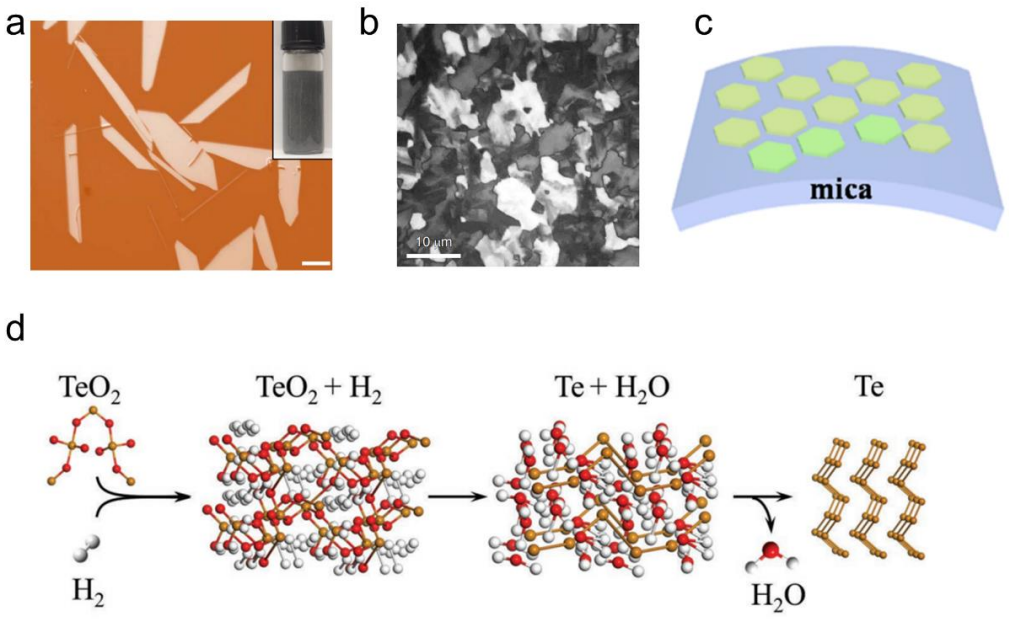

Figure 1.7 Two-dimensional Te samples prepared by solution and vapor methods. (a) Te flakes prepared by reduction of sodium tellurite[12]. (b) The optical image of Te films[21]. (c) Schematic of hexagonal 2D Te flakes on flexible mica substrates[23]. (d) The schematic of Te growth by reduction of TeO_2[26].

2D materials like graphene and MoS_2. Ali javey's group reported a cryogenic PVD process to acquire large scale Te films with thickness of 8 nm at the temperature of -80 ℃ and 30 nm at the temperature of -60 ℃[21]. The domain size of the Te films is decreased to 3 μm^2 by rising the substrate to -10 ℃. The substrate temperature determines the domain size and morphology of the Te films. If the temperature of the substrate is at room temperature, the Te morphology is small nanoparticles. Another group also reported a PVD method to grow hexagonal 2D Te flakes on mica substrate. The mica substrate has clean and flat surface which is good for 2D materials growth. The thickness range of Te flakes is 30-80 nm, that is still very thick for device fabrication[23]. Zhang et al demonstrated hydrogen-assisted CVD method to grow thin layer Te film[26]. They successfully acquired the Te flakes with thickness of 5 nm.

1.3 Contact engineering for field effect transistors

The complementary metal oxide semiconductor (CMOS) technology is based on field effect transistors (FET). The thin-layer transition metal dichalcogenides (TMDs) have great potential to realize high-performance FETs[126-131]. The development of transistors promotes device speed and integration. The new materials, and new technology to ensure device integration are emerging in recent years. Under the guideline of Moore's law, the semiconductor industry has entered the 10 nm technology node. Theoretical calculation shows that thinning the thickness of the channel is the foundation of the device size continues to decrease. Based on the material quantum

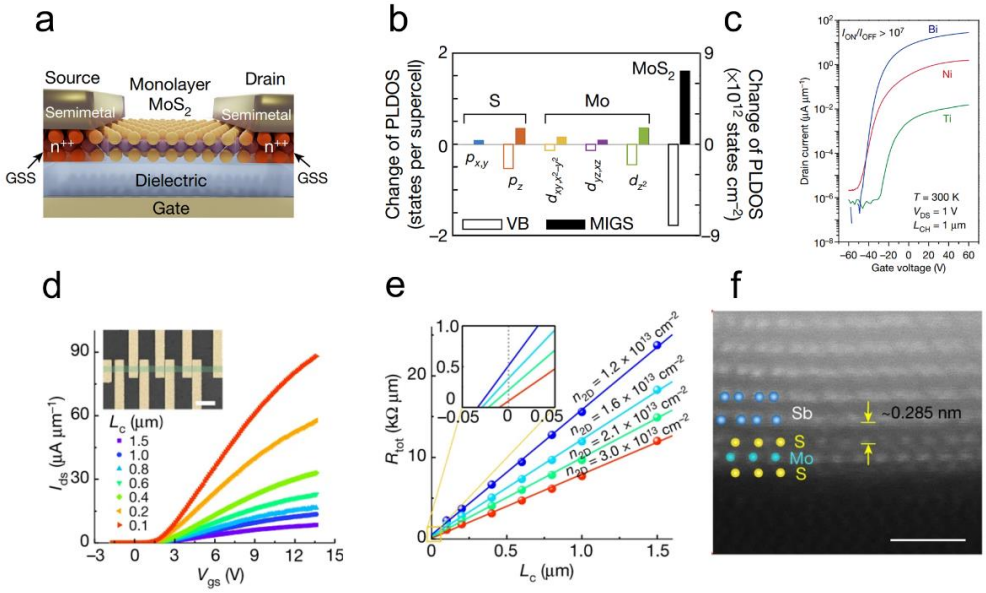

Figure 1.8 Recent works for n-type contact engineering. (a) The device structure of MoS2 FETs using Bi contact. (b) The MIGS comparison between Bi contact and Au contact. (c) The transfer characteristics of different contacts[11]. (d) Te transfer characteristics of Sb contacted MoS_2 FETs. (e) The contact resistance measured by transmission line method. (f) The cross-sectional image of Sb-MoS_2[17].

confinement effect, the traditional bulk material thickness reduced to less than 5 nm is very difficult. The intrinsic thickness of two-dimensional semiconductor material of less than 1 nm ultra-thin body makes the device application brought huge potential in future electronics. However, the performances of FETs based on 2D materials are limited by many other factors, such as interface scattering, high contact resistance, metal induced gap states etc. The metal-induced gap states (MIGS) and the energy barrier at the metal-semiconductor interface usually lead to high contact resistance and Fermi-level pinning, which restricts the performance improvement of devices[126-128, 132-

[140]. The mechanical transfer of metal electrodes is method for device fabrication. This method could reduce the MIGS but increase the tunneling resistance The excellent n-type FETs have been achieved by depositing low-work function metals and semimetal to suppress the MIGS and energy barrier height.

Recent studies have shown the advances of electrical contact to n-type two-dimensional (2D) semiconductors with low-work-function Bismuth (Bi) and Antimony (Sb) electrodes[11, 17, 141]. When a metal is close to the semiconductor material, the wavefunction of the metal may perturb the wavefunction of semiconductor, resulting the rehybridizations of the original wavefunction of semiconductor. Lain-Jong Li et al reported ultralow contact resistance of n-type FETs by using semimetal Bi with low work function the contact regime[11]. Compared to DOS of a common metal, the semimetal has a lower DOS near the Fermi-level. When a semimetal contacts a semiconductor, the lower DOS of semimetal can reduce the perturbation effect compared to metal contact semiconductor, leading to the reduce of MIGS. In addition, the low work function of Bi can reduce the SBH due to the band alignment of Bi and MoS_2. Therefore, the final contact resistance can be great reduce to 123 Ω μm and the ON-state current density reach 1.135 mA μm for monolayer MoS_2. Xin rang Wang's group use semimetal Sb (0112) as the contact and push the contact resistance to quantum limit. They further realize the contact resistance to 42 Ω μm for n-type MoS_2 FETs[17]. To fabricate low-resistance contact p-type FETs, Manish's group use high

work function metal Pt and Pd as contact[142]. The SHB can be effective reduced, ut the MIGS is non-negligible due to the high DOS of metal at the Fermi-level. Xingfeng Duan's group reported a lithography-free approach to fabricate sub-100-nano-channle-

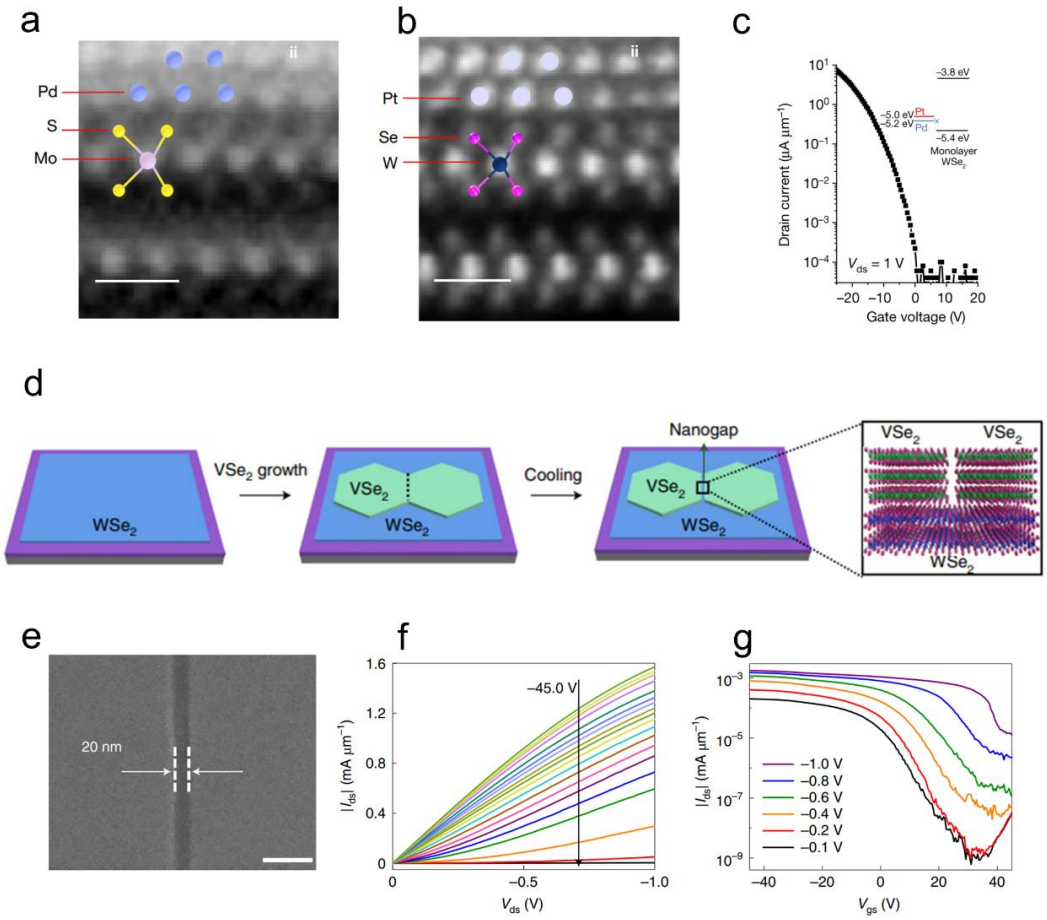

Figure 1.9 Recent works for p-type contact engineering. (a) The cross-sectional image of Pd-MoS_2. (b) The cross-sectional image of Pd-WSe_2. (c) The transfer curve of WSe_2 FETs with Pt contact, existing pure p-type characteristics[15]. (d) The schematic of WSe_2 FETs with VSe_2 contact. VSe_2 grow epitaxially on the top of WSe_2 layer to form the natural channel gap. (e)The SEM image of the VSe_2 contact WSe_2 FETs with channel length of 20 nm. (f) The output curves of WSe_2 FETs with channel length of 20 nm. (g) The transfer curves of WSe_2 FETs with channel length of 20 nm[20].

length bilayer WSe_2 FETs[20]. They directly growth metallic VSe_2 on WSe_2 to form the van der Waals contact. The ON-state current density is 1.72 mA μm^{-1} and the contact resistance is 500 Ω μm at 20-nm-leng channel. Overall, to realize the high-performance FETs with low-resistance contact is essential for future electronics.

1.4 Research Objectives

1.4.1 Untra-thin 2D Te growth

After the graphene was prepared by mechanical exfoliation, many other 2D materials have been studied. The family of 2D materials include various n-type semiconductors than can be applied to complementary devices. However, the application of p-type semiconductor is still limited. In recent years, BP as a typical p-type semiconductor have been studied but it has poor air stability, that limit its applications Te is a p-type semiconductor with higher stability than BP. Due to the unique crystal structure and properties, it has great potential for n-type FETs for future complementary circuits. Due to the intrinsic 1D chain structure of Te, 2D morphology is difficult to form. Although some researcher reported several methods like hydrothermal process and vapor deposition method to grow high quality and large area films, it is still challenging to acquire thin layer Te flakes.

In our work, we demonstrate an alloy-buffer-controlled method and we successfully acquire the single crystalline triangle Te flakes with thickness < 10nm. This method has not been reported before.

1.4.2 P-type contact engineering

The complementary metal oxide semiconductor (CMOS) technology is based on the complementary of both n-type and p-type FETs. The thin-layer 2D transition metal dichalcogenides have great potential to realize high-performance n-type and p-type field effect transistors. An important issue for high performance FETs is the large contact resistance. Recently, several strategies for low-resistance contact n-type FETs have achieved by using semimetal as the contact to reduce the MIGS. The high-performance p-type FETs with low-contact resistance is still needed to study.

The recent reported works for p-type FETs fabrication usually use high work function metals, that can reduce the SBH by band alignment. However, the intrinsic issue that the metal induced gap states are not solved due to high DOS of metal with zero band gap near the Fermi-level. Compared to metal, semiconductor Se has band gap and high work function. We introduce an ultrathin Se interfacial layer at the contact regime. The barrier heigh and the metal induce gap states can be great reduces. This Se interfacial layer strategy can also be extended to other p-type semiconductors.

1.5 Structure of Thesis

The structure of this thesis is outlined as follows:

Chapter 1: Introduction. In this chapter, the development of 2D materials and their applications are firstly introduced. Next, we review the recent works about 2D material synthesis by using different methods and their limitations. We then fucus on the p-type

elemental Te. The basic crystal structure, properties and device applications then be reviewed. Afterwards, we review some works about the p-type Te growth and the potential for 2D Te growth. Next, we discuss the recent development of contact engineering of complementary n- and p-type transistors. Some typical works for low contact resistance are demonstrated. The research objectives of this thesis then are listed.

Chapter 2: Alloy-buffer-controlled van der Waals epitaxial growth of aligned Tellurene. In this chapter, the aligned 2D Te with thickness of < 10nm are achieved by alloy-buffer-controlled growth. The alloy formation and the low lattice mismatch between mica substrate and Te promote the single crystalline and aligned 2D Te growth. The detailed material characteristics and theoretical calculations are discussed in this chapter.

Chapter 3: Introduction. Low-resistance contact to p-type semiconductors with Se interfacial layer. In this chapter, we introduce an ultrathin (1.2 nm) Selenium (Se) interfacial layer at the contact region to achieve low-resistance p-type FETs. The semiconducting characteristics and high work function of Se attribute to the high-performance p-type FETs. We characterized the device performance at room temperature to compare the ON-state current density and contact resistance. Low temperature test is performed to extract the barrier height. In addition, we also perform the theoretical calculations to understand the contact mechanism of Se interfacial layer. All the experimental results and theoretical calculations confirm the Se interfacial layer strategy can great optimize the device performance of p-type FETs.

Chapter 4: Conclusions and Outlooks.

Chapter 2 Alloy-buffer-controlled van der Waals epitaxial growth of aligned tellurene

2.1 Introduction

Due to the atomic level thickness and dangling band free of 2D materials, they exhibit unique physical and chemical properties[42, 143-149]. Recently, group VI elemental 2D materials such as Se and Te attracted many interests because of their unique crystal anisotropy, broadband photo response characteristics, high carrier mobility, that make them very promising candidates for future optoelectronics[150-157]. Te has a band gap of 0.34 eV in bulk phase and 1 eV in monolayer. Along c-axis, Te atoms are connected by covalent bond, that make Te to form a quasi 1D trigonal lattice structure.

In recent years, the free standing 2D flakes have been successfully synthesized by conventional hydrothermal process[158]. However, this method usually introduces residues and impurities after the synthesis process. In addition, this method is incompatible with modern semiconducting technologies. Large size Te film have also been grown by thermal evaporation. The grown Te product films are poly crystalline, and this thermal evaporation process need very stringent conditions such as low pressure and low temperature assisted by liquid nitrogen[21]. Among these growth method, chemical vapor deposition (CVD) is a widely used method to grow large area and high quality 2D materials[159-163]. The solid precursors are usually used as the source in the vapor phase deposition process, which make the distribution of the source vapor

show temporal and spatial non-uniform. This limitation is present great challenge for high uniformity 2D material growth. Besides, as the unique lattice structure of Te, its high anisotropic characteristics is another challenge to grow aligned and large size Te flakes onto a substrate.

In our work, we have successfully acquired ultrathin 2D Te flakes (<10 nm) by a conventional CVD process assisted by alloy buffer method on mica substrate. We firstly put a piece of Cu foil as the buffer source and then locate fresh-cleaved mica substrate onto the Cu foil. The Cu foil and mica substrate are very close to each other. The Te vapor is firstly adsorbed onto the Cu foil due to the strong adsorption energy. Then at a high temperature the Te vapor can be released and transfer to the mica surface to epitaxially grow. By introducing the Cu foil as an intermediate, the vapor source can be ensured to distribute both temporal and spatial homogeneous during the whole deposition process. After growth, the aligned Te products show triangle shapes on the mica substrates. TEM results confirm the growth direction that the (001) plane of Te grow along the (600) direction of mica due to the strong binding energies from theoretical calculations results. Our work demonstrate a strategy for growing 2D aligned single crystalline Te on mica substrates.

2.2 Methods

2.2.1 Material growth

A tube furnace was used to grow the 2D Te flakes under ambient pressure. The solid source in the upstream is Te particles which was in a ceramic boat The substrate is the mica substrate that was put in the hot center of the zone. Firstly, we flushed the tube with Ar for 10 minutes. The gas flow is 300 sccm (standard cubic centimeter per minute) then changed to 50 sccm during the growth process. The growth temperature is 600 ℃ and maintained tome is 10 minutes. After the growth finished, the tube furnace was cooled down to room temperature.

2.2.2 Mater characterization

The morphology of the Te flakes was characterized by an optical microscopy (Leica DM 1750M). The thickness was characterized by atomic force microscopy (SPM8, Bruker NanoScope 8). The WITEC Raman (Alpha 300R, 532 nm) was used to collect the Raman spectra. The atomic images were characterized by scanning transmission electron microscopy (Jeol JEM-2100F). The EDS mapping and SEM images were analyzed from scanning electron microscopy (SEM, TESCAN VEFA3).

2.2.3 Preparation of TEM samples

In our work, we analyzed the growth direction of Te on mica substrate by acquiring the diffraction patterns of Te and mica substrate at the same time. We used polymethyl

methacrylate (PMMA) to transfer the Te samples onto Cu grid to prepare the TEM sample of Te. Step 1: Spin-coated the PMMA layer with 500 rpm, 5 s following by baking process under 150 ℃ with 5mintes. Step 2: The PMMA-coated Te sample on mica were immersed into DI water for 2 hours. After around 2 hours, separated the PMMA-coated Te film onto the Cu grid. Step 3: Used acetone to remove the PMMA. For preparation pf the Te-mica overlapped sample, we exfoliated the Te-mica sample to an very thin layer and then used a double folding TEM grid to retain the Te-mica sample.

2.2.4 DFT calculations

We performed the theoretical calculations by using Vienna ab initio simulation package[164]. The exchange−correlation energy is applied by Perdew−Burke−Ernzerhof parametrization[165]. We firstly calculated the adsorption energy of Te on Cu foil and mica. We take Cu (110) and mica (001) planes as examples. We relaxed the slabs of Cu (110) and mica (001) planes to make the force less than 0.01 eV/Å and energy tolerance less than 10^{-5} eV on each atom. The k-points were set as 4 × 4 × 1 Monkhorst−Pack k-point mesh with gamma centered. The **Equation 2-1** of the adsorption calculation is defined as below:

$$E_{ads} = E_{total} - E_{slab} - N * E_{Te} \qquad (2-1)$$

where E_{ads} is the adsorption energy, E_{total} is the total energy of Te-Cu or Te-mica. E_{slab} is the energy of slab model. E_{Te} is Te atom energy. N is the number of Te atoms adsorbed on slab models.

We also calculated the interaction between mica and Te. We built the mica surface slab and Te chains model then fully relaxed them. The surface of mica (001) is covered by half K atoms to make the surface stable. The force and energy tolerance were set as 0.01 eV/Å and 10^{-4} eV respectively. The 2 × 2 × 1 Monkhorst−Pack k-point mesh was set for k-point samples. The binding energy of Te and mica is shown **Equation 2-2** as below:

$$E_b = \frac{E_{total} - E_{sub} - E_{Te}}{N} \qquad (2-2)$$

where E_b is the binding energy, E_{total} is the total energy of Te-mica, E_{sub} is the energy of mica (001) slab, E_{Te} is the energy of Te chains, N is the number of Te chains, here N is 3.

2.3 Results and discussion

2.3.1 Alloy-buffer-controlled growth

As illustrated before, the solid source distribution is both temporal and spatial non-uniform in a conventional vapor deposition system. For the conventional method, the solid source is usually located in the upstream or face-down to the substrate. At the beginning of growth, the amount of the solid source is predefined. During the growth

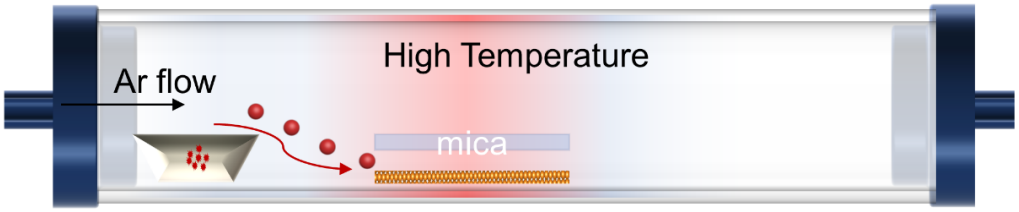

Figure 2.1 The schematic diagram of Te growth by CVD process in a tube furnace. The precursor is Te particles located in the upstream. The substrate is put on the high temperature center.

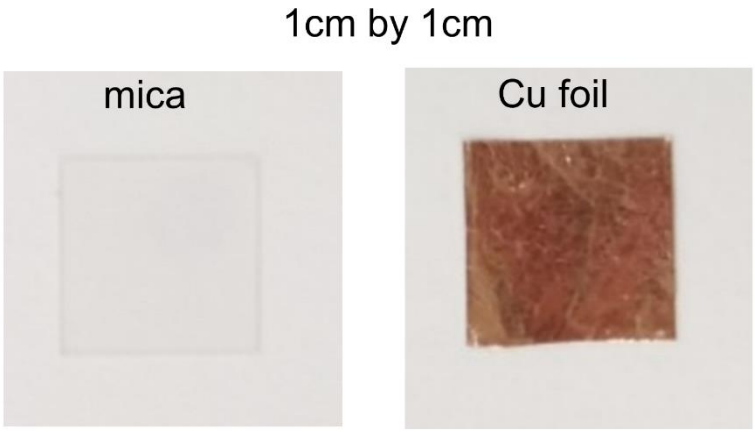

Figure 2.2 The images of transparent mica substrate and Cu foil. The mica substrate is put onto the top of Cu foil with close distance for space confined growth.

process, the amount of the source will decrease gradually and the distribution of the vapor in the tube are changed compared to the beginning of the growth[166, 167]. The concentration of the vapor will decrease with the decrease of the solid amount. In addition, the distribution of the vapor concentration is also non-uniform due to the typical horizontal configuration of a conventional tube furnace. To overcome the

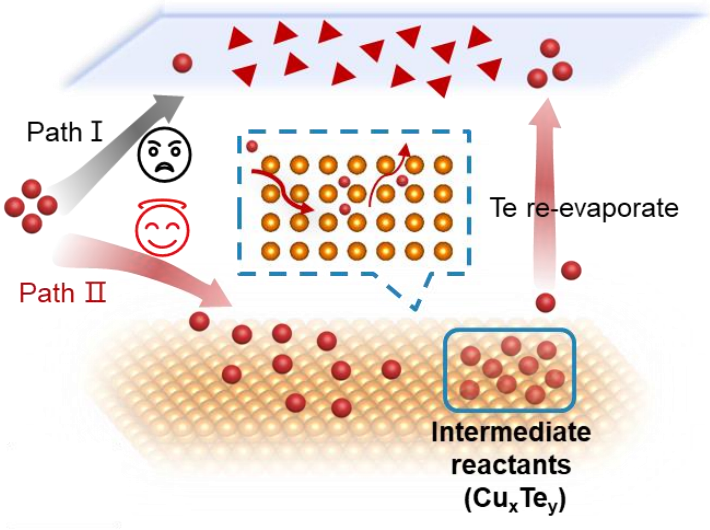

Figure 2.3 The detailed growth steps of Te growth with different paths.

abovementioned disadvantages of conventional vapor deposition method and precisely control the amount of solid precursor, we introduce a Cu foil as an intermediate source to grow high quality Te flakes. The grow schematic is shown in Figure 2.1. A piece of 1×1 cm^2 freshly cleaved mica substrate on a same size Cu foil is in the center zone of the tube furnace. The image of the mica substrate and Cu foil are shown in Figure 2.2. Due to the limited gap between mica substrate and Cu foil, the distribution of Te vapor can be controlled spatially and temporally uniform, which were not solved in conventional method.

The detailed vapor process of our design is illustrated in Figure 2.3. The Te particles are loaded in the upstream. With the temperature increase, the source was evaporated and move to the substrate regime. These Te vapors were adsorbed onto the mica surface and Cu foil. To compare the adsorption energy of Te-mica and Te-Cu, we

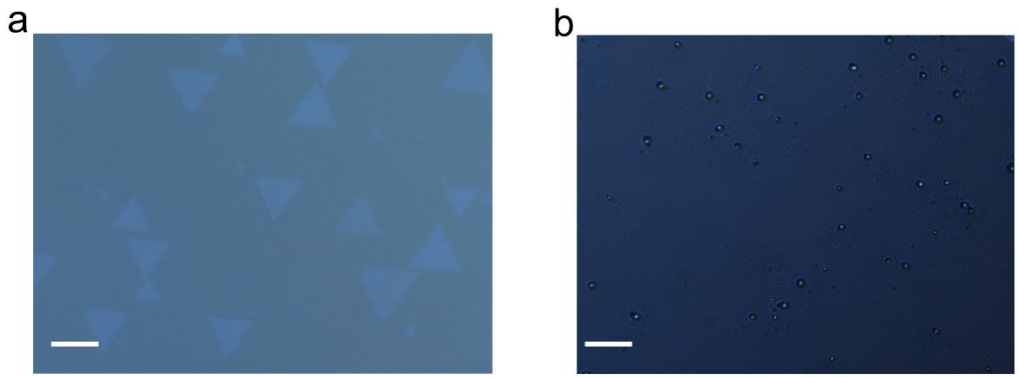

Figure 2.4 The experimental results of Te growth with and without Cu foil. (a) The optical image of Te flakes on mica substrate. With Cu foil assisted growth, the triangle Te flake can be observed on mica substrate after growth. (b) The optical image of mica substrate without using Cu foil. No Te flakes are observed. The scale bar is 10μm.

performed theoretical calculations. A single Te atom adsorbed in Cu and mica energy are -3.1 eV and -2.26 eV. The adsorption energy of Te on Cu foil is more negative, confirm that the strong adsorb interaction. We can conclude that the path II is a more thermodynamical favorable path. So the next step is that most Te atoms move into the Cu foil and then form the Cu-Te alloy at a suitable temperature range. As the growth time prolongs, the adsorbed Te atoms then re-evaporate from the alloy and transfer to the surface of mica substrate to epitaxially grow. The growth temperature was set to 600 ℃, which is higher than Te (449 ℃) and lower than Cu (1083 ℃) to make Te can be evaporated and Cu cannot be evaporated. We characterized the EDS analysis and found that there is no Cu signal in the as-grown Te flakes (Figure 2.4 a). Finally, the aligned and high-quality Te flakes can be acquired on the mica substrate. We also did

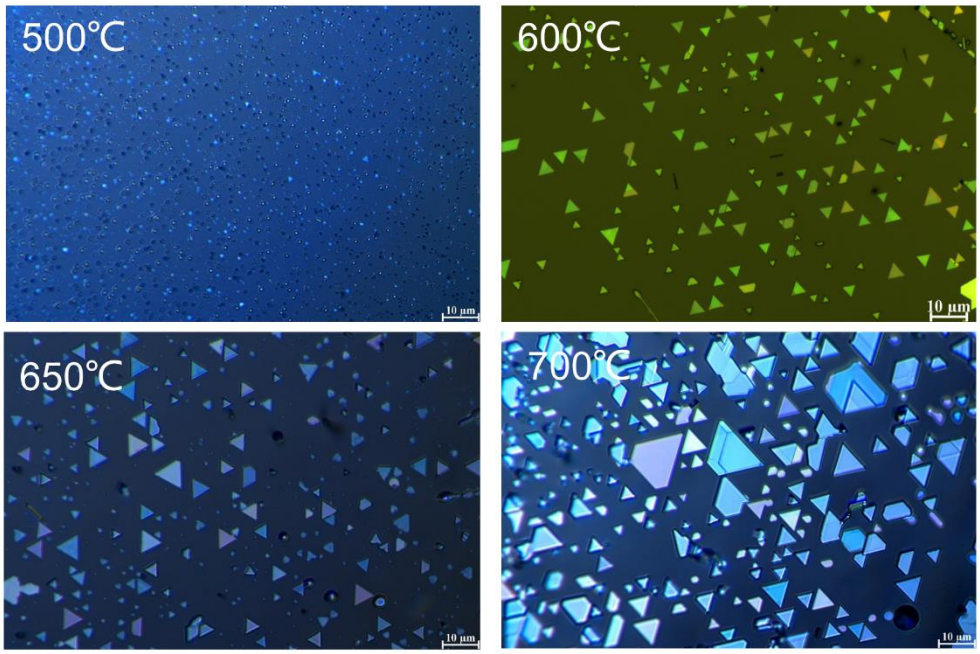

Figure 2.5 The temperature-dependent of Te growth. As temperature increases, the thickness increase. The optimal growth temperature is around 600 ℃.

the controlled experiment that without Cu as assistant, the number of Te flakes on mica substrates were nearly not observed, that means the Te vapor are limited adsorbed to grow on mica substrates. (Figure 2.4 b). We then studied the growth temperature (Figure 2.5) and time (Figure 2.6) for Te growth. When the growth temperature and growth time is 500 ℃ and 1 minute, we can observe that there are a few Te samples on mica substrate. At that temperature, the Cu-Te alloy cannot form so the Te vapor from Cu foil is not efficient, which limit the Te grow on mica. If the temperature and growth time increase to 700 ℃ and 30 minutes, the Te flakes are too thick because of the oversupply of re-evaporated Te vapor from Cu-Te alloy. After investigating the growth conditions with different growth temperatures and growth duration time, we found that 600 ℃ and 10

minutes should be a proper condition for thin Te growth. At this growth condition, the alloy formation can properly form to supply Te vapor for high quality Te growth.

The formation of the quasi 1D structure is due to the covalent bond connections of Te atoms along the c-axis. The optical images of the as-grown Te products on mica substrate in represented in Figure 2.4a. All the Te flakes exhibit triangle shapes and have specific growth directions on the mica surface. We characterized the thickness of Te flakes by AFM shown in Figure 2.7a. The as-grown Te flakes have ultrathin thickness (<10 nm) due to the confined growth strategy. With Cu foil as assistant, the amount of Te vapor is limited so the final thickness is ultrathin. The Raman spectra was

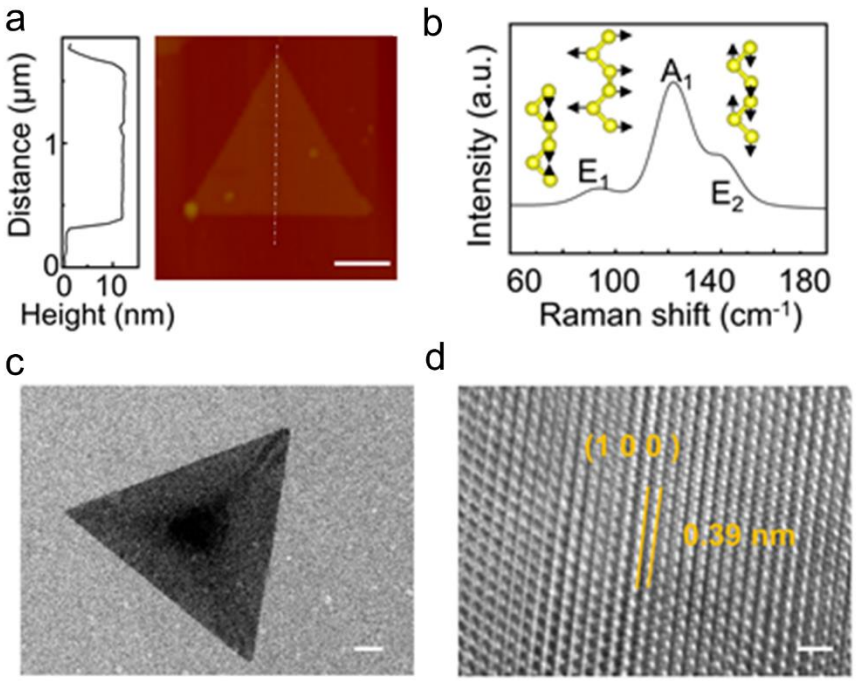

Figure 2.7 Material characterizations of as-grown Te flakes. (a)The AFM image of Te with thickness of ~10 nm. (b)Raman spectra of Te flake showing three vibration modes. (c) The TEM image of triangle Te flake. The scale bar is 0.5 μm. (d) The HRTEM of Te flake. The scale bar is 1 nm.

also analyzed in Figure 2.7b. There are there main Raman peaks of Te, 92, 120, and 140 cm^{-1} respectively. The bond-bending along z-axis of Te is the strongest A_1 120 cm^{-1}. The other two peaks correspond to E mode that is the interchain interaction mode. To characterize the crystal structure of the Te flakes, we also performed the TEM characterization. The TEM image of Te flakes is shown in Figure 2.7c. The Te flakes exhibit triangle shape. The high-resolution atomic image of Te atoms is in Figure 2.7d.

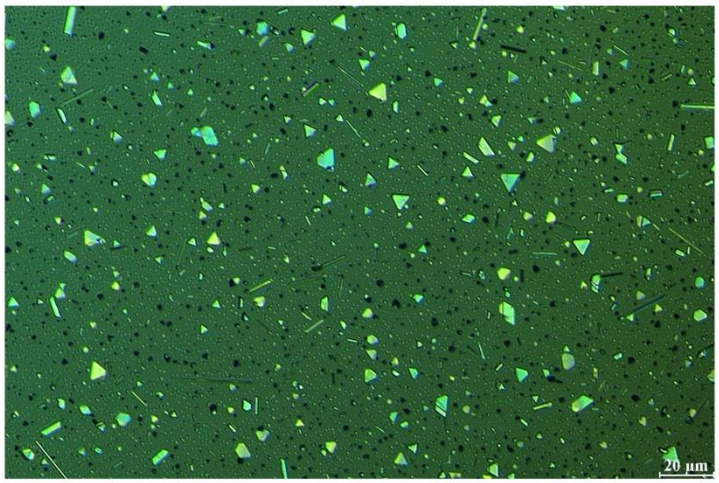

Figure 2.8 The optical image of Te on mica substrate by using Cu foil that have been used as source.

We analyzed the distance between interplane. The spacing is 0.39 nm, which is consistent with the (100) plane of previous reported Te.

Another control experiment was also conducted to confirm that precursor of the as-grown Te flakes is from Cu-Te alloy. In this control experiment, we use the Cu foil that have been used before to grow Te on mica. We put a piece of mica on the reused Cu foil but without Te solid source in the upstream under a same growth condition. After growth, there are many Te flakes on mica can be observed (**Figure 2.8**). This control experiment provides solid evidence that the as-grown Te flakes is supplied by Cu-Te alloy. The Cu-Te alloy formation is the key to grow Te, which provide a new strategy and controllable manner for elemental 2D materials growth via vapor deposition process.

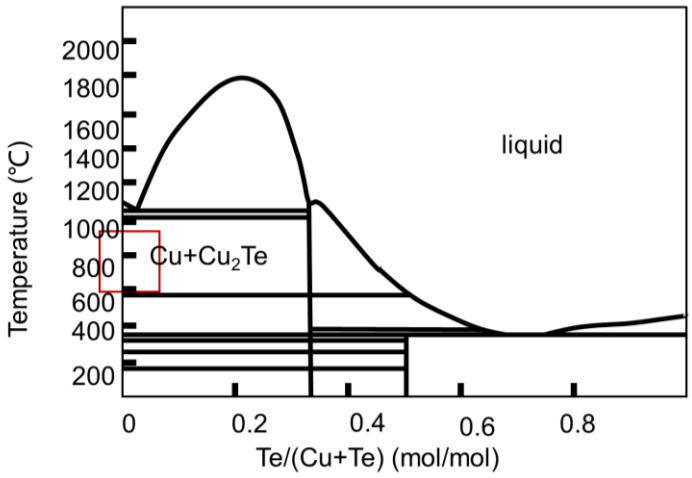

Figure 2.9 The binary phase diagram of Te and Cu. At the range from 600℃ to 1000℃, the Cu-Te alloy can form.

We conducted the Te growth at 600 ℃ to form the Cu-Te alloy from the phase diagram of Cu-Te is in Figure 2.9 The photos of Cu foil before and after Te growth is shown in Figure 2.10a. We can observe that an obvious color change of the foil, from gold to black. This color change confirms the chemical reaction that form new compounds between Te and Cu. The elemental analysis was characterized by scanning electron microscopy with energy dispersive spectroscopy (SEM-EDS). Elements Te and Cu distributed uniformly in the foil after growth. In addition, some boundaries are also observed due to the high temperature annealing during the growth process. To detect the elemental ratio of Cu and Te, X-ray diffraction (XRD) patterns confirm the existence of Cu_2Te and $Cu_{2-x}Te$. The ratio of Cu and Te is about 2:1 that were further confirmed by Energy dispersive spectroscopy (EDS) analysis. The high growth temperature confirms the alloy formation and supply the Te vapor source for following

growth step. Ultimately, Te is vaporized from alloy and moves to the mica substrate. The confined space between mica substrate and Cu foil results in an even spread of Te vapor. In contrast, triangular Te flakes are not observed without Cu foil, highlighting the crucial role of Cu foil for Te growth.

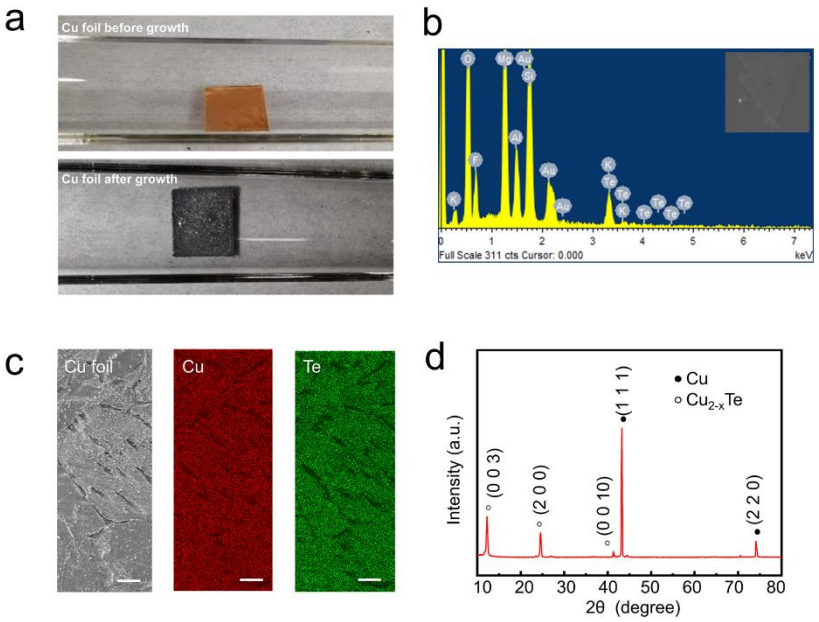

Figure 2.10 Material characterization of Cu foil after growth. (a) Cu foil before and after growth. Obviously, the foil is golden before growth but transmute into black, indicating the chemical reaction between Te and Cu. (b) The elemental analysis of Cu foil. (c) The SEM-EDS mapping of Cu foil after growth. (d) The XRD patterns of Cu foil after growth.

2.3.1 Van der Waals Epitaxy Growth of Tellurene

As mentioned in our previous conversion, the 2D Te have grown aligns well on the mica substrate. Most of the Te flakes exhibit consistent shapes, that implies the alignment phenomenon is present at the initial nucleation stage. The oriental angles of Te flakes on mica substrate are shown in Figure 2.11 statistically displays in two primary directions. These two orientations are indicated by triangles of different colors.

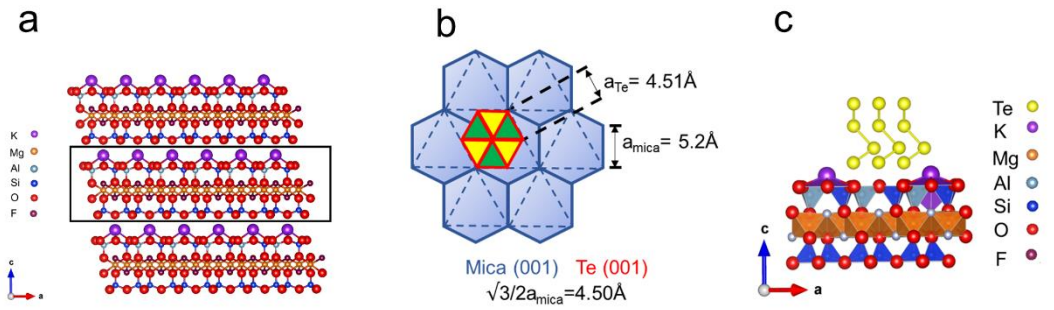

Figure 2.12 The lattice relationship between mica and Te. (a) The side view of mica lattice structure. (b) The schematic of Te and mica lattice structure. (c) The calculation model of Te on mica.

Specifically, the red triangle signifies 0°, while the blue triangle denotes 60°. From the provided inset optical images, it can be observed that there are two favored orientations, which corresponding to the defined angles 0° and 60°. Fascinatingly, the proportion of these two angles is nearly 1:1, with only a small number of flakes being misaligned. Two favored orientations of Te flakes can be distinguished, corresponding to the relative rotation angles of 0° and 60°, respectively.

To understand the distribution of Te orientation on mica substrates, we relationship between the lattice structures of mica and Te. Owing to the inert surface and atomic-level smoothness, Fluorophlogopite mica is an ideal candidate for the epitaxial growth of 2D materials. The lattice structure of mica is presented in Figure 2.12a. Mica exhibits hexagonal crystal symmetry that is same with Te. The schematic diagram of the lattice structure relationship between mica and Te is displayed in Figure 2.12b. The lattice

mismatch between mica and Te is remarkably small, at a mere 0.15 %. When the temperature is high, the migration of Te atoms move to the mica surface is increased. This can effectively boost growth rate of Te flakes. Moreover, the minor strain caused by the lattice mismatch can be dissipated at the high growth temperature, that further aiding in the epitaxial growth of high-quality Te flakes.

DFT calculations are carried out to gain insight into the interaction between Te and mica. We determined the binding energy between mica and Te, considering the angle between the Te triangle's alignment and the mica surface. The side view model of Te chains on the mica surface is depicted in Figure 2.12c. By rotating the Te chains, we calculated the relative energy to determine the preferred orientation on the mica surface. Two distinct orientations are clearly shown, which align well with our experimental data. Figure 2.13a-g provides all the energy-optimized configurations of Te on the mica surface at various angles. The results of these calculations (shown in Figure 2.13h.) indicate that the maximum binding energy between Te and mica is found at 0° (-2.65 eV) and 60° (-2.68 eV), which correspond to the two primary orientations seen in Figure 2.11. The lowest energy state, which is observed at 0° and 60°, indicates the thermodynamically preferred growth directions, thereby displaying the two primary growth orientations. On the other hand, the remaining angles exhibit higher binding energies. For instance, the orientation at 30° has the maximum binding energy (-2.60 eV), implying challenges in Te flakes grow along this orientation. Therefore, it can be established that the 0° and 60° orientations are the most stable arrangements, which

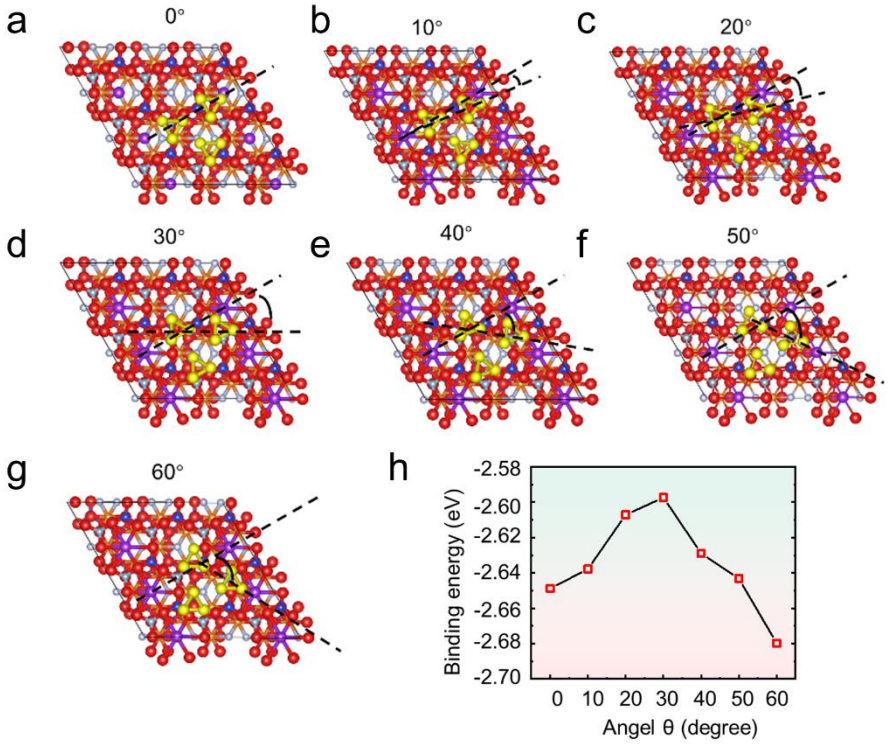

Figure 2.13 The theoretical calculation of Te on mica. (a-g) The calculation models of Te on mica surface with different angles. All the structures all fully relaxed. (h) The calculation of binding energy as the function of the angles.

corroborates our experimental findings. To sum up, we have successfully produced well-aligned Te flakes on a mica surface, which shows two main orientations. The analysis of the lattice constant relationship and DFT calculations lead us to conjecture that the orientations of Te flakes might be influenced by the epitaxial correlation between the mica surface and the Te crystal structure.

We carried out the characterization of the Te sample using Selected Area Electron Diffraction (SAED). The simulated SAED of mica and Te are depicted in Figure 2.14 a,b, which reveal the hexagonal structure to both mica and Te. Six equivalent lattice

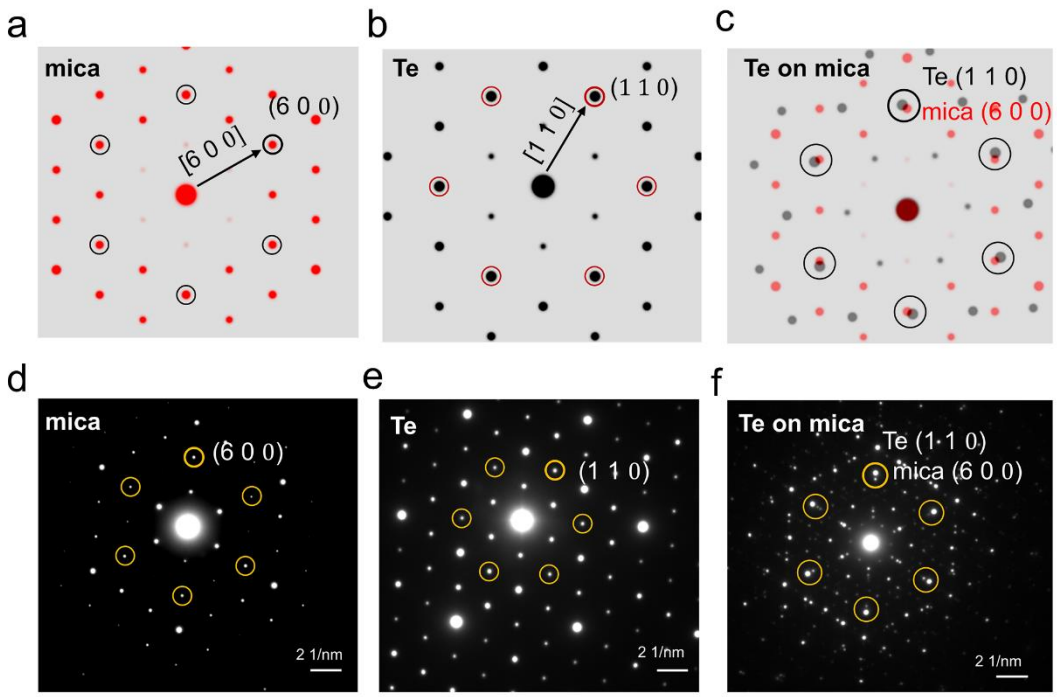

Figure 2.14 The simulated and experimental diffraction patterns. (a-c) The simulated diffraction patterns of mica, Te and overlapped Te-mica. (d-f) the experimental diffraction of combined Te-mica.

planes surround the symmetric diffraction patterns of mica and Te. To comprehend the growth direction of Te on mica, we perform a TEM characterization on ultrathin mica that has been exfoliated with Te. The exfoliated Te-mica overlapped sample is placed between two copper grids. The overlapped Te-mica SAED patterns are presented in Figure 2.14c. The red and black dots represent the SAED pattern of mica and Te respectively. These overlaid SAED patterns imply that the [110] direction of Te aligns with the [600] direction of mica. The experimental diffraction patterns of Te and mica both exhibit 6-fold symmetries. The diffraction spots can be indexed according to the

atomic structure of Te, as marked in Figure 2.14d,e. The experimental diffraction patterns are derived from the <001> axis, which is the direction of the Te chains. This implies that the Te chains develop at a perpendicular angle to the mica substrate. The indexing clearly indicates that the 2D Te is aligned along the [001] direction. The diffraction patterns of Te on mica, as shown in Figure 2.14f., indicate that the [110] axes of Te align with the [600] direction, revealing the epitaxial growth of Te on the mica substrate. It is observable that the experimental SAED patterns align well with the simulated SAED patterns.

Beyond the diffraction from Te and mica, some new diffraction spots can be interpreted as double diffraction occurring through an epitaxial growth of Te on mica. These extra patterns are probably a result of the lattice parameters between the Te layer on top and the mica layer beneath.

2.4 Conclusion

To summarize, we have developed a CVD method by introducing an alloy intermediate source to grow high aligned 2D Te flakes on mica substrates. This method overcomes the non-uniform spatial distribution issue in conventional CVD growth processes and enables repeatable, uniform growth. The favorable alignment of 2D Te flakes is attributed to the epitaxial growth on the mica surface along the [100] direction. The minimum binding energy between mica and Te is observed at 0° (-2.65 eV) and 60° (-2.68 eV). Moreover, the as-grown aligned Tellurene displays high uniformity and

ultra-smooth surfaces, as evidenced by AFM characterization. This research lays the groundwork for the more controlled growth of high-quality, aligned, single-crystalline Te.

Chapter 3 Low-resistance contact to p-type semiconductors with Se interfacial layer

3.1 Introduction

Electrical contact plays a dominant role in determining the performance of nanoscale devices[90, 168, 169]. By using the metal electrodes with the work functions in close proximity to the conduction band or valence band of semiconductors, the Schottky barrier height between metal and semiconductor can be greatly decreased. However, when the metal is close to the semiconductor, the overlapped wavefunctions of metal electrodes and semiconductors unavoidably result in metal-induced gap states (MIGS) after the rehybridizations of the semiconductor pristine wavefunctions[170-178]. These induced gap states lead to a Schottky barrier height independent on the metal work function. To establish low-resistance electrical contact to n-type two-dimensional (2D) semiconductors, researchers have adopted semimetal electrodes with low carrier density near their Fermi level and low work function[101, 102], including Bismuth (Bi), Antimony (Sb). However, it is still quite challenging to achieve low-resistance contact to p-type 2D semiconductors with the high-work-function metal electrode (Pt, Pd), because the high carrier density in Pt and Pd usually results in MIGS[179, 180]. The strong Fermi-level pinning effect induced by MIGS can result in high contact resistance. In addition, the harsh deposition conditions of Pt and Pd with high melting point (1769 ℃ for Pt, 1555 ℃ for Pd) may damage the interface of metal and semiconductor[181].

Selenium (Se) is an elemental material in group VI, which has the highest work function in the period table of elements. The electron configuration $3d^{10}4s^{2}4p^{4}$ of Se and its large electronegativity value (2.55) make Se difficult to remove electrons to the vacuum level, resulting in its high work function and facilitating the effective injection of holes into p-type semiconductors. The low melting point of Se (220 ℃) makes it easier to deposit without causing damage to the 2D materials, in contrast to the common metal with high work function metals (Pt and Pd). In addition, the densities of states (DOS) near its Fermi-level of Se is low because of its semiconducting characteristics[182]. The existence of low DOS of Se plays a crucial role in inhibiting the MIGS, thereby greatly reducing the Schottky barrier height. The high work function and the intrinsic semiconducting feature of ultrathin Se enable to form low-resistance electrical contact to p-type semiconductors.

In this work, we demonstrate a reliable way to realize high performances p-type transistors by introducing a high-work-function semiconducting Se interfacial layer at the contact region. The ultra-thin Se layer (1.2 nm thickness) ensures that the carriers can effectively inject into semiconductors through direct tunneling process. In addition, the interfacial Se layer can suppress the MIGS due to its intrinsic semiconducting properties. The p-type WSe_2 transistors with Se interfacial layer exhibit low contact resistance of 2.2 kΩ·μm and the saturation current density of 124.62 μA μm^{-1}. This methodology can be also extended to other p-type semiconductors. We demonstrate enhancements in the saturation current for p-type BP (from 8.6 μA μm^{-1} for Au-contact

to 42.7 μA μm^{-1} for Au-Se-contact) and carbon CNT (from 0.6 μA μm^{-1} for Au-contact to 1 μA μm^{-1} for Au-Se-contact) transistors.

3.2 Methods

3.2.1 Mechanical cleaving WSe_2 and BP films

CVT-grown WSe_2 crystals and BP bulk crystals were mechanically exfoliated with Scotch tape onto the 300-nm-thick SiO_2/Si substrate. The bulk crystals were purchased from Shanghai ONWAY Technology.

3.2.2 Device fabrication

After preparing the WSe_2 and BP films, photolithography was used to define the contact electrodes with long channel lengths with AZ-5214E resists. Electron beam lithography was used to define the short channel device contacts with PMMA-950K A4 resists. Thermal evaporation was adopted to deposit 1.2-nm-thick Se and 40-nm-thick Au in sequence. During the evaporation process, the distance between the substrate and the evaporated source are well controlled to 50 cm. The contact layer was deposited slowly under the 0.1 Å/s deposition rate. This distance ensured the evaporated film was uniform and did not damage the interface between 2D semiconductor and contact electrodes. Notably, the high vacuum pressure was also crucial for the contact film. We controlled both the base and working vacuum pressure up to 10^{-7} torr to deposit the

high-quality contact film. All the electrical measurements were conducted in a vacuum probe station by Keithley 4200 SCS semiconductor parameter analyzer.

3.2.3 Semiconducting CNT film preparation and Device fabrication

The semiconducting CNT powder was purchased from Nano Integris. The dispersant poly(m-phenylenevinylene-co-2,5-dioctyloxy-p-phenylenevinylene) [PmPV] was purchased from Sigma Aldrich. 0.5 mg S-CNT powder and 0.5 mg PMPV were added into 50 ml 1,2-dichloroethane ($C_2H_4Cl_2$). Then the solution was ultrasonic dispersed for 12 h at 15 ℃. The low-temperature ultrasonic is very important for CNT dispersion. The S-CNT solution was spin-coated at 800 rpm for 8 s and 3000 rpm for 40 s, followed by baking process at 120 ℃ for 4 min. The film was patterned by standard photolithography process and inductively coupled plasma (ICP) etching at 100 W for 30 s with 20 sccm O_2. Then the source and drain electrode were fabricated like WSe_2 and BP transistors fabrication process illustrated in Device Fabrication section.

3.2.4 Material Characterization

XPS and UPS characterizations were performed by the Nexsa XPS system. AFM were characterized by the Bruker MultiMode 8 SPM. Cross-section TEM samples were conducted by the Thermofisher Helios 5CX focused ion beam (FIB) system. A platinum protection layer was in situ deposited by electron beam deposition before FIB bombardment, followed by etching process the surrounding area to form the target lamella. The target lamella was exfoliated from the original substrate and transferred to

TEM grid inside the FIB chamber. HAADF-STEM characterization was acquired on Thermofisher Spectra300 with an acceleration voltage of 300 kV.

3.2.5 Schottky barriers extraction

To explore the Schottky barrier height of Au-WSe_2 transistors and Au-Se-WSe_2 transistors, we also studied the temperature-dependent characteristics of these transistors. The current of a Schottky transistor depends on the thermionic emission current and the thermally assisted tunneling current. At low temperatures, the drain current is related to the number of carriers that can overcome the Schottky barrier without thermionic emission. According to the principles of the thermionic theory, the drain current density can be expressed as: The ON-state current density of transistors is determined by the total contact resistance. With the increase of the drain voltage, the ON-state current will increase under various gate voltages at a given contact resistance. The ON-state current that reaches the maximum limit value is the saturation phenomenon. The saturation is influenced by many various reasons, and one significant reason is velocity saturation. By considering the total contact resistance R_c into the drain voltage V_{ds}, the effective drain voltage V'_{ds} can be given as:

$$I_{DS} = A^*_{2D} T^{1.5} \exp\left(-\frac{\Phi_B}{k_B T}\right)\left[1 - \exp\left(\frac{-V_{DS}}{k_B T}\right)\right] \qquad (3-1)$$

where A*2D is the Richardson constant of 2D material, T is the absolute temperature, k_B is the Boltzmann constant, Φ_B is the barrier height. The thermionic emission current dominates the drain current when the gate voltage (V_{GS}) is larger than the flat-band

voltage (V_{FB}). The gate voltage and the barrier height have a linear relationship. When the gate voltage is smaller than the flat-band voltage, the drain current is dominated by the thermally assisted tunneling current. When the gate voltage equals to the flat-band voltage, the barrier height and back-gate voltage undergo a transition from a linear relationship to a nonlinear one. At this point, the barrier height can be extracted from the Arrhenius plots.

3.2.6 DFT calculations

We performed the first-principles calculations by using the Vienna Ab initio Simulation Package (VASP 5.4.4)[164]. The exchange-correlation functional was based on Perdew–Burke–Ernzerho generalized gradient approximation[165]. We employed projected augmented wave potentials to describe the interactions between valence electrons and ion cores[183]. To include the vdW interactions, the DFT-D3 scheme was employed[184]. To understand the contact mechanism with and without Se interfacial layer, we built the slab models stacked by bilayer WSe_2 and four atomic layer Au (111) with and without Se layer. We built a supercell to ensure the lattice mismatch small than 5 %. The electrostatic potential profiles of contacts along the vertical direction were calculated using Poisson's equation. The force on each atom is less than 0.02 eV $Å^{-1}$ and the energy tolerance is 10^{-5} eV respectively for structure relaxation. The energy cut-off of the plane wave basis is chosen to be 500 eV. Considering the very large

models in these simulations, the Brillouin zone was integrated by sampling the Γ-point only.

3.2.7 Analysis of specific contact resistance with the transmission line method

We adopted the transmission line method to extract the contact resistance. The total resistance (R_t) includes two components,

$$R_t = 2R_c + R_{ch} = 2\frac{R_{sk}L_T}{W} + R_{sh}\frac{L}{W} \qquad (3-2)$$

where R_c is the contact resistance, R_{ch} is the channel resistance. R_{sk} is the modified sheet resistance beneath the contact, R_{sh} is the sheet resistance of the semiconductor in the channel. L is the channel length and W is the channel width. L_T *is* the transfer length, which is viewed as the effective length of the contact, where ρ_c is the specific contact resistivity,

$$L_T = \sqrt{\frac{\rho_c}{R_{\mathrm{sk}}}} \qquad (3-3)$$

Based on TLM method, we can assume $R_{sh} \approx R_{sk}$. The contact resistance ρ_c can be expressed as below, where L_C is the contact length

$$R_c = \sqrt{\rho_c R_{sh}}\, coth\left(\frac{L_C}{L_T}\right) = \frac{\rho_c}{L_T} coth\left(\frac{L_C}{L_T}\right) \qquad (3-4)$$

3.2.8 Analysis of specific tunneling resistivity

After introducing the Se interfacial layer, it is reasonable to suppose the tunneling resistance increases because of the semiconducting property of Se. We built an Au-Se-

WSe_2 supercell model to analyze the tunneling barrier at the interface. Because of the high work function of Se, the Schottky barrier is close to zero, where the barrier height is negligible. Thus, we mainly consider the field emission. Through Simmon's theoretical model[185, 186], the tunneling current density (J_t) can be obtained as below,

$$J_t = \frac{q}{4\pi^2\hbar w_t^2}\left\{\left(\Phi_t - \frac{qV}{2}\right)\exp\left[-2\frac{(2m_e)^{\frac{1}{2}}}{\hbar}\alpha w_t\left(\Phi_t - \frac{qV}{2}\right)^{\frac{1}{2}}\right]\right\}$$
$$-\left(\Phi_t + \frac{qV}{2}\right)\exp\left[-2\frac{(2m_e)^{\frac{1}{2}}}{\hbar}\alpha w_t\left(\Phi_t + \frac{qV}{2}\right)^{\frac{1}{2}}\right] \quad (3-5)$$

where q is the electron charge, is the reduced Planck's constant, V is the bias voltage, and Φ_t, w_t represent the tunnelling barrier width and height. α is the empirical factor. Here we assume α is 1 for an ideal square barrier. Then the tunnelling specific resistivity can be obtained at low bias,

$$\rho_t = \left(\frac{dJ_t}{dV}\right)^{-1} \approx \frac{4\pi^2\hbar w_t^2}{q^2}\frac{\exp\left(2\frac{(2m_e)^{\frac{1}{2}}}{\hbar}\alpha w_t\Phi_t^{\frac{1}{2}}\right)}{\frac{(2m_e)^{\frac{1}{2}}}{\hbar}\alpha w_t\Phi_t^{\frac{1}{2}} - 1} \quad (3-6)$$

We analyzed the electrostatic potential profile and extracted the tunneling barrier of Au-Se, and Se-WSe_2, respectively. At the interface of Au and Se, the $w_t \approx 1.85$ Å and $\Phi_t \approx 4.83$ eV. Thus, we can calculate $\rho_t \approx 3.30\times10^{-9}$ Ω cm^2. At the interface of Se and WSe_2, $w_t \approx 1.83$ Å and $\Phi_t \approx 4.57$ eV result $\rho_t \approx 2.98\times10^{-9}$ Ω cm^2. Notably, the small tunneling barrier of the internal Se layer can be negligible and ensure the electrons tunnel from Au to WSe_2.

3.2.9 Velocity saturation analysis in Au-Se-WSe_2 transistors

The ON-state current density of transistors is determined by the total contact resistance. With the increase of the drain voltage, the ON-state current will increase under various gate voltages at a given contact resistance. The ON-state current that reaches the maximum limit value is the saturation phenomenon. The saturation is influenced by many various reasons, and one significant reason is velocity saturation. By considering the total contact resistance R_c into the drain voltage V_{ds}, the effective drain voltage V'_{ds} can be given as:

$$V'_{ds} = V_{ds} - 2R_c I_{ON} \qquad (3-7)$$

with the decrease of channel length, when the electrical field along the lateral direction reaches a critical value, the velocity of carriers tends to saturate, that is called saturation velocity v_{sat}. This critical electrical field value is $E_{cr.}$ The ON-sate current I_{ON} reached the maximum:

$$I_{ON} = n_{2D} q v_{sat} \qquad (3-8)$$

where n_{2D} is the carrier density, q is the elementary charge. For 100 nm channel length Au-Se-WSe_2 transistor shown in Fig. 3d, v_{sat} can be extracted to ~1.27 × 10^6 cm s^{-1} when the saturation current density is 124.62 μA μm^{-1} at the n_{2D} of 6.19 × 10^{-12} cm^{-2}.

As the channel length reduces to a critical value, the WSe_2 reaches its critical electrical field with the increase of the drain voltage. This critical value of channel length is critical channel length L_{cr}.

$$E_{\mathrm{cr}} = \frac{V'_{\mathrm{ds}}}{L_{\mathrm{cr}}} = \frac{V_{\mathrm{ds}} - 2R_c n_{2D} q v_{sat}}{L_{\mathrm{cr}}} \qquad (3-9)$$

The critical electric field of WSe_2 is typically measured to be 7×10^4 V cm^{-1}[186]. Considering the Au-Se-WSe_2 transistor with $R_c \approx 2.2$ kΩ·μm at the n_{2D} of 6.19×10^{-12} cm^{-2} at V_{ds} of 1.25 V, we can extract that the L_{cr} is ~98 nm, which corresponds to our experiments. When the channel length is below 100 nm, the velocity saturation can be observed for the Au-Se-WSe_2 transistor.

3.3 Results and discussion

3.3.1 Semiconducting Se interfacial layer with high work function

When metal electrodes are contacted to a semiconductor surface, the charge transfer process leads to wavefunction rehybridization. The high carrier density of metal perturbs the semiconductor, leading to the presence of gap states and Schottky barrier independent on the metal work function. The semiconducting properties of Se contribute to the suppression of gap states due to its low density of states near the Fermi level. These low DOS can slightly perturb the wavefunctions of p-type semiconductors, resulting in the gap states suppression. Figure 3.1 shows the origin DOS of Se and

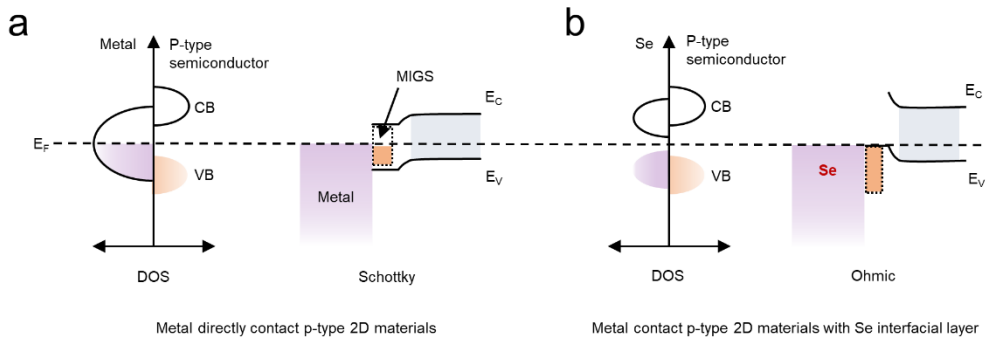

Figure 3.1 semiconducting Se interfacial layer. (a) The DOS and band diagram of common metal and p-type semiconductors. The shaded purple area and light blue are the electron-occupied states of common metal and p-type semiconductors, respectively. The gray area shows the gap region of p-type semiconductors. After contact, MIGS (navy area) and Schottky barrier are easily formed because of the wave function perturbation by common metal, resulting in the Fermi level pinned at the band gap of p-type semiconductors. (b) The DOS and band diagram of semiconducting Se and p-type semiconductors. The shaded purple area and light blue are the electron-occupied states of Se and p-type semiconductors. Because the DOS of semiconducting Se near the Fermi level is fewer than that of metal, the MIGS can be effectively suppressed. After rehybridizations of the semiconductor's pristine wavefunctions with these few states of Se, the new induced states are fewer than semiconductor contact with metal, results in suppressing Fermi level pinning effect.

typical p-type semiconductor. After the band alignment of the metal-Se-semiconductor, the low DOS of Se has negligible effect on inducing the gap states in semiconductors.

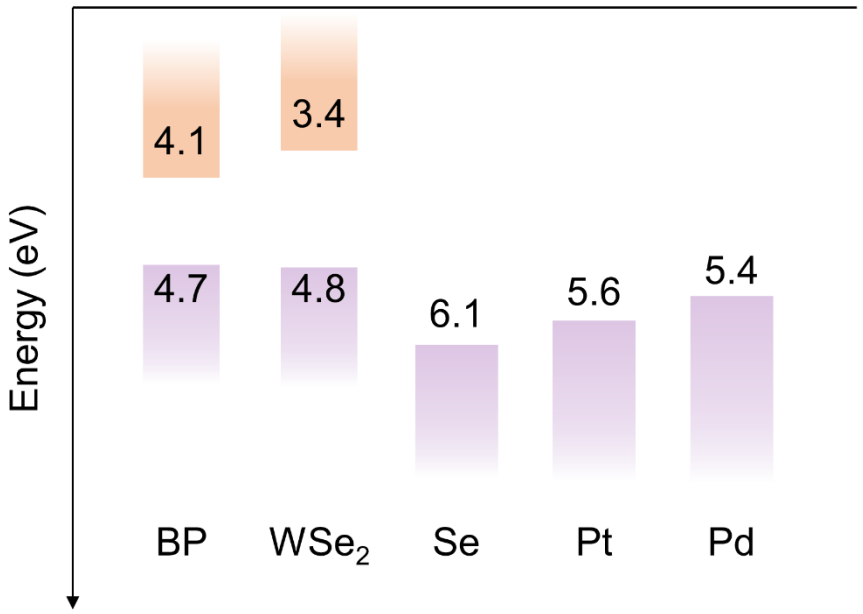

Figure 3.2 The energy band diagrams of common contact metals with respect to that of WSe_2.

In addition, the high work function of Se results in low Schottky barrier height because of the negligible energy difference of the work function of Se and valence band minimum (VBM) in the p-type semiconductor, which facilitates the effective carrier injection into the semiconducting channel. Since the work functions of Se, Pt, and Pd are all below the VBM of WSe_2 and BP (Figure 3.2), it is reasonable to predict that they have negligible Schottky barrier height. We introduce the ultra-thin Se interfacial layer between p-type semiconductor and metal electrode (see details in Methods), as schematically illustrated in cross-section of a back-gate transistor (Figure 3.3). However, our experimental results show that the devices with Pd and Pt metal electrodes exhibit inferior performance compared with that with Se interfacial layer.

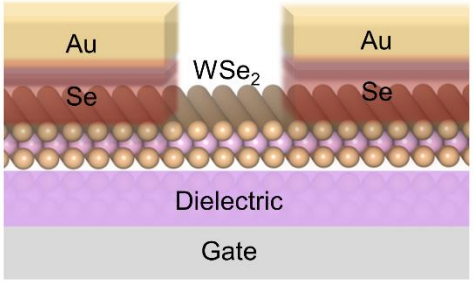

Figure 3.3 The cross-sectional schematic of the transistor with Se interfacial layer.

The primary reason is because metallic Pt and Pd contact with a semiconductor can lead to the gap states that cannot be disregarded. In addition, the high melting point of Pt and Pd requires a high-energy metal deposition process. By electron beam deposition, the interface of metal and WSe_2 may be damaged[187].

3.3.2 Se interfacial layer between metal and p-type semiconductor

Cross-sectional TEM images (Figure 3.4a-c) show the interface of Au-WSe_2 and Au-Se-WSe_2 structures. Both Au and Au-Se form clean interfaces with WSe_2 by the well-controlled deposition process. We achieved clean van der Waals (vdW) contacts (See Methods). The spacing between Au and the W atoms in WSe_2 is approximately 4.65 ± 0.2 Å (Figure 3.4 a). We can observe that the Se interfacial layer is a continuous layer from Fig. 2b. The spacing of the interfacial Se layer and W atoms in WSe_2 is approximately 4.56 ± 0.2 Å at the Se-WSe_2 interface (Figure 3.4c). The different interface gaps can result in different tunneling resistances. From Cs-corrected TEM image of Au-Se-WSe_2 (Figure 3.4 b,c), the Se atoms of WSe_2 remain intact after the

deposition of the thin Se layers. The energy dispersive spectroscopy (EDS) mapping (Figure 3.4 d-f) verifies that the Se layer is uniformly distributed and continuous at the interface. The ultrathin thickness of Se layer (1.2 nm) enables direct tunneling.

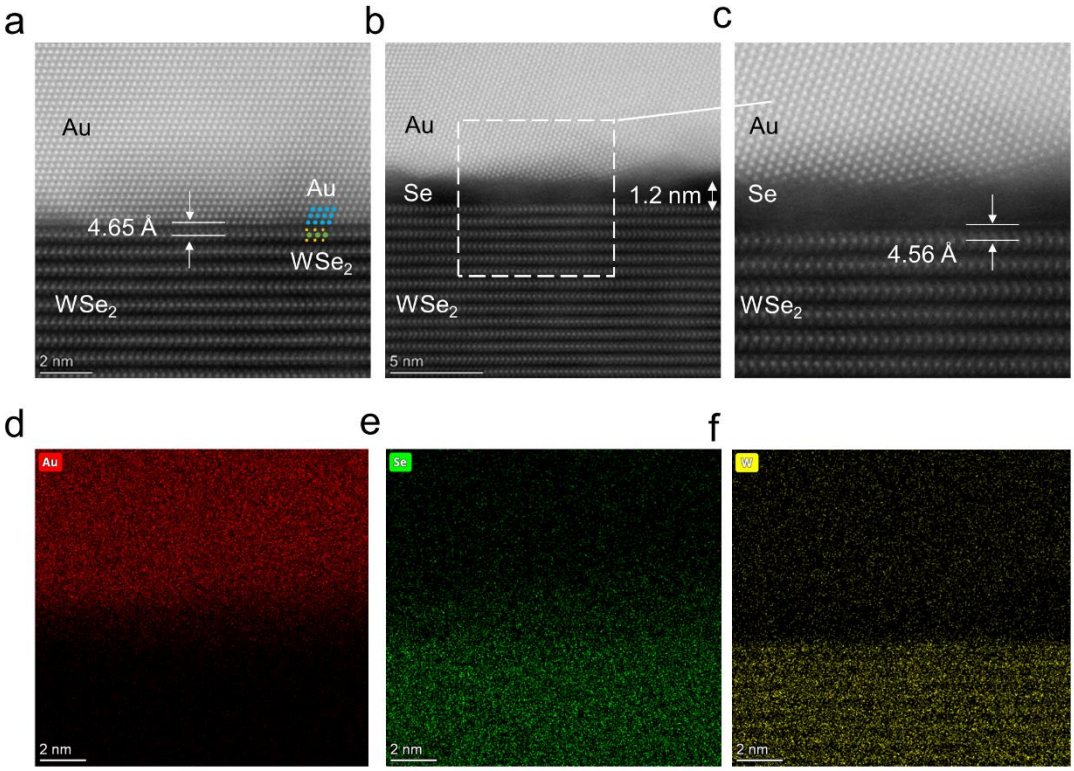

Figure 3.4 Se interfacial layer for low-resistance contact. (a,b) The cross-sectional STEM image of the Au-WSe_2 contact and Au-Se-WSe_2 contact. (c) Zoom-in atomic-resolution image of the marked area in b. (d-f) Corresponding EDS elemental mappings of the cross-sectional Au-Se-WSe_2 show the spatial distributions of elements Au, Se and W.

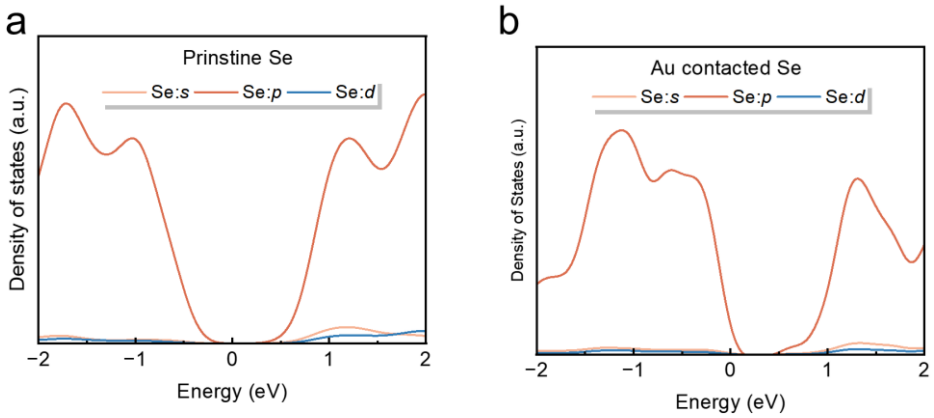

Figure 3.5 Density of state of pristine Se and Au contacted Se.

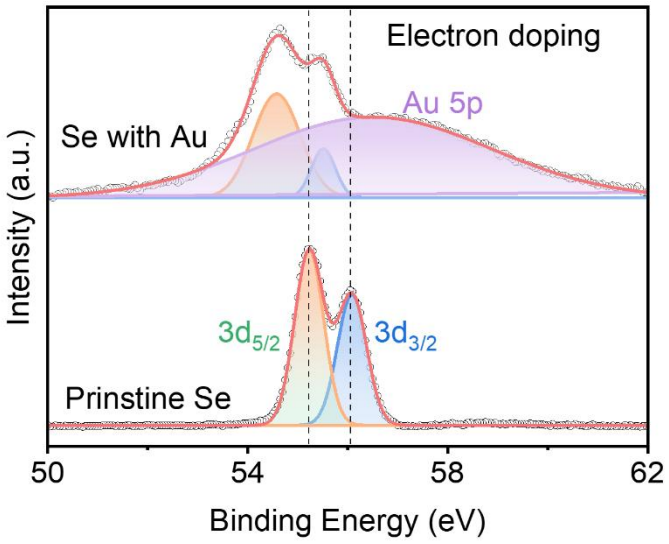

Figure 3.6 The shift of XPS spectra comparison of pristine Se and Au contact Se. After Au is contacted with Se, the Se 3d peaks of the XPS spectra shows a 0.6 eV shift, suggesting an increase in the electron concentration of Se due to doping by Au.

We perform density function theory (DFT) calculations on the projected density of states (PDOS) of Se with a band gap of 1.01 eV (Figure 3.5 a). When the Se layer is contacted with Au, the charge transfer can lead to heavy doping to the ultrathin Se. The

valence band of Se shifts upwardly because of the electron doping, resulting in the reduction of band gap of Se from 1.01 eV to 0.65 eV (Figure 3.5 b). After Au is contacted with Se, the Se 3d peaks of the XPS spectra shows a 0.6 eV shift (Figure 3.6), suggesting an increase in the electron concentration of Se due to doping by Au. This electron concentration increasing of Se leads to a decrease in binding energies, that confirm the upward shift of the valence band. Furthermore, the presence of this ultrathin Se interfacial layer facilitates carrier injection without compromising contact conductivity.

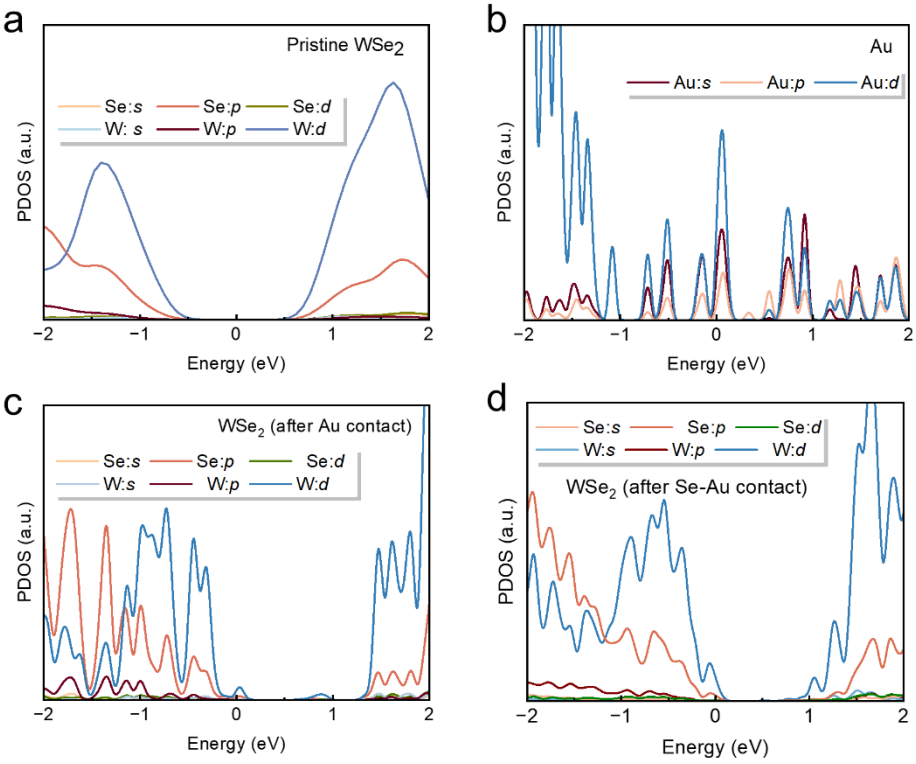

Figure 3.7 Theoretical calculation of MIGS. (a) The DOS of pristine WSe_2. (b) Metallic Au shows high states near the Fermi level. (c) The DOS of WSe_2 after contact Au. (d) The DOS of WSe_2 after contact Au with Se interfacial layer.

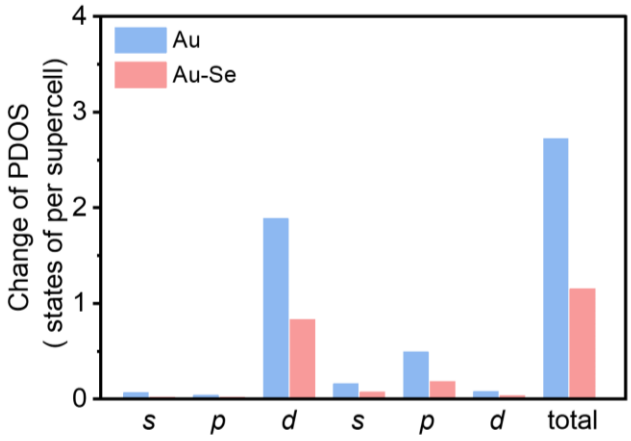

Figure 3.8 Theoretical calculation of MIGS. The change of MIGS comparison of Au contact and Au-Se contact. The blue bars represent the change of gap states induced by Au. The pink bars represent the gap states induced with Se interfacial layer. The gap states of each orbital of WSe_2 induced by Au-Se is obviously smaller than without Se interfacial layer.

The pristine WSe_2 is a p-type semiconductor with bad gap of 1 eV (Figure 3.7a). Metallic Au shows high states near the Fermi level (Figure 3.7b). When WSe_2 is in contact with Au electrode, the PDOS of WSe_2 shows obvious MIGS in resonance with Se (Figure 3.7c). With the Se interfacial layer, the gap states in WSe_2 are greatly reduced (Figure 3.7d). To quantitively compare the gap states of WSe_2 device with Au and Au-Se contact, we conducted a comparison of the gap states induced by Au and Au-Se on

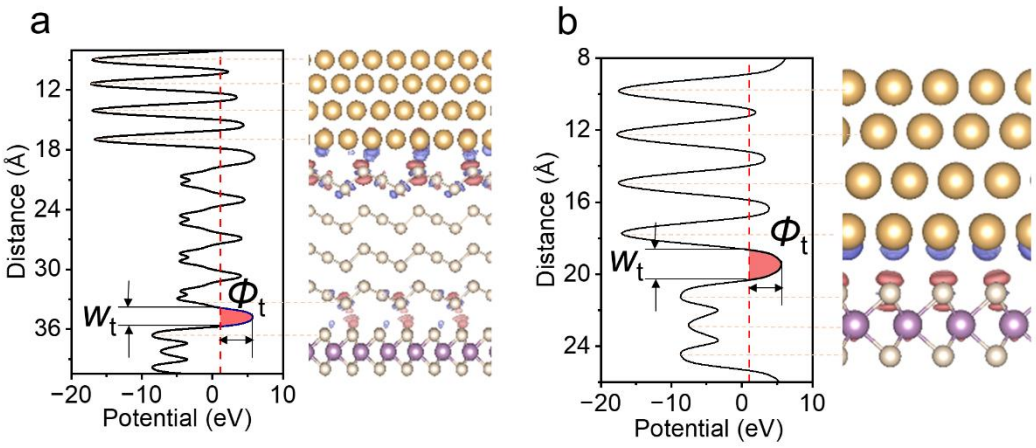

Figure 3.9 The electrostatic potential and differential charge density calculations. (a-b) The electrostatic potential profile (left panel) along the vertical direction using an isosurface of 0.005 e Bohr^{-3} the corresponding differential charge density (right panel) of Au-Se-WSe_2 and Au-WSe_2 in the atomic structure (red, positive; blue, negative). The electron tunneling barrier at the interface of Se and WSe_2 is shaded in red (width, w_t = 1.83 Å; height, Φ_t = 4.57 eV), resulting in a specific tunneling resistivity ρt 2.98×10^{-9} Ω cm^2. The electron tunneling barrier at the interface of Se and WSe_2 is shaded in red (width, w_t = 1.67 Å; height, Φ_t = 4.50 eV), resulting in a specific tunneling resistivity ρt 2.09×10^{-9} Ω cm^2. According to bader charge analysis, the charge transfer at the Au-WSe_2 interface is 0.12 e per Se atom.

WSe_2 in the s, p, and d orbitals respectively (Figure 3.8). The gap states of each orbital of WSe_2 induced by Au-Se is obviously smaller than without Se interfacial layer. We also analyze the electrostatic potential profile along the vertical stacked direction by building the supercell of Au-Se-WSe_2 and the corresponding charge density difference

Tunneling barrier	Au-WSe_2	Au-Se-WSe_2	
		Au-Se	Se-WSe_2
tunneling barrier width (w_t) / Å	1.67	1.85	1.83
tunneling barrier height (Φ_t) / eV	4.50	4.83	4.57
Tunnelling specific resistivity (ρ_t) / Ω cm^2	$2.09*10^{-9}$	$3.30*10^{-9}$	$2.98*10^{-9}$

Table 3.1 Comparison of tunneling barrier height, width and specific tunneling resistivity of various interfaces. These similar specific tunneling resistivities mean that the introduction of Se layer-induced tunneling resistance at the contact region can be negligible.

(Figure 3.9 a). At the interface of Au and WSe_2, the electrons directly transferred from Au to WSe_2 can be obviously observed (Figure 3.9 b). In contrast, the localized charge density was not observed at Se and WSe_2 interface, indicating the weak interaction between Se and WSe_2. According to Bader charge analysis, the charge transfer at Se-WSe_2 interface is 0.01 e per Se atom, which is much smaller than 0.12 e charge per Se atom transfer at Au-WSe_2 interface, indicting the interaction by metal is suppressed by Se interfacial layer.

To quantitively evaluate the tunneling resistance induced by semiconducting Se, we extract the tunneling barrier height (Φ_t) and width (w_t) to calculate the tunneling resistivity at the Au-Se interface and Se-WSe_2 interface. The tunneling barrier from Se to WSe_2 has a barrier width of 1.83 Å and a barrier height of 4.57 eV. This tunneling barrier induces the specific tunneling resistivity $\rho t \approx 2.98\times10^{-9}$ Ω cm^2, which is slightly

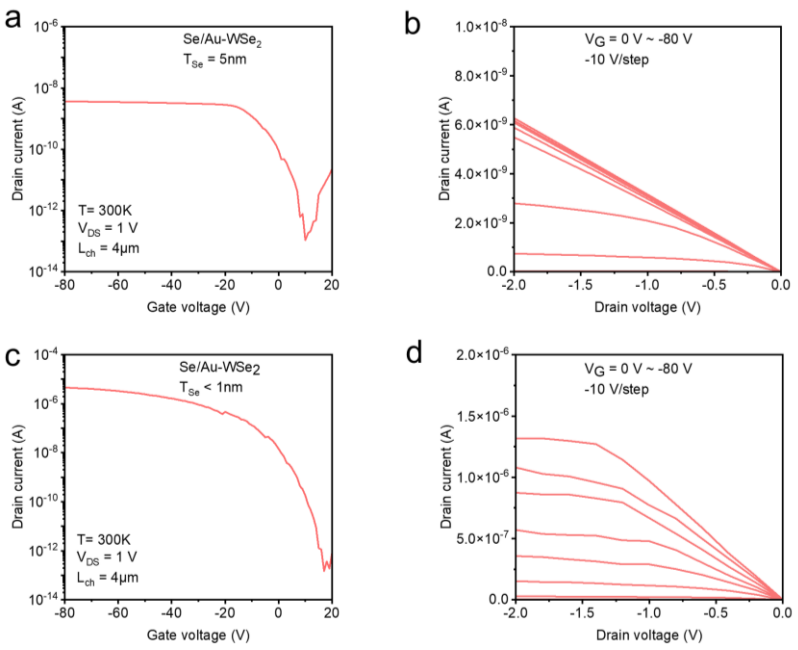

Figure 3.10 The different thicknesses of Au-Se-WSe_2 transistors. a,b, The transfer characteristic and output characteristic of Au-Se-WSe_2 transistor with 5-nm-thick Se interfacial layer. c,d, The transfer characteristic and output characteristic of Au-Se-WSe_2 transistor with Se interfacial layer thinner than 1 nm. These transistors exhibit low ON-state current density and poor out-put characteristics. The performance of the device declines when the thickness of Se exceeds 5 nm, primarily because of the tunneling resistance. With the Se thickness increase, the electron doping effect from Au is reduced, resulting in limited contact electricity. The direct tunneling possibility is also decreased due to the thick layer of Se. Therefore, the appropriate thickness of the Se interfacial layer plays a crucial role in the fabrication of high-performance WSe_2 transistors.

lower than Au-WSe_2 contact (3.30×10^{-9} Ω cm^2). This ultimately leads to disparities in barrier height and width, consequently resulting in different tunneling resistances.

These results suggest that the tunneling resistance induced by Se interfacial layer at the contact region is negligible, ensuring the holes can tunnel through Se layer and reach the semiconducting channel. Table 3.1 summarizes the tunneling barrier values. This ultrathin Se interfacial layer effectively suppresses the MIGS and induces negligible tunneling resistance. We fabricated the WSe_2 transistors with different thicknesses of

Se interfacial layer to investigate the effect of Se thickness on the device performance (Figure 3.10). When the thickness of Se exceeds 5 nm, the devices exhibit poor performance because of the high tunneling resistance. As the Se thickness increases, the electron doping effect from Au becomes weak. In addition, the probability of direct tunneling is also reduced with the increase of the thickness of Se interfacial layer. When the Se thickness is less than 1 nm, it is difficult to achieve a continuous layer formation by the physical vapor deposition process. Therefore, the appropriate thickness for the Se interfacial layer plays a crucial role for low-resistance electrical contact.

3.3.3 Electrical performances p-type WSe_2 transistors

Figure 3.11 a,b presents the representative transfer curves and output curves of Au-WSe_2 and Au-Se-contacted FETs with a channel length of 4 μm at room temperature. The Au-contacted FETs show a saturation current density I_{ON} of 3.33 μA μm^{-1}. The Au-Se-WSe_2 FETs exhibit a high saturation density of 22.54 μA μm^{-1} and a high ON/OFF ratio of > 10^8. The Au-WSe_2 transistors show non-linear output characteristics under

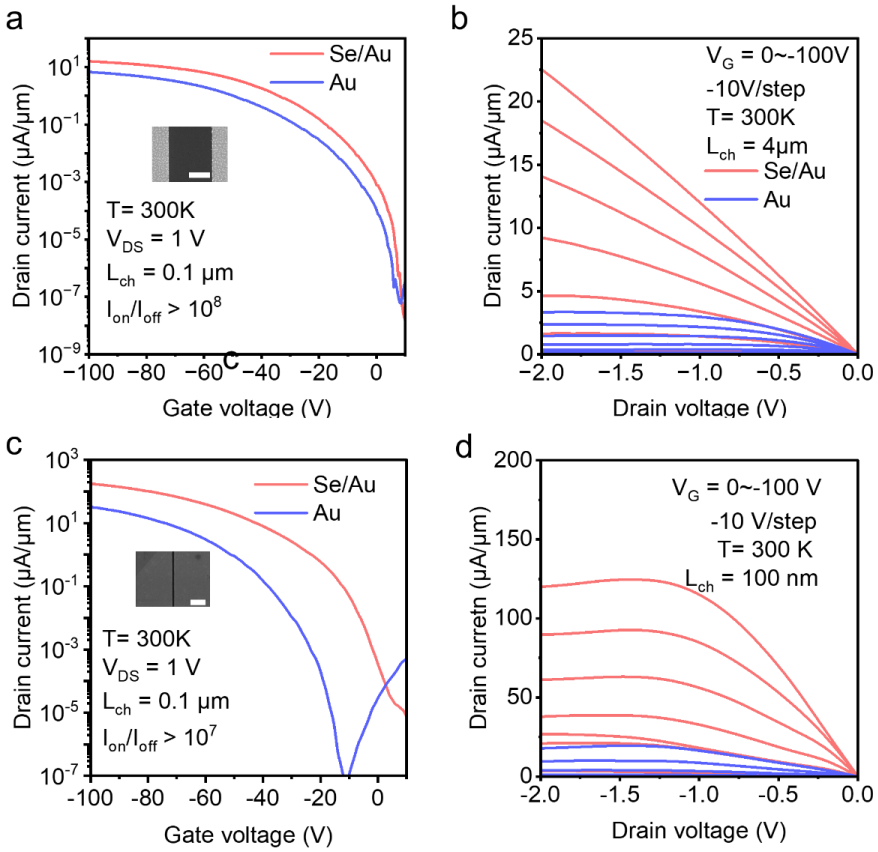

Figure 3.11 Comparison of Se interfacial contact and common Au-contacted WSe_2 FETs. (a, b) Comparison of transfer characteristics and output curves of Au-WSe2 FETs and Au-Se-WSe_2 FETs on 300-nm-thick SiO_2 dielectrics with Lch = 4 μm. Obviously, the Au-Se-WSe_2 FETs exhibit a higher ON/OFF ratio of > 10^8 and larger ON-state current density. Inset to a, SEM image of 4 μm channel device. Scale bar, 2 μm. (d,e) Comparison of short channel transfer characteristics and output curves based on Au-WSe_2 FETs and Au-Se-WSe_2 FETs on 300-nm-thick SiO_2 dielectrics with Lch = 100 nm. Inset to d, SEM image of 100-nm-length channel device. Scale bar, 1 μm. The Au-Se-WSe_2 FETs present larger ON-state current density and earlier saturation.

low bias voltage, indicating the presence of Schottky barriers at the interface of Au and

WSe_2. The Au-Se-WSe_2 transistors show linear relationship output characteristics at the low field regime, suggesting the formation of good Ohmic contact with the Se interfacial layer and lead to very high ON/OFF current ratios. When the channel length further decreases to 100 nm (Figure 3.11 c,d), the Au-Se-WSe_2 transistor exhibits higher I_{ON} (124.62 μA μm^{-1}) than Au-WSe_2 transistors (17.78 μA μm^{-1}) at Vds = 1.25 V. At the low field regime, the linear output characteristics are still observed of Au-Se-WSe_2 transistor. The Au-WSe_2 transistor exhibits saturation phenomena of output characteristics both at long channel with 4 μm and short channel with 100 nm at the Vds = 1.6 V and 1.25 V, owing to the large contact resistivity of Au-WSe_2 transistor. When the specific contact resistance is large (10.2 kΩ·μm for Au-contacted WSe_2 transistor and 2.2 kΩ·μm for Au-Se-contacted WSe_2 transistor from transfer length method), the number of electrons injected into the channel is limited, which will produce the early saturation and low saturation current. In addition, we also observe velocity saturation at the Au-Se-WSe2 short channel transistor, which happens for high drain current devices and short channel devices 26-29. As the electrical field increase in lateral direction, the drift velocity of the carriers will approach the saturation value because of the phonon scattering increase. The velocity saturation of short-channel Au-Se-WSe_2 FETs is studied to be ~1.27×10^6 cm s^{-1}, which determines the maximum current. The critical channel length is extracted to ~98 nm, suggest that the Au-Se-WSe_2 FETs can still work at the velocity saturation regime with short channel lengths. (see Methods for details). The low contact resistance of Au-Se-WSe_2 FETs ensure the

effective drain voltage is larger than the Au-WSe_2 FETs, which reduce the required drain voltage to achieve the velocity saturation regime.

We also fabricated WSe_2 transistors with various channel lengths using Au contact and Au-Se contact. (Figure 3.12). The 1-μm-length channel of Au-Se-WSe_2 transistors exhibit high saturation current density (28.12 μA $μm^{-1}$) than Au-WSe_2 transistors (6.04 μA $μm^{-1}$). When the channel length further reduces to 0.5 μm, the saturation current density of Au-Se-WSe_2 transistors increases to 59.48 μA $μm^{-1}$. The saturation current density of Au-WSe_2 transistor also increase to 14.36 μA $μm^{-1}$, but still lower than Au-Se-WSe_2 transistor with a same channel length. We analyzed the device-to-device variation in the transfer characteristics across 50 Au-Se-WSe_2 transistors. (Figure 3.13). The performances of the WSe_2 FETs are highly consistent with each other, confirming the high reliability of the method with Se interfacial layer. We then extract the contact resistance of Au-Se-WSe_2 transistor and Au-WSe_2 transistors by the transfer length method (TLM). According to Figure 3.14, the contact resistance of Au-Se-WSe_2 transistor is 2.2 kΩ·μm, much lower than that in the Au-WSe_2 device (10.2 kΩ·μm). The lower barrier height and contact resistance confirm our Se interfacial layer can effectively enhance the saturation current density of p-type transistors.

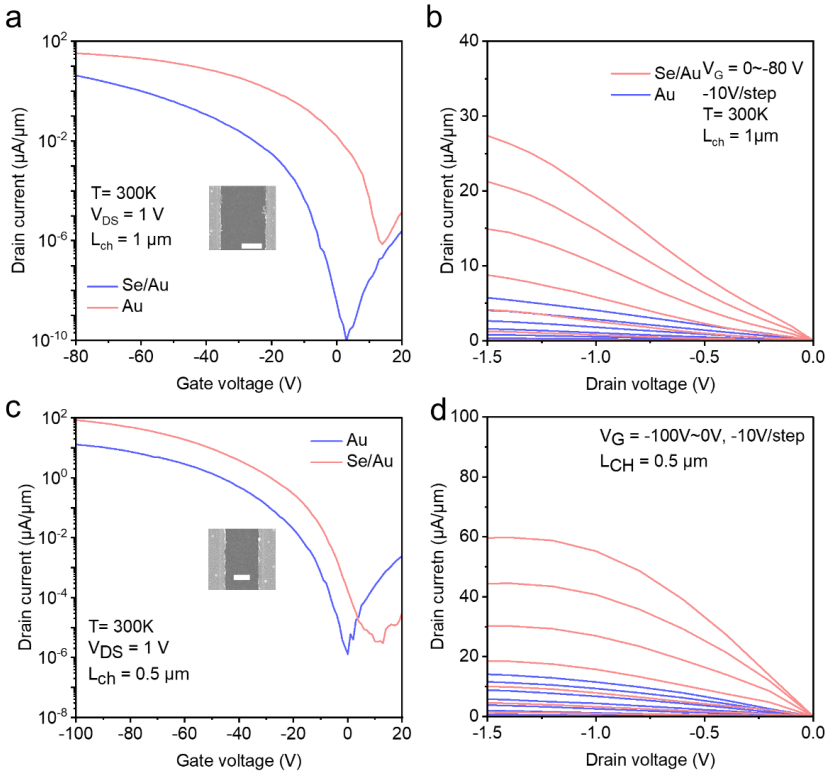

Figure 3.12 The electrical characteristics of WSe_2 transistors. (a,b) 1 μm channel length WSe_2 transistor. Inset to a, SEM image of the 1 μm Lch Au-Se-WSe_2 FET. The scale bar is 500 nm. (c,d) 0.5 μm channel length WSe_2 transistor. Inset to c, SEM image of the 0.5 μm Lch Au-Se-WSe_2 FET. Inset to c, SEM image of the 0.5 μm Lch Au-Se-WSe_2 FET. The scale bar is 250 nm. The 1-μm-length channel of Au-Se-WSe_2 transistors exhibit high ON-state current density of 28.12 μA μm^{-1} than Au-WSe_2 transistors (6.04 μA μm^{-1}) at Vds = 1.5 V. With the channel length further reduce to 0.5 μm, the ON-state current of Au-Se-WSe_2 transistors increase to 59.48 μA μm^{-1}. The ON-state current of Au-WSe_2 transistor also increase to 14.36 μA μm^{-1} at Vds = 1.5 V, but still lower than Au-Se-WSe_2 transistor with a same channel length The Au-Se-WSe_2 FETs present larger ON-state current density and earlier saturation.

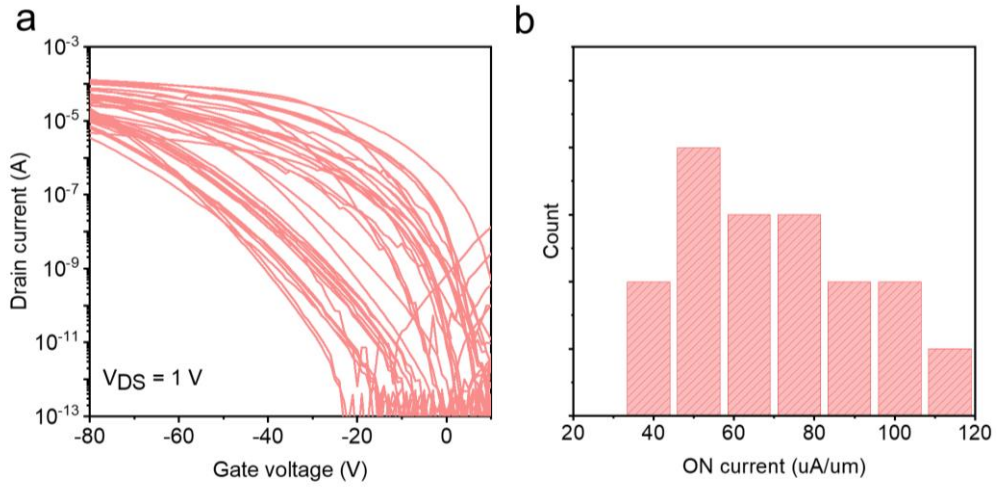

Figure 3.13 The device-to-device variation analysis. (a) Transfer curves of 50 WSe_2 FETs. (b) ON-state current histogram of devices.

To have better understanding on the electrical contact, we also fabricated the asymmetric contact WSe_2 transistors with one Au side and the other Au-Se side. We characterize the device twice with source and drain reversed, once using Au and Au-Se as the source electrodes, respectively. When switching the source from Au side to Au-Se side, the device shows a noticeable current increase even with the exact same channel (Figure 3.15). This phenomenon suggests that the Au-Se side has a lower contact resistance than the Au side. When a gate voltage is applied, the valence band bends downwards, promoting the injection of holes and contributing to the current flow. Since Se has a higher work function than Au, the barrier height at the Se-WSe_2 interface is lower than that at the Au-Se interface. When the Au-Se side is used as the drain terminal, it has a lower contact resistance, resulting in a higher drain current than when

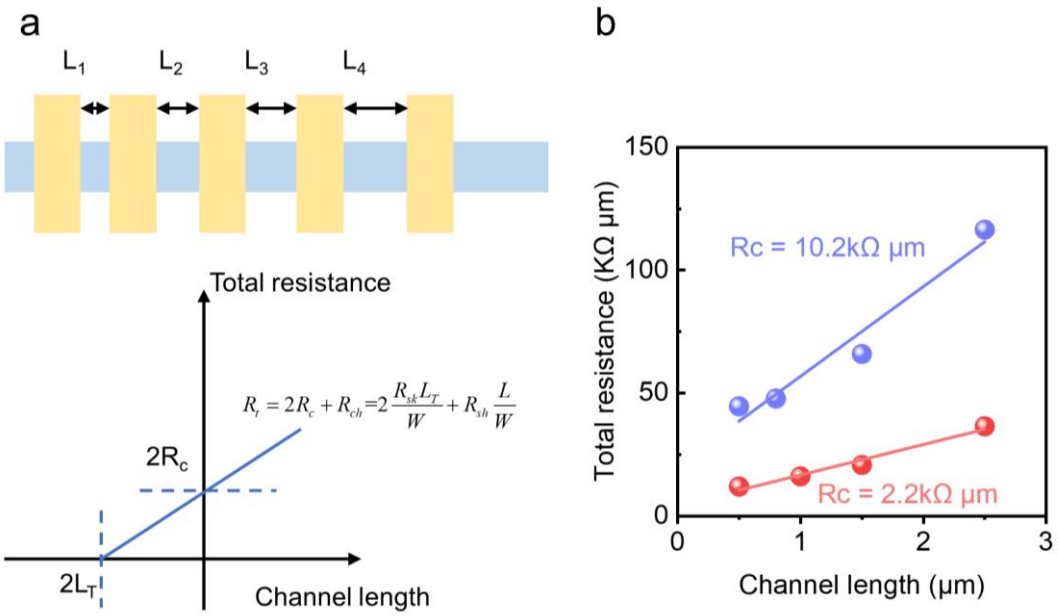

Figure 3.14 Contact resistance (RC) extraction using the transfer-length method (TLM). (a) Schematic of the device configuration for TLM. Linear relationship between total resistance and channel length for extraction of contact resistance RC and transfer length LT. (b) Contact resistance (RC) extraction using the transfer-length method (TLM) for Au-WSe_2 FETs and Au-Se-WSe_2 FETs on 300-nm-thick SiO_2 dielectrics. Blue and red circles are the total resistance of Au-WSe_2 FETs (blue) and Au-Se-WSe_2 FETs (red) versus channel length at carrier density of 6.19×10^{12} cm^{-2}.

Au is used as the drain terminal. Therefore, we can achieve a high saturation current when the negative gate voltage is applied to the Au-Se electrode. These studies on the asymmetric contact transistors provide alternative evidence that the Au-Se-contacted device has better performance than the Au-contacted device. To extract the barrier height of Au-WSe_2 and Au-Se-WSe_2 transistors, we performed the temperature-

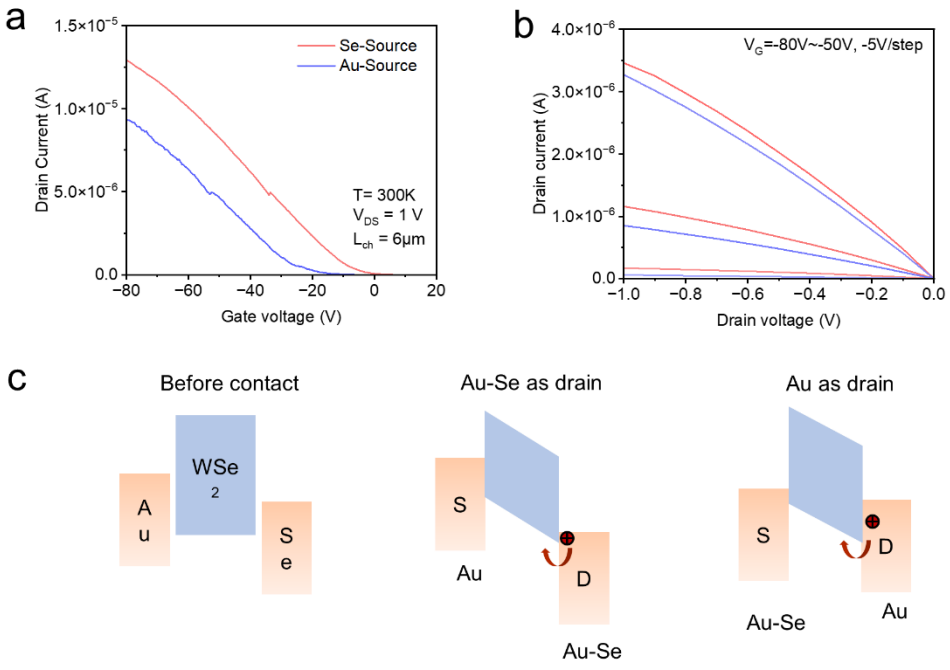

Figure 3.15 The electrical characteristics of WSe_2 transistors with asymmetric contact. (a, b) The typical transfer curves and output curves of asymmetric contact WSe_2 transistor. (c)The band diagrams of Au asymmetric contact WSe_2 transistor. Before contact, the Au and Se have different work functions. When switching the source from Au side to Au-Se side, Au-Se side has a lower barrier height than Au side, so the Au-Se side shows higher on-state current density than Au side.

dependent characterization according to the thermionic theory[188-191]. As temperature decrease, the saturation current of the Au-Se-contacted WSe_2 transistor increases due to the reduction of phonon scattering (Figure 3.16 a). Figure 3.16 b presents the Arrhenius plots under different gate voltages. The slope of the line corresponds to the barrier height at different back voltages. As shown in Figure 3.16 c, the SBH at flat

band is extracted to be 20 meV for Au-Se-WSe_2 transistor and 54 meV for Au-WSe_2 transistor (Figure 3.17).

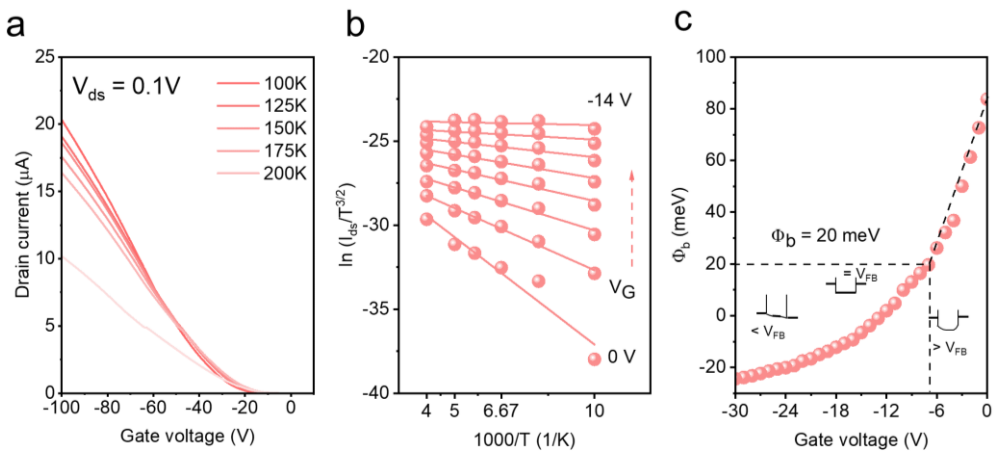

Figure 3.16 Low temperature characteristics of Au-Se-WSe_2 FETs. (a) The temperature-dependent characteristics of linear transfer curves of Au-Se-WSe_2 FETs with Lch = 4 μm. The drain current increases with the temperature decrease owing to the reduction of phonon scattering. (b) Arrhenius plots of Au-Se-WSe_2 FETs. The slope of the line is the barrier height at various back voltages. (c) The effective SBH for different back gate voltages.

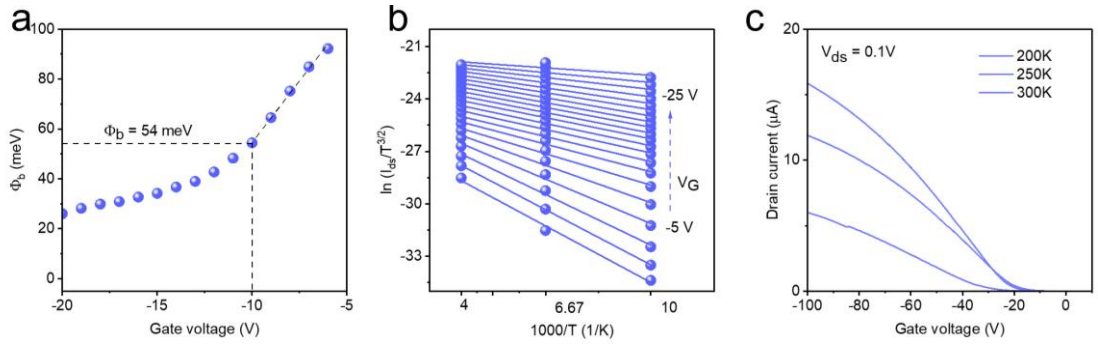

Figure 3.17 Low temperature characteristics of Au-WSe2 FETs. (a) the effective SBH for different back gate voltages. (b) Arrhenius plots of Au-WSe2 transistors. The slope of the line is the barrier height at various back voltages. (c) The temperature-dependent characteristics of linear transfer curves of 4 μA channel length Au-WSe2 transistors. The drain current increases with the temperature decrease owing to the reduction of phonon scattering.

3.3.4 Benchmark of p-type transistors with Se interfacial layer

To validate this contact strategy for other p-type semiconductors, we further fabricated back-gated FETs with various p-type semiconductors (black phosphorus, carbon nanotubes) as channel materials. Figure 3.18 a,b show the representative transfer curves and output curves of few-layer BP FETs. The Au-Se-contacted BP FET exhibits higher saturation current density (42.7 μA μm^{-1}) than Au-contacted FET (8.6 μA μm^{-1}).

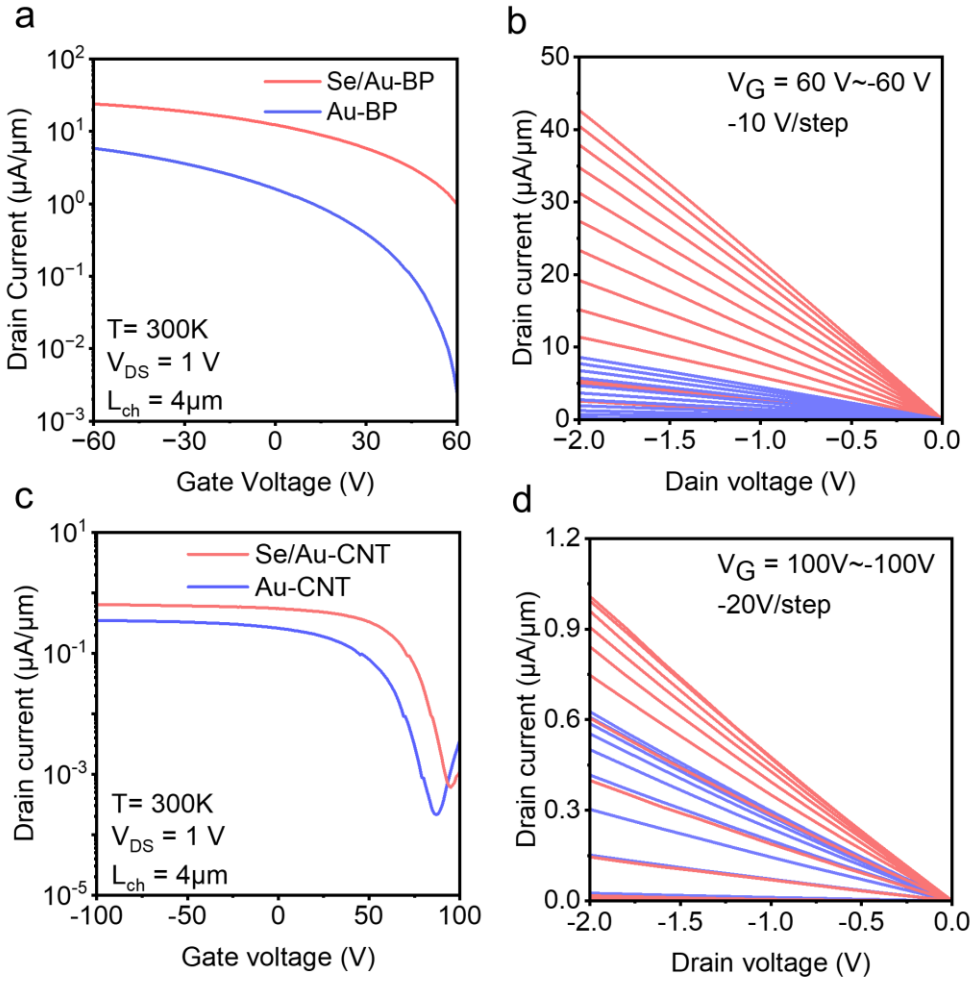

Figure 3.18 Electrical characteristics of Au-Se-BP FETs and Au-Se-CNT FETs. (a,b) The transfer characteristics and output characteristics of Au-BP FETs and Au-Se-BP FETs with Lch = 4 μm. (c,d) The transfer characteristics and output characteristics of Au-CNT FETs and Au-Se-CNT FETs with Lch = 4 μm.

The Au-Se-contacted CNT FET (Figure 3.18 a,b) also shows higher saturation current density (1 μA μm^{-1}) than Au-contacted FET (0.63 μA μm^{-1}). These results clearly demonstrate that the Se interfacial contact strategy can extend to other p-type semiconductors.

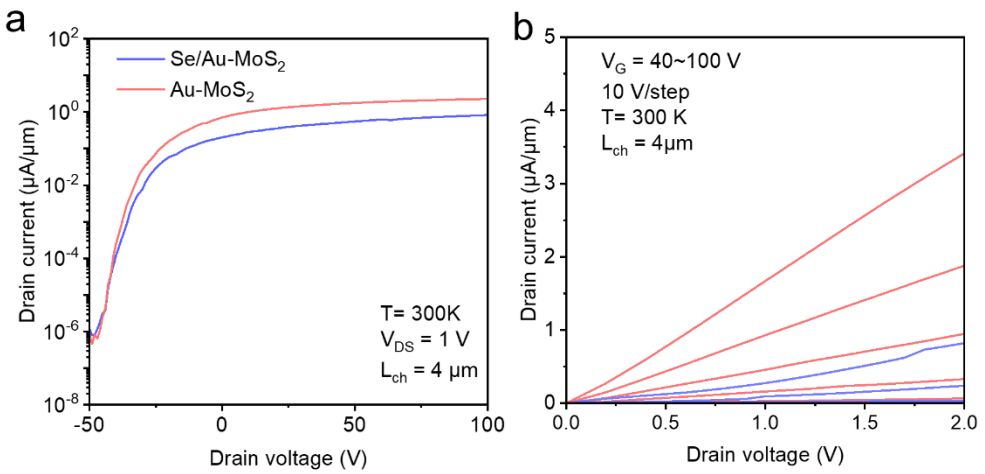

Figure 3.19 The electrical characteristics of Au-MoS_2 and Au-Se-MoS_2 transistors. (a) The transfer curves of Au-MoS_2 and Au-Se- MoS_2 FETs. (b) The output curves of Au-MoS_2 and Au-Se- MoS_2 FETs. Compared to the Au-MoS_2 transistor, the Au-Se-MoS_2 transistor shows small current density and non-linear output characteristics. The Au-Se-MoS_2 transistor exhibits saturation current (0.8 μA $μm^{-1}$) than Au-MoS_2 transistor (3.4 μA $μm^{-1}$).

In contrast, we also fabricated the n-type MoS_2 transistors with Se interfacial contact as a control device. (Figure 3.19). The Au-Se-MoS_2 transistor exhibits saturation current (0.8 μA $μm^{-1}$) than Au-MoS2 transistor (3.4 μA $μm^{-1}$). When using Au as the contact material, its low work function can result in a low energy barrier at the Au-MoS_2 interface. This can facilitate efficient electron injection from the contact into the n-type MoS_2 semiconductor. When using Au-Se as a contact for n-type MoS_2

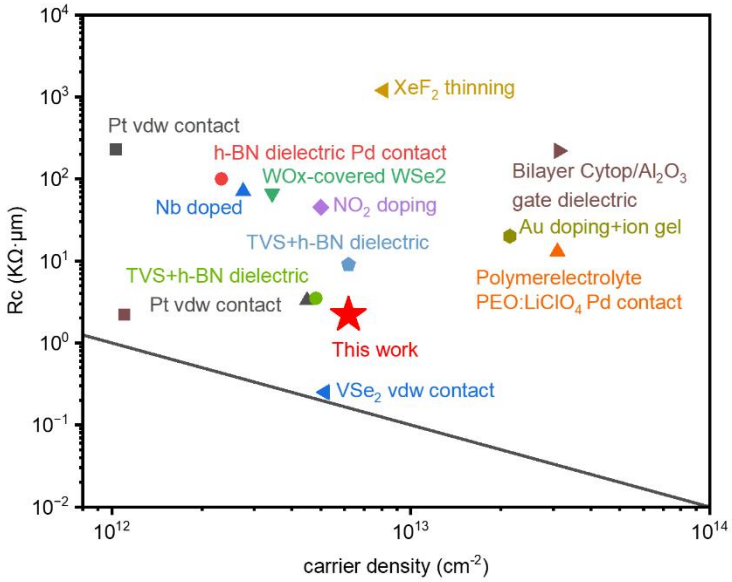

Figure 3.20 ON-state current density as a function of Lch of TMD FETs with various contact technologies reported in the literatures[1-10]. The black line represents the quantum limit of contact resistance. A review of existing literature shows that our Se interfacial layer contact methodology give better device performance with low contact resistance than most works.

transistors, the energy difference between the work function of Se and the Fermi level of MoS_2 (4.48 eV)[178] lead to a higher Schottky barrier compared to Au-WSe_2.

To further evaluate the performance of p-type 2D transistors, we benchmark the device performance parameters (contact resistance and saturation current density) with other p-type semiconductors to date. Figure 3.20 summarizes the relationship between contact resistance and carrier density. When the carrier density in the semiconductor is low, the contact resistance is relatively high. The contact resistance of the p-type WSe_2 transistor is significantly lower than that of other works with a comparable carrier

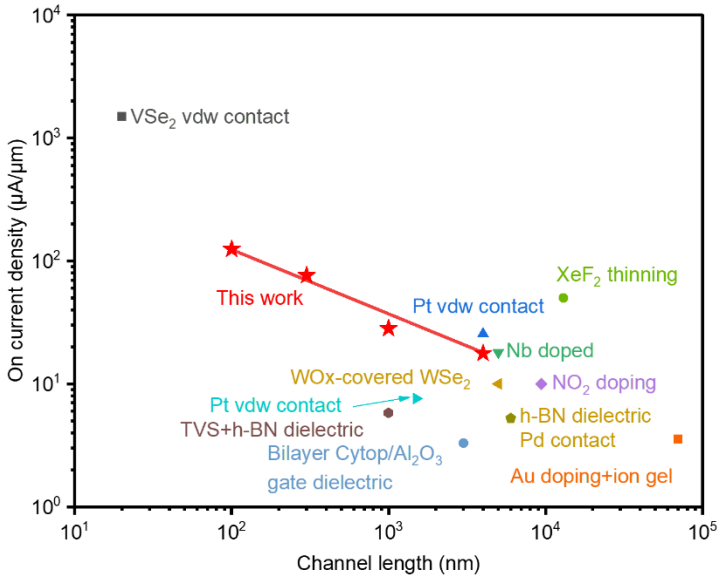

Figure 3.21 State-of-the-art contact technology for WSe2 transistors plotted as a function of carrier density.

density, specifically measuring as low as 2.2 kΩ·μm. Most works reported records are higher than 3 kΩ μm at an n_{2D} of ~10^{13} cm^{-2}. This low contact resistance value we achieved in our work strongly support the formation of an optimized metal-semiconductor contact. Figure 3.21 summarizes the ON-state current density as a function of channel length of WSe_2 transistors with different contact technologies. As the channel length reduces, the current density will increase. The achievement of the low contact resistance in our work lead to a comparable saturation current for the short channel device for p-type semiconductors. We demonstrate a superior saturated current density compared to most recent works with channel lengths shorter than 1 μm. When

the channel length reduces to 100 nm, the short-channel Au-Se-WSe_2 transistor has a saturated current density of 124.62 μA $μm^{-1}$.

In conclusion, we present a reliable method to reduce the contact resistance of p-type 2D transistors using standard laboratory technology. By adopting the ultrathin Se interfacial layer with semiconducting characteristics and the highest work function, we successfully suppress the metal-induced gap states and substantially reduce the Schottky barrier height. The contact resistance suppressed by Se interfacial layer is low to 2.2 kΩ μm. The long-channel Au-Se-WSe_2 transistors exhibit a high ON/OFF ratio over 10^8. The short-channel Au-Se-WSe_2 transistors have saturated current density increases from 17.78 μA $μm^{-1}$ to 124.62 μA $μm^{-1}$ compared to without Se interfacial layer contact. Owing to the unique properties of Se, our findings suggest the immense potential of our Se interfacial contact in enabling the development of high-performance p-type transistors.

3.4 Summary

In conclusion, we present a reliable method to reduce the contact resistance of p-type 2D transistors using standard laboratory technology. By adopting the ultrathin Se interfacial layer with semiconducting characteristics and the highest work function, we successfully suppress the metal-induced gap states and substantially reduce the Schottky barrier height. The contact resistance suppressed by Se interfacial layer is low to 2.2 kΩ μm. The long-channel Au-Se-WSe_2 transistors exhibit a high ON/OFF ratio

over 10^8. The short-channel Au-Se-WSe_2 transistors have saturated current density increases from 17.78 μA $μm^{-1}$ to 124.62 μA $μm^{-1}$ compared to without Se interfacial layer contact. Owing to the unique properties of Se, our findings suggest the immense potential of our Se interfacial contact in enabling the development of high-performance p-type transistors.

Chapter 4 Conclusions and Outlooks

In conclusion, this thesis demonstrates a new strategy for growth elemental p-type semiconductor Te, which has unique properties and great applications for future electronics. In addition, this thesis also studies the p-type contact by introducing Se interfacial layer at the contact regime to reduce the contact resistance, which is a dominant issue for high performance devices.

2D tellurium shows unique electronic and optical properties. Te is hexagonal crystal structure with helical chains along c-axis by the covalent bonding. It is easier for tellurium to form one dimensional chains and thick layers due to its unique crystal structure and strong interlayer force. In this thesis, we developed a CVD method that uses an as intermediate source to growth aligned Te flakes on mica substrate. XRD and SEM analysis confirm the Cu-Te alloy formation. This approach addresses the issue of non-uniform spatial distribution often encountered in traditional CVD growth processes, enabling consistent, uniform growth. The favorable alignment of the 2D Te flakes is due to the epitaxial growth on the mica surface in the [100] direction from TEM diffraction patterns. The grown aligned Te flakes exhibits high uniformity and ultra-smooth surfaces, as confirmed by AFM characterization. This study provides a foundation for more controlled growth of high-quality, aligned, single-crystalline Te.

For p-type FETs, the recent reported works for p-type FETs fabrication usually use high work function metals, that can reduce the SBH by band alignment. However, the intrinsic issue that the metal induced gap states are not solved due to high DOS of metal

with zero band gap near the Fermi-level. Compared to metal, semiconductor Se has band gap and high work function. We introduce an ultrathin Se interfacial layer at the contact regime. We performed theoretical calculations and conducted many device characterizations to confirm the significant role of Se interfacial layer for low contact resistance. By introducing the Se interfacial layer, the barrier heigh and the metal induce gap states can be great reduces. This Se interfacial layer strategy can also be extended to other p-type semiconductors. Due to the distinctive characteristics of Selenium, our research indicates that our Se interfacial contact holds great promise for facilitating the creation of high-performance p-type transistors.

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