NEUROMORPHIC APPLICATIONS BASED ON 2D MATERIALS FERROELECTRIC FIELD-EFFECT TRANSISTORS

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Neuromorphic Applications Based on 2D Materials Ferroelectric Field-effect Transistors

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CERTIFICATE OF ORIGINALITY

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Abstract

Drawing inspiration from biological neural networks, neuromorphic computing has emerged as a promising solution to overcome limitations imposed by traditional von Neumann architecture. Recently, two-dimensional (2D) materials have provided opportunities for achieving novel nanoelectronics and optoelectronic devices. In the meanwhile, ferroelectric materials possess spontaneous polarization that can be modulated dynamically, reversibly, and non-volatilely. Therefore, we focus on studying ferroelectric transistors based on 2D materials with different structures and investigating their potential neuromorphic applications.

Firstly, we design ferroelectric-tuned synaptic transistors by integrating 2D black phosphorus (BP) with flexible ferroelectric copolymer poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)). Through the nonvolatile ferroelectric polarization, the P(VDF-TrFE)/BP synaptic transistors show mobility value of 900 $cm^2 V^{-1} s^{-1}$ with 10^3 on/off current ratio and such devices can be operated with low energy consumption (~40 fJ) for each event. Reliable and programmable synaptic behaviors have been demonstrated, including paired-pulse facilitation (PPF), long-term depression (LTD), and long-term potentiation (LTP). The biological memory consolidation process is emulated through ferroelectric gate-sensitive neuromorphic behaviors. Inspiringly, the artificial neural network is simulated for handwritten digits recognition, achieving high recognition accuracy of 93.6%.

Secondly, it is still a challenge to process multiwavelength images in noisy

environments with simple device configuration and light-tunable biological plasticity. We demonstrate a prototype visual sensor based on ferroelectric copolymer (P(VDF-TrFE)) and 2D rhenium disulfide (ReS_2) with integration of recognition, memorization, and pre-processing functions in the same device. Such synaptic devices achieve impressive electronic characteristics, including current on/off ratio of 10^9 and mobility of 45 $cm^2V^{-1}s^{-1}$. Through constructing optoelectronic device array, we achieve target extraction process with wavelength-selective capability in noisy environment, closely resembling human retina for color recognition. The above outcomes bring a notable improvement from 72 % to 96 % in image recognition accuracy.

Thirdly, drawing inspiration from object motion sensitive ganglion cells, we propose OMD vision sensor with simple device structure by constructing WSe_2 homojunction modulated by ferroelectric copolymer. Operating under optically and zero power consumption mode, vision sensors can generate progressive and self-powered positive/negative photocurrents with discrete and uniform multi-states facilitated by intermediate ferroelectric modulation. This design enables a reconfigurable device to emulate long-term potentiation and depression for synaptic weights updating, which exhibit multi-levels exceeding 6 bits of 82 states resolution and uniform step of 6 pA. Such OMD devices also demonstrate non-volatility, reversibility, symmetry, and ultra-high linearity with fitted R^2 of 0.999 and 0.01/-0.01 nonlinearity values. Thus, vision sensors could implement motion detection by sensing only dynamic information while eliminating redundant data from static scenes. Neural network based on linear results

can recognize the essential moving features with high recognition accuracy 96.8%. We also present scalable potential via a 3×3 neuromorphic vision sensor array.

2D semiconductor/ferroelectric hybrids could mature rapidly and make inroads into modern electronics by simultaneously progressing in the material, device, and system levels. It is foreseen that such a combination could continue to offer more innovative opportunities.

List of Publications

1. **Zhaoying Dang,** Feng Guo, Zhaoqing Wang, Wenjing Jie, Kui Jin, Yang Chai, and Jianhua Hao, "Object motion detection enabled by reconfigurable neuromorphic vision sensor under ferroelectric modulation", *ACS Nano* 18, 27727 (2024).

2. **Zhaoying Dang,** Feng Guo, Yifei Zhao, Kui Jin, Wenjing Jie, and Jianhua Hao, "Ferroelectric modulation of ReS_2-based multifunctional optoelectronic neuromorphic devices for wavelength-selective artificial visual system", *Adv. Funct. Mater.* 34, 2400105 (2024).

3. **Zhaoying Dang**, Feng Guo, Huan Duan, Qiyue Zhao, Yuxiang Fu, Wenjing Jie, Kui Jin, and Jianhua Hao "Black phosphorus/ferroelectric P(VDF-TrFE) field-effect transistors with high mobility for energy-efficient artificial synapse in high-accuracy neuromorphic computing", *Nano Lett.* 23, 6752 (2023) (Selected as a supplementary cover).

4. **Zhaoying Dang**, Feng Guo, Zehan Wu, Kui Jin, and Jianhua Hao, "Interface engineering and device applications of 2D ultrathin film/ferroelectric copolymer P(VDF-TrFE)", *Adv. Physics Res.* 2, 2200038 (2023).

5. Feng Guo, Weng Fu Io, **Zhaoying Dang**, Yuqian Zhao, Sin-Yi Pang, Yifei Zhao, Xinyue Lao, and Jianhua Hao, "Bio-Inspired optoelectronic neuromorphic device based on 2D vdW ferroelectric heterostructure for nonlinearly preprocessing visual information and convolutional operation", *Adv. Electron. Mater.* DOI: 10.1002/aelm.202400528 (2024).

6. Feng Guo, Weng Fu Io, **Zhaoying Dang**, Ran Ding, Sin-Yi Pang, Yuqian Zhao, and Jianhua Hao, "Achieving reinforcement learning in a three-active-terminal neuromorphic device based on a 2D vdW ferroelectric material", *Mater. Horiz.* 10, 3719 (2023).

7. Yuqian Zhao, Zehan Wu, **Zhaoying Dang**, and Jianhua Hao, "Progress in the synthesis of 2D black phosphorus beyond exfoliation", *Appl. Phys. Rev.* 9, 041318 (2022) (Featured Article).

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Chapter 1 Introduction

1.1 Overview of neuromorphic development

With the exponential increase in information volume and the high-speed pace of transmission, particularly fueled by the advancements on the Internet and digital technology, individuals today confront a deluge of information requiring efficient processing. The need for hardware performance revolves around minimizing redundancy, maximizing power efficiency, and effectively handling extensive data calculations.[1] On the other hand, in the present von Neumann architecture based on metal oxide and semiconductor (MOS), the processing and storage units are physically segregated (Figure 1-1), leading to substantial time and energy wastage during data bus transmission.[2-3]

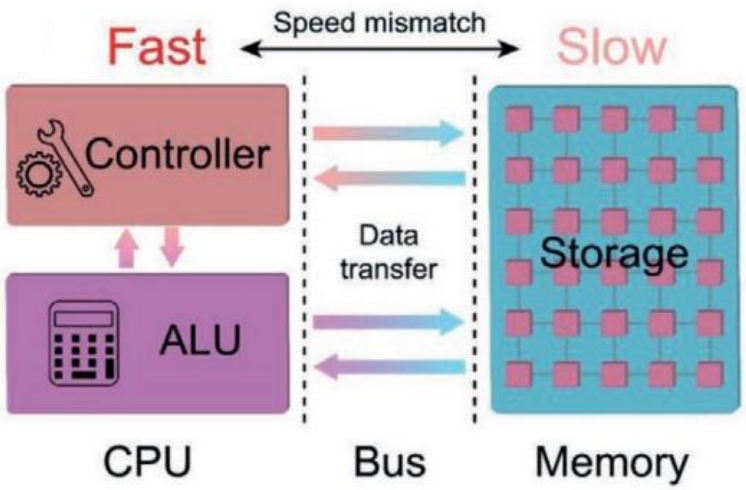


Figure 1-1 Traditional Von-Neumann architecture.[4]

Additionally, the mismatch between computing and memory performance has created a memory wall bottleneck, restricting data processing due to limited storage bandwidth.[5-6] Consequently, there is an urgent need to develop novel electronic

devices and data processing and calculation methods to address these challenges.

1.1.1 Generation of neuromorphic computation

The word of "neuromorphic" is first provided by Carver Mead in 1990s.[7-8] It refers to hybrid large-scale integrated computing systems including digital and analogue inspired by the neural architecture of the brain. The human brain can directly encode and manipulate information through massive parallel processing because information storage and processing are not separated.[9] Inspired from human brain, neuromorphic platforms include the following characteristics: analog data processing, asynchronous communication, and massively parallel information processing.[10] Designing of novel electronic devices can be regarded as one research orientations of neuromorphic computation. The goal is to emulate the structure and operation of biological neural networks, implementing dedicated electronic neural architectures including neurons and synapse circuits (Figure 1-2).

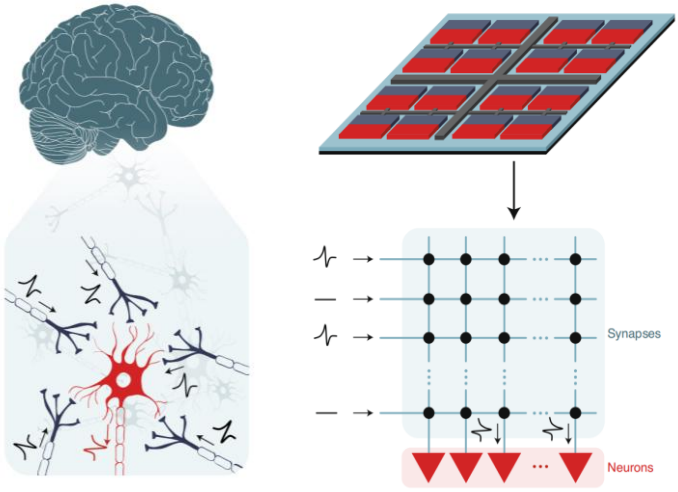


Figure 1-2: Schematic of the biological brain, neurons, and synapses architectures.[9]

Neuromorphic computation demonstrates significantly lower power consumption

than traditional processors due to the integration of non-volatile memory technologies and analog/digital circuitry processing units, as well as their learning capabilities in complicated data contexts. If fundamental technological challenges are addressed in the coming years, the development of energy-efficient and high-speed neuromorphic computers, along with advancements in neuromorphic device technology, will be propelled forward.

1.1.2 Construction of artificial neural network (ANN)

ANN origins from research on the biological nervous system and have evolved into a distinct branch of machine learning referred to as connectionist learning.[11] Through the modeling process based on biological neural system, researchers have put forward several essential concepts, including neurons, connections, weights, and layers, as shown in Figure 1-3.

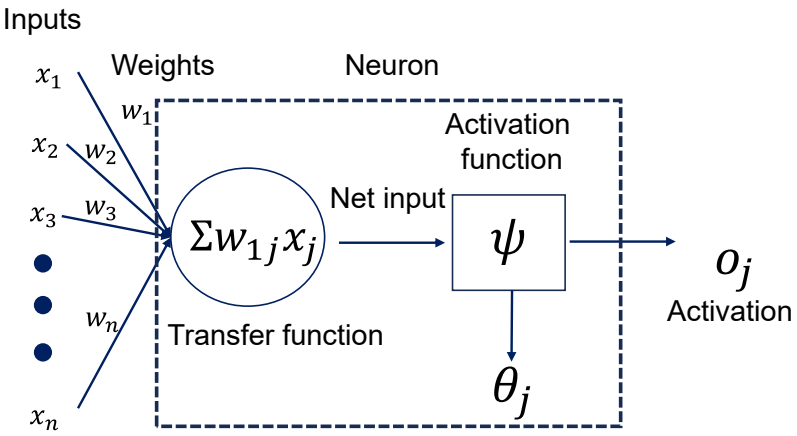


Figure 1-3: Illustration of the M-P neuron model, depicting essential components such as inputs, weights, and activation function.

The symbol x_i represents the connection to other neurons, signifying input signals (Input). The arrows originating from the input signals represent weights (w_i), indicating

the multiplication of x_i with its corresponding w_i. The resulting product is then input into the neuron. The neuron comprises two key components: net input, which is the summation of all input and weight products and threshold, which is combined with the net input and fed into the activation function. The activation function maps the net input to the output. Commonly employed activation functions include sigmoid, tanh, ReLU, Leaky ReLU, Maxout, and ELU.[12-13]

Just like neurons in biological neural systems, neurons in ANN receive information from other neurons and perform input aggregation based on the strength of their connections. The inputs are weighted and summed accordingly. The aggregated result is then subjected to modification by a threshold, while the activation function maps the modified result to provide output for subsequent neurons. The above neurons serve as the fundamental unit of ANNs, and the neural networks are formed by assembling neurons in a hierarchical structure including input, hidden and output layers (Figure 1-4). Computationally, ANNs consist primarily of two components: inference and training. Inference involves inputting information into the neural network and computing the output through successive layers. Training employs the results obtained from inference to compute the necessary weight adjustments, aiming to progressively approximate the desired output of the neural network.

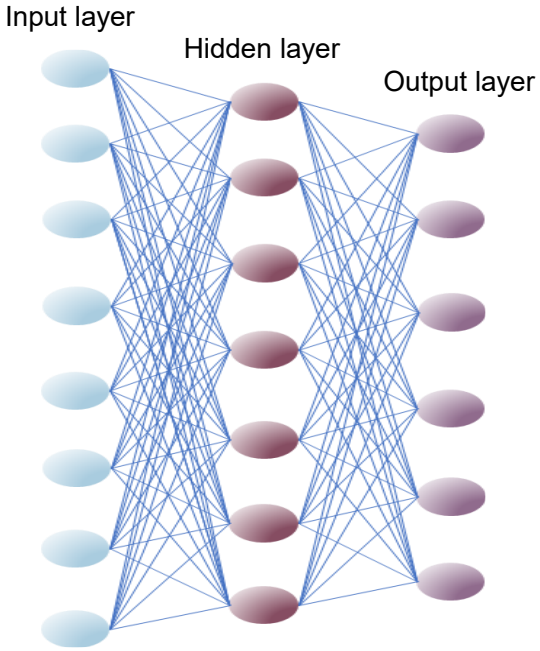


Figure 1-4 Multi-layers artificial neural network include input layer, hidden layer and the output layer.

ANNs are known for their data-driven computation, which is characterized by the presence of a large number of parameters and the necessity of utilizing extensive datasets during training to achieve effective feature extraction by the network.[14] Furthermore, the computational operations within ANNs primarily involve multiplication and addition, resulting in relatively modest demands on the general computational capabilities of processors.[15] Moreover, the operations between individual neurons in ANNs are largely independent, thus allowing for efficient parallel computations.[16] These distinctive characteristics underscore the importance of processors that possess high read bandwidth and robust parallel processing capabilities when applied in the context of ANNs.

Figure 1-5 demonstrates one application of multilayer perceptron (MLP) to classify

handwritten digits in the dataset of Modified National Institute of Standards and Technology database (MNIST), which was published in nature communications by Professor A. Q. Liu in 2021.[17] The researchers developed an optical neural chip and applied the recognition process to both complex-valued and real-valued neural networks. The initial 28 × 28 grayscale image is transformed into a compressed representation of four features by the input layer, after being reshaped into a 784 × 1 vector. The network architecture includes an input layer, a 4 × 4 hidden layer, and an output layer that maps the four hidden outputs to 10 classes, representing digits from 0 to 9. The model is trained using the complete training set, and 200 instances from the testing set are employed for on-chip validation. Figure 1-5(c) demonstrates that the complex-valued neural network outperformed its real-valued counterpart, achieving training and testing accuracies of 93.1% and 90.5%, respectively. These results provide evidence for the successful completion of the image recognition task.

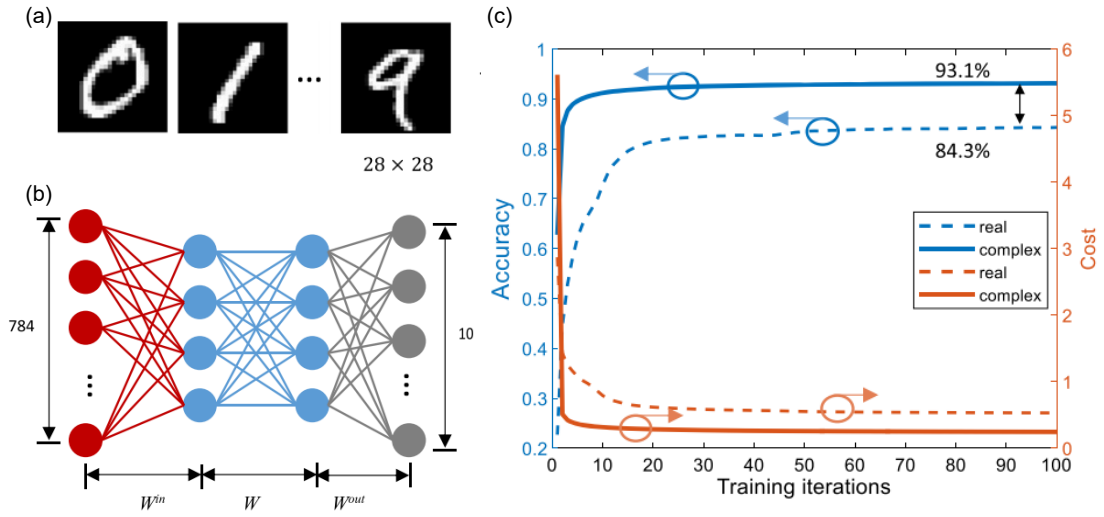


Figure 1-5: Application of multilayer perception (MLP). (a) The transformation of the

input image, initially sized as 28 × 28, into a stretched vector of dimensions 784 × 1. (b) The network architecture comprises an input layer (W_{in}), a hidden layer (W), and an output layer (W_{out}). Experiment includes all 10 digits, and the output layer maps the four hidden outputs to these 10 classes. (c) A performance comparison between the complex-valued and real-valued networks implemented on the same chip.[17]

1.2 Neuromorphic devices and their applications

Despite notable strides in the field of neural morphology computation, the cost associated with implementing artificial neurons and synapses using complementary metal-oxide-semiconductor (CMOS) technology and large-scale integrated circuits continues to be substantial. A few hundred transistors can merely simulate a restricted number of neurons and their corresponding synapses, whereas the human brain boasts an astonishing count of over 10^{11} neurons and 10^{15} synapses. Hence, relying solely on transistor stacking to attain AI on par with the human brain remains far from practical. Therefore, neuromorphic computation necessitates its own unique logic and devices.

1.2.1 Three typical memory electronic devices

In order to propel the progress of neuromorphic computing and the revolution of current state-of-the-art CMOS based platforms for lower power consumption and higher scalability, the exploration of novel materials and devices plays a critical role. By developing innovative electronic devices and customizing their characteristics, it becomes feasible to simulate the properties in biological elements, including synapses and neurons. Among versatile devices, memory devices have emerged as promising

contenders for achieving low-power and high-density within neuromorphic circuits. This is primarily attributed to their capability to modulate conductivity in response to electrical or optical pulses. Initially binary non-volatile memories are employed predominantly to facilitate high-performance solid-state storage. However, novel memory devices have evolved to offer analog tunability of conductivity and intricate switching dynamics. Consequently, these devices have the potential to enable novel computational functionalities, such as analog computation and the application of brain-like learning rules. Resistive random-access memory (RRAM), phase-change memory (PCM), and ferroelectric field-effect transistors (FeFETs) are three representative types of memory electronic devices that hold significant relevance in the field (Figure 1-6). RRAM is commonly characterized as a two-terminal passive device comprising of two metal electrodes separated by an intermediate insulating layer, typically composed of oxides like hafnium oxide (HfO_x) or tantalum oxide (TaO_x).[18] By applying bias voltages to the two terminals, the resistance of device can be alternated between high-resistance state (HRS) and low-resistance state (LRS). The resistance switching mechanisms in RRAM devices can be primarily classified into two categories: filamentary and interface-based mechanisms.[19-20] In the filamentary mechanism, an external electric field prompts the migration of metal ions from one electrode to the other, leading to the formation of precipitates that establish conductive paths. In the case of an oxide intermediate layer, the migration of oxygen ions generates conductive paths through oxygen vacancies. Conversely, the interface-based mechanism relies on

regulating the distribution of oxygen vacancies at the electrode/oxide or oxide/oxide interfaces, thereby demonstrating the resistance state transition process in the device.

Similarly to RRAM, phase-change memory (PCM) also operates as a two-terminal device with a sandwich-like configuration, featuring two metal electrodes separated by a layer of phase-change material.[21-22] These phase-change materials commonly consist of compounds based on Ge, Sb, and Te. By applying electric pulses to the electrodes, Joule heating is induced, enabling control over the proportion of crystalline and amorphous regions within the phase-change material. The transition between the crystalline and amorphous states aligns with the resistance state transition in the PCM device.[23]

FeFETs are a type of field-effect transistors in which ferroelectric materials are employed as the gate dielectric.[24] The phenomenon of ferroelectricity was initially discovered by Valasek in 1920.[25] It elucidates the remarkable capability of non-centrosymmetric crystalline materials to manifest non-volatile and adjustable polarization due to the formation of enduring electric dipoles. These transistors demonstrate the ability to exhibit non-volatile and multi-levels conductance states owing to the formation of stable electric dipoles for adjustable polarization within non-centrosymmetric crystal materials. When an external voltage is applied to a ferroelectric capacitor, transitioning from a negative to a positive value, a non-volatile polarization reversal takes place within the ferroelectric domains. This reversible process involves the transformation of the polarization state from a downward orientation to an upward

orientation, which can endure even after the voltage is returned to zero. Consequently, by employing non-volatile ferroelectric thin films as the gate dielectric in field-effect transistors, the channel of transistors can be modulated in a non-volatile manner due to the enduring nature of ferroelectric polarization. As a result, the corresponding transfer characteristics exhibit a substantial hysteresis window, thereby demonstrating a prominent hysteresis effect. A more comprehensive discussion on FeFETs will be emphasized in subsequent sections.

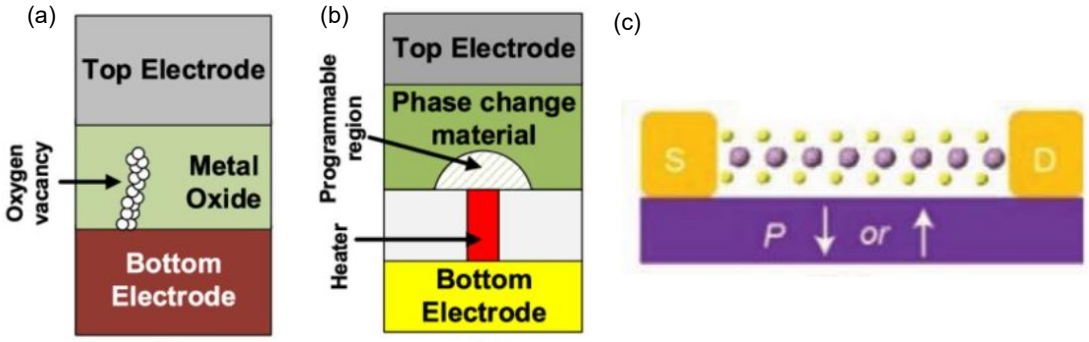


Figure 1-6: Structure of three typical memory electronic devices (a) RRAM, (b) PCM, and (c) FeFETs.[26-27]

1.2.2 Artificial synaptic devices

Brain-inspired computing chips provide an energy efficient approach for new chip architectures and device technologies. Each neuron is interconnected by more than 10000 synapses (Figure 1-7) in human brains responsible for receiving and transmitting signals to other neurons.[28] Upon the arrival of an action potential at the presynaptic neuron, neurotransmitter filled within the presynaptic neuron are released into the synaptic cleft. Through synaptic transmission, the neurotransmitter binds to receptors situated on the postsynaptic neuron. The resulting membrane potential changes in the

postsynaptic neuron are contingent upon the type of neurotransmitter released, such as calcium ions, sodium ions, potassium ions, or chloride ions. Once a specific threshold is reached, the postsynaptic neuron generates a fresh action potential. Consequently, synapses possess two fundamental properties: synaptic signal transmission and synaptic plasticity.[29-30] Synaptic signal transmission denotes the transfer of information between neurons via synapses. The action potential (electrical signal) of the presynaptic neuron undergoes conversion into neurotransmitter release (chemical signal). The efficiency of synaptic signal transmission can be adjusted by synaptic weights, where larger weights indicate greater neurotransmitter release and stronger connection strength during the transmission process. Synaptic plasticity pertains to the capacity of synaptic weights to be modulated based on the historical activity state of the neurons. Artificial electronic synaptic devices can mimic the biological functions of neurons such as synaptic plasticity of excitatory or inhibition to post-synaptic terminal by controlling neurotransmitter release, thereby facilitating the realization of synaptic functionalities.

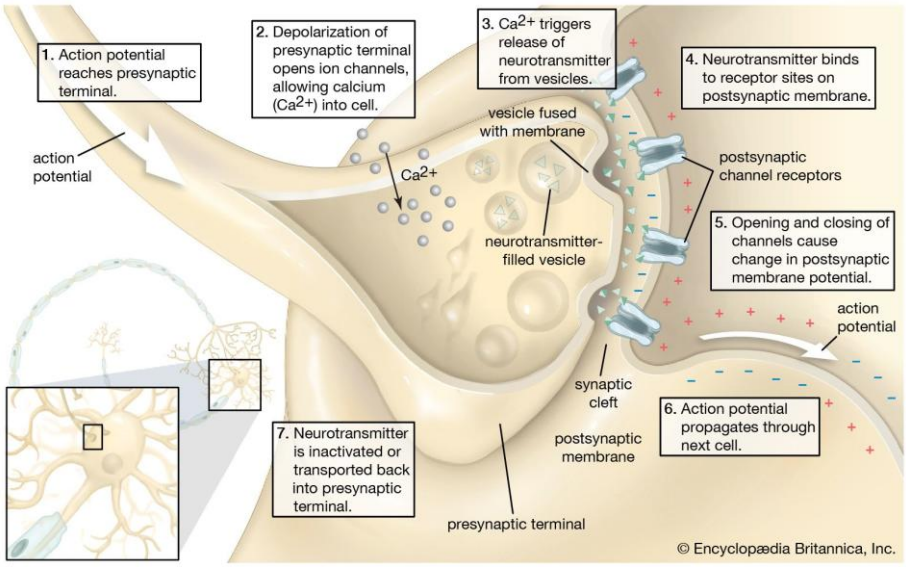


Figure 1-7: A schematic diagram depicting synaptic connections, which serve as the medium for information transmission between two neurons. (Image from the website: https://www.britannica.com/science/synapse)

The non-volatile and adjustable conductive states exhibited by neuromorphic devices can serve as replacements for adaptable synaptic weights. The input signal, which corresponds to the presynaptic neuron pulse, is applied to either the top electrode of a two-terminal device or the source electrode of a three-terminal transistor. This input signal is then multiplied by the conductance of device, representing the synaptic weight, resulting in the current output value. Larger synaptic weights yield greater output values. Synaptic plasticity can be emulated through mechanisms such as ion migration or polarization reversal of the gate dielectrics. Several classical synaptic plasticity simulations based on novel neuromorphic devices are described below.

(1) Short-term plasticity

Short-term plasticity encompasses the evanescent and reversible modulations in

synaptic weights within a temporal range spanning from milliseconds to minutes. These alterations depend upon the historical activity of synapses, giving rise to both short-term potentiation and short-term depression phenomena. The effective replication of short-term plasticity in synapses can be attained by harnessing various mechanism such as charge transfer in the hybrid inorganic–organic heterojunction.[31] Figure 1-8 demonstrates the PPD and PPF processes with a dynamic decline/enhancement of neurotransmitter release within MoS_2/PTCDA devices because the electrons transfer in both directions. Here, we take the PPF behavior as an example. The PPF phenomenon, representing a prototypical manifestation of short-term plasticity, denotes the augmentation of the postsynaptic neuron membrane potential when a pulse closely follows another. Figure 1-8(a) illustrates that the application of a second pulse immediately after the first pulse yields higher current values compared to the current elicited by the first pulse alone. As the time interval between the second and first pulses lengthens, the contribution of the augmented current diminishes. Figure 1-8(b) summarizes the correlation between the PPF ratio and the time interval, where the PPF ratio is defined as the ratio of the currents generated by the second pulse to the absolute value of the current produced by the first pulse, A2/A1. The PPF exhibits an exponential decay trend as the pulse time interval increases, aligning with the characteristics observed in biological synapses. This alignment validates the successful emulation of short-term plasticity by the MoS_2/PTCDA devices. Regarding the PPD phenomenon, the inhibitory synapse exerts additional suppression on the magnitude A of the

postsynaptic current with A2 < A1. Consistently, as the time interval Δt increases from 25 to 12,000 ms, both the PPD and PPF processes gradually approach 100% convergence, as anticipated.

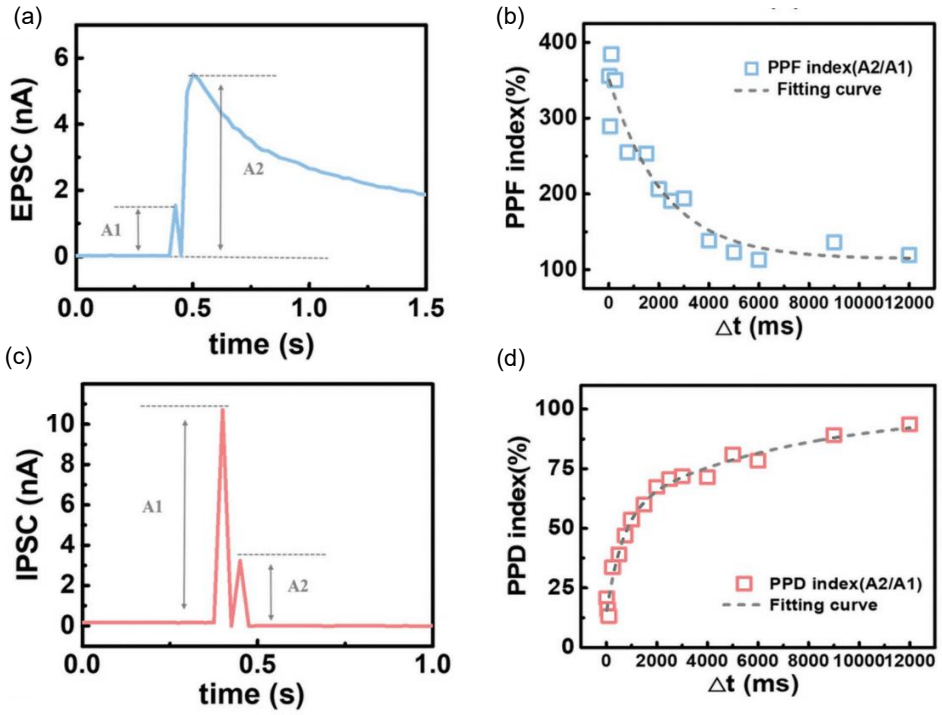


Figure 1-8: Short-term plasticity. The excitatory post-synaptic current (a) and inhibitory post-synaptic current (c) characteristics of the MoS_2/PTCDA hybrid heterojunction synaptic transistor elicited by a pair of gate pulses. The pulse intervals are set at 25 ms. The PPF index (b) and PPD index (d) denoted by A2/A1 are presented as a function of the interval time (Δt). The gray dashed line represents the fitting result obtained using a double exponential decay function.[31]

(2) Long-term plasticity

Unlike short-term plasticity, long-term plasticity represents the continuous changes in synaptic weights, lasting from hours to even several months.[32-33] The process of

increasing synaptic weights is known as long-term potentiation (LTP), whereas the decreasing synaptic weights is known as long-term depression (LTD). In neural synaptic devices, the implementation of LTP and LTD behaviors requires multi-conductance states. Simulating synaptic weight updates based on LTP and LTD behaviors is often considered for weight adjustment in ANNs.[34-35] The evaluation of simulated synaptic weight update behavior is primarily guided by several criteria: the stability of conductance states (multi-levels), the ratio between the maximum and minimum conductance in the weight update behavior (dynamic range or G_{max}/G_{min}), the symmetry and nonlinearity of LTP and LTD behaviors, as well as the uniformity among the multiple operations (cycle-to-cycle variation).[36-37] The quality of simulated synaptic weight update behavior will influence the recognition accuracy greatly in large-scale ANNs. As depicted in Figure 1-9, within the context of one-dimensional ferroelectric organic transistors integrated on a 100-micrometer silver wire, the gradual alteration of post-synaptic currents (PSC) corresponding to LTP and LTD is achieved through the application of continuous input pulse trains.[38] Notably, the dynamic range exhibits an increment in conjunction with the gate voltage ranges. Furthermore, the repetitive transition cycles of LTP and LTD reach a remarkable magnitude of 600 continuous cycles.

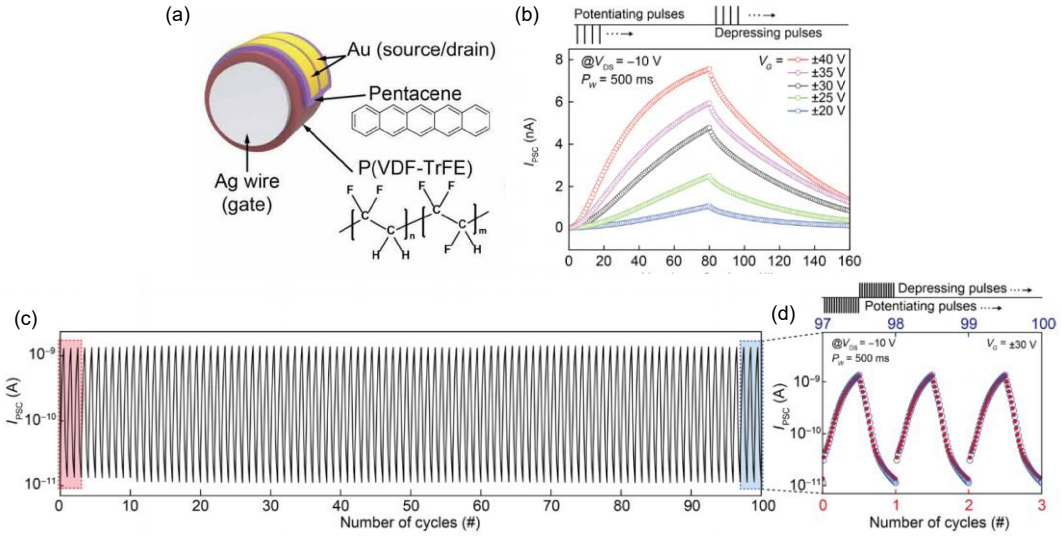


Figure 1-9: Long-term plasticity behavior. (a) Schematic representation of the one-dimensional organic artificial multi-synapses. (b) LTP and LTD behaviors observed under different pulse amplitudes with gate voltages ranging from ±20 to ±40 V. (c) Repetitive transitions of LTP and LTD over 100 cycles; and (d) First and last three cycles of the LTP and LTD processes shown in (c).[38]

(3) Spike-timing-dependent plasticity (STDP)

STDP represents the integration of LTP and LTD mechanisms, incorporating a temporal dimension. Synaptic weight updates between pre-neurons and post-neurons are contingent upon the temporal discrepancy between pre-synaptic and post-synaptic spikes arrival moment (Figure 1-10).[39-40] If the post-synaptic spikes are subsequent to pre-synaptic spikes, signifying a causal association between the interconnected pre- and post-neurons. In this regard, synaptic weights increase, reflecting the LTP behaviors. Furthermore, a reduced temporal gap between pre- and post-synaptic spikes indicates a heightened correlation between the neurons, resulting in a more substantial enhancement of synaptic weight. As the temporal discrepancy expands, the magnitude

of weight increase exhibits an exponential decay pattern. Conversely, when post-synaptic spikes preceded pre-synaptic spikes, it implies that the contribution to the post-synaptic spike predominantly originates from other pre-synaptic spikes rather than the specific pre-neuron. Consequently, synaptic weights connecting the pre- and post-neurons decrease, implying the occurrence of LTD behavior.

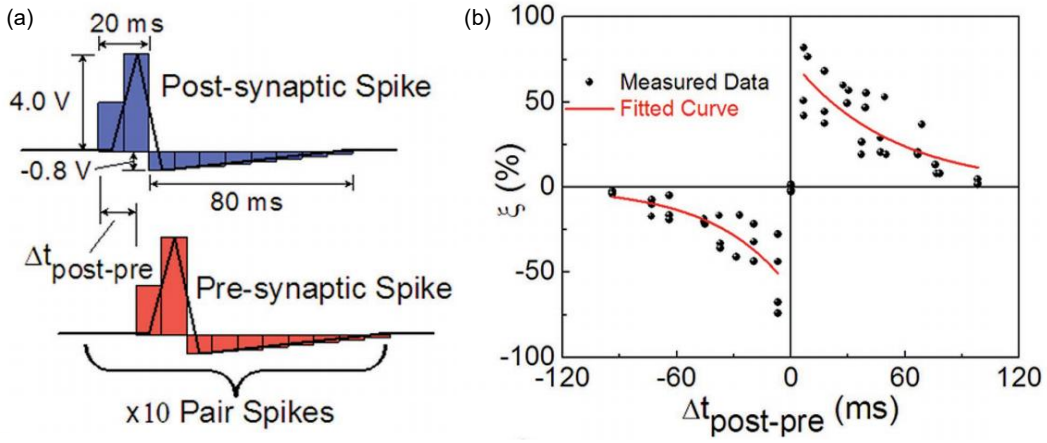


Figure 1-10: STDP behavior. (a) Illustration depicting pre- and post-synaptic spikes as defined for measuring STDP. (b) Temporal progression of synaptic weight in relation to the time interval between pre- and post-spikes.[41]

1.2.3 Versatile perceptual simulation based on neuromorphic devices

Versatile sensory perceptions include vision, smell, hearing, and tactile sense enable human to gather information from our lives.[42] Synapse-like connections with neurons undergo preliminary information pre-processing for sensory organs. This preprocessing involves intelligent functions such as modulation, filtering, amplification, and memorization, which occur prior to the transmission of information to the brain.[43] Here we mainly discuss the vision and tactile sense, which have been extensively studied and documented in the literatures.

In 2020, Nae-Eung Lee and colleagues presented a remarkable advancement in the field of tactile sensory organs through introducing a flexible and artificial synaptic device, inspired by Merkel cell-neurite complexes (Figure 1-11(a)).[44] This innovative device exhibits two distinct types of modulation: sensory memory and slow adaptation. The modulation is achieved through the adjustment of the nanocomposite composition of the gate dielectric layer and the switching of ferroelectric dipoles. The flexibility of the polyimide substrate enables its application in soft biomimetic devices, particularly in the development of intelligent soft electronic skins. Upon touch stimulation, the alignment of dipoles in the ferroelectric gate dielectric is induced by the triboelectric-capacitive coupling effect. This alignment, in turn, modulates the post-synaptic current signal, enabling the transduction of tactile information in a self-energy manner.

The encoding of multisensory information represents a crucial aspect in sensory processing. In 2022, Das et al. introduced a neuromorphic device that integrates a triboelectric tactile sensor with a photosensitive transistor, enabling the realization of visual and tactile sensing functions (Figure 1-11(b)).[42] This device successfully mimics the characteristic features and functionalities of a multisensory neuron, demonstrating a notable advancement in this field. It is worth noting that only a limited number of studies have truly captured the distinctive attributes of multisensory integration. For instance, Tang et al. attempted to perceive digits in a complex environment by employing both visual and tactile functions (Figure 1-11(c)).[45] However, their approach utilized electrical pulses to represent the output signals from

the tactile sensor. A method that can be easily achieved through the use of tactile sensors and through the conversion of pressure into electrical signals.

Furthermore, we firmly believe that the influence of multisensory integration should extend beyond the realms of visuo-tactile information processing, offering significant implications for various domains such as defense, space exploration, robotics, and AI systems. Additionally, the principles of multisensory integration can be extrapolated to encompass a broader range of sensory stimuli, including auditory, olfactory, thermal, and gustatory. This expansion opens up new avenues for research and potential applications in diverse sensory contexts.

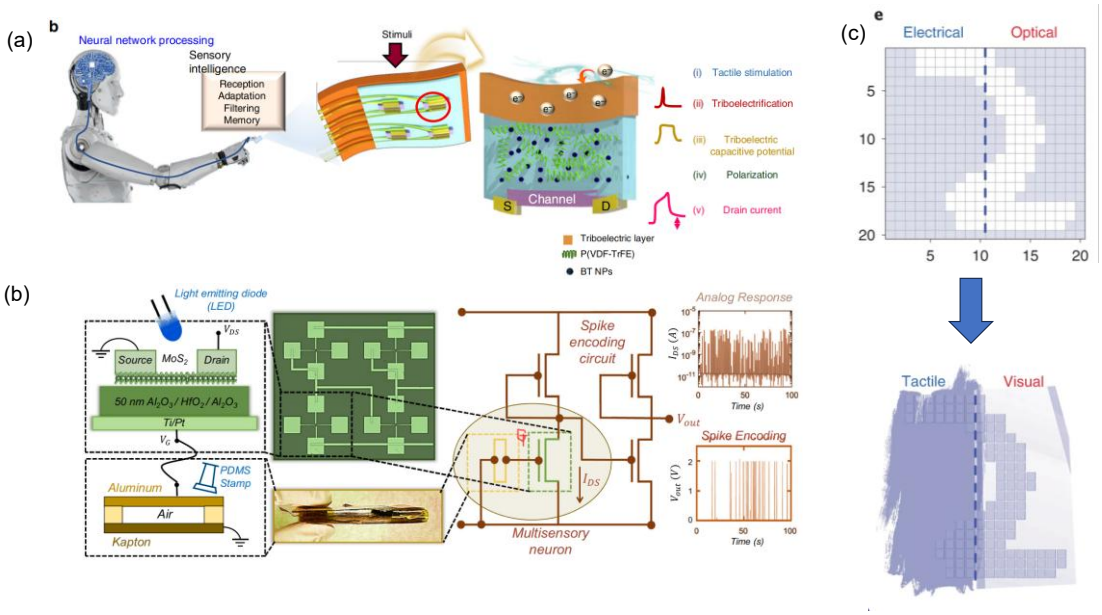


Figure 1-11: Perceptual simulation based on neuromorphic devices. (a) The reception of tactile stimuli occurs through a self-energy transducing mechanism via triboelectrification during finger touch in a flexible, artificial tactile sensory organ. (b) A bio-inspired visuo-tactile multisensory neuron is composed of a triboelectric tactile sensor connected to a photo transistor, accompanied by the associated spike encoding

circuit. (c) Detection of digits within a complex environment. The visual input is represented by optical pulses, while the tactile input is represented by electrical pulses.

From another perspective, neuromorphic vision sensors have been widely investigated recently. Presently, neuromorphic devices based on ANNs predominantly focus on visual tasks, such as image recognition and motion detection.[46] As a result, a comprehensive hardware system necessitates the inclusion of visual sensor units responsible for converting external visual information into electrical signals. The data generated by these visual sensors undergoes subsequent processing and enters the hardware for further computation and analysis, ultimately enabling the accomplishment of visual tasks.[47] Neuro-inspired vision sensor draws inspiration from our human eye's retina, as well as an innovative sensor-computation architecture (Figure 1-12(a)).[48] The computational framework employed in near-vision sensors incorporates specific preprocessing tasks at the sensor level, including noise reduction, contrast enhancement, and adaptive light intensity adjustment.[49-50] Through the execution of these preprocessing tasks, the volume of data can be effectively reduced, or irrelevant data can be avoided, leading to enhanced accuracy in subsequent data analysis and decision-making processes. Furthermore, the integration of sensing, storage, and computation within a unified architecture extends this concept by enabling the direct execution of more intricate high-level tasks, such as image recognition at the sensor level.[51] By conducting data processing and computation directly within or in close proximity to the

sensor, the requirement for extensive data transmission is significantly mitigated, resulting in improved bandwidth utilization and data processing efficiency, along with reduced computational power consumption and latency (Figure 1-12(b)).

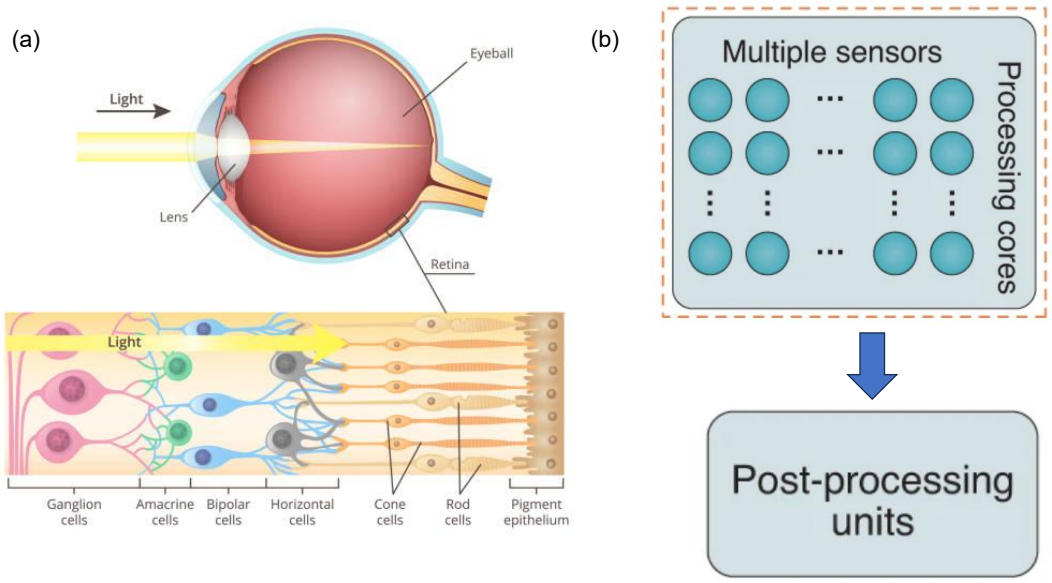


Figure 1-12: (a) Human retina structure. (b) In-sensor computing architecture.[52]

1.3 Research Status of 2D semiconductor/ferroelectric transistor

Ferroelectric materials have emerged as highly promising candidates for analog biomimetic synaptic devices and the advancement of neuromorphic computing systems, thanks to their unique non-volatile multi-state effects. The integration of 2D semiconductors with ferroelectrics has sparked considerable interest in both technology and academia. In recent years, the hybrid structure of 2D semiconductors/ferroelectric materials has led to the development of FeFETs and ferroelectric tunneling transistors, leveraging the proximal coupling within the system.[53-55] Consequently, there has been a significant rise in both theoretical studies and experimental investigations focused on the synergetic effect between 2D semiconductors and ferroelectrics (Figure 1-13). In

this section, we will provide a brief overview of 2D materials, ferroelectrics, and their applications in neuromorphic devices.

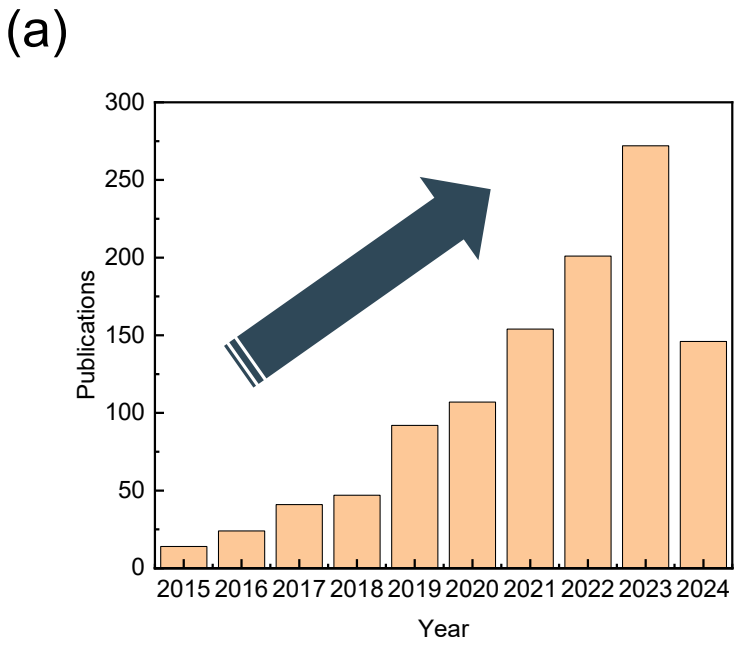


Figure 1-13: (a) The number of publications concerning 2D materials and ferroelectric materials searched by the web of science.

1.3.1 Brief overview of 2D materials

Elemental silicon-based microelectronic circuits have been continuously advancing in accordance with Moore's Law, relying on CMOS technology.[56] However, the development of highly integrated circuits encounters several technological challenges, including photolithography limitations imposed by minimum feature size, device integration, and interconnection.[57-58] Therefore, it becomes crucial to explore alternative options for miniaturization, particularly as traditional silicon-based transistors approach their physical limits. The emergence of 2D materials, such as graphene, transitional metal dichalcogenides (TMDCs), and BP, presents new

opportunities for fundamental electrical investigations. [59-66] 2D materials possess highly controllable properties that can be tuned through various methods, including electrostatic gate voltage, external strain, and chemical doping. For instance, the application of strain to BP materials can modify their energy bandgap and carrier migration along the zigzag direction, leading to topological phase transitions.[67] Our research group has also investigated the effect of biaxial strain on the Raman spectra of graphene on a piezoelectric substrate.[68] Furthermore, 2D materials exhibit atomically flat surfaces, lack dangling bonds, and possess layered van der Waals (vdWs) bonds. These distinctive characteristics make them suitable for constructing planar or vertical vdWs heterostructures through direct stacking (Figure 1-14)[69] Our group has also conducted a review on wide bandgap 2D materials-based hybrid heterostructures, highlighting their various device applications.[70]

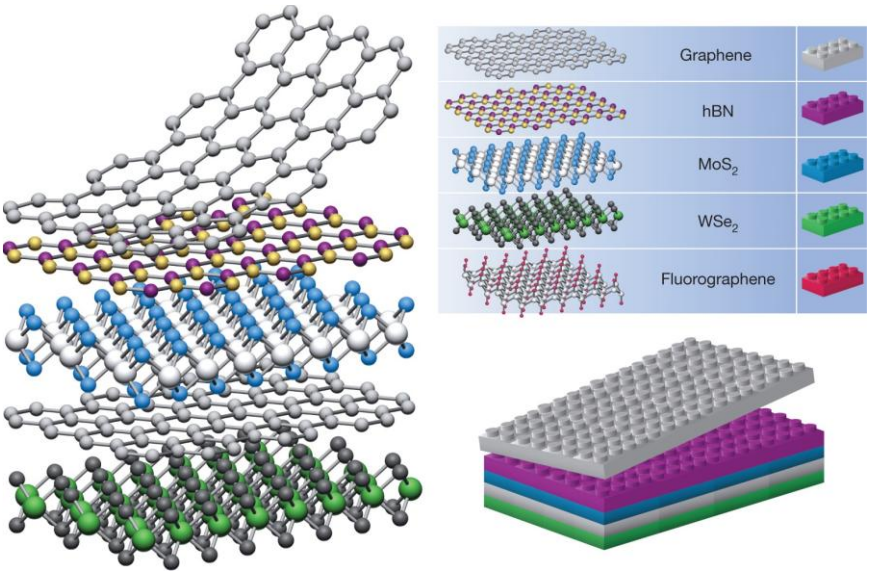


Figure 1-14: 2D materials and heterostructures based on them.[69]

Two primary methods widely employed for obtaining 2D materials are direct

mechanical exfoliation of layered vdWs semiconductors from single crystals and large-scale fabrication of 2D semiconductors on desired substrates. Mechanical exfoliation, although a trial-and-error process, has become the primary choice for initial scientific research on 2D materials. Typically, the exfoliation technique serves as a testbed for device optimization. Researchers have observed weak vdWs bonds between 2D layers after obtaining monolayer graphene from bulk graphite through exfoliation to maintain a single-crystal structure.[71-72] Consequently, precise exfoliation and transfer processes onto hosts have become focal points. In 2018, Shim et al. introduced the layer-resolved splitting (LRS) technique based on interfacial toughness differences, as depicted in Figure 1-15(a).[73] They utilized a 600 nm nickel film as the atomic adhesive to produce wafer-scale monolayer 2D materials. Subsequently, Huang et al. employed the Au-assisted mechanical exfoliation method and isolated over 40 types of single-crystalline monolayers (Figure 1-15(b)).[74] Unlike the LRS technique, the 2 nm Au-assisted exfoliation method eliminated the transfer step, and the gold film needed to be removed using a KI/I_2 solution for heterostructure integration.

In contrast, uniform, scalable, and thickness-controllable synthesis methods are more suitable for industrial applications of 2D materials. Conventional large-area growth techniques include chemical vapor deposition (CVD), pulsed laser deposition (PLD), and molecular beam epitaxy (MBE). Notably, our research group has summarized the advances in preparing 2D materials using the PLD method.[75] Specifically, we have achieved centimeter-scale growth of BP through pulse layer deposition and developed

large-scale BP-based devices, as depicted in Figure 1-15(c).[76] Further discussions on growth techniques and mechanisms can be found in other review articles.[77] However, directly growing large-area 2D materials on ferroelectric layers remains challenging due to compatibility issues and the potential degradation of 2D materials in high-temperature and high-pressure environments. Therefore, transferring 2D materials to ferroelectrics has emerged as another crucial topic, facilitated by the dangling bond-free surface of the 2D layers.[78] Recently, the robotic four-dimensional pixel assembly method (Figure 1-15(d)) has emerged for manufacturing vdWs heterojunctions with high speed and accuracy.[79] This technique has enabled the exploration of exotic physical phenomena through twisted structures.[80]

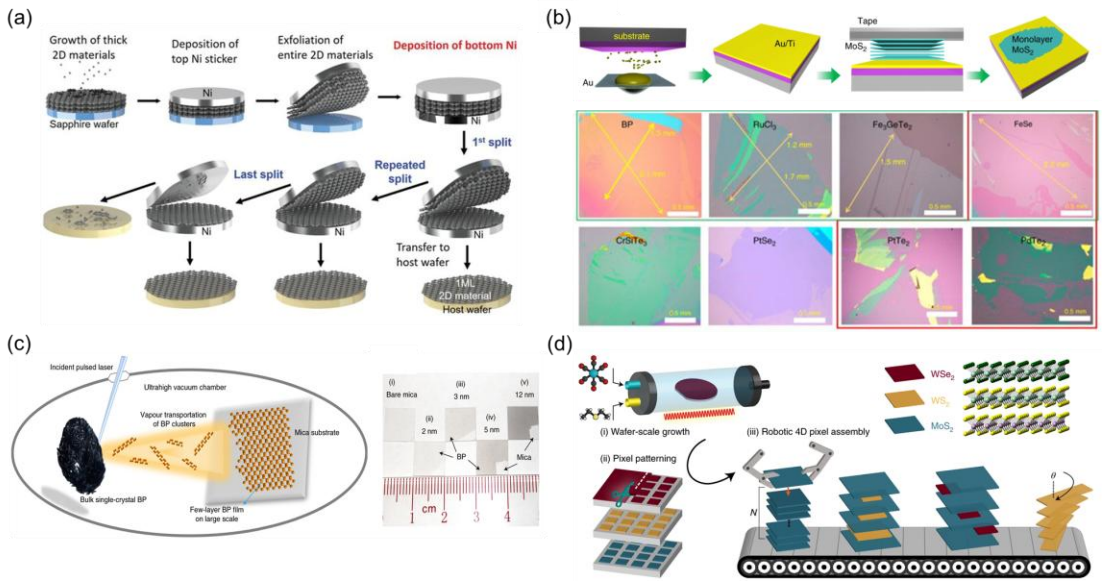


Figure 1-16: 2D materials fabrication method. (a) Processing flow of LRS for 2D materials lamination.[73] (b) Au-assisted mechanical exfoliation process (top) and optical images of the obtained large-area 2D materials (bottom).[74] (c) PLD process for fabrication of few-layer BP films, and images of BP films with different

thicknesses on mica substrate.[76] (d) Graphical representation of robotic four-dimensional pixel assembly.[79]

1.3.2 Mechanism of ferroelectric copolymer P(VDF-TrFE)

Ferroelectric materials exhibit switchable spontaneous polarization below the Curie point (T_c) due to the specific crystal class with a polar axis.[81] The ferroelectric phenomenon arises from the relative shift of cations and anions within the unit cell at the structural level. As intrinsic hierarchical materials, twenty non-centrosymmetric point groups constitute the basic piezoelectric structures, wherein negative and positive charges reside on opposite surfaces under stress. Out of these twenty piezoelectric point groups, ten possess unique polar axes and temperature-dependent spontaneous polarization, forming the pyroelectric point groups. However, only those materials whose spontaneous polarization can be reversed by an electric field are classified as ferroelectrics. Consequently, the strict structural requirements limit the range of materials that exhibit ferroelectric behavior, as illustrated in Figure 1-17.

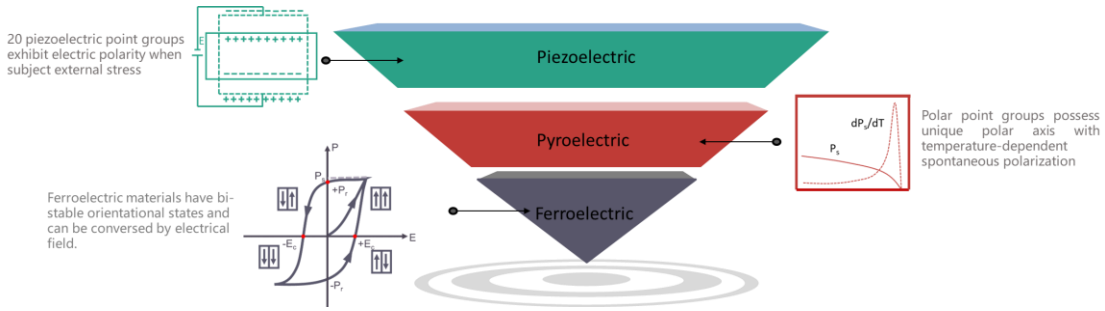


Figure 1-17: Relationships and specific features of piezoelectric, ferroelectric, pyroelectric, and dielectric materials.

The ionic displacements in ferroelectrics can extend over millimeters or self-organize

into complex mesoscopic structures and reorient in response to the applied stimuli.[82] To gain a comprehensive understanding of these behaviors, various characterization techniques are essential. A commonly employed method is the measurement of the polarization-electric field (P-E) loop, which directly characterizes the reversal of spontaneous electric polarization under an external electric field. The hysteresis loop is formed when the electric field is swept in opposite directions (Figure 1-18(a)). Ferroelectric polarization is closely related to domain orientation. Piezoresponse force microscopy (PFM) has been widely utilized to characterize ferroelectric properties, such as domain polarity, in thin films of ferroelectric materials (Figure 1-18(b)).[83] Moreover, unlike conventional dielectrics, ferroelectric materials exhibit a nonlinear relationship between applied voltage and stored charge (Figure 1-18(c)). The dielectric constant of ferroelectric materials is typically much higher than that of linear dielectrics due to the electric dipole effects in the crystal structure.[84]

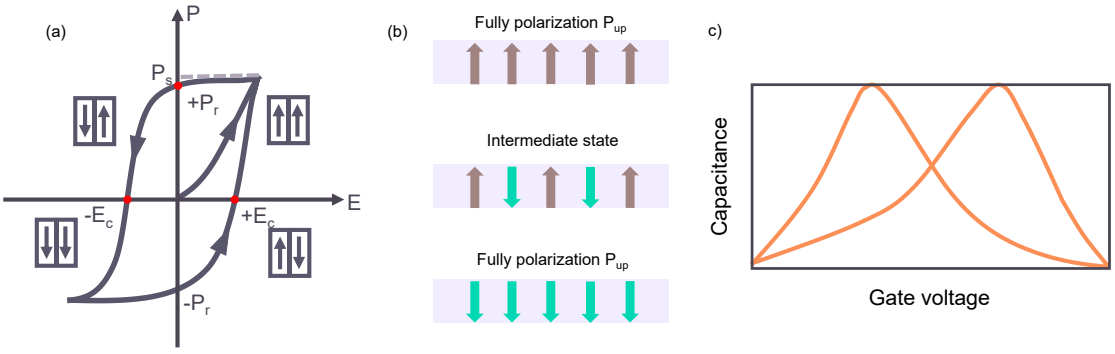
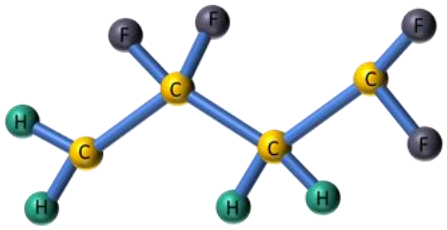
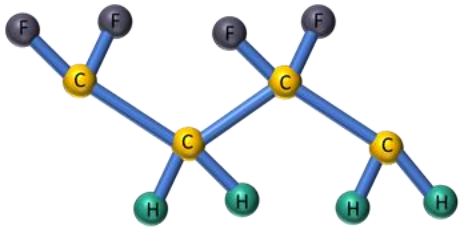
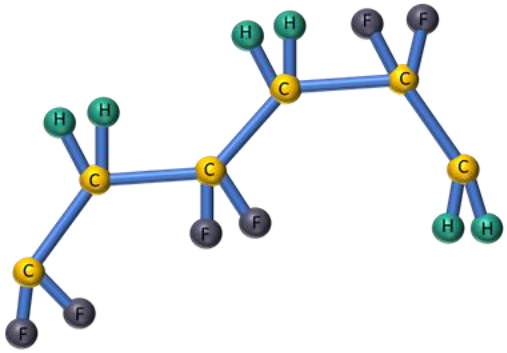


Figure 1-18: Properties of ferroelectric materials. (a) Typical P-E loop with ferroelectric domain conversion. (b) Three different ferroelectric polarization states. (c) Demonstration of capacitance–voltage curve of metal/P(VDF-TrFE)/metal capacitor.

Polyvinylidene difluoride (PVDF) is a prominent member among various ferroelectric polymers.[85] The ferroelectric properties of PVDF originate from the molecular dipoles created by positively charged hydrogen atoms and negatively charged fluoride atoms, with the repeated unit being CH_2-CF_2. The orientation of these dipoles is determined by the molecular conformation and packing. PVDF exhibits three distinct conformations: trans-gauche-trans-gauche (TGTG'), all-trans (TTTT), and intermediate trans-trans-trans-gauche (TTTG), as shown in Table 1.[86]

Table 1-1: Comparison of different PVDF phases

Phase	Package Way	Structure	Polarity
α	Trans-gauche conformation (TGTG).		Nonpolar
β	All-trans conformation (TTTT).		Polar
γ	Intermediate conformation (T3GT3G).		Nearly one half of the β-phase

These disparate molecular conformations lead to the formation of four crystalline structures. In the ferroelectric β-phase, the all-trans conformation arranges CH_2-CF_2 dipoles in a zigzag pattern perpendicular to the carbon chain axis. Although the α-phase

is the most stable polymer according to total energy, it is unsuitable for piezoelectric and ferroelectric applications due to the cancellation of dipole moments in its stereochemical conformation.[87] However, by applying external stimuli such as electrical, thermal, and mechanical deformation, the α-phase PVDF can undergo chain rotations and exhibit intriguing physical phenomena, suggesting that the potential energy barrier can be easily overcome. Moreover, different conformations of PVDF are associated with distinct physical signals, such as mid-IR absorption peaks, and their crystal structure remains unchanged under electrical polarization. Building upon these properties, He et al. achieved multilevel phase transformation in ultrathin PVDF films at the nanoscale using atomic force microscopy-based infrared spectroscopy. This technique enabled the realization of optical/ferroelectric multiplexing PVDF memory with high efficiency and storage density.[88] Additionally, nanocomposites comprising PVDF and carbon nanotubes have been successful in achieving a 100% crystalline β-phase, ensuring a large spontaneous polarization for ferroelectric activity.[89]

In order to achieve stable PVDF with a high ferroelectric polarization suitable for technical applications, the utilization of copolymer products like P(VDF-TrFE) proves to be advantageous. Through the copolymerization of vinylidene difluoride (VDF) with tetrafluoroethylene (TrFE) at varying proportions, a copolymer named (P(VDF-TrFE)) can be synthesized. The introduction of TrFE weakens the intermolecular forces within PVDF, resulting in the generation of an all-trans stereochemical conformation that aligns along the direction of the dipole moments.[90-91] Importantly, the conformational

phase is independent of the TrFE composition, ensuring that P(VDF-TrFE) consistently exists in the β-phase for the fabrication of ferroelectric films, thereby expanding its potential for broader applications. Furthermore, copolymer P(VDF-TrFE) (90%) exhibits higher crystallinity compared to PVDF (50%).[92] Consequently, significant efforts have been dedicated to fabricate oriented and crystalline P(VDF-TrFE).[93-94] In comparison to traditional manufacturing methods such as PLD and MBE, the solution fabrication process offers the convenience of not requiring high-temperature processing or complicated experimental equipment. Leveraging low-temperature spin-coating processes, polymer-based ferroelectrics like P(VDF-TrFE) can be readily fabricated onto the surfaces of 2D materials, establishing a favorable vdWs interface

To enhance the thermal stability of P(VDF-TrFE)-based ferroelectric memory devices, several methods have been employed. These include epitaxially growing P(VDF-TrFE) on a poly(tetrafluoroethylene) (PTFE) substrate,[95] adjusting the VDF/TrFE ratio,[96] and introducing a coupling effect between charged domain walls and charged defects.[97] In addition to the direct spin-coating method, the Langmuir-Blodgett technique has been utilized for the fabrication of P(VDF-TrFE) films. This technique involves depositing uniform molecular monolayers onto solid substrates, enabling low-voltage operation.[98] To achieve ordered structures and enhanced thermal stability in P(VDF-TrFE)-based ferroelectric random access memory (FeRAM), Guo et al. fabricated a self-assembled array of P(VDF-TrFE) lamellae with separated crystal and amorphous phases.[97] Compared to FeRAM devices obtained through spin-coating

with a thermal endurance of 70 °C, these self-assembled FeRAM devices exhibit improved thermal endurance of up to 90 °C. Overall, numerous studies have confirmed the exceptional performance of P(VDF-TrFE) copolymers as crucial components in ferroelectric devices due to their advantages, including significantly lower crystallization temperatures, higher content of the β-phase, ease of processability, and cost-effectiveness.

1.3.3 2D semiconductor/ferroelectric transistors for neuromorphic applications

By applying external programming pulses with appropriate amplitudes and widths, stable ferroelectric configurations can be established with upward and downward polarization states. Starting from 2012, nonvolatile resistance states with multiple levels and synaptic learning rules have been achieved by manipulating the ferroelectric domains in FeFETs and ferroelectric tunnel junctions (FTJs).[99] Although based on inorganic films such as PZT, ferroelectric synapse transistors displayed STDP and other pattern synaptic functions successfully.[100] Such electrical selectors possess complicated interconnectivity and reduced energy efficiency. (PVDF-TrFE) copolymer-based ferroelectric organic neuromorphic transistors will also demonstrate biocompatibility and flexibility properties.[101] Therefore, organic artificial synapses are one of the critical technologies for the realization of wearable intelligent electronics. In this regard, the 2D materials/copolymer ferroelectric transistors open an avenue for neuromorphic synaptic electronics.

For instance, by applying voltage pulses of suitable duration to the gate terminal, the

channel conductance exhibits synchronous evolution with an on/off ratio of 10^4, facilitated by gate polarization propagation (Figure 1-19(b)).[102] Moreover, by precisely timing the sequence of pre- and postsynaptic spikes, this device demonstrates synaptic plasticity through conductance changes, reflecting LTP, LTD, and STDP adaptation activities (Figure 1-19(c)). These behaviors align with the Hebbian learning rule.[103-104] Importantly, such a device exhibits desirable endurance properties and ultra-low power consumption. Furthermore, these synapses can be employed for the implementation of a remote supervised method in spiking neural networks. Figure 1-19(d) illustrates that by applying voltage pulses of opposite polarity to the gate, both potentiation and depression states can be achieved within the same device structure, realizing the concept of complementary synapses.[105] With the assistance of a remote supervision algorithm, two parallel-connected graphene-based FeFETs successfully executed a supervised learning process, resulting in a discrepancy of less than 1% between the desired time and the output time after 50 iterations (Figure 1-19(e-f)). However, compared to conventional semiconductors, the amplitudes and widths of the gate voltage pulses are several orders larger in order to achieve a high conductance ratio from zero bandgap graphene, leading to slower operation speeds and increased power consumption. To address this challenge, semiconducting 2D materials offer a solution due to their diverse band structures and tunable bandgaps. For instance, a WSe_2-based two-transistor synaptic cell can realize both STDP and reward-modulated STDP.[106] Under negative gate voltage, the Fermi level shifts towards the valence band for p-type

channels, resulting in increased conductance, while for n-type channels, the conductance decreases under the same voltage pulse (Figure 1-19(h)). In reward-modulated STDP, the weight update is stored in the eligibility trace prior to a pair of pre- and post-spikes. When the post-reward is received, the switch is activated, modulating the behavior into either STDP or anti-STDP (Figure 1-19(i)).

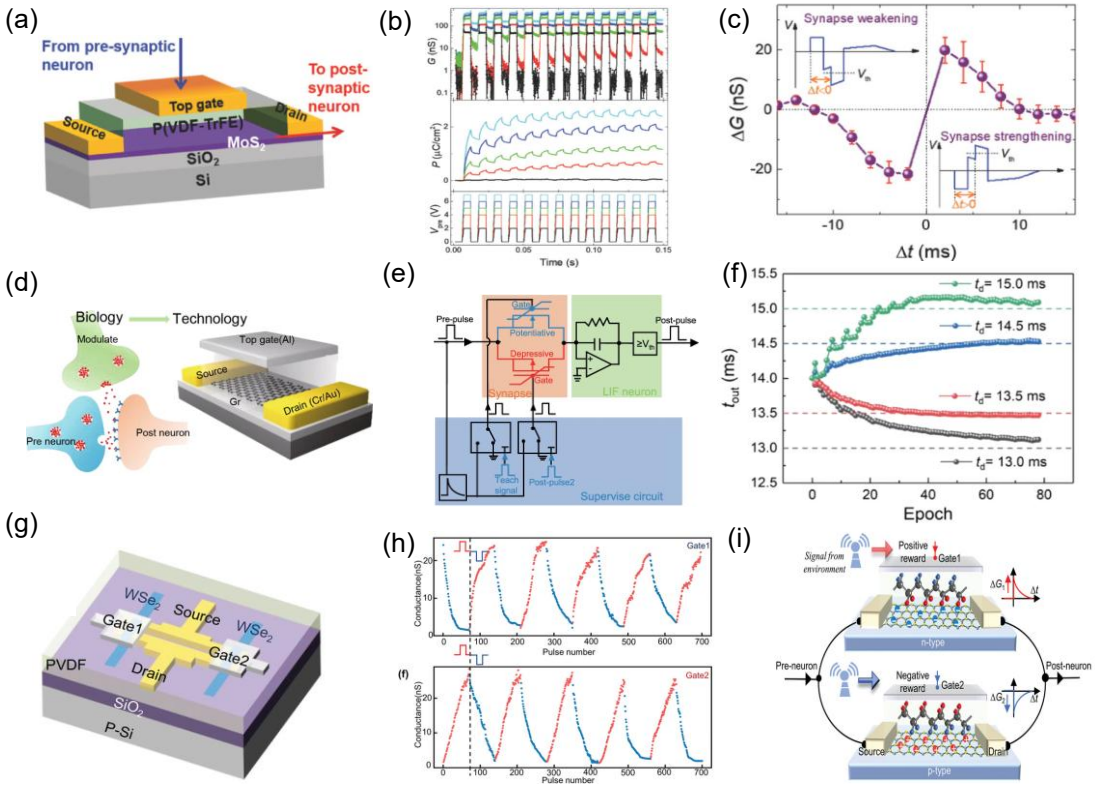


Figure 1-19: 2D semiconductor/ferroelectric transistors for neuromorphic applications. (a) Three-dimensional structure of the MoS_2/P(VDF-TrFE) synapse. (b) Synchronous change in channel conductance under voltage pulse sequences. (c) Modulation results of STDP. (d) Structure of the graphene/P(VDF-TrFE) synaptic transistor. (e) Schematic diagram of the remote supervised method module. (f) Convergence process for achieving the desired timing and output. (g) Schematic

representation of the complementary configuration of two parallel WSe_2/P(VDF-TrFE) transistors. (h) Weight update behaviors for the two transistors. (i) Hardware model for reward-modulated STDP.

1.4 Significance of this work

The significance of this research in the context of the thesis is as follows: Organic ferroelectric synapses demonstrate high performance and efficiency, making them promising candidates for unsupervised and supervised learning in artificial neural networks (ANNs). However, the use of 2D materials-based FeFETs in neuromorphic synaptic electronics is still in its early stages. Further endeavors are required to enhance synaptic functionalities by employing multi-functional semiconductor channel materials, innovative device structures, and comprehensive algorithms that accurately simulate neuron communication. Therefore, building upon the foundation of memory transistors utilizing low-dimensional materials and ferroelectrics, this study integrates the diverse physical and optoelectronic properties of memory transistors accompanied with the designed ANN framework for advanced applications such as static image recognition, image pre-processing, and dynamic perception (Figure 1-20).

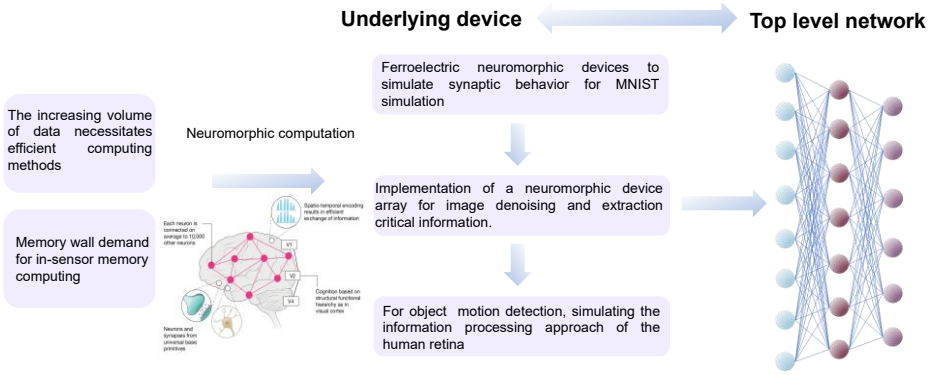


Figure 1-20: Research methodology of this thesis.

Firstly, extensive research efforts have focused on exploring polymer-based FeFETs integrated with 2D semiconductors through vdWs interface contacts for the development of neural networks. However, most of the existing studies have primarily involved low-mobility 2D nanosheets like ambipolar $MoTe_2$ or n-type MoS_2, which exhibit only small variations in conductance. As a result, these limitations hinder their application in energy-efficient and high-accuracy neuromorphic computing. Consequently, by combining p-type and high mobility BP with ferroelectric copolymer P(VDF-TrFE), we can demonstrate three-terminal ferroelectric synaptic transistors with good electronic and synaptic performance for handwritten digits recognition.

Secondly, one of the crucial functionalities of the retinal cell is the ability to discern colorful information while extracting relevant signals from the noisy environment. Also, by leveraging the color-recognition mechanism, extracting crucial light information can effectively reduce interference caused by redundant data and enhance the speed for further signal processing. However, it is still challenging to achieve such complicated sensing or learning purposes based on one simple optoelectronic synaptic device. Combination of 2D direct bandgap materials and ferroelectric materials as heterostructures holds potential for neuromorphic visual sensors. Therefore, we design a multi-functional optoelectronic ferroelectric synaptic transistor with the simultaneous synapse behaviors simulation, multi-color perception, and visual neuromorphic computing functionalities.

Thirdly, conventional motion detection architectures, which rely on image sensor platforms and entail the segregation of sensor, memory, and computational units, frequently give rise to substantial volumes of raw data and high power consumption.[107-109] The human retina possesses an inherent ability to efficiently perceive and process dynamic information. Therefore, we present a groundbreaking demonstration of a reconfigurable photodiode device utilizing tungsten di-selenide (WSe_2) and ferroelectric copolymer composed of P(VDF-TrFE) and successfully simulate the object motion sensitive function of ganglion cells in the retina. Through the multi-intermediate ferroelectric polarization states, a series of positive and negative self-power photocurrents can be used as synaptic weights updating states. Through the brightness difference between the static background and the moving individual, the mapped output results can solely convey the information form moving person while counteracting the bidirectional photo response through the interframe differential coding. Also, the critical information within the moving individual can be recognized via ANNs.

1.5 Structure of this work

The structure of this thesis is organized as follows:

Chapter 1: This chapter first provides a comprehensive overview about neuromorphic computation, 2D materials, ferroelectrics, and the research status about ferroelectric transistors. To enhance comprehension of this study, the subsequent

sections provide a detailed explanation of the significance of the research. Additionally, the thesis structure is outlined to facilitate ease of reading.

Chapter 2: This chapter provides a comprehensive overview of the commonly employed equipment. It also covers the device fabrication platform, including photolithography for nanodevices, as well as electrical measurement techniques. Furthermore, detailed simulation methods for neuromorphic computations are discussed in depth.

Chapter 3: We propose a design approach for ferroelectric-tuned synaptic transistors by integrating BP with the flexible ferroelectric copolymer P(VDF-TrFE). This integration enables the transistors to exhibit high carrier mobility, an excellent on/off ratio and low power consumption for each event, thereby facilitating accurate synaptic behavior simulation. Notably, we demonstrate the effectiveness of this approach by simulating an ANN for handwritten digit recognition, achieving a recognition accuracy of 93.6%.

Chapter 4: We propose a novel design for a multifunctional optoelectronic ferroelectric synaptic transistor to simulate the functionality of the retina, enabling light-intensity sensing, color discrimination, noise reduction and information extraction. By leveraging the light-induced conductance difference, the contrast of the target object is enhanced while minimizing the influence of surrounding noise signals by image pre-processing. Through training the optoelectronic device array, we successfully achieve image recognition with an impressive accuracy of 96%.

Chapter 5: By integrating both positive and negative photocurrents, we effectively emulate the OMD function of ganglion cells in the retina with our reconfigurable retinomorphic devices. Such single device successfully integrates in-sensor computing of optical stimuli sensing, multi-state weights memorization, and motion detection computation. Subsequently, the captured motion scene information is accurately recognized through an ANN, resulting in an impressive recognition accuracy of 96.8%. Additionally, we have successfully fabricated a uniform 3×3 motion sensor array, which exhibits excellent uniformity and scalability.

Chapter 6： The comprehensive exploration of integrating 2D semiconductors with ferroelectrics has generated considerable interest across multiple fields. This chapter addresses several key issues and existing challenges, aiming to foster the development of innovative device designs that enable low power consumption, reduced circuit complexity, and novel functionalities.

Chapter 2 Experimental Methods

2.1 Fabrication of 2D materials

In this thesis, we mainly use the mechanical exfoliation method to obtain high quality and single crystalline 2D materials. By exploiting the weak interlayer vdWs forces inherent in bulk 2D materials, we initiate the process by delicately peeling off the bulk material using adhesive tape, yielding a thinned, smooth, and flat sheet. Subsequently, the thinned sheet is meticulously affixed to the adhesive tape and subjected to repetitive folding, enabling further reduction in thickness and yielding an increasingly thinner 2D material on the tape. The tape, carrying the attached material, is then uniformly pressed onto a silicon wafer and allowed to rest for a specified duration. Subsequently, the tape and the silicon wafer are separated, leaving behind a few-layered 2D material on the silicon surface. Utilizing the mechanical exfoliation technique, we are able to obtain 2D materials with a few layers or even in monolayer. However, if the material is susceptible to reacting with water and oxygen present in the ambient air, it becomes essential to carry out the entire process within a specifically designed glove box.

2.2 Materials transfer method

Polydimethylsiloxane (PDMS) and polyvinyl butyral (PVB) are the primary polymers utilized in the dry transfer of thin films. PDMS is specifically suitable for transferring bilayer heterostructures, while PVB is well-suited for transferring metal electrodes. In this section, we will outline the dry transfer method employing PDMS and metal electrodes transfer through PVB.

To initiate the process, we first obtain the desired 2D material on a PDMS substrate through the previously described mechanical exfoliation technique. It is crucial to search for the sample under a microscope due to the distinct contrast between the sample on PDMS and a silicon wafer. And the layer count can be determined based on the transparency, with most single-layer materials easily identifiable on PDMS. Once the target sample is located on PDMS, a PDMS-coated glass slide is carefully positioned on the XYZ transfer platform, while the silicon wafer containing prepatterned electrodes for transfer is placed beneath the glass slide. After determining the desired transfer angle, the spacing between the sample on PDMS and the sample on the silicon wafer is adjusted until the two materials make contact. It is essential to proceed with the bonding process slowly to prevent the formation of bubbles. Upon achieving full contact between the two samples, the entire platform is heated to 60℃, and the PDMS is gradually lifted. This gradual lifting is crucial to prevent the detachment of the sample on PDMS from the silicon wafer. As the PDMS is gradually lifted, the interfacial forces between the heterostructures, which are stronger compared to the forces between the materials and PDMS, facilitate the separation of the material from PDMS, leaving the materials firmly adhered to the silicon wafer.

In this section, we will provide a further detailed explanation of the transfer process for metal electrodes. Initially, gold (Au) electrodes are fabricated on a pure silicon substrate. To facilitate the transfer, a PDMS film is carefully placed on a glass slide, which is pre-attached with a PVB film. Following the previously described procedure,

the electrodes on the silicon substrate can be lifted and transferred onto the surface of the PVB film. Subsequently, the silicon substrate is substituted with the desired sample, where the previously transferred electrodes are to be deposited. By utilizing the XYZ positioning capability of the transfer platform, the electrodes are accurately aligned directly above the designated location on the sample. Gradually, the glass slide, along with the PDMS/PVB assembly, is lowered until the two components make intimate contact. Afterward, controlled heating is applied to the system. As the temperature increases, the viscosity of PDMS disappears, enabling the gradual separation of PDMS from the PVB film. This step is executed by cautiously lifting the glass slide, ensuring a gradual and controlled detachment of the PDMS layer from the PVB film. Consequently, the PDMS layer separates from the PVB film, leaving the electrodes firmly attached to the sample surface. In the final step, the entire sample is immersed in ethyl alcohol, which effectively dissolves the PVB film. This immersion process ensures the removal of the PVB, thereby leaving only the transferred electrodes affixed to the sample surface.

2.3 Nanofabrication system

Based on the aforementioned material preparation and device heterostructure integration, it is necessary to explain the lithography process to form electrodes. In this study, the device fabrication process involves sequential steps of electrode pattern preparation, electrode deposition, and electrode delamination. The main equipment

employed for these processes includes a UV lithography machine and electron beam evaporation coating system.

The UV lithography machine is characterized by the following key parameters: light source: 350W UV light; resolution: <0.8μm max; alignment: top side alignment; alignment accuracy: <± 0.5μm; substrate: Up to 4 round wafer. The equipment details about electron beam evaporation are shown as following: substrate size: Up to 4-inch wafer; substrate rotation: 0 – 20 rpm; vacuum: achieve to 10^{-7} Torr; thickness control: inficon deposition controller; heater: Quartz lamp heater, max. 200°C; source: 4 pocket with 7cc capacity; controller: 4-channel sweep controller.

The preparation of electrode patterns is achieved through UV lithography. The UV lithography process involves the utilization of two types of photoresists: positive-tone and negative-tone. In general, positive-tone photoresists offer higher resolution capabilities, but they have lower sensitivity, and different lithography processes should be employed based on their respective types. In this study, we select AZ5214 and process parameters used in this paper are shown as follows:

1) Spin-coating photoresist: 500 rad/min, 10 s followed by 3000 rad/min, 30 s;

2) Pre-heating: 110 ℃, 3 min;

3) Exposure: 8 s

4) Developing: 25 s in AZ 300 MIF developing liquid;

5) Rinse: 20 s in deionized water

Following the aforementioned lithography processes, metal electrodes, specifically Cr/Au or Ti/Au, are meticulously deposited onto the sample surface using electron beam evaporation. The electrode fabrication is then finalized through a wet delamination process by acetone. To enhance the adhesion between the Au layer (usually 50 nm) and the material, a thickness of 10 nm metal is chosen for the Cr or Ti layer.

2.4 Electrical measurement equipment

The majority of electrical measurements in this study are performed utilizing a Keithley Semiconductor Parameter Analyzer along with an external vacuum probe station. During the I-V testing procedure, the device is connected to the 4200 unit via a source measurement unit (SMU). The SMU facilitated the application of current or voltage to the device while precisely measuring the voltage across the device and the current passing through it. Figure 2-1 illustrates the connection configuration for testing three-terminal devices using 4200 units. For two-terminal devices, the connection is established using two SMUs. In the case of three-terminal devices, one terminal is grounded in addition to the SMUs. Besides the SMUs, the 4200 unit also support ultra-fast pulse testing, which necessitates the utilization of a pulse measurement unit (PMU). The PMU provided ultra-fast voltage pulses while simultaneously measuring the pulse signals.

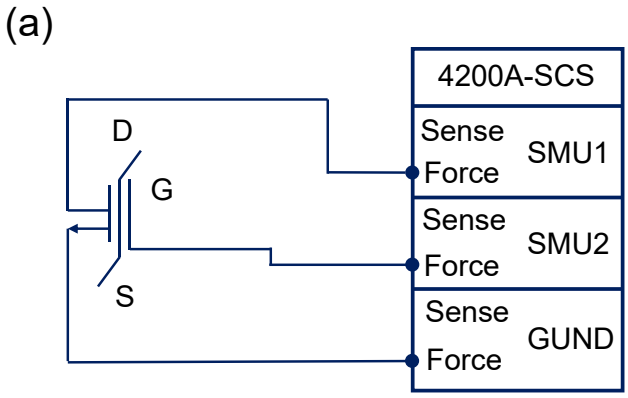


Figure 2-1 Connection configuration for testing three-terminal devices.

The preparation of materials and devices, as well as the testing instruments used, are presented in Table 2.

Table 2-1: Equipment information

Name of the instrument	Manufacturers	Model
Ultraviolet lithography machine	SUSS Micro Tec	SUSS MA6 Mask Aligner
Electron beam evaporation	DENTON VACUUM	Denton E-beam Deposition System
Transfer system	Metatest	E1-T
Probe station	Lake Shore Cryotronics, Inc	LAKESHORE_Cryogenic
Semiconductor Parameter Analyzer	Tektronix	Keithley 4200A-SCS Parameter Analyzer

2.5 Simulation method

For image recognition purpose, a three-layer ANN is constructed, consisting of an input layer, a hidden layer, and an output layer. The backpropagation algorithm is employed to update the weights, and the sigmoid function is utilized as the activation function. The updated weights are then mapped to the conductance state of the device using the CrossSim platform. The code is implemented in Python and executed within the Spyder integrated development environment (IDE). To simulate background noise signals, the Gaussian noise signals have a mean of 2.5E-9 and a variance of 1E-9 generated from C++ software program.

Moreover, six steps are employed to perform motion detection by utilizing inter-frame differential computation and image recognition of moving objects based on the motion detection results. (1) Neuromorphic vision sensor is developed to experimentally capture positive and negative response parameters using non-volatile photocurrents; (2) Multiple frames consisting of M×N pixels are acquired from a motion process, treating it as a continuous stream of images; (3) M×N positive (W^+) and negative (W^-) weight matrices are constructed based on the response parameters obtained in Step 1. These weight matrices are then applied to multiply the pixel values of different frames. For instance, the M×N pixels of frame $t_0(P_{t0})$ and $t_1(P_{t1})$ are multiplied by the positive and negative weight matrices W^+P_{t0} at t_0 and W^-P_{t1} at t_1, respectively; (4) The results obtained in Step 3 are summed to obtain the transformed pixel outcome, such as $W^+P_{t0} + W^-P_{t1}$. A step function is subsequently utilized to

enhance the differentiation of the accumulated data. (5) The processed data is transformed into a new image stream utilizing OpenCV, a widely-used open-source computer vision library renowned for its capabilities in image and video processing tasks; (6) Finally, an ANN is employed in conjunction with a corresponding training database to recognize the moving objects detected in Step 5. For instance, in this section, number recognition is performed by employing the PyTorch platform based on the MNIST database. Detailed flow chart of the above operation is illustrated in Supplementary Fig. S14. Figure 2-2.

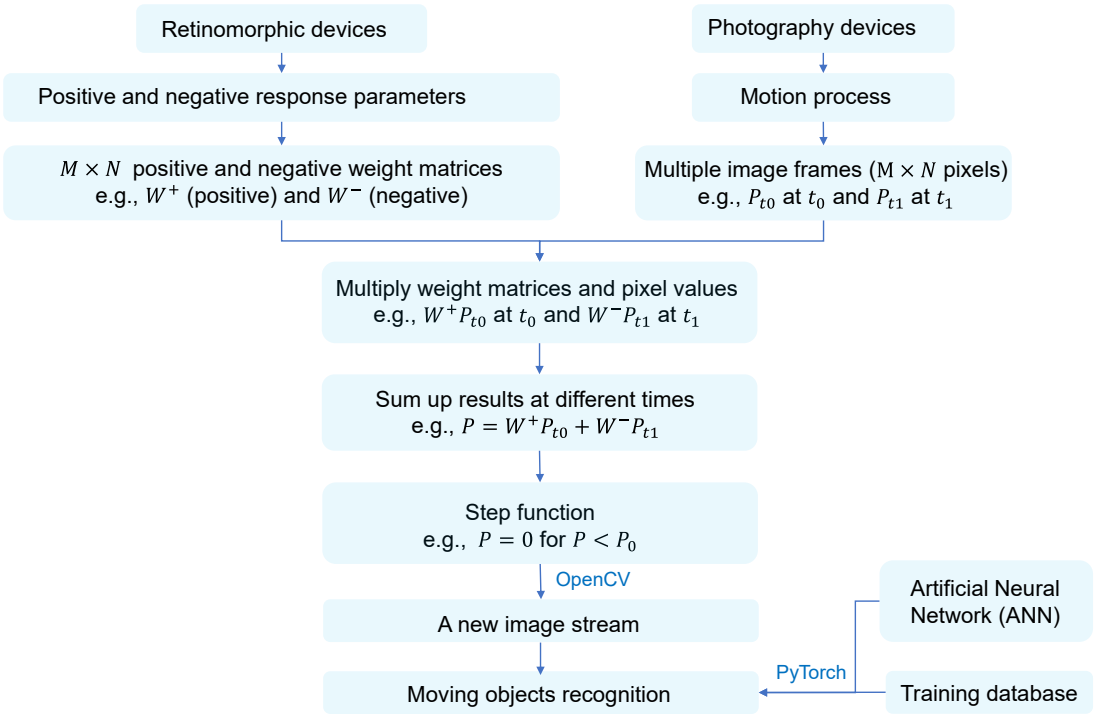


Figure 2-2: Flowchart depicting the processes of inter-frame differential computation and recognition for moving objects.

Chapter 3 P(VDF-TrFE)/BP artificial synapse for energy-efficient neuromorphic computing

3.1 Introduction

Biological synapses serve as fundamental connections among billions of neurons, enabling the simultaneous storage and processing of information through the modulation of synaptic plasticity.[110-112] These remarkable functionalities have inspired researchers to challenge the traditional von Neumann architecture and blur the distinction between memory and logic units, leading to the concept of in-memory computing.[113-114] The development of neuromorphic system aims to replicate the ability of brain to perform computing and memory tasks in parallel.[54, 115] The neuromorphic system becomes an attractive platform for next-generation computing with low power and fast speed to emulate knowledge-based learning. Among the various devices proposed for this purpose,[116-118] 2D FeFETs have gained widespread attention due to the unique capabilities offered by ferroelectric gating, including high doping density, reversible and nonvolatile modulation of channel carriers, and fast memory operations.[119-120]

In comparison to synapse transistors based on ferroelectric oxides,[121] organic ferroelectrics, specifically copolymer P(VDF-TrFE), present significant advantages such as low crystallization temperature, accessible fabrication methods, and high flexibility.[122-123] Consequently, extensive research efforts have been devoted to exploring polymer-based FeFETs integrated onto 2D semiconductors with the ultimate

goal of advancing neural network development.[124-125] However, previous studies in this field have predominantly focused on utilizing 2D nanosheets characterized by low mobility, such as ambipolar $MoTe_2$ or n-type MoS_2, resulting in limited variations in conductance. These limitations hinder the potential applications of such systems in energy-efficient and high-precision neuromorphic computing.

In this section, we demonstrate the realization of three-terminal ferroelectric synaptic transistors by combining p-type and high-mobility BP with ferroelectric copolymer P(VDF-TrFE). The developed FeFETs exhibit exceptional characteristics, including a high mobility of 900 $cm^2 V^{-1} s^{-1}$, a large on/off ratio of 10^3, and femtojoule-level energy consumption for each pulse event, which represent a state-of-the-art achievement in artificial synapses. We also investigate various synaptic behaviors, such as LTP, LTD, PPF, and the memory consolidation process under ferroelectric gate modulation. Notably, we simulate a hardware neural network for pattern recognition tasks, achieving an accuracy of 93.6%. With their high carrier mobility and significant conductance variations, the presented ferroelectric synaptic transistors hold great promise for energy-efficient applications in in-memory computation.

3.2 Device fabrication and materials characterization results

3.2.1 Device fabrication process

First, Ti/Au (10 nm/40 nm) metal electrodes are prepared on p-Si/SiO_2 (285 nm) substrates with standard lithography technique and electron beam deposition. 2D BP flakes are mechanically exfoliated onto the PDMS supports with blue tape. The BP

flakes are identified on the PDMS by the optical microscope, and then interested ones are selected for further dry transfer process. The P(VDF-TrFE) (70:30 in mol %) thin films (~300 nm thickness) as dielectric layers are made by the spin-coating process in the glove box. The detailed parameters for the spin-coating are 400rpm for 10 s and 3000 rpm for 40 s. The P(VDF-TrFE)/BP structures are finally annealed at 135 °C in a vacuum for 2 h. Finally, Al as top metal electrodes was deposited with the hard mask. We select Al as top gate electrodes based on several reasons: 1) Because Al metal is conductive for P(VDF-TrFE), keeping a steady state before reversing polarization orientation, and it can compensate for the polarization charges.[126] 2) Top electrodes Al can chemically react with fluoropolymers, including P(VDF-TrFE), and the diffusion process will be prevented during metal deposition.[127] 3) Compared with other metals, Al is relatively low-cost, making it suitable for large-scale production of P(VDF-TrFE) based capacitors. The process flow chart is shwon in Figure 3-1.

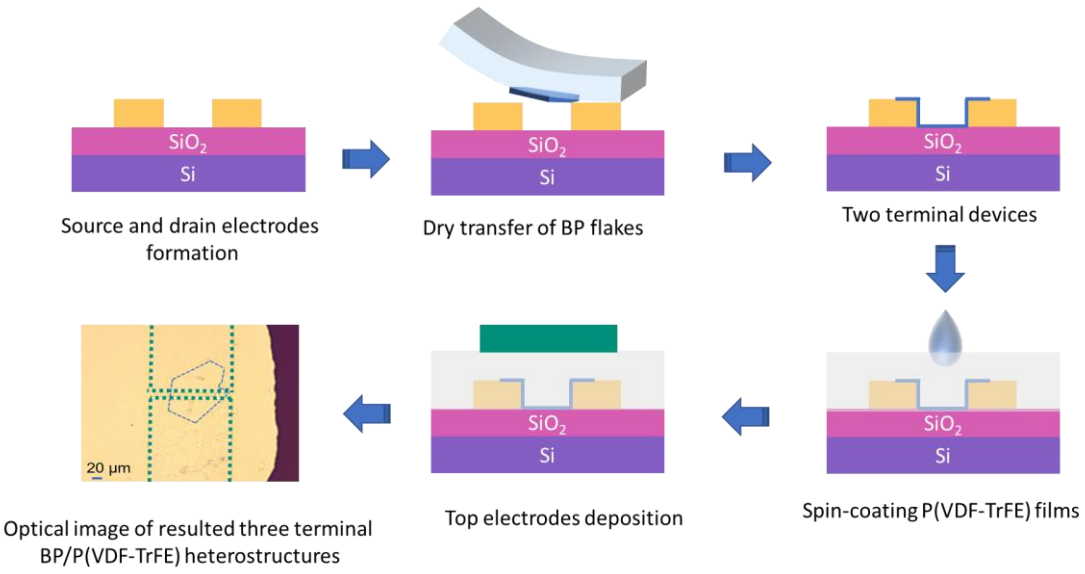


Figure 3-1: The whole fabrication processes of three-terminal P(VDF-TrFE)/BP

transistors.

Figure 3-2(a) displays the three-terminal architecture of FeFETs based on P(VDF-TrFE)/BP devices and the third terminal imposes signals. Ferroelectric layer P(VDF-TrFE) is a copolymer combining two homopolymers (Figure 3-2(b)). The ferroelectric polarization in P(VDF-TrFE) films origins from the opposite direction of dipole moments. Solution-based spin-coating fabrication method for P(VDF-TrFE) films followed by a low-temperature annealing process contributes to increasing crystallinity and developing clean interface.[128] Biological synapses operations are based on the ferroelectric effect of P(VDF-TrFE) and the tunable polarity of the BP channels.

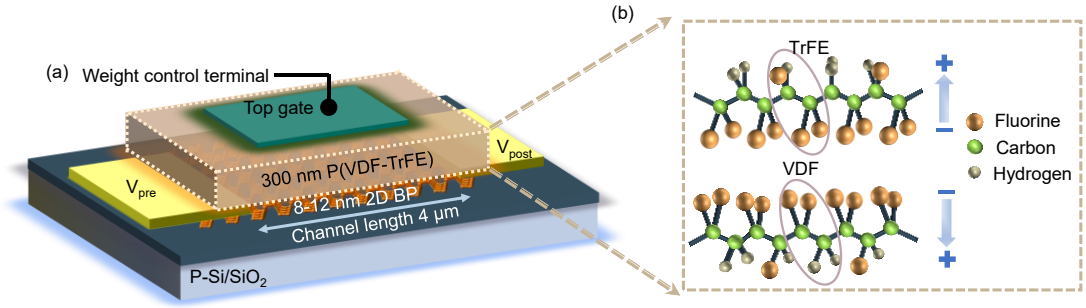


Figure 3-2: Structure of three-terminal P(VDF-TrFE)/BP. (a) Schematic configuration of top-gate 2D FeFETs with P(VDF-TrFE) gate dielectric and BP channel. (b) The right panel displays the chemical structure of P(VDF-TrFE) copolymer under opposite directions of dipole moments.

3.2.2 Materials characterization results

The Raman spectroscopy confirms the structural quality of the transferred few-layered BP. Figure 3-3(a) shows three typical characteristic peaks of A_{1g}, B_{2g}, and A_{2g}.[129] Atomic force microscopy (AFM) reveals a step-shaped texture (Figure 3-3(b)).

The thicknesses of BP used in FeFETs are approximately 8 nm (~13 layers) and 12 nm (~20 layers).

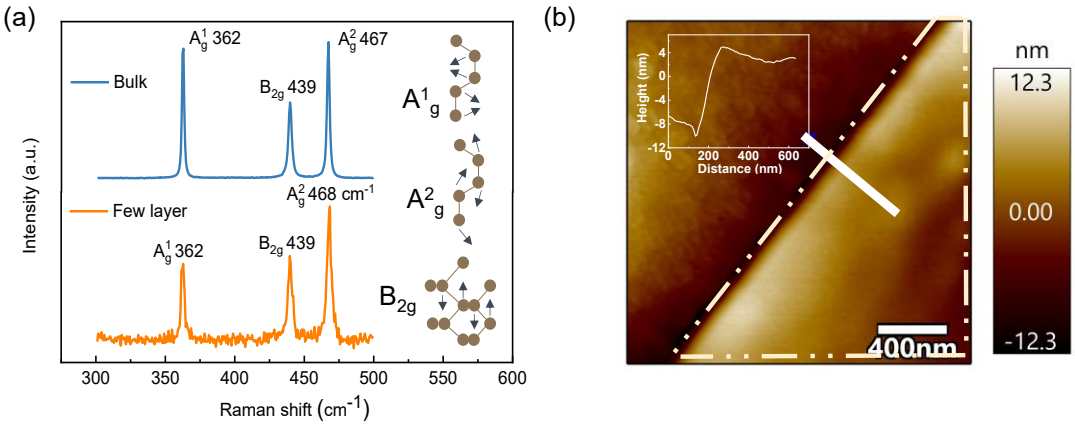


Figure 3-3: Characterization of BP. (a) Raman spectra of the bulk and few layered BP. (b) Surface topographic images of BP. Inset: AFM step-height profiles.

X-ray diffraction (XRD) spectra with the prominent peak at 19.7° confirm the formation of β-phase with (200) plane in P(VDF-TrFE) films (Figure 3-4(a)).[130] The spin-coating P(VDF-TrFE) films contain a high content of crystalline structure after low-temperature annealing. Furthermore, we note that the XRD peak intensity increases with the weight ratio of the solution, indicating that P(VDF-TrFE) films obtained from larger weight ratio solution possess a higher crystallinity. Taking the surface roughness and crystallization into account for synaptic device integration (Figure 3-4(b-c)), we fabricate P(VDF-TrFE) films with 6 wt% solution concentration and the thickness of the films is about 300 nm. Figure 3-4(d) presents the ferroelectric hysteresis loop of Al/P(VDF-TrFE)/Au capacitors, implying that the remnant polarization is about 4 $\mu C/cm^2$ and corresponding coercive voltage is $\approx$ 10 V.

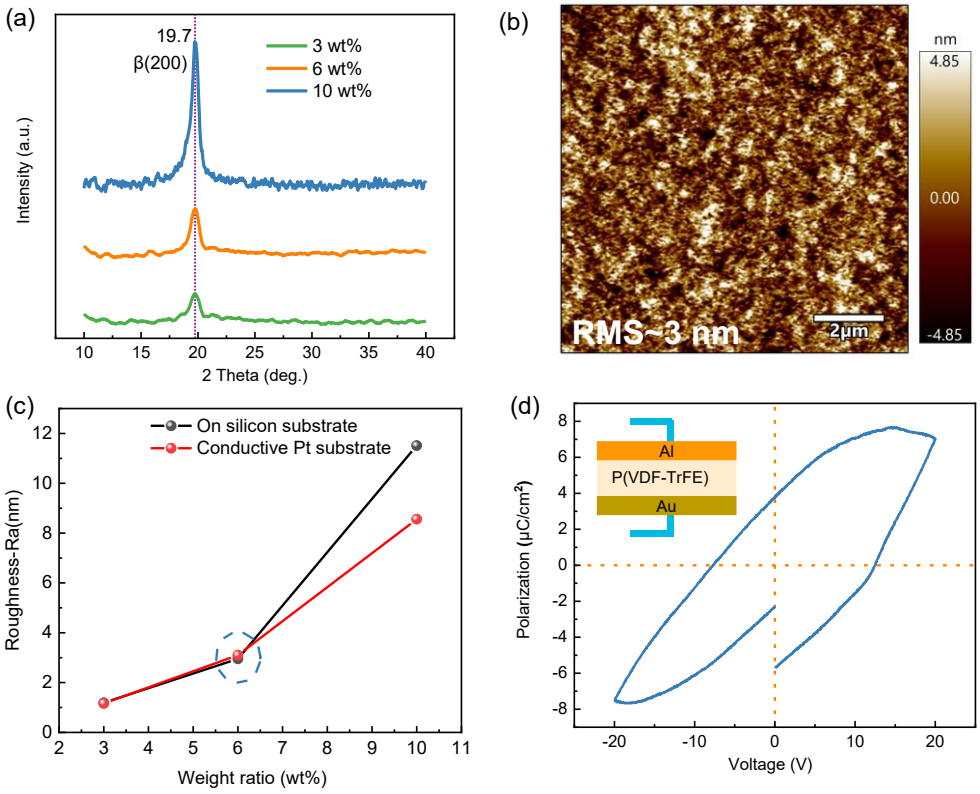


Figure 3-4: Characterization of P(VDF-TrFE). (a) XRD analysis results of P(VDF-TrFE) copolymer films fabricated under different solution concentration of 3 wt% ratio, 6 wt% ratio, and 10 wt% ratio. (b) AFM image of P(VDF-TrFE) film. (c) Surface roughness of different weight ratios P(VDF-TrFE) films on silicon (black curve) and on conductive Pt substrates (red curve). (d) Polarization-electric field hysteresis loop of the Al/P(VDF-TrFE)/Au capacitors at the test frequency of 10 kHz.

The ferroelectric amplitude and phase, as well as the switching process of ferroelectric domain reversal, are characterized using piezoresponse force microscopy (PFM).[131] Measurement setup of PFM is displayed in Figure 3-5(a). The experimental setup for PFM measurements is depicted in Figure 3-5(a). Figure 3-5(b) illustrates the contrast change observed in the parallelogram-like piezoelectric response of the Phase

1 channel, indicating the forced polarization of P(VDF-TrFE) films in the upward or downward direction under the applied writing voltage. Additionally, the amplitude loops exhibit a butterfly-like shape, further confirming the polarity of the P(VDF-TrFE) films. The Phase 2 channel exhibits a phase hysteresis loop, as shown in Figure 3-5(c). By applying a series of voltage pulses with opposite polarities, clear contrast is observed between downward and upward polarized domains in the P(VDF-TrFE) films after biased-tip scanning, as depicted in Figure 3-5(d).[132]

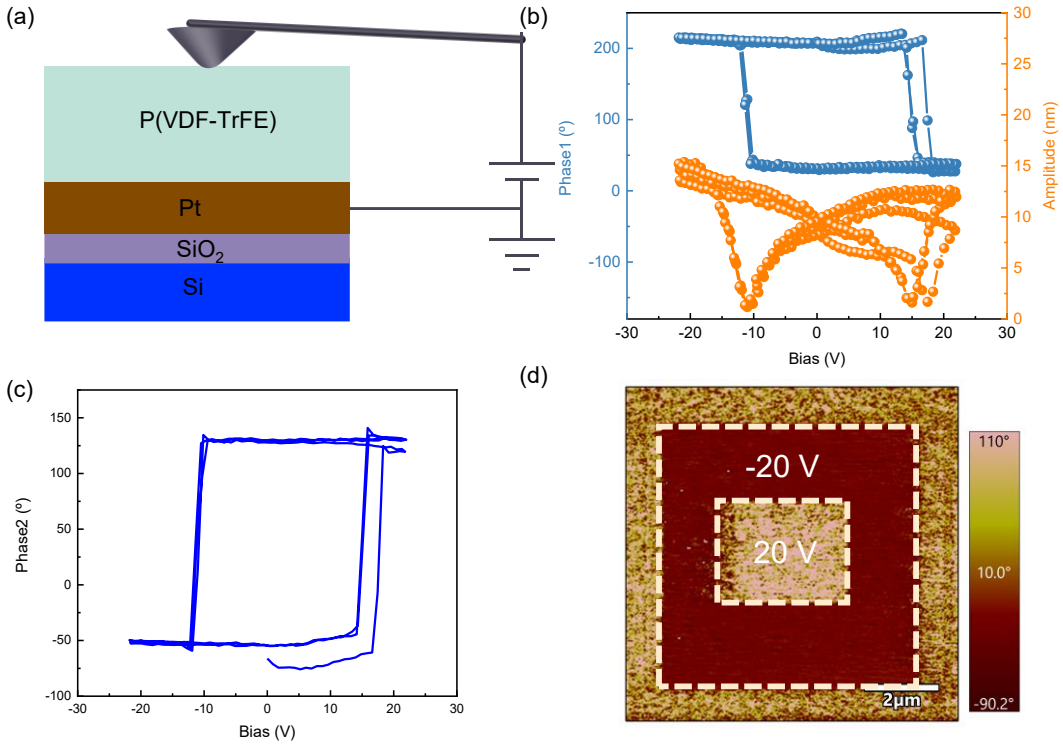


Figure 3-5: Ferroelectric characterization of P(VDF-TrFE). (a) Schematic of the PFM measurements setup. (b) The amplitude and phase hysteresis loops of P(VDF-TrFE) films. (c) The phase hysteresis loops from Phase 2 channel. (d) PFM images of

P(VDF-TrFE)/Pt (Pt bottom electrode). The "box-in-box" ferroelectric domain pattern is written with +20 V and -20 V tip bias.

3.3 Device working mechanism and the electrical measurements results

3.3.1 Device working mechanism

Here, we first clarify the working mechanism of ferroelectric effect on the active channel. Figure 3-6(a) illustrates the mechanism of controlling BP channel based on ferroelectric polarization. If the P(VDF-TrFE) layer is polarized upward under negative top gate voltage, the majority carriers (holes) in the p-type BP channel are fully accumulated (Figure 3-6(b)), and the barrier narrows to δ_1 (Top panel of Figure 3-6(c)). Meanwhile, holes in the BP channel will readily cross from the source to the drain, resulting in high drain current. On the contrary, carriers in the BP channel are exhausted if the P(VDF-TrFE) is polarized downward under positive gate voltage. The barrier height is enlarged to δ_2, hindering the carriers from crossing the barrier (Bottom panel of Figure 3-6(c)). Therefore, drain current becomes much smaller, corresponding to the high resistance state.

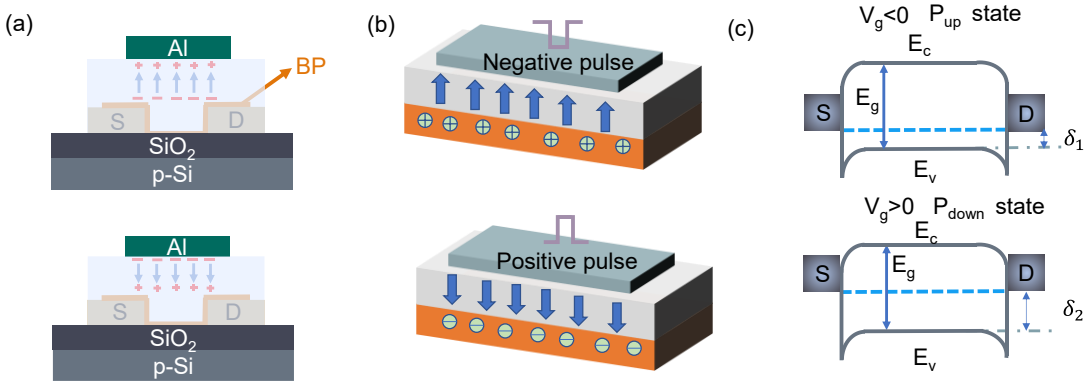


Figure 3-6 Device working mechanism of P(VDF-TrFE)/BP. (a) The cross-section structures of the device with dynamically modulating BP channel based on ferroelectric domain control. (b) P(VDF-TrFE) films are polarized to up and down under negative and positive voltage pulses, respectively based on the P(VDF-TrFE)/BP device structure. (c) Lateral energy band diagrams after experiencing the positive (bottom) and negative (top) voltage pulses. The E_c, E_V and E_g represent the minimum conduction band energy, maximum valence band energy, and bandgap of BP respectively. δ is the height from the bottom of the valence band to the Fermi level. δ_1 and δ_2 are related to the different polarization states.

3.3.2 Electrical measurements results

Prior to synaptic functions investigation, we characterize the transport properties of FeFETs. Figure 3-7(a) shows the cross-sectional view of three-terminal FeFETs with electrical probe settings for measurements. The output characteristics are exhibited in Figure 3-7(b), where the drain current increases considerably when the gate voltage changes from positive to negative. Linear output characteristics indicate that good ohmic contacts are formed at the contact region between electrodes and BP. Figure 3-7(c) illustrates the dual-sweep output curves and presents negligible hysteresis.

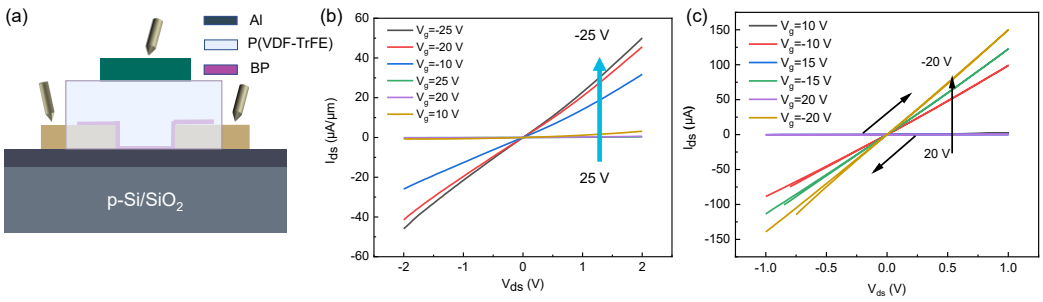


Figure 3-7 Output electrical properties of P(VDF-TrFE)/BP FeFETs. (a) Cross-section view of the P(VDF-TrFE)/BP FeFETs with probe position. (b) The output characteristics of the P(VDF-TrFE)/BP FeFETs, where top gate voltage varies from -25 V to 25 V. (c) Linear output curves under various top gate. The bias voltage sweep is fixed from -1 to 1 V with a dual-sweep setting. The negligible hysteresis result could exclude charge trap states within the interface of BP and P(VDF-TrFE) films.[133]

Figure 3-8(a) shows the collective results of the drain current when the gate voltage is swept from ±10 V to ±30 V in 5 V steps. The transport characteristics can be sorted into two parts: BP channel is turned on as the gate voltage sweeps from zero to the negative direction when P(VDF-TrFE) copolymer is polarized up. If the voltage is swept back to the positive direction, BP channel is fully depleted and P(VDF-TrFE) copolymer is polarized down. Therefore, the overall transfer curves show clockwise hysteresis direction and typical p-type transport behavior, and ferroelectric polarization reversal plays a dominant role in regulating electrical transportation behaviors. The ferroelectric hysteresis in transfer curves at forward and reverse bias voltages are both related to the ferroelectric polarization switching process. Therefore, Figure 3-8(a) and Figure 3-8(b) exhibit similar memory hysteresis loops. As the gate voltage is more than 10 V, memory windows are clearly observed because the larger gate voltage will result in a stronger polarization electric field in P(VDF-TrFE) films.[134] The minimum drain

voltage for transfer curves can be set as 1 mV (Figure 3-8(c)), which is meaningful for low-power nonvolatile memory operation and will be discussed later.

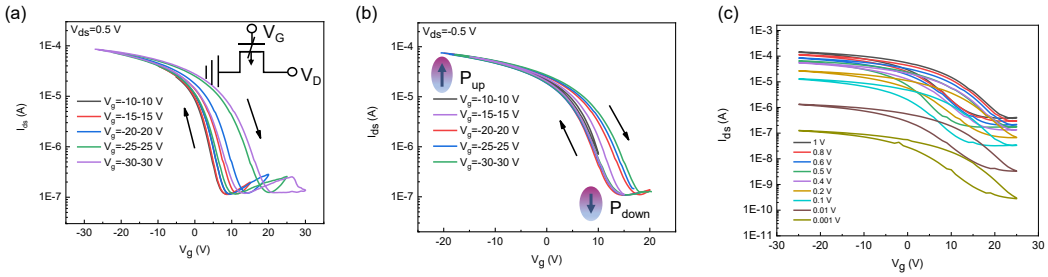


Figure 3-8: Transfer electrical properties of P(VDF-TrFE)/BP FeFETs. (a) Drain current vs. top gate memory hysteresis loops of typical P(VDF-TrFE)/BP FeFETs under positive bias voltage of 0.5 V (a) and a negative bias voltage of -0.5 V (b) where top gate voltage varies with a step of 5 V. Inset: circuit diagram of P(VDF-TrFE)/BP transistors. The clockwise hysteresis windows expand with increasing top gate voltage, showing cumulative polarization. (c) Drain current vs. top gate memory hysteresis loops and displacement characteristics of P(VDF-TrFE)/BP FeFETs under various positive bias voltage.

It should be pointed out that BP-based FeFETs display high linear mobility value of 500 $cm^2 V^{-1} s^{-1}$ for 12 nm BP and 900 $cm^2 V^{-1} s^{-1}$ for 8 nm BP at room temperature (Figure 3-9(a)) and carrier mobility values exhibit negligible differences for various gate voltage ranges (Figure 3-9(b-c)). Overall, the demonstrated P(VDF-TrFE)/BP transistors have shown advantages in terms of reducing structure complexity, high carrier mobility, satisfactory memory properties, and stable electrical performance.

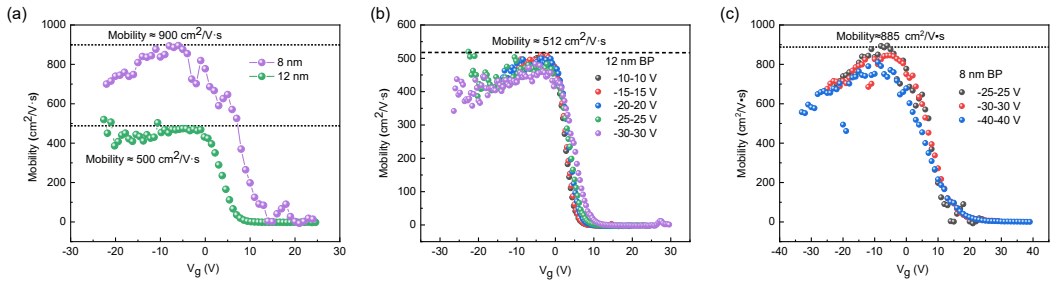


Figure 3-9: Mobility measurement of P(VDF-TrFE)/BP FeFETs. (a) Linear mobility plots of top gate P(VDF-TrFE)/BP FeFETs under room temperature. Sheet carrier mobility of two thicknesses BP samples: 12 nm (b) and 8 nm (c). The peak field-effect mobility values are 512 and 885 $cm^2/(V▪s)$ for 12 nm and 8 nm, respectively.

3.4 Synaptic behavior simulation based on P(VDF-TrFE)/BP

In light of the fact that P(VDF-TrFE) copolymer films exhibit a consecutive and discernible modulation of BP electrical conductivity, which serves as the fundamental basis for diverse synaptic plasticity, a comprehensive analysis of the synaptic performance of P(VDF-TrFE)/BP transistors will be presented in the following sections.

A biological synapse transmits various electrical or chemical signal from the presynaptic terminal to the postsynaptic terminal by tuning neurotransmitter content (Figure 3-10(a)).[135] In a three-terminal ferroelectric device, the gate terminal acts as the presynaptic function for signal transmission, whereas the channel layer is the postsynaptic terminal, and stimuli from the gate terminal can modulate its behaviors. Therefore, the signal transmission and learning process can be carried out simultaneously.

As shown in Figure 3-10(b), if one synaptic device is triggered by two electrical pulses, the PSC induced by the second pulse is much higher (A2>A1) owing to the ferroelectric nonvolatility. Under the minimum time interval, the intensity difference between two PSC signals reaches the maximum and decreases gradually when time interval increases (Figure 3-10(c)). PPF index is defined as the ratio of the amplitude difference of the PSC induced by the two consecutive electrical pulses (A2−A1) to the PSC of the first spike (A1), and it decreases to zero.[31, 136] The whole process emulates the phenomenon of neurotransmitter release enhancement in synapses.

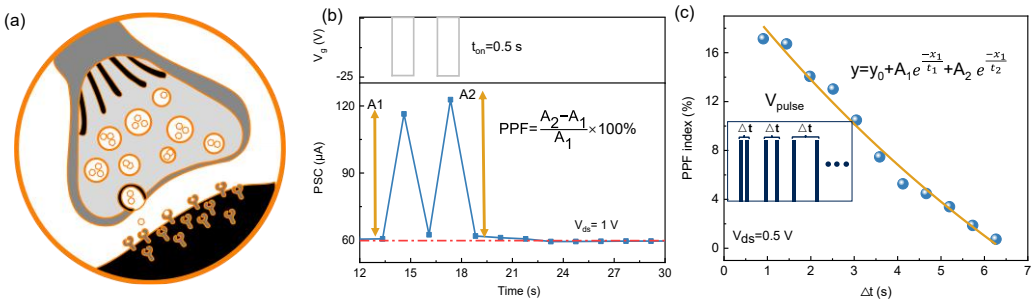


Figure 3-10: PPF behaviors of P(VDF-TrFE)/BP FeFETs. (a) Sketch of biologic synapse with signal transmission process. (b) PSC triggered by several consecutive electrical pulses and A is defined as the amplitude of PSC. (c) PPF index as a function of electrical pulse interval time Δt, the fitting curve exhibits that PPF decreases exponentially with the increase of Δt. Inset: Pulse voltage setting with increasing time interval.

Moreover, it has been observed that various programming schemes, encompassing pulse widths, amplitudes, and frequencies, exert a significant influence on the synaptic weight update characteristics. The influence of pulse width on the conductance states

is depicted in Figure 3-11(a), where an increase in pulse width from 10 ms to 100 ms leads to an augmentation in the conductance states.

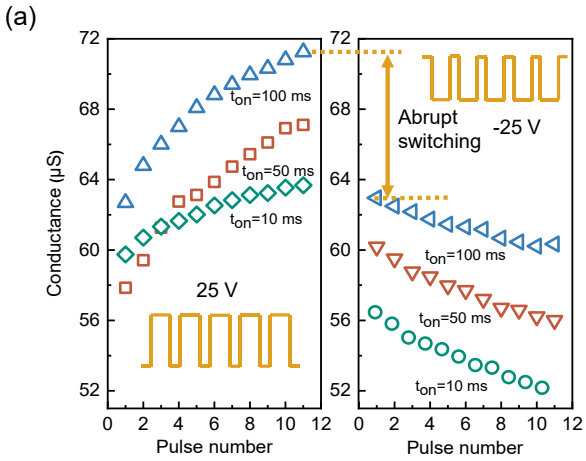


Figure 3-11: Conductance weight modulation within P(VDF-TrFE)/BP FeFETs. (a) The conductance weight modulation when P(VDF-TrFE)/BP synapses are subjected to a train of ±25 V voltage pulse under various pulse widths.

Additionally, the magnitude of the conductance can be effectively modulated by the gate voltage, wherein an increase in pulse amplitude corresponds to higher conductance levels, aligning with the synaptic behavior (Figure 3-12). Figure 3-12 demonstrates that the magnitudes of conductance variations increase proportionally under positive (Figure 3-12(a)) and negative (Figure 3-12(b)) gate voltage ranges. This observation indicates that a higher drive voltage facilitates a more pronounced switching of the ferroelectric polarization, resulting in a more substantial amplitude of conductance change. It is worth mentioning that larger pulse amplitudes can enhance the conductance ratio at the expense of reducing the number of intermediate conductance states.[137]

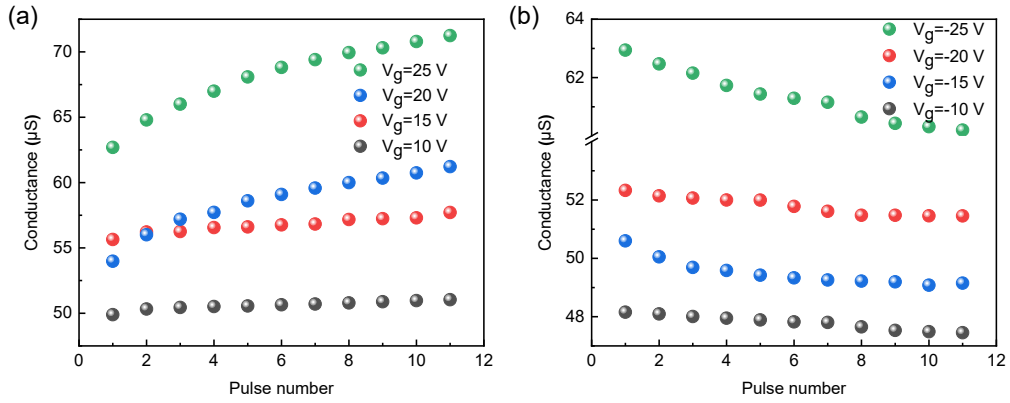


Figure 3-12: Amplitude of gate voltage pulse modulation on conductance. (a) The potentiation weight modulation from 10 to 25 V in 5 V steps for P(VDF-TrFE)/BP synapses. (b) The depression weight modulation from -10 to -25 V in 5 V steps for P(VDF-TrFE)/BP synapses.

Energy consumption for a single pulse event is related with pulse width and height[138] and is estimated to be 41.02 fJ under 1 mV source-drain voltage (Figure 3-13).

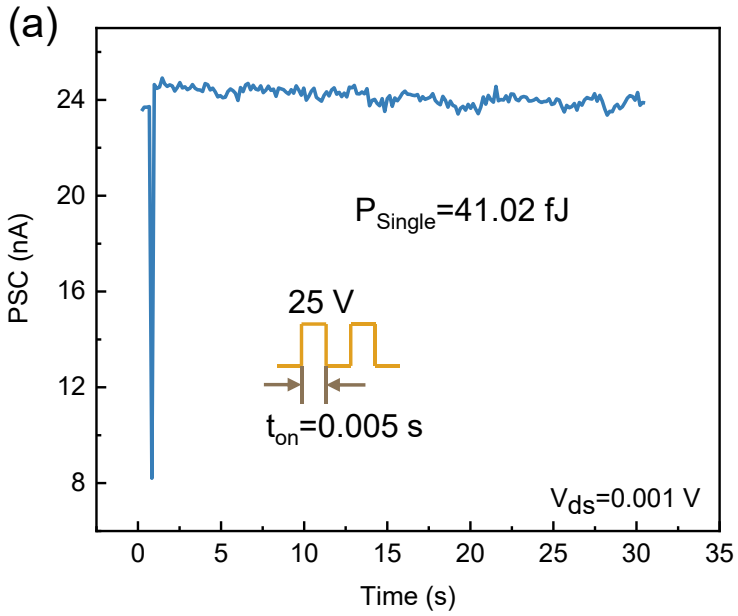


Figure 3-13: (a) Energy consumption of a single pulse event with fixed V_{ds}.

Such ultra-low energy consumption is comparable to human brain synapse (10 fJ). The energy consumption for a single pulse event is calculated based on the following

equation[139]:

$$P = I_{peak} \times t_{on} \times V \qquad (3-1)$$

where I_{peak} is the peak current through the active channel, t_{on} is the time duration of the synaptic event, and V is the source-drain voltage. The low energy consumption results from high carrier mobility of BP and effective ferroelectric gate modulation, which could promote signal transmission within synapse.[140-141] In addition, thanks to the small source-drain voltage under ohmic contact, consuming power in the nonvolatile FeFETs can be minimized for each synaptic event. The detailed power consumption with other reported synaptic transistors have been listed in Table 3-1, which suggests P(VDF-TrFE)/BP advantages for energy-efficient neuromorphic system.

Table 3-1. Comparison of energy consumption of P(VDF-TrFE)/BP with other artificial synapses

Functional materials	Active channel	Energy power consumption	Bias voltage (V)	Reference No.
P(VDF-TrFE)	PDVT-10 film	1.2 nJ	-10	[124]
P(VDF-TrFE)	P3HT nanowire	12.3 fJ	0.02	[142]
P(VDF-TrFE)	MoS_2	9.5 pJ	/	[125]
P(VDF-TrFE)	Pentacene film	37.95 nJ	-10	[143]
HfO_2	HfO_2 film	8 pJ	-3	[144]
h-BN	WSe_2	66 fJ	0.3	[145]
Li ion	α-MoO_3	0.16 pJ	2.5	[146]
P(VDF-TrFE)	**BP**	**41.02 fJ**	**0.001**	**This work**

In neurological system, synaptic weight update behaviors can be modulated under

different temporal patterns.[147] Figure 3-14(a) shows the plot of the conductance in response to successive spikes under positive gate voltage with frequency ranging from 0.8 to 4 Hz. Under positive gate pulses, higher stimulus frequency leads to a more prominent potentiation effect Figure 3-14(a)). By contrast, the peak values of the resulting conductance decrease with the stimulus frequency increasing under negative voltage (Figure 3-14(b)). The above phenomenon strongly illustrate that our P(VDF-TrFE)/BP neuromorphic device can serve as a frequency filter. To further describe the filtering property, the frequency-dependent conductance change percentage is exhibited in Figure 3-14(c), the conductance can increase from 35.6 % to 58.2 % and reduce from -0.9 % to -2.7% when the pulse frequency is increased.

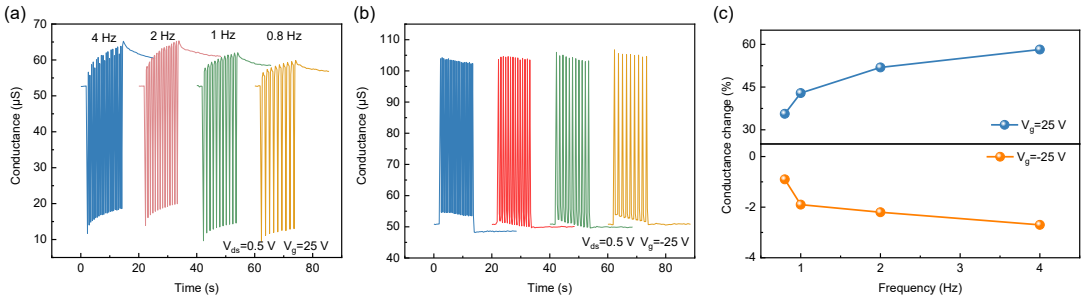


Figure 3-14: Spike frequency-dependent responses of channel conductance under 25 V (a) and -25 V (b). (c) Conductance gain and reduction under positive and negative pulse voltage plotted as a function of spike frequency.

We also simulate the memory strengthening process based on ferroelectric gate voltage tuneability. P(VDF-TrFE)/BP transistors can realize three memorizing modes by PSC change magnitude under different gate values. Artificial visual system and the three memorizing phases are exhibited in Figure 3-15. The information captured by

human eyes is first stored in IM (Instant memory) with a large capacity but a short duration. With stronger potent stimuli, IM will be transferred into STM (Short -term memory) in a more durable time. After that, through repetitive rehearsal or more intensive stimuli, information in STM will be changed into LTM (Long-term memory) and stored for a long time.[148] The intensity of stimuli determines the memory storage degree, and the connection strength between two neurons manifests the memory level.

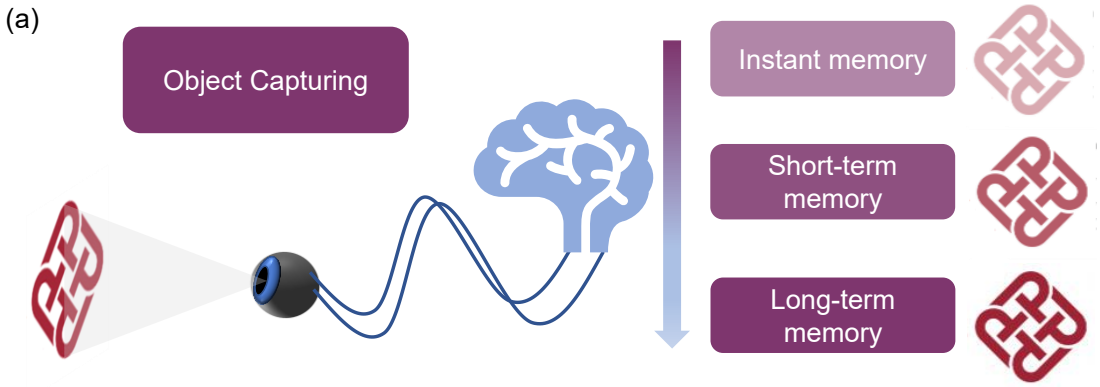


Figure 3-15: Artificial visual system and three memorizing phases.

In order to reflect the change of PSC and the degree of information storage, we define and calculate the memory parameter δ_M. From Figure 3-16(a-c), δ_M can be effectively adjusted by the ferroelectric gate voltage. δ_M is 4.34% (instant memory), 17.90 % (short-term memory), and 25.62% (long-term memory) under the gate voltages of 15 V, 20 V, and 25 V, respectively. The increased gate voltages will contribute to the switching of ferroelectric polarization and generate enhanced PSC change magnitude. Such results are similar to the biological memory consolidation process, represented by the amount of neurotransmitter release.[149]

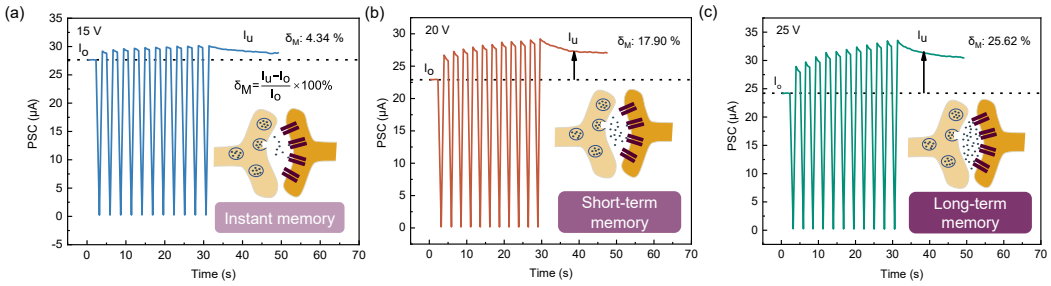


Figure 3-16: Memorization process demonstration. Electrical PSC response of P(VDF-TrFE)/BP synaptic transistors modulated by the different ferroelectric gate voltages of 15 V (a), 20 V (b), and 25 V (c), respectively. Inset: Schematic diagram of neurotransmitter release amount, representing synaptic connection strength under different gate voltages.

3.5 Pattern recognition with multilayer perception neural network.

In order to demonstrate detailed LTP and LTD synaptic behaviors, 40 successive ±25 V gate pulses are applied to the gate electrode (Figure 3-17(a)). The real-time conductance change of potentiation and depression under different gate voltage is displayed in Figure 3-17(b-c).

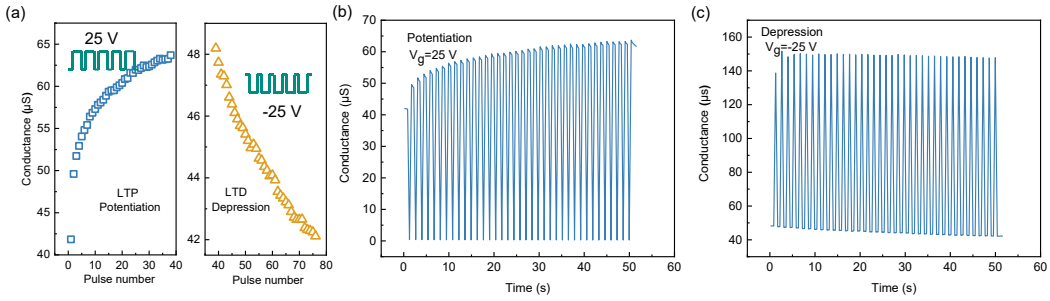


Figure 3-17: LTP and LTD behaviors of P(VDF-TrFE)/BP devices. (a) LTP and LTD operations under 25 V and −25 V (100 ms on time) with 40 pulses, respectively. The real-time potentiation (b) and depression (c) processes under 40 stimulations with

±25 V top gate voltage.

Figure 3-18 demonstrates the cycle-to-cycle variation by applying 400 consecutive pulses and shows little difference between each cycle. The nonlinearity parameter, asymmetric factor, and cycle variation are essential metrics for synaptic devices, which directly impact the accuracy for neuromorphic computing.

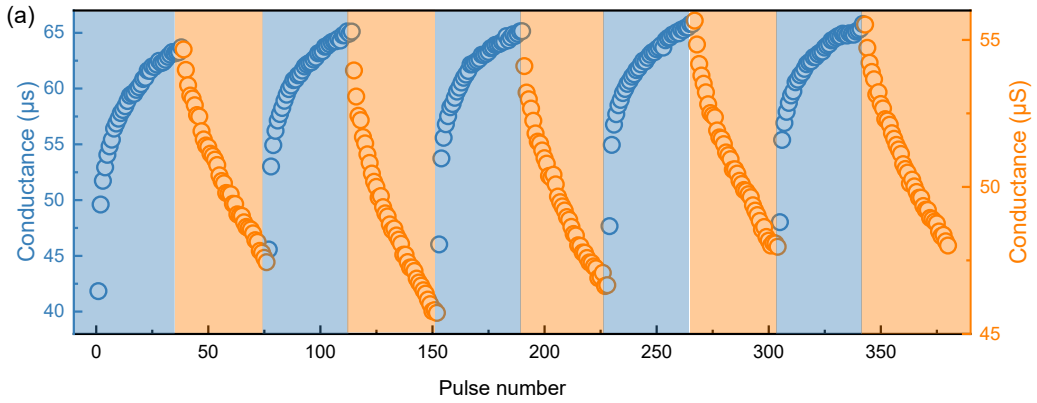


Figure 3-18: Cycle-to-cycle variation of P(VDF-TrFE)/BP based artificial synapses under 400 pulses stimulations.

Table 3-2 lists the obtained quantities based on analog weight update and detailed fitting equations and normalize results are provided in Figure 3-19. The nonideal factors of the demonstrated weight update for P(VDF-TrFE)/BP devices are obtained according to the following steps based on MATLAB script nonlinear_fit.m.

Table 3-2: Realistic LTP and LTD behaviors of P(VDF-TrFE)/BP synapses

	Nonlinearity parameter	Cycle-to-cycle variation	Asymmetric factor
LTD	2.07	0.011	0.463
LTP	4.47	0.014	

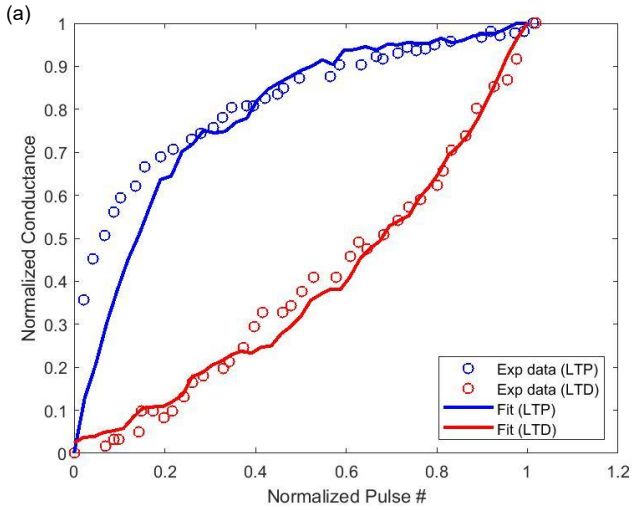


Figure 3-19: Fitting curve of P(VDF-TrFE)/BP weight update results in the plot of normalized conductance under the normalized number of pulses.

According to the results, both nonlinearities remain below 4.5, with a minimum value of 2.07, and the cycle-to-cycle variation is kept below 0.015. Maximum symmetry value is smaller than 0.47. The above results indicate that nonideal factors of the demonstrated P(VDF-TrFE)/BP are at the same levels with previous reported ferroelectric synapses based on graphene or WSe_2.[150]

Such device systems have successfully simulated different synaptic behaviors based on multilevel conductance states and laid foundation for further neuromorphic computation. Therefore, to perform pattern recognition applications, a multilayer perceptron ANN is integrated. For the simulation section on the CrossSim platform, we used an 8×8 pixel image version of handwritten digits, 28×28 pixel version of MNIST handwritten digits dataset, and Sandia file classification dataset.[151] Schematic diagram used for the input pattern recognition process consists of a three-layer network (Figure 3-20). In the system, the 784 neurons in the input layer correspond to the 28×28 (pixels)

of the MNIST image, and the 10 output neurons correspond to 10 classes of digits (from 0 to 9).[152] The multilayer perception system is an interconnected network.

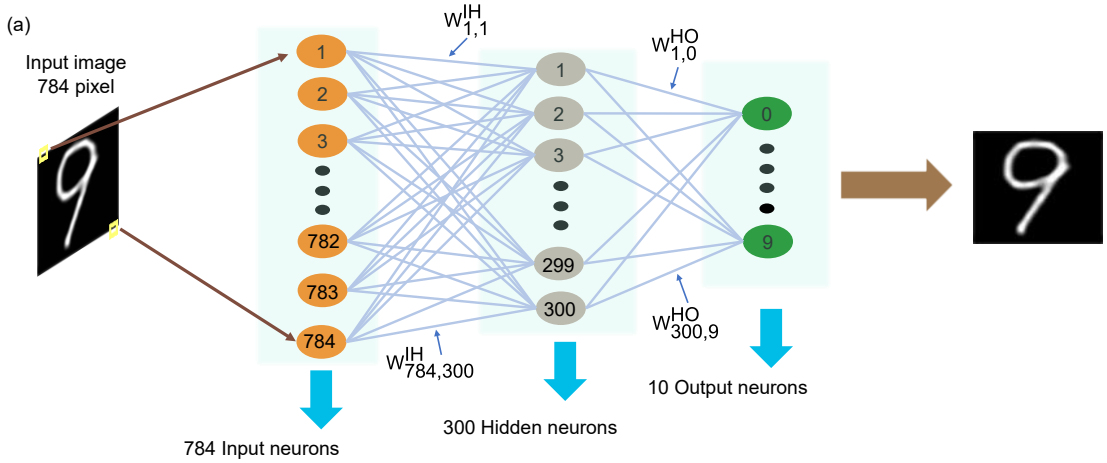


Figure 3-20: Schematic illustration of a three-layer (one hidden layer) neural network for recognition tasks.

A detailed circuit diagram of a synapse layer like a crossbar structure consisting of M×N P(VDF-TrFE)/BP transistors is shown in Figure 3-21. In programmable voltage operations, voltages are applied on the rows, and currents are read from the columns. Transport operation is also applicable with such voltage and current settings. Vector matrix multiply calculation is performed in each layer. Resulted numerical weights are reflected directly by the conductance states of FeFETs. In this crossbar array, every 2D synaptic transistor can be regarded as an individual memory element for matrix operations. Channel conductance states have been adopted as the synaptic weight updates for executing the back-propagation.[153]

The ANN simulation is based on the CrossSim platform in a Python environment. The number of devices used in the backpropagation training simulations depends on

the dataset. Each of the two layers used by algorithm requires a crossbar. For instance, the large image dataset has 784×300=235200 synapse crossbars in one layer and 300×10=3000 synapse crossbars in another layer.

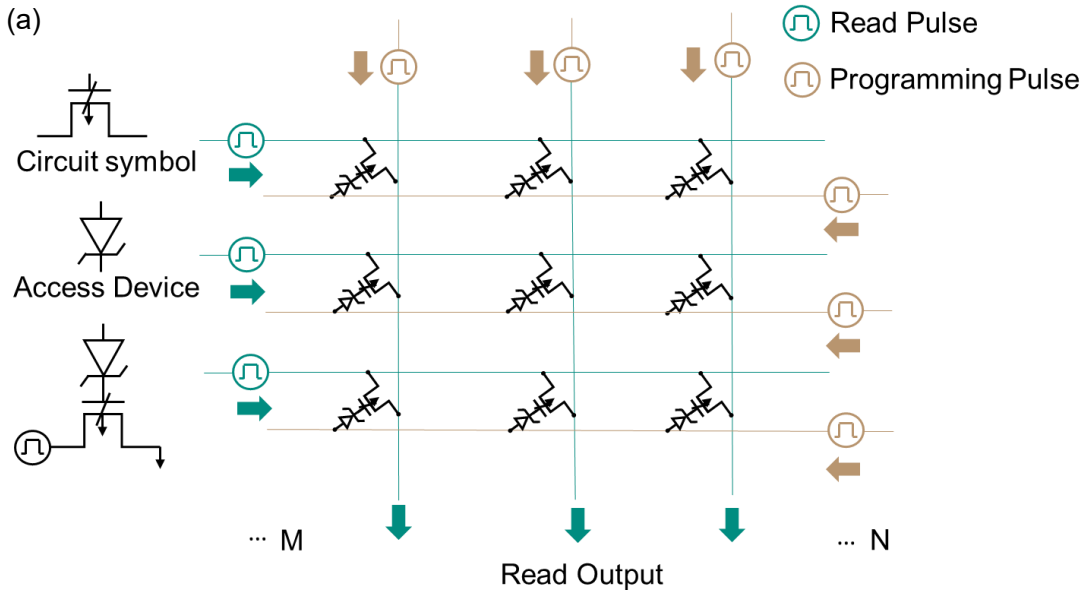


Figure 3-21: The voltage-controlled crossbar circuits based on P(VDF-TrFE)/BP FeFETs for analog matrix operations. This schematic includes a circuit symbol for hybrid devices and the access device that prevents FeFETs from discharging when it is not programmed.[154]

The recognition accuracy during 40 epochs of ideal synapse for the three classification datasets are shown in Figure 3-22. In the first few epochs, the recognition accuracy enhances dramatically and reaches saturation value of more than 90%, which approaches the neuromorphic algorithm limit. Note that the training outcomes of high accuracies between 90% and 94% are comparable to other state-of-the-art nonvolatile memories[155-156], and they can be further improved by various voltage pulse schemes. Therefore, ANN simulation at the system level indicates outstanding performance in

pattern recognition.

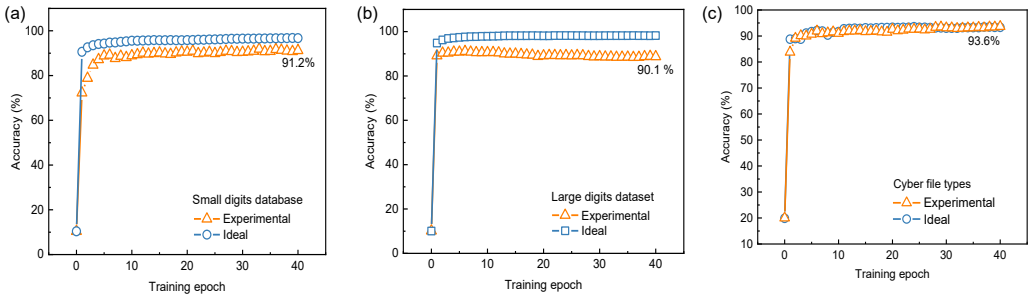


Figure 3-22: The simulated pattern recognition accuracy of small digits database (a), large digits database (b), and file types (c) of P(VDF-TrFE)/BP synaptic transistors compared with the ideal cases.

3.6 Conclusion

In conclusion, taking advantage of the emerging concept of 2D FeFETs, we have developed P(VDF-TrFE)/BP ferroelectric synapse based on ferroelectric gate tunability and a high degree of functionality for synaptic behavior operations. These findings highlight the prospects of 2D ferroelectric field-effect transistors as ideal building blocks for high-performance neuromorphic networks. The presented FeFETs can perform a large on/off ratio and high mobility under small bias voltage, with very low femtojoule level (~40 fJ) of energy consumption. Based on synaptic weight updates, a series of synaptic plasticity and biological memory consolidation process can be emulated. The neural network simulation shows a high recognition accuracy of ~93.6% for handwritten digits. The proof-of-concept device opens up a way for implementing energy-saving and highly integrated artificial neural system.

Chapter 4 Multifunctional optoelectronic neuromorphic devices for wavelength-selective artificial visual system

4.1 Introduction

Human visual system, consisting of the retina, optic nerve, and visual cortex, plays a crucial role in acquiring and filtering information from the external world with remarkable real-time perception and visual information processing abilities.[157] Compared to the traditional machine vision system based on von Neumann architecture, the bio-inspired neuromorphic vision systems can integrate features of the sensing, memory and processing.[158-161] Researchers have currently made progress in developing 2D materials-based visual devices that closely replicate the functions of various cells in the human visual system.[162-164] These innovative devices are capable of detecting and processing visual information[46, 165] and have also achieved the improved recognition accuracy.[166-169] Such synaptic devices contribute to the integration and energy-saving for computation architecture.[170-171] Neuromorphic optoelectronic vision system inspired by the biological platform displays potential for in-sensor computing.

One of the crucial functionalities of the retinal cell is the ability to discern colorful information while extracting relevant signals from the noisy environment, resembling the process involved in conducting color blindness screening tests. Also, by leveraging the color-recognition mechanism, extracting crucial light information can effectively reduce interference caused by redundant data and enhance the speed of next signal

processing. This characteristic closely aligns with the efficient information processing observed in the human visual system.[172-173] However, it is still challenging to achieve such complicated sensing or learning purposes based on one simple optoelectronic synaptic device. In this regard, channel materials with higher performance, more simplified structures and adjustable device mechanisms need to be investigated for multifunctional neuromorphic visual platforms. Combination of 2D direct bandgap materials and ferroelectric materials as heterostructures holds potential for neuromorphic visual sensors.[174-175] ReS_2 is adopted as channel layer for several reasons. 1) It manifests a direct bandgap over a broad range of thicknesses.[176] 2) ReS_2 demonstrates remarkable stability and enhanced light absorption capabilities, making it a promising candidate for optoelectronic applications.[177] 3) ReS_2 exhibits weak interlayer coupling and a low energy barrier for sulfur vacancy formation. Thus, the activation barrier experienced by electrons trapped at sulfur vacancies hinders radiative recombination[178-180] and the pronounced persistent photoconductivity effect (PPC) is more likely to be observed. On the other hand, the transparent ferroelectric copolymer P(VDF-TrFE) is used as dielectrics, allowing for efficient light transmission. The low-temperature spin-coating process compared with traditional ferroelectric materials facilitates the formation of a good vdWs interface between the semiconductor and ferroelectric copolymer.[181-182] Furthermore, ferroelectric copolymers exhibit exceptional mechanical stability and flexibility, making them highly suitable for thin film fabrication at comparatively low temperatures on various flexible substrates with

cost-effective processing techniques.[97, 183]

In this chapter, we design a multifunctional optoelectronic ferroelectric synaptic transistor consisting of 2D materials ReS_2 and ferroelectric polymer P(VDF-TrFE) with synapse behaviors simulation, multi-color perception and visual neuromorphic computing functionalities. The comprehensive study includes detailed optoelectronic performances and mixed-wavelength image preprocessing pertaining to basic synapse plasticity. Versatile synaptic behaviors, including PPF, short-term/long-term potentiation (STP/LTP), short-term memory (STM) and long-term memory (LTM) transition can be realized. Advanced neuromorphic feature of learning-forgetting-relearning process is also successfully mimicked. Based on single optoelectronic synapse, we establish a neuromorphic visual array model to simulate the retina for light-intensity sensing and color distinguishment. Through light-induced conductance difference, the contrast of the desired object becomes more obvious while reducing surrounding noise signals. The optoelectronic devices array is trained to implement image recognition with a high accuracy of 96%. These findings demonstrate the potential of the ferroelectric optoelectronic device to achieve perception, object recognition, and energy-efficient operations, bringing one step closer to replicating the human visual system.

4.2 Visual synaptic device and functional materials characterization

4.2.1 Visual synaptic devices

In Figure 4-1, an illustration of the biological human visual system is presented,

highlighting the three essential steps in vision information processing. Initially, optical signals are converted into electrical signals by the retina. The rod and cone photoreceptors play distinct roles in detecting light intensity and light colors, respectively.[184] Subsequently, these electrical signals travel through the optic nerves, reaching the visual cortex where visual features are extracted. Ultimately, visual features are transmitted to higher brain regions for cognitive processes.[185] Motivated by the diverse functionalities of the human vision system, three-terminal ferroelectric synaptic transistor is proposed to emulate the retina in terms of multi-wavelength sensing, electrical signal conversion, and image information processing.[186] The receptors on the postsynaptic neuron receive the external stimulus released from the presynaptic neurons through the diffusion effect of neurotransmitters. This process allows for the modulation of the strength and magnitude of the postsynaptic response, thereby reflecting synaptic plasticity.[187]

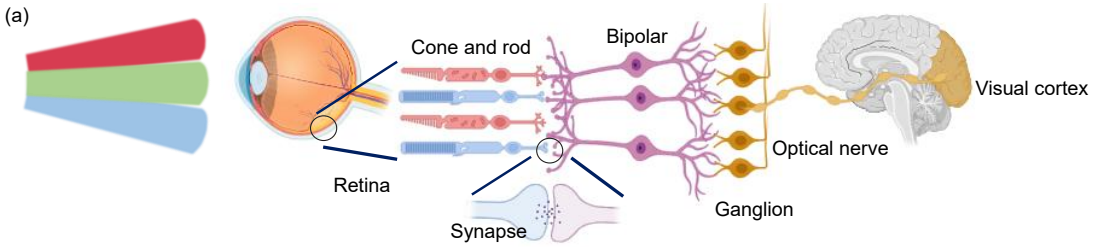


Figure 4-1: Schematic illustration of biological vision system including the retina, optical nerve, and visual cortex as well as a basic component of one synapse.

The detailed synaptic device structure including P(VDF-TrFE) and ReS_2 is displayed in Figure 4-2, which is regulated by optical and electrical signals.

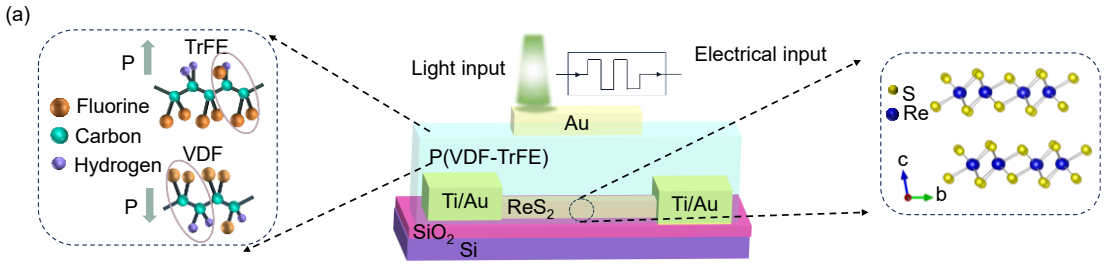


Figure 4-2: 3D structure of artificial optoelectronic synapse based on P(VDF-TrFE) and ReS_2.

Such devices are fabricated as follows (Figure 4-3): First, Ti/Au (5 nm/25 nm) metal electrodes are prepared on p-Si/SiO_2 (285 nm) substrates with standard lithography technique and electron beam deposition. 2D ReS_2 flakes are mechanically exfoliated onto the polydimethylsiloxane (PDMS) supports with blue tape. The ReS_2 flakes are identified on the PDMS by the optical microscope, and then interested ones are selected for further dry transfer process. The P(VDF-TrFE) (70:30 in mol %) thin films (~300 nm in thickness) as dielectric layers are made by the spin-coating process. The detailed parameters for the spin-coating are 400 rpm for 10 s and 3000 rpm for 40 s. The P(VDF-TrFE)/ReS_2 structures are annealed at 135 °C in the vacuum for 2 h. Finally, a semi-transparent Au electrode of 10 nm as the top metal electrode is transferred through PVB films. Then, the whole device is immersed into the ethyl alcohol solution for half an hour under 45 °C to dissolve the PVB film without damage to the P(VDF-TrFE) copolymer and the whole device structure.

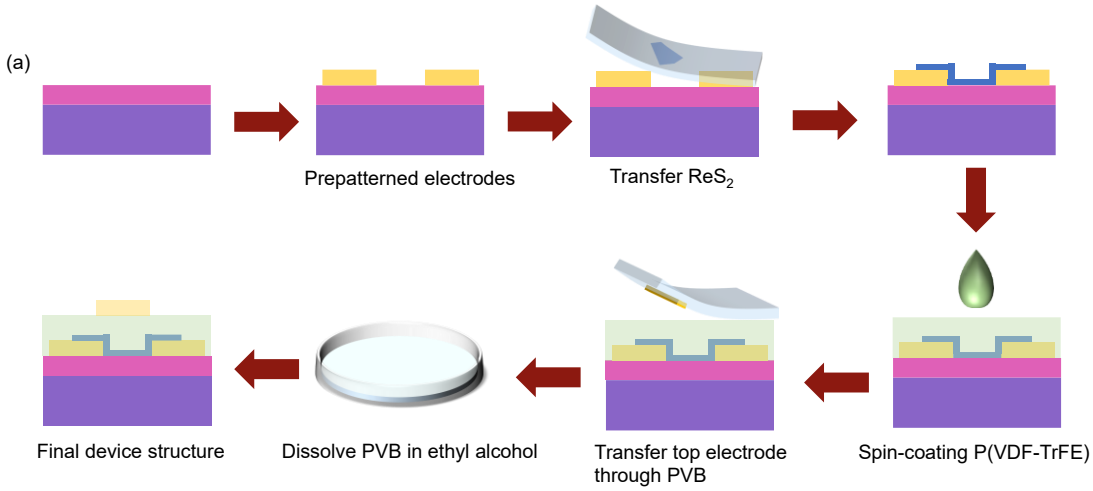


Figure 4-3: Device fabrication process diagram.

4.2.2 Functional materials characterization

The Raman spectrum of ReS_2 in Figure 4-4(a) shows characteristic peaks of A_g-type modes, located at 138 and 143 cm^{-1}, and E_g-type modes are located at 152, 162, 212, cm^{-1}. A_g mode and E_g mode correspond to the out-of-plane and in-plane vibrational modes of the Re atoms, respectively.[188] The thickness of ReS_2 is about 8 nm measured by AFM (Figure 4-4(b)). This β phase P(VDF-TrFE) is characterized by the alignment of molecular chains in the same direction, resulting in a high dipole moment due to the distribution of positively charged hydrogen atoms and negatively charged fluorine atoms.[189] The coercive voltage (V_c) is determined to be 15 V and the remnant polarization (P_r) is 6 $\mu C/cm^2$, as shown in Figure 4-4(c). Furthermore, the abrupt changes observed in the parallelogram-shaped piezoelectric response loops and butterfly-shaped amplitude loops indicate that the polarization is compelled to shift upwards or downwards under the influence of the applied writing voltage (Figure 4-4(d)). By applying voltage with opposite polarity, the ferroelectric domains exhibit

distinct phase differences, suggesting the stability to program the ferroelectric domains into arbitrary shapes (Figure 4-4(e)).

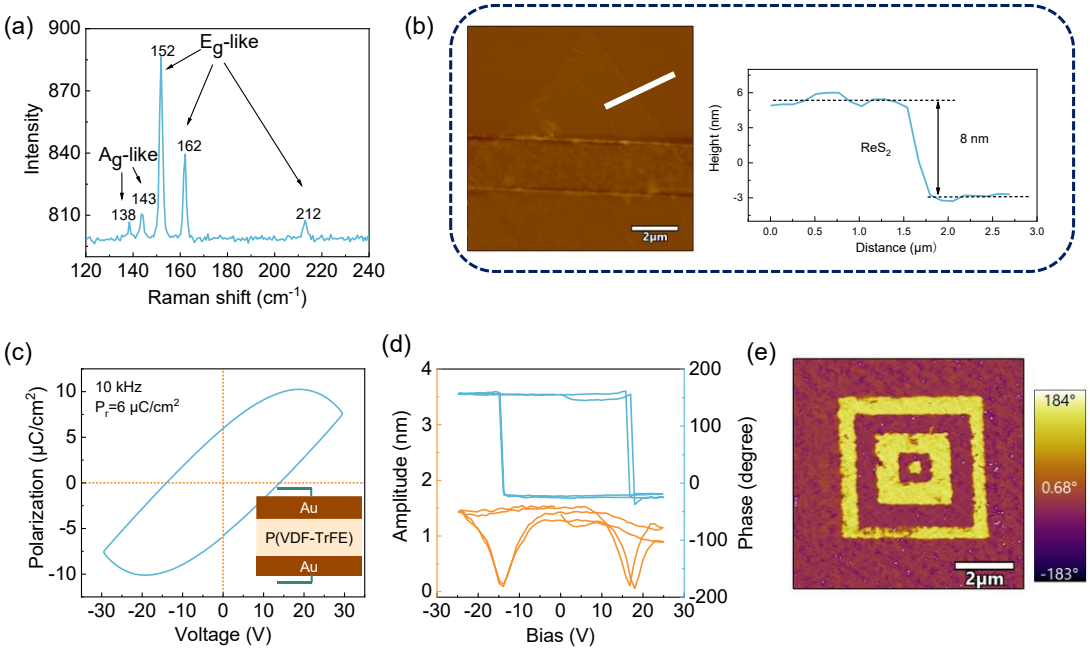


Figure 4-4: Characterization of ReS_2 and P(VDF-TrFE). (a) The Raman spectrum of ReS_2 nanosheet. (b) AFM image of the ReS_2 sample and AFM scan along the white line. (c) Ferroelectric hysteresis loop acquired in Au/P(VDF-TrFE)/Au capacitor at a test frequency of 10 kHz. (d) The hysteresis loops of PFM phase and amplitude observed in P(VDF-TrFE). (e) The PFM phase of P(VDF-TrFE) after being polarized by probes, demonstrating a "box-in-box" ferroelectric domain pattern.

4.3 Working mechanism and synaptic behavior measurement

4.3.1 Synaptic devices working mechanism

Figure 4-5 elucidates the working mechanism of ferroelectric synaptic devices P(VDF-TrFE)/ReS_2 through the band diagrams. In the fresh state, the distribution of dipoles in the ferroelectric layer is approximately random, and there is no significant

energy band bending in the ReS_2 channel (Figure 4-5(a)). By applying a positive gate voltage above V_c (Figure 4-5(b)), ferroelectric dipoles become orderly arranged pointing from the gate electrode to the ReS_2 channel and the polarization in the P(VDF-TrFE) layer is driven downward. Electron accumulation occurs on the ReS_2 channel. The energy band of ReS_2 at the interface bends downward while the Femic level is closer to the conductance band, which indicates the low-resistance state. Following the elimination of the electrical spikes, the alignment of the ferroelectric dipoles persists, generating the nonvolatile memory functionality. Meanwhile, a gradual alteration of the polarization domains occurs as the spike pulse is continuously applied, accompanied by a notable increase of electrons within the channel region. Therefore, subsequent spikes bring with them enhanced channel conductance. Such continuous evolution of ferroelectric domains can be regarded as the ferroelectric plasticity. Conversely, a negative electrical pulse induces upward polarization in the P(VDF-TrFE) polymer, depleting electrons in the ReS_2 channel and energy-band bends upward. At this time, the Fermi level is close to the valence band and high-resistance state is demonstrated, as shown in Figure 4-5(c). Similarly, such behavior is also featured with nonvolatile characteristic. When the inhibitory spikes are applied consecutively, the polarization domains are aligned upward gradually, thereby depleting electrons in the channel.

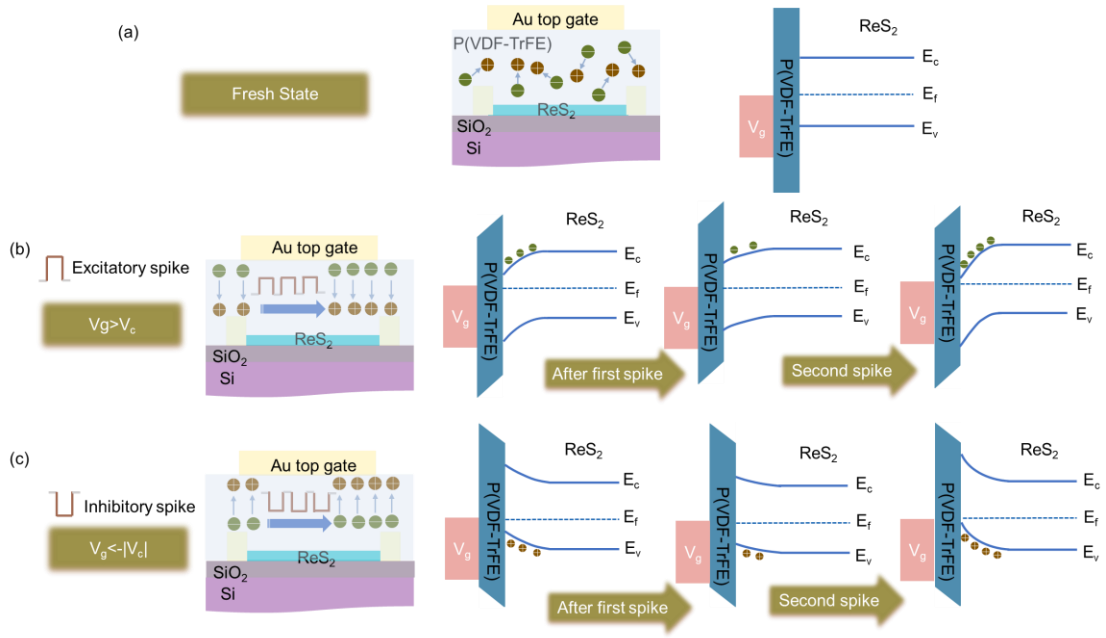


Figure 4-5: Working mechanism of the ferroelectric synaptic device P(VDF-TrFE)/ReS_2 under electronic mode. Dipoles distribution and energy band diagram of the ReS_2 ferroelectric transistor covered with P(VDF-TrFE) under (a) fresh state, (b) polarization down state, and (c) polarization up state, respectively.

4.3.2 Electronic performance

Electrical tunable synaptic plasticity is crucial for signal conversion and lays the foundation for information extraction reflected by PSC. All electrical characterizations are carried out in vacuum at room temperature. In Figure 4-6(a), a series of output curves ranging from 10 V to 25 V with a step of 5 V are presented. These output characteristics exhibit a linear correlation within a bias voltage range of -1 to 1 V, suggesting an Ohmic contact between the ReS_2 channel and Au electrodes. Subsequently, transfer curves of P(VDF-TrFE)/ReS_2 transistors are examined (Figure 4-6(b)). The ferroelectric field effect transistors based on multilayer ReS_2 possess high

current ratios of up to 10^9 between on and off states, suggesting a high-quality interface between ReS_2 and P(VDF-TrFE) and the effective ferroelectric modulation for the ReS_2 channel.[190] The measured transfer characteristics also exhibit a typical n-type behavior and a large memory window (≈14 V) during the hysteresis process, which is related to the nonvolatile ferroelectric polarization. Conversely, the ReS_2 device on a silicon substrate without ferroelectric gating does not exhibit a hysteresis window for both transfer (Figure 4-6(c)) and output (Figure 4-6(d)) characteristics, indicating that ferroelectric polarization plays a dominant role in tuning the electronic behavior of the channel.

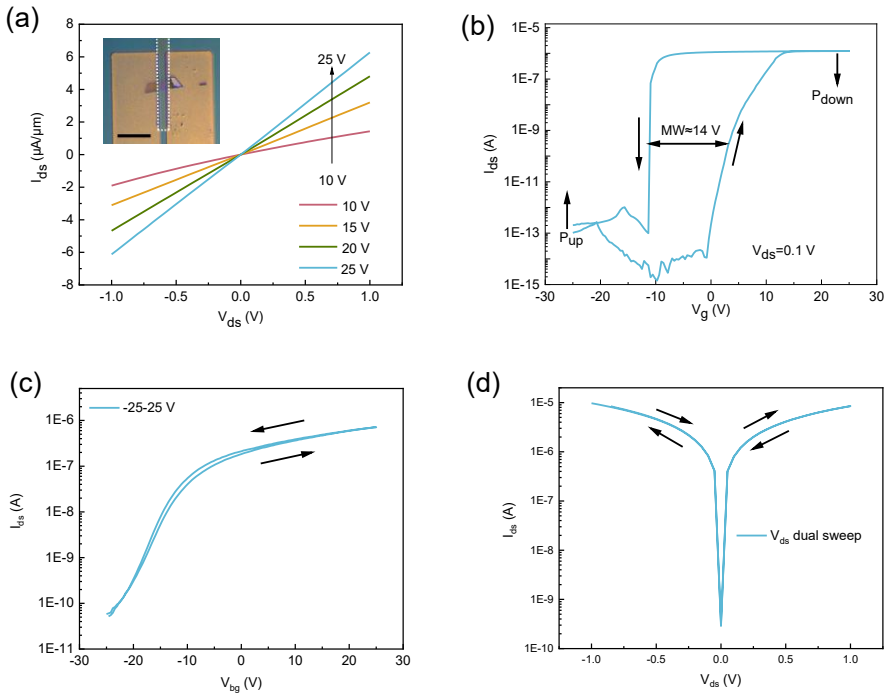


Figure 4-6: A series of output curves for P(VDF-TrFE)/ReS_2 and ReS_2 devices. (a) Output characteristics under various top gate voltage, indicating excellent linearity in the range of -1-1 V. (b) Transfer curve at V_{ds} of 0.1 V, demonstrating ferroelectric hysteresis behavior. (a) The transfer characteristic curve with a forward and backward

sweep of the ReS_2 sample on the silicon substrate without a ferroelectric top gate under a gate voltage of ±25 V. (b) Output curve in log scale under dual voltage sweep of ReS_2 device on a silicon substrate under the max drain-source voltage V_{ds} = 1 V. There is no obvious hysteresis phenomenon.

In the linear scale of the transfer curve, the hysteresis window becomes larger as the gate voltage range increases (Figure 4-7(a)). Moreover, the linear mobility is plotted (Figure 4-7(b)). The mobility values span a range of 40 to 45 $cm^2\ V^{-1}\ s^{-1}$ across all gate voltages. Therefore, it is worthwhile to mention that the electrical performance of P(VDF-TrFE)/ReS_2 devices are reasonably superior in terms of on/off ratio and carrier mobility.[191-192]

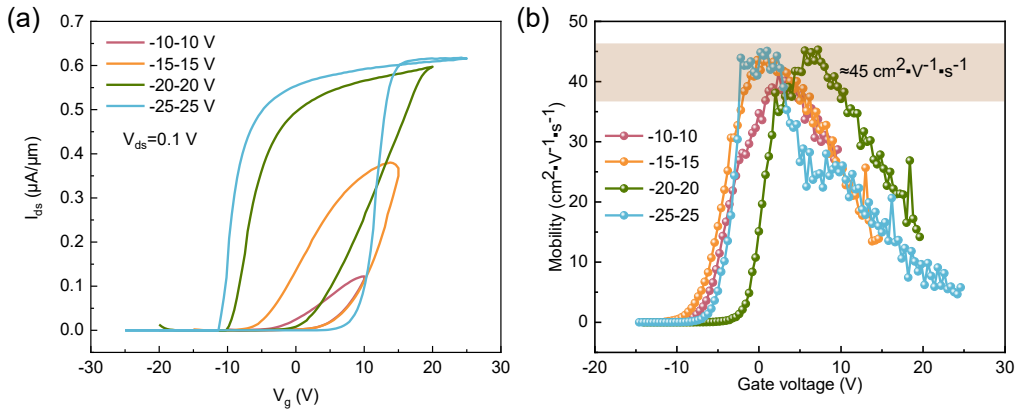


Figure 4-7: Transfer curves and mobility performance of P(VDF-TrFE)/ReS_2 transistors. (a) In the linear scale of transfer curves, the hysteresis window becomes greater as the gate voltage range increases under the bias voltage of 0.1 V. (b) Linear mobility plot of top gate P(VDF-TrFE)/ReS_2 transistors.

4.3.3 Synaptic behavior of ReS_2 based ferroelectric devices

The above performances confirm that the prepared devices possess nonvolatile

ferroelectric behaviors and the fundamental potential to emulate biological synaptic plasticity. Next, the synaptic behaviors based on a single electrical pulse are investigated. As shown in Figure 4-8(a), excitatory postsynaptic current (EPSC) responses are triggered by the gate voltage with amplitude from 10 V to 25 V while maintaining a constant pulse duration time of 0.1 s. Increasing the pulse amplitude leads to higher EPSC. Additionally, following stimulation with voltage pulses, the EPSCs do not return to their initial values, and a higher voltage amplitude will bring a more noticeable remaining current. This observation indicates a transition from short-term potentiation to long-term potentiation through voltage amplitude adjustment. Moreover, the pulse width also demonstrates effective modulation of the channel current. The EPSC gradually increases with an increase in pulse width, while the EPSC decay is slower for longer pulse widths Figure 4-8(b). Hence, larger amplitude and longer width are conducive to ferroelectric polarization, confirming a correlation between ferroelectric nonvolatility and EPSC modulation. Furthermore, we investigate the response speed of P(VDF-TrFE)/ReS_2 devices. The devices exhibit a response time of 2 ms when subjected to 20 V and -20 V write spikes, as illustrated in Figure 4-8(c-d). When a 2 ms fast write spike of 20 V (-20 V) is applied, the channel undergoes a transition from the initial low resistance state to a high resistance state (or from a high resistance state to a low resistance state). Notably, the channel current remains non-volatile, thereby demonstrating the fast programmability of P(VDF-TrFE)/ReS_2 ferroelectric transistors. The upper insert in the figure illustrates the actual waveform

of the fast write spikes.

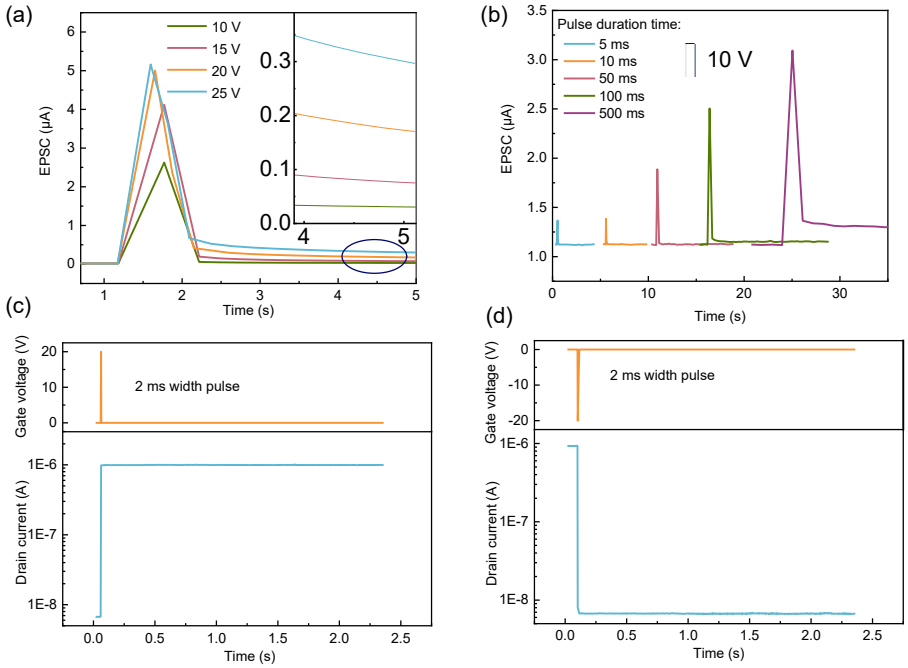


Figure 4-8: EPSC behaviors modulated by pulse amplitude and width and response speed of P(VDF-TrFE)/ReS_2 devices. (a) EPSC behaviors are triggered by a single electrical spike with different pulse amplitude (from 10 V to 25V) under 0.1 s pulse width, realizing the transition from short-term potentiation to long-term potentiation. (b) Different durations of a single electrical spike elicit distinct EPSC responses. The channel current transitions under the action of a 2 ms 20 V (c) and -20 V (d) write spikes.

It is widely recognized that short-term synaptic plasticity plays a pivotal role in information processing and human brain memory, and it primarily involves PPF. As illustrated in the inset of Figure 4-9(a), the emulation of PPF behavior is achieved by delivering a pair of pre-synaptic pulses (20 V, 100 ms) to the device. In this context, A1 and A2 denote the peak values of the current of the first and second pulse, respectively.

Notably, the EPSC elicited by the second pulse surpasses that of the first pulse, successfully simulating the PPF behavior. Subsequently, the relationship between the synaptic weights and the interval time can be analyzed by varying the interval time of the two pulses. The PPF index, depicted in Figure 4-9(a), can be mathematically expressed with equation (4-1) and fitted by exponential decay function (4-2):

$$PPF\ index = \frac{A_2 - A_1}{A_1} \times 100\ \% \qquad (4-1)$$

$$y = C_0 + C_1 e^{\frac{-x_1}{t_1}} + C_2 e^{\frac{-x_1}{t_2}} \qquad (4-2)$$

Parameters t_1 (67.88 ms) and t_2 (718 ms) represent the fast and slow relaxation processes, respectively, which are consistent with biological synapses in the range of milliseconds. C_0 represents a constant value of zero, indicating that the ratio of the PPF gradually approaches zero. Whereas C_1 and C_2 refer to the initial magnitudes of the two aforementioned phases.[193-194] The fitting curve demonstrates that the synaptic weights can be significantly improved by decreasing the interval time between the two consecutive pulses. When the interval time becomes sufficiently large, the EPSC reaches a saturation level and remains constant. The observed PPF behaviors in the ReS_2-based ferroelectric synaptic devices can be attributed to the accumulation of polarization in ferroelectric materials. When the interval time between two voltage spikes is shorter than the polarization relaxation time, the initially stimulated polarization, caused by the first spike, does not return to its original level by the time when the second spike arrives. Consequently, stronger polarization are accumulated after the second spike, resulting in an enhancement of the PSC.[195]

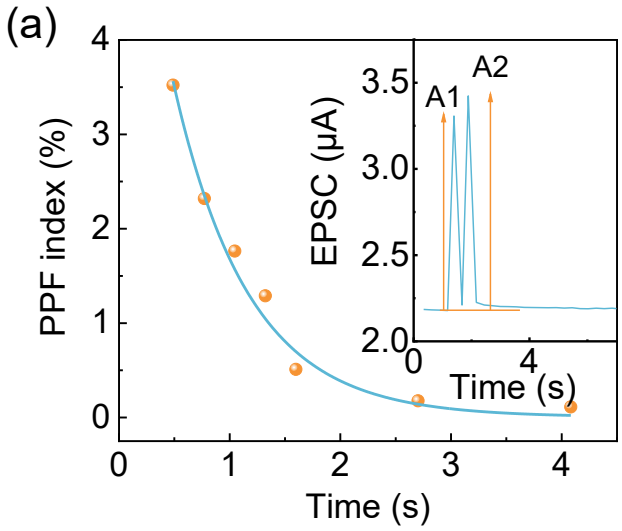


Figure 4-9: PPF index change with pulse interval time. The inset is EPSC triggered by two consecutive electrical pulses with an interval time of 100 ms.

Synaptic plasticity can also be modulated by different temporal patterns and the frequency-dependent behaviors have an impact on information transmission between neurons.[196] In this context, Figure 4-10(a) provides further insight into the EPSC response when several positive consecutive trains with varying frequencies are applied. At elevated spike frequencies, an augmented EPSC can be observed with a prolonged decay period. Moreover, the amplitude gain, defined as (An - A1)/A1, is used to characterize the filtering property of the device. An and A1 represent the EPSC amplitude of the first and last spikes, respectively. As depicted in Figure 4-10(b), the amplitude gain increases at high frequencies, reaching up to 15% at a frequency of 4.2 Hz, which is similar to the function of high-pass filtering.

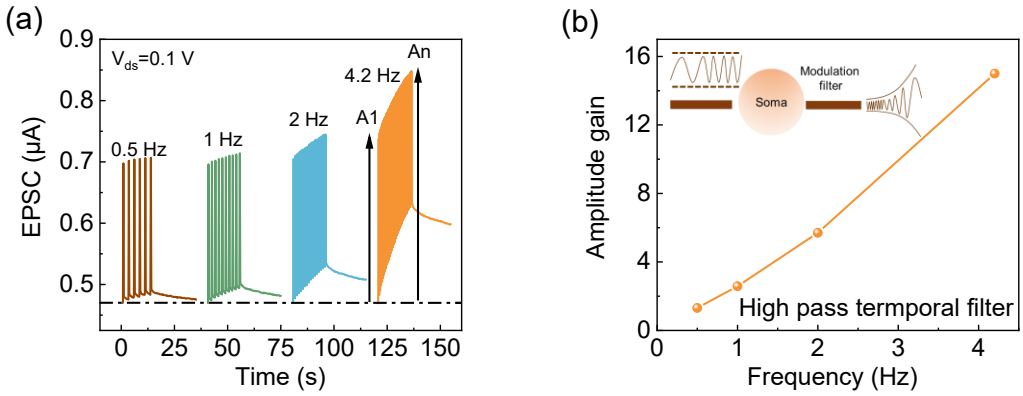


Figure 4-10: EPSC response under varying frequencies. (a) EPSC responses dependent on the frequency of electric spikes. (b) EPSC amplitude gain (An-A1)/A1 plotted as a function of external spike frequency based on the experimental result from (a). The insect image displays a schematic image of high pass filtering function.

The dynamics of P(VDF-TrFE) polarization, facilitated by voltage-tunable domain wall propagation, allows for the generation of multilevel resistive states and the modulation of connection strength between pre- and post-synapses.[197] Through the application of a sequence of identical voltage pulses of ±20 V exceeding the V_c to the ferroelectric P(VDF-TrFE) gate, a progressive alteration of channel conductance states is achieved. This enables the realization of LTP and LTD processes, based on the evolution of EPSC and inhibitory postsynaptic currents (IPSC). Here, Figure 4-11(a) illustrates the reliable and repeatable emulation of LTP and LTD behaviors in P(VDF-TrFE)/ReS_2. These experimental results demonstrate the effective emulation of biological synaptic behaviors in P(VDF-TrFE)/ReS_2, showcasing their potential for neuromorphic computation. The multi-level PSC represents that synaptic weights can be integrated into an ANN for handwritten recognition. The training is performed with

CrossSim platform.[198-199] Figure 4-11(b) presents a schematic diagram consisting of a three-layer network to illustrate the input pattern recognition process. The multi-layer platform is trained on different patterns at each epoch selected from the MNIST database, and the outcome is further tested.[146] The recognition accuracy of P(VDF-TrFE)/ReS_2 synapse during 40 epochs is shown in Figure 4-11(c). A significant increase is occurred in initial epochs, ultimately stabilizing at a saturation level of 89.95 %. Such high accuracy is comparable to state-of-the-art nonvolatile memories.[156, 200]

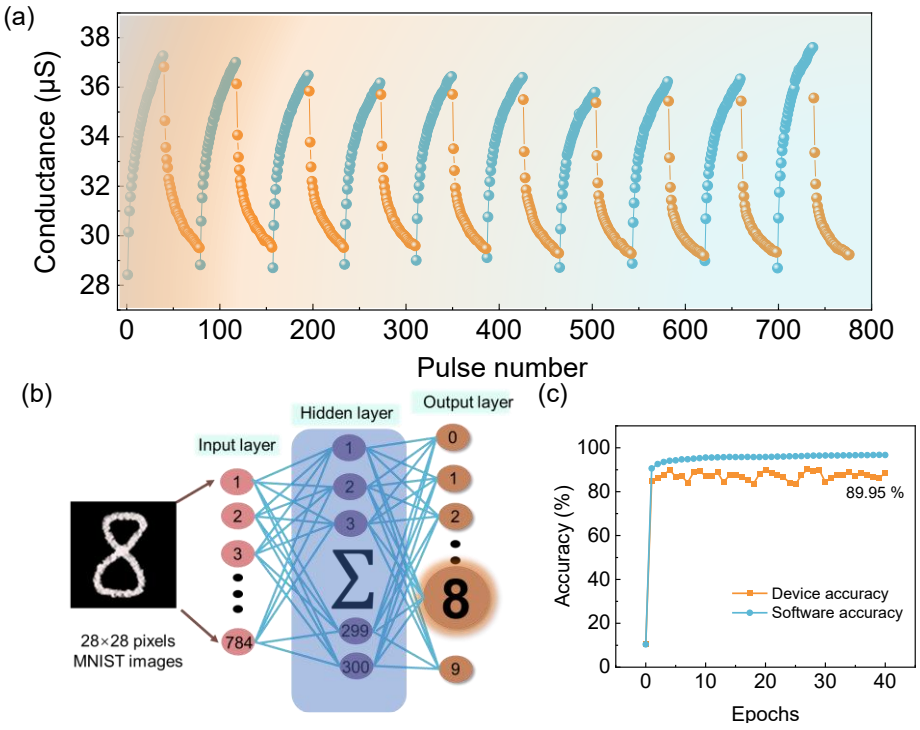


Figure 4-11: Multi-cycles conductance modulation within P(VDF-TrFE)/ReS_2 and recognition process. (a) Process of synaptic potentiation and depression by applying successive gate voltage spikes (V_g=±20 V t_{on}=100 ms). (b) Schematic diagram displays the digit recognition process using CrossSim for the benchmark simulation. (c) Accuracy of handwritten digit recognition based on LTP/LTD processes.

4.4 Optoelectronic behaviors of the artificial synapse and visual memory function

4.4.1 Optoelectronic behaviors

For biological visual systems, image pre-processing is a fundamental property of the human retina, contributing to the high-efficiency image recognition tasks. Beyond electronic operation mode, to build a neuromorphic vision system, it is imperative to study the light-tunable synaptic plasticity for perception and memory functions.[201] Also, to overcome the disadvantage of conventional artificial photoreceptors, P(VDF-TrFE)/ReS_2 optoelectronic devices can reflect light-tunable PSC states and integrate image data recognition, storage, and pre-processing within one device configuration. Thereafter, this study focuses on examining the effects of illumination conditions on PSCs.

Initially, we achieve the transition from short-term memory (STM) to long-term memory (LTM) to modulate the synaptic weight of the optoelectronic synapse by varying the amplitude and width of the light pulses. Figure 4-12(a) and Figure 4-12(b) illustrate the PSC of the P(VDF-TrFE)/ReS_2 optoelectronic device under different light durations (dark, 0.5, 1, 2, and 3 s) and light intensities (dark, 0.8, 3.5, 5.3, and 8.4 $\mu W/cm^2$) at a wavelength of 450 nm. Under the small light intensity or short light duration, the PSC increases slightly and returns to the initial level after removing optical stimuli, resembling the STM of the human brain. With an increase of light intensity or light duration time, the PSC increases gradually and decays slowly and maintains at a

higher level above the initial state, which behaves like LTM. The light-tunable behaviors can be attributed to the photo response of channel material ReS_2. PSC originates from the photogenerated carriers under illumination and the slow decay process results from the PPC effect within ReS_2, which mimics the information transmission of biological neural function.[202] We also illustrates the variation in PSC decay speed for different gate voltages (Figure 4-12 (c)). The initial stage reduction is rapid, followed by a gradual carrier de-trapping process. Additionally, we compared the photocurrent generation for each gate voltage, as shown in Figure 4-12 (d). The photocurrent increased from -2 V to 2 V gate voltage. This can be attributed to the positive gate voltage attracting electrons at the interface between the channel and the dielectric layer after the generation of electron-hole pairs in ReS_2 through light illumination.

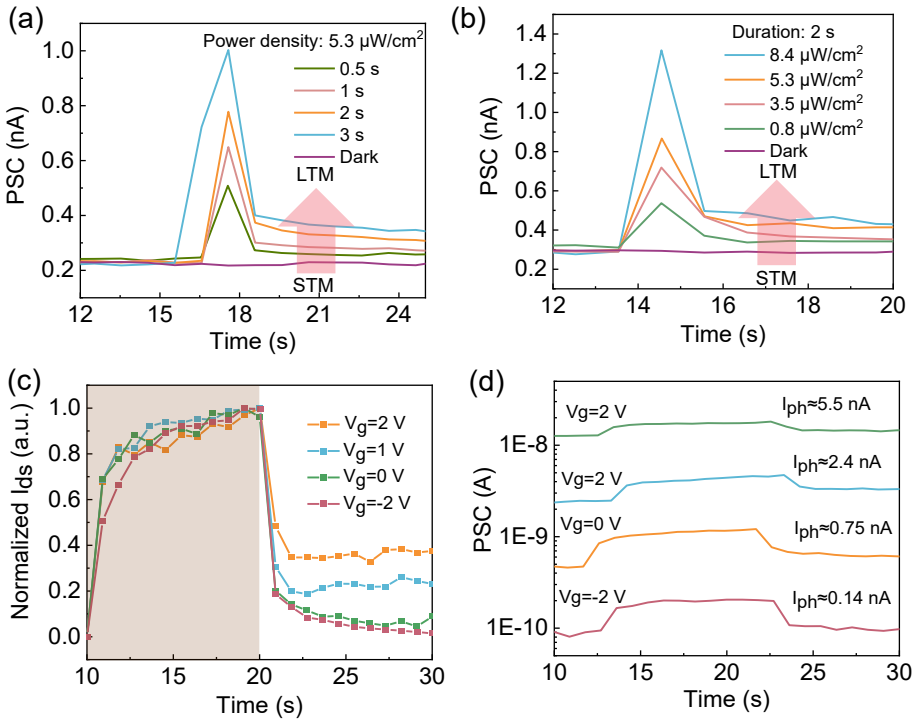


Figure 4-12: Dependent plasticity of synaptic devices in various duration time (a) and intensities (b) of light illumination under 0.1 V bias voltage. (c) Normalized photocurrent switching characteristics measured under various gate voltages with 450 nm light illumination at an intensity of 5.3 μW/cm^2 and a duration of 10 s. (d) Log-scale representation of the PSC measured under different gate voltages, along with a comparison of the photocurrents.

Specifically, the relaxation process after light removal is prolonged due to the localized effect of trap states such as sulfur vacancy in ReS_2.[203] We also implement density functional theory (DFT) calculations on defective ReS_2 models to further elucidate that trap states are in conjunction with the generation of S vacancy. The easily formed S vacancy and the related trap states are responsible for optoelectronic synaptic behaviors and more details are shown in Figure 4-13. Firstly, Figure 4-13(a) presents a comprehensive depiction of the atomic arrangement of both pristine monolayer ReS_2 and ReS_2 with a S vacancy. In the pristine atomic structure of monolayer ReS_2, six Re atoms form a proximity around the S atom. We conduct calculations to determine the formation energies of S vacancy in ReS_2. as shown in Figure 4-13(b). All the six cases show small formation energies of 1.89 eV~3.07 eV, indicating the formation of S vacancy in ReS_2 is energetically allowed. As shown in Figure 4-13(c), the pure ReS_2 monolayer is determined to possess semiconductor properties, exhibiting a direct energy gap of approximately 1.4 eV. The presence of S vacancy defect results in the generation of trap levels within the band structure (Figure 4-13(d)). According to their

relative positions to the fermi level, defect level 1 and 2 can be identified as the hole and electron trap states, respectively. Followed by the projected local density of states (Figure 4-13(e)) to distinguish the composition and to analyze the contribution source of these trap levels, we can confirm that the emergence of trap states is in conjunction with the generation of sulfur vacancy.

Such easy formations of S vacancy and the related trap states will benefit the photosensitive synaptic behaviors in the as-prepared P(VDF-TrFE)/ReS_2 devices. The mechanisms are schematically illustrated in Figure 4-13(f). Under light irradiation, the trap states effectively capture both electrons and holes. This enables additional thermal excitation processes, leading to extended lifetimes of the photogenerated carriers. These photoexcited carriers are responsible for the ultra-slow response, which aligns with the observed persistent photoconductivity effect phenomenon.

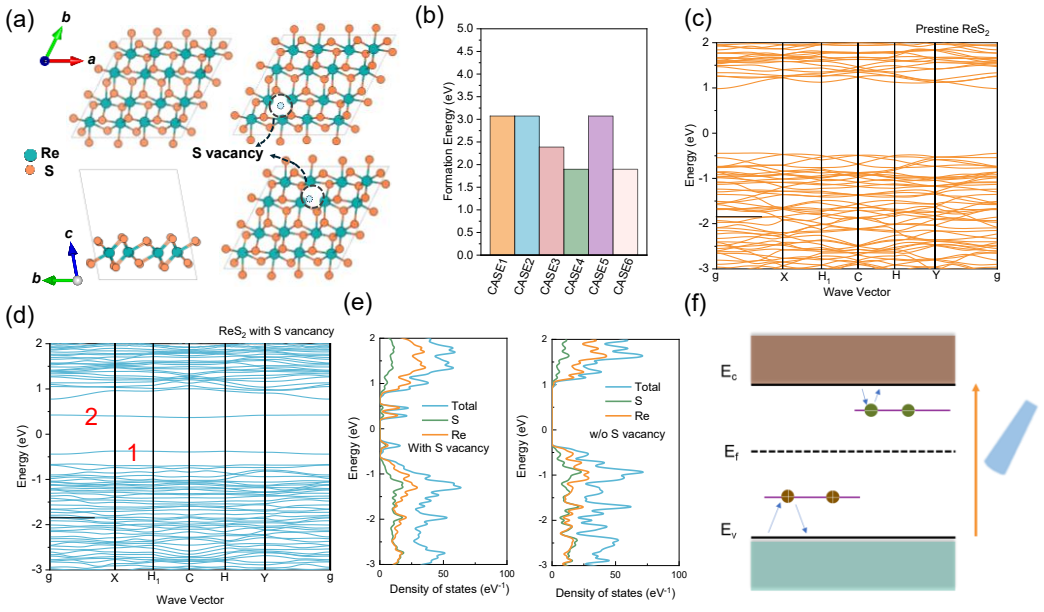


Figure 4-13: PPC effect analysis for ReS_2. (a) Atomic structure of pure monolayer

ReS_2 with and w/o S vacancy used in calculations. (b) DFT-calculated defect formation energies of S vacancies with six different configurations. The band structures of pristine monolayer ReS_2 (c) and ReS_2 with a S vacancy (d). The red numbers correspond to the two newly emerged trap levels that accompany the formation of the S vacancy defect. (e) Projected density of states of ReS_2 with and w/o S vacancy. (f) A schematic illustration featuring the involvement of trap states in semiconductor band structure.

4.4.2 Visual memory function

Moreover, the learning-forgetting-relearning process is also displayed based on P(VDF-TrFE)/ReS_2 optoelectronic devices by applying several continuous light pulses, as shown in Figure 4-14(a). On and off states of light pulses represent learning and forgetting processes, respectively. The PSC is increased during light stimulation and decays to an intermediate state after removal of optical source. Such decay signifies a slight forgetting of the acquired information within a short interval of time. The next optical stimulation represents the relearning process, and the PSC after the second pulse surpasses the initial value, indicating the consolidation of earlier information through the repeated learning process. Following all the optical stimuli, the PSC exhibits good repeatability and reaches maximum level. The current after the light irradiation can be used to demonstrate human visual forgetting curve, which approximates the exponential law[204] and the decay rate or memory duration can be modulated by different light intensities. Detailed memory retention ratio and its fitting curve can be found in Figure

4-14(b). We present the time-resolved response of the PSC under two different light intensities, namely 3.5 and 5.3 μW/cm², and notably stronger stimuli yields a larger PSC, suggesting a higher degree of learning. Also, the decay processes stimulated by light pulses can be fitted well through the double exponential decay function, as shown in Eq (4-3)[45]:

$$I = C_0 + C_1 exp\left(-\frac{x - x_0}{\tau_1}\right) + C_2 exp\left(-\frac{x - x_0}{\tau_2}\right) \qquad (4-3)$$

Regarding the relaxation time parameters, the time constants τ_1 and τ_2 correspond to two distinct decay mechanisms: rapid direct recombination and gradual carrier de-trapping, respectively. Among these processes, the slow decay characterized by time constant τ_2 significantly influences the duration of memory storage.[205] As illustrated in Figure 4-14(b), the decay curves of current retention under two different light intensities of 3.5 and 5.3 μW/cm^2, conform to the diagram presented in Figure 4-14(a). The retention decay curves are fitted using Eq (4-3). With an increase in light intensity from 3.5 to 5.3 μW/cm^2, the decay time constant τ_2 exhibits an increment from 20.86 to 25.73 s. These results suggest that photogenerated carriers accumulated in ReS_2 possess a relatively long lifetime, thus facilitating long-term visual memory behavior through the application of multiple optical pulses.[203] The entire process is accordance with the human memory model,[206] as shown in Figure 4-14(c) The process of information memorization can be divided into three stages: sensory memory in the short term can be transformed into STM after learning; through repeated cycles of training, forgetting, and relearning, this information can eventually be consolidated into LTM.

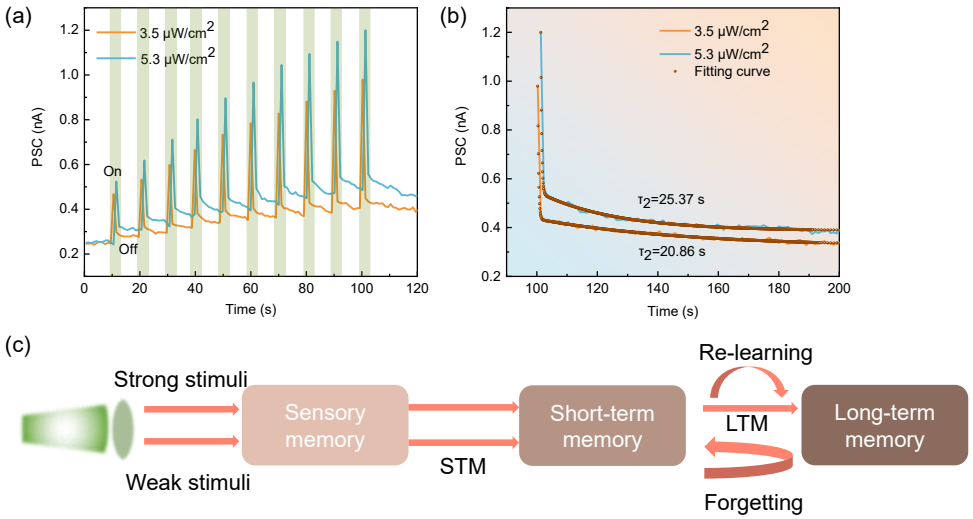


Figure 4-14: Learning–forgetting–relearning procedure simulation. (a) Light-tunable behaviors by ten consecutive light spikes under two different light intensities of 3.5 and 5.3 μW/ cm^2 with 5% duty cycle. The bias voltage is kept at 0.1 V. (b) The current retention decay curves under two different light intensity. (c) The learning–forgetting–relearning procedure based on the above continuous optical stimulations.

4.4.3 Visual information recognition

Interestingly, the PSC can be modulated by optical pulse number and increases gradually with the number of stimuli. Likewise, under continuous visual stimulation, our human visual system will implement image recognition and discrimination.[207] To simulate such biological activity, an optoelectronic synaptic array is designed based on the features of a single device which will receive different numbers of optical stimuli. The data acquired from device measurements are extended to array simulations, assuming that the sensing terminal represents an ideal uniform array composed of P(VDF-TrFE)/ReS_2 optoelectronic synaptic devices. Figure 4-15(a) illustrates different

numbers of optical pulses (1 s, 3.5 μW/cm²) applied to the optoelectronic device, forming a visual signal for target object "4". By applying more pulses, the synaptic strength of the device is enhanced according to the time-resolved measurements (Figure 4-15(b)). The time-resolved current curves are presented under various numbers of light pulses, where each optical pulse featured with a duration of 1 s and an interval of 1 s. The light intensity used is 5.3 μW/cm^2. It is observed that repetitive stimulation leads to a continuous increase in synaptic strength, facilitating the transition from short-term memory to long-term memory. Consequently, the investigation of LTP characteristics in neural morphological devices under the optical operation mode can be conducted by applying continuous multi-pulse stimulation.

The peak value of the PSC is normalized from 0 to 1. As shown in the 10×10 optoelectronic device array, the shape of the "4" object is difficult to distinguish from the background after the first optical pulse, indicating a relatively weak optical response at this stage. Based on the increased current response to more optical pulses, the demonstrated neuromorphic phototransistor exhibits capabilities in image recognition and memorization. Therefore, the synaptic weights and image contrast can be strengthened with an increasing number of optical pulses, bringing with a clearer representation of the object feature "4" through this image perceptual learning process. To identify the feature maps, an ANN is constructed with 784 input neurons, 200 hidden neurons, and 10 output neurons. Figure 4-15(c) demonstrates a gradual enhancement in the probability of image recognition for the digit "4" as the number of optical pulses

increases. Ultimately, it reaches a saturation point, indicating the transition from being indistinguishable to visible. This application confirms the effectiveness of the neuromorphic visual system in performing image recognition tasks, including enhancing contrast and storing visual information at the sensing stage.[208-209]

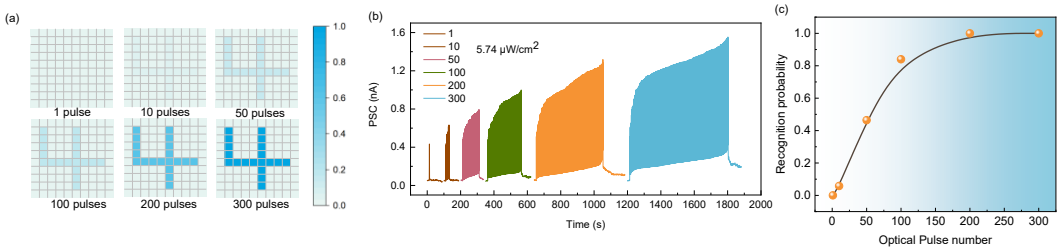


Figure 4-15: Optoelectronic synaptic array for image pre-processing and recognition. (a) The digit '4' is mapped to the 10×10 array by applying a different number of light stimuli to implement the image recognition task. (b) PSC response during multi-pulse stimulation. (c) Image recognition probability results with the change of light spike numbers.

We further use two optical intensities to capture light and shade from different objects. Taking the light bulb as an example (Figure 4-16), different optical intensities of 5.74 and 9.11 μW/cm² are used to modulate the outline of the light bulb and the light emitted from it, respectively. When a greater number of optical pulses are inputted into the neuromorphic visual array system for light bulb and illumination recognition, both shapes can be distinguished due to the memory capability. The bulb shape and light illumination correspond to different optical spike intensities of 5.74 μW/cm^2 and 9.11 μW/cm^2, respectively. The background units are normalized to 0, and the peak value of the EPSC from higher optical intensity is normalized to 1. As the number of optical

stimuli increases, the PSC associated with the light bulb and illumination area progressively increases, resulting in clearer object features. This enhancement is achieved through the LTP behavior of the optoelectronic device, in which the weak signals are amplified via perceptual learning within the sensing platform of the device array.

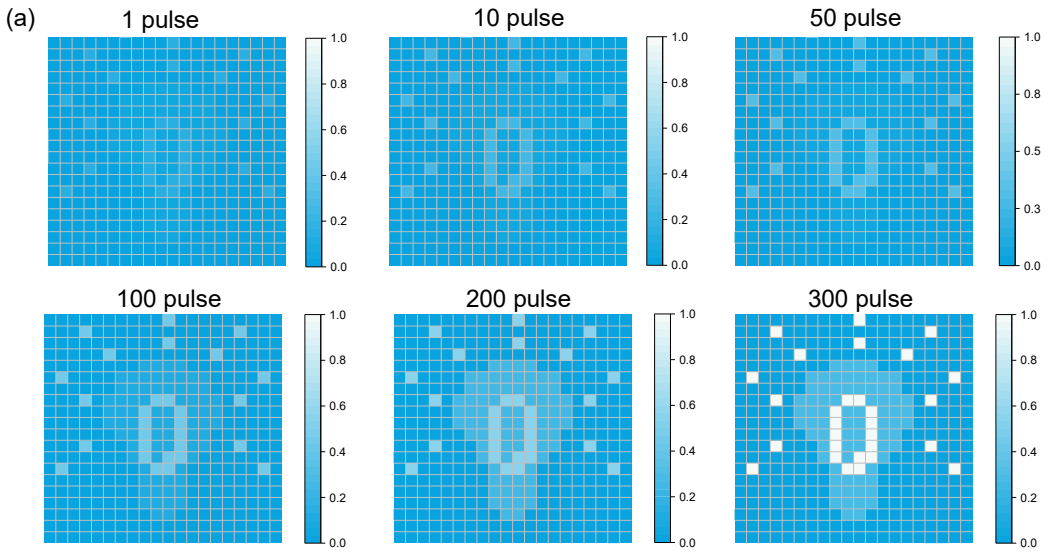


Figure 4-16: The contrast enhancement and memory process of the light bulb shape and light illumination under various numbers of input pulses.

4.5 Simulations of information extraction based on the optoelectronic array

To achieve a versatile neuromorphic visual processing platform, in addition to perceptual learning and image recognition based on a single wavelength, we also apply the optoelectronic device array to demonstrate complicated functions of multi-wavelength information extraction and surrounding noise signal reduction simultaneously.

The light-induced current is analyzed based on different wavelengths, as illustrated

in Figure 4-17(a). Three specific wavelengths, namely 450 nm, 530 nm, and 650 nm are employed, which correspond to the primary colors of blue, green, and red. These wavelengths are used to stimulate the optoelectronic devices at a fixed optical intensity of 5.3 μW/cm^2 and a constant pulse duration of 1 s. The PSC gradually increases as the wavelengths transition from 650 nm to 450 nm. This finding suggests that the wavelength-dependent photo response displays a high sensitivity to blue source illumination. We further investigate the light-induced conductance states under different pulse numbers with three wavelengths (Figure 4-17(b)). As light pulses number increases, the conductance of blue illumination become much higher and pronounced compared to green or red sources.

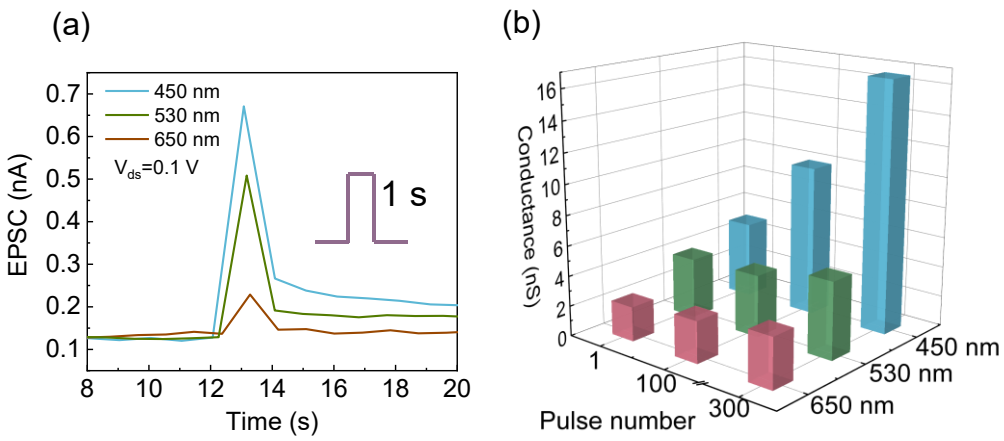


Figure 4-17: EPSC variation under various different wavelengths. (a) The time-dependent variation of EPSC is examined under a single optical pulse with various light wavelengths. The optical pulse possesses a power density of 5.3 μW/cm^2 and a duration lasting 1 second. (b) 3D histogram image of the conductance states as a function of pulse number under three wavelengths.

By leveraging the wavelength-sensing capabilities for blue light and the heightened

sensitivity achieved through increasing the number of optical pulses, the proposed visual sensor array has the potential to effectively extract blue information. As shown in Figure 4-18, the background section, the outline of the trophy, and the digit on the trophy are corresponded to the red, green, and blue colors in the original image. The relationship between optical wavelength and its position in the 20×20 optoelectronic device array is defined based on the original image. Each optoelectronic device in the array is assumed to be illuminated with three different pulse numbers according to above relationship. Optical-induced EPSCs are extracted from experimental results involving 1 pulse, 100 pulses, and 300 pulses. Additionally, the normally distributed noise signals are taken into consideration for image pre-processing. All the current responses and the undesired signals are normalized from 0 to 1 in each optoelectronic array mapping. With an increase in the number of pulses, the blue number on the trophy becomes more prominent, aligning with the above experimental results, while the noise signals become less noticeable. The finding suggests that by increasing the pulse number, the distinction between the blue features and other features can be intensified and the optoelectronic sensor array can effectively recognize blue targets while minimizing signals from other sources. Similar to the visual cortex, it records information that is crucial for brain while suppressing irrelevant parts or noises.[181]

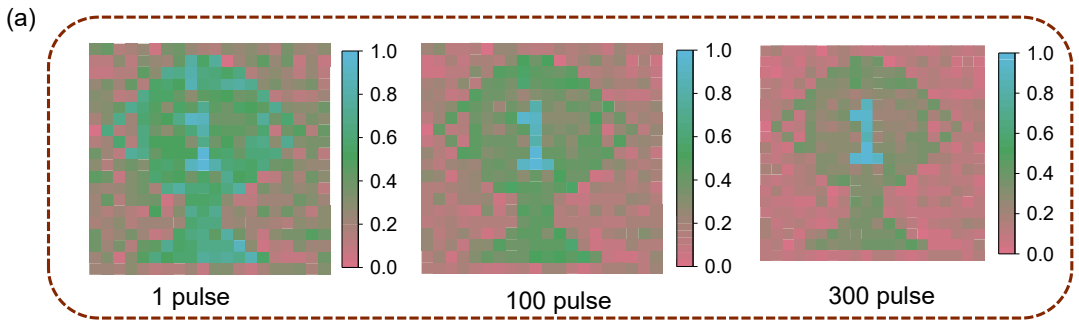


Figure 4-18: The information extraction and noise reduction processes with optical spikes number enhancement.

To explore the concept of bio-vision-inspired neuromorphic computation, a simulated visual system has been developed. This system includes the demonstrated neuromorphic vision sensor array and an ANN. After the outline of the blue digit on the trophy becomes highlighted while the background noise signals are depressed through the optoelectronic array. The preprocessed image is subsequently fed into the neural network for image training and recognition, as shown in Figure 4-19(a). Figure 4-19(b) illustrates the recognition rate of neuromorphic visual systems while considering noises. In the initial state, noticeable differences in recognition accuracy are observed among the three optical pulse settings. For one optical pulse illumination, the image recognition accuracy after 40 epochs is merely 72%, indicating that the network struggles to identify critical information displayed on the trophy due to surrounding interference. However, through image pre-processing via the optoelectronic array, the recognition rate significantly improves to 95% and 96% for 100 optical pulses and 300 optical pulses, respectively, after 40 training epochs. It is imperative to acknowledge that the acquisition of 300 pulses requires a considerable amount of time. However, it

is noteworthy that the precision attained with 100 pulses at an approximate 95% accuracy level is comparable to that achieved with 300 pulses, while requiring a significantly shorter duration. Therefore, the redundant signals have been reduced dramatically and previously unrecognizable information can be accurately extracted by our neuromorphic vision system in conjunction with the neural network.

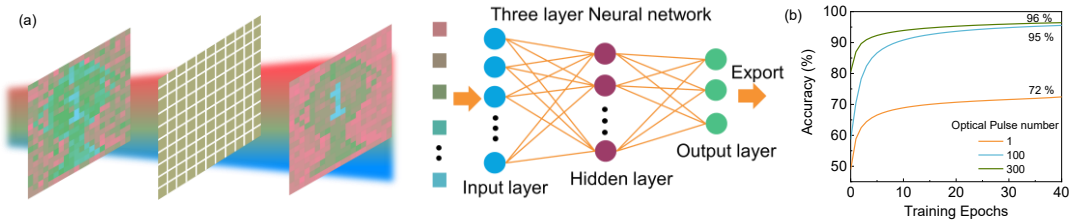


Figure 4-19: image recognition process under the different optical pulse settings. (a) Scheme of the image recognition using ANN. (b) Comparisons of the image recognition rate for the three optical pulse settings

4.6 Conclusion

To sum up, an artificial optoelectronic synaptic device based on P(VDF-TrFE)/ReS_2 has been successfully designed that can act as a sensory component to electrical and optical stimuli and emulate versatile biological behaviors through ferroelectric nonvolatile switching effect. The optical synapses array, with its light-tunable plasticity, allows for the implementation of learning processes including image recognition and contrast enhancement. Furthermore, the entire array can be utilized for multi-wavelength recognition in noisy environments, facilitating the information extraction while reducing noise signals. To address concerns regarding hardware and power consumption, we have constructed a neural network integrating the proposed

optoelectronic devices array. Through the redundant information reduction and the target extraction processes, the image pre-processing efficiency has increased from 72% to 96%. With these multifunctional features, this work inspires highly integrated neuromorphic systems and the development of wavelength-selective artificial visual platforms. Our study underscores the advantages of utilizing ferroelectric optoelectronic synapses in artificial visual platforms, as they offer simplified device structures and expedite the advancement of in-sensor neuromorphic computation.

Chapter 5 Object motion detection enabled by neuromorphic vision sensor

5.1 Introduction

Static image pre-processing, encompassing tasks such as noise reduction, brightness enhancement, and recognition, has been extensively demonstrated in diverse vision architectures.[51-52, 181, 210-211] In contrast, the domain of object motion detection (OMD) has emerged as a critical and burgeoning necessity across various applications, such as health monitoring, virtual reality, and intelligent transportation systems.[212-213] Conventional motion detection architectures based on dynamic vision system separate the sensor, memory, and computational units, resulting in substantial volumes of redundant data and high power consumption.[107-109] Increasing demand for object motion detection (OMD) requires shift of reducing redundancy, heightened power efficiency, and precise programming capabilities to ensure consistency and accuracy. The human retina possesses an inherent ability to efficiently perceive and process dynamic information at sensory stage.[157] This unique characteristic enables the reduction of data volume and minimizes power consumption, thereby boosting the efficiency of information processing.[214-215]

Neuromorphic vision sensors, drawing inspiration from the biological nervous system, have been developed to replicate human visual perception.[216-217] In the context of interference and learning applications, neural networks with high accuracy and energy efficiency play a pivotal role.[199, 218] The highly linear synaptic weights with

multiple distinguishable levels and excellent symmetry significantly impact the uniformity and accuracy of the vision sensor system. Above features have become fundamental requirements for specialized tasks such as image recognition, autonomous driving, and virtual reality motion learning.[219] Simultaneously, enhancing overall energy efficiency and establishing self-powered systems are essential for visual sensors.[220] By reducing power requirements, devices can operate seamlessly and continuously, which is particularly valuable for applications demanding long-term monitoring and perception. Additionally, neuromorphic visions sensor exhibits promising potential in various portable hardware applications, where minimizing power consumption effectively mitigates heat dissipation concerns. However, it remains a challenge to develop a visual sensor for motion detection that encompasses above advantages, including eliminating data redundancy, possessing discrete and stable multi-synaptic weights levels, and reducing power consumption. In this regard, the integration of two-dimensional (2D) materials with ferroelectrics holds tremendous promise.[221] The unique characteristic of ferroelectric gates, stemming from the presence of multiple intermediate levels between the fully "up" and "down" states, enables versatile regulation. This distinctive attribute facilitates precise control over doping degree and reversible modulation of atomically thin 2D materials.[27] Such approach enhances the flexibility and tunability in accurately programming neuromorphic devices to achieve ultra-linear and discrete multiple weights, offsetting the less-controllable methods and unpredictable fluctuation limitations associated with

vacancy migration and ion transport mechanisms.[222-224] Especially, in the reconfigurable architecture, the diverse local switching behaviors introduce additional dimensions for optoelectronic applications. Furthermore, utilization of ferroelectric modulation provides a promising alternative for low power consumption, eliminating the need for continuous external stimuli, and ensuring nonvolatile property.[225]

Therefore, we demonstrate a reconfigurable neuromorphic device based on ambipolar tungsten di-selenide (WSe_2)[174] and a ferroelectric copolymer poly(vinylidene fluoride) and trifluoroethylene (P(VDF-TrFE)). Opposite ferroelectric polarization from separated switching areas enables the precise and nonvolatile control of the PN and NP junctions in WSe_2, bringing with two signs of self-powered photocurrents. After progressively programming intermediate ferroelectric states, multiple bidirectional photocurrents of more than 6 bits resolution can be used for synaptic weights updating. Notably, such synaptic behaviors exhibit symmetricity, reversibility, high linearity for each cycle ($R^2 \approx 0.999$), and uniform step (≈ 6 pA) between each state, all of which provide stable foundation for accurate motion detection and computation.[226] By counteracting the symmetric bidirectional photocurrents, we can simulate the object motion sensitive function of ganglion cells in the retina.[165] Furthermore, we have fabricated a uniform motion sensor array to demonstrate scalability for future large-scale integration. Subsequently, the detected motion information is accurately recognized through an artificial neural network (ANN), achieving accuracy of 96.8%. Consequently, neuromorphic vision sensor seamlessly

integrates optical sensing, energy-efficient architecture, ultra-linear weights, and motion detection computation. Our work provides a promising solution for the advanced motion detection system.

5.2 OMD function illustration

The human visual system possesses the remarkable ability to accurately perceive motion and action, enabling high-speed responses in complex and uncertain surroundings.[227] In Figure 5-1(a), we illustrate the implementation of local motion detection, which relies on the intricate cellular structure of the human retina. Within the retina, bipolar cells act as integrative centers, receiving input from both upstream photoreceptor cells (rods and cones) as well as lateral amacrine cells. The amacrine cells contribute to the creation of center-surround antagonism, a contextual effect that modulates the activity of ganglion cells.[228] Notably, these ganglion cells exhibit selective responsiveness to differential motion, conveying information to the visual cortex through the optic nerve. Specifically, these cells remain inactive in response to self-induced motion, such as eye movements, but display robust firing when there is motion relative to the global background (Figure 5-1(b)).[229] These properties enable us to discern authentic motion from static scene, thereby increasing information analysis and computation efficiency.

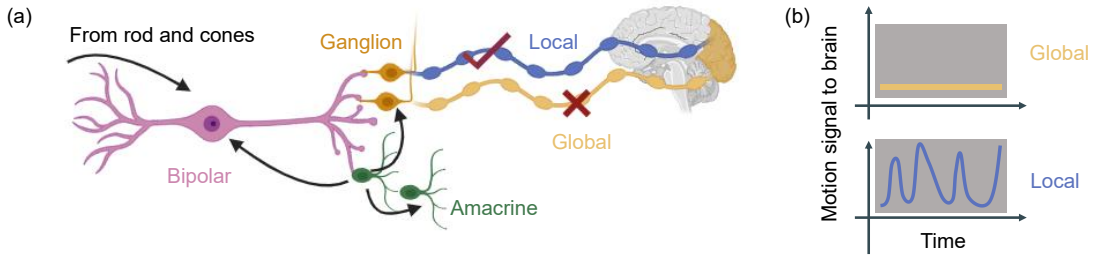


Figure 5-1: Sectional retina structure and its motion detection mechanism. (a) A schematic representation of a partial human retina, emphasizing the bipolar, amacrine, and ganglion cells while illustrating distinct responses to local and global information for motion detection (b).

Drawing inspiration from the human retina, we propose an OMD with bipolar photocurrent characteristics. Figure 5-2(a) illustrates the integration of ferroelectric and 2D materials within a neuromorphic vision sensor. By polarizing the ferroelectric gate dielectric in opposite directions through distinct pulses, the formation of PN and NP junctions is achieved under zero bias voltage for high energy efficiency. When subjected to optical illumination, self-powered positive and negative photocurrents are generated. These versatile intermediate photocurrent states enable the realization of LTP and LTD processes, exhibiting nonvolatile characteristics. Furthermore, the neuromorphic vision sensor can be fabricated into sensor arrays to facilitate large-scale integration. By leveraging inter-frame difference computations[230], moving subjects can be detected from sequential frames based on brightness differences while eliminating the static or global part with fixed brightness (Figure 5-2(b)). Thus, a single neuromorphic vision sensor transistor can perform multiple functions, including sensing optical stimuli, converting them into multi-levels electrical signals, and ultimately executing OMD processing analogous to the specialized ganglion cells.

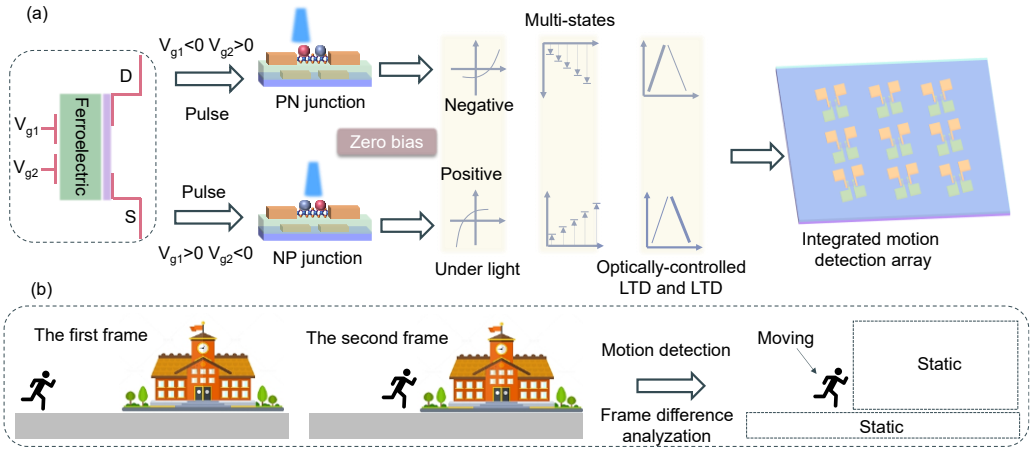


Figure 5-2: Neuromorphic vision sensor and its OMD functionality. (a) Neuromorphic vision sensor with PN and NP configurations, facilitating the generation of nonvolatile and intermediate negative and positive photocurrents. (d) Illustration of OMD functionality, emphasizing moving object while eliminating the static information.

5.3 Reconfigurable transistors under ferroelectric modulation

5.3.1 Device fabrication and materials characterization

Figure 5-3 displays a three-dimensional ferroelectric-modulated WSe_2 reconfigurable transistor. WSe_2 is selected as the channel semiconductor due to the intrinsic ambipolar property, efficient carrier tunability, and robust light-matter coupling and absorption with approximate bandgap range of 1.35-1.64 eV, changing with the films thickness.[231-234] These inherent characteristics contribute to the effective modulation of carrier within the WSe_2 channel through ferroelectric polarization. Moreover, the utilization of a stable organic ferroelectric material, namely P(VDF-TrFE), as the gate dielectric ensures low-temperature annealing while enabling

compatibility with the back-end-of-line regime.[27, 182, 235]

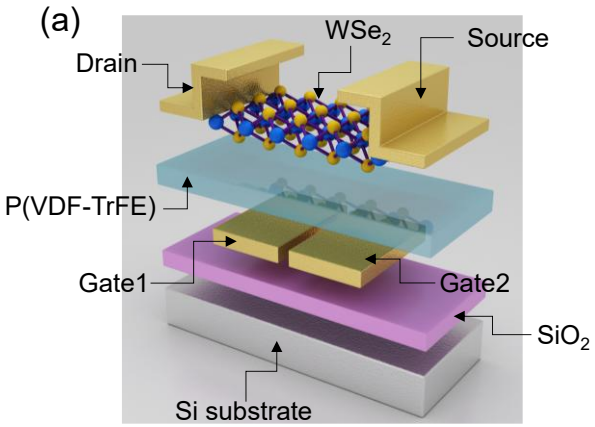


Figure 5-3: A three-dimensional image of the WSe_2/P(VDF-TrFE) transistor.

Figure 5-4 (a) and (b) provide the Raman spectra and thickness characterization of WSe_2, respectively. The most prominent peak arises from the superposition of two nearly degenerate vibrational modes, namely the E_{2g} and A_{1g} modes, with a frequency of approximately 248 cm^{-1}. Additionally, a spectral feature at around 257 cm^{-1} is attributed to a second-order peak resulting from a double resonance effect, specifically assigned as 2LA (M). This effect involves the longitudinal acoustic phonon at the M point in the Brillouin zone.[236] The out-of-plane B_{2g} mode is located at approximately 307 cm^{-1}.The ferroelectric nature of P(VDF-TrFE) is verified through piezo-response force mode (PFM) methods and polarization-electric field hysteresis, as depicted in Figure 5-4 (c) and (d).

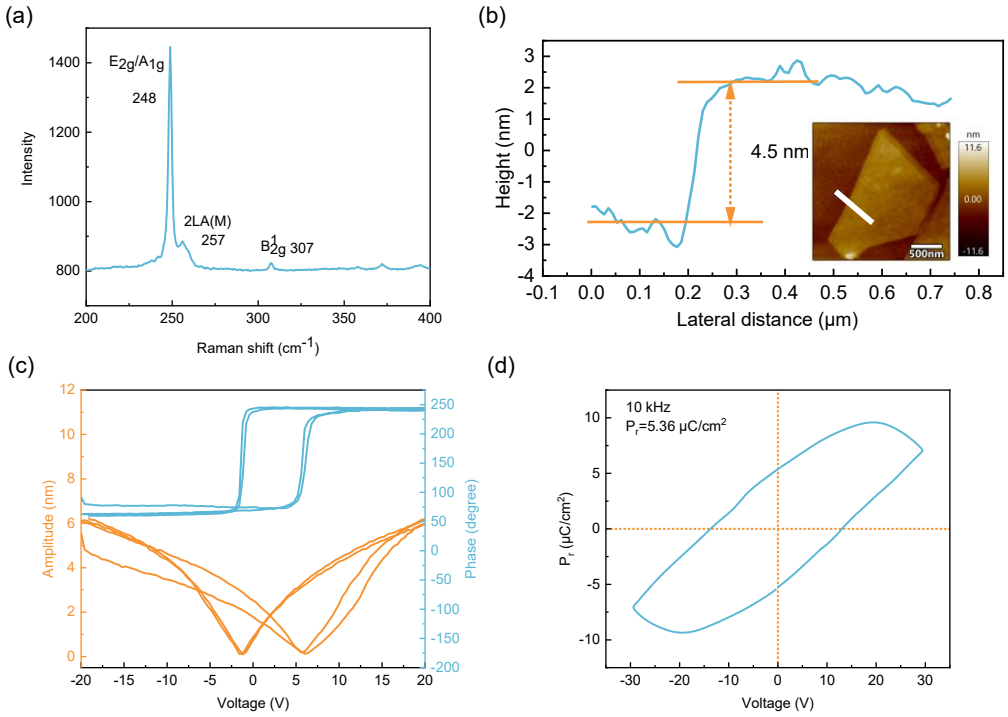


Figure 5-4: Characterization of WSe_2 and P(VDF-TrFE). (a) The Raman spectra of WSe_2. (b) The line profile analysis of the WSe_2 film thickness along the white line, as indicated in the inset of the surface topography AFM image. The analysis reveals an approximate thickness of 4.5 nm for the WSe_2 film. (c) The phase and amplitude hysteresis loops of P(VDF-TrFE) obtained through PFM. (d) The polarization-electric field (P-E) hysteresis curve of a P(VDF-TrFE) ferroelectric capacitor with Au electrodes at the top and bottom.

Next, we will explain the experiment process. Initially, SiO_2/Si substrates covered by photoresist undergo the ultraviolet photolithography process to pre-pattern two split gates. Subsequently, 10 nm Cr/50 nm Au electrodes are deposited onto the substrates using thermal evaporation, followed by a lift-off process in an acetone solution. The dielectric layers, consisting of P(VDF-TrFE) (70:30 in mol %) thin films with a

thickness of approximately 300 nm, are formed through spin-coating. These layers are then annealed at 135 ℃ for four hours. Few-layered WSe_2 flakes are obtained by mechanically exfoliating them from a bulk single crystal (purchased from HQ Graphene). Desired WSe_2 flakes are identified on a PDMS substrate and transferred onto the surface of the P(VDF-TrFE) layers using a 2D Transfer system. Finally, paired electrodes of 50 nm Au, serving as the source and drain electrodes, are transferred and aligned onto the WSe_2 channel. Figure 5-5 illustrates the process flow chart.

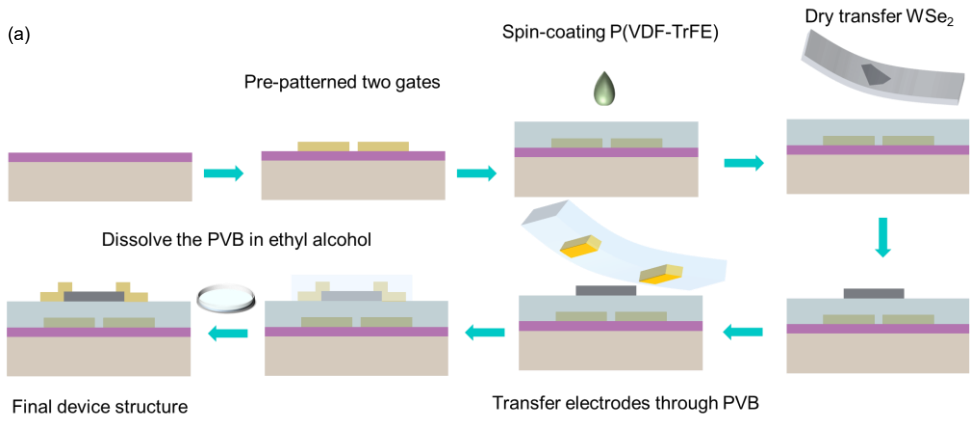


Figure 5-5: A detailed depiction of the device fabrication process, elucidating the sequential steps involved in its construction.

5.3.2 Reconfigurable demonstration

By employing two separated gates of Gate 1 and Gate 2, positioned beneath the P(VDF-TrFE) layer, independent ferroelectric domains are formed. Figure 5-6(a) illustrates the application of equal local gate voltages exceeding the ferroelectric coercive fields to induce fully polarization in the two distinct regions. In this regard, the WSe_2 device functions as a typical ferroelectric field-effect transistor, exhibiting symmetric ferroelectric hysteresis. Under the polarization up (P_{up}) or down (P_{down})

states, electrons and holes can be accumulated within the WSe_2 channel. The optical image of the device is provided as an inset to offer a visual representation. This configuration effectively exhibits the ambipolar nature of WSe_2, as evidenced by distinct anticlockwise and clockwise hysteresis loops observed for the n-type and p-type branches, respectively.[237] Furthermore, the near-equal magnitude and similar characteristics of the positive and negative ferroelectric switching currents (I_g) obtained from both gates, as depicted in Figure 5-6(b), serve as indicator of a small imprint field.[238] These findings validate the high quality of the P(VDF-TrFE) copolymers and the favorable interface between the P(VDF-TrFE) and WSe_2, thereby contributing to the enhanced photovoltaic performance.[239]

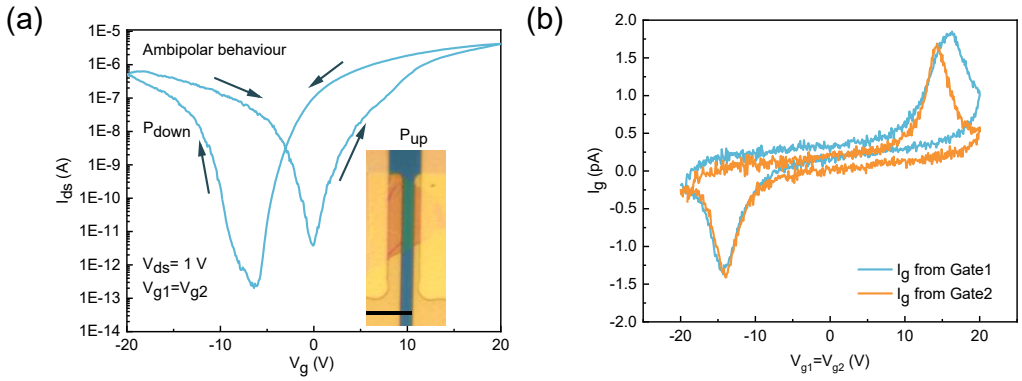


Figure 5-6: Typical transfer curve for WSe_2/P(VDF-TrFE) and the ferroelectric switching currents. (a) The transfer curve under equivalent gate voltages for the two gates. The inset displays a real optical image of the WSe_2/P(VDF-TrFE) device, providing a scale bar of 10 μm. (b) The ferroelectric switching currents (I_g) obtained from the two gate terminals.

In the asymmetric or unipolar mode, as illustrated in Figure 5-7(a-b), the ferroelectric

device exhibits behavior of an individual p-type or n-type transfer curve. By fixing one of the two gates and sweeping the other gate terminal, a clockwise or anticlockwise hysteresis is observed under a fully P_{down} or P_{up} state, respectively. These transfer curves, obtained under different gate setting modes, provide evidence of a high on-off ratio surpassing 10^7 and a large memory window exceeding 10 V. The obtained transfer curves not only demonstrate the potential for achieving high-performance applications but also emphasize the advanced capabilities of the ferroelectric-modulated WSe_2 transistor for memory and logic devices in various technological domains.[240-241]

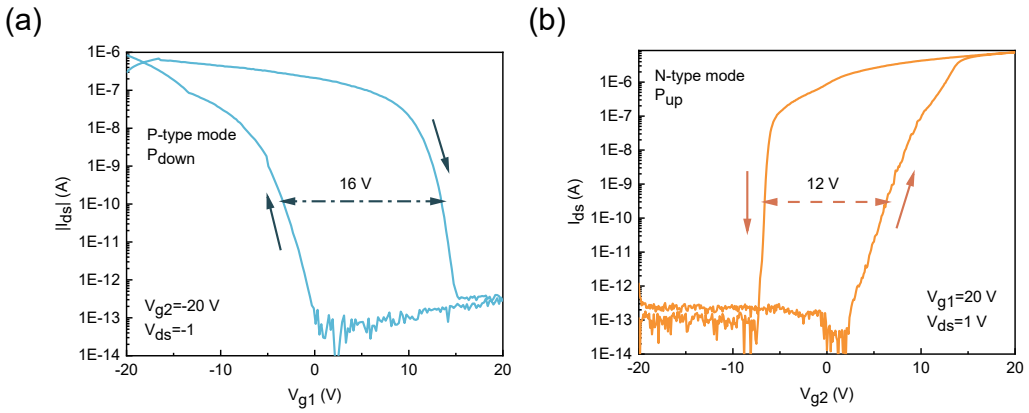


Figure 5-7: The ferroelectric hysteresis loops are depicted for the operation of the WSe_2/P(VDF-TrFE) device in both p-type (a) and n-type (b) modes.

Furthermore, the WSe_2/P(VDF-TrFE) transistors possess four distinct output curves by independently defining the two gates as depicted in Fig 5-8(a). Specifically, when opposite gate pulses (±20 V, 1 ms) are applied to the two gates, the device exhibits remarkable characteristics of NP and PN junctions during the reading process, with the bias voltage sweeping from -1.5 V to 1.5 V and the gates pulses subsequently removed. These characteristics include an impressive rectification ratio exceeding 10^3 and an

insignificant reverse current of less than 6 pA (V_{ds}=±1.5 V), which are in line with findings reported in prior studies.[242-243] Moreover, the gated regions within the WSe_2 channel can be precisely tuned to exhibit either NN or PP states, yielding quasi-linear characteristics when both gates are set to equal. Fig 5-8(b) depicts a detailed understanding of the working mechanism underlying these four configurations. This switching process results in the establishment of an internal electric field within the PN or NP junction. Conversely, when gate 1 and 2 are set to the same voltage level, the ferroelectric-induced built-in electric field diminishes to zero, leading to the formation of NN or PP states. Consequently, the independent tunability of the split gates enables the attainment of four distinct configurations.

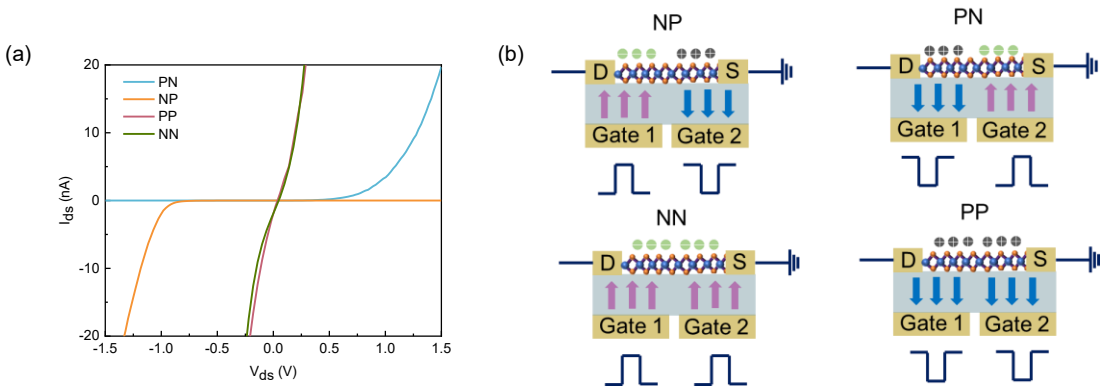


Figure 5-8: Four configurations for WSe_2/P(VDF-TrFE) devices. (a) The output curves correspond to the four configurations, showcasing the device's response under different settings. P(VDF-TrFE) is polarized using ±20 V gate voltages. (b) The utilization of different voltage values applied to the split gates, enabling complete switching of the ferroelectric domains in opposing directions.

5.4 Programmable WSe_2/P(VDF-TrFE) homojunction

5.4.1 Ferroelectric modulation for WSe_2/P(VDF-TrFE) homojunction

Through the phase images under versatile polarization conditions, we can obtain an investigation of intermediate ferroelectric polarization states. Figure 5-9(a) illustrates such process, highlighting the emergence of ferroelectric-modulated multi-states during the transition from a complete NP junction (1) to a PN junction (6). Initially, the ferroelectric domains are fully polarized, resulting in the formation of an NP state characterized by a -180° downward/upward phase difference, as depicted in the PFM phase image (1) of Figure 5-9. The P(VDF-TrFE) domains can also be manipulated to a mixed configuration with a neutral phase difference in the absence of applied voltages, depicted (2) in Figure 5-9. Through the gradual application of opposite voltage with NP state, ferroelectric domain undergoes a reversed switching process, as illustrated in (3)-(5) of Figure 5-9. Eventually, a fully polarized PN junction is achieved, and phase difference becomes 180°, as exemplified in (6) of Fig. 3(a). Figure 5-9 (b-g) depicts a more detailed understanding of the gate voltage operation and the corresponding phase differences. The results obtained from PFM analysis demonstrate that by applying opposite gate voltage pulses with the same absolute amplitudes to the two gates, the ferroelectric polarization areas can be effectively switched to reduce the original built-in electric field and reform an opposite built-in electric field. This allows for the subtle tuning of PN and NP junctions.

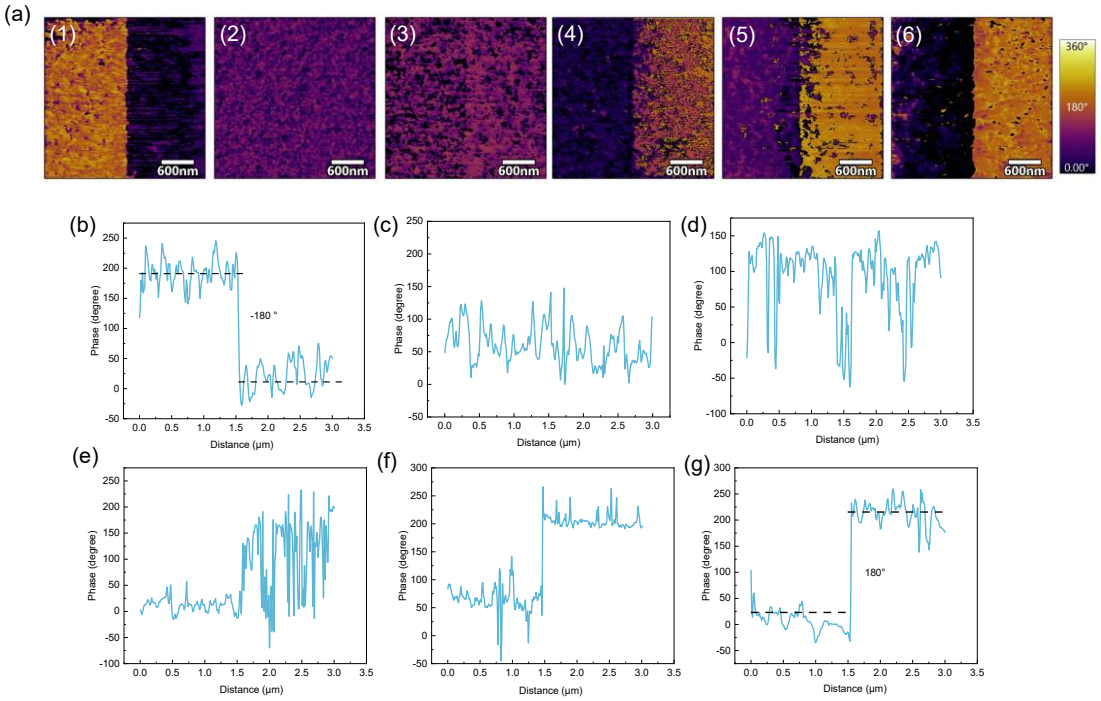


Figure 5-9: PFM phase image and corresponding phase difference transition. (a)PFM phase images depict the gradual transformation of homojunctions from NP to PN through ferroelectric polarization modulation. Phase difference during the ferroelectric domain flipping process. In this case, Gate 1 is chosen as an illustrative example, while Gate 2 is set to its opposite values. Figure (b) to (g) represent the corresponding gate voltages of -15 V, 0 V, 5 V, 7 V, 10 V, and 15 V to Gate 1, respectively.

5.4.2 Electronic configurations

From an electrical configuration standpoint, the gradual accumulation of electrons and holes occurs during the formation processes of the built-in field, and these charges are retained even after the removal of gate voltage operations. The dynamic process of such phenomenon is visually represented in Figure 5-10(a) and (b). During the

progressive polarization process induced by the application of enhanced gate voltage pulse amplitudes, the absolute channel current of both the PN and NP junctions exhibits a gradual increase. This behavior is clearly observed in the continuous rise of the source-drain currents, extracted at V_{ds}=1.5 V and depicted in Figure 5-10(c) and (d). Remarkably, this analog current modulation behavior highlights the ability to finely control and manipulate the device's performance. Importantly, during the read process, the gate pulses are removed due to the nonvolatile property of the device. This nonvolatility ensures that the stored charges and the resulting current remain stable and persistent, even in the absence of external gate voltage operations.

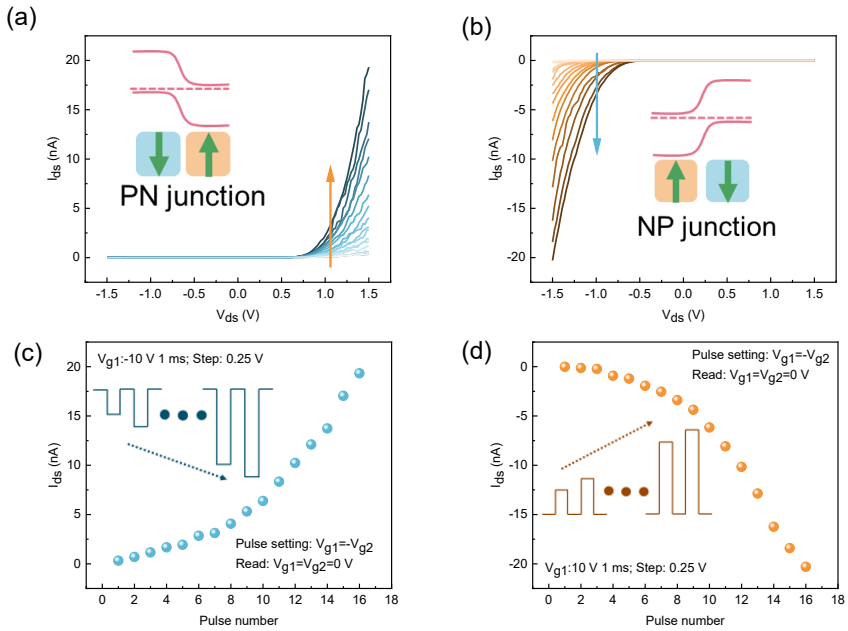


Figure 5-10: Analog current modulation behavior of WSe_2/P(VDF-TrFE). The output curves for PN (a) and NP (b) junctions, demonstrating the response of the devices under increased magnitude gate voltage pulses. Inset: illustration of band diagram under PN and NP homojunctions. The continuous changes in source-drain

currents as a function of gate voltage pulses at Vds=±1.5 are illustrated for PN (c) and NP (d). The specific gate voltage conditions are initiated at opposite 10 V and -10 V with a step of 0.25 V for PN and NP junctions, respectively, and then defined as zero during the read process.

Under the illumination of 450 nm light with increasing power intensity, the PN and NP photodiodes exhibit remarkable short-circuit photocurrents (I_{sc}), which illustrate a proportional relationship with the light intensity, as depicted in Figure 5-11(a). This photocurrent generation originates from the p-n junction and can be attributed to the photovoltaic effect.[244-246] Specifically, when the device is illuminated, the light-sensitive WSe_2 layer generates photogenerated electron-hole pairs, and these pairs are efficiently separated by the built-in electric field of the homojunctions. As a result, a self-driven I_{sc} is induced under zero bias voltage, demonstrating high power efficiency. It is noteworthy that the magnitudes of the photocurrents in the PN and NP junctions are nearly equal. This balanced response is crucial for the functionality of OMD, as it ensures consistent and reliable performance. Further discussion will be provided later in the paper. Furthermore, Figure 5-11(b) suggests a linear relationship between the I_{sc} and the input power intensity for both the PN and NP photodiodes. This linear response signifies a consistent and stable photodetection performance across the examined range of light intensity. The linearity of the photodiodes' response makes them particularly suitable for implementation in in-sensor computing applications, as compared to phototransistors.[247]

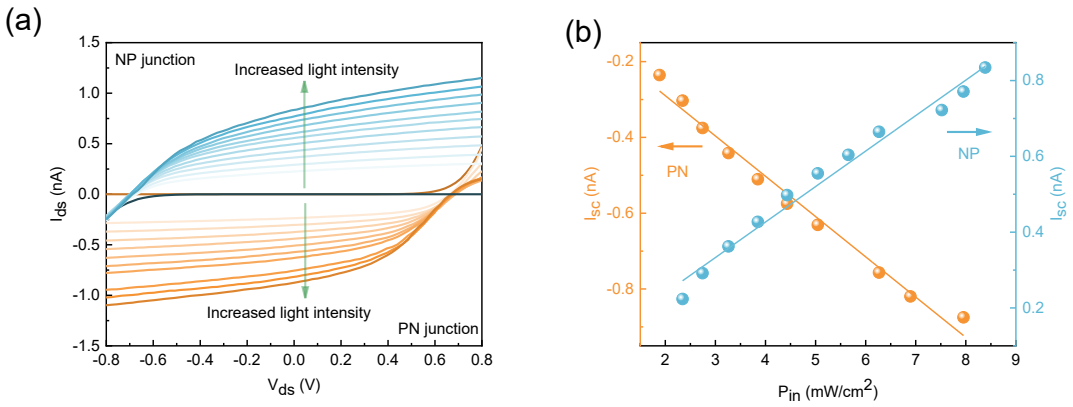


Figure 5-11: Light intensity tunable behaviors for WSe_2/P(VDF-TrFE) neuromorphic vision sensor. (a) The I_{ds}-V_{ds} curves under different input light intensity for PN and NP configurations. These curves demonstrate the generation of a significant I_{sc} under zero bias voltage. (b) The linear relationship between I_{sc} and the input power intensity for PN and NP configurations.

5.5 Programmable multi-states photocurrents

5.5.1 Progressive transition processes

The programmable and non-volatile nature of WSe_2/P(VDF-TrFE) transistors allows for the realization of intermediate photocurrent states in PN and NP junctions. By applying a series of gate voltage pulses under constant light intensity, multiple positive and negative photocurrents can be achieved. This is exemplified in Figure 5-12(a) and (b), where two gates with opposing voltage values are coupled to precisely control the device behavior. For instance, in the case of Figure 5-12(a) and Gate1 setting, a 20 V gate voltage pulse with a 1 ms duration is initially applied to Gate1, resulting in a -180° phase difference and the formation of an NP junction. This configuration induces a positive photocurrent under illumination. Subsequently, a -10 V gate voltage pulse with

the same duration is applied to Gate1 followed by negative gate pulse with same steps of 0.125 V. The sequence of gate voltage pulses is applied to gradually reduce the positive photocurrent, leading to a decrease in the built-in electric field of the NP junction, which is confirmed by the previous phase image analysis. A similar phenomenon is observed in Figure 5-12(b) when starting from the PN junction. Such reconfigurable architecture based on two separated gates beneath the ferroelectric gates provides a free and convenient platform to achieve reversible photocurrent tunability with opposite signs. The writing process involves setting Gate2 to the opposite voltage of Gate1 without any additional bias voltage. During the reading process of photocurrents, only optical pulses are applied, with gate and bias voltages defined as zero due to the nonvolatility property. Figure 5-12(c) and (d) offer magnified views of the circular regions corresponding to Figure 5-12(a) and (b), respectively. Notably, the positive and negative photocurrent variations demonstrate a pronounced step-like behavior, characterized by a consistently incremental or decremental change of uniform 6 pA for each optical pulse during reading process. This uniform step pattern facilitated by precise ferroelectric polarization programmability signifies a symmetrical, linear, and non-volatile modulation of the photocurrent, carrying potential for subsequent high-precision motion recognition tasks.[248-249]

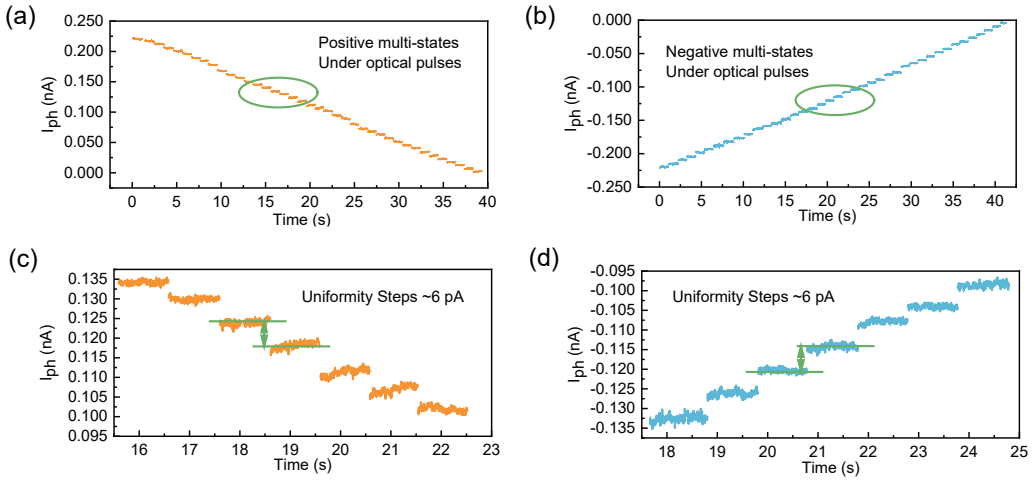


Figure 5-12: Photocurrent generation under opposite gate voltages pulse. The application of opposite gate voltages to the two separated gates initiates positive (a) and negative (b) photocurrents when starting from NP and PN configurations, respectively. The light pulse duration is 1 ms. An enlarged view of the circles reveals the stable steps of multi-levels of positive (c) and negative (d) photocurrents. These steps exhibit a uniform magnitude of approximately 6 pA.

The detailed gate voltage pulse configurations are presented in Figure 5-13. Gate voltage pulse configurations for multi-states photocurrent generation. Here, we take Gate1 as an example. Transition from PN to NP (a) and from NP to PN (b). The supplementary figure provides comprehensive insights into the specific gate voltage pulse settings employed in experimental study.

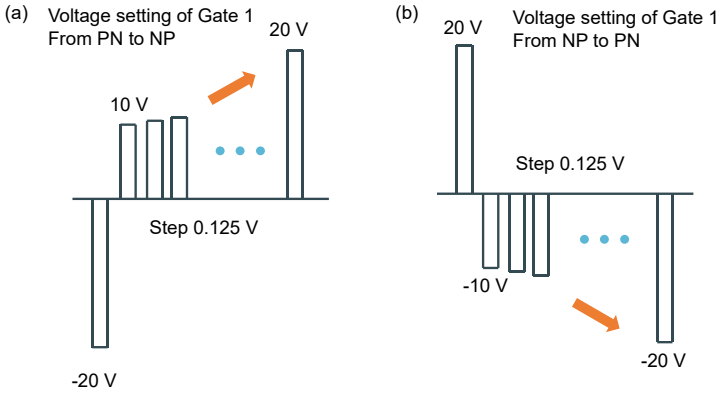


Figure 5-13: Gate voltage pulse configurations for multi-states photocurrent generation.

5.5.2 Nonvolatility and linearity of the multi-states

To further investigate the modulation of photocurrent, Figure 5-14(a) illustrates the transition from negative to positive values by gradually increasing the number of light pulses. Through a gradual increase in the pulse number, the photocurrent undergoes a progressive transition from negative to positive values, as indicated by the blue dotted lines. This transition corresponds to a transformation from the initial PN to the final NP configuration, resulting in the realization of approximately 82 discrete states resolution of more than 6 bits, exceeding the capabilities of certain previous studies.[36-37] Conversely, by applying negative Gate1 pulses in conjunction with positive Gate 2 pulses, a transition from the NP to PN configuration is induced, causing the photocurrent to revert to negative values, as depicted by the orange dotted lines. This behavior also yields 82 distinct states, indicating a highly symmetrical property. The number of states can be further enlarged by expanding the pulse range and reducing the pulse steps for higher programming capability. Importantly, both multi-level positive

and negative photocurrents can be repeatedly observed with reversibility property, as demonstrated in cycle 2 of Figure 5-14(a). This recurrence is made possible by the re-writability of the P(VDF-TrFE) ferroelectric material, which enables reliable and repeatable writing and erasing processes. These multi-level photocurrent states, characterized by bidirectional transitions, can be interpreted as LTP and LTD processes, analogous to synaptic weights in ANNs. To provide evidence of the linearity and uniformity of the versatile LTP and LTD states in response to optical pulses, we have examined the specific synaptic processes of partial LTP and LTD within a single cycle. This detailed analysis is depicted in Figure 5-14(b) and (c), which correspondingly illustrate the magnified views of the LTP and LTD processes. All the progressive photocurrents exhibit a degree of linearity with R^2 coefficients of approximate 0.999 for each individual LTP and LTD processes. The nonlinearity values of 0.01/-0.01 further highlight potential for high-performance neural network computation compared to previous studies.[250-251] Comparison of nonlinearity and the number of multiple bits is summarized in Table 5-1.

Table 5-1: States and Nonlinearity comparison between several neuromorphic devices

No.	Device structure	State counts	Nonlinearity	Reference
1	$MoTe_2$/P(VDF-TrFE)	More than 5	0.12/-0.12	[109]
2	WSe_2/P(VDF-TrFE)	6	0.56	[215]

3	Fe_7S_8 @MoS_2	More than 4	-/-3.12	[252]
4	MoS_2/P(VDF-TrFE)	7	3.42/-2.02	[125]
6	Pentacene/P(VDF-TrFE)	More than 6	0.25/-	[134]
7	h-BN/WSe_2	More than 6	3/-6	[253]
8	Germanium ferroelectric nanowire FET	More than 8	1.22/-1.75	[254]
9	WSe_2/Al_2O_3	More than 6	2.2/-2.1	[255]
10	$MoSe_2$/Bi_2Se_3	More than 4	3	[256]
11	Organic ion-gated transistors	More than 8	1.19/-4.37	[257]
12	$Hf_{0.5}Zr_{0.5}O_2$ FeFET	5	1.75/-1.46	[37]
13	**WSe_2/P(VDF-TrFE)**	**More than 6**	**0.01/-0.01**	**This work**

Therefore, gradual switching of ferroelectric polarizations facilitates the emulation of synaptic function and gives rise to the observed linearity for the synaptic weights updating. Moreover, Figure 5-14(c) demonstrates the long-term stability of 21 distinct photocurrent states encompassing positive, negative, and near-zero states, which can be extended to more states by finely tuning ferroelectric polarizations through the separated two gates. These states exhibit exceptional stability over a 150-second period,

comparable with previous works.[258-259] The integration of reconfigurable WSe_2/P(VDF-TrFE) devices results in the convergence of optical signal sensing, computation, and memory storage functionalities within a single device. Such comprehensive combination enables the generation of linear, uniform, bidirectional, and multiple photocurrent responses, thereby facilitating object motion sensitive operations that closely resemble the functioning of ganglion cells in the retina. Above ferroelectric-defined controllable multiple states provide stable and predictable manner for the accurate and uniform performance during training the neural network model compared with other ionic migration and vacancy generation working mechanism.

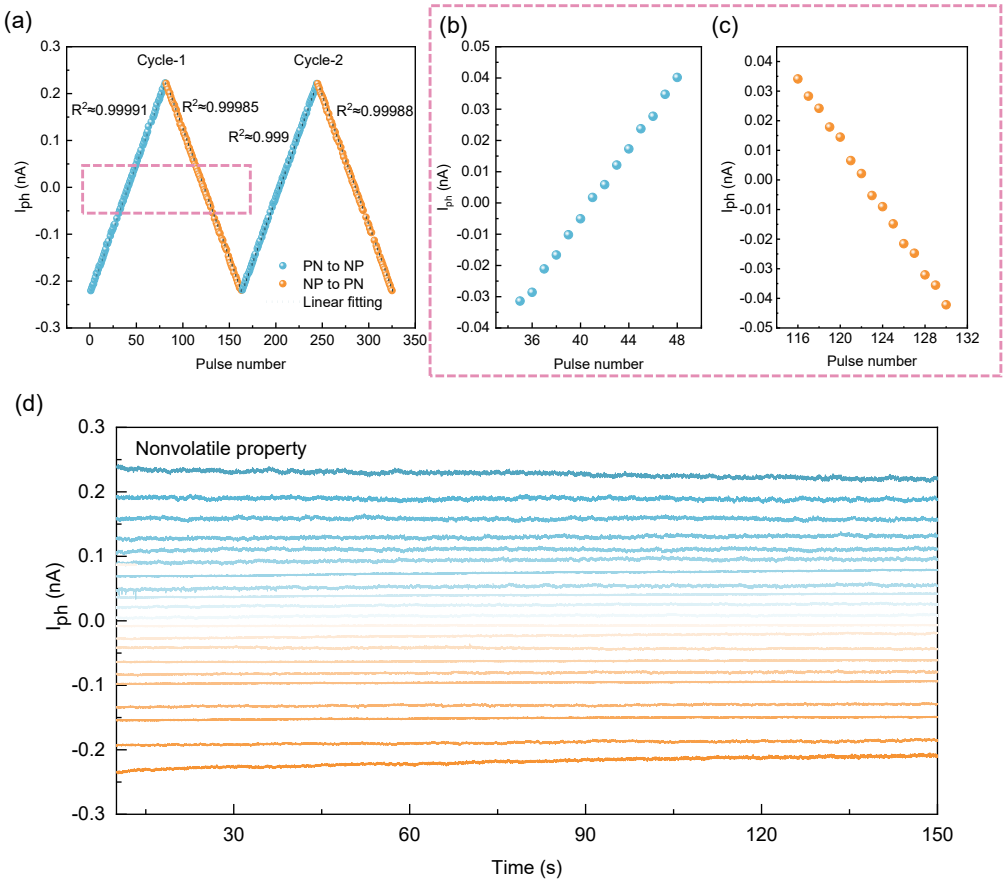


Figure 5-14: Bidirectional LTP and LTD processes and nonvolatility of the 21

states. (a) Two cycles of bidirectional LTP and LTD when the devices subjected to optical pulses under ferroelectric modulation. These processes demonstrate high linearity and symmetry. Magnified view of partial LTP (b) and LTD (c) processes in cycle-1. (d) The nonvolatility property of multiple photocurrents levels.

The diagrams of these gradual ferroelectric domain conversion processes are illustrated in Figure 5-15(a-b). In the case of Figure 5-15(a), during process (1), a positive (negative) gate voltage is applied to Gate 1 (Gate 2). By changing the direction of the gate voltage, the ferroelectric domains gradually polarize in the opposite direction, where a negative (positive) gate voltage is applied to Gate 1 (Gate 2), but its magnitude remains smaller than the coercive voltage. Consequently, the built-in electric field of the NP junction decreases, while the built-in electric field of the PN junction gradually forms as the gate voltage pulse and amplitude are further increased. The PN junction is fully formed when the left/right portion of the ferroelectric is completely polarized downward/upward, and the negative photoresponsivity reaches its maximum. A similar process occurs in diagram (b) when starting from a PN junction and transitioning to an NP junction.

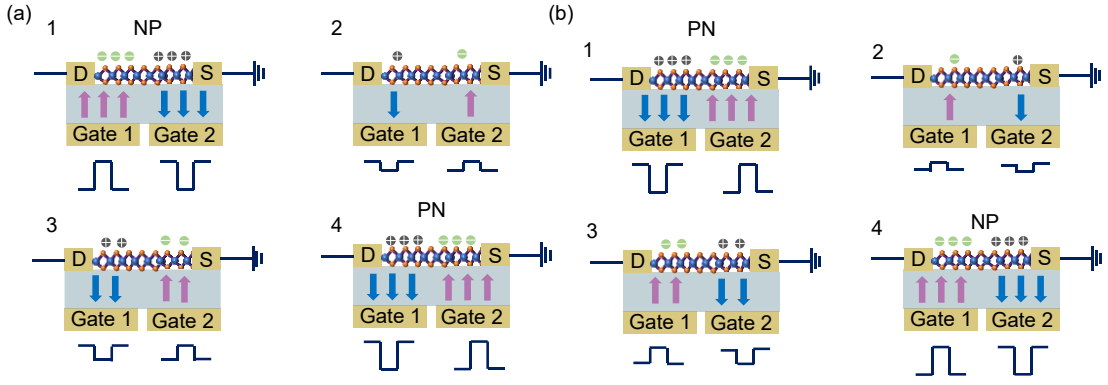


Figure 5-15: Progressive gate voltage pulse configuration ferroelectric modulation. By applying a gate voltage greater than the coercive voltage with opposite polarity to Gate 1 and Gate 2, the ferroelectric domains can be switched to NP (a) or PN (b) junctions.

Figure 5-16 presents the results of fitting the nonlinearity of the LTP and LTD processes, with fitted nonlinearity values of 0.01 and -0.01, respectively. The weight update data of WSe_2/P(VDF-TrFE) is obtained by fitting the data where the amplitude (A) is normalized, and the plot represents the normalized photocurrent against the normalized number of pulses.

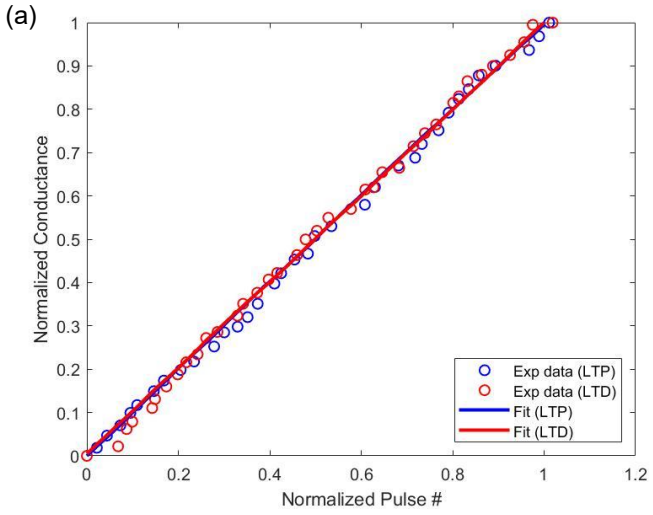


Figure 5-16: The results of fitting the nonlinearity of the LTP and LTD processes, with fitted nonlinearity values of 0.01 and -0.01, respectively.

5.6 OMD operation

By harnessing the symmetrical and multi-states of bidirectional photocurrents described above, neuromorphic vision sensors can replicate the functionality of retina in a single operation. These devices can effectively identify and collect moving targets

information from the surrounding background, mimicking the function of motion sensitive ganglion cells. Working mechanism and operation process of OMD are illustrated in Figure 5-17(a). The dynamic video can be segmented into many individual frames based on the time sequence from the beginning t_a to the final moment t_{end}. Along with the timeline (orange dotted line), the living room is unoccupied at the initial moment t_a, providing a static global background for subsequent comparison. Within a defined interval such as from t_b to t_j, a moving individual enters the living room, exhibits distinct hand gestures at various moments and then leaves the room. The dynamic individual serves as a contrasting element to the original static environment at t_a moment. In order to demonstrate the moving detection results, frames at t_a and t_d are taken as examples. Each frame image is assumed to comprise M×N brightness pixels and the original brightness distribution of t_a is depicted in Figure 5-17(b), with normalized brightness values ranging from 0 to 1. On the other hand, the photocurrent states of the WSe_2/P(VDF-TrFE) 2D neuromorphic vision sensor can be assembled into positive and negative M×N photocurrent matrices, which exhibit approximately equal absolute values due to their exceptional symmetry and linearity as we mentioned above. To perform frame difference calculations, the M×N positive and M×N negative conductance matrices are multiplied with the image brightness pixels at different moments of t_a and t_d, respectively, as indicated by the blue arrows in Figure 5-17(a). The two multiplied components are then summed together to map the brightness result of the output pixels, which allows for detecting the moving person in the living room,

as depicted by the pink arrows in Figure 5-17(a). Such results are stored within the pixels at the corresponding moment, thanks to the nonvolatility property of the neuromorphic vision sensor. We also conduct demonstrations of different hand gestures, such as waving and thumbs-up, at time moments of t_d and t_e, respectively. The output of processed brightness pixel can effectively capture such little difference as shown in the yellow box. Within a specific period, when the background remains static and no moving objects are present, the brightness difference of the output pixels approaches to zero, as illustrated in Figure 5-17(c). This behavior arises from the equality of absolute values between the positive and negative M×N photocurrent matrices for counteracting derived from the neuromorphic vision sensor. However, in the presence of a moving person during a given interval, the brightness of the static background pixels remains close to zero, while the brightness pixels corresponding to the moving person exhibit values more than zero and follow a normal distribution, as shown in Figure 5-17(d) and (e).

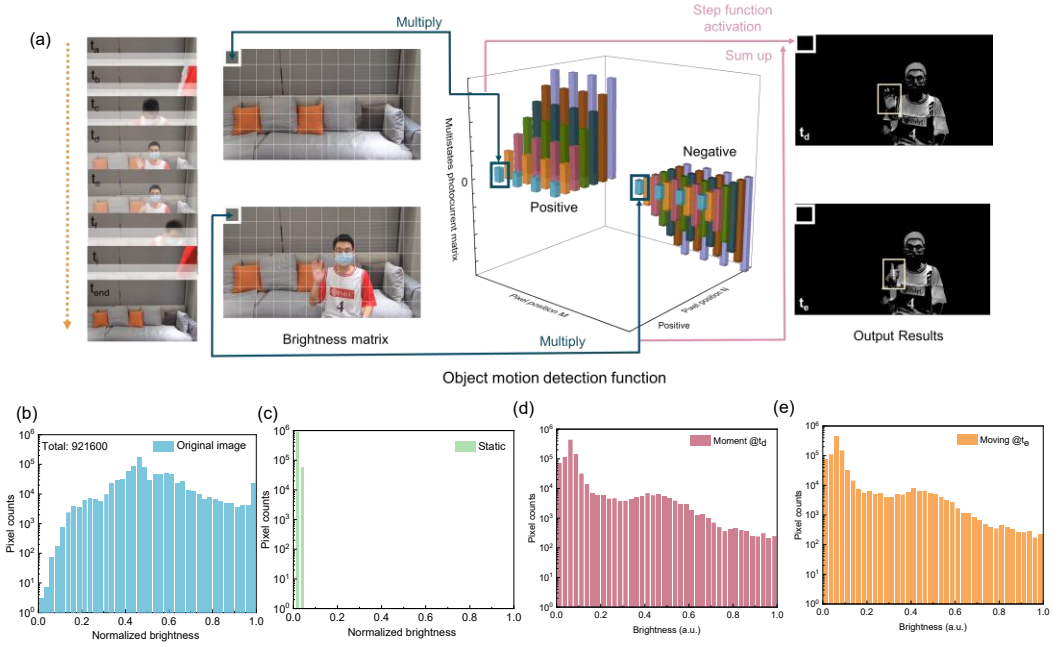


Figure 5-17: Working mechanism and operation process of OMD and brightness distribution. (a) The brightness pixels at different frame moments (e.g., t_a and t_d) are multiplied by the corresponding positive and negative photocurrent matrices WSe_2/P(VDF-TrFE). The resulting products are then summed to detect dynamic objects. (b) The distribution of brightness values across all pixels in the original image, consisting of a total of 921,600 pixels. Output brightness distribution of static pixel (c), dynamic pixel at t_d (d), and dynamic pixel at t_e (e) after motion detection.

In Figure 5-18, we present a comprehensive analysis of the other frames (t_b, t_c, t_f, t_j) along with their processed output pixels and brightness distributions. Supplementary Figure 5-18 showcases a comprehensive analysis of various frame images (t_b, t_c, t_f, t_j) in conjunction with their respective moving detection results and brightness distributions. These frames serve to illustrate the distinct processes of individuals entering, sitting and exiting the living room. Notably, our motion detection system,

leveraging the WSe_2/P(VDF-TrFE) neuromorphic vision sensor, demonstrates remarkable efficacy in accurately capturing the presence of moving individuals within each frame. The inclusion of these findings further strengthens the validity and reliability of our results.

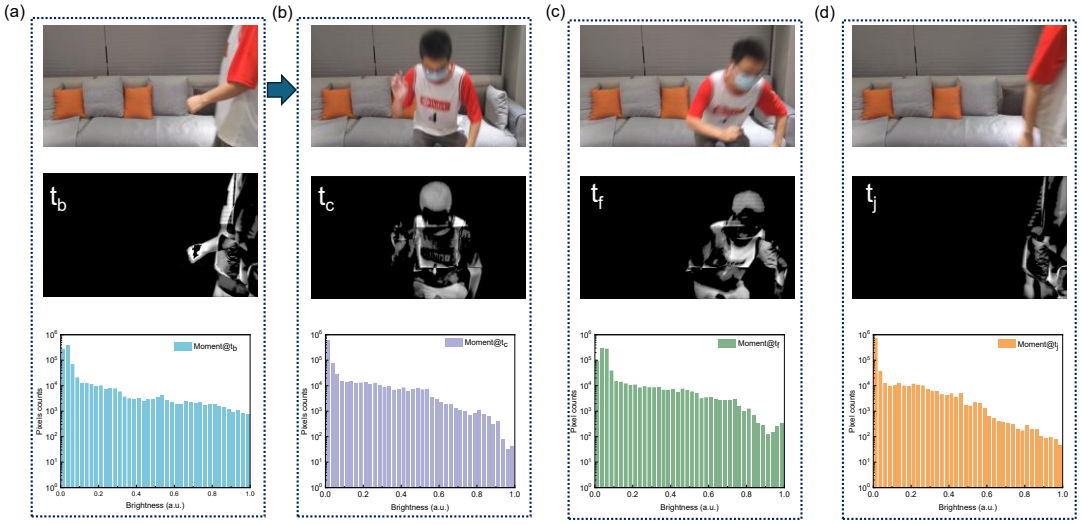


Figure 5-18: Comprehensive analysis of the other frames t_b (a), t_c (b), t_f (c), t_j (d).

Moreover, we provide experimental validation of a 3×3 reconfigurable neuromorphic vision sensor array, as illustrated in Figure 5-19. Each of the nine WSe_2/P(VDF-TrFE) neuromorphic vision sensors exhibit uniformity and demonstrates bipolar electrical behaviors, as illustrated in Figure 5-20. These findings establish a robust foundation for the advancement of scalable optical sensing and in-sensor computing applications.

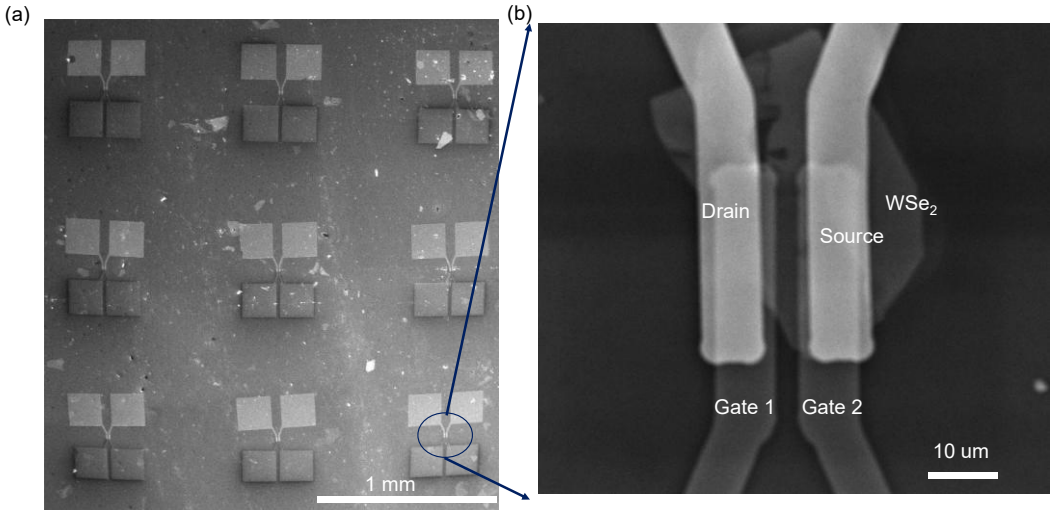


Figure 5-19: 3×3 pixel neuromorphic vision sensor array. (a) SEM image of the 3×3 pixel array based on WSe_2/P(VDF-TrFE) reconfigurable neuromorphic vision sensor device. (b) Enlarged image of one of the nine devices.

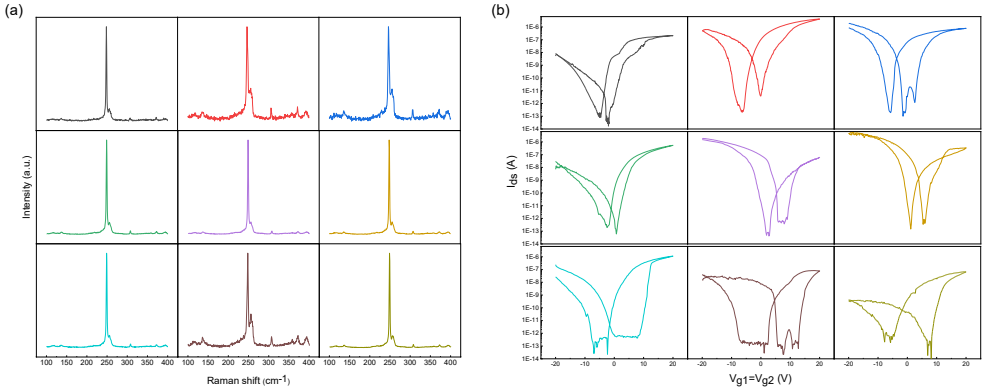


Figure 5-20: Uniformity characterization of the 3×3 pixel neuromorphic vision sensor array. (a) The Raman spectra of the nine WSe_2 devices within the neuromorphic vision sensor array, demonstrating their commendable uniformity. (b) The transfer characteristics of the nine WSe_2/P(VDF-TrFE) devices, measured at a bias voltage of 1 V. The results exhibit typical ferroelectric hysteresis behavior, highlighting both the consistency and uniformity of the devices.

Furthermore, the vital information pertaining to the moving object is inputted into an ANN, as depicted in Figure 5-21(a), leveraging the high-linear LTP and LTD behaviors

of WSe_2/P(VDF-TrFE). For simulation purposes, we utilize the Modified National Institute of Standards and Technology (MNIST) handwritten digits dataset and a three-layer network.[260] The classification accuracy over 40 epochs is depicted in Figure 5-21(b). During the initial epochs, the recognition accuracy experiences significant improvement and reaches a peak value of 96.8%. This high accuracy rate stems from the linear, symmetric, and distinguishable weight updating based on controllable ferroelectric polarization, aligning effectively with the outcomes of the software training process. Consequently, the WSe_2/P(VDF-TrFE) neuromorphic vision sensor showcases the OMD process, akin to certain ganglion cells. This bionic approach significantly reduces the generation and transmission of redundant data by emphasizing moving objects through an energy-efficient pre-processing platform.

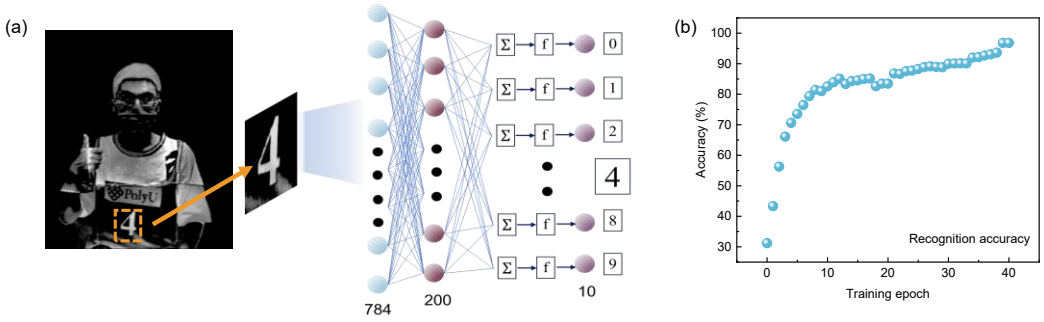


Figure 5-21: Dynamic feature recognition and accuracy result. (a) Recognition of dynamic target object. (g) Accuracy of the recognition process over 40 epochs, demonstrating the high accuracy of 96.8% during training.

5.7 Conclusion

In conclusion, we have employed a reconfigurable 2D WSe_2/P(VDF-TrFE) neuromorphic vision sensor with a straightforward device structure and construction

strategy for motion detection. High-precision programming ability is important for moving information processing. Previous fluctuations in each state without distinguishable and uniform step have hindered various neuromorphic applications. Our neuromorphic vision sensor demonstrates programmable tunability through progressive ferroelectric modulation, enabling the generation of self-powered bidirectional photocurrents with more than 6 bits of resolution and uniform step of 6 pA after each stimulation. These photocurrents possess desirable properties such as nonvolatility, symmetricity, reversibility, and high linearity (R^2=0.999). By leveraging the bidirectional photocurrent states, we have achieved efficient motion detection by collecting information solely from the moving object while minimizing redundant data generation, like the ganglion cells in the human retina. We also demonstrate a 3×3 neuromorphic vision sensor array for scalable application. Additionally, the constructed ANN recognizes the essential moving information with accuracy 96.8%. The integration of optical signal sensing, multi-states memorization, and power-efficient modulation capabilities in the neuromorphic vision sensor holds significant potential for expanding its application to other advanced vision hardware domains.

Chapter 6 Conclusion and Prospect

6.1 Conclusion

Neuromorphic computing has advanced through the exploration of innovative devices, the realization of array-level neural networks, and the improvement of algorithms. This doctoral thesis focuses on investigating the role of low-dimensional ferroelectric synaptic transistors as a fundamental element in this progression. Leveraging the atomic-level thickness of low-dimensional materials, the stable nonvolatility and easily processable properties of ferroelectrics, along with the advantages of multi-port read-write separation, we examine the extensive synaptic plasticity and neuromorphic computations demonstrated by low-dimensional memory transistors functioning as artificial synaptic devices.

The objective of this research is to contribute to the advancement of neuromorphic applications by elucidating the capabilities of these novel components and their potential for efficient and versatile neuromorphic systems. By strategically leveraging their extensive physical electronic characteristics and synaptic plasticity, we aim to exploit and maximize the innate potential of 2D materials and ferroelectricity. Developing p-type materials with high mobility is essential for achieving high-performance neuromorphic networks with a wide range for conductance modulation, surpassing the widely used n-type 2D materials. Additionally, synaptic devices utilizing direct bandgap materials effectively simulate human retina functions, such as image pre-processing through the optoelectronic array. Moreover, beyond static image

recognition, an emerging application in neuromorphic systems is object motion detection, which can be realized through the manipulation of intermediate ferroelectric polarization states. The main research results of this doctoral thesis are as follows:

Firstly, by integrating p-type BP with high carrier mobility and a ferroelectric copolymer P(VDF-TrFE), we have successfully fabricated three-terminal ferroelectric synaptic transistors. These FeFETs are characterized by a high mobility of 900 $cm^2 V^{-1} s^{-1}$ and an on/off ratio of 10^3. Moreover, we demonstrate low energy consumption at the femtojoule-level per pulse event, comparable to the performance of current state-of-the-art artificial synapses. Our investigation encompasses a comprehensive study of synaptic behaviors, including LTP, LTD, PPF, and memory consolidation processes, achieved through precise adjustments of the ferroelectric gate. Remarkably, our simulations of a hardware neural network for pattern recognition achieve accuracy rate of 93.6%. Leveraging the carrier mobility and conductance variation, the ferroelectric synaptic transistors presented in this study hold potential for energy-efficient applications in in-memory computing cells.

Secondly, we present a novel design and characterization of a multifunctional optoelectronic ferroelectric synaptic transistor, incorporating 2D direct bandgap material ReS_2 and ferroelectric copolymer P(VDF-TrFE), which demonstrates concurrent simulation of synapse behaviors, multi-color perception, and visual neuromorphic computing functionalities. Specifically, we achieve versatile synaptic behaviors, including PPF, STP/LTP, as well as STM and LTM transitions. Moreover,

we replicate the advanced neuromorphic feature of the learning-forgetting-relearning process. Leveraging a single optoelectronic synapse, we establish a neuromorphic visual array model that emulates the functionality of the retina, enabling light-intensity sensing and color discrimination thanks to the obvious PPC effect in ReS_2. Through light-induced conductance variation, we enhance the contrast of the desired object while reducing surrounding noise signals. After contrast enhancement and de-noising image pre-processing, our optoelectronic device array is trained to achieve image recognition accuracy of 96%. These promising findings substantiate the potential of ferroelectric optoelectronic devices in realizing perceptual capabilities, object recognition, and energy-efficient operations, thereby propelling us closer to the replication of the intricate human visual system.

Thirdly, to solve the fluctuation limitations and uncontrollable manner in the previous ion migration or vacancy modulation neuromorphic devices, we construct a reconfigurable neuromorphic vision sensor based on WSe_2/P(VDF-TrFE). Through precisely progressive programming of intermediate ferroelectric polarizations, versatile bidirectional photocurrent levels can be obtained with reversibility, nonvolatility, uniform and discrete steps of 6 pA, ultra-high linearity ($R^2 \approx 0.999$) and more than 6 bits resolution. Such phenomenon establishes a robust basis for highly controllable programming skills, ensuring accuracy in performance. Thereby, moving individuals within the static background can be emphasized with high efficiency by eliminating the redundant data from static scenes. Artificial neural network recognizes the important

feature of moving individual with accuracy outcome of 96.8%. A uniform 3×3 motion neuromorphic vision sensor array is also fabricated for further scalability. Our work seamlessly integrates optical sensing functionality, energy-efficient architecture, nonvolatile and predictable multiple states, and motion detection computation, making it a compelling solution for vision applications.

6.2 Prospect

The immersive investigation concerning the combination of 2D semiconductors and ferroelectrics has ignited significant interest in various fields. Ferroelectric functions in this system can enhance the overall performance and provide voltage-tunable ferroelectric polarization states to actively modulate the optical and electrical properties of 2D semiconductor layers. Although researchers have made significant progress in this area, 2D semiconductor/ferroelectric polymer devices are still in their infancy. Here several issues and challenges are put forward as follows and hopefully further innovative ferroelectric devices could be investigated.

First, a key challenge lies in the integration of large-area 2D semiconductor/ferroelectric hybrids with high quality and uniformity. Currently, significant scientific efforts are focused on developing scalable growth techniques for 2D layers, aiming to achieve continuous, single-crystalline films with precise control over the layer number. Simultaneously, spin-coating or pulsed laser deposition (PLD) techniques have demonstrated success in fabricating large-scale ferroelectric films. Therefore, it is crucial to explore the integration of mass-produced 2D materials and

ferroelectric layers for future applications. One promising research direction is the realization of a new concept of electrical writing and optical reading memory technology based on interconnected nonvolatile logic and memory devices. This approach has the potential to revolutionize memory storage and retrieval by combining the advantages of both electrical and optical functionalities. Furthermore, the development of large-scale integrated neural cells connected by an increasing number of synapses will drive the advancement of high-performance neuromorphic computing. This trend focuses on creating neural networks that closely mimic the complexity and connectivity of the human brain, enabling more sophisticated cognitive capabilities.

Secondly, interface engineering plays a crucial role in the performance of devices incorporating 2D materials, owing to their atomic-thin nature and high surface-to-volume ratio. Achieving a desirable interface between P(VDF-TrFE) and 2D layers is essential for realizing high mobilities in FeFETs. Precise control of surface topography and the construction of a clean interface are fundamental requirements for device applications. From an experimental perspective, it is necessary to carefully control the preparation environment, including factors such as water condensation and substrate temperature, to ensure optimal device performance. These considerations are vital for maintaining the integrity of the interface and maximizing device efficiency. Additionally, the solubility of P(VDF-TrFE) in acetone poses challenges for photolithography processes. To overcome this limitation, alternative methods and modified lift-off processes need to be implemented. This will enable the successful

patterning and integration of P(VDF-TrFE) into device structures, ensuring their compatibility with standard fabrication techniques.

Thirdly, P(VDF-TrFE) ferroelectric copolymers serve as crucial organic materials that address the incompatibility between inorganic materials and flexible substrates. While research on flexible and wearable devices based on P(VDF-TrFE) has focused on simulating tactile sensory organs, there is significant potential to explore their excellent ferroelectric properties in conjunction with neuromorphic devices for artificial information processing. However, it is important to address the challenges related to the stability and reliability of flexible devices based on P(VDF-TrFE). As the thickness of P(VDF-TrFE) films decreases, the performance of these devices can be compromised, leading to increased gate leakage current. To mitigate these issues, it is necessary to improve the performance of P(VDF-TrFE) film-based devices by incorporating additional insulating materials specifically designed for flexible electronics. The operating voltage can be further reduced through either thickness scaling of the ferroelectric layer or adoption of alternative ferroelectrics exhibiting lower coercive voltages. Notably, emerging sub-10-nm hafnium-based ferroelectrics demonstrate operational voltages as low as 2.4 V, highlighting their potential for low-power applications.[261] By enhancing the stability, reliability, and performance of P(VDF-TrFE) based flexible devices, we can unlock their full potential for various applications, including neuromorphic computing and artificial intelligence. Further research and development efforts should focus on optimizing the integration of P(VDF-

TrFE) with other insulators to enhance the performance and functionality of flexible electronic devices.

Overall, the successful integration of P(VDF-TrFE) films as gate dielectrics with diverse 2D materials has demonstrated improved device performance and introduced new working mechanisms. This integration of 2D semiconductor/ferroelectric hybrids has the potential to rapidly advance and establish a significant presence in modern electronics, optoelectronics, and neuromorphic applications. Future research holds immense promises for breakthroughs in the field of advanced functional devices.

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