TWO-DIMENSIONAL TRANSITION METAL DICHALCOGENIDES AND HIGH-K DIELECTRICS FOR HIGH-PERFORMANCE FIELD-EFFECT TRANSISTORS

ZHANG SONGGE

PhD

The Hong Kong Polytechnic University

2025

The Hong Kong Polytechnic University

School of Fashion and Textiles

Two-Dimensional Transition Metal Dichalcogenides and High-κ Dielectrics for High-Performance Field-Effect Transistors

Zhang Songge

A thesis submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy

August 2024

Certificate of Originality

I hereby declare that this thesis is my own work and that, to the best of my knowledge and belief, it reproduces no material previously published or written, nor material that has been accepted for the award of any other degree or diploma, except where due acknowledgement has been made in the text.

_____ (Signed)

ZHANG Songge(Name of student)

Abstract

Flexible electronics is an emerging electronic technology that fabricates electronic devices on flexible substrates. Broad applications prospects have been applied in fields such as information, energy, healthcare and national defense. It requires operating under a certain range of deformation, including bending, folding, twisting, compression and stretching, which puts forward requirements for new materials. Atomically thin two-dimensional (2D) materials, such as metallic graphene, semiconducting molybdenum disulfide (MoS_2) and insulating hexagonal boron nitride (hBN), have attract interests because of their high mobility (for semiconductors and conductors) and good mechanical properties. In this case, developing 2D devices is important for flexible electronics and systems.

This thesis developed a high-performance $MoSe_2$ field-effect transistors, an ultrathin high-κ dielectric materials for 8-in. level MoS_2 field-effect transistors, and 2D ferroelectric field-effect transistors with ferroelectric topological film, which is significant for 2D devices towards prolonging Moore's Law. The study focuses on the 2D materials synthesis and devices fabrication for high-performance with high on/off ratio, small SS and large on-state current.

For $MoSe_2$ growth and high-performance transistors fabrication, high-quality continuous $MoSe_2$ films with salt as metal sources are successfully synthesized. The domain size is around 120 μm, which is larger than that in most litheratures and oxide sources. Raman and PL also demonstrate its high-crystalline quality. Electrical measurement shows that the $MoSe_2$ film is uniform and transistors coule reach a high on/off ratio of 10^9 and a high on-state current of 12 μA/μm at 1 V bias, which is superior than that in reported literatures.

For ultrathin high-κ HfO_2 dielectrics, we utilize an optimized ALD process with two-oxidation step to deposit defect-free high-quality 1.3-nm-thick HfO_2 high-κ

dielectric layers on 8-inch wafers at only 200 °C. Our ultrathin HfO_2 film shows an extraordinarily small EOT of 0.27 nm, a ultrasmall leakage current of 10^{-14} A/μm^2 at 1 V bias voltage, and a robust breakdown electric field of approximately 32 MV/cm. We also fabricate MoS_2 transistors and circuits with 1.3-nm-thick HfO_2 as dielectric layers to demonstrate its practicality and gate controllability. Typical transistors exhibit large on-state current density of 250 μA/μm and an impressive on/off ratio of 10^8, accompanied by an ultra-low subthreshold slope of 60 mV/dec. Logic gates and memory devices are also fabricated on 8-inch wafers to demonstrate its substantial implications for the forthcoming advanced semiconductor processes in the angstrom era.

For topological ferroelectric field-effect transistors, ferroelectric topological structures are promising new candidates for high-performance memories with excellent stability and low power consumption. Abundant ferroelectric materials and topological structures have been found and investigated over the past decade; however, integration of them into memory devices has greatly delayed, mostly due to the constraint from their substrates. In this work, we demonstrate, for the first time, scalable topological ferroelectric field-effect transistors (Fe-FETs) based on large-scale uniform flux-closure topological ferroelectric films epitaxially grown on substrates with sacrificial layers. Unlike the previous coexistence of trivial and nontrivial domains, the rigid single flux-closure arrays can stably exist in freestanding films and can be erased by increasing temperature over a critical point, rather than undergoing a phase transition to ferroelastic domains as previously reported. Moreover, the flux-closure capacitors demonstrate exceptional performances such as small coercive voltages, negligible leakage currents, a remanent polarization reaching 195 μC/cm^2, and an endurance of up to 10^9 cycles. Furthermore, CMOS-compatible Fe-FET arrays are fabricated, featuring a large

memory window of 7 V, high ON/OFF ratio of 10^8, good endurance and stability, and superior flexibility. Our work paves a way towards the ferroelectric memory devices in future semiconductor industries and flexible electronics.

List of Publications

1. Li, N., **Zhang, S.**, Peng, Y., Li, X., Zhang, Y., He, C., & Zhang, G. (2023). 2D Semiconductor-Based Optoelectronics for Artificial Vision. *Adv. Funct. Mater.* **33**, (2023).
2. **Zhang, S.,** Chen, Y., Wang N., Chai, Y., Long, G., Zhang, G. Probe and manipulation of magnetism of two-dimensional CrI_3 crystal, *Acta Physica Sinica*, **70**, 127504 (2021)
3. **Zhang, S**., et al., Sub-3-Å EOT High-κ Dielectrics for Advanced Transistors, *Nat. Commun.*, under review
4. Yuchen Wang, **Songge Zhang**, Xiaoming Tao*, Guangyu Zhang* *et al.* Biomimetic high-order encoder for color-resolved recognition based on flexible MoS_2 ring oscillators, submitted to ***npj Flex. Electron.*** (Co-first author)
5. Feng-Hui Gong, **Songge Zhang**, Xiaoming Tao, Guangyu Zhang* *et al.* Topological flux-closure ferroelectric transistor arrays, submitted to ***Nat. Electron*** (Co-first author)
6. Song Zhou, Shulin Zhong, **Songge Zhang** *et al.* Structural Templating of Perpendicular Ferroelectricity in Textured Aurivillius Oxide Heterostructures, submitted to ***Adv. Mater.*** (Co-first author)
7. Chen, H., Wan, T., Zhou, Y., Yan, J., Chen, C., Xu, Z., **Zhang, S**., Zhu, Y., Yu, H., Chai, Y., Highly Nonlinear Memory Selectors with Ultrathin $MoS_2/WSe_2/MoS_2$ Heterojunction. *Adv. Funct. Mater.* **34**, (2024).
8. Yu, H., Huang, L., Zhou, L., Peng, Y., Li, X., Yin, P., Zhao, J., Zhu, M., Wang, S., Liu, J., Du, H., Tang, J., **Zhang, S.**, Zhou, Y., Lu, N. Liu, K., Li, N., Zhang, G. Eight In. Wafer-Scale Epitaxial Monolayer MoS_2. *Adv. Mater.* **36**, e2402855 (2024).

9. Long, G., Chen, Y., **Zhang, S**., Wang, N., Chai, Y., & Zhang, G. Probing 2D magnetism through electronic tunneling transport. *Materials & Design*, *212*, 110235. (2021)
10. Liu, J., Zhao, J., Li, L., Wei, Z., Li, J., Wang, Q., Yu, H., Zhou, L., Li, T. and Wu, F., Zhu, M., Sun, H., Chen, Y., Li, Y., **Zhang, S.**, Tian, J., Bai, X., Lu, N., Cao, Z., Lin, S., Wang, S., Du, L., Yang, W., Shi, D., Li, N., Zhang, G., Direct bonding and debonding of 2D semiconductors, *Nature Electronics*, under review.

Acknowledgements

I would like to express my gratitude to my three supervisors, Prof. Xiaoming Tao, Prof. Yang Chai and Prof. Guangyu Zhang. They give me the chance to study in the cross field of physics, devices, circuits and flexible systems. And now, I could master the technique in 2D materials growth, device fabrication, circuits design and flexible system construction. My three supervisors are real scholar. Their profound knowledge, enormous experience and inspiring passion on research guide me through the whole PhD period. I could get almost everything I need from my three supervisors, whether it is research method, sources or stamina. Without their help and assistance, I cannot accomplish my PhD study.

At the same time, I am happy to work with all members and colleagues in three groups, especially Prof. Na Li in Zhang group and Dr. Su Liu in Tao group. I meet with them every day to discuss the latest developments in the research. They enlighten me and help me when I don't have the means until I solve the problem. Without their help, I could not carry out the top-level project smoothly.

I also would like to express my thanks to engineers and technicians at PolyU and SLAB. They teach me how to use the facilities and facilitate my projects. They maintain the facilities work well at all the time during my PhD study.

Table of Contents

List of Figures

Chapter 1. Introduction

1.1. Background

1.1.1. Development of materials for nanoelectronics

For modern integrated circuits, also known of chips, its complex production process embraces UV and electron beam lithography, metal or dielectric deposition, etching and annealing. [1-3] Its feature size has been scaled down to nanometer scale. These complex processes will produce digital circuits, analog circuits and memory made up of tens of billions of transistors. [4-5] The base material for these transistors, however, is the semiconductor silicon. N-type silicon and P-type silicon form the basis of modern nano-electronic materials. [6-8] Silicon-based materials have many significant advantages in modern micro-nano electronics processes. First, silicon is the second most abundant element on Earth, after oxygen, which makes silicon materials relatively cheap and in plentiful supply. [9-12] This richness ensures the sustainability of silicon-based materials in mass production. Second, silicon has excellent semiconductor properties and is able to maintain stable electrical properties at high temperatures, which makes silicon an ideal material for manufacturing transistors and integrated circuits. Silicon has a moderate band gap of 1.12 eV and a high electron and hole mobility of 1350 $cm^2\ V^{-1}\ s^{-1}$ and $cm^2\ V^{-1}\ s^{-1}$, respectively. [13-16] These characteristics make silicon devices have the advantages of high voltage resistance, low reverse leakage current, high efficiency, long service life and good reliability. In addition, the silicon-based process has been very mature after decades of development, with perfect manufacturing and processing technology. This mature process technology makes large-scale production and high integration possible, further reducing production costs. [17-18] Silicon material also has the characteristics of non-toxic and harmless, harmless to the environment and human body, which is one of the

important reasons for its wide application. The chemical properties of silicon are stable, and it is easy to form a stable thermal oxide film, which is particularly important in the manufacturing of planar silicon devices, which can be used to achieve the surface passivation and protection of PN junction and can also form a metal-oxide-semiconductor structure to manufacture MOS field-effect transistors and integrated circuits. (Fig. 1-1) [19-21]

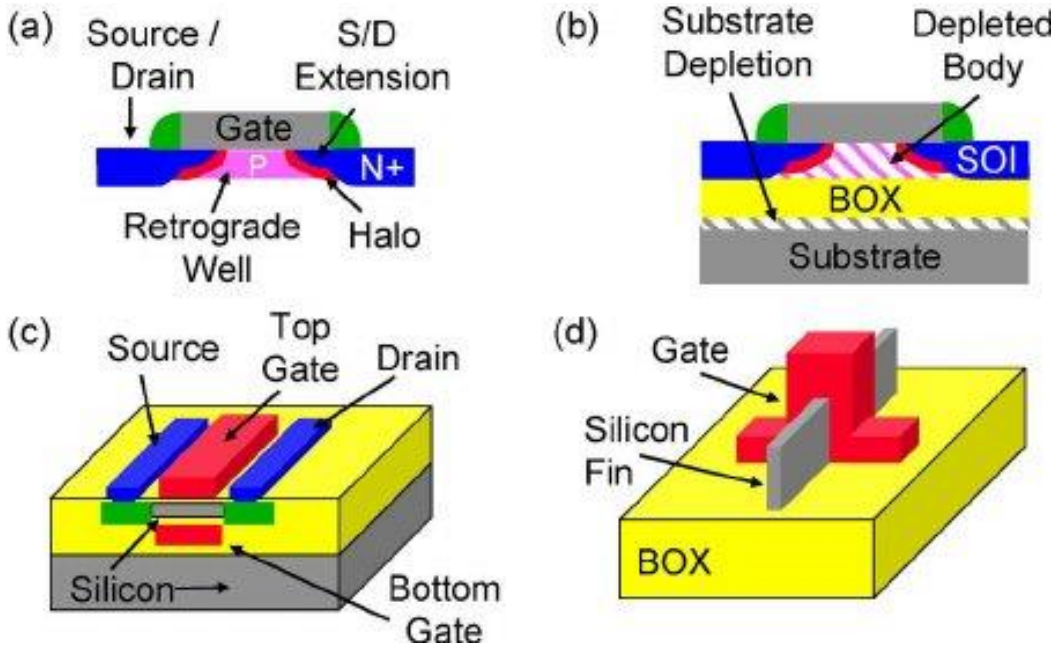

Fig. 1-1. Silicon transistors structures.

However, as transistor sizes enter the sub-10 nanometer era, silicon-based processes face more and more technical challenges and bottlenecks. [22-23] Specifically, at extremely small sizes, the electrical properties of silicon materials can decrease significantly, resulting in increased leakage current and slower switching speed, which negatively affects the performance and energy efficiency of devices. Second, silicon has a relatively low thermal conductivity, which can lead to heat dissipation problems in high-power and high-density integrated circuits. Because heat is difficult to dissipate effectively, the device can overheat,

which affects its stability and life. [24-25] In addition, silicon materials also have certain limitations in terms of mechanical strength and flexibility, which is particularly obvious in some applications requiring high mechanical properties. [26]

1.1.2. Why 2D materials

Two-dimensional materials with atomically flat surfaces and no hanging bonds can be easily synthesized into monolayers due to their weak interlayer vdW forces, which are critical in current chip development. [27-29] The thickness of the single layer material can not only reduce the chip size, but also impede the short channel effect at the limit miniaturization size, including the reduction of threshold voltage with the reduction of channel length, the reduction of drain barrier, carrier surface scattering, velocity saturation, ionization and hot electron effect. (Fig. 1-2) [30-35]

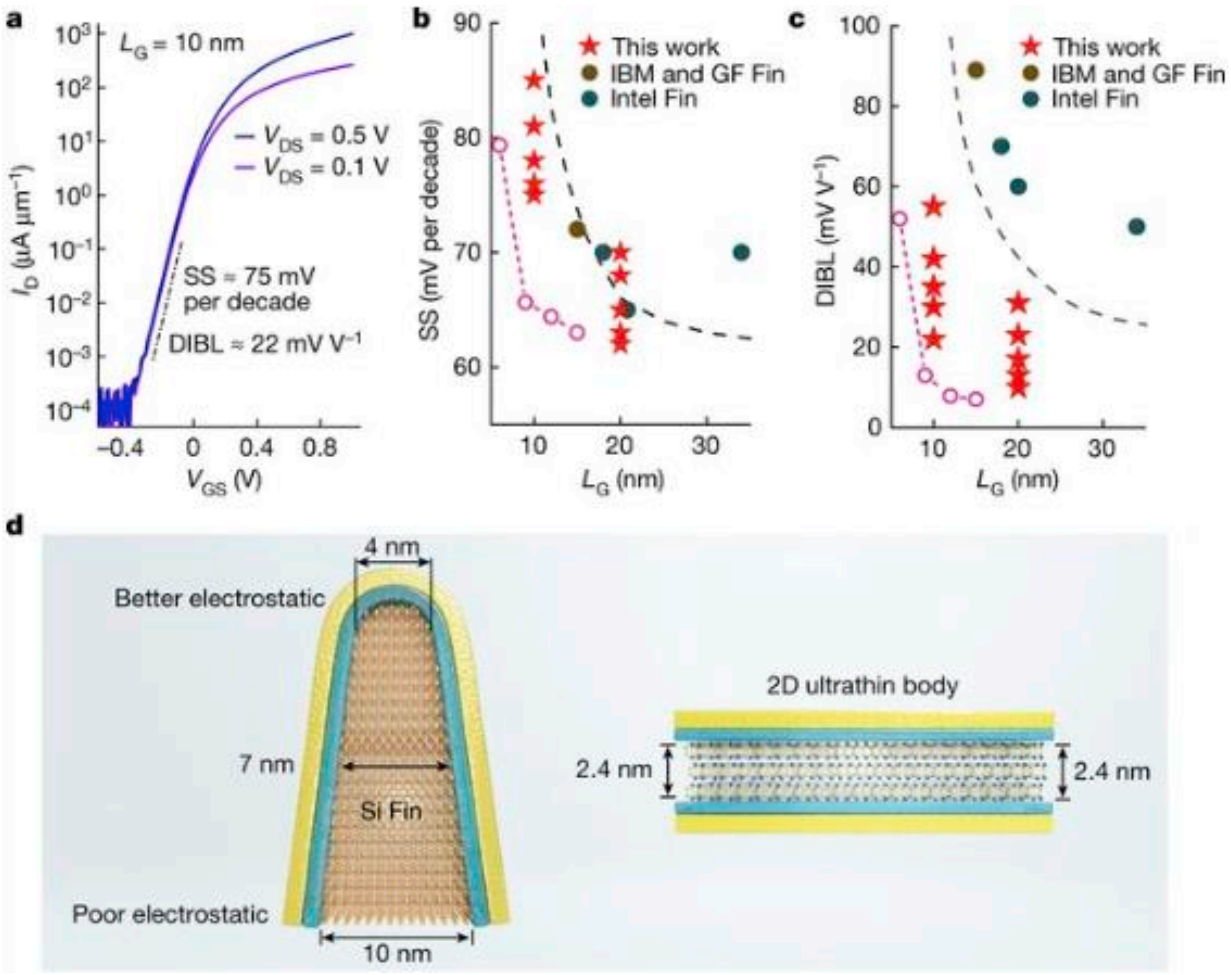

Fig. 1-2. Short-channel effect comparison of 2D InSe FETs and silicon FinFETs. [33]

In addition, the band gap of two-dimensional materials decreases with decreasing thickness, which brings rich physical connotation to two-dimensional materials, such as excitonic effects, valley properties, superconductivity, charge density wave and ferroelectricity. [36-40] Here, we take excitonic effects and ferroelectricity as examples. An exciton is a bound state of an electron and an electron hole (a position where an electron is missing) that are attracted to each other by the Coulomb force. [41-42] It is related to optoelectronic excitations of semiconductors. Excitonic states are weak in bulk materials while it is greatly enhanced when the thickness reduced to monolayer. In this case, many excitonic

effects could be observed, such as enhanced PL and complicated exciton structures. (Fig. 1-3) [43] Ferroelectricity describes materials with spontaneous electrical polarization and can be tuned with external electric field. Some ferroelectric materials, such as $PbTiO_3$, $BiFeO_3$, have been used in memory devices and actuators.

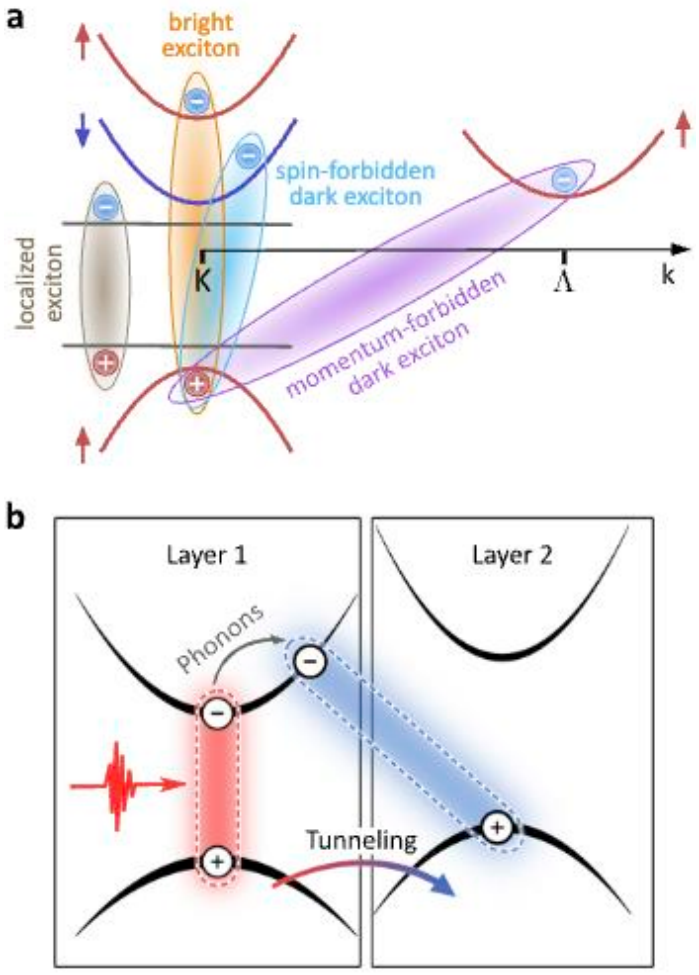

Fig. 1-3. Excitons in 2D materials and heterostructures [43]

Ferroelectricity arrived from ion migration, polar molecular groups, charge redistribution and spin structure. [44-47] When it comes to 2D materials, two types of ferroelectric materials attract many interests. The first type is ion or charge migration. The typical examples are In_2Se_3 and $CuInP_2S_6$. [48-49] In these two

materials, the migration of In atoms and Cu atoms is the main reason of ferroelectric properties. Ferroelectric field-effect transistors and ferroelectric semiconductor-channel transistors have been reported to fabricate with these two materials. The second type of ferroelectric material arising from layer sliding. Bilayer 3R-stacking BN, MoS_2 and WS_2 have been reported recently. [50-54] Fig. 1-4 shows the structures and mechanisms of 2D $CuInP2S6$, BA_2PbCl_4 perovskite and 3R-stacking ferroelectric materials.

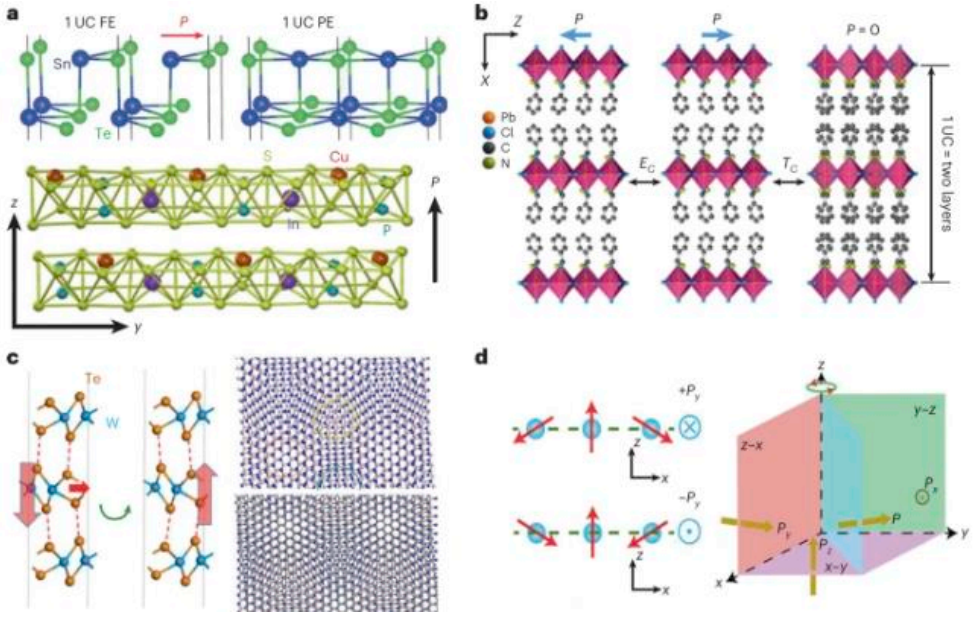

Fig. 1-4. ferroelectricity in 2D $CuInP_2S_6$, BA_2PbCl_4 perovskite and 3R-stacking ferroelectric materials [54]

In addition to rich physical properties, because the thickness of monolayer two-dimensional material is only one or a few atomic layers, its mechanical properties are also very excellent. [55] It can withstand thousands of bends without greatly affecting its mobility and photophysical properties. This is very advantageous in emerging flexible circuits and displays. Fig. 1-5 shows that using wafer-scale monolayer MoS_2 materials, Zhang et al. successfully developed flexible high-performance transistors and display backplane circuits. [56]

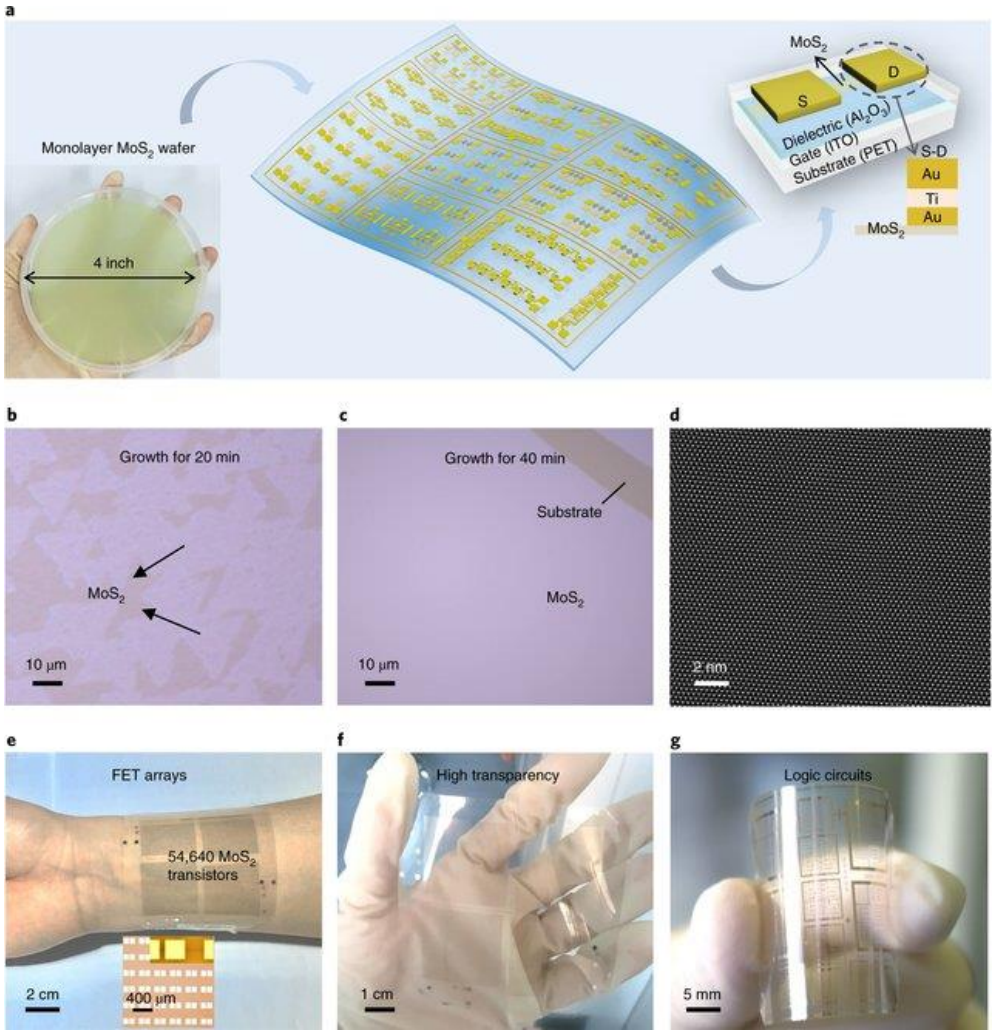

Fig. 1-5. Wafer-scale 2D MoS_2 transistors and circuits [56]

1.1.3. 2D Materials for More than Moore

In recent years, many work have been done in scaling down the size of 2D transistors, while endowing 2D devices more functions is also an important approach to enrich the complexity of chips. (Fig. 1-6) [57] More than Moore involves integrating new functionalities into 2D devices beyond traditional scaling. This includes adding capabilities like sensing, communication, memory, computing, energy harvesting and integrated functions. [58-59]

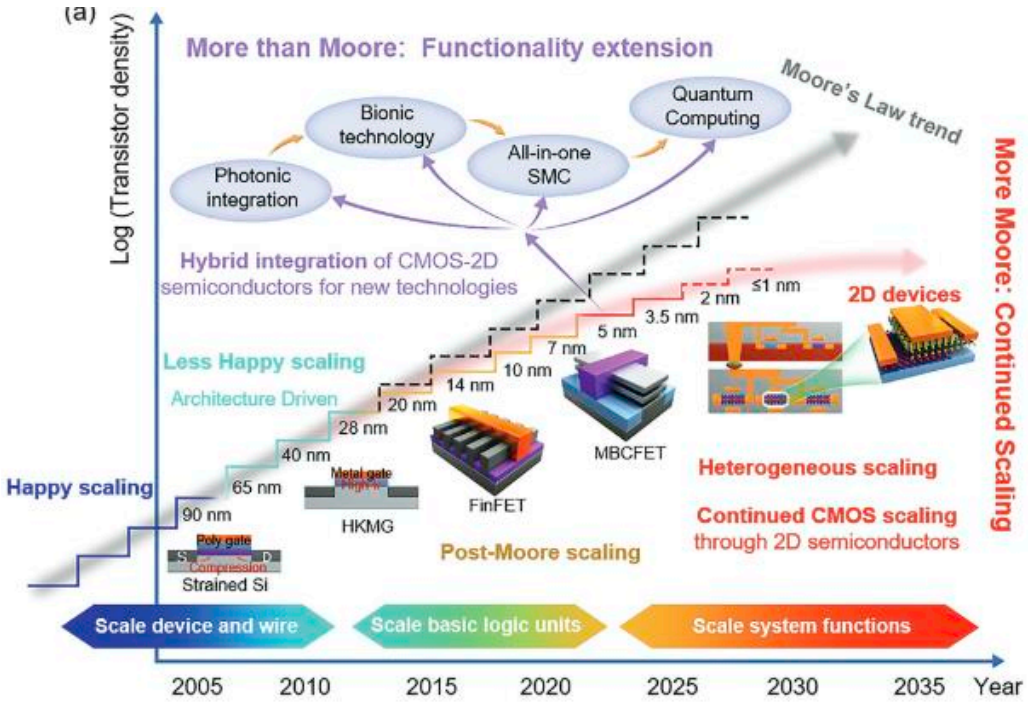

Fig. 1-6. 2D materials scaling for More Moore and More than Moore. [58]

In tradition computer structure, the parts of computing unit and memory unit are separated. It is called Von Neumann architecture. In this case, most of time and energy are used in communication between computing and memory unit, which is very energy consuming. [59] In recent years, researchers could combine memory devices and computing in 2D devices. Detailly, the conductance of 2D memory devices could be tuned continuously with external electrical field, and the results could be memorized in the same device at the same time. (Fig. 1-7) [60-62] This means that we could realize memory and computing functions in the same device (in-memory computing). It could save most of time and energy for whole systems. Due to the optoelectrical properties of 2D materials, light and magnetic signals could also affect the transport properties of 2D materials. Using these signals as an external gate, sensing, computing and memory functions could be realized at the same time, which called in-sensor computing or sensing-memory-computing integration. [63]

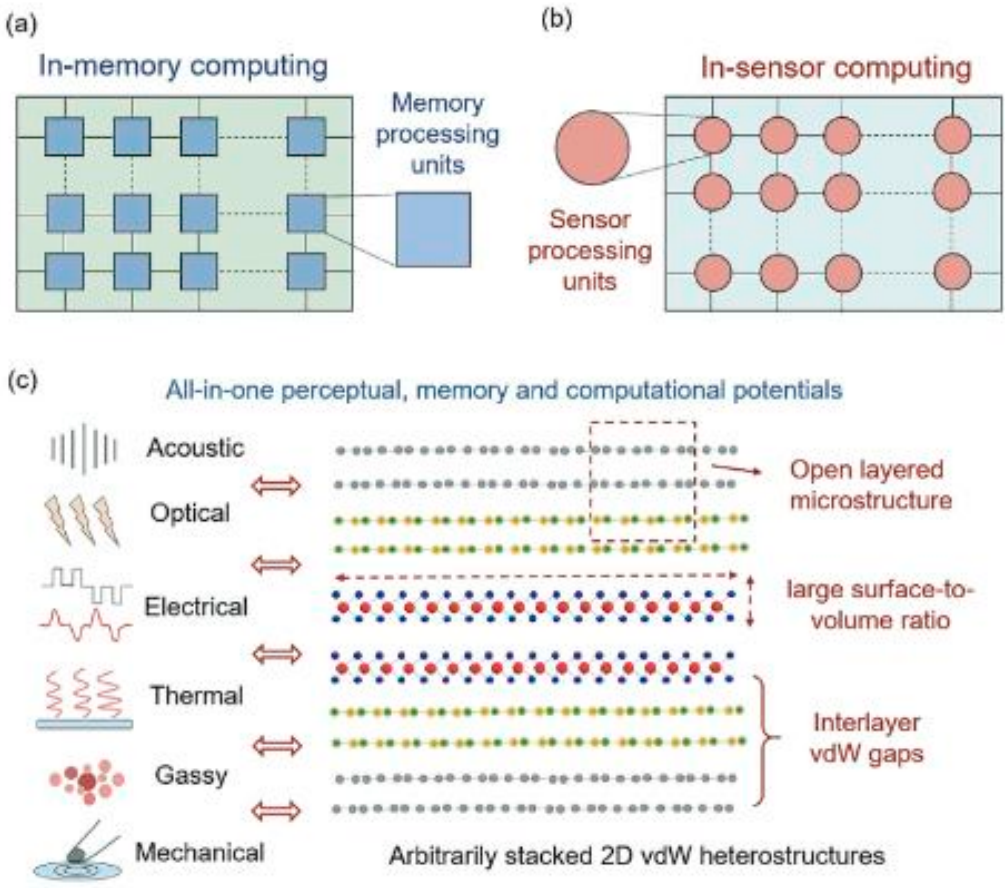

Fig. 1-7. Schematic of in-memory computing and in-sensor computing with 2D materials and devices. [63]

1.2. Problem statement

1.2.1. CVD of high-quality 2D materials

For chip-level wafer-scale 2D materials, sulfide defects and crystalline boundaries are two main factors on the quality, which could induce carrier scattering. To acquire high-quality 2D materials, low defect density and high-oriented films are wanted. Wei et al. introduce small account oxygen gas during MoS_2 monolayer. [64] By oxygen doping, the density of sulfide vacancy is greatly reduced. Accordingly, the on-state current and mobility are improved. For domain orientation control, Zhang group and Wang group have realized single-oriented

CVD growth of MoS_2 monolayer film via buffer layer and substrate engineering. (Fig. 1-8) [65-66] However, except MoS_2, the wafer-scale growth of other high-quality 2D materials with low defect density and controlled orientation is still not reported.

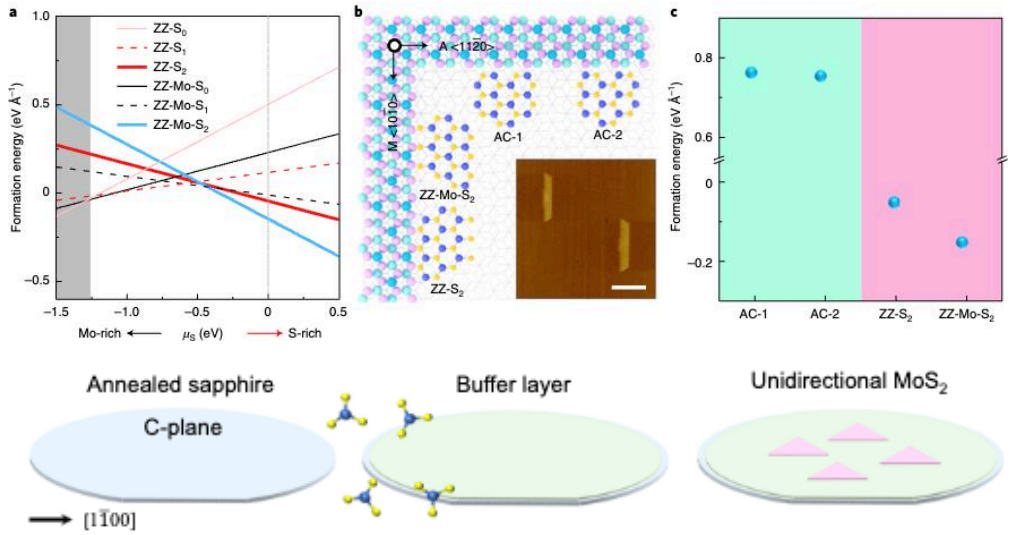

Fig. 1-8. Single-oriented MoS_2 growth via buffer layer and substrate engineering. [65-66]

1.2.2. Small equivalent-oxide-thickness dielectrics for MoS_2 transistors

HfO_2 and Al_2O_3 are two traditional dielectrics for field-effect transistors. At present, the thickness of these materials is still larger than 3 nm, thus the EOT of which are large than 1 nm. According to the IRDS 2024, the EOT of 2D materials transistors should be scaled down to 0.7 nm. Hence, developing a 2D materials compatible wafer-scale insulator film with low leakage current and high dielectric constant is emergency.

1.2.3. High-quality 2D field-effect transistors preparation

At present, most high-quality 2D materials are epitaxially grown on the sapphire or silicon oxide substrate. When fabricating devices, these materials need to be

transferred to the target substrate. Dry transfer and wet transferred are two methods while the residues are unavoidable. For high-quality 2D field-effect transistors preparation, transfer process in an important and critical step. Metal contact is another crucial procedure for high-quality 2D devices. The thickness of 2D materials is only one or a few atoms. Too high deposition velocity during metal contact deposition would break local surface, forming Schottky metal-semiconductor contact. In this case, the on/off ratio, saturation current and SS of 2D transistors would be affected.

1.3. Research objectives

In this PhD thesis, I concentrated on the 2D field-effect transistors performance from the angle of 2D materials and high-κ dielectrics. I will introduce high-quality wafer-scale chemical vapor deposition of $MoSe_2$ film and high-performance $MoSe_2$ transistors in Chapter 3. An ultrathin HfO2 film with modified oxidation atomic layer deposition method is reported in Chapter 4. It shows an ultrasmall EOT of 0.27 nm, which is the smllest value in litheratures.

1.4. Methodology

In this thesis, the 2D materials are grown with chemical vapor deposition. I will compare different growth parameters to acquire high-quality $MoSe_2$ film. TEM, Raman and PL are used to evaluate the quality and electrical measurement is also an important parameter and results. For device fabrication, standard fabrication procedures, such as UV lithography, electron beam evaporation and reactive ion beam etching, are used.

1.5. References

1. FAN, L., HUANG, C., ZHU, Z., LIU, H. & MA, X. Key factors in the physical design of high-performance chips. Sci. Sin. Informationis 54, 110 (2024).

2. Wang, Y. et al. Integration of two-dimensional materials based photodetectors for on-chip applications. Phys. Rep. 1081, 1–46 (2024).

3. Shulaker, M. M. et al. Three-dimensional integration of nanotechnologies for computing and data storage on a single chip. Nature 547, 74–78 (2017).

4. Arakawa, Y., Nakamura, T., Urino, Y. & Fujita, T. Silicon photonics for next generation system integration platform. IEEE Commun. Mag. 51, 72–77 (2013).

5. Suzuki, K., Tanaka, T., Tosaka, Y., Horie, H. & Arimoto, Y. Scaling theory for double-gate SOI MOSFET's. IEEE Trans. Electron Devices 40, 2326–2329 (1993).

6. McIntyre, P. Bulk and Interfacial Oxygen Defects in HfO_2 Gate Dielectric Stacks: A Critical Assessment. Electrochem. Soc. Trans. 11, 235–249 (2007).

7. Gopalakrishnan, K., Griffin, P. B. & Plummer, J. D. I-MOS: A Novel Semiconductor Device with a Subthreshold Slope lower than kT/q. Dig. Int. Electron Devices Meet. 289–292 (2002)

8. Yu, B. et al. FinFET Scaling to 10nm Gate Length. Dig. Int. Electron Devices Meet. 10.2.1-10.2.4 (2002)

9. Likharev, K. K. Hybrid CMOS/Nanoelectronic Circuits: Opportunities and Challenges. J. Nanoelectron. Optoelectron. 3, 203–230 (2008).

10. Choi, B.-D. & Kim, E.-S. Counting-Based Digital-to-Analog Converter Scheme for Compact Column Driver with Low-Temperature Polycrystalline Silicon Thin-Film Transistors. Jpn. J. Appl. Phys. 47, 1906 (2008).

11. Veldhorst, M. et al. A two-qubit logic gate in silicon. Nature 526, 410–414 (2015).

12. Franklin, A. D. Nanomaterials in transistors: From high-performance to thin-film applications. Science 349, aab2750 (2015).

13. Gritsenko, V. A., Perevalov, T. V. & Islamov, D. R. Electronic properties of hafnium oxide: A contribution from defects and traps. Phys. Rep. 613, 1–20 (2016).

14. Michalak, D. J. et al. Nanopatterning Si(111) surfaces as a selective surface-chemistry route. Nat. Mater. 9, 266–271 (2010).

15. Robertson, J. & Wallace, R. M. High-κ materials and metal gates for CMOS applications. Mater. Sci. Eng.: R: Rep. 88, 1–41 (2015).

16. Thompson, S. et al. A 90 nm Logic Technology Featuring 50nm Strained Silicon Channel Transistors, 7 Layers of Cu Interconnects, Low k ILD, and 1 um2 SRAM Cell. Dig. Int. Electron Devices Meet. 61–64 (2002).

17. Fu, C. et al. Understanding the microwave annealing of silicon. AIP Adv. 7, 035214 (2017).

18. Atabaki, A. H. et al. Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip. Nature 556, 349–354 (2018).

19. Vitale, S. A., Wyatt, P. W., Checka, N., Kedzierski, J. & Keast, C. L. FDSOI Process Technology for Subthreshold-Operation Ultralow-Power Electronics. Proc. IEEE 98, 333–342 (2010).

20. Huang, W. et al. Fidelity benchmarks for two-qubit gates in silicon. Nature 569, 532–536 (2019).

21. Simmons, S. A single silicon colour centre resolved. Nat. Electron. 3, 734–735 (2020).

22. Shtyk, A. & Chamon, C. Topological electronic properties of silicon. Phys. Rev. B 102, 195125 (2020).

23. Paesani, S. et al. Near-ideal spontaneous photon sources in silicon quantum photonics. Nat. Commun. 11, 2505 (2020).

24. Gramse, G. et al. Nanoscale imaging of mobile carriers and trapped charges in delta doped silicon p–n junctions. Nat. Electron. 3, 531–538 (2020).

25. Zheng, J. et al. Nonvolatile Electrically Reconfigurable Integrated Photonic Switch Enabled by a Silicon PIN Diode Heater. Adv. Mater. 32, 2001218 (2020).

26. Lou, J. et al. Multifield-Inspired Tunable Carrier Effects Based on Ferroelectric-Silicon PN Heterojunction. Adv. Electron. Mater. 6, 1900795 (2020).

27. Shiue, R.-J. et al. High-Responsivity Graphene–Boron Nitride Photodetector and Autocorrelator in a Silicon Photonic Integrated Circuit. Nano Lett. 15, 7288–7293 (2015).

28. Xu, M., Liang, T., Shi, M. & Chen, H. Graphene-Like Two-Dimensional Materials. Chem. Rev. 113, 3766–3798 (2013).

29. Shulaker, M. M. et al. Three-dimensional integration of nanotechnologies for computing and data storage on a single chip. Nature 547, 74–78 (2017).

30. Liu, G.-B., Xiao, D., Yao, Y., Xu, X. & Yao, W. Electronic structures and theoretical modelling of two-dimensional group-VIB transition metal dichalcogenides. Chem. Soc. Rev. 44, 2643–2663 (2014).

31. Jariwala, D., Sangwan, V. K., Lauhon, L. J., Marks, T. J. & Hersam, M. C. Emerging Device Applications for Semiconducting Two-Dimensional Transition Metal Dichalcogenides. ACS Nano 8, 1102–1120 (2014).

32. Li, S.-L., Tsukagoshi, K., Orgiu, E. & Samorì, P. Charge transport and mobility engineering in two-dimensional transition metal chalcogenide semiconductors. Chem. Soc. Rev. 45, 118–151 (2015).

33. Jiang, J., Xu, L., Qiu, C. & Peng, L.-M. Ballistic two-dimensional InSe transistors. Nature 616, 470–475 (2023).

34. Allain, A., Kang, J., Banerjee, K. & Kis, A. Electrical contacts to two-dimensional semiconductors. Nat. Mater. 14, 1195–1205 (2015).

35. Lei, S. et al. Optoelectronic Memory Using Two-Dimensional Materials. Nano Lett. 15, 259–265 (2015).

36. Guimarães, M. H. D. et al. Atomically Thin Ohmic Edge Contacts Between Two-Dimensional Materials. Acs Nano 10, 6392–6399 (2016).

37. Chhowalla, M., Jena, D. & Zhang, H. Two-dimensional semiconductors for transistors. Nat Rev Mater 1, 16052 (2016).

38. Raja, A. et al. Coulomb engineering of the bandgap and excitons in two-dimensional materials. Nat. Commun. 8, 15251 (2017).

39. Lo, C.-L. et al. Studies of two-dimensional h-BN and MoS2 for potential diffusion barrier application in copper interconnect technology. npj 2D Mater. Appl. 1, 42 (2017).

40. Resta, G. V. et al. Doping-Free Complementary Logic Gates Enabled by Two-Dimensional Polarity-Controllable Transistors. Acs Nano 12, 7039–7047 (2018).

41. Grisafe, B., Zhao, R., Ghosh, R. K., Robinson, J. A. & Datta, S. Electrically triggered insulator-to-metal phase transition in two-dimensional (2D) heterostructures. Appl Phys Lett 113, 142101 (2018).

42. Rivera, P. et al. Valley-polarized exciton dynamics in a 2D semiconductor heterostructure. Science 351, 688–691 (2016).

43. Mueller, T. & Malic, E. Exciton physics and device application of two-dimensional transition metal dichalcogenide semiconductors. npj 2D Mater. Appl. 2, 29 (2018).

44. Li, L. J. et al. Controlling many-body states by the electric-field effect in a two-dimensional material. Nature 529, 185–189 (2016).

45. Gong, C. et al. Discovery of intrinsic ferromagnetism in two-dimensional van der Waals crystals. Nature 546, 265–269 (2017).

46. Kang, K. et al. Layer-by-layer assembly of two-dimensional materials into wafer-scale heterostructures. Nature 550, 229–233 (2017).

47. Raja, A. et al. Coulomb engineering of the bandgap and excitons in two-dimensional materials. Nat. Commun. 8, 15251 (2017).

48. Li, L. & Wu, M. Binary Compound Bilayer and Multilayer with Vertical Polarizations: Two-Dimensional Ferroelectrics, Multiferroics, and Nanogenerators. ACS Nano 11, 6382–6388 (2017).

49. Fei, Z. et al. Ferroelectric switching of a two-dimensional metal. Nature 560, 336–339 (2018).

50. Mennel, L. et al. Optical imaging of strain in two-dimensional crystals. Nat. Commun. 9, 516 (2018).

51. Wang, Y. et al. Van der Waals contacts between three-dimensional metals and two-dimensional semiconductors. Nature 568, 70–74 (2019).

52. Wang, Y. et al. Van der Waals contacts between three-dimensional metals and two-dimensional semiconductors. Nature 568, 70–74 (2019).

53. Sun, Y. et al. Hybrid System Combining Two-Dimensional Materials and Ferroelectrics and Its Application in Photodetection. Acs Nano 15, 10982–11013 (2021).

54. Wang, C., You, L., Cobden, D. & Wang, J. Towards two-dimensional van der Waals ferroelectrics. Nat. Mater. 22, 542–552 (2023)

55. Wu, M. Two-Dimensional van der Waals Ferroelectrics: Scientific and Technological Opportunities. Acs Nano 15, 9229–9237 (2021).

56. Li, N. et al. Large-scale flexible and transparent electronics based on monolayer molybdenum disulfide field-effect transistors. Nat. Electron. 3, 711–717 (2020).

57. Meng, L. et al. Anomalous thickness dependence of Curie temperature in air-stable two-dimensional ferromagnetic 1T-$CrTe_2$ grown by chemical vapor deposition. Nat. Commun. 12, 809 (2021).

58. Wang, S., Liu, X. & Zhou, P. The Road for 2D Semiconductors in the Silicon Age. Adv. Mater. 34, e2106886 (2022).

59. Lee, D. H., Choi, S.-J., Kim, H., Kim, Y.-S. & Jung, S. Direct probing of phonon mode specific electron–phonon scatterings in two-dimensional semiconductor transition metal dichalcogenides. Nat. Commun. 12, 4520 (2021).

60. Wang, P. et al. Controlled Syntheses and Multifunctional Applications of Two-Dimensional Metallic Transition Metal Dichalcogenides. Acc. Mater. Res. 2, 751–763 (2021).

61. Cui, Q., Zhu, Y., Liang, J., Cui, P. & Yang, H. Spin-valley coupling in a two-dimensional VSi2N4 monolayer. Phys. Rev. B 103, 085421 (2021).

62. Caruso, F. et al. Two-dimensional plasmonic polarons in n-doped monolayer MoS_2. Phys. Rev. B 103, 205152 (2021).

63. Zhu, C. S. et al. Evolution of transport properties in FeSe thin flakes with thickness approaching the two-dimensional limit. Phys. Rev. B 104, 024509 (2021).

64. Shahnazaryan, V. & Rostami, H. Nonlinear exciton drift in piezoelectric two-dimensional materials. Phys. Rev. B 104, 085405 (2021).

65. Li, L. et al. Epitaxy of wafer-scale single-crystal MoS2 monolayer via buffer layer control. Nat. Commun. 15, 1825 (2024).

66. Li, T. et al. Epitaxial growth of wafer-scale molybdenum disulfide semiconductor single crystals on sapphire. Nat. Nanotechnol. 16, 1201–1207 (2020).

Chapter 2. Literature review

In this chapter, I will review recent progress of two-dimensional transition metal dichalcogenide (TMD) synthesis and dielectric. In the first part, six materials synthesis methods are introduced, including mechanical exfoliation, electrochemical intercalated exfoliation, molecular beam epitaxy, chemical vapor deposition, atomic layer deposition. In the second part, five type of dielectric materials are introduced, including conventional oxide, 2D materials, perovskite, molecular film and ionic materials.

2.1. Synthesis of TMD review

2.1.1. Mechanical exfoliation

Machine exfoliation is the first and most effective way to prepare 2D materials since 2004. [1] Adhesive tape is usually used to stick to the crystal material and peel it by using the characteristics of weak van der Waals forces between the layers of two-dimensional materials, which are easily destroyed by external forces applied. [2] This method can obtain thin layers of materials with close to crystal quality, but the yield is extremely low, large-area peeling is limited and very uneven [3-4], which will introduce folds and damage in the sample.

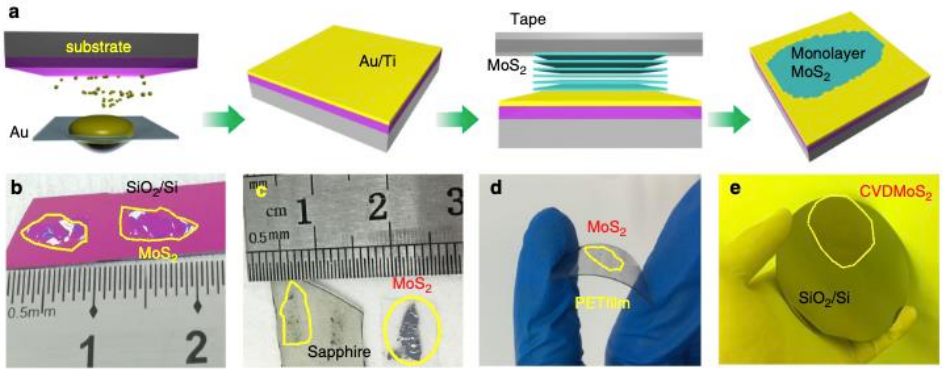

Fig. 2-1. Preparation of large-area MoS_2 by mechanical exfoliation [5]

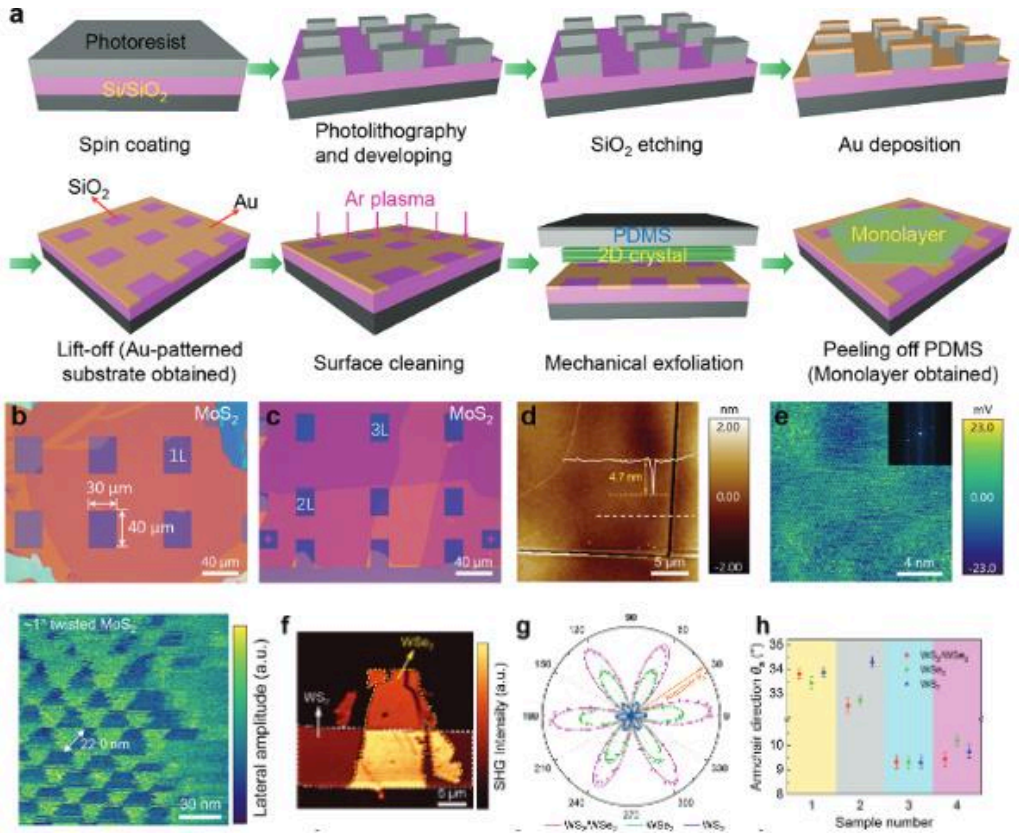

Fig. 2-2. Gold-template-assisted methods to construct monolayer or multilayer superlattice. [11]

At present, there are also auxiliary stripping methods that can prepare a large area of TMDs material. [5-6] As shown in Fig. 2-1, gold metal (Au) is deposited on the substrate surface covered with thin metal titanium (Ti) or chromium (Cr). According to the principle that the interaction between sulfur on the surface of Au and MoS_2 is stronger than the van der Waals interaction force between MoS_2 layers [7-9], After contact with the crystal, apply slight pressure with the tape, and then lift the tape to tear off most of the crystal, leaving a large area of single-layer MoS_2 film on the gold surface [10]. This method can obtain a high-quality single-layer material at the maximum millimeter level, but it is limited by the presence of metal, and there are certain difficulties in device fabrication. For example, Wu et al. reported a gold-template-assisted method to construct monolayer, multilayer or superlattices. (Fig. 2-2) [11] This method provides a general platform to exfoliate

high-quality and clean 2D materials and study their intrinsic optical and electrical transport properties.

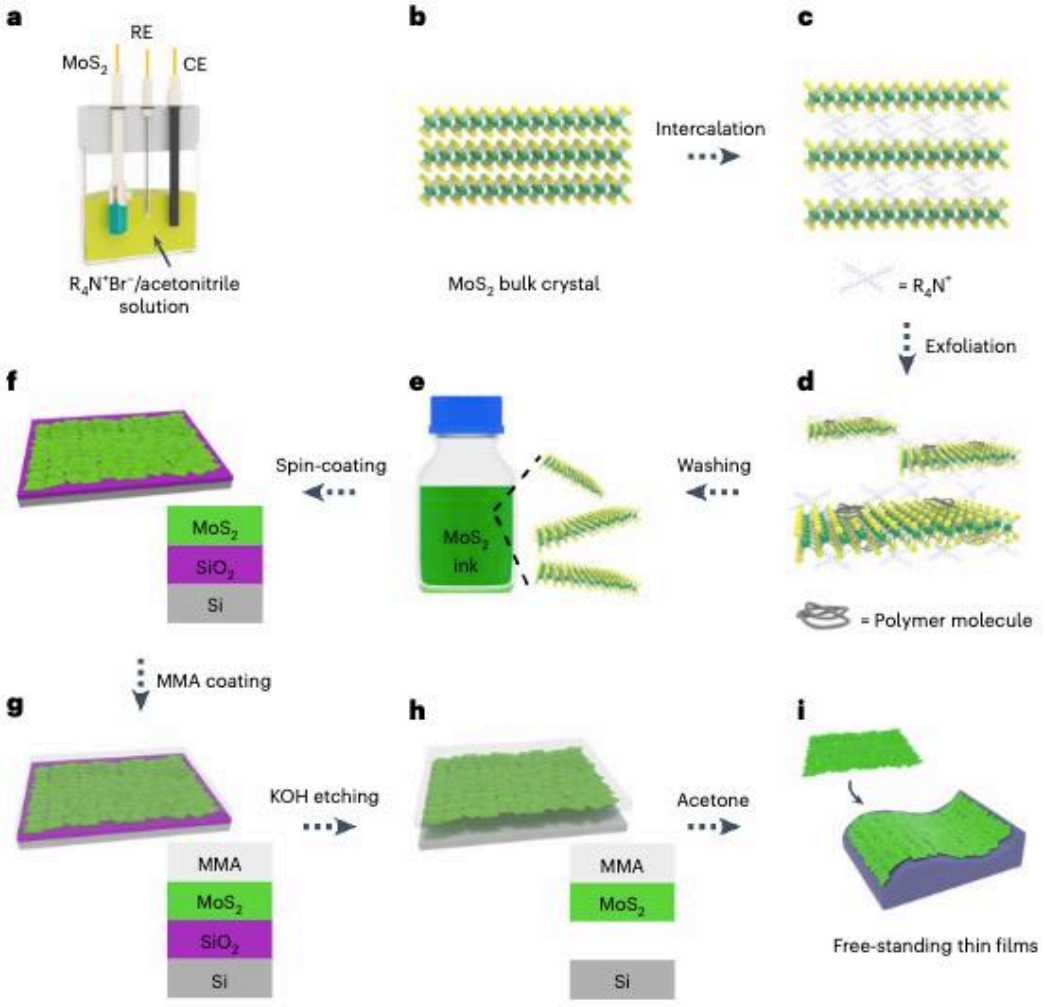

Fig. 2-3. Schematic illustration of electrochemical intercalated exfoliation [12]

2.1.2. Electrochemical intercalated exfoliation

Electrochemical intercalated exfoliation (Fig. 2-3) takes advantage of the weak van der Waals interaction between the layers of TMDs material, which is easy to be destroyed. [12] Through the action of surfactants or ions, the bulk material can be dispersed into thin layers in solution. This method can quickly prepare a large amount of thin TMDs materials while the probability of obtaining a single layer is

small, the size is limited, and the organic solvent is usually more toxic [13-15], so it is not suitable for practical applications. Fig. 2-4 shows that the ultrasonic powder is immersed in N-methylpyrrolidone (NMP) solvent for reaction, and a library of 2D nanosheets of different thickness can be prepared. From the optical and SEM images, it can be seen that the sample layers obtained by this method are not evenly distributed and have different sizes. It is difficult to prepare devices uniformly over a large area on the substrate [16]. In addition, there are lithium-ion intercalation methods, but it is easy to introduce defects and destroy the crystal structure [17].

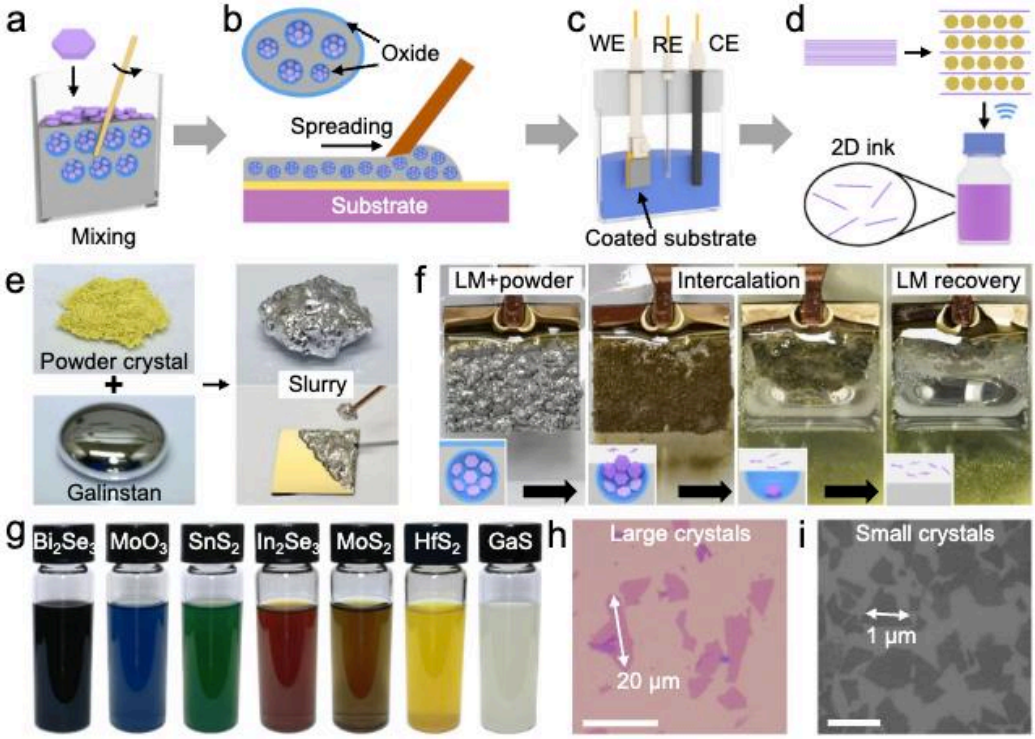

Fig. 2-4. Electrochemical intercalated exfoliation of a library of 2D materials with various size. [15]

2.1.3. Molecular beam epitaxy

Molecular Beam Epitaxy (MBE) is a method for heating and evaporating precursors in an ultra-high vacuum environment. The source atoms or atomic

clusters of evaporation move in a straight line toward the substrate and are sprayed onto the substrate for growth. The temperature and rate of molecular beam evaporation can be precisely controlled. The advantage is that the impurities are less, and the quality of the crystals grown is higher, but the instrument is complicated to operate, and the growth time is long and the cost is high. At present, the electrical properties of molybdenum diselenide prepared by MBE growth are still not ideal [18-19]. Fig. 2-5 shows the equipment and growth principle of MBE. [20] High-quality $MoSe_2$, CrI_3 and $CrTe_2$ have been grown with MBE, but the film is discontinuous, and the growth rate is very slow, only 1μm /min, which is difficult to meet the needs of large-area growth (Fig. 2-6) [21-24].

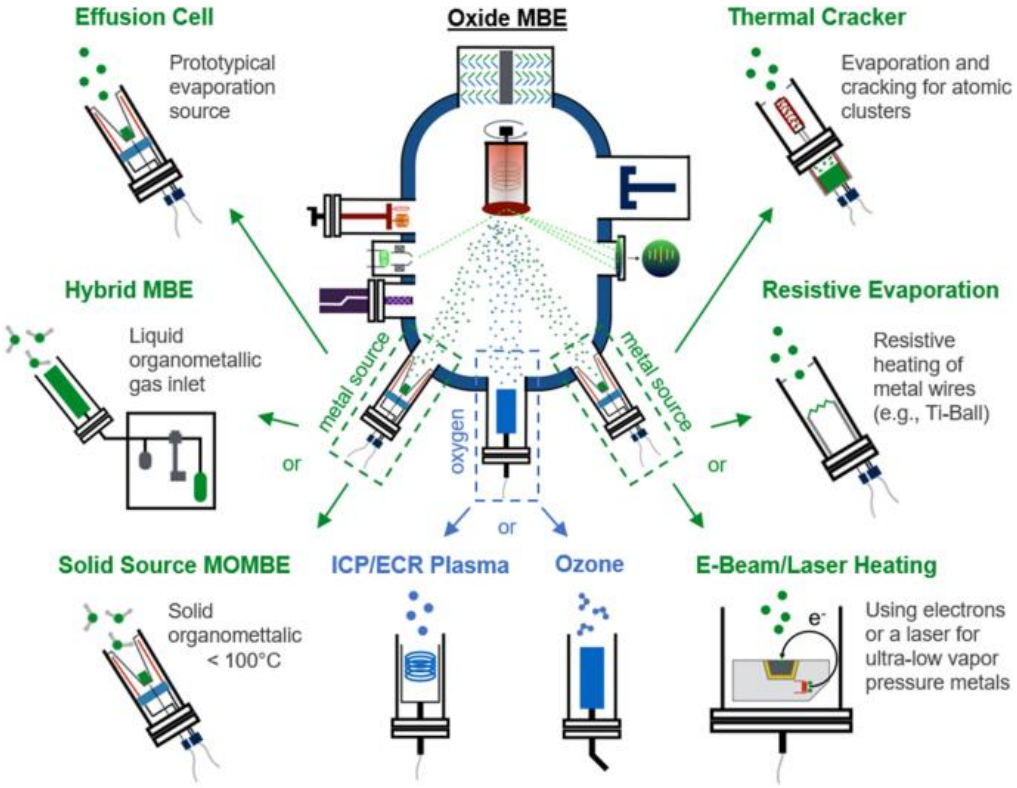

Fig. 2-5. Scheme of equipment and growth principle of MBE. [20]

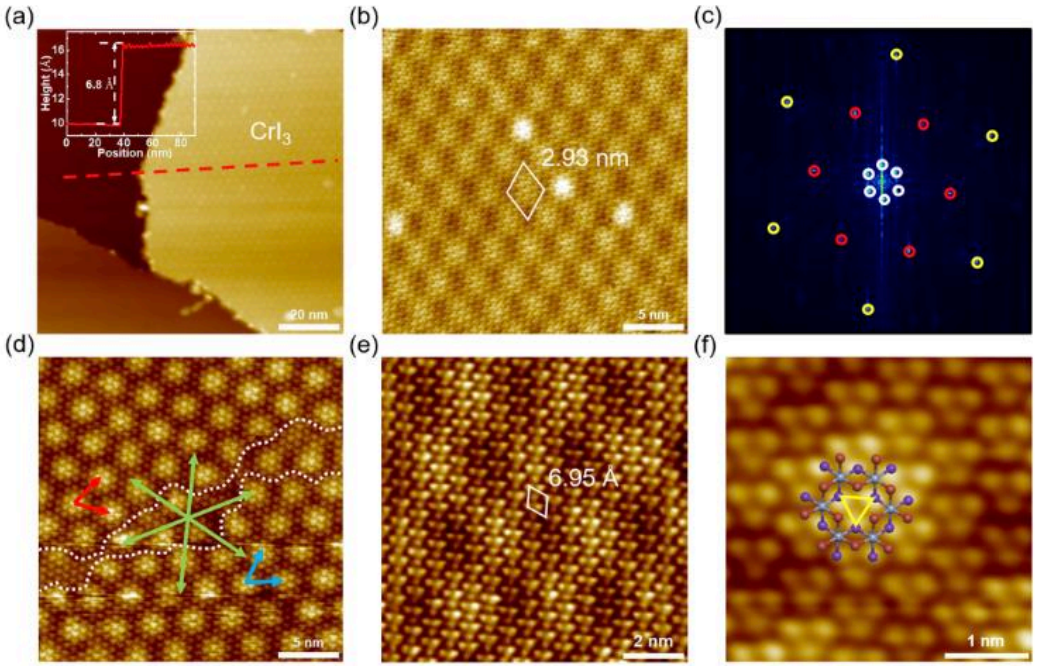

Fig. 2-6. STM of MBE-grown CrI_3 film [21]

2.1.4. Chemical vapor deposition

Chemical Vapor Deposition (CVD) is a commonly used controllable epitaxy method to synthesize 2D materials, such as metallic graphene, semiconducting MoS_2 and insulating hBN. With the advantages of simple equipment construction and easy regulation of reaction parameters, it has become a major method for epitaxy growth of two-dimensional materials [25-27]. According to the different pressure during the reaction, it can be divided into atmospheric pressure CVD (APCVD) and low-pressure chemical vapor deposition (LPCVD), under normal circumstances, the lower the pressure. (Fig. 2-7) The faster the gas flows in the cavity, the more uniform the transmission of the evaporation source, the better the deposition result, the lower the concentration of the evaporated precursor, which is more conducive to regulation, but requires a higher growth temperature. In the growth of large-area TMDs films, LPCVD is commonly used [28-30].

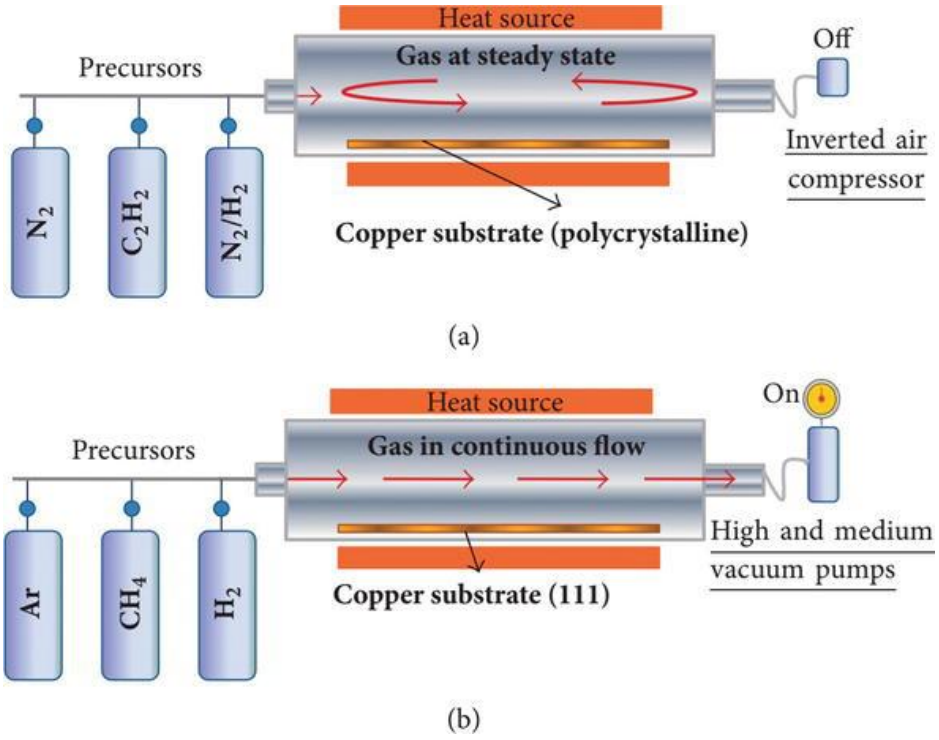

Fig. 2-7. Schematic illustration of APCVD and LPCVD

The precursor is a gas containing selenium and molybdenum, and the reaction mode is metal-organic CVD (MOCVD). Metal-organic precursors can exist stably in the cavity and decompose after reaching a certain temperature to provide the elements needed for growth. The advantage is that the precise control of the gas source can be achieved, the gas flow rate of the input cavity can be controlled, and the concentration can be maintained for a long time, which is favorable for the controlled growth of a large area continuous film [31-32].

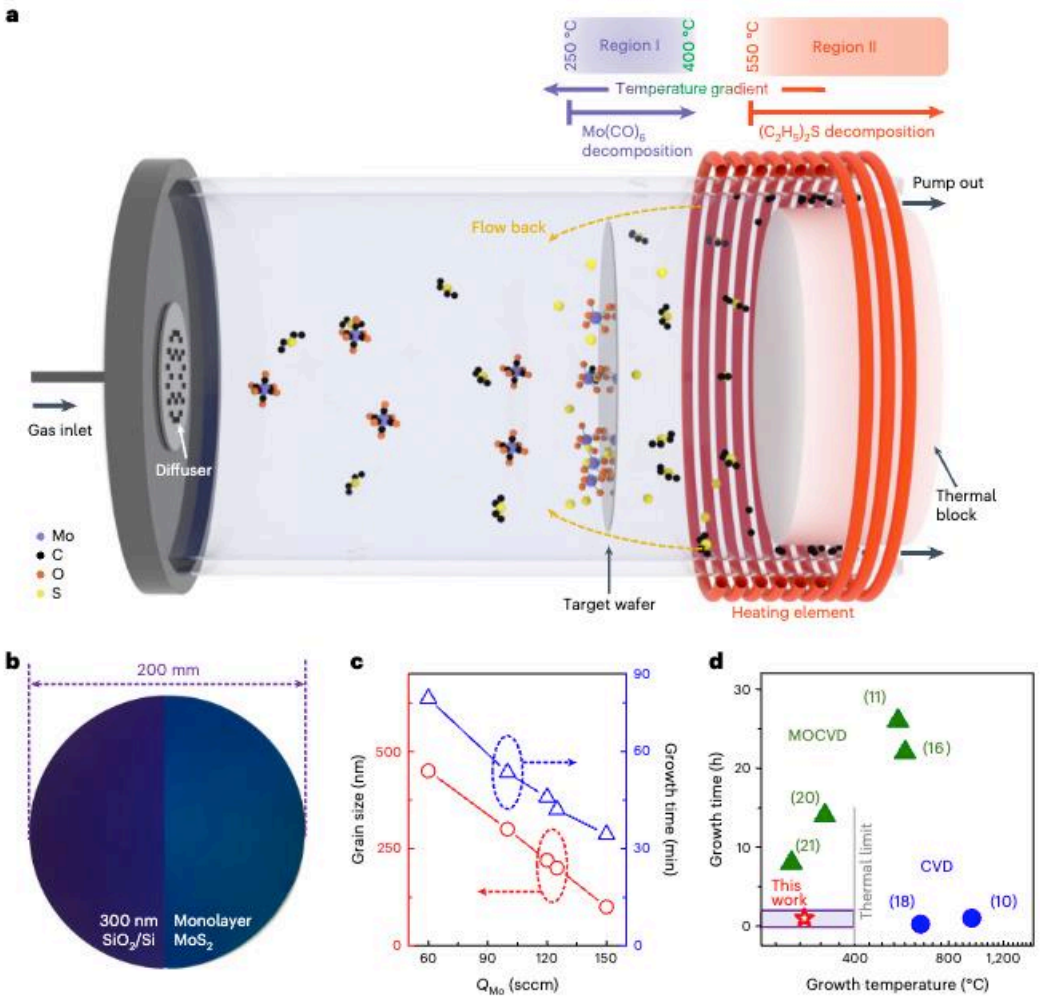

Fig. 2-8. MOCVD grown 200-mm MoS_2 monolayer film. [31]

The choice of substrate is also very important for CVD growth of 2D materials. In previous studies, silica [32], mica [33], gold [34], tungsten foil [35] or glass [36] were commonly used as substrates for growth. However, in actual growth, symmetry matching between material and substrate greatly affects wafer-level epitaxial growth [37]. C-plane sapphire has a specific lattice orientation, and the surface is smooth and flat after treatment, which can be used as the substrate of epitaxial growth TMDs material. In recent literature reports, 2D TMDs materials can induce single-oriented grain growth by steps on the sapphire surface [38-40], in addition, it has been recently reported that Au substrates can also induce single-

oriented TMDs films by steps [41], which provides a reference for achieving high-quality, crystal boundary free single-crystal film epitaxy. In addition, TMDs films with different morphologies can be grown depending on the location of substrate placement. For example, when the substrate is placed vertically compared with horizontally, the area and grain size of the continuous MoS_2 film obtained by epitaxy on the vertically placed substrate are larger [42]. Vertical placement can make the source more evenly dispersed on the substrate. A uniform wafer-scale $MoSe_2$ continuous film was obtained [43].

2.1.5. Atomic layer deposition

Atomic layer deposition (ALD) is a CMOS-compatible technology, which could operate at low temperature and deposit wafer-scale film. [44] In conventional 2D transistors fabrication, ALD is used to deposition insulators as dielectric layer while Tan et al. grew monolayer or few-layer MoS_2 film using ALD at 300 °C on sapphire with $MoCl_5$ and H_2S as sources. [45]

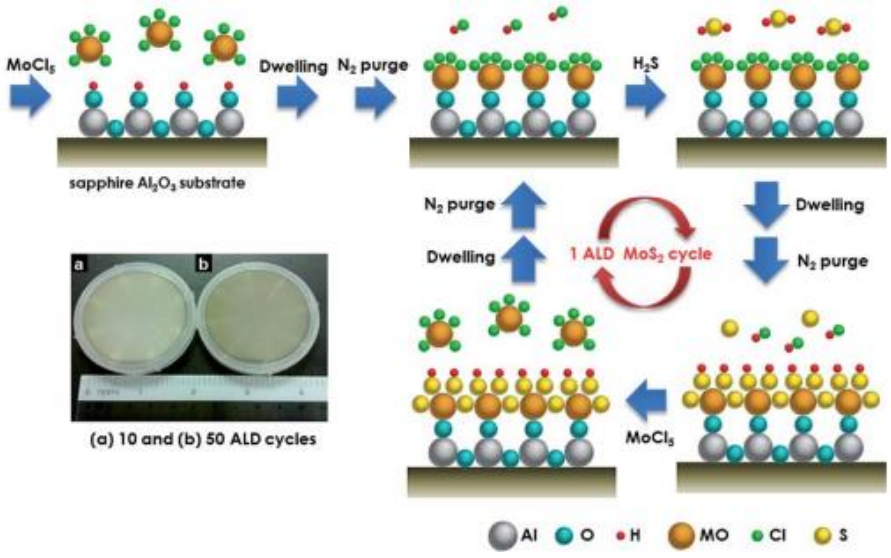

Fig. 2-9. Scheme of MoS_2 growth with ALD. [45]

2.2. Dielectric review

Dielectrics is an insulator that could be polarized under the external electrical fields. [46] When applying an external electrical field, positive and negative charges would move from the equilibrium positions to the opposite direction of the field direction. [47] As shown in the Fig. 2-10, these charges arise from the dipoles, ions and electrons, resulting in electronic, ionic and electrode polarization. After removing the external electrical field, these charges will move back to the equilibrium positions. [48]

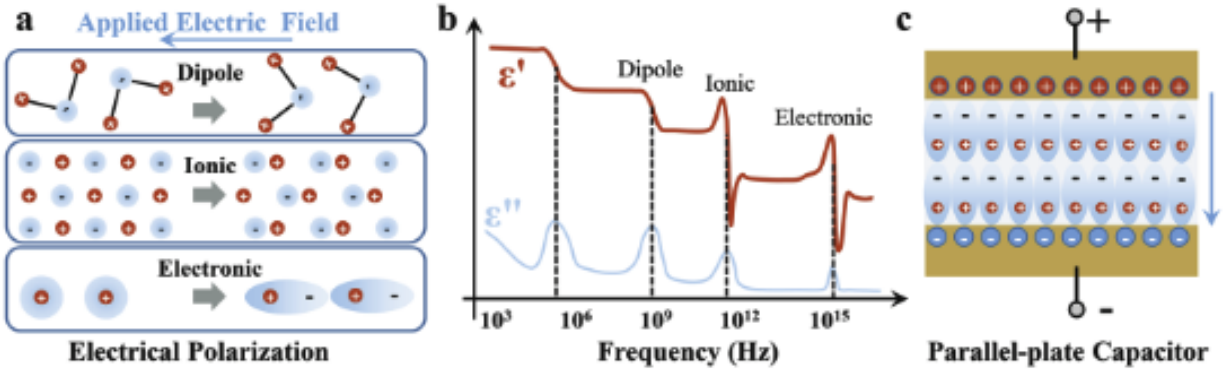

Fig. 2-10. Physical principles of dielectric materials. [48]

One of the most important application of dielectrics is properly working as a block of the field-effect transistors, in which the conductance of the channel semiconductor is tuned by gate via dielectric polarization. Since 45 nm node silicon transistors were invented in 2000, silicon oxide were replaced by high-κ dielectric materials, such as HfO_2 and ZrO_2, for getting a higher capacitance with a thinner dielectrics. [49-50]

For dielectrics, two intrinsic properties are important:

(1) The first one is bandgap. A large bandgap is desired for blocking gate leakage current, thus lowering the energy consumption of the devices. [51]

(2) The second one is relatively large dielectric constant, so as to enhance the gate controllability and reduce operation voltage. A dielectric constant of 10-30 is desired while too large dielectric constant is not wanted. This is because too high dielectric constant brings high dielectric loss, unavoidable hysteresis and source-induced leakage. [52]

(3) The third one is the quality of the dielectric film. The less defects in the film, the better the dielectric film is. Taking HfO_2 film as an example, if too many oxygen defects exist in the dielectric film, these defects will trap electrons when applying gate voltage, and then a large hysteresis emerges in the transfer curve of the transistor. This will induce the increasement of device variation. (Fig. 2-11) In addition, large concentration of oxygen defects will enlarge the gate leakage, because of the reduction of tunneling barrier comparing with dielectrics with less defects. [53]

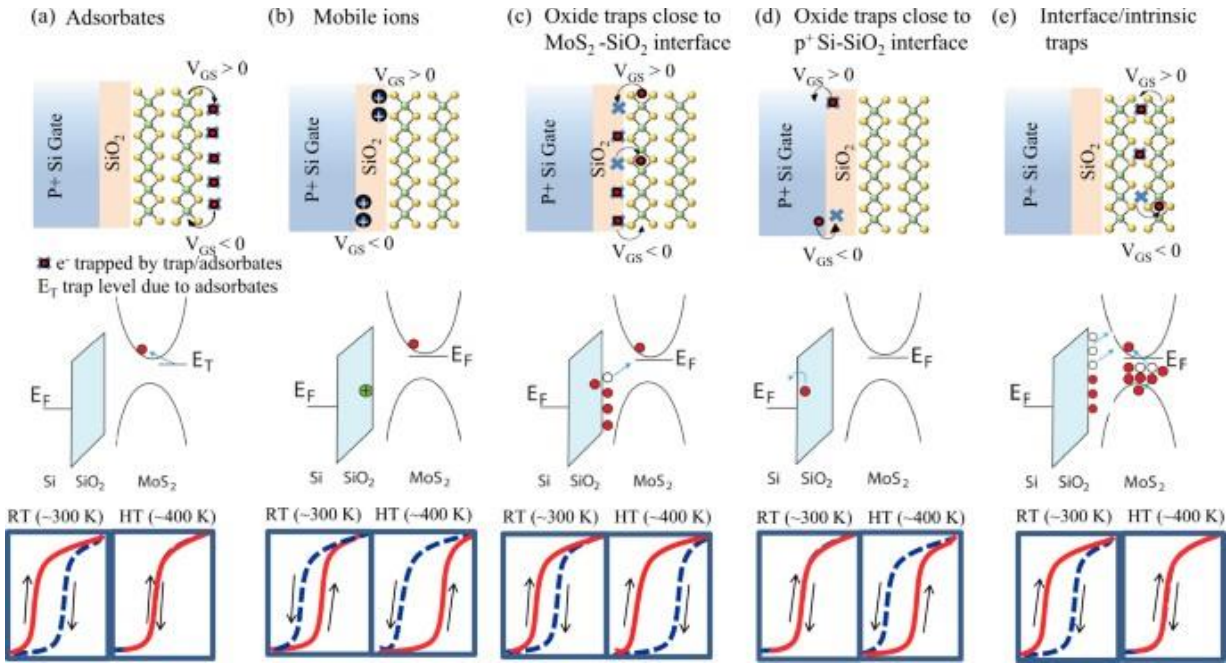

Fig. 2-11. Scheme of hystersis in 2D transistors. [53]

2.2.1. Conventional oxide dielectrics for 2D transistors

Due to the atomic flat and dangling bonds-free surface of 2D materials, traditional dielectric, such as HfO_2 and Al_2O_3, cannot deposit directly on 2D materials channel. [54] But they are still good candidate for metal gate/high-κ stack back-gated 2D transistors. Tang et al. reported scalable MoS2 transistors with 10 nm HfO_2 dielectrics. [55] These transistors show a large one-state current density around 750 μA/μm and small SS of 75 mV/dev. The hysteresis is only 11.5 mV, which could prove the high quality of HfO_2 dielectric film and great carrier controllability for MoS_2 channel.

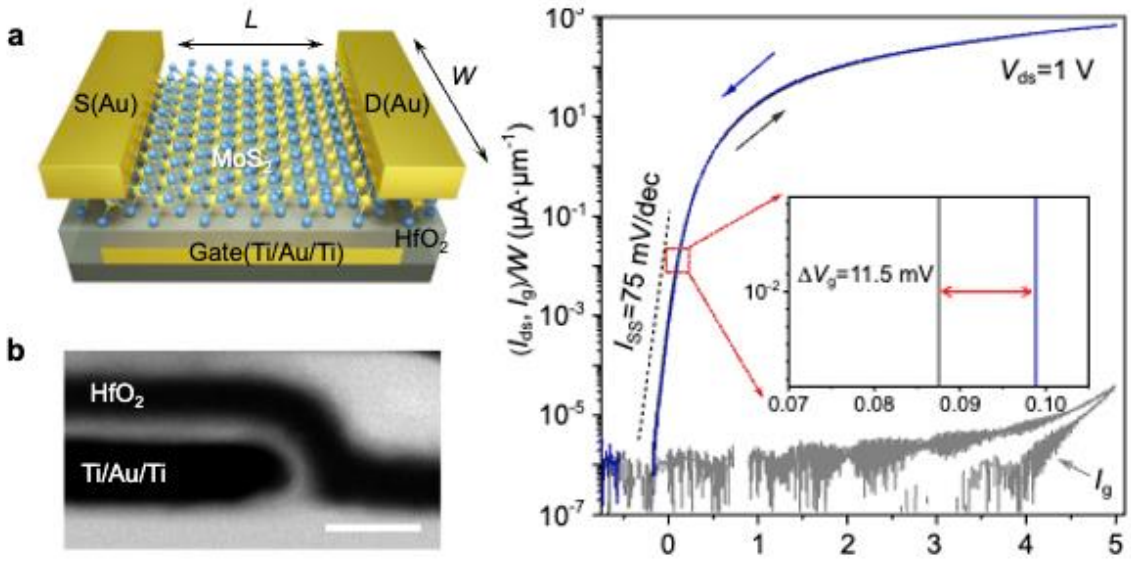

Fig. 2-12. MoS_2 back-gated transistors with HfO_2 dielectrics [55]

Although the dangling-free surface of 2D materials is not suitable for directly deposit oxide high-κ film, some approaches have been applied to make oxide dielectrics adapt with 2D materials, such as plasma process and seed layer. Peng et al. transferred one-layer MoS_2 to the channel MoS_2, and then used oxygen plasma to oxide the upper layer, so as to create a layer that could be deposited oxide directly. [56]

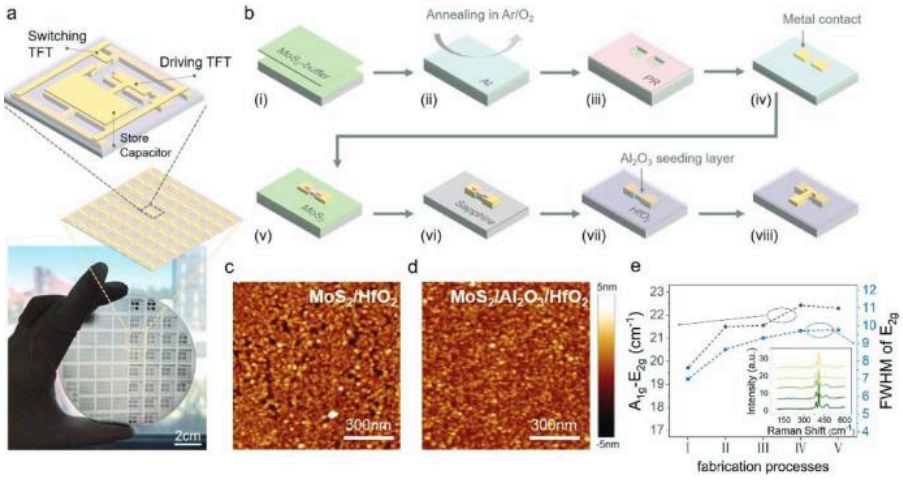

Fig. 2-13. Scheme of top-gated MoS_2 transistors fabrication with plasma-treated process. [56]

Except from the traditional HfO_2 dielectrics, some emerging dielectrics designed for 2D materials have been reported recently. For example, 2D Bi_2SeO5, $SrTiO_3$ perovskite, Sb_2O_3 molecular crystals and CaF_2 ion crystals. These dielectrics provide a platform for high-performance 2D transistors with ideal SS, small EOT and zero hysteresis. [58-61]

2.2.2. 2D dielectrics

2D materials could be stacked via vdW interaction. This inspires use 2D insulators as dielectrics for all-2D transistors. [62-63] hBN is such a 2D insulator with large bandgap and a suitable dielectric constant. Wu et al. have fabricated InSe transistors and charge-trap memory (flash memory) with hBN as dielectric layer or tunneling layer. [64] Because of the layered structure and high crystalline quality, thick BN could also act as isolating layer, which could shield interlayer current or voltage, so as to realize monolithic 3D stacking. [65]

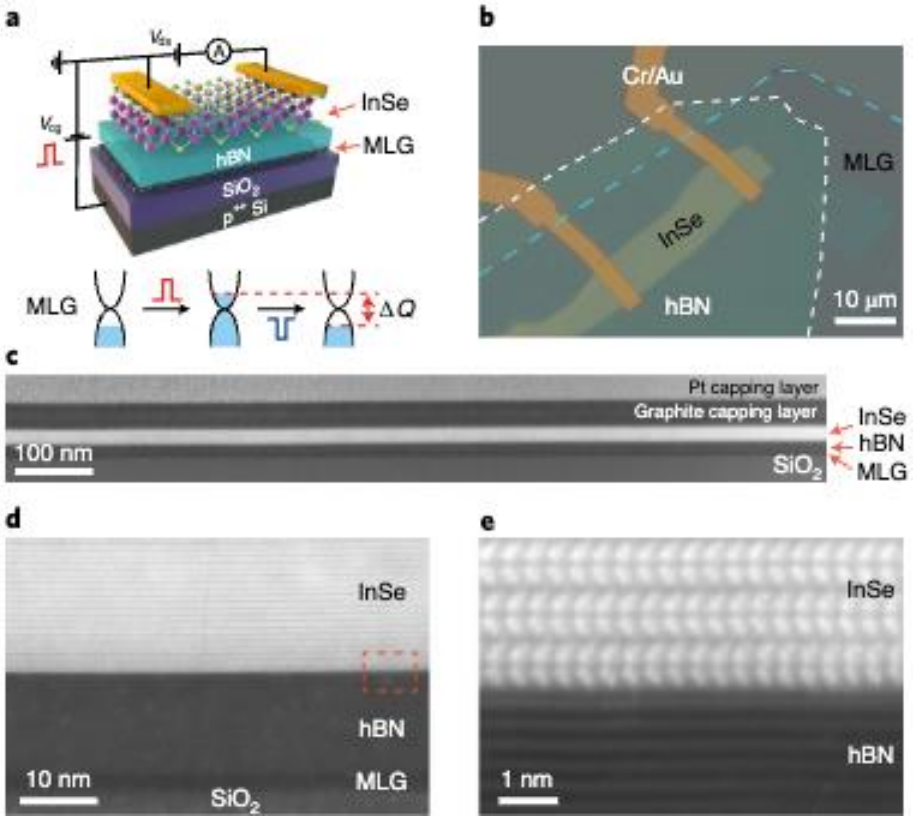

Fig. 2-14. Flash memory based on hBN dielectrics [64]

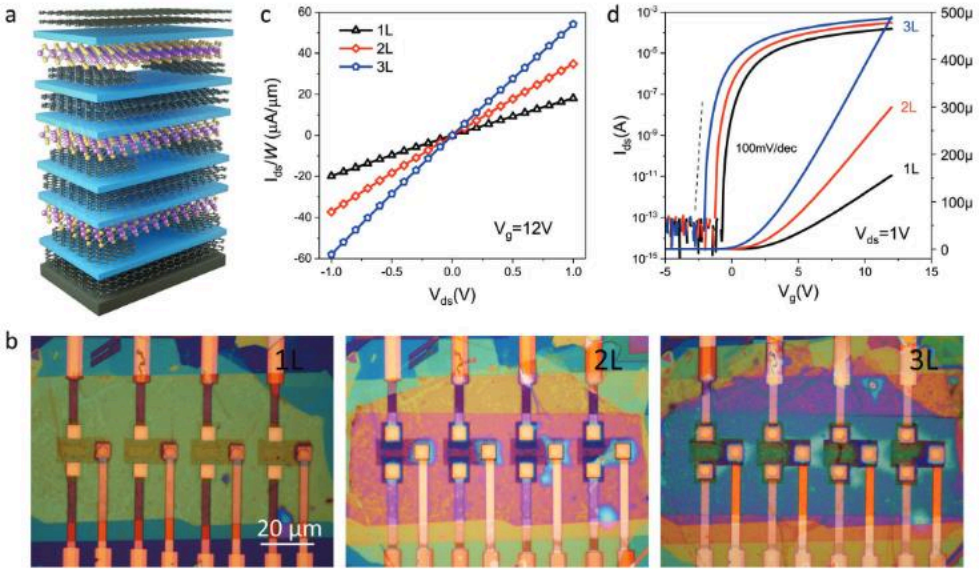

Fig. 2-15. Vertically stacked all 2D transistors with BN as isolating layer and dielectric layer. [65]

Bi_2OSe_5 is another 2D insulator. Its dielectric constant is much higher than hBN, thus could get ultrasmall equivalent oxide thickness below 5 A. Zhang et al. applied in-situ oxidation method to make Bi_2SeO_5 insulating dielectric from Bi_2O_2Se semiconductor. The single crystalline oxide Bi_2SeO_5 could reach a high dielectric constant of ~22 and a small leakage current of 0.015 A/cm^2 at gate voltage of 1 V, which reach the requirement of low power limit of IRDS. [66]

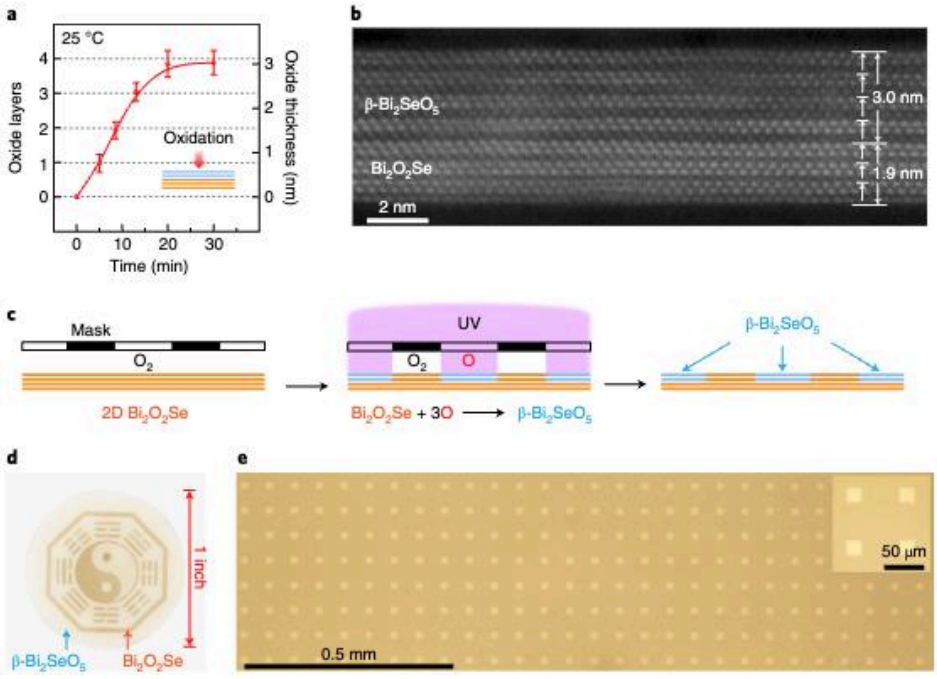

Fig. 2-16. In-situ oxidation synthesis of Bi_2SeO_5 from Bi_2O_2Se [66]

2.2.3. Perovskite dielectrics

Water-soluble $Sr_3Al_2O_6$ makes PLD-grown single-crystalline perovskite film be transferrable and can be integration with 2D materials. [67] Due to the ultrahigh dielectric constant of perovskite film, the equivalent oxide thickness of dielectric for 2D field-effect transistors could be reduced greatly. Huang et al. prepare free-standing $SrTiO_3/Sr_3Al_2O_6$ film epitaxially grown on the $SrTiO_3$ (111) substrate with pulse laser deposition. [68] The $SrTiO_3$ film shows a large dielectric constant of around 300 and small leakage current of 10^{-2} A/cm^2. For MoS_2 transistors, a

steep subthreshold swing of 70 mV/dev and large on/off ratio of 10^7. The EOT could be shrined down to sub-1-nm, much smaller than traditional HfO_2 and Al_2O_3.

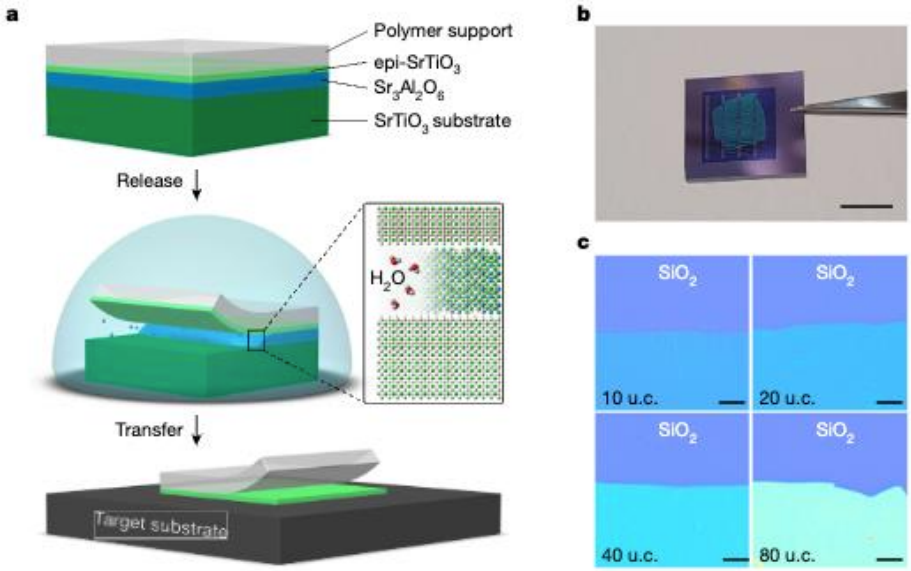

Fig. 2-17. Preparation of free-standing $SrTiO_3$ dielectrics for MoS_2 transistors [68]

2.2.4. Molecular dielectrics

Antimony trioxide is a type of inorganic molecular crystals and could be deposited with CMOS-compatible thermal evaporation deposition. Due to the low evaporation temperature around 490 °C, the Sb-O bonds cannot be broken during melting or deposition process, thus making Sb_2O_3 greatly suitable for MoS_2 transistors integration. [69] With Sb_2O_3 dielectrics, the top-gated and back-gated transistors could be fabricated successfully and reach a high on/off ratio of 10^8 and a small SS of 64 mV/dec. However, the dielectric constant is only ~11.5, not much high for MoS_2 transistors. Xu et al. designed hybrid Sb_2O_3/HfO_2 integration with molecular Sb_2O_3 as buffer layer. The EOT could be scaled down to 0.67 nm and the SS approaches the thermionic of 60 mV/dec. [70]

2.2.5. Ionic dielectrics

Fluoride ionic crystals is another type of insulator with high dielectric capability. The large ionic radius impedes the fluoride ion migration under gate voltage, which reduce the leakage current greatly. LaF_3, CaF_2, CeF_3 have been proved as excellent dielectrics for MoS_2 transistors with high on/off ratio of 10^8, an ultralow SS around 65 mV/dec and low current leakage below 10^{-6} A/cm^2. [71]

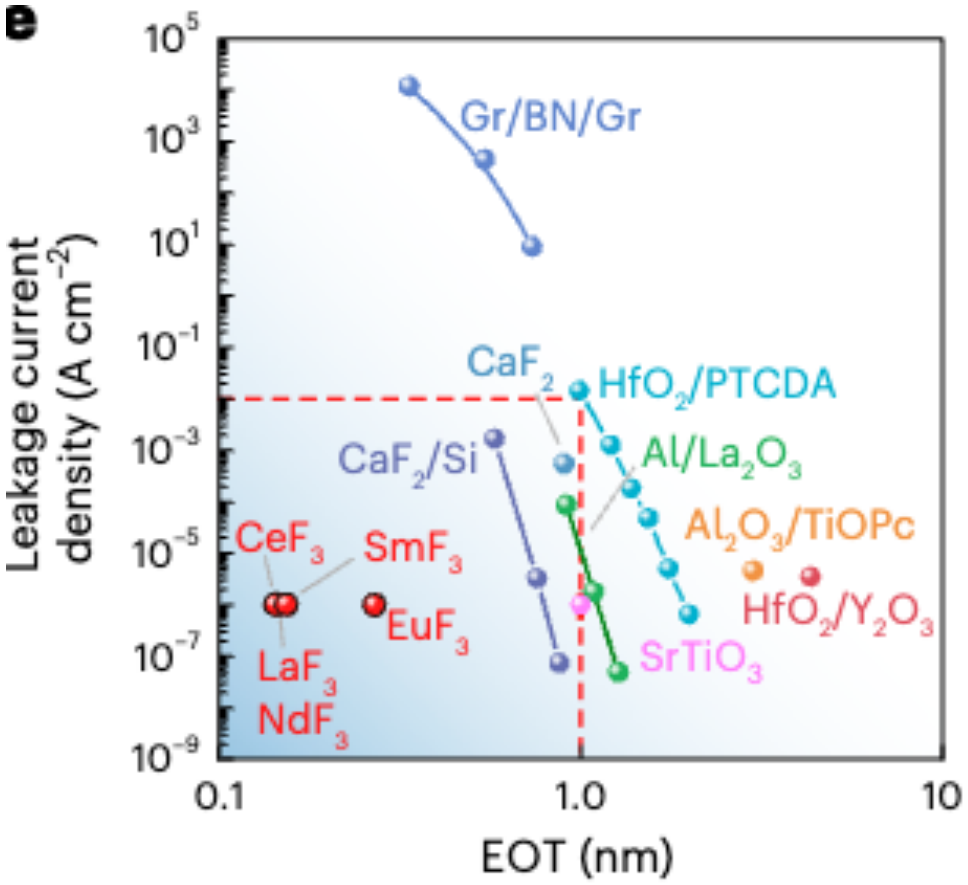

Fig. 2-18. Benchmark for fluoride dielectrics and tradition oxide dielectrics for MoS_2 transistors. [71]

2.3. References

1. Novoselov, K. S. et al. Electric Field Effect in Atomically Thin Carbon Films. Science 306, 666–669 (2004).

2. Sun, H., Sahin, O., Javey, A., Ager, J. W. & Chrzan, D. C. Theory of mechanical exfoliation of van der Waals bonded layered materials. Phys. Rev. Mater. 8, 064003 (2024).

3. Lee, Y., Chang, S., Chen, S., Chen, S. & Chen, H. Optical Inspection of 2D Materials: From Mechanical Exfoliation to Wafer-Scale Growth and Beyond. Adv. Sci. 9, 2102128 (2022).

4. Fu, Q. et al. One-Step Exfoliation Method for Plasmonic Activation of Large-Area 2D Crystals. Adv. Sci. 9, e2204247 (2022).

5. Huang, Y. et al. Universal mechanical exfoliation of large-area 2D crystals. Nat. Commun. 11, 2453 (2020).

6. Ding, S. et al. Ag-Assisted Dry Exfoliation of Large-Scale and Continuous 2D Monolayers. ACS Nano 18, 1195–1203 (2024).

7. Zhang, X. et al. Advanced tape-exfoliated method for preparing large-area 2D monolayers: a review. 2D Mater. 8, 032002 (2021).

8. Wang, N. et al. A universal method for large-yield and high-concentration exfoliation of two-dimensional hexagonal boron nitride nanosheets. Mater Today 27, 33–42 (2019).

9. Barnowsky, T., Krasheninnikov, A. V. & Friedrich, R. A New Group of 2D Non-van der Waals Materials with Ultra Low Exfoliation Energies. Adv. Electron. Mater. 9, (2023).

10. Pushkarna, I., Pásztor, A. & Renner, C. Twist-Angle-Dependent Electronic Properties of Exfoliated Single Layer MoS2 on Au(111). Nano Lett. 23, 9406–9412 (2023).

11. Wu, K. et al. Gold-Template-Assisted Mechanical Exfoliation of Large-Area 2D Layers Enables Efficient and Precise Construction of Moiré Superlattices. Adv. Mater. 36, e2313511 (2024).

12. Wang, S. et al. Electrochemical molecular intercalation and exfoliation of solution-processable two-dimensional crystals. Nat. Protoc. 18, 2814–2837 (2023).
13. Kaur, H. & Coleman, J. N. Liquid-Phase Exfoliation of Nonlayered Non-Van-Der-Waals Crystals into Nanoplatelets. Adv. Mater. 34, e2202164 (2022).
14. Jeon, Y. et al. Electrochemically exfoliated phosphorene nanosheet thin films for wafer-scale near-infrared phototransistor array. npj 2D Mater. Appl. 6, 82 (2022).
15. Wang, S. et al. A library of 2D electronic material inks synthesized by liquid-metal-assisted intercalation of crystal powders. Nat. Commun. 15, 6388 (2024).
16. Yu, J. et al. Tailoring lithium intercalation pathway in 2D van der Waals heterostructure for high-speed edge-contacted floating-gate transistor and artificial synapses. InfoMat (2024) doi:10.1002/inf2.12599.
17. Wu, Y. et al. Observation of an intermediate state during lithium intercalation of twisted bilayer MoS2. Nat. Commun. 13, 3008 (2022).
18. Zhang, L. et al. Molecular Beam Epitaxy of Two-Dimensional Vanadium-Molybdenum Diselenide Alloys. Acs Nano 14, 11140–11149 (2020).
19. Nunn, W., Truttmann, T. K. & Jalan, B. A review of molecular-beam epitaxy of wide bandgap complex oxide semiconductors. J. Mater. Res. 36, 4846–4864 (2021).
20. Nunn, W., Truttmann, T. K. & Jalan, B. A review of molecular-beam epitaxy of wide bandgap complex oxide semiconductors. J. Mater. Res. 36, 4846–4864 (2021).
21. Li, P. et al. Single-layer CrI3 grown by molecular beam epitaxy. Sci Bull 65, 1064–1071 (2020).
22. Zhou, D. et al. Epitaxial Growth of Main Group Monoelemental 2D Materials. Adv. Funct. Mater. 31, (2021).

23. Liu, X. et al. Wafer-Scale Epitaxial Growth of the Thickness-Controllable Van Der Waals Ferromagnet $CrTe_2$ for Reliable Magnetic Memory Applications. Adv. Funct. Mater. 33, (2023).
24. Liu, F. et al. Doping the Undopable: Hybrid Molecular Beam Epitaxy Growth, n Type Doping, and Field-Effect Transistor Using CaSnO3. ACS Nano 17, 16912–16922 (2023).
25. Zhou, S. et al. Ultrathin Non-van der Waals Magnetic Rhombohedral Cr_2S_3: Space-Confined Chemical Vapor Deposition Synthesis and Raman Scattering Investigation. Adv. Funct. Mater. 29, 1805880 (2019).
26. Li, M. et al. P type Doping in Large-Area Monolayer MoS2 by Chemical Vapor Deposition. ACS Appl. Mater. Interfaces 12, 6276–6282 (2020).
27. Ansh, A., Patbhaje, U., Kumar, J., Meersha, A. & Shrivastava, M. Origin of electrically induced defects in monolayer MoS2 grown by chemical vapor deposition. Commun. Mater. 4, 8 (2023).
28. Lei, M. et al. Low-temperature chemical vapor deposition growth of 2D materials. Electron (2024) doi:10.1002/elt2.43.
29. Chen, J. et al. Chemical Vapor Deposition of Large-Sized Hexagonal WSe2 Crystals on Dielectric Substrates. Adv. Mater. 27, 6722–6727 (2015).
30. Yang, Y. et al. Large-Domain Monolayer MoS2 Synthesis via Local-Feeding Metalorganic Chemical Vapor Deposition. ACS Mater. Lett. 6, 2802–2808 (2024).
31. Zhu, J. et al. Low-thermal-budget synthesis of monolayer molybdenum disulfide for silicon back-end-of-line integration on a 200 mm platform. Nat. Nanotechnol. 18, 456–463 (2023).
32. Kim, S. et al. Phase-Centric MOCVD Enabled Synthetic Approaches for Wafer-Scale 2D Tin Selenides. Adv. Mater. 36, e2400800 (2024).
33. Chen, C. et al. Growth of single-crystal black phosphorus and its alloy films through sustained feedstock release. Nat. Mater. 22, 717–724 (2023).

34. Zhou, Y. et al. van der Waals Epitaxial Growth of One-Unit-Cell-Thick Ferroelectric $CuCrS_2$ Nanosheets. Nano Lett. 24, 2118–2124 (2024).
35. Wang, P., Yang, D. & Pi, X. Toward Wafer-Scale Production of 2D Transition Metal Chalcogenides. Adv Electron Mater 7, 2100278 (2021).
36. Lee, J. & Shin, N. Toward an understanding of the mechanism of mixed-salt-mediated CVD growth of MoSe2. Appl. Phys. Lett. 123, 181902 (2023).
37. Li, B. et al. Thickness-Dependent Topological Hall Effect in 2D Cr5Si3 Nanosheets with Noncollinear Magnetic Phase. Adv. Mater. 35, e2210755 (2023).
38. Xu, J., Srolovitz, D. J. & Ho, D. The Adatom Concentration Profile: A Paradigm for Understanding Two-Dimensional MoS2 Morphological Evolution in Chemical Vapor Deposition Growth. Acs Nano 15, 6839–6848 (2021).
39. Qin, B. et al. Substrates in the Synthesis of Two-Dimensional Materials via Chemical Vapor Deposition. Chem Mater 32, 10321–10347 (2020).
40. You, J. et al. Salt-Assisted Selective Growth of H phase Monolayer VSe_2 with Apparent Hole Transport Behavior. Nano Lett. 22, 10167–10175 (2022).
41. Oh, J., Park, M., Kang, Y. & Ju, S.-Y. Real-Time Observation for MoS_2 Growth Kinetics and Mechanism Promoted by the Na Droplet. ACS Nano 18, 19314–19323 (2024).
42. Zhou, J. et al. Homo-Site Nucleation Growth of Twisted Bilayer MoS_2 with Commensurate Angles. Adv. Mater. e2408227 (2024) doi:10.1002/adma.202408227.
43. Karmakar, A. et al. Twisted $MoSe_2$ Homobilayer Behaving as a Heterobilayer. Nano Lett. 24, 9459–9467 (2024).
44. Schroeder, U., Park, M. H., Mikolajick, T. & Hwang, C. S. The fundamentals and applications of ferroelectric HfO_2. Nat. Rev. Mater. 7, 653–669 (2022).
45. Tan L, Liu B, Teng J H, Guo S, Low H Y, Loh K P, Atomic layer deposition of a MoS_2 film. Nanoscale, 6, 10584-10588 (2014).

46. Liu, L. et al. Zeolite-like molecules: Promising dielectrics for two-dimensional semiconductors. Sci. China Mater. 66, 233–240 (2023).
47. Kang, T. et al. High-κ Dielectric (HfO_2)/2D Semiconductor ($HfSe_2$) Gate Stack for Low-Power Steep-Switching Computing Devices. Adv. Mater. 36, e2312747 (2024).
48. Kaushik, N. et al. Reversible hysteresis inversion in MoS2 field effect transistors. npj 2D Mater. Appl. 1, 34 (2017).
49. Puurunen, R. L. et al. Hafnium oxide films by atomic layer deposition for high-κ gate dielectric applications: Analysis of the density of nanometer-thin films. Appl. Phys. Lett. 86, 073116 (2005).
50. Liu, W. H., Pey, K. L., Raghavan, N., Wu, X. & Bosman, M. Triggering voltage for post-breakdown random telegraph noise in HfLaO dielectric metal gate metal-oxide-semiconductor field effect transistors and its reliability implications. J Appl Phys 111, 024101 (2012).
51. Tan, Y. J. et al. A transparent, self-healing and high-κ dielectric for low-field-emission stretchable optoelectronics. Nat. Mater. 19, 182–188 (2020).
52. Zhu, W. et al. Ternary VOCl single-crystal as efficient gate dielectric for 2D field-effect transistors. 2d Mater 8, 025010 (2021).
53. Kaushik, N. et al. Reversible hysteresis inversion in MoS_2 field effect transistors. npj 2D Mater. Appl. 1, 34 (2017).
54. Kudo, K., Kimura, J., Suzuki, T., Nishiguchi, N. & Hara, A. Four-Terminal Polycrystalline-Silicon Thin-Film Transistors with High-κ HfO_2 Dielectric on Glass Substrate. 2021 28th Int Work Active-matrix Flatpanel Displays Devices Am-fpd 00, 118–119 (2021).
55. Tang, J. et al. Low power flexible monolayer MoS_2 integrated circuits. Nat. Commun. 14, 3633 (2023).

56. Peng, Y. et al. Gate-Last MoS_2 Transistors for Active-Matrix Display Driving Circuits. Adv. Funct. Mater. 33, (2023).
57. Kashir, A., Farahani, M. G., Kamba, S., Yadav, M. & Hwang, H. $Hf_{1-x}Zr_xO_2/ZrO_2$ Nanolaminate Thin Films as a High κ Dielectric. ACS Appl. Electron. Mater. 3, 5632–5640 (2021).
58. Robertson, J. High dielectric constant gate oxides for metal oxide Si transistors. Rep. Prog. Phys. 69, 327 (2006).
59. Gottlob, H. D. B. et al. 0.86-nm CET Gate Stacks with Epitaxial Gd_2O_3 High-k Dielectrics and FUSI NiSi Metal Electrodes. IEEE Electron Device Lett. 27, 814–816 (2006).
60. Terrés, B. et al. 2D-3D integration of high-κ dielectric with 2D heterostructures for opto-electronic applications. 2019 IEEE Int. Electron Devices Meet. (IEDM) 00, 33.5.1-33.5.4 (2019).
61. Osada, M. & Sasaki, T. The rise of 2D dielectrics/ferroelectrics. APL Mater. 7, 120902 (2019).
62. Pitner, G. et al. Sub-0.5 nm Interfacial Dielectric Enables Superior Electrostatics: 65 mV/dec Top-Gated Carbon Nanotube FETs at 15 nm Gate Length. 2020 Ieee Int Electron Devices Meet Iedm 00, 3.5.1-3.5.4 (2020).
63. Wen, J., Yan, C. & Sun, Z. The Application of a High-κ Polymer Dielectric in Graphene Transistors. Adv Electron Mater 6, 2000031 (2020).
64. Wu, L. et al. Atomically sharp interface enabled ultrahigh-speed non-volatile memory devices. Nat. Nanotechnol. 16, 882–887 (2021).
65. Tang, J. et al. Vertical Integration of 2D Building Blocks for All-2D Electronics. Adv. Electron. Mater. 6, (2020).
66. Zhang, Y. et al. A single-crystalline native dielectric for two-dimensional semiconductors with an equivalent oxide thickness

67. Holler, B. A., Crowley, K., Berger, M. & Gao, X. P. A. 2D Semiconductor Transistors with Van der Waals Oxide MoO_3 as Integrated High-κ Gate Dielectric. Adv Electron Mater 6, (2020). below 0.5 nm. Nat. Electron. 5, 643–649 (2022).
68. Huang, J.-K. et al. High-κ perovskite membranes as insulators for two-dimensional transistors. Nature 605, 262–267 (2022).
69. Liu, K. et al. A wafer-scale van der Waals dielectric made from an inorganic molecular crystal film. Nat Electron 4, 906–913 (2021).
70. Xu, Y. et al. Scalable integration of hybrid high-κ dielectric materials on two-dimensional semiconductors. Nat. Mater. 22, 1078–1084 (2023).
71. Meng, K. et al. Superionic fluoride gate dielectrics with low diffusion barrier for two-dimensional electronics. Nat. Nanotechnol. 19, 932–940 (2024).

Chapter 3. High-performance $MoSe_2$ transistors

Two-dimensional semiconductors, especially transition metal dichalcogenides (TMDs), have attracted many interests in advanced microfabrication for its potential extending Moore's law beyond silicon. Molybdenum disulfide (MoS_2) is a typical TMD n-type semiconductor and has been grown on SiO_2 or sapphire with domain size over a few hundred at wafer scale. [1-3] Compared with MoS_2, monolayer $MoSe_2$ has more abundant optoelectrical properties due to its narrow bandgap (1.6 eV). [4-7] However, the research on the growth mechanism of single-layer $MoSe_2$ is still not clear, and the prepared films are still dominated by multi-layer polycrystalline small areas, and the film quality is poor, and the device performance needs to be improved. [8] In order to realize the practical application of this new semiconductor material, the controllable preparation of high-quality, wafer-level continuous $MoSe_2$ films is an important breakthrough direction. [9] In this chapter, we will report 2 inch wafer scale $MoSe_2$ growth with vapor-liquid-solid method with large domain size. The two-dimensional field effect transistors with $MoSe_2$ as channel could achieve a high on/off ratio of 10^9 and a record of 12 μA/μm. We also have detailed statistics of the electrical properties of the large area transistor array, the threshold voltage of the device is concentrated between 1.5-2.5V, the average threshold voltage (Vth) is 2 V, and the large area device has a very stable threshold characteristics. This provides a basis for the realization of two-dimensional material large area devices integrated devices and optoelectronic devices.

3.1. Introduction

For the past half century, since the invention of the integrated circuit, Moore's Law has held that the number of transistors that can fit on a chip double about every two years. [10-11] Silicon transistors have been shrinking in size to meet the

requirements of Moore's Law. There are now tens of billions of transistors on a single chip. [12] However, as conventional silicon transistors enter the technology node below 10 nm and approach their physical limits, the leakage current caused by short-channel effects limits their scaling, so other materials have to be sought. [13] Two-dimensional (2D) semiconductors with atomic thickness and non-suspended bond planes have attracted great interest. The International Devices and Systems Roadmap (IRDS) listed 2D semiconductors as potential channel materials in 2017 and predicted that 2D electronic circuits would be commercialized by 2034. [14-15] Monolayer molybdenum diselenide ($MoSe_2$) is considered one of the most promising 2D semiconductor candidates in high-performance electronic circuits due to its inherently high mobility, excellent gate controllability, high on/off current ratio, and ultra-low standby current. [16] In fact, such single-layer TMD devices have been successfully demonstrated to work at a channel length of 1 nm. [17]

In order to realize their interesting transport and photoelectric properties in large-area integrated circuits, the large-area production of repeatable two-dimensional layered semiconductors is essential. [18] In recent years, there have been some reports on the thermochemical vapor deposition (CVD) of large area single or multilayer molybdenum disulfide, including metal-organic chemical vapor deposition, physical deposition and chemical synthesis. [19-20] However, large-scale wafer-level synthesis of $MoSe_2$ thin films is rarely reported, and the field-effect mobility of transistors is relatively low (usually $< 1\ cm^2\ V^{-1}\ s^{-1}$) compared to the stripped $MoSe_2$ monolayer. [21] In particular, since most of the growth grain sizes are sub-microns, the presence of large grain boundary densities is usually a limiting factor for carrier transport in molybdenum diselenide films prepared by the above methods. [22-23] Therefore, the key challenge involves achieving highly

crystalline two-dimensional layered semiconductor films over large areas with minimal content of structural defects such as grain boundaries. [24] In this way, samples with excellent electrical and mechanical properties comparable to those of bulk phase glass materials can be obtained. In this chapter, we use the salt-assisted chemical vapor deposition to grow 2-inch wafer-scale $MoSe_2$ films. [25] We will discuss the differences with salt sources and oxide sources using transmission electron microscopy, Raman spectroscopy, photoluminescence spectroscopy, and X-ray photoelectron spectroscopy to characterize the quality of the two samples. [26] We also made large-area field-effect transistors with samples from both sources. The two-dimensional field-effect transistors with $MoSe_2$ as channel could achieve a high on/off ratio of 10^9 and a record of 12 μA/μm. We also have detailed statistics of the electrical properties of the large area transistor array, the threshold voltage of the device is concentrated between 1.5-2.5V, the average threshold voltage (V_{th}) is 2 V, and the large area device has a very stable threshold characteristics. [27] This provides a basis for the realization of two-dimensional material large area devices integrated devices and optoelectronic devices.

3.2. CVD of $MoSe_2$ film with large domain size

3.2.1. Substrate preparation

In this work, we primarily utilized C-plane single crystal sapphire substrates and 300 nm SiO_2/Si substrates. Typically, sapphire substrates grown with oxide sources (MoO_x) do not require treatment, whereas those grown by salt-sources (Na_2MoO_3) need ultraviolet irradiation to enhance the adhesion of spin-coated solutions. The annealed sapphire substrates used in the experiments were prepared using a tube furnace with a flow of 10 sccm O_2 and 300 sccm Ar, annealed at 1000°C for 4 hours. For the SiO_2 substrates, a sequential ultrasonic cleaning process was employed using deionized water, alcohol, acetone, and isopropanol for 5-10

minutes each, followed by drying with a nitrogen gas gun to remove any residual liquids and dust.

3.2.2. $MoSe_2$ grown with oxide sources

The detailed steps for growth with oxide sources are as follows. Use ethanol-soaked lint-free paper to clean both ends of the quartz tube, sealing plates, and all necessary accessories such as quartz bowls, small quartz tubes, and quartz plates. Accurately weigh the selenium powder using weighing paper and place it into a small quartz bowl. Similarly, weigh the molybdenum pellets and place them into the slots of a small quartz tube. Place the quartz bowl containing selenium powder in the first temperature zone of the quartz chamber. Seal the small quartz tube containing molybdenum pellets with an upstream sealing plate using a rubber ring, ensuring the molybdenum source is positioned in the second temperature zone. Arrange the growth substrates sequentially on a quartz plate in the third temperature zone. Seal the quartz tube connections and connect the exhaust to a mechanical pump. Gently turn on the pump to avoid blowing away the molybdenum pellets, reducing the system vacuum to below $3*10^{-3}$ torr. Control the flow meters to introduce argon gas into the chamber through three separate routes, each at 100 sccm, maintaining the pressure around 1 torr. The heating tape is set to 280°C for 5 minutes. The first temperature zone is heated to 550°C over 18 minutes, the second zone to 700°C over 20 minutes, and the third zone to 930°C over 38 minutes. The heating times are controlled to ensure the first and third zones reach their set temperatures simultaneously. The selenium source's heating tape zone reaches its set temperature first, initiating growth for 25 minutes. Hydrogen is gradually introduced during the heating process. These steps ensure precise control over the whole growth process, enhancing the quality and consistency of the resulting materials.

3.2.3. $MoSe_2$ grown with salt sources

the detailed steps for growth with salt sources are as follows: Sodium molybdate solutions of varying concentrations were prepared using deionized water. After ultraviolet irradiation, 1 ml of the solution was dropped onto the sapphire surface and spin-coated at 5000 r/min for 60 seconds. The substrate was then baked on a hot plate at 80°C for 1 minute to quickly evaporate the deionized water, resulting in a spin-coated molybdenum source substrate. The quartz bowl containing selenium powder was placed in the first temperature zone of the quartz chamber, while the spin-coated substrate and growth substrate were placed in the third temperature zone. The first temperature zone was heated to 270°C over 5 minutes, the second zone to 600°C over 30 minutes, and the third zone to 900°C over 37 minutes. The remaining steps were the same as those for growth with oxide sources.

3.2.4. Growth results

By controlling the concentration of molybdenum source, growth temperature and hydrogen flow, the main influencing factors can be controlled, molybdenum source concentration and evaporation amount, and then improve the grain size, and is about 20 times the grain size of molybdenum oxide growth, the maximum size is about 120 μm, and can achieve 2 inches of homogeneous nucleated single layer molybdenum diselenide grain. Fig. 3-1 shows a sapphire wafer with monolayer molybdenum diselenide. The darker color of the outer ring of the wafer is due to the higher coverage of molybdenum diselenide at the edge. Fig. 3-2 shows the grain nucleation in different regions, and molybdenum diselenide with a larger grain size is formed within a relatively uniform range of 2 inches.

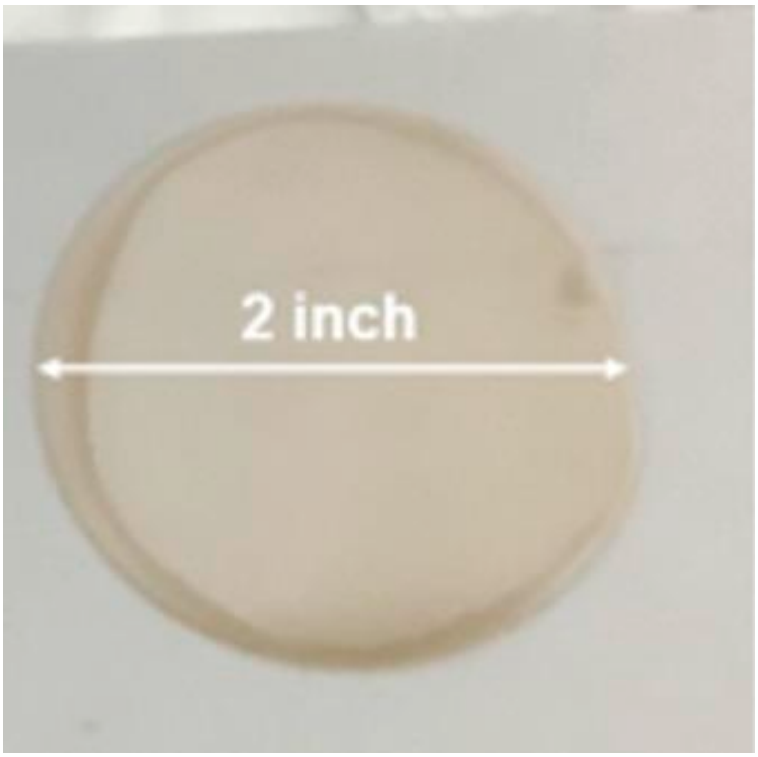

Fig. 3-1. Photos of 2 in. $MoSe_2$ wafer.

Fig. 3-2. Optical images of $MoSe_2$ domains.

After extended time, molybdenum diselenide continuous film can also be obtained, but limited to the quartz drawer placed during growth to reduce the source entry, it is currently possible to achieve a large area of cm level film, about 2 cm x 4 cm, and subsequently can be improved quartz accessories to achieve wafer level films.

As shown in Fig. 3-3a when the growth time is close to film formation, it is observed that the grains are gradually spliced into a single continuous film without any impurities and thick layers. Fig. 3-3b displays the observed single-layer molybdenum diselenide continuous film formation, which is continuous, uniform, and free of impurities over a large range.

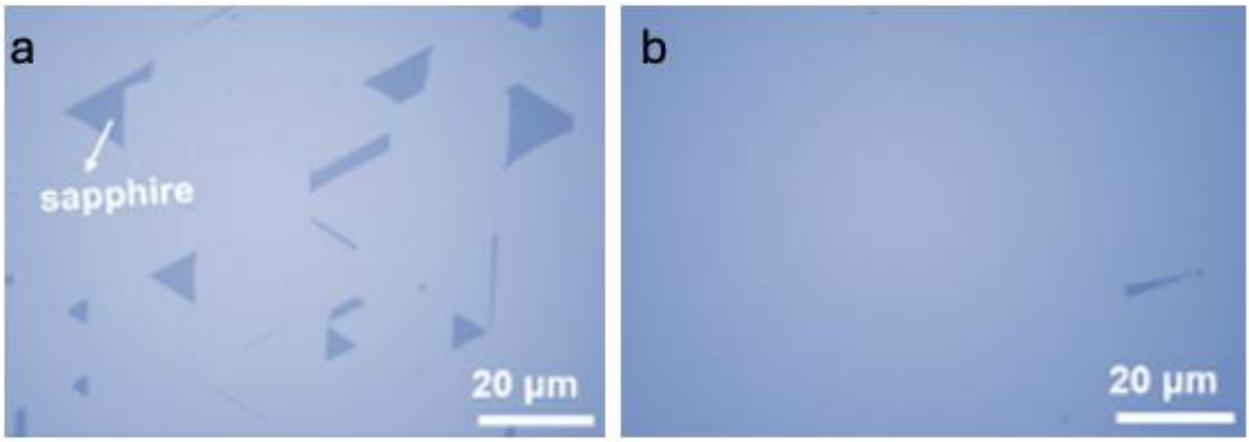

Fig. 3-3. Optical images of $MoSe_2$ continuous film after prolonging the growth time.

After adjusting the growth pattern, Fig. 3-4 is the AFM characterization of $MoSe_2$ grown with salt sources. [28] It can be directly observed that the molybdenum diselenide grains growing on the sapphire surface are of uniform height and flat surface, with a height of 0.6 nm. The roughness of the surface of the sample in Fig. 3-4 can be measured. The result indicates that the arithmetic mean deviation Ra of the height roughness of the sample is 0.0809 nm, and the Rq of the root mean square deviation relative to the contour mean line is 0.105 nm, which is a very small result, confirming the uniformity of the surface sample.

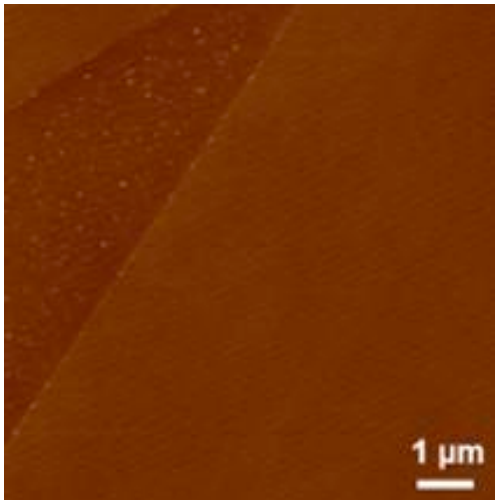

Fig. 3-4. AFM image of $MoSe_2$ domain on sapphire.

3.3. Optical properties of $MoSe_2$ film

In order to obtain the optical properties of molybdenum diselenide, the grain and film forming samples were measured by Raman and fluorescence spectra using fast confocal Raman imaging. During the measurement, the 532 nm laser and 600 grating are used to clearly observe the sample and focus the light spot on the corresponding measurement position of the sample under the 100 times objective lens. The light spot size is about 2 μm and the laser power is 3.2%, so as to avoid the sample perforation due to too high laser power and too long irradiation time, affecting the accuracy of the measurement results. [29]

Raman spectroscopy was performed on the $MoSe_2$ monolayer with oxide sources firstly. [30] As shown in the Fig. 3-5a, the peak position of A_{1g} peak corresponding to the out-of-plane vibration mode of the sample is 240 cm^{-1}, where the peak signal is the strongest and is not affected by stray peaks, which is usually the main characteristic peak of $MoSe_2$ Raman signal. The E_{2g} peak corresponding to the in-plane vibration mode is 287 cm^{-1}. Fig. 3-5b shows the $MoSe_2$ fluorescence spectrum of monolayer film formation, showing a strong fluorescence peak at 800

nm, corresponding to the direct transition optical band gap of monolayer molybdenum diselenide. After Lorentz fitting, it can be obtained that the half-peak full width (FWHM) of this sample is 78.4 meV, which indicates that the sample has poor crystallinity. In addition, the peak appearing near 1.79 eV is a characteristic peak of the sapphire substrate. Therefore, by measuring Raman and fluorescence spectra, it can be confirmed that the sample with oxide sources is monolayer molybdenum diselenide, but the sample quality is average.

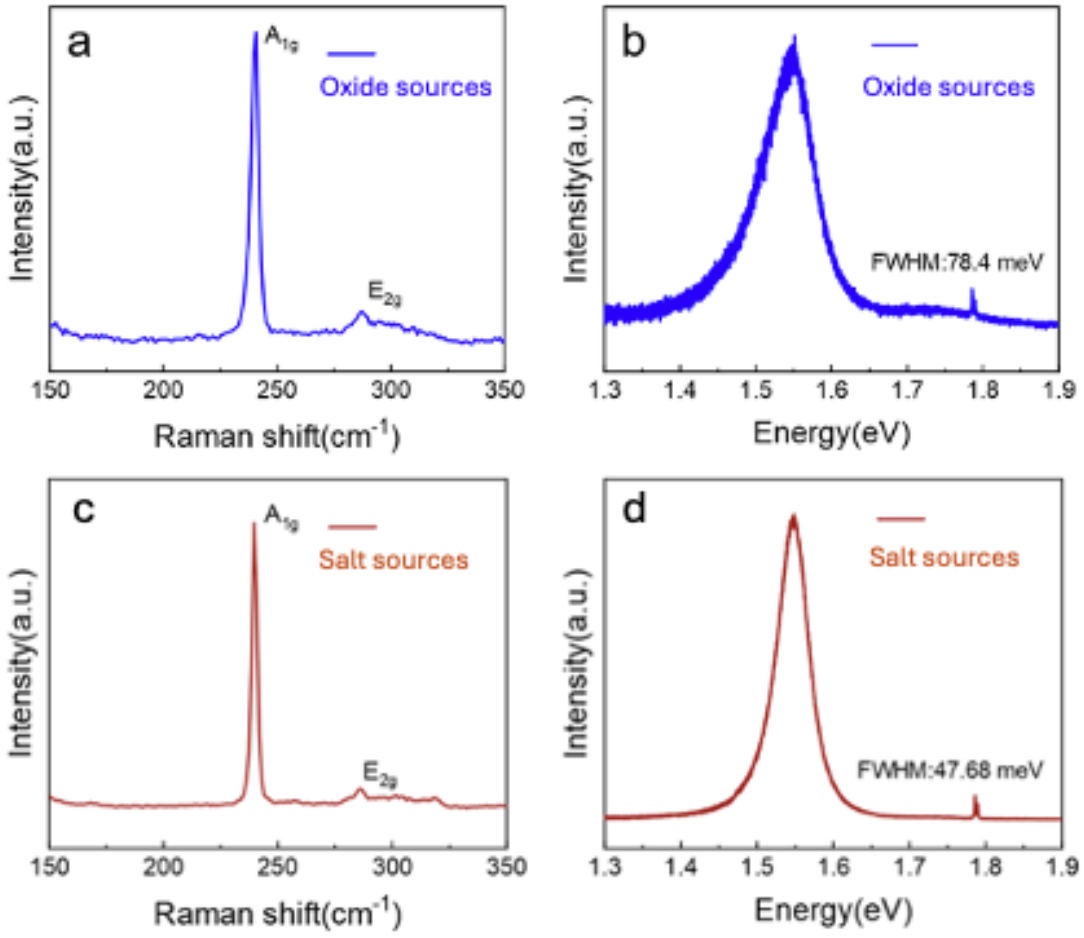

Fig. 3-5. Raman and PL spectra of $MoSe_2$ film with oxide and salt sources

Next, the molybdenum diselenide monolayer grown with salt sources was characterized by Raman spectroscopy with the same laser power and test time. Fig.

3-5c shows the $MoSe_2$ Raman spectra of monolayers grown in this way. The two main characteristic peaks of the sample Raman signal, A_{1g} peak, are 240 cm^{-1} and E_{2g} peak is 286 cm-1. Fig. 3-5d shows the $MoSe_2$ fluorescence spectrum of this sample, showing a strong fluorescence peak at 801 nm and a half-peak full width (FWHM) of 47.6meV, which is much smaller than that of $MoSe_2$ grown with salt sources, indicating higher quality and crystallinity and excellent optical properties. Therefore, it can be confirmed that the sample is monolayer molybdenum diselenide, and the optical properties of the sample are better.

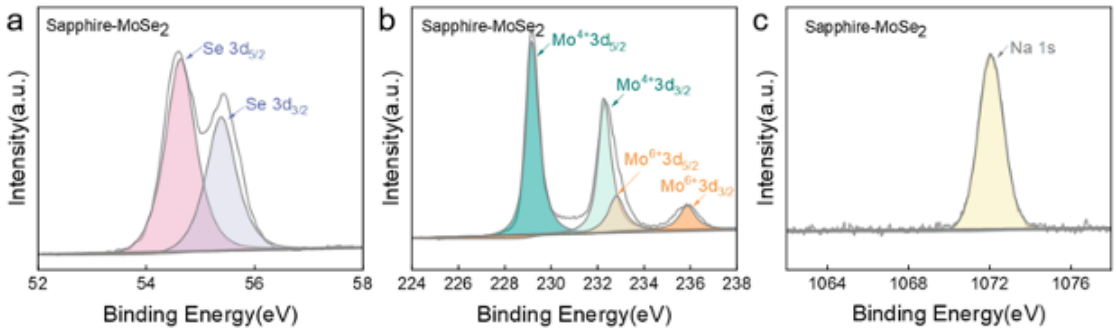

Fig. 3-6. XPS spectra of $MoSe_2$ film.

In order to confirm the elemental composition of $MoSe_2$ samples grown with salt sources, the samples grown by CVD were characterized by X-ray photoelectron spectroscopy to facilitate the analysis of elemental composition and valence states on the surface. Select the $MoSe_2$ film sample grown on sapphire, it can be found that the two peaks at the binding energy of 54.6 eV and 55.3 eV in Fig. 3-6 correspond to the absorption peaks of 3d5/2 and 3d3/2, respectively, at the two energy levels of Se element, where Se is -2 valence. The two peaks at the binding energy of 232.2 eV and 229.1 eV correspond to the absorption peaks of the two energy levels 3d5/2 and 3d3/2 of Mo element, respectively, where Mo is +4 valence, indicating that Mo^{6+} in sodium molybdate is reduced to Mo^{4+}, corresponding to Mo^{4+} in $MoSe_2$. Interestingly, there also exists two peaks with

binding energies of 232.8 eV and 235.9 eV, corresponding to the two energy levels of Mo^{6+}, 3d5/2 and 3d3/2, which are the unreduced Mo6+ in sodium molybdate. The absorption peak of Na in the sample was measured. As shown in Fig. 3-6c, the absorption peak of 1s level of Na element appeared at 1072 eV. These indicate that Mo^{6+} and Na^{+} peaks in the energy spectrum indicate that sodium molybdate remains in the sample or substrate.

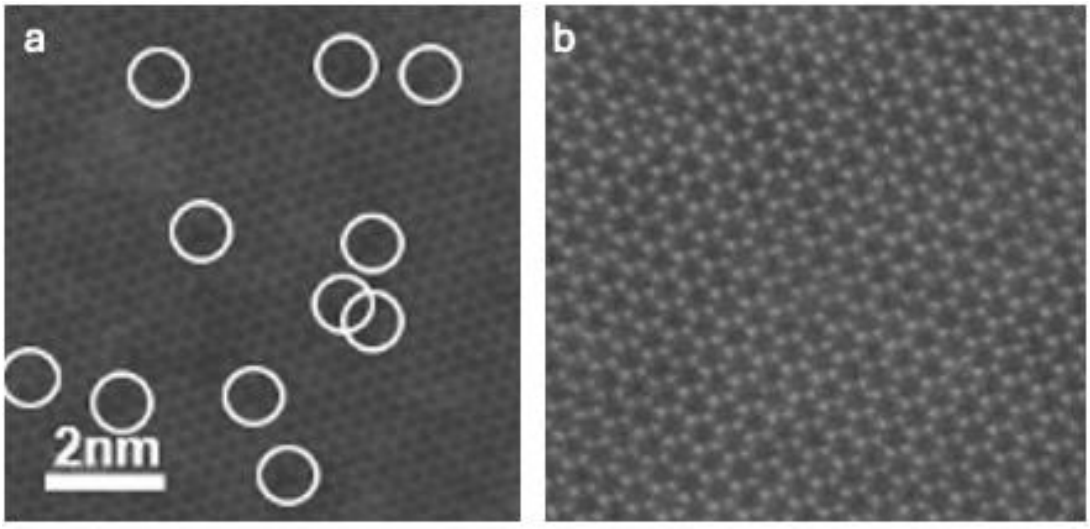

Fig. 3-7. Transmission electron microscope images of $MoSe_2$ films with oxide sources and salt sources

The high angle ring dark field (HAADF) image of a single layer of molybdenum diselenide is shown in Fig. 3-7. It can be seen from the image that molybdenum diselenide is arranged in a six-membered ring structure. According to the statistics within the range, the number of Se atoms missing is clearly observed as high as 13. The defect density is 9.02×10^{11} cm^{-2}, and the number of defects is large, mainly the vacancy of selenium, of which 4 are empty of the upper and lower layers of Se atoms, and 9 are empty of one Se atom. The main causes of defects are the grain splicing of TMDs with different orientations leads to the formation of grain boundaries, damage to the sample during the transfer process, and insufficient

supply of precursors during the growth process, etc. Defects in TMDs materials will reduce the mobility of carriers between the conduction and valence bands, and then affect the electrical properties of the subsequent processing devices. At present, the number of defects this samples are large and the crystallinity is not great. The HAADF image of monolayer molybdenum selenide grown with salt sources is shown in Fig. 3-7b. The complete six-membered ring structure of molybdenum disselenide can be seen, with atoms parallel to each other or showing a 60° Angle and uniform distribution. According to the high resolution image, the brightness of the image is proportional to the square of the atomic number, so the larger the original number, the higher the brightness of the atoms in the image, where the bright atom is the Se atom (atomic number 34 x 2), corresponding to the purple atom in the Fig., and the dark atom is the Mo atom (atomic number 42), corresponding to the blue atom in the Fig.. It can be intuitively seen that the number ratio of molybdenum atoms and selenium atoms is 1:1, and three molybdenum atoms are adjacent to selenium atoms to form a six-membered ring, which shows the 1H phase crystal structure of molybdenum diselenide sample. The distances (d) are 0.160 nm and 0.277 nm, respectively, corresponding to the $(11\bar{2}0)$ and $(10\bar{1}0)$ planes of monolayer $MoSe_2$. In Fig. 3-7, The central region has a set of six regular diffraction spots. The sample is hexagonal crystal system, indicating that the region is a single crystal with a crystal face spacing of 0.31 nm. Since the micro-gate used is not supported by carbon film, the edge of a single layer of molybdenum diselenide will be damaged at the cavity position, so the middle position of the sample is selected for detailed atomic phase diagram characterization. There is no obvious selenium defect compared with the sample grown with oxide sources. Therefore, the sample grown with salt sources has fewer defects, higher crystallinity and higher quality.

3.4. Electrical performance of $MoSe_2$ field-effect transistors

This section mainly uses molybdenum diselenide film with oxide sources to prepare a three-ended FET device. HfO_2 is used as the gate, and the oxide layer thickness is 5 nm. It is deposited on the surface of silicon oxide substrate by ALD, and continuous MoSe2 film with a grain size of 5 μm is used as the channel material for device preparation.

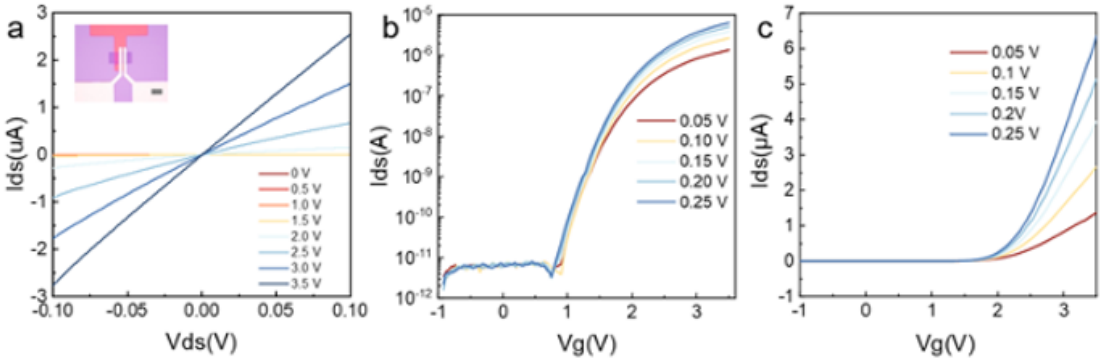

Fig. 3-8. Electrical measurement of transfer curve and output curve of $MoSe_2$ film

After the preparation of molybdenum diselenide large area effect transistor device, the electrical properties of the device were investigated. The probe station connected to the semiconductor parameter analyzer was used for measurement. The test was carried out at room temperature and low pressure, and the light was shielded to avoid affecting the performance of the device. The test uses the source and grid as voltage access terminals, and the drain is grounded. The electrical curves of molybdenum diselenide FET devices are shown in Fig. 3-8, where Fig. 3-8a is the output characteristic curve and Fig. 3-8b and 3-8c are the transfer characteristic curve under different coordinate systems. The different gate voltages in the output characteristic curve (I_d-V_d) correspond to the gradual increase in bias, and the channel current increases accordingly, showing a linear relationship, indicating that the electrode of the device and molybdenum diselenide are in ohmic

contact. In the case of constant source-drain voltage, with the increase of gate voltage, the carrier concentration of molybdenum diselenide increases, so the current increases, because the positive gate voltage electrode will increase the Fermi surface of molybdenum diselenide and reduce the barrier height. The N-type conductive behavior of molybdenum diselenide can be seen in the device transfer curve (I_d-V_g). I_d presents a switching state with the change of gate voltage V_g, and the ratio of the maximum current of the device to the minimum current is the switching ratio. The on-state current (I_{on}) of the device at a bias voltage (V_d) of 0.25 V is 0.318 μA/μm. The switching ratio of the device is 10^6. In addition, carrier mobility is also a way to judge the electrical performance of the device, and the mobility is calculated by measuring the actual effective field mobility of the device. The formula for calculating the field effect mobility μ is below.

$$\mu=L/W\cdot 1/C_{ox}\cdot 1/V_d\cdot(dI_d)/(dV_g)$$

Where L and W are the length and width of the channel respectively, and C_{ox} is the unit area capacitance of the grid dielectric layer. V_d, I_d and V_g are the source-drain bias, channel current and gate voltage of the device respectively. The mobility calculated according to the above formula is 1.4 $cm^2\ V^{-1}s^{-1}$ for $MoSe_2$ grown with oxide sources.

Then molybdenum diselenide obtained by VLS growth mode was used to prepare FET devices, and the electrical properties of the films grown by the two methods were further compared. The FET was prepared by using silicon oxide and alumina substrates with high dielectric constant as gate dielectric layers, and single grain samples of 20-120μm molybdenum diselenide and film forming samples obtained by VLS growth mode as channel materials.

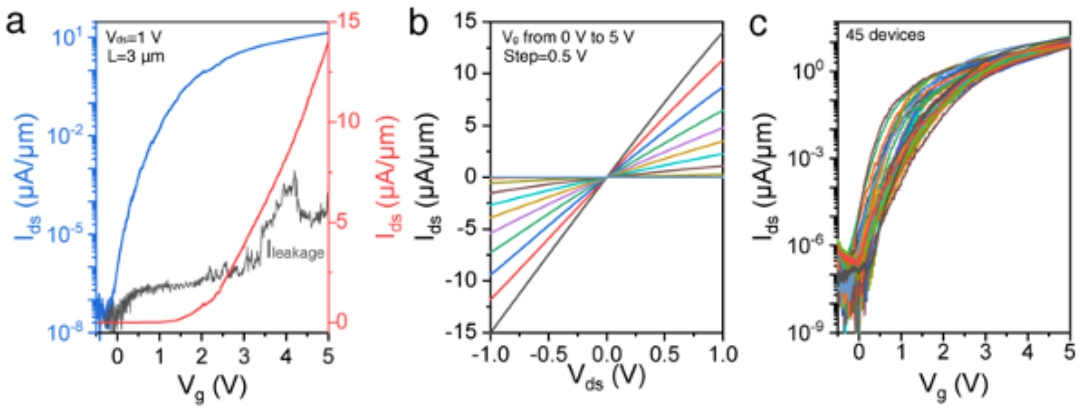

Fig. 3-9. Electrical measurement of $MoSe_2$ film with salt sources.

At the same time, in order to characterize the electrical properties of molybdenum diselenide film samples grown with salt sources, a large area field effect transistor (FET) was prepared. The film samples were transferred to an alumina oxide substrate, which was prepared with an alumina base gate prepared by ALD in advance, and field-effect devices with different aspect ratios were integrated. Fig. 3-9 shows the electrical curve of a batch of typical backgate FET prepared. Fig. 3-9a tests the device transfer characteristic curve with a channel length of 3 μm. It can be seen that under a relatively small bias voltage of 1 V, the on-state current can reach (I_{on}) 12 μA/μm, and the low on-state current (I_{off}) can reach as low as 10 fA. With a switch ratio of up to 10^9 and an extremely low leakage current, higher current density and higher switch ratio compared to previous device test results are seen. Fig. 3-9b shows that the device has good ohmic contact and maintains a good linear output as the bias increases. Fig. 3-9c shows the measurement structure of a large area molybdenum diselenide transistor array, and the transfer characteristic curves of 45 devices are counted and normalized. During the period, the on-state current is stable at about 10 μA/μm, and the threshold voltage is also concentrated, showing excellent electrical uniformity.

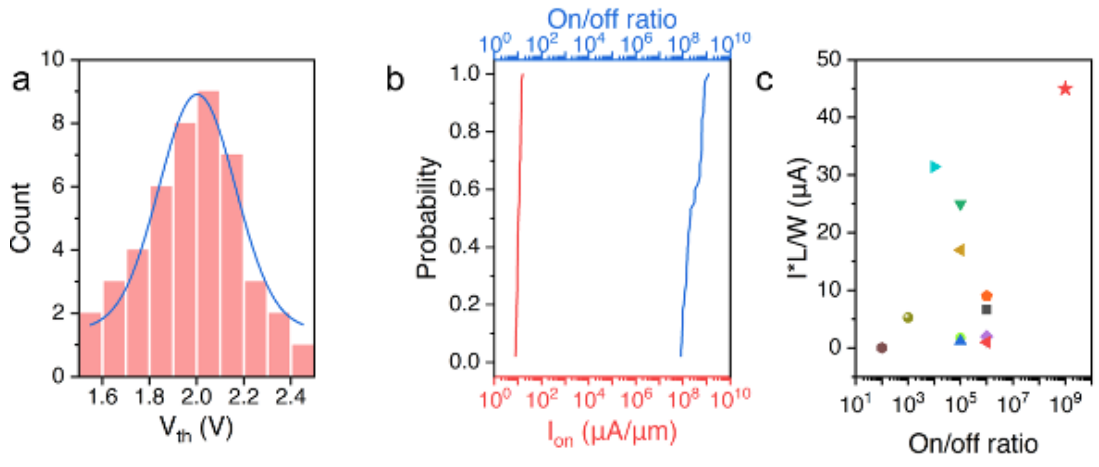

Fig. 3-10. The statistic data of 45-$MoSe_2$ FET with salt sources

The following detailed statistics of the electrical properties of the large-area transistor array can be seen from Fig. 3-10a that the threshold voltage of the device is concentrated in the range of 1.5-2.5V, and the average threshold voltage (V_{th}) is 2 V. The large-area device has a very stable threshold characteristic. Then, the switch ratio and current density of the device are further analyzed and counted in Fig. 3-10b. The current density is stable at about 10 μA/μm;, and the maximum can be achieved at 12 μA/μm; the switch ratio is stable between 10^8-10^9, and the maximum can be achieved at 10^9. Fig. 3-10c compares the switching ratio and equivalent current (I*L/W), as well as the product of the on-state current and channel length/width ratio of field-effect transistor devices prepared by molybdenum diselenide in recent years. By analyzing the performance of the device prepared by molybdenum diselenide grown with salt sources in this paper and that in previous literature, it is indicated that our $MoSe_2$ samples have very high electrical quality, and have great advantages in the equivalent current and switching ratio of $MoSe_2$ FET devices, with an equivalent current of up to 45 μA and a switching ratio of 10^9. It has great advantages in the uniformity of large area devices, which provides a basis for the realization of two-dimensional material large area devices integrated devices.

3.5. Summary and outlook

In conclusion, high-quality continuous $MoSe_2$ films with salt sources are successfully synthesized. The domain size is around 120 μm, which is larger than that in most litheratures and oxide sources. Electrical measurement shows that the $MoSe_2$ film is uniform and FET reach a high on/off ratio of 10^9 and a high on-state current of 12 μA/μm at 1 V bias.

3.6. References

1. Zhang Z, Zhu L, Wang D, et al. Ultrafast growth of large-area uniform, millimeter-size $MoSe_2$ single crystals on low-cost soda-lime glass [J]. Advanced Materials Interfaces, 2021, 8(12): 2100415.
2. Li T, Yang Y, Zhou L, et al. Halide vapor phase epitaxy of monolayer molybdenum diselenide single crystals [J]. National Science Open, 2023, 2(4): 20220055.
3. Kim M, Seo J, Kim J, et al. High-crystalline monolayer transition metal dichalcogenides films for wafer-scale electronics [J]. ACS Nano, 2021, 15(2): 3038-3046.
4. Jeon Y, Seo J, Kim J, et al. Wafer-scale two-dimensional molybdenum diselenide phototransistor array via liquid-precursor-assisted chemical vapor deposition [J]. Advanced Optical Materials, 2022, 10(3): 2101492.
5. Zhang D, Wen C, Mcclimon J B, et al. Rapid growth of monolayer $MoSe_2$ films for large-area electronics [J]. Advanced Electronic Materials, 2021, 7(6): 2001219.
6. Li S, Lin Y C, Hong J, et al. Mixed-salt enhanced chemical vapor deposition of two-dimensional transition metal dichalcogenides [J]. Chemistry of Materials, 2021, 33(18): 7301-7308.

7. Li S, Wang S, Tang D M, et al. Halide-assisted atmospheric pressure growth of large WSe_2 and WS_2 monolayer crystals [J]. Applied Materials Today, 2015, 1(1): 60-66.
8. Yang P, Zou X, Zhang Z, et al. Batch production of 6-inch uniform monolayer molybdenum disulfide catalyzed by sodium in glass [J]. Nature Communications, 2018, 9(1): 979.
9. Ben-Smith A, Choi S H, Boandoh S, et al. Photo-oxidative crack propagation in transition metal dichalcogenides [J]. ACS Nano, 2024, 18(4): 3125-3133.
10. Li S, Lin Y C, Zhao W, et al. Vapour–liquid–solid growth of monolayer MoS_2 nanoribbons [J]. Nature Materials, 2018, 17(6): 535-542.
11. Liu B, Fathi M, Chen L, et al. Chemical vapor deposition growth of monolayer WSe_2 with tunable device characteristics and growth mechanism study [J]. ACS Nano, 2015, 9(6): 6119-6127.
12. Hu J, Quan W, Yang P, et al. Epitaxial growth of high-quality monolayer MoS_2 single crystals on low-symmetry vicinal Au (101) facets with different miller indices [J]. ACS Nano, 2022, 17(1): 312-321.
13. Zhang Z, Ji X, Shi J, et al. Direct chemical vapor deposition growth and band-gap characterization of MoS_2/h-BN van der Waals heterostructures on Au foils [J]. ACS Nano, 2017, 11(4): 4328-4336.
14. Zhou X, Shi J, Qi Y, et al. Periodic modulation of the doping level in striped MoS_2 superstructures [J]. ACS Nano, 2016, 10(3): 3461-3468.
15. Dong J, Zhang L, Dai X, et al. The epitaxy of 2D materials growth [J]. Nature Communications, 2020, 11(1):5862.
16. Zheng P, Wei W, Liang Z, et al. Universal epitaxy of non-centrosymmetric two dimensional single-crystal metal dichalcogenides [J]. Nature Communications, 2023, 14(1): 592.

17. Fu J-H, Min J, Chang C-K, et al. Oriented lateral growth of two-dimensional materials on c-plane sapphire [J]. Nature Nanotechnology, 2023.
18. Xu X, Zhang Z, Dong J, et al. Ultrafast epitaxial growth of metre-sized single-crystal graphene on industrial Cu foil [J]. Science Bulletin, 2017, 62(15): 1074-1080.
19. Wang L, Xu X, Zhang L, et al. Epitaxial growth of a 100-square-centimetre single-crystal hexagonal boron nitride monolayer on copper [J]. Nature, 2019, 570(7759): 91-5.
20. Wang S, Pacios M, Bhaskaran H, et al. Substrate control for large area continuous films of monolayer MoS_2 by atmospheric pressure chemical vapor deposition [J]. Nanotechnology, 2016, 27(8): 085604.
21. Chang Y-H, Zhang W, Zhu Y, et al. Monolayer $MoSe_2$ grown by chemical vapor deposition for fast photodetection [J]. ACS Nano, 2014, 8(8): 8582-8590.
22. Chen J, Zhao X, Tan S J R, et al. Chemical vapor deposition of large-size monolayer $MoSe_2$ crystals on molten glass[J]. Journal of the American Chemical Society, 2017, 139(3): 1073-1076.
23. Shim G W, Yoo K, Seo S B, et al. Large-area single-layer $MoSe_2$ and its van der Waals heterostructures [J]. ACS Nano, 2014, 8(7): 6655-6662.
24. Kim K, Lee J U, Nam D, et al. Davydov splitting and excitonic resonance effects in Raman spectra of few-layer $MoSe_2$ [J]. ACS nano, 2016, 10(8): 8113-8120.
25. Wang X, Gong Y, Shi G, et al. Chemical vapor deposition growth of crystalline monolayer $MoSe_2$ [J]. ACS Nano, 2014, 8(5): 5125-5131.
26. Chen Y., Li Y., Hai Z., et al. Facile-synthesized $NiCo_2O_4$@$MnMoO_4$ with novel and functional structure for superior performance superca pacitors [J]. Applied Surface Science, 2018, 452: 413-422

27. Zhu X., Lu W. D., Optogenetics-Inspired tunable synaptic functions in memristors [J]. ACS Nano, 2018, 12(2): 1242-1249.
28. Chen H, Xie Y, Cui H, et al. In situ growth of a $MoSe_2$/Mo counter electrode for high efficiency dye-sensitized solar cells [J]. Chemical Communications, 2014, 50(34): 4475-4477.
29. Kang W T, Phan T L, Ahn K J, et al. Selective pattern growth of atomically thin $MoSe_2$ films via a surface-mediated liquid-phase promoter[J]. ACS Applied Materials & Interfaces, 2021, 13(15): 18056-18064.
30. Yue L, Kailiang Z, Fang W, et al. Scalable synthesis of highly crystalline $MoSe_2$ and its ambipolar behavior[J]. 2017.

Chapter 4. Sub-3-Å EOT High-κ dielectrics for Advanced Transistors

Scaling down the size on different directions in electronic devices is imperative for advanced semiconductor nodes, leading to compact, high-speed, energy-efficient integrated circuits. The shrinkage of equivalent oxide thickness (EOT) of dielectric layers stands as a pivotal element for silicon-based metal-oxide-semiconductor field-effect transistors, oxide thin-film transistors, and emerging two-dimensional transistors. Emerging materials, such as crystalline perovskite $SrTiO_3$, ionic crystals CaF_2, molecular crystals Sb_2O_3 and 2D materials Bi_2SeO_5 and Bi_2SiO_5 show a small EOT of sub-1-nm, but limited to the scalability, compatibility with Si-based process, poor gate controllability. Here, we report a defect-free high-quality 1.3-nm-thick hafnium oxide (HfO_2) high-κ dielectric layers on 8-inch wafers through optimized atomic layer deposition process with two-oxidation step at only 200 °C. Our ultrathin HfO_2 film shows an extraordinarily small EOT of 0.27 nm, a ultrasmall leakage current of 10^{-14} A/μm^2 at 1 V bias voltage, and a robust breakdown electric field of approximately 32 MV/cm. We also fabricate MoS_2 transistors and circuits with 1.3-nm-thick HfO_2 as dielectric layers to demonstrate its practicality and gate controllability. Typical transistors exhibit large on-state current density of 250 μA/μm and an impressive on/off ratio of 10^8, accompanied by an ultra-low subthreshold slope of 60 mV/dec. Logic gates and memory devices are also fabricated on 8-inch wafers to demonstrate its substantial implications for the forthcoming advanced semiconductor processes in the angstrom era.

4.1. Introduction

In the rapidly evolving landscape of semiconductor devices and circuits, scaling down from all directions enables higher integration, faster speed, reduced power consumption, and increased functionality, shaping the future of electronics[1-

3] .The scaling of equivalent oxide thickness (EOT) in dielectric layers stands as a cornerstone trend, profoundly impacting silicon-based metal-oxide-semiconductor (MOS) field-effect transistors (FETs), oxide thin-film transistors (TFTs), and emerging two-dimensional (2D) FETs [4-6]. EOT shrinkage not only enables higher integration density, vital for the contemporary demand for compact and energy-efficient electronic devices, but also plays a crucial role in rapid signal transmission and switching in in cutting-edge processors and communication devices [7]. Additionally, decreasing EOT allows equivalent functionality at lower voltages, thereby boosting energy efficiency and extending battery life of whole electronic systems [8].

EOT is defined as the thickness of a silicon oxide (SiO_2) layer that would yield electronic performance equivalent to that of a high-κ dielectric layer in use, which can be calculated using the following formula: $EOT=3.9\ t_{ox}/\varepsilon_{ox}$, where 3.9 and ε_{ox} are dielectric constant of SiO_2 and high-κ film, respectively and t_{ox} is the thickness of the high-κ film [9,10]. Hafnium oxide (HfO_2), aluminium oxide (Al_2O_3) and zirconium oxide (ZrO_2) grown by Atomic layer deposition (ALD) have been integrated with Si-based and 2D FETs [11-13]. Even if the EOT was reduced to aggressive 0.7 nm in 7 nm node of MOSFET, the gate leakage current reached up to 1 A/cm^2 [14]. The high-power consumption caused by such significant leakage current is challenging to be accepted in advanced semiconductor node. Another attractive approach is to adopt new dielectric materials, such as crystalline perovskite ($SrTiO_3$), ionic crystals (CaF_2), molecular crystals (Sb_2O_3) and 2D materials (Bi_2SeO_5 and Bi_2SiO_5) to reduce EOT and maintain low gate leakage current and high gate controllability at the same time [15-20]. These emerging dielectrics achieve a small EOT (sub-1 nm) and a low leakage current. ($<10^{-3}$ A/cm^2), highlighting their remarkable capabilities and promising application in the

Angstrom Era. Nevertheless, the scalability of these materials poses a significant challenge [21,22]. Most of these materials can only be synthesized in small pieces, making them incompatible with the industrial standard of at least 8-inch wafers. Additionally, the high growth temperatures (> 800 °C) required for these materials far exceed the limitations of Si CMOS back-end-of-line (BEOL) processes (< 400 °C). This necessitates an extra transfer step, potentially introducing unwanted impurities into the devices [23].

In this part, we utilize an optimized ALD process with two-oxidation step to synthesize defect-free high-quality 1.3-nm-thick HfO_2 high-κ dielectric layers on 8-inch wafers. The ultrathin HfO_2 films are fabricated at a remarkably low temperature of 200 °C, rendering them compatible not only with back-end-of-line (BEOL) integration of Si CMOS technology but also with oxide TFTs and even 2D FETs. The outstanding uniformity observed across the 8-inch wafers lays the foundation for future large-scale fabrication processes within semiconductor facilities. The exceptional achievement of an extraordinarily small EOT of 0.27 nm, the most diminutive reported in the current literature, can be attributed to its impressive dielectric constant of 18.8 and ultrathin thickness of 1.3 nm. Additionally, the HfO2 film exhibited an exceedingly low leakage current, measuring less than 10^{-14} A/μm^2 at 1 V bias voltage, and showcased a robust breakdown electric field of approximately 32 MV/cm. To evaluate its practicality and efficacy in gate control, we seamlessly integrated the 1.3-nm-thick HfO_2 film as the dielectric layer in cutting-edge 2D monolayer MoS_2 transistors. Remarkably, in devices featuring a 100 nm-long channel, the on-state current density soared to 250 μA/μm and an impressive on/off ratio of 10^8, accompanied by an ultra-low subthreshold slope (SS) of 60 mV/dec. Employing the same dielectric layer, μm-scale MoS_2 transistors exhibited stellar performance, underscoring its versatility

and potential in various transistor applications. Furthermore, leveraging the 8-inch 1.3 nm HfO_2 films and 8-inch monolayer MoS_2, we successfully fabricated logic gates and memory devices, such as inverter, AND, NAND, NOR and SRAM. Our HfO_2 thin film not only fulfils the requirements specified by International Roadmap for Devices and Systems (IRDS) 2022 but also holds substantial implications for the forthcoming advanced semiconductor processes in the angstrom era.

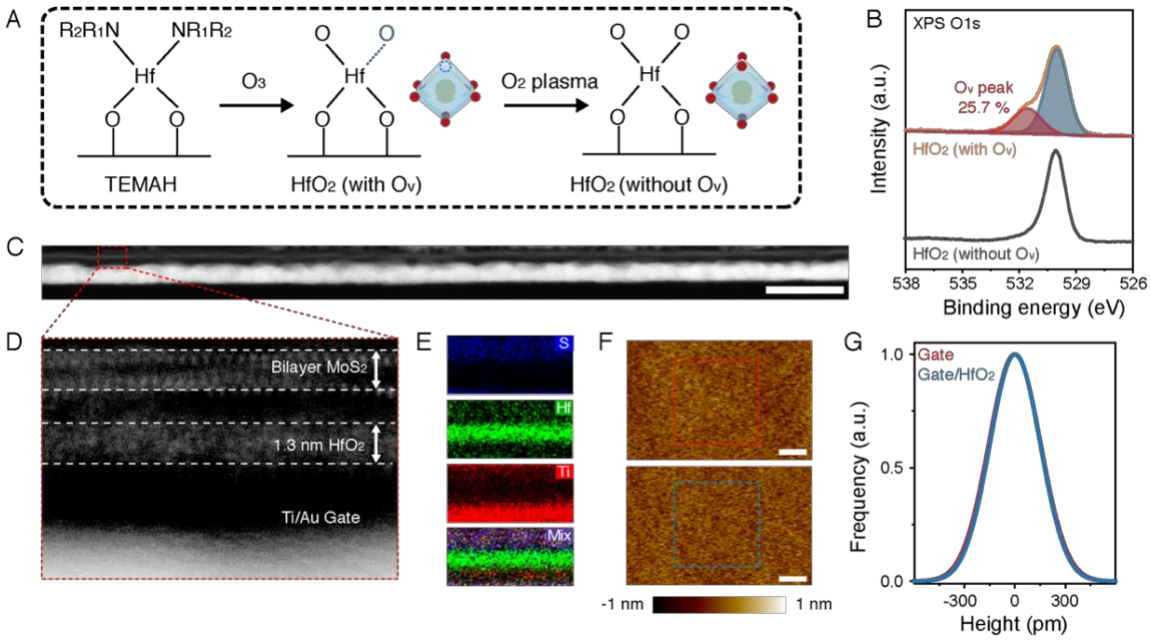

Fig. 4-1. Formation and structure characterization of the ultrathin HfO_2 film. (a) Schematic illustration of HfO_2 with and without O_v. (b) The XPS spectrum of O 1s in HfO_2 with and without O_v. (c) Cross-sectional STEM-HAADF image of the Gate/HfO_2/MoS_2 structure. (d) Enlarged STEM-HAADF image of Gate/HfO_2/MoS_2 stacking layer. (e) STEM-EDS elemental mapping of S, Hf, Ti, respectively, acquired from the same area in (d). (f) AFM images of the metal gate and after depositing HfO_2 without O_v. (g) Height histograms for the surfaces of samples in (f).

4.2. Deposition of ultrathin HfO_2 film with sub-3-Å EOT

We fabricate the ultrathin HfO_2 film with an optimized hybrid ALD process with a two-oxidation step using ozone (O_3) and oxygen plasma (O_2 plasma) as oxygen sources, respectively. (For standard HfO_2 dielectric film preparation, only one oxidation step was applied, which would induce oxygen vacancies (O_v, Fig. 4-1a). With an extra oxidation step with O_2 plasma, the O_v could be repaired and HfO_2 film quality was significantly improved. The X-ray Photoelectron Spectroscopy (XPS) spectrum of O 1s in Fig. 4-1B confirmed the process [24, 25]. An extra oxidation step reduces the O_v from 25.7% to almost zero.

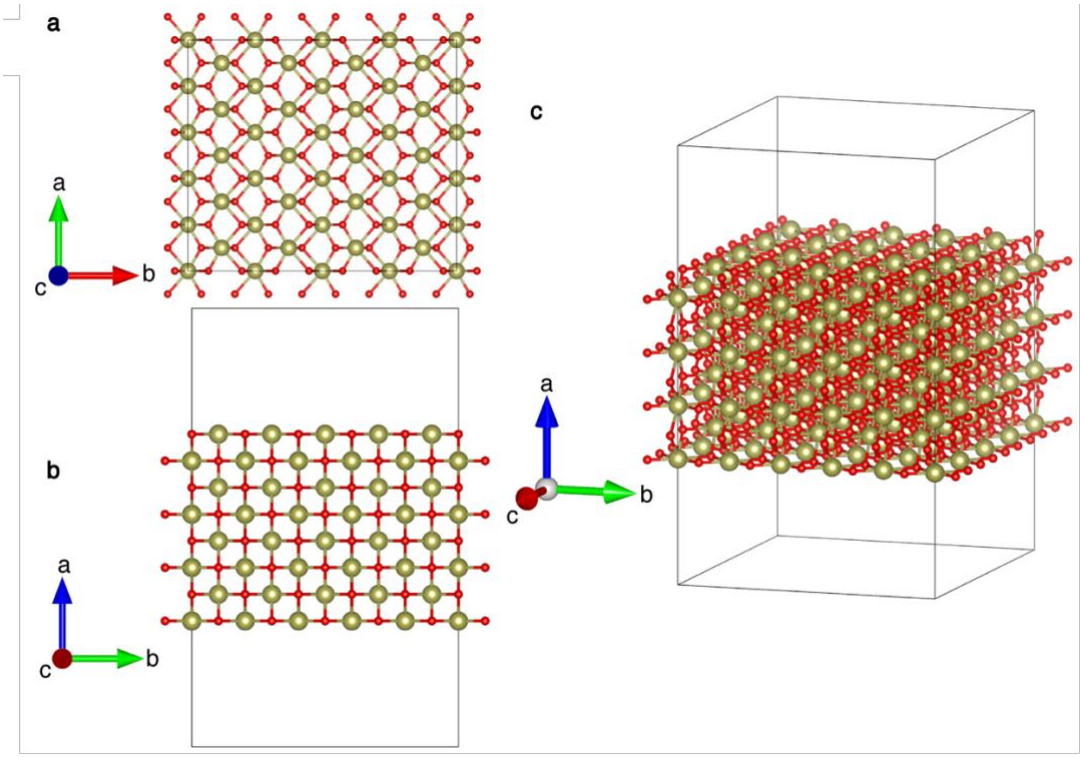

Fig. 4-2. The (a) top, (b) side and (c) perspective views of HfO_2 slab model.

We find that to achieve a continuous film deposition of the HfO_2 ultrathin film, a minimum of 10 cycles is necessary. To further confirm the physical thickness and analyze the quality of 10 cycles HfO_2 film, we show a cross-sectional scanning transmission electron microscopy (CS-STEM) image with a Gate/HfO_2/MoS_2

stacking structure, demonstrating the continuity and uniformity of the ultrathin HfO_2 film in an intermediate-scale observation range of 600 nm (Fig. 4-1c).

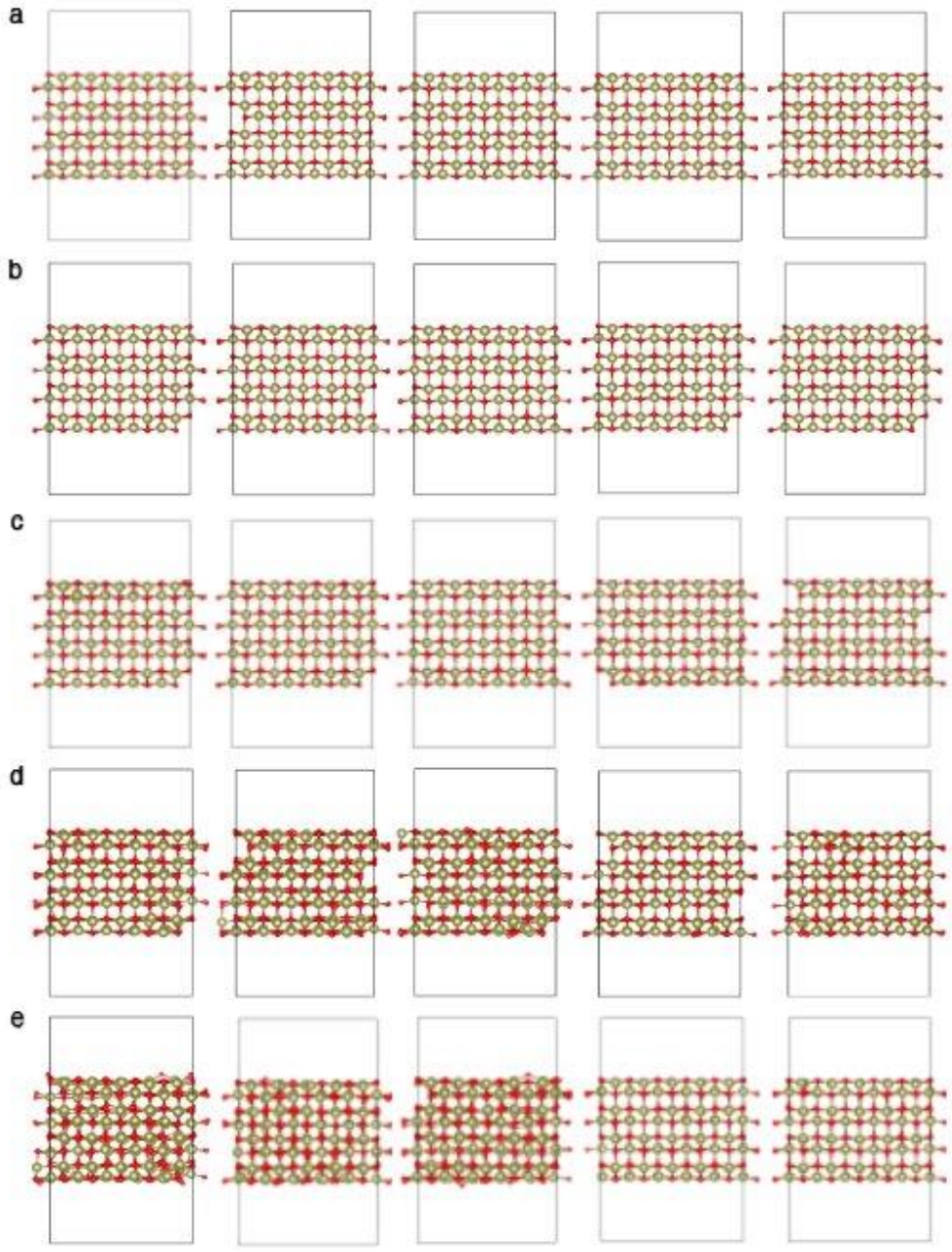

Fig. 4-3. The optimized structures of HfO2 slabs with different vacancy concentrations. (a) 2.2%, (b) 4.4%, (c) 7.2%, (d)10% and (e) 15.6%.

In the enlarged area, two stacking layers of bilayer MoS_2 and HfO_2 were visible clearly and the thickness of the HfO_2 film is found to be approximately equivalent to that of the bilayer MoS_2, measuring 1.3 nm (Fig. 4-1D and **Fig. 4-2**). Moreover, a 0.3 nm gap is observed between HfO_2 film and MoS_2 layer, indicating the clean van der Waals contact interface [26]. The elementary mapping of S, Hf and Ti confirmed the stacking structure of Gate/HfO_2/MoS_2 (Fig. 4-1e). We apply atomic force microscopy (AFM) to verify the uniformity in a larger scale (30 μm).[27] Both the Gate and Gate/HfO_2 exhibit a homogenous and dense surface without any holes (Fig. 4-1f). The mean roughness of Gate and Gate/HfO_2 are 241 and 239 pm, respectively, as shown in the height histogram (Fig. 4-1g).

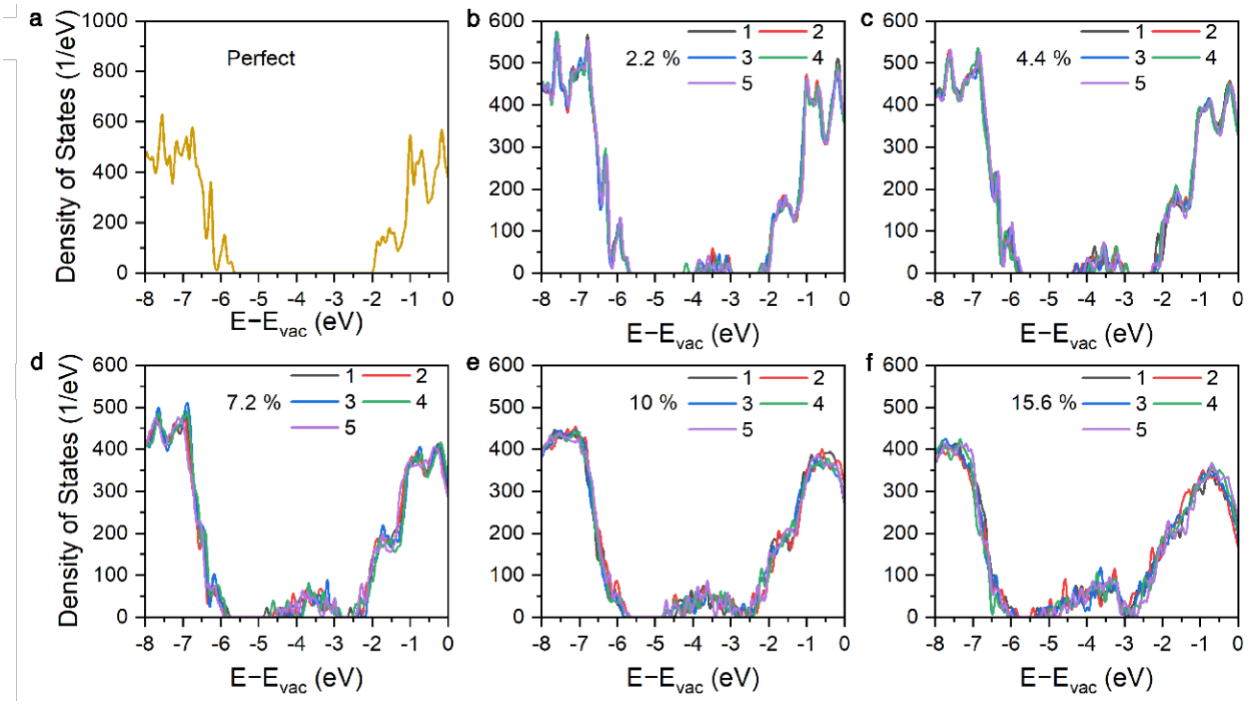

Fig. 4-4. The density of states of HfO_2 slabs with different O vacancy concentrations. For each vacancy concentration, five different random structures are considered. The energy is aligned by setting the vacuum level Evac of each system at zero.

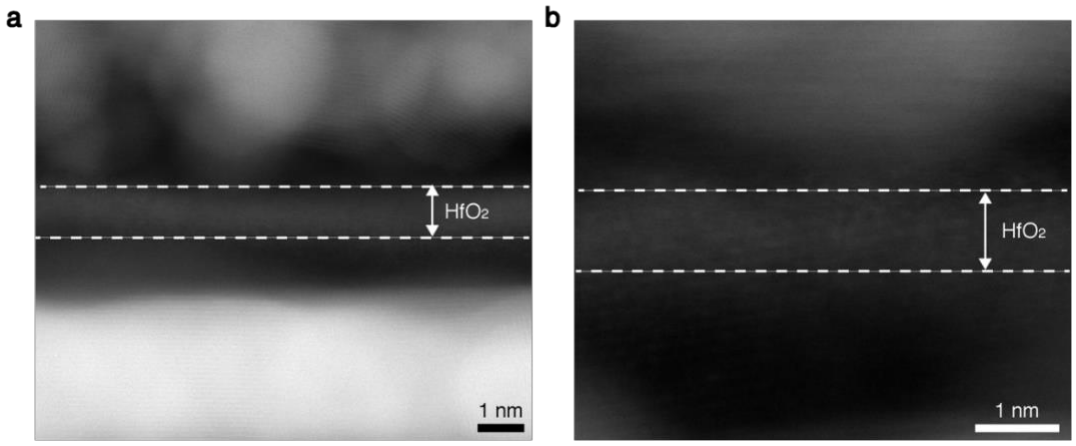

Fig. 4-5. Cross-sectional STEM image of 1.3 nm HfO_2 film in two different areas in Fig. 4-1c.

Scanning capacitance microscopy (SCM) characterization is performed to measure the equivalent oxide thickness (EOT) and effective dielectric constant (ε_{eff}) at high frequency of GHz level. We first investigated the SCM voltage signals of SiO_2 standard samples with gradient thickness (**Fig. 4-3**). Since the SCM voltage signals increase linearly with the increasement of sample capacitance, according to the formula $C=A\,\varepsilon_{eff}\,\varepsilon_0/d$, we will get a linear relationship between SCM voltage signals and $1/d_{SiO2}$ (**Fig. 4-4**). Here, the d_{SiO2} is equal to EOT of samples according to the definition of EOT. This means the EOT of samples could be calculated directly according to the measured SCM signals of samples (**Fig. 4-5** and **Fig. 4-9**a). The SCM voltage signals of ultrathin HfO_2 films with various thickness were measured, and corresponding EOT could be calculated. (Fig. 5-9b) The EOT show a linear relationship with the physical thickness of ultrathin HfO_2 film. When the physical thickness of HfO_2 film below than 5 nm, the EOT is accordingly smaller than 0.9 nm, meeting the technology target of IRDS 2022 (EOT < 0.9 nm before 2037). The smallest EOT of 0.27 nm is calculated in 1.3 nm HfO_2 film, which is the first reported materials with EOT < 0.3 nm. Based on the formular $EOT=3.9\,t_{ox}/\varepsilon_{ox}$, the dielectric constant is calculated around 22 when the physical thickness

was larger than 3 nm, while a little decrease of dielectric constant is obtained in the extreme small physical thickness of ultrathin HfO_2 film.

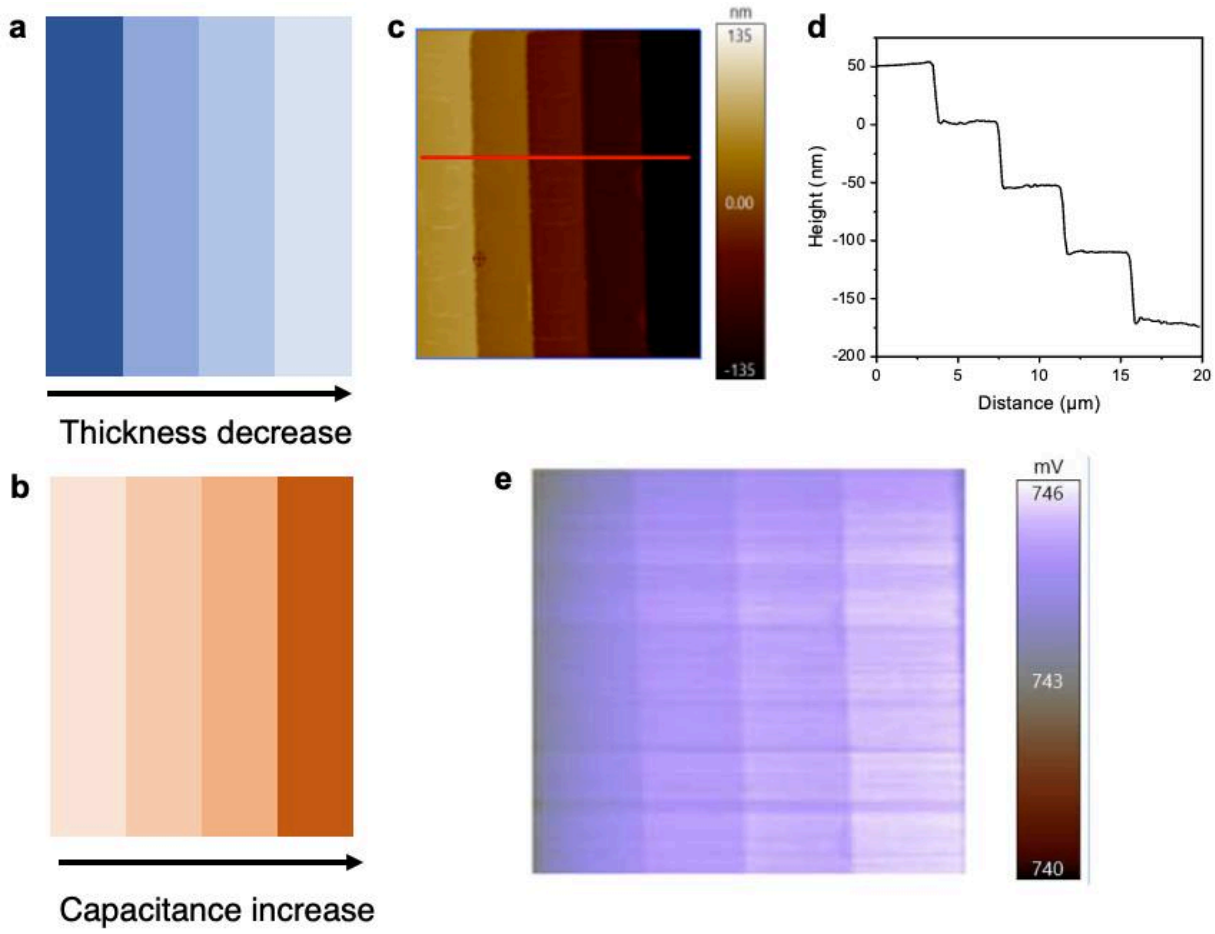

Fig. 4-6. The standard SiO_2 sample for SCM measurement. The schematic view of height (A) and capacitance (B) in SiO_2 standard samples. (C) AFM height diagram of the standard SiO_2 samples. (D) the height profile of four SiO_2 layers with decreased thickness. The origin thickness of the SiO_2 is 300 nm. (E) The SCM voltage signal diagram of the standard SiO_2 samples.

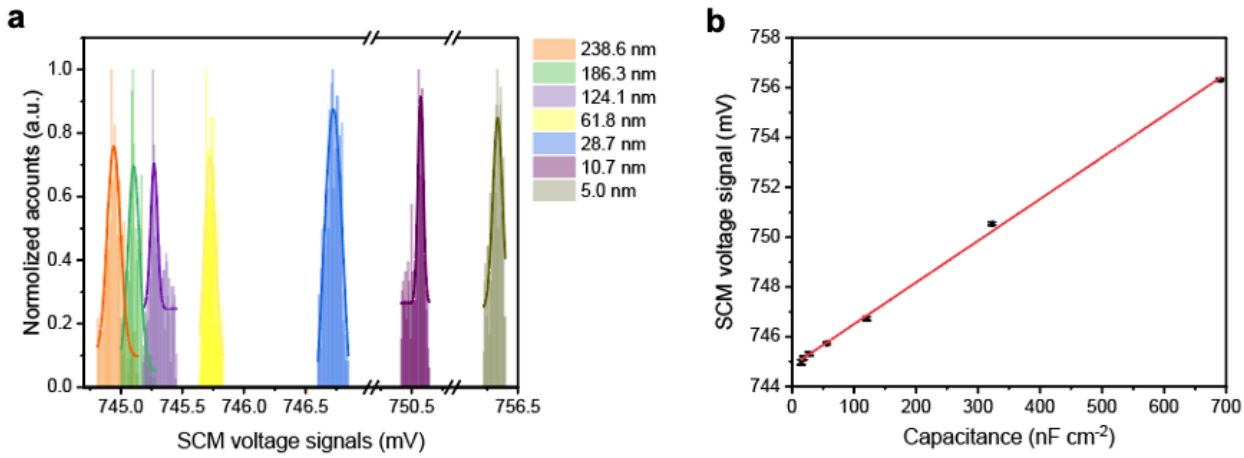

Fig. 4-7. The linear relationship between SCM voltage signals and capacitance of SiO_2 standard samples

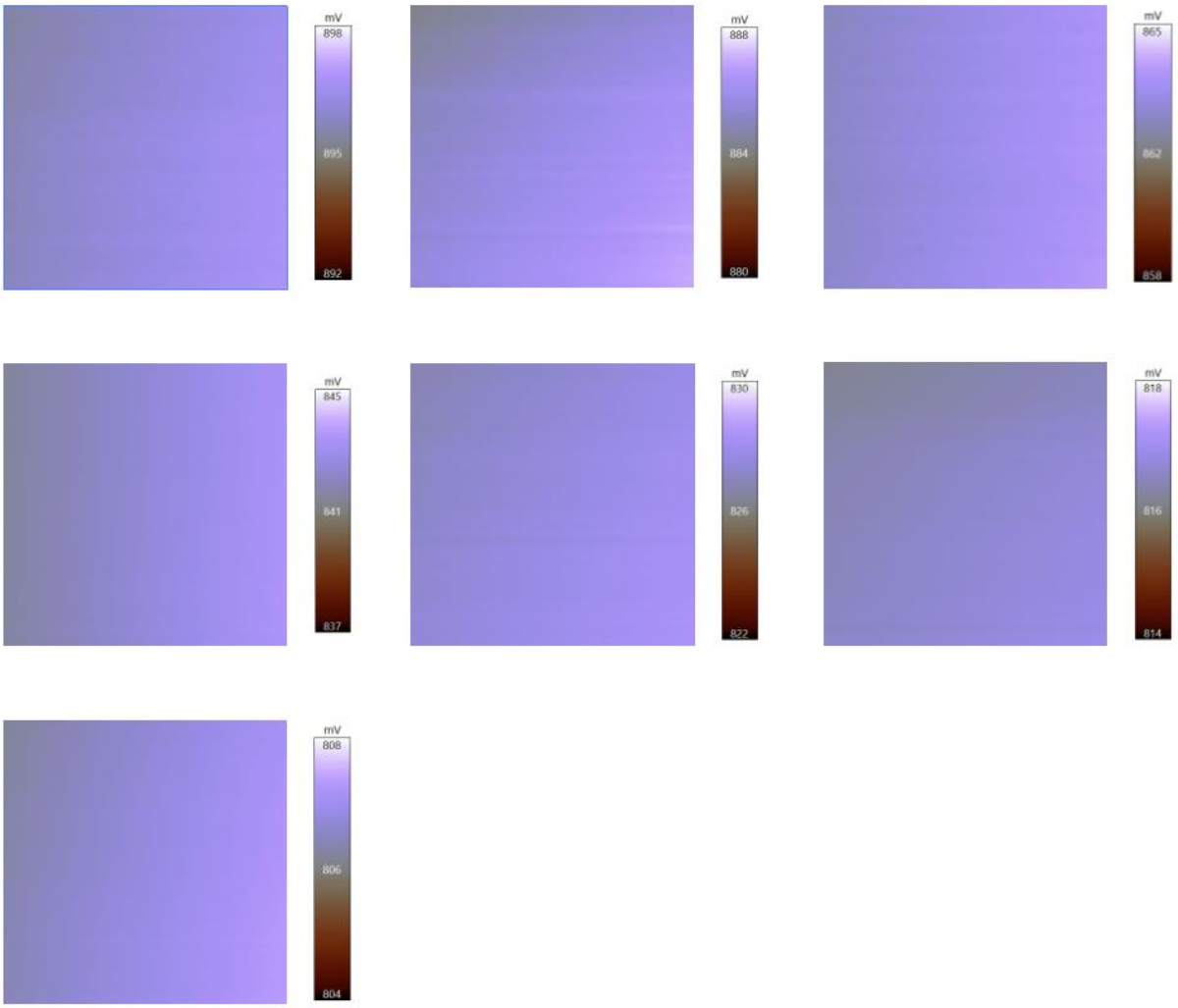

Fig. 4-8. SCM measurement of ultrathin HfO_2 films from 1.3 nm to 5.2 nm.

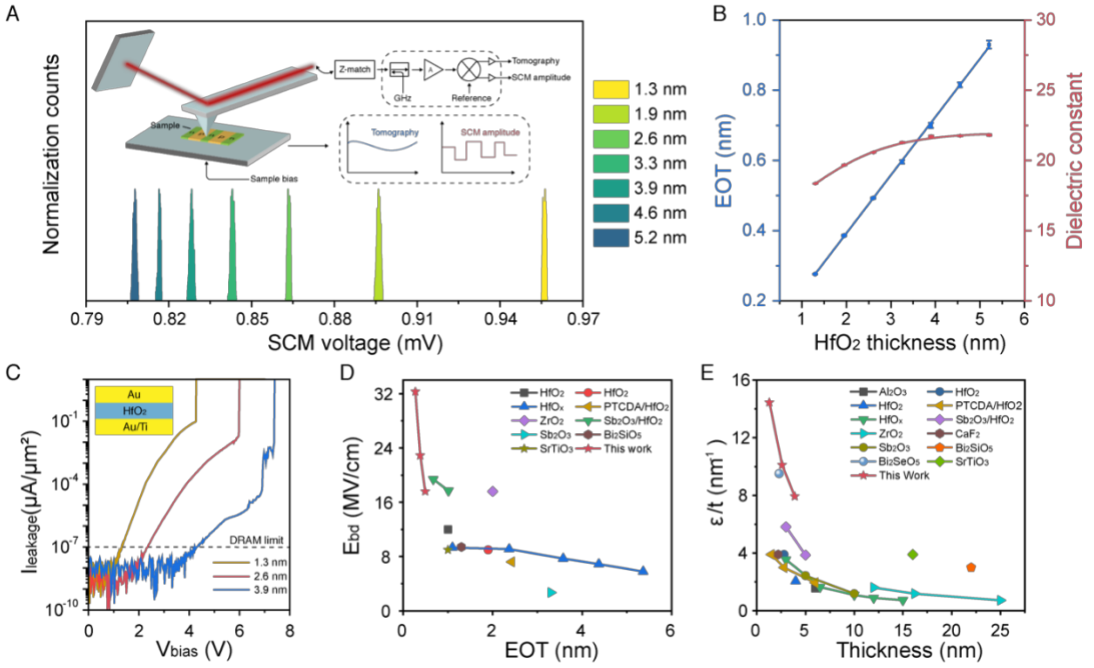

Fig. 4-9. Dielectric properties of the ultrathin HfO_2 films. (A) SCM voltage histogram of ultrathin HfO_2 films with various thickness. The insert shows the operation mechanism of SCM measurement based on AFM. (B) EOT and dielectric constant of ultrathin HfO_2 films with thickness from 1.3 nm to 5.2 nm. (C) bias-voltage-dependent leakage current density in Au/Ti/HfO_2/Au stacking structure with HfO_2 thickness from 1.3 nm to 3.9 nm. (D) The breakdown field versus EOT of dielectric materials, comparison with that reported recently, such as normal ALD oxide, perovskite, organic and oxide buffer layer/HfO_2 and 2D materials. (E) ε_{eff}/t versus physical thickness of dielectric materials.

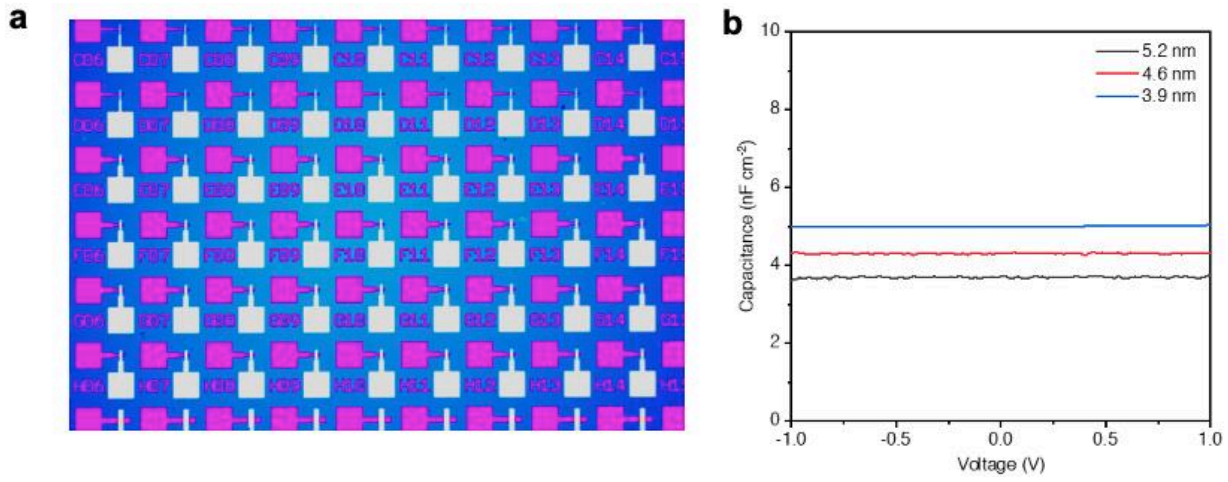

Fig. 4-10 (A). The optical image of HfO_2 MIM devices, (B) Electrical capacitance measurement of HfO_2 films with 3.9 nm, 4.6 nm and 5.2 nm, whose capacitance is coincident with SCM measurement.

The electrical characterization of ultrathin HfO_2 film is evaluated in sandwiched Metal-Insulator-Metal devices (Fig. 4-9c and **Fig. 4-6**). Three ultrathin HfO_2 films with thickness of 1.3 nm, 2.6 nm and 3.9 nm are measured. The breakdown voltage increases with the increase of film physical thickness. The leakage current of all samples remains consistently below the low-power limit of 0.015 A/cm^2 until they reach the point of breakdown. This observation underscores the robust performance and reliability of the samples under low-power conditions, highlighting their suitability for various applications. For the thinnest 1.3 nm HfO_2 film, the current leakage below 10^{-8} $\mu A/\mu m^2$ at bias voltage of 1 V, much lower than the dynamic random-access memory (DRAM) limit. Small current leakage ensures the transistor proper operation with small power consumption and good reliability when utilizing the 1.3 nm HfO_2 as dielectric layer. The current-time curves in Fig S6 also demonstrate the electrical stability of 1.3 nm HfO_2 film. The hard breakdown voltage was 4.2 V, equal to the electrical breakdown field of 32 MV/cm (**Fig. 4-8**). It is important to note that when compared with the optimized ALD process involving two oxidation steps, the 1.3 nm HfO_2 film synthesized using the standard ALD process (which includes only one oxidation step) exhibits direct breakdown under bias voltage (**Fig. 4-10**). We benchmark the HfO_2 film performance with the state-of-the-art sub-3-nm EOT dielectrics, such as normal-ALD HfO_2 film, crystalline perovskite $SrTiO_3$, ion crystals CaF_2 and 2D Bi_2SiO_5 (Fig. 4-9d). It is noteworthy that our ultrathin HfO_2 films exhibit the recording smallest EOT and highest electrical breakdown field at the same level, demonstrating its promising application in advanced low-power and high-performance field-effect transistors [28,29]. The parameter ε_{eff}/t represents the gate

controllability of dielectric films when integrated into transistors. Here, we plot the ε_{eff}/t against the physical thickness of dielectric films to compare the gate controllability with various dielectrics to make a comparative analysis of gate controllability across various dielectrics (Fig. 4-9e) [30]. The results indicate that the superiority of our ultrathin HfO_2 film over all previously reported dielectrics. This suggests that transistors employing our ultrathin HfO_2 film as dielectrics can achieve a high carrier density under the same effective gate voltage, while simultaneously maintaining minimal current leakage. It was noted that Bi_2OSe_5 also exhibited high ε_{eff}/t value with small physical thickness, while its current leakage up to 1 μA/ μm^2 [14,15,17-20,31-35].

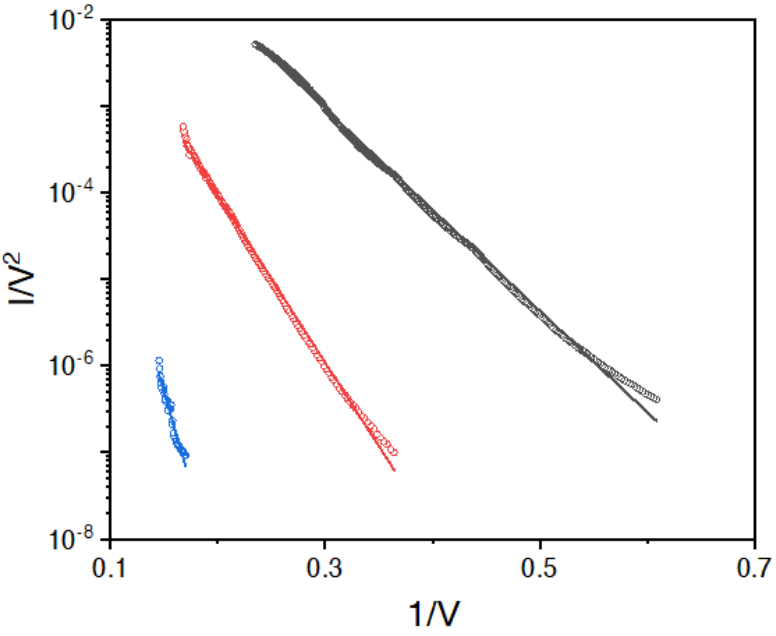

Fig. 4-11. Breakdown mechanism of F-N tunneling in 1.3 nm (black), 2.6 nm (red) and 3.9 nm (blue) HfO_2 film

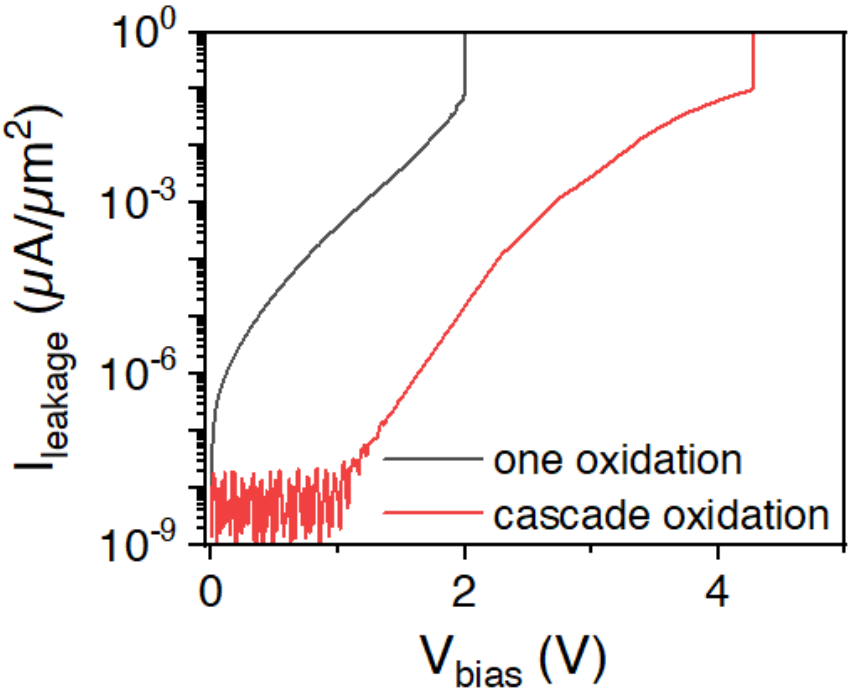

Fig. 4-12. The electrical measurement of ALD HfO_2 with normal one-oxidation step and MOALD with co-oxidation step

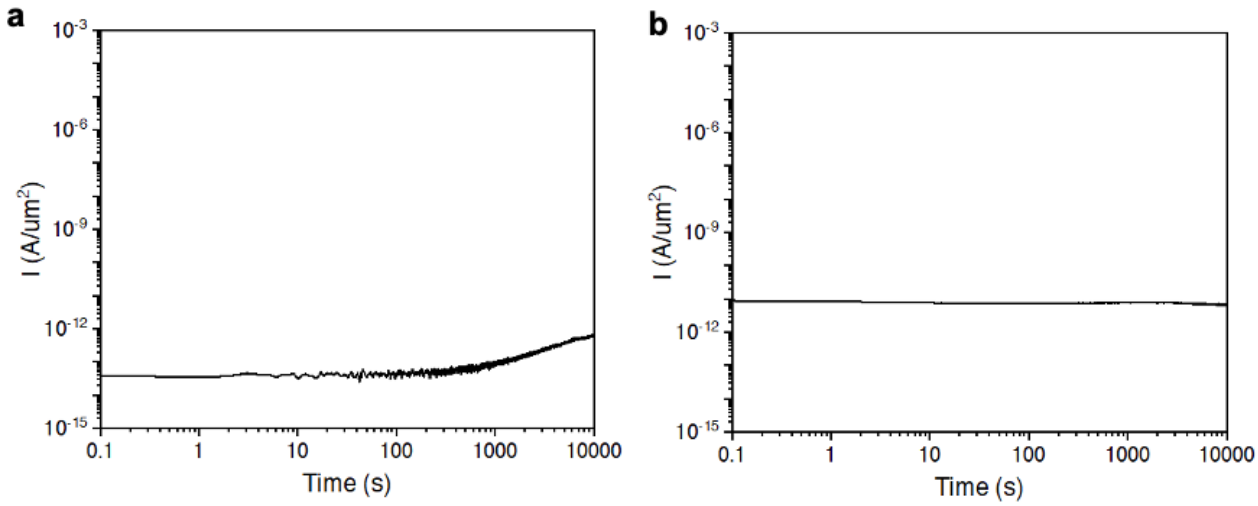

Fig. 4-13. The electrical stability of 2.7-Å-EOT HfO2 film under 0.8 V (A) and 1.0 V (B).

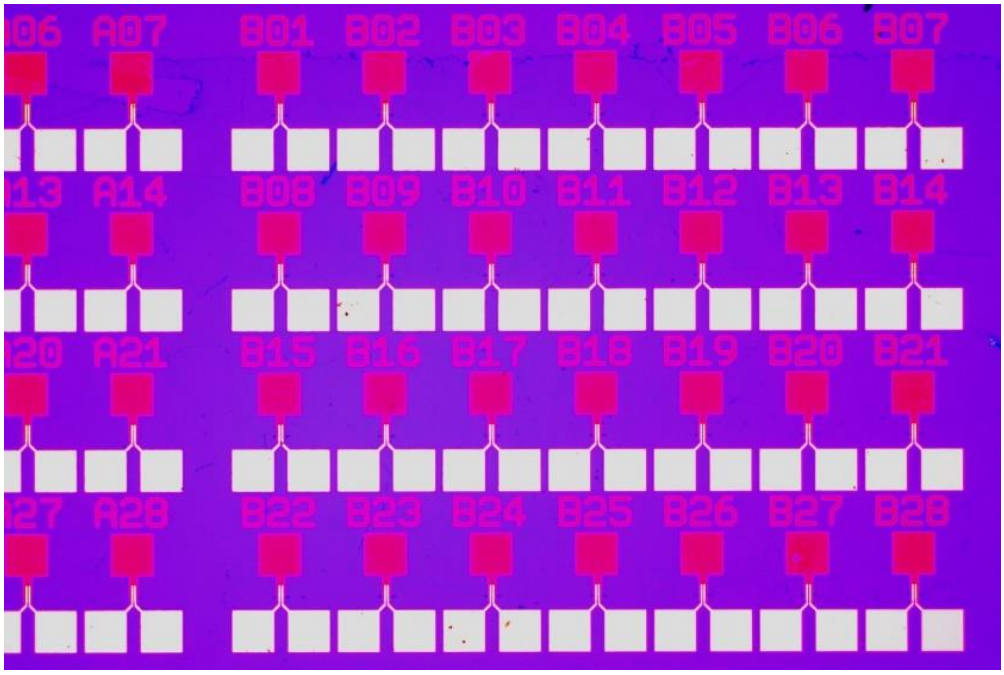

Fig. 4-14. Optical images of μm-length MoS_2 devices

4.3. Scalable MoS_2 field-effect transistors with ultrathin HfO_2 film

We integrate 1.3 nm HfO_2 dielectric films into 100 nm channel-length monolayer MoS_2 FETs. Fig. 4-15a show a typical transfer curve of transistors, validating the functional stability of 1.3 nm HfO_2 in transistors. The gate leakage is below 10^{-5} μA/μm at gate voltage of 1 V. The transfer curve also shows a small SS of 60 mV/dec and a large on-off ratio of 10^8. An ultrasmall hysteresis of 7 mV indicates the small trap density of 1.3 nm HfO_2 film and HfO_2/MoS_2 interfaces, which is partly attributed to the vdW contact of HfO_2 and MoS_2 (Fig. 4-15b). The on-state current density goes beyond 250 μA/μm at a gate voltage of 1 V and a source-drain voltage of 0.5 V, attributed to good gate controllability of HfO_2 dielectrics and high carrier density of MoS_2 film (Fig. 4-15c). Note that if semimetal Sb used as contact materials and short-channel (such as sub-10 nm channel length) is fabricated, the on-state current maybe further improves to a magnitude of mA/μm [36] μm-length MoS_2 devices (2 μm length and 5 μm width) are also fabricated to confirm the

effectiveness of HfO_2 dielectric film in a larger area (Fig. 4-15d and **Fig. 4-11**). A large on/off ratio and high on-state current (up to 120 μA) are maintained.

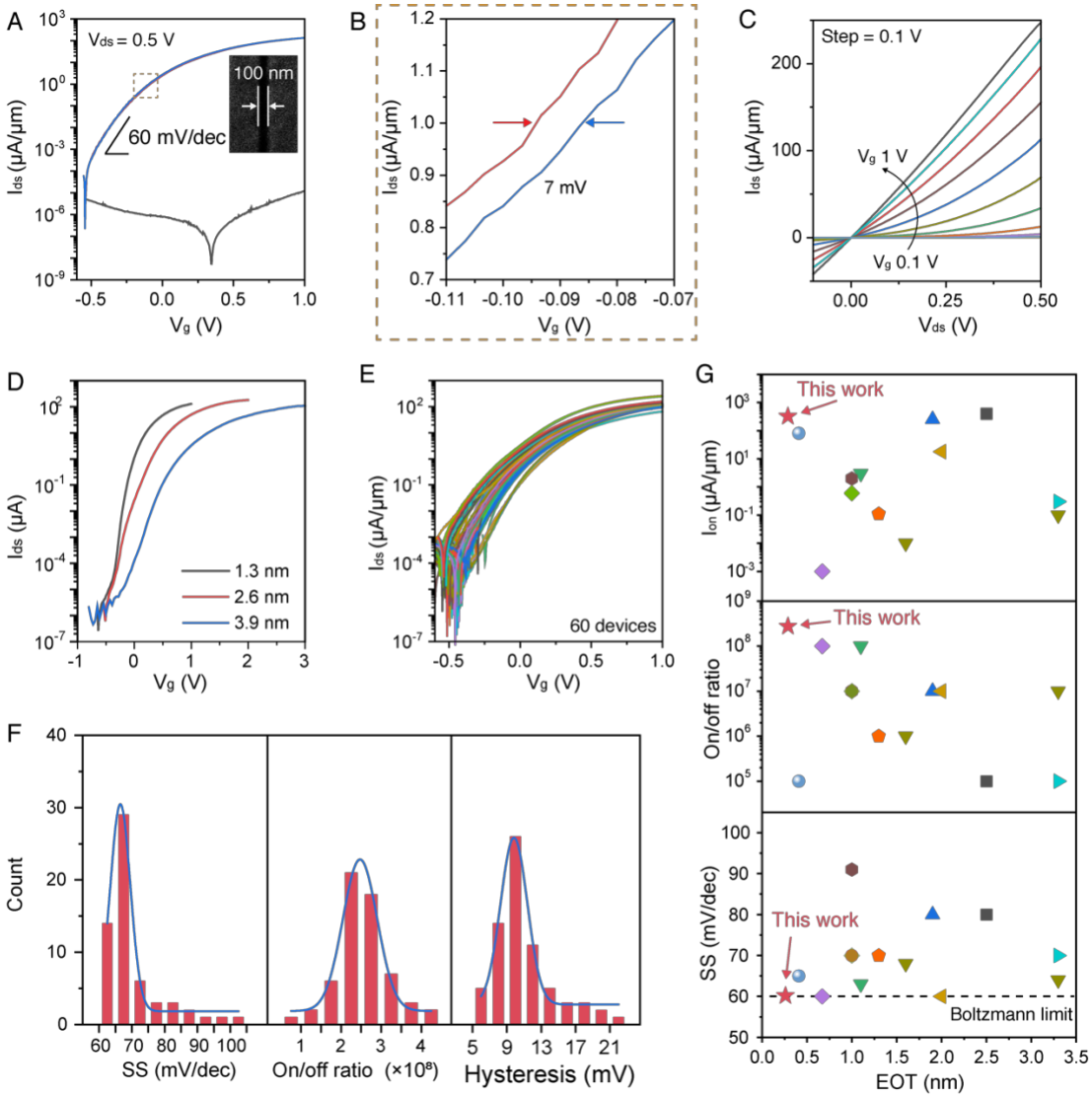

Fig. 4-15. 100 nm channel-length MoS_2 FET performance with 1.3 nm HfO_2 film as dielectric layer. (A) Bidirectional transfer curve and gate leakage of the MoS_2 FET with 1.3 nm HfO_2 dielectrics. The insert is SEM image of the device. (B) Enlarged area in (A), showing the hysteresis of the transfer curve. (C) Output curve of the MoS2 FET with 1.3 nm HfO_2 dielectrics. (D) 2 μm channel-length MoS_2 FET with 1.3 nm, 2.6 nm, and 3.9 nm HfO_2 dielectrics. (E) Transfer curves of 60 FET devices with 1.3 nm HfO_2 dielectrics and (F) their statistical

As the thickness of HfO_2 decreases, the SS of the devices become smaller, indicating the gate controllability increasement, which is consistent with the results in **Fig. 4-9**. Fig. 4-15e present the transfer curves of 60 MoS_2 FET devices with 100 nm-length channels. The corresponding SS, on/off ratio and hysteresis were analyzed in Fig. 4-15f. A number of devices shows a small SS of 62 mV/dec, a high on/off ratio of 2.51×10^8, and a small hysteresis of 10 mV. We summarize the on-state current, on/off ratio and SS values achieved from the two-dimensional FETs with sub-3.5-nm EOT dielectrics. Our devices exhibit superior performance than other FETs.

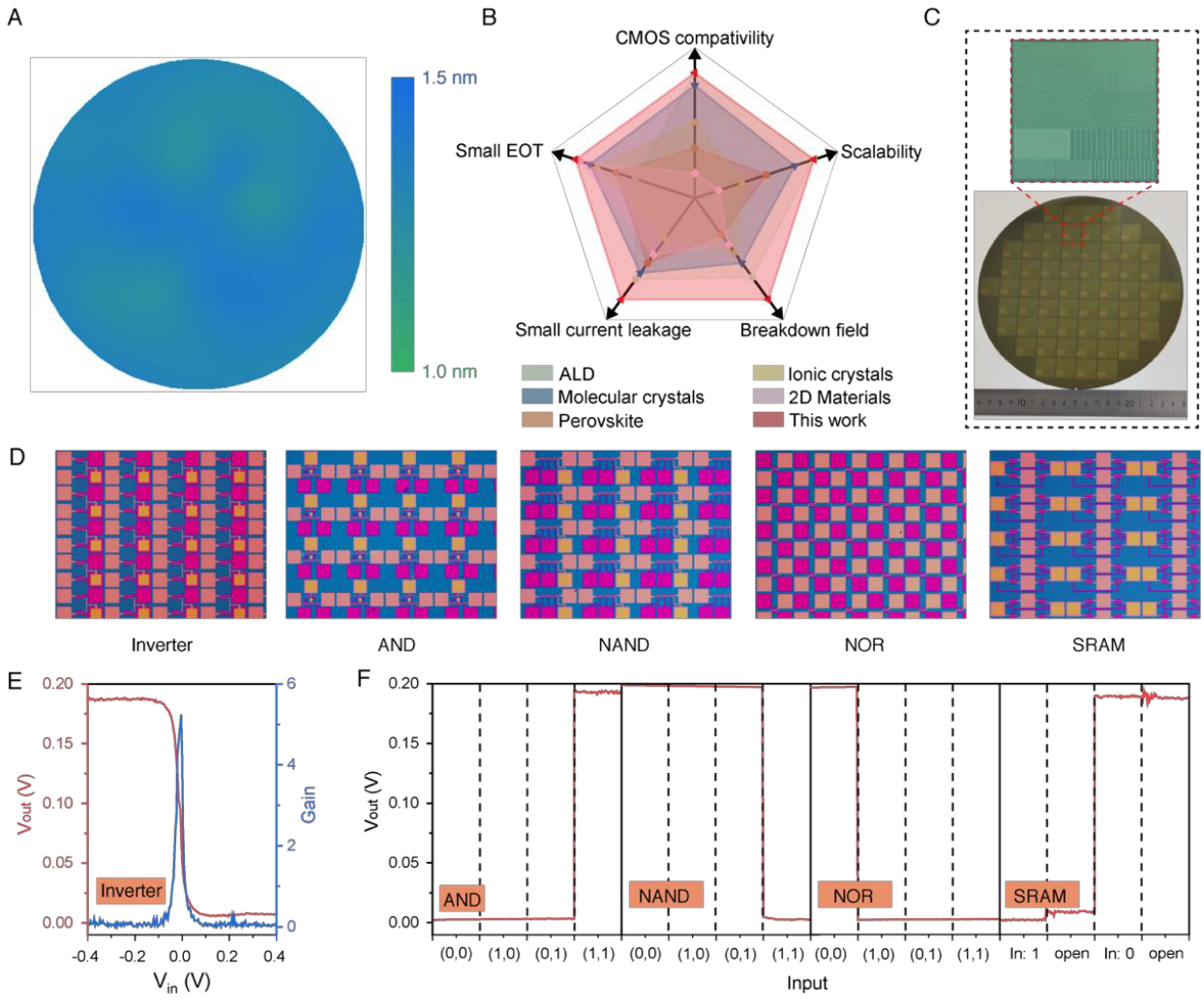

Fig. 4-16. 8-inch wafer of MoS_2 FET and circuits realization integrated with 1.3 nm HfO_2 film and monolayer MoS_2. (A) Ellipsometer height mapping of 8-inch wafer of 1.3 nm HfO_2 film. (B) A radar comparison between our work and other dielectric growth methods in terms of small EOT, small current leakage, breakdown field, scalability and CMOS compatibility. (C) Photos of 8-inch wafer of MoS_2 FET and circuits. (D) Optical images of logic Inverter, AND, NAND, NOR and SRAM devices. (E) Voltage transfer curve and gain of a logic inverter with V_{dd} = 0.2 V. (F) Output curves of logic AND, NAND, NOR and SRAM devices as a function of input voltage pulse of V_{dd} = 0.2 V.

4.4. 8-inch wafer scale MoS_2 circuits with ultrathin HfO_2 film

To confirm the scalability of the ultrathin HfO_2 film, we first deposit the 1.3 nm HfO_2 film on 8-inch wafer of SiO_2/Si substrate and measure its thickness using ellipsometer (**Fig. 4-16**a). This wafer-scale thin film demonstrates exceptional uniformity, boasting an average thickness of 1.3 nm with a margin of error of just 200 pm. Compared with reported sub-1-nm EOT materials, such as crystalline perovskite $SrTiO_3$, 2D Bi_2SeO_5 and Bi_2SiO_5, molecular crystals Sb_2O_3, ionic crystals CaF_2, and standard ALD PTCDA/HfO_2 film, our defect-free ultrathin HfO_2 film, prepared through a two-step oxidation process, indicates an unparalleled characteristics and superiority (Fig. 4-16b). For instance, its remarkably low growth temperature of just 200 °C enables seamless integration with silicon CMOS processes, making it ideal for applications in systems combining 2D materials with silicon. It can also be effectively utilized in Si-based and oxide thin-film transistor devices, a capability that sets it apart from both perovskite materials (1000 °C) and 2D materials (750 °C). Moreover, we have successfully developed a transistor dielectric layer on an 8-inch wafer, a milestone that significantly surpasses the limitations of other sub-1-nm materials (4-inch maximum). The ultrathin HfO_2 film also boasts remarkable gate control capability, an exceptionally high breakdown

electric field, and minimal leakage current, despite its incredibly physical thickness of only 1.3 nm and an EOT of 0.27 nm.

We further fabricated 8-inch monolayer MoS_2 FET and circuits with 1.3 nm HfO_2 film as dielectric layer (Fig. 4-16c and **Fig. 4-17**). As the logic gate and memory are the basic units of integrated circuits, we make inverters, AND, NAND, NOR logic gates and SRAM devices in a single die. (Fig. 4-16d) The voltage transfer curve of the inverter showed typical characteristics and gain of 5.2 with an ultralow supply voltage of 0.2 V (Fig. 4-16e). The power supply is significantly smaller than that of FETs made with other sub-1-nm EOT dielectric layers, owing to its ultra-thin thickness and exceptional gate control capabilities. The AND, NAND, NOR logic gates and SRAM could also be driven with 0.2 V. This significantly contributes to the reduction of the power consumption in the very large-scale circuits. (Fig. 4-16f)

4.5. Summary

In conclusion, we utilize an optimized ALD process with two-oxidation step to deposit defect-free high-quality 1.3-nm-thick HfO_2 high-κ dielectric layers on 8-inch wafers at only 200 °C. Our ultrathin HfO_2 film shows an extraordinarily small EOT of 0.27 nm, a ultrasmall leakage current of 10^{-14} A/μm^2 at 1 V bias voltage, and a robust breakdown electric field of approximately 32 MV/cm. We also fabricate MoS_2 transistors and circuits with 1.3-nm-thick HfO_2 as dielectric layers to demonstrate its practicality and gate controllability. Typical transistors exhibit large on-state current density of 250 μA/μm and an impressive on/off ratio of 10^8, accompanied by an ultra-low subthreshold slope of 60 mV/dec. Logic gates and memory devices are also fabricated on 8-inch wafers to demonstrate its substantial implications for the forthcoming advanced semiconductor processes in the angstrom era.

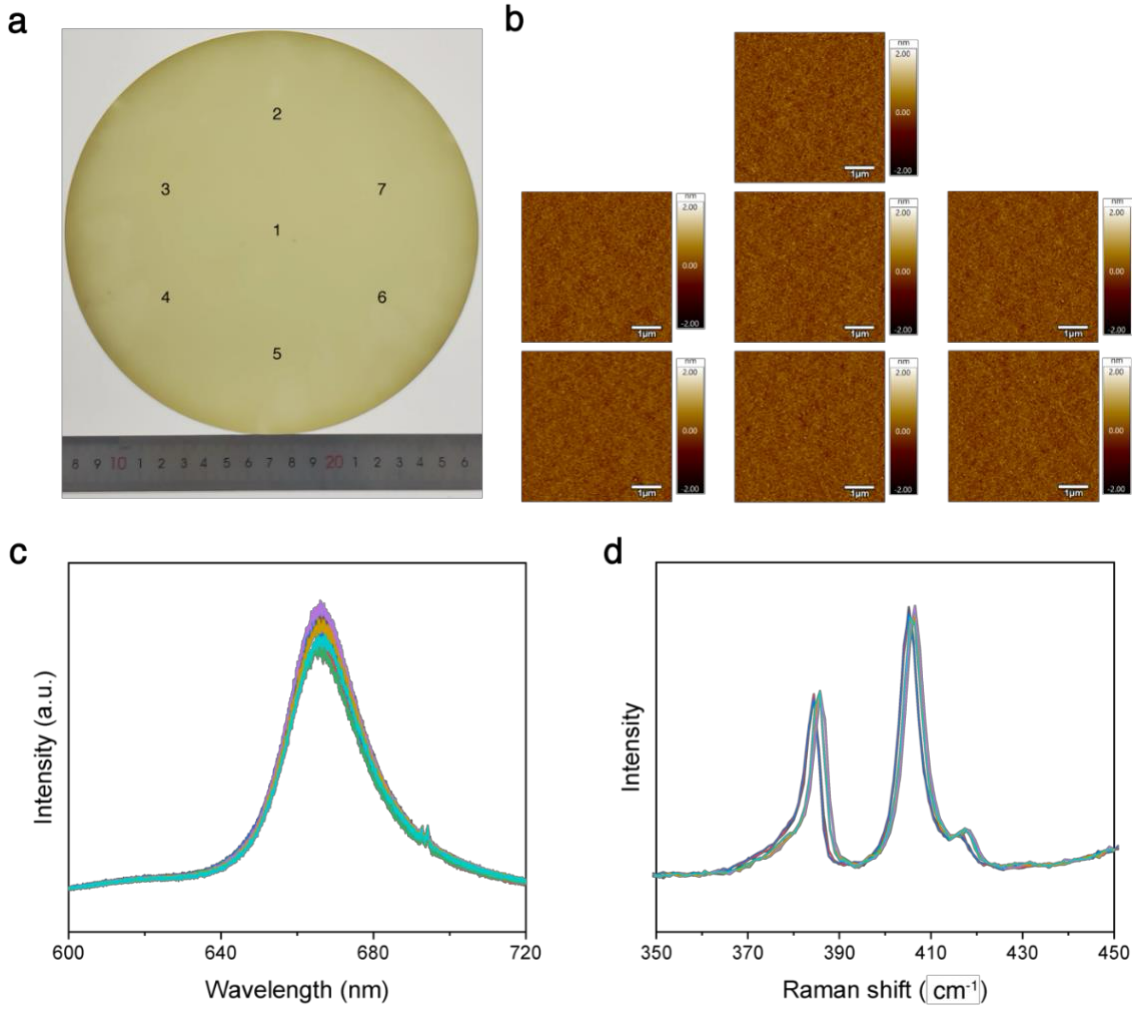

Fig. 4-17. The characterization of 8-inch MoS_2 samples. Each measurement was tested from 7 different point. (a) Optical images 8-inch MoS_2 wafers. (b) AFM, (c) PL and (d) Raman spectra of 7 points marked in (a).

4.6. References

1. Cao, W. et al. The future transistors. Nature 620, 501–515 (2023).

2. Mistry, K. et al. A 45nm Logic Technology with High-κ+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging. 2007 IEEE Int. Electron Devices Meet., 247–250 (2007).

3. Lundstrom, M. S. et al. Moore's law: The journey ahead. Science 378, 722–723 (2022).

4. Först, C. J. et al. The interface between silicon and a high-κ oxide. Nature 427, 53–56 (2004).
5. Desai, S. B. et al. MoS_2 transistors with 1-nanometer gate lengths. Science 354, 99–102 (2016).
6. Li, N. et al. Large-scale flexible and transparent electronics based on monolayer molybdenum disulfide field-effect transistors. Nat. Electron. 3, 711–717 (2020).
7. Tang, J. et al. Nat. Commun. 14, 3633 (2023).
8. O'Brien, K. P. et al. Process integration and future outlook of 2D transistors. Nat. Commun. 14, 6400 (2023).
9. Sicard, E. et al. Introducing 3-nm Nano-Sheet FET technology in Microwind. (2021).
10. Xu, Y. et al. Scalable integration of hybrid high-κ dielectric materials on two-dimensional semiconductors. Nat. Mater. 22, 1078–1084 (2023).
11. Cheema, S. S. et al. Ultrathin ferroic HfO2–ZrO2 superlattice gate stack for advanced transistors. Nature 604, 65–71 (2022).
12. International Roadmap for Devices and Systems. (2022).
13. Jin, Y. et al. Controllable Oxidation of ZrS_2 to Prepare High-κ, Single-Crystal m-ZrO_2 for 2D Electronics. Adv. Mater. 35, e2212079 (2023).
14. Li, W. et al. Uniform and ultrathin high-κ gate dielectrics for two-dimensional electronic devices. Nat Electron 2, 563–571 (2019).
15. Huang, J.-K. et al. High-κ perovskite membranes as insulators for two-dimensional transistors. Nature 605, 262–267 (2022).
16. Illarionov, Y. Yu. et al. Ultrathin calcium fluoride insulators for two-dimensional field-effect transistors. Nat Electron 2, 230–235 (2019).
17. Liu, K. et al. A wafer-scale van der Waals dielectric made from an inorganic molecular crystal film. Nat Electron 4, 906–913 (2021).

18. Zhang, Y. et al. A single-crystalline native dielectric for two-dimensional semiconductors with an equivalent oxide thickness below 0.5 nm. Nat. Electron. 5, 643–649 (2022).
19. Chen, J. et al. Vertically grown ultrathin Bi_2SiO_5 as high-κ single-crystalline gate dielectric. Nat. Commun. 14, 4406 (2023).
20. Lau, C. S. et al. Dielectrics for Two-Dimensional Transition-Metal Dichalcogenide Applications. ACS Nano 17, 9870–9905 (2023).
21. Ye, K. et al. An overview of advanced methods for the characterization of oxygen vacancies in materials. Trends Anal. Chem. 116, 102–108 (2019).
22. Qi, J. et al. A family of functional oxides of titanosilicates: A2TiSi2O8 (A= Ba, Sr) with temperature insensitive ultrahigh breakdown strength. J. Eur. Ceram. Soc. 40, 3027–3034 (2020).
23. Khaldi, O. et al. Correlations between first-principles calculations and electric properties of HfO2:Al2O3 alloys for metal–insulator–metal (MIM) capacitor applications. J. Appl. Phys. 128, 134101 (2020).
24. Xing, J. et al. Realizing High Comprehensive Energy Storage and Ultrahigh Hardness in Lead-Free Ceramics. ACS Appl. Mater. Interfaces 13, 28472–28483 (2021).
25. Hui, F. et al. Scanning probe microscopy for advanced nanoelectronics. Nat. Electron. 2, 221–229 (2019).
26. Bian, K. et al. Scanning probe microscopy. Nat. Rev. Methods Prim. 1, 36 (2021).
27. Matey, J. R. et al. Scanning capacitance microscopy. J. Appl. Phys. 57, 1437–1444 (1985).
28. Akinwande, D. et al. Graphene and two-dimensional materials for silicon technology. Nature 573, 507–518 (2019).

29. Das, S. et al. Transistors based on two-dimensional materials for future integrated circuits. Nat. Electron. 4, 786–799 (2021).
30. Li, T. et al. A native oxide high-κ gate dielectric for two-dimensional electronics. Nat. Electron. 3, 473–478 (2020).
31. Luo, P. et al. Molybdenum disulfide transistors with enlarged van der Waals gaps at their dielectric interface via oxygen accumulation. Nat. Electron. 5, 849–858 (2022).
32. Pang, C.-S. et al. Sub-1nm EOT WS_2-FET with IDS > 600μA/μm at VDS=1V and SS < 70mV/dec at LG=40nm. 2020 IEEE Int. Electron Devices Meet. (IEDM) 00, 3.4.1-3.4.4 (2020).
33. Zhu, K. et al. The development of integrated circuits based on two-dimensional materials. Nat. Electron. 4, 775–785 (2021).
34. English, C. D. et al. Approaching Ballistic Transport in Monolayer MoS_2 Transistors with Self-Aligned 10 NM Top Gates. 2016 IEEE Int. Electron Devices Meet. (IEDM), 5.6.1-5.6.4 (2016).
35. Li, M.-Y. et al. How 2D semiconductors could extend Moore's law. Nature 567, 169–170 (2019)
36. Liu, Y. et al. Promises and prospects of two-dimensional transistors. Nature 591, 43–53 (2021).

Chapter 5. Topological flux-closure ferroelectric transistor arrays

Ferroelectric topological structures are promising new candidates for high-performance memories with excellent stability and low power consumption. Abundant ferroelectric materials and topological structures have been found and investigated over the past decade; however, integration of them into memory devices has greatly delayed, mostly due to the constraint from their substrates. In this work, we demonstrate, for the first time, scalable topological ferroelectric field-effect transistors (Fe-FETs) based on large-scale uniform flux-closure topological ferroelectric films epitaxially grown on substrates with sacrificial layers. Unlike the previous coexistence of trivial and nontrivial domains, the rigid single flux-closure arrays can stably exist in freestanding films and can be erased by increasing temperature over a critical point, rather than undergoing a phase transition to ferroelastic domains as previously reported. Moreover, the flux-closure capacitors demonstrate exceptional performances such as small coercive voltages, negligible leakage currents, a remanent polarization reaching 195 $\mu C/cm^2$, and an endurance of up to 10^9 cycles. Furthermore, CMOS-compatible Fe-FET arrays are fabricated, featuring a large memory window of 7 V, high ON/OFF ratio of 10^8, good endurance and stability, and superior flexibility. Our work paves a way towards the ferroelectric memory devices in future semiconductor industries and flexible electronics.

5.1. Introduction

Modern memory technology usually requires a combination of multiple advanced properties, such as non-volatility, high speed (~ps), low power consumption (~fJ), and non-destructive detection of the memory state [1-3]. As highlighted in the International Roadmap for Devices and Systems (IRDS) 2023, ferroelectric memories are pivotal in the semiconductor industry [4], having these advanced properties. Over the past two decades, various ferroelectric materials, such as

doped hafnium oxide, PZT and AlScN, have been investigated and integrated with silicon-based complementary metal-oxide-semiconductor (CMOS) technology, while challenges remain for their applications in cutting-edge memory devices for the relatively large leakage currents, slow switching speeds, fatigue over time, low polarizations and unshrinkable domain sizes [5,6]. Therefore, it is extremely urgent to develop CMOS-compatible ferroelectric devices with excellent performances [7,8].

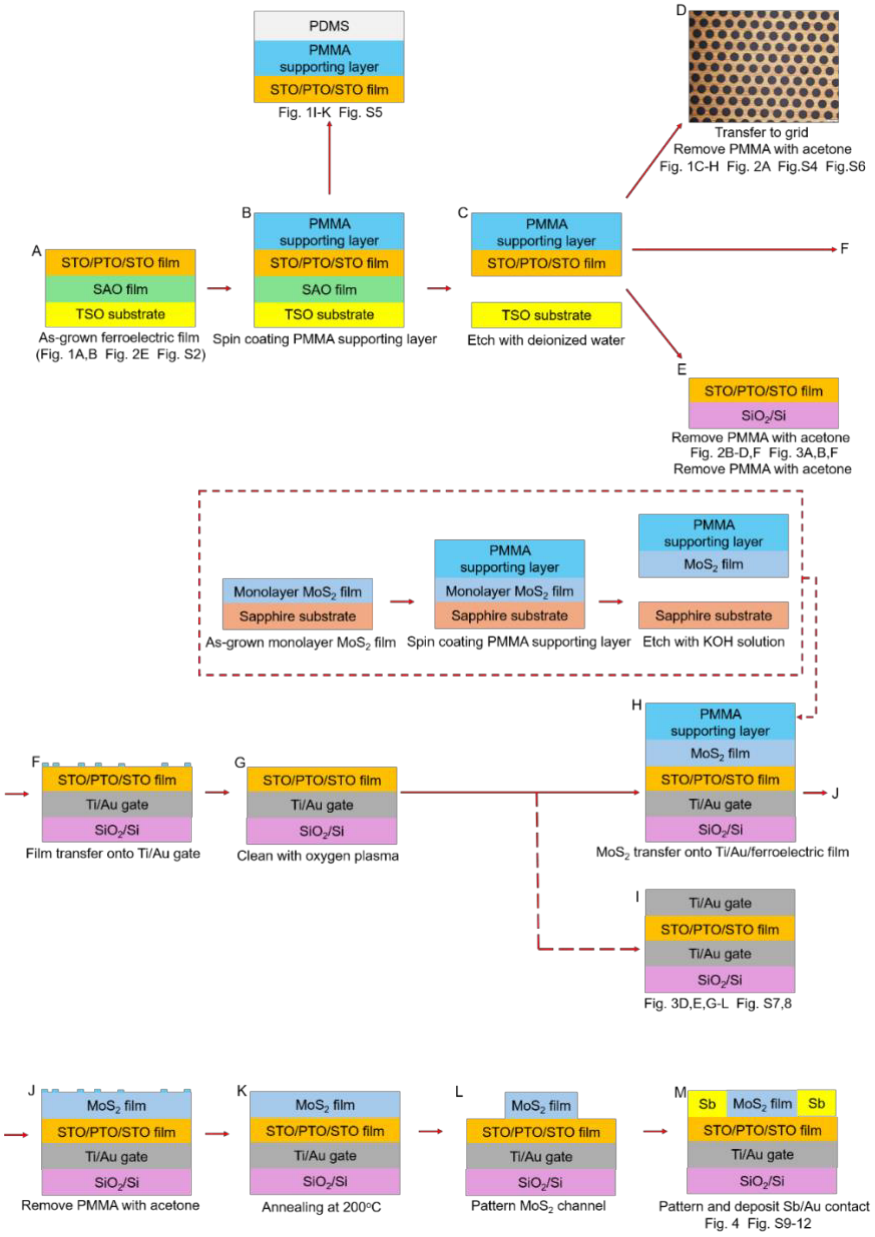

Fig. 5-1. Experiment flowchart. (**a**) Schematic showing detailed samples information. Multilayer films [SAO/(STO_7/PTO_{30})$_2$/STO_7] grown on $TbScO_3$ $(110)_o$ substrate. (**b**) Spin-coating PMMA on the sample surface. Sample with spin-coated PMMA adhered using PDMS. (**c**) Spin-coated PMMA sample in deionized water for SAO layer dissolution. (**d**) PMMA-supported film lifted with a holey carbon TEM grid, dried, and immersed in acetone to dissolve PMMA. (**e**) Transfer the PMMA-supported film onto the wafer, dry it, and immerse it in acetone to dissolve the PMMA. (**f** and **g**) Transfer the PMMA-supported film onto the wafer with deposited bottom electrodes, immerse it in acetone to dissolve the PMMA, and use plasma to clean residual PMMA from the sample surface. (**h**) Transfer MoS_2 onto a clean sample surface. Here, omission of MoS_2 film growth and transfer details. (**i**) Following the schematic diagram (G), deposition of top electrodes on the sample surface to fabricate capacitors. (**j**) Following the schematic diagram (H), transfer the sample into the acetone to dissolve the PMMA, and use plasma to clean residual PMMA from the sample surface. (**k**) Thermal treatment of the sample. (**l**) Channel fabrication. (**m**) Photolithography and electrode deposition.

Topological ferroelectrics (TFs), distinct from the conventional ferroelectric materials, possess topological protection of the ferroelectric states thus are resistant to the external disturbances, offering, in principle, an exceptional stability in topological electronic devices. TFs also exhibit regular spontaneous polarization (P_s), allowing the polarization state to be retained even after the external electric field is removed, thereby enabling the data storage without continuous power supply and significantly reducing the energy consumption. Since the discovery of periodic flux-closures in 2015 [9], a series of novel topological ferroelectric structures have been discovered and systematically studied, mostly in flux-closures and vortices [10-25]. To date, flux-closures in $PbTiO_3$/$SrTiO_3$ (PTO/STO) multilayers have been observed under a wide range of conditions. Known for their versatility, such flux-closures can appear at both insulating and conducting boundaries, exist in both multilayer and single-layer films, and can be modulated from both out-of-plane and in-plane ferroelectric topologies [9,26-28]. Previous

research suggests that flux-closures can form spontaneously as well as be artificially engineered, garnering considerable research interest. At present, the topological ferroelectric structures and physical properties have been investigated intensively, however, none of topological ferroelectric memory devices have been demonstrated. Main challenges include that: 1) the formation of topological structures is often constrained by their substrate, limiting the integration of ferroelectric topological structures into devices; 2) such nontrivial ferroelectric topological structures often coexist with their trivial structures, causing difficulties on achieving pure topological ferroelectric devices.

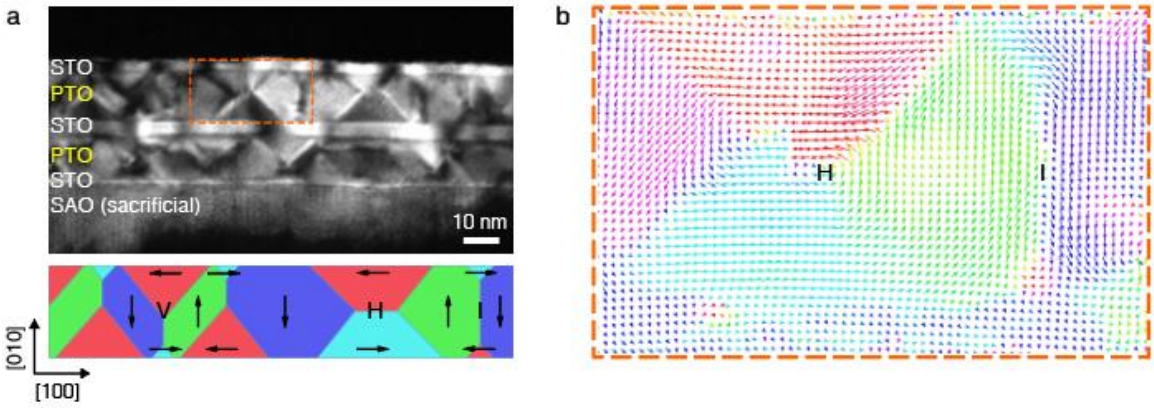

Fig. 5-2. (**a**) The cross-sectional DF image for SAO/(STO_7/PTO_{30})$_2$/STO_7 multilayer films grown on TSO $(110)_o$ substrates. The sacrificial SAO layer is dissolved in deionized water to release the top films. The top right inset shows the "V", "H" and "I" type flux-closures. The white arrows indicate the directions of P_s. (**b**) The P_s distribution map extracted from the red dashed box in (a).

In this work, we demonstrate, for the first time, scalable topological ferroelectric field-effect transistors (Fe-FETs) based on large-scale and pure flux-closure topological ferroelectric films. Topological ferroelectric STO/PTO/STO multilayers are epitaxially grown on substrates with sacrificial layers (water-soluble $Sr_3Al_2O_6$ (SAO) layer, Fig. S1, Materials and Methods). Such sacrificial layers are employed to aid the transfer of such films from their substrates [29-31].

After releasing a STO/PTO/STO multilayer from the substrate, we observe that pure flux-closure domains exist in the freestanding films without any *a*/*c* or a_1/a_2 phase impurities. By transfer of such STO/PTO/STO multilayers on top of monolayer MoS_2, a typical 2D semiconductor, we fabricated arrayed Fe-FETs which show excellent low-power characteristics of ferroelectric topological structures, including low leakage current, high remanent polarization, and long-term stability.

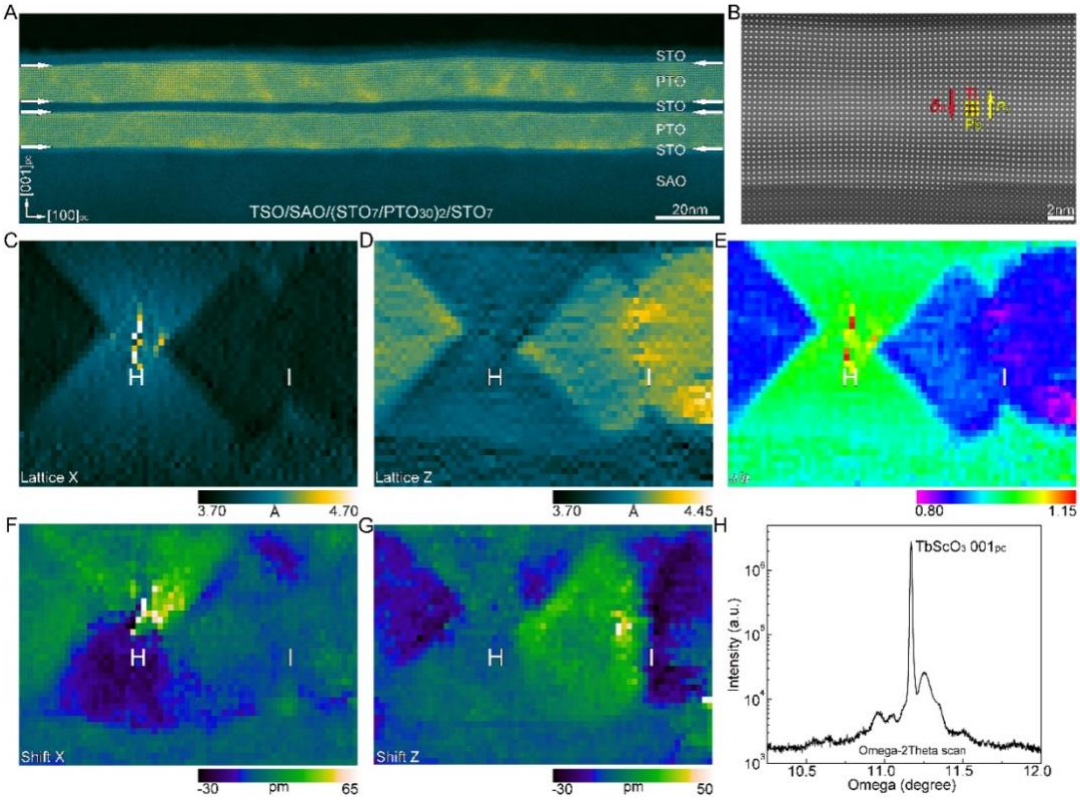

Fig. 5-3. Structural characterization of SAO/(STO$_7$/PTO$_{30}$)$_2$/STO$_7$ multilayer films. (**a**) Low-magnification HAADF-STEM image of the cross-sectional of SAO/(STO$_7$/PTO$_{30}$)$_2$/STO$_7$ multilayer films grown on TSO $(110)_o$ substrate. (**b**) Enlarged HAADF-STEM image showing "H" and "I" type flux-closure structures. The yellow and red circles denote the position of Pb^{2+} and Ti^{4+} columns, respectively. The red arrow denotes the direction of Ti-displacement (δ_{Ti}) vectors, which is the reversed spontaneous polarization direction (P_s). The polarization distribution map extracted based on (B) is located in main text fig. 1B. (**c**) In-plane lattice

spacing map (Lattice X). (**d**) Out-of-plane lattice spacing map (Lattice Z). (**e**) *c*/*a* map (Lattice Z / Lattice X). (**f**) In-plane ion displacement (Shift X). The in-plane component of ionic displacement. (**g**) Out-of-plane ion displacement (Shift Z). (**h**) High-resolution Omega-2Theta symmetric scans for the SAO/$(STO_7/PTO_{30})_2/STO_7$ multilayer films grown on TSO $(110)_o$ substrate.

5.2. Materials and Methods

5.2.1. Materials

We have grown a series of films under different thicknesses and strain conditions

$TSO/SAO/(STO_7/PTO_{30})_2/STO_7$

$TSO/SAO/STO_7/PTO_{30}/STO_7$

$DSO/SAO/PTO_{70}$

$TSO/SAO/STO_{14}/PTO_{30}$

$TSO/SAO/PTO_{44}$

Subscript indicates the number of unit cells. All sacrificial SAO layers have the chemical formula $Sr_3Al_2O_6$. The TEM, STEM and freestanding experiments were completed using $(STO_7/PTO_{30})_2/STO_7$ films deposited on TSO substrates. The 2-terminal capacitor and 3-terminal transistor experiments were completed using $STO_7/PTO_{30}/STO_7$ films deposited on TSO substrates. TSO and DSO substrates have an orthogonal structure, which can be analyzed as a pseudo-cubic structure. The PTO films directly grown on DSO substrates tend to form ferroelastic domains.

5.2.2. Methods

Multilayer films growth

The different films were deposited on multiple substrates by PLD, using the Coherent ComPex Pro 201 F KrF excimer laser with a wavelength of $\lambda = 248$ nm. A sintered ceramic SAO target with standard stoichiometric ratio was used for SAO layer deposition. A single crystal STO target was used for STO layer deposition. A sintered ceramic PTO target with standard stoichiometric ratio was used for PTO layer deposition. Prior to deposition, the SAO, STO and PTO targets were pre-sputtered for 3000 laser shots. The substrate was pre-heated to 850 °C to clean its surface, maintained at 850 °C for the growth of SAO, and then cooled down to 700 °C for the growth of STO and PTO. During deposition, the target-substrate distance was 40 mm, the environment was ultra-high vacuum for SAO growth, the oxygen pressure was 75 mTorr for STO and PTO growth, the laser energy was 300 mJ, and the repetition rate was 4 Hz. After deposition, these samples were annealed at 700 °C for 5 min and then cooled down to 200 °C with a cooling rate at 5 °C·min^{-1} in ultra-high vacuum. In this work, the growth of the multilayer films was carried out using the software's built-in program.

Fabrication of freestanding multilayer films

In the initial stage, PMMA was spin-coated onto the surface of the as-grown sample, such as TSO/SAO/(STO_7/PTO_{30})/STO_7/PMMA, and the sample was then placed on a heating stage and heated at 70 °C for 10 min to cure. After curing, the sample was immersed in deionized water until the SAO layer was completely dissolved, leaving the (STO_7/PTO_{30})/STO_7/PMMA film suspended on the surface of the deionized water. The suspended film was then carefully collected using a TEM grid and allowed to air dry. Finally, the PMMA was dissolved in acetone. In the meantime, to prepare cross-sectional samples, the suspended film was transferred onto a Si/SiO_2 wafer and allowed to air dry. The sample was then

immersed in acetone to remove PMMA on the surface. More details of the experimental process can be found in Fig. 5-1.

Synchrotron X-ray diffraction

The RSM experiments were conducted at the BL02U2 beamline of the Shanghai Synchrotron Radiation Facility, leveraging a Huber 6-circle diffractometer equipped with an Eiger 500K area detector, renowned for its exceptional precision. These highly accurate RSMs were employed to study the reciprocal superstructure satellite peaks in freestanding films. For clarity in presentation, we illustrate the reciprocal space plane from a front-view perspective. To explore the symmetry of the samples, the in-plane angles (Phi) were fixed at 0 and 90 degrees during data acquisition. Theta scans were performed near the $SrTiO_3$ [0 0 0.95] position, utilizing the Eiger area detector for image collection. This approach enabled the construction of a comprehensive reciprocal space distribution through data splicing and transformation. The conversion from real space to reciprocal space was carried out using a custom MATLAB code developed by our team. During the experiments, the incident light energy was approximately 10.405 kev, with the horizontal and vertical FWHM of the light spot measuring 160 × 80 micrometers. The sample dimensions were 10 × 10 mm, ensuring compatibility with the beamline's precision capabilities.

TEM sample preparation and experiments

The high-quality carbon (C) and tungsten (W) layers were deposited onto the surfaces of sample, capacitor, and transistor to prevent damage during focused ion beam (FIB) processing. In addition, the C and W layers also possess electrical conductivity to meet the requirements for imaging in FIB processing. Cross-sectional samples were prepared using the FIB technique with the ThermoFisher

Helios 5UX system. Thinning of the cross-sectional samples was conducted using a gallium ion beam operated at an accelerating voltage of 30 kV. As the sample thickness decreased, the beam current was progressively reduced from 0.44 nA to 0.26 nA and subsequently to 90 pA. This was followed by gentle milling with a gallium ion beam at an accelerating voltage of 5 kV and a beam current of 21 pA to mitigate the formation of a surface amorphous layer induced by ion implantation damage. DF and BF images of both cross-sectional and plan-view samples were acquired on a JEOL JEM-F200 TEM at 200 kV. SAED patterns were also collected from a flat area of the samples, which were transferred to holey carbon films. Atomic-resolved HAADF-STEM images and Super-EDS data were obtained on a double spherical aberration-corrected ThermoFisher Spectra 300 at 300 kV, equipped with a field emission gun.

In-situ study

In-situ experiment was carried out using a Tecnai G^2 F30 TEM. The real-time DF and BF TEM images were recorded using a double-tilt holder with heating function.

Peak finding

To distinguish between A-site (Pb and Sr) and B-site (Ti) atoms based on atomic column intensity in HAADF-STEM images, the whole image brightness and contrast were adjusted. The positions of atomic columns were accurately determined using 2D Gaussian fitting, performed with Matlab software [65,66]. The lattice spacing, c/a and Ti^{4+} shift (δ_{Ti}) were then calculated.

Large scale strain analysis by geometric phase analysis (GPA)

The GPA was carried out using the open-source software Strain++, which can be accessed at the website https://jjppeters.github.io/Strainpp/. Strain++ is maintained by J. J. P. Peters. The GPA is a highly effective method for assessing crystal lattice variations over large image areas, demonstrating significant potential for mapping strains. In addition, strain analysis and peak finding share similarities in terms of lattice rotation angles.

Piezoelectric force microscopy (PFM)

The hysteresis loops were measured using the Dual AC Resonance Tracking (DART) mode under ambient conditions at room temperature (Cypher, Asylum Research).

Film transfer for device

The $STO_7/PTO_{30}/STO_7$ film grown on 1 cm^2 substrate was cut to 25 mm^2 size. PMMA was first coated onto the $STO_7/PTO_{30}/STO_7$ film at 2000 r.p.m. (round / per minute) for 120 s. After soaking the sample in room-temperature pure water overnight, the $STO_7/PTO_{30}/STO_7$ film detached from the grown substrate. Next, target substrates, such as SiO_2 or a flexible substrate, were used to pick up the $STO_7/PTO_{30}/STO_7$ film. Acetone was then used to remove the PMMA after soaking for 3 hours. Finally, oxygen plasma at 100 W was applied to remove polymer residues from the $STO_7/PTO_{30}/STO_7$ film.

Au/STO_7/PTO_{30}/STO_7/Au capacitor fabrication

Metal-FE-Metal (MFM) structure devices (Au/$STO_7/PTO_{30}/STO_7$/Au capacitors) were fabricated for electrical behavior and macroscopic ferroelectricity measurement. UV lithography and electron beam evaporation were used to define the pattern and deposit the Au bottom electrode. Next, $STO_7/PTO_{30}/STO_7$ film was

transferred onto the Au bottom electrode via PMMA-assisted method. Au top electrodes were defined and deposited using the same process as the bottom electrode.

P-E loop measurement

P-E loop measurements of Au/STO_7/PTO_{30}/STO_7/Au capacitors were performed using TF Analyzer 3000. The standard bipolar voltage profile was employed, where the voltage was linearly increased from zero to the peak voltage V_{max}, then uniformly reduced to $-V_{max}$, and finally restored to zero. The measurement frequency was 10 kHz. The corresponding current-voltage curve was extracted from the P-E loop by dividing the change in polarization by the time intervals.

STO_7/PTO_{30}/STO_7/MoS_2 Fe-FETs fabrication

Firstly, Ti/Au gate metal was defined and deposited using UV lithography and electron beam evaporation. The STO_7/PTO_{30}/STO_7 film was then transferred on the Au gate metal as ferroelectric layer via the PMMA-assisted method. Next, CVD-grown MoS_2 was transferred onto the STO_7/PTO_{30}/STO_7 film using the same method described earlier [67-69]. To define the MoS_2 channel, oxygen plasma at 150 W was used to etch the redundant MoS_2 region. Finally, antimony (Sb) metal was employed as the contact metal in the Fe-FETs. Note that the vacuum was maintained at 10^{-7} torr during Sb metal deposition. M-F-S (Au/STO_7/PTO_{30}/STO_7/MoS_2) Fe-FETs were obtained.

Electrical measurement of STO_7/PTO_{30}/STO_7/MoS_2 Fe-FETs

All electrical measurements were performed at vacuum of 10^{-5} torr and at room temperature in a Lake Shore probe station using a Keysight B1530 semiconductor

analyzer system. A source measurement unit was used to measure the DC (direct current) I-V characteristics of all Fe-FETs.

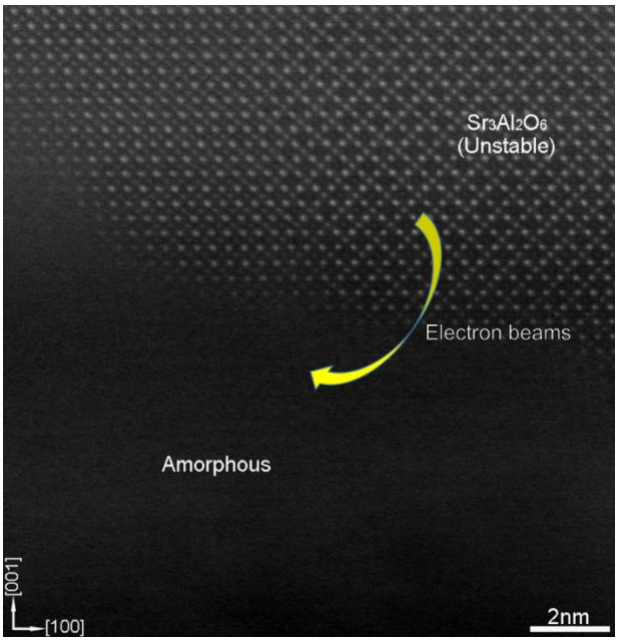

Fig. 5-4. $Sr_3Al_2O_6$ sacrificial layer. SAO is very sensitive to electron beam. Prior to image scanning, a section of the SAO region experienced a transition into an amorphous state.

6.3. Stable flux-closure in oxide multilayers epitaxially grown on SAO buffer layer

Fig. 5-2a shows a cross-sectional transmission electron microscopy (TEM) dark-field (DF) image of $(STO_7/PTO_{30})_2/STO_7$ multilayer films, providing an overview of the periodic array of flux-closures in two 12 nm PTO layers. The inset at the top-right corner of Fig. 5-2a presents a schematic illustration of the "V", "H", and "I" type flux-closure configurations. These flux-closure configurations coexist within the same PTO layer, driven by its coupling to the SAO layer with larger lattice constants. A low-magnification, high-resolution high-angle annular dark-field (HAADF) scanning TEM (STEM) image of multilayer films reveals uniform contrast in each PTO layer, indicating chemically homogeneous compositions (Fig. 5-3a), while slight contrast variations suggest the existence of domain walls.

Distinct wavy STO/PTO interfaces are observed in Fig. 5-3a, suggesting a significant disclination strain at presence. In Fig. 5-2b, the "H" and "I" type flux-closure patterns, characterized by closed head-to-tail P_s (dipole moments), are determined by reversed Ti displacement vectors relative to their nearest Pb atoms (Fig. 5-3b). At the core of the "H" type flux-closure, the lattice constant, c/a ration, and ionic displacement (δ_{Ti}) show significant increases, originating from the substantial disclination strain that disrupts the tetragonal structure at the flux-closure core (Fig. 5-3c-g**)**. Furthermore, the θ−2θ symmetric XRD patterns confirm that these multilayers exhibit good epitaxy quality, e.g., atomic scale flat surface (Fig. 5-3h). In addition, the SAO structure, which is easily dissolved in water, is highly susceptible to transformation from crystalline to amorphous under electron beam irradiation (**Fig. 5-4**).

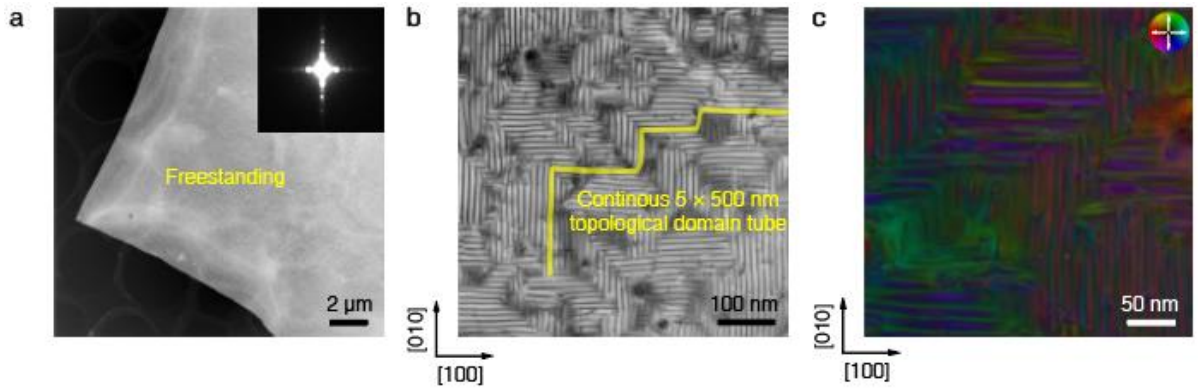

Fig. 5-5. (**a**) The low-magnification plan-view HAADF-STEM image of $(STO_7/PTO_{30})_2/STO_7$ films transferred to a holey carbon TEM grid. An enlarged single electron diffraction spot was inserted to the top right of the HAADF-STEM image. (**b**) Plan-view DF under-focus STEM imaging of freestanding $(STO_7/PTO_{30})_2/STO_7$ films showing the widespread occurrence of flux-closure along the [100] and [010] directions. (**c**) The DPC image showing the opposite electric field directions for the adjacent flux-closure tubes.

6.4. **Preserving single flux-closure ferroelectrics in freestanding films**

After removing the substrates to facilitate the device fabrications, it is challenging if such flux-closures persist in plan-view freestanding multilayer films. To address this issue, the multilayer films were transferred onto a holey carbon TEM grid after removing sacrificial SAO films. **Fig. 5-5**a and **Fig. 5-6**a show low-magnification HAADF-STEM image and bright-field (BF) image of the freestanding multilayer films, respectively. The inset in the top-right corner of Fig. 5-5a is a magnified image of a single diffraction spot from the selected area electron diffraction (SAED) pattern in Fig. 5-6b and c, confirming the presence of topological domains distributed along the [100] and [010] directions. The interference fringes in Fig. 5-6a reveal the freestanding multilayer film of undulation, as height variations are presented. Subsequently, under-focused HAADF-STEM images of the freestanding films (Fig. 5-5b), flux-closure tubes align along the [010] and [100] directions can be observed which is consistent with the information inferred from the satellite peaks of a single diffraction spot (Fig. 5-5a). Interestingly, the tubular flux-closures along the [100] direction and those along the [010] direction remain independent at the junction, indicating that the flux-closure possess rigid characteristics. Differential phase contrast (DPC) images further indicate that the electric field directions of adjacent flux-closure tubes are opposite (Fig. 5-5c). As the electric field direction is opposite to the polarization direction, this also demonstrates that the polarization directions of the periodic flux-closure array in the cross-sectional view alternate between clockwise and counterclockwise. Similarly, diffraction contrast analysis corroborates that the flux-closure tubes are aligned along the [100] and [010] directions (Fig. 5-6d-g). Atomic-resolution HAADF-STEM images clearly reveal the subtle tubular features of flux-closure (Fig. 5-6h). Notably, the flux-closure tubes are observed to be stable near sample edges or cracks without disappearing or undergoing structural evolution (Fig. 5-6i).

In previous studies, nontrivial flux-closure structures often coexist with trivial *a*/*c* and a_1/a_2 domains [10,15,25], and that the flux-closure arrays are typically constrained by the substrate, which significantly hinders their integration into devices. As shown above, the flux-closure arrays are stable in freestanding multilayer films. For devices fabrication, such multilayer films are required to be transferred to target substrates and a concern is that if the flux-closure arrays are still stable. **Fig. 5-7**a is an optical micrograph of transferred multilayer films on PMMA/PDMS. Surfaces of the transferred multilayer films are smooth with no obvious cracks. Note that, when the freestanding multilayer film was directly transferred onto PDMS without spin-coating a PMMA layer on its surface, cracks and wrinkles would appear (**Fig. 5-8**). Fig. 5-7b and c show synchrotron radiation reciprocal space maps (RSMs) of multilayer films supported by flexible PDMS. The flux-closure satellites and finite size oscillations along the out-of-plane direction (Q_z) suggest that the flux-closure arrays are coherent throughout the entire multilayer film thickness. A butterfly-shaped intensity modulation, reminiscent of classical *a*/*c* trivial domains with alternating in-plane and out-of-plane polarization, is observed [26]. Here, we clarify that the nontrivial flux-closure structure is also composed of a pair of *a* domains with horizontal polarization distribution and a pair of *c* domains with vertical polarization distribution. In terms of morphology, crystallographic orientation, reciprocal space, and functional properties, nontrivial flux-closure and trivial *a*/*c*, a_1/a_2 domains are completely different. In comparison with previous synchrotron radiation experimental results [10,15,25,26], the RSMs in Fig. 5-7b and c lack diffraction information from the substrate, single *a*/*c* and a_1/a_2 domains, and only display diffraction peaks from the exclusive flux-closure arrays. The findings reveal that the multilayer films on PMMA/PDMS exclusively comprise homogeneous flux-closure arrays.

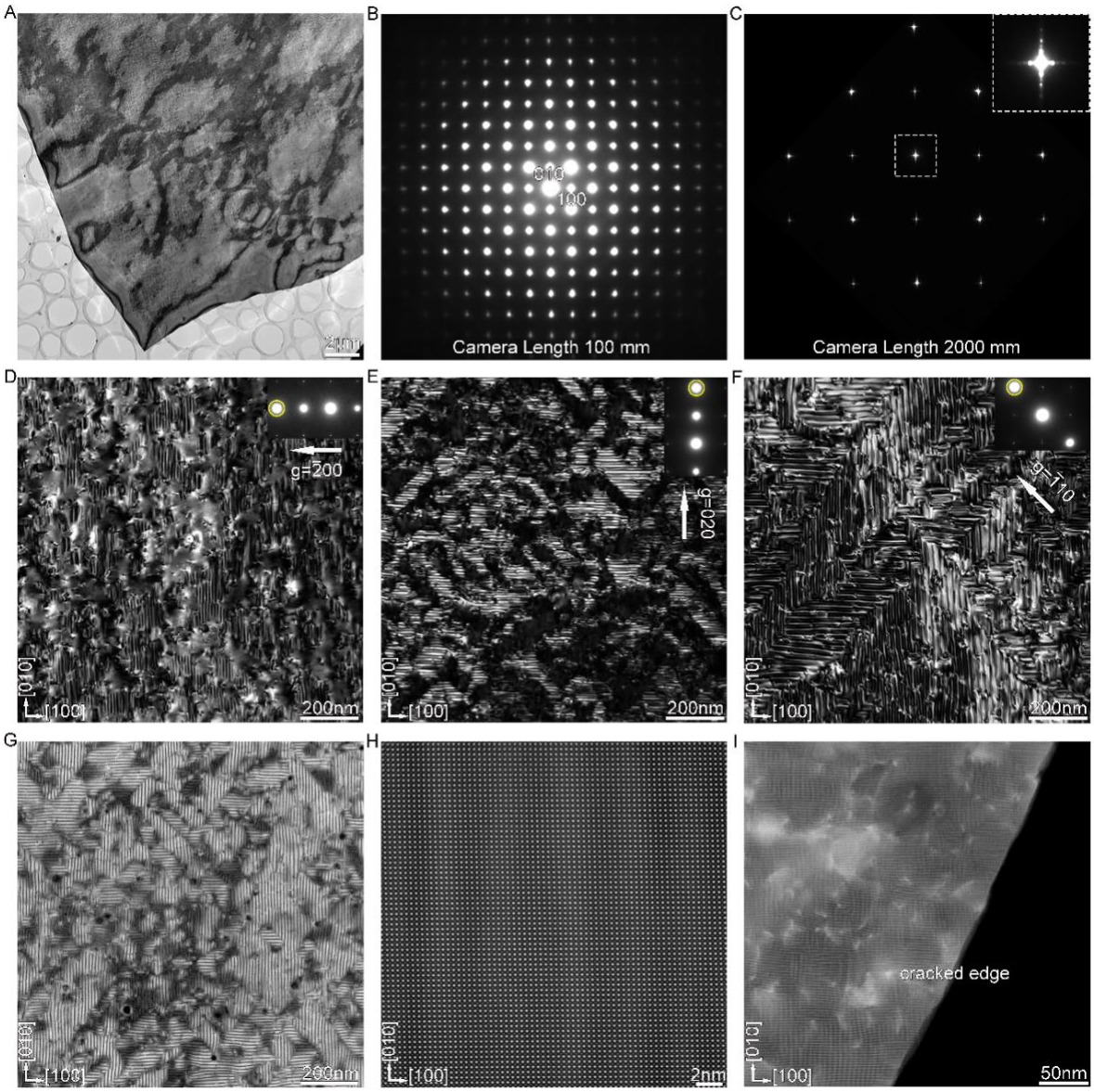

Fig. 5-6. Freestanding homogeneous flux-closure topological structures. (**a**) The low-magnification plan-view BF image of $(STO_7/PTO_{30})_2/STO_7$ films transferred to a holey carbon TEM grid. The interference fringes in (A) indicate that the freestanding film is in a fluctuating state. (**b**) SAED pattern of the freestanding multilayer films. It is note that when the camera length is small, the satellite diffraction spots formed by the topological structures are obscured. (**c**) A localized SAED pattern acquired with a camera length of 2000 mm. An enlarged single electron diffraction spot was inserted to the top right of the image (c) and fig. 1(c). (**d** to **f**) Diffraction contrast analysis of large-scale homogeneous flux-closure. Note that the DF images taken by g = $\bar{2}00$, g = 020, g = $\bar{1}10$, respectively. (**g**) Plan-view DF under-focus STEM imaging

of freestanding $(STO_7/PTO_{30})_2/STO_7$ films, showing the widespread occurrence of flux-closure along the [100] and [010] directions. (**h**) The atomic-resolved HAADF-STEM image revealing faint flux-closure contrast features. (**i**) The HAADF-STEM image of the cracked edge of the freestanding multilayer films.

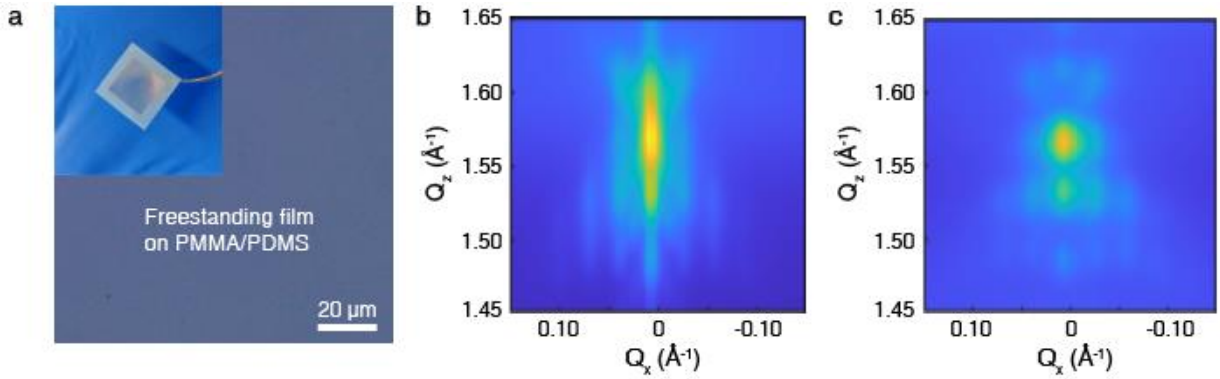

Fig. 5-7. (**a**) Optical microscopic image of the released multilayer films with the mechanical support of PDMS. The size of the released multilayer films in the illustration is 10 mm × 10 mm. (**b** and **c**) 001 RSM obtained before and after rotating the released multilayer films by 90°.

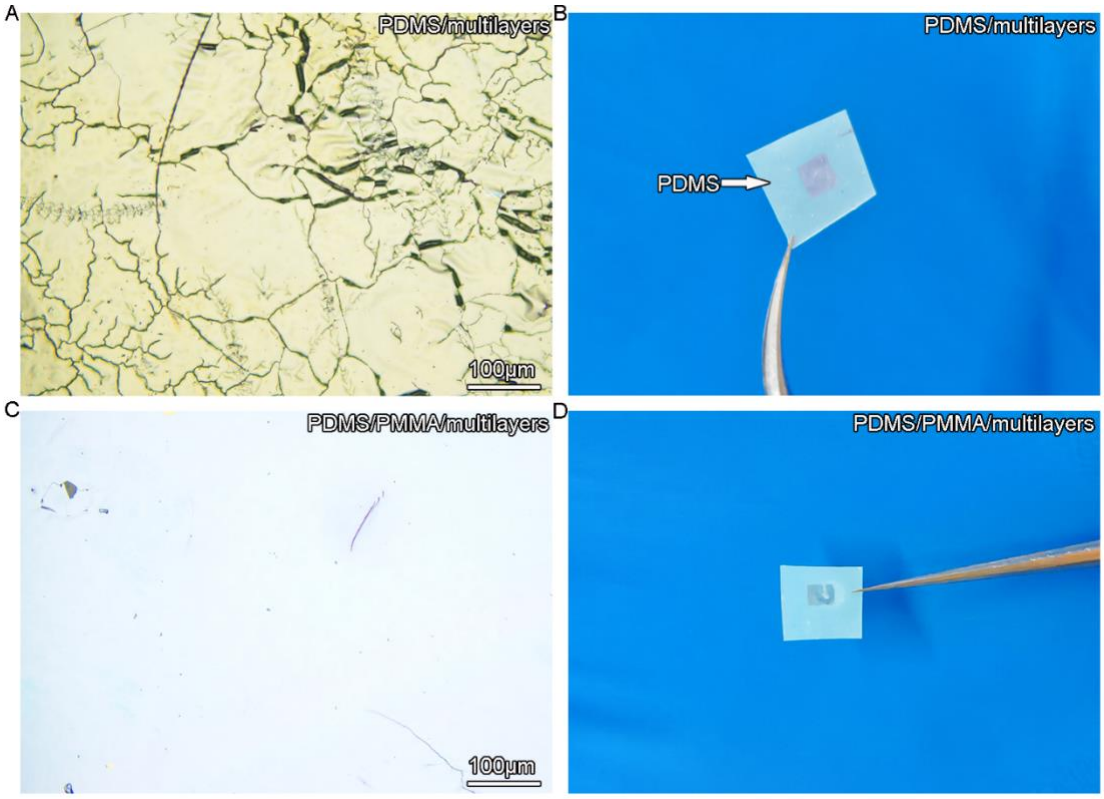

Fig. 5-8 Comparison of film quality transferred with and without PMMA. (**a** and **b**) Optical microscopic images of the released multilayer films with the mechanical support of PDMS. (**c** and **d**) Optical microscopic images of the released multilayer films with the mechanical support of PMMA/PDMS. Spin-coat a layer of PMMA, which is soluble in acetone, onto the prepared sample surface. Subsequently, cover the PMMA layer with PDMS. Immerse the resulting sample structure [TSO/SAO/$(STO_7/PTO_{30})_2$/STO_7/PMMA/PDMS] in deionized water for further processing. Therefore, we find that the quality of films transferred using PMMA is superior to those transferred without PMMA.

6.5. Abnormal topological phase transition path and strain-enhanced behavior

In order to evaluate the thermal stability of flux-closure structures, *in-situ* heating and cooling experiments are performed on these freestanding multilayer films. **Fig. 5-9**a and **Fig. 5-10** show a series of DF and BF images, respectively, illustrating the evolution behavior of freestanding flux-closures at various temperatures. The flux-closure structure remains stable even by heating from 298 to 623 K. At 673 K, some residual contrast of the flux-closure structure is still observable. As the temperature rises to 698 K, only faint remnants of the flux-closure structure are visible. Due to the significant lattice mismatch between SAO and STO, dislocations inevitably form during multilayer film growth. These dislocations persist in the freestanding multilayer film following transfer. These dislocations most likely play a pinning role in the transition of flux-closure structure, delaying its disappearance. At 723 K, the flux-closure morphology vanish completely in the freestanding multilayer films. During the cooling process, the flux-closure structure reappears, and the temperature-induced transition of the flux-closure structure is reversible. Previous studies on *in-situ* stimulation of the flux-closure structure (such as force, electric, electron beam, temperature etc.) suggest that the flux-closure structure first transitions into a/c or a_1/a_2 domains, and evolves

ultimately into a single-domain state under substrate constraints [25]. An important behavior is that, in freestanding multilayer films, the flux-closure structure does not transition into trivial domains as the temperature increases; instead, it directly disappears. This abnormal behavior represents a distinct sing phase transition pathway which is expected to be beneficial for data addressing.

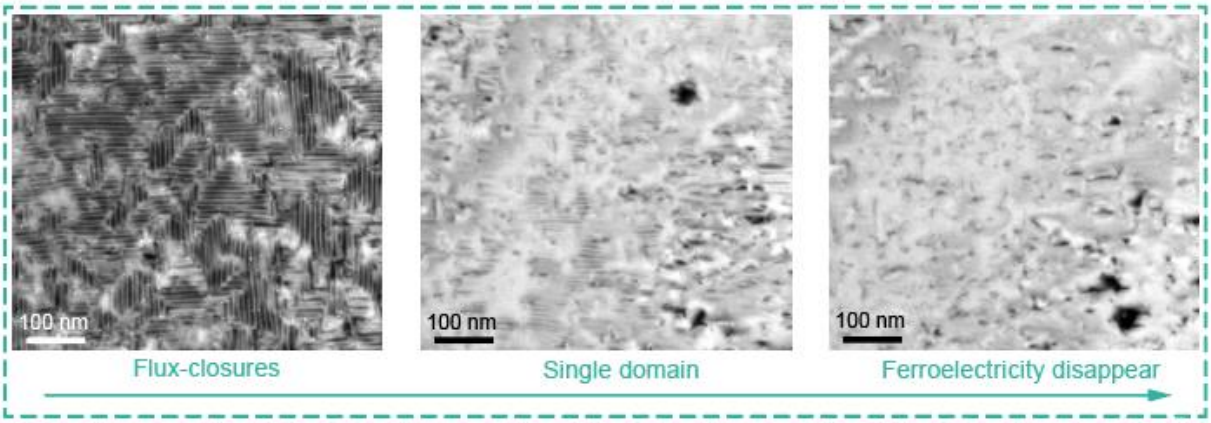

Fig. 5-9. Plan-view TEM images of flux-closure acquired in time series under different temperatures. With the increase of temperatures, flux-closure contrast gradually disappears.

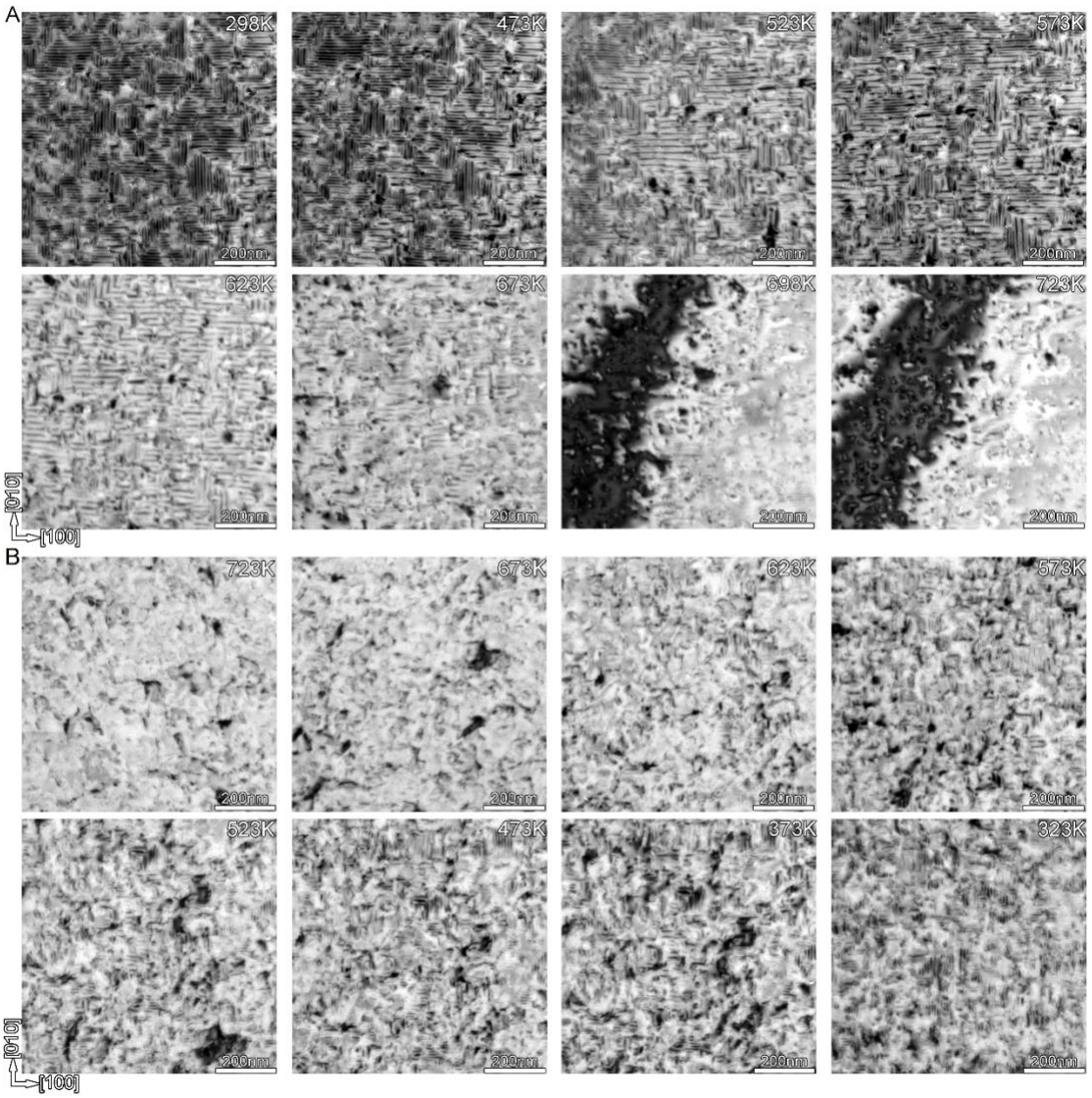

Fig. 5-10. Real-time reversible topological phase transitions of freestanding uniform flux-closure multilayer. (**a**) Chronological plan-view TEM image of freestanding flux-closure as the temperature gradually increases. When the temperature reaches 623 K, the flux-closure remains stable. However, at 673 K, subtle indications of flux-closure instability begin to emerge. (**b**) Chronological plan-view TEM image of freestanding flux-closure as the temperature gradually decreases. Here, it is necessary to clarify that during the heating or cooling process, freestanding films are highly susceptible to warping or fluctuations. This instability renders the initially tracked region unsuitable for flux-closure imaging, necessitating the relocation to alternative regions and the re-tilting of the sample to acquire images.

Fig. 5-11a is an optical micrograph of the multilayer film transferred onto Si/SiO_2, featuring flux-closure array. The optical micrograph demonstrates the high quality of multilayer films, with no cracks during the transfer process. The natural air-drying process effectively smooths out any fluctuations and undulations of STO/PTO multilayer films on the Si/SiO_2 surface. Fig. 5-11b shows the cross-sectional TEM BF image of $(STO_7/PTO_{30})_2/STO_7$ multilayer films on Si/SiO_2, providing an overview of the periodic array of "V" type flux-closures in PTO layers. Although the film experiences fluctuations during the transfer process, accompanied by changes in the state of strain, the flux-closure structure remains preserved without any transformation or evolution. Additionally, atomic-resolution X-ray energy dispersive spectroscopy (EDS) was conducted to analyze the elemental distribution in the multilayer films, as shown in Fig. 5-11c. The results reveal that both interfaces are sharp, with no evidence of inter-diffusion. Later, we compared the strain states of the "V" type flux-closure arrays in the initial growth samples [$TSO/SAO/(STO_7/PTO_{30})_2/STO_7$] and those transferred onto Si/SiO_2 [$Si/SiO_2/(STO_7/PTO_{30})_2/STO_7$] (**Fig. 5-12**). The strain of the "V" type flux-closure arrays in the multilayer film transferred to Si/SiO_2 shows a significant increase in terms of ε_{xx}, ε_{yy}, and ε_{xy}, which arises from the fluctuations of the freestanding multilayer film during the transfer process. Additionally, the large strain state suggests the presence of significant macroscopic polarization, which will be further confirmed in subsequent studies.

6.6. Characterization of the ferroelectric properties in transferred flux-closure films

Piezoresponse force microscopy (PFM) was used to confirm the ferroelectricity of the flux-closure in $STO_7/PTO_{30}/STO_7$ film after transfer onto Si/SiO_2 substrate (Materials and Methods). As shown in the amplitude-voltage butterfly loops and

phase-voltage hysteresis loops in **Fig. 5-13**, the freestanding flux-closure film exhibits obvious polarization reversal properties under an external electrical field, demonstrating strong ferroelectricity on Si/SiO_2. Compared to the PTO film grown on the $DyScO_3$ (DSO) substrates, the freestanding flux-closure film shows a higher piezoelectric response and a smaller coercive voltage of 8 V.

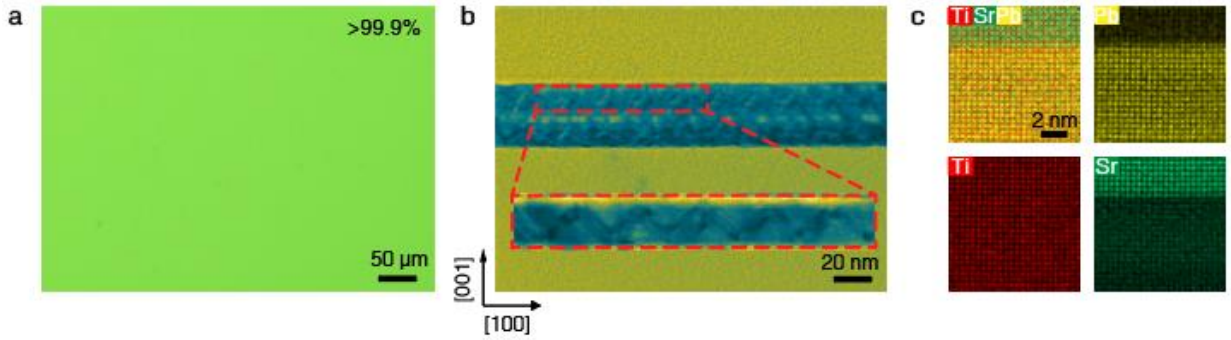

Fig. 5-11. (**a**) Optical microscopic image of the transferred multilayer films onto Si/SiO_2. (**b**) Cross-sectional BF image for $(STO_7/PTO_{30})_2/STO_7$ multilayered films integrated onto Si/SiO_2 wafer. The red dashed box is enlarged to show the "V" type flux-closure patterns. Multiple interfaces are marked by white arrows. (**c**) Atomic-resolved super-EDS mapping showing the sharp interfaces of PTO/STO.

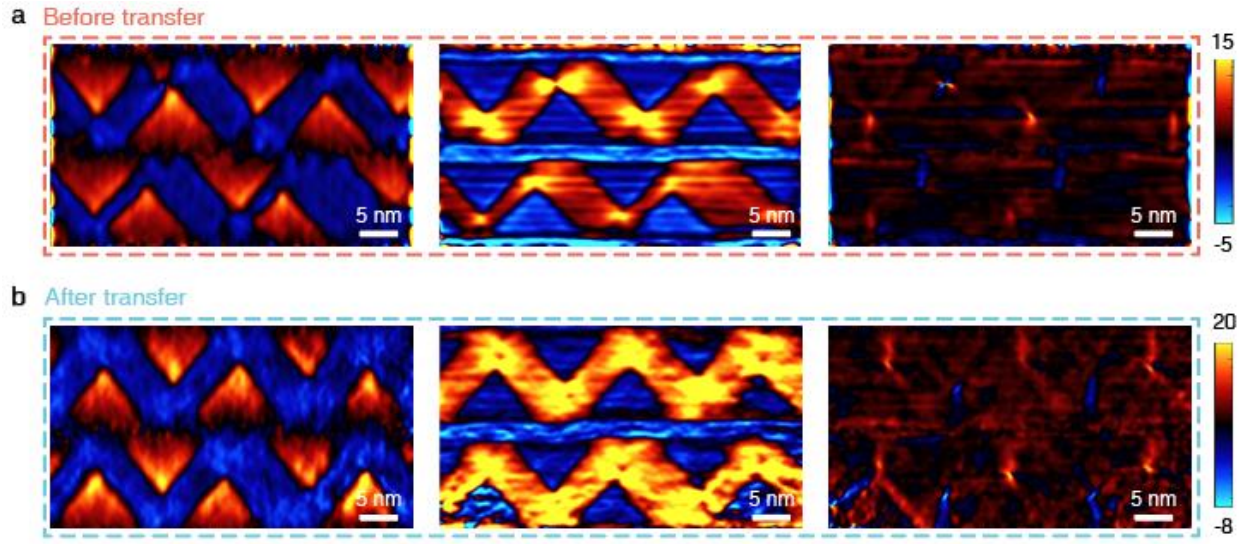

Fig. 5-12. GPA and comparison of uniform flux-closure before (**a**) and after (**b**) transfer (In-plane strain, ε_{xx}; out-of-plane strain, ε_{yy}; shear strain, ε_{xy}). Note the very inhomogeneous distribution of the strains.

A metal-ferroelectric-metal (MFM) capacitor structure was also fabricated to measure the electrical behavior and macroscopic ferroelectricity, where STO/PTO/STO film serving as ferroelectric layer and gold (Au) metal acting as both the bottom and top electrodes (**Fig. 5-14**a). Here, a crossbar array architecture is designed to increase the devices density for applications such as ferroelectric random-access memory and ferroelectric tunnel junction (**Fig. 5-15**). Fig. 5-14b and c show the cross-sectional HAADF-STEM and DPC images of Au/STO/PTO/STO/Au capacitors, respectively. The atomic-resolution DPC image (Fig. 5-14C) and geometric phase analysis (GPA) maps confirm the existence of topological flux-closure in the fabricated capacitors. Note that the high-temperature electrode deposition process is less harmful to the flux-closure structure and the homogenous flux-closure structure can stably exist within the capacitor array.

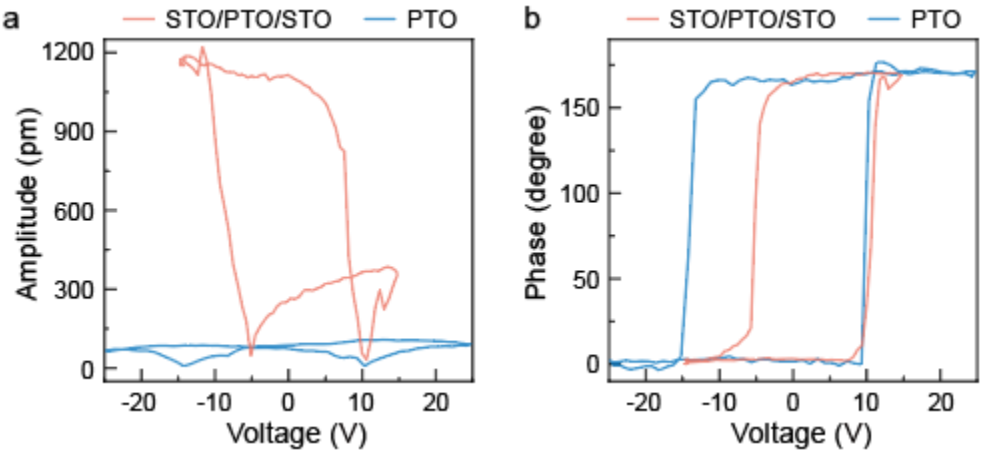

Fig. 5-13. PFM amplitude-voltage butterfly loop (**a**) and phase-voltage hysteresis loop of different films (**b**). For example, for (DSO)Si/SiO_2/PTO sample, the SAO/PTO film was initially

grown on an DSO substrate (cyan line). Characterization of loop behaviour after all the films were integrated onto Si/SiO_2.

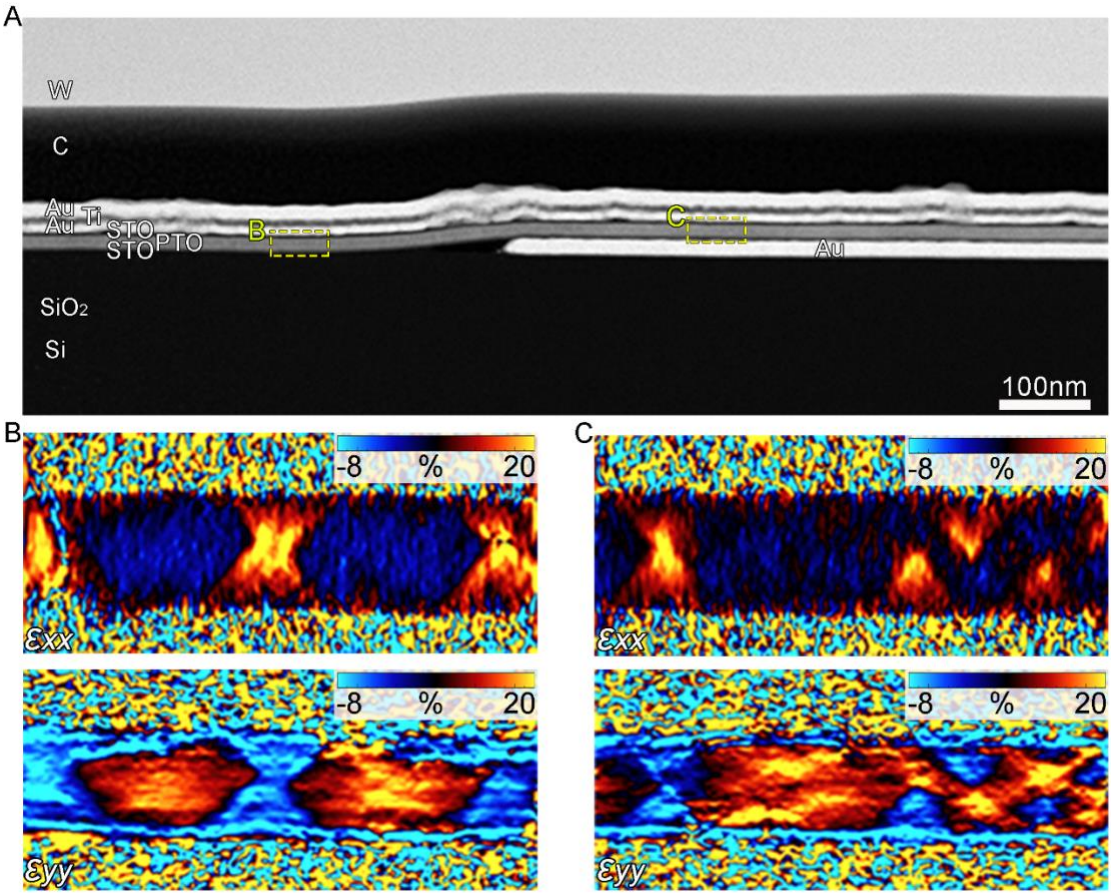

Fig. 5-14 The device structure diagram of 2-terminal capacitor. (**a**) The cross-sectional HAADF-STEM image for the $Au/STO_7/PTO_{30}/STO_7/(Au/Ti/Au)$ capacitor integrated onto Si/SiO_2. The C and W layers on the surface were deposited during the FIB sample preparation process to protect the film from damage caused by ion and electron beams. (**b** and **c**) GPA of $STO_7/PTO_{30}/STO_7$ films from the yellow dashed line box area in (a).

Based on the fabricated ferroelectric capacitor arrays, we further conducted electrical performance tests for leakage currents, polarization, fatigue characteristics, and other related properties. As shown in **Fig. 5-16**a, STO/PTO/STO film exhibits a high breakdown field of 11 MV/cm, while pure PTO and PTO/STO films show significantly lower breakdown fields, despite all

three films having a thickness of 16 nm. Hence, the robust electrical behavior could be attributed to the intrinsic topological flux-closure domain. Endurance measurements shown in **Fig. 5-17** also reveal negligible leakage current under bias voltage for a long time. A typical P-E loop curve is shown in Fig. 5-16b, where the P_r is ~ 195 μC/cm^2 and the polarized voltage is ~ 2 V, outperforming all other reported perovskites type ferroelectric films previously investigated (Fig. 5-16c). Despite the high Pr of 236 μC/cm^2 in the PTO and PbO mixed films with a thickness of 129 nm [32-37], our STO/PTO/STO film, which is only 16 nm thick and contains only the topological flux-closure structure, exhibits a significant increase in strain after being transferred as a freestanding film (Fig.5-16b and c). This means that the flux-closure structure will display a large P_r. Furthermore, it is noteworthy that the thickness of the STO layer in the STO/PTO/STO film is approximately 7 u.c.. Although STO serves as a dielectric layer, the large disclination strain and polarization effects in the PTO typically will penetrate through the STO layer, causing noticeable ion displacement in the STO layer, indicating the presence of ferroelectric characteristics. Endurance and device-to-device variations confirm their stability and uniformity (Fig. 5-16d and e), making them suitable for large-scale applications. In Fig. 5-16f we summarize and compare the performance of our flux-closure films with others in terms of P_r and E_c [38-51], and it is clear that our films exhibit the best overall performances.

6.7. **Fabrication of STO/PTO/STO/MoS_2 Fe-FET arrays**

Based on the abnormal direct phase transition path, homogenous flux-closure domains and robust ferroelectric properties, metal-ferroelectric-semiconductor-metal FETs (MFSFETs) were fabricated to explore the applicability of uniform topological flux-closure ferroelectric films in the advanced memory technology. Here, STO/PTO/STO films and two-dimensional (2D) monolayer MoS_2 films

serve as the ferroelectric layers and channel layers, respectively (**Fig. 5-18**a). The detailed fabrication process is illustrated in Fig. 5-1f-m. Optical images (Fig. 5-18a, **Fig. 5-19** and **Fig. 5-20**) show the as-fabricated large-scale Fe-FET arrays.

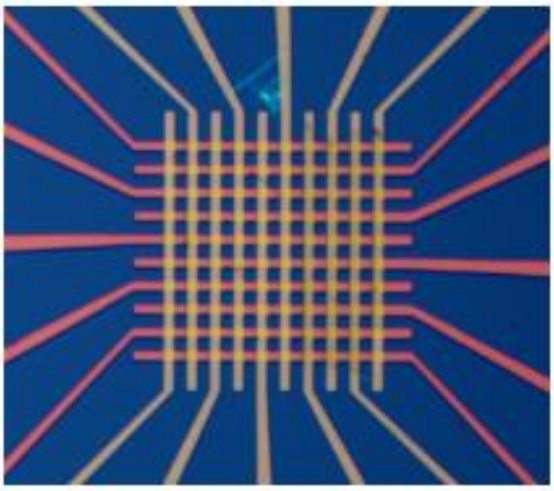

Fig. 5-15. Optical image of the Au/STO_7/PTO_{30}/STO_7/Au capacitor

Cross-sectional HAADF-STEM images confirmed the preservation of the topological flux-closure domains in the Fe-FET (**Fig. 5-21**). In Fig. 5-18b, transfer curve of Fe-FETs with STO/PTO/STO films exhibited a significant anticlockwise hysteresis, contrasting with the hysteresis-free behavior of HfO_2/MoS_2 FETs, which is typical characteristic of Fe-FETs. As shown in Fig. 5-18c, the linear output curve also validated the effective Sb metal contact with MoS_2. Under higher drain voltages, a negative differential conductance phenomenon is observed, indicating the ferroelectric properties in STO/PTO/STO/MoS_2 devices (**Fig. 5-22**). The STO/PTO/STO/MoS_2 Fe-FETs demonstrate exceptional memory performances, with a high on/off ratio of 10^8 and a wide memory window of 7 V with an ultrathin 16 nm STO/PTO/STO film (0.43 V/nm). Besides, negligible leakage current provided precondition for the stable operation of these STO/PTO/STO/MoS_2 Fe-FETs, as shown in **Fig. 5-23**a and b.

A comprehensive evaluation of all transistor arrays are shown in Fig. **5-24**a in which 150 devices are included for statistical analysis. As shown in Fig. 5-24b, these devices show narrow variations in threshold voltages (V_{th}), memory windows (MW) and on/off ratios, superior much when compared to other 2D Fe-FETs [52-64]. The normalized memory window and on/off ratios of different material systems are summarized in **Fig. 5-25** [52-64]. We can see that our Fe-FETs with a flux-closure structure exhibit excellent memory windows and large switching ratios. Compared to other material systems, Fe-FETs with a flux-closure structure show advantages in information memory applications. Finally, we have also completed the integration of flexible Fe-FETs with flux-closure multilayer films, expanding the application scenarios of freestanding multilayer films (**Fig. 5-26**). Our device demonstrations suggest a bright future of scalable ferroelectric memory with topological ferroelectric STO/PTO/STO films.

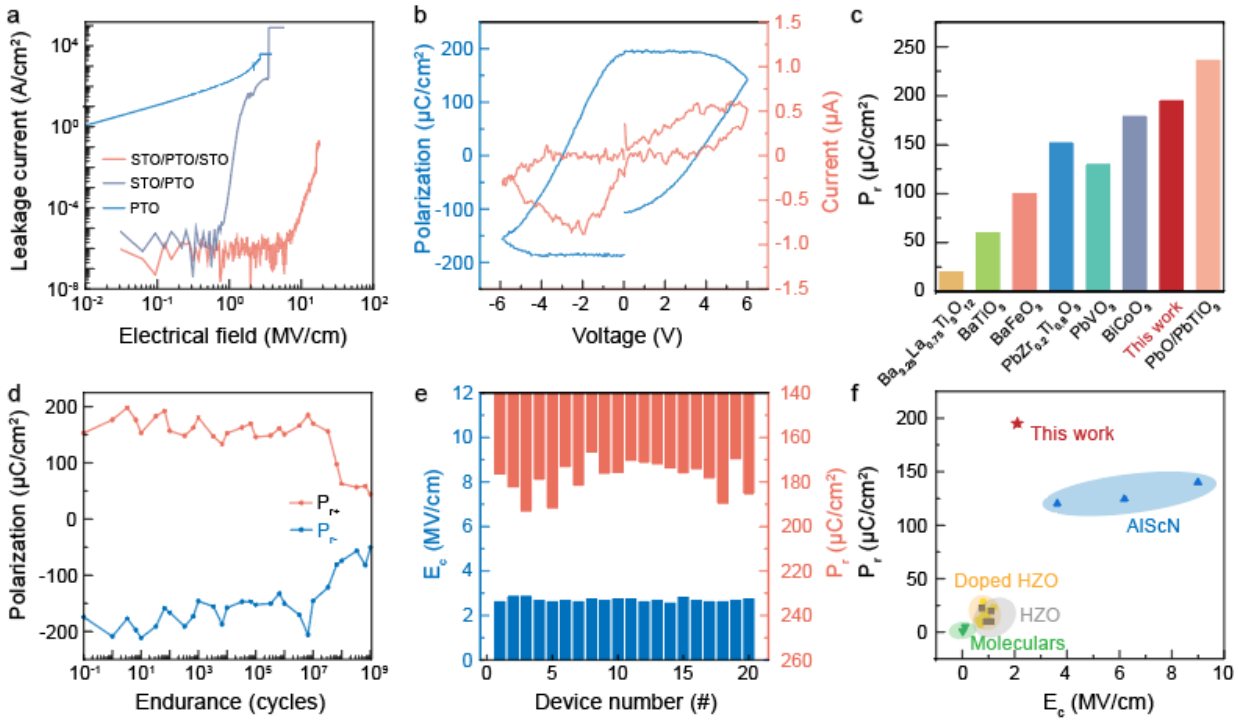

Fig. 5-16. (**a**) Leakage current and breakdown field for Au/STO_7/PTO_{30}/STO_7/Au capacitor, Au/STO_{14}/PTO_{30}/Au capacitor and Au/PTO_{44}/Au capacitor. (**b**) P-E curves of the

Au/STO_7/PTO_{30}/STO_7/Au capacitor with PUND measurements. (**c**) Comparison of single polarization of the present flux-closure capacitor with the previously experimentally measured P_r in films, from left to right: $Bi_{3.25}La_{0.75}Ti_3O_{12}$ [32], $BaTiO_3$ [33], $BiFeO_3$ [34], $PbZr_{0.2}Ti_{0.8}O_3$ [35], $PbVO_3$ [36], $BiCoO_3$ [36], $PbTiO_3$ and PbO [37]. (**d**) Endurance properties of the Au/STO_7/PTO_{30}/STO_7/Au capacitor. (**e**) Device-to-device variation of E_c and P_r for 20 devices. (**f**) Benchmark of E_c and P_r comparing with other ferroelectric film. AlScN [38-40], moleculars [41-42], HZO [43-46], Doped HZO [45,47-51].

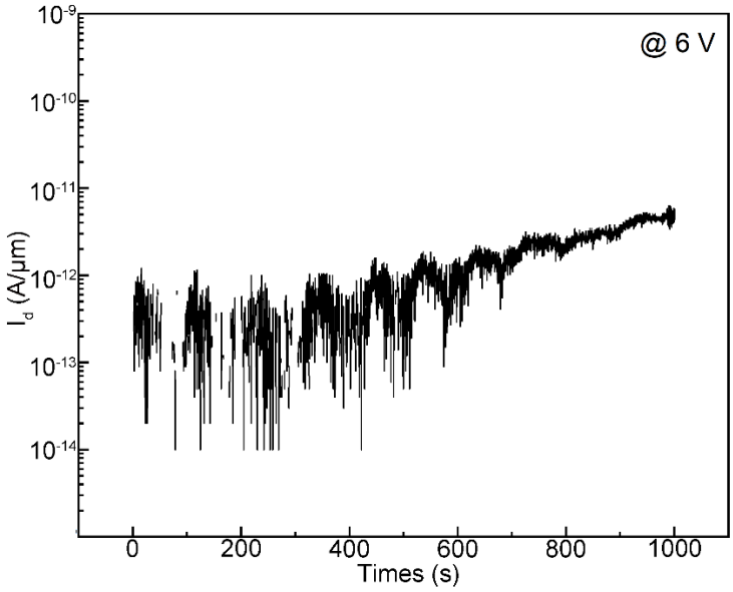

Fig. 5-17. Endurance measurement of leakage current when applying 6 V bias.

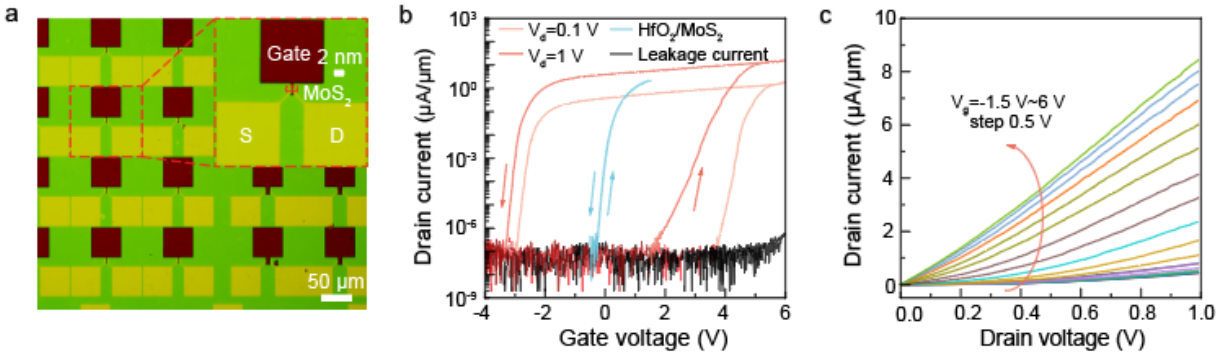

Fig. 5-18. (**a**) Optical images of Fe-FETs with MoS_2 as channel and STO_7/PTO_{30}/STO_7 as ferroelectric layer. Transfer **(b)** and output (**c**) curves of the STO_7/PTO_{30}/STO_7/MoS_2 Fe-FETs.

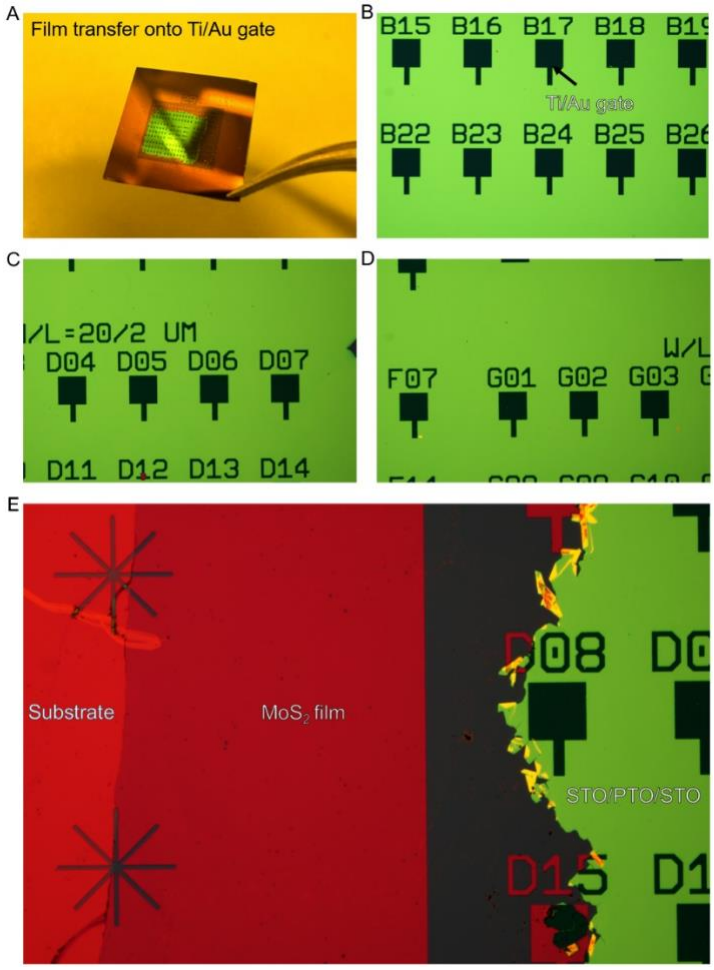

Fig. 5-19 Optical images in the Fe-FET fabrication process. (**s** to **f**) Photos and optical images of $STO_7/PTO_{30}/STO_7$ film transferred onto Ti/Au gate. (**e**) Optical image of $STO_7/PTO_{30}/STO_7$ film/MoS_2 on Ti/Au gate.

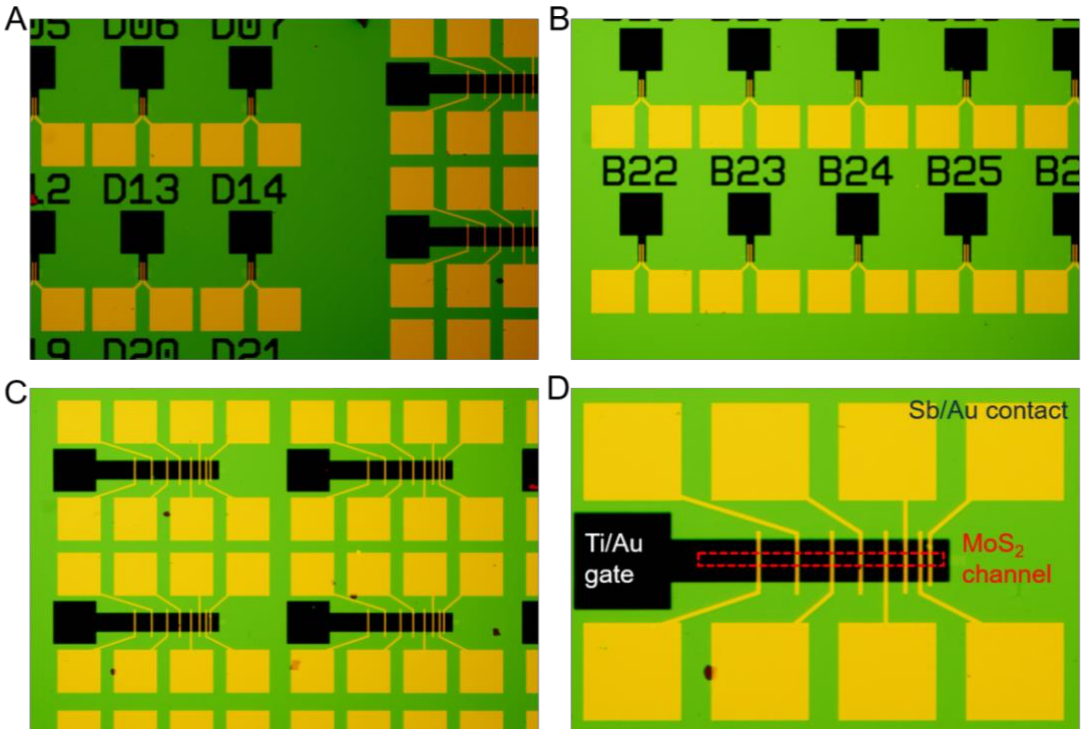

Fig. 5-20. Optical images of $STO_7/PTO_{30}/STO_7/MoS_2$ Fe-FETs.

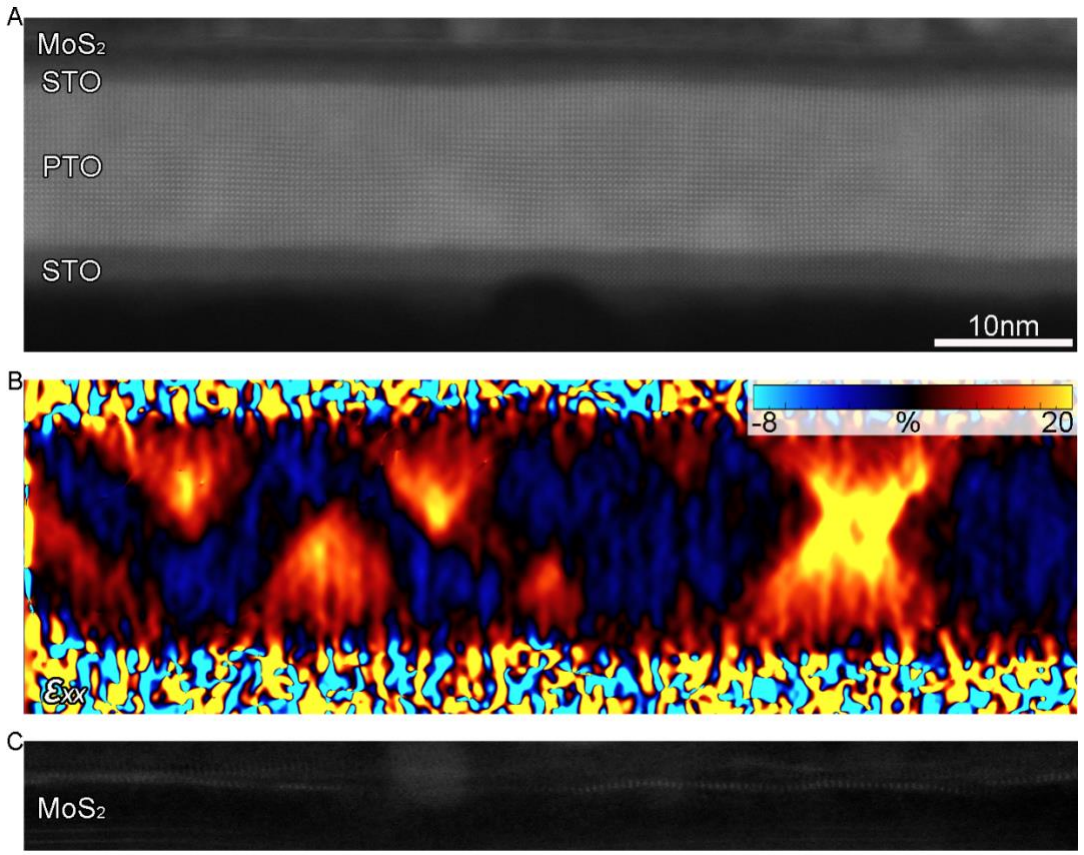

Fig. 5-21. The localized device structure diagram of Fe-FETs. (**a**) The cross-sectional HAADF-STEM image for the $STO_7/PTO_{30}/STO_7/MoS_2$ 3-terminal transistor integrated onto Si/SiO_2. (**b**) GPA of $STO_7/PTO_{30}/STO_7$ films from the (a). (**c**) The atomic-resolved HAADF-STEM image of MoS_2 layer.

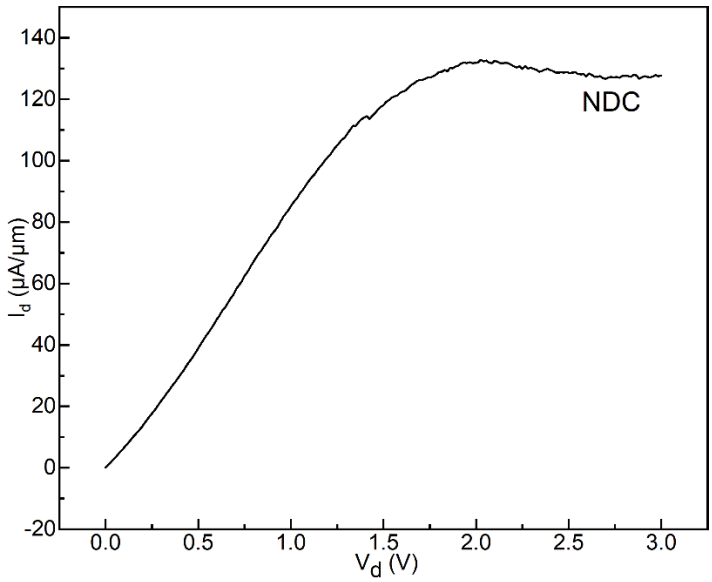

Fig. 5-22. Negative differential conductance phenomenon in $STO_7/PTO_{30}/STO_7/MoS_2$ Fe-FETs.

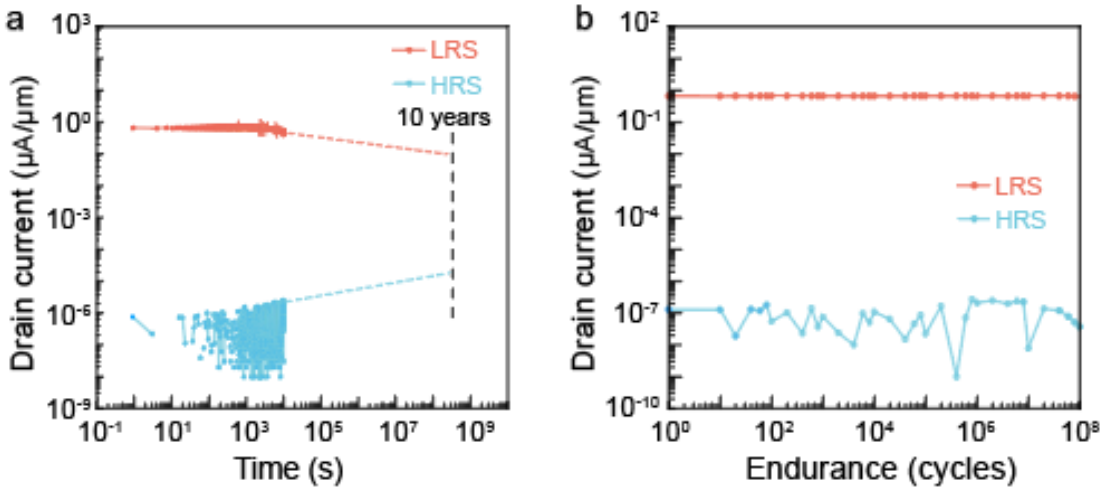

Fig. 5-23. Retention (**a**) and endurance (**b**) of $STO_7/PTO_{30}/STO_7/MoS_2$ Fe-FETs

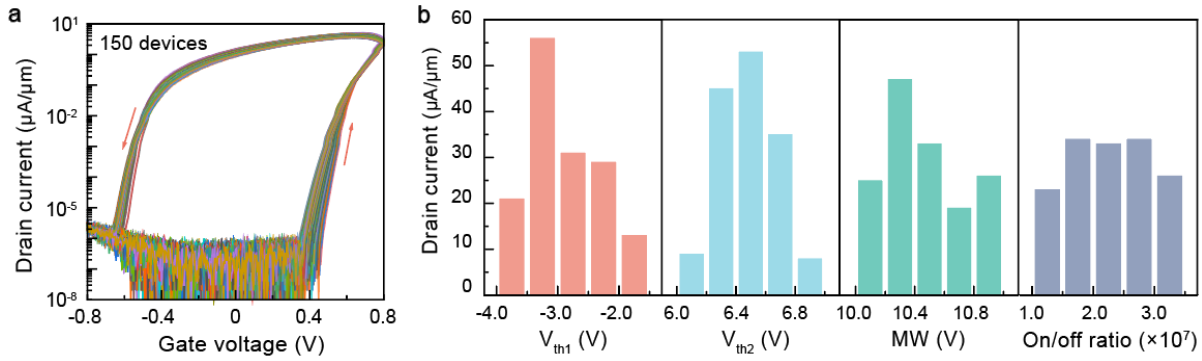

Fig. 5-24. (**a**) Statistics for 150 $STO_7/PTO_{30}/STO_7/MoS_2$ Fe-FETs devices. (**b**) Threshold voltages distribution, memory windows and on/off ratio distribution from (a).

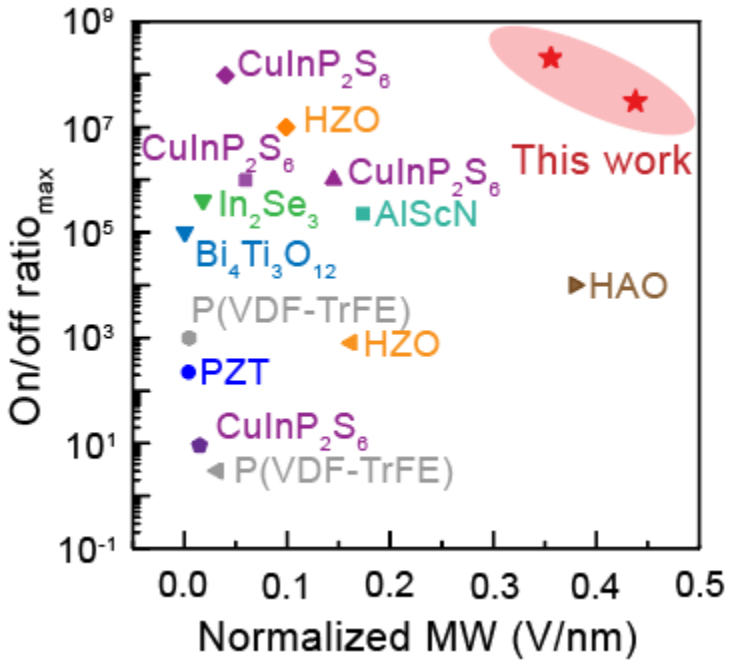

Fig. 5-25. Benchmark of normalized memory windows and on/off ratio compared with other Fe-FETs. HAO [52], HZO [53,54], AlScN [55], $CuInP_2S_6$ [56-59], In_2Se_2 [60], $Bi_4Ti_3O_{12}$ [61], PZT [62], P(VDF-TrFE) [63,64].

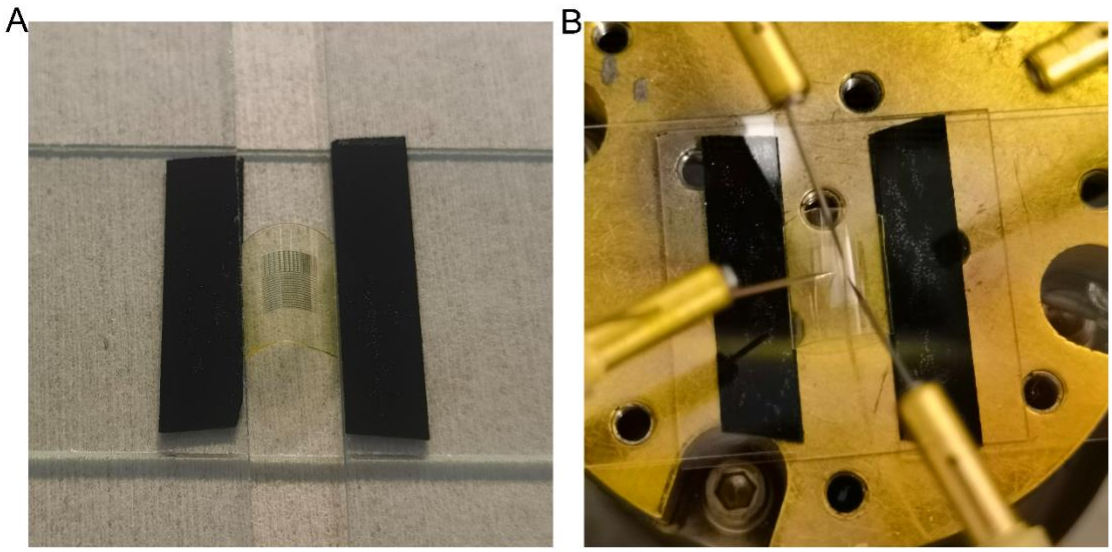

Fig. 5-26. Photos of flexible $STO_7/PTO_{30}/STO_7/MoS_2$ Fe-FETs.

6.8. **Conclusions**

Large-scale homogenous STO/PTO/STO topological flux-closures are epitaxially grown on sacrificial SAO layers. In freestanding multilayer films, a single rigid flux-closure structure exists, contrary to the previously believed coexistence of flux-closure structures and ferroelastic domains. These flux-closure structures in freestanding films, equivalently distributed along the [100] and [010] directions, exhibit a simple transformation pathway from topologically nontrivial to single domain. Moreover, we fabricated large-scale topological ferroelectric transistor arrays, inheriting the excellent stability and low power characteristics of ferroelectric topological structures. The flux-closure array capacitors demonstrate exceptional performance, with no detectable leakage current below 10 V, a remanent polarization (P_r) reaching 195 μC/cm^2, and a cycle endurance of up to 10^9 at 1 MHz. Notably, the E_c/E_b (coercive field/breakdown field) is as low as 0.15. The CMOS-compatible Fe-FETs show a large memory window of ~ 0.43 V/nm, high on/off ratio of 10^8, stable retention for up to 10 years, superior uniformity and flexible applications. This work moves a significant step towards the ultimate

ambition of realizing ferroelectric devices in future semiconductor industries and flexible electronic products.

6.9. **References**

1. Datta, Suman, Wriddhi Chakraborty, and Marko Radosavljevic. "Toward attojoule switching energy in logic transistors." *Science* 378.6621 (2022): 733-740.
2. Everschor-Sitte, Karin, et al. "Topological magnetic and ferroelectric systems for reservoir computing." *Nature Reviews Physics* 6.7 (2024): 455-462.
3. Meier, Dennis, and Sverre M. Selbach. "Ferroelectric domain walls for nanotechnology." *Nature Reviews Materials* 7.3 (2022): 157-173.
4. International Roadmap for Devices and Systems (IRDS™) 2023, Beyond CMOS & Emerging Materials Integration (ieee.org). https://irds.ieee.org/editions/2023
5. Schroeder, Uwe, et al. "The fundamentals and applications of ferroelectric HfO." *Nature Reviews Materials* 7.8 (2022): 653-669.
6. Martin, Lane W., and Andrew M. Rappe. "Thin-film ferroelectric materials and their applications." *Nature Reviews Materials* 2.2 (2016): 1-14.
7. Cao, Wei, et al. "The future transistors." *Nature* 620.7974 (2023): 501-515.
8. Kum, Hyun S., et al. "Heterogeneous integration of single-crystalline complex-oxide membranes." *Nature* 578.7793 (2020): 75-81.
9. Tang, Y. L., et al. "Observation of a periodic array of flux-closure quadrants in strained ferroelectric $PbTiO_3$ films." *Science* 348.6234 (2015): 547-551.
10. Damodaran, Anoop R., et al. "Phase coexistence and electric-field control of toroidal order in oxide superlattices." *Nature Materials* 16.10 (2017): 1003-1009.

11. Guo, Mengfan, et al. "Toroidal polar topology in strained ferroelectric polymer." *Science* 371.6533 (2021): 1050-1056.
12. Li, Qian, et al. "Subterahertz collective dynamics of polar vortices." *Nature* 592.7854 (2021): 376-380.
13. Yadav, Ajay K., et al. "Spatially resolved steady-state negative capacitance." *Nature* 565.7740 (2019): 468-471.
14. Rusu, Dorin, et al. "Ferroelectric incommensurate spin crystals." *Nature* 602.7896 (2022): 240-244.
15. Stoica, Vladimir A., et al. "Non-equilibrium pathways to emergent polar supertextures." *Nature Materials* 23.10 (2024): 1394-1401.
16. Sánchez-Santolino, Gabriel, et al. "A 2D ferroelectric vortex pattern in twisted $BaTiO_3$ freestanding layers." *Nature* 626.7999 (2024): 529-534.
17. Wang, Y. J., et al. "Polar meron lattice in strained oxide ferroelectrics." *Nature Materials* 19.8 (2020): 881-886.
18. Li, Zhongwen, et al. "High-density array of ferroelectric nanodots with robust and reversibly switchable topological domain states." *Science Advances* 3.8 (2017): e1700919.
19. Das, S., et al. "Observation of room-temperature polar skyrmions." *Nature* 568.7752 (2019): 368-372.
20. Govinden, Vivasha, et al. "Ferroelectric solitons crafted in epitaxial bismuth ferrite superlattices." *Nature Communications* 14.1 (2023): 4178.
21. Han, Lu, et al. "High-density switchable skyrmion-like polar nanodomains integrated on silicon." *Nature* 603.7899 (2022): 63-67.
22. Shang, Hongxing, et al. "Mechanical control of polar patterns in wrinkled thin films via flexoelectricity." *Physical Review Letters* 132.11 (2024): 116201.

23. Xu, Tao, et al. "Mechanical Rippling for Diverse Ferroelectric Topologies in Otherwise Nonferroelectric $SrTiO_3$ Nanofilms." *Physical Review Letters* 132.8 (2024): 086801.
24. Nahas, Y., et al. "Inverse transition of labyrinthine domain patterns in ferroelectric thin films." *Nature* 577.7788 (2020): 47-51.
25. Li, Xiaomei, et al. "Atomic-scale observations of electrical and mechanical manipulation of topological polar flux closure." *Proceedings of the National Academy of Sciences* 117.32 (2020): 18954-18961.
26. Hadjimichael, Marios, et al. "Metal–ferroelectric supercrystals with periodically curved metallic layers." *Nature Materials* 20.4 (2021): 495-502.
27. Gradauskaite, Elzbieta, et al. "Defeating depolarizing fields with artificial flux closure in ultrathin ferroelectrics." *Nature Materials* 22.12 (2023): 1492-1498.
28. Checa, Marti, et al. "On-demand nanoengineering of in-plane ferroelectric topologies." *Nature Nanotechnology* 20.1 (2025): 43-50.
29. Zhang, Jinfeng, et al. "Super-tetragonal $Sr_4Al_2O_7$ as a sacrificial layer for high-integrity freestanding oxide membranes." *Science* 383.6681 (2024): 388-394.
30. Dong, Guohua, et al. "Super-elastic ferroelectric single-crystal membrane with continuous electric dipole rotation." *Science* 366.6464 (2019): 475-479.
31. Ji, Dianxiang, et al. "Freestanding crystalline oxide perovskites down to the monolayer limit." *Nature* 570.7759 (2019): 87-90.
32. Park, B. H., et al. "Lanthanum-substituted bismuth titanate for use in non-volatile memories." *Nature* 401.6754 (1999): 682-684.
33. Choi, Kyoung Jin, et al. "Enhancement of ferroelectricity in strained $BaTiO_3$ thin films." *Science* 306.5698 (2004): 1005-1009.
34. Zhang, J. X., et al. "Microscopic origin of the giant ferroelectric polarization in tetragonal-like $BiFeO_3$." *Physical review letters* 107.14 (2011): 147602.

35. Nagarajan, V., et al. "Dynamics of ferroelastic domains in ferroelectric thin films." *Nature materials* 2.1 (2003): 43-47.
36. Uratani, Yoshitaka, et al. "First-principles predictions of giant electric polarization." *Japanese journal of applied physics* 44.9S (2005): 7130.
37. Zhang, Linxing, et al. "Giant polarization in super-tetragonal thin films through interphase strain." *Science* 361.6401 (2018): 494-497.
38. Ryoo, Seung Kyu, et al. "Fabrication of Ultrathin Ferroelectric $Al_{0.7}Sc_{0.3}N$ Films under Complementary-Metal-Oxide-Semiconductor Compatible Conditions by using HfN0. 4 Electrode." *Advanced Materials* 37.1 (2025): 2413295.
39. Sun, Wenxin, et al. "Integration of ferroelectric $Al_{0.8}Sc_{0.2}N$ on Si (001) substrate." *IEEE Electron Device Letters* 45.4 (2024): 574-577.
40. Yassine, Mohamed, et al. "Influence of structural properties on the ferroelectric behavior of hexagonal AlScN." *Journal of Applied Physics* 132.11 (2022).
41. Choi, Hwa Seob, et al. "Tailoring the coercive field in ferroelectric metal-free perovskites by hydrogen bonding." *Nature Communications* 13.1 (2022): 794.
42. Wang, Bin, et al. "Room temperature lead-free multiaxial inorganic–organic hybrid ferroelectric." *Inorganic Chemistry* 58.20 (2019): 13953-13959.
43. Wang, Yuan, et al. "A stable rhombohedral phase in ferroelectric Hf $(Zr)_{1+x}O_2$ capacitor with ultralow coercive field." *Science* 381.6657 (2023): 558-563.
44. Cao, Rongrong, et al. "Effects of capping electrode on ferroelectric properties of $Hf_{0.5}Zr_{0.5}O_2$ thin films." *IEEE Electron Device Letters* 39.8 (2018): 1207-1210.
45. Walke, Amey M., et al. "La Doped HZO based 3D-Trench Metal-Ferroelectric-Metal Capacitors with High Endurance ($>10^{12}$) for FeRAM Applications." *IEEE Electron Device Letters* (2024).
46. Zarubin, Sergei, et al. "Fully ALD-grown TiN/$Hf_{0.5}Zr_{0.5}O_2$/TiN stacks: Ferroelectric and structural properties." *Applied Physics Letters* 109.19 (2016).

47. Buragohain, Pratyush, et al. "Effect of film microstructure on domain nucleation and intrinsic switching in ferroelectric Y: HfO_2 thin film capacitors." *Advanced Functional Materials* 32.9 (2022): 2108876.
48. Muller, Johannes, et al. "Ferroelectricity in simple binary ZrO_2 and HfO_2." *Nano letters* 12.8 (2012): 4318-4323.
49. Richter, Claudia, et al. "Si doped hafnium oxide—a "fragile" ferroelectric system." *Advanced Electronic Materials* 3.10 (2017): 1700131.
50. Li, Yu-Chun, et al. "Domain switching characteristics in ga-doped HfO_2 ferroelectric thin films with low coercive field." *Nano Letters* 24.22 (2024): 6585-6591.
51. Chernikova, Anna G., et al. "Improved ferroelectric switching endurance of La-doped $Hf_{0.5}Zr_{0.5}O_2$ thin films." *ACS applied materials & interfaces* 10.3 (2018): 2701-2708.
52. Kim, Ik-Jyae, and Jang-Sik Lee. "Unlocking large memory windows and 16-level data per cell memory operations in hafnia-based ferroelectric transistors." *Science Advances* 10.23 (2024): eadn1345.
53. Shen, Pin-Chun, et al. "Ferroelectric memory field-effect transistors using CVD monolayer MoS_2 as resistive switching channel." *Applied Physics Letters* 116.3 (2020).
54. Zhao, Ruiting, et al. "Reconfigurable aJ-Level Ferroelectric Transistor-Based Boolean Logic for Logic-in-Memory." *Nano Letters* 24.35 (2024): 10957-10963.
55. Kim, Kwan-Ho, et al. "Scalable CMOS back-end-of-line-compatible AlScN/two-dimensional channel ferroelectric field-effect transistors." *Nature Nanotechnology* 18.9 (2023): 1044-1050.

56. Gao, Xinzhu, et al. "Realization of flexible in-memory computing in a van der Waals ferroelectric heterostructure tri-gate transistor." *Nano Research* 17.3 (2024): 1886-1892.
57. Wang, Xiaowei, et al. "Van der Waals engineering of ferroelectric heterostructures for long-retention memory." *Nature communications* 12.1 (2021): 1109.
58. Si, Mengwei, et al. "Ferroelectric field-effect transistors based on MoS_2 and $CuInP_2S_6$ two-dimensional van der Waals heterostructure." *ACS Nano* 12.7 (2018): 6700-6705.
59. Singh, Prashant, et al. "Two-dimensional CIPS-InSe van der Waal heterostructure ferroelectric field effect transistor for nonvolatile memory applications." *ACS nano* 16.4 (2022): 5418-5426.
60. Park, Sangyong, et al. "Laterally gated ferroelectric field effect transistor (LG-FeFET) using α-In_2Se_3 for stacked in-memory computing array." *Nature Communications* 14.1 (2023): 6778.
61. Wang, Zhongwang, et al. "Reconfigurable Quasi-Nonvolatile Memory/Subthermionic FET Functions in Ferroelectric–2D Semiconductor vdW Architectures." *Advanced Materials* 34.15 (2022): 2200032.
62. Ko, Changhyun, et al. "Ferroelectrically gated atomically thin transition-metal dichalcogenides as nonvolatile memory." *Adv. Mater* 28.15 (2016): 2923-2930.
63. Sun, Yanmei, et al. "Multilevel memory and artificial synaptic plasticity in P (VDF-TrFE)-based ferroelectric field effect transistors." *Nano Energy* 98 (2022): 107252.
64. Dang, Zhaoying, et al. "Black phosphorus/ferroelectric P (VDF-TrFE) field-effect transistors with high mobility for energy-efficient artificial synapse in high-accuracy neuromorphic computing." *Nano letters* 23.14 (2023): 6752-6759.

65. S. M. Anthony, S. Granick, Image analysis with rapid and accurate two-dimensional gaussian fitting. *Langmuir* **25,** 8152–8160 (2009).
66. Jia, Chun-Lin, et al. "Unit-cell scale mapping of ferroelectricity and tetragonality in epitaxial ultrathin ferroelectric films." *Nature Materials* 6.1 (2007): 64-69.
67. Si, Mengwei, et al. "A ferroelectric semiconductor field-effect transistor." *Nature Electronics* 2.12 (2019): 580-586.
68. Han, Wei, et al. "Phase-controllable large-area two-dimensional In_2Se_3 and ferroelectric heterophase junction." *Nature nanotechnology* 18.1 (2023): 55-63.
69. Yang, Tilo H., et al. "Ferroelectric transistors based on shear-transformation-mediated rhombohedral-stacked molybdenum disulfide." *Nature Electronics* 7.1 (2024): 29-38.

Chapter 6. Conclusion and future research

6.1. Conclusion

In conclusion, this thesis developed a high-performance $MoSe_2$ field-effect transistors and an ultrathin high-κ dielectric materials for 8-in. level MoS_2 field-effect transistors, which is significant for 2D devices towards prolonging Moore's Law. The study focuses on the materials synthesis and devices fabrication for high-performance with high on/off ratio, small SS and large on-state current.

For $MoSe_2$ growth and high-performance transistors fabrication, high-quality continuous $MoSe_2$ films with salt as metal sources are successfully synthesized. The domain size is around 120 μm, which is larger than that in most litheratures and oxide sources. Raman and PL also demonstrate its high-crystalline quality. Electrical measurement shows that the $MoSe_2$ film is uniform and transistors coule reach a high on/off ratio of 10^9 and a high on-state current of 12 μA/μm at 1 V bias, which is superior than that in reported literatures.

For ultrathin high-κ HfO_2 dielectrics, we utilize an optimized ALD process with two-oxidation step to deposit defect-free high-quality 1.3-nm-thick HfO_2 high-κ dielectric layers on 8-inch wafers at only 200 °C. Our ultrathin HfO_2 film shows an extraordinarily small EOT of 0.27 nm, a ultrasmall leakage current of 10^{-14} A/μm^2 at 1 V bias voltage, and a robust breakdown electric field of approximately 32 MV/cm. We also fabricate MoS_2 transistors and circuits with 1.3-nm-thick HfO_2 as dielectric layers to demonstrate its practicality and gate controllability. Typical transistors exhibit large on-state current density of 250 μA/μm and an impressive on/off ratio of 10^8, accompanied by an ultra-low subthreshold slope of 60 mV/dec. Logic gates and memory devices are also fabricated on 8-inch wafers to demonstrate its substantial implications for the forthcoming advanced semiconductor processes in the Angstrom Era.

Large-scale homogenous STO/PTO/STO topological flux-closures are epitaxially grown on sacrificial SAO layers. In freestanding multilayer films, a single rigid flux-closure structure exists, contrary to the previously believed coexistence of flux-closure structures and ferroelastic domains. These flux-closure structures in freestanding films, equivalently distributed along the [100] and [010] directions, exhibit a simple transformation pathway from topologically nontrivial to single domain. Moreover, we fabricated large-scale topological ferroelectric transistor arrays, inheriting the excellent stability and low power characteristics of ferroelectric topological structures. The flux-closure array capacitors demonstrate exceptional performance, with no detectable leakage current below 10 V, a remanent polarization (P_r) reaching 195 μC/cm^2, and a cycle endurance of up to 10^9 at 1 MHz. Notably, the E_c/E_b (coercive field/breakdown field) is as low as 0.15. The CMOS-compatible Fe-FETs show a large memory window of ~ 0.43 V/nm, high on/off ratio of 10^8, stable retention for up to 10 years, superior uniformity and flexible applications. This work moves a significant step towards the ultimate ambition of realizing ferroelectric devices in future semiconductor industries and flexible electronic products.

6.2. Future research

Two-dimensional materials and field-effect transistors have been the research focus for replacing silicon-based devices. According to the IRDS 2024, 2D materials and devices would be commercial before 2037. So, developing more functions and higher performance for 2D devices is important and urgent.

For $MoSe_2$ film, in this thesis, we measured its electrical performance. It is known that bandgap of $MoSe_2$ is smaller than that of MoS_2, so, the optical and optoelectronic performance of $MoSe_2$ should also be researched in the future. It is worth noting that constructing $MoS_2/MoSe_2$ heterostructure would prepare a

platform for research on layer exciton and moire exciton, which maybe helpful in future photodetectors and photovoltaic devices. High-quality wafer-scale $MoSe_2$ film also make these heterostructure devices be and industrial and commercial one day.

Ultrathin HfO_2 film with 1.3-nm thickness is important for low-power electronics in the 2D transistors and circuits. In this thesis, I fabricated back-gated transistors while in the industrial, top-gated and gate-all-around are more common. So, in the next step, I would like to make gate-all-around transistors to expand the application of ultrathin HfO_2 film. Maybe a higher carrier density of MoS_2 be foreseen. Except MoS_2 transistors, graphene, WSe_2 and other 2D materials could also work as channel materials and ultrathin HfO_2 works as high-κ dielectrics. More single devices and complementary circuits, such as inverter, should be demoed with such thin dielectric film.

In summary, using wafer-scale 2D materials and compatible high-κ dielectric film, more functional devices and high-performance devices should be prepared to make the 2D nanoelectronics be realized in the future.