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A Study of Copper Thickness Distribution in Electroplating of Printed Circuit Boards

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Abstract

Copper electroplating is a very critical process for the printed circuit board (PCB) industry and it is increasingly important to maintain an even copper deposition over the PCB surface as circuitry design gets finer and denser. Although there has been considerable amount of research efforts to enhance plating quality of PCBs over the last few decades, most of the studies still rely on relatively small or laboratory scale experimental set-up. With the collaboration of a local PCB manufacturer, the project has made an important attempt to study the copper deposition behaviour in an industrial tank with a plating window of 144 inches. An industrial copper electroplating tank was designed and set up in the project such that seven hardware factors can be varied and their effect on copper deposition distribution can be examined.

In the study, the Taguchi methodology was employed to examine the effect of plating tank design and configuration including anode geometry, anode distribution, electrode separation, relative size of the electrodes, cathode oscillation velocity, eductor orientation, eductor flow rate, and the current density on copper thickness distribution. Two consecutive sets of Taguchi design of experiment (DOE) were carried

out for both planner and pattern substrates PCBs, in which a total of 58 industrial scale experiments were carried out. The mean response of each factors were examined, and the experimental results showed that the copper deposition evenness can be improved using the enhanced hardware settings for current densities commonly used in the PCB industry. Strong interactions demonstrated that previous result or models based on a laboratory scale set-up may not be applicable to full scale production. The Copper thickness distribution along the 144" PCB cathode was also studied from top to bottom and from one end to the other, and the edge effect was examined. The significance of the findings to the PCB industry was discussed and the outcomes of the project have led to a good foundation for further theoretical investigations.

List of Publication

1. **H.T. Chow** and **K.C. Chan**, "Enhancement of hardware factor for industrial PCB electroplating process", *Journal of Electronics Manufacturing*, to be Submitted
2. **H.T. Chow** and **K.C Chan**, "Deposition Behaviour of Copper in Electroplating Industrial Printed Circuit Boards", *Transactions of Institute of Metal Finishing*, to be submitted.

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1. Introduction

1.1 Copper Plating Problems in PCB Industry and Topsearch

Electro-plating is a very critical process in printed circuit boards (PCBs) industry. As the geometry of PCBs and integrated circuit is becoming smaller, the copper plating distribution over the PCB surface is becoming more important. An evenly distributed surface copper deposition is critical for the fine features manufacturing for the chemical etching after the electroplating process. The deposition evenness over the PCB surface is directly related to etch rate, thus the shape and width control of the circuitries created. The shape and line width control, which are directly related to the electrical performance of the end products, are of significant importance especially when recent advance PCB features are downsized to 2mil (50μm) in mass production.

In order to meet the market demand, PCB shops need to improve the plating process so that fine lines and circuitries can be manufactured in mass production. Academic researches have been carrying out in different areas of the copper electroplating process. These include the effect of chemistry, hardware design as well

as the nature of the current application on the deposition behaviour. However, most of the results reported were based on the studies of a limited number of process factors in relatively small scale equipment, which might not be well applied due to the complexity of the industrial process. The interactions between process factors also limit the application and integration of these academic findings into the industrial arena. There is a need to conduct a systematic study to examine the effect of hardware design factors on the plating quality using industrial plating tanks. This can help provide a better understanding of the copper electroplating process in industrial scale and to provide verification or integration of the results and efforts from academic researches.

1.2 Research Collaboration with PCB Manufacturer

This research was a collaboration project between Industrial and Systems Engineering Department of the Hong Kong Polytechnic University and Topsearch Printed Circuits (HK) Ltd. The funding of the research was supported by the Topsearch and the University-Industry Collaboration Program (UICP) of Innovative Technology Fund of the Industrial Department of the Hong Kong Special Administrative Region (HKSAR).

The UICP aims at stimulating private sector interest in R&D through leveraging the knowledge and resources of universities. The emphasis is on close collaboration between private companies and universities in Hong Kong. The Teaching Company Scheme of the program aims at fostering university-industry partnership by supporting local companies to take graduate students from local universities to assist in proprietary R&D work.

Topsearch Printed Circuits Company Ltd is one of the leading Hong Kong based PCB manufacturers. The manufacturing facility of Topsearch is set up in Shenzhen, China while headquartering in Hong Kong. Topsearch invests on research and development in different areas of the PCB industry and is collaborating different research programs with the universities. These include the set up of a joint environmental research center with the Beijing Tsing Hua University as well as PCB technology research programs with the Hong Kong Polytechnic University. Experiments were carried out in an industrial plating tank in the Shenzhen factory of Topsearch.

1.3 Objectives of the Project

The prime objective of the project is to study the effect of different hardware settings on the copper electroplating quality of the PCB industry in terms of copper deposition evenness. The specific objectives of the project are:

1. To develop a copper plating tank set-up in industrial scale for experimental investigations
2. To apply the Taguchi method to study the effect of different electroplating process factors on the copper deposition evenness
3. To examine the copper deposition evenness on the PCB substrate across the cathode in the PCB industrial electroplating process

2. Literature Review

2.1 Industrial Copper Electroplating Process of PCB Industry

2.1.1 Panel Plating and Pattern Plating

Traditional copper plating process in PCB industry consists of panel plating and pattern plating. In panel plating, copper is deposited onto the entire PCB surface of a thin layer of base copper and through holes. From industrial point of view, panel plating can provide a more uniform copper deposition over the entire PCB surface. However, the cost of panel plating is relatively higher due to the cost of copper is relatively more expensive. An evenly thickened copper layer will also increase the difficulties for the subsequent etching process control to provide well-defined circuitries.

In pattern plating, copper is deposited onto the desired circuitries and features by electroplating over an organic protective mask laminated on the PCB surface. Tin plating, after copper plating, is also required to protect the desired circuitries and features from the subsequent chemical etching process. From industrial point of view,

pattern plating can provide a more precise control of circuitry dimension and minimize the waste of copper which is relatively expensive. However, a greater variation in copper deposition thickness would always be found due to the localized current effect induced by the conductive circuitry pattern. Over building of copper and tin may also increase the difficulties in removing the organic protective mask before the etching process.

2.1.2 Copper Electroplating Hardware

The hardware of the copper electroplating process of the PCB industry is one of the critical concerns in production of reliable PCB products. It will affect the copper deposition thickness on the PCB surface while a specified thickness of hole wall copper is required to be plated. The electrochemical process includes a pair of anode and cathode in a well-agitated electroplating cell. In traditional PCB electroplating process, copper pallets contained in metallic anode baskets would be employed as the anodes while the PCB itself would be employed as the cathode. The anode baskets are distributed along an anode bar while the PCB will be attached to the cathode bar, both running across the width of the plating cell.

Good agitation for the electroplating process ensures that the electrolyte in the process can be well stirred, thus enhances the mass transfer for the electrochemical reaction. This is important, especially in large scale industrial plating cell, as the mass transfer of chemicals in the electrolyte is always one of the major limitations of copper deposition for the process, especially within through holes. Air sprinkling, vibration or/and oscillation of cathode bar as well as eductor circulations are the common agitation system used for traditional PCB electroplating process.

2.2 Research on Copper Electroplating

Works on and basics of electroplating factors were reported widely in previous literatures [1-4]. The effect of different copper electroplating process factors, such as the effect of chemicals, on plating performance was also investigated and studied [5, 6]. The importance of uniformity of plating thickness of plate through holes (PTHs) over the entire work piece (PCB) was discussed by Kessler and Alkire [7]. It is important to obtain an even copper plating thickness over the surface of PCBs. There have been considerable amount of efforts to investigate the relationship of various plating parameters and their corresponding effects on PCBs. Although good attempts have been made to use pulse current, hardware design parameters and new plating bath composition to enhance plating process, design of plating tanks as a whole which is known to significantly affect plating quality is still based on previous experiences and industrial rules of thumb. Literatures were reported extensively (for example [8]), however, only in laboratory scales on the relationship between few design factors and the plating thickness variation, although the technology of through mask plating had been used for the electroplating of PCBs for more than 20 years [9].

Computer softwares were also developed for simulation of the industrial

electroplating process including the design of plating tanks. Simulation and design tools for electroplating were also updated by Druesne and Afzali [10]. In the report, the computer software ACIS® was described and introduced. The software was developed based on boundary element analysis. In the studies, the modeling of plating a rack with zinc and full optimization of hard chromium plating of valves were carried out with ACIS® computer software. The results of the simulation of the electroplating process generated by the computer software were in close agreement with the measurements taken from the plating cell. Other studies also reported that the reliability of computer simulation for electroplating design could be verified by different industrial applications [11, 12].

Design of experimental (DOE) will be a practical tool to provide an insight into the multi-parameter nature of the electroplating process. Numerical techniques, such as boundary element methods, were reported but few have been published in experimental approach for problem solving [13]. Numerical methods are constrained due to complexity of surface feature for PCB electroplating. Poon et al., [9, 13] reported the relationship of plating thickness variation and various plating parameters recently with experimental approach but only few plating tank design factors were

considered.

Although it is well known that the deposition thickness will be thicker at lower pattern density, such as isolated traces and PTHs on PCBs, it was only first described by Romankiw et al., until the 70's [14]. Horkans and Romankiw [15] also reported and discussed such effect in their later studies. The hypothesis of "crowding" of flux at isolated features was suggested. Yung et al. [16] also reported similar observations in their work. Theoretical and mathematical modeling of such effect on patterned features was also carried out by Mehdizadeh et al. with potential-theory for electroplating [17, 18]. The active-area-density (AAD) was introduced in their work which defined a fractional electro-active area within a particular region of interest. The AAD concept was also employed by other researchers including Choi and Kang [19] and Poon et al. [9]. In the study by Poon et al., the concept of active area density ratio was further elaborated which provided a more detailed study of effect of plating parameters on the variation of deposition thickness in the PCB plating process.

2.2.1 Modeling of Current Density Distribution

Models of current density distribution in acid copper electro-deposition were reported by researchers with mathematical treatment. However, these numerical models are limited by the correctness of the physiochemical description of the system and the precision in which the process parameters are known. The nonlinear electrode kinetics and mass transfer characteristics of electrolyte also make analytical solutions impractical even for the simplest geometries [20, 21]. Current distribution is critical for the deposition thickness because the deposition rate is proportional to the current density at a location. It is also worthwhile to note that other factors, for example the chemical component mass transfer at the boundary layer, can also affect the plating distribution.

A review of current distribution modeling was carried out by Poon and Williams [8] based on studying how the deposition uniformity was affected and optimized by the various process and product parameters of the system. A study by Dokovic [22] is particularly appropriate to the PCB electroplating. These size scales includes:

1. Work piece scale – current distribution over the whole object under

electrodeposition such as PCB panel.

2. Pattern scale – current distribution among the patterns on the surface of the work piece with different densities of features such as the lithographic patterns over a PCB panel.

3. Feature scale – current distribution within an individual feature of a pattern such as the through hole, blind-via or conductor wire in a circuit pattern on a PCB.

4. Roughness scale – the microscopic roughness or asperities of an individual feature.

The work piece level, pattern level and feature level modeling will be discussed in detail since the objective of this project is to study the quality of plating in a macro-scale point of view. Work piece and pattern level modeling are of particular interest because they resemble the panel and pattern plating of the PCB industry.

2.2.1.1 Work Piece Level Modeling

The nature of analytical methods has limited early investigations to flat surface and simple geometries. Numerical analysis developed later has enabled studies to be

carried out for more complex geometries. For the electroplating process in the PCB industry, electrodes are set up in a parallel planar geometry and two and three dimensional models have been proposed by researchers based on a similar setting.

Moulton [23] presented a classical solution for the primary current distribution for two electrodes placed on the boundary of a rectangle. Wagner [24] proposed with formal mapping of the parallel electrode to solve the primary current distribution. His study concluded that the primary current density is infinite at both ends of the electrode and decreases exponentially and symmetrically until a minimum value at the centre of the electrode. This implies that the deposition rate at both end of the electrode will be much faster than that in the middle.

$$\frac{i}{i_{avg}} = \frac{2}{\pi\sqrt{1-(x/m)^2}} \quad \text{.......... (1)}$$

where x = the distance measured from the center of the electrode,

i (mA/cm^2) = current density at a point of distance x from the center of the electrode,

i_{avg} (mA/cm^2) = the average current density over the electrode and

$2m$ = the length of the cathode (cm)

In the study carried out by Hine et al. [25], the effect of the ratio of electrode size, the separation of electrodes as well as the gap between the electrode and the insulating side wall was studied. It was concluded quantitatively that the larger the electrodes and the smaller the gap width, the more uniform the current distribution would be. However, the current distribution was not shown explicitly as their focus was placed on the relative share of current at the two sides of the electrode under different cell geometries.

Yoshida et al. [26] and Koseki et al. [27, 28] reported the effect of unequal electrode length, different electrode separations and different gaps between the electrode and the insulating side wall on current density distribution. Their studies concluded that current uniformity could be enhanced when:

1. The anode is narrower than the cathode,
2. The electrode separation is smaller than half-length of the cathode, and
3. The edges of the cathode are in contact with the side walls, although only a weak

influence was observed.

The minimum electrode separation, however, was not defined in their study although it is of particular importance for the plating tank design. The practical application of their model was also criticized by Poon and Williams [9, 13] – the assumption of negligible polarization has restricted the current density used in their experiments to a very low value of 5 mA/cm^2.

Choi and Kang [19] also reported a three dimension model to predict the current distribution on a uniformly patterned cathode with an auxiliary electrode. The concept of active-area-density (AAD), developed by Mehdiazdeh et al. [17, 18], was used and they concluded that a smaller AAD will lead to a more uniform current distribution. It was further concluded that uniform current distribution could be obtained by proper combination of auxiliary electrode and the ADD. However, there was no comparison with experimental data in the paper. It is also worthwhile to notice that the study was carried out with electrodeposition of permalloy (80% Ni – 20% Fe) instead of copper, although the study may be applicable and applied to electroplating of copper.

Other studies of current distribution based on the work piece level were also reported by various researchers. Hull cell work piece modeling was carried out by Matlosz et. al., [29] and the DIN standard [30] offers an empirical formula for the primary current distribution in a Hull cell panel (cathode):

$$\frac{i(z)}{i_{avg}} = 2.331 \cdot \log \frac{1}{1-z} - 0.08 \quad \text{.......} \quad (2)$$

where $i(z)$ is the local current density of a point at a normalized distance z measured from the low current density edge and $0.186 < z < 0.941$. Researchers including Moulton [23], Hine et. al. [25] and Yoshida et al. [26] also reported by similar methods in solving the primary distribution problem. The current distribution estimated as:

$$\frac{i(z)}{i_{avg}} = \frac{z^{1.273}}{(1-z)^{0.359}}(1.733 - 0.736z) \quad \text{.......} \quad (3)$$

was found to be in good agreement with the empirical solution offered in the Norm DIN standard [30].

2.2.1.2. Pattern Level Modeling

As mentioned, PCB pattern plating is a typical example of this pattern level category. Although PCB pattern plating has been widely used in the industry for more than 20 years, little was reported literarily until a formal mathematical treatment in 1988 according to Poon and Williams [8]. The two possible reasons are:

i. the significant amount of work reported for work piece and feature modeling, particularly through-hole plating, suggests that problems in these two domains are of sufficient complexity to demand the effort of the most researchers in this areas

ii. the numerical technique required to solve the pattern scale problem, notably the boundary element method (BEM), has evolved as a viable tool only after its successful application in solving problems at the other scales

It is well known in the PCB industry that the distribution of patterns (design feature and circuitries) is having a significant effect on the resulting current distribution, thus the electrodeposition thickness in the through mask plating process.

The effect was first described by Romankiw et al. [32]. In the study, the use of on-board "current thieves" which utilizes dummy patterns on the board surface was introduced to even out the current distribution. Other approaches described by researchers to solve the problem of uneven electrodeposition due to the pattern effect included employing an auxiliary cathode with separate galvanostatic control as off-board current thief [33, 34]. The on-board and off-board "current thieves" have been widely applied in nowadays PCB industry nowadays.

Mehdizadeh et al. [17] proposed the first theoretical model of current distribution over a patterned substrate using the potential theory model for electrodeposition. The expression active area density (ADD) was introduced in their paper in 1992 [18]:

$$AAD = \frac{A_{act}}{A_{sup}} \qquad (4)$$

where A_{act} is the active area exposed to electrode-position over a particular region, e.g. the actual area of circuitry patterns over a PCB, and A_{sup} is the superficial area of that region, e.g. the geometric area of the PCB.

According to the AAD concept, they concluded that the pattern-induced nonconformity can be reduced by:

1. Increasing the bath conductivity,
2. Application of a smaller average superficial current density over the cathode; This, however, will reduce plating rate,
3. Reducing the ADD contrast among different regions on the substrate,
4. Reducing the size of the zone over which the AAD contrast occurs, and
5. Reducing the average AAD over the entire substrate.

The findings in their work, however, did not provided a practical solution for the PCB plating process from the perspective of production efficiency and product design criteria.

The model was further elaborated later by the same author in Mehdizadeh et al. [18]. The modified model gives better deposition thickness prediction, especially in the case of application of high current density such as that in commercial plating process, than the previous model by introducing an enhancement factor. The model

shows that both active area density effect and the pattern driven mass transfer effects are contributing to the non-uniform current distribution over lithographic patterns. In their study, the "edge effect" of non-uniform current distribution was also reported numerically. They found that the primary current distribution is a step profile in inverse proportion to the active-area-density ratio. In order to prevent the concentrating of current density into the patterned region, they introduced the use of "current thief", or appropriate auxiliary electrodes to reduce the non-uniformity of current distribution.

Other studies of current distribution based on the pattern level were also reported by various researchers. Horkans and Romankiw [15] described the "crowding" of current lines into isolated pattern and Yung et al. [16] mentioned the effect of circuit layout on the macro-scale thickness uniformity.

2.2.1.3 Feature level Modeling

Good examples for feature level scale are the through holes and rectangular trench of a polymeric mask on a PCB. The influence of mass transfer and concentration over-potential as well as the evolution of the electrode shape during the deposition process become highly important [22] in feature scale modeling.

The effect of various plating factors on plating uniformity was reported by Alkire and Mirarefi [35]. Their study was regarded as the first mathematical analysis of through-hole problem [16]. The mathematical analysis was later confirmed experimentally by Engelmaier and Kessler [36]. They also found that the process window can be enlarged by adding organic additives, which is appropriate for both the PCB and chemical supplying industry.

Middleman [37] also showed that, although his assumption was considered controversial [22], periodic flow reversal was much more effective in promoting uniform reaction rate along the hole length than steady flow in one direction.

Experimental approach modeling was also recently carried out by Poon et al. [13] to study the effect of various factors on the variability in blind-via electroplating. It was verified experimentally that the optimum combination of the average current density and the electrode separation respect to minimum thickness variability across the whole work piece.

Theoretical analysis of the plating of high aspect ratio (HAR) through-holes was carried out by Lanzi and Landau [38]. The limiting current due to mass transfer and ohmic resistance effect was calculated and two expressions were developed:

Mass transfer:

$$\bar{i}_{L,avg} = \frac{FD_{iCb}}{R_0}\{1.15A^{1/3} - 1.2 - 0.65A^{-1/3}\} \quad \text{.......... (5)}$$

Ohmic resistance:

$$i_{c,\Omega} = \pi^2 RTR_{0\kappa} / \alpha_c FL^2 \quad \text{.......... (6)}$$

where $\bar{i}_{L,avg}$ is the average current density at the limiting mass transfer rate (mA/cm^2);

Di is the diffusion coefficient of cupric ion (cm^2/s);

A is a convection variable jointly determined by hole/bath geometry and electrolyte characteristic;

$i_{c,\Omega}$ is the upper limit of the (secondary) current density at the center of the hole imposed by ohmic resistance (mA/cm^2).

It was concluded from the study that the ohmic resistance imposed the critical limitation on the current density within the through holes. The dominant effect of ohmic resistance on current density within a through hole was also reported by Yung et al. [16]. Alkire and Ju [39] also suggested improving the plating uniformity in HAR holes by reducing the effect of ohmic resistance by

1. increasing the electrolyte conductivity, κ,
2. reducing the hole length, L, and increasing the radius, R_0,
3. miniaturizing the hole for a given aspect ratio, thus reducing L^2/R_0,
4. reducing α_c by altering the reacting kinetics with organic additives.

The recommendations were also rectified by the general model of Hazlebeck and

Talbot [40] for the case of ohmic-limited plating.

Other experimental approaches to study the current distribution on feature scale were also reported by various researchers. Barringer and Carano [41] used a 2^3 full factorial design to study the effects of bath temperature, leveling agent and the acid/copper ratio on electrodeposition evenness. Haluzan and Reichenbach [42] employed a Taguchi L_{18} orthogonal array to study the effect of the concentration of copper, formaldehyde, caustic soda, temperature and deposition time on the electroless deposition rate and coverage. Forrest and Reed [43] investigated the effects of the same set of parameters on the S/H ratio of electroplated copper in HAR through-holes using a replicated D-optimal design of 32 runs. Bokisa and McFarland [44] employed a general factorial design to study the influence of aspect ratio, current density and copper sulphate concentration upon the S/H ratio of plated-through holes.

2.2.2 The Effect of Anode on Electroplating

Until recent years anodes have been amongst the least considered factors in electroplating process and in early textbooks very little space was given to their use and design etc. However, anode related process parameters (e.g. shape of anodes [45]) are well known of having significant effect on plating efficiency and quality.

Cobley and Gabe [46] presented the application of different types of anode and the future developments for more efficient anodes. Soluble copper anode is commonly used in the PCB industry for copper electrodeposition but few studies have been carried out to report the effect of anode related parameters on the electrodeposition thickness variation at work-piece-level. The usage and performance of insoluble anodes, however, were reported by different researchers. Sriveeraraghavan et al. [45] performed a study on the effect of different shapes of insoluble and soluble anodes on plating thickness distribution and porosity. It was reported that soluble anodes of square, circular and rectangular shape with equal area to the cathode can be used. Soluble anode of triangular shape with 50% lesser area as that of the cathode can be used and may also reduce the cost of anodes and minimizing the impurities build up while maintaining similar current efficiency and metallic plating distribution. It is

also worthwhile to note that the plating thickness variation in their study was not optimized based on the experimental data. Further verification of the experimental result was not reported.

Cobley et al. [47] also reported and summarized the application of insoluble anode. A set of criteria was established, which an insoluble anode material should meet if it is to be successfully employed in an acid copper horizontal electroplating machine in their studies

2.2.3 The Effect of Agitation on Electroplating

Agitation is a critical process factor in the electroplating process but received relatively little investigation over the 150 years of electroplating process development [48]. It is well known that appropriate agitation can have significant effects including:

1. Avoiding stagnation by dispersing products and transport reactants,
2. Increasing deposition rates through stirring to reduce electrode diffusion layer thickness,
3. Removal of heat from the interface and equilibrate the deposit or coating,
4. Incorporating particles in the deposit (composite coating production), and
5. Modify the deposit properties of grain size, hardness etc. [48]

One of the major effects of agitation is to provide a thin and uniform layer, the diffusion layer, for a restricted concentration variation of chemistry of the electrode surface, which was reported by Lyons [49].

Air bubbling is still being used in the PCB electroplating process due to its simplicity, relative effectiveness and reasonably low cost. The relative importance of

air sparging in comparison with mechanical board oscillation and their effects on the mass transfer rate over the entire board surface as well as in the interior of the through-hole was also reported [50]. However, research [48] showed that a 20-30% loss in conductivity of the plating solution can be induced by air bubbling and the loss over the plating process tank is not uniform. It is concluded that in the electrodeposition process where good throwing power is required, the performance of electroplating is related to the type and degree of agitation used. The significance and importance of solution conductivity for electrodeposition solutions and their efficient used were discussed by Guvendik and Gabe [51]. This significant loss in solution conductivity is important from the efficiency of plating point of view and is critical for the PCB industry. Among the different forms of agitation, the use of eductors in the electroplating process for PCB industry is becoming popular.

2.2.3.1 The Use of Eductor

The use of eductors, which are available in many proprietorial forms, is in principle old technology but has recently been adapted to use in electroplating application. One of the pioneers reporting the effect of educator on PCB

electroplating is Ward et al. [48]. In their study, the effect of eductor on the deposition thickness variation across 18"x24" copper boards was reported. The effect of a single, 4, 6 and 8 eductors for agitation was investigated. A comparison was also made between educators and air bubbling as an agitation mean for copper electroplating process. It was concluded based on their experimental result that a faster deposition rate, reduction in variation of deposition thickness across the panels as well as minimization of the 'edge effect' on large panels can be achieved by using educators for agitation. The author also commented that the geometry of eductor is believed to be a significant feature of its effectiveness.

In another study, Ward and Gabe [52] reported the used of eductor agitation and showed its importance in the contest of surface heat dispersal of the electrodes, thus improvement on deposition properties that are temperature sensitive can be achieved.

2.2.3.2 Other Forms of Agitation

Studies were also carried out at an earlier time by Gabe et al. [53-55] to investigate the effect of vibratory agitation for electrodeposition. The characterization

of vibratory agitation, together with the effect of vibration on deposition rate and composite plating were reported. The study [54] found that the rate of electrodeposition could be enhanced by 5-20 times.

In the study carried out by Duchanoy and Lapicque [56], the effect of flow pattern on current distribution was discussed. Velocity and flow characteristic of the fluid flow across the substrate were reported to be directly related to the current distribution.

2.2.4 Pulse Current Electroplating

The use of pulse current electroplating in different industries and academic research have been developing and reported extensively over the pass few decades. Pulse plating has been regarded as a better deposition mode than DC electroplating since the relaxation period during the reverse plating and/or rest enables larger currents to be applied during the pulse-plating period without the concentration depletion of reactants [57]. The anticipated advantages of pulse plating [58] based on previously reported work can be enumerated:

i. improved physical properties including increased hardness [59-61] as a result of finer grained structure [62], reduced porosity [63-67], and also increased density, ductility and electrical conductivity [68, 69];

ii. increased deposition current density, and hence plating rate, by virtue of operating nearer the instantaneous limiting current density [70, 71];

iii. improved adhesion of the deposit to the substrate, possibly due to oxide film reduction [70], and

iv. improved plating distribution and thickness uniformity especially in relation to recesses [70, 71].

Bai and Hu [72] reported the effects of five plating modes, including DC potentio-static and galvanostatic, pulse-rest and pulse-reverse plating and cyclic voltammetry, on the morphology and roughness of Copper deposits. Kalantary and Gabe [58] also investigated the cathode efficiency and coating properties in pulse plating. They concluded that the cathode efficiency can be increased under certain unipolar pulse conditions. The coating properties including the microhardness, tensile strength and elongation are directly affected by the pulse technique used.

In a later study by Hu and Wu [73], the delectrodeposition of various copper deposits was also carried out by means of cyclic voltammetric, potentiostatic, galvanostatic, pulse-rest and pulse reverse plating modes. It was report in the study that either cyclic voltammerty or reverse plating rendered the significant dissolution of grain peaks and resulted in a relatively smooth electroplating surface

2.2.5 Electrolyte – Chemical Additive and Conductivity

The potential gradients in solution, the electrolyte composition and the influence of organic additives are of major concern for copper electrodeposition and have been studied for over 50 years [74]. The significance of solution conductivity for electrodeposition solutions and their efficient usage were discussed by Guvendik and Gabe [51]. In the report, the conductivity data for copper, tin, iron, nickel, zinc as well as other plating solutions were presented and reviewed. Chemical additives in electrolyte solutions also play important roles in copper electroplating [75]. It is of great importance in the PCB industry as the demand of integrated circuit and via hole filling is increasing. In the research by Gau et al [75], it was found that the addition of thiourea and polyethylene glycol, which are usually added in PCB electroplating chemistry to influence nucleation, could help in forming of smooth copper film but did not promote copper filling ability. Hydroxyl amine sulphate was purposed for use as a gap filling promoter in helping copper electroplating. It was demonstrated in their study that copper could be electroplated into fine trenches without void when hydroxyl amine sulfate was presented in the plating solution.

Reid [74] reported the dependence of IC filling processes upon plating bath

chemistry and polarization characteristics. In the study, it was found that filling is most readily achieved by using additives containing a polymer suppressor and a mercapto accelerator. Highly polarized electrolytes which maintain strong current suppression on the wafer surface and aid in uniform nucleation within features are beneficial to high aspect ratio feature filling.

In the research carried out by Miura and Honma [76], via-filling for build up process of PCBs and the ultra large scale integration (ULSI) wiring formation without void and over plate has been examined. Acid cupric sulfate bath containing chloride, polyethylene glycol, bis (3-sulfopropyl) disulfidedisodiu, Janus Green B and thiourea was employed as the electroplating electrolyte in the study. It showed that void-free filling can be achieved in the range of 0.18-180 μm via holes and trenches by the selection of these additives.

2.2.6 Copper Electroplating Optimization for the PCB Industry

Over the pass few decades, many studies were reported based on laboratory scale investigation to evaluate the effect of different factors on copper electroplating for the PCB industry. Researchers [41-44] studied the through hole plating process of the PCB industry with statistical experimental design and empirical modeling. These studies were focused on feature scale but had shown obvious directions of process improvement in the form of a set of recommended factor settings.

Poon et al. reported the effect of various plating parameters on plating distribution [8-9, 13]. In their studies, fractional factorial and central composite designs experiments were carried out sequentially to model empirically the main effects. Possible interactions of the major process parameters on the average plating thickness and its variations in a blind via electroplating process were also reported. The effect of active current density, electrode separation, aspect ratio and the depth of the via-holes on the deposition uniformity were studied. It was identified that the significant process parameters affecting the work piece level uniformity are the average current density and the electrode separation [8]. The effect of the interaction between active current density and electrode separation is also significant to the variation of the work piece

level electrodeposition thickness [9]. Empirical models were developed in the studies to describe the effect of electrode separation, current density and active area density ratio on the deposition evenness in terms of the thickness standard deviation. The interactions between these factors were also described in their studies and reported in the models.

In a recent report by Tan and Lim [20], experiment was carried out in laboratory with experimental approach. The relationship of uniformity of electrodeposition and various factors was studied and reported. The factors involved in the study were offset voltage, bath agitation, temperature, anode-cathode separation and bath concentration. The effect of the factors were investigated and reported in a one-at-a-time basis. The research employed the wire beam electrode (WBE) which has been developed recently into a means of simulating the conventional one-piece electrode surface under electroplating and of measuring the distribution of electroplating current [21]. It was found that the offset voltage, bath agitation, temperature, anode cathode separation and bath concentration were having effects on the copper deposition evenness. Combination of the best values of each factor, however, did not provide any further improvement on the plating deposition evenness. This implied there were significant

interactions between the factors studied.

Other researches were also carried out to perform studies on the deposition behaviour of the electroplating process [77-82].

2.3 Taguchi Methodology and Development

2.3.1 Introduction to the Taguchi Methodology

The Taguchi methodology originated from Japan, introduced by G Taguchi, is a common tool employed by engineers for process enhancement/optimization. It should be seen as a very good engineering method rather than a philosophy. However, it does have a philosophical basis which is often excessively emphasized [83]. The Taguchi Method carries the major features of:

1. Pushing quality back to the design stage since quality control or statistical process control can never fully compensate for a bad design,
2. Routine optimization of product and process design prior to manufacture,
3. Initial emphasis on design not inspection (off-line),
4. To produce robust products with intrinsic quality and reliability characteristics,
5. It is a prototype methodology, primarily involving real physical prototypes,
6. Statistics is not the main point, and
7. Operational methodology with a philosophical basis – in the "loss-to-society".

The Taguchi methodology is always introduced by similar guidelines of

application. These include:

1. Brainstorming,
2. Statement of objectives,
3. Identification of factors – Control, signal, output as well as the noise factors,
4. Definition of the Signal to Noise Ratio,
5. Selection of appropriate orthogonal array, and
6. Experiment and analysis – mean response and signal to noise graphical analysis.

The orthogonal array and signal to noise analysis are the major features of the Taguchi application. The orthogonal array, a fractional factorial design, provides an experimental approach to investigate the process with a minimal number of experiments. The signal to noise ratio, which is a major source of criticism of the methods, is:

1. A performance measure to choose control levels that best cope with noise,
2. adapted to improve statistical properties, and
3. constructed so that the maximum is optimum (since intuitively we wish to maximize the signal relative to the noise) [83].

The signal to noise ratio (S/N_N) depends on the criterion for response [84]:

1. Nominal is best

$$S/N_N = 10\,Log\frac{\frac{1}{n}(S_m - V_e)}{V_e} \quad \text{.......... (7)}$$

where

$$S_m = \frac{(\sum y_i)^2}{n}, \quad \text{.......... (8)}$$

$$V_e = \frac{\sum y_i^2 - \frac{(\sum y_i)^2}{n}}{n-1} \quad \text{.......... (9)}$$

2. Smallest is best

$$S/N_N = -10\,Log\frac{1}{n}(\sum y_i) \quad \text{.......... (10)}$$

3. Biggest is best

$$S/N_N = -10\,Log(\frac{1}{n}\sum\frac{1}{y_i}) \quad \text{.......... (11)}$$

2.3.2 Progress and Case studies of the Taguchi Methodology

The rapid growth of the interest in Taguchi Methodology in Europe and United States in the 1980's has led to a great expansion in the number of published case studies [83, 84]. Conferences of the Taguchi Methods [83], for example, were held by researchers to share the experience of experimental approaches for industrial quality control. The method was applied to different industrial sectors including electronics, information technology, process industry, automotive and plastics for process improvement as early as the design stage. Many of these case studies were published as industrial journal, conference papers and technical paper collections of private companies [85 –92]

The development in the Taguchi methodology has also been taking place worldwide. In a recent study by Huang [93], he developed the classical Taguchi quality selection model to the general. The classical Taguchi method considers the case there is one input characteristic and one output characteristics and it aims at selecting the best input mean to minimize the loss of quality. Huang developed the case of there are n input characteristics and m output characteristics.

3. Research Methodology

3.1 Introduction

In order to provide an understanding of the effect of eight process factors on the copper electrodeposition behaviour, the Taguchi methodology was used. This enabled the study to be carried out with feasible number of experiments in an industrial scale. The evolutionary nature of the Taguchi DOE approach, which always allows further elaboration of subsequent DOE to be carried out based on the results of the previous, has also made hardware factor settings enhancement feasible and practical.

Although the Taguchi approach was employed, the complexity of the PCB industrial plating process was introducing limitations in the study in terms of time and resources. Experiments of the Taguchi DOE were carried out with both substrates (PCB) with and without pattern – namely the pattern and panel electroplating respectively. Analysis was focused on the panel plating result while the pattern plating result was regarded as a control or reference. A second Taguchi DOE was setup based on the result of the first one. A total of 58 industrial experiments were carried out

3.2 Taguchi experiment setup

A seven three levels and one two levels factors DOE was set up according to Taguchi method. The $L_{18}(2^1x3^7)$ experimental set was set up in which a total of eight factors can be examined at the same time. The $L_{18}(2^1x3^7)$ matrix was listed in table 1 for reference. A total of 18 experiments would be done for each DOE set to study the effect of the eight factors on copper plating quality and efficiency.

The upper, (nominal) and lower levels of each parameters were listed in table 2. The DOE were repeated with two sets of cathode substrates including:

1. Substrates (PCBs, panel plating) without pattern
2. Substrate (PCBs, pattern plating) with circuitry design which are subjected to a larger deposition thickness variation based on mass production experiences.

Result analysis was based primarily on substrates without pattern to minimize any current crowding effect for simplicity. Control experiments were carried out with the substrates with pattern from an industrial point of view. While optimizing the hardware factors with the DOE with substrate without pattern, the general industrial specification should be met for both types of substrate. This ensured a requested minimal throwing power to be achieved, thus adequate copper thickness in through

hole from the industrial point of view.

The second set of Taguchi experiment was carried out based on the finding of the first set of DOE result. In the second set of experiment, hardware factors that could be modified in practice were analyzed. A DOE of 4 factors, two level of each were layout by a $L_8(2^4)$ Taguchi orthogonal matrix (Table 3).

Experiment was repeated with the optimized hardware setting for verification, and simulation experiment with production hardware setting were also carried out for reference. This provided a verification, comparison and contrast of the plating performance before and after the hardware factors optimization.

3.2.1 Definition of Hardware Factors

The hardware factors examined in the experiment are:

1. Anode cathode distance: the distance between the center line of anode bar (anode baskets) and that of the cathode bar (PCB).
2. Anode distribution: the distance or spacing between each pair of adjacent anode baskets along the anode bar.
3. Relative anode cathode dimension: the ratio of the length of anode basket to the length of the PCB. Since the length of anode baskets was fixed, PCBs of different length were used in the experiment.
4. Anode geometry: the shape of the copper pallets. Copper pallets of shape that are commonly available in the market were used in the experiment.
5. Oscillation velocity of cathode: the oscillation frequency of cathode bar along the direction of the bar.
6. Eductor orientation: the perpendicular vertical angle of the eductor jet that hit the PCB plane.
7. Eductor flow rate: the flow rate of electrolyte that pumped through and magnified by the eductors.

8. Current density: the computer controlled current density of the plating equipment

3.2.2 Choice of Process Factors for the experiment

Although the Taguchi method was employed in the project to study the multi-factor nature PCB copper electroplating process, only eight process factors were chosen due to the limitations of the experimental set up and the project duration. These eight factors were reported to have significantly effect on copper thickness distribution and could be controlled in the newly designed industrial plating system. The total number of experiments carried out based on the eight process factors was 58. Pulse plating parameters (such as current waveform and duty cycle) are known to be other important factors affecting the plating quality, but the number of experiments will be increased tremendously if they are considered, and it is unable to finish the experiments within the project period. Eductor agitation is also an important factor affecting the quality of plating deposition, and there are continuous research efforts in the PCB manufacturing industry to improve the eductor design. In this project, the design of the new industrial tank only allows the change of eductor orientation at the bottom of the plating tank and the flowrate. A new plating tank must be designed if

other eductor agitation parameters have to be studied.

Factor	A	B	C	D	E	F	G	H
1	A1	B1	C1	D1	E1	F1	G1	H1
2	A1	B1	C2	D2	E2	F2	G2	H2
3	A1	B1	C3	D3	E3	F3	G3	H3
4	A1	B2	C1	D1	E2	F2	G3	H3
5	A1	B2	C2	D2	E3	F3	G1	H1
6	A1	B2	C3	D3	E1	F1	G2	H2
7	A1	B3	C1	D2	E1	F3	G2	H3
8	A1	B3	C2	D3	E2	F1	G3	H1
9	A1	B3	C3	D1	E3	F2	G1	H2
10	A2	B1	C1	D3	E3	F2	G2	H1
11	A2	B1	C2	D1	E1	F3	G3	H2
12	A2	B1	C3	D2	E2	F1	G1	H3
13	A2	B2	C1	D2	E3	F1	G3	H2
14	A2	B2	C2	D3	E1	F2	G1	H3
15	A2	B2	C3	D1	E2	F3	G2	H1
16	A2	B3	C1	D3	E2	F3	G1	H2
17	A2	B3	C2	D1	E3	F1	G2	H3
18	A2	B3	C3	D2	E1	F2	G3	H1

Table 3.1 Taguchi DOE $L_{18}(2^1x3^7)$ Matrix

Factors	Level		
	1	2	3
A. Anode Geometry	A1 – Spherical	A2 – cylindrical	/
B. Anode Distribution	B1 – 2"	B2 - 3"	B3 - 4"
C. Anode Cathode Distance	C1 –12"	C2 - 13"	C3 – 14"
D. Relative Anode-cathode Dimension	D1 - 23.5"/20"	D2 - 23.5"/22"	D3 - 23.5"/24"
E. Oscillation Velocity	E1 – 10 cycles/min	E2 – 12 cycles/min	E3 – 14cycles/min
F. Eductor Orientation	F1 – 0°	F2 - (7.5°)	F3 – 15°
G. Eductor Flow rate	G1 – 50 gal/min	G2 – 60 gal/min	G3 – 70 gal/min
H. Current Density	H1 - 13ASF	H2 - 18ASF	H3 - 23ASF

Table 3.2 Parameter levels summary

	Anode Distribution	Cathode Oscillation Velocity	Eductor Orientation	Eductor Flow rate
1	B1	E2	F1	G2
2	B1	E2	F1	G3
3	B1	E3	F2	G2
4	B1	E3	F2	G3
5	B2	E2	F2	G2
6	B2	E2	F2	G3
7	B2	E3	F1	G2
8	B2	E3	F1	G3

Table 3.3 Taguchi $L_8(2^4)$ Matrix

3.3 Experimental setup

Experiments were carried out in the copper electroplating line in Topsearch Printed Circuit (Shenzhen) Ltd. The plating line (Figure 3.1) was manufactured by Protek Technology Ltd. and the production line is equipped with the Dutch Reverse Pulse Rectifiers (Figure 3.2). The cross section design drawing of the electroplating cell is also presented in Figure 3.3.

The experiments were carried out with MacDermid pulse plating chemical PPR1 and the bath components were maintained and measured according to the specification of the chemical from MacDermid in Topsearch.

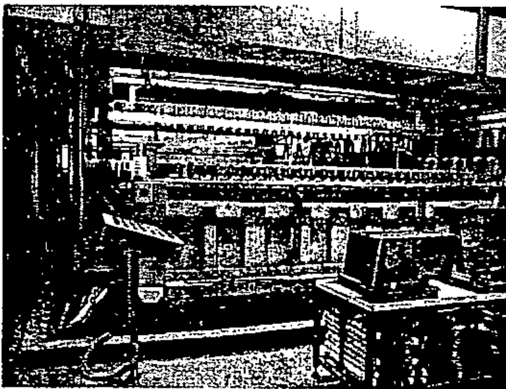


Figure 3.1 The Protek Pulse Plating line

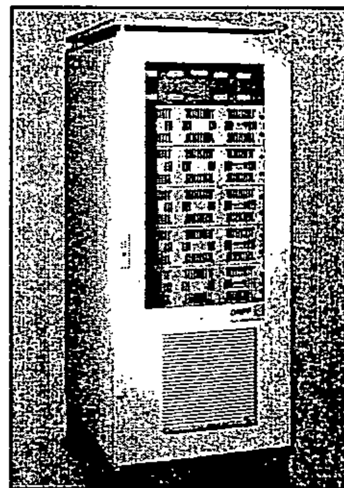


Figure 3.2 Dutch Reverse Pulse Plating Rectifier

The chemical bath was processed with carbon treatment to remove organic chemical by-products for every 54 experiments, or on a weekly basis, whichever

come first.

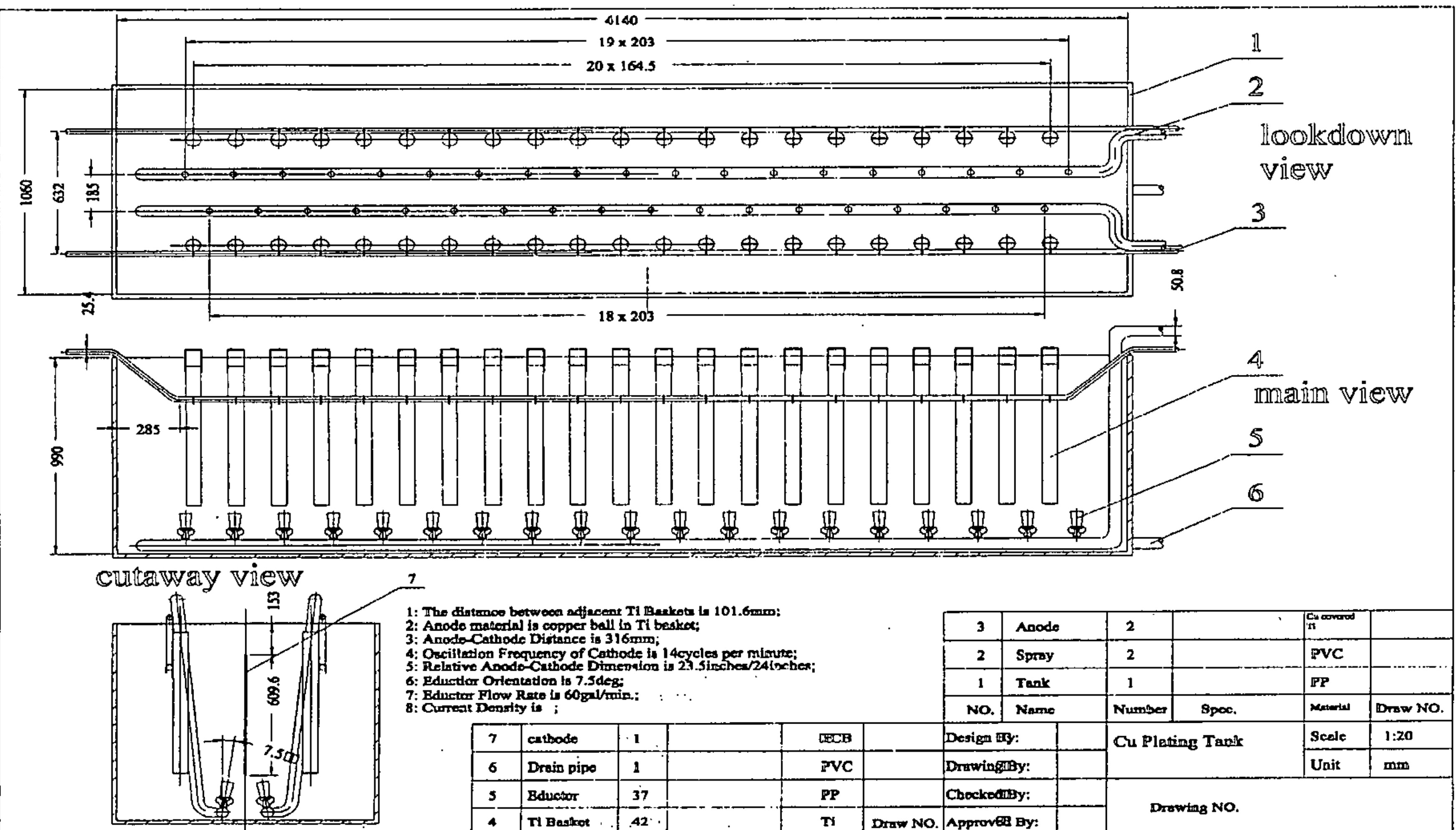
The experimental copper electroplating tank was designed and integrated at the end of the production line in such a way that:

1. The position of the anode bar can be manually relocated; Marking was used on the tank walls in order to define the anode-cathode distance.
2. The anode baskets attached on the anode bar can be manually relocated for testing different anode distribution/separation along the anode bar.
3. The two series of eductors at the bottom can be adjusted in a planar rotational motion to provide different emerging angle of chemical 'jets' from the eductors to the cathode.
4. A pump with adjustable flow rate was installed and connected to the eductors to provide different eductor flow rates, and flow-meters were connected to the eductors to measure the eductor flow rate.
5. Frequency controller was installed to the motor responsible for cathode oscillation to vary the cathode oscillation velocity.

Both micro-sectioning and Coating Measuring Instrument (CMI, Model CMI 500 series) technique were employed to collect deposition thickness data. Three

cross sections at the top, middle and bottom of each panel were carried out to measure the copper deposition thickness. The copper thickness data obtained from cross section analysis was used primarily in the study while the CMI data was collected for reference. Hole wall copper thickness data was also collected in order to provide a reference from industrial process point of view. The cross sections were inspected and measurements were taken with a Leica microscope (Model DMIRM) with 25 to 200x magnification, equipped with measuring software (DC100 and IM50).

Figure 3.3 Drawing of the Plating Tank



4. Result

Although the Taguchi methodology was employed for the study, the number of experiments carried out was large because a total of eight process factors were studied together. In order to provide a better understanding and validity, the evolution nature of the Taguchi method was employed and the investigation was divided into two different phases

4.1 Enhancement of Plating Process Factors with Taguchi Methodology – Phase I

4.1.1 Taguchi Mean Response Analysis

The effect of each factor could be more clearly investigated and reported by the mean response analysis according to the Taguchi methodology. The mean response of the hardware factors in the experiment was studied according to the standard deviation of the thickness across the cathode (PCB substrates) bar. The mean response of each factor was resulted from the average of the respond of the sample factor levels under the same experimental conditions.

4.1.1.1 Anode Geometry

It was found from the experiment that the two different anode geometries levels were having a significant effect on the deposition evenness (Figure 4.1). Spherical copper pallets in anode basket for electroplating resulted in a smaller standard deviation of deposition thickness. The mean response standard deviation was improved from 0.2585 to 0.2374 mil when spherical copper pallets were used instead of hemi-spherical copper pallets as the anode material.

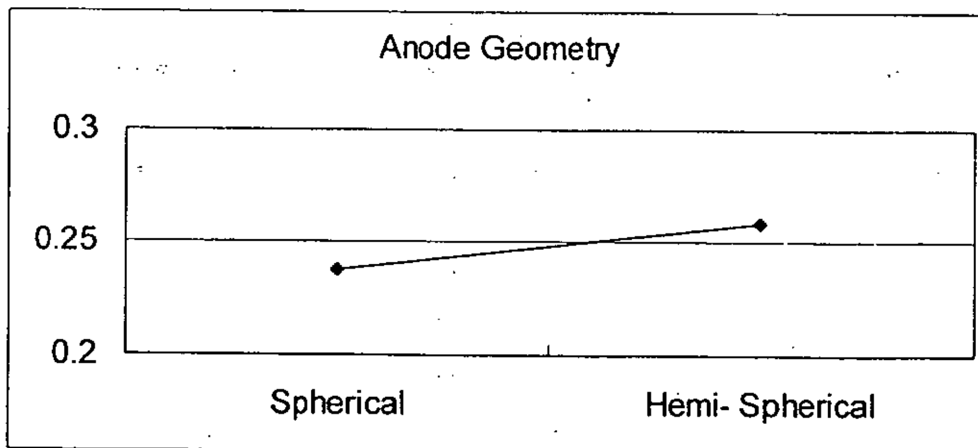


Figure 4.1 Mean Response of Hardware Factor – Anode Geometry

4.1.1.2 Anode Distribution

It was found from the experiment that the mean response of anode distribution differed significantly between the factor levels. The best response was located at when the anode baskets were distribution by 2 inches from each other. The mean standard

deviation was reduced from about 0.5mil when 3 and 4 inches anode basket separation were used to 0.2085mil when the anode basket separation was reduce to 2 inches (Figure 4.2).

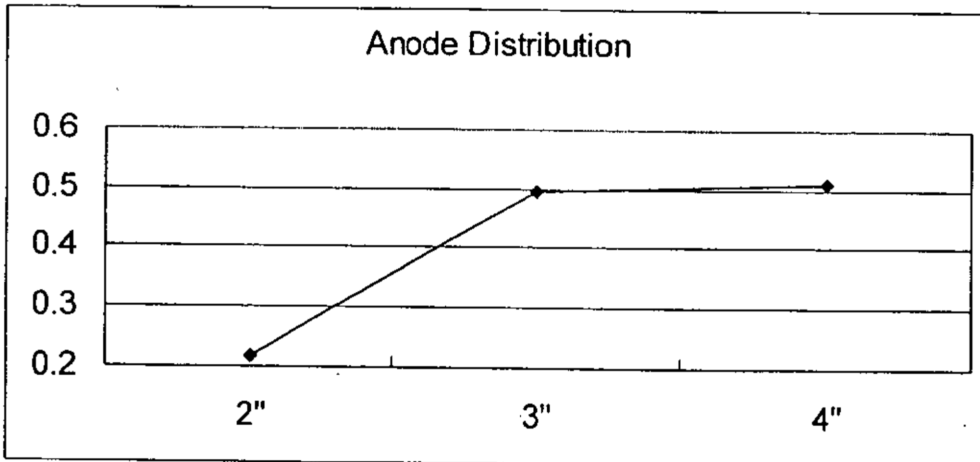


Figure 4.2 Mean response of hardware factor – Anode Distribution

4.1.1.3 Anode Cathode Distance

It was found from the experiment that the smallest mean standard deviation of deposition thickness was located when the anode-cathode distance was at 12.44 inches (316mm) (Figure 4.3). This was a setting which is very close to that of the mass production 12.99 inches (330mm). The smallest standard deviation was 0.2085mil when the anode-cathode distance was set at 12.44 inches (316mm). The standard deviation then increased to 0.2342mil when the distance increased to 366mm. It decreased back to 0.2185mil when the distance was further increased to 416mm.

This was very interesting since it was believed commonly in the industry that deposition evenness can be improved when the distance between anode and cathode increases.

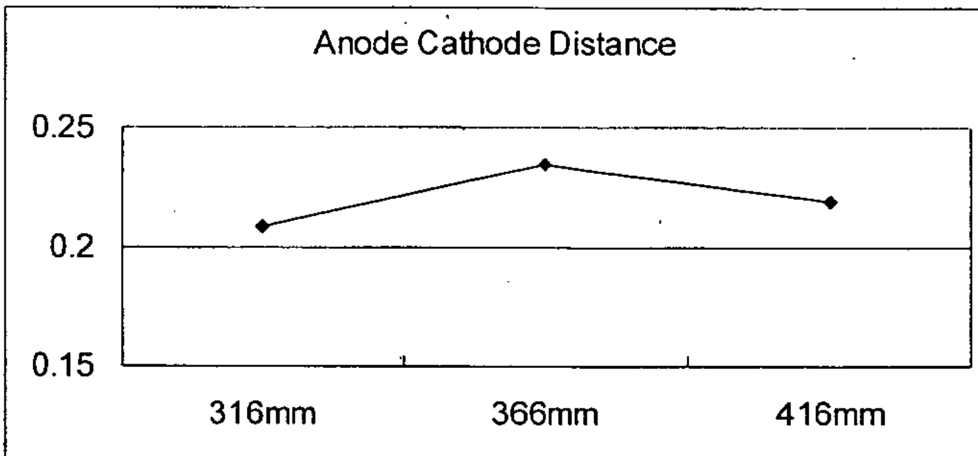


Figure 4.3 Mean response of hardware factor – Anode Cathode Distance

4.1.1.4 Relative Anode Cathode Dimension

It was found from the experiment that when the length of cathode was similar to that of the anode, the mean response standard deviation of deposition thickness was the smallest among the three different settings. The standard deviation of deposition thickness decreased from about 0.25mil to0.2033mil when the length of the cathode was increasing and approaching the length of the anode.

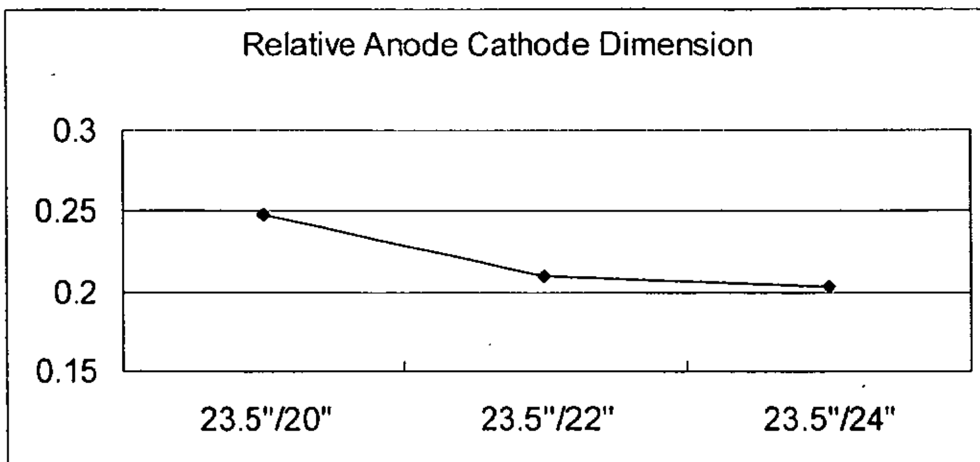


Figure 4.4 Mean response of hardware factor – Relative Anode Cathode Dimension

4.1.1.5 Cathode Oscillation Velocity

It was found from the experiment that an optimal point was located when the oscillation velocity of the cathode bar was at 12 cycles/min. However, the differences between the three mean standard deviations were not significant. The smallest standard deviation when the oscillation velocity was at 12 cycles/min was 0.2137 mil while the maximum found among the three settings was 0.2248mil.

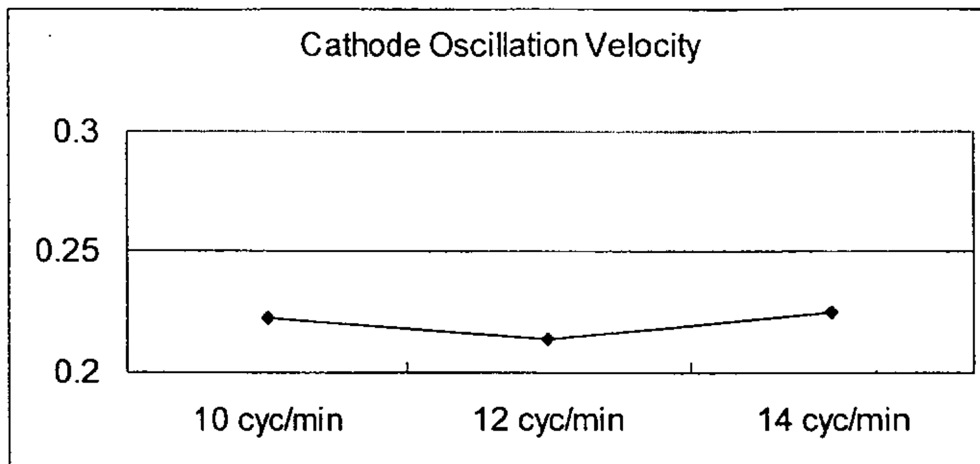


Figure 4.5 Mean response of hardware factor – Cathode Oscillation Velocity

4.1.1.6 Eductor Orientation

It was found from the experiment that when the perpendicular emerging angle of the eductor jet to the cathode was set at 0 degree, the mean standard deviation of deposition thickness was the smallest. The smallest deviation value at 0 degree was found to be 0.2048mil. The standard deviation increased while the emerging angle to the cathode increased. The mean response deposition thickness standard deviation at 15 degree was 0.2308mil.

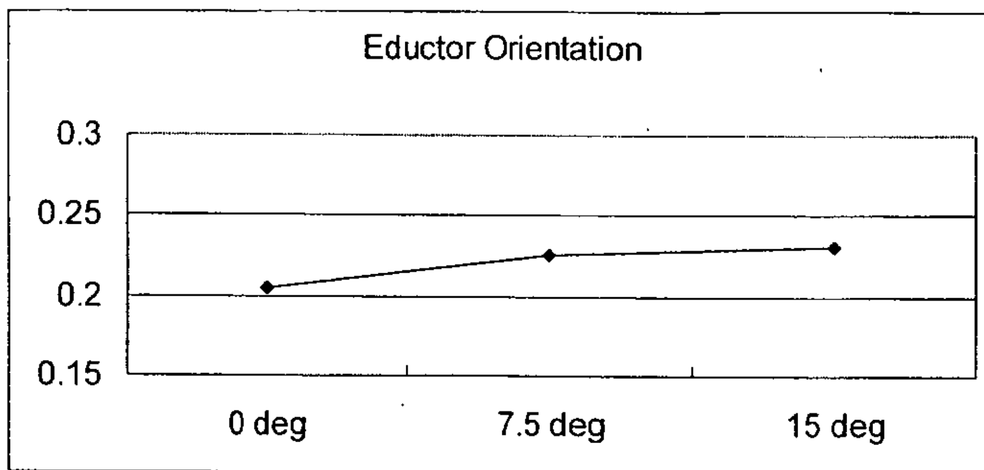


Figure 4.6 Mean response of hardware factor – Eductor Orientation

4.1.1.7 Eductor Flowrate

It was found from the experiment that there was no significant difference in the deposition thickness standard deviation responses between the three different flow rate settings. The three standard deviation mean responses ranged from 0.2180mil to 0.2235mil and the minimum was located when the flow rate was set at 60 gal/min. According to the Taguchi methodology, the optimized eductor flow rate setting was chosen to be the smallest standard deviation response of deposition thickness at 60gal/min. (Figure 4.7)

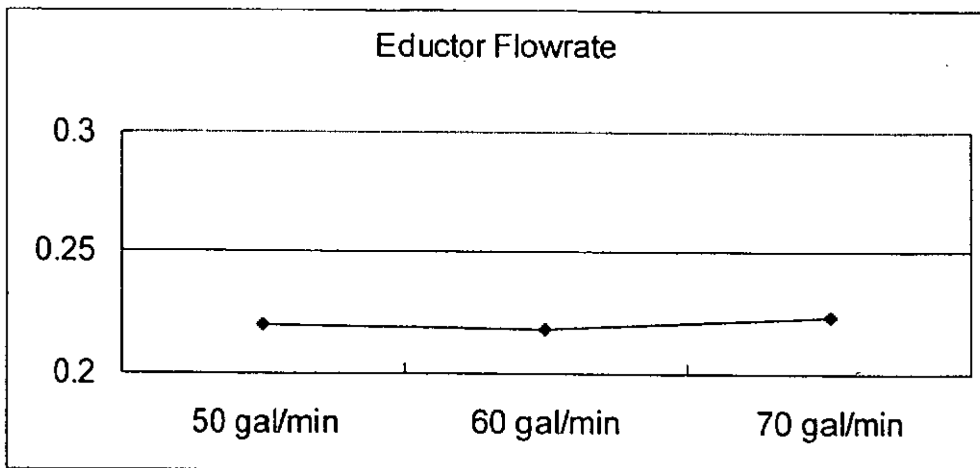


Figure 4.7 Mean response of hardware factor – Eductor Flow Rate

4.1.1.8 Current Density

It was found from the experiment that the mean responses of different current densities were significantly different. The smallest standard deviation was obtained at when 13ASF was used. The mean response standard deviation increased when the current density increased, and they were reported as 0.1491mil, 0.2023mil and 0.3097mil when 13ASF, 18ASF and 23ASF were used respectively (Figure 4.8).

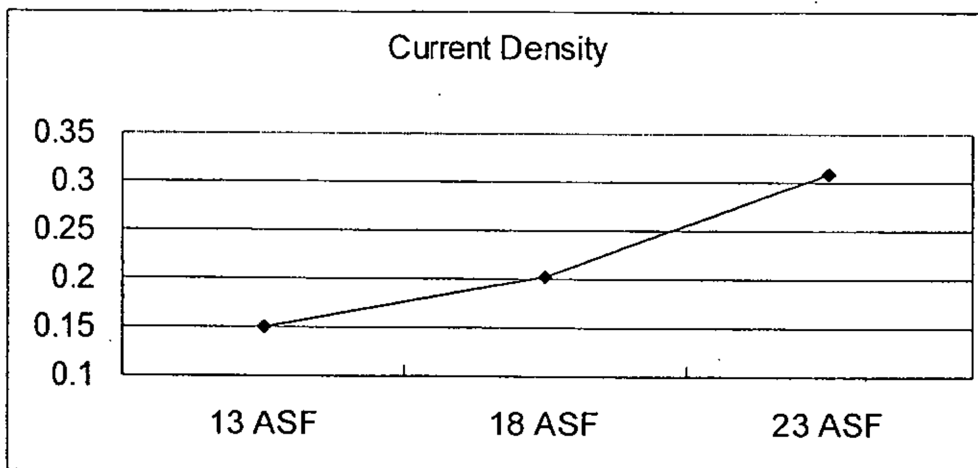


Figure 4.8 Mean response of factor – Current Density

Among the factors investigated in the experiment, only current density and the anode distribution showed significant differences in the mean responses between the studied levels. In most of the mean response analysis, it could be seen graphically that the upper and lower limit of the factors did not provide wide enough coverage to demonstrate the optimum response. It was also observed that for some factors, eductor flow rate for example, the mean responses over the levels investigated did not show a statistically meaningful difference. These have to be further verified.

4.1.2 Enhanced Hardware settings

According to the L_{18} orthogonal array (Table 3.1) and the corresponding mean response analysis, it was found from the experiment (Table 4.1) that three of the hardware settings according to the production setup in the electroplating tank agreed with the enhanced settings. A total of 42 experiments were carried out in the first phase of Taguchi analysis – The L_{18} Taguchi DOE to locate the enhanced hardware settings and current density for panel and pattern plating. The result of the enhancement was repeated for verification in terms of copper deposition evenness. As a control, experiment with the hardware setting employed in mass production was also carried out and repeated.

A comparison of the enhanced and recent production setting is listed is table 4.

	A. Anode geometry	B. Anode distribution	C. Anode Cathode distance	D. Relative anode-cathode dimension	E. Cathode oscillation velocity	F. Eductor orientation	G. Eductor flow rate	H. Current density
Optimized (From L_{18})	A1 Spherical	B1 (2")	C1 (316mm)	D2 (23.5"/24")	E2 (12cyc/min)	F1 (0.0°)	G2 (60gal/min)	H1 (13ASF)
Current production condition	A1 Spherical	B2 3"	330mm	Production Panel size	E2 12cyc/min	F2 7.5°	G3 70gal/min	H3/H1 23/13ASF

Table 4.1 Comparison of Recent production and Enhanced Process Setting for Copper Electroplating tanks.

The enhanced factors found from the experiments that were different from the

recent mass production setting were anode distribution, eductor orientation and eductor flow rate. Form the result of the first DOE, it was found that the copper deposition evenness over the cathode surface can be improved by modifying the recent production settings. The deposition thickness from the enhanced hardware setting was found more evenly distributed along the cathode bar in terms of the standard deviation of the deposition thickness. The standard deviation of the deposition thickness were improved from 0.1470mil to 0.1315mil by 1.3%

	Average Thickness Variation		Average Thickness	Improvement
	Production Setting	Enhanced Setting		
Std Deviation	0.1470	0.1315	1.196	1.3%

Table 4.2 Comparison of Deposition Evenness between Recent Production and Enhanced Hardware Settings

It is worth mentioning that according to the PCB structure, the bonding strength of copper-copper interface would always be much larger than that of the copper-epoxy interface. After the hardware modification, the change of mechanical properties in the electroplated copper would not play a significant effect in the PCB reliability in the range of factor settings. It might be interesting to study the microscopic changes of the copper deposition before and after the hardware modification.

4.2 Plating Performance of Enhanced Hardware Settings under Different Current Densities

Although the enhanced current density was found to be the lower limit of the levels (13ASF), experiments were repeated with the higher current density – 23 ASF in order to provide a more valid result from mass production point of view. The result of deposition evenness is listed in table 4.3a and 4.3b. The deposition behavior was compared with the recent production (table 4.4a and 4.4b) and enhanced hardware settings with both 13ASF and 23ASF. Example of the cross section photos from the processes with two different current densities were shown in figure 4.9a – f

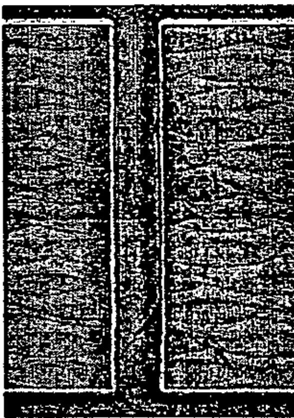


Figure 4.9a

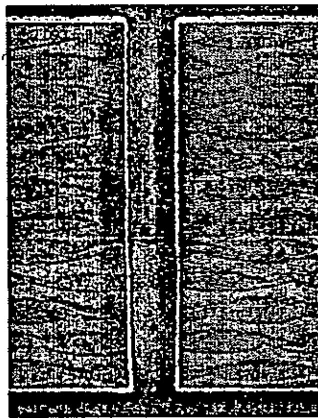


Figure 4.9b

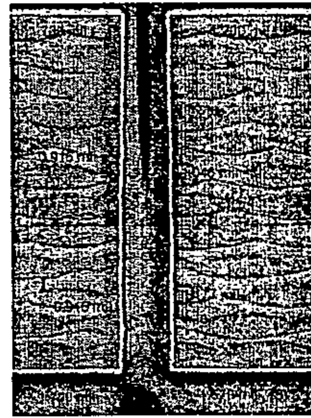


Figure 4.9c

Figure 4.9a – c Example of cross section photos from experiments with 23ASF

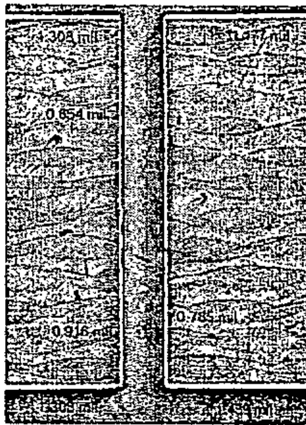


Figure 4.9d

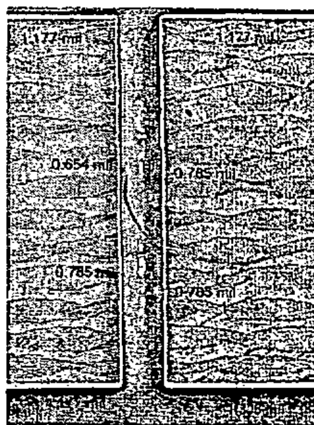


Figure 4.9e

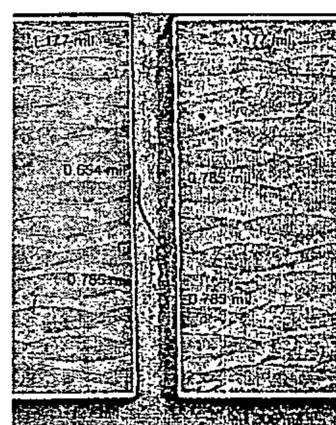


Figure 4.9f

Figure 4.9d – f Example of cross section photos from experiments with 13ASF

Interestingly, it was found from this elaboration experiment that with the enhanced hardware settings, improvement of deposition evenness was observed on both cases when 13 and 23ASF current density were applied. The comparison of deposition thickness standard deviation was listed in table 4.5. With the enhanced hardware settings, an improvement up to 4.3% in deposition thickness standard deviation was achieved when a current density of 23 ASF was used.

First Trial – Enhanced Setting

	Anode Geometry	Anode distribution	Anode cathode distance	Relative anode cathode dimension	Cathode oscillation velocity	Eductor orientation	Eductor flow rate	Current density	Average thickness	Deviation across cathode	Standard Deviation	Average deviation within panel
1	A1	B1	C1	D3	E2	F1	G2	H1 - 13ASF	1.176	0.4	0.143	0.324
2	A1	B1	C1	D3	E2	F1	G2	H3 - 23 ASF	1.693	0.789	0.273	0.628

Thickness Variation (Stdev)		
13ASF	Across Cathode	0.143
23ASF	Across Cathode	0.217

Table 4.3a Comparison of Deposition Behavior with Enhanced Hardware Settings with 13 and 23 ASF Current Density – Trial 1

Second Trial – Enhanced setting

	Anode Geometry	Anode distribution	Anode cathode distance	Relative anode cathode dimension	Cathode oscillation velocity	Eductor orientation	Eductor flow rate	Current density	Average thickness	Deviation across cathode	Standard Deviation	Average deviation within panel
1	A1	B1	C1	D3	E2	F1	G2	H1 - 13ASF	1.202	0.452	0.119	0.355
2	A1	B1	C1	D3	E2	F1	G2	H3 - 23 ASF	1.711	0.766	0.295	0.713

Thickness Variation (Stdev)		
13ASF	Across Cathode	0.12
23ASF	Across Cathode	0.295

Table 4.3b Comparison of Deposition Behavior with Enhanced Hardware Settings with 13 and 23 ASF Current Density – Trial 2

1st Trial - Production setting

	Anode Geometry	Anode distribution	Anode cathode distance	Relative anode cathode dimension	Cathode oscillation velocity	Eductor orientation	Eductor flow rate	Current density	Average thickness	Deviation across cathode	Standard Deviation	Average deviation within panel
1	A1	B2	C1	D3	E1	F2	G3	H1 - 13ASF	1.198	0.49	0.141	0.306
2	A1	B2	C1	D3	E1	F2	G3	H3 - 23 ASF	1.747	0.99	0.308	0.704

Thickness Variation		
13ASF	Across Cathode	0.141
23ASF	Across Cathode	0.308

Table 4.4a Comparison of Deposition Behavior with Production Hardware Settings with 13 and 23 ASF Current Density – Trial 1

2nd Trial – Production setting

	Anode Geometry	Anode distribution	Anode cathode distance	Relative anode cathode dimension	Cathode oscillation velocity	Eductor orientation	Eductor flow rate	Current density	Average thickness	Deviation across cathode	Standard Deviation	Average deviation within panel
1	A1	B2	C1	D3	E1	F2	G3	H1 - 13ASF	1.206	0.47	0.153	0.312
2	A1	B2	C1	D3	E1	F2	G3	H3 - 23 ASF	1.812	0.877	0.352	0.771

Thickness Variation		
13ASF	Across Cathode	0.153
23ASF	Across Cathode	0.352

Table 4.4b Comparison of Deposition Behavior with Production Hardware Settings with 13 and 23 ASF Current Density – Trial 2

	Average Thickness Variation		Average Thickness	Improvement
	Production Setting	Optimized Setting		
13ASF	0.1470	0.1315	1.196	1.3%
23ASF	0.3300	0.2560	1.741	4.3%

Table 4.5 Comparison of deposition evenness for production and enhanced setting

4.3 Process Factor Enhancement – Taguchi Analysis Phase II

In order to provide a better understanding and verification of the DOE result obtained from the first phase, a second DOE was carried out. A total of sixteen experiments were carried out to verify the enhanced hardware setting while only four hardware factors were investigated with both pattern and panel plating.

4.3.1 Enhanced Hardware settings for Pattern Plating from First DOE

As a control experiment, the enhanced hardware settings for the pattern plating were also located. According to the mean response analysis, some of the hardware settings were different from that of the optimum found from the panel plating experiment. The enhanced setting of the L_{18} experiment for pattern plating was listed in table 4.5 for reference.

L_{18} DOE	A. Anode geometry	B. Anode distribution	C. Anode Cathode distance	D. Relative anode-cathode dimension	E. Cathode oscillation velocity	F. Eductor orientation	G. Eductor flow rate	H. Current density
Panel Plating	A1 Spherical	B1 (2")	C1 (316mm)	D2 (23.5"/24")	E2 (12cyc/min)	F1 (0.0°)	G2 (60gal/min)	H1 (13ASF)
Pattern Plating	A1 Spherical	B2 (3")	C1 (316mm)	D2 (23.5"/24")	E3 (14 /min)	F2 (7.5°)	G2 (60gal/min)	H1 (13ASF)

Table 4.6 Comparison of Enhanced Process Factors of Panel and Pattern Plating from DOE Phase I

It is also important to realize that although the current density of 13 ASF was recognized as one of the optimal settings, it did allow enough copper deposition to be built up within the time (60min) of the plating cycle used in the experiment (mass production electroplating program). In the PCB industry, the 13ASF plating program will usually follow with additional pattern plating. The reason for the combined plating process is out of the scope of this study.

4.3.2 Comparison of the Enhanced Hardware Settings from Phase I & II

The result from the first L_{18} Taguchi was further elaborated. The enhanced hardware settings of the pattern plating and panel plating were compared. Four of the hardware settings were found different from the first phase Taguchi DOE with panel

and pattern plating process. These four factors were chosen for further study while the other factors were kept constant based on the enhancement resulted from the L_{18} matrix. The enhanced hardware settings of the result of the second phase DOE (L_4 matrix) was listed in table 4.7

	A. Anode geometry	B. Anode distribution	C. Anode distribution	D. Relative anode-cathode dimension	E. Cathode oscillation velocity	F. Eductor orientation	G. Eductor flow rate	H. Current density
Second Phase DOE	A1 Spherical	B2 3"	C1 (316mm)	D3 (23.5"/24")	E3 14/min	F2 7.5°	G2 (60gal/min)	H1 (13ASF)
First Phase DOE	A1 Spherical	B1 2"	C1 (316mm)	D3 (23.5"/24")	E2 12/min	F1 0°	G2 60gal/min	H1 (13ASF)

Table 4.7 Comparison of Enhanced hardware settings from First and Second Phase Taguchi DOE

It was found from the second Taguchi matrix that some of the hardware settings were different from those reported from the first DOE. The enhanced anode distribution was found at 3" from the second phase DOE instead of 2" from the first phase. A higher cathode oscillation velocity at 14 cycles/min was also reported instead of 12cycles/min. The best response of eductor orientation was found at 7.5 degree instead of 0 degree. The mean responses of thickness deposition standard deviation were showed in Figure 4.9-4.12.

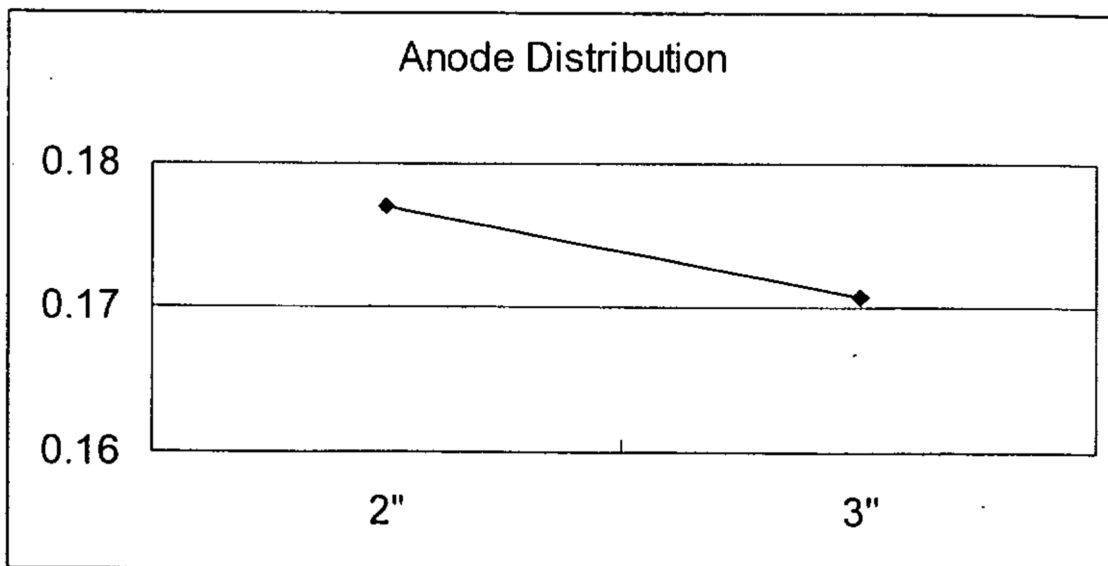


Figure 4.10 Anode Distribution Mean Response of L_8 DOE

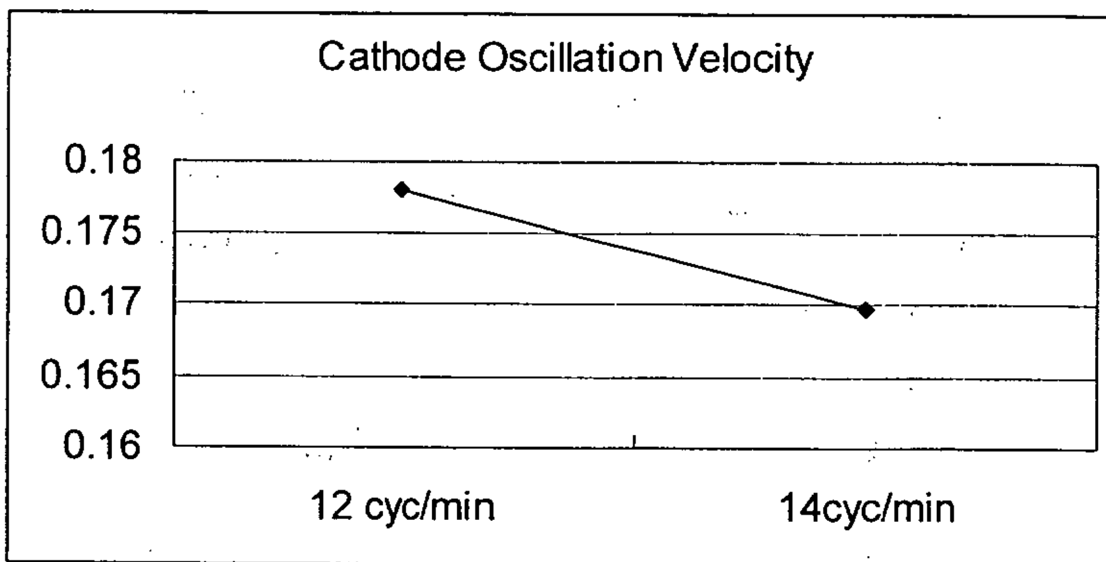


Figure 4.11 Cathode Oscillation Velocity Mean Response of L_8 DOE

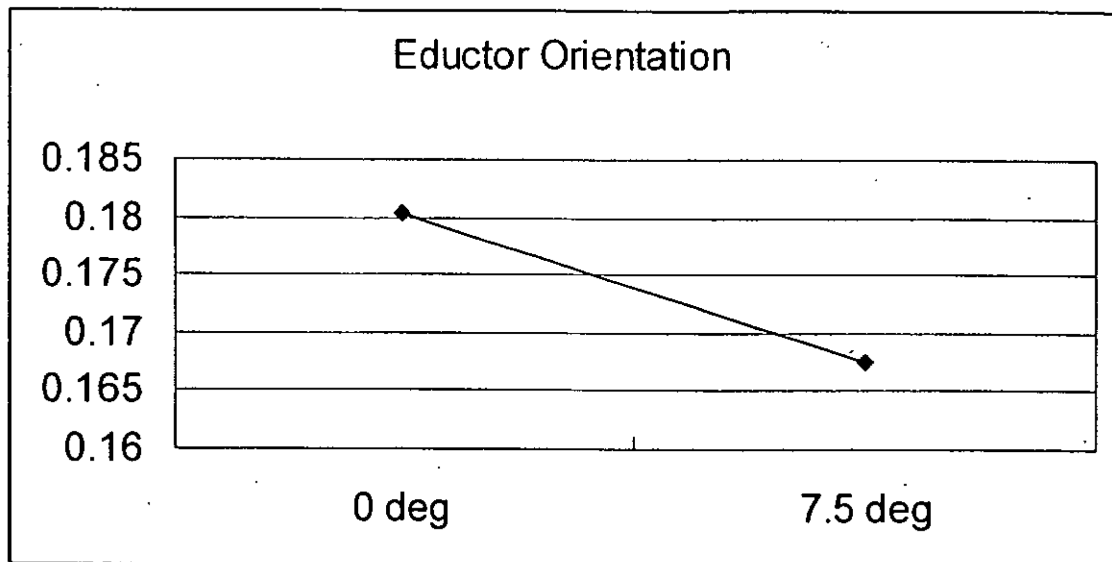


Figure 4.12 Eductor Orientation Mean Response of L_8 DOE

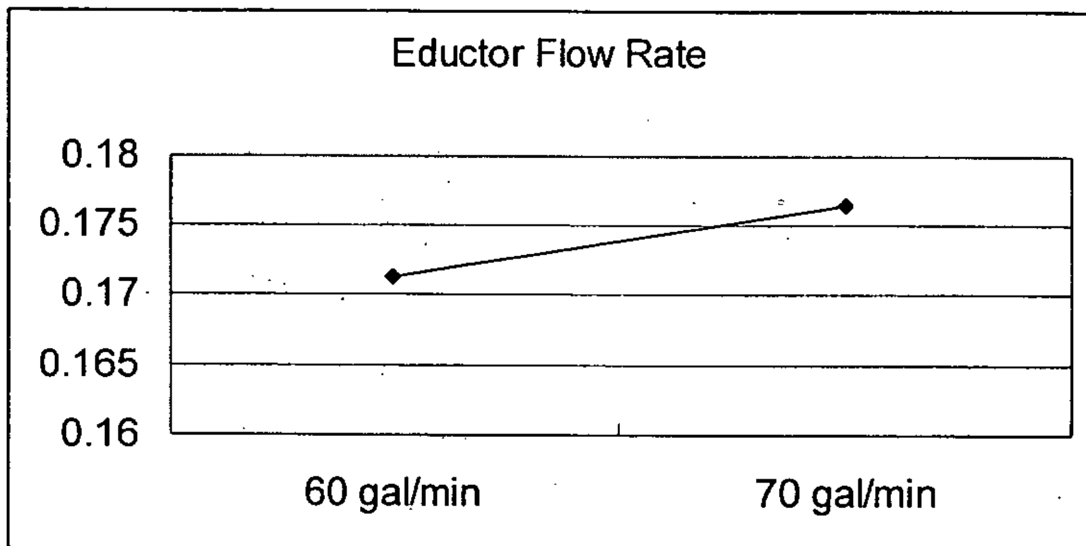


Figure 4.13 Eductor Flow Rate Mean Response of L_8 DOE

5. Discussion

5.1 Hardware factors and Current density

It was observed from the enhanced hardware settings of the L_{18} Taguchi DOE that the deposition thickness distribution was improved. The best current density found in the DOE was at the lower limit over the test range in terms of copper deposition evenness. This agrees with the general believes and experiences from within the PCB industry as well as the finding by Poon et al [9, 13] and Tan and Lim [20]. As predicted from the modeling by Poon et al, a lower current density would result in a lower work-piece-level variability. Tim and Lim also reported the smallest standard deviation of deposition when the lowest current setting when a -40mV of offset voltage was applied.

Interestingly, it was found from the L_{18} experiment that the improvement of the deposition evenness from the enhanced hardware setting applied to both current density of 13 and 23ASF. This showed that the enhancement of hardware settings was having a dominant, or at least an equivalent effect on plating distribution to that of current density. This agrees with the finding of Tan and Lim [20] that both hardware factors and current density (anode cathode separation, bath agitation and

offset voltage) are critical and have significant effect on the uniformity of electro-deposition.

In the modeling by Poon et al [9, 13] electrode separation was also included and found to be one of the major factors affecting the work-piece level variability. According to the model [9], electrode separation is having a positive effect while the current density is negative on the standard deviation of the deposition thickness. The interaction between the two factors will also increase the standard deviation on deposition thickness. According to the model [9]:

$$SD = 1.6573 - 0.0982C + 0.3667D - 0.1887C^2 + 0.7386D^2 + 0.5573CD \qquad (12)$$

where SD – Standard deviation

C – Current Distribution

D – Electrode separation

The result from the L_{18} agrees with the fact that there are interactions between hardware factors based on previous researches.

5.2 Difference in Deposition Behaviour between Pattern Plating and Panel Plating

5.2.1 Enhancement of factors – Taguchi Analysis Phase I

The enhanced hardware settings for panel plating and pattern plating were found different in the L_{18} experiment. This implies that the conductor feature design on the cathode surface is having a significant effect on the behaviour of copper deposition on the cathode. This agrees with the finding by Poon et al. [13]. The active area density and its ratio were studied and were found to have a significant effect on the thickness variability.

According to the studies by Poon et al. [13], interaction factors were also built into the models. These interactions include the electrode separation and current density (equation 13) as well as the feature design- active area density ratio of PCB, electrode separation and current density. According to the model:

$$\sigma = 6.1565 + 1.7857ACD + 0.3492ES + 1.8303AADR + 0.7091ACDxES + 0.188ACDxAADR - 0.1483ESxAADR + 0.0871ACDxESxAADR \quad (13)$$

where σ = Standard deviation of deposition thickness

ACD = Average Current Density

ES = Electrode Separation

AADR = Active Area Density Ratio

Verification of the model was carried out with the enhanced settings of this research where the current distribution was equal to 13ASF (13.993 mA/cm^2) and the electrode separation was 316mm (31.6cm). The standard deviation obtained from equation 12 was 178.61µm or 7.032mil. This was not in agreement with the observation from the experimental results. The deviation of deposition thickness on the surfaces or within the through holes was always much less than that found from the experiment. Sample cross sections photos from this study were showed in figure 5.1a – 5.1f. The deviation predicted from the model by Poon et al. is much larger than the reported value in the study.

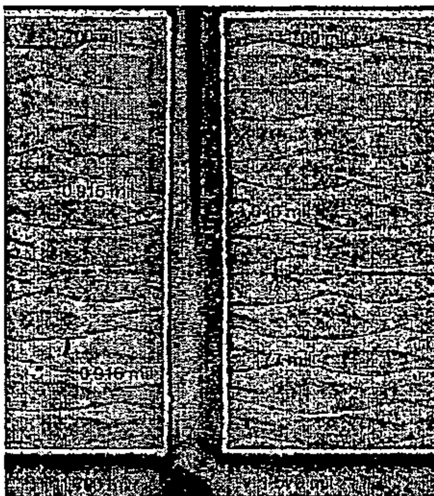


Figure 5.1a

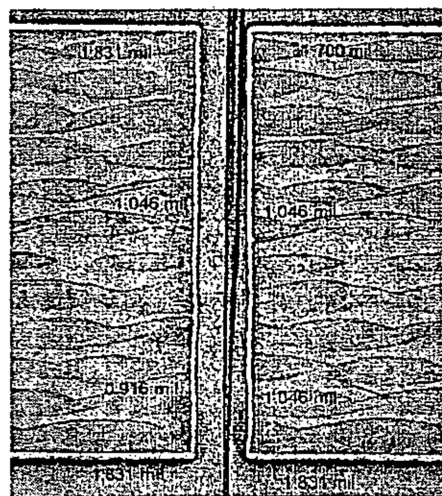


Figure 5.1b

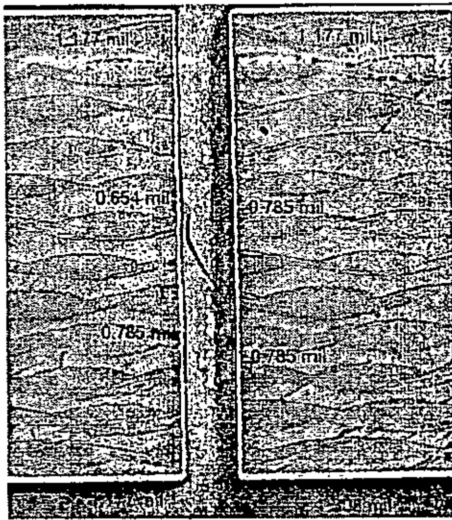


Figure 5.1c

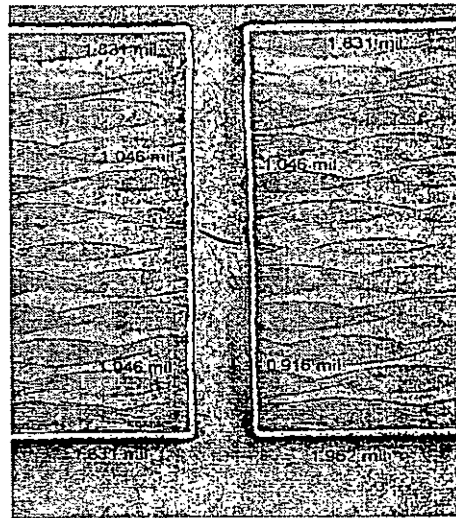


Figure 5.1d

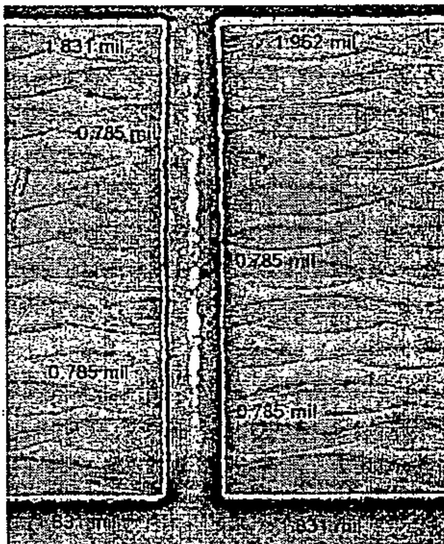


Figure 5.1e

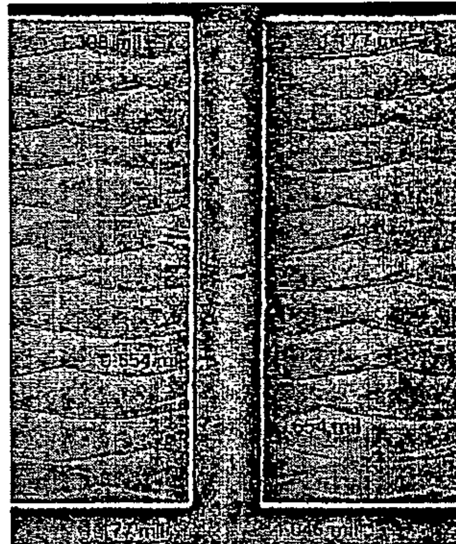


Figure 5.1f

Figure 5.1a-5.1f. Sample Cross Section Photos from DOE experiment

The major deviation of the model was introduced by the large electrode separation (31.6cm) adopted in this study which has significantly increased the SD of the model prediction. This implies that the model (equation 12) may not be well applied to a traditional industrial scale electroplating process in which the electrode

separation is usually larger than 25.4cm. Another possible factor leading to the breakdown of the model was the deposition thickness. It is common in the industry that a minimum of 0.7mil (18 μm) of copper should be deposited onto the wall of through holes. Poon et al did not specify the deposition thickness domain in which the model (equation 12) would be valid. The contradiction of the model from Poon et al with the result of this research also implies that the interactions of different hardware factors could possibly be different in different ranges.

5.2.2 Enhancement of Factors – Taguchi Analysis Phase II

The result from the second Taguchi optimization (L_8) did not agree with the result from the first (L_{18}). The experiment of the second DOE was carried out with only four factors. The four factors were chosen based on the difference between panel plating and pattern plating from the first L_{18} DOE. However, according to the Taguchi methodology, the experimental condition of the hardware setting combinations would be different. This can possibly introduce different mean responses of the factors studied in the each of the L_{18} and L_8 DOE. This indicated that there were strong interaction between the different hardware factors and current density used. This also agrees with the finding by Poon et al [9, 13] and Tan and Lim [20].

In the study by Tan and Lim, the combining of the positive factors did not provide a more positive result. This was explained by the possibility of complex inter-relationships between parameters when they were brought together.

The models by Poon et al (equation 12 and 13) also indicate that the interaction between current density and different hardware settings is having an effect on the standard deviation of deposition on the cathode. However, the predicted value of the model (equation 12) did not agreed with the experimental result in industrial scale.

Since more process factors were involved in this research, the interactions between factors are expected to be more complicated. It was showed in this research that the models and results from previous researchers, which were based on laboratory scale, might not be applicable for industrial size process. The interactions of process factors may be different in different scales of process factors. These interaction effects have to be further studied.

5.3. Deposition Behaviour across the Cathode

While studying the standard deviation of deposition thickness across the cathode, it will be important to look into the deposition behaviour in terms of local vicinities of the cathode. This is critical for the PCB electroplating process since the mass production process always integrates more than one PCB along the cathode over the large plating window of the equipment.

In this research, it was found that the deposition thickness would be different over different areas of the cathode bar – the eight PCBs

5.3.1 Top to Bottom

It was observed from the experiments that there was a difference in deposition thickness on the cathode bar among the top, center and bottom of the cathode. Figure 5.2 – 5.5 are the thickness distribution across the cathode. It can be clearly seen from the plots of the thickness deposition that the bottom of the cathode are having a relatively thicker deposition when compared with those of the top and the middle. From the plots, the difference of deposition thickness between the middle and the bottom part of the cathode is not significant. However, it can be clearly seen

from Table 5.2-5.5 that the deposition thickness at the top was relatively higher than that in the middle on the cathode.

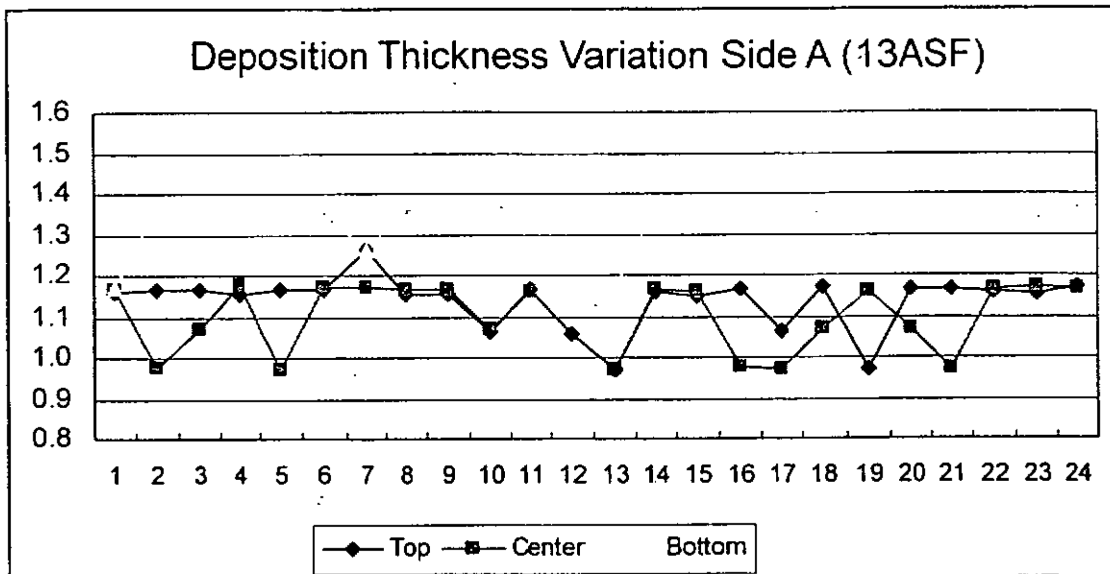


Figure 5.2a Deposition Behaviour over the 144" Cathode – with Enhanced Hardware and Current Density settings – A

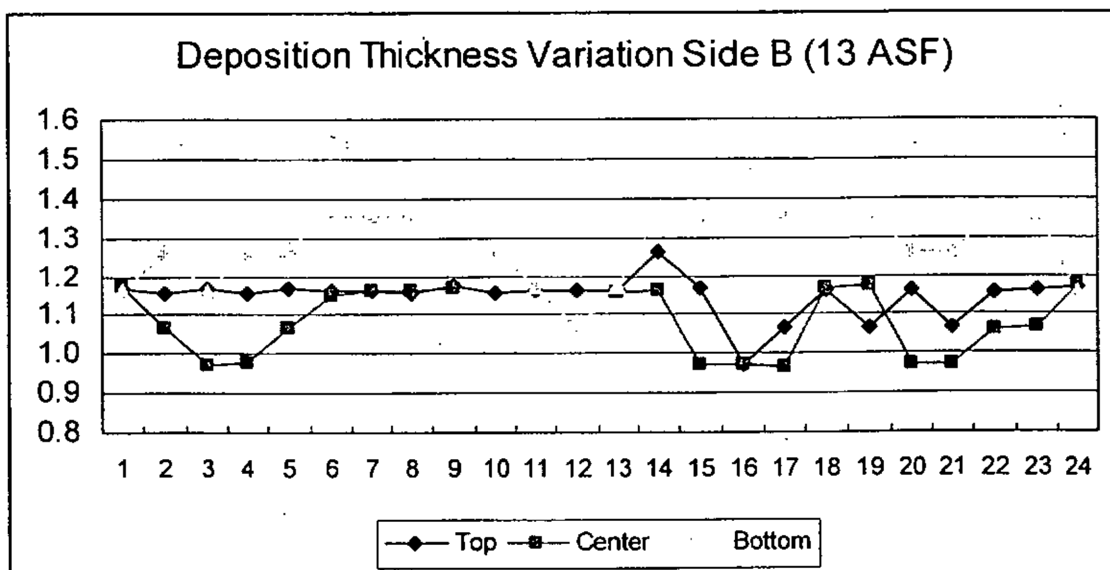


Figure 5.2b Deposition Behaviour over the 144" Cathode – with Enhanced Hardware and Current Density settings – B

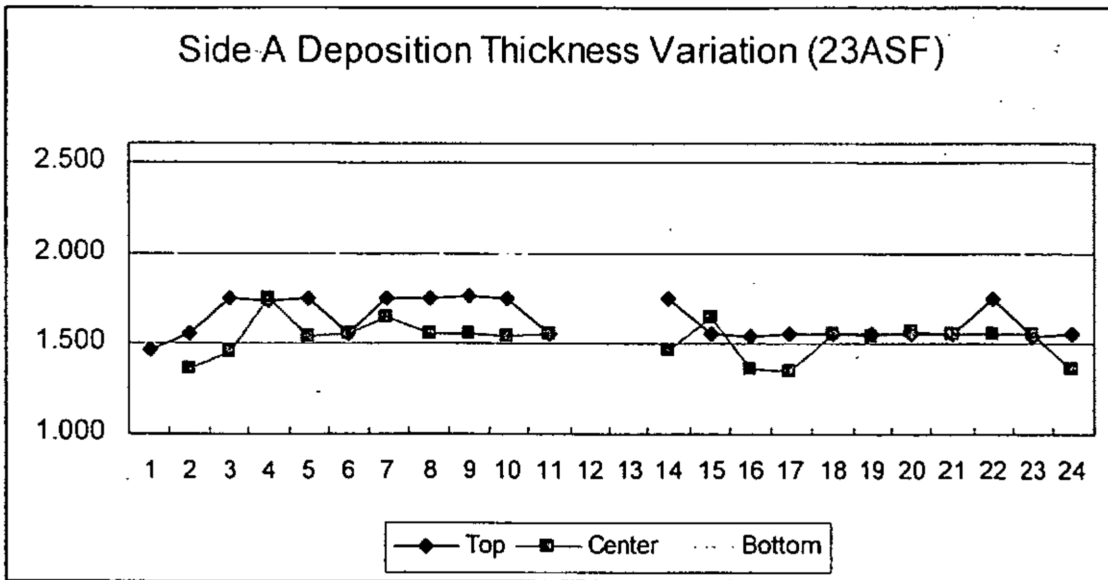


Figure 5.3a Deposition Behaviour over the 144" Cathode – with Enhanced Hardware settings and 23ASF – A

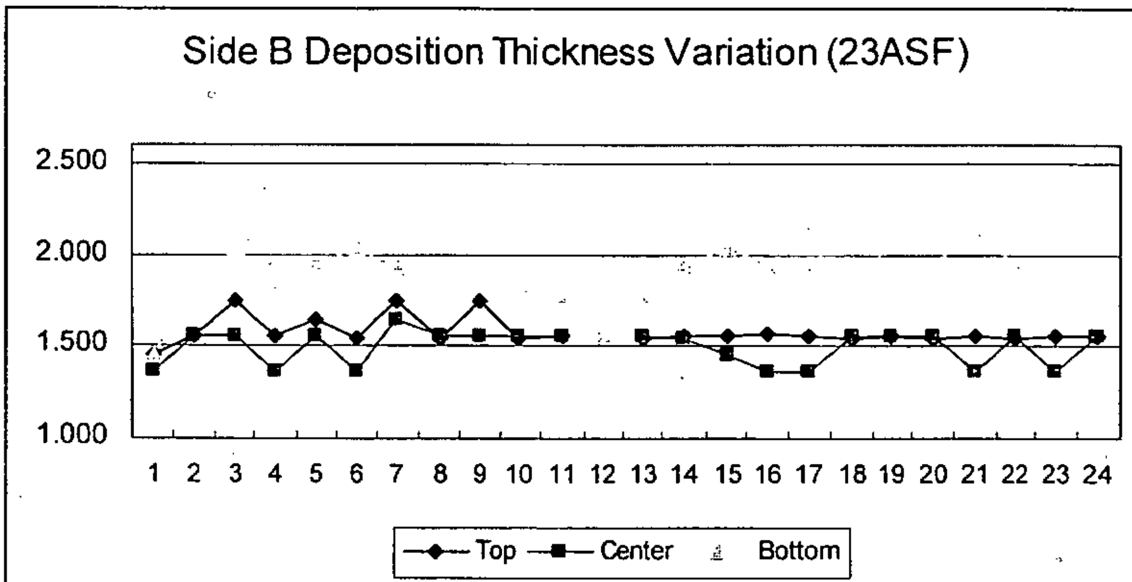


Figure 5.3b Deposition Behaviour over the 144" Cathode – with Enhanced Hardware settings and 23ASF – B

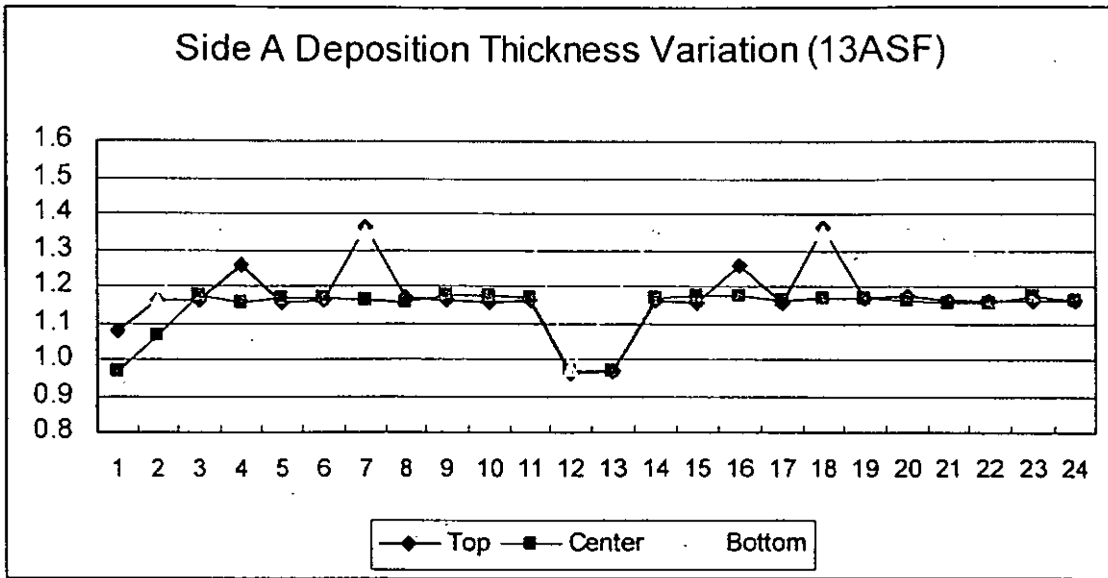


Figure 5.4a Deposition Behaviour over the 144" Cathode – with Production Hardware settings and 13ASF – A

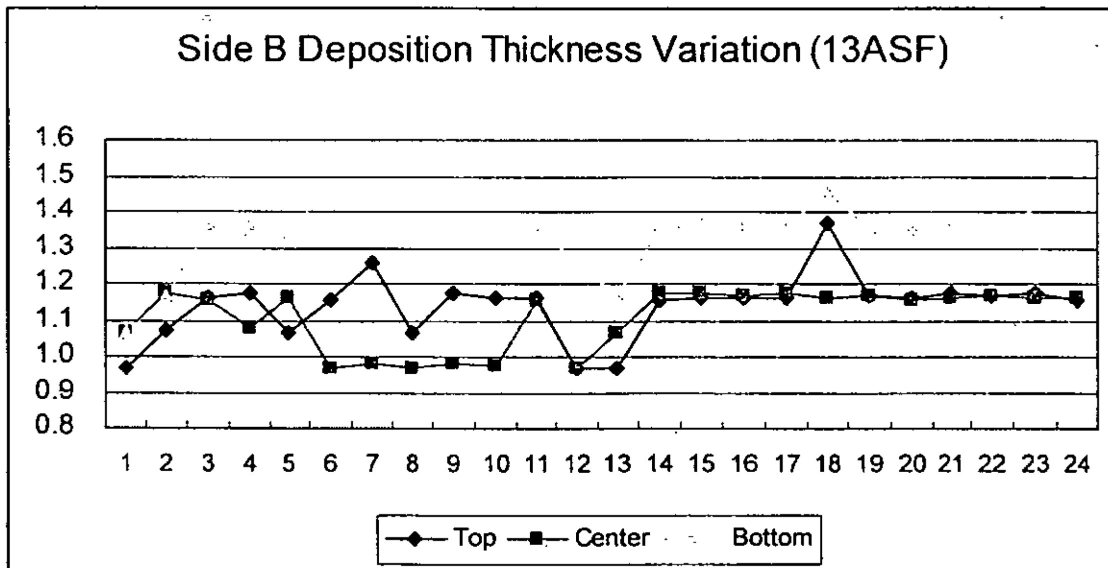


Figure 5.4b Deposition Behaviour over the 144" Cathode – with Production Hardware settings and 13ASF – B

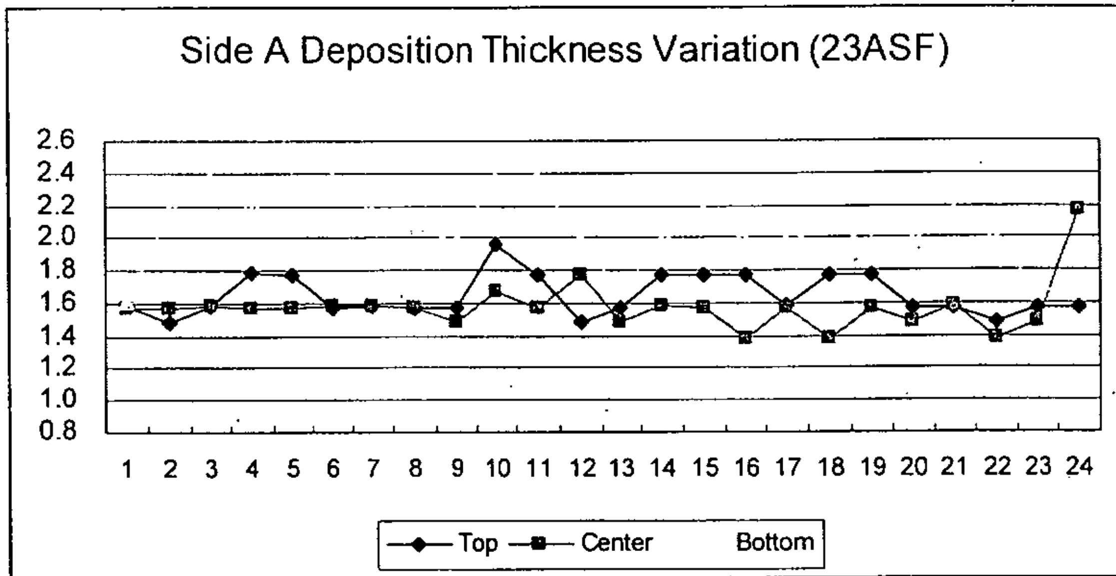


Figure 5.5a Deposition Behaviour over the 144" Cathode – with Production Hardware settings and 23ASF – A

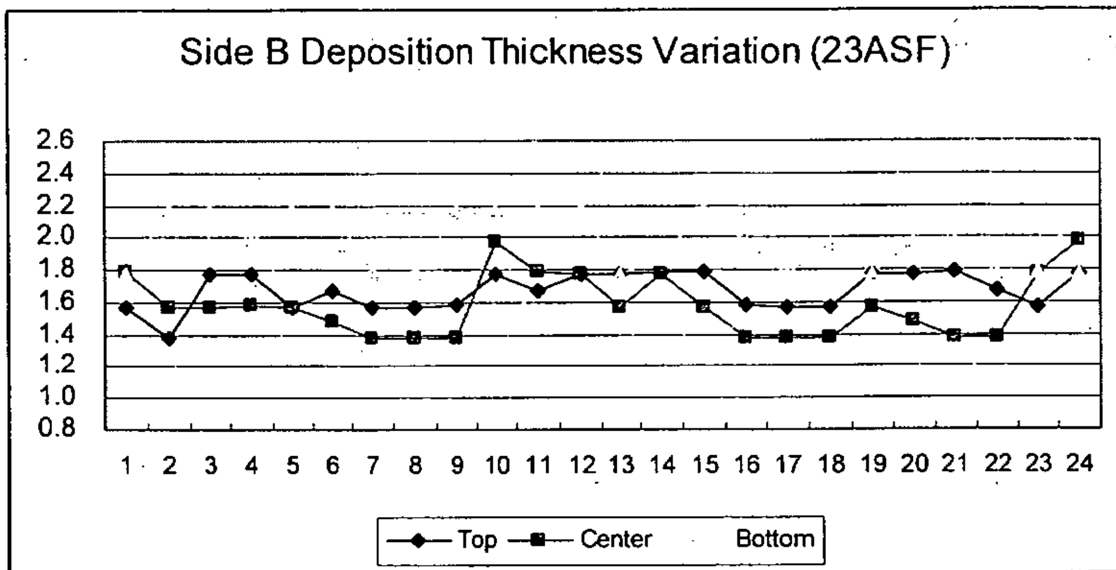


Figure 5.5b Deposition Behaviour over the 144" Cathode – with Production Hardware settings and 23ASF – B

	Average Thickness (mil)		
13 ASF	Side A	Side B	Average
Top	1.138	1.147	1.1426
Center	1.098	1.081	1.0898
Bottom	1.332	1.279	1.3054

Table 5.1 Deposition Thickness Behaviour from Top to Bottom – with Enhanced Hardware settings and 13ASF

	Average Thickness (mil)		
23 ASF	Side A	Side B	Average
Top	1.138	1.147	1.1426
Center	1.098	1.081	1.0898
Bottom	1.332	1.279	1.3054

Table 5.2 Deposition Thickness Behaviour from Top to Bottom – with Enhanced Hardware settings and 23ASF

	Average Thickness (mil)		
13 ASF	Side A	Side B	Average
Top	1.167	1.141	1.1538
Center	1.137	1.105	1.1208
Bottom	1.312	1.331	1.3215

Table 5.3 Deposition Thickness Behaviour from Top to Bottom – with Production Hardware settings and 13ASF

	Average Thickness (mil)		
23 ASF	Side A	Side B	Average
Top	1.646	1.672	1.6586
Center	1.573	1.576	1.5742
Bottom	2.049	1.967	2.0080

Table 5.4 Deposition Thickness Behaviour from Top to Bottom – with Production Hardware settings and 23ASF

The effect can be explained by the crowding of current density or the edge effect from the top to the bottom of the cathode. The effect was also reported previous researchers. Tan and Lim [20] also reported similar effect in their experiment – electroplating currents tend to concentrate at edges and points. However, a significantly thicker deposition was observed at the bottom part of the cathode. This implies the edge effect was more significant at the bottom part of the cathode. This can be explained by the edge effect was diversified by the conductive plating clips of the cathode bar to the PCBs at the top of the PCB surfaces.

5.3.2 Side to Side

The deposition thickness distribution of the cathode can also be studied in figure 5.2 – 5.5. It was observed in the experiment that smaller deposition thickness happened at three vicinities across the cathode from side to side – on the two edges and in the middle. This can be explained, similar to the thickness variation from top to bottom, by the design of the equipment. In the industrial equipment, in order to carry out the electroplating process with PCBs (eight PCB side by side in the batch process in the experiment), the handling of the array of PCBs is very important. The equipment was designed such that there is an electro-active frame with three "push bars", at the two sides and in the middle of the cathode rack, to handle the PCB array for electroplating. These push bars were inducing the edge effect and to diversify the current distribution at these three points of the PCB array surfaces.

Except in the three different vicinities of the three "push bars", the average thickness from the left to the right of the cathode PCBs did not show a significant difference. The average deposition thickness on the left, in the middle and on the right portions of the cathode is listed in Table 5.5 to 5.8.

The findings in this research also agreed with the mathematical analysis carried

out by Shih et. al. [94]. In their study, the current distribution on a planar cathode, the Laplace equations are solved by mean of potential theory [95-98], and using also Green's theorem [96-99] the resultant Fredholm integral equations of the second current distribution are solved numerically using a computer [99-102]. The ratio of the local cathodic current density (i) to the average current density (i_{avg}) was plotted against the surface of the cathode in different domains (k_c/A) where k_c = Wagner polarization parameter (cm) and A = the half-breadth of the electrode (cm) (Figure 5.6a – c).

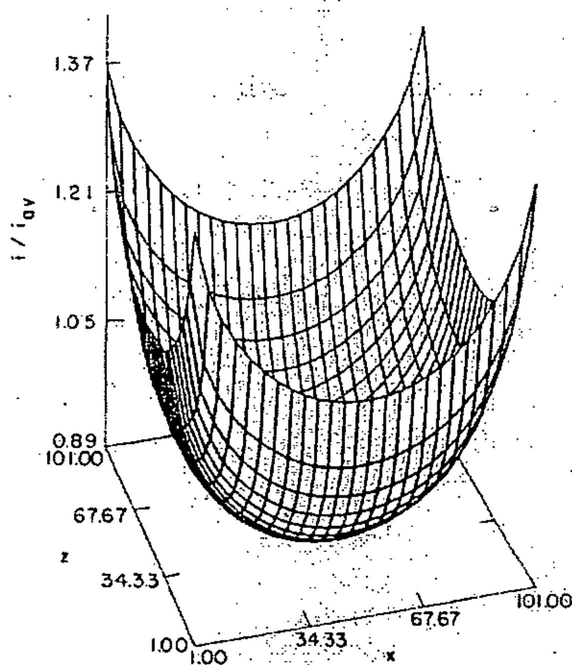


Figure 5.6a Three Dimensional Current Distribution over Cathode surface at Domain of k_c/A=0.25

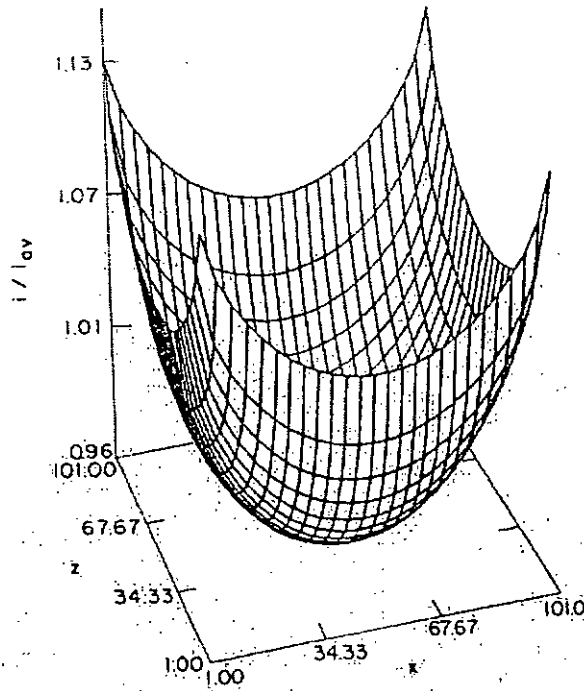


Figure 5.6b Three Dimensional Current Distribution over Cathode Surface at Domain of k_o/A=2.5

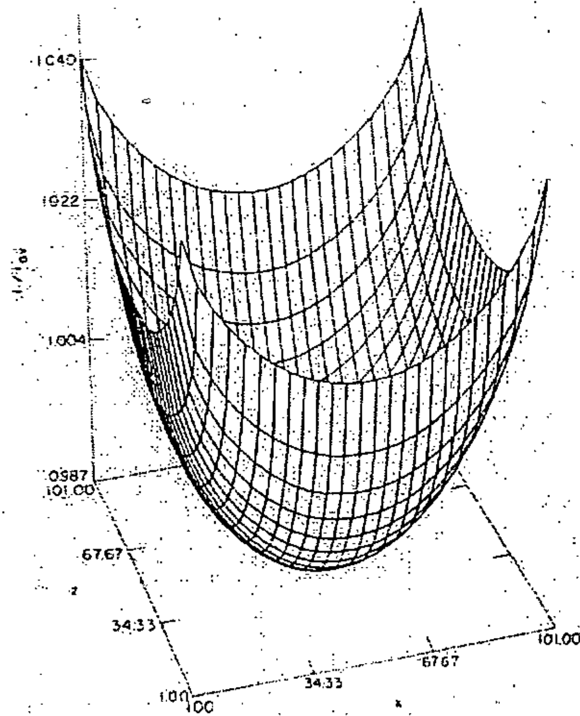


Figure 5.6a Three Dimensional Current Distribution over Cathode Surface at Domain of k_o/A=10

The three-dimensional analysis shows that the local current density reaches a maximum at the corners of a planar electrode. A gradient in current density exists along the edge between the corner and mid edge position.

In another study carried out by Mehdizadeh et.al. [103], a potential-theory model has been used to study the current distribution in the electroplating process. They showed that the strong influence of auxiliary electrode can be used to improved uniformity on a flat cathode. An optimal distance between the auxiliary electrode and cathode and the insulating wall of the plating exist. This implies that additional electro-active feature is having a significant effect on the current distribution. This agrees with the observations in this study that the electro-active push bars and cathode clips were having an effect on the copper distribution uniformity.

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	Average Thickness (mil)		
13 ASF	Side A	Side B	Average
Left	1.208	1.176	1.1922
Center	1.153	1.163	1.1583
Right	1.186	1.173	1.1795

Table 5.5 Deposition Thickness Behaviour from Side to Side – with Enhanced Hardware settings and 13ASF

	Average Thickness (mil)		
23 ASF	Side A	Side B	Average
Left	1.733	1.657	1.6951
Center	1.752	1.641	1.6964
Right	1.723	1.665	1.6941

Table 5.6 Deposition Thickness Behaviour from Side to Side – with Enhanced Hardware settings and 23ASF

	Average Thickness (mil)		
13 ASF	Side A	Side B	Average
Left	1.229	1.178	1.2032
Center	1.176	1.181	1.1784
Right	1.229	1.237	1.2330

Table 5.7 Deposition Thickness Behaviour from Side to Side – with Production Hardware settings and 13ASF

	Average Thickness (mil)		
23 ASF	Side A	Side B	Average
Left	1.794	1.715	1.7543
Center	1.782	1.791	1.7860
Right	1.713	1.712	1.7125

Table 5.8 Deposition Thickness Behaviour from Side to Side – with Production Hardware settings and 23ASF

6. Conclusions

It can be concluded from the research that the hardware setting of large scale industrial electroplating tank can be successfully enhanced by the Taguchi methodology.

1. Improvement in plating distribution evenness has been successfully achieved in the industrial plating tank. It can be applied to both when low and high current densities are used. This indicates that the effect of hardware settings and current density are important in terms of overall plating evenness. It also indicates that the hardware factor settings are playing a very important role in the deposition evenness, at least of the same significance as that of current density in the electroplating process.
2. It was found that the enhanced hardware settings for pattern and panel plating are different. This implies that different settings should be used for the industrial electroplating process when substrates of different feature designs are involved. This is more important in the PCB industry since the circuitry design of different PCBs is always different.
3. There are strong interactions between the different hardware factors and

current density. The interaction between these factors is significant such that the DOE result cannot be repeated with part of the hardware settings fixed while testing only the rest of the factor settings.

4. The experimental result based on relatively small or laboratory scale may not be well applied to industry. The interactions of different process factors are different over different ranges of process factor operation.
5. There is different deposition thickness over a large rectangular cathode of the PCB electroplating process. This is induced by the current crowding effect and can be offset by introducing additional conductors at different positions of the cathode bar. This agrees with and verifies the finding from numerical analysis by previous researchers.

7. Suggested Topics for Further Investigation

The findings in this research also raised interesting topics for further investigation. This includes:

1. As different PCBs carry different features, the enhanced hardware setting is valid only for PCB with bare copper surfaces. Since both panel and pattern plating are both of significance from PCB industrial point of view, studies can be repeated and continue to verify a general setting for both plating process.
2. The interactions of different process factors over different ranges should be further studied. It was shown in this research that results obtained from laboratory scale may not be well applied to industrial scale.
3. Since it is obvious that there are strong interactions between the hardware factors and current density, a more detail factorial design or Taguchi matrix with interaction DOE should be carried out to investigate the effect of the interactions.
4. One of the main objectives of the project is to improve the thickness variations across the whole PCB. The effect of enhancement can be better demonstrated with a fuller survey of production boards before and after hardware modification. In order to provide a systematic review of the effect of enhancement, the concept of active area density and active area density ratio can be used, and experiments

can be carried out with pattern and planar PCBs as well as quantified patterned cathode substrates. It is then able to compare the plating deposition variation before and after hardware enhancement.

5. In order to further study the effect of pulse plating and eductor agitation parameters on the electroplating process, more experiment work is suggested to be carried out with different hardware factors and current densities.

8. Statement of Originality and Contribution to Knowledge

In this study, an industrial copper electroplating tank was designed and set up in the study in which seven hardware factors can be varied. It is a first design which provides an industrial scale investigation of the copper electroplating process. This includes the enhancement of hardware settings for cathode PCB substrates with surface features of different densities. The seven hardware factors included are anode-cathode distance, cathode oscillation velocity, eductor orientation, eductor flow rate, anode distribution, relative anode cathode dimension and anode geometry.

It was found in the study that models or results based on in laboratory scale might not be well applied to industrial scale. This implies and verifies the strong interactions between the electroplating process factors. The response of these factors and complex interactions will react differently in different ranges of operation setting.

It is also important to note that from the Taguchi Methodology, a set of enhanced hardware setting was developed. The setting has been used in a PCB shop for mass production for more than 6 months and the effect of enhancement was proven for both 13 and 23ASF, two of the commonly used plating current densities in

the electroplating process. The enhancement has contributed to the PCB shop which allows mass production of 3mil line and 3mil spacing circuitry design. The result of the study and by the specially designed industrial equipment laid a good foundation for future investigation.

9. Appendices

1st Trial - Production setting

	Anode Geometry	Anode distribution	Anode cathode distance	Relative anode cathode dimension	Cathode oscillation velocity	Eductor orientation	Eductor flow rate	Current density	Average thickness	Deviation across cathode	Standard Deviation	Average deviation within panel
1	A1	B2	C1	D3	E1	F2	G3	H1 - 13ASF	1.198	0.49	0.141	0.306
2	A1	B2	C1	D3	E1	F2	G3	H3 - 23 ASF	1.747	0.99	0.308	0.704

Thickness Variation		
13ASF	Across Cathode	0.141
23ASF	Across Cathode	0.308

2nd Trial - Production setting

	Anode Geometry	Anode distribution	Anode cathode distance	Relative anode cathode dimension	Cathode oscillation velocity	Eductor orientation	Eductor flow rate	Current density	Average thickness	Deviation across cathode	Standard Deviation	Average deviation within panel
1	A1	B2	C1	D3	E1	F2	G3	H1 - 13ASF	1.206	0.47	0.153	0.312
2	A1	B2	C1	D3	E1	F2	G3	H3 - 23 ASF	1.812	0.877	0.352	0.771

Thickness Variation		
13ASF	Across Cathode	0.153
23ASF	Across Cathode	0.352

Production Setting

Average Thickness Variation		
13ASF	Across Cathode	0.147
23ASF	Across Cathode	0.330

	Average Thickness Variation	
	Production Setting	Optimized Setting
13ASF	0.1470	0.1315
23ASF	0.3300	0.2560

Phase I DOE L18

Frist Trial - Optimized Setting

	Anode Geometry	Anode distribution	Anode cathode distance	Relative anode cathode dimension	Cathode oscillation velocity	Eductor orientation	Eductor flow rate	Current density	Average thickness	Deviation across cathode	Standard Deviation	Average deviation within panel
1	A1	B3	C1	D3	E3	F2	G2	H1 - 13ASF	1.176	0.4	0.143	0.324
2	A1	B3	C1	D3	E3	F2	G2	H3 - 23 ASF	1.693	0.789	0.273	0.628

Thickness Variation (Stdev)		
13ASF	Across Cathode	0.143
23ASF	Across Cathode	0.217

Second Trial - Optimized setting

	Anode Geometry	Anode distribution	Anode cathode distance	Relative anode cathode dimension	Cathode oscillation velocity	Eductor orientation	Eductor flow rate	Current density	Average thickness	Deviation across cathode	Standard Deviation	Average deviation within panel
1	A1	B3	C1	D3	E3	F2	G2	H1 - 13ASF	1.202	0.452	0.119	0.355
2	A1	B3	C1	D3	E3	F2	G2	H3 - 23 ASF	1.711	0.766	0.295	0.713

Thickness Variation (Stdev)		
13ASF	Across Cathode	0.12
23ASF	Across Cathode	0.295

Optimized Setting

Average Thickness Variation		
13ASF	Across Cathode	0.1315
23ASF	Across Cathode	0.256

Experiment with Production Hardware settings

	Anode Geometry	Anode distribution	Anode cathode distance	Relative anode cathode dimension	Cathode oscillation velocity	Eductor orientation	Eductor flow rate	Current density	Average thickness	Deviation across cathode	Standard Deviation	Average deviation within panel
1	A1	B2	C1	D3	E1	F2	G3	H1 - 13ASF	1.203	0.492	0.138	0.299
2	A1	B2	C1	D3	E1	F2	G3	H3 - 23 ASF	1.747	0.99	0.308	0.704

Thickness Variation		
13ASF	Across Cathode	40.90%
	Within Panel	24.85%
23ASF	Across Cathode	56.67%
	Within Panel	40.30%

DOE Phase II L18

	Anode Distribution	Cathode oscillation velocity	Eductor orientation	Eductor flow rate	Average thickness	Deviation across cathode	Standard Deviation	Average deviation within panel
1	B2	E2	F1	G2	1.081	0.589	0.188	0.422
2	B2	E2	F1	G3	1.293	0.596	0.187	0.381
3	B2	E3	F2	G2	1.189	0.589	0.181	0.392
4	B2	E3	F2	G3	1.161	0.582	0.152	0.312
5	B3	E2	F2	G2	1.123	0.494	0.156	0.33
6	B3	E2	F2	G3	1.19	0.689	0.181	0.395
7	B3	E3	F1	G2	1.18	0.451	0.16	0.378
8	B3	E3	F1	G3	1.147	0.621	0.186	0.423

Mean Respond (Δ Thickness)		
B	2"	3"
Cathode	0.177	0.17075
Panel	32.09%	32.87%

B=3"

E	12 cyc/min	14cyc/min
Cathode	0.178	0.16975
Panel	32.77%	32.19%

E=14 cyc/min

F	0 deg	7.5 deg
Cathode	0.18025	0.1675
Panel	34.35%	30.61%

F=7.5 deg

G	60 gal/min	70 gal/min
Cathode	0.17125	0.1765
Panel	33.36%	31.60%

G=60 gal/min

Pulse Plating Chemical Control Range

Item	Component	Operating Range	Specification	Optimal operating value
Copper Plating Tank	$CuSO_4 5H_2O$	70 - 80g/l	55 – 95g/l	75g/l
	H_2SO_4(AR)	11.5-12.5%(v/v)	8 - 16%(V/V)	12%(V/V)
	HCL	65-85PPM	50 - 100PPM	75PPM
	79288 (Pulse Plating Leveler)	By Hull Cell	≥10ml/L	≥10ml/L
	79289 (Pulse Plating Brightener)	By Hull Cell	≥5ml/L for pulse plating operation	/

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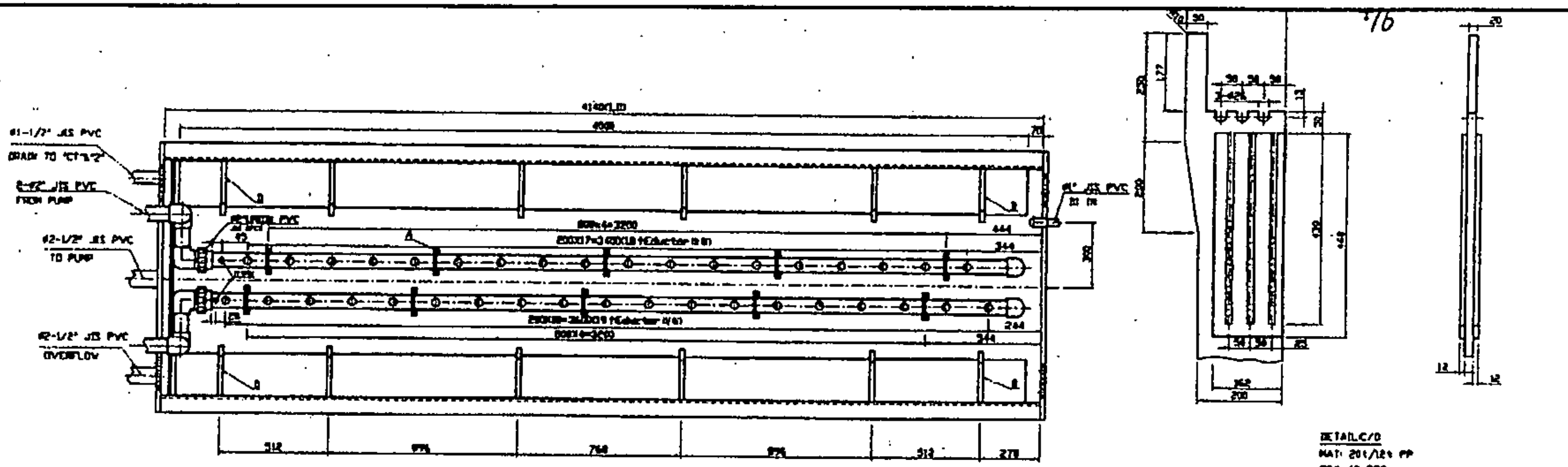

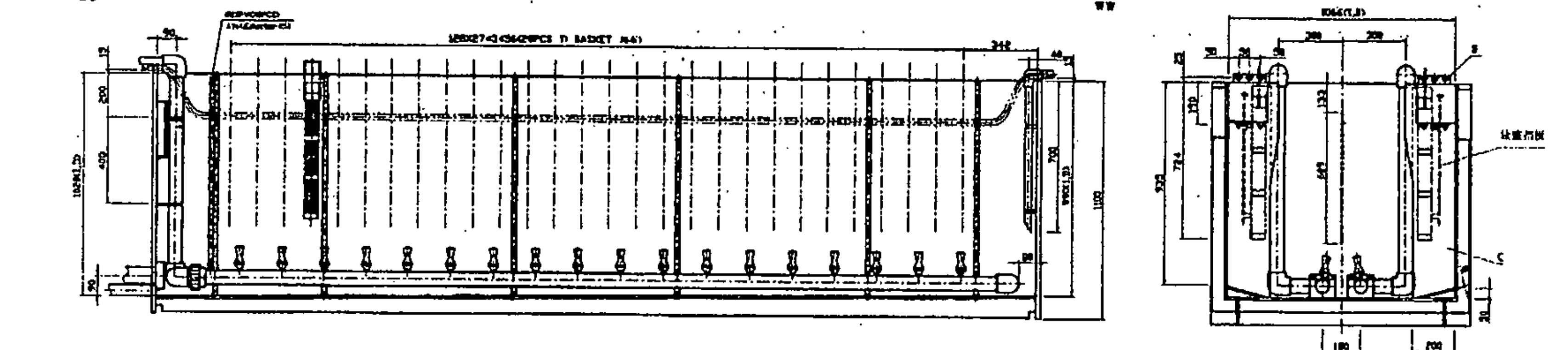

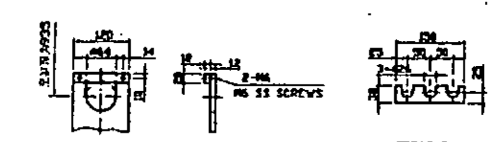

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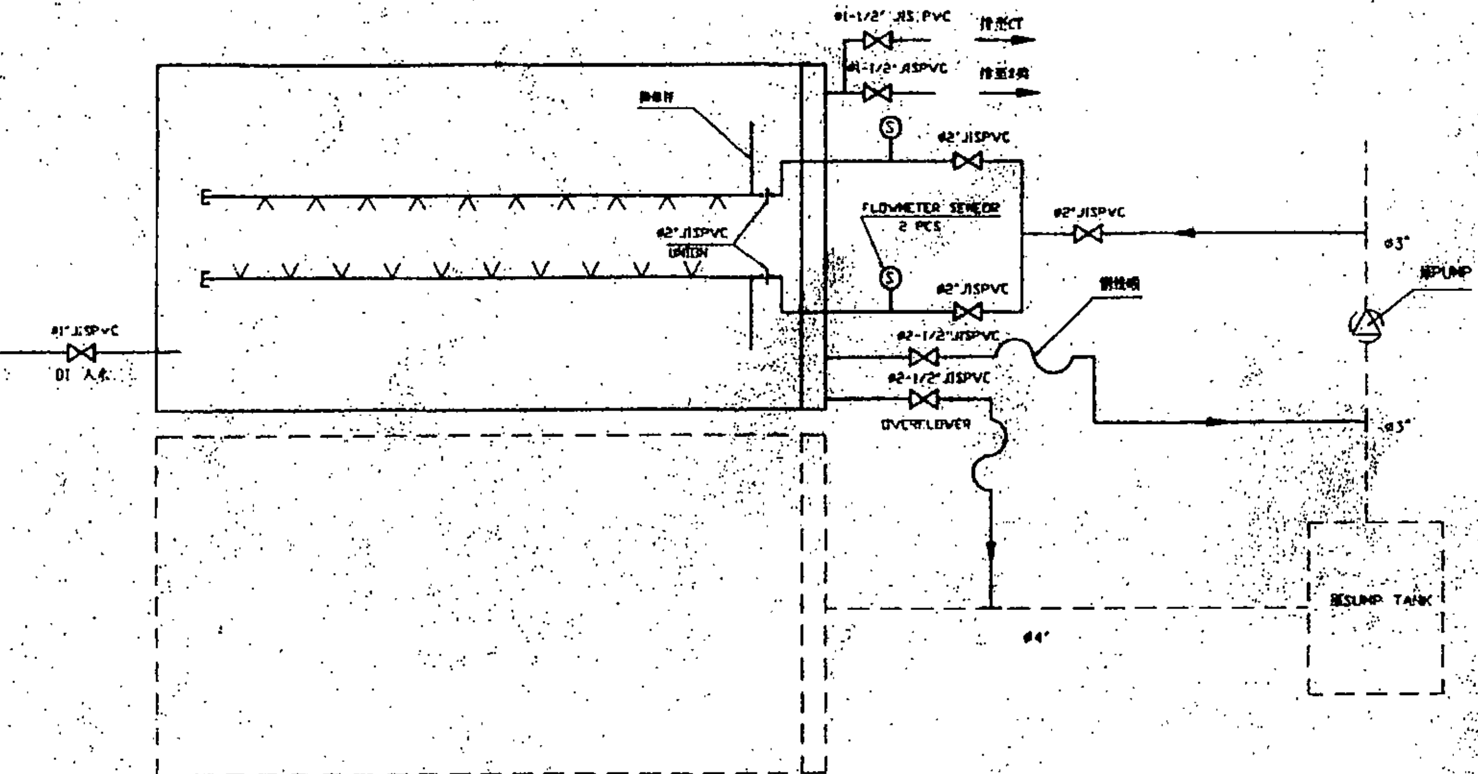
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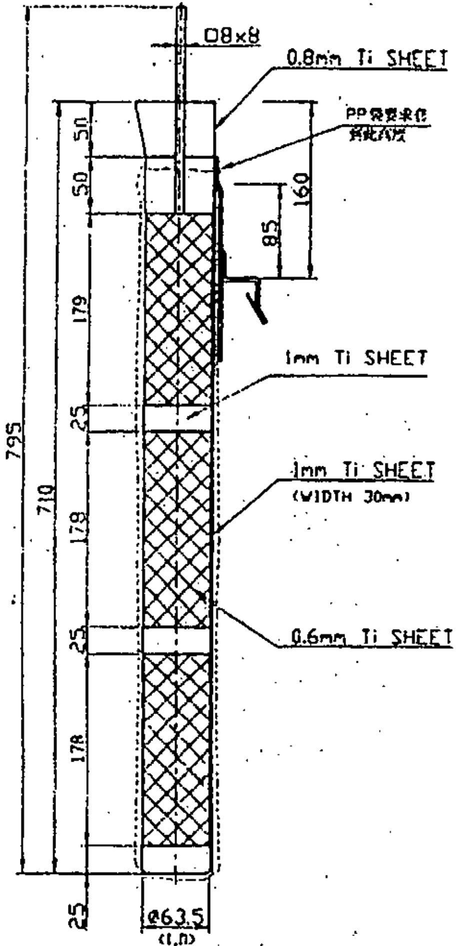

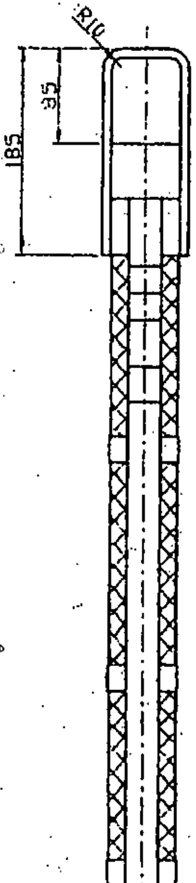

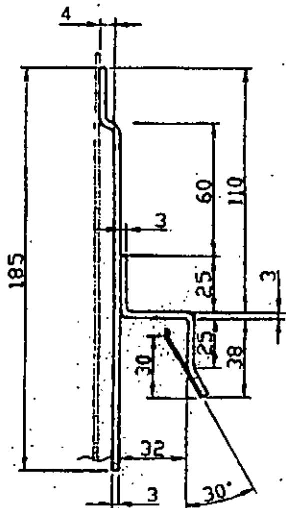

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QTY: 56 PCS

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PROTEK TECHNOLOGY LIMITED

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