The Hong Kong Polytechnic University

The Department of Electronic and Information Engineering

AC to DC Conversion Improvement Techniques in Switching Converters and Their Applications

by

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Doctor of Philosophy

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CERTIFICATE OF ORIGINALITY

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Abstract

AC/DC conversion is usually found in two locations in a switching converter. The first one is at the input of the converter, the purpose being to convert the low-frequency AC voltage into a DC voltage which can be used by the subsequent high-frequency switching converter stage. The other AC/DC conversion is found at the output of the converter and its purpose is to rectify the high-frequency switched AC voltage and to provide suitable filtering in order to produce a smooth DC output. Usually, significant power loss and unwanted current harmonic distortions in these two locations are undesirably found under certain conditions, such as low input AC voltage, high input mains frequency and high output current.

In this thesis, two new design approaches for AC/DC conversion are described, namely, “input rectifierless converter” and “output filterless converter”. The goal is to have a higher conversion efficiency, lower current harmonics and reduced ripple in the two AC/DC conversion locations mentioned above. The input rectifierless converter approach has the advantages of eliminating rectifiers and avoiding crossover distortions. A general method for synthesizing input rectifierless converters using a minimum of two DC/DC converters is proposed. A detailed analysis on the requirement of the constituent converters is presented. A specific converter structure has been developed for aircraft power system applications using the basic configuration. The proposed basic configuration is also found suitable and proven to be a minimum configuration for general impedance synthesis. Prototypes have been tested and experimental results for synthesizing impedances are presented in this thesis.

For the high-frequency AC/DC conversion at the output of a switching converter, a filterless AC/DC conversion technique based on overlapping AC voltage sources is proposed. A new topology has been created with high conversion efficiency and low output ripple voltage, which is suitable for high output current and low output voltage applications.

The contributions of this thesis are summarized as follows:

I AC/DC conversions at the input (low frequency) and the output (high frequency) of switching converters have been studied.

II A general synthesis method for input rectifierless AC/DC converters based on a two-converter configuration has been proposed. The method forms the basis for systematic generation of new input rectifierless topologies that can eliminate the otherwise unavoidable distortions caused by the input rectifiers and the input current phase lead.

III Using the synthesis method for input rectifierless AC/DC converters, a specific application circuit has been developed for aircraft power supply applications.

IV The proposed two-converter configuration for rectifierless AC/DC conversion has been extended to general impedance synthesis.

V A filterless AC/DC conversion technique has been studied. The technique eliminates the problems caused by conventional output filters, such as high conduction loss in high output current applications. In addition, a technique for reducing switching loss of the output rectifiers has been proposed.

VI A specific converter topology has been derived to implement the filterless AC/DC conversion technique as well as the proposed switching loss reduction technique that improves both the converter efficiency, the ripple and noise specifications.

Acknowledgements

I wish to thank and show my sincere appreciation to a few people who are important to the completion of this thesis.

First, I would like to thank my supervisor, Dr Y. M. Lai, for his encouragement and great support during the course of my PhD study. My sincere thanks are due to my co-supervisor, Prof. Michael Tse, who has been very supportive in the past six years. I appreciate very much their valuable guidance and suggestions to my work. Their deep involvement in every detail of the research work is absolutely important to the completion of this thesis.

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Chapter 1 Introduction

1.1 Background and Motivation

Switching converters offer significant improvement in conversion efficiency, performance, and compactness for electrical power supply systems over conventional linear power supplies. They have become a mandatory choice in today's electronic appliances that require high efficiency, high performance, small size and light weight. With the continuous rapid development of electronic systems, the requirements of switching converters have become increasingly stringent. According to a 5-year power technology roadmap from ON Semiconductor, the required power density of switching converters will increase three-fold and the power loss will be reduced by 55% from 2003 to 2008. Researchers have been working hard to create new devices and develop new converter topologies to meet the ever more demanding requirements.

One major function of a switching converter is the AC/DC conversion. This is usually done by using rectifiers and a filter to provide a smooth DC voltage output. The concepts and basic circuit configurations for achieving the purpose have not changed significantly over the years.

Figure 1-1 shows a typical configuration of an AC/DC switching converter. There are mainly two locations where AC/DC conversion is found in an AC/DC converter. The first AC/DC conversion is to convert the AC input voltage from the AC mains into a DC voltage which will be used by the subsequent switching converter stage. The other is to convert the high frequency switched AC voltage generated by a switching circuit into a smooth DC output voltage for use by the intended appliance.

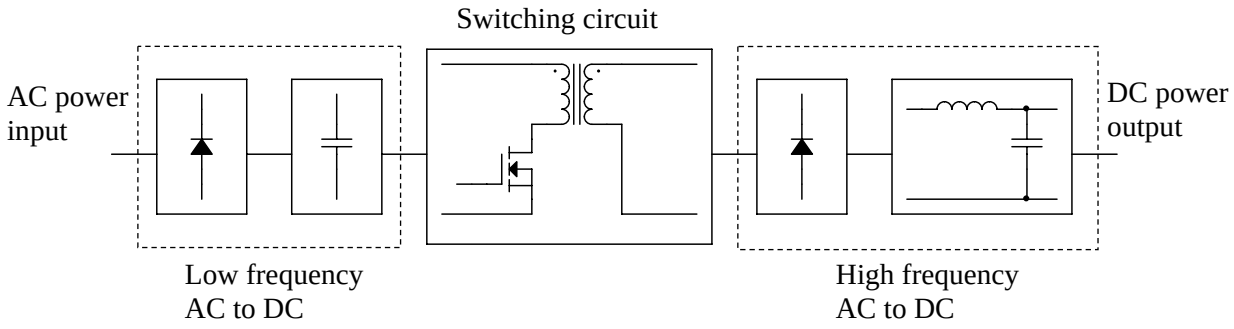


Figure 1-1: A typical configuration of AC/DC switching converters.

The front-end AC/DC conversion operates at the mains frequency which is usually low when compared with the switching frequency of the core switching converter. The reason for low mains frequencies is for efficient long distant transmission. For traction power networks, 16.7 Hz, 25 Hz and 50 Hz are used as the mains frequencies. In aircraft power systems, 400 Hz is usually used as the mains frequency to effectively reduce the size and weight of magnetic components. The most widely used mains frequencies are 50 Hz and 60 Hz for the domestic AC power supply.

The AC mains voltage is rectified to DC voltage by means of rectifiers. In the filter circuit, magnetic components are seldom included for most applications because heavy and large sized cores are required for operation at such a low frequency. Capacitors are usually the only components for the filters.

Nowadays, stringent requirements are imposed for the front-end AC/DC conversion, especially in aspects of power loss [IC99, LTPPL04, LMS00] and input current harmonics [S02, S05, GSBM03a, D90].

The power loss of the low-frequency AC/DC conversion is dominated by the conduction loss of input rectifiers [IC99, LTPPL04, LMS00]. There has not been much improvement in the rectifiers used for such purposes although continuous improvements and certain breakthroughs have been found in other semiconductor devices like MOSFETs [KJV01]. The loss is “irreducible” as it is originated from the physical forward voltage drop of diode rectifiers [IC99, LG90]. The forward drop V_F of diode rectifiers is usually found to be about 1 to 1.2 V at the rated current. For the bridge rectifiers that are usually used in single-phase input switching converters, the total forward drop is $2V_F$. The power loss of the bridge rectifier increases as the input mains voltage decreases. At a root-mean-squared input mains voltage of 85 V, which is usually the lower limit of the universal input voltage range required for domestic AC power operated converters, the efficiency drop due to the input bridge rectifier in a power-factor-correction (PFC) regulator is approximately 2 to 3%. From the power-loss viewpoint, it contributes about 25 to 37.5% of the total power loss of the converter if the overall converter conversion efficiency is assumed to be 92%. This shows that the rectifiers in the low-frequency AC/DC conversion at the front end contribute to the major power loss in an AC/DC converter especially at low input mains voltage. Engineers’ solutions have been mainly developed around the provision of suitable cooling, like adding heatsinks, to keep the devices within the operating temperature limit.

Another major problem is the generation of input current harmonics. The need for reducing input current harmonics is actually imposed by the international

standards like EN61000-3-2 and DO160 (for aircraft power systems) that define the allowable line frequency harmonics produced by electronic equipment including switching converters drawing power from the mains. PFC regulators provide a good solution to the problem but researchers report that the front-end AC/DC conversion circuit introduces crossover distortion [IC99, LTPPL04, S02, LL06]. Such crossover distortion also gives rise to another distortion caused by the dynamic response of the PFC regulation after the crossover period [S02, S05, GSBM03b, PCS05]. The distortion becomes more significant when the mains frequency is comparatively high, such as that in aircraft power supply systems.

The second AC/DC conversion required in a switching converter is to convert high-frequency switched AC voltage to a smooth DC output for direct use by electronic appliances. The efficiency of the conversion depends very much on the operating conditions such as the switching frequency of the converter [BGMMPR03, R01, TDE03, LOO95], the required output voltage and current level [CL05, XLPP01], and the output ripple and noise specifications.

The trend towards high power density transpires that power converters will operate at increasingly higher switching frequency. This increases the switching loss of the rectifying devices due to the reverse recovery of rectifying diodes and the switching delay of rectifiers.

In the past decades, integrated circuits and electronic systems have been developed rapidly. The device complexity and the on-chip transistor density are almost doubled every two years. These developments have boosted the demand for high supply current. On the other hand, the supply voltage for integrated circuits is continuously being lowered in order to increase the operating speed, control the increase of power consumption and improve the reliability. The trend of low output

voltage and high output current not only increases the conduction loss of the second AC/DC conversion, but also the sensitivity of the conversion efficiency to the voltage drop across the rectifiers and output filters.

For the output voltage ripple and noise levels, the industrial standard requirement is typically 1% of the output voltage. Lower output voltage requires smaller ripple and noise levels that in turn call for more effective output filtering. Larger inductances for the filtering chokes as well as larger capacitor banks are needed to reduce the ripple current and output ripple voltage in order to meet the specifications. This not only increases the size of the output filter, therefore reduces the power density of converters, but also increases the loss of the inductive components. Simple magnetic wire-wound inductors in general cannot meet nowadays' high current and high inductance requirements, and special winding structures using thick copper strips increase the complexity and are difficult to manufacture.

The use of synchronous rectifiers in the output AC/DC conversion has taken the advantages of low-voltage MOSFET devices and the remarkable reduction in conduction loss. The robust parallel operation of MOSFETs has made synchronous rectifiers a ready solution for combating conduction loss [BGMMPR03]. However, the switching loss of synchronous rectifiers is quite high when compared to conventional Schottky diodes because of the switching delay and poor reverse recovery characteristics of the MOSFET's body diode [BGMMPR03, LOO95]. Extra care should be taken to the selection of MOSFETs with fast switching characteristics, or the advantages of synchronous rectifiers will be dimmed.

Summarizing the aforementioned problems, the root causes of the problems found in the front-end low-frequency AC/DC conversion are the physical constraints

of the input rectifiers and the construction of basic rectifying circuits. New breakthroughs either in the device performance or the basic circuit configurations are required for the needed improvements in order to meet the foreseeable requirements. Eliminating the input rectifiers seems to be an ultimate solution. In the past, specific converter topologies, which can handle AC input directly without using front-end rectifiers, have been proposed by researchers. However, they are seldom found in commercial switching converter products. One major reason is the lack of a clear theoretical foundation and a systematical synthesis procedure for designing such “rectfierless” converters. Generating suitable topologies to fit their intended applications becomes a highly non-trivial task.

For the output high-frequency AC/DC conversion, techniques for reducing switching loss of the rectifying devices and the output ripple current or voltage would be the main research focus. The method of interleaving the output current of multiple converters has been a feasible solution; however, the ripple current reduction is highly sensitive to the operating duty cycle and input voltage.

This thesis focuses on input rectifierless and output filterless converters that can provide simple and robust solutions to the various problems associated with AC/DC conversion in switching power converters. The techniques developed in this thesis provide effective solutions to tackle these problems. Practical circuits are designed for different applications, with experimental results verifying the design objectives and the intended performance.

1.2 Outline of the Thesis

The major research focus of this thesis is the AC/DC conversion in switching converters. In general, two AC/DC conversions are identified. They are located at the input front end and the output of switching converters that operate at low mains frequencies and high converter switching frequencies, respectively. Chapter 2 and Chapter 3 collectively review the problems and performance constraints of the two AC/DC conversions based on conventional techniques. Chapter 4 through Chapter 9 present improvement techniques to the problems and illustrate the techniques with application examples.

In Chapter 2, the major problems of front-end low-frequency AC/DC conversion are addressed. The associated power loss and input current harmonics are analyzed.

Chapter 3 addresses the problems of high-frequency AC/DC conversion at the output of switching converters. The conduction and switching losses of output rectifiers are analyzed and the problems of output filter design with respect to the relevant industrial standards are discussed.

Chapter 4 considers the fundamental synthesis problem of input rectifierless converters. The aim of such converters is to convert an unrectified AC voltage to a DC voltage without using input rectifiers. A configuration using a combination of DC/DC converters for AC/DC conversion is proposed. The construction of such a converter is derived systematically based on a fundamental idea of introducing a DC “stack” voltage to the input AC source. The simplest structure consisting of two DC/DC converters is obtained. The criterion for choosing the two DC/DC converters in terms of the voltage conversion ratio is derived. The power flow of the simplest configuration is analyzed and the power processed by the two DC/DC converters is

derived under the condition of sinusoidal AC voltage source input. The analysis results give a formula related to the requirement of the stack voltage for minimum power circulation. This formula is useful for the optimization of the overall efficiency. A control scheme is derived for providing regulation to the DC output as well as shaping the input current waveforms. An input rectifierless AC/DC converter topology is generated from the simplest configuration developed. Effective control has been derived to provide the necessary input PFC function.

Chapter 5 presents a practical circuit synthesis based on the minimum configuration of input rectifierless AC/DC converter derived in Chapter 4 to realize a PFC regulator suitable for aircraft power system using a high mains frequency of 400 Hz. The problems of input harmonic current generated by a conventional PFC topology employing input bridge rectifier at high mains frequency are addressed. A control scheme that introduces a variable stack voltage to the input AC mains to reduce the amount of power loss due to power circulation is proposed. A power flow analysis is given, which shows that the new control scheme together with the current-programming control can significantly reduce the amount of circulating power and hence improve the conversion efficiency. A 100 W PFC regulator has been prototyped for experimental verifications. The measured conversion efficiency and input current waveforms confirm the high conversion efficiency and the elimination of crossover distortions at 400 Hz mains frequency.

Chapter 6 gives another application example of the input rectifierless converter synthesis technique derived in Chapter 4. A general impedance synthesizer is implemented based on the minimal configuration that consists of two DC/DC converters. This chapter is arranged to firstly derive the minimum requirements of constructing a general impedance synthesizer out of simple DC/DC converters. It

has been shown that the minimum configuration requires one storage element and two simple DC/DC converters with separate control for input current programming and power flow balancing. A circuit is designed accordingly and prototyped to realize a general impedance synthesizer. Control schemes are proposed with different circuit parameters derived for synthesizing pure inductance, pure capacitance, inductive and capacitive impedances. The frequency responses of the synthesized impedances are compared with those of the corresponding ideal impedances.

Chapter 7 addresses and studies a filterless AC/DC conversion technique for high-frequency operation. The idea is based on connecting two AC voltage sources with square waveforms in parallel. A simple simulation is first given to show the capability of the technique to provide a ripple-free DC output voltage without the need of an output filter. Operating conditions and practical constraints of the technique are discussed. The switching loss of rectifiers used in the proposed circuit is analyzed. Based on this filterless AC/DC conversion approach, a technique for reducing the switching loss of the rectifiers is presented. Basically, in this method, the switching loss reduction is achieved through the current commutation between the two AC sources and it has been analyzed with practical considerations of parasitic inductances. Conditions to achieve low switching loss are derived.

Chapter 8 presents a topology that implements the AC/DC conversion technique described in Chapter 7. The topology is based on two asymmetrical drive half-bridge converters with their output voltages overlapped for a finite period of time. The basic operating principle is given. The current commutation process between the converters during the overlapping period is analyzed in detail. Conditions for zero current switching of the output rectifiers are given. Formulas for calculating the

required circuit component values and the output ripple current amplitude are derived for facilitating practical design.

Finally, Chapter 9 summarizes the main contributions of this thesis and proposes some possible future works.

Chapter 2 Review of Front-End Low-Frequency AC/DC Conversion in Switching Converters

2.1 Introduction

The design of DC/DC converters has enjoyed a wealth of sophisticated techniques. Standardized design guidelines are available for engineers to choose topologies, design feedback controllers, and select optimized parameters for the applications concerned. However, in designing an AC/DC converter that derives power from the AC mains, a simple AC/DC conversion is usually introduced at the front end, followed by a familiar DC/DC converter to provide a DC voltage output. In practice, a simple AC/DC conversion process involving a bridge rectifier and some filtering capacitors is needed at the input front end of single-phase off-line switching converters. The research focus has been on the performance improvement of the DC/DC converter that follows the AC/DC conversion.

The work described in this thesis is concerned with techniques for improving the AC/DC conversion in switching converters. The problems associated with the simple front-end AC/DC conversion are practically important as eliminating them is crucial to the satisfaction of today's stringent requirements. This chapter aims to review the performance of conventional rectifying circuits as well as to reveal the problems associated with such circuits in terms of power loss and harmonic distortions.

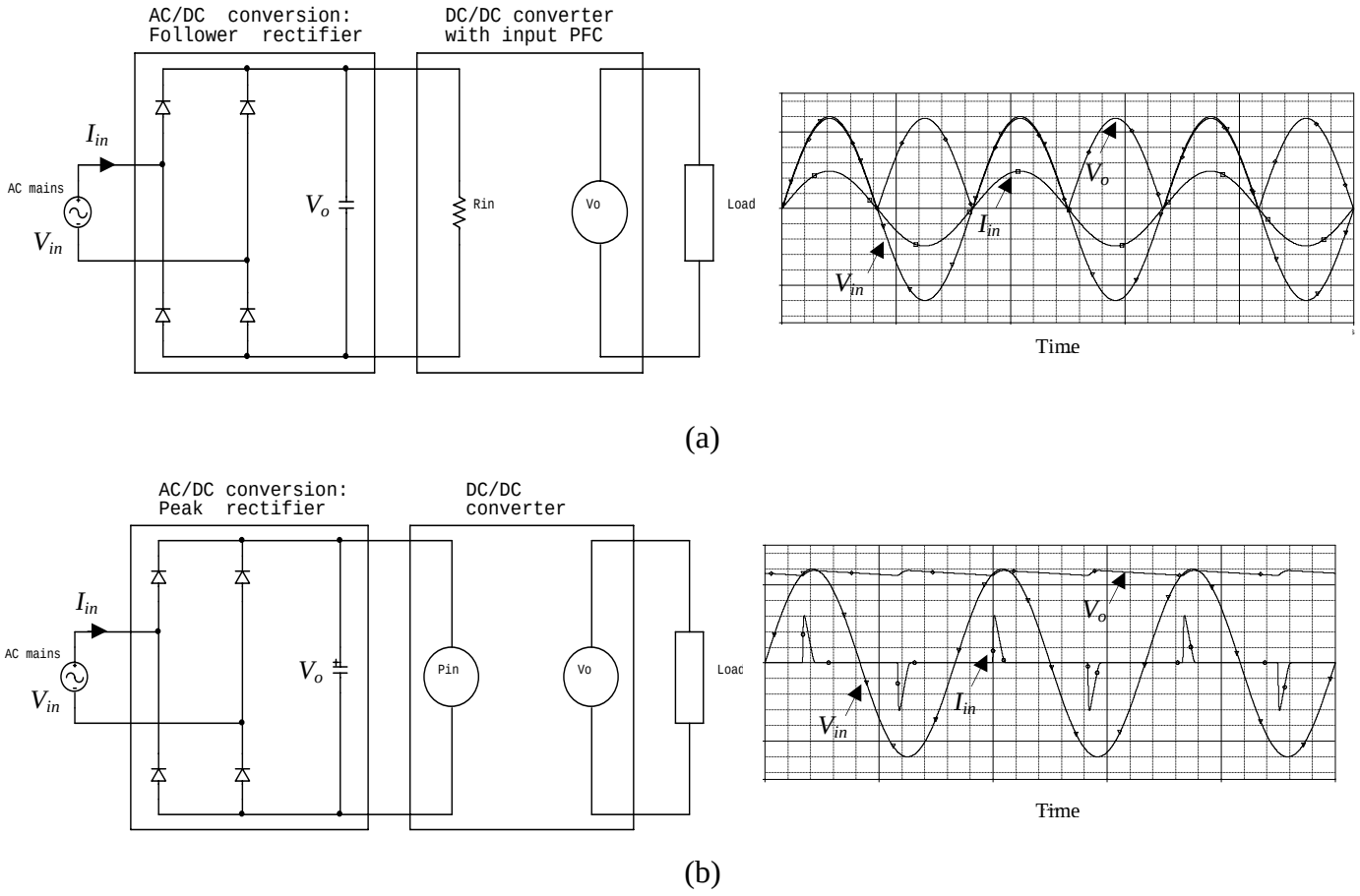


Figure 2-1: (a) Full-wave follower rectifier circuit using small capacitance for high-frequency ripple current filtering and its general operating waveforms; (b) full-wave peak rectifier circuit using high filtering capacitance and its general operating waveforms.

Two typical circuit schematics are shown in Figure 2-1. Both circuits share a similar configuration, which consists of a bridge rectifier and a filtering capacitor. Magnetic components are seldom used in practice because of their bulkiness at low-frequency operation, as mentioned in Chapter 1.

2.2 Power Loss of Diode Rectifier

The switching loss of diode rectifiers for this front-end application is very small because of low operating frequencies. The major loss is due to the forward voltage

drop of the rectifiers during conduction of current. The forward drop of a diode depends on its construction type, and silicon p-n junction diodes are usually used for this application because their breakdown voltage can be as high as 600 V which is required by the universal line voltage operation.

2.2.1 Forward drop of diode junction

The relationship between the forward junction voltage $V_{\text{F\_junction}}$ and the current of a diode is governed by the diode equation shown in (2-1), where I_r and V_B are diode parameters depending on the doping density and the junction type. Figure 2-2 shows a typical plot of the forward current against the forward voltage of a silicon p-n junction diode.

$$I_F = I_r \cdot \left(e^{\frac{V_{\text{F\_junction}}}{V_B}} - 1 \right) \qquad (2\text{-}1)$$

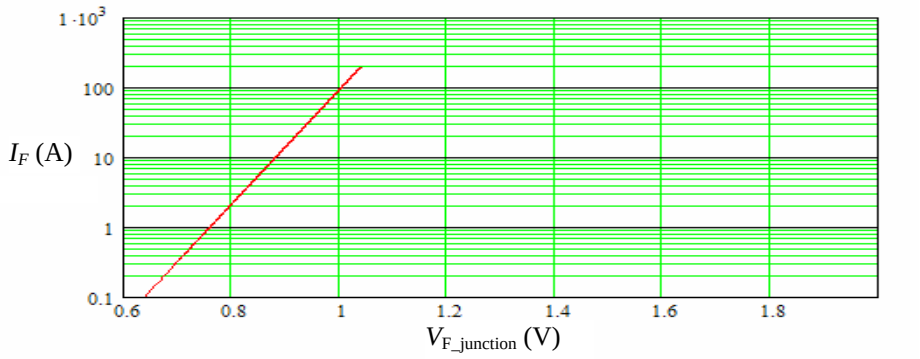


Figure 2-2: A typical plot of I_F – $V_{\text{F\_junction}}$ of silicon p-n junction diode.

It can be observed that the diode current increases exponentially after a certain threshold forward voltage. For silicon p-n junction diodes used in input rectifiers, the threshold is about 0.65 V. Clearly, this physical characteristic affects the conduction loss and hence limits the performance of rectifiers.

2.2.2 Forward drop due to the conductivity of semiconductor

In addition to the forward drop of diode junction, the comparatively low conductivity of semiconductor also contributes to the forward drop [LG90] when the diode conducts current. The resistive drop of a diode depends on the semiconductor dimensions and the current rating of the diode.

2.2.3 Forward drop due to junction and resistance

Combining both the forward junction voltage and the resistive drop of semiconductor in a diode, the forward voltage of a diode is given in (2-2), where R_{diode} is the diode equivalent resistance. Figure 2-3 shows the forward current characteristics against the diode forward drop and junction characteristics.

$$V_F = V_B \cdot \ln\left(\frac{I_F}{I_r} + 1\right) + I_F \cdot R_{\text{diode}} \qquad (2\text{-}2)$$

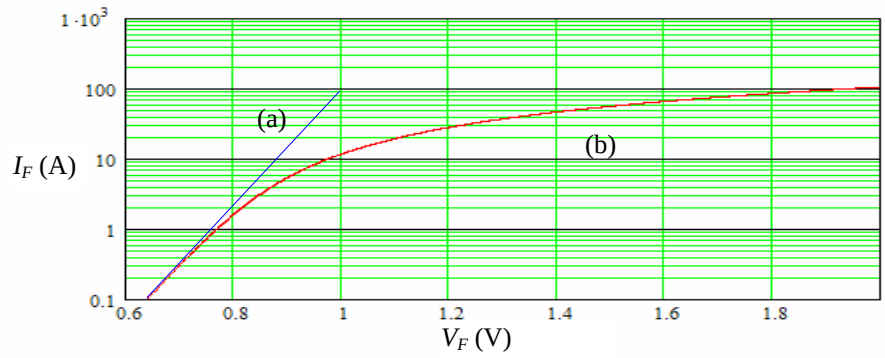


Figure 2-3: I_F – V_F plot: (a) Junction forward drop only; (b) forward drop with diode resistance.

It can be observed that the diode voltage is dominated by the junction forward drop at low current, and the effect of the diode resistance emerges and becomes significant at high current. Typically, the forward drop due to the junction characteristic does not differ much among diodes of the same type and similar reverse breakdown voltage. Diodes with a higher current rating have smaller diode

resistance. Usually the diode resistance is designed to be insignificant at the rated current of the diode.

Figure 2-4 shows the V-I characteristics (per diode) of Fairchild's bridge rectifiers with different current ratings. It can be shown that the device GBPC35 with the highest current rating of 35 A provides the least forward drop at high current but behaves similarly to the lowest rated diode GBPC12 (12 A) at low current region where the forward voltage is dominated by the physical characteristics of the junction. From the power loss viewpoint, rectifiers at a higher current rating have less power loss due to resistive voltage drop, but the loss in circuit level due to the junction characteristics remains significant, as shown in Figure 2-5.

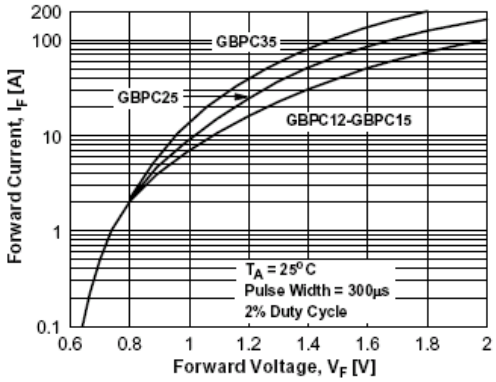


Figure 2-4: I_F –V_F plot of four 600 V bridge rectifiers from Fairchild with current rating of 12 – 35A (extracted from datasheet - GBPC 12, 15, 25, 35 series Rev. C1 of Fairchild Semiconductor Corporation).

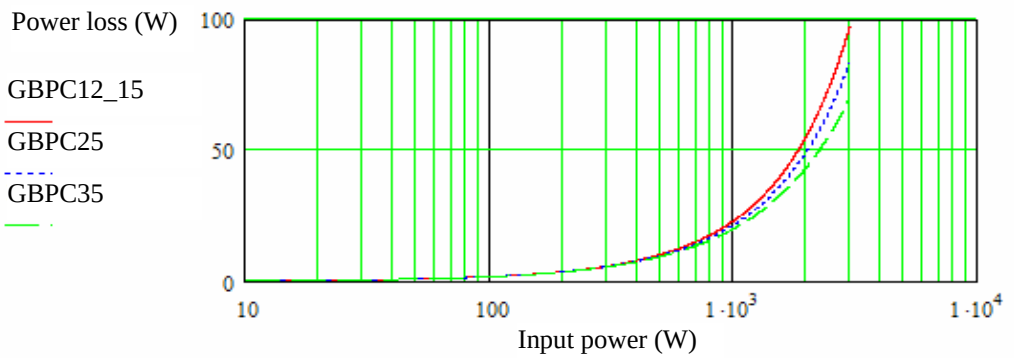


Figure 2-5: Power loss of the bridge rectifiers at different input power levels.

2.3 Loss Introduced by Conventional Front-end AC/DC Conversion

The major and irreducible loss of the front-end AC/DC conversion is due to the input bridge rectifier. In this section, rectifier losses of both the conventional peak and follower rectifiers are analyzed for different mains voltage (from 30 Vrms to 264 Vrms) and power levels (from 10 W to 300 W). For the peak rectifier, since the input current profile, which affects the loss, depends on the value of the filtering capacitor, different ripple voltage levels of the output voltage (e.g., 20%, 10%, 5% and 1%) should be considered in the analysis. As described in the previous sections, the irreducible part of the power loss in diode rectifiers is due to the diode junction characteristics and the bulk resistance of semiconductor. To reveal the practical problem concerning this irreducible loss, the current rating of the bridge rectifier used for the analysis is higher than the current being handled in order to minimize the controllable loss caused by the resistance of the diode. The bridge rectifier GBPC15-600, which has a rated reverse breakdown voltage of 600 V and rated average current of 15 A, is chosen for the analysis.

2.3.1 Loss in bridge rectifiers in conventional front-end AC/DC conversion vs. input mains voltage

Figure 2-6 shows a plot of the loss of the input bridge rectifier in terms of the percentage of input power against the input mains voltage. The power level used for the test is 300 W. The traces $P_{\mathrm{Vfollower}}$, $P_{\mathrm{V20\%}}$, $P_{\mathrm{V10\%}}$, $P_{5\%}$ and $P_{\mathrm{V1\%}}$ show the calculated results for the follower rectifier, the peak rectifier with output ripple voltage of 20%, 10%, 5% and 1% of the DC voltage, respectively. It can be observed that the loss increases as the input voltage decreases. The results are

obvious because the voltage drop of the rectifying diodes become more significant when the input voltage is low. Figure 2-6 also indicates that the loss depends on the output ripple voltage. Lower output ripple voltage requires larger filtering capacitor, which in turn reduces the conduction angle, increases the crest factor as well the rms current of the input bridge rectifier. The loss thus increases.

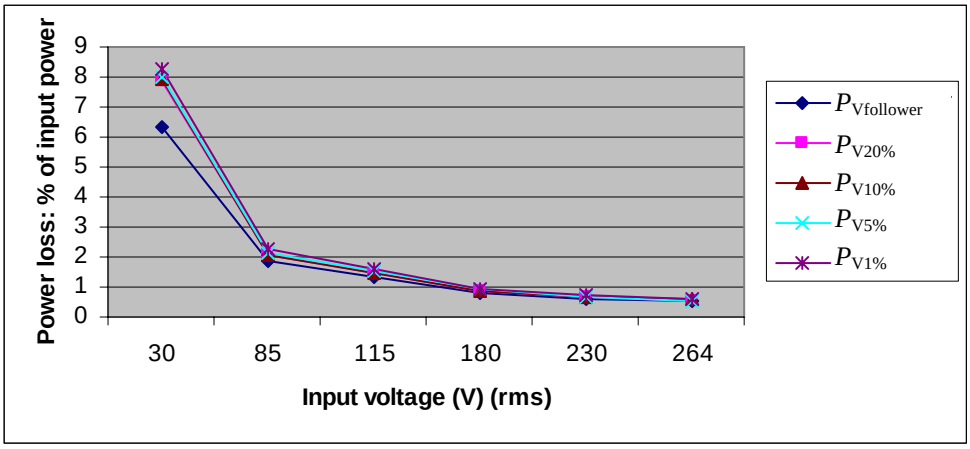


Figure 2-6: Loss of input rectifier in terms of % of input power (300 W) against mains voltage.

At 85 Vrms input (usually the lowest value of the universal input range), 2% of the input power is wasted in the input bridge rectifier. Figure 2-7 shows the percentage of total loss contributed by the input bridge rectifier with the assumption that the total conversion efficiency of the power converters is 92%. More than 20% of the total loss of the converter is due to the input bridge rectifier.

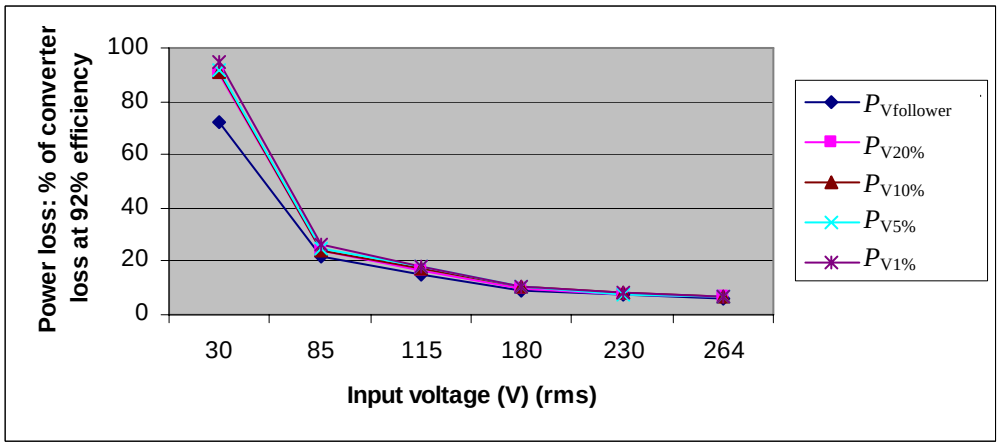


Figure 2-7: Loss of input bridge rectifier in terms of % of converter loss against mains voltage. Overall converter efficiency is 92%.

2.3.2 Loss in bridge rectifiers in conventional front-end AC/DC conversion vs. input power

Figure 2-8 and Figure 2-9 show the power loss of bridge rectifiers against different input power levels ranging from 10 W to 300 W at 85 Vrms input. The actual loss, as well as the contribution to the total loss, increases with the input power. Since the current rating of the bridge rectifier used for the calculations is sufficiently high that the resistive loss is not significant, the characteristics shown in the two plots are dominated by the irreducible junction loss.

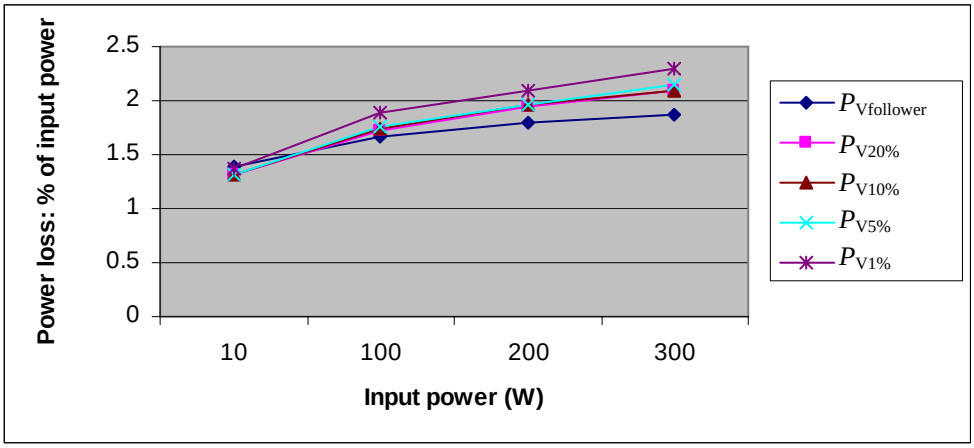


Figure 2-8: Loss of input rectifier in terms of % of input power against input power.

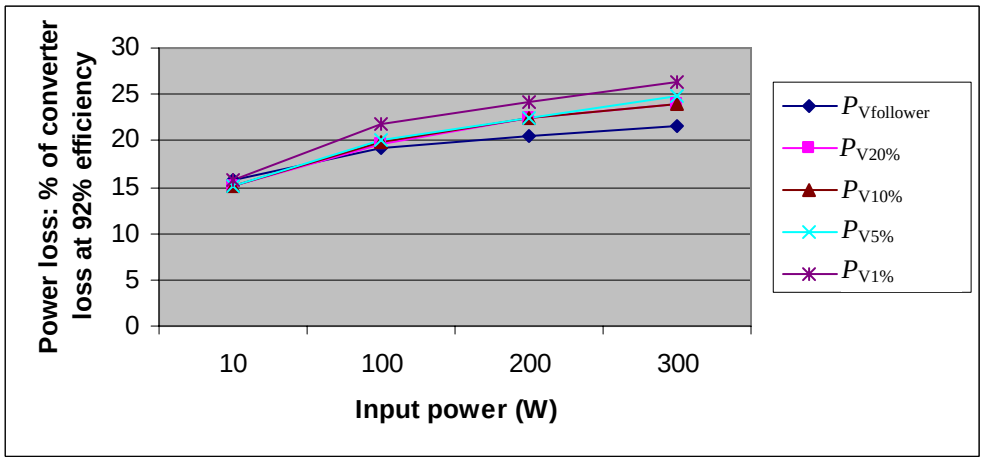


Figure 2-9: Loss of input rectifier in terms of % of power loss against input power. Overall converter efficiency is 92%.

2.3.3 Loss in the bridge rectifier in a practical 300 W PFC regulator design

The photo and specifications of a 300 W PFC regulator provided by semi-conductor manufacturer Infineon as an evaluation board is shown in Figure 2-10.

(a)

Input voltage	85 VAC – 264 VAC
Input frequency	50 Hz
Output voltage and current	400 VDC, 0.75 A
Output power	300 W
Overall conversion efficiency	>90% at full load
Switching frequency	62.5 kHz

(b)

Figure 2-10: (a) A 300 W PFC evaluation board from Infineon and (b) specifications (extracted from the application note – EVALPFC2-ICE1PCS01 V2.0 of Infineon Technologies Asia Pacific).

The circuit topology employs a conventional front-end follower rectifier plus a DC/DC boost converter. The power losses and the contributions to the total power loss of major components are evaluated by PowerEsim[1] at 85 Vrms input and the results are shown in Table 2-1. Among the main power components of the PFC regulator, the input bridge has the highest loss and contributes to 25.66% of the total power loss which matches with the analysis given in the previous sections.

Table 2-1: Loss distributions of major components.

Component description	Part no.	Power loss	Percentage power loss
Input bridge rectifier	RBU805M	5.66 W	25.66%
Boost inductor 1.208mH	-	4.486 W	20.34%
Boost MOSFET	SPP20N60C3	3.516 W	15.94%
Boost diode	SDP04S60	1.445 W	6.553%

[1] PowerESim is a switching converter simulator developed by PowerELab Limited.

2.4 Input Current Harmonic Distortion Caused by Conventional Front-end AC/DC Conversion

The harmonic currents drawn from the AC mains by electronic equipment including switching converters are required to comply with international regulations like EN61000-3-2 and DO160 (for aircraft power system with high mains frequency of 400 Hz). The limits of the two standards are shown in Table 2-2 to Table 2-6.

Table 2-2: Class A limits of EN61000-3-2.

EN61000-3-2 Class A limits	
Harmonic Order *n*	Maximum permissible harmonic current Ampere
Odd harmonics	
3	2.30
5	1.14
7	0.77
9	0.40
11	0.33
13	0.21
$15 \leq n \leq 39$	$0.15 * 15/n$
Even harmonics	
2	1.08
4	0.43
6	0.3
$8 \leq n \leq 40$	$0.23 * 8/n$

Table 2-3: Class B limits of EN61000-3-2.

EN61000-3-2 Class B limits	
Harmonic Order *n*	Maximum permissible harmonic current Ampere
Odd harmonics	
Odd harmonics	1.5 * limits of Class A
Even harmonics	
Even harmonics	1.5 * limits of Class A

Table 2-4: Class C limits of EN61000-3-2.

EN61000-3-2 Class C limits	
Harmonic Order *n*	Maximum permissible harmonic current % of $I_{fundamental}$
2	2
3	30 *circuit power factor
5	10
7	7
9	5
11≤ *n* ≤39 (odd harmonics only)	3

Table 2-5: Class D limits of EN61000-3-2.

EN61000-3-2 Class D limits	
Harmonic Order *n*	Maximum permissible harmonic current mA/Watt
Odd harmonics	
3	3.4
5	1.9
7	1.0
9	0.5
11	0.35
13≤ *n* ≤39	3.85/*n*

Table 2-6: Current harmonics limits of DO160 for aircraft power system.

DO160 harmonic current limits	
Harmonic order	Maximum permissible harmonic current (single phase) % of $I_{fundamental}$
Odd harmonics	
Odd Triplen (n = 3, 9,……39)	15/*n*
Odd non-Triplen (*n* ≤ 37)	30/*n*
Even harmonics	
n = 2, 4	1/*n*
6 ≤ *n* ≤ 40	0.25/*n*

2.4.1 Current harmonic distortion generated by conventional peak rectifiers

Because of the use of large filtering capacitance, the input current conduction angle is small and high current harmonics is generated. Figure 2-11 and Figure 2-12 show the peak rectifier schematic and the simulated waveforms, respectively. The

mains voltage is 220 Vrms, 50 Hz, and the input power of the circuit is 75 W (the lowest power level that falls under the Class D EN61000-3-2 standard). The input current conducts only near the peak of the input sinusoidal voltage and the simulated current harmonics is listed in Table 2-7 with the EN61000-3-2 limits for comparison. The results show that the peak rectifier circuit cannot pass the regulation and the situation is even worse when the power level increases. This implies that the use of conventional peak rectifier circuit for input power levels higher than 75 W would fail to comply with EN61000-3-2 standard.

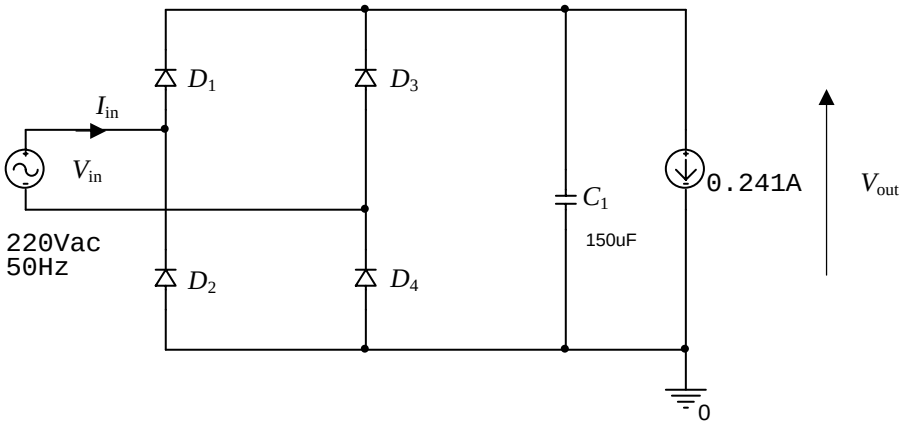


Figure 2-11: Peak rectifier AC/DC conversion with output power of 75 W.

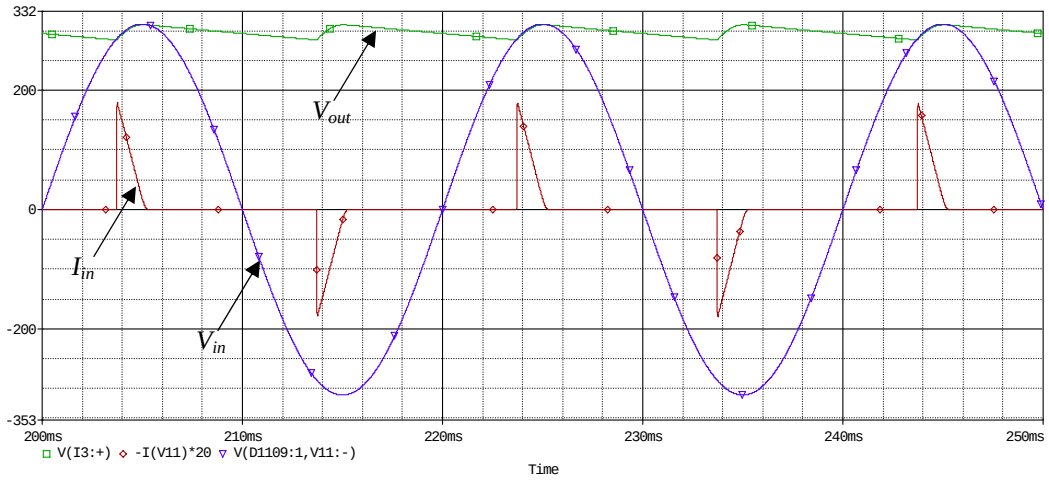


Figure 2-12: Simulated waveforms of input voltage (V_{in}), input current (I_{in}) and output voltage (V_{out}).

Table 2-7: Simulated current harmonics generated from the 75 W front-end peak rectifier.

Harmonic order	Simulated current harmonics /mA	EN61000-3-2 Class D limit /mA	Results
3	438.86	255.00	Fail
5	334.03	142.50	Fail
7	325.15	75.00	Fail
9	273.62	37.50	Fail
11	238.09	26.25	Fail
13	193.67	22.21	Fail
15	149.00	19.25	Fail

2.4.2 Current harmonics generated by conventional follower rectifiers

The PFC switching regulator, which offers a resistive input characteristic, has solved most of the problems in meeting the international standards. The conventional circuit topology used for realizing the PFC function is shown in Figure 2-1 (a). It is composed of a follower rectifier for the front-end AC/DC conversion, followed by a DC/DC boost converter with suitable control. The follower rectifier is usually realized by a bridge rectifier and a low value capacitor which usually ranges from ~10 nF to several μF depending on the ripple current required to be handled. In general, the method can be applied in domestic AC mains applications, but researchers [S02] revealed that the current harmonic distortion caused by the follower rectifier could be serious at high mains frequencies such as those used in aircraft power systems.

2.4.2.1 Root causes of the distortions in follower rectifiers

In the follower rectifier, although the value of the filtering capacitor is small, the current demanded by the boost converter with a resistive input characteristic is also small. This makes the discharging rate of the capacitor lower than the rate of change of the input AC mains around the zero-crossing. During a finite interval of

time which depends on the capacitance of the filtering capacitor and the power demanded by the boost converter, the capacitor voltage does not follow the voltage waveforms of the AC mains. Figure 2-13 shows the schematic of follower rectifier, and Figure 2-14 and Figure 2-15 show the operating waveforms.

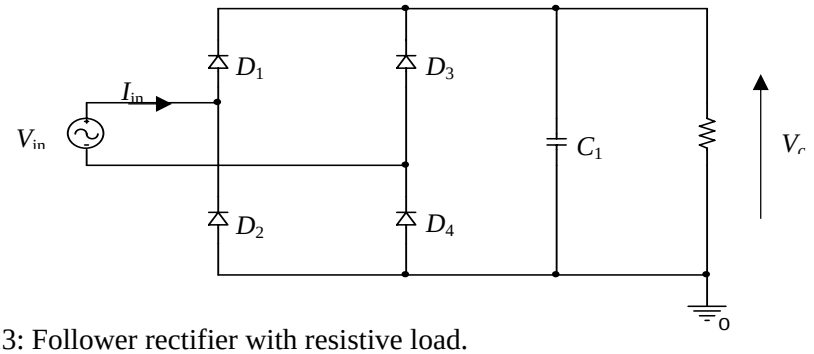


Figure 2-13: Follower rectifier with resistive load.

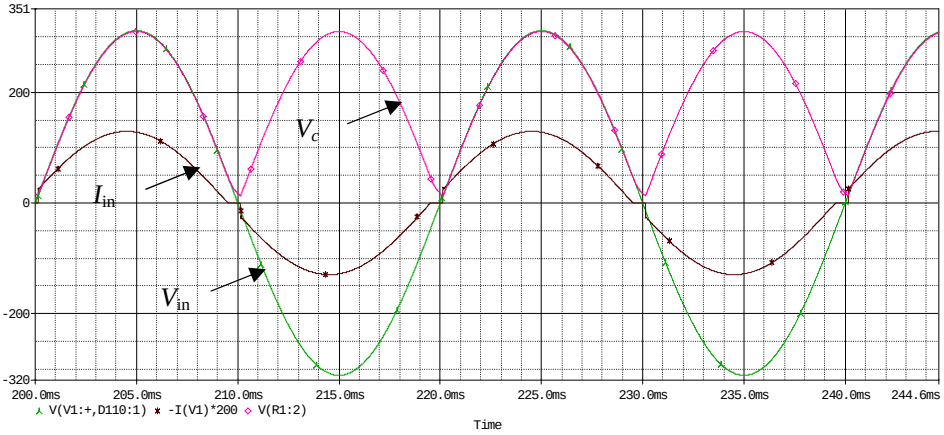


Figure 2-14: Waveforms of follower rectifier with resistive load.

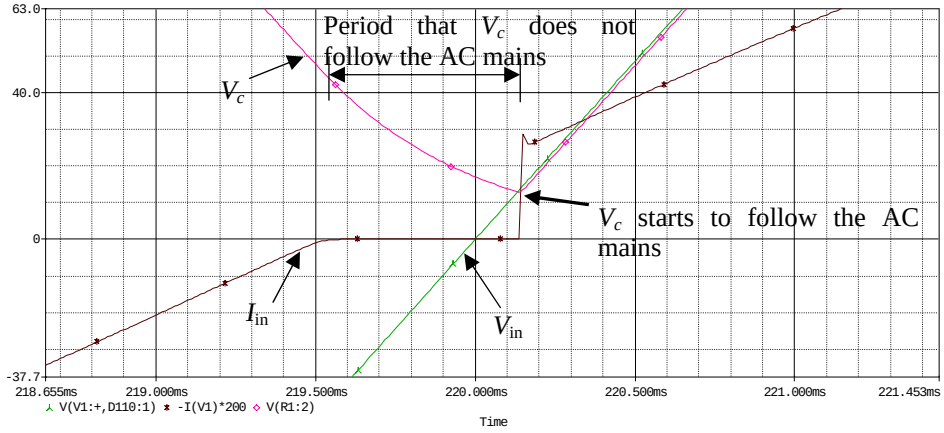


Figure 2-15: Close-up view at the mains zero-crossing region of follower rectifier with resistive load.

During the period when V_c does not follow the AC mains voltage, the input bridge is reverse biased even when the input voltage is positive. As soon as the mains voltage catches up with the voltage across C_1 that forward biases the bridge rectifier, current starts to conduct again. This dead zone creates the crossover distortion. The time period of the dead zone and the significance of the distortion created are expected to increase with the value of the filtering capacitor and the mains frequency. Some researchers [S02, S05, LL06, PCS05] attributed the distortion to the current drawn.

2.4.2.2 Simulated results of the cross-over distortion

Crossover distortion in terms of amplitudes of current harmonics of a follower rectifier with a resistive load (perfect PFC) is simulated by PSPICE. The input voltage and the input power are fixed at 220 Vac and 100 W, respectively, with the input mains frequency f_{in} and the filtering capacitor value C_1 varied. The results are compared with the international standards in Table 2-8 to Table 2-11 and the corresponding input current waveforms are shown in Figure 2-16 to Figure 2-19. Current harmonics are recorded up to the 21st order. The current harmonics at 400 Hz mains frequency are significantly higher than those at 50 Hz. With C_1 changed from 0.1 μF to 1 μF, the amount of current harmonics increases for both mains frequencies, but becomes very significant in the case of f_{in} = 400 Hz. The distortion level can be reflected from the input current waveforms. Generous margins can be observed in the case of f_{in} = 50 Hz when compared with the class D limits of EN61000-3-2 with typical values of C_1. However, for the 400 Hz case, with C_1 = 1 μF, it fails to meet the more stringent DO160 limits for aircraft power systems.

Table 2-8: Current harmonics with V_{in}= 220 Vac, f_{in} = 50 Hz, P_{in} = 100 W, and C_1 = 0.1 μF.

Harmonic order *n*	Simulated harmonic current /mA	EN61000-3-2 class D limits /mA	Results
3	8.84	340	Pass
5	6.63	190	Pass
7	6.26	100	Pass
9	5.57	50	Pass
11	5.24	35	Pass
13	4.88	29.61	Pass
15	4.49	25.66	Pass

Table 2-9: Current harmonics with V_{in}= 220 Vac, f_{in} = 50 Hz, P_{in} = 100 W, and C_1 = 1 μF.

Harmonic order *n*	Simulated harmonic current /mA	EN61000-3-2 class D limits /mA	Results
3	4.89	340	Pass
5	1.83	190	Pass
7	1.05	100	Pass
9	0.68	50	Pass
11	0.49	35	Pass
13	0.39	29.61	Pass
15	0.32	25.66	Pass

Table 2-10: Current harmonics with V_{in}= 220 Vac, f_{in} = 400 Hz, P_{in} = 100 W, and C_1 = 0.1 μF.

Harmonic order *n*	Simulated harmonic current /mA	DO160 limits /mA	Results
1	642.88	-	-
3	5.338	32.144	Pass
5	5.153	38.572	Pass
7	4.999	27.552	Pass
9	4.844	10.714	Pass
11	4.690	17.533	Pass
13	4.505	14.835	Pass
15	4.320	6.428	Pass
17	4.104	11.344	Pass
19	3.888	10.150	Pass
21	3.641	4.592	Pass

Table 2-11: Current harmonics with V_{in}= 220 Vac, f_{in} = 400 Hz, P_{in} = 100 W, and C_1 = 1 μF.

Harmonic order *n*	Simulated harmonic current /mA	DO160 limits /mA	Results
1	746.381	-	-
3	276.676	37.319	Fail
5	126.542	44.782	Fail
7	77.212	31.987	Fail
9	72.922	12.439	Fail
11	49.33	20.355	Fail
13	47.185	17.224	Fail
15	40.751	7.463	Fail
17	32.172	13.171	Fail
19	31.165	11.784	Fail
21	27.882	5.331	Fail

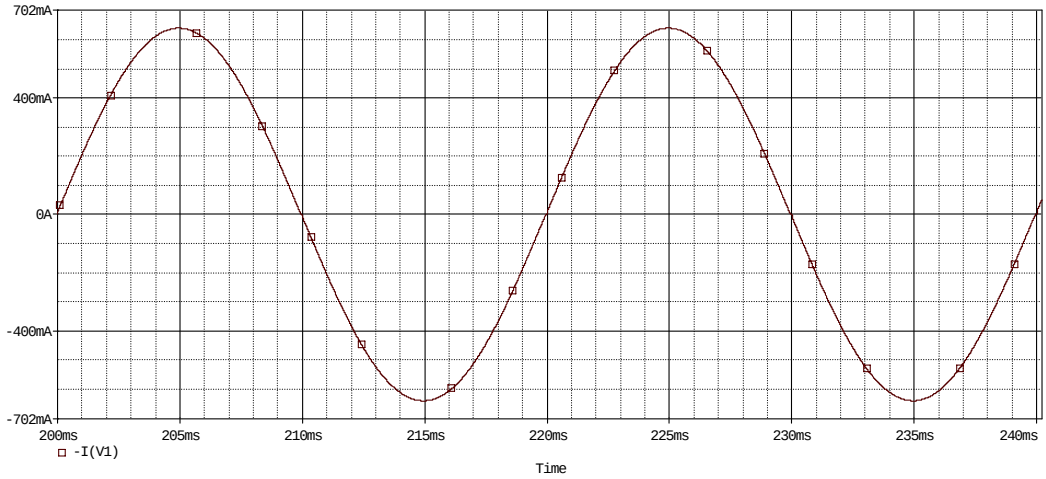


Figure 2-16: Input current with V_{in}= 220 Vac, f_{in} = 50 Hz, P_{in} = 100 W, and C_1 = 0.1 μF.

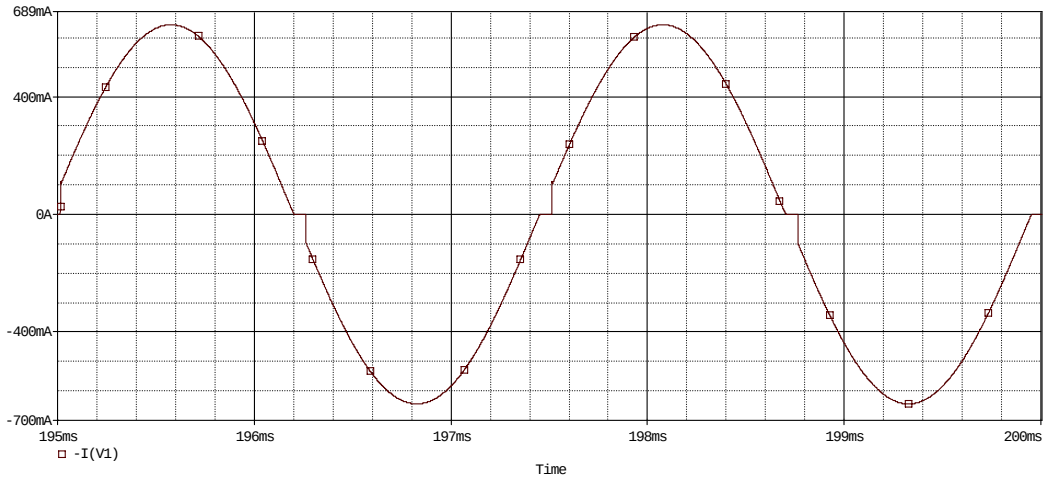


Figure 2-17: Input current with V_{in}= 220 Vac, f_{in} = 50 Hz, P_{in} = 100 W, and C_1 = 1 μF.

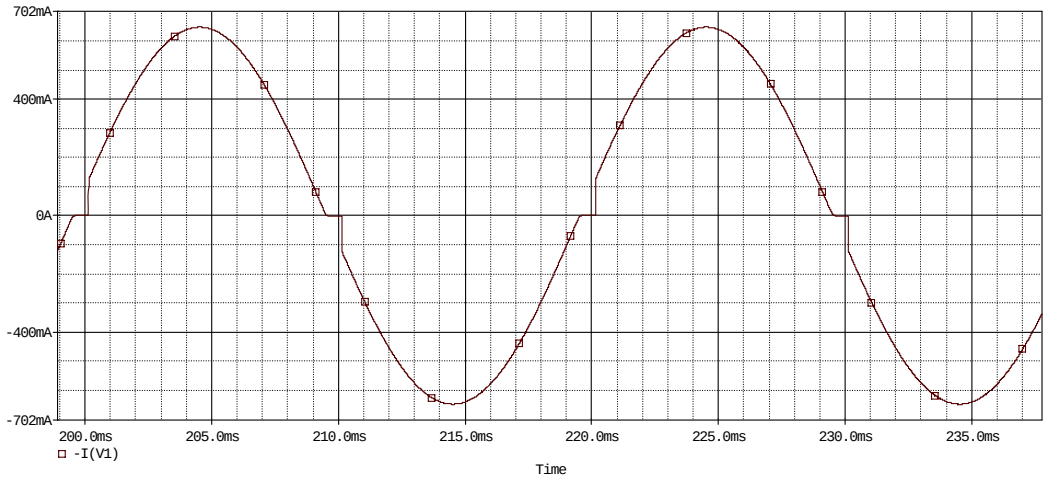


Figure 2-18: Input current with V_{in}= 220 Vac, f_{in} = 400 Hz, P_{in} = 100 W, and C_1 = 0.1 μF.

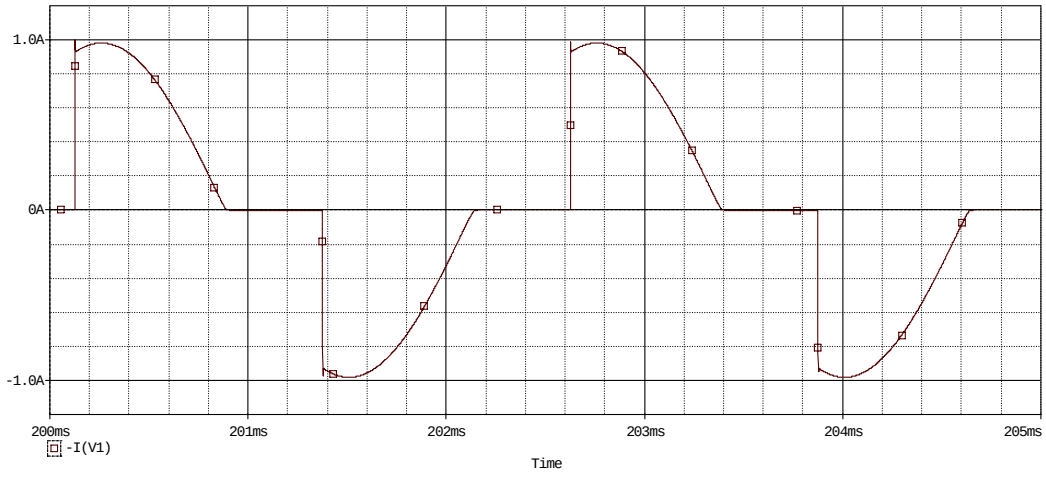


Figure 2-19: Input current with V_{in}= 220 Vac, f_{in} = 400 Hz, P_{in} = 100 W, and C_1 = 1 μF.

2.5 Conclusion

In this chapter, we analyze the loss and the input current harmonics produced by the conventional front-end AC/DC conversion, which consists of a bridge rectifier and filtering capacitors. The two major problems are found to be caused by the input rectifiers. The loss introduced by the input rectifiers generally contribute more than 20% of the total power loss of switching converters and it is irreducible due to the physical properties of diode forward junction voltage. This makes the input rectifiers

usually the hottest components found in today's high efficiency converters. It represents an obstacle for further improving the power density and conversion efficiency of switching converters to meet future requirements. As for the input current harmonics, it has been shown that the conventional rectifying circuits alone can fail to meet the stringent requirements, such as the DO160 for aircraft power systems at a high mains frequency. When the PFC converter provides imperfect resistive characteristic and the dynamic response is considered, the total distortion generated can be more severe. In addition, variable and higher mains frequency ranging from 360 Hz to 800 Hz may be used in the future aircrafts [S02]. This makes converter design with conventional techniques very difficult.

Chapter 3 Review of the Output High-Frequency AC/DC Conversion

3.1 Introduction

The output AC/DC conversion performs mainly two functions. The first is to rectify the high-frequency switched AC signal from the main transformer and the second is to filter the high-frequency components of the rectified voltage and provides smooth DC output. Although many switching converter topologies exist, the circuit configurations being used for the conversion are predominantly the traditional half-wave and full-wave rectifier followed by an *LC* filter.

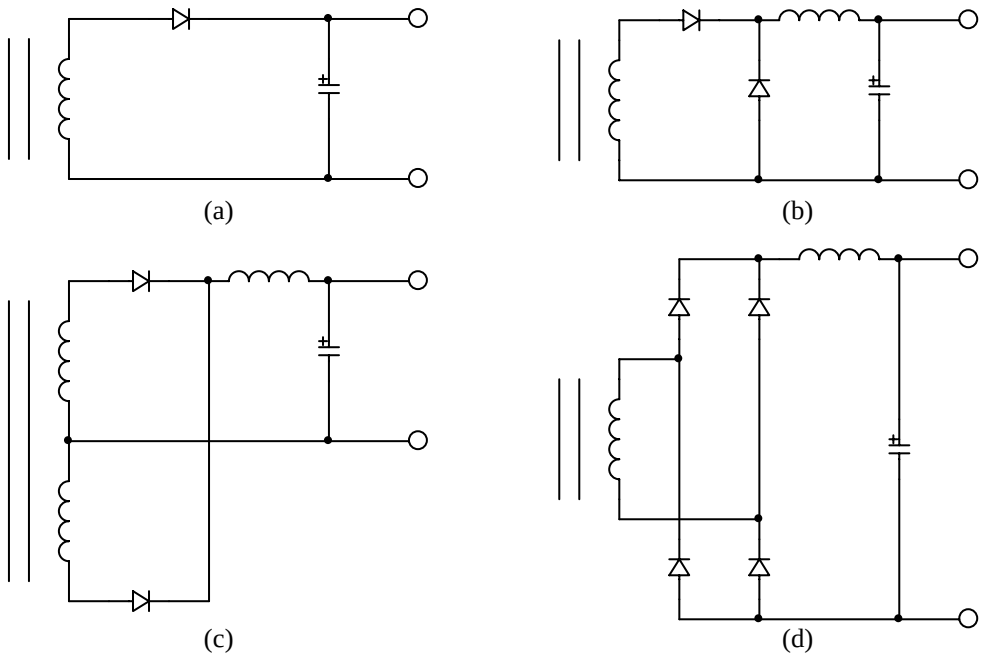


Figure 3-1: Conventional output AC/DC conversion circuits in isolated converters. (a) and (b) Half-wave configurations; (c) and (d) full-wave configurations.

Figure 3-1 shows the circuit configurations that are generally used. The circuits can be divided into two parts, the rectifying circuit and the low-pass *LC* filter. This

chapter reviews the power loss of the rectifying circuits and the problems encountered in the output filter design, with special considerations of the current industrial requirements and trends of low output voltage, high output current and low output ripple and noise.

3.2 Power Loss in the Output Rectifying Circuit

Unlike the front-end low-frequency AC/DC conversion discussed in Chapter 2, the switching loss of output rectifiers can be significant because they are operating at a switching frequency which ranges from tens to hundreds of kHz. The operating frequency of switching converters is expected to rise continuously because of the high power density requirement. On the other hand, the rectifier's voltage drop can be comparable to the output voltage. Coupled with the high output current requirement, the conduction loss of output rectifiers reduces the overall conversion efficiency considerably. In the following sections, both the switching loss and conduction loss of output rectifiers are analyzed. The performance of different rectifier types will be discussed.

3.2.1 Switching loss of output rectifiers

The switching loss of output rectifiers is mainly due to the reverse recovery time [LG90] when the rectifiers are turned off. In all hard switched topologies, output rectifiers are turned off by a low-impedance voltage source and the equivalent circuit is shown in Figure 3-2. The low impedance that limits the rate of change of the rectifier current is usually provided by the parasitic inductance of circuit connections and the leakage inductance of the main transformer. Figure 3-3

shows typical diode voltage and current waveforms during the turn-off phase. The diode D shown in Figure 3-2 starts to turn off when the reverse voltage V_R is applied. The diode current starts to fall at a rate of $di_D/dt = V_R/L$. Reverse current flow occurs during the reverse recovery time t_{rr} which is divided into two parts: t_a and t_b. In the period t_a, the reverse current removes the charges stored in the junction during forward conduction and this period increases with the amplitude of the forward current. During this period, the diode voltage is kept low and the loss introduced is negligible. After the period t_a, the reverse diode voltage starts to build up as the reverse current continues to remove the remaining stored charges for the period t_b. The energy loss E_r during this period is significant and is given by (3-1), assuming a linear rate of change of diode current and voltage. The switching power loss of diode D is simply the product of E_r and the switching frequency f_{sw}, as given in (3-2).

$$E_r = \frac{V_R^2 \cdot t_a \cdot t_b}{4 \cdot L} \tag{3-1}$$

$$P_{sw} = \frac{V_R^2 \cdot t_a \cdot t_b}{4 \cdot L} \cdot f_{sw} \tag{3-2}$$

For example, for an ulta-fast p-n junction diode with t_a = 20 ns and t_b = 40 ns (t_{rr} = 60 ns) under the operating conditions of f_{sw} = 300 kHz, V_R = 30 V and L = 50 nH, the rate of change of diode current di_D/dt is limited to 600 A/μs and the loss calculated from (3-2) is 1.08 W.

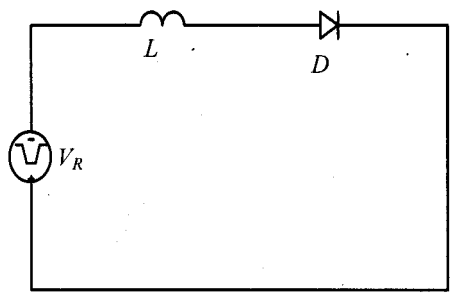


Figure 3-2: A general equivalent circuit to represent the turning off of a diode rectifier.

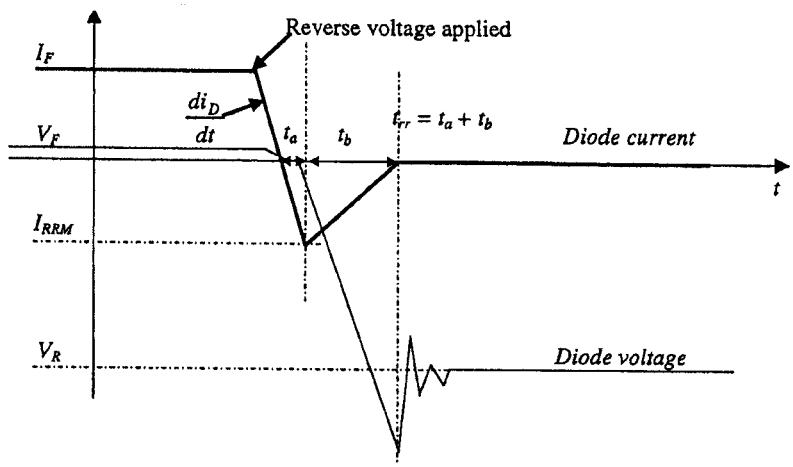


Figure 3-3: Typical reverse recovery waveforms of diode rectifier.

From (3-2), we can observe that the switching loss of a diode rectifier increases with the switching frequency, the reverse recovery time and especially the applied reverse voltage since the loss is proportional to the square of the reverse voltage amplitude.

3.2.2 Conduction loss of output rectifiers

The conduction loss of an output rectifier operating at a high switching frequency is mainly due to the rectifier forward voltage drop. Since the AC voltage handled by output rectifiers is usually quite low, the power loss due to the output rectifier voltage drop is far more significant than that in the AC mains side. The efficiency of the output AC/DC conversion is given by (3-3). Figure 3-4 shows the calculated efficiency for Schottky diodes with typical forward voltage drop of 0.4 V at high current. The range of output voltage given in the plot is typical of low-voltage converters. It can be observed that the loss is more than 30% for the case of $V_o = 0.8$ V.

$$Eff_{\text{rectifier}} = \frac{V_o}{V_o + V_D} \tag{3-3}$$

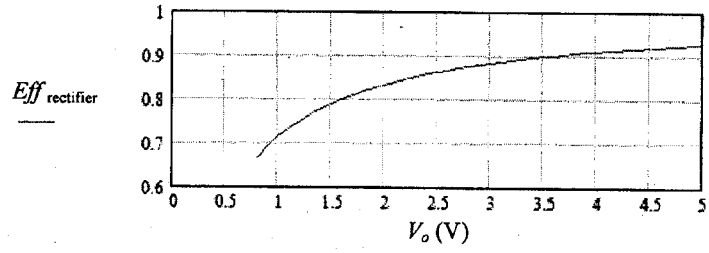


Figure 3-4: A plot of efficiency due to output Schottky rectifier with forward drop = 0.4 V.

3.2.3 Performance of different rectifier types for the output AC/DC conversion

Different types of rectifiers have different performances in terms of conduction loss and switching loss. This section gives a brief discussion on the issue.

3.2.3.1 P-n junction diode for output AC/DC conversion

The forward voltage drop of p-n junction diodes is about 1 to 1.2 V. This type of diodes is usually used in converters with high output voltage (>24 V) because the conversion efficiency is too low for low output voltage converters.

A wide range of t_{rr} can be found in this type of diodes for different applications. The ultra-fast type, with t_{rr} ranging from ~15 ns to 100 ns, is usually used for the output AC/DC conversion. The switching loss can be large and comparable to the conduction loss in some applications where the reverse voltage is high and the driving impedance is low for turning off the diode rectifier at high forward current, as described in Section 3.2.1. These limit the applications of this type of diode rectifiers to low output voltage and high output current converters.

3.2.3.2 Schottky diodes for output AC/DC conversion

Schottky diodes have the lowest forward voltage drop, which is about half of the forward voltage drop of p-n junction diodes. This makes the Schottky diode a

popular choice for converters whose output voltage is as low as 3.3 V. For low output voltage applications, the diode drop becomes significant and synchronous rectification using MOSFETs is preferred.

As for the switching loss, Schottky diodes exhibit negligible reverse recovery time and provide excellent switching characteristic that makes them suitable for very high frequency operation.

3.2.3.3 Synchronous rectifiers for output AC/DC conversion

Today's MOSFETs provide very low on-state resistance, which is in the order of milli-ohm. With suitable driving signals, MOSFETs can be arranged to operate as synchronous rectifiers which have very low conduction loss [LOO95]. Easy parallel operation of MOSFETs makes it easy to control the power loss to a desired level. The use of synchronous rectifiers for the output AC/DC conversion reduces the conduction loss by an order of magnitude when compared to diode rectifiers. This makes the synchronous rectifier a good choice for AC/DC conversion in low voltage and high current applications.

As for the switching loss, synchronous rectifiers are similar to the ultra-fast p-n junction diodes described in Section 3.2.1 because of the presence of an inherent body diode [LOO95] in parallel with the MOSFET conduction channel. Usually, the loss of synchronous rectifiers is dominated by the switching loss because of the high switching frequency. This dims the merit of synchronous rectifiers and imposes a limit to the usable switching frequency.

3.3 Problems of Output Filter Circuits for Low Voltage and High Current Applications

Because of the high operating frequency of the output AC/DC conversion, magnetic components are usually used together with capacitors to form a high-order filter for effective reduction of switching noise. In general, industrial standard requires the output ripple and noise voltage to be within 1% of the output voltage. This makes the design of output filter for low output voltage applications very difficult when size and loss are taken into consideration.

The conventional output filter consists of an inductor and a capacitor to form a second-order low-pass filter. In practice, there are mainly three ways to meet the stringent ripple and noise requirement, namely, reducing the equivalent series resistance (ESR) of the filter capacitor, increasing the inductance of the output choke, and increasing the switching frequency. The pros and cons of these three methods will be discussed below.

3.3.1 Reducing ESR of output filter capacitor

Since the output ripple voltage is proportional to the ESR of the output capacitor, reducing the ESR can effectively lower the ripple voltage level as well as the power loss of the output capacitor. Ideally, this can be accomplished by connecting capacitors in parallel, which effectively divides the ESR by the number of capacitors used. Practically the connections between the capacitors introduce resistance and inductance, and will limit the effectiveness of parallel operation. In addition, the increase in the number of output capacitors increases the size of the converter.

3.3.2 Increasing inductance of output inductor

This can reduce the output ripple current and hence the output voltage ripple. To handle the same current with larger inductance, larger cores are required in order to lower the magnetic flux density to prevent core saturation. This increases the converter size and reduces the power density. Large inductance can also be achieved by increasing the number of winding turns of the inductor at the expense of higher conduction loss. To ensure low conduction loss at high current operation, special winding structures using thick copper strips are required. Figure 3-5 shows inductor windings for high current operation.

Figure 3-5: Output inductor with multiple turns using thick copper strip.

3.3.3 Increasing converter switching frequency

The output ripple current is inversely proportional to the converter switching frequency. Thus, the output voltage ripple can be reduced by increasing the switching frequency, which in turn reduces the size of the magnetic core as well as the required number of turns of the output inductor, resulting in lower conduction loss. However, this also brings along increased switching loss of rectifiers and power switches.

3.3.4 Reducing output ripple by circuit design

Some topologies provide small output ripple by using coupled inductors or paralleling converters with ripple cancellation. Current interleaved converter topologies are widely used because of their excellent output ripple cancellation [C95, R98, WXYL00, XRYL01] that significantly alleviates the demand for output capacitors. The size of output inductors can also be reduced since large ripple current is allowed in the individual converters. On the other hand, when considering the loss, the inductance of the output inductor in each converter cannot be reduced drastically since large ripple current will increase the conduction loss in the individual converters. In addition, the effect of output ripple cancellation is highly dependent upon the operating duty cycle, and the resulting output ripple current can be unexpectedly high when the operating duty cycle deviates from the designed value [LPP03]. This requires an output capacitor bank to be installed for the worst-case ripple cancellation.

3.4 Conclusion

The major problems of the conventional high-frequency AC/DC conversion at the output of switching converter have been reviewed. The switching loss and conduction loss of different rectifier types are analyzed, with special emphasis on the low voltage and high current applications. Synchronous rectifiers using MOSFETs represent a very feasible solution to the reduction of conduction loss. However, the switching loss due to the inherent body diode characteristics has to be further reduced. It has been shown that the switching loss of rectifiers can be significantly reduced by lowering the reverse voltage during the turn-off period.

This provides useful insights into new topology development. As for the output filter part, the limitations of conventional methods for reducing loss, size and output ripple for low voltage and high current applications have been described. The widely used current interleaved converters for output ripple current cancellation have been briefly discussed. The ripple cancellation effect in current interleaved converters is sensitive to the operating duty cycle. This poses a design problem and limits the effectiveness of the output filter. The problems studied in this chapter provide useful insights for the development of new techniques for the output AC/DC conversion, as will be discussed in detail in Chapter 7.

Chapter 4 Synthesis of Input Rectifierless Converters

The two major problems discussed in Chapter 2, namely, the irreducible loss and the zero-crossing distortion, introduced by conventional front-end AC to DC conversion circuits are basically created by the input rectifiers. Removing the front-end rectifiers seems to be the ultimate solution to the problems. Instead of looking into particular rectifierless AC/DC converter topologies, this chapter discusses the basic construction procedures and topological possibilities of creating rectifierless AC/DC converters out of simple DC/DC converters. Based on the proposed procedures, simple DC/DC converters, e.g., buck, buck-boost and boost converters, can be used to realize rectifierless AC/DC conversion.

It will be shown that the composition of two separately controlled DC/DC converters are sufficient for producing a regulated DC output voltage and shaping the input current, without the need for input rectifiers. Some design constraints will be discussed, emanating from the limitation of the conversion ratios that can be achieved by particular DC/DC converters. Selected topologies are verified experimentally. This kind of rectifierless converters finds applications in airborne power supplies and general impedance synthesizer where low input current harmonic distortions are required.

4.1 Introduction

AC/DC converters without input rectifiers have received some attention because of their relative advantages in eliminating power loss in rectifiers and reducing

harmonic distortions. In airborne applications where the mains frequency is as high as several hundreds Hz, the phase-lead effect of the input rectifier bridge in a PFC converter has been found to cause significant zero-crossing distortions which are impossible to eliminate [S02]. Without input rectifiers, AC/DC converters would be free from zero-crossing distortions.

One straightforward approach to implement a rectifierless AC/DC converter is to construct two circuits (two complete converters), each working for either positive or negative half cycle of the line period. This approach, however, requires rather complicated circuits [KB98]. Another possibility is to put the equivalent rectification in the secondary side where the diodes perform high-frequency as well as line-frequency rectification. This approach usually requires four quadrant switches and complicated topologies. Also, the high-current low-voltage condition in the secondary may present difficulty in raising the overall efficiency [SE94]. Recently, suitable converters having inherent AC/DC conversion capability have been studied by Ikriannikov and Cuk [IC99]. However, such converters, known as bipolar-gain converters [IC99], do not seem to have a systematic origin from which general synthesis procedures can be derived.

In this chapter we consider the fundamental synthesis problem of a converter that converts an unrectified AC voltage to a DC voltage, without using an input rectifier. Our aim is to derive the simplest topology for AC/DC conversion, based on a combination of DC/DC converters.

4.2 Derivation of the Simplest Rectifierless AC/DC Converter

We begin with a black-box specification of AC/DC conversion. Let $u(t)$ be the output voltage, and $e(t)$ be the input voltage. The AC/DC conversion specifies that

$$\begin{cases} u(t) = U \\ e(t) = E \cdot \sin(2 \cdot \pi \cdot f_{\mathrm{e}} \cdot t) \end{cases} \qquad (4\text{-}1)$$

In other words, we consider the usual conversion of a sinusoidal input voltage having a peak of E and frequency f_e into a fixed output voltage U. Our purpose is to derive the simplest input-rectifierless topology based on DC/DC converters that can fulfill the above black-box requirement.

4.2.1 Basic construction

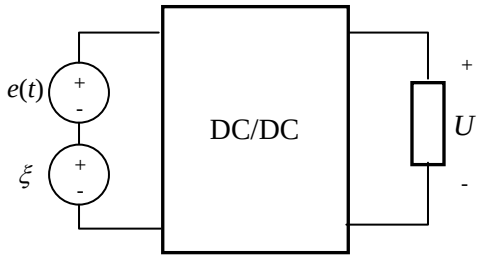
First of all, we observe that simple DC/DC converters only convert a DC voltage to another DC voltage. Thus, the use of a DC/DC converter for AC/DC conversion is handicapped mainly by its input side which cannot admit negative voltage values. The problem can be hypothetically solved if one stacks up a sufficiently large DC voltage over the AC input voltage before feeding into a DC/DC converter. This idea is illustrated in Figure 4-1(a), where ξ denotes the stack-up voltage. Obviously, we need

$$\xi > E \qquad (4\text{-}2)$$

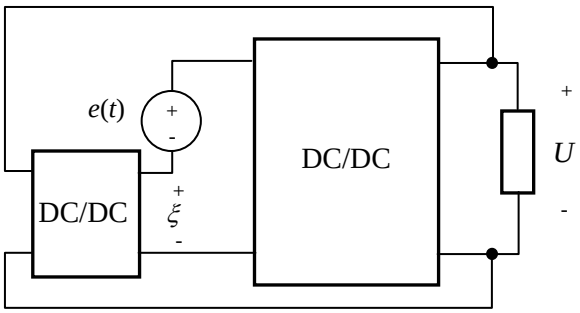
Our next logical step is to create the required ξ. Clearly we need a second DC/DC converter which choicelessly must convert from the output voltage U. This gives the basic configuration shown in Figure 4-1(b), which is simply a series connection of two DC/DC converters. We may now construct our black-box AC/DC converter as shown in Figure 4-2.

Remarks on isolation – It should be noted that when constructing the practical circuit, care should be taken to avoid short-circuit paths that may affect voltage conversion. One simple solution is to use isolated converters, though not always

necessarily, to realize either converter 1 or converter 2. Moreover, if full isolation is required between $e(t)$ and U, then both converters should be isolated.



(a)



(b)

Figure 4-1: AC/DC conversion using (a) a DC/DC converter with a stack up voltage; (b) two DC/DC converters.

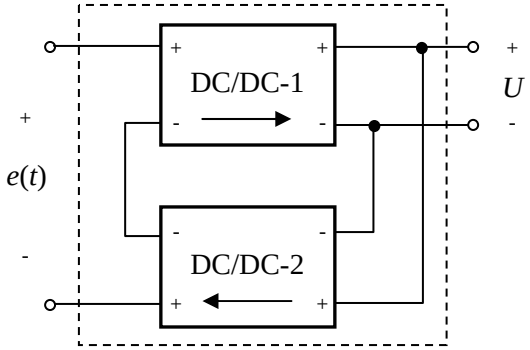


Figure 4-2: Simplest input rectifierless AC/DC converter.

4.2.2 Constraints on voltage conversion ratios

As shown in Figure 4-2, converter 1 (labeled as DC/DC-1) must be capable of converting a variable DC voltage to a fixed DC voltage, whereas converter 2 (labeled as DC/DC-2) converts a fixed DC voltage to another fixed DC voltage. Suppose the voltage conversion ratios of converter 1 and converter 2 are k_1 and k_2, respectively. We have

$$U = k_1\left(e(t) + \xi\right) \tag{4-3}$$

$$\xi = k_2 \cdot U \tag{4-4}$$

Combining the above equations, the overall conversion ratio is given by

$$\frac{U}{e(t)} = \frac{k_1}{1 - k_1 \cdot k_2} \quad \text{for } e(t) \neq 0 \tag{4-5}$$

The case when $e(t) = 0$ corresponds to zero-crossing of the input waveform, i.e., $t = n / 2f_e$ where $n = 0, 1, 2, ...$

In this case, the input to converter 1 and the output from converter 2 are both equal to ξ, giving

$$k_1 = \frac{U}{\xi} \quad \textit{and} \quad k_1 \cdot k_2 = 1 \quad \text{for } e(t) = 0 \tag{4-6}$$

To determine the constraints on the choice of DC/DC converters, we first observe that

$$k_2 = \frac{\xi}{U} \tag{4-7}$$

and from (4-3), we have

$$\frac{U}{\xi + E} < k_1 < \frac{U}{\xi - E} \tag{4-8}$$

Table 4-1: Choice of converters.

	Case I	Case II	Case III	Case IV
Cases	$\xi+E > \xi > \xi-E > \boldsymbol{U}$	$\xi+E > \xi > \boldsymbol{U} > \xi-E$	$\xi+E > \boldsymbol{U} > \xi > \xi-E$	$\boldsymbol{U} > \xi+E > \xi > \xi-E$
Converter 1	Step-down	Step up/down	Step up/down	Step-up
Converter 2	Step-up	Step-up	Step-down	Step-down

We can see that the conversion ratios k_1 and k_2 depend on $\xi+E$, ξ, $\xi-E$ and U. The constraints on the two conversion ratios (choice of DC/DC converters) depend on the value of U and there are four different cases which are given in Table 4-1.

4.2.3 Power flow analysis

We now consider the way in which power is processed in the basic configuration shown in Figure 4-2. First of all, assume that the input current has the form

$$i_{in}(t) = \hat{i}_{in} \cdot \sin(2 \cdot \pi \cdot f_e \cdot t) \tag{4-9}$$

and that the condition for power balance gives

$$\hat{i}_{in} = \frac{2 \cdot P_o}{E} \tag{4-10}$$

where P_o is the output power. Thus, the power processed by converter 1 (labeled as DC/DC-1), $p_1(t)$, is

$$p_1(t) = \left(E \cdot \sin(2 \cdot \pi \cdot f_e \cdot t) + \xi\right) \cdot i_{in}(t) \tag{4-11}$$

and that by converter 2 (labeled as DC/DC-2), $p_2(t)$, is

$$p_2(t) = \xi \cdot i_{in}(t) \tag{4-12}$$

Integrating (4-11) and (4-12) over a half mains cycle, we get the power processed by converter 1 during the positive mains cycle and the negative half mains cycle, respectively, as

$$P_1^+ = 2 \cdot f_e \cdot \int_0^{1/2 f_e} \left(E \cdot \sin(2 \cdot \pi \cdot f_e \cdot t) + \xi\right) \cdot i_{in}(t) dt$$
$$= P_o \cdot \left(1 + \frac{4 \cdot \xi}{\pi \cdot E}\right) \quad (4\text{-}13)$$

and

$$P_1^+ = 2 \cdot f_e \cdot \int_{1/2 f_e}^{1/ f_e} \left(E \cdot \sin(2 \cdot \pi \cdot f_e \cdot t) + \xi\right) \cdot i_{in}(t) dt$$
$$= -P_o \cdot \left(\frac{4 \cdot \xi}{\pi \cdot E}\right) \quad (4\text{-}14)$$

Likewise, we get the power processed by converter 2 during the positive mains cycle and the negative half mains cycle as

$$P_2^+ = -P_2^- = P_o \cdot \left(\frac{4 \cdot \xi}{\pi \cdot E}\right) \quad (4\text{-}15)$$

Thus, we clearly see that the average power processed by converter 1 is P_o and that by converter 2 is zero. Both converters are required to be *bi-directional* since during the negative half mains cycle, power flow is essentially reversed. The overall effect is a circulation of power, which is equal to $(4\xi / \pi E)$, between the two converters. Such circulation may undesirably degrade the efficiency. Hence, to reduce this circulation, we need to design the circuit with a lower ξ / E, meaning that the stack-up voltage ξ should be kept to minimum, as would be expected intuitively.

4.3 Circuit Implementation of Simple AC/DC Converters

The implementation of an AC/DC converter based on the foregoing configuration can be carried out by inserting appropriate DC/DC converters to the model. Figure 4-3 (a) shows a non-isolated AC/DC converter which is constructed

with a buck converter and a flyback converter serving as converters 1 and 2, respectively, and Figure 4-3 (b) shows another non-isolated AC/DC converter which is constructed with a buck converter and a boost converter serving as converters 1 and 2, respectively. Note that in Figure 4-3 (c) and (d), the flyback converter achieves polarity reversal, and does not provide isolation for the entire AC/DC converter unless the other DC/DC converter is also isolated.

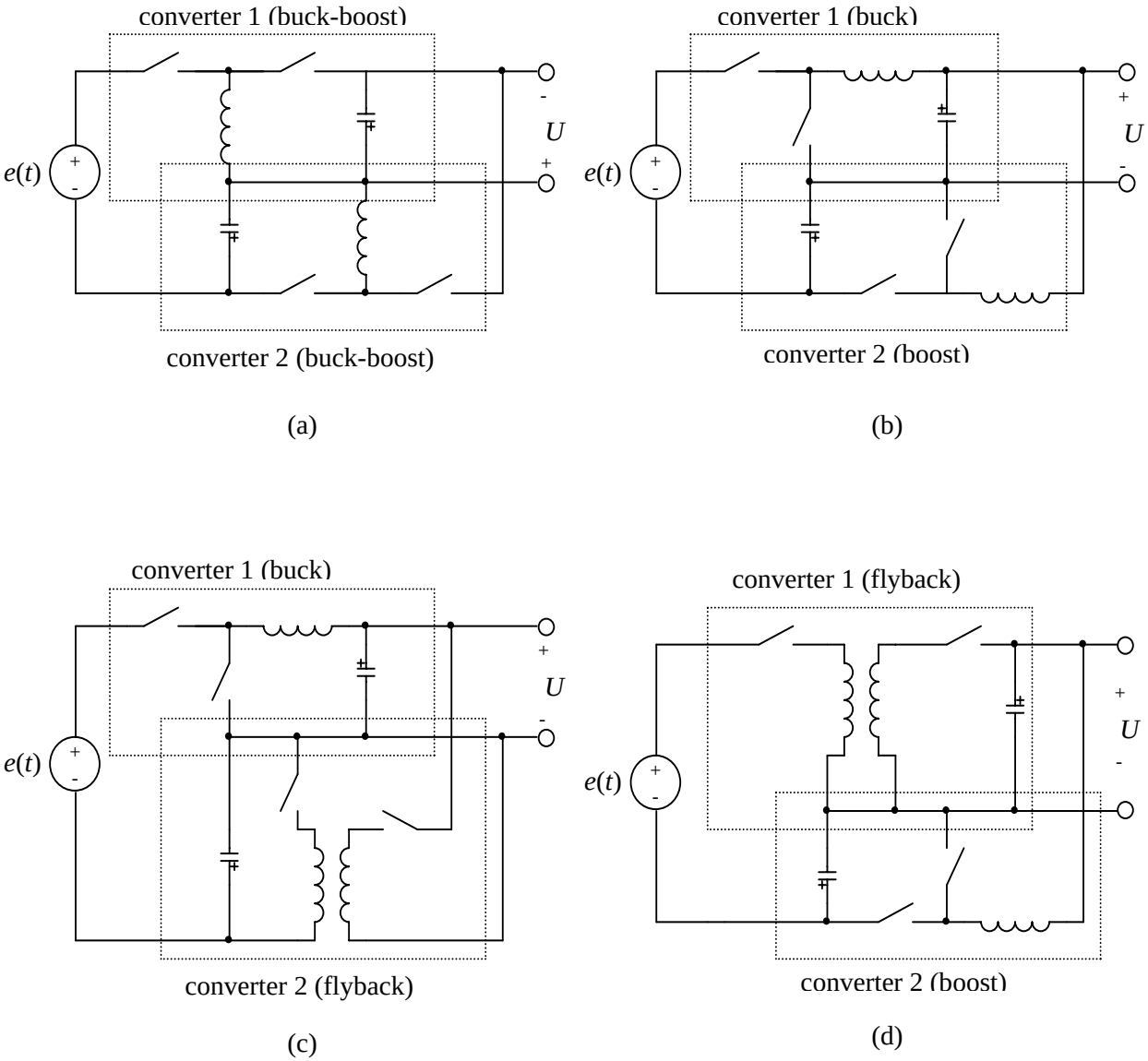


Figure 4-3: Examples of simple input rectifierless AC/DC converters. A flyback converter needed in (c) and (d) in lieu of buck-boost converter to reverse voltage polarity.

4.4 Extension of Basic Topologies

The same idea can be implemented with higher-order DC/DC converters. For example, the Cuk converter has two possible DC outlets which can be used as input to converter 2, as described in Section 4.2. Likewise, the zeta and SEPIC converters can serve the purpose. Figure 4-4 shows the conceptual arrangement.

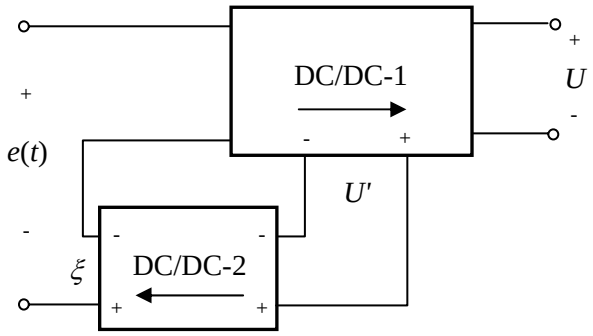


Figure 4-4: Implementation of input rectifierless AC/DC converter using higher-order DC/DC converter (DC/DC-1 can be Cuk, SEPIC or zeta converter).

Suppose converter 1 (labelled as DC/DC-1 in Figure 4-4) has an extra output voltage U' which can be used to feed converter 2 (labelled as DC/DC-2). Let k_{11}, k_{12} and k_2 be the voltage ratios defined as follows.

$$k_{11} = \frac{U}{e(t) + \xi} \tag{4-16}$$

$$k_{12} = \frac{U'}{e(t) + \xi} \tag{4-17}$$

$$k_2 = \frac{\xi}{U'} \tag{4-18}$$

The constraints imposed on the voltage ratios can be derived in a similar manner as in Section 4.2. First of all, ξ must be larger than E, i.e.,

$$k_2 > \frac{E}{U'} \tag{4-19}$$

Moreover, k_{11} and k_{12} are not independent. For the Cuk converter, for example, we have $1 + k_{11} = k_{12}$, which means

$$U' = U + e(t) + \xi \quad \text{with Cuk as converter 1.} \tag{4-20}$$

Obviously, we have $U' > U$, since $e(t) > -E$ for all time. Thus, (4-19) becomes

$$k_2 > \frac{E}{U} \quad \text{with Cuk as converter 1.} \tag{4-21}$$

So, if $E > U$, converter 2 should be a step-up converter; otherwise it can either be a step-up or step-down converter. As for converter 1, we observe that

$$\frac{U}{\xi + E} < k_{11} < \frac{U}{\xi - E} \tag{4-22}$$

Thus, if $U / (\xi + E) > 1$, converter 1 must be a step-up converter; if $U / (\xi - E) < 1$, converter 1 must be a step-down converter; and if $U / (\xi + E) < 1$ and $U / (\xi - E) > 1$, then converter 1 must be able to do both step-down and step-up at different time in a line cycle. If the Cuk converter is used, the duty cycle can be controlled to satisfy these conditions.

4.5 Control Approach

Suppose it is required that the input current be shaped to achieve unity power factor, in addition to a well regulated output voltage [ZJ92, AFR96, R94]. We may summarize the control requirements as follows:

- To produce a tightly regulated DC output voltage.
- To shape the input current to give unity power factor.
- To crudely control the level of the DC stack-up voltage.

It can be shown theoretically that two separate control parameters are needed to achieve the above requirements [TC00]. In our circuit, the allowable control parameters are the duty cycles of the two converters. Thus, in general, two control

loops should be designed, one for regulating the output voltage and the other for shaping the input current. Furthermore, since the converters are bi-directional, feedback can be assigned arbitrarily to the converters. Two cases are therefore possible:

(i) Converter 1 shapes the input current while converter 2 regulates the output voltage, as shown in Figure 4-5 (a).

(ii) Converter 1 regulates the output voltage while converter 2 shapes the input current, as shown in Figure 4-5 (b).

The converter responsible for shaping the input current can also provide crude regulation for the stack-up voltage, as is usually done in practical power factor correction control.

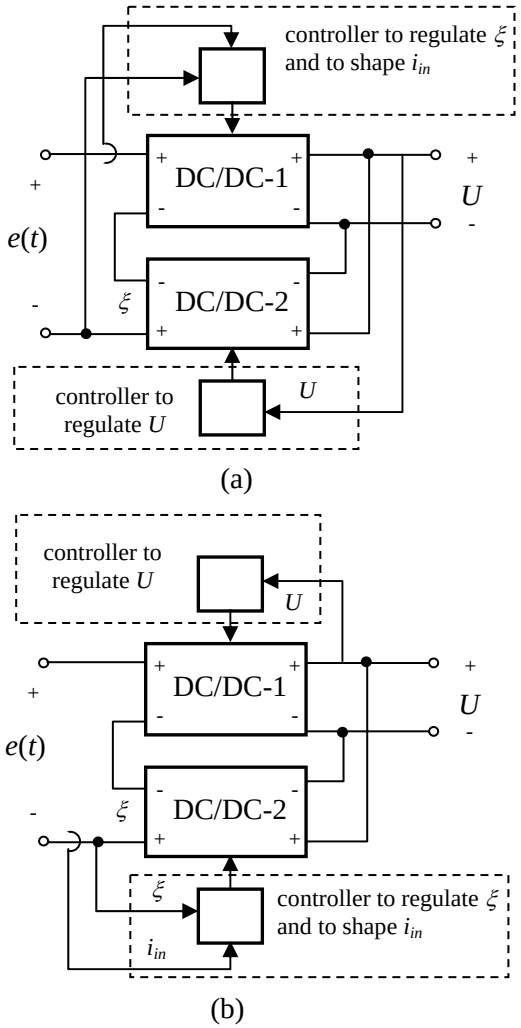


Figure 4-5: Outline of two possible control approaches.

4.6 Experimental Verification

In this section, we report experimental results of a selected AC/DC converter as the ones shown in Figure 4-3 (d) that has been constructed using the afore-described synthesis process. Figure 4-6 shows the experimental converter prototype that consists of a flyback converter with transformer turn ratio n : 1 as converter 1 and a boost converter as converter 2.

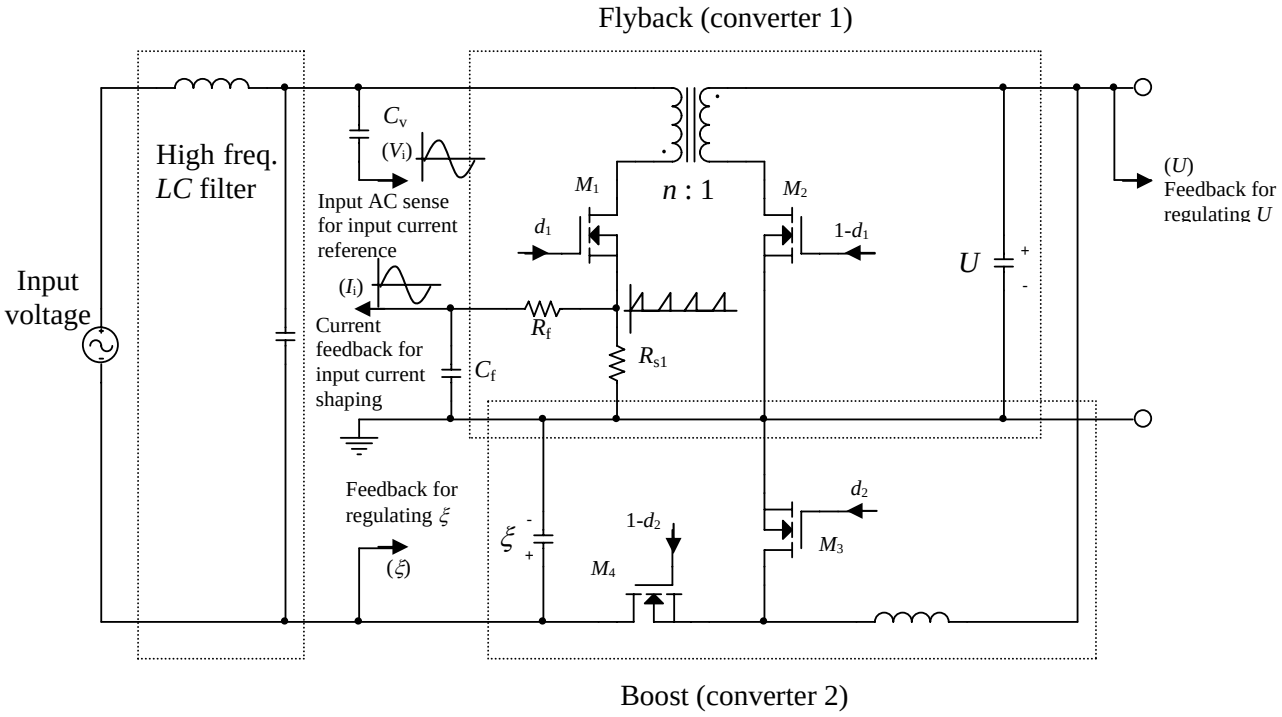


Figure 4-6: Experimental converter circuit.

Referring to Table 4-1, this particular choice of converter type is suitable for the cases where $E > U$ and ξ being any value. Moreover, efficiency consideration would suggest a low value for ξ.

The control consists of two separate feedback loops, as discussed in Section 4.5. In particular, we employ the configuration shown in Figure 4-5 (a), i.e., an input current shaper applied to flyback converter (converter 1) and an output regulator

applied to the boost converter (converter 2). The input current shaper also regulates the stack-up voltage ξ. Figure 4-7 shows the control circuits.

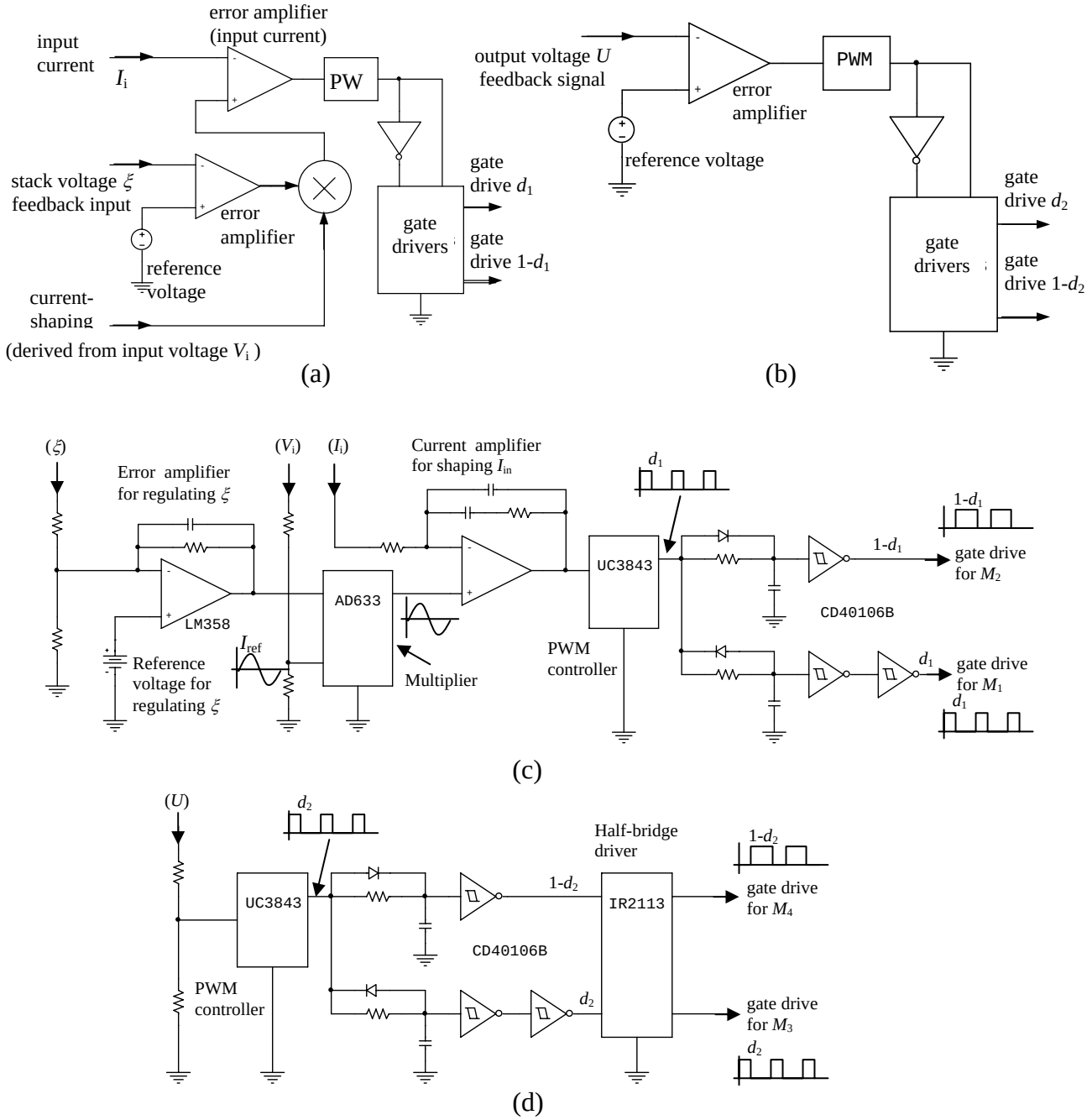


Figure 4-7: The control circuits (a) For the flyback converter; (b) For the boost converter; (c) Practical control circuit for the flyback converter; and (d) Practical control circuit for the boost converter.

Figure 4-7 (c) shows the schematic for the implementation of the controller for flyback converter. To perform PFC function, the current reference I_{ref} for shaping input current I_i should be derived from the input AC voltage V_i which can be obtained by sensing the input terminal of the flyback converter through the capacitor C_v that block the DC stack voltage ξ as shown in Figure 4-6. For the sense of input current I_i for feedback control, it can be observed that it is equal to the average current of M_1 and can be obtained through the current sense resistor R_{s1} followed by a *RC* filter consisting of R_f and C_f. The complementary gate drive signals with duty cycle of d_1 and 1-d_1 required by M_1 and M_2 for flyback operation are derived from the output of the PWM controller UC3843 by logic inverter CD40106B with *RC* dead time circuit to prevent simultaneous conduction of M_1 and M_2.

Figure 4-7 (d) shows the schematic for the implementation of the controller for the boost converter. Output voltage regulation is realized by PWM controller UC3843 and the required complementary gate drive signals for M_3 and M_4 are derived similarly as described in the flyback control. Since the gate drive for M_4 is not referenced to ground, a half-bridge driver IR2113 is used to provide the required high side driving signal.

The test results are summarized in Table 4-2 for two different choices of ξ. The waveforms of the input voltage, input current, output voltage and stack-up voltage are shown in Figure 4-8. It may be of interest to examine the conversion ratios of the individual converters for different input voltage levels, in order to verify the analytical equations developed in Section 4.2.2. Let d_1 and d_2 be the duty cycle of converter 1 and converter 2, respectively. Then, k_1 and k_2, as defined previously, are $k_1 = d_1 / n(1 - d_1)$ and $k_2 = 1 / (1 - d_2)$, respectively, where n is the flyback transformer turn ratio. Table 4-3 shows the values of duty cycles and voltage ratios

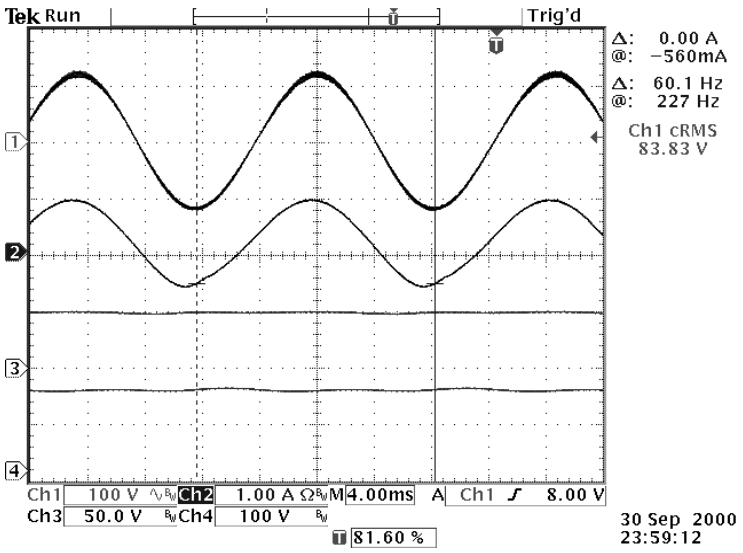
for a few input voltage levels. Note that at the zero crossing of the input voltage, i.e., $e(t) = 0$, the product of the two conversion ratios is equal to one, as predicted in Section 4.2.2. Also, we observe that the efficiency of the converter drops significantly when the stack-up voltage is large, consistent with our earlier analysis of the power circulation problem.

Table 4-2: Experimental measurement for an input rectifierless AC/DC converter using a flyback converter and a boost converter.

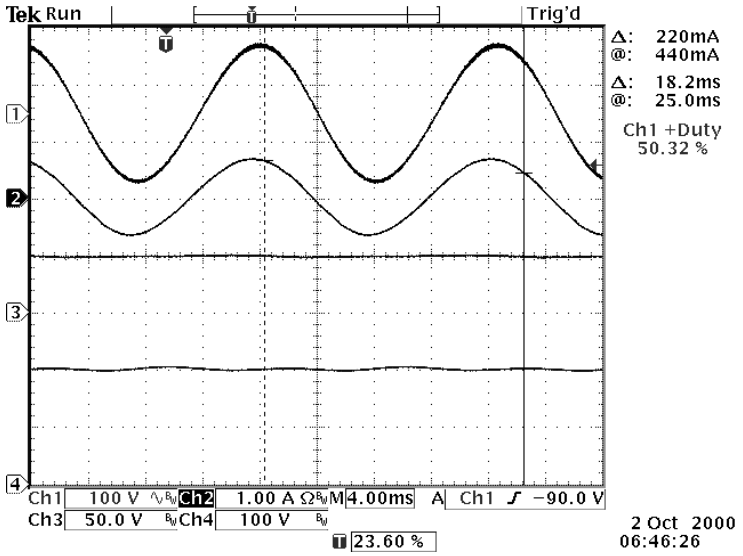
Parameters	Test 1	Test 2
Input voltage E	121 V (peak)	121 V (peak)
Input current $\hat{i}_{in}$	0.735 A (peak)	0.637 A (peak)
Output voltage U	48 V	48 V
Output current	0.7 A	0.5 A
Flyback turn-ratio	1 : 1	3 : 1
Stack-up voltage ξ	140.83 V	199.41 V
Power input P_{in}	44.5 W	38.5 W
Power output P_o	33.6 W	24 W
Efficiency	75.9%	62.3% (consistent with higher ξ)

Table 4-3: Measured duty cycles and voltage ratios for different input voltage levels for an input rectifierless AC/DC converter using a flyback converter and a boost converter.

	input = -98 V		input = 0 V		input = +86 V	
	Test 1	Test 2	Test 1	Test 2	Test 1	Test 2
U	48 V	48 V	48 V	48 V	28 V	48 V
ξ	142 V	204 V	140 V	202V	139 V	198 V
d_1	0.515	0.575	0.263	0.434	0.190	0.349
d_2	0.657	0.757	0.657	0.757	0.653	0.757
k_1	1.062	0.451	0.345	0.245	0.235	0.179
k_2	2,915	4.115	2.915	4.115	2.881	4.115
k_1k_2	3.096	1.856	**1.04**	**1.008**	0.677	0.737



(a) Test 1



(b) Test 2

Figure 4-8: Waveforms of input voltage, input current, output voltage and stack-up voltage for (a) stack-up voltage = 140 V; and (b) stack-up voltage = 204 V. Trace 1: input voltage (100 V/div), Trace 2: input current (1 A/div), Trace 3: output voltage (50 V/div), Trace 4: stack-up voltage ξ (100 V/div), time base (4 ms/div).

Finally, no zero-crossing distortion is expected even at high input line frequency. Figure 4-9 shows the input voltage and current waveforms with the line frequency

raised to 400 Hz. The recorded input current waveform is distortion free at zero-crossing.

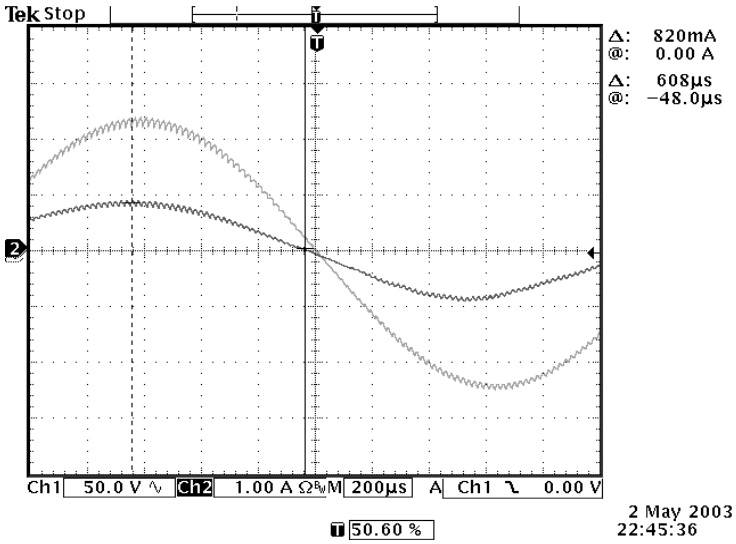


Figure 4-9: Waveforms of input voltage and input current at 400 Hz line frequency showing total elimination of zero-crossing distortion, with input voltage = 85 V(rms), stack-up voltage = 147 V, input power = 46.5 W. Trace 1: input voltage (50 V/div); trace 2: input current (1 A/div); time base (200 μs/div).

4.7 Conclusion

Most conventional AC/DC converters contain a front end AC to DC conversion with an input rectifier which provides a rectified full-wave input voltage for subsequent processing by one or more converters depending upon the functional requirements [T03, EMS90].

This chapter points out the basic construction procedure and topological possibilities of creating AC/DC converters out of simple DC/DC converters. We show that DC/DC converters can be used to construct AC/DC converters without the need for input rectifiers. In particular, it has been shown that

- two DC/DC converters are sufficient;
- the two DC/DC converters should permit bi-directional power flow;

- the two DC/DC converters should be separately controlled to achieve output regulation and input current shaping;
- Some power is being circulated between the two converters.

Furthermore, some design constraints have been discussed, emanating from the limitation of the conversion ratios that can be achieved by particular types of converters. The idea has been experimentally tested with a prototype circuit.

While the presented work focuses on the basic synthesis problem, the efficiency issue may be a practical concern. Essentially, since circulating power always exists, loss becomes inevitable and can be quite large if the stack-up DC voltage is not properly controlled. Note that the loss is proportional to the ratio of the stack-up voltage to the peak input voltage. Thus, as a simple rule, the stack-up voltage should be just above the peak input voltage in order to maintain proper operation. In this chapter, the power flow analysis and the derived circulation power is based on using constant DC stack voltage. Actually, the stack voltage is not limited to a constant value. Time varying stack up voltage that follows the input mains may be able to minimize the ratio of the stack-up voltage to the input voltage further and hence reduces the circulation power for improving the conversion efficiency.

Finally, as a remark of potential applications, AC/DC converters without input rectifiers are devoid of phase lead effect and hence can eliminate zero-crossing distortions in power-factor-correction applications. Also, the problem of zero-crossing distortions is particularly serious when the mains frequency is high, as in the case of aircraft power systems. Thus, AC/DC converters without input rectifiers can be used to construct PFC power supplies for airborne applications. The cross-over distortion-free and bi-directional power flow capability that allows reactive

power handling, make the proposed input rectifierless AC/DC converter topologies suitable for the synthesis of general impedance.

Chapter 5 Application of Rectifierless Topology to PFC Regulator with Low Input Current Distortion

This chapter presents an application of input rectifierless AC/DC conversion. The circuit can be used as a PFC voltage regulator for applications where the mains frequency is high and the allowed input current harmonics is low, e.g., in aircraft power systems. The proposed converter applies the minimal configuration consisting of two basic converters, a combination of a boost and a buck converter, as given in case IV of Table 4-1. The proposed PFC converter can completely eliminate any crossover distortion, which can be significant for conventional converters employing input rectifiers. In addition, the proposed converter allows bi-directional energy flow, ensuring that all inductors work in continuous conduction mode, hence eliminating the distortion due to the abrupt change of dynamic response when the operating mode changes. The proposed PFC converter has incorporated a control method which drastically reduces the circulating power of the power circuit described in Chapter 4 and raises the conversion efficiency that comparable to nowadays PFC converters. Analysis and design of the power and control circuits will be given. An experimental system will be presented for verification purposes.

5.1 Introduction

The aim of PFC converters is to reduce the input current harmonics and provide a high power factor to the AC mains supply. A front-end AC/DC conversion using a

bridge rectifier followed by a boost converter operating at critical conduction mode or in continuous conduction mode under average current mode control is being widely used for PFC applications [R94]. Researchers have revealed two major distortions in such PFC configurations [S02, GSBM03a].

1) The input bridge rectifier and capacitor placed after the bridge rectifier for eliminating high-frequency ripple current cause zero-crossing distortion even with ideal resistive load. It has been shown in Chapter 2 with simulations. Sun [S02] also reported that the use of conventional average current mode control method to boost converters for PFC applications introduces extra leading phase to the input current relative to the input mains voltage, giving rise to crossover distortion especially for high mains frequency such as in airborne applications where the line frequency is 400 Hz. Figure 5-1 shows the crossover distortion of the input current of a commercial PFC converter employing an input bridge rectifier.

2) Another distortion is caused by the change of operating mode of the boost inductor when the load and/or input voltage is changed. The dynamics of the converter changes abruptly, causing distortion to the input current. Although critical conduction mode operation can alleviate the problem, it is undesirable for high power applications since the high ripple current flow in the inductor and switches increases the conduction loss. Moreover, the problem can be reduced by adding a special correction factor to the input current sampling circuit [GSBM03a], at the expense of an increased complexity of the control circuits. Figure 5-2 shows the distortion at the change of operating mode.

In this chapter we propose a PFC converter topology that can eradicate the distortions described above. This topology is derived from the general synthesis procedure for rectifierless AC-DC conversion topologies presented in Chapter 4.

The specific converter configuration chosen for this application is shown in Figure 5-3 (a). Also, the specific choice of constituent DC-DC converters, as shown in Figure 5-3 (b), has been found to give lowest voltage stress on the switches. Moreover, it has been revealed in Chapter 4 that this rectifierless topology suffers from circulating power loss, which becomes significant when the stacking voltage is large. Thus, in this chapter, instead of using a constant DC stacking voltage, we introduce a variable stacking voltage, resulting in significant reduction of the circulating power and loss.

A remark worth mentioning, before we describe details of the circuit, is that the circuit looks a *prima facie* kind of four-quadrant converters. However, we demonstrate in this chapter how such a circuit can be systematically decomposed into two basic DC-DC converters, thus allowing suitable control strategies to be more readily developed to satisfy any desired operation.

In the following sections, the operation of the proposed circuit will be reviewed to explain how circulating power loss can be reduced in this circuit. Experimental results verifying the operations of the circuit and its ability in eliminating distortion at high line frequency (400 Hz) will then be presented. Conclusion is given in the last section.

5.2 Operation Analysis of the Proposed PFC Voltage Regulator Topology

The power conversion stage consists of two DC-DC bi-directional converters, as shown in Figure 5-3 (b). DC-DC converters 1 and 2 are boost and buck converters according to the power flow directions shown by the solid arrows.

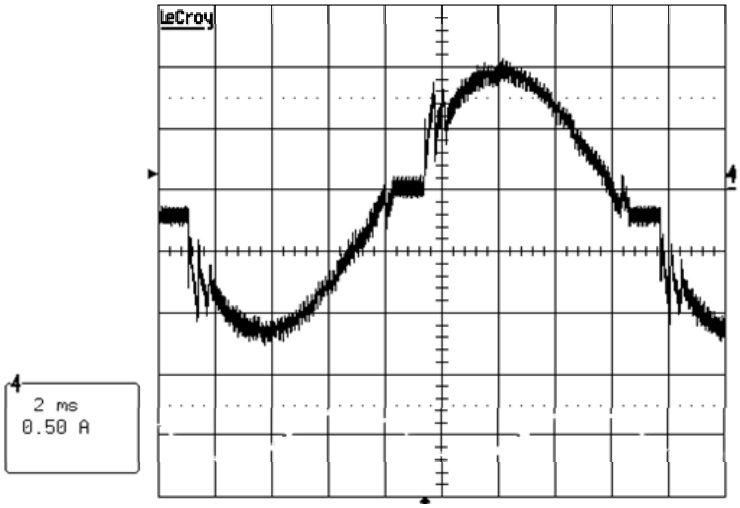


Figure 5-1: Input current waveform with crossover distortion recorded from commercial PFC product.

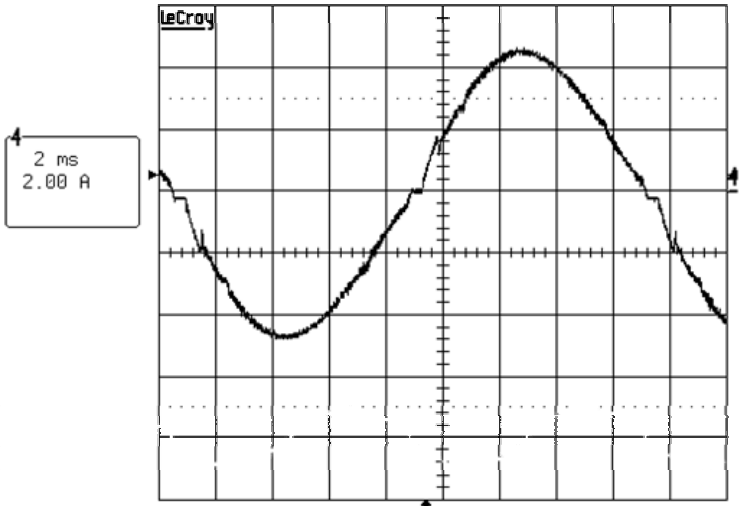


Figure 5-2: Distortion due to mode change.

To realize the input rectifierless AC-DC conversion, DC-DC converter 2 should provide a stacking voltage $\xi(t)$ to the mains V_i such that the input voltage of DC-DC converter 1, V_1, is always positive regardless of V_i. To satisfy this condition, the output voltage U and $\xi(t)$ must satisfy

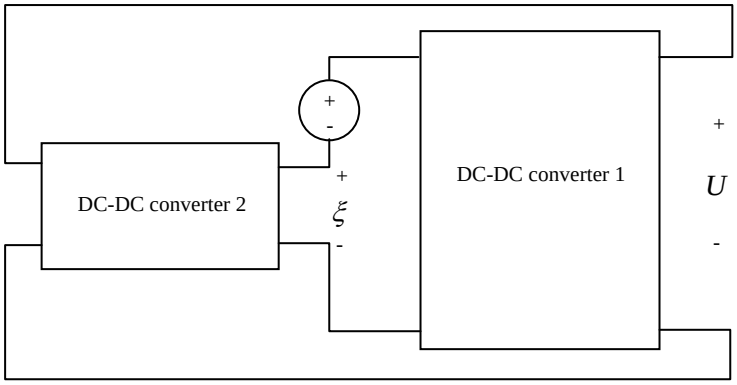
$$U > D_2(t) \cdot U = \xi(t) > E \cdot \sin(2 \cdot \pi \cdot f_e \cdot t) \qquad \text{for all } t \qquad (5\text{-}1)$$

where all symbols are defined in Figure 5-3.

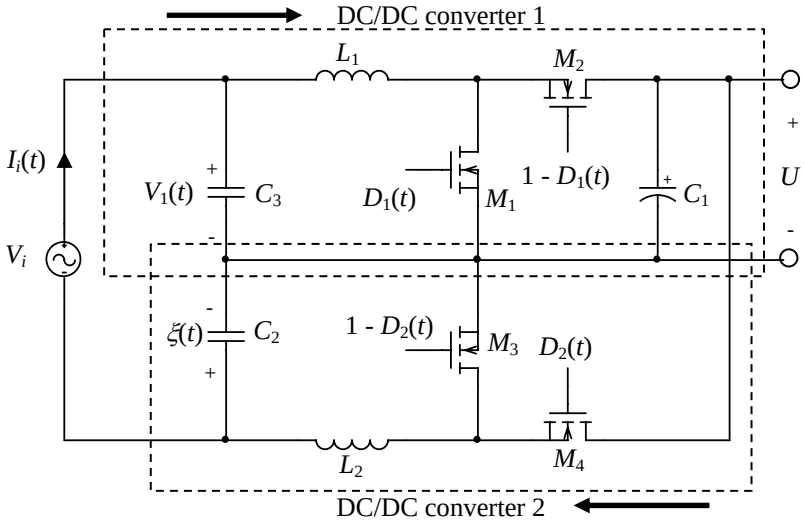
This implies that U must be greater than the amplitude of the input AC voltage E and the overall conversion is a step-up operation. Since the conversion ratio of

DC-DC converter 1 is equal to 1 / (1 – $D_1(t)$), the relationship between U, V_i, $D_1(t)$, and $D_1(t)$ is given by

$$U = \frac{V_i}{1 - D_1(t) - D_2(t)} \tag{5-2}$$



(a)



(b)

Figure 5-3: Rectifierless AC/DC converter. (a) General configuration; (b) specific circuit choice with the boost and buck converters realizing the two constituent DC/DC converters.

5.2.1 Reduction of circulating power

The topology used for PFC converter implementation has a drawback in conversion efficiency due to circulation power. It has been shown in Chapter 4 that

the circulating power is equal to $4\xi / \pi E$ times the output power P_o when stacking voltage ξ is kept constant. This means that the minimum circulating power flows around DC/DC converters 1 and 2 is $4P_o / \pi$ since ξ must be greater than E. To reduce the circulating power, a time varying component, which is in anti-phase to V_i , is proposed to add a to the stacking voltage in order to provide "just enough" stackup DC voltage during the negative cycle. It can be done by equating the duty cycle of M_1 and M_4, i.e., $D_2(t) = D_1(t) = D(t)$. Under this condition, the stacking voltage $\xi(t)$ as well as the output voltage U and the input voltage to DC/DC converter 1 can be derived as follows.

$$U = \frac{V_i}{1 - 2 \cdot D(t)} \quad \text{or} \quad D(t) = \frac{1}{2}\left(1 - \frac{V_i}{U}\right) \tag{5-3}$$

$$\xi(t) = D(t) \cdot U = \frac{1}{2}\left(U - V_i\right) \tag{5-4}$$

$$V_1(t) = \xi(t) + V_i = \frac{1}{2}\left(U + V_i\right) \tag{5-5}$$

We can see that $\xi(t)$ contains a time varying component $V_i / 2$, which is in antiphase to V_i. In addition, (5-5) shows that V_1 is always positive with $U > E$ and satisfies the basic requirement.

To derive the circulating power when the converter operates for PFC, we can assume that the input current I_i is controlled to follow the shape of the mains V_i with amplitude equals to $2P_o / E\eta_{\text{overall}}$, where η_{overall} is the overall of the converter, i.e.,

$$I_i = \frac{2 \cdot P_o}{E \cdot \eta_{\text{overall}}} \cdot \sin(2 \cdot \pi \cdot f_e \cdot t) \tag{5-6}$$

Then, the circulating power $P_{\text{circulate}}$ is given by

$$\begin{aligned} P_{\text{circulate}} &= 2 \cdot f_e \cdot \int_0^{1/2 f_e} \left(V_i + \xi(t)\right) \cdot I_i dt - P_o \\ &= \left(\frac{2 \cdot U}{\pi \cdot E \cdot \eta_{\text{overall}}} - \frac{1}{2}\right) \cdot P_o \end{aligned} \tag{5-7}$$

It can be seen that the minimum circulation power $(2/\pi - 1/2)P_o$ or equivalently 13.67% of P_o can be achieved when U is made close to E. The circulating power is reduced by a factor of 9.32 when compared with $4P_o/\pi$ for the case with constant stack-up voltage.

Obviously, if η is the efficiency of each constituent converter, the total loss due to the circulating power is

$$Loss_{\text{circulatie}} = 2 \cdot P_{\text{circulate}} \cdot \left(\frac{1}{\eta} - 1 \right) \tag{5-8}$$

Also, as power goes directly to the output through DC/DC converter 1, the loss is

$$Loss_{\text{direct}} = P_o \cdot \left(\frac{1}{\eta} - 1 \right) \tag{5-9}$$

Hence, the overall efficiency is

$$\begin{aligned} \eta_{\text{overall}} &= \frac{P_o}{P_o + loss_{\text{circulate}} + loss_{\text{direct}}} \\ &= \frac{P_o}{P_o + P_o \cdot \left(\frac{1}{\eta} - 1 \right) \cdot \left(\frac{4 \cdot U}{\pi \cdot E \cdot \eta_{\text{overall}}} \right)} \\ &= 1 - \frac{4 \cdot U}{\pi \cdot E} \cdot \left(\frac{1}{\eta} - 1 \right) \end{aligned} \tag{5-10}$$

Alternatively, we can write

$$\eta = \frac{1}{1 + \frac{\pi \cdot E}{4 \cdot U} \cdot (1 - \eta_{\text{overall}})} \tag{5-11}$$

which can be used to estimate the constituent converter efficiency from the measured overall efficiency.

Remarks – From the foregoing discussion, the two converters seems to be processing power redundantly, doubling the overall converter size. However, using the proposed control of the circulating power, the net increase in the power processed by each converter is not significant. Under the conditions of an anti-phase

stacking voltage and the afore-described controlled output voltage with $U = E$, the circulating power given by (5-7) is 13.67% of P_o. As shown in Figure 5-4, during the positive half cycle of the input voltage, converter 1 processes an average power of $1.1367P_o$ while converter 2 processes and average power of $0.1367P_o$. By symmetry, during the negative half cycle, converter 2 processes and average power of $1.1367P_o$ while converter 1 processes an average power of $0.1367P_o$. Therefore, each converter processes an average of power $0.6367P_o$, and the whole converter thus processes an average power of $1.2733P_o$, which is 27.33% more than those converters without power circulation. Hence, the overall increase of the proposed converter size is expected to be 27.33%.

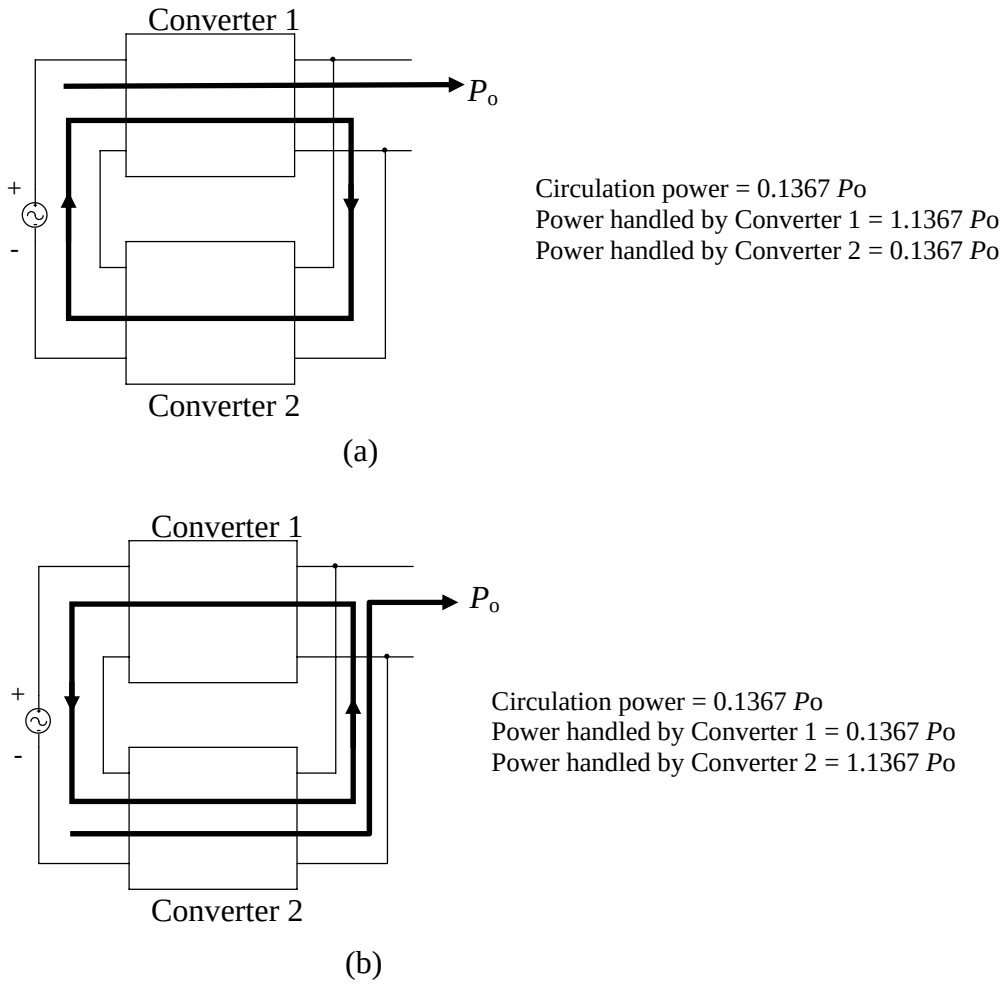


Figure 5-4: The block diagrams indicate circulating power for (a) positive input cycle, and (b) negative input cycle.

5.2.2 Control circuit realization for PFC

The simplified control circuit shown in Figure 5-6 (a) is used for the PFC control. The input current error amplifier forces the input current to follow the reference derived from V_i. Figure 5-6 (b) shows the practical implementation. The reference voltage for regulating the output voltage U is made proportional to the input voltage amplitude. This makes U decrease with E and reduces the ratio U / E at low AC voltage input which helps to reduce circulation power derived in (5-7). The theoretical basis of the control possibility has been discussed in [TC00, T03].

5.3 Experimental Results

A PFC converter using the proposed topology has been built for verification. The operating switching frequency is 50 kHz. The output voltage was made to vary with the input mains amplitude as described in the previous section. The current sensing has been implemented indirectly as shown in Figure 5-7. Since the input current is proportional to the differential voltage across the sensing resistors R_{s1} and R_{s2}, it can be obtained using a differential amplifier as shown in Figure 5-7. All MOSFETs are IRFB18N50. Also, the input filter takes the form of a differential-mode filter, which consists of two 200 μH inductors and a 1 μF capacitor.

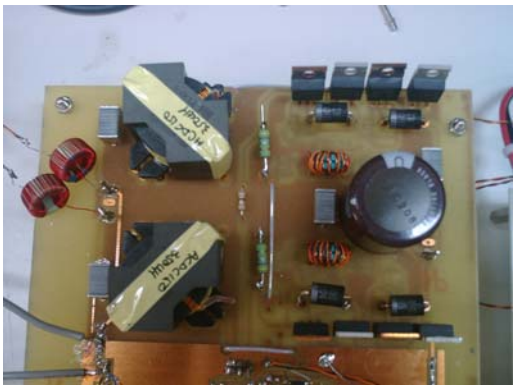


Figure 5-5: Prototypes built for experimental verifications.

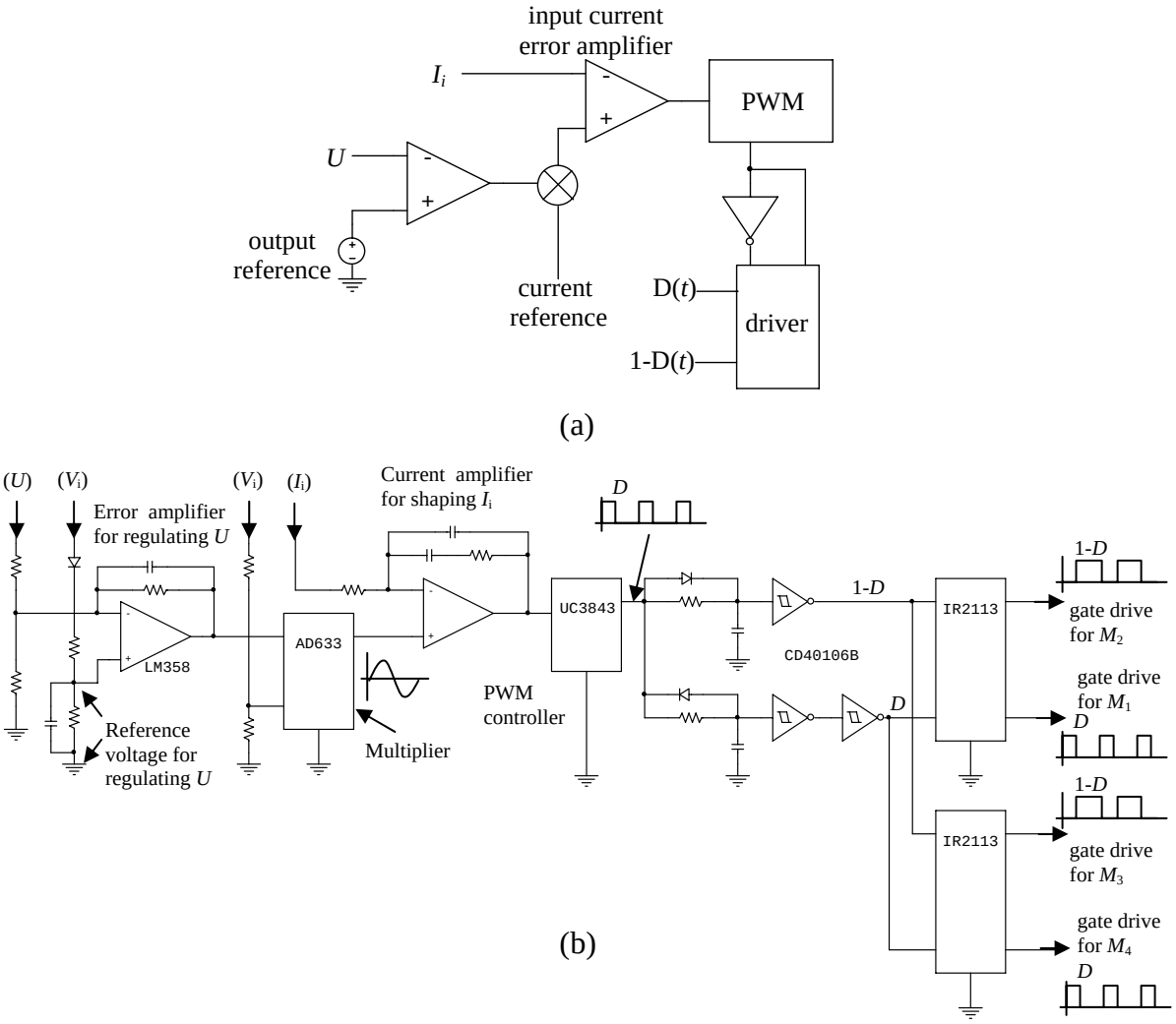


Figure 5-6: The control circuit for power factor correction. (a) The simplified schematic; and (b) The practical implementation.

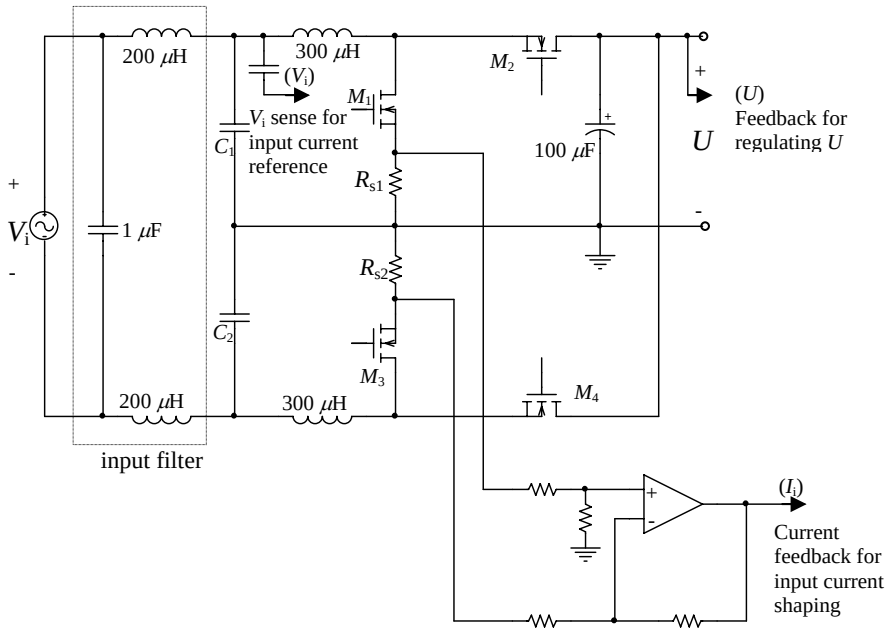


Figure 5-7: Experimental circuit showing input current sensor and input filter. The input current is proportional to the differential voltage across current sensing resistors R_{s1} and R_{s2}.

Table 5-1: Experimental results.

Test	Input voltage	Output voltage	Output power P_o	Measured efficiency $\eta_{overall}$
1	90 V (rms)	174.4 V	100 W	**93.8% (with circulating power control)**
2	90 V (rms)	382.62 V	100 W	87.3% (without circulating power control)
3	230 V (rms)	380.2 V	100 W	**94.5% (with circulating power control)**

Some test results are shown in Table 5-1. From the results of Test 1 and using (5-11), the constituent converter efficiency η can be estimated, i.e., η = 96.6%. The results of Test 2 can be used for consistency check. Assuming η = 96.6% for Test 2 (without circulating power control), we get the overall efficiency as 86.5%, which agrees with the measured data. Test 3 repeats Test 2 with a different set of input and output voltages.

Figure 5-8 shows the operating waveforms of V_1, $\xi(t)$, V_i and I_i. It can be observed that $\xi(t)$ is in anti-phase to V_i and its magnitude reduces when V_i is positive in order to reduce the circulation power.

Figure 5-9 and Figure 5-10 show the operating waveforms at 400 Hz mains frequency and no significant distortion has been found. Figure 5-11 is the blow-up waveforms of V_i and I_i, and no crossover distortion has been observed even when a noticeable phase lead of the input current due to the input filter is present at 230 V, 400 Hz input.

Figure 5-12 shows the operating duty cycle at different values (0 V and 300 V) of V_i. The calculated (using (5-3)) and the measured duty cycles are in perfect agreement. At V_i = 0 the calculated and measured duty cycle are 0.5 and 0.499 while at V_i = 300 V, the calculated and measured duty cycle are 0.105 and 0.119, respectively.

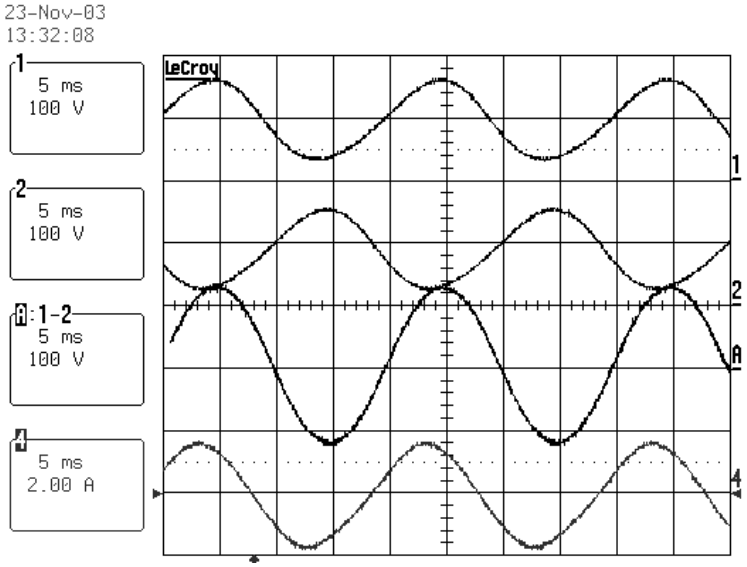


Figure 5-8: Waveforms of V_1 (Ch1), $\xi(t)$ (Ch2), V_i (ChA) and I_i (Ch4), for input voltage = 90 V (rms) and line frequency = 50 Hz.

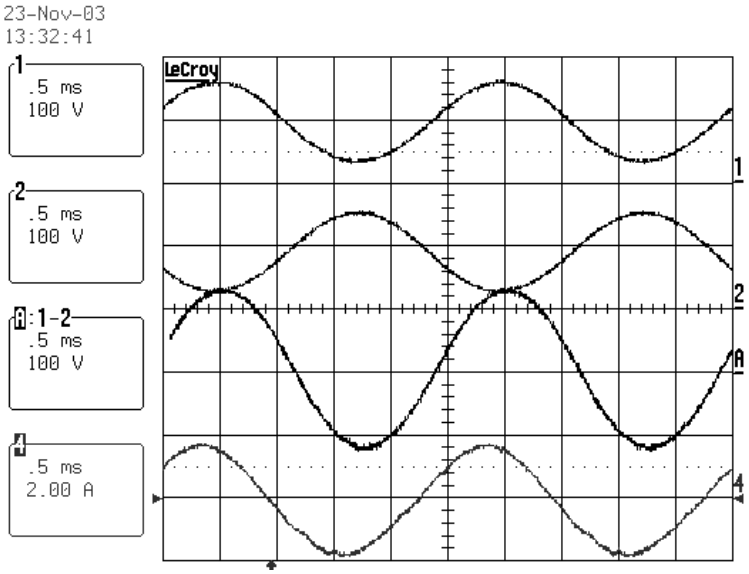


Figure 5-9: Waveforms of V_1 (Ch1), $\xi(t)$ (Ch2), V_i (ChA) and I_i (Ch4), for input voltage = 90 V (rms) and line frequency = 400 Hz.

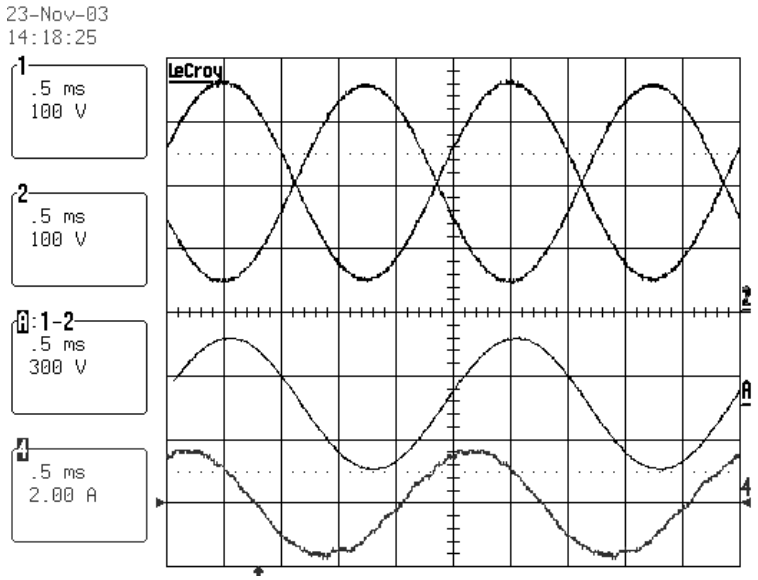


Figure 5-10: Waveforms of V_1 (Ch1), $\xi(t)$ (Ch2), V_i (ChA) and I_i (Ch4), for input voltage = 230 V (rms) and line frequency = 400 Hz.

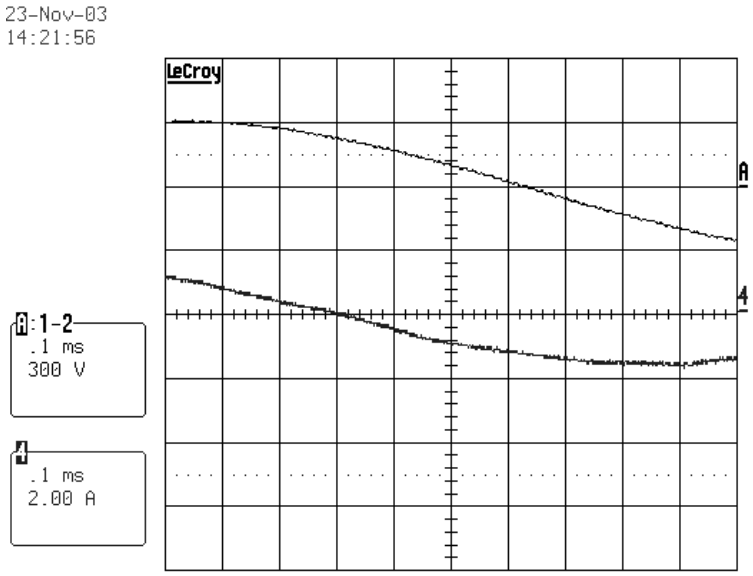
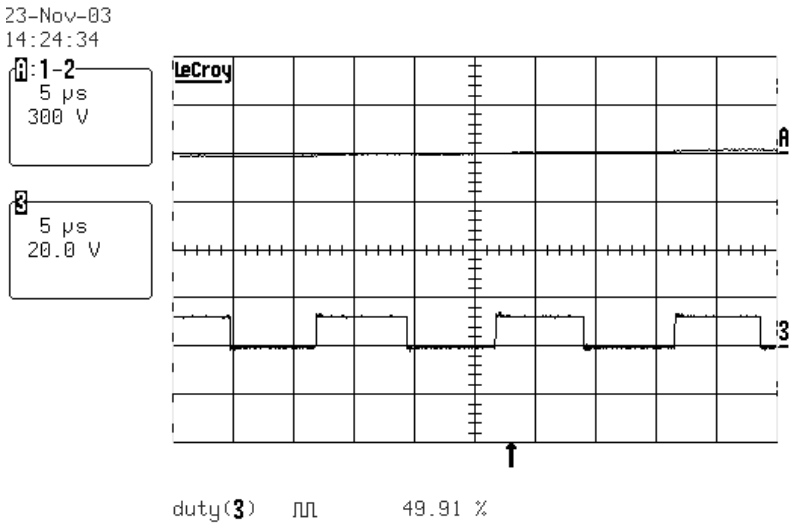
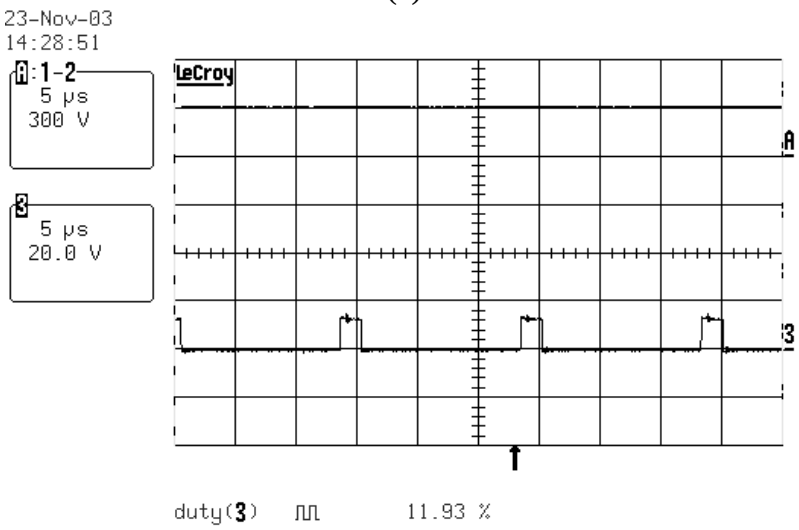


Figure 5-11: Close-up view of waveforms of V_i (ChA) and I_i (Ch4), for input voltage = 230 V (rms) and line frequency = 400 Hz.



(a)



(b)

Figure 5-12: Waveforms of V_i (ChA) and $D(t)$ (Ch3) at (a) zero crossing point; (b) input voltage = 300 V.

5.4 Conclusion

This chapter presents an input rectifierless PFC converter which is derived from the general synthesis procedure for input rectifierless AC/DC conversion described in Chapter 4. The converter inherently eliminates the two addressed major distortions found in PFC regulator and features low input current harmonics, as there is no change of conduction mode of inductors and it eradicates the crossover

distortion due to the input rectifier and the phase lead of input current introduced by filtering capacitor and control circuits in conventional PFC converters. It should be pointed out that there is phase difference between the input voltage and the input current because of the leading phase current drawn by the input filtering capacitor. The phase difference is expected to increase with input voltage and mains frequency that reduces the power factor. In practice, it can be improved by reducing the value of input filtering capacitor. Obviously, the inductance of the input filtering inductor must be increased at the same time in order to maintain the capability of the input filter.

A significant improvement in conversion efficiency is achieved when compared with the results obtained in Chapter 4. One of the major reasons is that a control circuit has been designed which reduces the circulation power significantly. Another reason is because of the choice of converter configuration (case IV in this application) where a boost converter is used for converter 1 instead of flyback converter with isolation transformer in Chapter 4. The boost converter not only provides less voltage and current stress for switches which lowers both conduction and switching loss but also provides lower loss in magnetic component where the loss due to leakage inductance is not found in boost converter but significant in flyback converters.

In addition to the reduction of circulation power, the proposed variable stack voltage control also reduces the input terminal voltage variations of converter 1 as well as the variation of duty cycle to cope with the input AC voltage when compared with constant stack voltage. With input AC voltage amplitude = E, the duty cycle variation $\Delta D_{\text{variable\_stack}}$ of the proposed control scheme is,

$$\Delta D_{\text{variable\_stack}} = D_{\max} - D_{\min} = \frac{1}{2}\left(1+\frac{E}{U}\right) - \frac{1}{2}\left(1-\frac{E}{U}\right) = \frac{E}{U} \qquad (5\text{-}12)$$

and the input voltage variation $\Delta V_{1\_variable\_stack}$ of converter 1 with the proposed control scheme is,

$$\Delta V_{1\_variable\_satck} = \frac{1}{2}(U+E) - \frac{1}{2}(U-E) = E \tag{5-13}$$

For constant stack voltage, the duty cycle variation $\Delta D_{constant\_stack}$ is,

$$\Delta D_{constant\_stack} = D_{max} - D_{min} = \left(1 + \frac{E}{U} - D_2\right) - \left(1 - \frac{E}{U} - D_2\right) = 2\frac{E}{U} \tag{5-14}$$

and the input voltage variation $\Delta V_{1\_constant\_stack}$ of converter 1 with constant stack voltage is,

$$\Delta V_{1\_constant\_stack} = (U+E) - (U-E) = 2E \tag{5-15}$$

It can be observed that both the input voltage and the operating duty cycle variation of constant stack voltage control are twice the case of the proposed control scheme with variable stack voltage. Since the operating duty cycle is directly driven by the current error amplifier output, the errors in shaping the input current according to the input voltage (which relates to the total harmonic distortion THD) in the constant stack voltage control should be twice of the case when the proposed variable stack voltage control is applied under the conditions with the same current error amplifier gain and PWM gain.

With low input current harmonic distortions and compatible conversion efficiency, the proposed PFC converter is suitable for airborne power systems requiring low input current harmonics with a relatively high mains frequency. Furthermore, unlike the conventional AC/DC converter employing input rectifiers with irreducible loss due to the forward voltage drop of diode rectifiers, it is expected that the conversion efficiency of the proposed input rectifierless topology

can be improved further if better MOSFET devices with lower on-state resistance are used. Possible future work may proceed along the idea of rectifierless configurations [IC99] as well as other practical design tradeoff considerations [ZJ92]. Finally, it should be pointed out that the two-converter configuration described in this chapter represents a minimal converter configuration that can be used to emulate any input impedance, not limited to pure resistance. The application of general input impedance synthesis will be presented in the next chapter.

Chapter 6 Application of the Proposed Input Rectifierless Converter to General Impedance Synthesis

The special input characteristics of the input rectifierless converter proposed in Chapter 4, like programmable input current without crossover distortion and bi-directional power flow capability, are found essential to the application of general impedance synthesis. This chapter provides a proof that the proposed input rectifierless converter is suitable for the application. It starts with a review of switching converter with particular emphasis on their fundamental functions in terms of terminal voltages and currents. Then, a minimal configuration of switching converters for synthesizing any impedance is derived which shows that the proposed input rectifierless converter is sufficient for general impedance synthesis. A design of general impedance synthesizer using a circuit derived in Chapter 4 will be presented with experimental results of emulating different impedances.

6.1 Introduction

Many problems in electrical engineering are reducible to one of *impedance synthesis* or *imitation* [K55, N88]. Basically, the impedance observed from the terminals of a given circuit is defined as the ratio of the voltage across the terminals and the current flowing into and out of the terminals, as shown in Figure 6-1. In power electronics, for instance, impedance imitation is central to many applications, be it known or clearly recognized by the engineers. Power factor correction (PFC), a specific example provided in Chapter 5, effectively requires the input impedance to

be resistive [T03, GCPAU03]. Thus, *imitating* a resistor for the input of a converter is the basic requirement for achieving a high power factor for the converter. Many control problems can also be interpreted as a kind of impedance modification, e.g., shaping the load transient of a converter is essentially a process of modifying the output impedance of the converter [PTL99]. The application is relevant to power electronics, and may also be applicable to other branches of electrical engineering. For instance, programmable reactive components using some high-frequency converters are useful elements for control applications.

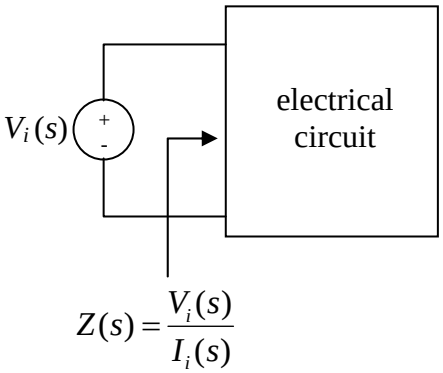


Figure 6-1: Impedance definition.

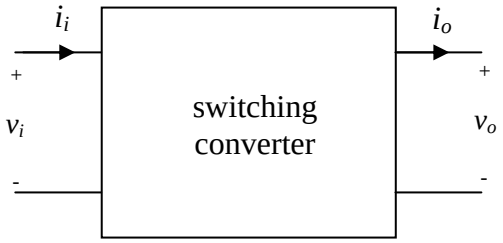


Figure 6-2: Simple switching converter as two-port.

6.2 Review of Switching Converters

We consider a *simple switching converter* as a two-port circuit, as shown in Figure 6-2. Let the input voltage, input current, output voltage and output current be v_i, i_i, v_o, and i_o respectively. In practice, a simple switching converter may contain a

high-frequency storage element and a pair of switches, such as the buck, buck-boost and boost converters, as shown in Figure 6-3 [SB85]. Note that the output capacitor is not considered as part of the converter and the converter therefore *has no low-frequency storage capability.* The switches are switched periodically at a high frequency (usually hundreds of kHz). The switching frequency can be regarded as being so high that all variables v_i, i_i, v_o, and i_o are relatively slow varying. This assumption holds for all power electronics applications with ideal switching converters operating at infinite switching frequency. Precisely, we write

$$f_{\max} << f_s \qquad (6\text{-}1)$$

where $f_{\max}$ is the maximum frequency of v_i, i_i, v_o, and i_o, and f_s is the switching frequency of the converter. Specific power processing functions are achieved by adjusting or controlling the relative durations of the "on" and "off" intervals of the switches.

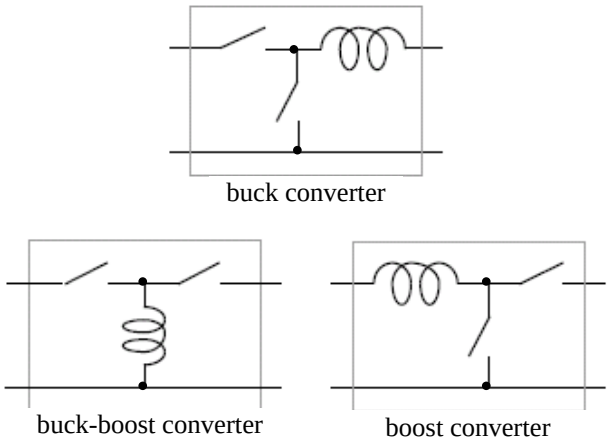


Figure 6-3: Simple switching converters for voltage source terminations. Duals of these circuits can be likewise derived for current source terminations using capacitor and switches.

The most fundamental property of an *ideal* switching converter is the conservation of power under *slowly varying terminal voltage and current conditions.* Clearly, the average input power over one repetition period (also called switching period) must be equal the average output power over the same period, i.e.,

$\int_T v_i \cdot i_i \, dt = \int_T v_o \cdot i_o \, dt$. Here we emphasize that the equality of energy is valid only if the switching frequency is very much higher than the variation of all terminal variables. Thus, the ideal converter does not store or dissipate any energy over a repetition period under the condition of slowly varying terminal voltages and currents. Of course, real converters are never 100% efficient, but here, we ignore this loss to keep our discussion simple. Moreover, in practice, we only consider v_i, i_i, v_o, and i_o being *slowly varying,* i.e., varying at a frequency which is much lower than the switching frequency of the converter. Hence, the ideal power conservation equation becomes

$$v_i \cdot i_i = v_o \cdot i_o \quad (">" \text{ in practice}) \qquad (6\text{-}2)$$

where v_i, i_i, v_o, and i_o can be regarded as "instantaneous" variables if they satisfy (6-1). In other words, equation (6-2) holds only when we consider low-frequency (i.e., slowly varying) voltage and current variables. Precisely, in practice, (6-2) is an approximation, the integrity of which improves as the switching frequency gets higher.

In addition to the power conservation property, a defining objective of a switching converter is that *given one of the terminal variables (normally the input voltage v_i) and possibly some constraints on the terminal variables (as, for instance, enforced by the load characteristics), a switching converter attempts to regulate or program* **one or more** *of the remaining three terminal variables by controlling some parameter.* For example, for DC power supplies, the input voltage is given, and the switching converter aims to regulate the output voltage by controlling the duty cycle. Moreover, for power factor correction, the input voltage is given (normally a rectified sinewave), and the switching converter aims to program the input current

such that it varies at the same frequency and in phase with the input sinewave voltage.

Note that the above definition implicitly assumes that all terminal voltages and currents are slowly varying compared to the switching frequency. Thus, theoretically, if the switching frequency approaches infinity, the switching converter can process voltage or current of arbitrarily high frequencies.

6.3 Minimal Configuration of Impedance Synthesizer Based on Switching Converters

In finding the basic configuration of an impedance synthesizer, we first observe that an impedance can be realized by programming the current if the voltage is given, and vice versa. This fits the definition of the switching converter described in Section 6.2. Thus, a switching converter can be used to program the input current i_i given its input voltage v_i in order to create the desired impedance seen from the converter's input as PFC converter as an example. Here, both v_i and i_i are slowly varying in the sense of (6-1). Moreover, the switching converter is subject to the constraint of (6-2), i.e., power conservation. Clearly, general impedance cannot be synthesized with one converter terminated with a fixed load impedance because (6-2) cannot generally be satisfied. Thus, *one switching converter is insufficient for general impedance synthesis.* Clearly, we need to balance the power by ensuring that the output of the converter "emits" the right amount of "instantaneous" power. Note again that "instantaneous" refers to relatively low-frequency variables assuming a much higher switching frequency.

If two switching converters are available, one of them can be used to program the input current (given the input voltage) so as to achieve the desired impedance.

The other can then be used to match the power conservation requirement by controlling its output to dissipate or generate the correct amount of real power since $v_i\, i_i = v_o\, i_o$ (again in the low-frequency sense) must be satisfied by both converters. This is possible according to the definition of the switching converter described in Section 6.2 that, given the load (a resistor or a DC current source), the converter can adjust or control its output voltage v_o so as to emit or absorb a desired amount of DC power to or from the output port. Clearly, there must then exist a low-frequency storage element connecting between the two converters in order to absorb the right amount of instantaneous power to meet the power balance for both converters. Thus, the minimum configuration consists of

- two switching converters,
- one storage element (at frequency up to $f_{\max} << f_s$)
- one dissipative element or power source.

Obviously the dissipative element can be realized by a negative power source (e.g., current load). Furthermore, because power flow can be in either direction, the converters must be bi-directional.

6.4 Implementation

The derived criteria required by general impedance synthesis show that the proposed input rectifierless converter in Chapter 4 satisfies all conditions with an additional dissipative element or power source connected externally. A minimal configuration is shown in Figure 6-4. Note that the choice of the exact types of converters 1 and 2 remains a design issue.

To synthesize a desired impedance $Z(s)$, we have to ensure the correct magnitude and phase relationships between v_i and i_i. Essentially we want i_i to follow

a reference template i_{ref} which is related to v_i as follows, in the complex frequency domain:

$$I_{\text{ref}}(s) = V_i(s) \cdot G(s) \tag{6-3}$$

Where $G(s)$ is the transfer function from he input voltage to the reference template. Assume that the transfer function from I_{ref} to I_i is

$$K(s) = \frac{I_i(s)}{I_{\text{ref}}(s)} \tag{6-4}$$

Suppose $Z(s)$ is to be synthesized. Then $G(s)$ becomes

$$G(s) = \frac{1}{K(s) \cdot Z(s)} \tag{6-5}$$

Thus, in the circuit implementation, we have to realize this transfer function in order to synthesize the required impedance. A block diagram showing the control requirement is shown in Figure 6-5.

Clearly, $K(s)$ in general depends on the converter response. However, if the bandwidth of the converter response is much higher than that of the applied voltage v_i, we may assume that $K(s)$ is nearly a constant equal to K, i.e., i_i is proportional to i_{ref}. Thus, we can find the control transfer function $G(s)$ from (6-5).

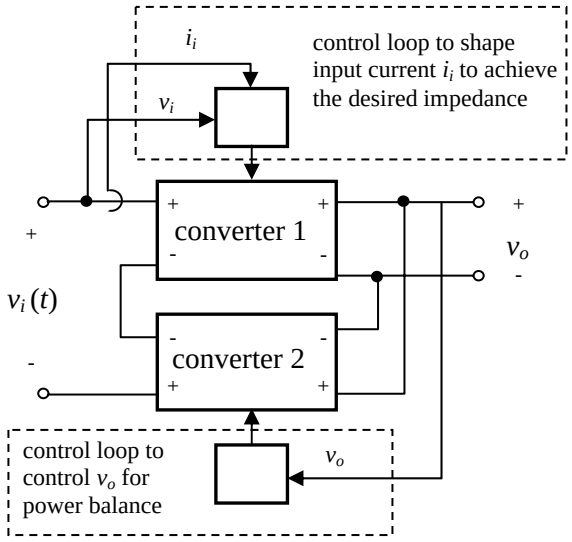


Figure 6-4: A minimal configuration, with at least one low-frequency storage within either converter 1 or 2.

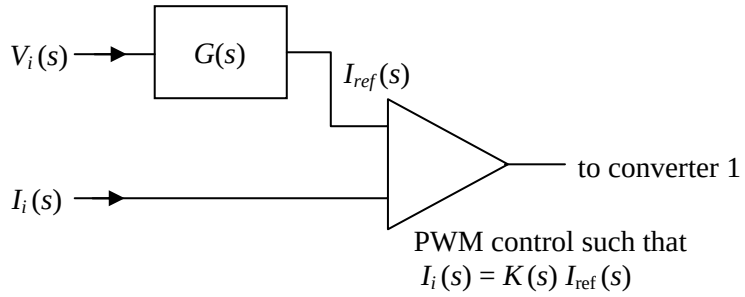


Figure 6-5: Current shaping control for achieving the required magnitude and phase relationships between input voltage and input current. $K(s)$ is nearly constant if all variables are slowly varying relative to the switching frequency.

6.4.1 Example 1: Pure inductance synthesis

The impedance of a pure inductor is

$$Z(s) = s \cdot L \tag{6-6}$$

where L is the inductance to be synthesized. Thus, the required $G(s)$ is

$$G(s) = \frac{1}{s \cdot K \cdot L} \tag{6-7}$$

which can be implemented using the circuit shown in Figure 6-6. For other possible circuit realization, see [SGL90]. With $R_4 = R_5$ and $|sC_1R_2| >> 1$, we have

$$G(s) \approx \frac{1}{s \cdot C_1 \cdot R_1} \quad \Rightarrow \quad L \approx \frac{C_1 \cdot R_1}{K} \tag{6-8}$$

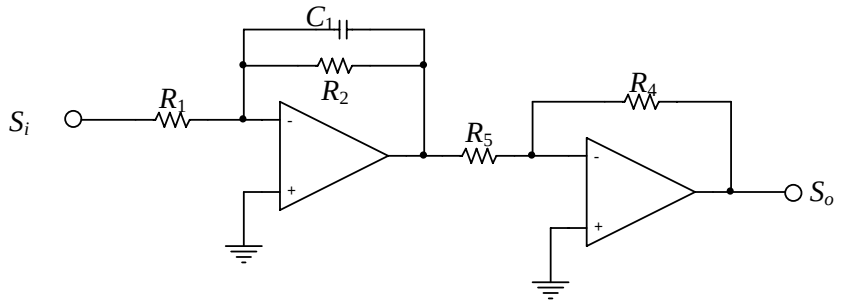


Figure 6-6: Circuit implementation $G(s)$ for inductive impedance synthesis. Here, $G(s) = S_o / S_i = 1 / (R_1/R_2 + sC_1R_1)$, with $R_4 = R_5$.

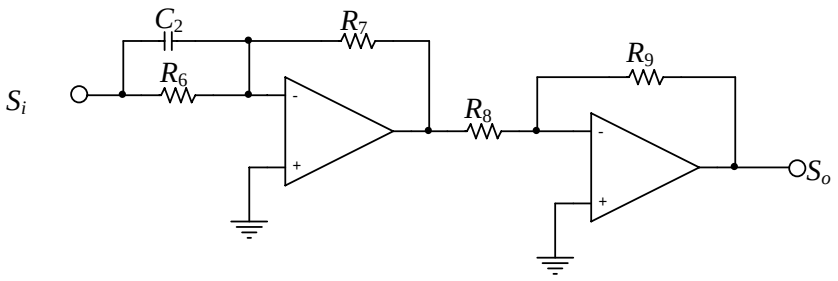


Figure 6-7: Circuit implementation $G(s)$ for capacitive impedance synthesis. Here, $G(s) = S_o / S_i = (1 + sC_1R_1)R_7 / R_8$, with $R_8 = R_9$.

Hence, by appropriately choosing the values for C_1, R_1, R_2, etc., we can synthesize a pure inductance. It should be reiterated that the synthesis is effective only for the range of frequencies much lower than the switching frequency of the constituent DC/DC converters. For instance, choosing C_1 = 2.2 μF, R_1 = 270 kΩ, R_2 = 2.2 MΩ, $R_4 = R_5$ = 10 kΩ, we have $|sC_1R_2| \gg 1$ for the frequency range 20 Hz to 200 Hz. The synthesized inductance is 0.594/K H, where K can be predetermined experimentally.

6.4.2 Example 2: Pure capacitance synthesis

Likewise, a pure capacitance can be synthesized. In this case, the required $G(s)$ is sC/K, if C is the capacitance to be synthesized. The appropriate circuit for constructing $G(s)$ is shown in Figure 6-7. With $R_8 = R_9$ and $|sC_2R_6| >> 1$, we have

$$G(s) \approx s \cdot C_2 \cdot R_7 \quad \Rightarrow \quad C \approx K \cdot C_2 \cdot R_7 \qquad (6\text{-}9)$$

Hence, by appropriately choosing the values for C_2, R_6, R_7, etc., we can synthesize a pure capacitance. For instance, choosing C_2 = 100 nF, R_6 = 820 kΩ, R_7 = 220 Ω, $R_8 = R_9$ = 10 kΩ, we have $|sC_2R_6| >> 1$ for the frequency range from 20 Hz to 200 Hz. The synthesized capacitance is 22K μF, where K can be found experimentally.

6.4.3 Example 3: Inductive impedance synthesis

The impedance of a series connection of an inductor L and a resistor R_L is

$$Z_{LR}(s) = s \cdot L + R_L \tag{6-10}$$

and $G(s)$ can be calculated according to (6-5) as

$$G(s) = \frac{1}{K \cdot R_L \cdot \left(1 + \frac{s \cdot L}{R_L}\right)} \tag{6-11}$$

Thus, the transfer function $G(s)$ is a single pole system and can again be implemented with the circuit of Figure 6-6.

6.4.4 Example 4: Capacitive impedance synthesis

The impedance of a parallel connection of a capacitor C and a resistor R_C is

$$Z_{CR}(s) = \frac{R_C}{1 + s \cdot C \cdot R_C} \tag{6-12}$$

and hence $G(s)$ can be calculated according to (6-5) as

$$G(s) = \frac{1}{K \cdot \left(\frac{R_C}{1 + s \cdot C \cdot R_C}\right)} = \frac{1}{K} \cdot \frac{1 + s \cdot C \cdot R_C}{R_C} \tag{6-13}$$

Thus, the transfer function $G(s)$ is a one zero system and can also be readily implemented with the circuit of Figure 6-7.

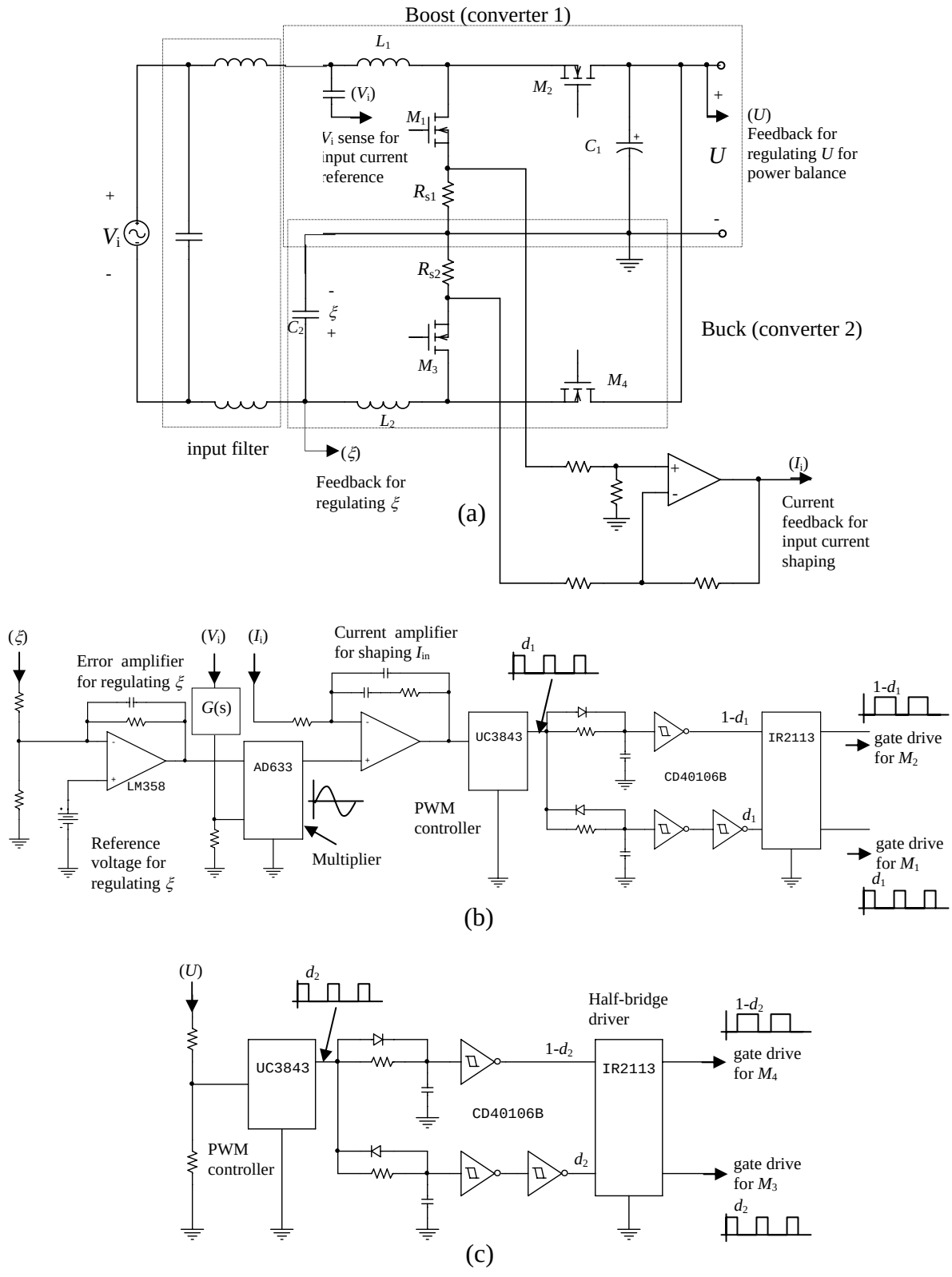


Figure 6-8: The experimental impedance synthesizer. (a) The main converter; (b) The controller for current shaping; and (c) The controller for achieving power balance.

6.5 Experimental Results

A particular choice of practical converter types and the schematic of control circuits for the implementation of the impedance synthesizer is shown in Figure 6-8. Here, the input v_i is a sinusoidal voltage source, and the output v_o is connected to a current load. The switching frequency is 50 kHz. The four examples described previously are evaluated.

Our first experiment is the synthesis of pure inductance. The inductance to be synthesized is 0.5 H. The circuit for realizing the $G(s)$ transfer characteristic has been shown earlier in Figure 6-6, and the parameters used are C_1 = 2.2 μF, R_1 = 270 kΩ, R_2 = 2.2 MΩ, $R_4 = R_5$ = 10 kΩ. The measured value for the gain K is 1.18 A/V. As analyzed before, this set of parameters can provide a synthesized inductance of $0.594/K$ = 0.503 H for the frequency range from 20 Hz to 200 Hz. The test input voltage magnitude is 50.5 V (rms). The measured impedance magnitude and phase angle are shown in Figure 6-9. A typical set of waveforms is shown in Figure 6-10.

Our second experiment is the synthesis of pure capacitance. The capacitance to be synthesized is 25 μF. The circuit for realizing the $G(s)$ transfer characteristic has been shown earlier in Figure 6-7, and the parameters used are C_2 = 100 nF, R_6 = 820 kΩ, R_7 = 220 Ω, $R_8 = R_9$ = 10 kΩ. The measured value for the gain K is 1.18 A/V. As analyzed before, this set of parameters can provide a synthesized capacitance of $22K$ = 25 μF for the frequency range from 20 Hz to 200 Hz. The test input voltage magnitude is 14.5 V (rms). The measured impedance magnitude and phase angle are shown in Figure 6-11. A typical set of waveforms is shown in Figure 6-12.

The third impedance to be synthesized is L = 0.3 H in series with R_L = 50 Ω. We have realized $G(s)$ using the same circuit of Figure 6-6, with C_2 = 1 μF, R_1 = 360 kΩ,

R_2 = 6.2 kΩ, and R_4 = R_5 = 10 kΩ. The transfer function K was found to be 1.18 A/V. This set of parameters gives a synthesized inductive impedance of 49.206 Ω in series with 0.305 H, for the frequency range from 20 Hz to 200 Hz. The test input voltage magnitude is 30.4 V (rms). The measured impedance magnitude and phase angle are shown in Figure 6-13. A typical set of waveforms is shown in Figure 6-14.

Our final impedance to be synthesized is a parallel connection of C = 21 μF and R_C = 300 Ω. We have realized $G(s)$ using the same circuit of Figure 6-7, with C_2 = 10 nF, R_6 = 660 kΩ, R_7 = 1.8 kΩ, and R_8 = R_9 = 10 kΩ. The transfer function K was found to be 1.18 A/V. This set of parameters gives a synthesized capacitive impedance of 310.73 Ω in parallel with 21.24 μF, for the frequency range from 20 Hz to 200 Hz. The test input voltage magnitude is 20.6 V (rms). The measured impedance magnitude and phase angle are shown in Figure 6-15. A typical set of waveforms is shown in Figure 6-16.

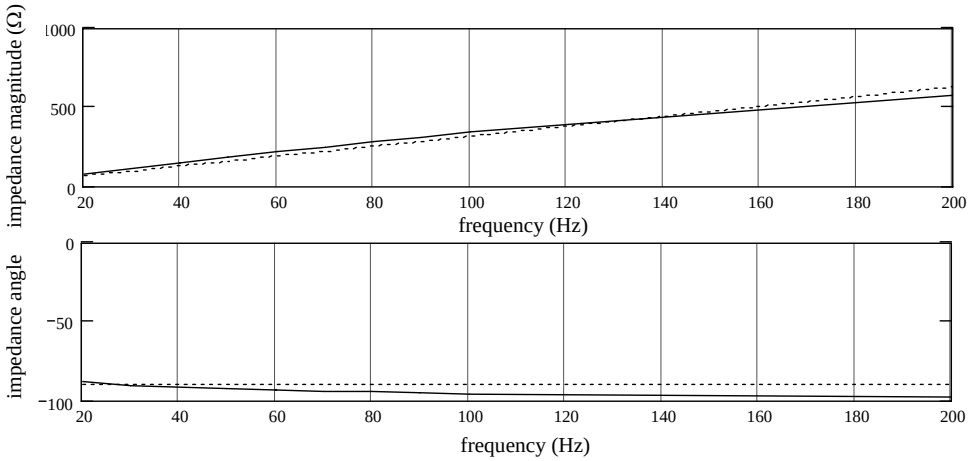


Figure 6-9: Measured impedance magnitude and phase angle of the synthesized 0.5 H pure inductance. Solid line: measured results from the experimental circuit; dash line: ideal characteristic of an inductor of 0.503 H.

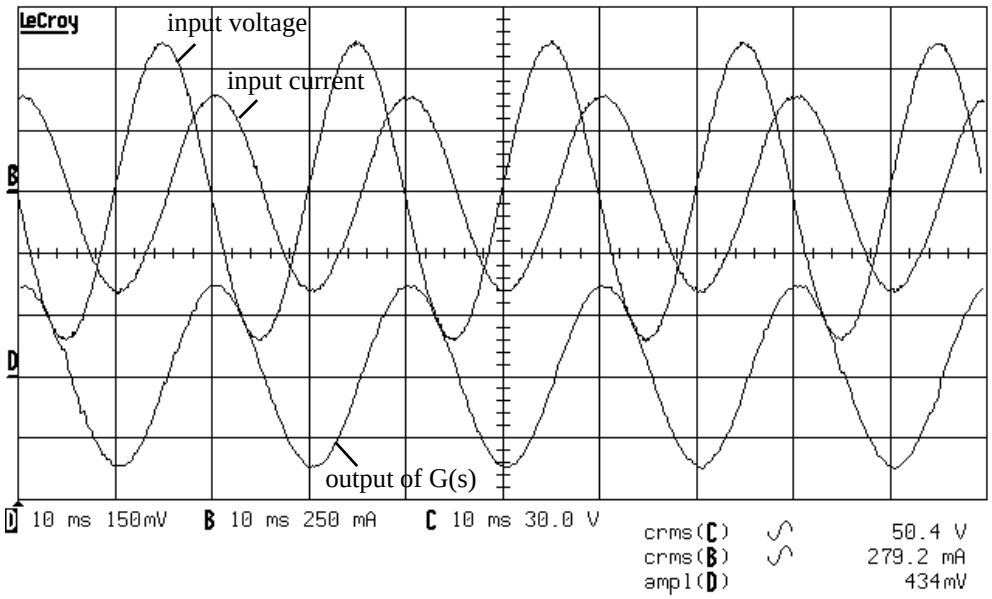


Figure 6-10: Measured waveforms of synthesized pure inductance with input at 50 Hz.

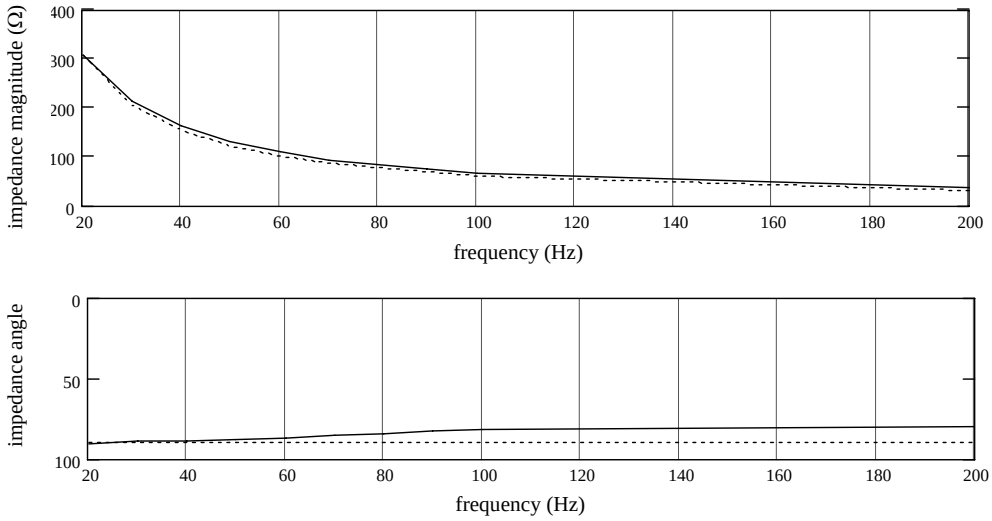


Figure 6-11: Measured impedance magnitude and phase angle of the synthesized 25 μF pure capacitance. Solid line: measured results from the experimental circuit; dashed line: ideal characteristic of a capacitor 25 μF.

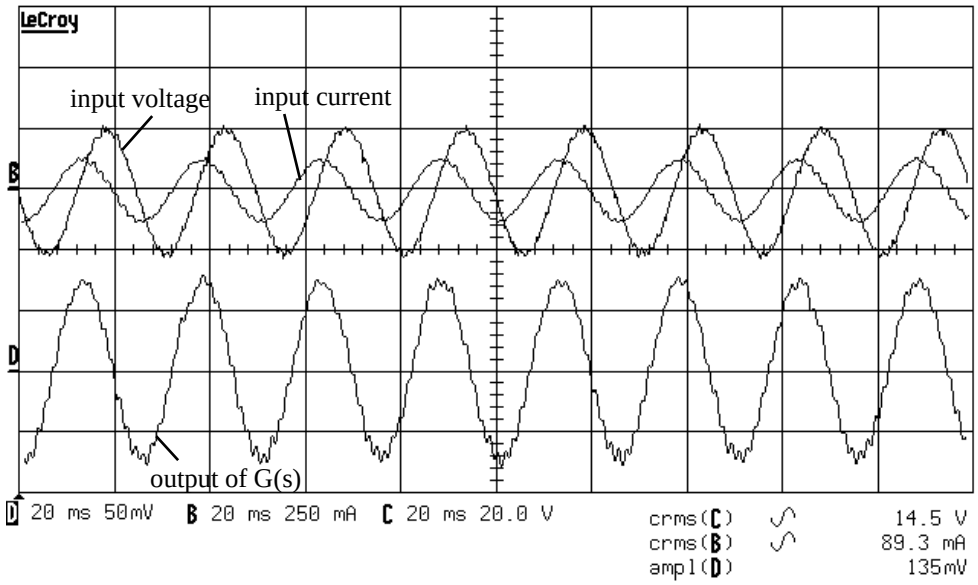


Figure 6-12: Measured waveforms of synthesized pure capacitance with input frequency at 50 Hz.

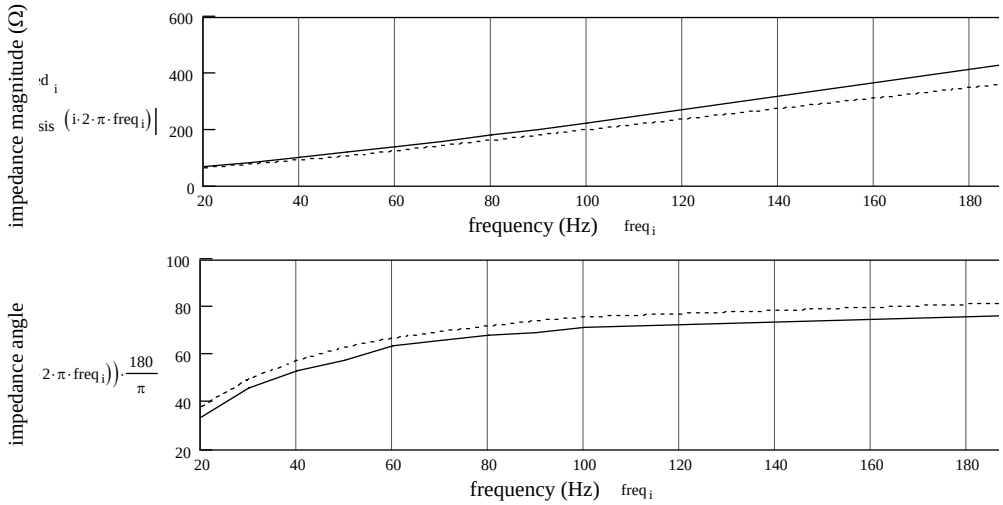


Figure 6-13: Measured impedance magnitude and phase angle of the synthesized inductive impedance of 50 Ω in series with 0.3 H. Solid line: measured results from the experimental circuit; dashed line: ideal characteristic of the inductive impedance.

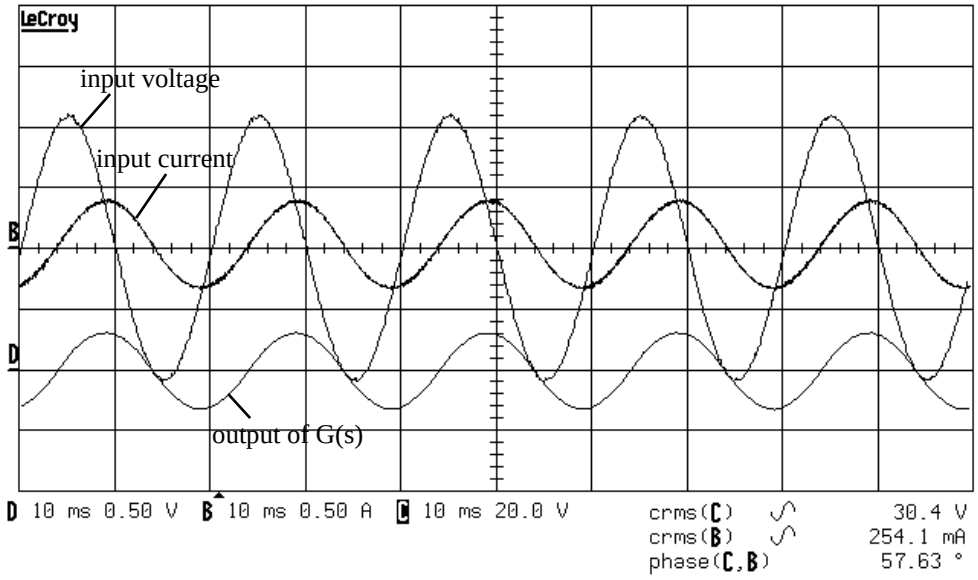


Figure 6-14: Measured waveforms of synthesized inductive impedance with input at 50 Hz.

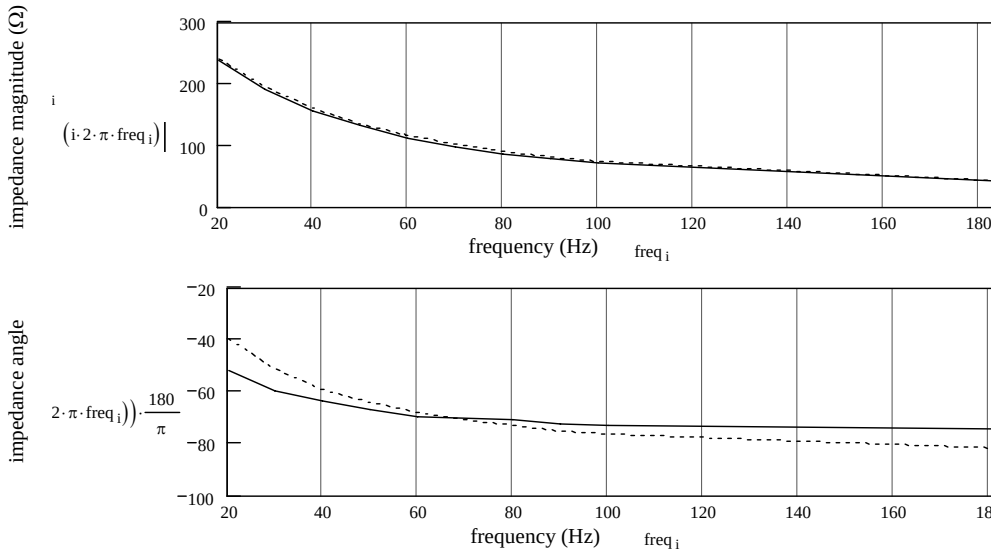


Figure 6-15: Measured impedance magnitude and phase angle of the synthesized capacitive impedance of 300 Ω in parallel with 21 μF. Solid line: measured results from the experimental circuit; dashed line: ideal characteristic of the capacitive impedance.

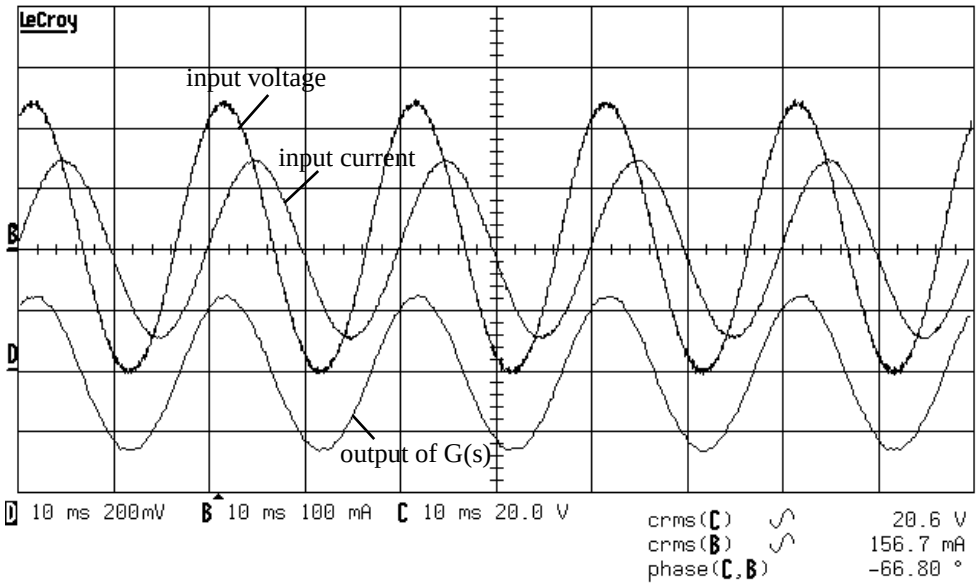


Figure 6-16: Measured waveforms of synthesized capacitive impedance with input at 50 Hz.

6.6 Conclusion

This chapter presents an application of the input rectifierless converter to general impedance synthesis. A minimum configuration of high frequency switching converters for the application has been derived. It shows that the input rectifierless converter configuration presented in Chapter 4 is sufficient for general impedance synthesis provided with a dissipative element or a power source. The method basically involves programming the input voltage to current relationship and providing the necessary power buffering capability. Using the proposed synthesis method, we can imitate any impedance for control purpose, such as in power factor correction. For the purpose of illustration, we have evaluated four cases experimentally, corresponding to the synthesis of pure inductance, pure capacitance, lossy inductive impedance and lossy capacitive impedance.

Chapter 7 A Filterless AC/DC Conversion Technique with Low Switching Loss

7.1 Introduction

In Chapter 3, the problems of the high-frequency AC/DC conversion located at the output of switching converters are addressed. For low output voltage and high output current applications, the conduction loss of the rectifiers and the output filter components increases significantly because it is proportional to the square of the output current. The low output voltage requirement also makes the design of the output filter difficult because the allowed output ripple voltage is usually linked to the output voltage level. According to the general industrial standard, the ripple has to be less than 1% of the output voltage. Larger output filtering choke or capacitor bank is therefore needed in order to meet the specification, but its use is contradictory to the high power density requirement. Furthermore, the high power density requirement requires converters to operate at a high switching frequency in order to reduce the size of magnetic components. However, the switching frequency is limited by the switching loss of semiconductor switching devices. Recently, synchronous rectifiers, which use MOSFET devices for rectification purpose, provide remarkable reduction in conduction loss, but the switching loss can be significant due to the reverse recovery characteristics of the intrinsic body diode of MOSFET devices. This chapter introduces a new technique for the output high-frequency AC/DC conversion that can theoretically eliminate the output filter. In addition, a method is proposed to reduce the switching loss of output rectifiers.

7.2 Output Ripple Reduction with Sinusoidal AC Voltage Sources

It is well known that a three-phase power supply, consisting of three sinusoidal voltage sources, provides much less ripple voltage than a single-phase supply. The reason is that the three voltage sources overlap each other in such a way that when one of the three voltage sources goes out, another voltage source comes in and takes over the output load. Figure 7-1 shows the output ripple voltage waveforms of the two supply systems. Less ripple voltage is expected when more voltage sources share the load and the filter for providing smooth DC voltage becomes less critical.

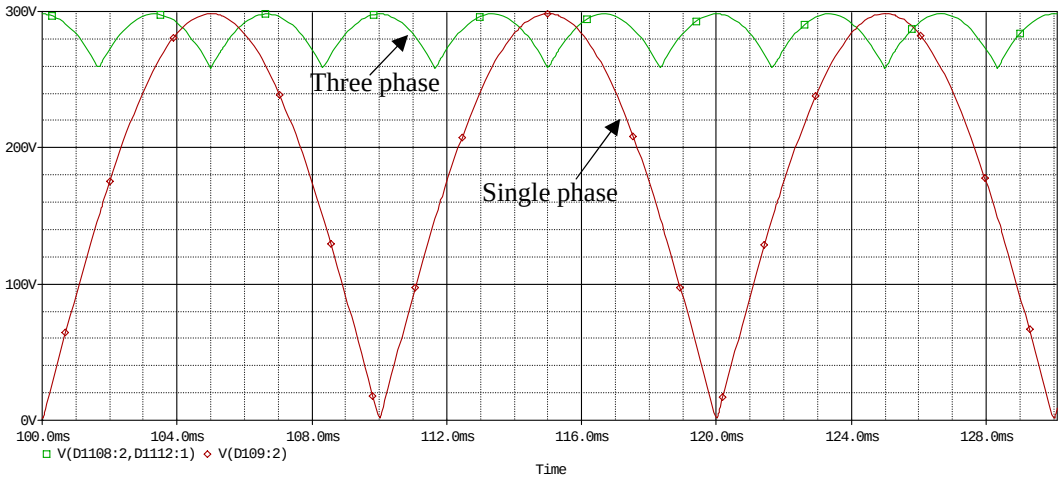


Figure 7-1: Output ripple voltage of three phase and single phase power source after rectification.

7.3 Output Ripple Reduction with Square-Wave AC Voltage Sources

The output ripple voltage produced by a multi-phase sinusoidal voltage source is actually produced in the non-overlapping period where only one source stands out and appears across the load.

For AC voltage sources with rectangular waveforms, the result is very different. A minimum of two AC voltage sources with rectangular waveforms satisfying the following conditions can provide pure DC output after rectification.

- The two AC voltage sources have the same amplitude. Depending on the sign of the output voltage, the two sources may take a positive or negative amplitude.
- The two AC voltage sources overlap in the positive or negative cycle when the output voltage is positive or negative respectively. Thus, at any time, at least one of the voltage sources appears across the output.

Figure 7-2 (a) shows a circuit for simulation with two voltage sources satisfying the above conditions. Figure 7-2 (b) shows the simulated waveforms. It can be observed that the output DC voltage is ripple free even in the absence of an output filter. The output DC voltage is equal to the positive amplitude of the AC sources in this case and hence can be controlled by controlling the amplitude of the AC voltage sources.

The idea was first proposed by Poon [PLP02] and it provides the basics of the filterless AC/DC conversion technique discussed here. In practice, the amplitude of the two AC voltage sources may not be perfectly matched and a very small filter is usually required to filter out the unmatched voltage difference as well as the high-frequency switching noise (much higher than the converter switching frequency).

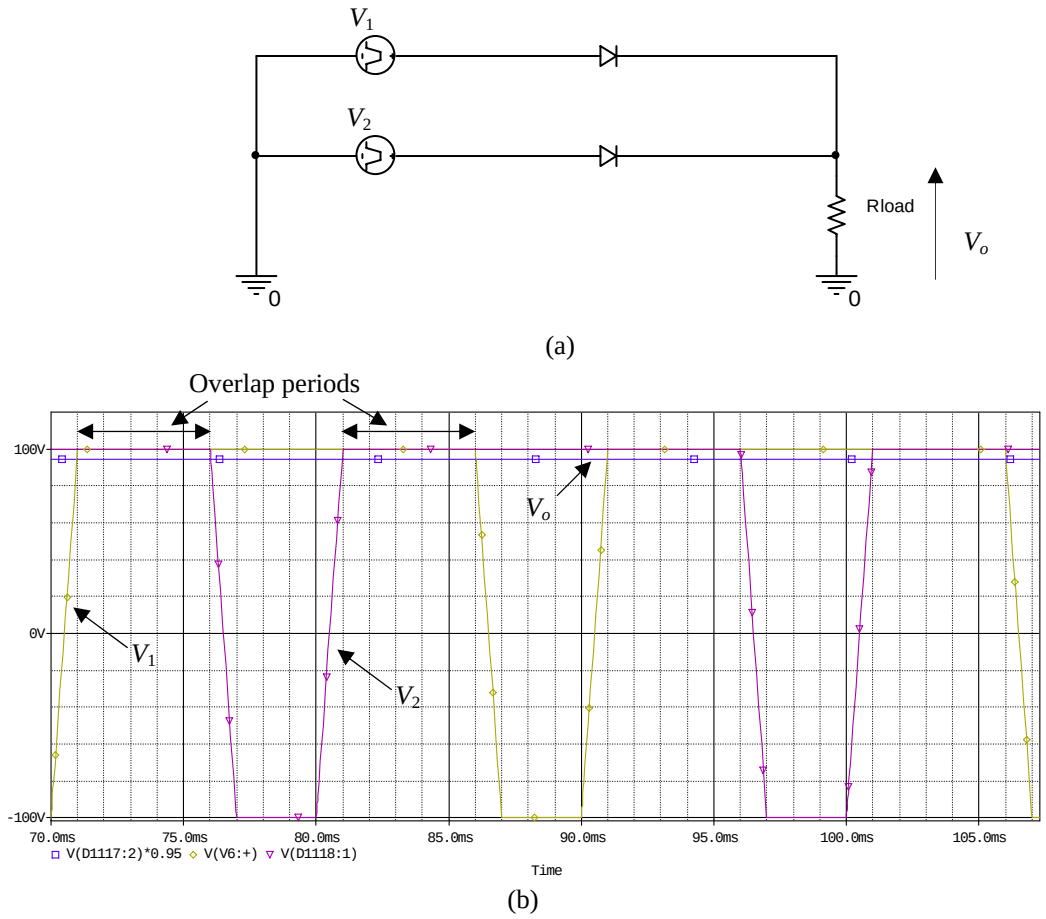


Figure 7-2: Filterless AC/DC conversion. (a) Schematic; (b) simulated waveforms.

7.4 Switching Loss of Rectifiers

Figure 7-3 shows a practical equivalent circuit realizing the afore-described technique. Parasitic inductances due to interconnections and leakage of the main transformer have been included. Figure 7-4 shows the operating waveforms. The rectifier D_1 for rectifying V_1 conducts the output load current during the non-overlapping period from t_0 to t_1 when only V_1 is present as shown in Figure 7-5 (a). The two voltage sources overlap during the period from t_1 to t_2 when V_2 enters the positive cycle with amplitude equal to V_1. During the overlapping period, current does not commute from V_1 to V_2 because there is no voltage difference across the parasitic inductances and the current flowing through D_1 is maintained. It is

described in Figure 7-5 (b). Current starts to commute from V_1 to V_2 only when V_1 goes negative. D_1 is then turned off by a reverse voltage $V_R = V_p + V_n$ as described in Figure 7-4 and Figure 7-5 (c) and the rate of change of the diode current di_{D1}/dt is limited by the parasitic inductance $L = L_1 + L_2$. As the rectifiers are turned off by the negative voltage of the voltage sources, the switching loss is expected to be similar to conventional hard-switching topologies.

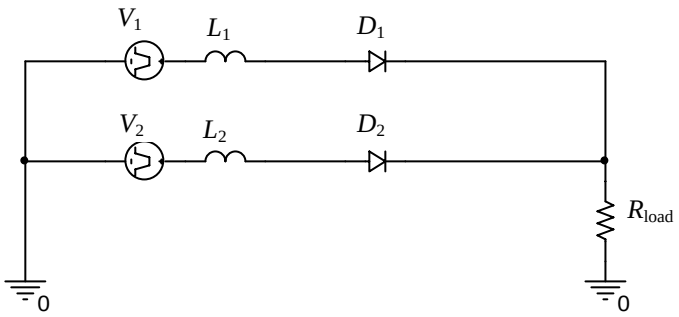


Figure 7-3: Filterless topology with parasitic inductance included.

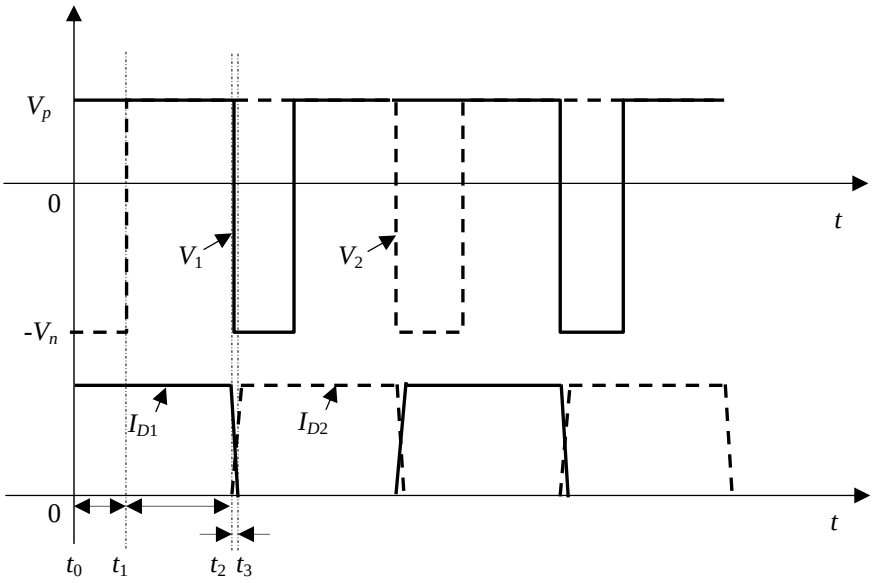
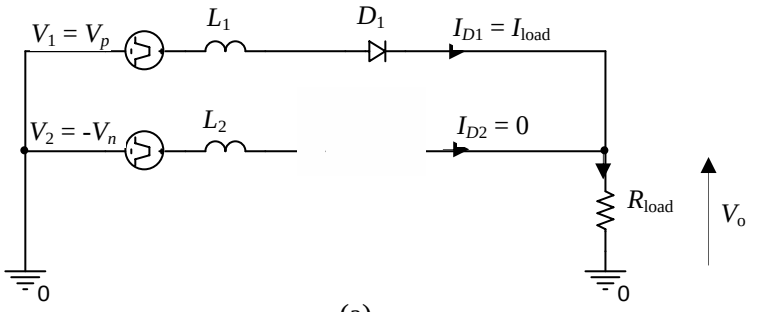
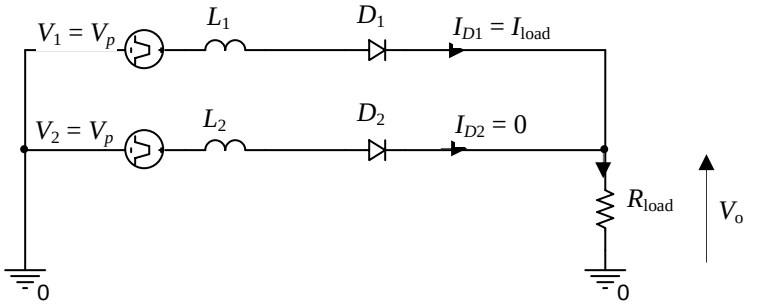


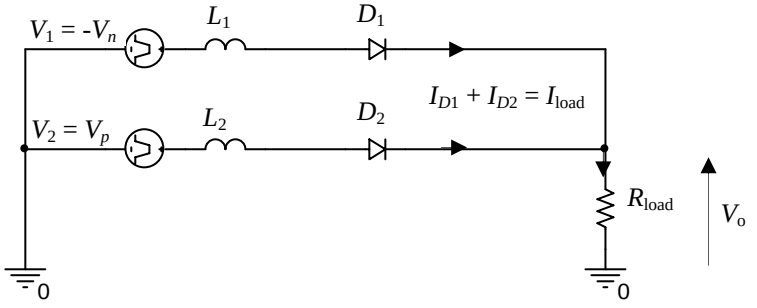
Figure 7-4: Operating waveforms or the filterless topology with parasitic inductance.



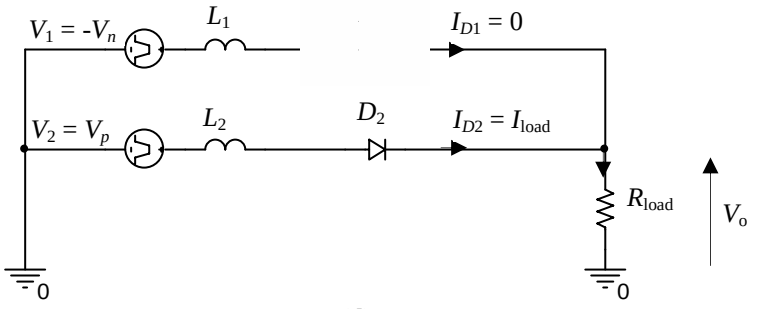
(a)



(b)



(c)



(d)

Figure 7-5: (a) D_1 takes over the loading current from t_0 to t_1; (b) No commutation during the overlapping period from t_1 to t_2; (c) Current commutates from D_1 to D_2 by reverse voltage $V_p + V_n$ during t_2 to t_3; (d) D_2 takes over the loading current after t_3.

In Chapter 3, it has been shown that the switching loss of a rectifier is proportional to the square of the reverse voltage V_R. Thus, reducing V_R can significantly reduce the switching loss of rectifiers. This can be realized by introducing a small ripple voltage V_{ripple} to V_1 and V_2, as shown in Figure 7-6. Instead of square waveform with flat top, the two voltage sources start with higher voltage in the positive cycle and then fall down continuously to lower voltage before entering the negative cycle. This ensures a voltage difference ΔV between the two voltage sources during the overlapping period T_v and the new come-in voltage source, V_2, will always have higher voltage. Thus, current commutation is allowed to start earlier from V_1 to V_2 which will take over the loading current after the overlapping period. If current commutation can be completed within T_v, D_1 can be turned off by a much lower reverse voltage ΔV. Similarly D_2 is also turned off by reverse voltage ΔV by symmetry.

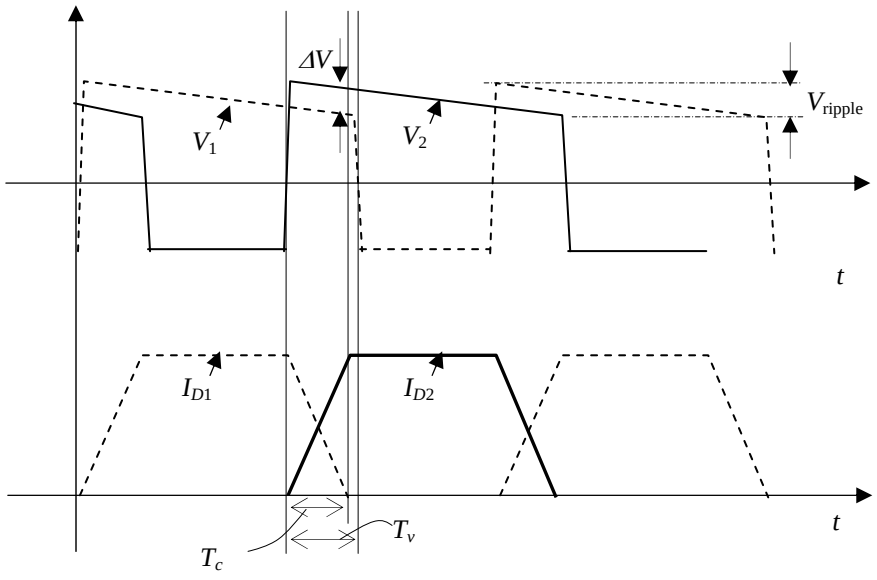


Figure 7-6: Current commutation starts and completes within the overlapping period T_v.

To ensure that low V_R is applied to the rectifiers during current commutations, the current commutation time T_c must be shorter than the overlapping period T_v. The required conditions are given by (7-1) and (7-2).

$$\frac{\Delta V_{avg}}{L_1 + L_2} \cdot T_c = I_{\text{load}} \tag{7-1}$$

$$T_c < T_v \tag{7-2}$$

where I_{load} is the output loading current and ΔV_{avg} is the average voltage difference between the two AC voltage sources within the overlapping period.

Although the output voltage is not perfectly smooth and is dependent on the introduced ripple voltage, the situation is much better than conventional topologies and a significant reduction in the size of output filter is expected. Figure 7-7 shows the simulated waveforms of the proposed switching loss reduction technique with L_1 = L_2 = 80 nH, V_{ripple} = 1 V, switching frequencies of V_1 and V_2 = 100 kHz, V_o = 5 V and I_{load} = 10 A. It can be observed that current commutation is completed within the overlapping period which ensures low turn off voltage of the rectifiers.

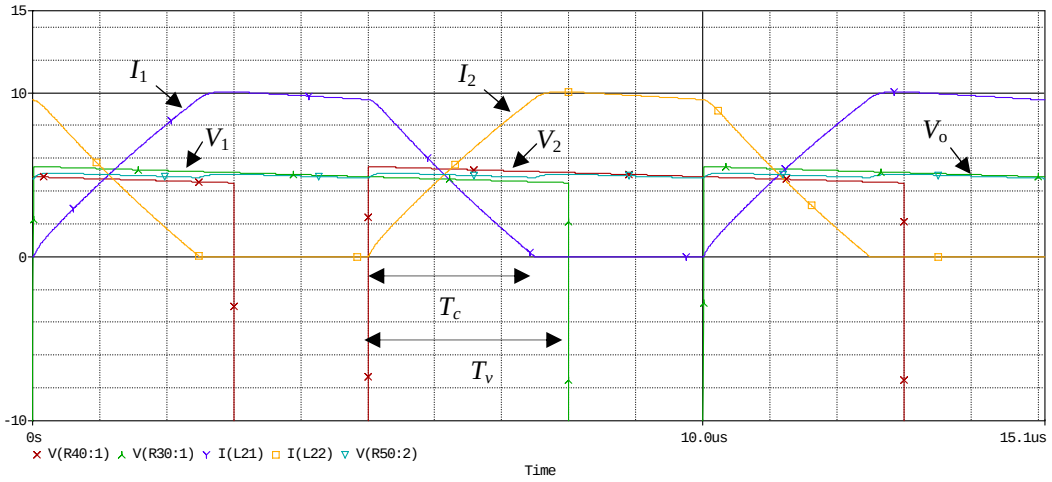


Figure 7-7: Simulated waveforms of the filterless AC/DC conversion implemented with the proposed switching loss reduction technique.

7.5 Conclusion

This chapter has introduced an AC/DC conversion technique which theoretically provides ripple free DC voltage output without the need of an output filter. This immediately provides a solution to the problems associated with the output filter. The switching loss of the rectifiers used in the filterless technique has been analyzed. A technique for switching loss reduction is proposed. This is by reducing the reverse voltage needed to turn off the rectifiers as the switching loss is proportional to the square of the reverse voltage. This allows the switching frequency to be higher and power density to increase.

Chapter 8 Application of Filterless AC/DC Conversion Technique to Realize a Low Output Ripple DC/DC Converter

This chapter presents a new converter topology [PLP02] which implements the two techniques described in Chapter 7. The converter is useful for applications requiring very low output current ripple. The proposed converter consists of two asymmetric half-bridge converters whose output voltages overlap in a finite interval of time. This converter provides well regulated and smooth DC output with a very small output filter. The output voltage is regulated by direct amplitude modulation. Unlike the standard interleaved converters, the proposed converter is robust to input voltage and operating duty cycle variations. Furthermore, equal current sharing is automatically achieved under all conditions, thus ensuring full utilization of the rectifiers for wide input and output ranges. Zero-current turn-off for the output rectifiers can be achieved with proper circuit design proposed in this chapter. An isolated DC/DC converter prototype with 5 V output voltage and 20 A output current has been built to verify the design.

8.1 Introduction

Low output current ripple is an important design criterion for DC/DC converters, especially for low-voltage applications. The removal of current ripple is traditionally achieved by output filter. However, output filter incurs significant loss which lowers the efficiency of the converter. Also, in practice, output filters take up considerable amount of space and limit the operating temperature. If high-capacity

electrolytic capacitors are used, the converter may suffer a reduced life-time. Recently, parallel-connected DC/DC converters with interleaved operating cycles have been a popular design choice for achieving smooth DC output [C95, R98, WXYL00, XRYL01]. However, interleaving can satisfactorily reduce output current ripple only for a narrow range of operating points and the cancellation process is sensitive to input voltage and operating duty cycle variations. Alternatively, a two-stage converter has been proposed to provide low-ripple output [TSZ02]. However, the additional cascaded buck regulating stage inevitably lowers the overall conversion efficiency. In this chapter, we propose a new converter topology which provides smooth DC output for wide ranges of input and load conditions, using a very small output filter. The circuit, consisting of two overlapping asymmetric half-bridge converters, is easy to implement, insensitive to input voltage and operating duty cycle changes, and naturally achieves zero-voltage turn-on of primary switches and zero-current turn-off of output rectifiers. The rest of the chapter is organized as follows. We will introduce the basic topology in the next section, and describe the detailed operation in Section 8.3. Experimental verification will be presented in Section 8.4.

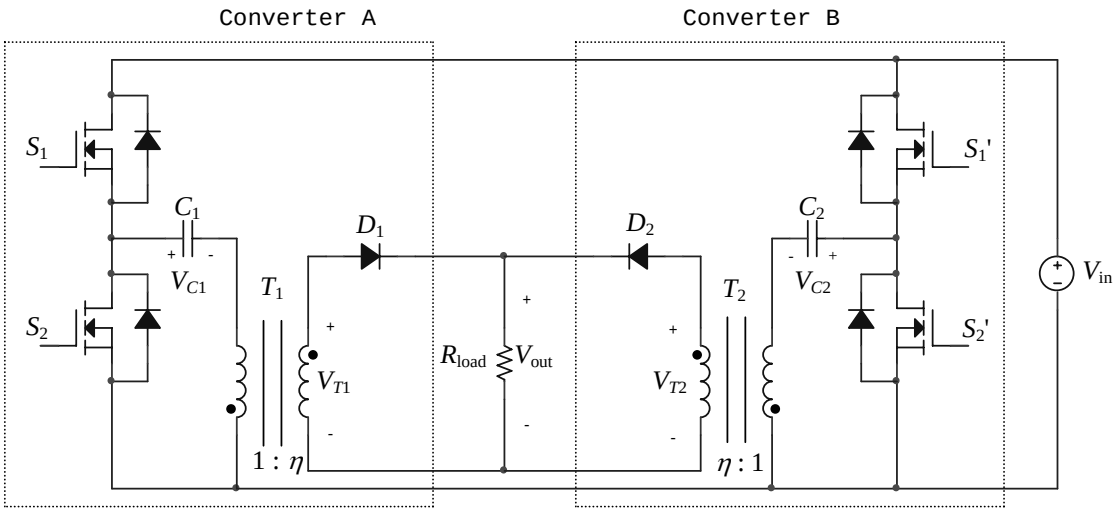


Figure 8-1: Basic circuit topology of the proposed low-ripple output DC/DC converter.

8.2 Operating Principle of New Low-Ripple DC/DC Converter

The proposed converter topology is conceptually shown in Figure 8-1. It consists of two identical asymmetric half-bridge converters [LSGDF97, MALB04, PLP03, IM90, CXL01] with their outputs connected in parallel. Referring to Figure 8-1, S_1 and S_2 in converter *A* are driven asymmetrically with duty cycle always less than 0.5. The gate drive signals for the switches are shown in Figure 8-2. Note that a dead time T_d is introduced to prevent cross conduction between S_1 and S_2, as well as to allow zero-voltage turn-on of the two switches [HSB00, MNMF99, CC02]. When S_1 is on, capacitor C_1 is charged up by the magnetizing current of T_1. At the same time, the polarity of T_1 is arranged such that D_1 is off. Proper design of the magnetizing inductance of T_1 will enable S_2 to turn on at zero voltage after S_1 is off. The energy stored in C_1 will then discharge through the primary winding of T_1 and S_2, and be coupled to the secondary circuit with D_1 forward biased. At this moment, the output voltage V_{out} is equal to VT_1 which is simply ηV_{C1}, where η is the turns ratio of the output winding to the primary winding of T_1 and as well as T_2. The operation of converter *B* is the same as that of converter *A*, with the gate drive signals for S_1' and S_2' in anti-phase to those of S_1 and S_2. The gate drive signals arrangement for S_1, S_2, S_1' and S_2' makes sure that the on-periods of S_2 and S_2' always overlap for two intervals of duration T_v when the duty cycle is less than 0.5, as illustrated in Figure 8-2. Here we assume that T_d is much less than the switching period and thus can be ignored. The overlapping interval is the key feature of the proposed topology which ensures that there is always a DC voltage, equal to either ηVC_1 or ηVC_2. If C_1 and C_2 are large enough, then the output voltage is a smooth and constant DC voltage whose magnitude is given by (8-1) and (8-2).

$$V_{\text{out}} = \eta \cdot V_{C1} = \eta \cdot V_{C2} \tag{8-1}$$

$$V_{\text{out}} = \eta \cdot D \cdot V_{in} \tag{8-2}$$

where D is the duty cycle and η is the turns ratio of transformers T_1 and T_2. Note that the dynamic range of D is from 0 to 0.5.

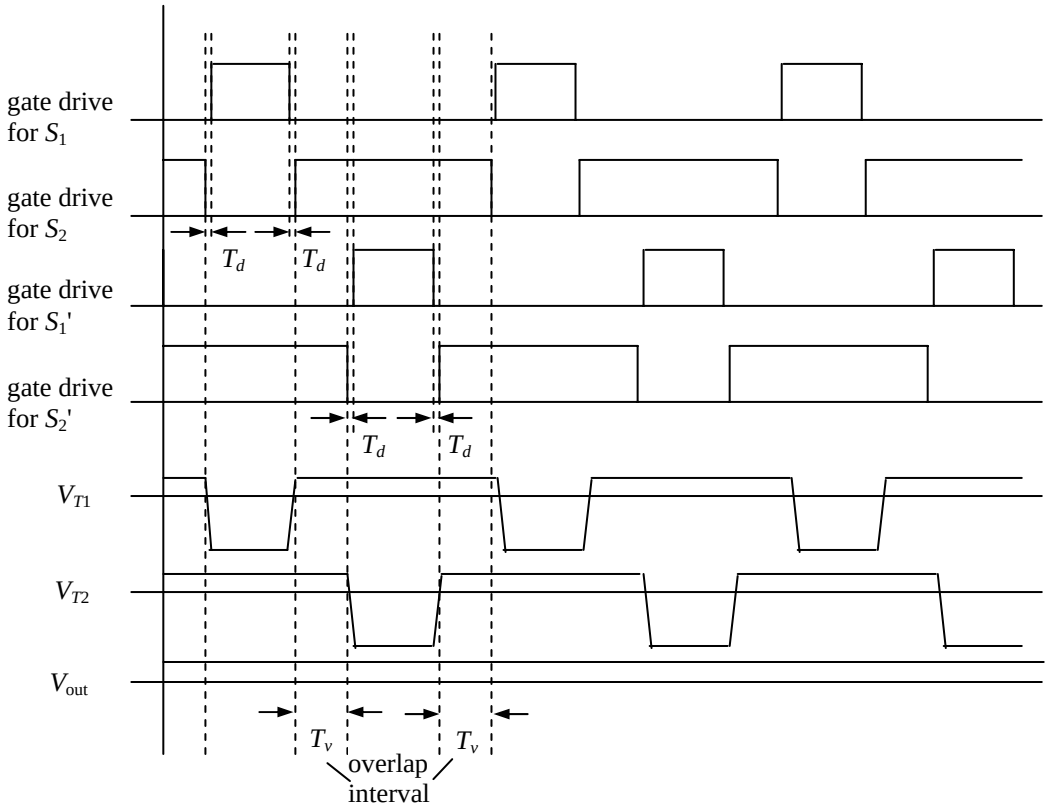


Figure 8-2: The driving signals for the primary switches showing the key feature of overlapping intervals together with transformer secondary voltage and output voltage.

It is worth noting that since the two converters are identical and symmetrically connected, the currents shared by the two output rectifiers are equal under all conditions, thus ensuring full utilization of the output rectifiers.

8.3 Detailed Circuit Operation

The conceptual operation of the converter was described in Section 8.2 and in practice, parasitic elements of the transformers such as magnetizing inductance and leakage inductance exist and the effects to the operation of the proposed converter are discussed in this section.

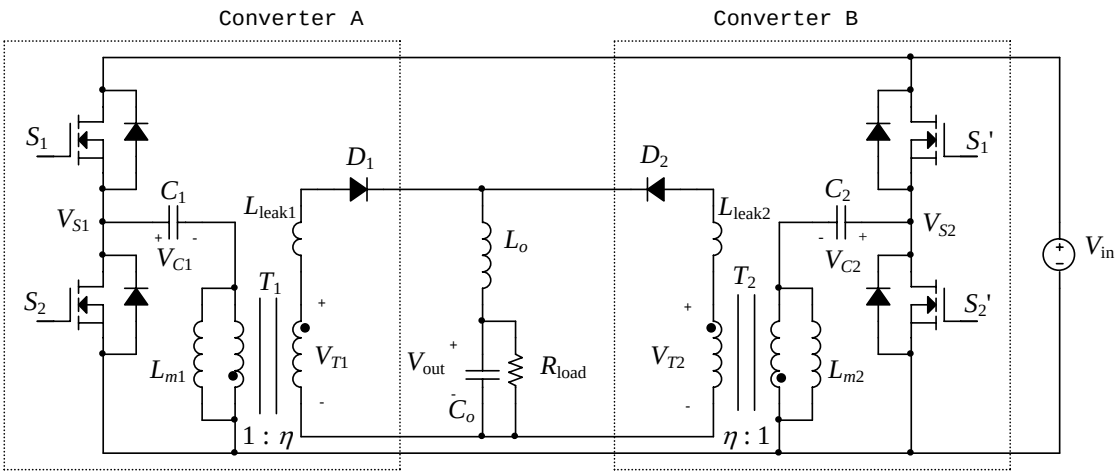


Figure 8-3: Detailed circuit schematic of the proposed low-ripple output DC/DC converter including transformer magnetizing inductance, leakage inductance and a very small output L-C filter.

Figure 8-3 shows the detailed circuit schematic of the proposed converter. It should be noted that an output filter consisting of an inductor L_o and a capacitor C_o has been included. However, unlike conventional output *LC* filters which are required to filter out the rectified square voltage pulse in order to provide smooth DC output, this output filter is simply required to remove unwanted high-frequency voltage ringing and the ripple voltage reflected from C_1 and C_2. Thus, the size of this output filter can be much smaller than that of conventional output filters.

The gate drive signals for the switches, as described in Section 8.2, produce pulsating voltages V_{S1} and V_{S2} across the primary windings of transformers T_1 and T_2 and their series connected DC blocking capacitors C_1 and C_2, as indicated in Figure 8-3.

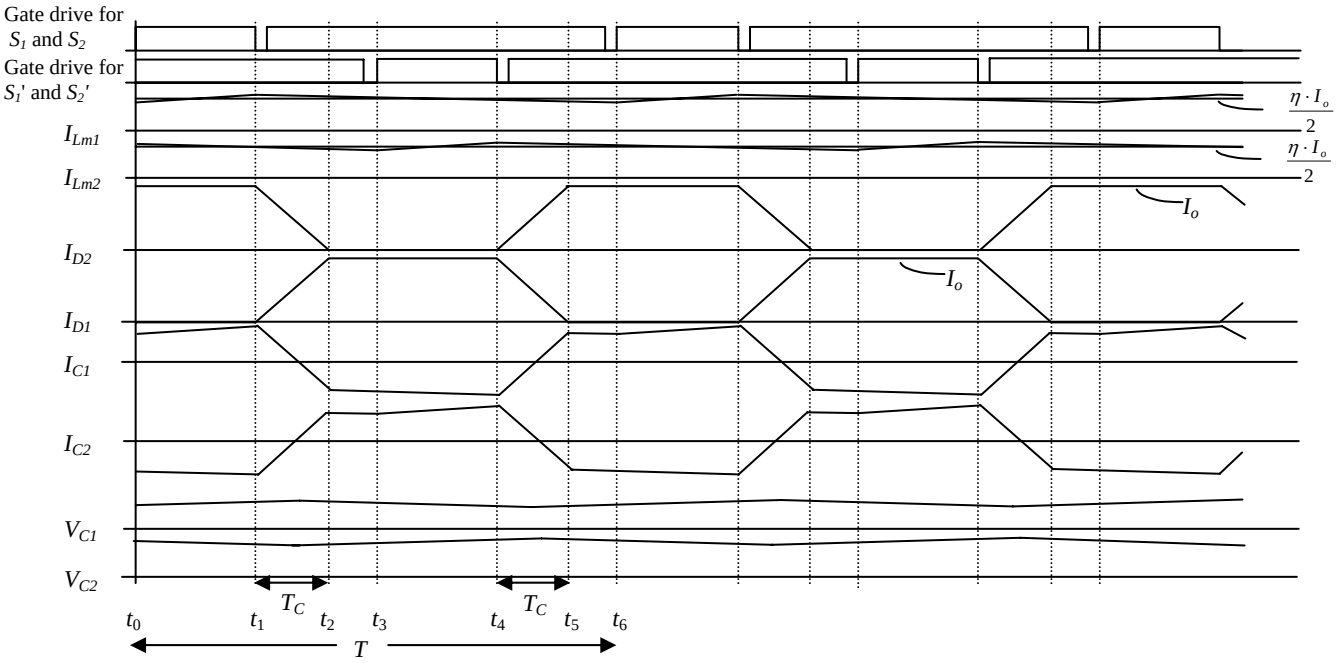


Figure 8-4: Detailed operating waveforms – complete current commutation between converters A and B.

8.3.1 Conditions for complete current commutation during the overlap period

With the introduction of leakage inductances of T_1 and T_2, the output loading current commutates from one converter to the other during each overlap period. The detailed operating waveforms with complete current commutation during the overlap period are shown in Figure 8-4. This allows the output rectifiers to turn off at zero current. At t_1, the output current starts to commutate from converter *B* to converter *A* and ends at t_2 and similarly the output current starts to commutate from converter A to converter B at t_4 and ends at t_5.

The average current commutation rate I_r depends on the average voltage across the two leakage inductors L_{leak1} and L_{leak2}. It is equal to the average voltage

difference, V_{cmm}, between C_1 and C_2 reflected to the secondary sides during the commutation periods. With $L_{leak1} = L_{leak2} = L_{leak}$, I_r is given by (8-3).

$$I_r = \frac{V_{cmm} \cdot \eta}{2 \cdot L_{leak}} \tag{8-3}$$

The commutation ends when the output current is completely handover from converter *A* to *B* and vice versa. The commutation time T_c is given by (8-4).

$$I_r \cdot T_c = I_o \tag{8-4}$$

The condition that ensures complete current commutation is that T_c should be less than the overlap period T_v which is (8-5).

$$T_v = \left(\frac{1}{2} - D\right) \cdot T \tag{8-5}$$

Hence the condition for complete current commutation is given by (8-6).

$$T_c \le \left(\frac{1}{2} - D\right) \cdot T \tag{8-6}$$

The essential parameter V_{cmm} can be calculated by knowing the current flowing through C_1 and C_2. The current waveforms I_{C1} and I_{C2} for capacitor C_1 and C_2 respectively are shown in Figure 8-4. It can be observed that the capacitor current is equal to the difference of two current components, the magnetizing current and the reflected output current of the corresponding connected transformers and converters. Suppose $C_1 = C_2 = C$, $L_{m1} = L_{m2} = L_m$, with the capacitor current profiles as shown in Figure 8-4, it can be shown that V_{cmm} is given by (8-7) where ΔI_{Lm} is the peak to peak value of the magnetizing current.

$$V_{cmm} = \frac{1}{C} \cdot \left[\frac{\eta \cdot (3 \cdot T - 4 \cdot T_c)}{12} \cdot I_o - \frac{T \cdot (1 - 2 \cdot D) - 2 \cdot T_c}{8 \cdot (1 - D)} \cdot \Delta I_{Lm} \right] \tag{8-7}$$

Solving equation (8-3),(8-4) and (8-7), T_c is given by (8-8).

$$T_c = \frac{1}{2 \cdot b_1} \cdot \left[-b_2 + \sqrt{b_2{}^2 + 4 \cdot b_1 \cdot b_0} \right] \tag{8-8}$$

Where

$$b_0 = \frac{2 \cdot L_{leak} \cdot I_o}{\eta}, \quad b_1 = \frac{1}{C} \cdot \left[\frac{\Delta I_{Lm}}{4 \cdot (1-D)} - \frac{\eta \cdot I_o}{3} \right], \quad b_2 = \frac{1}{C} \cdot \left[\frac{\eta \cdot T}{4} \cdot I_o - \frac{(1-2 \cdot D) \cdot T}{8 \cdot (1-D)} \cdot \Delta I_{Lm} \right]$$

To satisfy (8-6) in order to ensure complete current commutation, the capacitance of the DC blocking capacitors should satisfies (8-9).

$$C \le \frac{\eta^2 \cdot T_v}{24 \cdot L_k} \cdot (3 \cdot T - 4 \cdot T_v) \tag{8-9}$$

If the magnetizing ripple current ΔI_{Lm} is designed to be small, the commutation time T_c can be approximated by (8-10).

$$T_c = \frac{1}{8 \cdot \eta} \cdot \left(3 \cdot \eta \cdot T - \sqrt{9 \cdot \eta^2 \cdot T^2 - 384 \cdot L_{leak} \cdot C} \right) \tag{8-10}$$

(8-10) gives important characteristics of commutation time. It is a constant that is dependent on circuit parameters but is independent of the output current and the input voltage.

8.3.2 Output ripple current analysis:

After the current commutation period, only one converter is powering up the output. Considering the conduction period from t_2 to t_4 as shown in Figure 8-4, the DC blocking capacitor C_1 is discharged by the reflected output current and at the same time charged by the magnetizing current of T_1. A good approximation of the rate of change of capacitor voltage is given by (8-11) by assuming that the output

peak-to-peak ripple current ΔI_o is small when compared with the output current I_o, and the magnetizing current is approximately equal to its DC component $\eta I_o / 2$.

$$\frac{dV_{c1}}{dt} = -\frac{\eta \cdot I_o}{2 \cdot C} \tag{8-11}$$

The voltage drop across the output inductor L_o and the leakage inductance L_{leak} is then equal to the reflected voltage of C_1 minus the output voltage V_o. With the output voltage regulated to constant, the output inductor current i_{Lo} is given by (8-12).

$$\frac{d^2 i_{Lo}}{dt^2} = -\frac{\eta^2 \cdot I_o}{2 \cdot (L_o + L_{leak}) \cdot C} \tag{8-12}$$

Solving (8-12) with the approximation that the output voltage V_o is equal to the average voltage of C_1 during the conduction period, the output inductor current is parabola in shape and the peak-to-peak ripple inductor current is given by (8-13).

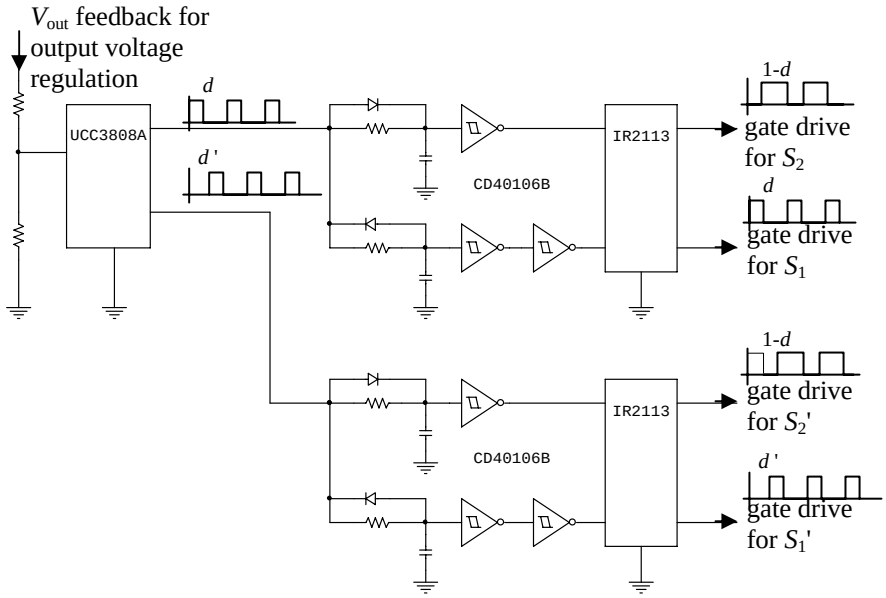
$$\Delta I_o = \frac{\eta^2 \cdot I_o}{16 \cdot (L_o + L_{leak}) \cdot C} \cdot \left(\frac{T}{2} - T_c \right)^2 \tag{8-13}$$

It can be observed from (8-13) that inductor ripple current is proportional to the output current and insensitive to the input voltage. The ripple current amplitude can be reduced by increasing the inductance of the output filtering inductor and maximizing the capacitance of the DC blocking capacitor according to (8-9) for zero current switching of the output rectifiers.

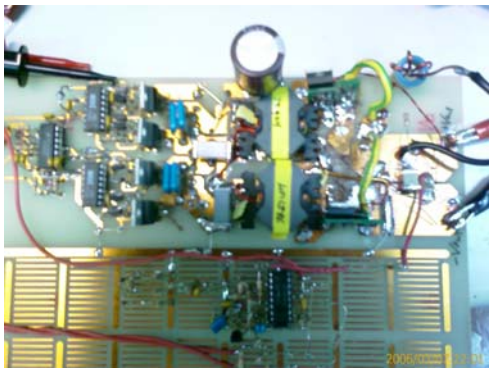
8.4 Experimental Verification

A DC/DC converter using the afore-described topology has been built and tested as shown in Figure 8-5 (b). The input range is 36 V to 72 V, the output voltage is 5 V, and the output current is 20 A (i.e., 100 W output power). To improve the efficiency,

we have employed the active diode technology (a current driven synchronous rectifier technique) for realizing the output rectifiers D_1 and D_2 [PLPX00, XLPP01]. The control circuit of the prototype is realized by a push-pull PWM controller UCC3808A as shown in Figure 8-5 (a). Each output of the push-pull controller is divided into two asymmetric signals by logic inverter gates to drive the upper and lower switches. The dead time for preventing shoot through is implemented by an RC delay circuit.



(a)



(b)

Figure 8-5: (a) The simplified control circuit using commercial push pull controller. (b) A photo of the DC/DC converter using the proposed topology.

8.4.1 Calculation and Selection of Parameter Values

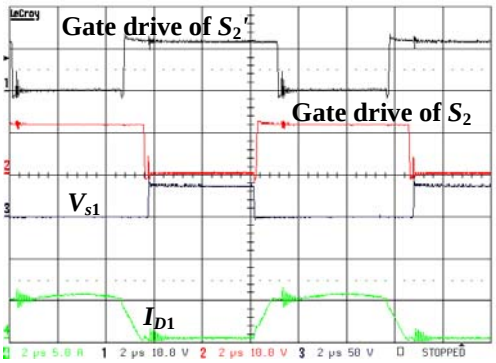
The transformers T_1 and T_2 are designed to have a secondary to primary turns ratio $\eta = 0.347$, magnetizing inductances L_{m1} and L_{m2} of 75 μH and measured output leakage inductance L_{leak} of 101 nH (including connection wiring to the output synchronous rectifiers D_1 and D_2). The switching frequency is set to 100 kHz and the output voltage is regulated to 5 V.

The circuit parameters are calculated according to the equations presented in Section 8.3. To ensure zero-current turn-off of the output rectifiers, C_1 and C_2 should be less than 1.151 μF at 36 VDC input. For practical purposes, 1 μF metallized capacitors are employed. The inductance and capacitance of the output small *LC* filter are 900 nH and 100 μF (ceramic capacitor) respectively.

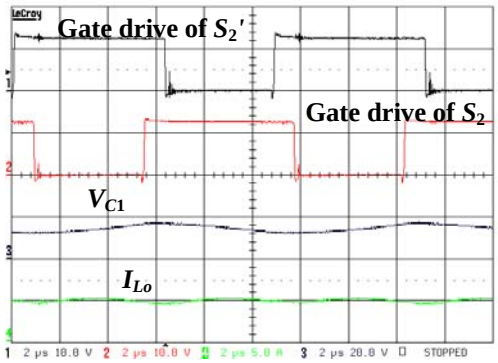
8.4.2 Results

Table 8-1: Measured and calculated key operation parameters.

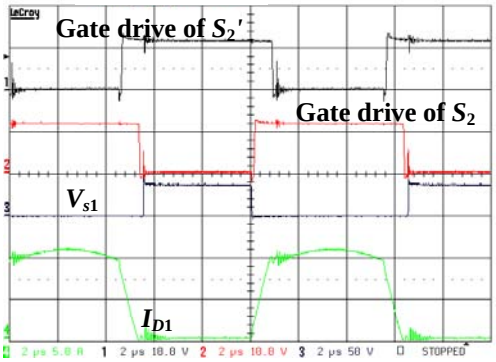
Parameters	Measured and calculated results			
Measured output current - I_o	5 A	20 A	5 A	20 A
Measured output voltage - V_o	5.0817 V	5.0822 V	5.0842 V	5.0848 V
Measured input voltage - V_{in}	36.8 V	36.6 V	72.0 V	71.8 V
Measured commutation time T_c	803 ns	740 ns	960 ns	789 ns
Calculated commutation time T_c using equation (8-8)	764.3 ns	743.3 ns	1030 ns	797.8 ns
Calculated commutation time T_c using simplified equation (8-10)	736.8 ns	736.8 ns	736.8 ns	736.8 ns
Measured peak to peak output current ΔI_o	0.57 A	3.10 A	0.52 A	3.10 A
Calculated peak to peak output current ΔI_o using equation (8-8), (8-13)	0.675 A	2.727 A	0.593 A	2.658 A
Calculated peak to peak output current ΔI_o using equation (8-10), (8-13)	0.684 A	2.736 A	0.684 A	2.736 A



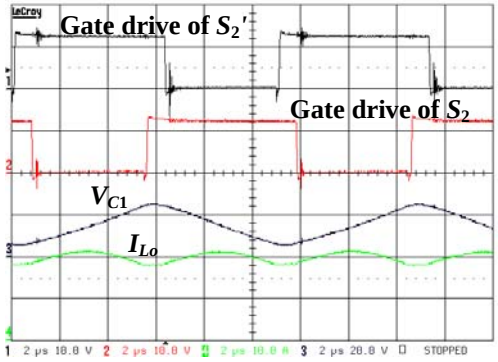
(a): Input voltage = 36V, Output current = 5A



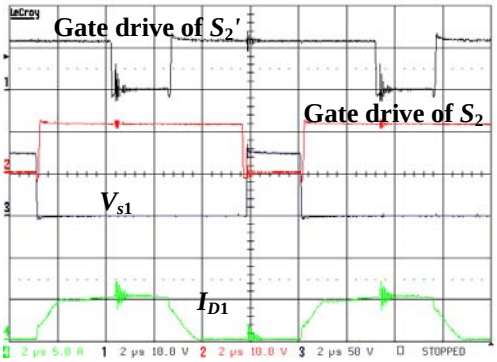
(b): Input voltage = 36V, Output current = 5A



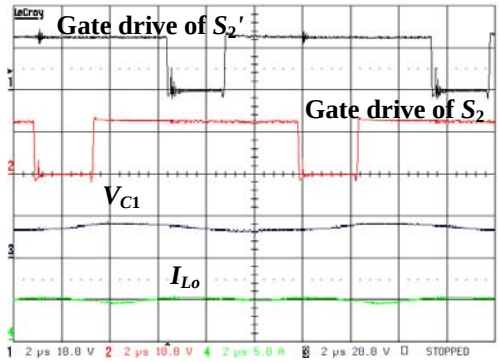
(c): Input voltage = 36V, Output current = 20A



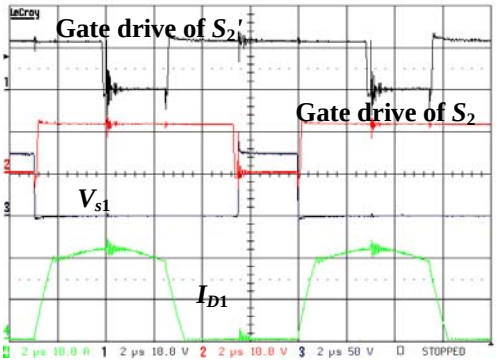
(d): Input voltage = 36V, Output current = 20A



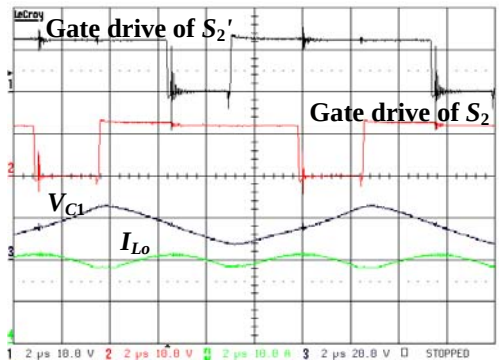
(e): Input voltage = 72V, Output current = 5A



(f): Input voltage = 72V, Output current = 5A



(g): Input voltage = 72V, Output current = 20A



(h): Input voltage = 72V, Output current = 20A

Figure 8-6: (a) – (h): Measured waveforms at different input and output conditions.

Figure 8-6 (a) – (h) shows the measured waveforms of V_{s1}, V_{C1}, gate drive of S_2 and S_2', current of D_1 (I_{D1}) and current of L_o (I_{Lo}) at minimum and maximum input and light and full loading conditions. The output inductor current waveforms are parabola like in shape that matches with (8-12) derived in section 8.3. The waveform of I_{D1} clearly shows that it falls to zero before the switch off of S_2 in all cases. Measured key operation parameters, T_c and ΔI_o are compared with the calculated values in Table 8-1. The results show that the derived equations provide good estimation to the commutation time and output ripple current amplitude. It can also be observed that the measured output ripple current is insensitive to input voltage variations and matches with (8-13).

Conversion efficiencies of the prototype measured at nominal line of 48 VDC are 93.12%, 93.056% and 90.33% at output current of 5 A, 10 A and 20 A respectively. The output ripple and noise waveform is shown in Figure 8-7 (a). With the small filter, the measured peak to peak output voltage ripple at switching frequency is 6.6 mV. With the high frequency voltage spike counted, the measured peak to peak ripple and noise is 28.4 mV. Figure 8-7 (b) shows the zero voltage turn on waveform of S_2 with the drain voltage falls to zero before the gate drive appears.

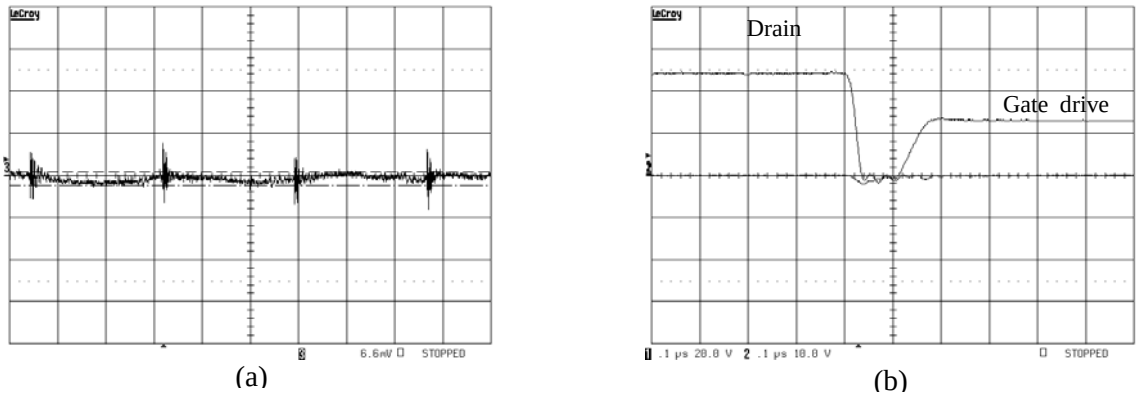


Figure 8-7: (a) Output ripple and noise measurement; (b) Zero voltage switching of S_2.

Remarks: The same output filter is applied to a two-phase isolated interleaved converter which operates at the same switching frequency and with duty cycle of 0.5 at 36 V DC input. It is found that the peak-to-peak output ripple current is 0 A at 36 V DC input, but 27.78 A at 72 V DC input. This is about 9 times higher than that of the proposed topology at worst case. For a single-ended forward converter operating with the same switching frequency and duty cycle of 0.5 at 36 V DC input, the peak-to-peak output ripple current is 27.78 A at 36V DC input and 40.667 A at 72 V DC, which is 13.12 times higher than that of the proposed topology.

8.5 Conclusion

This chapter presents an application of the two techniques described in Chapter 7. A new DC/DC converter using a dual asymmetric half-bridge topology for achieving very low output ripple voltage and high efficiency has been described. This converter requires a very small output filter that improves the conversion efficiency and eliminates the need for low reliability electrolytic capacitors. High efficiency is maintained as a result of zero-current turn-off of the output rectifiers especially when synchronous rectifiers are used. Symmetric structure of the proposed converter also guarantees equal current sharing of the two rectifiers, thereby maximizing their utilization. Experimental results show that the output ripple current is reduced 9 times in the worst case when compared with a two-phase isolated interleaved converter, and about 13.12 times when compared with a single-ended forward converter operating with the same output filter and at the same switching frequency. The measured results also match with the equation given in Section 8.3.

The low output-ripple converter topology described in this chapter is patented with US patent no.: US6,697,266 B2 [PLP02].

Chapter 9 Conclusion

In this thesis, we studied some practical problems associated with AC/DC conversion in switching converters and described several techniques for alleviating these problems. This chapter summarizes the contributions of this thesis and proposes some possible future work.

9.1 Summary

1. Problems associated with conventional low-frequency AC/DC conversion at the input of a switching converter have been reviewed. Two major problems, namely the irreducible power loss and the current harmonic distortion, have been described in detail.
2. Problems associated with conventional high-frequency AC/DC conversion at the output of a switching converter have been discussed, with particular emphasis on the low output voltage and high output current requirements.
3. A general synthesis method for input rectifierless AC/DC converters based on a two-converter configuration has been described. According to this synthesis method, a variety of new input rectifierless topologies can be created systematically. The detailed construction requirements and constraints have been derived systematically. The power circulation problem of the proposed converter configuration has been considered by a power flow analysis and the results provide useful insights into efficiency improvement.

4. Based on the synthesis method for input rectifierless converters, a PFC regulator suitable for applications with high AC mains frequency has been designed. The circuit eradicates the problem of high input current harmonic distortion caused by input rectifiers and the change of dynamic response due to the change of operation mode of inductors. A control mechanism has been proposed that drastically reduces power circulation and provides high converter efficiency.
5. The proposed two-converter configuration for rectifierless AC/DC conversion has been found useful for general impedance synthesis. A proof has been given to show that the two-converter configuration is indeed the minimum configuration required to realize a general impedance synthesizer. Pure inductance, pure capacitance, inductive and capacitive impedances have been synthesized experimentally.
6. A filterless AC/DC conversion technique has been introduced. The technique is based on overlapping two AC voltage sources with rectangular waveforms. The technique provides an ultimate solution to the problems imposed by conventional output filters such as high conduction loss in high output current applications. Based on the filterless approach, a technique for reducing switching loss of the output rectifiers has been proposed.
7. A new converter topology has been designed to demonstrate the filterless AC/DC conversion technique as well as the proposed switching loss reduction technique. The converter provides high conversion efficiency and very low output ripple. The output rectifiers operate at zero-voltage and zero-current turn off that significantly reduces the switching loss. In practice, with a very small output filter, the output ripple current is small and insensitive to

the input voltage variation. Detailed operating principles have been described with design equations given to facilitate the choice of circuit parameters for achieving the desired operations.

9.2 Proposed Future Works

In Chapter 4, we proposed a general input rectifierless AC/DC converter synthesis method using two DC/DC converters. It has been found that there are four different combinations of DC/DC converters in terms of conversion ratios that can realize an input rectifierless AC/DC converter. The differences of the four combinations in terms of performance, such as voltage and current stress of power switches, have not been studied in detail. The information may be useful for a better and more educated topology selection.

The efficiency of the proposed input rectifierless AC/DC converter is sensitive to the amount of circulating power, as shown in the efficiency figures obtained in Chapter 4 (using constant stack-up voltage) and Chapter 5 (with time varying stack-up voltage). Different control schemes are worth studying for further improvement in conversion efficiency.

In Chapter 6, we proposed an application to general impedance synthesis. Stability problems have been encountered during experimental measurements and were solved in a trial-and-error manner. The stability problem is expected to be a major concern if impedance, which is inherently unstable, is to be synthesized, e.g., negative impedance. Detailed stability analysis is necessary.

The output filterless technique shown in Chapter 7 is realized by overlapping two AC voltage sources with rectangular waveforms. The duty cycle of the AC

voltage source should be greater than 0.5 in order to guarantee a certain overlap time period. This limits the dynamic response of the converter. Overlapping multiple AC voltage sources may be able to increase the operating duty cycle range and is worth investigating.

List of Publications

Journal Papers

1. J. C. P. Liu, C. K. Tse, N. K. Poon, B. M. H. Pong and Y. M. Lai, "Synthesis of input rectifierless AC/DC converters," *IEEE Transactions on Power Electronics*, vol. 19, no. 1, pp. 176–182, Jan 2004.
2. J. C. P. Liu, C. K. Tse, N. K. Poon, B. M. H. Pong and Y. M. Lai, "A PFC voltage regulator with low input current distortion derived from a rectifierless topology," *IEEE Transactions on Power Electronics*, vol. 21, no. 4, pp. 906–911, July 2006.
3. J. C. P. Liu, C. K. Tse, N. K. Poon, B. M. H. Pong and Y. M. Lai, "Synthesis of general impedance with simple DC/DC converters," *IEEE Transactions on Power Electronics*, submitted.
4. J. C. P. Liu, N. K. Poon, B. M. H. Pong and C. K. Tse, "Low output ripple DC/DC converter based on an overlapping dual asymmetric half-bridge topology," *IEEE Transactions on Power Electronics*, accepted.

Conference Papers

5. J. C. P. Liu, C. K. Tse, N. K. Poon, Y. M. Lai and B. M. H. Pong, "Synthesis of input rectifierless AC/DC converters," *IEEE Power Electronics Specialists Conference Record*, pp. 17–21, Vancouver, June 2001.

6. J. C. P. Liu, C. K. Tse, N. K. Poon, Y. M. Lai and B. M. H. Pong, “A PFC topology with low input current distortion suitable for aircraft power supplies,” *IEEE Power Electronics Specialists Conference Record*, pp. 20–25, Aachen, Germany, June 2004.
7. J. C. P. Liu, C. K. Tse, N. K. Poon, B. M. H. Pong and Y. M. Lai, “General impedance synthesizer using minimal configuration of switching converters,” *Proc. European Conference on Circuit Theory and Design*, pp. 173–176, Cork, Ireland, August 2005.
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