THE HONG KONG POLYTECHNIC UNIVERSITY

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STUDY OF HfAlO HIGH-*k* GATE DIELECTRIC THIN FILMS ON COMPRESSIVELY STRAINED $Si_{1-x}Ge_x$

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CERTIFICATE OF ORGINALITY

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Abstract

To find a suitable high-*k* dielectric material in replacing SiO_2 as gate dielectric is an urgent demand in the advanced complementary metal-oxide-semiconductor (CMOS) technology. However, the carrier mobility degradation due to the high-*k* gate dielectric induced phonon and Coulomb scattering effect limits the application of high-*k* gate dielectric materials. Compressively strained $Si_{1-x}Ge_x$ (SiGe) surface channel may serve as a solution to the carrier mobility degradation problem. However, interfacial reaction, in particular the GeO_x formation and Ge diffusion that result in large amount of interfacial traps and charge traps in the dielectric, is a main issue. On the other hand, HfAlO is a promising high-k gate dielectric as substitute for SiO_2 due to its thermodynamic stability and low leakage current. In this project, synthesis and characterizations of HfAlO thin films on SiGe are studied. The reactions at the film-SiGe interface and the corresponding electrical properties of the MOS capacitors are investigated.

The HfAlO high-*k* gate dielectric thin films were grown on compressively strained $Si_{1-x}Ge_x$ (x=17%) by pulsed-laser deposition (PLD) technique. Structural and electrical properties of the films were investigated by x-ray photoemission spectroscopy (XPS), high-resolution transmission electron microscopy (TEM), and measurements of high-frequency (1MHz) capacitance-voltage (*C-V*), conductance-voltage (*G-V*) and leakage current-voltage *(I-V)*.

The ratio of Hf/Al in the HfAlO films, oxygen partial pressure and substrate temperature during film growth, and post-growth thermal annealing temperature are important factors to the film and interfacial properties. The results revealed that the ratio of Hf/Al affects the flat-band voltage shift of the MOS capacitors, and thus the density of fixed charges and charge traps in the dielectric films. Low oxygen partial pressure results in extremely thin interfacial layer, while high oxygen pressure results in thicker

interfacial layer. The post-growth thermal annealing is also found to be critical to the interfacial reaction. The optimized condition for the HfAlO film growth has been achieved.

In order to study the merit of HfAlO compared to HfO_2, interfacial reactions and electrical properties of HfO_2 and HfAlO high-*k* gate dielectric films on strained SiGe fabricated by PLD are investigated. It is found that HfAlO films can reduce GeO_x formation and reduce Ge segregation at the interfacial layer during the film annealing process. Such suppression effect is attractive since it can reduce defects and degradations, and thus improve the carrier mobility. In addition, the suppression of GeO_x formation by utilizing the Si-cap on SiGe layer is investigated, and it revealed a more significant suppression effect when both HfAlO dielectric and Si-cap were associated.

List of Publications

Journal Paper:

1 K. K. S. Curreem, P. F. Lee, K. S. Wong, J. Y. Dai, M. J. Zhou, J. Wang, and Q. Li, "*Comparison of interfacial and electrical characteristics of HfO_2 and HfAlO high-k dielectrics on compressively strained $Si_{1-x}Ge_x$*" Appl. Phys. Lett. **88,** 182905 (2006).

Conference Paper:

2 K. K. S. Curreem, P. F. Lee, J. Y. Dai, "*Effects of oxygen partial pressure on structural and electrical characteristics of HfAlO high-k gate dielectric grown on strained SiGe by pulsed-laser deposition*" (accepted for publication to Materials Science in Semiconductor Processing on June 2006)

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I struggled so long if I should insert His name in this thesis because I afraid this work may disgrace His name. Nevertheless, I finally decided to do so because I have tried my best. My heavenly Father, the greatest shepherd, the Lord of the lords and the King of the kings, thank you for your constant guidance and protection in all of the time. May your name be glorified as you are deserved! In Jesus name I pray. AMEN!

The last but not least, I would like to express my great appreciation to my beloved one, Miss K.W. Hau (*Gloria*) and our parents, without their patient support and endless love, completion of this thesis would not have been possible.

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Chapter 1

Introduction

1.1 Why high-*k* dielectrics?

The success of semiconductor industry relies on continues improvement of integrated circuit performance since the late of 1970's and the rapid progress since the late of 1980's. This improvement is achieved by continues shrinking the metal-oxide-semiconductor field effect transistor (MOSFET) in size. Indeed, the reduction of the device dimensions allows higher density of devices being integrated on Si chip, providing higher speeds and lower cost [1].

One of the key elements that allowed the successful scaling of silicon-based MOSFETs is the excellent material and electrical properties of the gate dielectric in these devices: SiO_2. This material indeed gives several important features that have allowed its use as gate insulator. First of all, amorphous SiO_2 can be thermally grown on silicon with excellent control in thickness and uniformity, and naturally forms a very stable interface with the silicon substrate. Secondly, SiO_2 presents an excellent thermal and chemical stability, which is essential for the complementary MOS (CMOS) process that includes annealing processes at high temperature (up to 1000 °C). A remarkable note should be pointed out is that the band gap of SiO_2 is very large (~9 eV), which offers excellent electrical isolation properties with large energy band offsets with the conduction and valence bands of Si. Furthermore, in modern CMOS processing, the

defect charge densities are in the order of 10^{10} /cm^2, and interface state densities of ~10^{10} cm^{-2}eV^{-1} are routinely obtained[1]. All these superior properties allow the fabrication of properly working MOSFET with SiO_2 gate dielectric layers in past decades.

Nevertheless, as will be discussed in the next section, the improvement achieved by further aggressive down scaling of MOSFET can not withstand for the advanced CMOS technology due to the unacceptable excessive leakage current flowing through the MOS structure. In ultrathin SiO_2 gate dielectric, charge carriers can flow through it by direct tunneling mechanism as illustrated in Fig. 1.1.

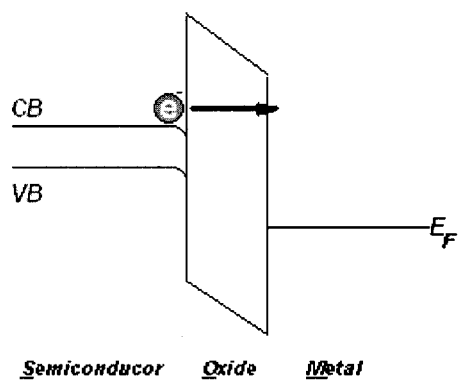

Fig 1.1 Schematic energy band diagram of a MOS structure illustrating an example for direct tunneling of an electron from the Si substrate through the gate oxide and reaches the gate. CB and VB are denoted as conduction band and valance band, respectively. E_F is the Fermi energy of the gate electrode[2].

From the electrical point of view, the MOS structure behaves like a parallel plate capacitor: when a gate voltage V is applied to the gate, the charges on the metal gate are compensated by opposite charges in the semiconductor; while the latter charges form the surface channel connecting the source (S) and drain (D) of the transistor. Figure 1.2 illustrates the typical MOSFET structure.

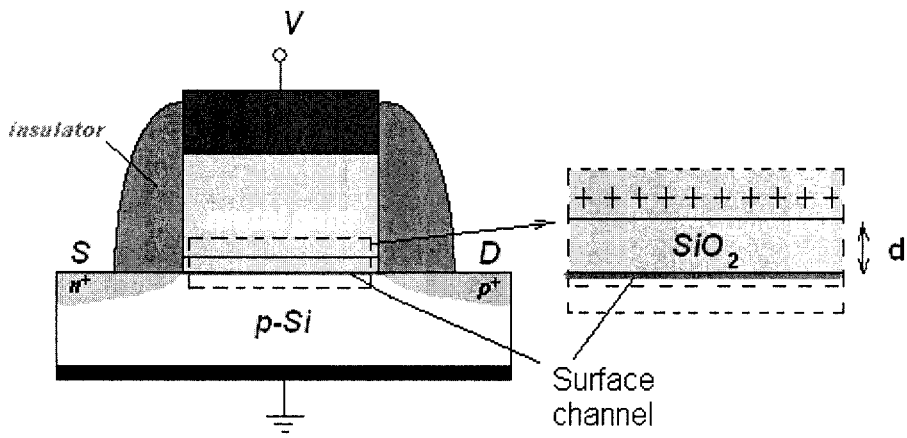

Fig 1.2 Schematic diagram of a typical *n*-MOSFET (where *n* is denoted as n-channel in *p*-type semiconductor), illustrating the behavior of the MOS structure when a voltage V_g is applied to the gate. The inset shows that the MOS structure can be illustrated as a parallel plate capacitor[3].

The capacitance C of this parallel plate capacitor is given by

$$C = \frac{A\varepsilon_r}{d} (\equiv \frac{Ak\varepsilon_o}{d}), \qquad 1.1$$

where A is the capacitor area, ε_r is the permittivity of gate oxide, d is the gate thickness, k is the dielectric constant and ε_o is the permittivity of free space (8.85×10^{-14} Fcm^{-2}). From the equation (1.1), it appears that decreasing of thickness d allows us to

increase the capacitance of the parallel capacitor, and hence increase the number of charges in the surface channel for a fixed value of V. However, as pointed out above, the SiO_2 layer thickness is approaching its limit which means that it can not contribute the increment of capacitance anymore. Therefore, in order to achieve the goal, an alternative way of using a gate oxide with a relatively higher dielectric constant (so-called high-k material) than that of SiO_2 is proposed. As a result, one can then use a substantially thicker (physical thickness) gate layer for reduced leakage and improved gate capacitance.

1.2 High-k dielectrics as alternative gate oxides

Among the potential candidates HfO_2, Al_2O_3, Y_2O_3, La_2O_3, Ta_2O_5, TiO_2 and ZrO_2, etc, HfO_2 is considered as one of the most promising high-k gate dielectrics to replace SiO_2 due to its favorable properties including high-k value (k=25), good thermodynamic stability on Si, low leakage current (at amorphous phase) and large band gap (5.7 eV) [4-7]. Therefore, the HfO_2/Si system has received tremendous attention. Nevertheless, it has been found recently that, pure amorphous HfO_2 exhibits crystallization during thermal annealing (>550 ^{o}C) and it induces grain boundaries enhanced leakage current which is unfavorable for the application. More importantly, it acts like a transparency to oxygen atom at elevated temperature[8-11]. Upon thermal annealing in oxygen gas ambient, oxygen atom can fast diffuse through the gate oxide and react with Si substrate forming an uncontrollable relatively low-k interfacial layer. This interfacial layer limits the further scaling of the equivalent oxide thickness (EOT) of HfO_2.

Indeed, there is a systematic consideration (will be presented in more details in Chapter 2) of the required properties of gate dielectric, which are the key guidelines for selecting an alternative gate dielectric. Upon the examinations, almost all of the investigated high-k dielectrics, including HfO_2, turned out to be favorable in some of these areas, but so far, there is almost no candidate can satisfy all respects to the guidelines. As a result, it initiates the research of other encouraging alternatives which are pseudobinary alloy systems such as $(ZrO_2)_x(SiO_2)_{1-x}$ and $(HfO_2)_x(SiO_2)_{1-x}$ where $(0 \le x \le 1)$[1]. By this purpose, combination of two oxides is possible to combine the desirable properties from two different oxides and eliminate the undesirable properties of each individual material.

Several research groups (including our work) have demonstrated that HfO_2 alloyed with Al_2O_3 (alumina) grown on Si is one of the potential pseudobinary system which can improve the properties[8-13]. They show that the new system can increase the crystallization temperature considerably which can stabilize the HfAlO dielectric in an amorphous structure up to a temperature of 1000 °C [9]. As Al_2O_3 is a good barrier of oxygen, it brings this desirable property to HfAlO dielectric. Furthermore, regarding to the combination offering a reasonable value of dielectric constant (9~25) and large band offset values to Si, HfAlO is considered as a very attractive and promising alternative candidate.

Nevertheless, serious degradation of carrier mobility has been found for almost all high-*k* dielectrics when applied on MOSFET. It is believed that such degradation is

induced by phonon and Coulomb scattering effect upon utilizing such high-*k* materials grown on Si substrate[14-16]. It degrades the carrier mobility considerably and therefore, becomes an important issue and challenge on utilizing high-*k* materials into MOS transistor.

There are several approaches to solve the high-*k* material induced channel mobility degradation problem, such as utilizing Ge and strained-Si channel [17,18]. Compressively strained-SiGe channel (the merit of this high mobility channel will be presented in next section) is considered as another approach toward the solution. For this reason, the system of high-*k* gate dielectric of HfO_2 grown on compressively strained-SiGe has been considered to be a novel system, and the study on its characteristics has attracted a great deal of attention. Nevertheless, the HfO_2/SiGe system meets another problem of Ge segregation and diffusion from the SiGe substrate [19,20]. This problem greatly affects the electrical performance because of the formation of Ge-rich layers and uncontrollable formation of GeO_x inside the dielectric film and at the interface[19]. Such characteristics lead to high interface state density, large amount of interfacial traps, charge traps and high fixed charge density at the SiGe based MOS transistors and they should be solved.

1.3 Why compressively strained SiGe?

To know the meaning of compressively strained SiGe, an illustration is given in Fig. 1.3. When an epitaxial Si film is grown on a Si substrate, Fig. 1.3(a), because there is a natural matching of the crystal lattice, it results in a high quality single crystal layer. On the other hand, when an epitaxial SiGe film is grown on a Si substrate, Fig. 1.3(b), because there is a large difference of lattice constants (lattice mismatch between Ge and Si is ~4.17 %), it forms a compressively strained SiGe layer.

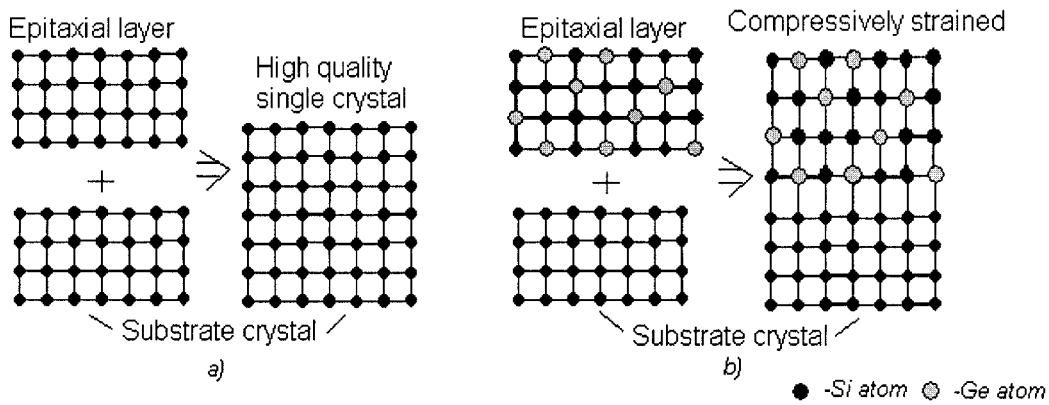

Fig 1.3 Schematic representation of compressively strained SiGe layer[21].

Indeed, the degree of the compressive strain depends on the size of lattice mismatch, and the size of lattice mismatch depends on the fraction of Ge in the $Si_{1-x}Ge_x$ layer. In this thesis, compressively strained $Si_{1-x}Ge_x$ with a fraction x equal to 0.17 was used. For convenient reason, strained SiGe will be simply used in the following

Chapters.

The merit of compressively strained SiGe channel which can offer an enhancement on hole mobility is attributed to its intrinsic electronic properties: difference in band structure (bandgap) between unstrained and strained states. Although, compressive strain in the effective channel region alters its energy level on conduction band is small (not shown), the effect on the near band edge of valence band is significantly large as illustrated in Fig.1.4. This effect has a very strong correlation to the basic property of the hole mobility.

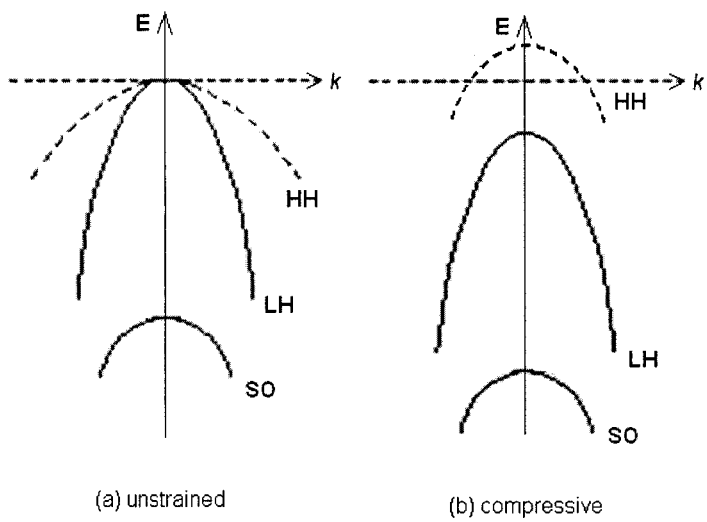

Fig 1.4 E-*k* diagrams for the Si valence band under two strain conditions. The shifts and deformations are schematic only and are exaggerated for emphasis[22].

Figure 1.4 is two exaggerated schematic diagrams showing the effect of compressive strain on the shift of the band alignment and the shape deformation. In unstrained material, Fig. 1.4(a), the valence band maximum is composed of three bands:

the degenerate heavy-hole (HH) and light-hole (LH) bands at k=0, and the split-off (SO) band which is slightly lower in energy. Very close proximity (44 meV) of the SO band to the top of the valence band is one of the reasons for poor hole transport properties in Si. It should be noted that the "heavy" and "light" refer to the effective masses of the holes in each band notated in Fig. 1.4.

In compressively strained material, in Fig. 1.4(b), it shows that the strain not only alters the energy bands shift but also deforms the shape of bands. The latter effect reduces the effective mass in the bands considerably and is the origin of hole mobility enhancement offered by compressively strained SiGe.

There are two points need to be noticed. First, since there is a critical thickness of strained SiGe on Si, beyond that thickness, the strain will be relaxed by forming misfit dislocations at the SiGe/Si interface. Therefore, the thickness we selected is 15 nm which is less than the critical thickness and there is no interfacial dislocations found. Second, the compressive strain in SiGe can be relaxed when it is subjected to thermal annealing at a temperature higher than 800 °C. Therefore, the process temperature in the project should be much lower than 800 °C. In addition, it is not an easy task to fabricate a high quality epitaxy SiGe film on Si without defects in the past. However, advanced fabrication techniques make this possible nowadays. In my project, the SiGe/Si wafers were fabricated by *IQE silicon compounds Co. Ltd.* based on our design.

1.4 Literature review and motivation

In semiconductor industry, it is highly desirable to find a suitable high-*k* material to replace the currently used SiO_2 as the gate dielectrics in future advanced CMOS technology. Muller *et al.*[23] found that the full band gap of SiO_2 can only be obtained after at least two mono-layers of SiO_2. This indicates that within two mono-layers of the Si channel interface, oxygen atoms do not have the full arrangement of oxygen neighbors and therefore can not form a full band gap that exists in the "bulk" of the SiO_2 film. Tang *et al.*[24] even set an *absolute physical thickness limit* of SiO_2 of 7 Å. Furthermore, with this rapid shrinking, excess leakage current becomes a serious problem. Chin *et al.*[25] reported that the leakage current of a Al_2O_3 film on Si substrate with a thickness of 48 Å, which equals to an equivalent oxide thickness of 21 Å, exhibited a leakage current of 10^{-8} A/cm^{-2} at 1 *V* gate bias. Compared to ~10^{-1} A/cm^{-2} for 21 Å of pure SiO_2, it is seven orders of magnitude lower.

Furthermore, Fig. 1.5 shows an interesting plot reported by Brar *et al.* which demonstrates a comparison of SiO_2 and high-*k* dielectric with respect to the current density and the power consumption as a function of gate voltage [26]. The SiO_2 curve is measured while the curve representing the high-*k* dielectric is calculated. The curve for a high-*k* film has shown about four orders of magnitude reduction on leakage current and four orders of magnitude lower power consumption than that of SiO_2. They clearly suggested the essential calling of a gate dielectric with a permittivity higher than that of SiO_2 to meet the low-power application requirements.

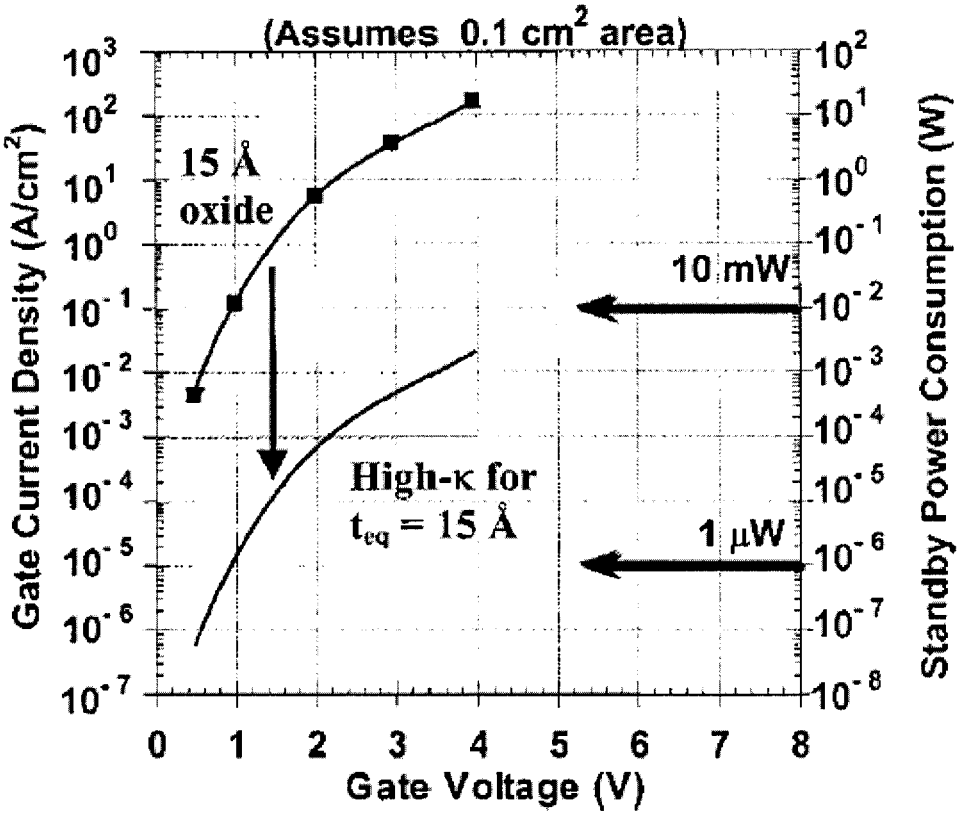

Fig. 1.5 Power consumption and gate leakage current density for a chip which has a 15 Å-thick SiO_2 gate dielectric compared to the potential reduction in leakage current by an alternate dielectric exhibiting the same equivalent oxide thickness. Assumes at total gate area of 0.1 cm^2 [26].

Recent publications proposed that HfO_2 is a very promising alternative dielectric material to work with Si substrate[4,6,27]. However, poor interfacial stability induced degradation of the channel mobility in HfO_2/Si system was reported. This poor interfacial stability was interpreted to be caused by the incapable properties of HfO_2, nearly transparency to oxygen and low crystallization temperature were suggested to be two of those [13,28,29].

In year 2000, J. Robertson and his co-workers have reported one of the most influencing theoretical calculations on the electrical and relevant properties of various potential high-*k* materials (as illustrated in Table 1), and some of the most fundamental and crucial requirements for the selection guidelines were provided with clear explanations. One of the most important requirements they have emphasized is that, the electron barrier or conduction band (CB) offset is one of the key criteria in the selection of a gate oxide, and it must be over 1 eV in order to give adequately low leakage current. Those guidelines directly eliminate most of the high-*k* materials.

It agitates, however, an increasing interest to use multilayer or compounds of two-oxide dielectric of Al_2O_3 and HfO_2 in order to improve the dielectric properties and interfacial stability with Si [30]. Al_2O_3 is probably the only material that has a band gap (~8.8 eV) and band alignment similar to those of SiO_2, and it is a good barrier to oxygen and ionic transport. On the other hand, HfO_2 has a relatively high-*k* value of ~25 and relatively small band gap (~5.7 eV). Compensative characteristics for the composite of HfO_2 and Al_2O_3 were well studied by various groups [9,29,31,32]. They have demonstrated that the adding of Al_2O_3 into HfO_2 can retard the crystallization of pure HfO_2 up to 1000 °C and evidenced that the composite is thermodynamic stability on Si interface. Li and his co-worker found that both the thermal stability and the resistance to oxygen diffusion of HfO_2 are improved by adding Al, and they stated that the improvement is closely correlated with the Al percentage in the films [9]. The finding from M.H. Cho and his co-workers also suggested that the thermal stability of HfAlO films is largely depended on the incorporation of Al_2O_3 into the HfO_2 film[33]. Therefore, it is possible to

achieve high-*k* dielectric oxide with high thermal stability as well as high band gap using a composite of these two oxides.

Table 1.1 Comparison of relevant properties of high-*k* candidates

Material	Dielectric constant (*k*)	Band gap E_g (eV)	ΔE_c (eV) to Si	Crystal structure(s)
SiO_2	3.9	8.9	3.2	Amorphous
Al_2O_3	9	8.8	2.8	Amorphous
Y_2O_3	15	5.6	2.3	Cubic
La_2O_3	30	4.3	2.3	Hexagonal, cubic
Ta_2O_5	26	4.5	1-1.5	Orthorhombic
TiO_2	80	3.5	1.2	Tetragonal (rutile, anatase)
HfO_2	25	5.7	1.5	Monoclinic, tetragonal, cubic
ZrO_2	25	5.8	1.4	Monoclinic, tetragonal, cubic

Calculated by Robertson. Ref [30]

Nevertheless, the charge carrier mobility degradation in the field effect transistor channel due to the high-*k* dielectric induced phonon and charge scattering effect limits the implementation of high-*k* gate dielectrics in the advanced CMOS technology [16,17,19,34]. It has been noticed recently that the use of the enhanced hole mobility of strained SiGe surface channel may be a way to overcome the mobility degradation problem. Z.H. Shi and his co-workers have reported that 36% drive current enhancement for compressively strained $Si_{0.8}Ge_{0.2}$ over Si was exhibited for PMOSFETs with physical channel length down to 180 nm [18]. The physical channel length down to 70 nm was also reported by them as 17% drive current enhancement was achieved. The

faction (x) in the Si_xGe_{1-x} under investigation by many research groups is ranged from 0.15-0.3, and all of the results clearly demonstrated that using strained SiGe channel is a good method to solve the hole mobility issue in high-*k* gate transistor [14,17,18,20].

Therefore, it is potentially attractive to use this high mobility channel of compressively strained SiGe together with high-*k* gate dielectrics. However, the conventional thermal oxidation of SiGe leads formation of Ge-rich layers at the oxide/SiGe interface and causes serious degradation of oxide properties. This effect causes serious problem for use of SiGe in mainstream MOSFET devices. Some research groups have showed that an ultrathin Si-overlayer (or called Si-cap layer) on the strained SiGe shown satisfactory results on suppressing such problem caused by Ge segregation and Ge piled up at the oxide-substrate, and one of the groups has shown that Si-cap of 20 Å was effective to prevent the problem and commented that the electrical properties obtained from their samples with the Si-cap were superior to those without the Si-cap [17].

Most recently, there were many investigations focused on the thermal stability of HfO_2 dielectric on SiGe epitaxial layer [16,17,19,34]. In contrast, to the best of our knowledge, there are few reports demonstrating that HfAlO can serve as a solution to the degradations when applied on SiGe surface channel MOSFET by its compensated and superior properties [8].

In this thesis, I carried out the study of synthesis and characterization of HfAlO

ultrathin films on compressively strained SiGe. The ratio of Hf/Al in the HfAlO films, oxygen partial pressure and substrate temperature during film growth, and post-growth thermal annealing were studied, and the importance of each of the above parameters was revealed. In addition, the comparison between HfAlO and HfO_2 on the interfacial reactions and electrical properties was carried out. Suppression effects on interfacial reaction were demonstrated, indicating the superior of using HfAlO gate dielectric over pure HfO_2. Furthermore, the suppression effect was also demonstrated upon utilizing an ultrathin Si-cap layer (~9 Å) on the compressively strained SiGe.

1.5 The scope of the thesis

In *Chapter 1*, the driving force to implement high-*k* dielectrics in MOSFET and the motivation (with literature review) to study the HfAlO on compressively strained SiGe channel are introduced.

Background knowledge of synthesis and characterization of HfAlO ultrathin films on compressively strained SiGe will be presented in *Chapter 2*. In particular, pulsed-laser deposition (PLD) technique, MOS physics and various structural characterization techniques such as x-ray photoemission spectroscopy (XPS) will be introduced.

Chapter 3 presents the investigation results of structural and electrical property dependence on the ratio of Hf/Al in the HfAlO films, oxygen partial pressure and

substrate temperature during film growth, and post-growth thermal annealing temperature. It also presents a discussion section on electrical characterization such as capacitance-voltage (C-V) and conductance-voltage (G-V).

Chapter 4 focuses on the comparison study between HfAlO and HfO_2 on the interfacial reactions and electrical properties when implemented on SiGe. Suppression effects of HfAlO, in comparison with HfO_2, to the GeO_x formation at the interface, and the effect of ultrathin Si-cap layer on SiGe are presented.

In the last chapter--*Chapter 5*, a conclusion of this thesis and proposed future work will be presented.

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Chapter 2

Background Knowledge and Research Methodology

In Chapter 2, background knowledge about the film growth technology, metal-oxide semiconductor (MOS) physics and characterization methods will be introduced. In particular, I will introduce the following three parts: (1) Principles and methods of pulsed-laser deposition which is the main growth technique in this project; (2) Basic knowledge about the MOS device, which is fundamental theory in our basic consideration when selecting alternative gate dielectrics and assessing a dielectric/substrate system; (3) Structural and electrical characterization methods.

2.1 Deposition technique

Pulsed-laser deposition (PLD) technique is considered as one of the most flexible technique to offer a large freedom of choice in target materials, ablation characteristics, ambient gas and its pressure, and substrate temperature. All these parameters influence film structure and properties. It is especially attractive for research on novel dielectrics due to its short cycle time and one can easily investigate a wide range of different materials and compositions at a relatively low operation temperature. For these reasons, it satisfied our desires on investigating the potentially attractive composite of HfO_2 and Al_2O_3 high-k gate dielectrics with different Hf:Al atomic ratios. In addition, the compressive strain in the SiGe epitaxial layer can be maintained during the low deposition temperature. Regarding to MOS transistor application with high-k materials,

controlling the thickness and roughness of the thin films down to an atomic scale is crucial.

Figure 2.1 shows the schematic diagram of a PLD system consisted with a vacuum chamber, a temperature controllable substrate holder, and target material. An excimer laser with wavelength of 248 nm is placed outside the vacuum chamber.

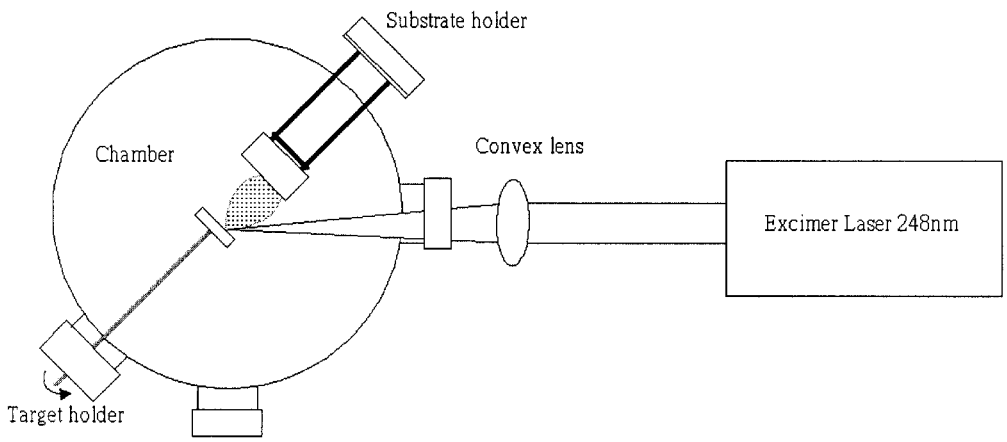


Fig 2.1 Schematic diagram of the PLD system.

The physical processes involved in PLD are rather complicated despite its ease of operation. The PLD process can be divided into three stages: (1) ablation, (2) plasma expansion, and (3) deposition of ablated species on a substrate with subsequent film growth. All stages are indeed important in understanding the relationship between film deposition condition and the resulting film properties.

2.1.1 Ablation

The PLD process starts with the ablation of the target material. A couple of hundred high-power laser pulses irradiate the target during the deposition of a thin film of around 10 nm. When the high power and tightly focused laser pulses irradiate the target, photon energy is absorbed by the target surface inducing target-laser interaction with a thermal cycle. Photon energy absorption generates thermal energy and this thermal energy conducts into a certain depth of a localized area and causes localized material melting. Indeed, the process is highly dependent on the laser fluence, the absorption coefficient, thermal conductivity of specific target and the target surface characteristics such as the film stoichiometry and its roughness. When this thermal energy cannot be fully dissipated through thermal conduction, the local temperature rises rapidly. Once it reaches the material's evaporation temperature, material is dissociated and ablated out from the target.

2.1.2 Plasma expansion

For the second stage, the vaporized material including ions, electrons, molecules and neutral atoms started to expand into surrounding ambient gas driven by the pressure gradient. The dynamic flow of these energetic particles constitutes luminous plasma which is called a plume. This plume is highly dependent on the ambient pressure: a divergent plume is the result when film is deposited in high vacuum, while convergent plume is the result when film is deposited in poor vacuum. Due to the plume dimension dependence on the background pressure, it raises the importance of target-to-substrate

distance in the deposition process. P.E. Dyer and his co-workers[1] have shown that E/P_o is the scaling parameter for the plume length, where E is the laser-pulse energy, and P_o is the background gas pressure.

Our frequently used ambient gas is oxygen gas and the use of it is mainly to compensate the loss of a constituent. The oxygen pressure mainly affects the oxygen content in the deposited thin film. For example, the deposited oxide thin film tends to suffer from oxygen vacancy defects when the deposition is done in oxygen gas deficient. Therefore, more understanding of these interrelation parameters is crucial to determine the general growth condition and to understand the film's structural and electrical characteristics.

2.1.3 Deposition of ablated species on a substrate with subsequent film growth

The ablated material will finally reach the substrate surface and, consequently a layer of film will be deposited. In this stage, the surface temperature of the substrate is the key parameter which offers the ablated species mobility through several atomic distances on the surface for sticking to favorable sites. The substrate temperature is also one of the key parameters to determine the ultimate structure of the films: epitaxial, polycrystalline or amorphous. Of course, films with different structure have their own specific uses. For the high-k dielectric in MOS transistor application, in order to avoid the grain boundary induced current leakage in polycrystalline structure, an amorphous structure is rather preferable. In amorphous films, no crystalline structure can be

identified.

Above is the brief introduction for the three physical processes involved in the PLD, and indeed every single physical process can be expanded into a chapter to discuss. However, it is not the scope for this thesis. One can clearly see that PLD involves various deposition parameters, and each of them can strongly affect and determine the film properties. Once we acquire the understanding on each parameter and the experience on handling them, various structures can be fabricated.

2.2 MOS physics

2.2.1 Ideal MOS structure

A MOS structure is shown in Fig. 2.2, where d is the thickness of the gate oxide and V is the applied voltage on the metal gate electrode. Indeed, both the interfaces of metal/oxide and oxide/semiconductor are important to the device performance. In this thesis, we will particularly focus on the latter interface. This oxide/semiconductor interface, which is usually about ~5 Å thick, serves as a transition between the atoms associated with the materials in the gate oxide and semiconductor. As will be discussed, this interface region can considerably alter the overall characteristics of the MOS capacitor.

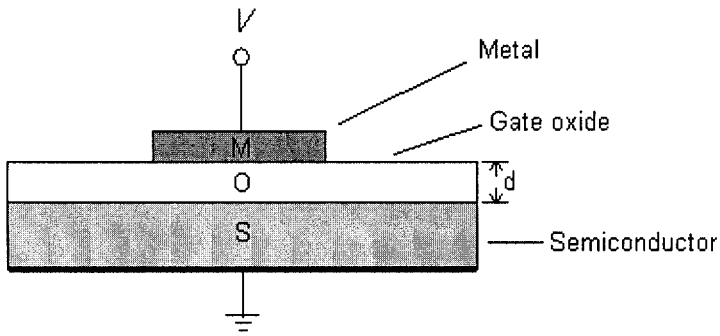


Fig 2.2 Metal-oxide-semiconductor (MOS) structure[2].

Figure 2.3 shows an energy band diagram of an ideal MOS capacitor (p-type semiconductor) for V=0 where Φ_M is the metal work function, χ is the semiconductor electron affinity, E_g is the semiconductor band gap, Φ_B is the potential barrier between the metal and dielectric, and Ψ_B is the potential difference between the Fermi level E_F and the intrinsic Fermi level E_I. An ideal MOS capacitor is defined as three points:

(1) At zero applied voltage, there is no energy difference between Φ_M and the semiconductor work function Φ_S or the work function difference Φ_{MS} is zero, i.e.

$$\Phi_{MS} \equiv \Phi_M - \left(\chi + \frac{E_g}{2q} + \Psi_B \right) = 0, \qquad (2.1)$$

In other words, the band is flat (flat-band condition) when there is no applied V.

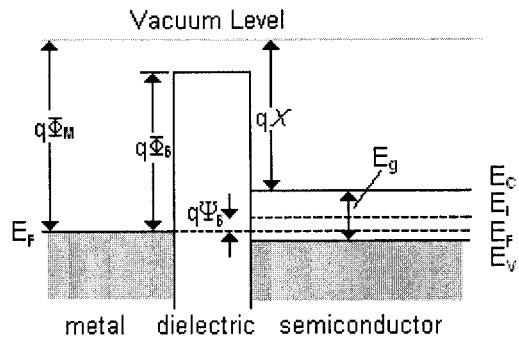


Fig 2.3 Energy-band diagram of an ideal MOS capacitor at V=0 for *p*-type semiconductor[3].

(2) The only charges which can exist in the structure under any biasing conditions are those in the semiconductor and those with the equal but opposite sign on the metal surface adjacent to the insulator.

(3) There is no carriers transport through the gate oxide under dc bias condition or the resistance of the insulator is infinity.

When this ideal MOS diode is biased with positive or negative voltages, there are basically three cases which may exist at the semiconductor surface as illustrated in Fig. 2.4.

(1) When a negative voltage (V<0) is applied to the metal gate, Fig. 2.4(a), the top of the valence band bends upward. Since the carrier density depends exponentially on the energy difference (E_F-E_V), this band bending causes an accumulation of majority carriers (holes) near the semiconductor

surface. For an ideal MOS capacitor, there is no current flow in the structure. So the Fermi level remains constant in the semiconductor. This is the case of "accumulation".

(2) When a small positive voltage (V>0) is applied, Fig. 2.4(b), the bands bend downward, and the majority carriers are depleted. This is the case of "depletion".

(3) When a larger positive voltage is applied, Fig. 2.4(c), the bands bend even more downward such that the intrinsic level E_i at the surface crosses over the Fermi level E_F. At this point the number of electrons at the surface is larger than that of the holes, and the surface is thus inverted which is the case of "inversion". Similar results can be obtained for *n*-type semiconductor.

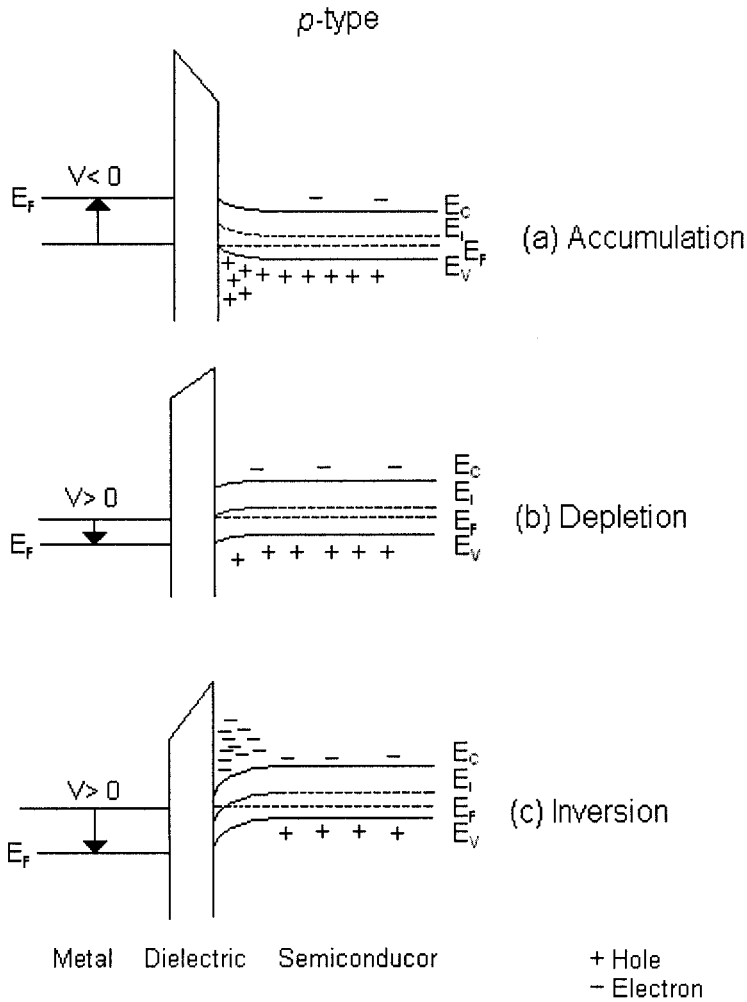


Fig 2.4 Three different cases of the energy band diagrams for an ideal MOS structure when $V \neq 0$ for p-type semiconductor[4].

Figure 2.5(a) shows a more detailed band diagram at the surface of an ideal MOS capacitor (*p*-type semiconductor) with bands bending of the semiconductor identical to that shown in Fig. 2.4 (c). Figure 2.5 (b) shows the corresponding charge distribution.

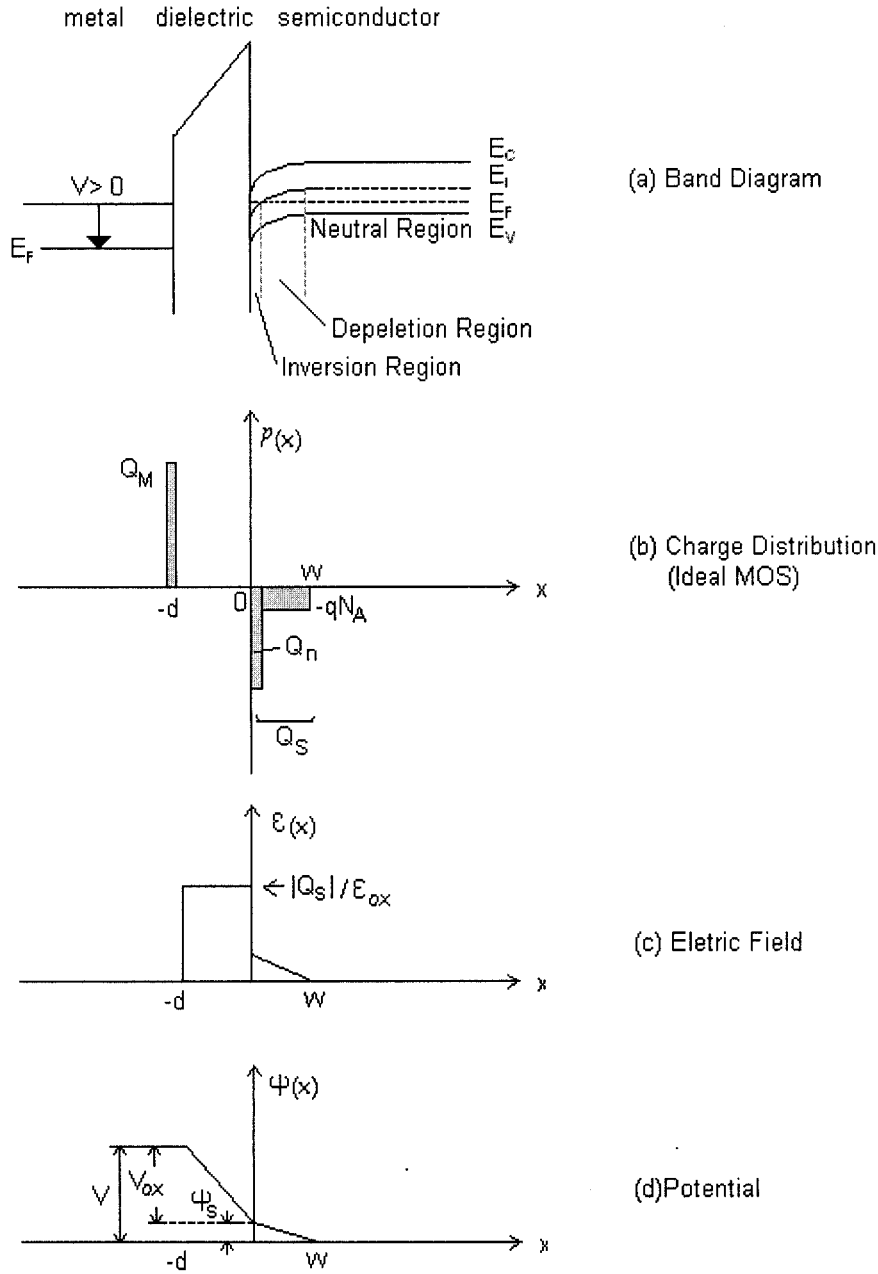


Fig. 2.5 Schematic diagram of (a) band alignment of an ideal MOS structure, (b) charge distribution under inversion condition, (c) electric field distribution and (d) potential distribution[5].

For charge neutrality of the system, it is required that

$$Q_M = Q_N + qN_A W = Q_S, \tag{2.2}$$

where Q_M is charges per unit area on the metal, Q_N is the electrons per unit area in the inversion region, $qN_A W$ is the ionized acceptors per unit area in the space-charge region with space-charge width W, and Q_s is the total charges per unit area in the semiconductor. Figure 2.5(c) and (d) show the electric field and the potential obtained by the first and the second integrations of Poisson's equations, respectively.

In Fig. 2.5(c), it is clear that with the absence of any work-function differences, the applied voltage will partially appear across the insulator and partially across the semiconductor. Thus

$$V = \psi_s + V_{ox}, \tag{2.3}$$

where ψ_s is the semiconductor surface potential and V_{ox} is the potential across the gate oxide which is given by

$$V_{ox} = \frac{Q_s}{C_{ox}}, \tag{2.4}$$

where C_{ox} is the capacitance of the gate oxide. The total capacitance, C, of the system is a series combination of the gate oxide capacitance, C_{ox}, and the depletion capacitance C_D, i.e.

$$C = \frac{C_{ox} C_D}{C_{ox} + C_D} \tag{2.5}$$

For a given dielectric thickness d, the value of C_{ox} becomes constant as illustrated in Fig. 2.6(b), while C_D is varied with V. Hence, total capacitance C is directly depended on V.

This relationship leads to an interesting quantity: threshold voltage, V_T, beyond which ($V>V_T$) strong inversion status begins and current starts to flow through the buried channel right below the interface. The typical *C-V* curve of an ideal MOS capacitor is shown in Fig. 2.6, where C_{min} is the minimum capacitance when surface depletion region occurs.

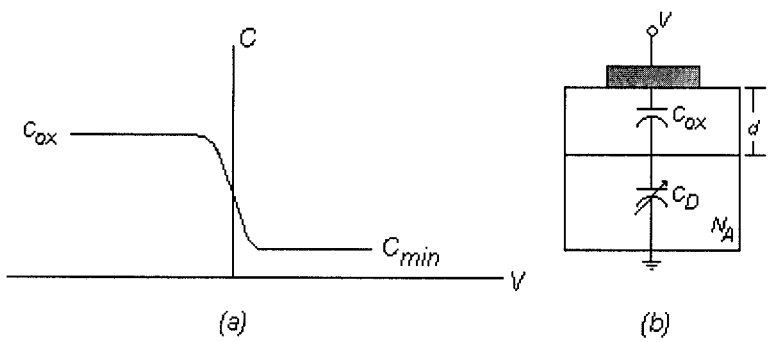


Fig. 2.6 Schematic diagram shows (a) a typical MOS *C-V* curve sketch, and (b) the equivalent circuit of series combination of the gate oxide capacitance, C_{ox}, with constant thickness d, and the semiconductor space charge capacitance C_D[6].

2.2.2 Practical MOS structure

In practical MOS capacitor, the definitions for the ideal MOS previously presented do not hold any more. By contrast, there are many states and charges exist in the structure that affecting the ideal MOS characteristics. The basic classification of these

states and charges are shown in Fig.2.7[7]. They are: (1) interface states which is defined as energy levels within the forbidden band gap at the dielectric/semiconductor interface which can exchange charges with the semiconductor in a short time; (2) surface charges include immobile fixed charges, mobile ions and ionized traps which are located near of or at the semiconductor surface; and (3) space charges include the mobile ions and the ionized traps inside the dielectric.

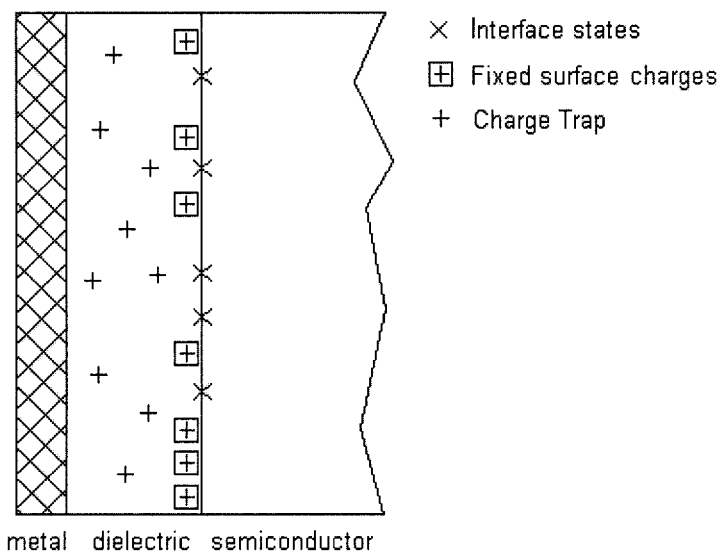


Fig 2.7 Basic classification of states and charges in the non-ideal MOS structure[7].

2.2.2.1 Effect of interface states

The interface states have been theoretically studied by Tamm[8], Shockley[9], and others[10,11] showing that they exist within the forbidden gap due to the interruption of the periodic lattice structures at the surface of a crystal. This interface state is considered as

a donor state if it can be neutral or it can become positive by donating (giving up) an electron. For an acceptor interface state, it can be neutral or it can become negative by accepting an electron. When a voltage is applied, the surface potential will move up or down with the valence and conductance bands while the Fermi level remains fixed. A change of charges in the interface state occurs when it crosses the Fermi level. This change of charges will contribute to the MOS capacitance and alter the ideal MOS curve. With the help of the equivalent circuit (will be discussed in Section 3), conductance G is introduced and it is found that C-V and G-V characteristics are highly correlated to the change of charges in the surface states. Therefore, the interface state density D_{it} can be determined from the combination of a single frequency C-V and G-V measurements using Hill's method[12]. The expression used for calculating the D_{it} is given by:

$$D_{it} = \left(\frac{2G_{\max}}{qA\omega}\right)\left[\left(\frac{G_{\max}}{\omega C_{ox}}\right)^2 + \left(1-\frac{C_m}{C_{ox}}\right)^2\right]^{-1}, \qquad (2.6)$$

where G_{max} is the maximum conductance in the G-V curve with its corresponding capacitance (C_m), C_{ox} is the oxide capacitance, ω is the angular frequency and A is the metal gate area of the capacitor. For SiO_2/Si interface, the typical value of D_{it} is ranged in the order of magnitude of ~10^{10}-10^{11} $cm^{-2}eV^{-1}$.

2.2.2.2 Effects of surface charges and space charges

The surface charges include the fixed charge, mobile ions and ionized traps which are located near or at the gate-oxide/semiconductor interface; while the space charges include the mobile ions and the ionized traps in the dielectric. The fixed charge has the

following properties. It is fixed and cannot be charged or discharged over a wide variation of applied voltage. Its density (Q_{fc}) is not greatly affected by the oxide thickness, while it depends on the oxidation and annealing conditions, and on the semiconductor orientation. The effect of the fixed charge is more or less similar to that of space charges on the MOS capacitance curve, which causes a parallel shift of the *C-V* curve along the voltage axis. The amount of the fixed charges can be calculated by the voltage shift (ΔV) of the *C-V* curve:

$$Q_{fc} = \Delta V \cdot C_{ox} \quad . \tag{2.7}$$

This can be explained with the help of Fig.2.8 (a). When positive fixed surface charges are present, the electric field E in the gate-oxide is higher than the field on the semiconductor surface E_s. Therefore, more charges in the metal electrode are required to create equal but opposite charges. Consequently, a larger voltage is required to compensate them and it causes a shift of the *C-V* curve as illustrated in Fig.2.8 (b).

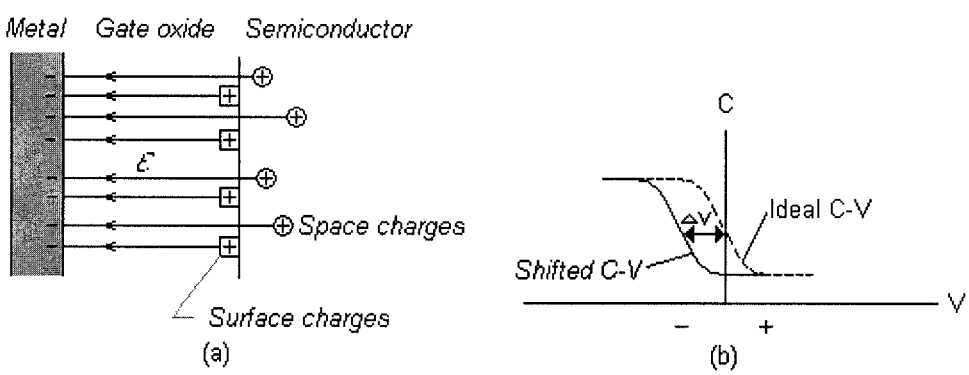


Fig. 2.8 Effect of surface charge on MOS curve[13].

2.2.3 Equivalent oxide thickness (EOT)

Figure 2.9 illustrates the schematic diagram of two parallel capacitors with different dielectrics, SiO_2 and high-k dielectric, to offer the same total capacitance. In order to increase the total capacitance by thinning SiO_2 dielectric (<10 Å), let's consider a parallel plate capacitor:

$$C = \frac{k\varepsilon_o A}{d}, \tag{2.8}$$

where k is the dielectric constant of the material, ε_o is the permittivity of free space, A is the area of the capacitor, and d is the thickness of the dielectric. This expression for C can be rewritten in terms of d_{eq} (i.e. the equivalent oxide thickness of the high-k dielectric when it is assumed to be SiO_2) and k_{ox} (=3.9, the dielectric constant of SiO_2) as illustrated as equation (2.9)

$$C = \frac{k_{ox}\varepsilon_o A}{d_{eq}}. \tag{2.9}$$

As we have the relation of:

$$\frac{k_{ox}}{d_{eq}} = \frac{k_{high-k}}{d_{high-k}}, \tag{2.10}$$

therefore, we have this equation:

$$d_{high-k} = \frac{k_{high-k}}{k_{ox}} d_{eq} = \frac{k_{high-k}}{3.9} d_{eq}, \tag{2.11}$$

where $k_{high\text{-}k}$ and $d_{high\text{-}k}$ are the dielectric constant and thickness of a high-k dielectric, respectively. As a result, this relationship allows us to use a physically thicker high-k dielectric (for example $d_{high\text{-}k}$ =20 Å) to attain an ultrathin SiO_2 (d_{eq}=5 Å) when k~16. Therefore, the equivalent oxide thickness (EOT) for this high-k dielectric is 5 Å.

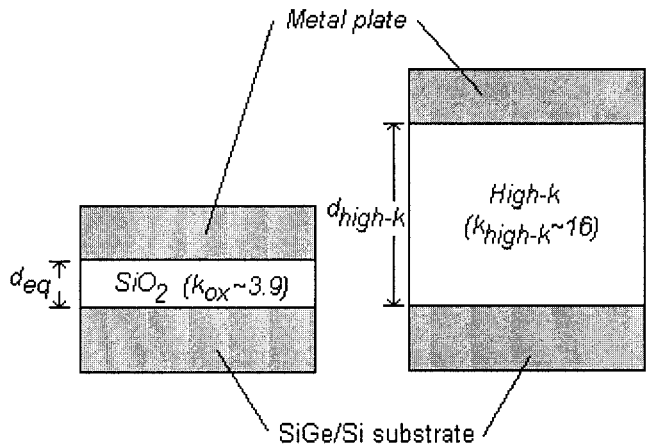


Fig. 2.9 Schematic diagram showing two parallel capacitors with two different dielectrics, SiO_2 and high-*k* dielectric, which offer the same total capacitance.

2.2.4 Material properties consideration

All of the material systems discussed earlier in Chapter 1 must meet a set of criteria to perform as successful gate dielectric. We now consider a summary of the appropriate material properties for the selection of materials for gate dielectric applications.

2.2.4.1 Permittivity and barrier height

Selecting a gate dielectric with a high permittivity than that of SiO_2 is essential to improve the performance associated with the scaling of the device dimensions. For many simple oxides, permittivities have been measured on bulk samples and in some cases even on thin films (below the 10 nm-thickness regime) shown in table 1.1 from Chapter 1. But for the more complex materials, the dielectric constants may not be well known. The required permittivity must be balanced against the barrier height for the tunneling process. For electrons traveling from the Si substrate to the gate, this is the conduction band offset,

$$\Delta E_C \equiv q\left(\chi - \left(\Phi_M - \Phi_B\right)\right), \tag{2.12}$$

where the notations have identical definitions to the energy diagram shown in Fig. 2.3; while for the electron traveling from the gate to the semiconductor substrate, this is Φ_B. This concern is a must because leakage current increases exponentially with decreasing barrier height (and thickness) for electron direct tunneling transport [14] . Therefore, in order to obtain low leakage current, it is desirable to find a gate dielectric that has large ΔE_C value to the semiconductor and gate metal. Various values of ΔE_C for dielectric-Si systems were calculated by Robertson and Chen [14] and are illustrated in Fig. 2.10.

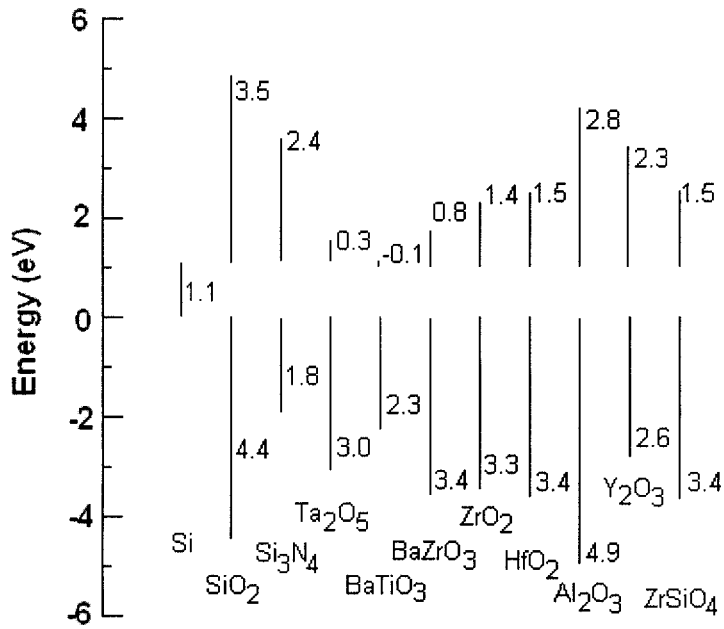


Fig. 2.10 Band offset calculations for a number of potential high-*k* gate dielectric materials[15,16].

These calculations are an important insight into the potential dielectric considerations. If the experimental ΔE_C values for these oxides are less than 1.0 eV, they will likely be excluded for being used as oxides in gate dielectric application, since electron transport would lead to unacceptable high leakage currents. Since many potential gate dielectrics do not have reported ΔE_C values (for example HfAlO), the closest and attainable indicator of the band offset is its band gap (E_g).

Although many researchers originally assumed that selecting a dielectric with k>25

would be necessary to replace SiO_2, the more relevant consideration is whether the desired device performance can be obtained. It is therefore more appropriate to find a dielectric which not only provides a moderate increase in k compared to 3.9 for SiO_2, but also produces a large tunneling barrier and high-quality interface with Si. For the case of Al_2O_3 (k=9) incorporated with HfO_2 (k=25), the overall permittivity of this alloying is inevitably lower than that of the pure HfO_2, but this trade-off can be very favorable, for the improved stability.

2.2.4.2 Thermodynamic stability

For any thin gate dielectric/substrate systems, the interface plays a key role, and in most cases is the dominant factor in determining the overall electrical properties. Most of the systems investigated show unstable and undesirable interfaces attributed by reactions. An important approach toward predicting and understanding the relative stability of a particular three component system for device application can be explained through ternary phase diagrams[17,18] as illustrated in Fig. 2.11. It shows an analysis of the relevant chemical reactions for the Hf-Si-O ternary system governed by Gibbs free energies. The tie lines in the phase diagram for the Hf-Si-O system indicate that the metal oxide HfO_2 and the compound silicate $HfSiO_4$ will both be stable in direct contact with Si up to high temperatures. The gray shaded area denotes a large phase field of $(HfO_2)_x(SiO_2)_{1-x}$ compositions which are also expected to be stable on Si up to high temperatures. Furthermore, even within the shaded area, compositions with high O levels are preferred because this will be more likely to prevent silicide phase formation.

Of course, the illustration can be extended to predict the possibility of our HfAlO/SiGe system by appropriate modifications.

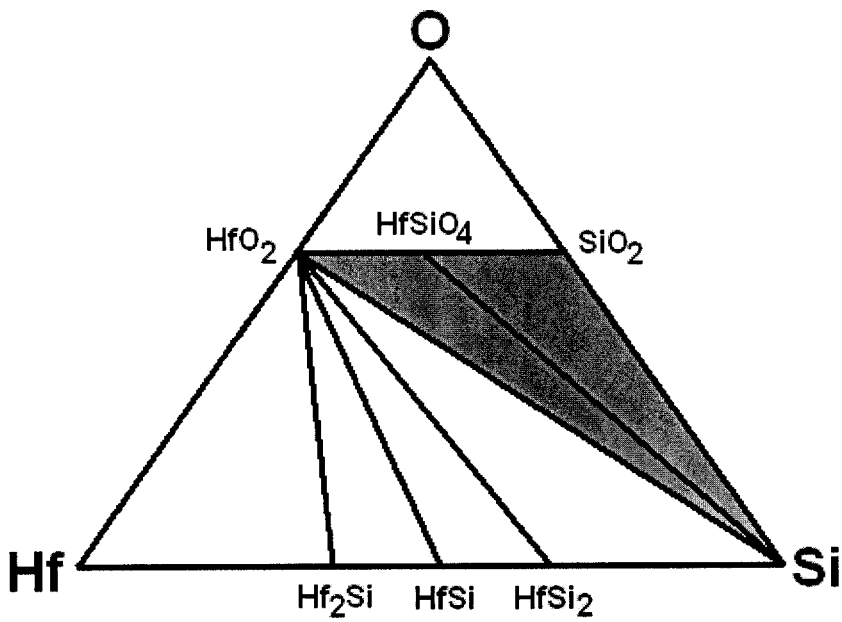


Fig. 2.11 Ternary phase diagram for Hf-Si-O compound[17,18].

Again, the *k* value of $(HfO_2)_x(SiO_2)_{1-x}$ system are substantially lower than that of pure HfO_2, but as mentioned in previous sub-section, this trade-off for interfacial control will be acceptable as long as the resulting leakage current is low enough.

2.2.4.3 Interface quality

A clear goal of any potential high-k dielectric is to attain a sufficiently high-quality interface with the substrate channel, say as close as possible to that of SiO_2/Si. In fact, it is difficult to imagine any material creating a better interface than that of SiO_2/Si, and typical production SiO_2 gate dielectric have a D_{it} of about 10^{10}-10^{11} $cm^{-2}eV^{-1}$. Most of the high-k materials reported in the Chapter 1 show the D_{it} ranged from~10^{11} to 10^{12} $cm^{-2}eV^{-1}$. It is crucial to understand the origin of the interface properties of any high-k gate dielectric, so that an optimal high-k/SiGe interface may be obtained. Any silicide bonding which forms near the channel interface will tend to produce unfavorable bonding conditions leading to poor leakage current and poor electron channel mobility.

In order to maintain high-quality interface and channel mobility, it is expected to have no silicide phases present at or near the channel interface. Furthermore, if a metal-oxide gate dielectric has many different stable oxidation states, an extra attention should be paid because it may generate another defect of oxygen vacancies or electron trap sites at the interface. HfO_2 has been previously reported as having high oxygen diffusivity. This is a serious concern regarding control of the interface. Any annealing treatments which have an excess of oxygen presence will lead to rapid oxygen diffusion through the oxides, resulting in a relatively low-k interface layer and it should be forbidden.

2.2.4.4 Film morphology

As discussed in Chapter 1, polycrystalline structure of gate dielectric is undesirable due to the presence of grain boundaries serving as high-leakage paths. In addition, grain size and orientation changes throughout a polycrystalline film can cause significant variations in k leading to irreproducible properties.

On the other hand, the most desirable phase of materials of the advanced gate dielectrics are the materials which can be remained in a glassy phase (amorphous) throughout the necessary processing treatments. However, nearly all metal oxides of interest shown in Table 1.1 from Chapter 1 (exception of Al_2O_3) tend to form a polycrystalline film during deposition or heat treatments. It is important to note that the phases listed in Table 1.1 are bulk properties and there will certainly be some suppression of crystallization for very thin films as gate dielectrics.

Above are the fundamental theories provided for the basic consideration when selecting alternative gate dielectrics and assessing the dielectric/substrate system.

2.3 Research methodologies

In this Section, structural characterizations including transmission electron microscope (TEM) and x-ray photoelectron spectroscopy (XPS), and electrical characterizations including capacitance-voltage (C-V) and conductance-voltage (G-V) measurements will be presented in sequence.

2.3.1 Structural characterizations

Transmission electron microscope (TEM)

TEM is an important tool for studying the microstructure of materials. For thin gate oxide film thickness and morphology, cross-sectional high-resolution TEM (HRTEM) is always served as the final judgment. HRTEM is also a very powerful tool for investigating the interfacial reaction that may happen at the gate oxide/semiconductor interface. The cross-sectional TEM samples were made by conventional method including mounting the sample with film side face to face, mechanical polishing and ion-milling.

X-ray photoelectron spectroscopy (XPS)

XPS is a surface sensitive analytic tool that able to examine the composition and the chemical state of the surface elements up to 3 nm depth, and it is an ideal tool in characterization of dielectric chemical state and interfacial reaction.

The principle of XPS can be described as follow. When an atom is exposed to electromagnetic radiation, an electron in the atom may have a chance to absorb the energy and leave the atom if the energy is sufficient large enough. This leaving (emitted) electron is called photoelectron and this phenomenon is called photoelectric effect. It can be illustrated by the following equation:

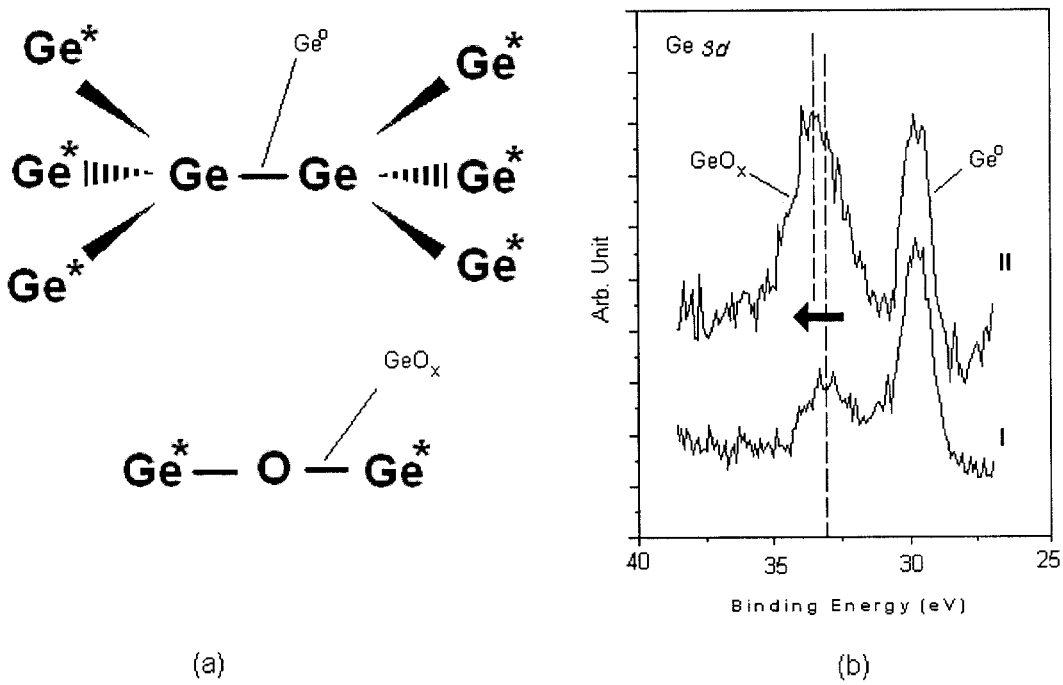
$$h\nu = E_b + E_k + \phi, \tag{2.13}$$

where E_b is the ionization energy or binding energy of the electron in the material, E_k is the kinetic energy carried by the emitted electron, $h\nu$ is the incoming photon energy, and ϕ is the work function of the sample. By detecting the kinetic energy of this photoelectron, the binding energy can be determined. This binding energy is characteristic and it is contributed from the electron configuration between two elements. Thus, XPS offers a finger-print for the bond identification.

Fig. 2.12(a) shows the compositions of elemental form of Ge^{o} and GeO_x ($x \leq 2$), and Fig. 2.12(b) shows the XPS spectra of their corresponding peaks in the Ge *3d* core level of (I) as-grown, and (II) annealed, samples of HfAlO on SiGe/Si substrate. The x-axis and y-axis of the XPS spectra represent the binding energy and the intensity with arbitrary unit, respectively. In Fig. 2.12(b), we can see that the peak of GeO_x has a higher binding energy than that of Ge^{o}. This is because the bond strength of Ge-O is greater than that of Ge-Ge. There are two interesting points need to be highlighted. First, noticeable binding energy shift of the GeO_x peak to the left indicates the bond was strengthened upon annealing. This strengthening effect is attributed by more fully oxidization of GeO_x (the value of x tends to 2), thus a greater bond strength or higher binding energy means a more stable state. The second interesting point is an observable peak height increment of GeO_x peak of the sample after annealing indicates the content of the corresponding peak is increased.

In addition, there is another method which offers a fast estimation to the strength of the bond by comparing their values of electro-negativities (shown in Table 2.1). This

electro-negativity value gives a rough guide for the strength of an atom which is willing to be bonded with. For example, O has higher electro-negativity than that of Al, if they bond with another O atom, the binding energy of the composition of O-O should be higher than that of Al-O.



(a) (b)

Fig. 2.12 Schematic diagram shows (a) compositions of elemental form of Ge^{o} and GeO_x ($x<2$) where terminating atoms, Ge^{*}, represent the next shell of Ge atom or O atom, and (b) the corresponding peaks in the Ge *3d* core level obtained from the sample of (I) as-grown, and (II) annealed, of HfAlO on SiGe by XPS.

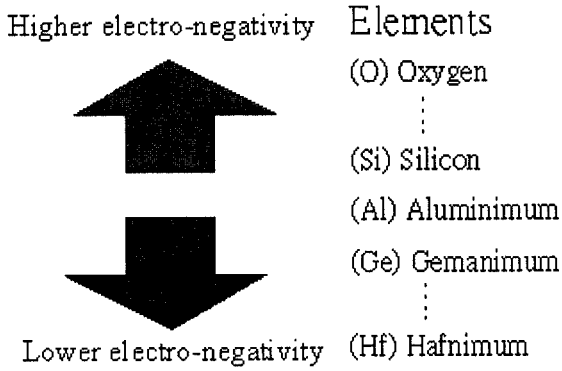


Table 2.1 Reference of electro-negativity on various elements.

2.3.2 Electrical characterizations

Both capacitance-voltage (*C-V*) and conductance-voltage (*G-V*) measurements were carried out to characterize the MOS property, due to the fact that they are sensitive to the dielectric film and interface properties of the MOS capacitor. Figure 2.13 shows the schematic diagram of a MOS capacitor structure consisted of platinum (Pt) as the metal gate, HfAlO as the high-*k* gate dielectric and SiGe/Si as the capacitor substrate.

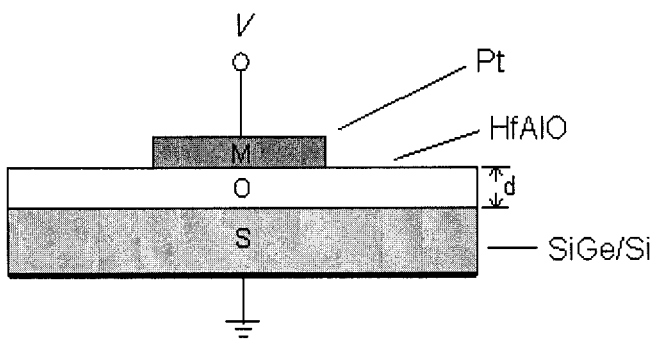


Fig. 2.13 Typical MOS structure.

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Chapter 3

Characteristics of HfAlO gate dielectric on compressively strained SiGe

3.1 Introduction

Compared to the HfAlO/Si system, the growth and structure of HfAlO on compressively strained SiGe is more complicated. First, in order to maintain the strain in SiGe, the growth temperature and the post-annealing temperature must be lower than the strain relaxation temperature. Secondly, from the interfacial structure viewpoint, due to the volatility of Ge, the interfacial reaction and Ge diffusion may be a serious problem. High quality HfAlO film on strained SiGe is essential for gate dielectric application and the quality of the HfAlO film is directly affected by some factors including the ratio of Hf/Al, oxygen partial pressure and substrate temperature during film growth, and thermal annealing temperature. These factors determine the film structure, interfacial structure and reaction, and therefore determine the electrical properties of the MOS capacitors. In this Chapter, research results covering the effects of Al content in HfAlO films grown on compressively strained SiGe and the effects of oxygen partial pressure on both structural and electrical characteristics are presented.

3.2 Experimental details

The HfAlO films with different ratios of Hf:Al (1:0, 1:1 and 1:6) were grown by PLD on Si substrates with a layer of 15-nm compressively strained p-type $Si_{1-x}Ge_x$ (x=17 %) on top. The SiGe layer is doped with boron with concentration of $2\times10^{17}/cm^3$ forming a p-type SiGe. To make comparison with control samples, corresponding films were also grown on Si substrate with identical fabrication process and condition. The SiGe/Si substrates were treated by conventional HF-last process to remove the native oxide and leaving hydrogen terminal surface. A KrF excimer laser (λ=248 nm) with laser fluence of 6 J/cm^2 was used for film deposition. In order to prevent SiO_2 formation and relaxation of strain within SiGe layer, the dielectric films were grown in a base pressure of 2×10^{-3} Pa at a relatively low substrate temperature of 500 °C without introducing oxygen gas. The post thermal annealing was carried out in N_2 ambient at 650 °C for 45 min. The film morphology and structural properties were studied by means of high-resolution transmission electron microscopy (HRTEM) using a JEOL 2010 electron microscope and x-ray photoelectron spectroscopy (XPS). For electrical property characterization, the MOS capacitor structures were fabricated by depositing Pt dot electrodes on both as-grown and annealed samples. High-frequency (1MHz) capacitance-voltage (C-V) measurement using a HP4194A impedance analyzer was carried out to evaluate the MOS capacitor electrical properties.

3.3 Results

3.3.1 Effects of Al content in HfAlO film on its structural and electrical characteristics

Figure 3.1 shows HRTEM images of the as-grown HfO_2, HfAlO (1:1) and HfAlO (1:6) on Si and SiGe deposited in high vacuum (without introducing any oxygen gas) at a substrate temperature of 500 °C. It is apparent that all samples are in an amorphous structure and no crystal lattice image can be observed. From the TEM images, the film thicknesses for the samples of HfO_2, HfAlO (1:1) and HfAlO (1:6) can be determined to be 5-nm, 10-nm and 27-nm, respectively. It is obvious that there is Al contents dependence for the HfAlO film thickness, and the thickness of HfAlO (1:6) film is 5 times thicker than that of HfO_2 film. This is due to the reason that the growth rate of films is highly depended on how easy the target material can be evaporated by each laser pulse. This finding is consistent with the fact that the growth rate of Al_2O_3 films is much faster than that of HfO_2 in our experiments.

In Figs. 3.1(a), (b) and (d), thin interfacial layers (IL) were observed indicating that SiO_x and/or GeO_x rich layers were formed during film deposition. By contrast, the IL in Fig. 3.1(c) and (e) are negligible, suggesting that HfAlO (1:6) has ability of suppressing the formation of IL. It should be noted that for the as-grown sample, if there is IL formation, it should be contributed by oxidization or chemical reaction during deposition process rather than oxygen diffusion through the gate dielectric layer. The fact that the TEM image of HfO_2/Si is missing in Fig. 3.1 is due to the failure of TEM sample preparation. But in fact, HfO_2/Si system, especially the interfacial characteristics

has been well studied in our group before[1]. To understand the chemical reaction and bonding structures at the interface, XPS analysis was carried out.

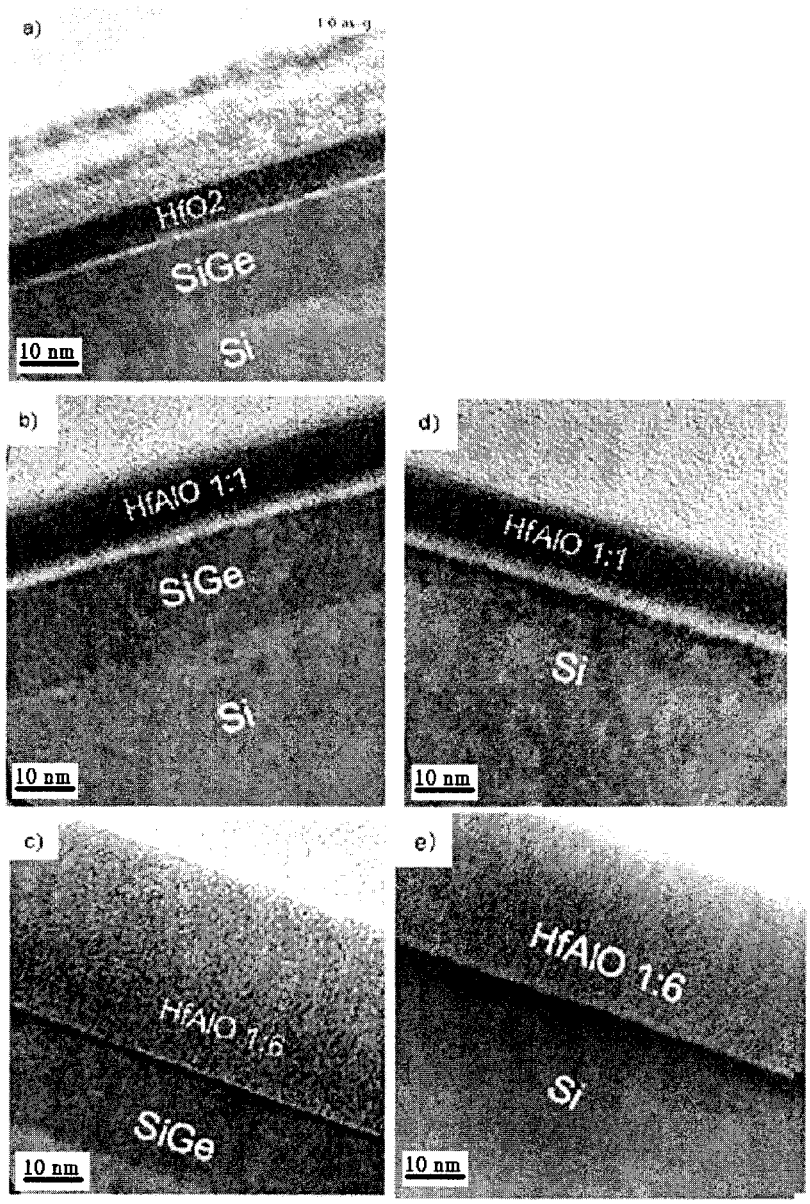

Fig. 3.1 HRTEM images for (a) Pure HfO_2 on SiGe, (b) HfAlO (1:1) on SiGe, (c) HfAlO (1:6) on SiGe, (d) HfAlO (1:1) on Si, and (e) HfAlO (1:6) on Si at high vacuum before thermal annealing.

XPS spectra for Hf *4f* core levels of the as-grown samples of (a) pure HfO_2, (b) HfAlO (1:1) and (c) HfAlO (1:6) deposited on SiGe at high vacuum are shown in Fig. 3.2. Generally, it is observed that the positions of the peaks are experiencing a higher binding energy shift with the increase of Al content in HfAlO films. A similar result was reported by Li *et al.*[2,3]. They have found that in the $(HfO_2)_x(Al_2O_3)_{1-x}$ /Si system, where x is the HfO_2 mole fraction value ranged from one to zero, there was an observable core level peak positions shift of Hf *4f*, Al *2p*, and O *1s* toward higher binding energy with the increase of Al_2O_3 concentration. The higher binding energy shift suggests the existence of higher bonding strength components in HfAlO (1:6), such as Hf-Al-O, Hf-Si-O and Hf-Ge-O. The elements of Al, Si and Ge possess higher electro-negativity than that of Hf. However, to determine the bonding types precisely, more XPS spectra including Si *2s*, O *1s*, Ge *3d* and Al *2p* should be given for further analysis.

In Fig. 3.2(a), the peaks at the lower binding energy side (indicated by the solid arrows) suggest the existence of Hf-Si or Hf-Ge bond at the HfO_2/SiGe interface, even though there is no Hf-silicide phase formed at the interface in the TEM images. Similarly, a noticeable but small shoulder (indicated by hollow arrow) in Fig. 3.2(b) can also be interpreted as the formation of Hf-Si bonding near the interface. However, there is no trace of Hf-Si or Hf-Ge bonding at the HfAlO (1:6)/SiGe interface. The significant difference of XPS Hf *4f* peaks in the figure is a clearly evidence that the Al content in HfAlO is very important to prevent silicide formation.

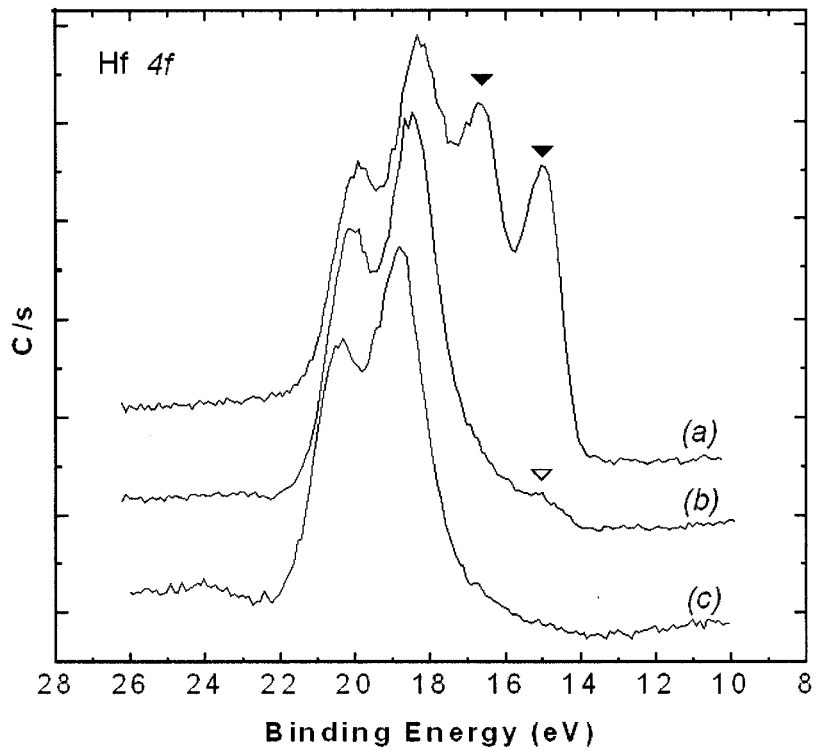

Fig. 3.2 XPS spectra for Hf *4f* core level of as-grown samples of (a) Pure HfO_2, (b) HfAlO (1:1) and (c) HfAlO (1:6) on SiGe.

Figure 3.3 shows the *C-V* characteristics of the annealed samples of HfO_2 and HfAlO with different ratios of Hf:Al grown on Si and SiGe substrates. As can be seen from the plots, there are two significant distinctions on the *C-V* characteristics between the films grown on Si and SiGe. First, the films grown on Si substrate show a general negative flat band voltage (V_{FB}), while the films grown on SiGe/Si substrate show a generally positive V_{FB}. As the metal gate is identical, this particular characteristic should be due to the intrinsic electronic properties difference (i.e. different work function (Φ_S) of Si (~4 *V*) and SiGe (~4-4.75 *V*) substrates[4]). As discussed in Chapter 2, the value of Φ_S is dependent on the values of its semiconductor electron affinity (χ), its semiconductor band gap (E_g) and its potential difference(ψ_B) between its Fermi level

(E_F) and its intrinsic Fermi level (E_I) as illustrating in Fig. 2.3.

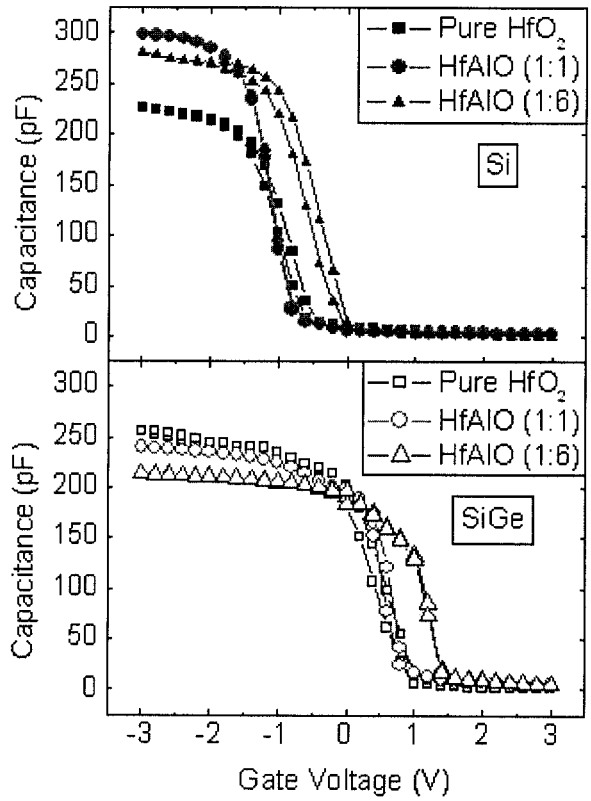

Fig. 3.3 *C-V* measurements at 1MHz of the samples of pure HfO_2, HfAlO (1:1) and HfAlO (1:6) on Si (upper) and SiGe/Si (bottom) substrates. All samples have been thermal annealed in N_2 at 650 °C for 45 min.

Secondly, one can clearly see that for the HfAlO (1:6) films, both films grown on Si and SiGe exhibit a larger shift of *C-V* curves to the positive side. This finding has been suggested to the attribution of the more negative fixed charge introduced by the incorporation of more Al ions.

3.3.2 Effects of oxygen partial pressure on structural and electrical characteristics of HfAlO films grown on compressively strained SiGe

To study the effects of oxygen partial pressure, a series of oxygen partial pressures were used as the only various parameter during film deposition. The ratio of Hf:Al in the HfAlO films in this comparison experiment is selected as 1:1. The experimental procedure is more or less the same with the above Section. The substrates were treated by conventional HF-last process first. And then the working chamber was pumped to high vacuum of 5×10^{-5} Pa. In order to suppress the substrate oxidization in the oxygen gas ambient before film deposition, no oxygen gas was introduced until the substrate reached a steady elevated substrate temperature (550 °C). The series of oxygen partial pressures during film growth were set to 5 Pa, 5×10^{-1} Pa and 5×10^{-5} Pa by introducing appropriate amount of O_2 gas flow, while 5×10^{-5} Pa is the base vacuum. The post thermal annealing was performed in N_2 ambient at 650 °C for 45 min after the film growth. The samples were then examined by HRTEM for the structural characterization. For electrical characterization, the MOS capacitor structures were fabricated by depositing Pt dot electrodes with an area of 3.14×10^{-4} cm^2 on both the as-grown and annealed samples for *C-V* measurement.

Figures 3.4(a) and (c) show the HRTEM images of the as-grown samples of HfAlO films grown on SiGe with oxygen partial pressure of 5 Pa, and base vacuum of 5×10^{-5} Pa, respectively, and the corresponding annealed samples were shown in Figs 3.4(b) and (d). It clearly shows that in all samples, the HfAlO films are in an amorphous structure.

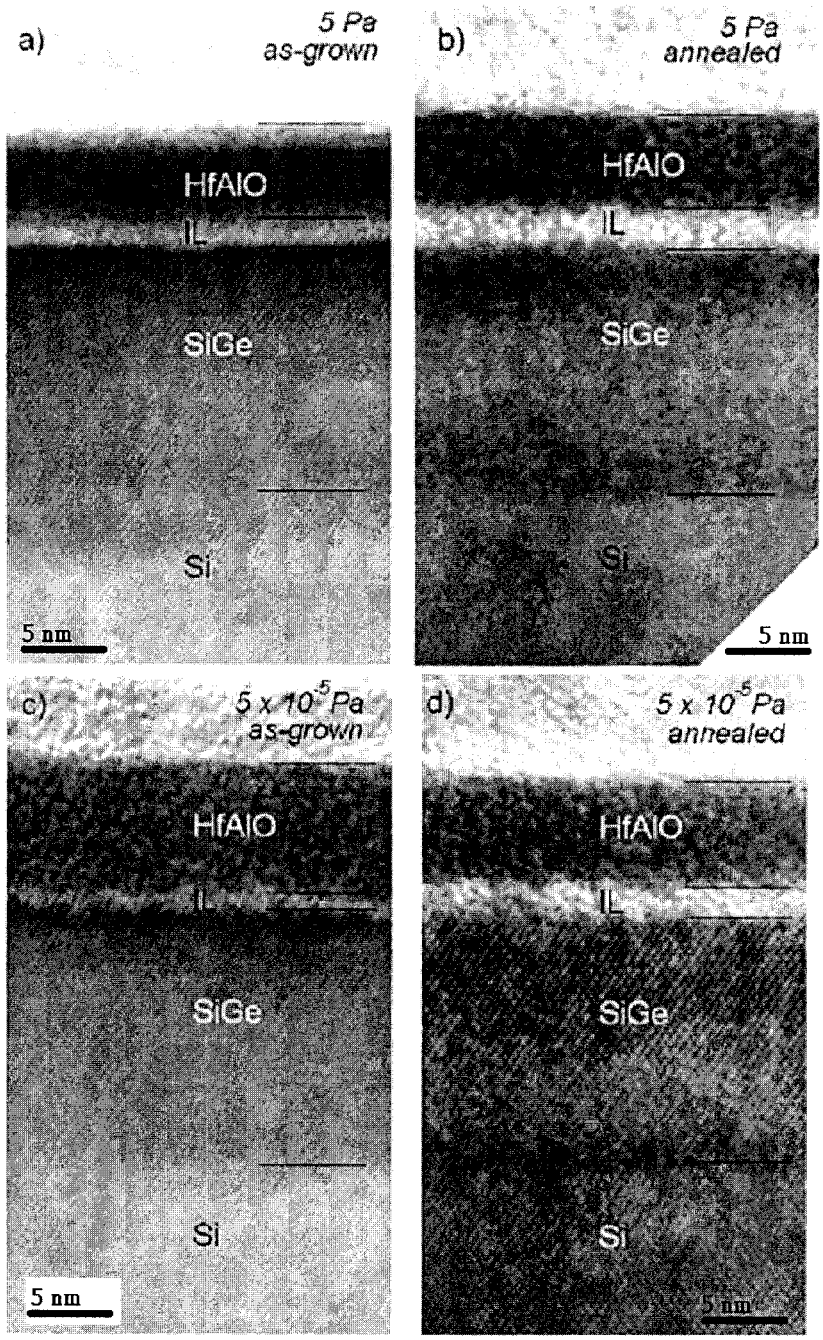

Figure 3.4 Cross-sectional TEM images showing the interfacial structures of HfAlO (Hf:Al=1:1) films grown on SiGe/Si of (a) and (c) as-grown samples with oxygen partial pressure of 5 Pa and $5x10^{-5}$ Pa, respectively, and (b) and (d) are their annealed samples.

It should be pointed out that there is no dislocation or any misalignment can be seen from the HRTEM images at the SiGe/Si interface for the as-grown and annealed samples. This confirms that the epitaxial SiGe layer remains compressively strained and no strain relaxation occurred after annealing at 650 °C.

Another important feature that can be revealed from Fig. 3.4 is the oxygen partial pressure dependence of the thickness of interfacial layer, which appears white in contrast at the interface. A general trend that can be seen from Fig. 3.4 is that higher oxygen pressure during film growth corresponds to a relatively thicker interfacial layer, and the annealed samples result in increased interfacial layer. The interfacial reaction at the high-*k*/Si interface is a common phenomenon for most of the high-*k* materials. However, it will be more complicated, since besides the possible SiO_x or Hf-Si-O formation at the interface, we also need to consider the formation of GeO_x and Hf-Ge-O or their combinations. Therefore, a more detailed study of the interfacial reaction is necessary and will be presented in the next Chapter. However, the formation of Hf-silicide at the interface can be ruled out, especially in the annealed sample, since most silicide cannot sustain oxidation under high temperature annealing.

For the electrical measurement, it is well known that series resistance is one of the important parameters of small signal energy loss in a MOS capacitor, and it causes a serious error in the determination of interfacial properties from electrical measurements[5]. Therefore, the magnitude of this resistance should be carefully determined before applying series resistance corrections. Figure 3.5 shows the effect of a relatively high series resistance in the capacitance and conductance measurements of

the HfAlO films at a high frequency (1MHz).

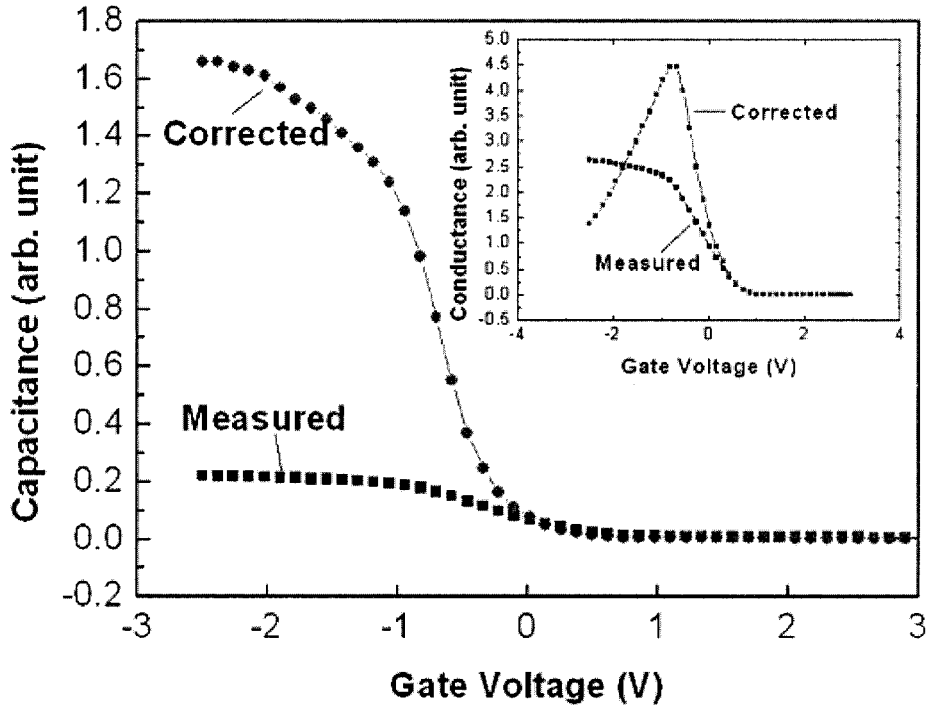

Fig. 3.5 High frequency *C-V* and G-*V* characteristics (inset) of the MOS structure. *C-V* and G-*V* characteristics were corrected with series resistance consideration.

The absence of a *G* peak in the *G-V* characteristic curve before the correction indicates that the sample suffers from relatively high series resistance [6]. Such a high series resistance produces the dominant loss, and thus completely masks the interface trap loss. By determining the value of series resistance and applying a correction to the measured capacitance and conductance, errors can be minimized. The corrected capacitance, C_c, and corrected conductance, G_c, at a frequency of interest are given by[6]

$$C_c = \frac{(G_m^2 + \omega^2 C_m^2)C_m}{a^2 + \omega^2 C_m^2}, \tag{3.1}$$

and

$$G_c = \frac{(G_m^2 + \omega^2 C_m^2)a}{a^2 + \omega^2 C_m^2}, \tag{3.2}$$

respectively. In these equations,

$$a = G_m - (G_m^2 + \omega^2 C_m^2)R_s, \tag{3.3}$$

where C_m and G_m are the measured capacitance and conductance, respectively.

Figure 3.6 shows high-frequency *C-V* characteristics of as-grown and annealed Pt/HfAlO/SiGe MOS capacitors for the films deposited at various oxygen partial pressures. A general trend that can be seen from Fig. 3.6(a) is that, as the oxygen partial pressure decreases during the film growth, the *C-V* curves are stretched out and exhibit a shift to the left. The shift of the *C-V* curves in this direction is an indication of positive fixed charges present in the dielectric layer. The stretch-out of the *C-V* curve is due to the density increase of interfacial traps which can be interpreted as due to the existence of dangling bonds of Si or Ge acting as charge traps. These dangling bonds may appear as a result of the lack of oxygen atoms at the interface.

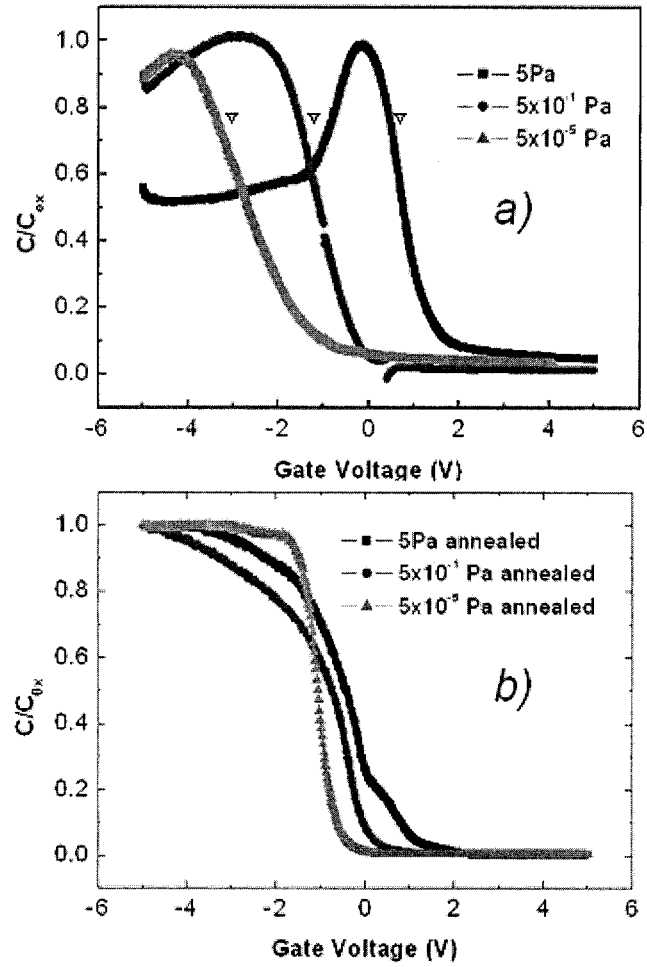

Fig 3.6 *C-V* plots show the *C-V* characteristics of as-grown (a), and annealed (b), HfAlO (1:1) samples grown with various oxygen partial pressures.

After annealing, it is apparent that the fixed charge and interfacial trap densities have been reduced significantly, as seen in Fig. 3.6(b). It is interesting to note that, the annealed sample grown at 5×10^{-5} Pa corresponds to a very good *C-V* curve with the smallest stretch-out, even though it is the worst before annealing (Fig. 3.6(a)). This may be understood by considering that the HfAlO film grown at a good vacuum contains more oxygen vacancies and is more transparent to oxygen, thus after annealing, more oxygen vacancies are filled inside the film and at the interface, and

therefore, the density of fixed charges inside the film and of interface traps at the interface is reduced. It should be noticed that, since the Pt dot electrodes were deposited at the same condition under room temperature for all samples deposited at different oxygen partial pressures, including the as-grown and annealed samples, the contribution of work function difference of electrodes to the C-V curve shift between different samples can be ruled out.

The effective dielectric constants of the annealed HfAlO films were calculated using the accumulation capacitance (C_{acc}). A gradual increment of its value from ~10 to ~16 with the increment of the oxygen partial pressure from 5×10^{-5} Pa to 5 Pa is observed. This change is attributed to the change in the film stoichiometry and thickness. From the high-frequency *C-V* and *G-V* measurements, the values of interface state density (D_{it}) of the as-grown and annealed samples were calculated by using Hill's method [7].

The annealed sample grown with oxygen partial pressure of 5×10^{-1} Pa exhibits the lowest value of D_{it} of ~2.1×10^{10} $cm^{-2}eV^{-1}$ and the films grown with 5 Pa and 5×10^{-5} Pa have D_{it} ~2.5×10^{10} and ~1.0×10^{11} $cm^{-2}eV^{-1}$, respectively. The lower values of D_{it} gave by the annealed samples than that of as-grown samples suggests that the post deposition annealing causes a general improvement of the interface quality. Although, the lowest value of D_{it} of ~2.1×10^{10} $cm^{-2}eV^{-1}$ obtained by Hill's method calculation may not be absolutely precise, the lowest value of D_{it} obtained for the annealed sample grown with the oxygen partial pressure of 5×10^{-1} Pa to 5 Pa suggests a better interface quality. It seems that the value of D_{it} is not very sensitive to the pressure. It should be

noticed that, since the main purpose of the D_{it} measurement was to study the relative effect of film growth and processing conditions, we only calculated the interface state densities for different samples based on single-frequency 1 MHz C-V measurement, which gave us the density of states at a single energy in the forbidden gap. However, some of the interface states may be too slow to follow this high frequency to be visible in *C-V* curves, and therefore the interface state densities we obtained may be underestimated.

Finally, all *C-V* characteristics with a dual voltage sweep from inversion to accumulation and back to inversion by the bias voltages of -5 V to +5 V were measured. Only negligible hysteresis loops can be found in all *C-V* measurements, suggesting that the charge trap densities inside the films are low. This result implies that the Ge diffusion inside the HfAlO films is relatively low.

3.4 Discussion on electrical characterizations

The above results and Section 3.2 had clearly shown the superior and capability of using *C-V* characterization on the extraction of the hidden and complicated interfacial characteristics over a few Å-thick interfacial layer which was known as the most crucial factor to the overall performance of the whole MOSFET including its carrier mobility. In the following sub-section, another two common effects, including the existence of hump in the *C-V* curve and the *C-V* stretch-out, will be presented. The methodology of *G-V* measurement will also be introduced in this section.

Capacitance-voltage (*C-V*) measurements

Figure 3.7 shows a typical *C-V* characteristic curve which obtained from one of our annealed samples of HfAlO films grown on SiGe/Si substrate. A hump, in the *C-V* curve near *V*~ 1.8 V measured at 1MHz (noticed by a hollow arrow), is well known as the presence of a large number of interface trap (~10^{12} $cm^{-2}eV^{-}$) located in the lower part of the SiGe band gap[8-10].

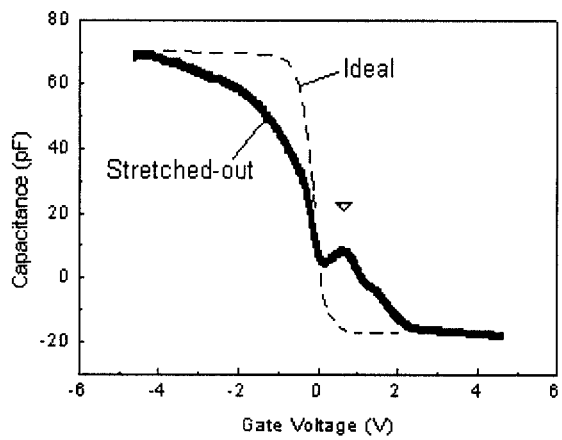

Fig. 3.7 *C-V* characteristic curve affected by interface traps located at the bottom part of the SiGe bandgap.

Furthermore, it is well known that *C-V* characteristics of non-ideal MOS capacitor can be stretched-out along the voltage axis as illustrated in Fig. 3.7 (an ideal *C-V* curve represented by a dotted-line is provided for comparison purpose). This voltage stretch-out is classically attributed to an increase in the interface trap level density which can be interpreted as the existence of dangling bonds at the interface due to the lack of oxygen atoms. M. Houssa *at el.*[11] also reported the same observation of

stretched-out of the *C-V* curves due to the increase of interface states upon annealing. In addition, they have also shown that the defects can be passivated after H_2 gas ambient annealing.

Conductance-voltage (*G-V*) measurements

The basic equivalent circuit incorporating with the interface states effect is shown in Fig. 3.8 (a).

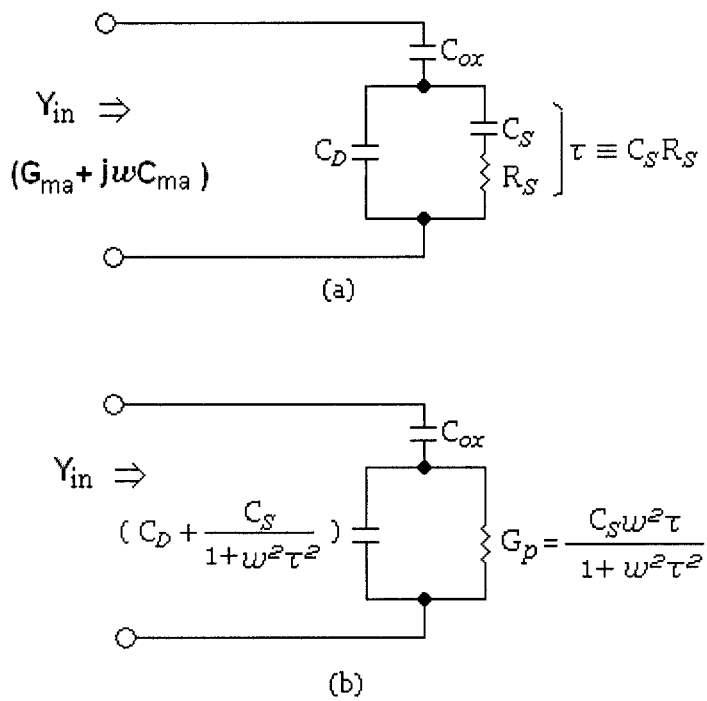

Fig .3.8 Equivalent circuits include interface states effect where C_s and R_s are associated with surface state densities[12].

In the figure, C_{ox} and C_D are identical to those shown in Fig. 2.6 (b). C_S and R_S are the capacitance and resistance associated with the interface states, and they are functioned by the semiconductor surface potential. The product $C_S R_S$ is defined as the surface state lifetime which determines the frequency behavior of the interface states. The parallel branch of the equivalent circuit in Fig. 3.8 (a) can be converted into a frequency-dependent capacitance C_P in parallel with a frequency-dependent conductance G_P as shown in Fig 3.8 (b) with

$$C_P = C_D + \frac{C_S}{1+\omega^2\tau^2} \tag{3.4}$$

and

$$\frac{G_P}{\omega} = \frac{C_S \omega\tau}{1+\omega^2\tau^2}, \tag{3.5}$$

where $\tau \equiv C_S R_S$. The input admittance, Y_{in}, is given by

$$Y_{in} = G_{in} + j\omega C_{in}, \tag{3.6}$$

where

$$G_{in} = \frac{\omega^2 C_{ox}{}^2 C_S \tau}{(C_D + C_{ox} + C_S)^2 + \omega^2\tau^2 (C_D + C_{ox})^2} \tag{3.7a}$$

and

$$C_{in} = \frac{C_{ox}}{(C_D + C_{ox} + C_S)}\left[C_D + C_S \frac{(C_D + C_{ox} + C_S)^2 + \omega^2\tau^2 (C_D + C_{ox})C_D}{(C_D + C_{ox} + C_S)^2 + \omega^2\tau^2 (C_D + C_{ox})^2}\right]. \tag{3.7b}$$

To evaluate the interface-state density, one can either use the capacitance measurement or the conductance measurement since the equations of (3.7a) or (3.7b) contain similar information about the interface states. However, it will be shown that

the conductance technique can give the most accurate results especially for MOS capacitors with relatively low interface-state density (~10^{10} $cm^{-2}eV^{-1}$).

A detailed and comprehensive discussion on the conductance method is given by Niclollian and Goetzberger[13]. In the capacitance measurement, the difficulty arises from the fact that the interface-state capacitance must be extracted from the measured capacitance which consists of oxide capacitance, depletion capacitance, and interface-state capacitance. In contrast, this difficulty does not apply to the measured conductance because it is directly related to the interface states.

The principle of the MOS conductance technique is easily illustrated by the simplified equivalent circuit shown in Fig. 3.8(b). We can see that, in the equation (3.5), $\frac{G_P}{\omega} = \frac{C_S \omega\tau}{1+\omega^2\tau^2}$ does not contain C_D but only depends on the interface-state branch of the equivalent circuit. At a given bias, G_P/ω can be measured as a function of frequency. A plot of G_P/ω versus $\omega\tau$ will go through a maximum when $\omega\tau = 1$. This gives $\tau(\equiv C_S R_S)$ directly. The value of G_P/ω at the maximum is $C_S/2$. Thus it gives C_S and $\tau(\equiv C_S R_S)$ directly from the measured conductance. Once C_S is known, the interface state density is obtained by using the relation $N = C_S/qA$, where N is the number of interface state density, A is the metal plate area, and q is the electronic charge. A typical value of N in a Si-SiO_2 system is ranged from 10^{10}-10^{11} $cm^{-2}eV^{-1}$.

Although, the conductance spectra technique given by Nicollian and Goetzberger (1967) requires lengthy analysis and is time consuming, it is worth to be introduced as an understanding for the basic concept and the superior of using conductance measurement over capacitance measurement. After the technique was reported, there were many other approximation techniques raised up. However, nearly all of them had shown their incapability on interpretation when the interface-state density is less than 10^{11} $cm^{-2}eV^{-1}$. In 1979, W. A. Hill and C.C. Coleman reported a new and fast single frequency technique[14] (which is using in this thesis) as a more accurate alternative compared to other approximation methods. This technique is one of the most popular approximation techniques. The data required for this technique are only a single high frequency *C-V* measurement and a corresponding *G-V* measurement and the approximated calculation formula is given as

$$D_{it} = \left(\frac{2G_{\max}}{qA\omega}\right)\left[\left(\frac{G_{\max}}{\omega C_{ox}}\right)^2 + \left(1-\frac{C_m}{C_{ox}}\right)^2\right]^{-1},$$

which is identical to equation 2.6.

3.5 Summary

In summary, for the first part of this Chapter, the effects of Al contents in the HfAlO films on its structural and electrical characteristics were investigated. Changing Al content in HfAlO significantly changes the structural and electrical properties. For the second part of this Chapter, the dependence of oxygen partial pressures on structural and electrical characteristics of HfAlO (Hf:Al=1:1) high-*k* gate dielectric films were

investigated. The interfacial layer thickness and *C-V* characteristics of the HfAlO films were found to be depend on the growth oxygen pressure. The investigation suggests that an optimized oxygen partial pressure is crucial to obtain a HfAlO film with low density of defects in the dielectric and at the dielectric/SiGe interface.

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Chapter 4

Comparison of interfacial and electrical characteristics of HfO_2 and HfAlO high-*k* dielectrics on compressively strained SiGe

4.1 Introduction

The previous chapter has clearly shown the dependence of structural and electrical properties of HfAlO gate dielectric, when deposited on compressively strained SiGe, on both the ratio of Hf/Al and the oxygen partial pressure. It reveals that the ratio of Hf/Al affects the flat-band voltage of the MOS capacitors; while low oxygen partial pressure results in extremely thin interfacial layer, and high oxygen pressure produces thicker interfacial layer. The post-growth thermal annealing is also found to be critical to the interfacial reaction.

The electrical property study revealed that alumina addition in the HfO_2 plays a key role in affecting the C-V characteristics. The results suggest that the properties of the HfAlO/SiGe and HfO_2/SiGe interfaces are significantly different, especially in interface chemical structure. In this Chapter, interfacial reactions and electrical properties of HfAlO and pure HfO_2 high-*k* gate dielectric films on compressively strained SiGe are investigated. In particular, the suppression effect on GeO_x formation at the interfacial layer by adding alumina in HfO_2 will be illustrated. In addition, the influence of Si-cap will also be presented.

4.2 Experimental details

To study the merit of HfAlO (Hf:Al=1:1) over pure HfO_2, both of them were deposited on Si substrates with a layer of 15 nm compressively strained p-type $Si_{1-x}Ge_x$ (x=17%) on top. The experimental procedure is more or less the same to the previous Chapter. Substrates were treated by conventional HF-last process by the same way to remove the native oxide from the surface. The dielectric films were then grown by pulsed-laser deposition (PLD) with a base pressure of $\sim 2\times 10^{-4}$ Pa and an oxygen partial pressure of 2 Pa at 550 °C. The post thermal annealing was carried out in N_2 ambient at 600 °C for 45 min. In order to investigate the interfacial chemical structure, a set of samples with very thin (about 1.5 nm) HfO_2 and HfAlO films were deposited for the x-ray photoelectron spectroscopy (XPS) analysis. Such thickness allows an XPS investigation of the film and the interface simultaneously, and thus information on interfacial reactions can be obtained. The interfacial microstructure was observed by transmission electron microscopy (TEM) using a JEOL 2010 electron microscope. For electrical property characterization, thicker films with thickness of about 5 nm were deposited. The MOS capacitor structures on strained SiGe were fabricated by depositing Pt dot electrodes for both as-grown and annealed samples. Both high-frequency (1MHz) capacitance-voltage (*C-V*) measurement using a HP4194A impedance analyzer, and current-voltage (*J-V*) measurement were carried out.

4.3 Results

4.3.1 Suppression effects of HfAlO on GeO_x formation

Figure 4.1 shows the XPS spectra of the Hf *4f*, Ge *3d* and Si *2p* binding energies of the as-grown and annealed HfO_2 and HfAlO films on SiGe. The peak positions were calibrated using C *1s* lines as the reference. For the as-grown samples in Fig. 4.1(a), the two distinct peaks corresponding to the Hf $4f_{7/2}$ and $4f_{5/2}$ of Hf-O bond are distinguishable; while they become difficult to be resolved for the annealed samples, especially the HfO_2 film. This peaks broadening is due to the formation of Hf-silicate or germanate at the interface during the thermal annealing. Convolution of Hf-silicate and/or germanate peaks with Hf *4f* peaks results in the broadening of the Hf-O peaks. In addition, very clear difference in the Hf *4f* peaks broadening can be observed for the annealed HfO_2 and HfAlO films. We believe that this relatively less broadening effect for the annealed HfAlO film compared to that of the annealed HfO_2 film can be attributed to the fact that the presence of Al in the film reduces oxygen diffusion in the film and thus reduces the formation of Hf-silicate and germanate at the interface.

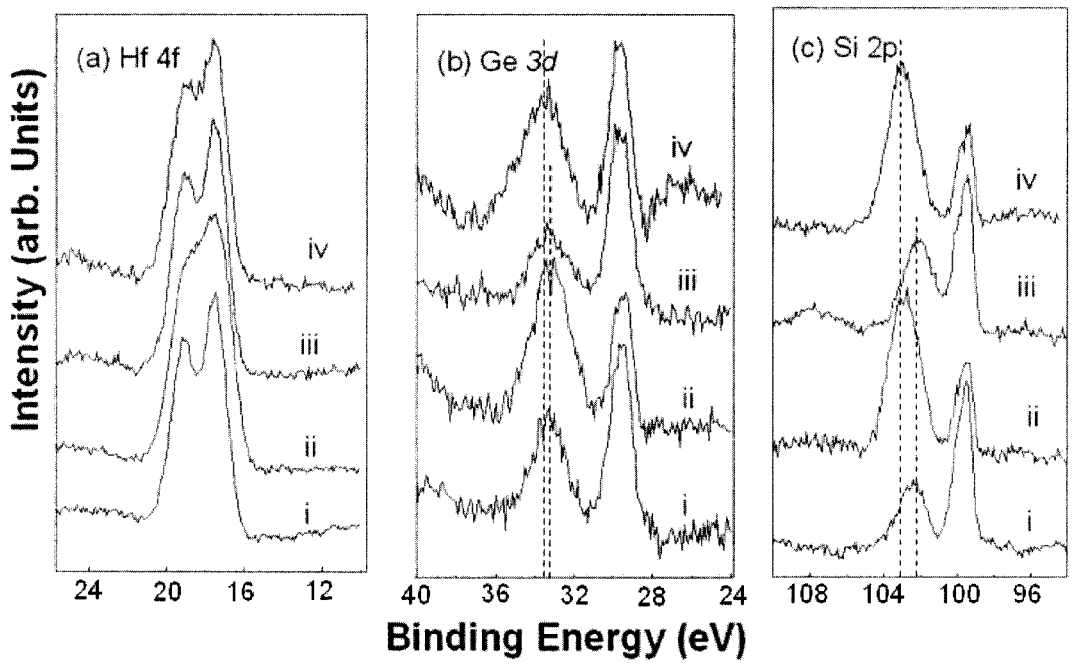

Fig. 4.1 XPS spectra of (a) Hf *4f*, (b) Ge *3d* and (c) Si *2p* binding energies for the films of (i) as-grown HfO_2, (ii) annealed HfO_2, (iii) as-grown HfAlO and (iv) annealed HfAlO grown on compressively strained SiGe.

Figure 4.1(b) shows the XPS spectra of Ge *3d* binding energies for the HfO_2 and HfAlO thin films before and after thermal annealing. Curve fittings of the Ge *3d* core level spectra reveal that the two peaks correspond to the chemical bindings of Ge-Ge and Ge-O_x, respectively. The main peak at the binding energy of ~29.3eV originates from the elemental form of Ge in the SiGe substrate; and the peak at the higher binding energy indicates the presence of GeO_x resulted from Ge oxidation at the interfacial region. By comparing the peak intensities between the as-grown and annealed HfO_2 samples, one can find the huge increment of the GeO_x peak intensity which indicates severe oxidation of Ge at the HfO_2/SiGe interface after thermal annealing. On the other

hand, for the annealed HfAlO film, there is only a small increment of the GeO_x peak intensity and the Ge peak is still higher than the GeO_x peak, suggesting that adding alumina into HfO_2 suppresses further oxidation of Ge at the HfAlO/SiGe interface. In addition, a very careful examination of the binding energy of GeO_x peak of the four samples reveals that there is a slightly higher binding energy shift of Ge which is attributed to more fully oxidized Ge or formation of Ge-Al-O. Thus more energy is needed to break the bond, resulting in higher thermal stability and lower diffusivity of Ge compared to GeO_x ($x<2$). This Ge diffusion suppression effect is also revealed by the absence of hysteresis loop in the following *C-V* result. It is interesting to notice from Fig 4.1(c), however, that this suppression effect is not that obvious for the formation of SiO_x at the interface, suggesting that HfAlO may have some selectivity in suppressing the formation of GeO_x and SiO_x at the IL.

Figure 4.2 shows the HRTEM images of both "thin" and "thick" films of annealed pure HfO_2 and HfAlO on SiGe, respectively, which revealing the interfacial structures and reactions. In the figure, it can be seen that, after thermal annealing, the IL formed at the interface for all samples. Comparing the IL of HfO_2/SiGe to those at the HfAlO/SiGe, they are relatively thicker and rougher. This illustrates the presence of alumina in the HfO_2 films helps to improve the interfacial structure during post thermal annealing.

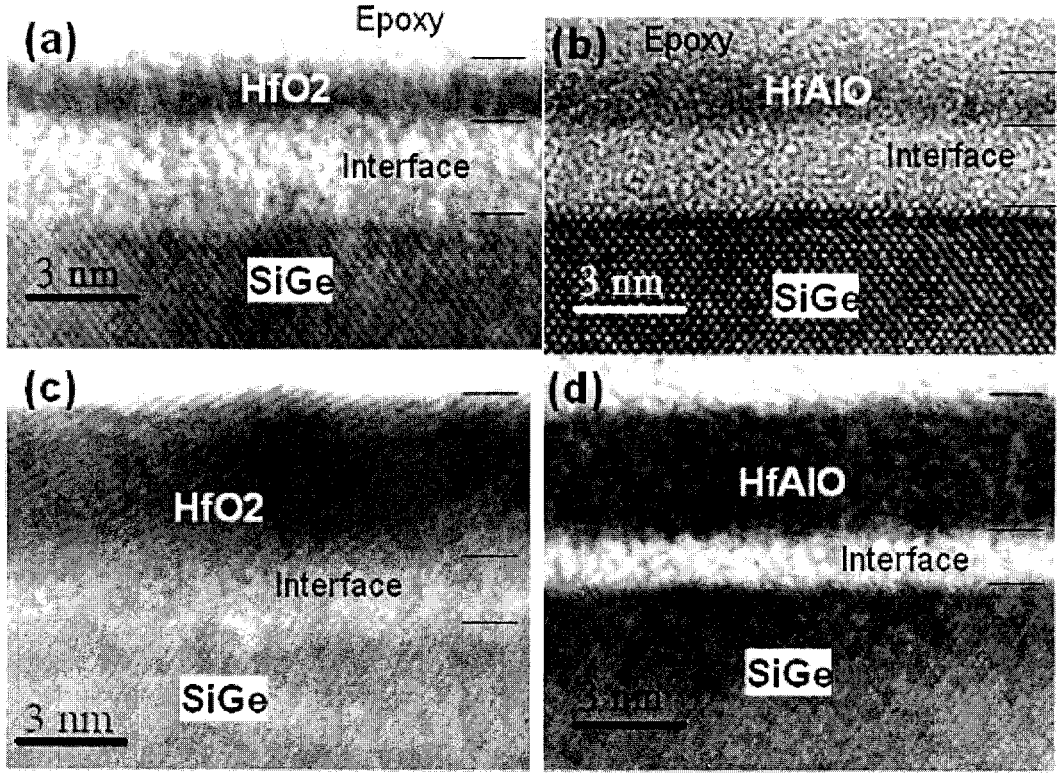

Fig 4.2 Cross-sectional TEM images shows the interfacial structures for the annealed samples of (a) thin HfO_2, (b) thin HfAlO, (c) thick HfO_2 and (d) thick HfAlO.

It is also worth noting that after annealing at 600°C, the HfO_2 films are crystallized while the HfAlO films remains amorphous. The existence of grain boundaries in the crystallized HfO_2 is believed to be responsible for the formation of rougher interface attributed by unbalanced oxygen diffusion since oxygen diffuse along the grain boundaries is faster than that inside the grains.

4.3.2 Electrical property study

Figure 4.3 shows the leakage current characteristics of the as-grown and annealed HfO_2 and HfAlO "thick" films on SiGe. Generally, HfAlO films give lower leakage

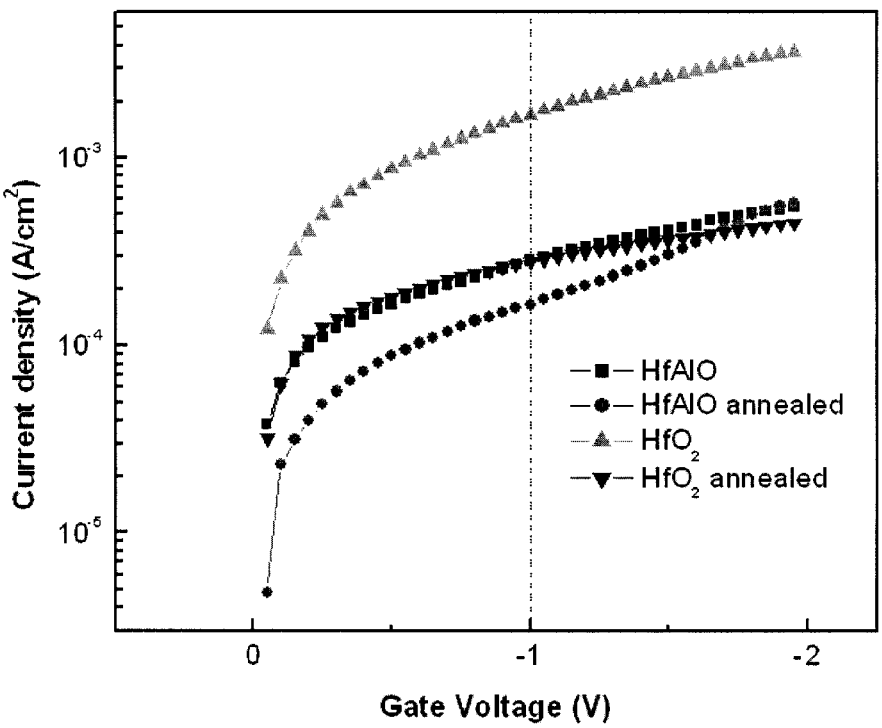

Fig 4.3 *J-V* characteristics for the HfO_2 and HfAlO films before and after thermal annealing in N_2 ambient at 600 °C for 45 min.

current density than those of HfO_2 films. After thermal annealing process, there is large decrease of the leakage current which is attributed to the increase of the interfacial layer thickness and the reduction of oxygen deficiencies. The relatively larger leakage current for the annealed HfO_2 film compared to the annealed HfAlO film is attributed to the large amount of path through the grain boundaries of the crystallized oxide layer.

Figure 4.4 shows characteristic *C-V* curves of the as-grown and annealed HfO_2 and HfAlO films on SiGe. A significant change can be seen in Fig. 4.4(a) for the HfO_2 film after annealed. For the as-grown HfO_2 film, there is a large negative flat band voltage shift (V_{FB}) and a hysteresis loop during forward and reversed bias sweep. The large negative shift indicates the existence of positive fixed charges in the HfO_2 film. The positive fixed charge in the HfO_2 films has been theoretically explained recently by Robertson[1], and was attributed to oxygen vacancies. Therefore, the right shift of the *C-V* curve after annealing can be explained as a result from reduction of the number of oxygen vacancies in the HfO_2 film. The large anti-clockwise hysteresis loop presented indicates charge trapping in the oxide, and the diffusion of Ge into the oxide is believed to be responsible for the observed charge storages[2,3]. The oxide trapped charge density (N_{ot}) can be calculated from the *C-V* loop by the following formula[3].

$$N_{ot} = \frac{C_{acc} \times \Delta V_{FB}}{qA}, \tag{4.1}$$

where C_{acc} is the accumulation capacitance, ΔV_{FB} is the hysteresis width, q is the electron charge and A is the electrode area. The density of the trapped charges is calculated to be about $7 \times 10^{12}\,cm^{-2}$. Although, the hysteresis loop disappears after thermal annealing, the *C-V* curve shows large stretch-out indicating the formation of high density of interface traps. The significant decrease of the accumulation capacitance for the annealed HfO_2 film is due to the formation of thick Si and Ge-riched interfacial layer. In Fig. 4.4(b), however, the *C-V* curve is normal with very small flat-band voltage shift. The change of accumulation capacitance of HfAlO film after annealing is also very small, indicating very limited reduction of the dielectric constant of the film. It

may be also due to the relatively small increment of IL thickness between the HfAlO/SiGe interface. The dielectric constant of HfAlO films is ~9 and the equivalent oxide thickness are ~2.4 nm, calculated from the accumulation capacitance serially connected to the IL and HfAlO films.

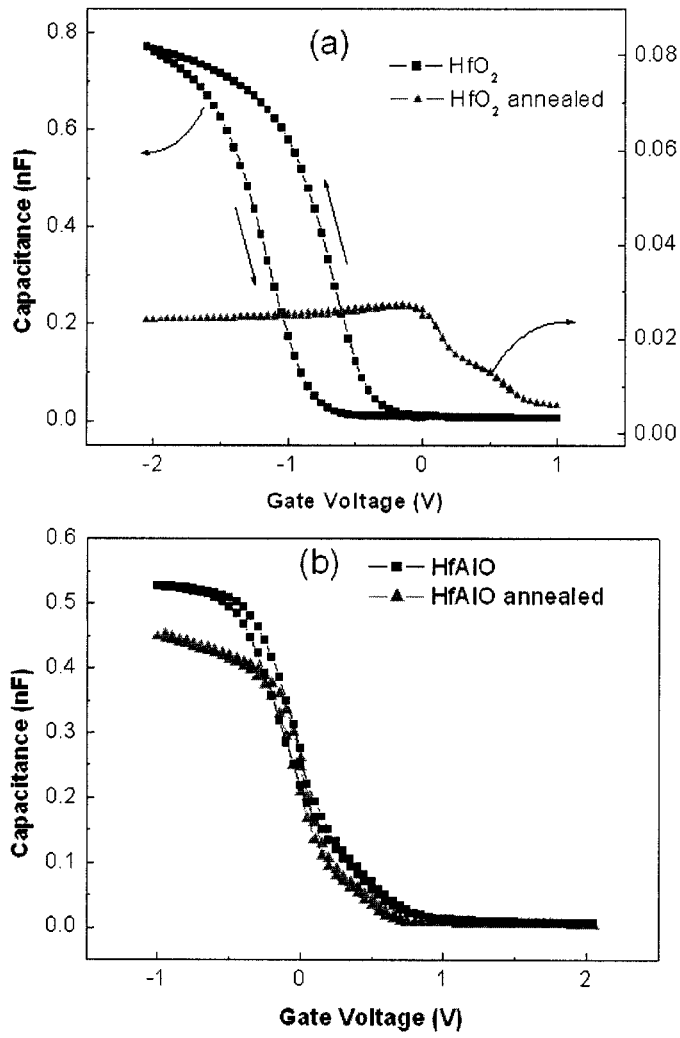

Fig 4.4 High-frequency (1MHz) *C-V* characteristics for (a) HfO_2 and (b) HfAlO films before and after thermal annealing.

The merit of adding alumina in HfO_2 can be considered in terms of suppression of the interfacial reactions, Ge diffusion and GeO_x formation. The XPS and *C-V* results suggest that the HfAlO reduces the interfacial reaction, which is evidenced by the relatively lower Ge-O peak and smaller interfacial layer thicknesses and roughness. Even though TEM results do not show distinct difference in interfacial layer thickness, the fact of less GeO_x presence in the XPS result and the disappearance of hysteresis loop in the *C-V* measurement suggest that adding alumina in HfO_2 may reduce the Ge diffusion into the dielectric layer as alumina serves as an effective diffusion barrier.

4.3.3 Suppression effects of Si-cap layer on GeO_x formation

Since Ge diffusion and GeO_x formation at the high-*k* dielectric/SiGe interface has been proven to be detrimental to the performance of the MOSFET due to the formation of interfacial states and charge traps in the dielectric layer, it has been proposed that a very thin layer of Si-cap on SiGe can act as a sacrificing layer to prevent the Ge diffusion and GeO_x formation [2,4]. In this section, the merit of Si-cap layer in suppressing the GeO_x formation at the high-*k*/SiGe interface will be demonstrated.

A very thin (9 Å) layer of Si-cap has been grown on top of the SiGe/Si wafers (provided by IQE Silicon Compounds Co. Ltd based on our design). The Si-cap layer is believed to be free from strain since the lattice constant of the compressively strained SiGe is identical to that of Si substrate. To study the formation of GeO_x formation at the interface, the interfacial chemical state for different samples were investigated by XPS

analyses. Figures 4.5 to 4.8 show the XPS spectra of Ge *3d* core levels of totally 16 samples with four different conditions: with and without Si-cap, before and after annealing, different oxygen partial pressures, 2×10^{-4} Pa and 5 Pa, and two different dielectrics, HfAlO and HfO_2.

Figures 4.5 shows the Ge *3d* XPS spectra of the samples grown in oxygen gas ambient of 5 Pa, where (a) is the as-grown HfAlO film without Si-Cap, (b) is the as-grown HfAlO films with Si-Cap, and (c) and (d) are their annealed samples. Four arrows were added into all figures to help for the descriptions. Arrows 1 and 4 illustrate the effect of the existing of Si-cap and, arrows 2 and 3 illustrate the effect of thermal annealing to the GeO_x formation. By comparing the relative strength of the Ge *3d* peaks corresponding to the GeO_x and Ge element, the suppression effect of Si-cap on GeO_x formation during film growth and the subsequent post thermal annealing can be seen.

Following arrow 1 to compare Figs. 4.5 (a) and (b), a slight effect of the Si-cap layer to reduce the GeO_x formation during HfAlO film growth can be seen. Figures 4.5 (c) and (d) clearly show that after thermal annealing, the relative height of GeO_x peaks increases. However, it is apparent that the increase of GeO_x peak for the sample without Si-cap increases more significantly. This clearly illustrates the suppression on GeO_x formation at the interface by the presence of a Si-cap layer on SiGe.

Figure 4.6 shows the Ge *3d* XPS spectra of another group of four samples for

comparison when HfO_2 films are deposited on SiGe with and without Si-cap. One can clearly see that the GeO_x peak of Fig.4.6(c) exhibits the most significant increment from that of Fig. 4.6(a), suggesting the formation of large amount of GeO_x at the interface. By comparing Figs. 4.5 and 4.6, one can see that almost all the GeO_x peaks for the HfO_2 samples are relatively higher than that of the HfAlO samples. This again, proves that HfAlO dielectric films are better than HfO_2 in preventing the GeO_x formation when applied on SiGe.

The XPS spectra of Ge *3d* peaks of another two groups of samples, HfAlO and HfO_2 films, deposited at much lower oxygen gas pressure (2×10^{-4} Pa) are shown in Figs. 4.7 and 4.8, respectively. The same trends and results can be drawn from these two groups of samples. For example, the very thin Si-cap on SiGe can act as a sacrificing layer to prevent the formation of GeO_x and thus improve the interfacial quality. In addition, one can also see by comparing Figs. 4.7 and 4.8 with Figs. 4.5 and 4.6, that more GeO_x is formed at the interface for the HfO_2 films deposited at oxygen deficient condition. Therefore, an appropriate oxygen gas pressure is necessary in order to obtain a better quality of interface with less GeO_x formation.

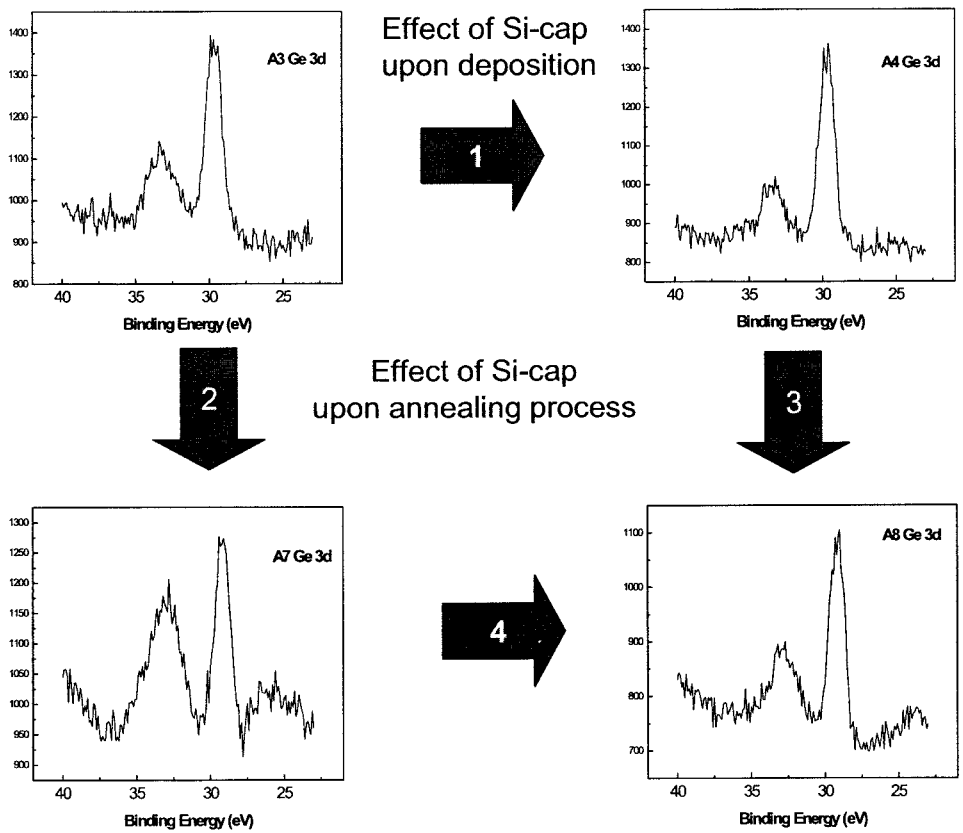

Fig. 4.5 XPS spectra of Ge *3d*: (a) as-grown in oxygen gas ambient (5 Pa) of **HfAlO** dielectric without Si-Cap, (b) as-grown in oxygen gas ambient (5 Pa) of HfAlO dielectric with Si-Cap, and their corresponding samples annealed at 600 °C in N_2 for 45 min.: (c) annealed HfAlO dielectric without Si-Cap, and (d) annealed HfAlO dielectric with Si-Cap, respectively.

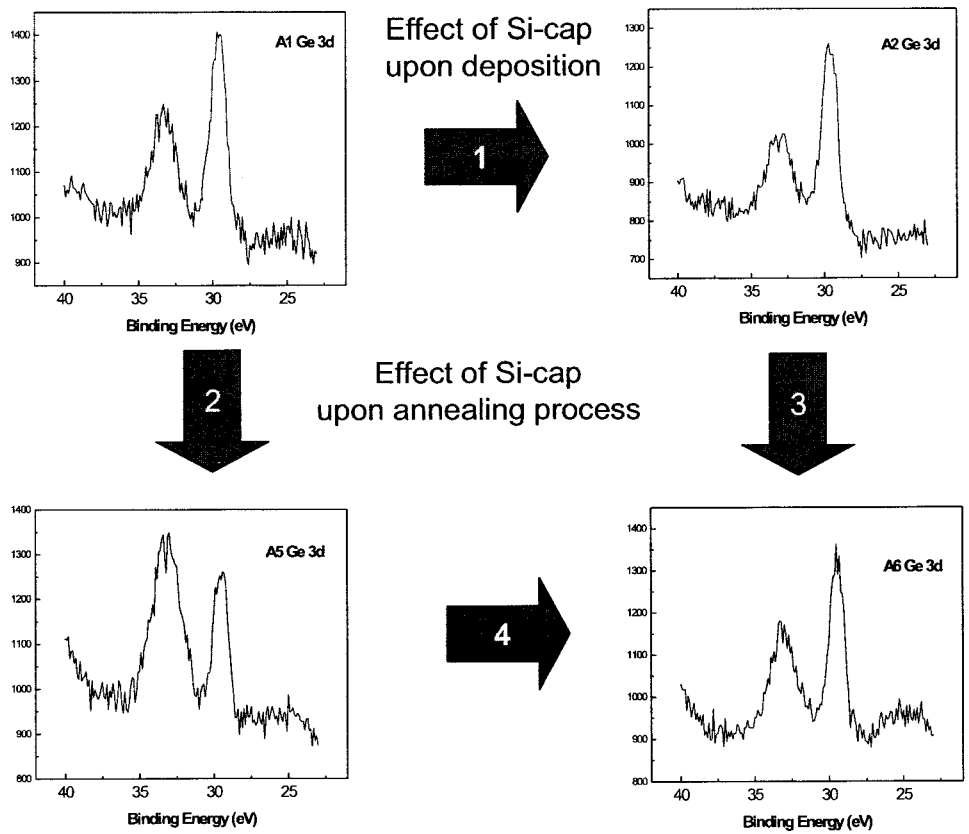

Fig. 4.6 XPS spectra of Ge *3d*: (a) as-grown in oxygen gas ambient (5 Pa) of **HfO_2** dielectric without Si-Cap, (b) as-grown in oxygen gas ambient (5 Pa) of HfO_2 dielectric with Si-Cap, and their corresponding samples annealed at 600 °C in N_2 for 45 min.: (c) annealed HfO_2 dielectric without Si-Cap, and (d) annealed HfO_2 dielectric with Si-Cap, respectively.

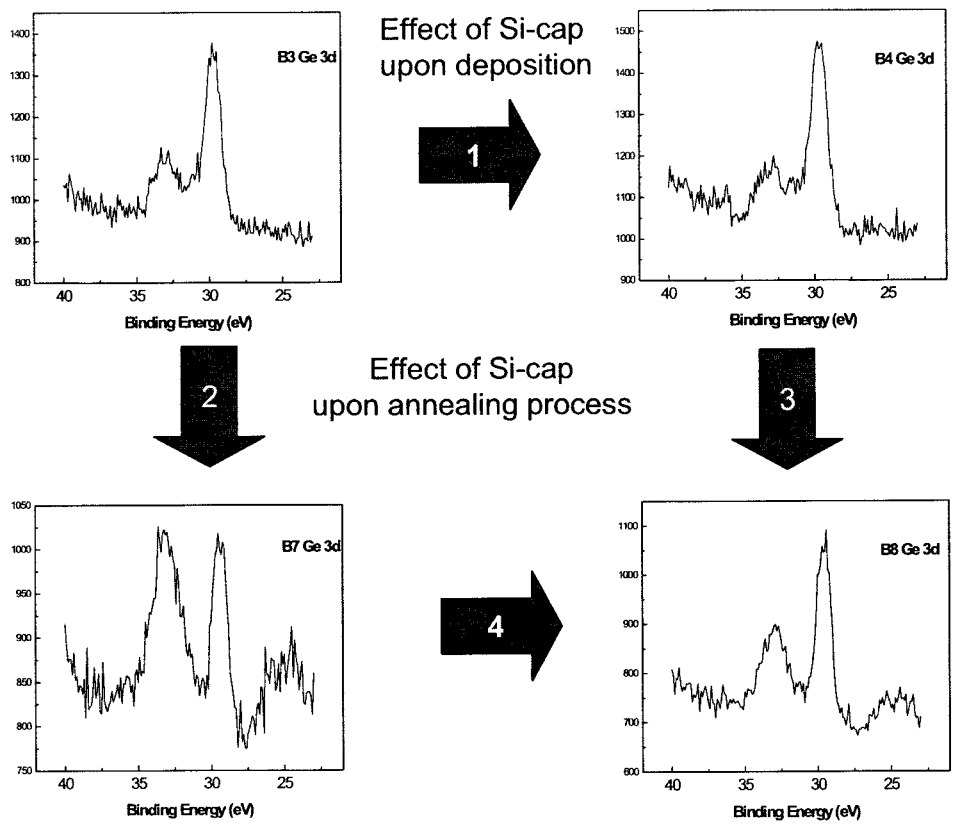

Fig. 4.7 XPS spectra of Ge *3d*: (a) as-grown in oxygen gas deficient (2×10^{-4}Pa) of **HfAlO** dielectric without Si-Cap, (b) as-grown in oxygen gas ambient (2×10^{-4}Pa) of HfAlO dielectric with Si-Cap, and their corresponding samples annealed at 600 °C in N_2 for 45 min.: (c) annealed HfAlO dielectric without Si-Cap, and (d) annealed HfAlO dielectric with Si-Cap, respectively.

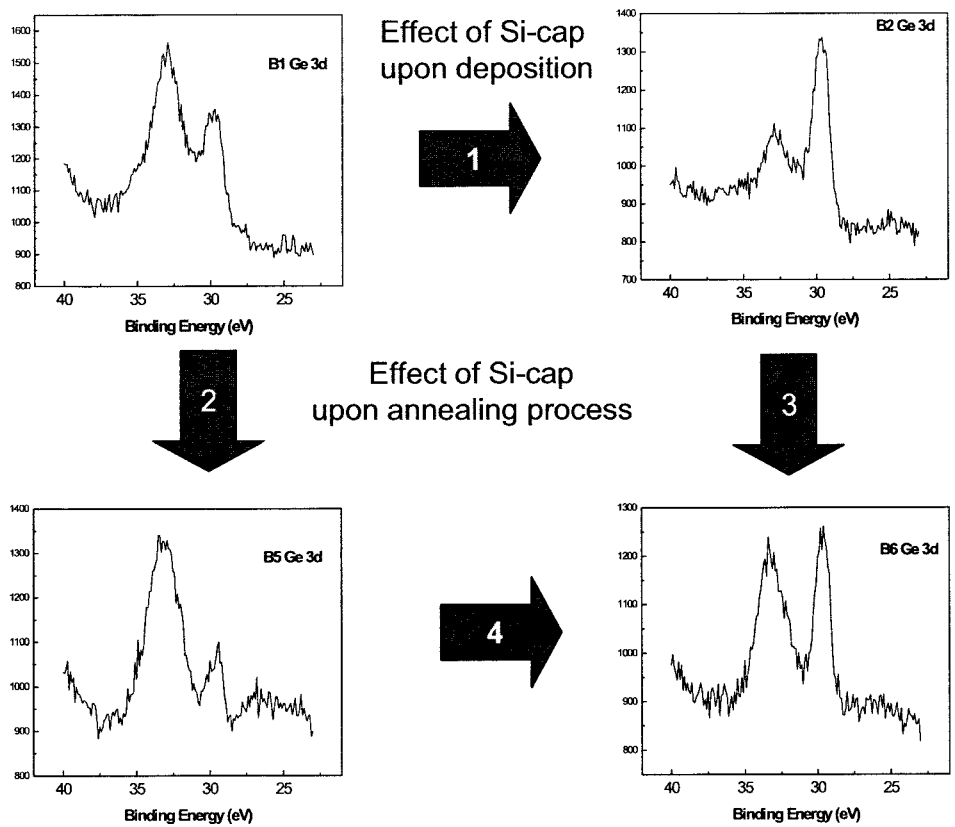

Fig. 4.8 XPS spectra of Ge *3d*: (a) as-grown in oxygen gas deficient (2×10^{-4} Pa) of **HfO_2** dielectric without Si-Cap, (b) as-grown in oxygen gas ambient (2×10^{-4} Pa) of HfO_2 dielectric with Si-Cap, and their corresponding samples annealed at 600 °C in N_2 for 45 min.: (c) annealed HfO_2 dielectric without Si-Cap, and (d) annealed HfO_2 dielectric with Si-Cap, respectively.

4.4 Summary

In conclusion, suppression of GeO_x formation and Ge diffusion has been achieved by adding alumina into the HfO_2 gate dielectric film on the strained SiGe. The corresponding electrical performance has also been improved, as evidenced by the decrease of the leakage current and charge traps in the dielectric layer and interface. In addition, the suppression of Ge diffusion and GeO_x formation by utilizing the Si-cap on SiGe layer has been investigated by XPS analyses. A more significant suppression effect has been demonstrated when both HfAlO dielectric and Si-cap were associated. This dual utilization is novel and attractive in the advanced MOSFET applications.

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Chapter 5

Conclusion and future work

In this thesis, synthesis and characterizations of HfAlO thin films on $Si_{83}Ge_{17}$(SiGe), in particular, the interfacial reactions at the dielectric/SiGe interface and the corresponding electrical properties of the MOS capacitors have been studied. As a comparison, HfO_2 films on SiGe were also studied in parallel with HfAlO on SiGe.

The HfAlO and HfO_2 films were grown by pulsed-laser deposition technique at relatively lower substrate temperature. Compressively strained SiGe/Si and Si-cap/SiGe/Si wafers were used as the substrates to study the interfacial reaction at the dielectric/SiGe interface and thus the electrical properties of the MOS capacitors which are characterized by *C-V*, *G-V* and *I-V* measurements. The structure properties of the dielectric films and the interfacial structure are characterized by means of TEM and XPS analyses.

The effects of Al contents in the HfAlO films on its structural and electrical characteristics have been investigated. It revealed that the changing of Al content in HfAlO films significantly changes its structural and electrical properties, and the XPS Hf *4f* spectra suggest the influence of the Al content to the formation of Hf-Si bonding. Furthermore, dependence of interfacial layer thickness and *C-V* characteristics of the HfAlO films on the growth oxygen pressure were also revealed. Therefore, optimized Al content in the HfAlO and the oxygen pressure during film deposition are crucial to obtain a good interface with low density of defect in the dielectric and dielectric/SiGe interface.

In order to study the merit of HfAlO compared to HfO_2, interfacial reactions and electrical properties of HfO_2 and HfAlO high-*k* gate dielectric films on strained SiGe have been investigated. It revealed that HfAlO films can reduce GeO_x formation at the

interface during the film growth and post thermal annealing process. Such suppression effect in GeO_x formation is attractive since it can reduce charge traps and interfacial defects, and thus improve the carrier mobility.

In addition, the suppression of Ge diffusion and GeO_x formation by utilizing the Si-cap on SiGe layer has also been investigated by XPS analyses. A more significant suppression effect has been demonstrated when both HfAlO dielectric and Si-cap were associated. This dual utilization is novel and attractive in the advanced MOSFET application.

Nevertheless, there are still a lot of work needs to be done to prove the capability for the application of HfAlO on SiGe channel with improved hole mobility. The MOS field effect transistor structures need to be fabricated to demonstrate the increase of hole mobility. In addition, the process compatibility of HfAlO on SiGe channel MOS processing need to be further studied.