The Hong Kong Polytechnic University

Department of Building Services Engineering

Harmonics Regulation and Mitigation in Low-voltage Distribution Systems of Large Buildings

Yuan Zhenhuan

A thesis submitted in partial fulfillment of the requirements for

the Degree of Doctor of Philosophy

November, 2006

Certificate of Originality

I hereby declare that this thesis is my own work and that, to the best of my knowledge and belief, it reproduces no material previously published or written, nor material that has been accepted for the award of any other degree or diploma, except where due acknowledgement has been made in the text.

Yuan Zhenhuan

Department of Building Service Engineering

The Hong Kong Polytechnic University

Hong Kong SAR, China

November, 2006

Abstract

Electronic equipment such as computers, fluorescent lightings, and solid-state motor drives continues to proliferate in modern buildings. Such equipment generates significant harmonic currents in the power distribution systems of the buildings, and may cause malfunction or failure of sensitive equipment. In high-rise commercial buildings, the harmonics situation is even worse due to their "high-rise" nature. The long feeders/rising mains as well as the distribution transformers cause significant harmonic voltage drops along these circuits, and distort the power supply especially on the upper floors in the buildings. Disputes on harmonics are consequently unavoidable due to the ambiguous responsibility among the utility, the landlord and the tenant. This thesis discussed the control of harmonics in the low-voltage distribution systems of high-rise commercial buildings from three different aspects, that is, (1) electrical wiring to minimize the harmonic pollution, (2) harmonic regulation in buildings to manage the harmonics effectively, and (3) harmonic filtering with the proposed voltage-detection-based shunt active power filter (SAPF) to mitigate the harmonics in the distribution systems.

Electric cables are widely used for the power distribution in buildings. It is necessary to characterize the harmonic impedance of these cables in order to mitigate effectively the harmonic propagation within the building distribution

systems. An experimental investigation was made to identify the harmonic impedance of typical power cables used as feeders and rising mains in the buildings. An impedance database was built for commonly-used single-core and multi-core armored cables with the cross-section areas of 95mm^2, 120mm^2, 150mm^2, 185mm^2, 240mm^2, 300mm^2, 400mm^2 and 630mm^2. The impact of the cable type, the arrangement formation and the setup environment on the harmonic impedance was revealed as well. Those results and conclusions are helpful in the design of wiring systems in large buildings so as to prevent harmonic pollution effectively. They are also useful in conducting harmonic assessment for harmonic management in the building distribution systems.

To manage harmonics in commercial buildings effectively, harmonic regulation based on UK Engineering Recommendation G5/4 was recommended for the building distribution systems. The harmonic limits of both voltage and the current as well as the procedures of harmonic assessment in buildings were proposed according to other widely used standards such as the IEEE519-1992 standard and IEC standards on harmonics. The proposed harmonic-assessment scheme provides a method to assess the connection of the harmonic-producing equipment into the existing system. To solve the disputes on harmonics responsibilities among the parties in the building were recommended Depending on the types of the distribution systems, the guidelines of equipment selection and installation were provided for achieving a compatible environment

in the buildings. The procedure was demonstrated in a typical large commercial building.

In order to comply with the harmonic limits within commercial buildings, effective mitigation measures should be made available for landlords to control excessive harmonic pollution in the building distribution systems. In this thesis, a SAPF based on voltage detection was proposed to control harmonic voltage over the whole building distribution system. The control strategy based on a multi-channel and complex-gain control was developed. The multi-channel complex-gain controller was based on the harmonic synchronous reference frames, and provided an independent control on both the magnitude and the phase of the reference currents. This control method is helpful as well in improving stability margins. Apart from harmonic mitigation over the distribution systems, the proposed SAPF also has the capability of damping harmonic resonance. A three-dimensional space vector PWM technique was adopted in the proposed SAPF. Theoretical derivation of the proposed control strategy was conducted, and analytical models were deduced to analyze both the characteristics of the proposed SAPF and the performance of harmonic voltage control along the long distribution circuits. Computer models on the platform of MATLAB/SIMULINK were developed, and digital simulations were performed to validate the analytical results. The prototype of the SAPF using a DSP chip of TMS320F2812 was developed. The proposed control algorithms were

successfully implemented. Finally the laboratory testing system including the line simulator was set up. Experiments were conducted to validate the proposed control method and filtering performance of the SAPF connected in a distribution system.

The proposed approaches may be extended for harmonic control in utility distribution systems especially in a deregulated market, as these systems essentially are similar in terms of supply and demand relationship.

Acknowledgements

I must express my grateful thanks to my Supervisor, Dr. Du Yaping, Associate Professor from the Department of Building Services Engineering (BSE), The Hong Kong Polytechnic University, for his readily available supervision, valuable suggestions, patient guidance, continuous help and encouragement throughout the course of the work.

My special thanks go to The Hong Kong Polytechnic University for financially supporting this project. I would like to also thank Mr. Fung Wing-kwong and other technicians in the laboratory for their assistances and supports in my experimental works.

Finally, I would like to express my deepest appreciation to my family members: my parents, Zhang Jingjing – my wife. I would not have finished my work without their on going patience, supports and understandings.

Table of Contents

List of Figures

Chapter 2

Chapter 4

Chapter 5

Chapter 6

Chapter 7

Chapter 8

List of Tables

Chapter 8

Chapter 1

Introduction

1.1 Background

With the proliferation of electronic equipment such as fax machines, copiers, printers, computers, fluorescent lightings and building automation control, harmonics in commercial buildings are increasingly of concern as distorted current and voltage may cause unexplained tripping of protective devices, malfunction of end-user equipment, overheating of conductors, high neutral displacement voltage, and may reduce reliability, efficiency and life expectancy of connected equipment. The qualified power supply within the distribution systems in buildings becomes more difficult to obtain.

The “high rise” nature of high-rise commercial buildings may aggravate the harmonic problems in the buildings. Long electric cables as well as distribution transformers in a building can cause significant harmonic voltage drops along the circuits. This aggravates the power quality especially for the consumers on the upper floors. In addition, for structural and transportation reasons, light-weight single-phase transformer banks are employed in buildings. Such transformer banks are inferior in harmonic suppression, compared with the conventional three-phase core-type transformers. Problems associated with

harmonics have been experienced continuously in the distribution systems of high-rise commercial buildings.

The absence of specific and detailed harmonic regulation in high-rise buildings has led to the poor management of harmonics. The ambiguous responsibility of harmonic control in buildings has degraded the power quality. This also results in a mass of disputes arising from harmonic problems. In addition, the measures of harmonic mitigation applied in buildings generally aims at reducing harmonic currents from centralized loads or at the point of common coupling next to a distribution transformer. The harmonic distortion within the building are may remain unchanged. All these make it unavailable to address effective harmonic control in the low-voltage distribution systems of high-rise commercial buildings.

1.2 Objectives

In order to prevent potential and/or to solve existing harmonic problems, the research on harmonic modelling, regulating, mitigating and analyzing in power systems has been carried out extensively. It is noted that the distribution systems in high-rise commercial buildings have unique features in the aspects of harmonic generation, control and mitigation. A research study on harmonics regulation and mitigation in the building distribution systems was carried out.

The objectives of this thesis were identified, as follows:

- Characterize harmonics over building LV distribution systems
- Investigate electrical wiring to prevent the harmonic pollution
- Develop harmonic regulation in large buildings to manage the harmonics effectively
- Propose harmonic mitigation solution using the proposed voltage-detection-based shunt active power filter (SAPF) to achieve effective harmonic control in the distribution systems
- Develop the guidelines of equipment selection and installation for achieving a compatible environment in the buildings.

The knowledge of harmonics over building distribution systems, which is necessary to conduct the research, was not fully available although a number of studies on harmonics from loads had been carried out. Both harmonic current and voltage were identified and characterized based on a survey at main LV switchboards, risers or feeders, meter rooms, and final circuits.

Electric cables are widely used for power distribution in buildings. It is necessary to characterize the harmonic impedance of these cables in order to mitigate effectively the harmonic propagation within the systems. An experimental investigation was made to identify the harmonic impedance of typical power cables used as feeders and rising mains in the buildings. Those

results and conclusions are helpful in the design of the wiring systems in large buildings so as to prevent the harmonic pollution effectively. They are also useful in conducting harmonic assessment for harmonic management in the building distribution systems.

To manage harmonics in commercial buildings effectively, harmonic regulation in local large buildings was recommended, and was demonstrated in a typical building distribution system. The proposed harmonic-assessment scheme provides a method to assess the connection of the harmonic-producing equipment into the existing system. To solve the disputes on harmonics responsibilities among the parties in the building were recommended.

In order to comply with the harmonic limits within commercial buildings, effective mitigation measures should be made available for landlords to control excessive harmonic pollution in the building distribution systems. In this thesis, a SAPF based on voltage detection was proposed to control harmonic voltage over the whole building distribution system. The proposed SAPF is an effective tool for the landlord to manage the harmonics in buildings. The current harmonics injected into a utility network can be reduced in accordance with the corresponding limits, while the qualified voltage in the building distribution system remains. With the developed tool an appropriate tariff scheme on harmonic current from tenants may be possibly implemented in the buildings

The proposed approach may be extended for the use of harmonic control in utility distribution systems especially in a deregulated market, as these systems essentially are similar in terms of supply and demand relationship.

1.3 Thesis Outline

Chapter 1 introduces the background of the research topic, and highlights the objectives of this thesis.

Chapter 2 provides an overview of harmonics in the low voltage (LV) distribution systems of high-rise commercial buildings. The typical features of the building distribution systems are firstly introduced. Then common sources of harmonics in the commercial buildings are identified. The negative effects of harmonics in buildings are discussed. Three recorded cases of harmonic problems in Hong Kong are presented to illustrate the necessities of harmonics control in building distribution systems.

Chapter 3 reviews the issues of harmonic control in the LV distribution systems of buildings. Firstly, major international and national standards on harmonics are briefly presented. Problems in regulating harmonics in commercial buildings are then addressed Active power filters, which are proved as an

effective device to alleviate harmonics in electrical systems, are reviewed. The application of the active power filters within the buildings is addressed, and the problems in filter application are identified. Other strategies of harmonic control are introduced briefly, including those applied at both the equipment level and the system level.

Chapter 4 presents an investigation into the harmonic impedance of electric power cables using an experimental method. An impedance database was built for commonly-used single-core and multi-core armored cables with the cross-section areas of 95mm^2, 120mm^2, 150mm^2, 185mm^2, 240mm^2, 300mm^2, 400mm^2 and 630mm^2. The impact of the cable type, the arrangement formation and the setup environment on the harmonic impedance is presented as well.

Chapter 5 addresses harmonic regulations in commercial buildings, which are necessary in controlling harmonics effectively within the building. Firstly, a harmonic assessment procedure based on UK Engineering Recommendation G5/4 is proposed, and is applied to building distribution systems. The harmonic limits of both voltage and current in the systems are recommended according to other widely used standards such as the IEEE519-1992 standard and IEC standards on harmonics. Further, the responsibilities among all parties in controlling harmonics within the buildings are recommended. The procedure is demonstrated in a typical high-rise commercial building.

Chapter 6 proposes a shunt active power filter (SAPF) based on voltage detection to achieve effective mitigation of harmonics over a building distribution system. The strategy of multi-channel complex-gain control is presented. The multi-channel complex-gain controller operates on harmonic synchronous reference frames, and provides independent control on both the magnitude and the phase of reference currents. This control method is helpful as well in improving the margins of system stability. A three-dimensional space vector PWM technique is adopted in the proposed SAPF. Theoretical derivation of the proposed control strategy is presented, and analytical models are deduced to analyze both the characteristics of the proposed SAPF and the performance of harmonic voltage control along the long distribution circuits.

Chapter 7 presents the validation of the proposed SAPF with computer simulations. Computer models on the platform of MATLAB/SIMULINK are described, and digital simulations are presented to validate the analytical results. The characteristics of the proposed SAPF are addressed such as the DC loop performance, the transient response of the SAPF and the tracking of the reference currents etc.. To demonstrate the performance of the proposed SAPF, the proposed SAPF was tested under several cases. The issues, such as the role of the multi-channel complex-gain controller on filtering performance, system

stability, resonance damping, as well as the impact of the digital low pass filter are discussed.

Chapter 8 describes the implementation of the proposed SAPF. A prototype of the SAPF using a DSP chip of TMS320F2812 was developed, and described in this chapter. The proposed control algorithms were successfully implemented. The laboratory experiment system including the SAPF prototype and the line simulator was set up. Experiments were conducted, and the results are presented in this chapter to validate the proposed control method and filtering performance of the SAPF connected in a distribution system.

Chapter 9 summarizes the conclusions of the research works conducted and outlines the works to be carried out in the future. The conclusions on harmonic characteristics in high-rise commercial buildings, the cabling, harmonic regulation and responsibility sharing for harmonic management, and harmonic control by the proposed SAPF are made. The future work is identified, which includes the adaptive control of the control gain of the SAPF, and the cooperation of multiple active power filters in high-rise commercial buildings.

Chapter 2

Harmonics in High-rise Commercial Buildings

2.1 Introduction

This chapter provides an overview of harmonics in the low voltage (LV) distribution system of high-rise commercial buildings. The typical features of the building distribution system as well as the typical configurations are introduced firstly. Common sources of harmonics in the commercial buildings are then identified. The negative effects of harmonics in buildings are discussed. Three recorded cases of harmonic problems in Hong Kong are presented to illustrate the necessities of harmonics control in building distribution systems.

2.2 High-rise Commercial Buildings in Hong Kong

Different parts in the world have different definitions of a high-rise building. In Hong Kong, a building is classified as the high-rise building if it is taller than 30m [FSD 1998]. As one of capital and transportation centers in the world, high-rise commercial buildings in Hong Kong have the following typical features:

a) Most of the commercial buildings are of high-rise and above 30 stories,

some of which are up to 80 stories.

b) Nearly all recently-built buildings employ a curtain walling system. This means intensive HVAC design should be catered for the glazing heat through the curtain wall.

c) In high-rise buildings, it should be well considered to arrange the lift installation because the space requirement for the lifts has a major impact on the usable space. Hence, the design of lifts should make a trade-off among cost, space and passenger transfer capability. Usually, a multi-zone system is adopted in the commercial building. With this arrangement, many lift shafts are saved and corresponding construction cost is also reduced. However, to cater for the high transportation capability with the minimum capacity, high speed lifts with advanced variable voltage variable frequency control are frequently used.

d) The humid climate in Hong Kong also increases the loading of HVAC installations.

e) Because of flourishing business for most tenants in commercial buildings, modern office equipment is employed massively.

2.3 Building Distribution Systems

2.3.1 Major Components in the Distribution Systems

a) Utility power supply

Due to ever-increasing demand by businesses, high-rise commercial buildings draw very large amounts of power and consume significant amounts of energy [IEEE Task Force 1985]. The Utility usually feed the buildings by a number of 11kV/380V distribution transformers via 11kV underground cables. With this consideration, a high voltage switch room is usually required on the ground floor of the buildings to locate the ring-main-units and switch gears, etc. [HKE 1995].

b) Distribution transformers

Traditionally distribution transformers are placed on the ground floor. With the increasing power loadings in the building, significant energy losses and voltage drops in the long building distribution systems become the issues of concern. The possible solution is to re-locate the distribution transformers in the areas near the load centers. Placing the distribution transformers on the upper floor may cause problems in providing transportation and maintenance access to the transformers. In practice, three 500 kVA single-phase transformers which are wired in star connection are employed to form 1500 kVA three-phase units. This measure, however, exacerbates harmonic problems and the electromagnetic

interference (EMI) in the buildings

c) Distribution Circuits

Feeders and rising mains are the major elements in buildings distribution systems, and the circuits of 100m length are not uncommon in a high-rise building. In practice, feeders and rising mains are generally by power cables, air-insulated busbars (busbar trunking), and fully-insulated busbars (busduct). Normally, busbar trunking or busduct has a large rating up to the transformer full-load current, while power cables are capable of carrying the current of up to1000 A. The distribution board fed from the rising mains is situated in a meter room close to load centers, and supplies electricity to various loads on the floor. The distribution board for tenant loads has a typical rating of 200-400 A.

d) Standby Generating-Sets

The standby generating sets are part of the building distribution system in a building. They provide standby power for fire services loads as well as other essential loads in the building in case of a failure in mains supply.

A generating set has a transient reactance, which is much greater than that of the mains supply. If harmonic currents generated from the connected non-linear loads flow back to the standby generating set, significant harmonic voltage distortion will be developed on the terminals of the generating set. Therefore,

the standby generating set is usually oversized to cater for the excessive harmonic distortion.

e) Centralized reactive power compensation

Centralized capacitor banks are required in building distribution systems to compensate reactive power consumption by loads. According to the requirement of Utilities, the minimum power factor is 0.85 (lagging). Usually the capacitor banks are installed at the main switchboard on the ground floor. They may be installed on chiller plant rooms on the roof as the HVAC equipment is the dominant one consuming reactive power.

f) Loads in commercial buildings

Loads in commercial buildings include HVAC systems, lighting and small power loads, lifts and escalators, and others. HVAC systems are the large group of loads in air-conditioned commercial buildings. Lighting and small power equipment is the second and third largest loads in the buildings.

✧ HVAC systems

The power or energy losses in HVAC systems are significant. To minimize these losses high efficiency motors are usually used. Recently, variable speed drives (VSDs) have been employed significantly for the motors that enable the driven equipment to be operated over a range of speeds in an efficient way. The major

advantage of VSDs is to improve the overall efficiency of the HVAC system under partial-load conditions. Electronic types of VSDs include the current source inverter, the cycloconverter, the load-commutated inerter, and the pulse-width-modulated (PWM) and voltage-source inverter, etc.. The rich harmonics is the drawback of modern VSDs, which pollute the power distribution systems in the buildings.

✧ Lamps and luminaries

The lamps used in buildings can be classified as the fluorescent lamps, high intensity discharge lamps and incandescent lamps. All the fluorescent lamps and high intensity discharge lamps need ballasts in operation. The functions of ballasts are to supply controlled power to heat lamp electrodes and starting voltage to ionize lamp gas, to create electron discharge stream between electrodes and limits current, and to controls power to the lamp for proper operation.

There are two types of ballasts used for fluorescent lamps and high intensity discharge lamps, that is, electromagnetic ballast and electronic ballast. An electromagnetic ballast represents the traditional copper-iron control gear for lamps. It needs an external glow starter. A capacitor is required for power factor correction. The initial cost for installing this category of ballasts is relatively low compared with electronic ballasts. Electronic ballasts have the potential of

lower ballast losses. Using electronic ballasts can enhance significantly system efficiency as well as light output quality. Accordingly the operating cost of these systems is lower than that with electromagnetic ballasts.

With the increasing usage of more sophisticated lamp equipment that incorporated electronics switching devices, the power quality consideration should bear more concern in a lighting system. Some electronic ballasts may be equipped with active filters to reduce current distortion. The electronic ballasts for compact fluorescent lamps, however, don't have such filters. They generate significantly high current distortion. Additionally, the capacitors installed for magnetic ballasts if any worsen the harmonic distortion.

✧ Lifts and escalators

The Code of Practice for Energy Efficiency of Electrical Installations (COP) [Energy Advisory Committee 1998] requires that all electrically driven equipment and motors forming part of a vertical transportation system shall comply with the Code of Practice for Energy Efficiency of Lift and Escalator Installations. It is quite common to use modern lift driving systems (e.g. ACVV, VVVF etc.) for the concern of energy efficiency in the lift installations. However, harmonics arising from the usage of these electronic drives would be an issue of concern in discussing power quality of the distribution system in buildings.

Dedicated feeders are usually adopted for lifts and escalators to facilitate separate metering and monitoring of the energy consumption for future energy management and auditing purpose.

✧ Electrical appliances

Electrical appliances used in a building include computers, printers, copiers, facsimile machines etc.. They cover all of the building with a great quantity. The energy used by office equipment, approximately 50% is for personal computers (PC) and monitors, 25% is for computer printers, with remaining 25% for copiers, facsimile machine, and other miscellaneous equipment [Y. Du etc. 1998a]. These modern office appliances are considered as the harmonic producing equipment. They are usually equipped with a single-phase rectifier circuit, which generates significant harmonic distortion of the current in the circuits.

2.3.2 A Typical Building Distribution System

Illustrated in Figure 2.1 is a typical LV distribution system found in high-rise buildings. The utility supplies electrical power to LV customers via a distribution transformer. The transformer is installed in the transformer room within a building, and is connected to a main LV switchboard in the adjacent

switchroom. The main switchboard feeds distributed loads via radial LV distribution circuits. A standby generating set is installed within the building, and is connected to the essential busbar within the main switchboard via an automatic changeover switch. This generating set supplies electricity to the essential loads only if the mains supply fails. A capacitor bank may be installed in the LV siwtchroom and connected to the busbar within the main LV switchboard for the improvement of power factor.

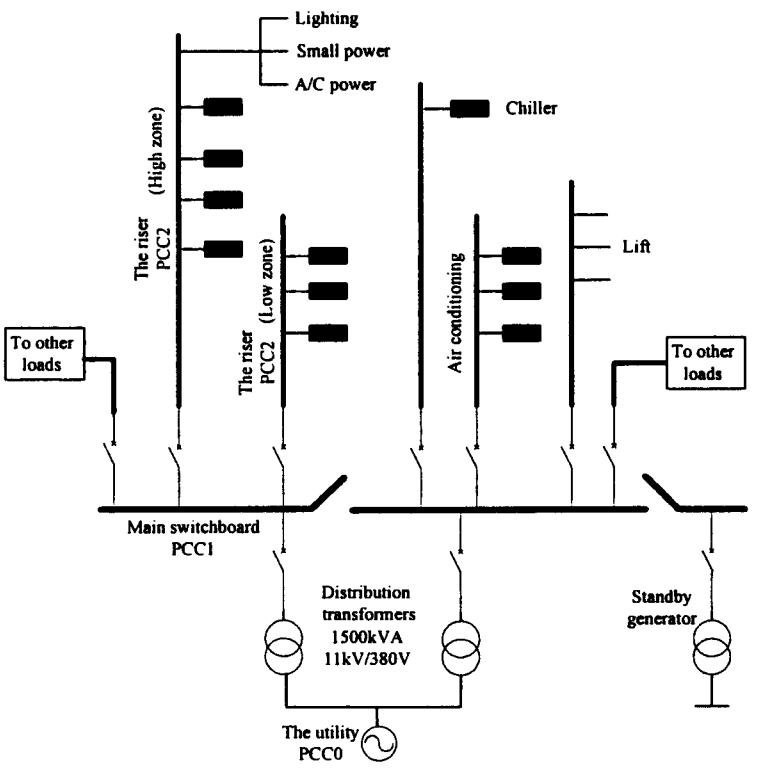

Figure 2.1 Typical LV distribution system in a high-rise building

The vertical distribution circuits in a building may be classified as rising mains circuits (distributed loads), or feeder circuits (centralized loads). These are three-phase four wire circuits, and are normally made by electric power cables

or air-insulated busbars (busbar trunking), or fully-insulated busbars (busduct). The length of 100 meters is not uncommon in a high-rise building. These circuits feed HVAC power equipment, public lighting, lift power equipment, tenant office equipment, etc. in the building.

The raising mains circuit feeds a number of distribution boards situated in the meter rooms close to load centers. Metering boards are provided after the distribution boards in the meter rooms as the distribution boards serve as the interface between the supply network and the customer installations

2.3.3 Deficiency of Existing Distribution Systems

As engineers design LV electrical systems according to the same supply rules and wiring regulations, most of the electrical systems, hence, have more or less the similar deficiencies.

a) Utility companies strictly requires that the type and setting of protective devices on the customer main switch should be so selected that they can be graded properly with the utility company's feed protection. By fulfilling this, the discrimination in the further outgoing circuits cannot exhibit proper discrimination.

b) The supply rules and wiring regulations mention little about non-linear loading and harmonic currents in the distribution systems of buildings. As a result, no designer cares to prepare their design with the consideration of harmonic problems. For example, there is no ammeter in a main switchboard to read neutral current. Hence, any overloading in the neutral conductor due to harmonic current is never known until the accident occurs. What is more, the possible harmonic resonance problem, which may occur in the capacitor bank and inductive loads due to harmonic currents, is neither known nor addressed.

c) As mentioned above, single-phase transformers are positioned on the upper floor of buildings in order that the transformers can be placed at the load centres. This, however, creates a severe electromagnetic interference problem arising from the high current carrying conductors connecting the transformers and the main switchboard. Other than this, the wye-connected single-phase transformers create also the harmonic problem which does not happen in the core-type three-phase transformers.

d) Due to the congested environment in the high-rise commercial building, electromagnetic fields from current carrying cables and busbar frequently cause the EMI problem to nearby sensitive equipment, i.e. computer terminals.

2.4 Sources of Harmonics in Buildings

A pure sinusoidal waveform without harmonic distortion is a hypothetical quantity and not a practical one. Even at the point of generation, the voltage waveform still contains a small amount of distortion due to non-uniformity in the excitation magnetic field and discrete spatial distribution of coils around the generator stator slots. The voltage distortion at this point normally is low, typically less than 1.0%.

The end-user equipment generates currents that contain rich harmonics, especially in high-rise commercial buildings. As harmonic currents travel back to the utility's network, the current distortion results in additional voltage distortion due to impedance of the path including distribution transformers, e main switchboards, rising mains circuits, final circuits and other components. The harmonic voltage distortion gradually increases towards to the end-user equipment. This section briefly describes the common nonlinear loads found in high-rise commercial buildings.

a) Variable speed drive (VSD)

About 56% of electrical power is used for electric motors, of which about 10% are controlled by VSDs that are becoming commodities in more and more applications today [F. Abrahmsen 2000]. VSDs can be found in most of building services installations ranging from chilled water pump sets, variable air

handling units and high speed lifts. For the system with a VSD, the reactive power into the motor is not seen from the line side. The reactive power is circulated through the inverter switches and not fed to the motor from the distribution transformer. In this way the VSD actually lowers the system load by canceling the reactive power from the motor. The trade-off is that the current is no longer sinusoidal, so the VSD decreases the fundamental component but increases the harmonic components. The resulting power factor may easily be higher with the VSD than for a directly line-operated motor.

The problem of harmonics in VSDs becomes increasingly severe when the size of the drivers increases. Meanwhile, harmonic behavior is varying with the operating mode. In the lift installation, for example, the situation is worst when the lift is on no-load down or on full-load up, because the motor has to do work against the counter weight. Furthermore, the non-ideality of the LV distribution system also interacts with the VSDs. In view of harmonic problems, voltage unbalance, which is caused mainly due to the uneven allocation of single-phase loads across all three phases, may make the rectifier to draw/generate third harmonic currents from the supply. And the capacitor paralleled with induction motors or other large linear loads may excite a harmonic resonance at some frequency.

b) Switched-mode power supplies (SMPS)

A switched-mode power supply, or SMPS, is an electronic power supply unit that incorporates a switching regulator — an internal control circuit that switches the load current rapidly on and off in order to stabilize the output voltage The switching regulator is used as replacements for simpler linear regulators when higher efficiency, smaller size or lighter weight is required. It provides a buffer circuit that provides power with the characteristics required by the load from a primary power source with characteristics incompatible with the load. It makes the load compatible with its power source.

SMPSs are used extensively in a wide range of building equipment, such as copiers, personal computers, printers, fax machines and other electronic devices. They generate significant harmonic currents in the distribution systems due to the large number and high density in the high-rise building. As these devices are single-phase powered they generate the odd harmonics, with the third harmonic being dominant. The current waveform of a PC and its associated printer, for example, normally has a THD of 110% and power factor (PF) of 0.66. Additionally, the harmonic currents injected into the LV distribution system are randomly in time and location.

c) Lighting installations

Fluorescent lamps are employed extensively in high-rise buildings, and create harmonic problems. Although new generations of electronic ballasts have been

developed to operate fluorescent lamps at a lower harmonic output, electromagnetic ballast is still widely applied in many existing installations. Even in some new constructions, the electromagnetic ballast occupies the large part because of the cost. In addition, the capacitor which is connected to the ballast to improve the circuit power factor may worsen the harmonic distortion. Meanwhile, the high harmonic level for a typical office lighting circuit is not only due to the non-linear characteristics itself, but also the voltage distortion thus resulted further causes more harmonic currents.

d) Other nonlinear equipment

Saturated power transformers and shunt reactors are the another class of non-linear loads. Saturated magnetic cores may generate harmonic currents during steady-state operation, as well as transient harmonic currents and temporary over-voltages following a major switching operation in the transformer's vicinity, with a critical case of energizing the transformer itself. The steady-state magnetizing currents of power transformers are only 1-2% of the rated current but they may reach 10-20 times their rated value when transformers are switched on to the system, exhibiting a current spectrum which is rich in harmonics.

The battery charge circuit is another harmonic source in the system. The individual harmonics generated by such a circuit depend on the initial battery

voltage, and the overall harmonic content produced by clusters of battery chargers on the same busbar varies according to time and involves random probability.

2.5 The Effects of Harmonics in The Systems

The harmonic currents from various sources finally merge into a rising mains circuit, which results in harmonic voltage distortion due to the non-trivial impedance of the circuit as well as the impedance of the distribution transformers. These harmonic voltage and harmonic current not only affect the equipment connected to the distribution system, but also have a negative impact on the building distribution system itself.

2.5.1 Harmonic Effects on Equipment

The effects of harmonics on equipment have been fully discussed in many papers [Ahmed E.E. etc. 2005, Suarez J.A. etc. 2005, Massey G.W. 1994, Wagner V.E. etc 1993]. It is understood that harmonics may cause unreliable operation of distribution systems, malfunction of end-user equipment, overheating of conductors, and may reduce efficiency and life expectancy of connected equipment. The following is a brief summary on the harmonic effects.

a) Distribution transformers

Harmonic currents in a distribution transformer cause an increase in copper losses and stray flux losses while harmonic voltages cause an increase in iron losses. These harmonic currents/voltages lead to a high temperature rise in the transformer, compared with purely fundamental sinusoidal current and voltage operation. Generally, the losses are proportional to square of the frequency and the voltage or current. As a result, the transformer would be de-rated if it supplies electricity to non-linear loads. K-factor transformers are designed to cope with the overheating problem caused by harmonics. The value of the factor K is determined by the formula of $K = \sum I_h^2 h^2$, where I_h is harmonic distortion of current at the order of h.

b) Electric cables

Harmonic currents in the conductors of electric cables result in more heating than that resulted from only sinusoidal currents carrying due to skin effect and proximity effect. These two effects depend on frequency as well as conductor size and space, and increase the equivalent AC resistance, which in turn leads to increased $I^2 R_{AC}$ losses.

Harmonic currents at the zero sequence are generally in phase in a three-phase four-wire circuit and thus the 3rd currents flow into the neutral conductor. It

could be possible that the neutral current exceeds the phase current. Under such a condition, the overheating in neutral conductor becomes un-negligible. In practice, over-sizing of the neutral conductor is employed to avoid the over-heating problem.

The harmonic impedance of the cables is not strictly proportional to the order of harmonic due to the skin effect and proximity effect. The detail of these effects will be explained in Chapter 4.

c) Motors and generators

Harmonic voltages or currents give rise to additional losses in stator windings, rotor circuits, and stator and rotor laminations. The losses in the stator and rotor conductors are greater than those associated with the DC resistances because of eddy currents and skin effect. Leakage fields set up by harmonic currents in the stator and rotor end-windings produce extra losses. In the case of induction motors with skewed rotors the flux changes in both stator and rotor and high frequency can produce substantial iron losses. In the case of synchronous machine, more harmonic heating losses in the rotor will be caused because pairs of stator harmonics produce the same rotor frequency. For example, harmonic pairs like the 5^{th} and the 7^{th} can create the 6^{th} harmonic current in the rotor. These extra losses make the overall machine temperature rise and local overheating.

Harmonic currents present in the stator of an AC machine produce an induction motoring action. This motoring action gives rise to shaft torques in the same direction as the harmonic field velocities so that all positive sequence harmonics will develop shat torques aiding shaft rotation whereas negative sequence harmonics will have the opposite effect. This brings undesired torque requirement to the loads.

d) Consumer equipment

- *Television receivers* Harmonics which affect the peak voltage can cause changes in TV picture size and brightness.
- *Fluorescent lighting* For electromagnetic ballasts, the capacitor for power factor correction with the inductance of the ballast and circuit may have a resonant frequency. If this corresponds to a generated harmonic, excessive heating and failure may result.
- *Computers* Computers usually require the THD of the supply voltage is less than 5% and one individual harmonic component is less than 3% of the fundamental voltage. Higher distortion values may result in mis-operation of the control equipment which in turn can lead to production and process interruption which can have high economical consequences.
- *Switch-mode power supply equipment* This equipment is often synchronizing its operation to the voltage zero crossings or to other aspects of

the voltage wave shape. Harmonic voltage distortion can lead to the shifting of the voltage zero crossing or change the point where one phase to phase voltage becomes higher than another phase to phase voltage. Both of these are important points for different kind of power electronic circuit controls. Misinterpretation of these points by the control systems can lead to the malfunction of the control system.

e) Switchgears and relaying

Excessive harmonic currents cause in switchgears additional losses leading to reduced fundamental current carrying capability. An increased temperature of insulating components results in shortening of their lifetime.

Older solid-state tripping devices on LV circuit breakers have responded to the peak currents. This type of tripping devices may cause nuisance tripping in feeders supplying non-linear loads. New tripping devices respond to the RMS values of the current.

For MCCBs containing a thermal trip element, the element may heat up more quickly at the high harmonic frequency. The breaker may be cheated by opining at an overall current well under its normal trip setting. In magnetic-trip breakers, their operation depends upon electromagnetic force. The force is proportional to the square of peak current. Hence, a high 3^{rd} harmonic current, leading to

abnormally high overall peak, could open the breaker at an overall ampere value less than its pre-set tripping point.

The response of the protective relays to the distortion depends a lot on the measuring principle used and there are no any common rules which could be used to describe what the impact of harmonics on large variety of the relays is. However, it can be said that normal harmonic distortion levels in networks do not cause problems in relay operation.

f) Power factor correction capacitors

Capacitors can dramatically change the system impedance under system resonant conditions. The reactance of a capacitor decreases with increasing frequency, and therefore, the capacitor acts as a sink for harmonic currents. This effect increases the heating and dielectric stress of its insulation material. The presence of voltage distortion produces an extra power loss in capacitors expressed by $\sum_{h=1}^{\infty} C(\tan\delta)\omega_h V_h^2$, where $\tan\delta = R/(1/\omega C)$ is the loss factor, $\omega_h = 2\pi f_h$ and V_h is the RMS voltage of the harmonic at the order of h. The increased heating and voltage stress due to harmonics result in the reduced life of the capacitors.

The major concern arising from the use of capacitors in the building distribution systems is the possibility of the system resonance. This leads to harmonic

voltages and currents that are considerably higher than they would be in the case without resonance.

2.5.2 Harmonic Resonance in Distribution Systems

In a distribution system, the response of the system is equally as important as the source harmonics. In fact, the distribution system is quite tolerant of the current injected by harmonic-producing loads unless there is some adverse interaction with the impedance of the system. The response of the distribution system at each harmonic frequency determines the true impact of the non-linear load on harmonic voltage distortion. The possible resonance in the system as well as the interference with the protection devices is discussed in this section.

a) Series resonance

A series resonant circuit is the one with a low impedance to the flow of current at the frequency of resonance when the inductive reactance is equal and opposite to the capacitive reactance. An example of a series circuit in the distribution system is the system inductance in series with the power factor correction capacitors when viewed from the side of the utility at the point of common coupling

In the resonant condition, the voltage at the point of common coupling is

multiplied by the series resonant circuit with the multiplied voltage appearing across the power factor correction capacitors. The magnitude of multiplication is determined by the circuit quality factor, which is further affected by the resistance of the circuit.

b) Parallel resonance

A parallel resonant circuit is the one with a high impedance to the flow of current at the frequency of resonance when the inductive reactance is equal and opposite to the capacitive reactance. An example of a parallel circuit in a power system is the power factor correction capacitor connected in parallel with the source when viewed from the harmonic source. If this parallel resonance frequency occurs at or near a harmonic current produced by the loads, severe voltage distortion and harmonic current amplification will result. Usually, it takes only a very small current to excite a large current that will oscillate between the energy storage of the capacitor and the energy storage of the inductance in the power system. The magnitude of this oscillating current is limited only by the resistance in the circuit. Therefore, a circuit with high quality factor will have a relatively high oscillating current. The circuit resistance or loading will limit the amplification of the parallel resonant circuit.

In fact, the increase in harmonic current is often enough to cause nuisance fuse blowing and capacitor bank failure. It is therefore important to note that the

application of capacitors to at a main LV siwthcboard will not cause amplification of harmonic currents.

2.6 Recorded Harmonic Problems in Local Buildings

Harmonic problems in high-rise commercial buildings have been reported in the past few years. The following are a few of the problems recorded.

2.6.1 Excessive Harmonic Current in A Neutral Conductor

The harmonic problem was not known until the tenant's computer installation at 15/F failed to work in a twin-office building, which is 42 storey and 46 storey high in its two towers. The affected tenants' equipment in the 42-storey tower was fed by the single-phase transformer at roof serving 42/F to 15/F. The site investigation indicated that the neutral voltage was too high at the tenant's outlets to be acceptable as compared to that measured in other office tower at that time. It was suspected first that the problem might be due to the poor cable joint and under-sizing of the neutral conductor, but soon it was proved to be irrelevant. The causes of this problem were finally identified. First, the harmonic currents from lighting loads generated an excessive harmonic voltage drop in the neutral conductor. Second, the single-phase transformers introduced a magnification effect of the 3^{rd} harmonic voltage and current in the system. As

the proposed remedial method was costly and complicated, the tenant eventually moved out.

2.6.2 Burn-out of a Capacitor Bank

The capacitor bank burnt-out incident occurred after the capacitor bank was in use for several months. As recorded, nearly all capacitors in the bank were damaged and the incident was sent to a consultant for investigation. The detail of the investigation report was not released. It just revealed that there ware some defects in the capacitor bank and harmonics were the triggering force for such a failure. The problem was finally solved after the lift company modified their lift control circuit, which was blamed for generating the harmonic current. Meanwhile, the capacitor bank was replaced by a new brand and the "reinforced type" was employed, as the typical way to tackle the burnt-out capacitor bank in Hong Kong. Although detail of the investigation report was not released, it was suspected that the capacitor bank was damaged by the harmonic over-voltage arising from the resonance.

Harmonic problems such as capacitor bank failure, conductors overheating and protective devices premature tripping, etc. were occasionally heard in Hong Kong. People here, however, hesitated to carry out detailed investigation. The following are probably the reasons:

a) The detailed investigation usually involves in shutting down of equipment and installations, which are not acceptable in office buildings;

b) The investigation usually costs a lot and takes a fairly long period, say from months to a year;

c) Most of the management staffs treat these problems as trivial and simply think the problems to be caused by poor material quality and workmanship.

On the contrary, harmonic problems in other countries, say USA and UK, etc. have long been studied and documented. Standards or recommendations are available to help suppressing harmonics in power system.

2.6.3 Harmonic Problem Associated with Distribution Transformers

Distribution transformers are usually placed at the load center in buildings in order to minimize both voltage drop and distribution losses. A three phase 1500kVA core-type transformer weighs more than 4500kg and hence poses a severe structural constraint and transportation problem when placing on the upper floor in a building. To solve the problem, the utility company usually install 3 number of single-phase transformers connected in delta-wye instead. This, however, may bring the harmonic problem into the distribution system.

In the three single-phase transformers, all transformer iron cores are

independent and offer a totally independent low-reluctance iron path for the in-phase zero sequence flux arising from triplen harmonies and unbalanced loading conditions. This low reluctance means high magnetizing shunt impedance, which is neglected in the equivalent circuit.

For the three-phase core type transformer, all zero sequence flux would join together at the yoke junction and the only return path for this flux is through the tank and air of the transformer. This obviously is a path with high reluctance, which means zero sequence magnetizing current is high and the shunt magnetizing impedance would be too low to be disregarded. Since this shunt path has a similar effect to that of a delta tertiary, the equivalent circuit of the wye-wye core type construction transformer corresponds somewhat to the configuration of a three winding transformer with wye-wye-delta connection. The delta tertiary winding can provide third harmonic magnetizing current necessary for a sinusoidal output voltage. In addition, the tertiary winding also assists in unbalanced loading conditions, since it causes the load to be distributed more evenly in the primary phases. Hence, it is not surprising that a three-phase core type transformer is superior to the 3-single phase transformers in supplying unbalanced and harmonic loads.

In practice, it is found that under the light load (l/3 full load) both the third harmonic voltage and current have more or less the same order irrespective of the type of supply transformers. The magnitude of neutral to earth voltage is

acceptable under both types of transformers. When the loading is increasing, the output from the supply transformer, which consists of three single-phase transformers, becomes worse. The output from the other type of the supply transformer is still acceptable even under the full-load conditions. This verifies that the supply transformer, which consists of three single-phase transformers with windings connected in delta-wye will have a magnification effect on the third harmonic current and voltage.

2.7 Summary

This chapter provided a whole picture of the LV distribution system in local high-rise commercial buildings. The typical features and the normal configurations of the building distribution systems were presented. Major components found in buildings were introduced briefly. A typical building LV distribution system was described.

Harmonics in commercial buildings were then identified, which included variable speed drives, switched-mode power supplies, lighting installations and other equipment such as the saturated transformers, battery charge circuits etc.. In a word, the harmonic sources in a building are large in number and small in size.

Thirdly, the negative effect of harmonics was presented. Harmonics in current and voltage not only affected the normal operation of connected equipment, but also cause harmonic resonance in the system. Three recorded cases in Hong Kong were provided to show the harmonic problems in building distribution systems.

To avoid any potential problems in distribution systems, it is necessary to address effective control of harmonics in commercial buildings.

Chapter 3

Control of Harmonics in Buildings

3.1 Introduction

As described in Chapter 2, the proliferation of electronic equipment in high-rise commercial buildings has resulted in deterioration of power quality. The distorted voltage and current (harmonics) produced undesirable effects on the equipment connected in the building distribution systems. This has brought more and more attention from utilities, building owners, tenants and manufacturers. Research on harmonic control has been conducted extensively. Some measures for preventing, limiting and mitigating harmonics have been applied in the buildings.

This chapter reviews the measures of harmonic control in the LV distribution systems of buildings. Firstly, major international and national standards on harmonics are briefly presented. Problems in regulating harmonics in commercial buildings are then addressed Active power filters, which have been proved as an effective device to alleviate harmonics in electrical systems, are reviewed. The application of the active power filters within the buildings is addressed, and the problems encountered in filter applications are identified. Other strategies of harmonic control are introduced briefly, including those

applied at both the equipment level and the system level.

3.2 Harmonic Standards

With the growth of global trade, the need for equipment manufactured in one country to comply with standards in another has prompted concerted effort in formulating international standards on harmonics. The key is to maintain a globally acceptable electromagnetic environment that co-ordinates the setting of emission and immunity limits. This is achieved by using compatibility levels. All equipment intended to operate in that environment is required to have immunity at least at the compatibility level of a disturbance. Then, a margin appropriate to the equipment concerned is normally provided between the compatibility and immunity levels.

In order to determine the proper emission limits, the concept of planning level is used in some countries. This is a locally specific level of disturbance adopted as a reference for the setting of emission limits from large installations in order to co-ordinate those limits with the limits adopted for equipment intended to be connected to the power system. The planning level is normally lower than the compatibility level. And this margin between these two levels takes into account the structure and electrical characteristics of the system, e.g. possible system resonance and an upward drift in the levels due to future loads. Also, the uncertainty about the impedance of the system and harmonic source is made allowance.

IEEE Standard 519-1992 and IEC 61000 series on harmonics are two representative standards, which were developed by IEEE and IEC, respectively. The European Union, through the Electromagnetic Compatibility directive, has sought to ensure the removal of technical barriers to trade by requiring equipment to operate satisfactorily in its specified electromagnetic environment, and by protecting the public electricity distribution form disturbances emitted by equipment through limiting these emissions. Engineering recommendation ER G5/4, then, came into force.

The international standards are generally used as a basis for global co-ordination. Consequently, an individual country or area makes the appropriate adjustment to accommodate various national priorities. In Hong Kong, the Energy Efficiency & Conservation Sub-committee of the Energy Advisory Committee sets the harmonic current limits in LV distribution systems in the Code of Practice for Energy Efficiency of Electrical Installations (COP) [Energy Advisory Committee 1998]. These limits were derived from IEEE Standard 519-1992. Table 3.1 shows the summary of these major standards on harmonics.

Table 3.1 Summary of major standards on harmonics

	Popularity	Application scope	Voltage limit	Current limit	Practice	Deficiency
IEEE Std. 519-1992	North America	Whole system	5% for THD, 3% for individual	According to I_{sc}/I_L at PCC, TDD (%)	Easy	Consider the building electrical system as one point, no voltage prediction
IEC 61000 series	Europe	Mainly on equipment	compatibility level, no planning level for LV	Less than 16A and more than 16A	Difficult	Too fussy to practice in buildings, no planning level
ER G5/4	UK	Both whole system and equipment	5% for THD, 4% for the 3^{rd}, 5^{th}, 7^{th}	IEC Std., maximum ratings, pre-calculate current	Moderate	Should be simplified
Local practice	Hong Kong	Whole system based on simple assumptions	No detailed planning level	Based on 40KA short circuit level (IEEE Std.)	Easy	Too simple to be safe

3.2.1 IEC Standards

IEC 61000 series, developed by International Electrotechnical Commission, put more emphases on harmonic emission from equipment so that the standards are considered as the equipment-level standards. The IEC standards were developed originally for some parts of Europe. These documents enforce equipment manufacturers to find cost-effective solutions to meet the standards. The

standards guarantee the equipment connected has lower harmonic emissions than the limits, and the electrical system will operate compatibly if the equipment is connected. A concise description of these documents is provided as follows.

IEC 61000-2-1 It outlines the major harmonic sources in three categories of equipment: power system equipment, industrial loads and residential loads.

IEC 61000-2-2 The compatibility levels of the harmonic and inter-harmonic voltage distortion in public low-voltage power industrial systems is discussed in this document.

IEC 61000-2-12 This document deals with compatibility levels for low-frequency conducted disturbance, in this case relating to medium voltage power supply systems. It also covers the subject of injected signals such as those used in ripple control.

IEC 61000-3-2 It contains limits for harmonic current emissions from equipment with input currents up to 16 A per phase. It also specifies the measurement circuit, supply source and testing conditions as well as the requirements for the instrumentation.

IEC 61000-3-4 It contains limits for harmonic current emissions from equipment with input currents greater than 16 A per phase.

IEC 61000-3-6 This document indicates the capability levels for harmonic voltages in low and medium voltage networks as well as planning levels for MV, HV and EHV power systems. It then makes an assessment of emission limits for distorting loads in MV and HV power systems.

IEC 61000-3-12 It provides limits for the harmonic currents produced by equipment connected to low-voltage systems with input currents up to 75 A per phase and subject to restricted connection.

IEC 61000-4-7 The subject of testing and measurement techniques are covered. It is a general guide on harmonic and inter-harmonic measurements and instrumentation for power systems and equipment connected thereto.

3.2.2 IEEE Standard 519-1992

IEEE Standard 519-1992 sets the harmonic limits at the point of common coupling (PCC). This is a system-level harmonic standard because it considers the emission of sub-systems connected at the PCC. IEEE Standard 519-1992 was developed originally for North America.

The standard provides guidelines for harmonic current limits at the PCC, which is the interface of the customer and the utility. The rationale behind the use of the PCC as the reference location is simple. It is a given fact that within a particular electric power system, harmonic currents will be generated and propagated. Harmonic current injection at the PCC determines how one user might affect other users and the utility that supplies the power. In the document, the harmonic current limits are defined according to the ratio of the maximum available short circuit current at the PCC to the maximum demand load current. As the ratio increases, the percentage of the harmonic currents that are allowed also increases. This means that larger power users are allowed to inject into the system only a minimal amount of harmonic current (as a percentage of the fundamental current). Such a scheme tends to equalize the amounts of harmonic currents from large and small users at the PCC.

IEEE Standard 519-1992 also provides guidelines for harmonic voltage levels at the PCC. Generally, limiting the voltage distortion at the PCC is the responsibility of the utility. It can be expected that the harmonic voltage level at the PCC will be within the specified limits of the standard if the harmonic current from the user's circuit complies with the limits defined in the standard. When the IEEE 519 harmonic limits are used as guidelines within a user's sub-system, the PCC is the common junction between the harmonic generating

loads and other electrical equipment in the power system.

3.2.3 Engineering Recommendation (ER) G5/4

Different from the standards mentioned previously, Engineering Recommendation (ER) G5/4 developed from ER G5/3, which took effect in 2001 in United Kingdom, presents a detailed procedure for guiding the connection of harmonic-producing equipment/installation into a utility system. [UK Electricity Association 2001] With this procedure the reliability of the system after connecting the new equipment is probably guaranteed. Three stages of harmonic assessment are adopted.

ER G5/4 sets harmonic limits for both voltage and current distortion, and regulates the harmonic levels over the whole system. The concept of planning level is used to ensure the harmonic voltage distortion below the compatibility level. For small power equipment, IEC standards are introduced whereas possible, which simplifies the assessment. For other new connections, the harmonic current limits are pre-calculated based on the proper compatible margin.

However, if the background of the system is distorted exceeding the limit, the new installation may not be allowed installed. In such cases, the background

should be improved firstly.

3.2.4 Application of Harmonics Standards/regulations in Buildings

I. Harmonic limits in buildings

There is no local standard or regulation on harmonics developed in Hong Kong. However, the Code of Practice for Energy Efficiency of Electrical Installations (CoP), developed by the Energy Efficiency & Conservation Sub-committee of the Energy Advisory Committee, recommends the harmonic current limits in LV distribution systems. Table 3.2 shows the maximum THD of current given in the CoP.

Table 3.2 Current emission limits given in the COP (%)

Load current (A)*	<40	[40, 400]	[400, 800]	[800, 2000]	>=2000
Maximum THD (%)	20	15	12	8	5

Note * Rated current at 380/220V

It is noted that Table 3.2 is simply a copy of the limits given in IEEE519-1992 on the basis of a short circuit fault level of 40kA. In fact, the fault level is not constant within a building distribution system, and much lower at the end of a sub-main circuit or feeder circuit due to system impedance. This means that the limits of harmonic current emissions in local buildings are less stringent. As this local document does not address the detailed voltage distortion limits in building distribution systems, such relaxation may cause uncontrollable (e.g.,

excessive) voltage distortion. Setting harmonic current limits only is not enough to ensure the compatibility environment in the buildings. Additionally, the lack of detailed harmonic regulation leads to ambiguous responsibility of the utility, the landlord and the tenant on harmonic control, which may give rise to the disputes among them when harmonic problems occur. Consequently, more serious harmonic pollution will occur in the distribution systems.

To apply these limits for harmonic control in the building distribution systems, two fundamental issues need to be identified, that is, the harmonic assessment and the relationship among the utility, the landlord and the tenant.

II. Harmonic assessment

In a building distribution system in Hong Kong, the utility treats the whole system as a simple node, and is concerned about harmonic currents injected into the utility network via the distribution transformer. To the landlord and the tenants in the building, the distribution system itself is not a node as the harmonic situation varies within the system. The distributed harmonic currents as well as the non-trivial impedance of the distribution circuits lead to harmonic voltage drop in the system. Harmonics may exceed the harmonic limits on the down stream circuit even if the harmonic voltage at the point of common coupling (PCC) complies with the limits. Thus, setting harmonic voltage limits equally on different floors may not be appropriate. Consequently, setting of

harmonic current limits should be made according to the features of the building distribution system.

ER G5/4 provides a good framework for harmonic assessment. It sets a three-stage procedure to assess harmonic levels for the new connection of the harmonic-producing load. The definition of the planning levels and the pre-calculated current limits ensure the studied system below the compatibility level. Also, IEC standards are adopted to limit the harmonic current emissions if possible. For small power equipment, a simple procedure or judgment such as by IEC standards is enough to determine whether the connection is acceptable, whereas for large power equipment which will lead to big disturbance on the system if connected, the necessary calculation should be conducted to predict the impact of the connection on the existing electrical system. It is indicated that ER G5/4 combines the system-level and the equipment-level features, which may be suitable to introduce into the building LV distribution systems. Therefore, by taking into account the characteristics of local building LV distribution systems, it is possible to develop a procedure to control harmonics in local high-rise buildings.

III. Responsibility of all parties in commercial buildings

Harmonics is a problem to all parties involved in power supply and power utilization in a building, i.e. the landlord, the tenant and the utility. Generally, the utility is

responsible for providing qualified power supply at the entrance of the building system while the tenants and the landlord are responsible for limiting harmonic emissions from their loads. However, it is impossible for the utility to identify and monitor all of harmonic sources in the building due to the ownership. The utility is only concerned of the harmonic level at the entrance of the building. Consequently, the customers in buildings may not be served by the qualified voltage due to the non-trivial system impedance as well as excessive harmonic current distortion. It seems to be inadequate even if a well-developed harmonic standard is applied to the building systems. The responsibility in control of harmonics should be identified.

3.3 Active Power Filter (APF)

The active power filter (APF) technology is now mature for providing compensation for harmonics, reactive power, and/or neutral current in electric systems. It has evolved in the past twenty to thirty years of development with varying configurations, control strategies, and solid-state devices. APFs are also used to eliminate voltage harmonics, to regulate terminal voltage, to suppress voltage flicker, and to improve voltage balance in three-phase systems. This wide range of objectives is achieved either individually or in combination, depending upon the requirements and control strategy and configuration which have to be selected appropriately.

One of the major factors in advancing the APF technology is the revolution of fast self-commutating solid-state devices. In the initial stages, thyristors, bipolar junction transistors (BJT's) and power MOSFET's were used for the main circuit of APFs. Later, static induction thyristors (SIT's) and gate-turn-off thyristors (GTO's) were employed to set up the APF to achieve large current rating. With the introduction of insulated gate bipolar transistors (IGBT's), the APF technology entered a real boost and, at present, they are considered as ideal solid-state devices for setting up an APF configuration because of its low gating loss, proper switching frequency and large current capability.

The signal detection is necessary and important to the control system of an APF. The improvement of sensor technology has also contributed to enhancing the performance of the APF. The availability of Hall-effect sensors and isolation amplifiers at a reasonable cost and with adequate ratings has improved the APF's performance.

The breakthrough in the microelectronics results in the great development of the APF. Starting from the use of discrete analog and digital components, the progression has been to microprocessors, microcontrollers, and digital signal processors (DSP). Nowadays by virtue of DSP technique it is possible to implement complex algorithms on-line at a reasonable cost. This development successfully improves the dynamic and steady-state performance of the APF.

With these improvements, the APF is capable of providing a fast dynamic response to the change of harmonics in the system. Moreover, it is possible to compensate quite a sum of higher order harmonics (up to the 25th).

In the following parts, the major parts of APFs including the classification, the signal detection, the derivation of the reference currents, the current regulator and the analysis methods for analyzing the performance of the APFs are reviewed. Finally the issues arising from applying the APFs in commercial buildings are discussed.

3.3.1 Classification of APFs

An APF can be classified in different ways, such as according to the type of a converter, the method of connection, the number of poles and the source of derived harmonic signals.

According to the type of a converter, an APF may be classified as the one with a current-source inverter (CSI) structure or a voltage-source inverter (VSI) structure. The current-source APF behaves like a harmonic current source, which injects pre-determined harmonic currents into the system to eliminate the harmonics in the system. Normally, a large inductor is required to be placed at the DC side. It can be drawn that such an APF has higher power losses due to

large fundamental current flowing through the main circuit. The voltage-source APF is more popular in the market since it is cheaper, lighter and expandable to multilevel structure to enhance the performance with a lower switching frequency. Generally, a capacitor is required to be placed at the DC side to form a DC voltage bus. The required harmonic currents result from the harmonic voltage applied on the output inductors.

According to the method of connection to the electrical system, an APF can be classified as a shunt APF, or a series APF or a hybrid APF. The shunt APF is easy to install as it is connected to the AC system in parallel. The shunt APF is intended to suppress harmonic current, compensate reactive power and balance unbalanced current. The series APF is generally designed to cancel harmonic voltage in the AC system or regulate the terminal voltage of the system. A matching transformer is required to implement the series connection. The hybrid APF refers to the APF with a shunt module and a series module or the APF in combination with passive filters. The former one is also called the unified power quality conditioner. Its main purpose is to provide clean power to important loads. The unified power quality conditioner suppresses harmonic voltage as well as harmonic current at the point of connection. A DC-link component, such as a large capacitor or inductor is used to store energy, which is shared by the shunt part and the series part. The expensive cost and complex control strategy are the main obstacles to apply such a hybrid APF. The latter

one may have the combination of a series active filter with a shunt passive filter or a shunt active filter with a shunt passive filter. In such an application, the passive filter is dedicated to absorb low orders of harmonics and the active filter is dedicated to mitigate high orders of harmonics. This feature can reduce the rating of the active power filter, and consequently save the cost.

According to the number of poles in the APF, an APF can be classified as a single-phase (two-pole) APF, or a three-phase (three-pole or four-pole) APF. The single-phase APF consists of a single-phase full-bridge circuit with a DC-link element used to store energy. It aims at mitigating harmonics from single-phase loads. The three-pole APF is applied in a three-phase three-wire system, and generally contains a three-phase full-bridge circuit with a DC-link component. The four-pole APF is employed in a three-phase four-wire system. There are two configurations for the forth-pole connection. In the configuration of split-capacitor that is appropriate to small rating, the fourth pole (N) is connected to the midpoint of the capacitor so that the neutral current flows through the capacitor. The control strategy for the split-capacitor configuration is more complex. In the configuration of four-pole switching, the fourth pole connected to the neutral line is considered as another phase (the fourth phase). Hence the APF with this configuration is considered as a simple extension of the three-pole APF. Although the number of self-commutating solid-state device increases the control strategy is simple compared with that in the APF with the

split-capacitor configuration.

According to the source of derived harmonic signals an APF can be either the one of current detection or the one of voltage detection The current-detection APF extracts harmonics from source current or/and load current. It constitutes a control loop between the harmonic current in the AC system and the compensating current from the APF. Such a APF is mainly applied to compensate the harmonic current produced by centralized loads. On the other hand, the voltage-detection APF forms a feedback loop between the detected harmonic voltage and the compensating current. It is suitable to apply in a distribution system to eliminate harmonic propagation. The voltage-detection technique is applied to the unified power quality conditioner as well, as it is designed to mitigate both harmonic currents and harmonic voltages at the point of connection.

3.3.2 Signal Detection

Necessary information of the mains and the APF outputs needs to be collected in order to achieve the control objectives. Normally the signals to be collected include mains voltage, load current, source current, compensating current and DC-bus voltage/current. These voltages and currents are firstly sensed by potential transformer (PT) and current transformer (CT), respectively. The

transformer outputs are then processed by signal-conditioning circuits, which are either hardware based (analog) or software based (digital). The conditioned signals are converted by ADCs (analog to digital converter) and processed by a control system. Appropriate anti-noise measures may need to be considered for avoiding noise interference.

Both the PTs and CTs play an important role in an APF. The proper specification of PTs/CTs helps not only to achieve good performance of an APF but also to reduce its cost. According to their construction these measuring transformers are classified as either magnetic transformers or hall-effect transformers. The magnetic transformers are cheaper but with a poor frequency response, especially in phase. To compensate the phase error between the primary and the secondary, some phase-correction circuits, consisting of operation amplifiers and passive elements, are integrated into the products. However, the phase compensation is made at extremely low frequency only. The frequency response is not well improved. Hall-effect transformers may be the solution. They provide good frequency response at the frequency of tens of kHz up to several hundred kHz. The precision of the hall-effect transformers is also better than that of magnetic transformers, which helps to achieve the good performance of the APF. The major disadvantage is their high cost.

3.3.3 Derivation of Reference Signals

The derivation of reference signals from the collected information (such as detected voltages and currents at the point of connection) is the essential part of an APF. The computation time, the time delay arising from signal sampling and the precision of harmonic extraction all have a significant impact on the performance of the APF, such as that of transient and steady state responses.

The derivation of reference signals are carried out either in the frequency domain or in the time domain. The derivation methods in the frequency domain generally have a good precision. In these methods the Fourier transform is applied on the distorted voltage and/or current to extract harmonic components, which serve as the reference signals. [S. Mariethoz etc. 2002, M. EI-Habrouk etc. 2001, S. Luo etc. 1991] The Fourier transformation, in fact, is to find the solution of a set of nonlinear equations, which needs a great number of computations and consequently leads to a long response time. Although the modified Fourier transform-based methods adopting the sliding window can improve the dynamic response [M. EI-Habrouk etc., 2001], one main cycle is required to track the load change completely. Therefore, it is suitable for slowly varying load conditions. Moreover, Fourier transform-based methods cannot be used to split the fundamental current up into the positive-sequence/negative-sequence components and active/reactive power components of the positive-sequence fundamental current.

The derivation methods in the time domain are based on the instantaneous calculation on detected harmonic-containing signals to extract harmonic components, and have been widely addressed. These methods include the well-known instantaneous reactive power theory, the generalized theory of the instantaneous reactive power, the synchronous reference frame method, the synchronous detection method, the flux-based controller, the notch filter method, the PI controller, the sliding mode controller, fuzzy control, the theory of instantaneous symmetrical components, the controller based on an enhanced phase-locked loop, etc.

The instantaneous reactive power theory was initialed and developed by Hirofumi Akagi *et al* [Akagi.H etc. 1984, Akagi.H etc. 1999]. It has been widely implemented in APFs for harmonics control. [Sozanski, K. etc. 2002, Young-Gook Jung etc. 1999, Mishra M.K. etc. 2000, Cardenas V. etc. 1998] The theory transforms the voltage and current signals in the a-b-c frame to the terms in the α-β frame by Clark transformation. The instantaneous active and reactive powers are computed in the α-β frame. Harmonic active and reactive powers are extracted from the total instantaneous active and reactive powers computed by virtue of a low-pass filter or a high-pass filter. The reverse Clark transformation is adopted to convert harmonic active and reactive powers in the α-β frame into the reference signals in terms of voltage or current in the a-b-c frame.

The control methods reported in [Mahesh K. Mishra etc. 2001] were derived from the generalized theory of the instantaneous reactive power, which was formulated and proposed by Peng *et al.* [F. Z. Peng etc. 1996, Fang Zheng Peng etc. 1998] The generalized theory of instantaneous reactive power for three-phase power systems gives a generalized definition of instantaneous reactive power, which is valid for sinusoidal or non-sinusoidal, balanced or unbalanced, three-phase power systems with or without zero- sequence currents and/or voltages.

In the synchronous reference frame method [You Xiaojie etc. 2003] and Flux-based controller [S. Bhattacharya etc. 1996], the voltage and current signals are transformed into the terms in the synchronous rotating frame. In this frame, the fundamental component is shifted to DC component. By using a low-pass filter or a high-pass filter harmonic components are extracted, which are used to calculate the reference signals. In a notch-filter method [Rastogi M. etc. 1995, Quinn C.A. etc. 1992], harmonic components are obtained by the notch filter on the distorted voltage or current to remove the fundamental component. That the derived components have magnitude and phase error is the disadvantage of this technique.

In the PI controller [Wu J. C. 1996, Joos G. etc. 2000, Jou H.-L. 1995, Torrey

D.A. etc. 1995], the fuzzy control method [Singh B.N. etc. 1998, Hamadi A. etc. 2004] and the sliding mode controller [Torrey D.A. etc. 1995, Bor-Ren Lin etc. 2001, Mendalek N. etc. 2002], the close loop of DC bus is executed to maintain the DC-bus level to the desired value. The output of the controllers is then the magnitude of the desired supply current, from which the load current is subtracted, and consequently the reference signal is derived.

In the controllers based on synchronous detection method [Chin Lin Chen etc. 1994, Young-Gook Jung etc. 2003], the relationship of per-phase voltage and current is determined, and the reference signals to be added back to the AC network are determined based on three approaches (a) that each phase shares equal real power of total demand, (b) that each line carries equal line current, and (c) that each phase possesses equal load resistance, viewing from source-side after compensation. It provides the capability to balance line currents and voltages, achieves unit power factor, and eliminates harmonic currents in the load-side. The control algorithm proposed in [A. Ghosh etc. 2000] is based on the theory of instantaneous symmetrical components to generate instantaneous reference current waveforms to balance a given load. In [Karimi-Ghartemani M. etc. 2005], the controller based on an enhanced phase-locked loop is developed to extract the amplitude, phase angle and frequency of the fundamental component of the distorted input signals. All these methods make it possible and flexible to apply APF to various conditions

of AC systems.

3.3.4 Current Regulators

With advance of converter/inverter technology, the current control techniques for APFs have also been extensively studied. The current controller of an APF is designed to force the output of the APF infinitely close to the reference signals computed by the derivation method. However, the harmonic currents to be compensated may be time varying, and are generally unpredictable. Hence, good tracking of the reference signals has to be ensured. The gating signals to the solid-state devices of APF, consequently, are generated to achieve the desired output. Some techniques provide satisfactory performance in the applications, such as hysteresis control, deadbeat control, PI control, etc.. In some control methods, the output of the controller is not exactly the gating signals. PWM technique, such as space vector modulation method and carrier-based PWM, would be required to convert these commands in terms of voltage or current into the gating signals.

The hysteresis current control is a simple and extremely robust control technique. It forms an instantaneous feedback loop, which detects the current error between the compensating current and calculated reference current, and directly produces the gating signals to the devices of APF by hysteresis window.

It provides a wide-band control to meet the requirement of fast transients and high current-harmonic content with high accuracy and unconditioned stability. The basic hysteresis technique is affected by the drawbacks of a variable switching frequency and of a heavy interference among the phases in the case of a three-phase system with insulated neutral. Further development has been done to overcome the original inconveniences and improve the performance of the control system. The problem of interference among the phases has been solved in [L. Malesani etc. 1990]. Fixed modulation frequency has been achieved by a variable width of the hysteresis band as function of the instantaneous output voltage [L. Malesani etc. 1990, Q. Yao etc. 1993]. This is achieved either by means of a phase-locked loop (PLL) control or by a feed-forward action operating on the control thresholds [L. Malesani etc. 1995, L. Sonaglioni 1995, Malesani L. etc. 1997].

Another well-known current control technique is the deadbeat control [Nishida K. etc. 2002, Hosseini S.H. etc. 1998, S. Buso etc. 1997], which has the advantage of being suitable for a fully digital implementation. The calculation of this algorithm is normally implemented in the α-β frame. A space vector modulation technique, which also suits for digital realization, is often applied to generate the gating signals. The advantage of the deadbeat technique is that it may not need to measure the line voltage for computing the reference signals. This is because the algorithm may have an estimation of the line voltage

instantaneous value, which can also be used for the current reference generation. The deadbeat controller, however, is limited in its performance by the time delay. Over-sampling and executing the control routines twice in a modulation period are considered to less the sensitivity of time delay of the digital controller. [D. G. Holmes etc. 1996] As a result, such delay in current reference tracking can be reduced to a single modulation period. By adopting a prediction technique for the current reference the time delay can be further compensated. In [Hamasaki S. etc. 2003], an observer-based state estimation is used in the deadbeat control for compensation of the calculation time delay. In [Nishida K. etc. 2004], an advanced deadbeat control method using an adaptive line enhancer for a single-phase voltage-source APF is introduced. To cancel both one sampling period delay and the delay in the DSP control strategy, the desired APF compensating current of two sampling periods ahead has to be predicted. Accordingly, the settling time is reduced in the transient state.

The error between the reference current and APF output current is processed by a proportional integral (PI) regulator to generate the voltage reference for PWM modulation. This is called the linear current controller. Although the analog implementation of this controller ensures the system has a fast response, rather unsatisfactory performance is of concerns due to the bandwidth limitation of the regulator and a poor rejection of the disturbances caused by the line voltage at the fundamental frequency. The digitalization of the linear current control in the

synchronous reference frame results in the rejection of this disturbance much more effective because the fundamental line voltage is seen as a constant quantity. The bandwidth limitation of the PI regulator, however, still implies significant errors in the tracking of the high order harmonics. The application of the input passive filters is a solution to eliminate higher order harmonics but the large space requirement for the passive filter may be a problem.

3.3.5 Methods for Performance Analysis

The transfer-function method based on Laplace transformation has been reported in literature [Fang Zheng Peng 1998, H.-H. Kuo etc. 2001, Burgos R.P. etc. 1998, Graovac D. etc. 2001, Phipps J.K. 1997] to analyze the continuous system characteristics including the system stability and concerned performance. Transfer functions in the s-domain are employed to analyze the characteristics of the concerned system. For some current regulators such as deadbeat or predictive method, the implementation in the discrete time domain is applied. The analysis of the performance of the system is based on the z-domain. [G. –K. Hung etc. 2001, Luigi Malesani etc 1999]

As a useful alternative approach, the digital simulation method has been extensively applied to verify theoretical prediction because of the effectiveness

and the easiness in APF implementation. This method can provide the creditable results not only of the system but also of the specific parts.

The method based on the time-domain [Hongyu Li etc. 2005, Gawlik W.H.M. 2003], which presents clear physical interpretation, is widely adopted in many cases. The time-domain method is used to investigate the transient performance and step response and others of an APF. The disadvantage of this method is that the computation is expensive. In addition it can not reveal the frequency response of the studied system.

3.3.6 Application of APFs in High-rise Buildings

Studies have been extensively conducted to find the solutions of harmonic mitigation in high-rise buildings. An active power filter is an effective solution to the harmonic pollution in high-rise buildings. It has been proven having best performance in eliminating, absorbing or blocking harmonics and dynamic response to the harmonics in the system. With the development of power electronics and micro-electronics technologies, the cost of APFs is decreasing while their capacity is increasing. These accelerate the application of APFs in the buildings to alleviate the harmonic pollution.

It was discussed that it is necessary to maintain voltage quality on the system,

and to limit harmonic current injected into the utility network in the meanwhile. The harmonic voltage distortion in the distribution system of buildings in fact results from the harmonic currents as well as the harmonic impedance of the system. Therefore, it may be concluded that the harmonic currents flowing through the distribution circuits are the main problem in high-rise buildings. The mitigation of the currents in the distribution circuits may make it possible to control the harmonic current injection to the utility and to reduce the harmonic voltage distortion presented to the tenant.

In order to limit the harmonic current injected into the utility network, it is quite nature to install a shunt APF at the main LV switchboard. This APF measures the total harmonic current from all the loads connected to this system, and generated compensating current to suppress the harmonic current into the utility network. This is a global compensation. Because of the large demand on electricity in the building, the total current at the main LV switchboard can be as high as 3000A. For this reason the series APF is seldom installed in buildings. Moreover, the harmonic voltage distortion along the distribution circuit is mainly because of the harmonic currents as well as the impedance, which is not a harmonic voltage source. Therefore the shunt APF is more suitable to the building LV distribution systems.

The harmonic detection methods have much influence on the control strategy and filtering performance of the shunt APF (SAPF). As described before, for the SAPF, there are normally three kinds of harmonic detection methods, that is, load current detection, supply current detection and voltage detection at the installation point. Load current detection and supply current detection are suitable for shunt active filter installed at the vicinity of one harmonic-producing load or a group of harmonic-producing loads. Voltage detection is suitable for the shunt device of the unified power quality conditioner. It is also suitable to install on the long feeder distribution systems to eliminate harmonic propagation. [Hirofumi Akagi etc. 1999, and Keiji Wada etc. 2002] An active filter based on voltage detection acts as the impedance with the low resistance for the harmonic frequencies while for the fundamental frequency infinite impedance is presented. This feature may result in a low harmonic voltage distortion at the installation point of the SAPF, which also may reduce the whole harmonic voltage distortion along the riser.

Moreover, for the case of harmonic elimination in a long distribution circuit, the voltage detection method is more preferable because the harmonic current sources locate both the upstream and/or the downstream of the installation point of the SAPF. The influence or the compensation of the SAPF based on current detection is limited within the branches adjacent to the installation point of the SAPF. However, for the voltage detection method, this is not a problem because

the harmonic voltage distortion along the riser is an accumulated result. The compensating currents will always output if there is excessive harmonic voltage existing so that it is possible to mitigate harmonic currents along the distribution circuit. This also provides the voltage-detection-based SAPF with the system-level feature. Therefore, to install the SAPF based on voltage detection on the riser may be a solution to harmonic control over the building LV distribution system. And actually the harmonic voltage control is considered as the target and achieved by the mitigation of the harmonic currents flowing through the distribution circuit.

It is a common practice to install harmonic mitigation device at the entrance of the building LV distribution system. This is for avoiding excessive harmonic currents flowing into the utility side. However, it is not helpful to reduce the harmonic voltage drop along the riser and reduce the harmonic currents flowing through the building. In some cases, the SAPF is installed at the connection point of the specific loads to guarantee the pure current injected into the source side or the qualified voltage to the loads. However, it is impossible to identify all harmonic sources in buildings. The end of the riser may be a solution to the location of the SAPF based on voltage detection. It was reported that to install the SAPF based on voltage detection at the end of the feeder may eliminate harmonic propagation. [Hirofumi Akagi etc. 1999] Moreover, the harmonic voltage at the end of the riser is the most severe. The application of the SAPF

may effectively reduce the harmonic voltage distortion along the riser. Additionally, the method of voltage detection may be the most suitable solution for the SAPF if installed at the end.

3.4 Other Strategies for Harmonic Limit Compliance

There are various techniques for improving power quality in building distribution systems. These measures may be categorized into the equipment-level measures and the system-level measures

3.4.1 Equipment-level Measures

Most mitigation techniques at the equipment level are intended to make the input current more continuous so as to reduce the harmonic current distortion in the input circuit of the equipment. They include multilevel techniques for converters, line reactors, DC link chokes, zig-zag transformers, delta/wye connection for the harmonic-producing loads etc..

The multilevel techniques were developed with the booming of the power electronics. Six-pulse rectification is obtained from three-phase two-way configurations. The term of six-pulse comes from the waveform of DC voltage, which has six pluses in one cycle compared with three pulses in the one-way

converter. In general, the more pulses the DC voltage has, the waveform of input AC current is more close to the sinusoidal waveform. Consequently, the harmonic contents will be less. The twelve-pulse converter can be implemented by using one wye/wye connected transformer and one delta/wye connected transformer. It is known that the phase shift caused by the different connection is 30 degrees.

Line reactors offer significant magnitudes of inductance which can alter the way that current is drawn by a non-linear load such as an input rectifier bridge. The reactor makes the current waveform less discontinuous resulting in lower current harmonics. Since the reactor impedance increases with frequency, it offers large impedance to the flow of higher order harmonic currents.

The DC link choke electrically presents after the diode rectifier bridge and before the DC bus capacitor. The DC link choke performs very similar to the three-phase line impedance. The ripple frequency that the DC link choke has to handle is six times the input ac frequency for a six-pulse variable speed drive. However, the magnitude of the input ripple current is small. The DC link choke is less expensive and smaller than a 3-phase line reactor. However, the effective impedance offered by a DC link choke is only half its numerical impedance value when referred to the ac side.

Zig-zag transformers and delta/wye connection for the harmonic-producing loads are both for the mitigation of zero-sequence harmonics. A zig-zag transformer consists of 6 identical windings, two per phase, connected such as that the winding vectors “zig” and “zag” from neutral to earth line. With this arrangement, the triple-n harmonics are diverted from the neutral to the phase conductors like a triple-n harmonic filter. When the load current contains triple-n harmonics, the input line current contains only the unbalanced triple-n harmonics. Similarly, the delta/wye connection for the harmonic-producing loads can also cancel the balanced triple-n harmonics. Since there is no neutral conductor in the delta-connected system, the balanced triple-n harmonic current is not allowed to flow in the system.

3.4.2 System-level Measures

The system-level measures refer to those applied on the distribution system for global control of harmonics. These measures may be the most cost-effective measures in solving harmonic problems in buildings. With these strategies, the harmonic compliance in large buildings would be possible and the harmonic alleviation may be achieved at the design stage.

The passive filter is one of the simple methods for harmonic control as well power factor correction improvement, which is achieved by adding tuned series

reactors in the capacitor banks. This prevents magnification of any characteristic harmonic components from the harmonic-producing loads. The tuned frequency for the series reactor/capacitor combination is selected somewhere below the harmonic frequency of interest (e.g. 4.7 for the 5^{th} order) to prevent a parallel resonance at any characteristic harmonic. However, this approach has the disadvantages such as the bulky setup, less orders of harmonics filtered, unchangeable response to variable harmonics from systems, and the risk of harmonic resonance etc..

The end-user equipment in buildings generates currents that contain rich harmonics. Such currents propagate towards the utility network from the equipment, and result in additional voltage along the transformer, feeder and rising mains circuits, and final circuits. Harmonic voltage is developed in the distribution system of buildings as the harmonic current. As the harmonic voltage in the distribution system is greatly affected by impedance of system components, it would be necessary to select appropriate electrical components for the system. In Hong Kong, the backbone of a distribution system, that is, feeder and rising main circuits is made by busducts, busbar trunking systems and cables. For fixed current rating the busduct has the least impedance because of its compact structure, while the busbar trunking system has the most impedance. Electric cables are the most common type of conductors used in buildings due to the low cost or small space required. The impedance of electric

cables is much affected by the cable type, the installation environment and the arrangement formation. Appropriate selection of the cables helps to reduce the impedance of the system, and then to alleviate the harmonic voltage along the distribution system. The harmonic voltage can be reduced further if the distribution circuits, such as feeder and rising mains circuits are made short. This measure can be implemented by locating the distribution transformers on the upper floor close to load centers of the building.

The appropriate arrangement of the harmonic-producing equipment in a building is another important measure to prevent excessive harmonic pollution in the building distribution system. As there is a large amount of single-phase harmonic-generating loads in the building, these harmonic-producing loads should be allocated evenly in three phases. The three-phase even allocation may reduce the harmonic current flowing into the neutral conductor as well as the phase conductors. It was demonstrated in [Y. Du etc. 1998a] that grouping dissimilar loads may reduce the harmonic current. This is due to cancellation of harmonic currents arising from diversified phase angles. Further more, mixing non-linear loads with linear loads can be considered if the limit of harmonic current distortion in percentage is of concern.

3.5 Summary

This chapter reviewed two issues related to harmonic control in high-rise buildings, that is, harmonic regulation in building distribution systems and mitigation for harmonic limit compliance.

As there is no detailed harmonic regulation for high-rise commercial buildings in Hong Kong, it is difficult to manage harmonics in buildings effectively and to respond to harmonic disputes quickly. ER G5/4 provided a good framework for harmonic assessment in electrical systems, which was introduced to manage harmonics in high-rise commercial buildings.

The mitigation measures for harmonic limit compliance were reviewed. The technology of APFs was introduced briefly. The SAPF based on voltage detection may be suitable for the building distribution system. They may be installed at the end of distribution circuits, which make it possible to control harmonics in the building. Other strategies for harmonic alleviation were then presented, such as the passive filters, the multilevel technique of converters, the line reactors, the DC link chokes, the zig-zag transformers, the delta/wye connection for the harmonic-producing loads etc.. In addition, the appropriate arrangement of the loads or the reduction of the harmonic impedance of the distribution circuits may help to alleviate harmonics problems in buildings.

Chapter 4

Harmonic Characteristics of Electric Cables

4.1 Introduction

Electric cables are one of major components in power distribution systems in buildings. Harmonic impedance of these cables is the essential parameter in system design and analysis. Such impedance is used to set up the model of the system, to evaluate harmonic distortion levels, to design filtering devices, to assess harmonic limits, and so forth. [IEC 1996a, IEEE 1992, G.J. Wakileh 2001, Y. Du etc. 1998b] It is also required in the energy-efficiency code published by the Hong Kong government. [Energy Advisory Committee 1998]

Traditionally, electric cables in a three-phase distribution circuit are modelled by average resistance and effective reactance at 50Hz under balanced current conditions. Such impedance data for the cables manufactured to British Standards are available in BS 7671 [BSI 1992], which are tabulated against conductor material, insulation material, conductor size, and installation method. With the lack of harmonic impedance information, the data at 50Hz are often used to deduce cable impedance at harmonic frequencies. It is often assumed that cable inductance is frequency-variant, and cable resistance is proportional to the skin factor if frequency is of concern. However, it was found that the

resistance and reactance differ significantly from the actual data at harmonic frequencies, and even at 50Hz in some cases. The inductance of some system components is frequency-variant. Furthermore, these tabulated data are not applicable if the harmonic current is not symmetrical, or when the cable system is not fully transposed.

This chapter investigated the harmonic impedance of electric cables using an experimental approach. An impedance database was built for commonly-used single-core and multi-core armored cables with the cross-section areas of 95mm^2, 120mm^2, 150mm^2, 185mm^2, 240mm^2, 300mm^2, 400mm^2 and 630mm^2. The impact of the cable types, the arrangement formation or the setup environment on the harmonic impedance was revealed as well. Those results and conclusions are helpful in the design of wiring systems in buildings so as to prevent the harmonic propagation effectively. Those results are also useful in conducting harmonic assessment for harmonic management in high-rise buildings.

4.2 Multi-core Armored Cables

There are various types of cables used for power distribution in high-rise commercial buildings. However, XLPE insulated cables with stranded copper conductors to BS/IEC standards are widely used in Hong Kong. In these cables,

the copper strands are built up from a number of wires with the diameter of a few millimetres [H. Yang etc. 1996]. Usually they have 0 or 1 wire placed in the conductor axis, and followed by 6 wires in the next layer, then 12 wires, 18 wires, and so on [H. Yang etc. 1996], as illustrated in Figure 4.1. The stranded conductors are covered by insulation material, and continuously rotated along the cable axis. The cable conductors are enclosed by a layer of steel wires if it is an armored multi-core cable. In the consideration of eddy-current losses, single-core cables are not equipped with a magnetic armoring.

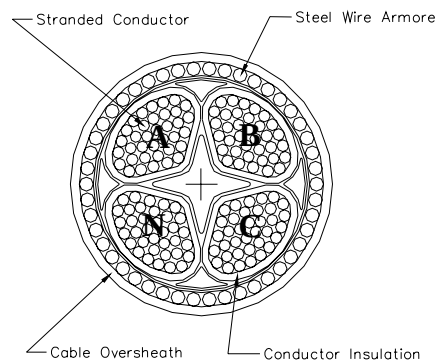

Figure 4.1 Cross section of a multi-core armored cable with stranded conductors

As these cables have a complicated conductor structure, it is very difficult to derive analytical formulas for cable impedance. Accordingly, experimental methods were employed to reveal cable impedance at harmonic frequencies. In the experimental, 600/1000V, 4/c XLPE-insulated steel-wire-armored (SWA) cables were selected as the samples because these types of cables are frequently used in buildings. Sample cables with cross-section areas of 95mm^2, 150mm^2, 150mm2, 185mm^2, 240mm^2, 300mm^2 and 400mm^2 were tested and phase impedance matrices up to the 49th order were obtained.

4.2.1 Experimental Setup for Multi-core Armor Cables

The cables under test have four core conductors, which are denoted as Phase A (or R, r), B (or Y, y), C (or B, b) and N (or n). A phase impedance matrix $\mathbf{Z_h}(h$ = 1, 3, 5, …) is necessary to characterize such cables at a harmonic frequency, as given by,

$$\mathbf{Z_h} = \begin{bmatrix} Z_{aa,h} & Z_{ab,h} & Z_{ac,h} \\ Z_{ba,h} & Z_{bb,h} & Z_{bc,h} \\ Z_{ca,h} & Z_{cb,h} & Z_{cc,h} \end{bmatrix} \tag{4.1}$$

The elements of the impedance matrix are determined experimentally using a current-injection method. Figure 4.2 illustrates the measurement of 4/c cable impedance using the method of single-phase current injection

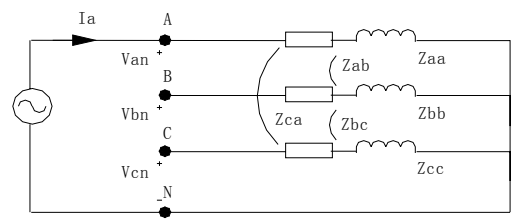

Figure 4.2 Measurement of harmonic impedance using single-phase current injection methods

During the experiment, a single-phase harmonic current is injected into the Phase A conductor. Voltages and currents on the cable are then recorded. By applying the Fourier transform harmonic voltages $V_{h,an}$, $V_{h,bn}$, $V_{h,cn}$ and current $I_{h,a}$ at order h are obtained. Self and mutual impedances at order h for Phase A are calculated using the following equations:

$$Z_{aa,h} = V_{an,h} / I_{a,h}\big|_{I_{b,h}=I_{c,h}=0} \tag{4.2a}$$

$$Z_{ab,h} = V_{bn,h} / I_{a,h}\big|_{I_{b,h}=I_{c,h}=0} \tag{4.2b}$$

$$Z_{ac,h} = V_{cn,h} / I_{a,h}\big|_{I_{b,h}=I_{c,h}=0} \tag{4.2c}$$

The same procedure is applied to both Phases B and C, other elements of the impedance matrix are obtained.

Figure 4.3 shows the experimental setup for measuring cable impedance in the laboratory. It was connected to a current injection set at one end, and shorted at the other end. The current injection set consisted of three Y-connected step-down transformers, three linear power amplifiers and one signal generator. As illustrated in Figure 4.3, the harmonic voltage was obtained from the linear power amplifier and converted into the testing current using the step-down transformer. The magnitude and phase angle of the harmonic voltage or current were controlled by the signal generator. The signal generator is capable of generating signals containing either a single AC component or multiple components at different harmonic frequencies. The sample cables under test were normally more than 10 meters long.

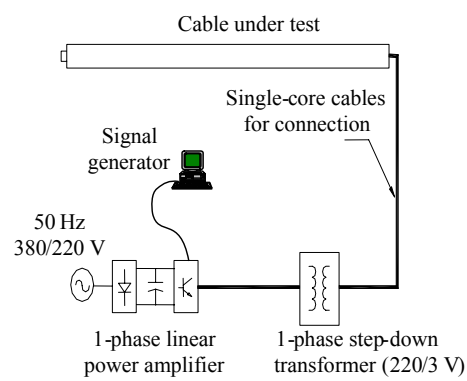

Figure 4.3 Experimental setup for measuring cable impedance

A PM3000A power analyzer together with three current transforms (CTs) was employed to measure voltage, current and power on the tested cable. The analyzer has 12 voltage ranges from 0.5V to 2000V (peak), and is capable of measuring small cable voltage, which was in the range of 0.3-1 volts in most of the cases. This instrument had a basic accuracy of 0.1% under the condition of full analyzer ranges. The CTs had a magnitude accuracy of 0.2%, and a phase accuracy of 0.3° in the frequency range of 5 Hz – 2.5 kHz.

The method of single-phase current injection was employed in the measurement. It was noted in an IEC standard [IEC 1993] that the compatibility levels of harmonic voltage were specified for orders up to 49. The current injected into the tested cable, then, contained either an AC component at 50Hz or its harmonic component at an order up to 49. The magnitude of the injected current was determined by the output voltage of the power amplifier, which remained unchanged in the measurement of harmonic impedance at all orders. The magnitude of the output voltage was selected in such a way that the fundamental current was equal to 50% of the cable rating. The magnitude of the injected current, therefore, decayed with the inverse of harmonic order.

4.2.2 Measurement Results

I. Phase impedance matrices

Full impedance matrices of the sample cables at the orders of up to 49 were obtained through the measurement. For illustration, impedance matrices of two cables at two different frequencies are presented in Table 4.1.

It is noted from Figure 4.1 that the conductors of phases A and C are symmetrical with respect to the conductor of phase B or phase N. Therefore, the following impedance formulas are obtained,

$$\begin{aligned} Z_{aa,h} &= Z_{cc,h} \\ Z_{ab,h} &= Z_{cb,h} \end{aligned} \tag{4.3}$$

It is noted again that voltage $V_{an,h}$ is equal to voltage $V_{ac,h}$ plus voltage $V_{cn,h}$ when an exciting current is injected into the phases A and N conductors. Because of the symmetrical structure of the cable voltage $V_{ac,h}$ is the same as voltage $V_{bn,h}$. The following impedance formulas yield:

$$\begin{aligned} Z_{aa,h} &= Z_{ba,h} + Z_{ca,h} \\ Z_{cc,h} &= Z_{ac,h} + Z_{bc,h} \end{aligned} \tag{4.4}$$

Table 4.1 Impedance matrices at two frequencies (20^{o}C)

CSA (mm^2)	Order h	$\mathbf{Z}_h$ (mΩ/m)		
95	3	0.4396+j0.4534	0.2348+j0.3126	0.2039+j0.1440
		0.2348+j0.3126	0.4698+j0.6265	0.2342+j0.3124
		0.2039+j0.1440	0.2342+j0.3124	0.4398+j0.4580
300	49	0.8035+3.5619	0.5100+j2.2973	0.2913+j1.2517
		0.5100+j2.2973	1.0297+j4.5931	0.5153+j2.2980
		0.2913+j1.2517	0.5153+j2.2980	0.8197+j3.5556

These formulas were verified with the measurement data. According to Table 4.1 the errors of using (4.3) and (4.4) for impedance calculation are generally less than 1%. These errors were mainly the measurement errors, such as those caused by the measuring instruments. It is also found in the table that mutual impedance between any two adjacent phases is approximately equal to 50% of the self impedance of phase B, that is,

$$Z_{ab,h} = Z_{bc,h} = \frac{1}{2} Z_{bb,h} \tag{4.5}$$

Thus, a phase impedance matrix for a 4/c cable contains two independent elements only, that is, $Z_{aa,h}$ and $Z_{bb,h}$. Other elements in the matrix can be derived from these two elements. A full impedance matrix at order *h* is, then, expressed by

$$\mathbf{Z}_h = \begin{bmatrix} Z_{aa,h} & 0.5Z_{bb,h} & Z_{aa,h} - 0.5Z_{bb,h} \\ 0.5Z_{bb,h} & Z_{bb,h} & 0.5Z_{bb,h} \\ Z_{aa,h} - 0.5Z_{bb,h} & 0.5Z_{bb,h} & Z_{aa,h} \end{bmatrix} \tag{4.6}$$

With (4.6) the positive, negative and zero impedances $Z_{1,h}$, $Z_{2,h}$ and $Z_{0,h}$ were derived, as follows:

$$\begin{aligned} Z_{1,h} = Z_{2,h} &= \frac{2Z_{aa,h} + Z_{bb,h}}{6} \\ Z_{0,h} &= \frac{2Z_{aa,h} + Z_{bb,h}}{6} \cdot 4 \end{aligned} \tag{4.7}$$

It is noted from (4.7) that the positive or negative sequence impedance is equal to 25% of the zero sequence impedance for all tested cables at the order of up to 49.

II. Harmonic Resistance

Figure 4.4 shows the values of resistance ratios against harmonic order for 95mm^2 and 300mm^2 cables. They are the cable resistances $R_{aa,h}$ and $R_{bb,h}$ normalized with the corresponding DC resistance. It was noted that the resistance ratios increased as the harmonic order or the cable size increased. The resistant ratio $R_{bb,h}/R_{dc}$ for these cables reached 5.4 and 8.5 at order 49, respectively. The increase of cable resistance is due to the skin and proximity effects of the cable conductors, as well as to eddy current losses within the steel wire armor.

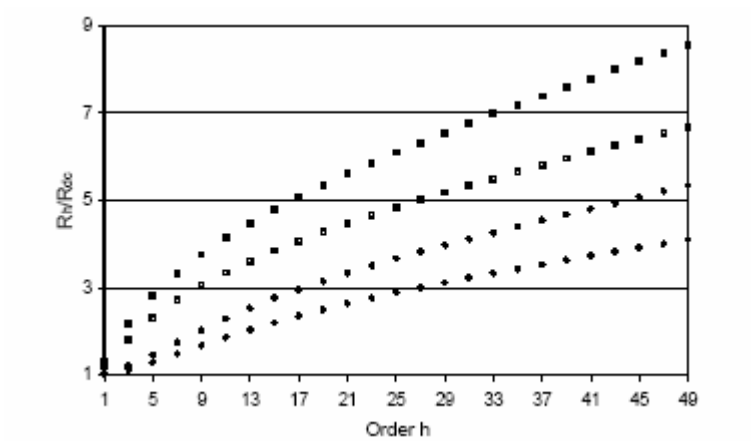

Figure 4.4 Resistance ratio of two 4/c armored cables
□ and ■ $R_{aa,h}$, $R_{bb,h}$ of the 300mm^2 cable
○ and ● $R_{aa,h}$, $R_{bb,h}$ of the 95mm^2 cable

III. Harmonic Inductance

Figure 4.5 shows the values of inductance ratios $L_{aa,h}/L_{aa,1}$ and $L_{bb,h}/L_{bb,1}$ against harmonic order for 95mm^2 and 300mm^2 cables. Because of the difficulty in obtaining the DC inductance, the corresponding inductances at 50Hz were selected as the reference. It was noted that cable inductance declined with

harmonic order, and could be lower than 50% of its 50Hz value at order 49.

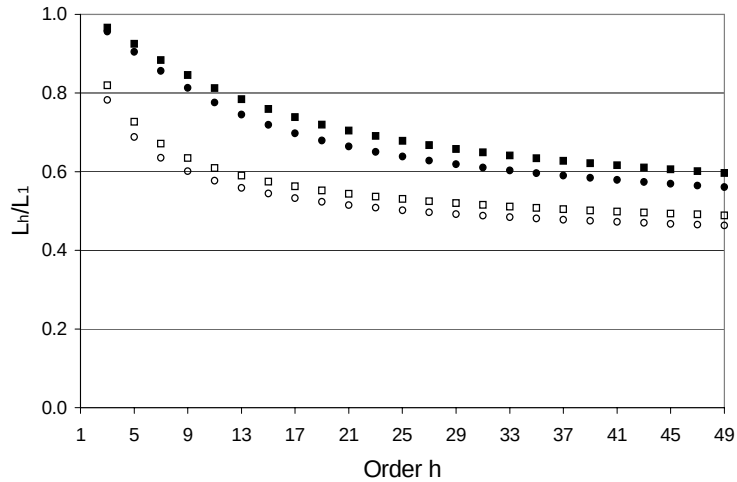

Figure 4.5 Positive-sequence inductance of two 4/c armored cables
□ and ■ $L_{aa,h}$ and $L_{bb,h}$ of the 300mm^2 cable
○ and ● $L_{aa,h}$ and $L_{bb,h}$ of the 95mm^2 cable

Cable inductance is comprised of the internal inductance of stranded conductors and the external inductance between these conductors. Because of the compact structure of the cable, internal inductance becomes a non-trivial component. It is greatly affected by current distribution within the conductors. At harmonic frequencies the current tends to flow along the conductor surface because of skin and proximity effects. The internal inductance accordingly becomes smaller than that at 50Hz. The external inductance is determined by conductor spacing and diameter. It is, however, affected by induced current generated in conductors nearby, such as the neutral conductor and steel wires. The induced current tends to generate a magnetic field in the opposite direction. The resultant flux linked to the conductors is reduced, subsequently the external inductance of the cable.

It was found that cable inductance was frequency-dependent. Both the skin and proximity effects of cable conductors yield a decline in internal inductance against frequency. However, the induced current in conductors nearby results in a decline in external inductance. A decline of 50% in cable inductance was observed in large-size cables. The declining rate is generally greater at lower orders and becomes very much lower at higher orders.

4.2.3 Empirical Formulas

It was noted that the resistance ratios increased with cable size or inverse of cable resistance. The ratios were then plotted against harmonic order normalized with DC resistance, that is, $X = 8\pi h f_1 \times 10^{-7} / R_{dc}$, where f_1 is the fundamental frequency. Figure 4.6 shows the values of the resistance ratios $R_{aa,h}/R_{dc}$ and $R_{bb,h}/R_{dc}$ against normalized harmonic order X for all tested cables from the first order to the forty-ninth order. It was interesting to note that the points for $R_{aa,h}/R_{dc}$ or $R_{bb,h}/R_{dc}$ fell in a narrow band. Empirical formula of the resistance ratios against the normalized harmonic order X were then derived by using curve fitting techniques, as follows:

$$\frac{R_{aa,h}}{R_{dc}} = \frac{1.126 + 1.253X + 0.3617X^2}{1 + 1.577X + 0.05544X^2 - 0.0001640X^3} \tag{4.8a}$$

$$\frac{R_{aa,h}}{R_{dc}} = \frac{0.8688 + 0.7677X + 0.1971X^2}{1 + 0.6917X + 0.02355X^2 - 6.9623\times10^{-5}X^3} \tag{4.8b}$$

An error band of ±5% was also plotted for each ratio curve in Figure 4.6. The

average values of the absolute error for $R_{aa,h}$ and $R_{bb,h}$ were 1.7% and 2.2%, respectively, and the highest value was 6.5%. The values of the DC resistance for 4/c cables have been tabularized in an IEC standard [IEC 1993], and are presented in Table 4.2.

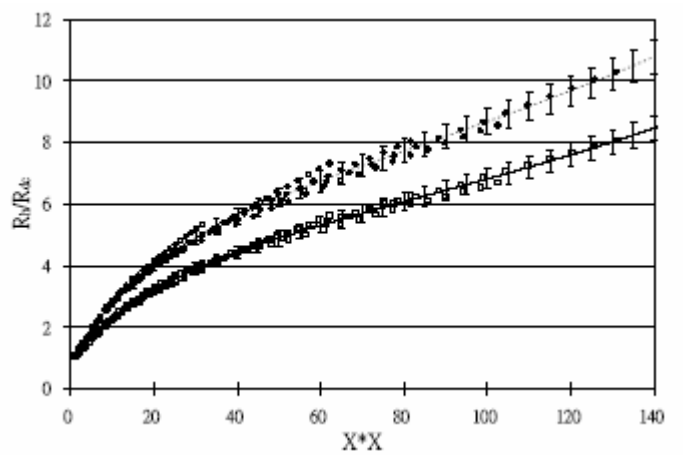

Figure 4.6 Resistance ratios for all 4/c armored cables

☐ and ○ Measured values of $R_{aa,h}/R_{dc}$ and $R_{bb,h}/R_{dc}$

— and --- Empirical formula of $R_{aa,h}/R_{dc}$ and $R_{bb,h}/R_{dc}$

Similar to cable resistance, the derivation of empirical formulas for cable inductance was attempted. The inductance ratios $L_{aa,h}/L_{aa,1}$ and $L_{bb,h}/L_{bb,1}$ were again plotted against the normalized harmonic order, $X = 8\pi h f_1 \times 10^{-7}/R_{dc}$. For illustration only the values of the inductance ratio $L_{aa,h}/L_{aa,1}$ for all tested cables are shown in Figure 4.7. Two empirical formulas were then derived as follows:

$$\frac{L_{aa,h}}{L_{aa,1}} = \frac{1.105 + 0.06831X + 0.0005560X^2}{1 + 0.1351X + 0.001215X^2} \tag{4.9a}$$

$$\frac{L_{aa,h}}{L_{aa,1}} = \frac{1.134 + 0.07301X}{1 + 0.1639X} \tag{4.9b}$$

Table 4.2 Reference values of resistance and inductance (20°C)

CSA (mm2)	R_{dc} (uΩ)	$L_{aa,1}$ (uH)	$L_{bb,1}$ (uH)
95	193	498.0	695.3
150	124	520.0	717.3
185	99.1	519.6	710.7
240	75.4	512.5	696.7
300	60.1	473.2	644.2
400	47.0	483.2	650.5

An error band of ±5% was also plotted for the ratio curve in Figure 4.7. The average value of the absolute error for $L_{aa,h}$ and $L_{bb,h}$ were 1.9% and 2.1%, respectively, and the highest value was 4.5%. The values of inductances $L_{aa,1}$ and $L_{bb,1}$ at 50Hz for 4/c cables are presented in Table 4.2.

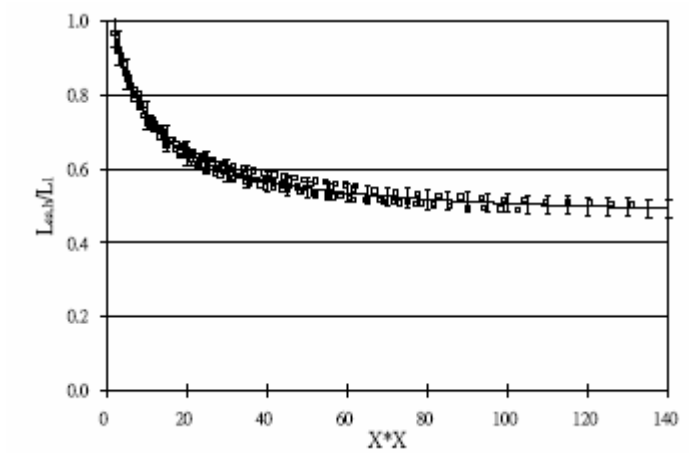

Figure 4.7 Positive-sequence resistance of all 4/c armored cables

☐ Measured values of $L_{aa,h}/L_{aa,1}$

— Empirical formula of $L_{aa,h}/L_{aa,1}$

4.3 Single-core Cable with Aluminum Armor

Modern polymeric-insulated cables normally contain a semi-conducting insulation shield with provision for fault current return by a concentric metallic path in the form of wires, tapes or a solid metallic armor, which provides mechanical and corrosion protection in the meanwhile. For being easy to handle and with heat dispersion consideration, single-core cables are often used for connecting transformers to main low voltage switchboard in Hong Kong. At other places where there is a high loading current single-core cables are also preferably considered. However, induced voltages are produced when currents flow through the cables. Although cable jackets capable of withstanding high electrical stress permits high standing voltages on the armor or sheath, over-voltage is not allowed. For example, practice in the United States appears to permit a steady-state sheath voltage of 65V-90V while in British 65V level is used. [IEEE 1988] Generally speaking, armor bonding of these cables in cooperation with grounding is necessary. Different bonding methods were introduced and illustrated in [IEEE 1988], and some other publications [IEEE 1988, K. Ferkal etc. 1996, Y. Du etc. 2001, George J. Anders 1997] also present the application of bonding methods including calculation of induced voltage and current, losses in cables, selection and impact of bonding methods etc..

Solid bonding for cable armor is the simplest solution to the problem of armor

voltages. However, currents are induced in the armor by the current flowing in the power conductors, which are not negligible. The induced currents in the armor may reduce the current rating of the cables. [IEEE 1990] Moreover, the induced current causes energy losses in the armor. In Hong Kong, the CoP of Energy Efficiency Code sets out the minimum requirements on energy efficiency of electrical installations in buildings. Therefore, the impact of bonding methods should be investigated in order to comply with the requirements in buildings. In addition, parameters of the cable such as harmonic impedance may change due to the interaction of conductor currents and induced currents.

In the following part, the impact of bonding methods for aluminum-armored single-core cables is discussed. The performance of these cables is presented against cable formations. The cables under discussion are the 185 mm^2 armor single-core XLPE-insulated cables. Appropriate formations and bonding strategies for the cables in buildings are discussed.

4.3.1 Cable Formations and Bonding Methods

Single-core armored cables are used for three-phase power distribution in buildings. They are normally deployed on tray (e.g. galvanized iron tray), trunking or directly fixed on wall, floor and ceiling. According to local practices,

single-core cables are often arranged in three different formations, that is, flat and touching, flat and spaced and trefoil formations, as illustrated in Figure 4.8. Cable spacing in the flat and spaced formation usually is one diameter of these single-core cables.

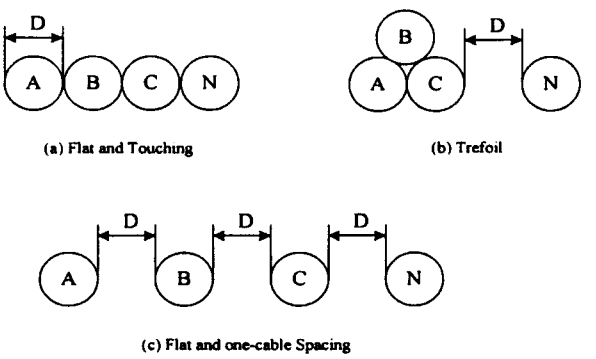

Figure 4.8 Formations of single-core armored cables

In order to reduce magnetic losses single-core cables do not has magnetic armoring. Non-magnetic armoring (e.g., aluminum armoring) may be provided if additional mechanical protection or others is required. For cables with non-magnetic armor, a bonding method should be considered. Generally, solid bonding, which refers to bonding of the armor of all cables in the installation at their two ends, is required to diminish the voltage induced along the armor. This technique may generate significant eddy current in the armor, and subsequently it is necessary to derate the cables. The additional losses are unavoidable. In other words, the solid bonding method changes the parameters of the conductor due to the armor currents. Therefore, in most cases, the cables are laid in as close as possible to minimize the magnetic flux linking both the conductors and

close as possible to minimize the magnetic flux linking both the conductors and armors as long as heat dissipation is enough.

Special bonding techniques such as single-point amd cross bonding methods are used in view of economics or minimizing the heat generation by induced current. Single point bonding refers to bonding of cable armor at one point only along their length. While cross bonding refers to bonding of the cable armor in multiple consecutive sections with different phase notation so as to approximately neutralize the total induced voltage in three consecutive sections. The techniques of single-point bonding and cross bonding are generally applied to the cables with a short length and a long length, respectively. For the cables installed in buildings only the single-point bonding system is considered here.

4.3.2 Experimental Setup for Single-core Armor Cables

Figure 4.9 shows the experimental setup of harmonic impedance measurement. Three-phase harmonic currents were generated from a harmonic current source. They were applied to sample cables under test. Voltages, currents and powers on the cables were measured with Power Analyzer PM3000A. The recorded data, then, were used to determine harmonic impedance of these cables.

The cables under test were four single-core armored cables to BS6724. These

cables had a conductor size of 185mm^2, and a length of 10 meters. In the experiment the cables run in parallel, and were arranged according to Figure 1, that is, in the flat and touching formation, or flat and spaced formation or trefoil formation. The single-core armored cables were connected together at one end with a copper busbar, and connected to a current source at the other end. The armors of these cables were bonded either at one cable end or at two cable ends depending whether the single-bonding method or solid bonding method is employed.

The harmonic current source consisted of one harmonic signal generator, three power amplifiers and three step-down transformers, as illustrated in Figure 4.9. In the experiment, three-phase currents were injected into the cables under test via the step-down transformers. These currents generated three-phase voltages on the cables.

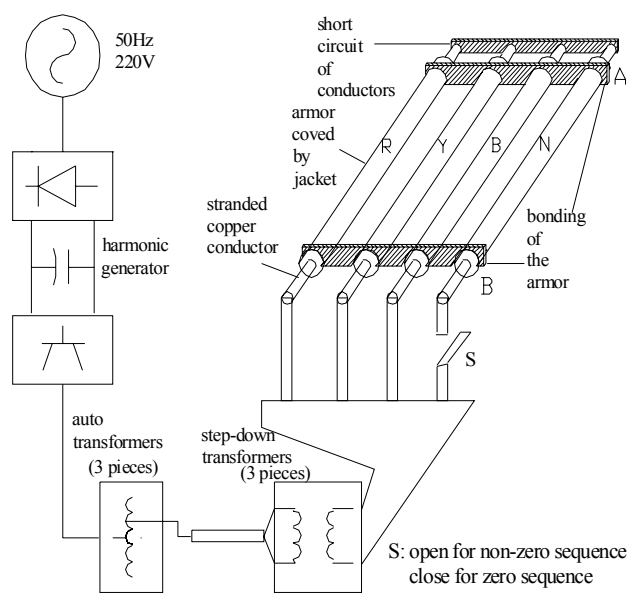

Figure 4.9 Laboratory setup with the flat and spaced formation for the cables in solid bonding

In the measurement of harmonic impedance distorted voltages were generated from the power amplifiers. They contained one fundamental component and one harmonic component at the orders up to 49. The ratio of the fundamental voltage to the harmonic voltage remained one for all orders. The fundamental voltages were positive sequence, while the harmonic voltages were either zero or positive sequence depending on whether the order was triplen or nor. The neutral cable was connected to the supply only during the zero-sequence impedance measurement, as illustrated in Figure 4.9.

4.3.3 The Impact of Armor Bonding Methods

In the experiment voltages, currents, and active power of order *h* on three cables were recorded with PM3000A. Both resistance R_h and reactance X_h of order *h* per phase, then, were calculated by

$$\begin{aligned} R_h &= P_h / I_h^2 \\ X_h &= \sqrt{(V_h / I_h)^2 - R_h^2} \end{aligned} \tag{4.10}$$

where V_h, I_h and P_h are the average values of all phase voltages, phase currents, and phase powers at order *h*, respectively. As an example, the results of three types of configuration for the cables in free air are presented. Figure 4.10 and Figure 4.11 present the unit resistance of the cables under the non-zero

Figure 4.12 present the unit reactance of these cables under the same conditions. The abbreviation 'SPB' used in the results means 'single point bonding' while 'SB' for 'solid bonding'. Symbols (a), (b), and (c) in these figures represent the different formations as shown in Figure 4.8. For the fundamental component, balanced three-phase currents at half of rated value were applied to the single-core cables. The voltage ratio of the fundamental to harmonics is 1.

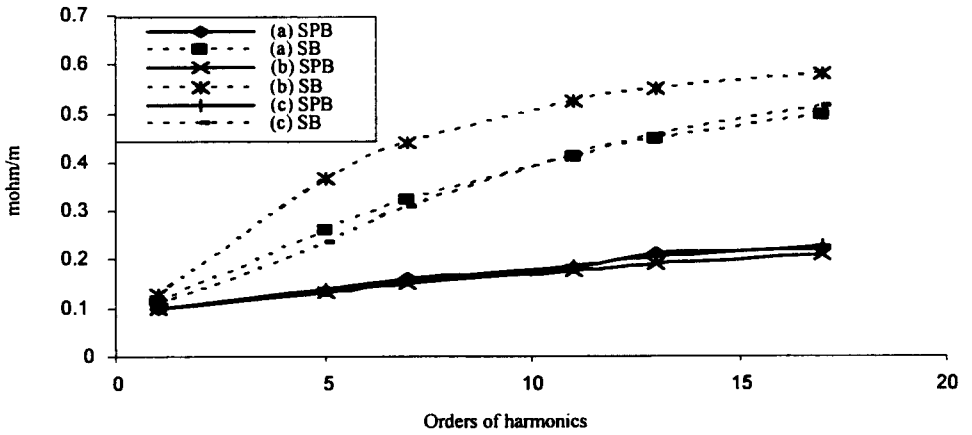

Figure 4.10 Cable resistances under the positive-sequence current

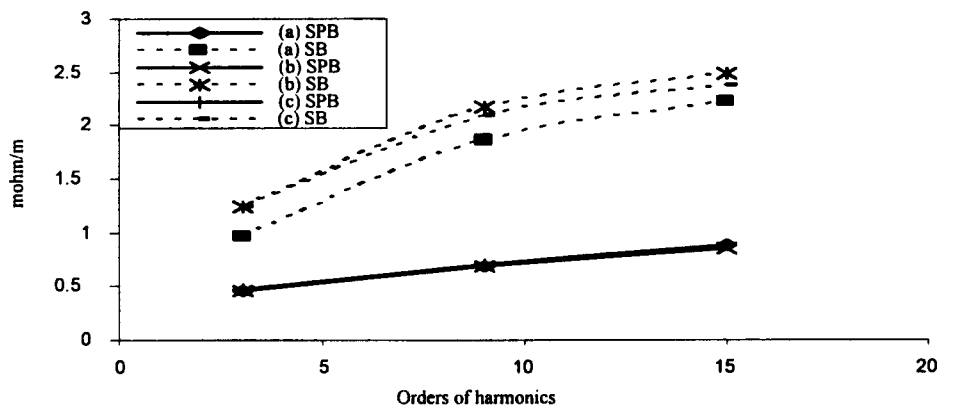

Figure 4.11 Cable resistances under the zero-sequence current

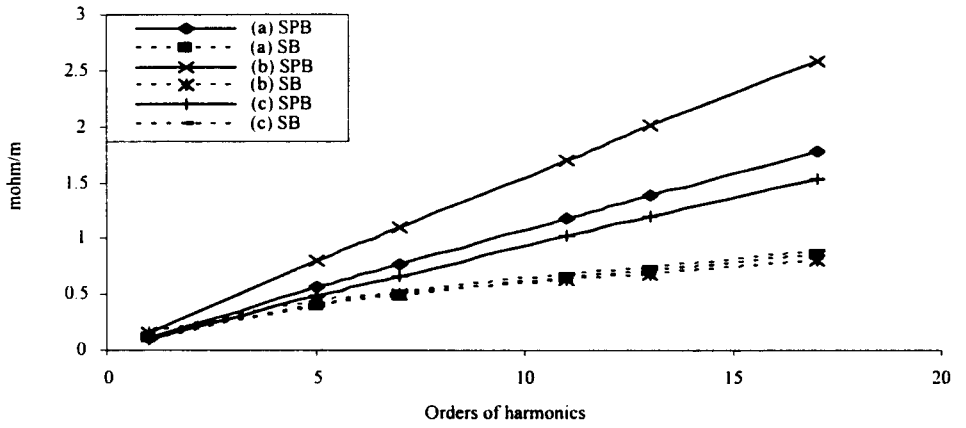

Figure 4.12 Cable reactance under the positive-sequence current

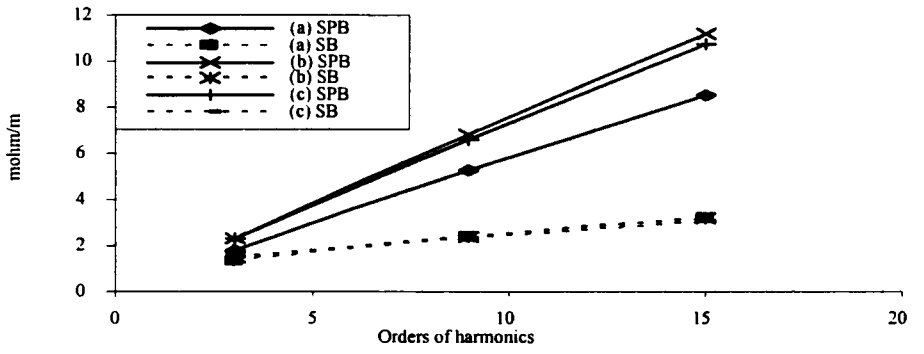

Figure 4.13 Cable reactance under the zero-sequence current

The cable resistances per meter are shown in Figure 4.10 and Figure 4.11. It is concluded that the resistance of the cable in solid bonding is larger than that in single point bonding. The largest ratio of resistance in solid bonding to that in single point bonding is up to 3.2. It is noted that the resistance of the cables in solid bonding tends to saturate at higher frequencies. Dr. K. Ferkal *et al.* discussed in [K. Ferkal etc. 1996] that the proximity effect factor had a maximum value at some frequency because the existence of the armor current cancelled the effect of the external magnetic fields when frequency was high. Therefore, the

Therefore, the induced current of the armor blocks a further increase of the resistance at higher frequencies.

The reactance against harmonic order is presented in Figure 4.12 and 4.13. The reactance for the cables in solid bonding is smaller than that in single point bonding. This is due to the existence of the mutual inductance between the armor loop and conductor loop. The inductance of the conductor consists of self-inductance and mutual inductance. For simplicity in analysis, two two-conductor loops are considered. One is the loop formed by the phase conductor and neutral conductor, and the other is formed by the armour in two cables. Because the induced current in armour flows in the opposite direction, compared with current in the conductors, the mutual inductance turns negative. Consequently, the total inductance of the conductor is reduced for the cables in solid bonding.

4.3.4 Impact of Cable Formations

The deployment of cables has a significant impact on the harmonic impedance. The experimental results on the impact of cable formations, that is, (a) flat and touching formation, (b) trefoil formation and (c) flat and spaced formation as illustrated in Figure 4.8, are presented in this section. The experimental results

on the impact of cable management systems, that is, (a) free air, (b) metal tray and (c) metal trunking, are presented as well.

The ratio of cable impedance with one formation to that with the reference formation, and the ratio of cable impedance with one management system to the reference are plotted in the figures. The reference cable management system is the one for cables installed in free air. In these figures, r_i and x_i represent cable resistance and reactance with either formation i or management system i.

I. The impact of different formations

The impact of cable formations is illustrated in this section. The cables were installed in free air. The reference cable formation is the flat and touching formation.

Figure 4.14 and 4.15 shows the impact of the formation on cable impedance under the single point bonding configuration. It is shown in these figures that Formation (c) results in an increase of the reactance and a decrease of the resistance, compared with the results of Formation (a). At higher orders, the increment of the reactance reaches 51% and the decrement of the resistance reaches 22%. With the impedance of the cables with Formations (a) and (b) is close to each other. Under the single-point bonding configuration, the descending order of the cable formations is flat-and-touching, trefoil and

flat-and-spacing formations for the resistance; flat-and-spacing, flat-and-touching and trefoil formations for the reactance.

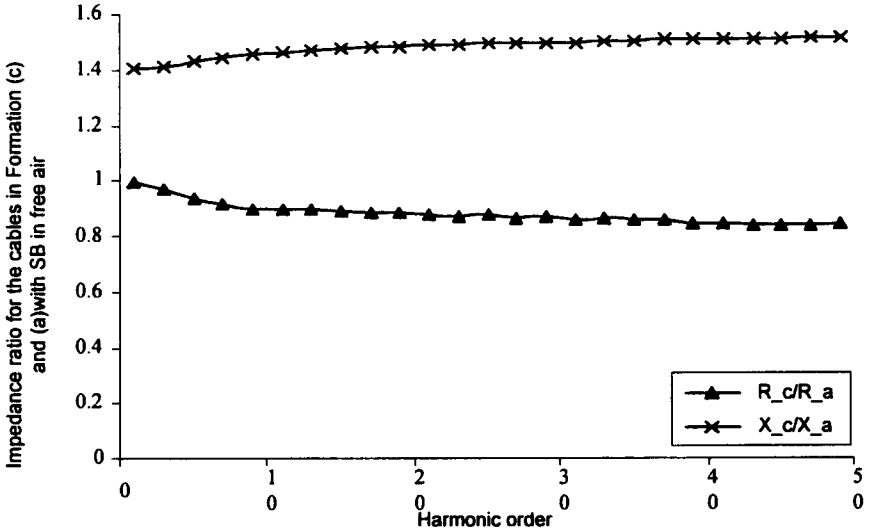

Figure 4.14 Impact of flat-and-spacing formation over flat-and-touching formation under the single-point bonding configuration

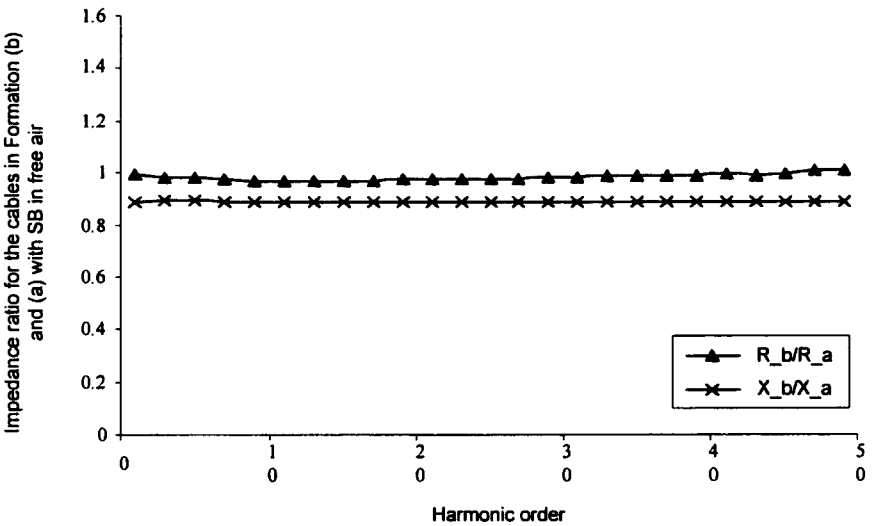

Figure 4.15 Impact of trefoil formation over flat-and-touching formation under the single-point bonding configuration

It is shown in Figure 4.16-4.17 that the bonding method has a great impact on the cable impedance. Under the solid bonding configuration, there is no significant difference of the impedance ratio with difference formations at higher orders. The descending order of the cable formations is the

flat-and-spacing formation, the flat-and-touching formation and the trefoil formation for both resistance and reactance..

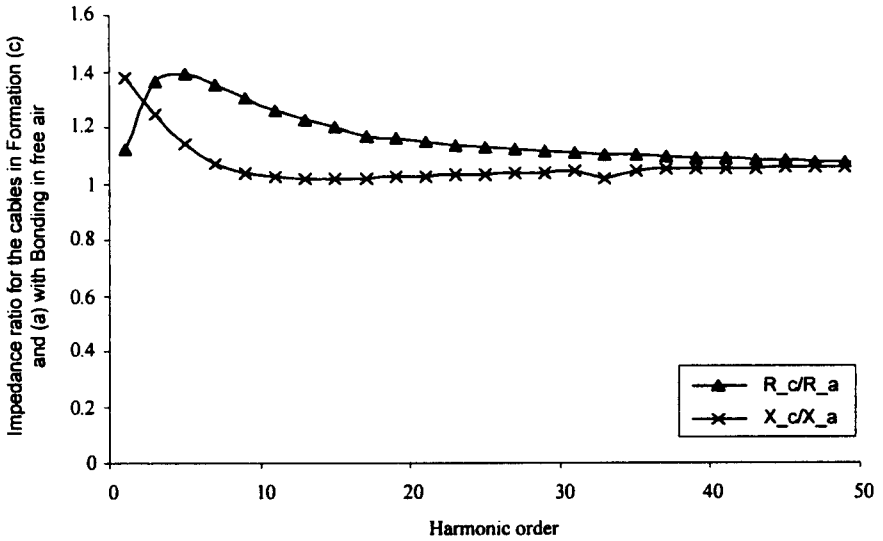

Figure 4.16 Impact of flat-and-spacing over flat-and-touching formations under the solid bonding configuration

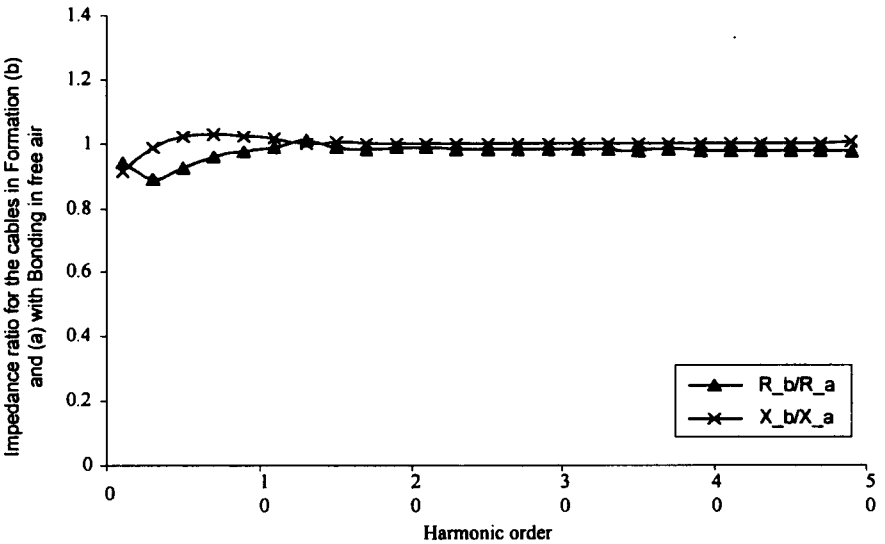

Figure 4.17 Impact of trefoil over flat-and-touching formations under the solid bonding configuration

II. The impact of the cable management systems

Similar to the previous discussion, the cables were arranged in flat and touching formation. The reference case is the case in which cables were installed in free

air. Figure 4.18-4.19 shows the results under the sing-point bonding configuration, and Figure 4.20-4.21 presents the results under the solid bonding configuration.

Under the single-point bonding configuration the reactance of the cables is not sensitive to the cable management system employed. The maximum value of the reactance ratio is observed at the fundamental frequency. This indicates that metal around these cables does not play an important role in cable reactance. However, the resistance ratio changes dramatically against harmonic order, and reaches a value of more than 2 at higher orders. At higher orders harmonic resistance contributed by eddy-current within the tray or trunking is significant.

Figure 4.20-4.21 present the results of impedance ratios under the solid bonding configuration. It is noted in both figures that these impedance rations do not have significant difference. The maximum difference is observed at lower orders, but does not exceed 20% in both cases. This indicates that the eddy-current in metal tray and metal trunking has no significant effect. In these cases, the armor of these cables was bonded solidly at their two ends. Significant induced currents were generated within the loop of the cable armor, and canceled the magnetic flux outside these cables. This reduced the eddy-current within the tray and trunking, subsequently reduced the degree of impact of such metalwork on cable impedance.

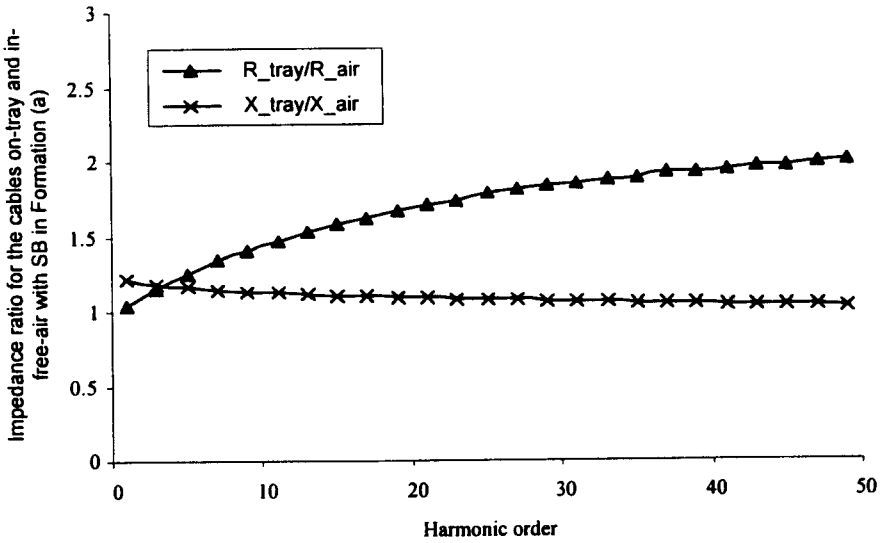

Figure 4.18 Impact of on-tray system over in-air system under the single-point bonding configuration

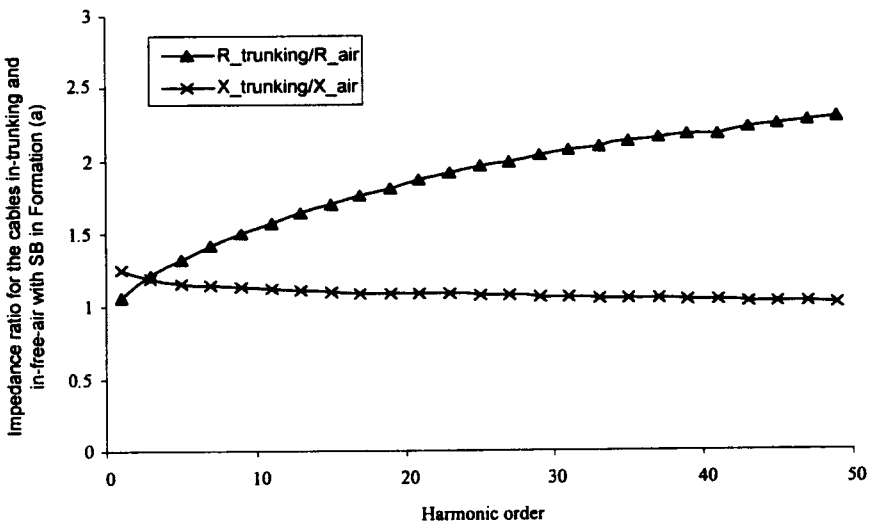

Figure 4.19 Impact of in-trunking system over in-air system under the single-point bonding configuration

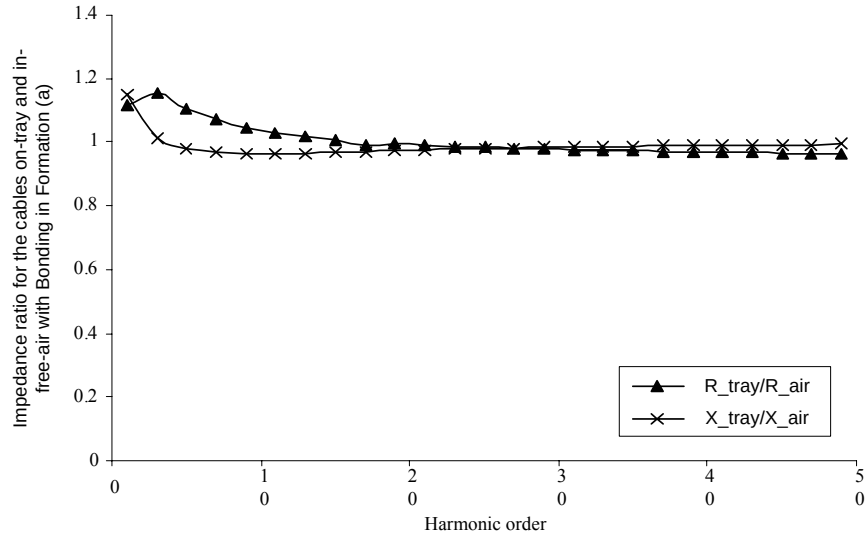

Figure 4.20 Impact of on-tray system over in-air system under the solid bonding configuration

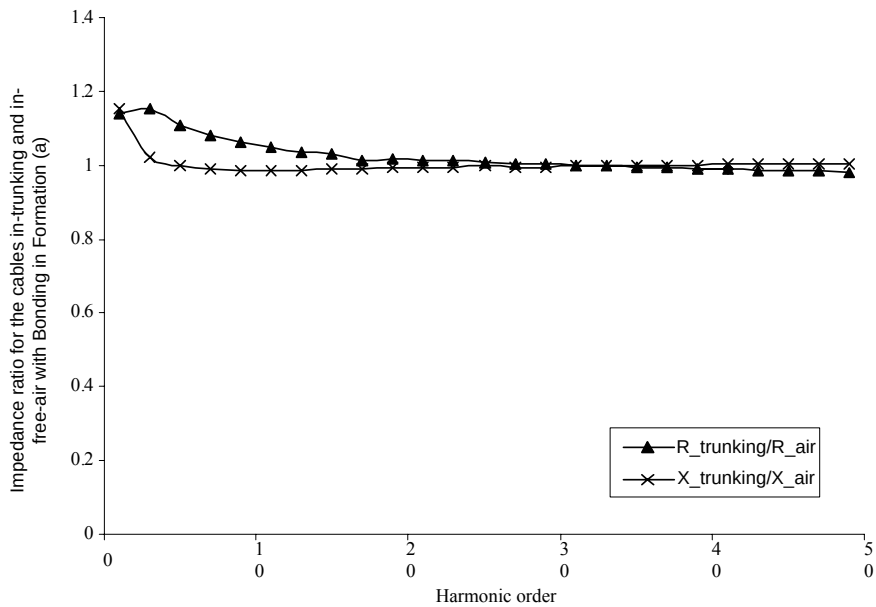

Figure 4.21 Impact of in-trunking system over in-air system under the solid bonding configuration

4.4 Single-core Cables without Armor

In buildings non-armored single-core cables with thermosetting insulation of rated voltage 600/1000 V are also used in distribution system. In this thesis two types of single-core cables, e.g. 400 mm^2 and 630 mm^2 to BS 7889, were

selected for the investigation into the harmonic characteristics of non-armored single-core cables under different deployments. .

Similar to the armored single-core cables, non-armored single-core cables can be arranged in three formations: (a) flat and touching, space and (b) touching, and (c) trefoil formations, and normally deployed (a) in free air, (b) on tray, (c) in trunking. The harmonic characteristics of 400mm2 non-armored single-core cables are discussed in this section..

4.4.1 Impact of Cable Formations

The impact of cable formations on cable impedance was investigated experimentally. The cables were installed in free air. The reference cable formation is the flat and touching formation. The results in free air condition are presented as Figure 4.22-4.23.

Compared with the flat and touching formation, it is shown in Figure 4.20 that the resistance in the flat and spacing formation decreases down to 72%-88% at higher orders. The reactance, however, increases with the harmonic order. The reactance increases by 44% at the fundamental, and by 65% at order 49. The resistance in Figure 4.23 decreases as well. The reactance with the trefoil formation decreases compared with that in the flat and touching formation.

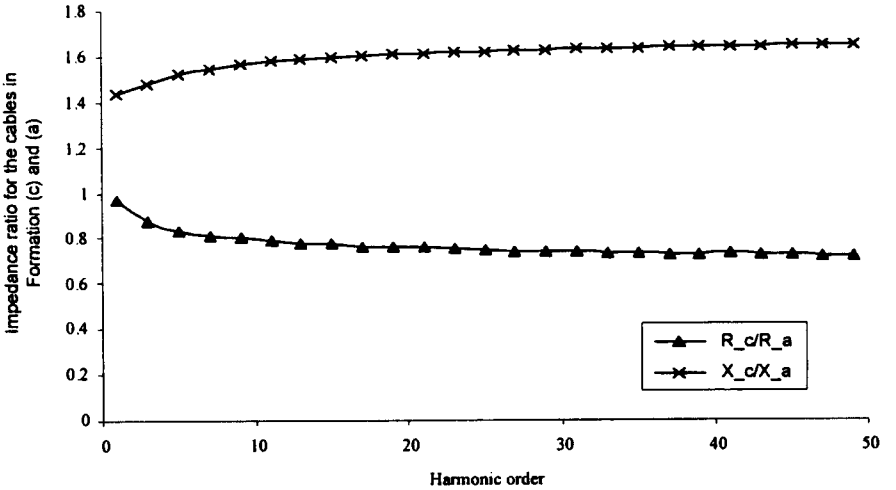

Figure 4.22 Impact of flat and spacing formation over flat and touching formation

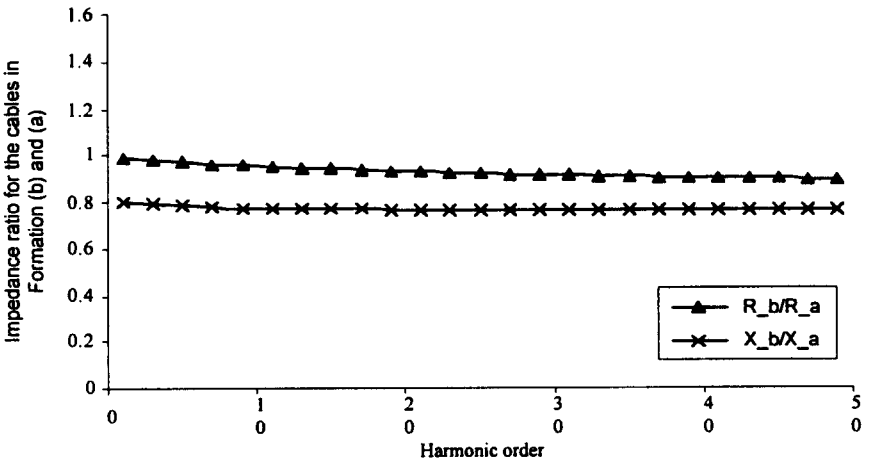

Figure 4.23 Impact of trefoil formation over flat and touching formation

It can be drawn from the results that the resistance with both the flat-and-spacing and trefoil formations is less than that with the flat and touching formation. The descending order of the cable formations is flat-and-touching, trefoil and flat-and-spacing formations for resistance, and flat and spacing, flat and touching, and then trefoil formations for reactance.

4.4.2 Impact of Cable Management Systems

Similar to the previous discussion, the cables were arranged in flat and touching formation. The reference case is the case in which cables were installed in free air. Figure 4.25-4.26 shows the results of cable resistance and reactance.

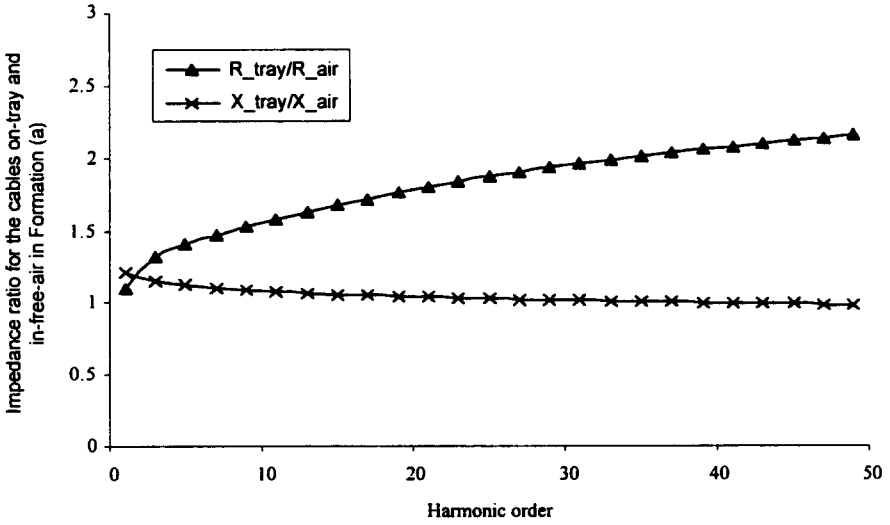

Figure 4.24 Impact of on-tray system over in-air system

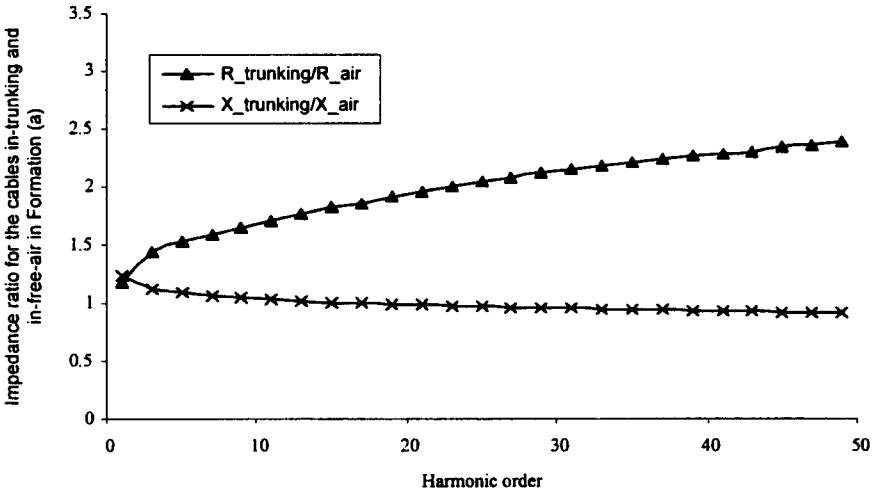

Figure 4.25 Impact of in-trunking system over in-air system

It is noted from Figure 4.24-4.25 that both resistance and reactance rations in two cases are similar. The reactance of the cables with three management

systems is very close except at the fundamental frequency. The resistance of the cables with three different systems is significantly different at harmonic orders. It can be drawn that the impact of cable management systems on the resistance is significant. It can be obtained that the trunking has the most significant impact on the impedance of the cables due to strong eddy current within the trunking.

4.5 Summary

An experimental method was employed to investigate the harmonic impedance of electric cables, which are widely used in building LV distribution systems. Multi-core armored cables with cross-section areas of 95mm^2, 120mm^2, 150mm^2, 185mm^2, 240mm^2, 300mm^2, 400mm^2, as well as single-core aluminum-armored cables and single-core non-armored cables were selected. Harmonic impedance of the orders up to 49 was obtained from the measured data.

Harmonic impedance data may serve as a reference for designers or engineers to select appropriate cable installation methods to mitigate harmonic distortion in a system.

(a) Multi-core armored cables

- Cable resistance increases as increasing harmonic order due to both skin and proximity effects as well as eddy current losses within the steel wire armor.
- Cable inductance is frequency-dependent, and declines with increasing harmonic order.
- Empirical formulas of both cable resistance and inductance were derived.

(b) Single-core aluminum-armored cables

- Cables are normally derated if a solid bonding method is employed. Cable resistance is large, but cable inductance is small for cables in solid bonding, compared with those in single-point bonding.
- In single-point bonding the cable formation has a significant impact on cable impedance. In solid bonding, the impact of the cable formation is not significant

(c) Single-core non-armored cables

- The resistance of the cables in the flat touching or trefoil formation is the most significant, while the inductance of the cables in flat-spaced formation is the most significant.
- Cables may be installed in trunking, tray or free air. Trunking has the most significant impact on cable impedance at lower harmonic orders. Because of the cancellation effect arising from the induced current in trunking the impedance of the cables in trunking can be lower than that in free air.

Chapter 5

Harmonic Management in High-Rise Commercial Buildings

5.1 Introduction

Appropriate cabling for LV distribution systems in buildings may effectively reduce harmonic impedance so as to improve the voltage quality along the circuits. This measure is usually taken in the stage of system design. In existing buildings it is quite natural to assess new harmonic-producing loads before connecting them to the supply in order to avoid excessive harmonic pollution in buildings. Therefore, it is necessary to investigate possible harmonic regulation in buildings.

Existing harmonic standards may be applied to regulate harmonics in high-rise commercial buildings. It is known that the harmonic standards can be categorized into the system-level standard such as IEEE Standard 519-1992 and the equipment-level standard such as IEC standards. Just as they names imply, the system-level standards focus on harmonic management at the point of common coupling (PCC) while the equipment-level standards focus on harmonic emission from the harmonic-producing equipment connected to the PCC. In this chapter these standards are adopted as the reference in managing harmonics in commercial buildigns.

In this chapter, harmonic management in buildings is proposed with the help of ER G5/4 in local high-rise commercial buildings. Some suggestions are presented according to the characteristics of local building distribution systems. Furthermore, the responsibilities among different parties in controlling harmonics in commercial buildings are recommended.

5.2 Harmonic Assessment in Commercial Buildings with ER G5/4

ER G5/4 uses a three-stage procedure for harmonic assessment in an electrical system. The assessment procedure in a building is presented in the following parts, and is illustrated with the aid of the example in a 29-floor building. Special features of local supply and building distribution systems are taken into account in the assessment.

5.2.1 Outline of ER G5/4

I. Planning levels for individual harmonics

ER G5/4 explicitly defines the planning levels for individual harmonic voltage distortion and total harmonic voltage distortion (THDV) at the point of common coupling (PCC). The predicted voltage distortion caused by non-linear loads at PCC should be less than the corresponding planning level generally. These

planning levels are normally set to be less than or equal to the compatibility levels given in IEC 61000-2-2 and 61000-2-12. This feature ensures the compatibility of harmonics in the whole system. Table 5.1 shows the planning levels in 380V and 11kV systems. Similar to other standards, the probability of the levels of harmonic voltage distortion should be taken into consideration by using the values of background distortion that is no exceeded for 95% of the time [UK Electricity Association 2001].

Table 5.1 Planning levels of harmonic voltage distortion (up to 15^{th})

Order *h*	3	5	7	9	11	13	15	THD
11kV (%)	3	3	3	1.2	2	2.5	0.3	4
380V (%)	4	4	4	1.2	3	2.5	0.3	5

II. Pre-calculated limits of harmonic current emissions

Maximum permissible harmonic current emissions are pre-calculated based on an assumption that the system may supply four such larger sources or their equivalent in terms of larger number of smaller sources. The calculation is done on the premise that the existing levels of harmonic voltage distortion are less than 75% of planning levels. This means that the connection is permitted given that the emission limits are complied and the new non-linear load does not contribute more than 25% of the planning levels at the point of connection. The permissive maximum current emission is calculated by,

$$I_h = \frac{V_{hp} \cdot F \cdot 10^6}{k \cdot h \cdot \sqrt{3} \cdot V_s \cdot 100} \cdot 25\% \qquad (5.1)$$

where h is the harmonic order,

V_{hp} is the planning voltage at order h in percentage,

F is the typical fault level at PCC in MVA,

k is the harmonic impedance factor related to system resonance,

V_s is the nominal system line voltage at PCC in volts,

I_h is the maximum permissible current emission for new connection in amp.

III. Three-stage assessment

A three-stage assessment is introduced in ER G5/4 to determine whether or not the connection of a harmonic-producing installation to a supply network is permitted. The assessment in Stage One is applicable to a 230/400V system (the building LV distribution system), and that in Stage Two to the system rated less than 33kV and that in Stage Three to the system rated above 33kV. If the connection is not permitted in Stage One, detailed calculations should be conducted in Stage Two or even in Stage Three. At Stage Three, no connection is possible without any harmonic mitigation if the prediction of total harmonic distortion and individual harmonics exceeds the planning levels.

IV. Using IEC Standards wherever possible

IEC standard series on harmonics, such as IEC61000-2 and 61000-4, are well-known documents, and are applied in many countries, especially in Europe.

Generally speaking, these documents are used to limit harmonic emissions from individual equipment. ER G5/4 adopts the limits given in these standards in the initial assessment for an installation. ER G5/4 also adopts the concepts of system planning levels and harmonic voltage prediction used in IEC61000-3-6 in the assessment for MV and HV aggregate loads as well as LV installations. This feature enables ER G5/4 to be aligned with the international standards. Also, this feature simplifies the procedure of harmonic assessment for most small power equipment.

5.2.2 Examples of Harmonic Assessment in Local Buildings

I. Building distribution systems

Typical LV distribution systems in high-rise buildings have been described in detail in Chapter 2. Usually the utility is responsible for its supply cables and equipment up to service terminations, or the incoming terminals of the customer's main circuit breaker where the supply is taken directly from its 11kV/380V transformer or 11kV switchgear. The Δ/Y_0-connected transformer or switchgear is normally located on the ground floor, and feeds various radial distribution circuits in the building. Risers are the major distribution element, and 100m length is not uncommon in a high-rise building. In practice, rising distribution is made by power cables or air-insulated busbars (busbar trunking), or fully-insulated busbars (busduct). Normally, busbar trunking or busduct has a

large rating up to the transformer full-load current, while power cables are capable of carrying upwards of 1000 A. Distribution boards are situated in the meter rooms together with utility's watthour meters. They feed various loads on the corresponding floors. For tenant loads, the distribution boards have a rating of typically 200-400 A. Figure 5.1 shows a typical part of the distribution system in a building.

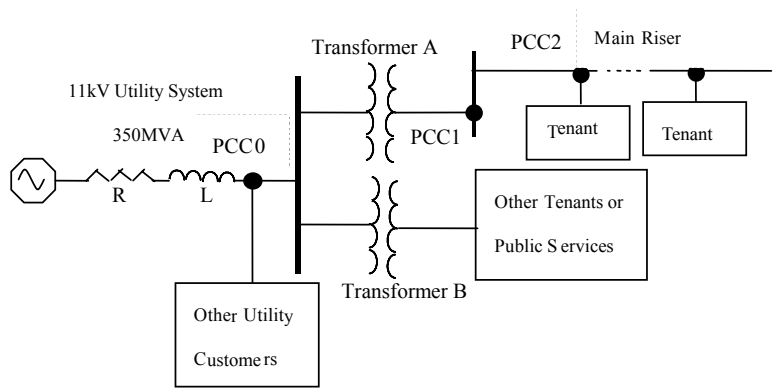

Figure 5.1 Distribution system in a commercial building

II. Selection of Points of Common Coupling (PCCs)

The PCC is the point in a system where other customers can be served. As ER G5/4 defines the planning levels at the PCC, the selection of PCC is the first issue to be addressed when assessing harmonics in a building.

Three parties are normally involved in the supply connection in a building, namely, the utility, the landlord and the tenant. The utility deploys its supply system up to the entrance of the building via distribution transformers. The

landlord connects its LV distribution system to the entrance to get service for itself and its tenants. This system, then, serves as an interface between the utility supply and tenant's equipment or landlord's equipment. Logistically this distribution system as a whole is treated as the PCC. However, the primary side of the transformer is considered as the PCC (PCC0) if the distribution transformer is owned by the landlord. It should be noted that the customers served by the LV distribution system may not be treated equally as the system impedance in the building is no longer trivial. To facilitate the following discussion, PCC1 and PCC2 are introduced as shown in Figure 2.1 or 5.1, which are located at the main LV switchboard and the distribution board in a meter room, respectively.

III. Procedure of harmonic assessment in buildings

The procedure of harmonic assessment in buildings is presented in Figure 5.2 according to ER G5/4. In Stage One the limits of harmonic current emissions in IEC 61000-3-2 [IEC 1995] and 61000-3-4 [IEC 1998] are applied firstly to determine the connection of a new installation less than 75A. For the installation failing to comply with these standards, a table of maximum permissible harmonic current emissions on the base of a 10MVA fault level is applied. The document exempts the assessment of small rating converters and AC regulators. Stage One is applied inside the building electrical system.

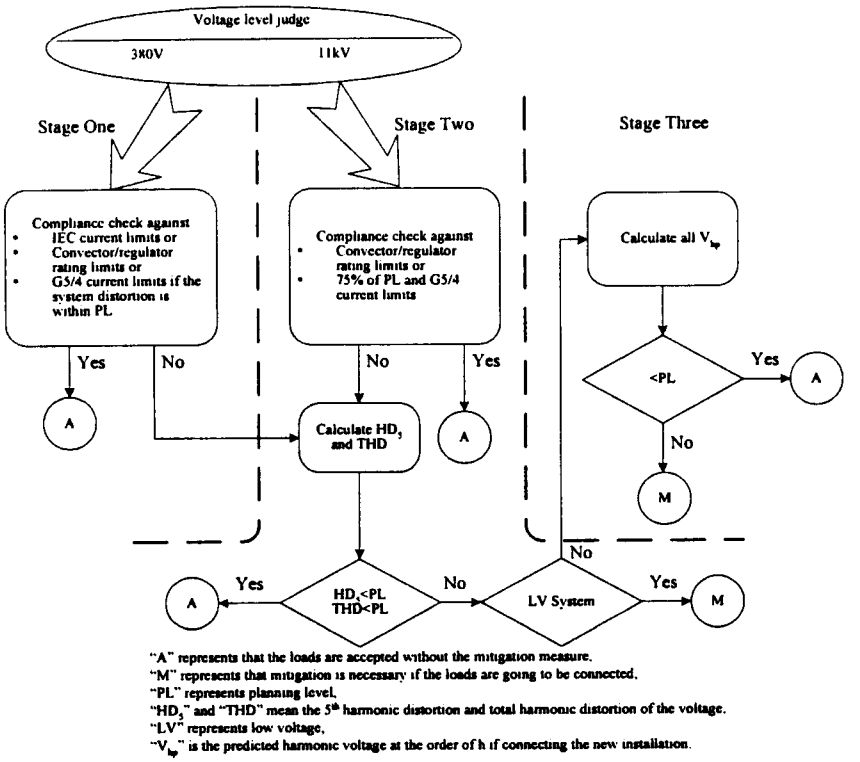

Figure 5.2 Procedure for harmonic assessment in commercial buildings

If the installation fails in the assessment at Stage One, the Stage-Two assessment is required. In Stage Two a simple reactance model of the supply source, which allows for any low-order harmonic resonance, is employed for harmonic voltage prediction. Mitigation becomes necessary if the predicted 5^{th} order or the total harmonic distortion (THD) does not meet the planning levels. Stage Two is the last stage of the assessment for the connection inside the building LV distribution system.

Stage Two is also applicable to the utility system rated at 11kV. The assessment procedure for the connection of an installation to such a system is similar to that to the system rated at 380V. The converter/AC regulator rating and/or harmonic

current emissions are checked first against the tables given in ER G5/4. The 5th order and total harmonic distortion of voltage needs to be calculated when the assessment fails. If the predicted 5th order or the total harmonic distortion is greater than the planning level of the system at 11kV, the Stage-Three assessment, which is based on a more detailed system model, is applied. In Stage Three, all orders of the predicted harmonic voltages may be calculated.

IV. Notes on implementation of ER G5/4

A. Prediction of voltage distortion at PCCs

According to ER G5/4, the resultant voltage distortion after the connection needs to be determined if its background levels at PCC exceed 75% of the planning levels. The resultant voltage distortion is calculated by an addition of the voltage distortion caused only by the new installation into the existing distortion. Connection to a network without mitigation is not permitted if the THDV or the 5th harmonic distortion of voltage (Stage Two) is greater than the corresponding planning level.

Voltage distortion caused by a new load at PCC is the product of its harmonic current and system impedance. This calculated voltage distortion is expressed as a percentage of the system phase voltage. At a particular harmonic frequency it is given by,

$$V_{hc} = I_h \cdot Z_h \cdot \frac{\sqrt{3}}{V_s} \cdot 100\% \quad (5.2)$$

and

$$Z_h = k \cdot h \cdot \frac{V_s^2}{F} \cdot 10^6 \quad (5.3)$$

where h is the harmonic order,
I_h is the harmonic current in RMS drawn by the new load at PCC,
V_s is the nominal system line voltage at PCC in volts,
F is the system short-circuit level at PCC in MVA,
V_{hc} is the calculated harmonic voltage distortion at the PCC associated with the new load expressed as a percentage of the phase voltage.

ER G5/4 adopts the approach described in IEC 61000-3-6 in predicting the resultant voltage distortion at PCC. For harmonics up to the 5th and triple-n harmonics, the predicted value is simply the arithmetical summation of the background level by measurement and the value caused by the new load, that is,

$$V_{hp} = V_{hm} + V_{hc} \quad (5.4)$$

For other harmonics, a phase difference of 90º between the background level and the new-load level is assumed. The predicted value, then, is expressed as,

$$V_{hp} = \sqrt{V_{hm}^2 + V_{hc}^2} \quad (5.5)$$

B. Limits of harmonic emissions at PCCs

In Hong Kong the short circuit capacity at 11kV is approximately equal to 350MVA. The distribution transformer is typically rated 1500kVA with a short-circuit impedance of 6-6.5%. Therefore, the short-circuit current at the secondary side of the transformer is about 35-38kA resulting in a short-circuit capacity of 23-25MVA at PCC1. A figure of 25MVA is adopted in this paper.

This figure is applicable to PCC2 if the impedance of LV distribution systems is negligible. With Equation (5.1), the maximum permissible harmonic current emissions at PCCs of local buildings are derived, and given in Table 5.2. It should be mentioned that these limits are applicable if the background levels are less than 75% of the planning levels.

Table 5.2 Limits of current harmonics at PCCs

Order h	3	5	7	9	11	13	15
Limit at PCC0 (A)	22.96	13.78	9.84	6.12	8.35	8.83	0.92
Limit at PCC1 or PCC2 (A)	126.62	75.97	54.26	25.32	51.8	36.52	3.8

V. Harmonics measurement

In order to determine the background levels, harmonic measurements need to be carried out at the main LV switch room (PCC1) and the meter room (PCC2). For the purpose of illustrating the assessment procedure, a 29-stories building was selected for the measurements. The measurements were taken during 10:00am-12:00pm and 2:00pm-5:00pm on weekdays. Each measurement lasted for a few minutes at an interval of 3-30 seconds. It was noted that the variation of system harmonic levels was very small during working hours. For simplicity of discussion, harmonic values (up to 15^{th}) at the main LV switchboard (PCC1) and on 28F (PCC2) are listed in Table 5.3.

Table 5.3 Results of harmonics measurements in a commercial building

Order	3	5	7	9	11	13	15	THD_v
V_{hm} (PCC1) (%)	3.98	1.88	0.45	0.22	0.19	0.12	0.11	4.44
I_{hm} (PCC1) (A)	231	60.8	16.0	4.48	6.40	3.47	1.65	
V_{hm} (PCC2) (%)	5.58	2.64	0.63	0.31	0.26	0.17	0.16	6.22
I_{hm} (PCC2) (A)	14.6	6.60	3.99	0.77	0.82	0.43	0.49	

VI. Harmonic assessment

A. At PCC0

Suppose a new installation having identical loads and harmonic current emissions is to be connected to the 11kV supply network at PCC0. In this case the distribution transformer of the new installation is owned by the landlord. The assessment, then, directly comes into Stage Two because of the voltage level at PCC0.

The background levels of harmonics at PCC0 should be measured first. Because of the difficulty in accessing utility's supply systems, harmonics data at PCC1 are used by viewing the transformer as a potential or current transformer. Table 5.4 shows both 75% of planning levels and background levels at PCC0. The table does not include the triple-n components because of the delta/star connection of this transformer. As the background levels are less than their corresponding planning levels, a simple check of harmonic current emission against the maximum permissible current limits given in Table 5.4 is required. Table 5.5 shows both harmonic current emissions from the new installation and their limits. Clearly, the connection of the new installation to the supply network is allowed without mitigation.

Table 5.4 Comparison of planning and background levels at PCC0

Order *h*	5	7	11	13	THD
75% of planning level (%)	2.25	2.25	1.5	1.725	3
Background level (%)	1.88	0.45	0.19	0.12	1.95

Table 5.5 Comparison of harmonic emissions and limits at PCC0

Order *h*	5	7	11	13
Emission limit (A)	13.8	9.8	8.4	8.8
Emission level (A)	2.1	0.55	0.29	0.22

B. At PCC1

Similar to the previous discussion, the assessment is carried out assuming that an identical new LV installation is to be connected at PCC1. The stage-one assessment of this new installation fails because of its high harmonic current emissions. It is noted that the existing background levels shown in Table 5.3 exceed the 75% of the planning levels at PCC1. The assessment has to come into Stage Two and a prediction of resultant voltage distortion is required using the simple reactance model. The resultant voltage distortion is predicted by an addition of the distortion caused only by the new installation into the existing distortion using Equations (5.3) and (5.4). The results are shown in Table 5.6.

Table 5.6 Results of harmonic distortion at PCC1

Order *h*	3	5	7	9	11	13	15	THD
V_{hm} (%)	3.98	1.88	0.45	0.22	0.19	0.12	0.11	4.44
V_{hp} (%)	5.80	2.68	0.54	0.27	0.21	0.13	0.14	6.43

It is noted that THDV exceeds the limit although the 5th harmonic distortion is less than the limit. This is due to the excessive 3rd order harmonic current. If the 3rd order harmonic current emission is reduced, THDV at the PCC1 can be within the planning level. It is, therefore, recommended applying mitigation measures at PCC1 in order to connect the installation to the supply network.

C. At PCC2

PCC2 on 28/F is selected for assessing the possibility of connection without mitigation. For simplicity of discussion, the new installation is identical to the existing one on 28/F. As the background levels at PCC2 shown in Table 5.2 exceeds 75% of the planning levels, the Stage-Two assessment using the simple reactance model becomes necessary. Table 5.7 shows the predicted values of resultant harmonic voltage at PCC2. It is noted that the predicted THDV at PCC2 is greater than the planning level of 5%. In fact, the existing background level exceeds the planning level already. No connection is allowed even though a mitigation measure is applied to the new installation. The connection may be possible if the existing background levels are reduced to be lower than the planning levels.

Table 5.7 Results of harmonic distortion at PCC2

Order h	3	5	7	9	11	13	15	THD
V_{hm} (%)	5.58	2.64	0.63	0.31	0.26	0.17	0.16	6.22
V_{hp} (%)	5.70	2.73	0.63	0.32	0.26	0.17	0.17	6.36

5.3 Discussion on Harmonic Regulation in High-rise Buildings

5.3.1 Reliable Assessment

The harmonic evaluation normally is carried out at the point of common coupling (PCCs). The utility considers the whole LV distribution system as one node. Only the entrance of the electrical service is concerned and limited within the planning level of 5%. Because of the special features of building distribution systems, it is difficult to have a constant voltage distortion level in the whole system. This means on the down stream of the electrical entrance harmonics must exceed the harmonic limits even if the voltage at the electrical entrance complies with the limits. In order to ensure the qualified power, it may be important to regulate the harmonic limits in high-rise buildings.

By following the assessment procedure in ER G5/4, the resultant harmonic voltage distortion at the PCC after the connection will be probably less than the planning levels as well as the compatibility levels given in IEC 61000-2-2. In fact, the harmonic current emission limits used in ER G5/4 are derived from the planning levels by using an impedance model of the system. The voltage distortion caused by the new installation will not exceed 25% of the planning levels even if the harmonic emissions reach the maximum limits. As long as the background levels are less than 75% the planning levels, the resultant voltage

distortion will meet the planning levels at PCC. This minimizes the risk of harmonic problems and ensures the compatibility of harmonics in the whole system although the connection requirements are stricter in some aspects than other standards.

5.3.2 Harmonic Current Limits in High-rise Buildings

The maximum permissible harmonic current emission in ER G5/4 is based on the fault level values at the PCC. The PCC in the system is defined by ER G5/4 as the point in the public Supply System, electrically nearest to a customer's installation, at which other customers' loads are, or may be, connected. The customer may demonstrate compliance on the basis of specific fault level information for the proposed PCC provided to the customer by the utility. In Hong Kong, the distribution transformers in buildings normally are owned by the utility. From the point of the view of the utility, the LV distribution system as a whole is the PCC. Hence, the fault level of the PCC should be the information at the secondary of the transformer, that is, the PCC1 in the thesis. This PCC is an average node utilized to assess the harmonic distortion of the LV system.

However, from the points of the view of the tenant and the landlord the LV distribution system is considered as a small-scale distribution system, instead of

a dimensionless bus node. The fault level on upper floors is smaller than that at PCC1. It is of risk to assess the new loads' connection to the distribution system by using the harmonic limits at PCC1. The resultant harmonic voltage distortion on the system would be much more serious than expected.

One of the solutions is that the harmonic limits are calculated according to the fault level at the point of connection. Therefore, PCC2s should be defined in the distribution system for the assessment of harmonics, which are located at the position of local distribution boards in meter rooms. For simplicity of assessment and management, the fault level of the top of the distribution circuit may be used. Since the impedance of the distribution circuit is already taken into account, the maximum permissible currents become more conservative.

5.3.3 Expanding The Judging Terms in Harmonics Regulation

The 5^{th} harmonics is one of the increasing harmonic components in recent years. It is selected in ER G5/4 to be an indicator for judging whether or not the installation can be connected without mitigation. In fact, the 3^{rd} harmonic component is still dominant in the LV distribution systems of local buildings. It is unwise to judge by the 5^{th} harmonic voltage distortion without considering the richest harmonic component. It is understood that the triple order harmonics are usually blocked at the distribution transformer because of its delta/star

connection. These harmonics, however, may cause a problem in LV distribution systems because of excessive voltage and current at triple-n orders. Table 5.8 and Table 5.9 present the harmonic voltage distortion measured at PCC1 selected from a survey. [Y. Du etc. 1998a] It is observed in Table 5.8 that the harmonic voltage distortions of the 3rd and 5th harmonics are both severe in all three types of connections. In Table 5.9, the 3rd harmonic distortion in Government offices reaches its extreme. Therefore, it would be necessary to include the 3rd order harmonic voltage distortion in judging the connection together with the 5th order harmonic voltage distortion and total harmonic voltage distortion at PCCs. Further, for the specific case, such judging terms for the harmonic regulation in buildings should be determined by the real situation of the case. If the 7th harmonic is most dominant, the judging terms may be extended to consider the 7th harmonic also.

Table 5.8 Measured voltage distortion at PCC1 in % of 220V

	Tenant connection		Landlord connection		Mixed connection	
	Max	Mean	Max	Mean	Max	Mean
V_3 (%)	8.38	3.10	2.01	0.76	3.03	0.91
V_5 (%)	7.77	4.09	1.68	1.12	5.47	1.90

Table 5.9 Measured voltage distortion at PCC1 in % of 220V

	Commercial Tenants		Government offices	
	Max	Mean	Max	Mean
V_3 (%)	12.2	7.40	23.5	11.3
V_5 (%)	3.74	2.20	7.60	4.61

5.4 Responsibility in Harmonic Control

5.4.1 Responsibilities of All Parties

Three parties, i.e. the utility, the landlord and the tenant, are normally involved in power supply and utilization in buildings. ER G5/4 provides an alternative approach to implement harmonic regulation and management in such electrical systems. It is not only more comprehensive to share the responsibilities among all the parties in building distribution systems, but also more feasible to achieve harmonic control in buildings.

According to foregoing parts, the PCC0 in the typical LV distribution system is the interface of the utility and the building (including the landlord and the tenant), and the riser (PCC2) is the interface of the landlord and the tenant. It is noted that there are two power-providers, namely the utility for the landlord and the landlord for the tenant. Also, there are two power-consumers, the landlord and the tenant. It is commonly recognized that the utility is responsible for the harmonic voltage distortion at PCC1, meanwhile the tenant is responsible for harmonic emission from their loads. However, it is impossible for the utility to identify and monitor all of the harmonic sources in the building.

It is natural that a customer is responsible for limiting the harmonic currents

from the tenant's equipment at PCC2 according to equipment-level standards. A landlord needs to take necessary measure to ensure voltage quality over the building distribution system to all customers within the building. On the other hand, the landlord needs to take necessary measures to ensure the harmonic current emission at PCC1 in accordance with the harmonic limits. The utility is responsible for voltage quality at PCC1.

5.4.2 Necessity of Applying Mitigation Measures

Although ER G5/4 makes it possible for a landlord to manage harmonics practically, there are still cases uncovered. In ER G5/4, planning levels were set against nominal system voltage. At 400V, the planning level of THDV is equal to 5%. This figure is applied to the whole LV distribution system in a building no matter where the customer is located, either on the ground or on the 50^{th} floor of a high-rise building. In fact, because of the non-trivial impedance of a distribution circuit the voltage drop is comparable to the harmonic voltage at PCC1. A survey on the LV distribution system of a building was carried out and published in [Y. Du etc. 1998a]. Thirteen buildings were selected, which had sixteen to fifty stories high except for one with three stories. The measurements were taken at PCC1 and PCC2 during office hours. Both Fluke 41 and Dranetz PPP1 were used to collect data. Table 5.11 and 5.12 present the results of measurements.

Table 5.10 Harmonics at PCC1

	Tenant connection		Landlord connection		Mixed connection	
	MAX	MEAN	MAX	MEAN	MAX	MEAN
Irms (A)	1904	1256	952	568	1470	706.
Ithd (%)	26.5	**15.8**	12.3	**9.13**	20.4	**11.0**
Vrms (V)	226	219	223	220	225	221
Vthd (%)	8.50	**5.79**	2.79	**1.84**	6.63	**2.57**

In Table 5.10, both maximum and mean values are presented due to the variation of harmonic levels at sites. At PCC1, the buildings were classified into three groups such as tenant connection, landlord connection and mixed connection according to the connection of LV distribution systems.

Table 5.11 Harmonics at PCC2 (local distribution boards)

	Commercial tenants		Government offices	
	MAX	MEAN	MAX	MEAN
Irms (A)	129	64.0	70.7	31.1
Ithd (%)	37.4	**23.3**	36.2	**20.0**
Vrms (V)	223	217	224	216
Vthd (%)	12.3	**7.92**	17.0	**11.9**

At PCC2, the harmonics of commercial tenants and government offices were selected to show in Table 5.11. It was concluded from the data that the harmonic distortion was more serious than that at PCC1. It was reported that the harmonics in lifts, small power circuits and A/C power circuits were most severe. In the survey, the total harmonic voltage distortion on risers can be over 10% in local buildings, and 17% in an extreme case. Figure 5.3 depicts the variation of THD_V along the raising main circuits in one office building. The

whole building is separated into three zones: low zone (1/F - 13/F), middle zone (14/F - 31/F) and high zone (32/F - 48/F). This figure shows that the level of total harmonic voltage distortion increases with floor No.. The most serious voltage distortion (THD_V =16.3%) occurs on the topmost floor. Similar distortion patterns are observed in other buildings.

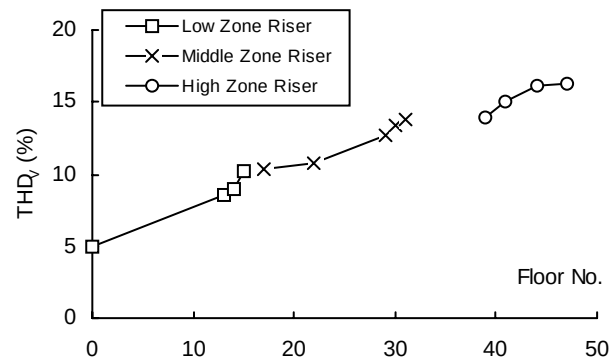

Figure 5.3 THD of voltage in one office building

Therefore, it is very difficult to keep the total harmonic distortion within 5% at PCC2 even if the total harmonic distortion at PCC1 is close to 5%. The harmonic assessment in buildings provides a tool for the landlord to manage harmonics. Although it may maximally regulate the harmonics in the building to reduce the risk of harmonic pollution, the uncertainties such as unavailable information and variable loading may cause excessive harmonic voltage distortion along the distribution circuits. Additionally, the demand of the harmonic-producing loads may increase with the coming of the new tenants, which requires the building LV distribution system to have a larger harmonic capacity. These indicate that the measures of harmonic mitigation should be applied in the building distribution systems.

It is suggested that the landlord be responsible for installing the mitigating devices to control harmonics in the distribution systems. The landlord is responsible for mitigating harmonic currents at PCC1, meanwhile maintaining qualified voltage over the system. Correspondingly, the concept of harmonic tariff may be possibly implemented in buildings. Customers pay the landlord for excessive harmonic currents injected into the building distribution systems. The landlord takes care of these harmonic currents and provides quality voltage over the system by installing system-level mitigation devices, such as voltage-detection shunt active power filters, as proposed in later chapters.

5.5 Summary

In this chapter, harmonic regulation in high-rise buildings was investigated. Based on ER G5/4, a procedure of harmonic assessment was developed, and applied to the building LV distribution systems. Some adjustments, such as expanding the judging terms were made considering the special features of the distribution systems in high-rise commercial buildings.

The responsibilities in harmonic control in commercial buildings are then recommended. The landlord is responsible for the harmonic currents injected to the utility network at PCC1, and the harmonic voltage to the tenant within the

building. The utility is responsible for voltage quality at PCC1 while the tenant is responsible for the current emission from their loads at PCC2.

Chapter 6

Proposed Shunt Active Power Filter and Its Analytical Analysis

6.1 Introduction

In this chapter, a shunt active power (SAPF) filter based on voltage detection method is presented to control harmonic voltage in a building distribution system. The harmonic voltage distortion is suppressed by injecting appropriate harmonic currents into the system. This proposed voltage-detection SAPF has a novel multi-channel complex gain controller, which is designed to improve the system stability margin and to make the output of the SAPF tunable. A system model of both the proposed SAPF and a typical building distribution system is developed. Transfer functions in the s domain are derived for both SAPF and distribution components in multiple reference frames. Characteristics of the proposed SAPF in the system are then investigated in the frequency domain. Both stability and performance of the proposed SAPF connected to the distribution system are discussed finally.

6.2 Proposed Shunt Active Power Filter

Shown in Figure 6.1 is the configuration of a representative voltage-detection SAPF connected to a building distribution system. For simplicity, only one

distribution transformer and one distribution circuit are presented in the figure. In order to control harmonic voltage distortion along the circuit, the SAPF is installed on the upper floor near the end of the circuit, as recommended in [Keiji Wada etc. 2002].

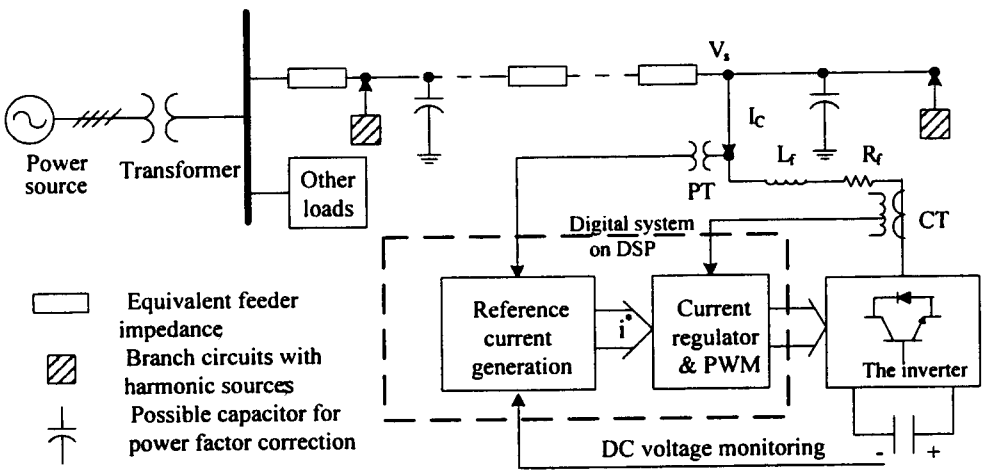

Figure 6.1 Configuration of a SAPF connected to a building distribution system

The proposed SAPF detects system voltages at the point of connection with potential transformers. These voltages are conditioned by analogue conditioning circuits, and are converted into digital signals in the controller by analogue-to-digital converters (ADs). Harmonic components V_h are extracted from these digital voltages, and reference currents i_h are generated in the controller, as seen in Figure 6.1 and Figure 6.2. With the current controller and the PWM technique, the demanding voltage is outputted to the power device. The output currents or the compensating currents, which track the current reference signals, are obtained via the output voltages applied on the output

inductors. The block diagram of the SAPF is presented in Figure 6.2.

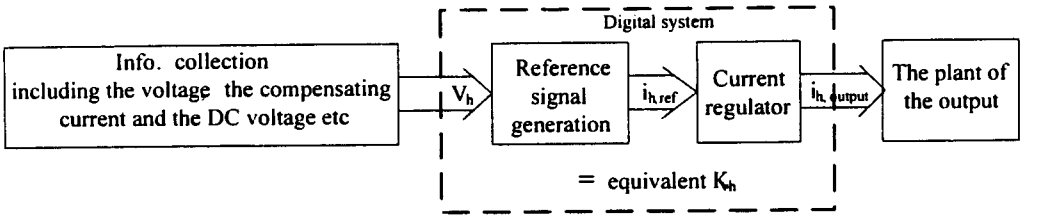

Figure 6.2 Block diagram of the proposed SAPF

6.2.1 Power Circuit

Shown in Figure 6.3 is the power circuit of the SAPF based on a voltage detection method. The power circuit is comprised of a three-phase four-pole voltage-fed inverter, a DC capacitor and output inductors. Each pole of the inverter consists of two series-connected IGBTs with an inverse parallel diode each. As the output plant of the SAPF, the smoothing inductors connect the inverter to the distribution system.

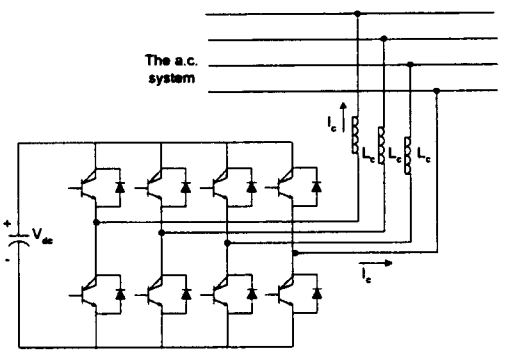

Figure 6.3 Power device of the SAPF

6.2.2 Multi-Channel Complex Gain Controller

The gain controller in a SAPF is designed to generate reference current signals. The diagram in Figure 6.4 shows the algorithm used in the multi-channel complex-gain controller. The controller receives the measured three-phase and DC-side voltages, and processes these signals in three different channels, namely positive, negative and zero sequence channels. A DC channel is also included in the controller to generate a reference current signal for remaining the DC-bus voltage. The outputs of these channels are summed to form the reference current signals, which will be processed by the current regulator at the next stage.

Three voltages in the a-b-c frame are firstly transformed into the components in the α-β-γ frame by the Clarke transformation, as shown in Equation (6.1).

$$\begin{bmatrix} V_\alpha \\ V_\beta \\ V_\gamma \end{bmatrix} = \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ 0 & 1/\sqrt{3} & -1/\sqrt{3} \\ 1/3 & 1/3 & 1/3 \end{bmatrix} \cdot \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{6.1}$$

Voltages V_α and V_β contain both positive and negative components, while voltage V_γ contains all zero-sequence components. Harmonic components are extracted from these signals via the transformation in the d-q synchronous frame. To obtain positive and negative sequence components at harmonic order h, both voltages V_α and V_β are transformed to V_d and V_q in the d-q frame by the Park transformation as,

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \sin(\pm h\omega t) & -\cos(\pm h\omega t) \\ \cos(\pm h\omega t) & \sin(\pm h\omega t) \end{bmatrix} \cdot \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{6.2}$$

where symbols "-" and "+" are used for the negative-sequence and

positive-sequence components, respectively. Symbol "ω" is the fundamental angle frequency. Equation (6.2) transforms the harmonic quantities of order h in the α-β-0 reference frame into the DC quantities in the harmonic synchronous d-q reference frame. It is noted that a Butterworth low-pass filter (LPF) has a unitary gain at the DC frequency and significant attenuation at other harmonic frequencies. After applying the LPF on voltages V_d and V_q, these DC components remain in the channels, and other components attenuate significantly. The outputs are represented by $v_{d,dc}$ and $v_{q,dc}$.

The current reference signals are the commanding signals for the current regulator. Under the ideal condition, the compensating currents are exactly the same as the reference ones. The SAPF can be viewed as a pure resistor installed at the point of connection at each harmonic order, as illustrated in Equation (6.3).

$$\begin{aligned} i_d &= k_{vh} \cdot V_{d,dc} \\ i_q &= k_{vh} \cdot V_{q,dc} \end{aligned} . \qquad (6.3)$$

where k_{vh} is the equivalent control gain at order *h*.

Because of time delay and limited frequency bandwidth introduced in the controller, the filter performance is degraded. It is necessary to add leading compensation in the controller for. The compensation should be made in both amplitude and phase angle of the current reference. By the inverse Park transformation, the reference current signals at order h in the synchronous frame

(d-q) are transformed into those in the stationary frame (α-β), as shown in Equation (6.4).

$$\begin{bmatrix} i_{\alpha h} \\ i_{\beta h} \end{bmatrix} = \begin{bmatrix} \sin\left(h\omega t + \alpha_h\right) & \cos\left(h\omega t + \alpha_h\right) \\ -\cos\left(h\omega t + \alpha_h\right) & \sin\left(h\omega t + \alpha_h\right) \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{6.4}$$

where α_h is the phase angle at order h for phase compensation. It is noted that one channel is designed for one harmonic order so that Equation (6.4) can be easily implemented in the synchronous frame (d-q frame), as shown in Figure 6.4. Both d-axis and q-axis currents in one channel, i_d and i_q now become,

$$i_d = V_{d.dc} \cdot \left|k_{vh}\right| \cdot \cos\left(\alpha_h\right) \pm V_{q.dc} \cdot \left|k_{vh}\right| \cdot \sin\left(\alpha_h\right) \tag{6.5}$$

$$i_q = \mp V_{d.dc} \cdot \left|k_{vh}\right| \cdot \sin\left(\alpha_h\right) + V_{q.dc} \cdot \left|k_{vh}\right| \cdot \cos\left(\alpha_h\right) \tag{6.6}$$

Where the signs of "$\pm, \mp$" in the Equations are for positive sequence and negative sequence components, respectively. Here, phase angle α_h can be considered as the angle of gain k_{vh}. Hence, gain k_{vh} is a complex number at order h in the synchronous d-q reference frame, and expressed by $\left|k_{vh}\right| \angle \alpha_h$. The amplitude $\left|k_{vh}\right|$ and the angle α_h are both adjustable. Consequently, the reference current signals in the stationary reference frame output to the current regulator is obtained by the inverse Park transformation, as shown in Equation (6.7).

$$\begin{bmatrix} i_{\alpha h} \\ i_{\beta h} \end{bmatrix} = \begin{bmatrix} \sin\left(h\omega t\right) & \cos\left(h\omega t\right) \\ -\cos\left(h\omega t\right) & \sin\left(h\omega t\right) \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix} \tag{6.7}$$

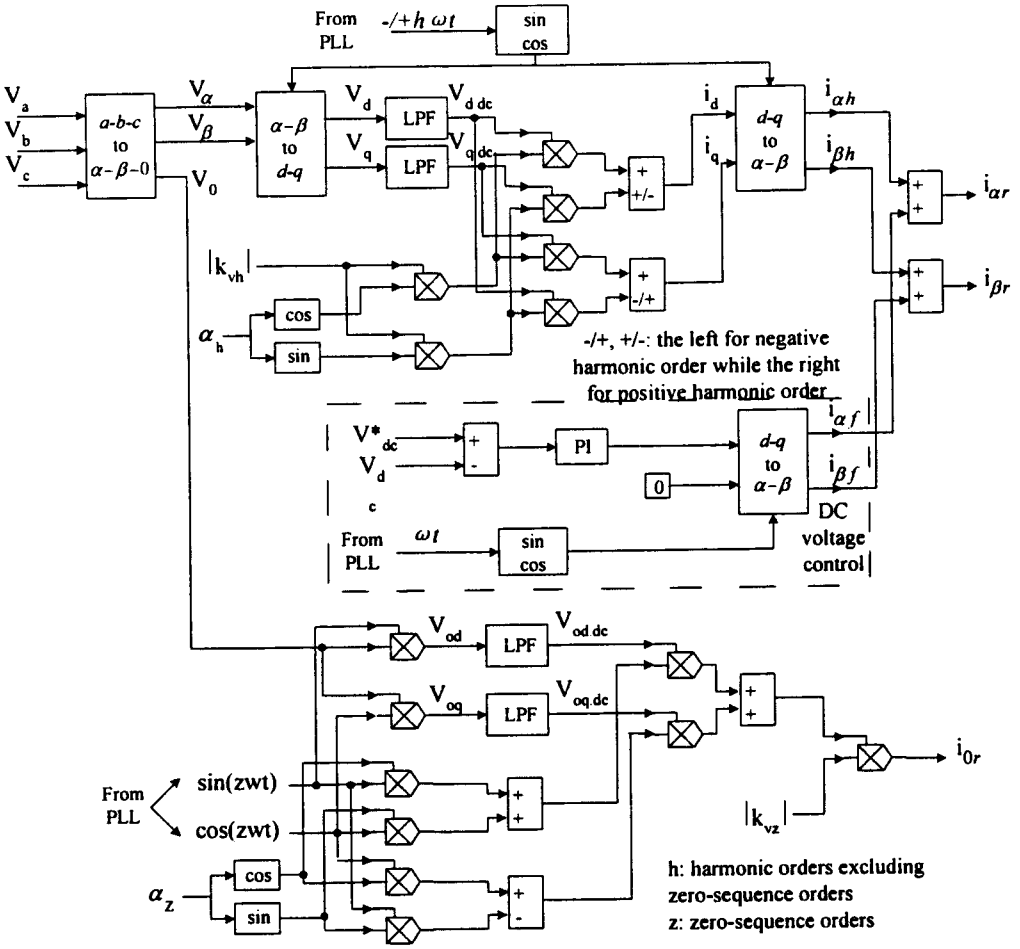

Figure 6.4 Generation of current reference signals

The process of extracting zero sequence components V_{0z} at order z is different from that of extracting non-zero-sequence components. As the zero-sequence components are all in phase, the normal formulation of Park transformation can not be applied to extract harmonic components of the zero sequence quantities. In the proposed controller, the orthogonal transformation is applied to the zero-sequence quantities. As a result, two quantities V_{od} and V_{oq} at order z are obtained as follows,

$$V_{od} = V_o * \sin(z\omega t) \tag{6.8}$$

$$V_{oq} = V_O * \cos(zwt) \tag{6.9}$$

Consequently, the zero-sequence components at order z is transformed to DC quantities while others are transformed to the quantities at the frequencies of $\pm 6n, (n = 1, 2, 3...)$. The Butterworth LPF is applied again, and the DC quantities from the LPF are obtained as follows,

$$V_{od,dc} = \frac{1}{2} V_z \cdot \cos(\alpha_{z0}) \tag{6.10}$$

$$V_{oq,dc} = \frac{1}{2} V_z \cdot \sin(\alpha_{z0}) \tag{6.11}$$

where Both V_z and α_{z0} are the amplitude and initial phase angle of zero-sequence component at order z, respectively. Similar to the non-zero-sequence components, leading compensation is introduced here again by. $|k_{vz}|$ and α_z. The following the reference current at order z in the static frame is expressed by

$$i_z = \frac{1}{2} |k_{vz}| \cdot V_z \cdot \sin(zwt + \alpha_{z0} + \alpha_z) \tag{6.12}$$

It is indicated in Equation (6.12) that the reference current signal at order z is controlled by complex gain k_{vz} in both the amplitude and the phase angle. Equation (6.12) can be rewritten in terms of quantities, $V_{od,dc}$ and $V_{oq,dc}$, as seen in Figure 6.4, and is expressed by,

$$i_z = |k_{vz}| \cdot \left[(\sin(zwt) \cdot \cos(\alpha_z) + \cos(zwt) \cdot \sin(\alpha_z)) \cdot V_{od,dc} + (\cos(zwt) \cdot \cos(\alpha_z) - \sin(zwt) \cdot \sin(\alpha_z)) \cdot V_{oq,dc} \right] \tag{6.13}$$

The current reference signal i_{or} in Figure 6.4 is the summation of the reference signals from all channels for zero-sequence quantities.

The DC module in the controller is intended to keep the DC bus voltage stable.

PI control is employed in the controller to generate the reference signal from the error of the detected DC-bus voltage v_{dc} and its reference value v_{dc}^{*}, as shown in Figure 6.4. In order to provide active power to the DC bus to maintain the DC voltage constant, the output of the PI control is a d-axis component, and the corresponding q-axis component is set to be zero. The inverse Park transformation based on the fundamental rotating vectors is then applied to transform the d-q quantities into the α-β quantities. Obviously, these α-β quantities $i_{\alpha f}$ and $i_{\beta f}$ are the reference signals at the fundamental frequency, as shown in Figure 6.4. Finally, these fundamental reference signals and all reference signals from other e channels are summed, and the results $i_{\alpha r}$ and $i_{\beta r}$ are the final reference signals outputted to the current controller.

6.2.3 Current Regulator

A current regulator is designed to output compensating currents by tracking the reference current signals obtained from the multi-channel complex gain controller. The current regulator contains two major parts: the generation of the commanding voltage and the PWM scheme to produce the pulse signals for power devices.

I. Generation of the commanding voltage

In the current regulator the error between the compensating currents and the

reference current signals is processed to generate the commanding voltage which is used to reduce the error in the next switching period. Literatures [Simone Buso etc. 1998, Luigi Malesani etc. 1997, Luigi Malesani etc. 1999] have been published to discuss different control methods used in the current regulator, including the proportional control, the predictive control/deadbeat control and the hysteresis control etc.. For the sake of simplicity, the proportional (P) control is applied in this current regulator to generate the commanding voltages used in the PWM scheme. The P control is one of the common and simple control methods in the application. It has constant amplitude-frequency and zero phase-frequency characteristics, which eliminate the phase lag or lead in this part. Although different control methods may have different effects on the performance of a SAPF, it is undoubted that a basic approximation for the performance of the proposed SAPF will be provided using the P control. The output of the P controller is sent to the PWM scheme as the commanding voltage.

II. PWM scheme based on the three-dimensional space vector method [Richard Zhang etc. 2002, Manuel A. Perales etc. 2003]

With the commanding voltages from the current regulator, the PWM scheme generates the pulse signals for switching operation of the power devices. As shown in Figure 6.2, the four-leg topology of the inverter is adopted in the proposed SAPF. This topology can effectively provide the neutral connection in

a three-phase four-wire system. Therefore, a three-dimensional space vector modulation (SVM) is used for the four-leg voltage-source inverter. The three-dimensional SVM has been broadly used in the application of inverters, rectifiers, and active filters to handle the neutral current caused by the unbalanced and/or nonlinear loads.

The purpose of SVM is to synthesize the commanding voltage as the switching vectors which are represented by the switching signals for operation of the converter. The three-dimensional SVM is a superset of the traditional two-dimensional SVM. It inherits all the merits of the traditional two-dimensional SVM. In the following part, the three-dimensional SVM adopted for the proposed SAPF is presented, including the definition of the switching vectors, the method to synthesizing the reference vector and the sequence scheme of the switching vectors.

With a pulse width modulation control, [Richard Zhang etc. 2002] the AC terminal voltages of the switching network are pulsating in a switching period. The average values of a switching period can represent the transient value of the AC terminal voltages. After a cycle-by-cycle averaging process, the average AC terminal voltages are expressed as

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \begin{bmatrix} d_{an} \\ d_{bn} \\ d_{cn} \end{bmatrix} \cdot V_{dc} \tag{6.14}$$

where d_{an}, d_{bn}, and d_{cn} are line-to-neutral duty ratios, and V_{dc} is the DC-bus

voltage.

With the neutral connection, the sum of the three-phase variables is not always zero. It is suggested that any commanding vector V_{ref} be represented by three independent variables in a three-dimensional orthogonal coordinate, that is, the α-β-γ coordinates as,

$$V_{ref} = V_\alpha + jV_\beta + kV_\gamma \tag{6.15}$$

where v_α, v_β, and v_γ are the vectors in the α, β, and γ axes. The symbols of "j" and "k" are the basic vectors in the β and γ directions, respectively. The transformation of the a-b-c frame to the α-β-γ frame is expressed as Equation (6.2), and the inverse transformation is as follows,

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 \\ -1/2 & \sqrt{3}/2 & 1 \\ -1/2 & -\sqrt{3}/2 & 1 \end{bmatrix} \cdot \begin{bmatrix} V_\alpha \\ V_\beta \\ V_0 \end{bmatrix} \tag{6.16}$$

The total number of the switching vectors is sixteen because of four legs in the system. The switching vectors can be represented by the ordered sets $[s_a \;\; s_b \;\; s_c \;\; s_n]$, which represents the switching states of phase A, B, C and N. s_a=1 denotes that the upper device in phase A is open, and s_a=0 denotes that the bottom device in phase A is closed. The same notation is applied to other phases. It is noted that there are tow zero switching vectors, denoted "0000" and "1111", and others are non-zero switching vectors. Once the combination of the switching states is specified, the terminal voltage is also obtained. Table 6.1 shows the line-to-neutral voltages for all sixteen switching combinations. By applying the Clark transformation, the AC terminal voltages in the α-β-γ frame

are also derived and shown in Table 6.2.

Table 6.1 Phase voltages for all sixteen switching combinations in the a-b-c frame

	1110	0110	1010	1100	0010	0100	1000	0000
V_{an}	V_{dc}	0	V_{dc}	V_{dc}	0	0	V_{dc}	0
V_{bn}	V_{dc}	V_{dc}	0	V_{dc}	0	V_{dc}	0	0
V_{cn}	V_{dc}	V_{dc}	V_{dc}	0	V_{dc}	0	0	0
	0001	0011	0101	1001	0111	1011	1101	1111
V_{an}	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$	0	$-V_{dc}$	0	0	0
V_{bn}	$-V_{dc}$	$-V_{dc}$	0	$-V_{dc}$	0	$-V_{dc}$	0	0
V_{cn}	$-V_{dc}$	0	$-V_{dc}$	$-V_{dc}$	0	0	$-V_{dc}$	0

Table 6.2 Voltages for all sixteen switching combinations in the α-β-γ frame

	1110	0110	1010	1100	0010	0100	1000	0000
V_{α}	0	$-2/3\cdot V_{dc}$	$1/3\cdot V_{dc}$	$1/3\cdot V_{dc}$	$-1/3\cdot V_{dc}$	$-1/3\cdot V_{dc}$	$2/3\cdot V_{dc}$	0
V_{β}	0	0	$-1/\sqrt{3}\cdot V_{dc}$	$1/\sqrt{3}\cdot V_{dc}$	$-1/\sqrt{3}\cdot V_{dc}$	$1/\sqrt{3}\cdot V_{dc}$	0	0
V_{γ}	V_{dc}	$2/3\cdot V_{dc}$	$2/3\cdot V_{dc}$	$2/3\cdot V_{dc}$	$1/3\cdot V_{dc}$	$1/3\cdot V_{dc}$	$1/3\cdot V_{dc}$	0
	0001	0011	0101	1001	0111	1011	1101	1111
V_{α}	0	$-1/3\cdot V_{dc}$	$-1/3\cdot V_{dc}$	$2/3\cdot V_{dc}$	$-2/3\cdot V_{dc}$	$1/3\cdot V_{dc}$	$1/3\cdot V_{dc}$	0
V_{β}	0	$-1/\sqrt{3}\cdot V_{dc}$	$1/\sqrt{3}\cdot V_{dc}$	0	0	$-1/\sqrt{3}\cdot V_{dc}$	$1/\sqrt{3}\cdot V_{dc}$	0
V_{γ}	$-V_{dc}$	$-2/3\cdot V_{dc}$	$-2/3\cdot V_{dc}$	$-2/3\cdot V_{dc}$	$-1/3\cdot V_{dc}$	$-1/3\cdot V_{dc}$	$-1/3\cdot V_{dc}$	0

It is noted that these switching vectors are located regularly in the three-dimensional orthogonal space. They are distributed in seven layers according to the values of the γ axis, V_{γ}. These layers are at the values of $\pm V_{dc}$, $\pm\frac{2}{3}V_{dc}$, $\pm\frac{1}{3}V_{dc}$, and zero. Figure 6.5 shows the three-dimensional structure. It can be seen that the projection of all the vectors on the α-β coordinate forms a hexagon, which is same as the switching vectors of two-dimensional SVM.

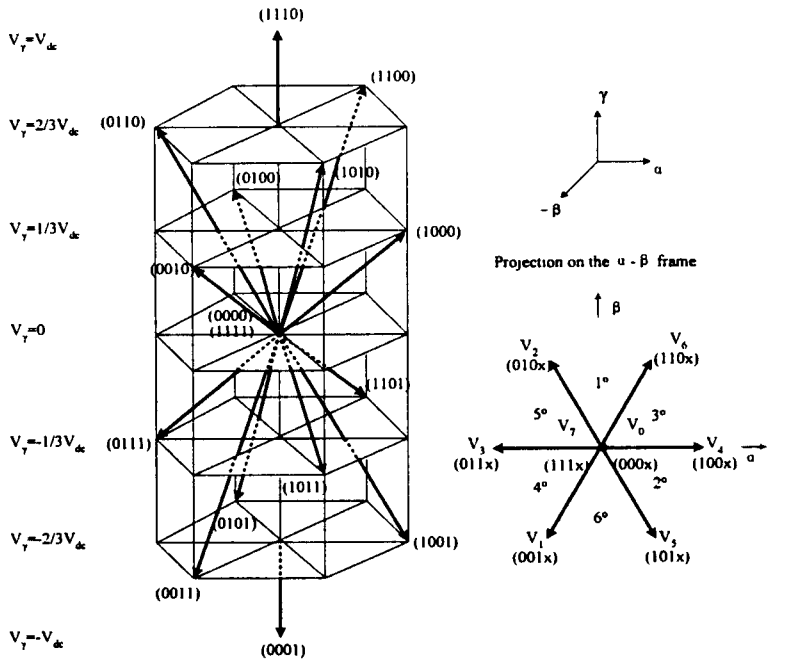

Figure 6.5 The structure of the three-dimensional space vector

For the application of proposed SAPF, the commanding voltages are generated and sent to the algorithm of the three-dimensional SVM. These voltages are demodulated and finally realized by the related switching vectors. Normally, there are two steps to apply three-dimensional SVM: synthesizing the commanding voltage and sequencing of the switching vectors.

From Figure 6.5, all the sixteen switching vectors divide the space into twenty-four small spaces at one of which any commanding voltage can locate. The projections of the switching vectors on the α-β plane divide the space into six prisms, and each prism contains four sectors. Each sector is enclosed by three non-zero switching vectors. The step of synthesis of the commanding voltage is to determine which sector the commanding signal is located, and to

determine the projection of the reference signal on the adjacent switching vectors. It takes two steps, namely prism identification and sector identification, to determine the location of the commanding voltage. The projection of six prisms on the α-β coordinate indicates that the identification of the prism can refer to the method used on the two-dimensional SVM. Based on the projection of the reference voltage on the α-β plane, the prism marked 1º to 6º as shown in Figure 6.5 is identified. To be easily implemented, the prism identification method is realized by the following algorithm:

- The projections are calculated as

$$\begin{bmatrix} V_{ref1} \\ V_{ref2} \\ V_{ref3} \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ \sqrt{3}/2 & -1/2 \\ -\sqrt{3}/2 & -1/2 \end{bmatrix} \cdot \begin{bmatrix} V_{\alpha ref} \\ V_{\beta ref} \end{bmatrix} \tag{6.17}$$

- The prism is determined by

If v_{ref1}>0, then A=1,

If v_{ref2}>0, then B=1,

If v_{ref3}>0, then C=1, and the number of the prism is $A+2\cdot B+4\cdot C$.

The sector in a prism is determined by the number of positive sign of line-to-neutral voltages. Table 6.3 lists all combinations of any three adjacent switching vectors. Each combination forms a tetrahedron as one sector. The symbols “+”, “-” or “0” are the sign of the line-to-neutral voltage. For example, the vector “0101” resulting in “-0-” means the line-to-neutral voltages are “0-to-1”, “1-to-1” and “0-to-1” for phase A, B and C, respectively. It is noted that for the switching vectors in each sector the signs of the line-to-neutral

voltages are non-conflicting. It is indicated that the number of the sector can be represented by the number of the positive signs. For example, the switching vectors in sector 2 have two positive signs of three vectors. However, it seems to be difficulty to obtain the number of the positive signs in the α-β-γ frame. A simple algorithm in the a-b-c frame is developed. By using the inverse Clark transformation, the reference voltages in the α-β-γ frame are transformed to the voltages in the a-b-c reference frame. For each sector, the voltage polarities in the two coordinates are both non-conflicting and with the same sets.

Table 6.3 The combination of three adjacent switching vectors

Prism\Sector	0	1	2	3
1º	V1=0001, --- V2=0101, -0- V3=1101, 00-	V1=0100, 0+0 V2=0101, -0- V3=1101, 00-	V1=0100, 0+0 V2=1100, ++0 V3=1101, 00-	V1=0100, 0+0 V2=1100, ++0 V3=1110, +++
2º	V1=0001, --- V2=1001, 0-- V3=1011, 0-0	V1=1000, +00 V2=1001, 0-- V3=1011, 0-0	V1=1000, +00 V2=1010, +0+ V3=1011, 0-0	V1=1000, +00 V2=1010, +0+ V3=1110, +++
3º	V1=0001, --- V2=1001, 0-- V3=1101, 00-	V1=1000, +00 V2=1001, 0-- V3=1101, 00-	V1=1000, +00 V2=1100, ++0 V3=1101, 00-	V1=1000, +00 V2=1100, ++0 V3=1110, +++
4º	V1=0001, --- V2=0011, --0 V3=0111, -00	V1=0010, 00+ V2=0011, --0 V3=0111, -00	V1=0010, 00+ V2=0110, 0++ V3=0111, -00	V1=0010, 00+ V2=0110, 0++ V3=1110, +++
5º	V1=0001, --- V2=0101, -0- V3=0111, -00	V1=0100, 0+0 V2=0101, -0- V3=0111, -00	V1=0100, 0+0 V2=0110, 0++ V3=0111, -00	V1=0100, 0+0 V2=0110, 0++ V3=1110, +++
6º	V1=0001, --- V2=0011, --0 V3=1011, 0-0	V1=0010, 00+ V2=0011, --0 V3=1011, 0-0	V1=0010, 00+ V2=1010, +0+ V3=1011, 0-0	V1=0010, 00+ V2=1010, +0+ V3=1110, +++

The reference voltage is achieved by the switching vectors with different duties as given,

$$V_{ref} = d_1 \cdot V_1 + d_2 \cdot V_2 + d_3 \cdot V_3 + d_z \cdot V_z \tag{6.18}$$

where d_1, d_2, d_3, d_z are the duties of the non-zero switching vectors V_1, V_2, V_3 and zero switching vector V_z, respectively. The duties of each vector can be calculated from the projections of the reference voltage on the selected non-zero switching vectors.

$$\begin{bmatrix} d_1 \\ d_2 \\ d_3 \end{bmatrix} = \frac{1}{V_{dc}} \cdot T_{3\times3} \cdot \begin{bmatrix} V_{\alpha ref} \\ V_{\beta ref} \\ V_{\gamma ref} \end{bmatrix} \tag{6.19}$$

$$d_z = 1 - d_1 - d_2 - d_3 \tag{6.20}$$

All the related matrixes $T_{3\times3}$ are calculated and presented in Table 6.4.

Table 6.4 The related matrixes for the three-dimensional space vector PWM

Prism\Sector	0	1	2	3
1º	$\begin{bmatrix} 1/2 & -\sqrt{3}/2 & -1 \\ -3/2 & \sqrt{3}/2 & 0 \\ 3/2 & \sqrt{3}/2 & 0 \end{bmatrix}$	$\begin{bmatrix} -1/2 & \sqrt{3}/2 & 1 \\ -1 & 0 & -1 \\ 3/2 & \sqrt{3}/2 & 0 \end{bmatrix}$	$\begin{bmatrix} -3/2 & \sqrt{3}/2 & 0 \\ 1 & 0 & 1 \\ 1/2 & \sqrt{3}/2 & -1 \end{bmatrix}$	$\begin{bmatrix} -3/2 & \sqrt{3}/2 & 0 \\ 3/2 & \sqrt{3}/2 & 0 \\ -1/2 & -\sqrt{3}/2 & 1 \end{bmatrix}$
2º	$\begin{bmatrix} -1 & 0 & -1 \\ 3/2 & \sqrt{3}/2 & 0 \\ 0 & -\sqrt{3} & 0 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 & 1 \\ 1/2 & \sqrt{3}/2 & -1 \\ 0 & -\sqrt{3} & 0 \end{bmatrix}$	$\begin{bmatrix} 3/2 & \sqrt{3}/2 & 0 \\ -1/2 & -\sqrt{3}/2 & 1 \\ 1/2 & -\sqrt{3}/2 & -1 \end{bmatrix}$	$\begin{bmatrix} 3/2 & \sqrt{3}/2 & 0 \\ 0 & -\sqrt{3} & 0 \\ -1/2 & \sqrt{3}/2 & 1 \end{bmatrix}$
3º	$\begin{bmatrix} -1 & 0 & -1 \\ 3/2 & -\sqrt{3}/2 & 0 \\ 0 & \sqrt{3} & 0 \end{bmatrix}$	$\begin{bmatrix} 1 & 0 & 1 \\ 1/2 & -\sqrt{3}/2 & -1 \\ 0 & \sqrt{3} & 0 \end{bmatrix}$	$\begin{bmatrix} 3/2 & -\sqrt{3}/2 & 0 \\ -1/2 & \sqrt{3}/2 & 1 \\ 1/2 & \sqrt{3}/2 & -1 \end{bmatrix}$	$\begin{bmatrix} 3/2 & -\sqrt{3}/2 & 0 \\ 0 & \sqrt{3} & 0 \\ -1/2 & -\sqrt{3}/2 & 1 \end{bmatrix}$
4º	$\begin{bmatrix} 1/2 & \sqrt{3}/2 & -1 \\ 0 & -\sqrt{3} & 0 \\ -3/2 & \sqrt{3}/2 & 0 \end{bmatrix}$	$\begin{bmatrix} -1/2 & -\sqrt{3}/2 & 1 \\ 1/2 & -\sqrt{3}/2 & -1 \\ -3/2 & \sqrt{3}/2 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & -\sqrt{3} & 0 \\ -1/2 & \sqrt{3}/2 & 1 \\ -1 & 0 & -1 \end{bmatrix}$	$\begin{bmatrix} 0 & -\sqrt{3} & 0 \\ -3/2 & \sqrt{3}/2 & 0 \\ 1 & 0 & 1 \end{bmatrix}$
5º	$\begin{bmatrix} 1/2 & -\sqrt{3}/2 & -1 \\ 0 & \sqrt{3} & 0 \\ -3/2 & -\sqrt{3}/2 & 0 \end{bmatrix}$	$\begin{bmatrix} -1/2 & \sqrt{3}/2 & 1 \\ 1/2 & \sqrt{3}/2 & -1 \\ -3/2 & -\sqrt{3}/2 & 0 \end{bmatrix}$	$\begin{bmatrix} 0 & \sqrt{3} & 0 \\ -1/2 & -\sqrt{3}/2 & 1 \\ -1 & 0 & -1 \end{bmatrix}$	$\begin{bmatrix} 0 & \sqrt{3} & 0 \\ -3/2 & -\sqrt{3}/2 & 0 \\ 1 & 0 & 1 \end{bmatrix}$
6º	$\begin{bmatrix} 1/2 & \sqrt{3}/2 & -1 \\ -3/2 & -\sqrt{3}/2 & 0 \\ 3/2 & -\sqrt{3}/2 & 0 \end{bmatrix}$	$\begin{bmatrix} -1/2 & -\sqrt{3}/2 & 1 \\ -1 & 0 & -1 \\ 3/2 & -\sqrt{3}/2 & 0 \end{bmatrix}$	$\begin{bmatrix} -3/2 & -\sqrt{3}/2 & 0 \\ 1 & 0 & 1 \\ 1/2 & -\sqrt{3}/2 & -1 \end{bmatrix}$	$\begin{bmatrix} -3/2 & -\sqrt{3}/2 & 0 \\ 3/2 & -\sqrt{3}/2 & 0 \\ -1/2 & \sqrt{3}/2 & 1 \end{bmatrix}$

The step of sequencing the switching vectors is to determine the switching sequence of the selected switching vectors. In order to minimize the harmonic contents and the losses, the symmetrically aligned sequence scheme with two zero switching vectors as well as the selected non-zero switching vectors is adopted. It uses the zero switching vector "0000" to transfer the state from one switching period to another period, which may reduce the current ripple and harmonic components. The zero vector "1111" is applied to the middle of the switching period to reach the symmetrically alignment. Figure 6.6 shows an example of the switching during two switching periods.

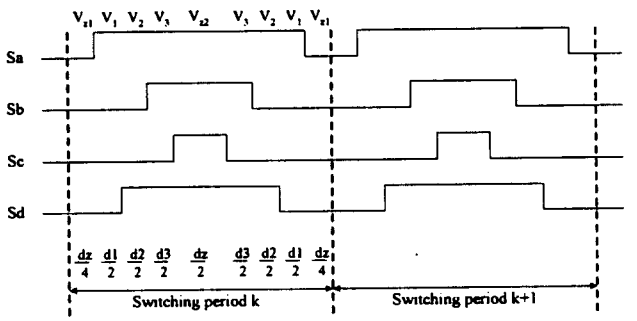

Figure 6.6 An example of the switching during two switching periods

6.3 Analytical Model of the Proposed SAPF

In this section analytical models for both the proposed SAPF and the distribution system are developed. These models are expressed in the s domain, and transfer functions for the SAPF and the whole system are derived. These transfer functions will be used to discuss characteristics as well as performance of the SAPF

6.3.1 The Building Distribution System

Figure 6.7 shows the equivalent model of a typical building distribution system. The distribution circuit is modeled as a π-type circuit with longitudinal impedance $Z_{2s} = R_2 + j2\pi fL_2$. The distributed capacitance of the circuit is neglected as this is an LV circuit. Capacitors C_1 and C_2, represents those for power factor correction. They may be connected to the circuit at its two ends if any.

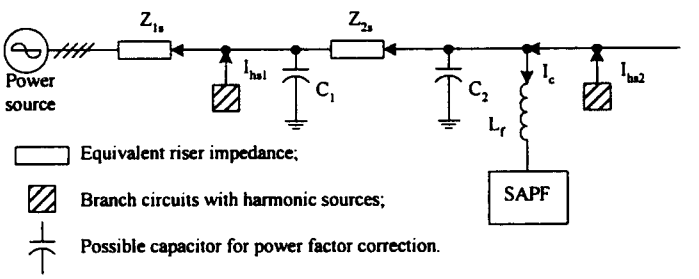

Figure 6.7 Circuit Model of the distribution system

The supply network includes both the distribution transformer and the high-voltage circuit, and is represented with an equivalent impedance $Z_{1s} = R_1 + j2\pi fL_1$. The high-voltage circuit is typically modeled as an equivalent impedance, which is determined by the fault level at 11kV ranging from 70MVA to 350MVA. Distribution transformers used in Hong Kong, are normally rated 500kVA, 1000kVA or 1500kVA with the short-circuit impedance of 4%-7%. The short-circuit impedance is frequent-dependant, but constant resistance and inductance are generally acceptable for harmonic study.

[Ting M.W. 1988] The harmonic currents arising from the magnetizing effect or saturation characteristic are not the primary harmonic currents, and are neglected in this study. Other factors such as the nonlinear resistance characteristics of the magnetizing branch and winding stray capacitance are also neglected. [Ting M.W. 1988] These distribution transformers are usually in delta-star connection to prevent zero sequence currents flowing into the utility system. In general, the supply network is represented with an equivalent impedance $Z_{1s} = R_1 + j2\pi fL_1$. It is determined by both the high-voltage circuit impedance and the transformer impedance, but the transformer impedance only under non-zero sequence conditions. For simplicity in discussion the supply circuit is assumed to be free of background harmonics.

Most of harmonic-producing loads in buildings may be categorized into current sources of harmonics and voltage sources of harmonics. Generally the current sources of harmonics are more dominant than the voltage sources of harmonics. The typical voltage source of harmonics, for an example, is the rectifier circuit with a capacitor at the DC side. In practice, there is normally an equivalent inductance in series with the output circuit of this type of loads to smooth the harmonic distortion. This measure may turn the loads (with output inductance) to be a harmonic current source. Consequently, these loads are modeled as harmonic current sources in this section. As the harmonic currents from these loads flow through the distribution circuit, these loads are grouped together, and

are connected to the distribution circuit at certain locations, as illustrated in Figure 6.7.

The phase angle of the harmonic current from a load is a key factor in modeling distributed harmonics-generating loads and assessing the harmonic current the distribution circuit. This is because harmonics currents from different loads can be greatly cancelled if the phase angles vary significantly. Assuming all harmonic current sources with the same phase angle is one of the methods to address the phase angle problem. This approach may result in conservative estimation of harmonic distortion in the system. In this thesis, the harmonic current sources at different floors are set with the same phase angle.

6.3.2 Analytical Models of the Multi-channel Complex Gain Controller

As seen in the previous section, the control strategy of the multi-channel complex gain controller is realized in both the stationary reference frame and the synchronous reference frame. It is necessary to express the outputs of the controller in a function of time, and to derive the s-domain transfer function in the stationary frame using the properties of Laplace Transformation.

The reference signals are obtained by summing the outputs from all the channels. To derive the s-domain model for the controller, the signals in a single

channel at order h is analyzed. In this case both the positive and negative sequence voltages at order h in the d-q coordinate system are derived by the Park transformation, and expressed by

$$\begin{bmatrix} V_d^+ \\ V_q^+ \end{bmatrix} = \begin{bmatrix} \sin(h\omega t) & -\cos(h\omega t) \\ \cos(h\omega t) & \sin(h\omega t) \end{bmatrix} \cdot \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{6.21}$$

$$\begin{bmatrix} V_d^- \\ V_q^- \end{bmatrix} = \begin{bmatrix} \sin(-h\omega t) & -\cos(-h\omega t) \\ \cos(-h\omega t) & \sin(-h\omega t) \end{bmatrix} \cdot \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{6.22}$$

In the time-domain, the control process in the d-q reference frame is denoted $H_{dq}(t)$. Then the reference currents in the d-q coordinate system are obtained, as follows:

$$\begin{bmatrix} i_d^+ \\ i_q^+ \end{bmatrix} = H_{dq}(t) * \begin{bmatrix} V_d^+ \\ V_q^+ \end{bmatrix} \tag{6.23}$$

$$\begin{bmatrix} i_d^- \\ i_q^- \end{bmatrix} = H_{dq}(t) * \begin{bmatrix} V_d^- \\ V_q^- \end{bmatrix} \tag{6.24}$$

where the symbol of $*$ denotes a convolution product. By applying the inverse Park transformation to the reference currents, the reference currents of both the positive and negative sequence in the α-β coordinate are obtained,

$$\begin{bmatrix} i_\alpha^+ \\ i_\beta^+ \end{bmatrix} = \begin{bmatrix} \sin(h\omega t + \alpha_h) & \cos(h\omega t + \alpha_h) \\ -\cos(h\omega t + \alpha_h) & \sin(h\omega t + \alpha_h) \end{bmatrix} \cdot \begin{bmatrix} i_d^+ \\ i_q^+ \end{bmatrix} \tag{6.25}$$

$$\begin{bmatrix} i_\alpha^- \\ i_\beta^- \end{bmatrix} = \begin{bmatrix} \sin(-h\omega t - \alpha_h) & \cos(-h\omega t - \alpha_h) \\ -\cos(-h\omega t - \alpha_h) & \sin(-h\omega t - \alpha_h) \end{bmatrix} \cdot \begin{bmatrix} i_d^- \\ i_q^- \end{bmatrix} \tag{6.26}$$

The reference currents of the channel in the static frame are expressed by the sum of both the positive and negative sequence quantities, namely,

$$\begin{aligned} i_\alpha &= i_\alpha^+ + i_\alpha^- \\ i_\beta &= i_\beta^+ + i_\beta^- \end{aligned} \tag{6.27}$$

Substituting Equations (6.21-6.26) into Equation (6.27) yields the reference

currents in terms of the controller inputs, that is, the measured system voltages.

$$\begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = \begin{bmatrix} 2\cdot\left\{\sin(h\omega t+\alpha_h)\cdot\left[H_{dq}(t)*\left(\sin(h\omega t)\cdot V_\alpha(t)\right)\right]+\cos(h\omega t+\alpha_h)\cdot\left[H_{dq}(t)*\left(\cos(h\omega t)\cdot V_\alpha(t)\right)\right]\right\} \\ 2\cdot\left\{\sin(h\omega t+\alpha_h)\cdot\left[H_{dq}(t)*\left(\sin(h\omega t)\cdot V_\alpha(t)\right)\right]+\cos(h\omega t+\alpha_h)\cdot\left[H_{dq}(t)*\left(\cos(h\omega t)\cdot V_\beta(t)\right)\right]\right\} \end{bmatrix} \tag{6.28}$$

It can be drawn from Equation (6.28) that the quantities in α-axis and β-axis are demodulated in a single-order channel, as shown in Figure 6.8 (a) and (b). It is noted that the control process denoted by $H_{dq}(t)$ are the same in both d- and q-axis The function of $H_{dq}(t)$ are determined by the low pass filter as well as the control gain k_{vh}.

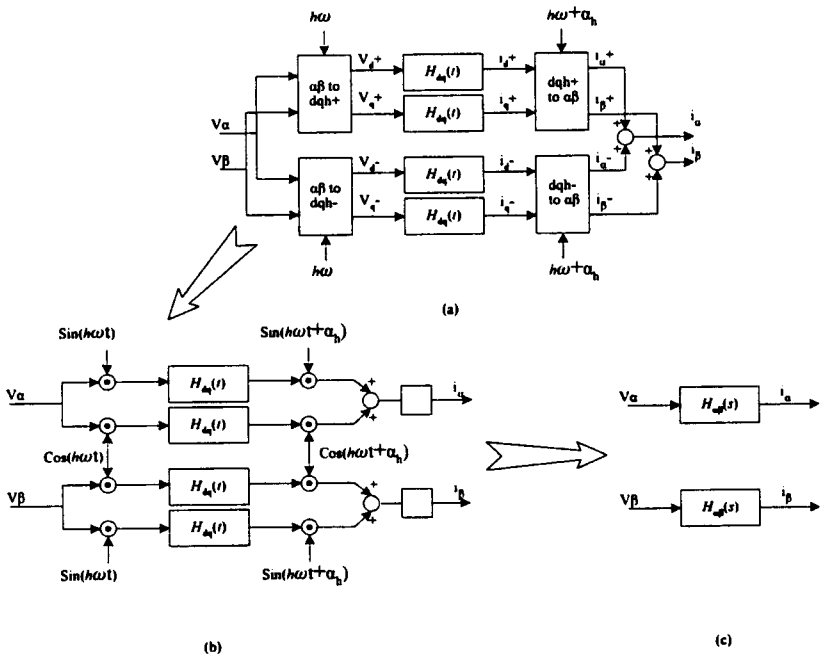

Figure 6.8 Derivation of the reference currents

Equation (6.28) can be rewritten as,

$$i_{\alpha\beta}(t)=2\cdot\left\{\left[V_{\alpha\beta}(t)\cdot\sin(h\omega t)\right]*H_{dq}(t)\right\}\cdot\sin(h\omega t+\alpha_h)+\left\{\left[V_{\alpha\beta}(t)\cdot\cos(h\omega t)\right]*H_{dq}(t)\right\}\cdot\cos(h\omega t+\alpha_h) \tag{6.29}$$

where $V_{\alpha\beta}$ and $i_{\alpha\beta}$ represent the voltage and current in either the α-axis or the β-axis. To simplify the following derivation, two intermediate functions are introduced, which are defined by

$$a_1(t) = \left[V_{\alpha\beta}(t) \cdot \cos(h\omega t)\right] * H_{dq}(t) \tag{6.30}$$

$$a_2(t) = \left[V_{\alpha\beta}(t) \cdot \sin(h\omega t)\right] * H_{dq}(t) \tag{6.31}$$

Applying the Laplace transformation to Equations (6.30-6.31) yields

$$\begin{aligned} A_1(s) &= L\left\{\left[V_{\alpha\beta}(t) \cdot \cos(h\omega t)\right] * H_{dq}(t)\right\} \\ &= H_{dq}(s) \cdot L\left\{V_{\alpha\beta}(t) \cdot \cos(h\omega t)\right\} \\ &= \tfrac{1}{2} \cdot H_{dq}(s) \cdot \left\{V_{\alpha\beta}(s + jh\omega) + V_{\alpha\beta}(s - jh\omega)\right\} \end{aligned} \tag{6.32}$$

$$\begin{aligned} A_2(s) &= L\left\{\left[V_{\alpha\beta}(t) \cdot \sin(h\omega t)\right] * H_{dq}(t)\right\} \\ &= H_{dq}(s) \cdot L\left\{V_{\alpha\beta}(t) \cdot \sin(h\omega t)\right\} \\ &= \tfrac{j}{2} \cdot H_{dq}(s) \cdot \left\{V_{\alpha\beta}(s + jh\omega) - V_{\alpha\beta}(s - jh\omega)\right\} \end{aligned} \tag{6.33}$$

By applying Laplace transformation again to Equation (6.29), the transfer function of the single channel, as shown in Figure 6.8 (c), is obtained

$$H_{\alpha\beta h}(s) = \frac{i_{\alpha\beta}(s)}{V_{\alpha\beta}(s)} = \cos(\alpha_h) \cdot \left[H_{dq}(s - jh\omega) + H_{dq}(s + jh\omega)\right] - j \cdot \sin(\alpha_h) \cdot \left[H_{dq}(s + jh\omega) - H_{dq}(s - jh\omega)\right] \tag{6.34}$$

where $H_{dq}(s)$ is the expression of $H_{dq}(t)$ in the s-domain. By using the first order Butterworth LPF the transfer function of the single channel in the d-q frame is expressed by

$$H_{dq}(s) = \frac{|k_{vh}| \cdot A_0}{1 + s \cdot T_c} \tag{6.35}$$

where T_c and A_0 are the time constant and the gain of the LPF, respectively. Consequently, the transfer function of a single channel, for generating the reference current signals in the α-β frame is derived as

$$H_{\alpha\beta h}(s) = 2 \cdot |k_{vh}| \cdot A_0 \frac{\cos(\alpha_h) \cdot (1 + s \cdot T_c) - \sin(\alpha_h) \cdot h\omega \cdot T_c}{(1 + s \cdot T_c)^2 + (h\omega \cdot T_c)^2} \tag{6.36}$$

By summing all the selected channels, the total transfer function of the multi-channel complex-gain controller is obtained, that is,

$$H_{\alpha\beta}(s) = \sum_h H_{\alpha\beta h}(s) \tag{6.37}$$

6.3.3 Analytical Model of the Current Regulator

The analytical model of the current regulator can be derived according to the discussion in the previous section. Figure 6.9 presents the current control loop used in the proposed SAPF system. The error between the reference current and the detected compensating current in the α-β-γ reference frame is controlled by the proportional function $G_c(s)$, which results in the commanding voltage v_o^*. Therefore, $G_c(s)$ in Figure 6.9 is expressed as the proportional gain K_c. The function $G_{vo}(s)$ represents the unit time delay of the space vector PWM. In the s-domain, the effect of the time delay T can be approximated by a first order lag system if the frequencies of interest are small in comparison with 1/T as given by

$$G_{vo}(s) = \frac{1}{1 + s \cdot T_{vo}} \tag{6.38}$$

where T_{vo} is the delay time. $G_{Lf}(s)$ is the transfer function of the output plant of the proposed SAPF, and is given by

$$G_{Lf}(s) = \frac{1}{s \cdot L_f + R_f} \tag{6.39}$$

Where both R_f and L_f are the resistance and inductance of the plant. The resistance can be negligible in an actual system. Hence, the closed loop transfer function of the current controller is given by

$$G_{ci}(s) = \frac{i_c(s)}{i_{\alpha\beta ref}(s)} = \frac{G_c(s)G_{vo}(s)G_{Lf}(s)}{1 + G_c(s)G_{vo}(s)G_{Lf}(s)} \tag{6.40}$$

where $i_c(s)$ is the compensating current. Substituting Equations (6.38-6.39) into Equation (6.40) yields

$$G_{ci}(s) = \frac{K_c}{T_{vo} \cdot L_f \cdot s^2 + L_f \cdot s + K_c} \tag{6.41}$$

The critically damping system should be selected in order to achieve the performance of the current controller without overshoot or oscillation in the time domain. As a result, the same characteristic roots should be selected, that is, K_c should be selected to be

$$K_c = \frac{L_f}{4 \cdot T_{vo}} \tag{6.42}$$

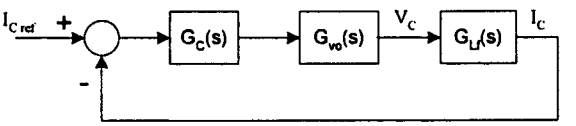

Figure 6.9 Block diagram of a current regulator

6.3.4 Transfer Function of the Proposed SAPF

By ignoring any distortion in the signal conditioning circuits, the transfer function of the proposed SAPF is expressed by both transfer functions of the proposed controller and the current regulator. Using the functions given in (6.30-6.41), the filter transfer function is expressed by

$$\frac{i_c(s)}{V_s(s)} = H_{\alpha\beta}(s) \cdot G_{ci}(s) = \sum_h H_{\alpha\beta h}(s) \cdot \frac{K_c}{T_{vo} \cdot L_f \cdot s^2 + L_f \cdot s + K_c} \tag{6.43}$$

where $V_s(s)$ is the phase voltages at the point of connection.

6.4 Traditional SAPF Based on Voltage Detection

The SAPF based on voltage detection is not extensively studied compared with the current-detection SAPF. The SAPF based on voltage detection in [Hirofumi Akagi etc. 1999, Keiji Wada etc. 2002] is selected as the traditional one for

comparison. The control strategy of the traditional voltage-detection SAPF is implemented in the synchronous rotating reference frame. Similar to the proposed SAPF, the frame transformation is unavoidable. The fundamental synchronous reference frame, however, is used only in the traditional SAPF. In the fundamental synchronous reference frame, the harmonic components are extracted from the detected voltage by a high pass filter in both axes. As a result, the fundamental component of the detected voltage is filtered out in the fundamental synchronous reference frame. The extracted harmonic components are multiplied by a real-value control gain. The reference currents are obtained accordingly. In order to make a comparison with the proposed SAPF, the same current regulator is adopted in both SAPFs.

The analytical model of the traditional SAPF is not difficult to obtain. A first order high pass filter is used again in the controller. Hence the transfer function in the fundamental synchronous reference frame is expressed by

$$H_{dqtrad}(s) = \frac{k_v \cdot A_1 \cdot T_{hpf} \cdot s}{1 + T_{hpf} \cdot s} \tag{6.44}$$

where k_v is the control gain, T_{hpf} and A_1 are the time constant and the compensating gain of the high pass filter, respectively. Similarly, the equivalent expression in the stationary reference frame is derived as

$$H_{\alpha\beta}(s) = k_v \cdot T_{hpf} \cdot A_1 \cdot \frac{T_{hpf} \cdot s^2 + s + T_{hpf} \cdot \omega^2}{T_{hpf}^2 \cdot s^2 + 2T_{hpf} \cdot s + T_{hpf}^2 \omega^2 + 1} \tag{6.45}$$

With the consideration of the current regulator, the transfer function of the traditional SAPF is obtained as

$$\frac{i_{ctrad}(s)}{V_s(s)} = H_{\alpha\beta}(s) \cdot G_{ci}(s) = k_v \cdot T_{hpf} \cdot A_1 \cdot \frac{T_{hpf} \cdot s^2 + s + T_{hpf} \cdot \omega^2}{T_{hpf}^2 \cdot s^2 + 2T_{hpf} \cdot s + T_{hpf}^2 \omega^2 + 1} \cdot \frac{K_c}{T_{vo} \cdot L_f \cdot s^2 + L_f \cdot s + K_c} \quad (6.46)$$

6.5 Characteristics of the Proposed SAPF

In this section characteristics of the proposed SAPF are investigated. Table 6.5 shows the filter parameters adopted for analysis. The output series inductance generally ranges from hundreds of μH to several mH. It is set to be 1 mH in the analysis. The switching frequency of IBGT modules is set to be 10 kHz, which is considered high enough harmonic orders below 20. Accordingly, the corresponding unit time delay arising in SVPWM is equal to 100 μs. In the controller, the cutoff frequency of the low pass filter is set at 10 Hz. The detailed discussion of the low pass filter will be presented in the later chapters. The corresponding time constant of the low pass filter is 15.9 ms. The proportional control gain in the current regulator is set at 2.5 according to the Equation (6.42).

Table 6.6 shows the parameters of a typical building LV distribution system. It is assumed that the distributed capacitance of the circuit is neglected, and the capacitor bank for power factor correction is installed at either one of two circuit ends. Both L_1 and R_1 are the equivalent inductance and the resistance of the supply network. Both L_2 and R_2 are the line inductance and line resistance of the distribution circuit.

Table 6.5 Key parameters of the SAPF

Smoothing series inductance	L_f	1 mH
Switch frequency	Fs	10 kHz
Low pass filter time constant	Tc	15.9 ms
Unit time delay	T_{vo}	100 μs
Proportional control gain	K_C	2.5

Table 6.6 Parameters of the distribution system in Figure 6.7

Equivalent inductance	L_1	20.4 μH
Equivalent resistor	R_1	0.8 mohm
Line inductance	L_2	0.08 mH
Line resistor	R_2	0.044 ohm
Equivalent capacitor	C_1	250 μF
Equivalent capacitor	C_2	250 μF

6.5.1 Frequency Response of the SAPF

I. Generation of the reference currents

By recalling Equations (6.36-6.37) and substituting the values given in Table 6.5, the transfer function of the controller, a ratio of the generation reference currents i_{cref} to the detected terminal voltage, can be rewritten as

$$\begin{aligned}\frac{i_{cref}(s)}{V_s(s)} &= \sum_h 2\cdot|k_{vh}|\cdot A_0 \frac{\cos(\alpha_h)\cdot(1+s\cdot T_c)-\sin(\alpha_h)\cdot h\omega\cdot T_c}{(1+s\cdot T_c)^2+(h\omega\cdot T_c)^2} \\ &= \sum_h 2\cdot|k_{vh}|\cdot \frac{1+s\cdot 0.0159}{(1+s\cdot 0.0159)^2+(4.9926\cdot h)^2}\end{aligned} \tag{6.47}$$

where h and k_{vh} are the harmonic order and the control gain of the corresponding order, respectively. Generally, in the building distribution system, the 3rd, 5th and 7th harmonics are the dominant components, and the 11th, 13th, 17th and 19th harmonics may present in the system with moderate values. These harmonics are selected for the analysis of frequency response of the SAPF. The control gain at these orders is set as 1.

Figure 6.10 shows the bode diagram of Equation (6.47), which illustrates the frequency response of the controller. It is seen that the harmonics of concern are extracted from the detected voltages with no distortion. At these harmonic orders, the corresponding phase angles are close to zero, which indicates that there is no phase shift in each channel. The attenuation of other harmonics is well achieved by these channels. The fundamental component of the voltages is attenuated by more than 20 dB.

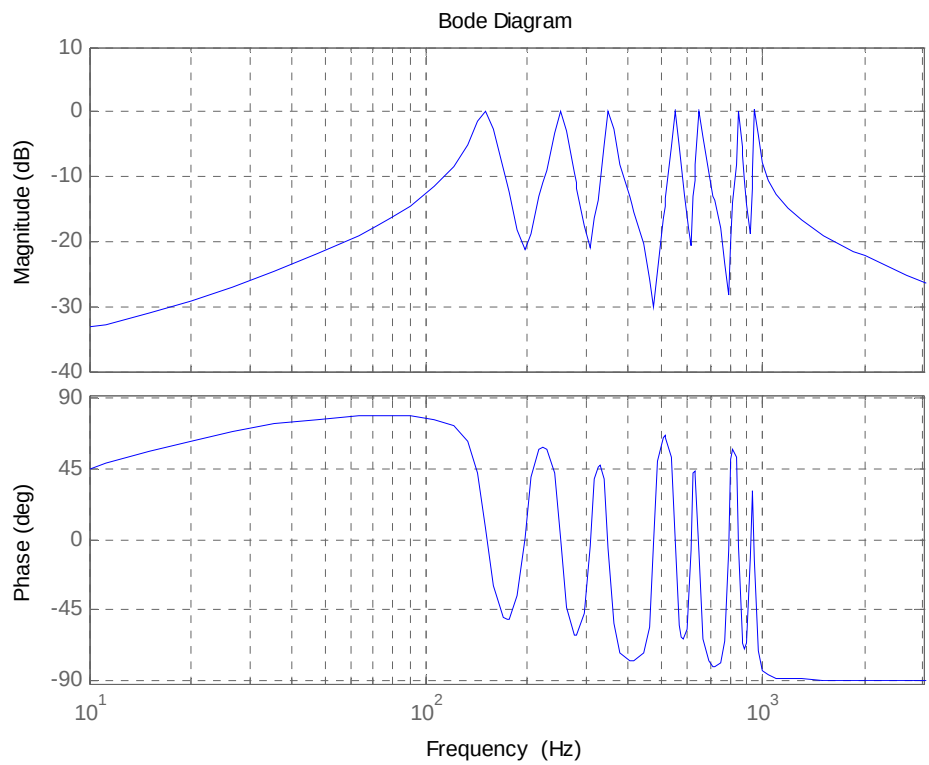

Figure 6.10 Performance of reference currents generation with k_{vh}=1 and T_c=0.0159

If the current regulator is ideal, that is, the compensating currents of the SAPF are same as the reference currents, the controller determines the performance of the SAPF. Control gain k_{vh} has a significant impact on the system performance.

Figure 6.11 shows the frequency response of the channels in the controller when k_{vh} are all set at 2. As indicated in Equation (6.44), the phase response is not affected by k_{vh} while the magnitude response is proportional to the control gain k_{vh}. However, the other components at non-interested orders may be attenuated. It may be necessary to increase the values of the control gain k_{vh} for achieving satisfactory performance. In order to improve the selectivity of the channels, the cutoff frequency should be decreased. The cutoff frequency is set at 5 Hz with the time constant τ_c at 0.03185. It can be seen in Figure 6.12. that the attenuation is increased and the magnitudes of harmonic components in these orders are similar to those in Figure 6.11.

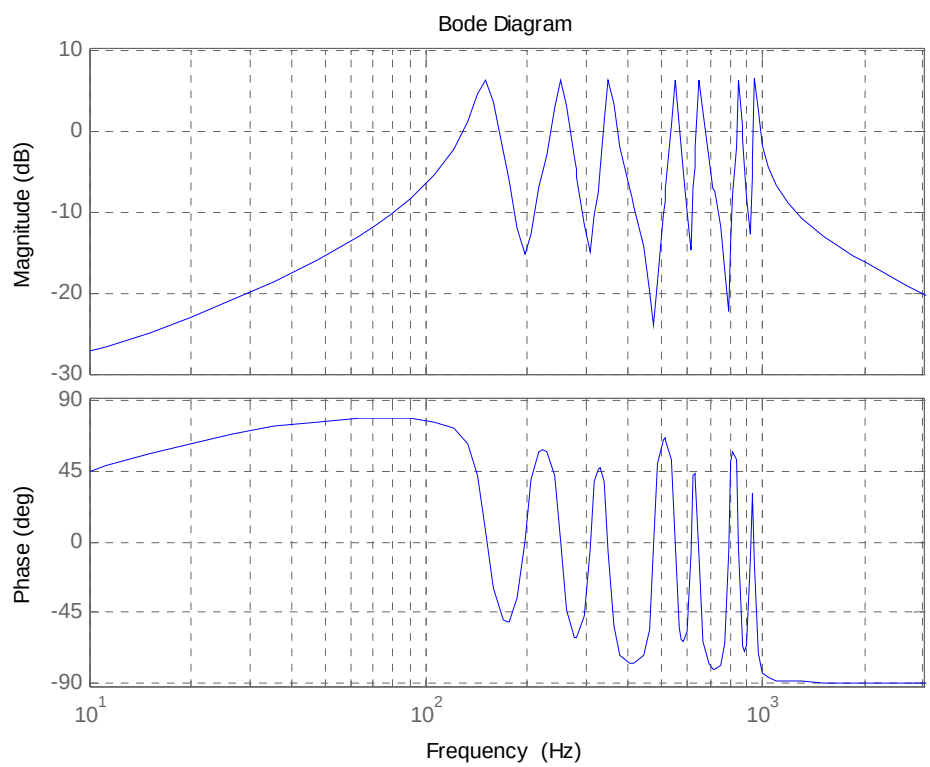

Figure 6.11 Frequency response of the generation of the reference currents with k_{vh}=2 and τ_c=0.0159

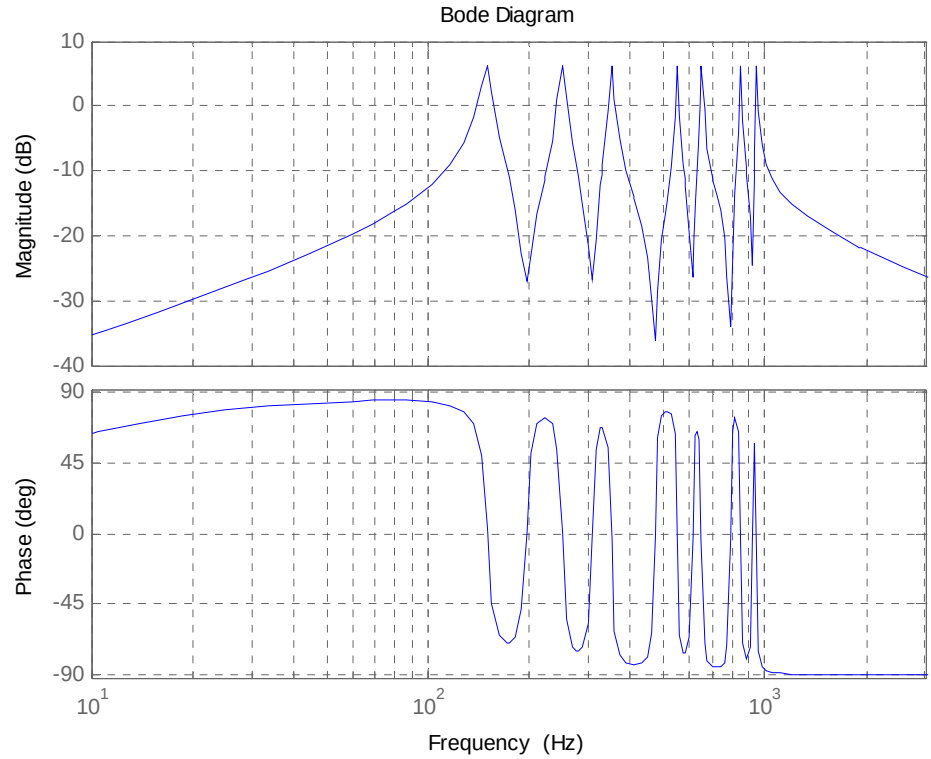

Figure 6.12 Frequency response of the generation of the reference currents with k_{vh}=2 and T_c=0.03185

II. Whole proposed SAPF

In this thesis, a proportional control is used in the current regulator. The parameters of the current regulator are listed in Table 6.5. The transfer function (6.41) is then expressed by

$$\frac{i_c}{i_{cref}} = \frac{K_c}{T_{vo} \cdot L_f \cdot s^2 + L_f \cdot s + K_c} = \frac{2.5}{10^{-7} \cdot s^2 + 10^{-3} \cdot s + 2.5} \tag{6.48}$$

The corresponding bode diagram is presented in Figure 6.13. It is noted that the magnitude of the current regulator does not always keep unitary. The attenuation reaches 0.7 at 517 Hz and it reaches 0.39 at 1 kHz. Additionally, the minus phase angle that is closer to -180º reduces the margin of system stability.

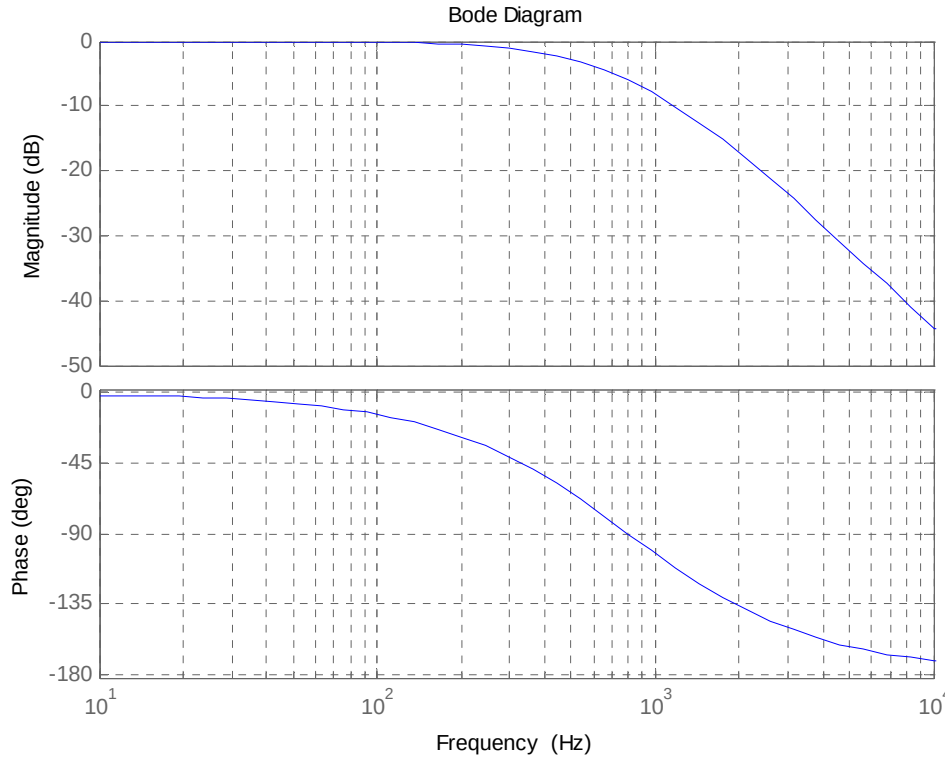

Figure 6.13 Frequency response of the current regulator

With the consideration of the current regulator, the compensating currents are the output while the detected voltages are the input of the proposed SAPF system. The proposed SAPF based on voltage detection can be considered as the admittance connected to a building LV distribution system. Its value can be evaluated by using Equation (6.43). With the filter parameters given in Table 6.5, the equivalent admittance is

$$Y=\frac{i_c(s)}{V_s(s)}=\sum_h\left(2\cdot|k_{vh}|\cdot A_0\frac{\cos(\alpha_h)\cdot(1+s\cdot T_c)-\sin(\alpha_h)\cdot h\omega\cdot T_c}{(1+s\cdot T_c)^2+(h\omega\cdot T_c)^2}\right)\cdot\frac{K_c}{T_{vo}\cdot L_f\cdot s^2+L_f\cdot s+K_c}$$
$$=\sum_h\left(2\cdot|k_{vh}|\cdot\frac{1+s\cdot 0.0159}{(1+s\cdot 0.0159)^2+(4.9926\cdot h)^2}\right)\cdot\frac{2.5}{10^{-7}\cdot s^2+10^{-3}\cdot s+2.5} \quad (6.49)$$

The bode diagram of the equivalent admittance with all control gain set at 1 and the cutoff frequency set at 10 Hz for all orders is shown in Figure 6.14. Under

this condition, the SAPF is definitely stable because all the magnitudes are below 0 dB. It is also indicated that the equivalent admittance can be adjusted by the control gain at different orders. The larger control gain at order h results in the smaller equivalent impedance. With the proper value of the cutoff frequency, the characteristic of sharp selection may be obtained, which can attenuate unwanted components as well as adopt a high value of the control gains. It can also be drawn that the equivalent impedance (admittance) at the concerned frequencies is not always resistive but inductive in most orders.

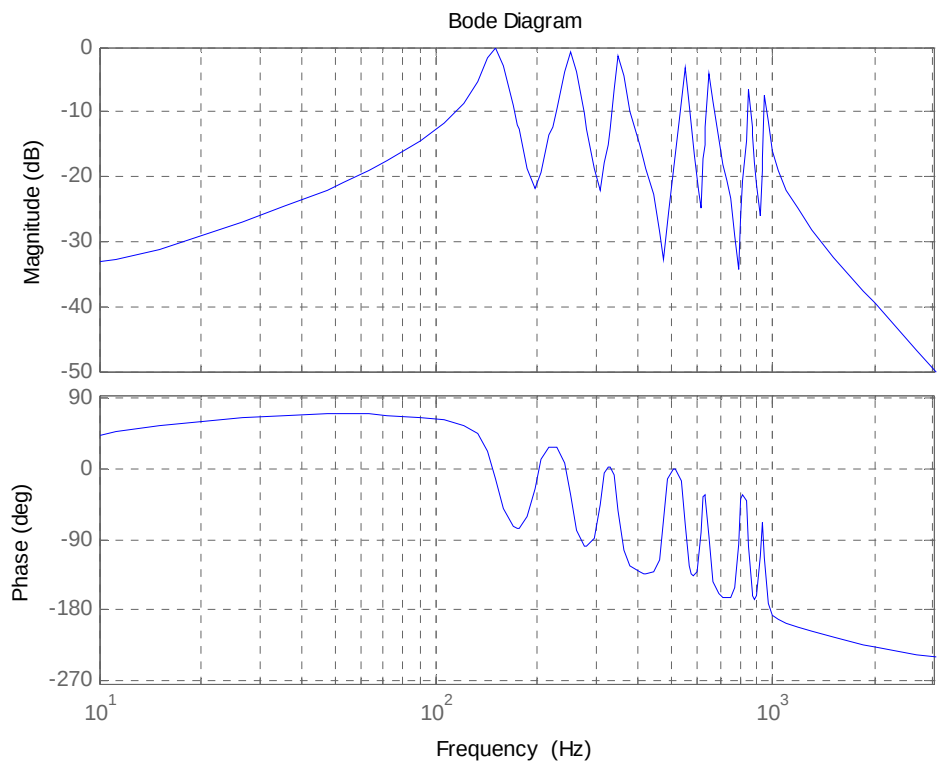

Figure 6.14 Frequency response of the equivalent admittance of the proposed SAPF with k_{vh}=1 and T_c=0.0159

In order to compare the performance with the traditional voltage-detection SAPF, the frequency response of the traditional voltage-detection SAPF is

drawn in Figure 6.15 according to Equation (6.45). The parameter is same as the case in Equation (6.46) as shown in Equation (6.50).

$$\frac{i_{ctrad}(s)}{V_s(s)} = k_v \cdot 0.0159 \cdot \frac{0.0159 \cdot s^2 + s + 1569.175}{0.0002528 \cdot s^2 + 0.0318 \cdot s + 25.9499} \cdot \frac{2.5}{10^{-7} \cdot s^2 + 10^{-3} \cdot s + 2.5} \tag{6.50}$$

From Figure (6.14-6.15), it can be seen that there is some attenuation in the magnitude and phase delay in the phase response for all typical harmonic orders due to the existence of the current regulator. As a result, the connected SAPF would not be always considered as the resistive impedance. In some cases such as the damping of harmonic resonance in the system, resistive impedance may have better performance. It would be difficult for the traditional voltage-detection SAPF to tune as the possible requirement based on existing control strategy. The change of the current regulator may improve the output performance of the SAPF.

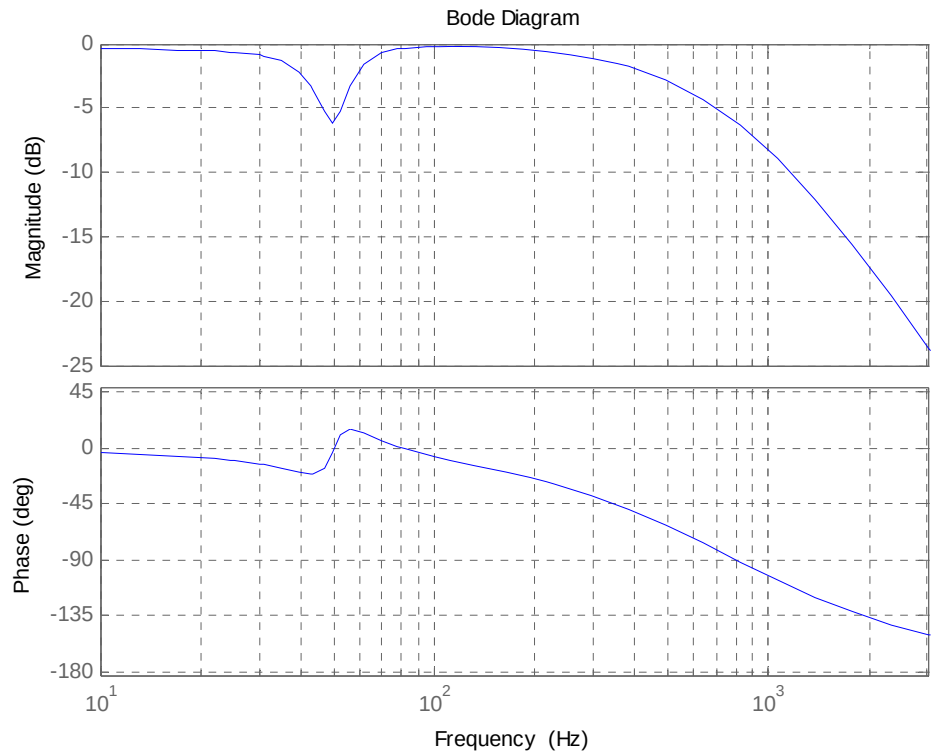

Figure 6.15 The frequency response of the equivalent admittance of the traditional voltage-detection SAPF with k_{vh}=1 and T_c=0.0159

In the proposed SAPF, the complex control gain makes it possible to tune the output of the SAPF by adjusting the angle of the control gain. Considering the case with the control gain set at 2 and the cutoff frequency set at 10 for all orders Hz, the impact of α_h on the system is investigated. Equation (6.49) is rewritten as

$$\begin{aligned} Y = \frac{i_c(s)}{V_s(s)} &= \sum_h \left(2 \cdot |k_{vh}| \cdot A_0 \frac{\cos(\alpha_h) \cdot (1 + s \cdot T_c) - \sin(\alpha_h) \cdot h\omega \cdot T_c}{(1 + s \cdot T_c)^2 + (h\omega \cdot T_c)^2} \right) \cdot \frac{K_c}{T_{vo} \cdot L_f \cdot s^2 + L_f \cdot s + K_c} \\ &= \sum_h \left(2 \cdot |k_{vh}| \cdot \frac{\cos(\alpha_h) - \sin(\alpha_h) \cdot 4.9926 \cdot h + s \cdot \cos(\alpha_h) \cdot 0.0159}{(1 + s \cdot 0.0159)^2 + (4.9926 \cdot h)^2} \right) \cdot \frac{2.5}{10^{-7} \cdot s^2 + 10^{-3} \cdot s + 2.5} \end{aligned} \quad (6.51)$$

From the phase response in Figure 6.11, the phase delay at the harmonic orders of concern can be read, as shown in Table 6.7. With the compensating phase

angles in Table 6.7 at frequencies of concern the frequency response of the proposed SAPF is shown in Figure 6.16. The results show that the remaining phase is close to zero, which means the proposed SAPF presents an equivalent resistive impedance at the concerned frequencies.

Table 6.7 The impact of α_h on the system

Order h	3	5	7	11	13	17	19
Phase delay	-18	-36	-53	-71	-89	-99	-114
Compensating phase α_h	13	33	51	62	83	94	111
Remaining phase	-1.75	-1.33	-1.34	-1.27	-1.34	-1.35	1.19

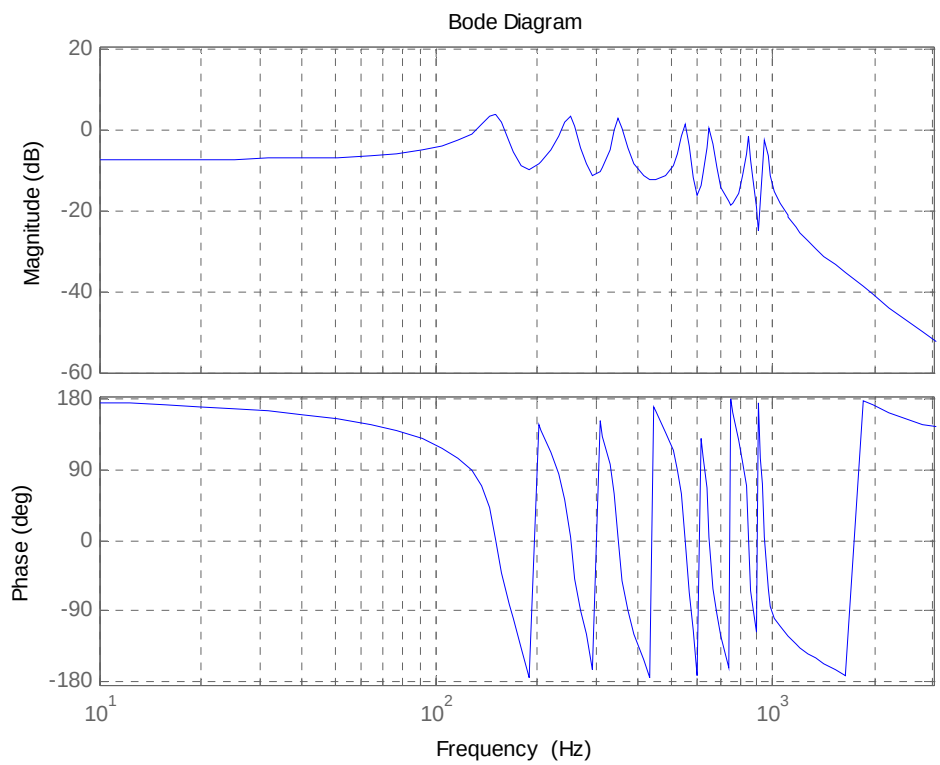

Figure 6.16 The frequency response of the proposed SAPF with k_{vh}=2, T_c=0.0159 and α_h adjusted

6.5.2 Stability of the Proposed SAPF System

Stability of the proposed SAPF system connected to a distribution system is discussed in this section. The stability of a close loop system can be judged from bode diagrams. In the bode diagrams. the difference of zero dB to the magnitude with -180º phase angle represents the gain margin. The difference of the phase angle with zero dB magnitude to -180º represents the phase margin. Only if both the gain margins and the phase margin are large than zero, the system is stable.

It is noted in Figure 6.7 that both the SAPF based on voltage detection and the distribution system forms a closed-loop system. The block diagram of this combined electrical system is shown in Figure 6.17. The SAPF outputs the compensating currents to the distribution system at the point of connection. These currents together with the harmonic source currents flow through the upstream circuits, and generate harmonic voltage in the distribution system, as well as at the point of connection. As indicated in Figure 6.17, the harmonic source currents serve as the input of the closed-loop system while the output of the SAPF is the output of the closed-loop system. Hence, the stability analysis is conducted in the electrical system containing both the SAPF based on voltage detection and the distribution system.

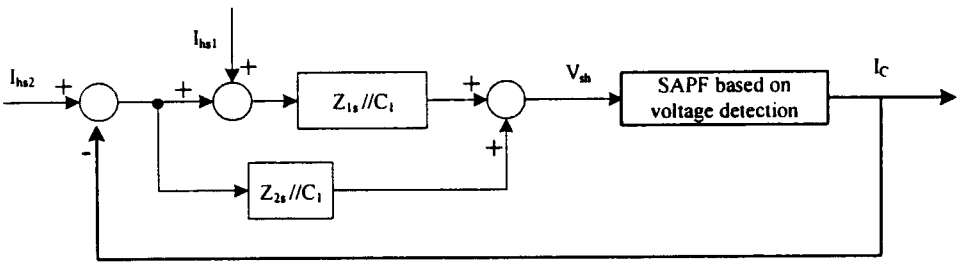

Figure 6.17 Equivalent closed-loop control

In this section, the role of the proposed multi-channel complex-gain controller in improving the stability margin of the system is illustrated. It also improves the maximum value of the control gain. The feature of multiple channels in the controller makes the proposed SAPF set different control gain values at different orders. This allows users to focus on individual dominant harmonics and to actually improve the utilization of the SAPF. The feature of complex gain in the controller makes the SAPF adjustable in both magnitude and phase angle.

To demonstrate these features of the proposed SAPF, the distribution system shown in Figure 6.7 is simplified, as seen in Figure 6.18. The parameters of the distribution system are listed in Table 6.8. The settings of the proposed SAPF are the same as those in Table 6.5

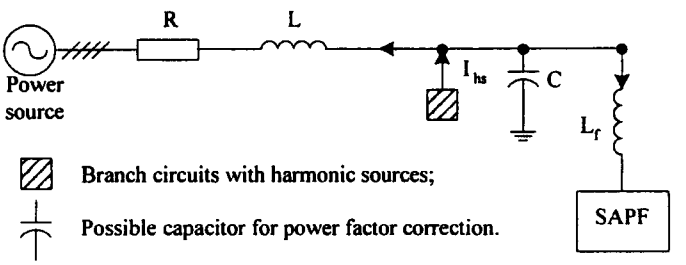

Figure 6.18 Simple configuration of the system for stability analysis

Table 6.8 Parameters of the distribution system in Figure 6.18

Equivalent inductance	L	0.08 mH
Equivalent resistor	R	0.2 ohm
Equivalent capacitor	C	250 μF

According to Figure 6.17 and 6.18, the transfer function of the closed-loop system is expressed as,

$$\frac{I_c}{I_{hs}} = \frac{Y_{sys}}{Y_{sapf} + Y_{sys}} \tag{6.52}$$

where I_c and I_{hs} are the output of the SAPF and harmonic source, respectively. Y_{sys} and Y_{sapf} are the equivalent admittance of the distribution system in Figure 6.18 and the connected SAPF. The traditional one and the proposed one are presented as Equation (6.46) and (6.43), respectively.

I. The critical stability condition for the traditional voltage-detection SAPF and the proposed SAPF

The critical stability condition limits the possible maximum values of the control gains. With the increase of the control gain, the closed-loop system is close to the critical stability condition, and even becomes instable due to too large control gains. By using the bode diagrams, the critical conditions of the traditional SAPF connected and the proposed SAPF connected are found. And the maximum control gains are obtained. In order to compare with each other, the control gain in different channels of the proposed controller is set with the same magnitude.

Figure 6.19 shows the critical stability system with the traditional SAPF connected. The value of corresponding maximum control gain k_v is equal to 1.63. The critical stability system with the proposed SAPF connected is shown in Figure 6.20. It is found that the value of maximum control gain k_{vh} is equal to 2.11. It can be seen in Figure 6.20 that with the maximum control gain the closed-loop system is under critical stable condition. Although the maximum value of the proposed SAPF is larger than that of the traditional one, both values are not large enough to fulfill the requirement in application of the SAPF. Additionally, the stability margins should be improved to guarantee the system stable. Therefore, adjustments should be made. For the traditional SAPF, it is difficult to adjust the parameters to improve the stability margins. In the following parts, the role of the multi-channel complex-gain controller is discussed.

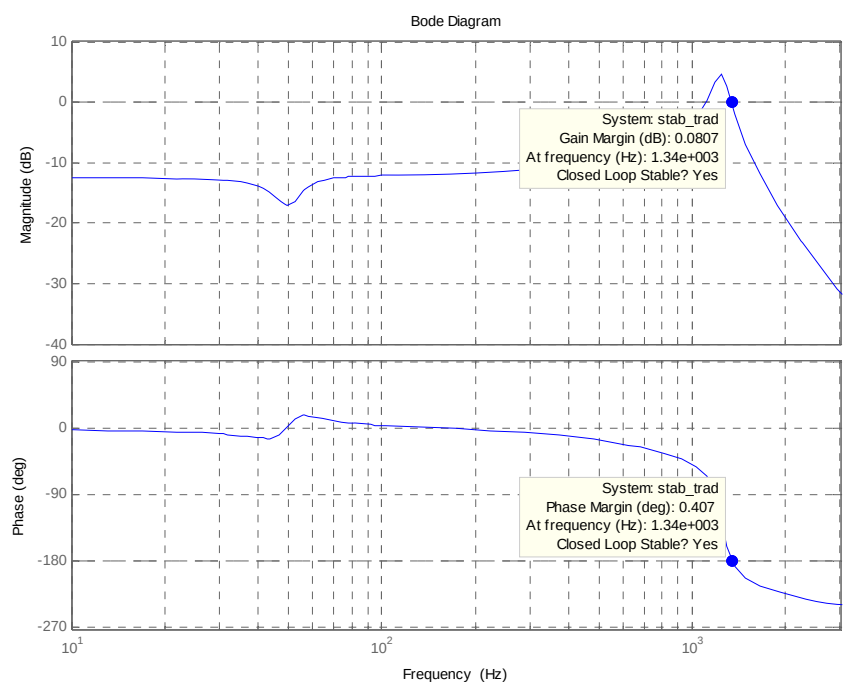

Figure 6.19 Critical stability system with the traditional SAPF connected

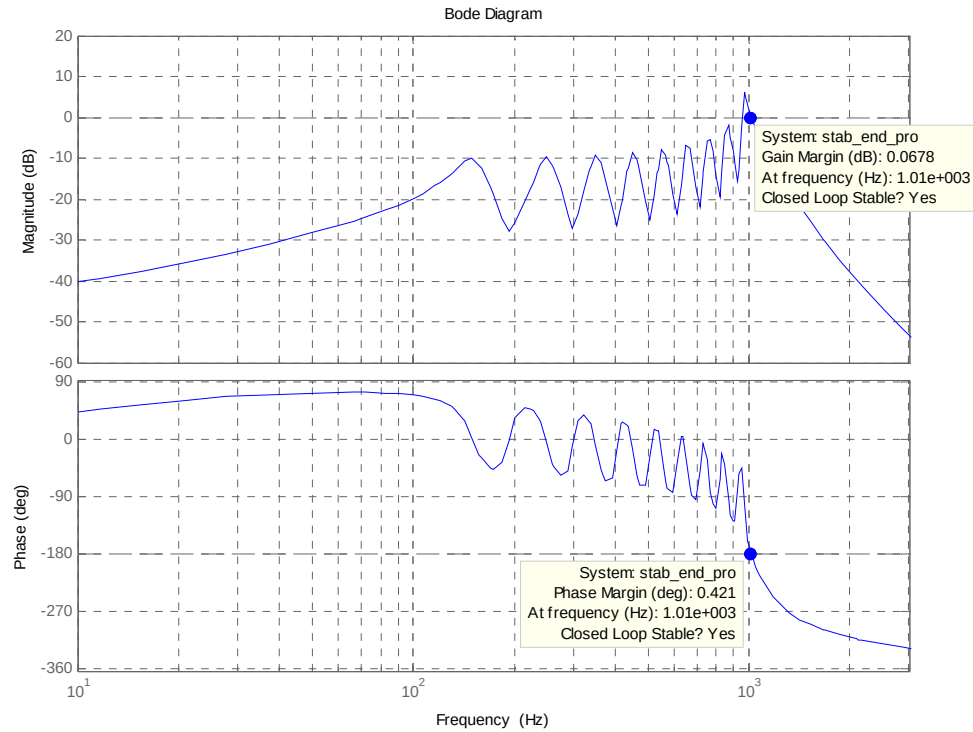

Figure 6.20 Critical stability system with the proposed SAPF connected

II. The role of the magnitude of the control gain

With other parameters of the proposed SAPF remaining unchanged, the system turns unstable when the control gain is increased, as shown in Figure 6.21 (the control gain set at 3). In the proposed controller, the control gain can be set to be different values in different channels. In this case, in order to improve the stability margins, the control gain in the channels at orders 15, 17, and 19 is reduced to 1 while the control gain in other channels remains unchanged. The results are shown in Figure 6.22.

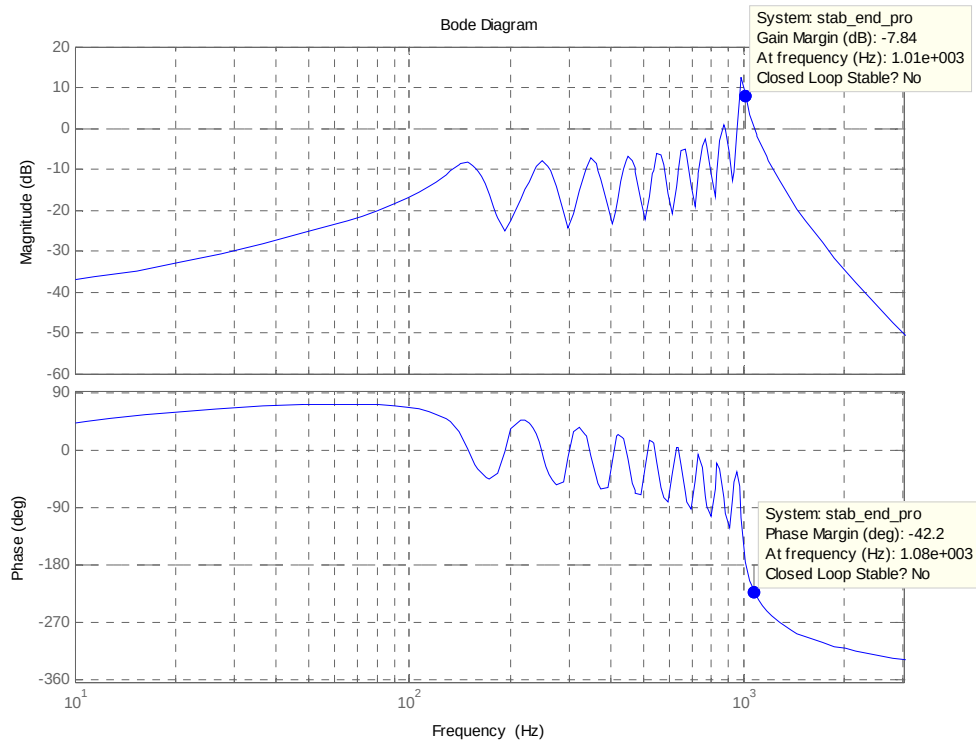

Figure 6.21 Instable system with the control gain at 3

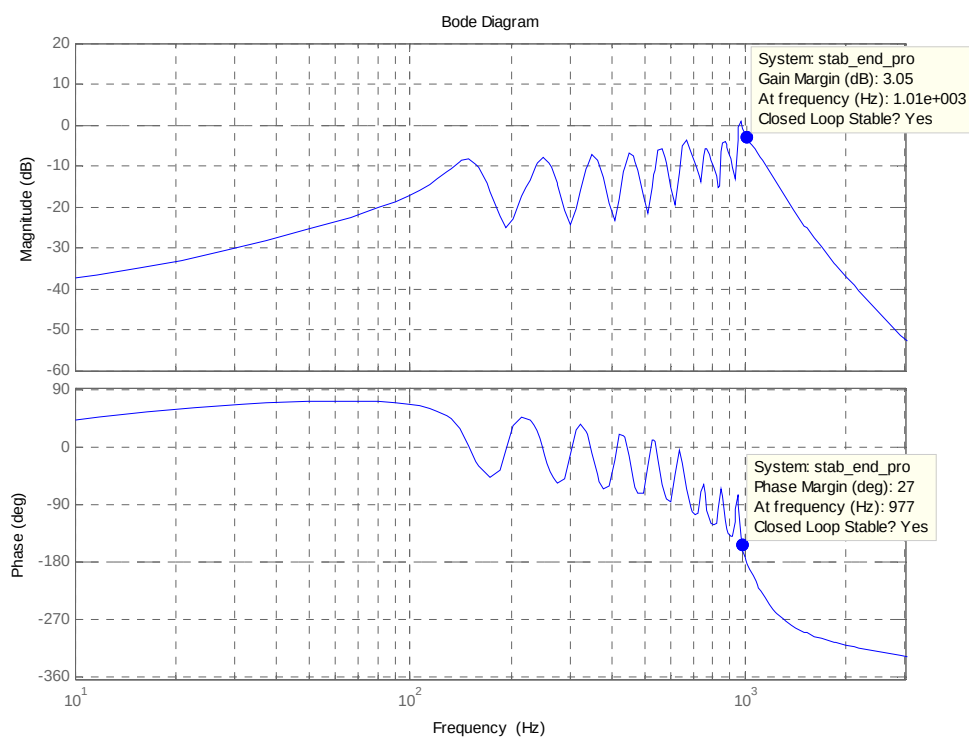

Figure 6.22 Stability margins improved by using uneven gain values

Another benefit of this uneven-value gain for the channels is that it improves the effectiveness of the system. Considering 5^{th} and 7^{th} harmonics are dominant in the system, the control gain in these two channels can be increased to a high level while the system remains stable. This is achieved by reducing the control gain at other channels. Figure 6.23 presents the results with the control gains at 10 for the 5^{th} and 7^{th} harmonics and 1 for others. It can be seen that the system is still stable although the maximum control gain reaches about 5 times of that before the adjustment (2.11).

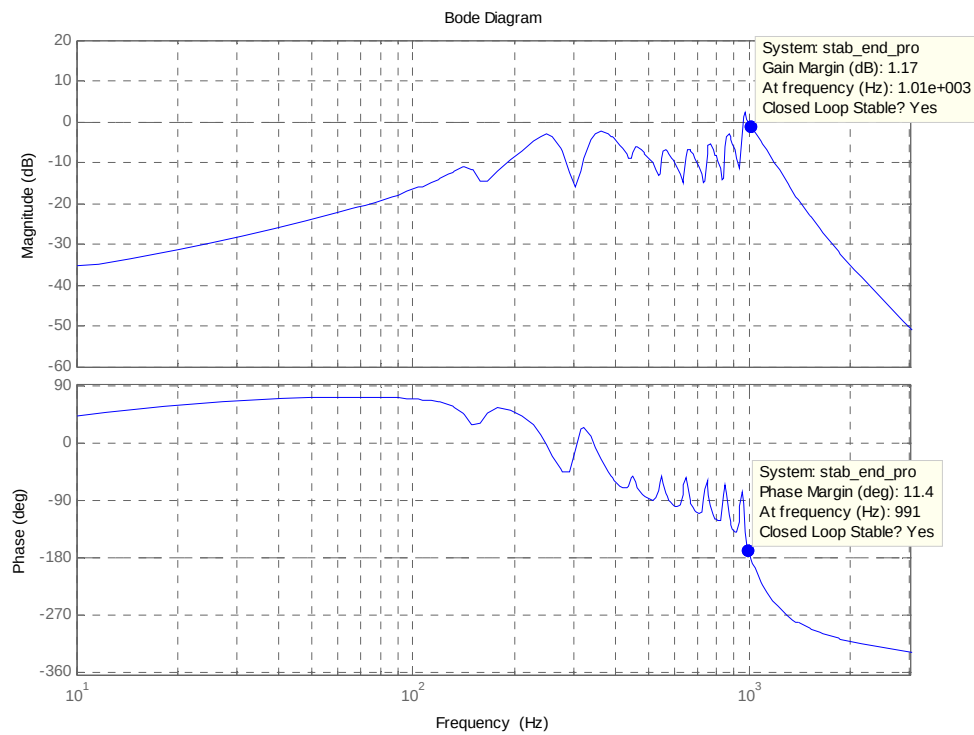

Figure 6.23 Stable system with an increase of the maximum control gain

III. The role of the angle of the control gain

In order to clearly show the role of the angle of the control gain, the magnitude

of the control gain in all channels remains unchanged (e.g., 3). From Figure 6.21, it is indicated that if the phase angle at 1080 Hz is raised, the system turns stable. At the point with a negative margin, a positive phase (leading) compensation is necessarily adopted in the controller. By adjusting the value of the angle obtained from the bode diagram, the stable system turns stable finally, with a positive angle compensation of 63° at order 19. The result is presented in Figure 6.24.

Moreover, the stability margins may be further improved by adjusting the angles at other orders. Figure 6.25 gives the result of the case with the compensation angles of 63°, 49°, and 40° at orders 19, 17, and 15, respectively. It is drawn that the stability margins are improved from 0.341 to 2.41.

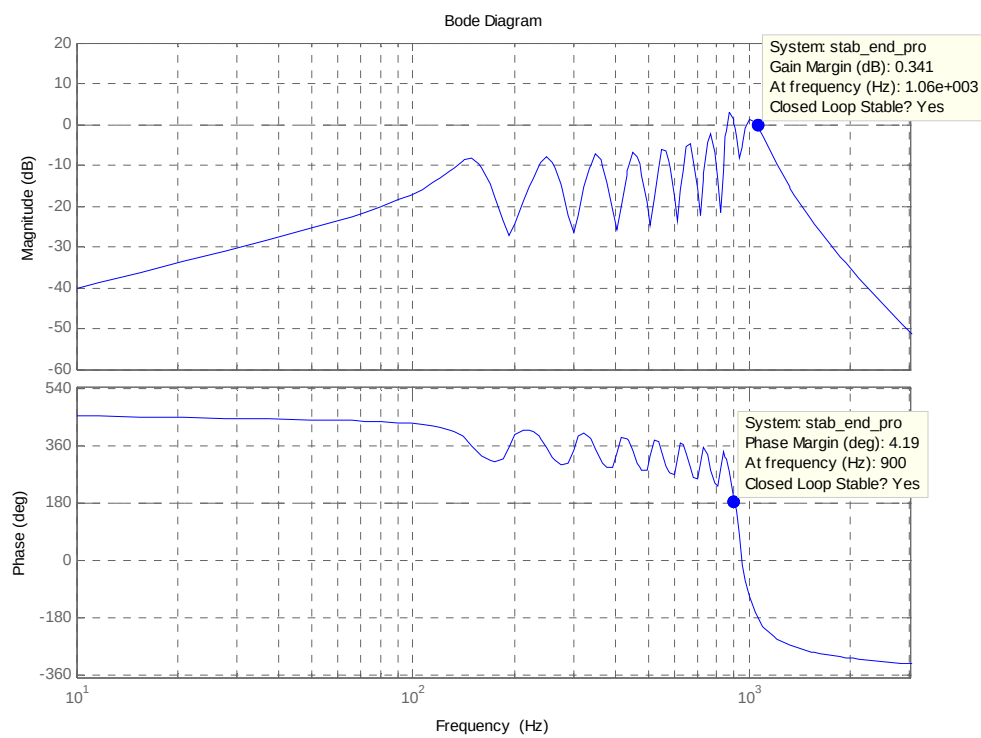

Figure 6.24 Stable system with the angle compensation in the control gain

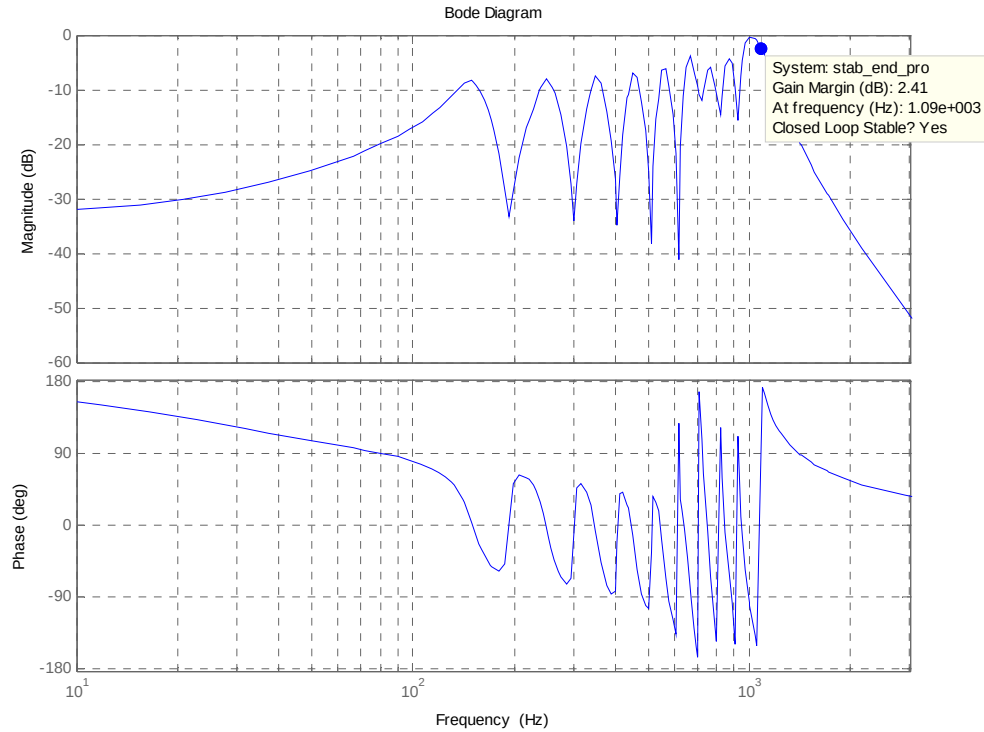

Figure 6.25 Improvement of the stability margins by adjusting the angles in the control gain

IV. The role of the cutoff frequency of the low pass filter

The cutoff frequency of the low pass filter may have a significant impact on the stability of the proposed controller. Compared with the case in Figure 6.21, the case with the cutoff frequency at 3 Hz and others unchanged is shown in Figure 6.26. The improvement of the stability margins is obvious, which reach 10.4 dB and 37.4º for gain margin and phase margin, respectively.

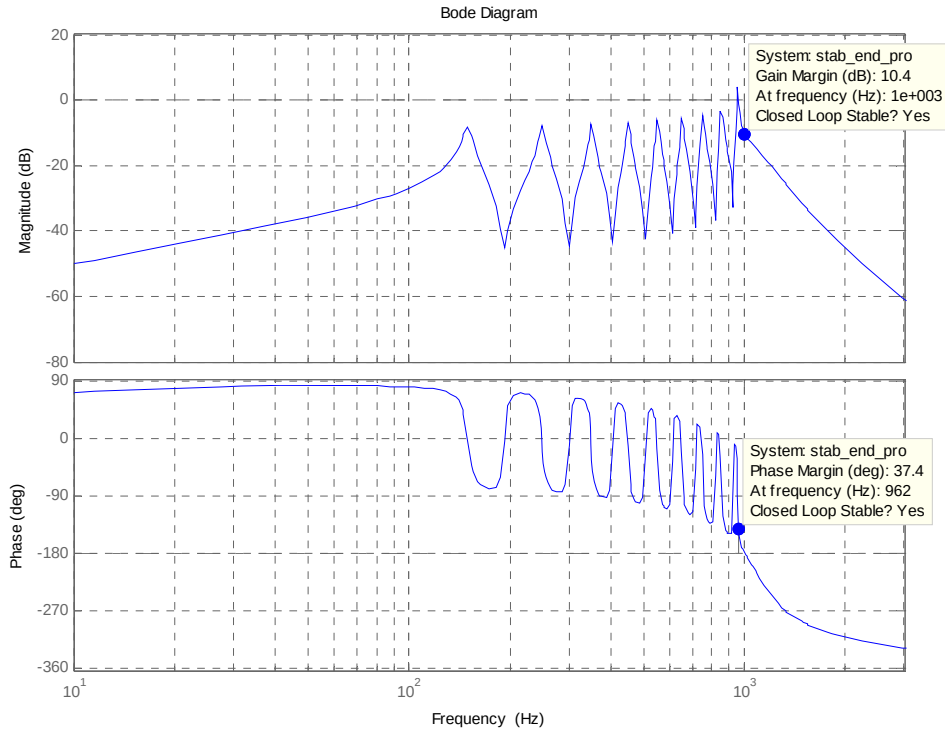

Figure 6.26 Role of the cutoff frequency of the low pass filter in improving the system stability

6.5.3 Selection of the Parameters

It is indicated that the selection of the parameters of the control system has much impact on the stability of the system. It also can be predicted that these parameters have significant impact on the performance of the proposed SAPF. The stability conditions should be essentially satisfied. The approaches used in the thesis such as by the analysis of the transfer function in the s-domain, computer simulation methods are effective methods. In this section, the strategies of determining the cutoff frequency of the low pass filter and the initial control gains is discussed.

The cutoff frequency of the low pass filter determines the width of the pass-band of the filter. The larger cutoff frequency leads to the coupling of different channels while the smaller cutoff frequency may result in the attenuation of the desirable signals and big response time. It can be seen that the minimum difference of the concerned harmonic frequency may be 100 Hz. This means the low pass filter should at least provide enough attenuation to the 100 Hz in the harmonic synchronous channels. However, it seems too relax because the fundamental component in the detected signal is much large than the harmonic components. The filtered signals may still contain considerable fundamental components. Additionally, there are always some noises in most channels with width and unpredictable frequencies. Therefore, for conservative implementation, the cutoff frequency may be set within 15 Hz. Generally, if there is enough resources for the implementation of the system, smaller cutoff frequency will obtain more precise control and better results. The characteristics of the low pass filter can be analyzed in advanced in commercial software such as MATLAB.

Although the values of the control gain, in fact, may be varied according to the details of the compensated system, the initial values should be determined. It is shown that if the control gain in all channels is set to be a large value the system may be instable. The most significant harmonic components result in the largest value of the control gain in all the channels, such as the 5^{th} and 7^{th} orders of

harmonics. These values may be determined by

(a) the stability conditions, which are achieved by the bode figures or satisfy the following conditions.

$$\begin{cases} \left|H_{apf}(s)\right| = 1 \\ \angle H_{apf}(s) + 180^{\circ} \rangle 0 \end{cases} \quad \text{and} \quad \begin{cases} \angle H_{apf}(s) + 180^{\circ} \langle 0 \\ \left|H_{apf}(s)\right| \langle 1 \end{cases}$$

where $H_{apf}(s)$ is the derived transfer function of the proposed SAPF, and $\left|H_{apf}(s)\right|$, $\angle H_{apf}(s)$ are the magnitude and the phase angle, respectively.

(b) referring to the system impedance compensated like $k_{vh} = \frac{1}{Z_h}$, which is a reference value used as the basis. [Keiji Wada etc. 2002] The actual values should be determined according to the compensating requirement. The less expected harmonic voltage distortion left, the larger values are.

6.6 The Performance of The Proposed SAPF

As discussed before, the proposed SAPF based on voltage detection is installed at the end of the distribution circuit. The parameters of the system are given in Table 6.6, and the configuration of the distribution system is shown as in Figure 6.7.

To assess the effectiveness of harmonic mitigation by the SAPF, a ratio of the voltage with the SAPF being connected over that with the SAPF being disconnected is introduced. Using the transfer functions of the distribution system and the SAPF, the ratio can be derived as,

$$\frac{V_{con}(s)}{V_{discon}(s)} = \frac{1/Y_{total}}{1/Y_{sapf}} = \frac{Y_{sapf}}{Y_{total}} \tag{6.53}$$

where Y_{sapf} and Y_{total} mean the admittance before installing the SAPF and after installing the SAPF, seen from the point of the installation of the SAPF. Substituting the model of the distribution system and the proposed SAPF, the admittance of the LV distribution system and of the total system are written as,

$$Y_s = \frac{s^4 L_1 L_2 C_1 C_2 + s^3 (R_1 L_2 C_1 C_2 + R_2 L_1 C_1 C_2) + s^2 (L_1 C_1 + L_1 C_2 + L_2 C_2 + R_1 R_2 C_1 C_2) + s(R_1 C_1 + R_1 C_2 + R_2 C_2) + 1}{s^3 L_1 L_2 C_1 + s^2 (R_1 L_2 C_1 + R_2 L_1 C_1) + s(L_1 + L_2 + R_1 R_2 C_1) + R_1 + R_2} \tag{6.54}$$

and

$$\begin{aligned} Y_{total} = & \frac{s^4 L_1 L_2 C_1 C_2 + s^3 (R_1 L_2 C_1 C_2 + R_2 L_1 C_1 C_2) + s^2 (L_1 C_1 + L_1 C_2 + L_2 C_2 + R_1 R_2 C_1 C_2) + s(R_1 C_1 + R_1 C_2 + R_2 C_2) + 1}{s^3 L_1 L_2 C_1 + s^2 (R_1 L_2 C_1 + R_2 L_1 C_1) + s(L_1 + L_2 + R_1 R_2 C_1) + R_1 + R_2} \\ & + \sum_h \left(2 \cdot |k_{vh}| \cdot A_0 \frac{\cos(\alpha_h) \cdot (1 + s \cdot T_c) - \sin(\alpha_h) \cdot h\omega \cdot T_c}{(1 + s \cdot T_c)^2 + (h\omega \cdot T_c)^2} \right) \cdot \frac{K_c}{T_{vo} \cdot L_f \cdot s^2 + L_f \cdot s + K_c} \end{aligned} \tag{6.55}$$

In order to investigate the mitigation effect, the following conditions are considered, one for the capacitors band being disconnected and the other for the capacitors bank being connected. The case with the capacitor bank being disconnected is to analyze the worst harmonic-polluted case in that the capacitor may bypass some contents of the harmonics and to exclude the possible harmonic resonance. The case with the capacitor bank being connected is tuned to proper frequency to identify the effect of the proposed SAPF on the harmonic resonance.

6.6.1 Harmonic Compensation for the System without the Capacitor Bank

Substituting the parameters in Table 6.5-6.6 to the Equation (6.55), the

Equations are simplified as,

$$
\begin{aligned}
Y_{total} &= \frac{1}{s(L_1+L_2)+R_1+R_2} + \sum_h \left(2\cdot|k_{vh}|\cdot A_0 \frac{\cos(\alpha_h)\cdot(1+s\cdot T_c)-\sin(\alpha_h)\cdot h\omega\cdot T_c}{(1+s\cdot T_c)^2+(h\omega\cdot T_c)^2} \right) \cdot \frac{K_c}{T_{vo}\cdot L_f\cdot s^2+L_f\cdot s+K_c} \\
&= \frac{1}{s\cdot 0.0001004+0.0448} + \sum_h \left(2\cdot|k_{vh}|\cdot \frac{\cos(\alpha_h)-\sin(\alpha_h)\cdot 4.9926\cdot h+s\cdot\cos(\alpha_h)\cdot 0.0159}{(1+s\cdot 0.0159)^2+(4.9926\cdot h)^2} \right) \cdot \frac{2.5}{10^{-7}\cdot s^2+10^{-3}\cdot s+2.5}
\end{aligned}
\tag{6.56}
$$

By substituting above two equations into the Equation (6.53), the bode diagrams are drawn by using MATLAB to investigate the mitigation effect. The impact of the parameter k_{vh} is analyzed.

In Figure 6.27 the ratios of the voltage with the SAPF being connected over that with the SAPF being disconnected are presented with the different values of k_{vh}. In order to identify the impact of k_{vh} clearly, only the control gains at the 5th and 7th harmonics are considered and the value of α_h is considered to be zero. It can be seen that with the increase of the control gains, the harmonic mitigation is more effective. When the $k_{v5}=k_{v7}=32$, the ratios are 0.18 and 0.14 for the 5th and 7th harmonics, respectively. For an example, the voltage distortions are both 5% before connecting the SAPF, after connected the voltage distortions are reduced to 0.9% and 0.7% for the 5th and 7th harmonics, respectively.

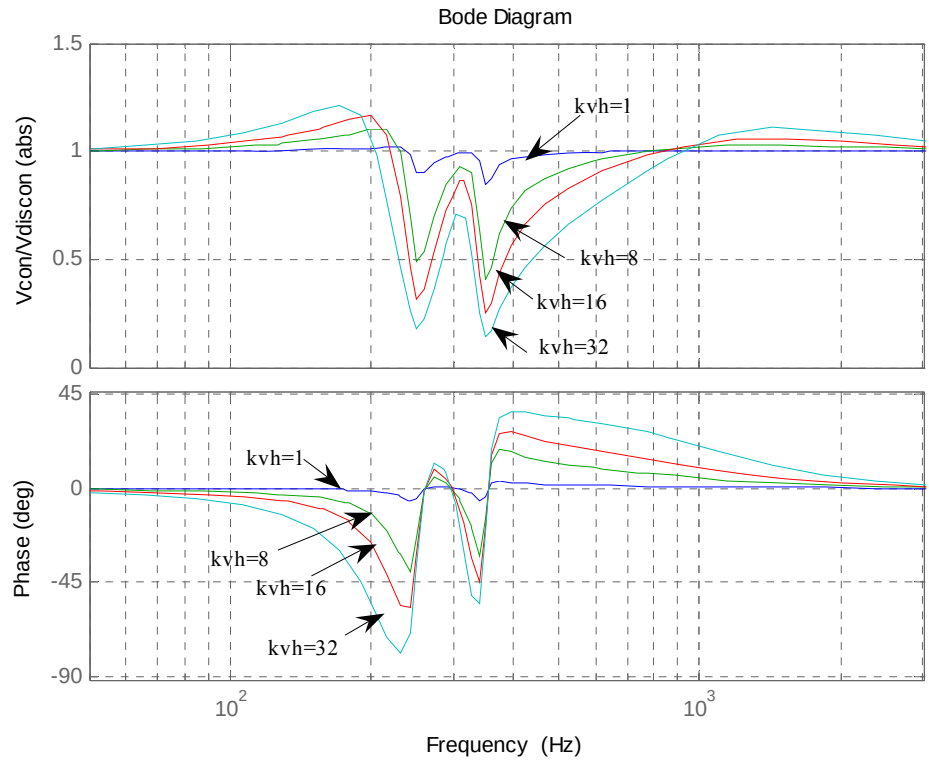

Figure 6.27 The voltage ratios at installation point with the different values of k_{vh}

6.6.2 Harmonic Compensation for The System with the Capacitor Bank

In order to study the damping effect of the proposed SAPF, the distribution system is tuned to form a harmonic resonance at a lower order. For simplicity, only the capacitor C_2 is switched on and the line inductance is assumed as 0.8 mH. Consequently, a parallel resonance is observed with the resonant frequency near the 7^{th} order, as shown in Figure 6.28. Then, the Equations (6.54-6.55) become

$$Y_s = \frac{s^2\left(L_1C_2 + L_2C_2\right) + s\left(R_1C_2 + R_2C_2\right) + 1}{s\left(L_1 + L_2\right) + R_1 + R_2} = \frac{s^2 \cdot (2.051\text{e-}7) + s \cdot (1.12e-5) + 1}{s\left(0.0008204\right) + 0.0448} \quad (6.57)$$

$$Y_{total}=\frac{s^2\left(L_1C_2+L_2C_2\right)+s\left(R_1C_2+R_2C_2\right)+1}{s\left(L_1+L_2\right)+R_1+R_2}+\sum_h\left(2\cdot\left|k_{vh}\right|\cdot A_0\frac{\cos\left(\alpha_h\right)\cdot\left(1+s\cdot T_c\right)-\sin\left(\alpha_h\right)\cdot h\omega\cdot T_c}{\left(1+s\cdot T_c\right)^2+\left(h\omega\cdot T_c\right)^2}\right)\cdot\frac{K_c}{T_{vo}\cdot L_f\cdot s^2+L_f\cdot s+K_c}$$
$$=\frac{s^2\cdot(2.051\text{e-}7)+s\cdot(1.12e-5)+1}{s(0.0008204)+0.0448}+\sum_h\left(2\cdot\left|k_{vh}\right|\cdot\frac{\cos\left(\alpha_h\right)-\sin\left(\alpha_h\right)\cdot 4.9926\cdot h+s\cdot\cos\left(\alpha_h\right)\cdot 0.0159}{\left(1+s\cdot 0.0159\right)^2+\left(4.9926\cdot h\right)^2}\right)\cdot\frac{2.5}{10^{-7}\cdot s^2+10^{-3}\cdot s+2.5} \quad (6.58)$$

The equivalent impedance is drawn by using MATLAB to investigate the damping effect, as shown in Figure 6.29. The k_{v7} is set at 1. It is clearly that the impedance at 351 Hz is reduced from 73.2 ohms to 1.26 ohms. The impedance at 302 Hz is reduced slightly. However, the impedance at 397 Hz is increased from 7.84 ohms to 9.32 ohms. It may be indicated that the resonance frequency is shifted upward.

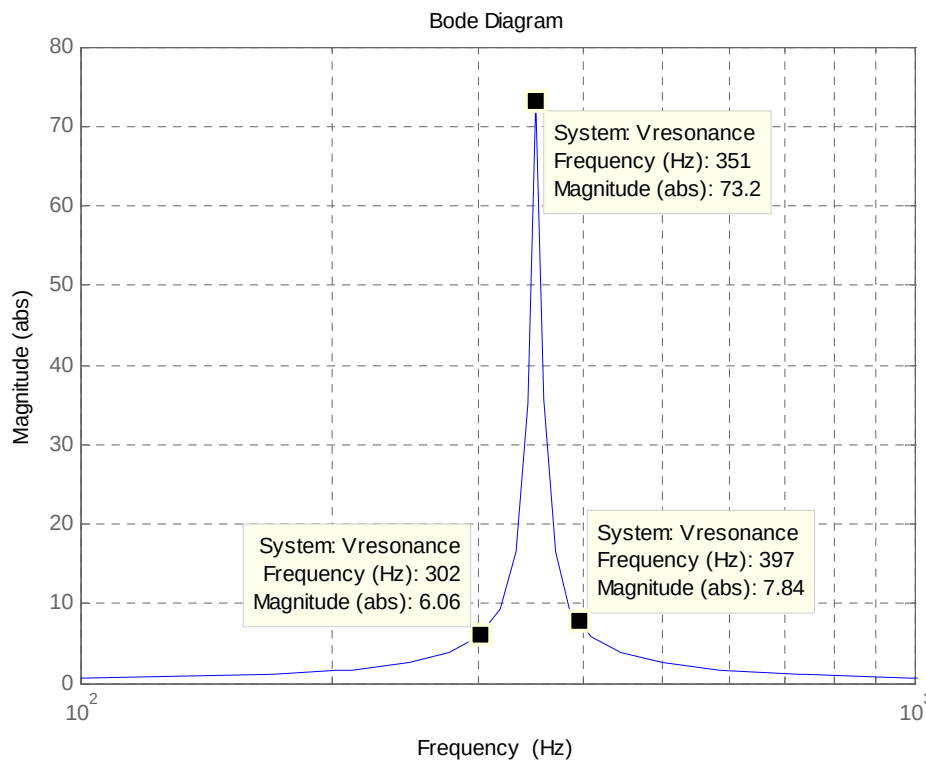

Figure 6.28 Harmonic resonance round the 7th harmonic ($1/Y_{sapf}$)

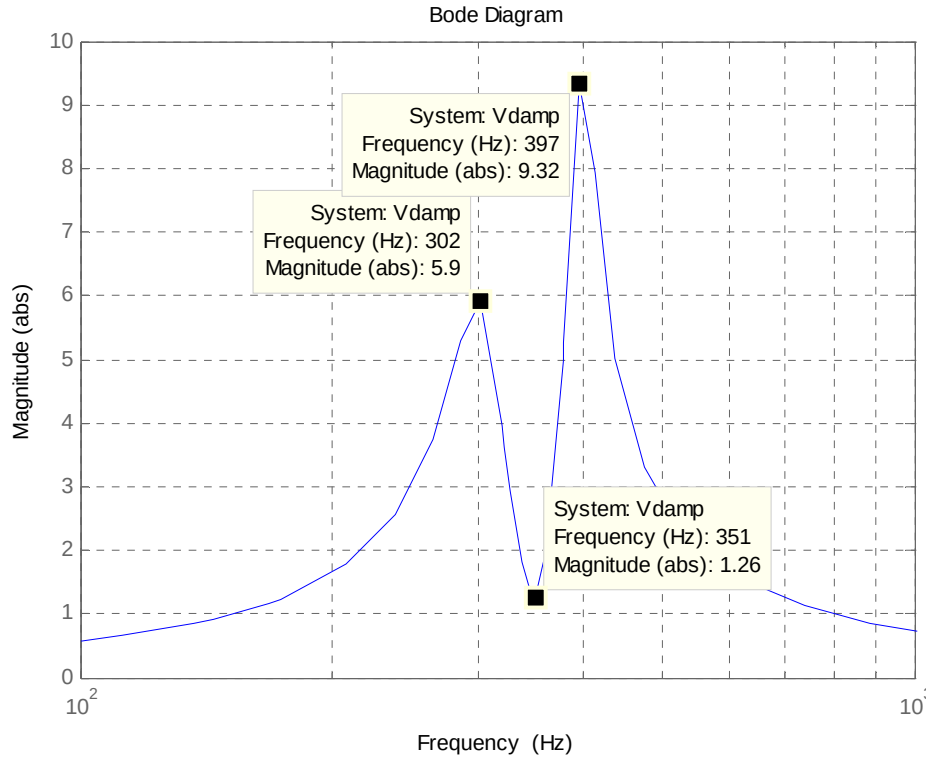

Figure 6.29 Damping effect of the SAPF ($1/Y_{total}$)

The phenomenon of shifting of the resonance frequency is observed. To reveal the shift of resonant frequency, the transfer function of the system impedance seen from the point of installation $Z_{total} = 1/Y_{total}$ is analyzed. Shown in Figure 6.30 is shifting of the resonance frequency with increasing k_{v7}. It is noted that the larger control gain, the smaller equivalent impedance is, which results in more damping of harmonic resonance. Also, with the increasing control gain, the possible resonance frequency is shifted upward.

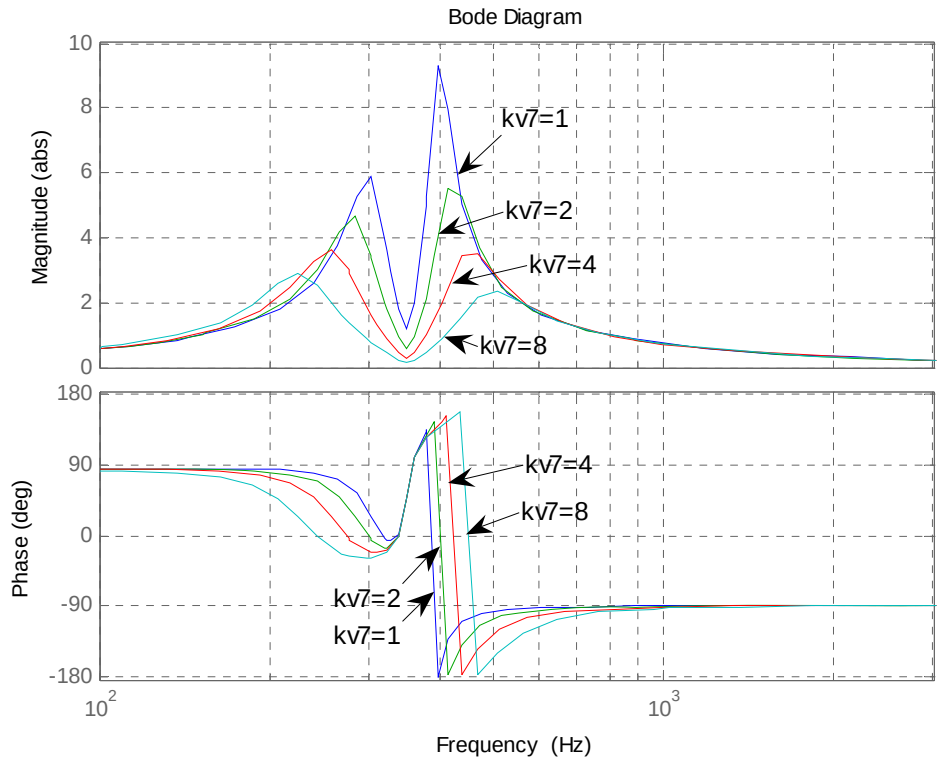

Figure 6.30 Upward shifting of the resonance frequency with increasing k_{v7}

As seen in Figure 6.30 selecting appropriate values of the corresponding control helps to damp out the possible resonance further.

6.7 Summary

In this chapter, a shunt active power (SAPF) filter based on voltage detection was proposed which aims at eliminating harmonic voltage distortion along the building distribution system.

The multi-channel complex gain controller was developed, which improved the stability margins of the proposed SAPF system and the maximum values of the

control gain. The complex control gains made the output of the SAPF tunable. The SAPF may behave like a resistor, inductor, capacitor, or a combination of these elements. Using the techniques of unequal-value gain in different channels and the phase compensation at higher orders the problem of system instability, which is a common problem to voltage-detection SAPFs, can be shoveled effectively.

The performance of the proposed SAPF shows the capability of improving harmonic voltage distortion and damping of harmonic resonance in radial electrical systems. The large magnitude of the control gains may result in better effect if the system is stable.

The analytical analysis in the s-domain is proven as one of effective approaches for such control systems. The analytical model of the proposed SAPF as well as the LV distribution system is derived in the s-domain. The approach of deriving transfer functions of the control system with multiple reference frames may be extended to other applications.

In the following chapters, the computer simulations and experiments in the laboratory will be presented to validate the proposed SAPF.

Chapter 7

Computer Simulation of the Proposed SAPF

7.1 Introduction

In this chapter, the computer simulation is conducted on the platform of MATLAB/SIMULINK for validation and characterization of the proposed SAPF.

Simulation models of both the building distribution system and the proposed SAPF are developed first. The characteristics of the proposed SAPF are then addressed, such as the DC loop performance, the transient response of the SAPF and tracking of the reference currents etc.. Several issues, such as the impact of both the control gain and the low pass filter on system stability, filtering performance, resonance damping, etc. are investigated.

7.2 Simulation Models on the Platform of MATLAB/SIMULINK

MATLAB is a high-performance language for technical computing. It integrates computation, visualization, and programming in an easy-to-use environment where problems and solutions are expressed in familiar mathematical notation. It is broadly applied in Math and computation, Algorithm development, Data

acquisition, Modeling, simulation, and prototyping, Data analysis, exploration, and visualization, Scientific and engineering graphics, Application development, etc..

In the last few years, Simulink has become the most widely used software package in academic and industry for modeling and simulating dynamic systems. It may become easy to build models from scratch, or take an existing model and add to it. Simulations by Simulink are interactive, which means if change parameters on the fly and immediately see what happens. In the simulink environment, the results can be analyzed and visualized by instant access to all the analysis tools in MATLAB. There are many toolboxes that provide specific, basic and detailed models in some professional domains. It makes the procedure of modeling and simulating easier and interesting. Simulink is also practical. With thousands of engineers around the world using it to model and solve real problems, knowledge of this tool is helpful in many researches. For modeling and simulating power electric system, the blockset of SimPowerSystems is the most important block set. SimPowerSystems and other toolboxes or blocksets work together with Simulink to model or to simulate electrical and control systems.

The system model for computer simulation includes two sections, the section of the distribution system and the section of the SAPF system. Modeling of the

distribution system is mainly done by using the standard blocks available in the block set of SimPowerSystems. These standard blocks have been already developed for power sources, distribution transformers, cables or lines, capacitor banks, harmonic-producing loads, power devices such as IGBTs with inverse diodes, linear loads, voltage/current measurement tools, bus bars and other normal appliances used in the system. With these standard blocks, a three-phase four-wire model is set up for the simulation. For increasing simulation speed the distribution system is implemented in the discrete time with the step of 1e-6 second.

In the proposed SAPF, both voltages and currents in the system are sampled every 100e-6 second. These measured signals are processed to generate the switching vectors within the digital control loop every 100e-6 second. As the switching frequency in the power device is 10kHz, the switching vectors, applied to the IGBT modules is updated again 100e-6 second. Figure 7.1 illustrates a block diagram of the SAPF model. In the controller, the control components are realized by directly using existing blocks in the SIMULINK library, such as constant, mathematic operation, logic operation, digital low pass filter, PI controller and so on. The control algorithms are achieved by simply combining these basic blocks, such as Clarke transformation, Park transformation.

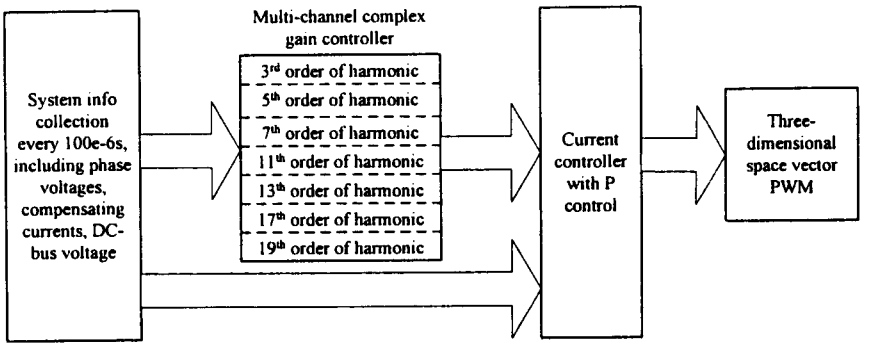

Figure 7.1 Block diagram of the proposed SAPF model in the SIMULINK

Figure 7.2 describes the configuration of the system to be simulated in the MATLAB/SIMULINK platform. Table 7.1 shows the system parameters adopted in the computer simulation. The three-phase power supply is rated 11kV (RMS) and 50Hz with an equivalent short circuit impedance. The distribution transformer is rated 11kV/380V 1500 kVA with the short-circuit impedance of 6%. Two configurations of the distribution circuit are considered in the simulation, which represent the short rising main circuit and the long rising main circuit, respectively. The capacitor bank has a capacitance of 250 μF per phase. In studying the damping effect of the proposed SAPF, harmonic resonance in the distribution system is tuned at the frequency around 350 Hz. The output inductors of the proposed SAPF have an inductance of 1 mH. Both sampling rate of the controller and switching frequency of the power device are set at 10 kHz.

Table 7.1 Information of the system in the simulation

The distribution system				The proposed SAPF	
11kV SCC	350MVA			DC-bus capacitor	2350μF
Transformer	1500kVA, 11kV/380V, 6%			Output inductance	1mH
Feeder/Riser impedance		Resistance	Inductance	Switching frequency	10kHz
	Case I	52.8mΩ	95.5μH		
	Case II	0.2 Ω	0.82mH	P control gain	2.5
Harmonic loads	Single-phase and three-phase Rectifiers			Cutoff frequency of low pass filter	10 Hz
Capacitor for PFC	250μF				

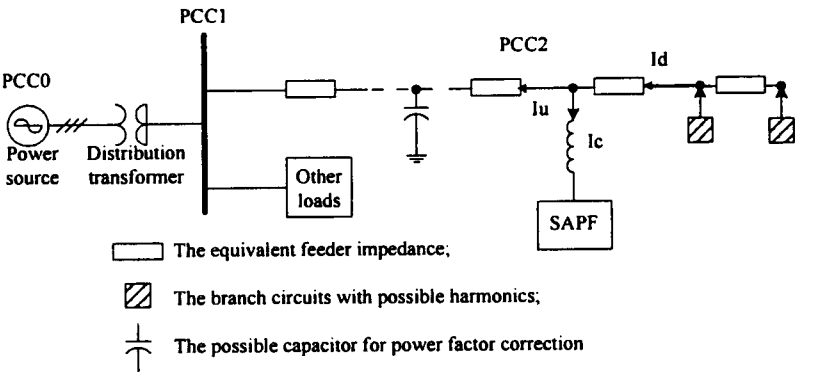

Figure 7.2 Configuration of the system to be simulated in the MATALB/SIMULINK platform

7.3 Characteristics of the Proposed SAPF

In this section, the characteristics of the proposed SAPF are investigated, including charging of the DC-bus voltage, the transient response, and tracking of the reference currents. These have a significant impact on the performance of the SAPF.

7.3.1 Charging of the DC-bus Voltage

Charging of the DC-bus capacitor in the proposed SAPF is made by the DC-bus voltage control loop, which is the control channel operated at the fundamental frequency in the multi-channel complex gain controller. This charging process is not affected by the configuration of the distribution system. A stable DC-bus voltage is necessary for the SAPF to provide a good performance in filtering harmonics. The unexpected ripple in the DC bus will cause a disturbance in the output of the SAPF. On the other side, a change of the filter output also affects the DC bus voltage. The abrupt large variation in the output may result in a big change in the DC bus, which in the extreme case leads to the DC bus uncontrollable.

Figures 7.3 (a) and (b) present voltage and current responses on the DC-bus capacitor during a charging process. As the PI control method is adopted in the DC-bus voltage control loop, the DC-bus voltage is charged fast. It reaches its peak value after about 6 ms, and quickly returns to the setting value of 600 V and becomes stable after 15 ms. It is noted that the DC-bus voltage has a slight ripple around 600 V, which mainly results from the power losses in the IGBT modules and the output filter.

Figure 7.3 (b) shows the charging current in the DC-bus capacitor. The charging current contains much high-frequency components especially at the frequencies around 10kHz, which result from the switching operation of the IGBT modules.

At the early stage of capacitor charging, the charge current is significantly high due to low initial voltage on the DC-bus capacitor. With the positive real power flowing into the DC bus continuously, the DC-bus voltage is increased, and the charging current is decreased. After the DC-bus voltage is stabilized, the charging current remains at a very low level.

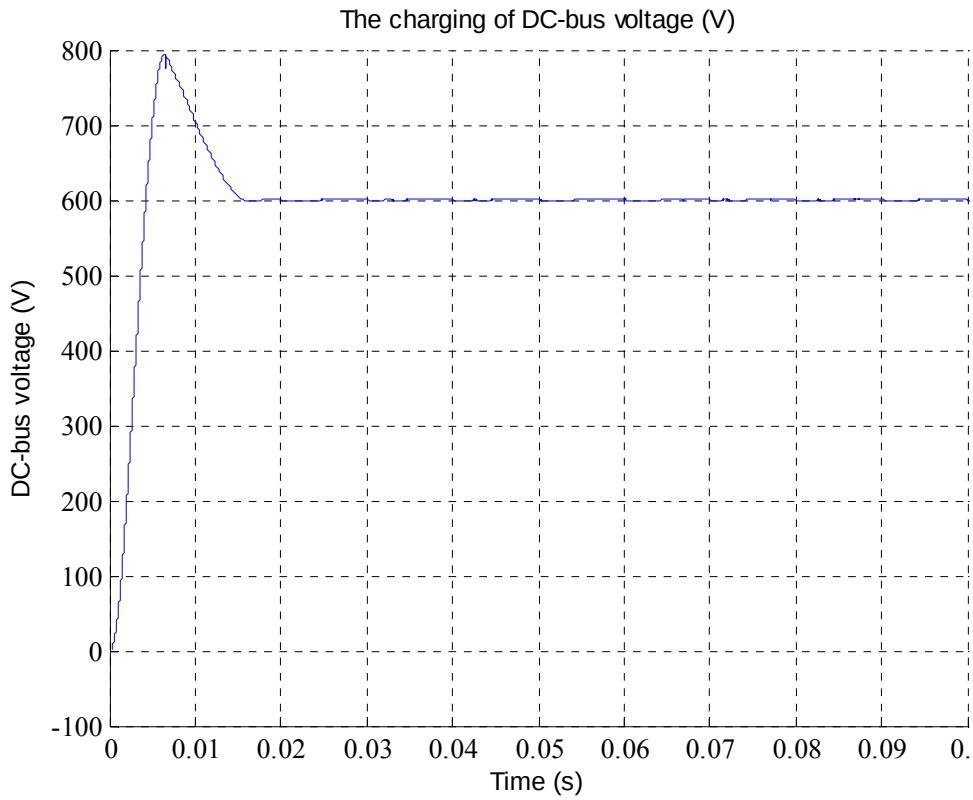

Figure 7.3 (a) DC-bus voltage in the charging process

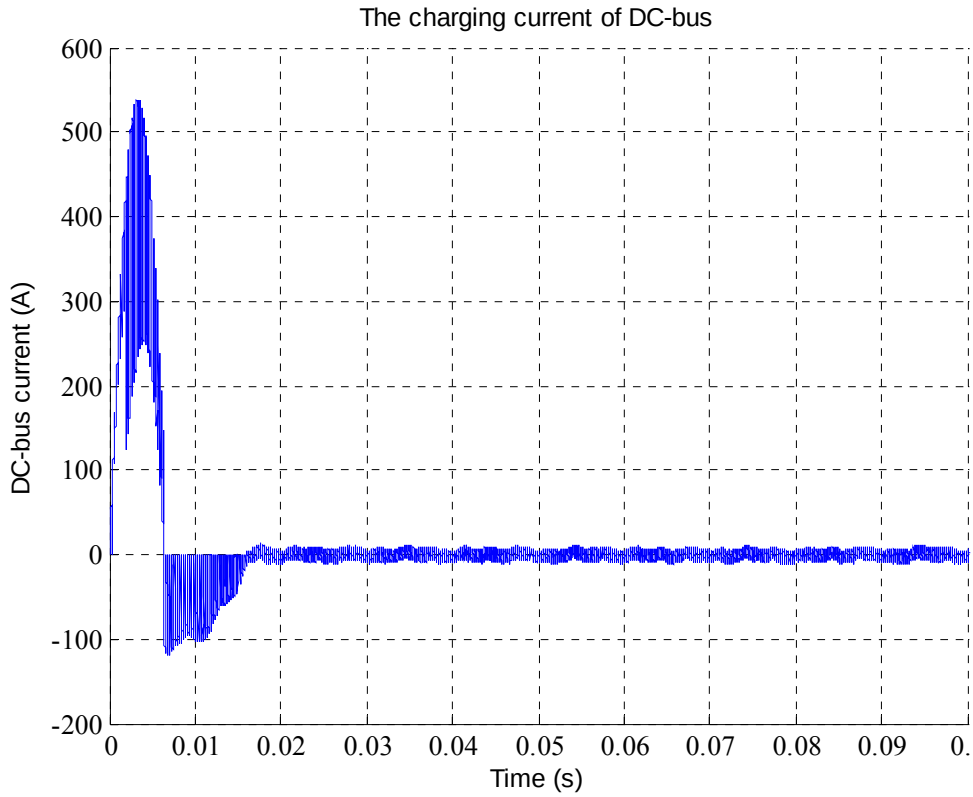

Figure 7.3 (b) DC-bus current in the charging process

7.3.2 Transient Response of the SAPF

The transient response of the proposed SAPF is examined under the configuration (I). All the control gain is set at 16 for channels, except the one for DC-bus voltage control. Two cases are considered in the simulation. In the first case, the harmonic-producing loads are suddenly increased by 100%, as shown in Figure 7.4 (a). In the second case, all the harmonic-producing loads are suddenly connected to the system, as shown in Figure 7.4 (b). In those figures current from harmonics-generating loads Id, compensating current Ic, current in the supply circuit Iu, phase voltage at the connection point Vs and DC-bus voltage VDC are all presented.

The sudden change of the harmonic-producing loads in both cases is made at the time of 0.15 s. As seen from these figures the compensating currents from the SAPF are increased to maintain lower harmonic distortion in the system at 0.15 sec. After one fundamental cycle, the compensating currents are nearly stable, which is clearly observed in Figure 7.4 (b). This shows the quick response of the control system in the proposed SAPF. As seen from these figures, the phase voltage seems to be unaffected by that change. Also, the DC-bus voltage remains stable during the transient period.

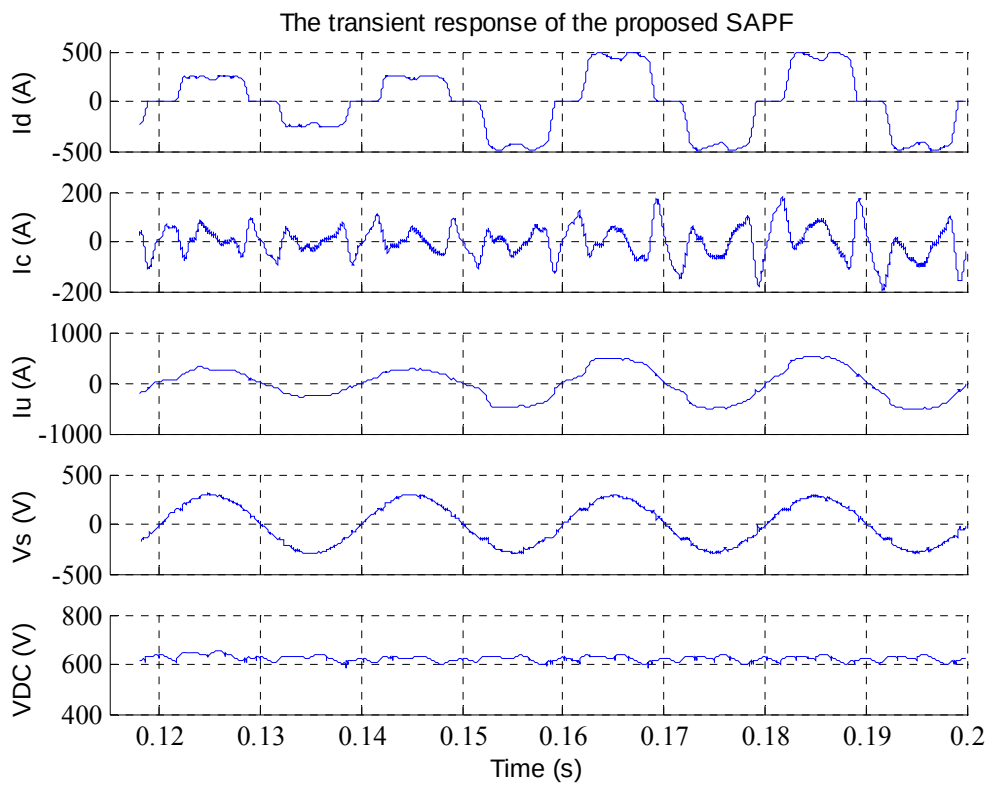

Figure 7.4 (a) Transient responses of the proposed SAPF with an increase of harmonic-producing loads by 100%

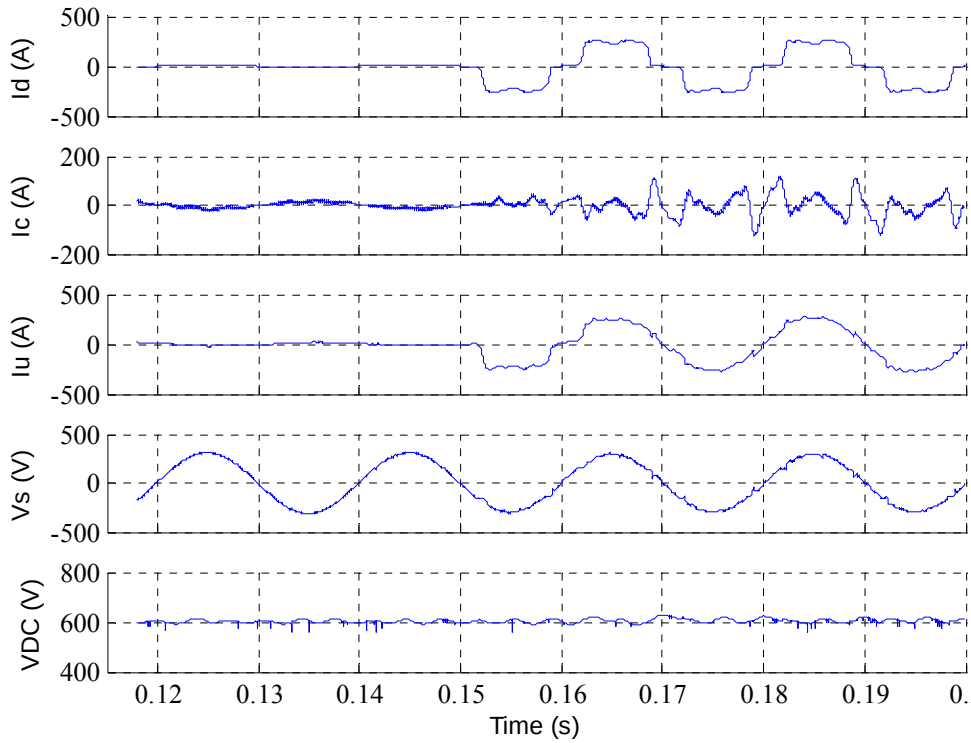

Figure 7.4 (b) Tansient responses of the proposed SAPF with a sudden connection of harmonic-producing loads to the distribution system

7.3.3 Tracking of the Reference Currents

Tracking of the reference currents is primarily conducted by the current regulator. In the proposed SAPF, the proportion control is adopted in the current regulator. The drawback of this method, such as limited bandwidth can be compensated by the multi-channel complex gain controller. The impact of the current regulating method on SAPF performance is less significant. This has been addressed in the previous chapter.

The low pass-bandwidth is the main feature of a P controller which leads to

magnitude attenuation and phase shifting at the higher frequencies. Figure 7.5 shows one part of the reference current and the compensating current curves obtained in the simulation. The reference current and the compensating current are indicated by the solid curve and the dashed curve, respectively. It is found that the two curves basically match in most parts although the compensating current has a slight time delay, compared with the reference current. At the time of around 0.155 s, the compensating current misses tracking the reference one. In addition, the compensating current contains rich high-frequency components at about 10 kHz, which results from the switching operation of the IGBT module. This switching ripple is actually filtered by the switching ripple filter connected in parallel with the SAPF before the compensating current goes into the electrical system.

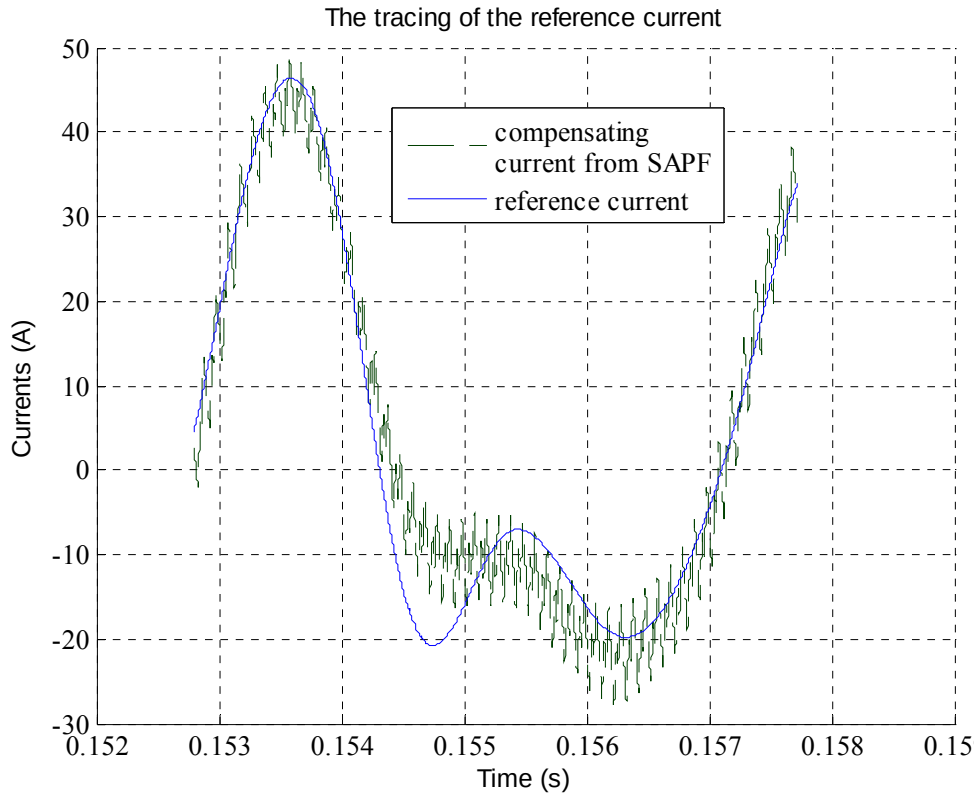

Figure 7.5 Tracing of the reference currents

7.4 Performance of the Proposed SAPF

7.4.1 Harmonic Mitigation by Varying the Control Gain

In order to investigate the role of the control gains in the controller, the simulation was conducted under the configuration (I) by varying the control gains in the multi-channel and complex-gain controller. For simplicity in comparison, the control gain in one case is set to be same value with zero phase angle.

Figure 7.6 shows the phase voltage of the connection point and the current in

the supply circuit when the proposed SAPF is not connected. The major harmonic components at orders up to 19th are listed in Table 7.2. In the table the fundamental components are expressed in RMS values, and the harmonic components are presented in percentage of the fundamental value. It can be seen that both the phase voltages and supply currents contain much harmonic contents.

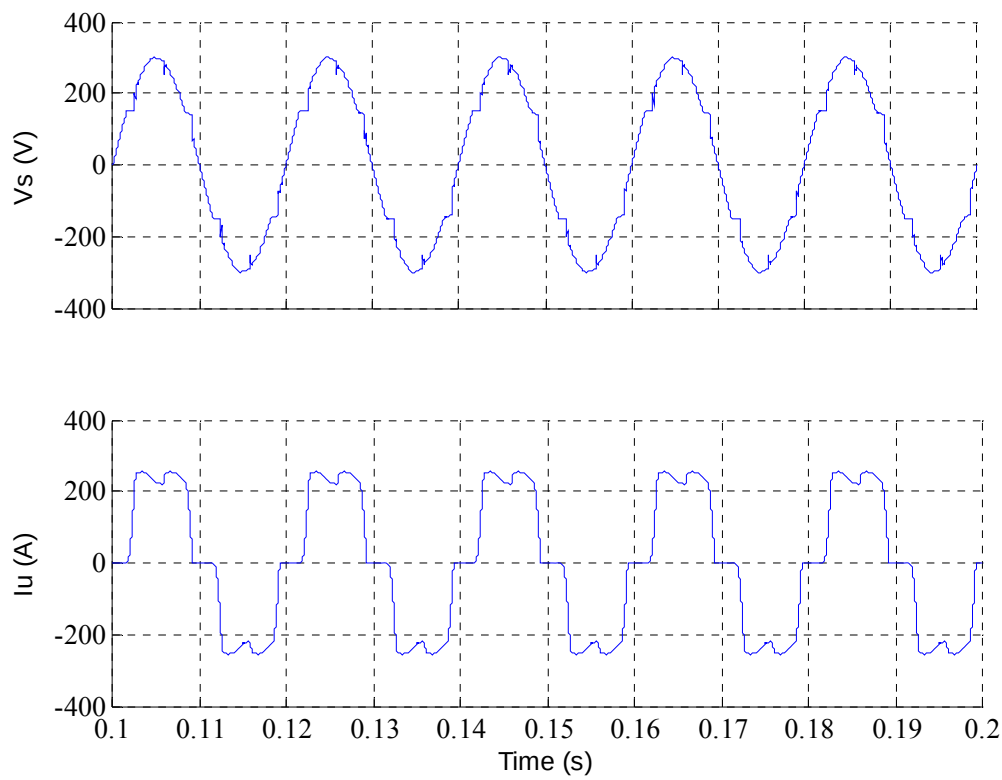

Figure 7.6 System voltage and current when the proposed SAPF is not connected

Figure 7.7 shows the simulation results when the proposed SAPF is switched on. Different values of the control gain were selected in the simulation. Both the phase voltage at the connection point and the current in the supply circuit are

presented when the control gain varies from 1 to 32. The result of the spectrum analysis is listed in Table 7.2. It is clearly seen that the harmonic distortion of the phase voltages and the supply currents at most of harmonic orders decreases with the increasing control gain. The harmonic voltage distortion at each order decreases below 1% when the control gain is set at a value more than 16.

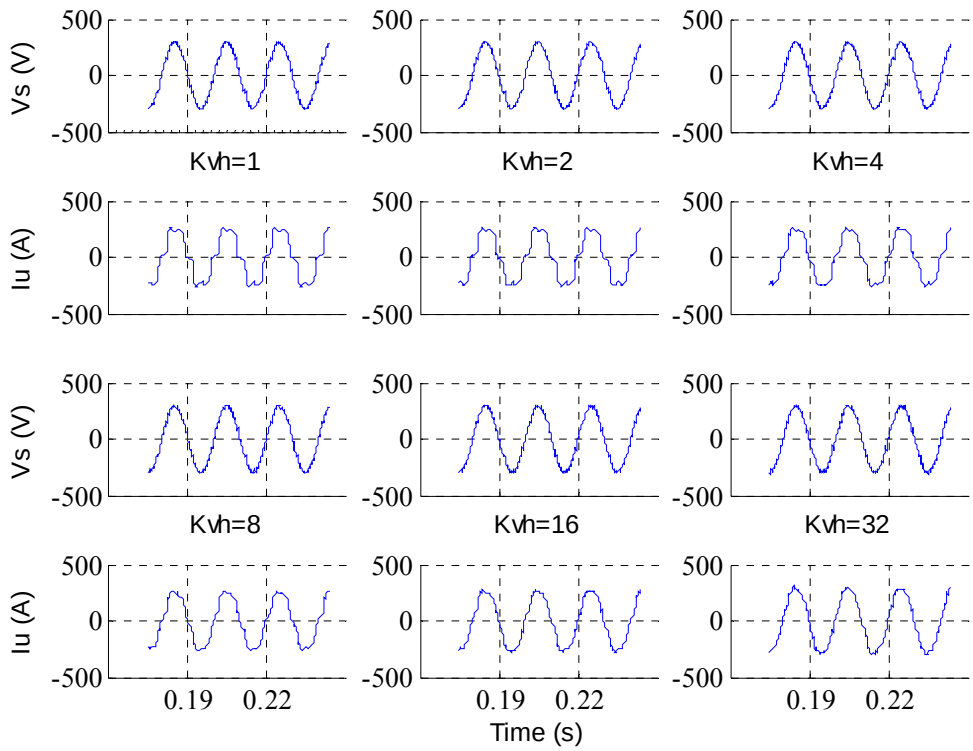

Figure 7.7 Simulation results when the proposed SAPF is switched on

Table 7.2 Results of the spectrum analysis when the proposed SAPF is switched on

	Order	1	5 (%)	7 (%)	11 (%)	13 (%)	17 (%)	19 (%)
Ref. (SAPF disconnected)	Vs	295V	3.76	2.34	2.64	1.76	1.80	1.08
	Iu	265A	22.1	9.92	7.28	4.11	3.17	1.66
kvh=1	Vs	295V	3.42	2.07	2.24	1.56	1.46	1.02
	Iu	265A	19.9	8.60	6.23	3.55	2.68	1.58
kvh=2	Vs	297V	2.93	1.78	1.78	1.18	1.28	0.77
	Iu	264A	17.7	7.50	5.15	2.88	2.20	1.33

kvh=4	Vs	296V	2.47	1.42	1.39	0.88	0.95	0.71
	Iu	264A	14.8	6.06	3.79	2.20	1.67	1.10
kvh=8	Vs	295V	1.73	1.02	0.95	0.64	0.68	0.34
	Iu	267A	10.4	4.42	2.43	1.42	1.09	0.67
kvh=16	Vs	295V	1.05	0.78	0.51	0.27	**0.31**	**0.17**
	Iu	279A	5.99	3.08	1.33	0.65	0.68	0.39
kvh=32	Vs	295V	0.31	0.41	0.31	0.07	**0.37**	**0.20**
	Iu	290A	1.69	1.34	0.86	0.24	0.62	0.31

7.4.2 Damping of Harmonic Resonance by the Proposed SAPF

The voltage-detection SAPF is capable of damping harmonic resonance occurring in the system. To investigate its damping performance the distribution system is tuned to have the harmonic resonance at 350 Hz with the parameters of configuration (II). The parameters of the proposed SAPF as well as the distribution system are given in Table 7.1. The control gains in the multi-channel complex-gain controller are set to be 1, 1, 3, 1, 1, 1, and 1 for harmonics at order 3, 5, 7, 11, 13, 17 and 19, respectively. The control gain at order 7 is relatively large as the resonance occurs at 350 Hz. Figure 7.8 and Table 7.3 show the simulated results of both phase voltages and supply currents when the proposed SAPF are switched off and switched on. In Table 7.3 the fundamental components are presented in RMS values, and the harmonic voltages and currents are given in percentage of the fundamental. The system impedance at the point of connection is shown in the table again. It is found that the voltage distortion at order 7 decreases from 8.9% to 3.6% and others are all below 3%. The equivalent system impedance at order 7 is reduced from 17.2 Ω

to 6.9 Ω when the proposed SAPF is switched on.

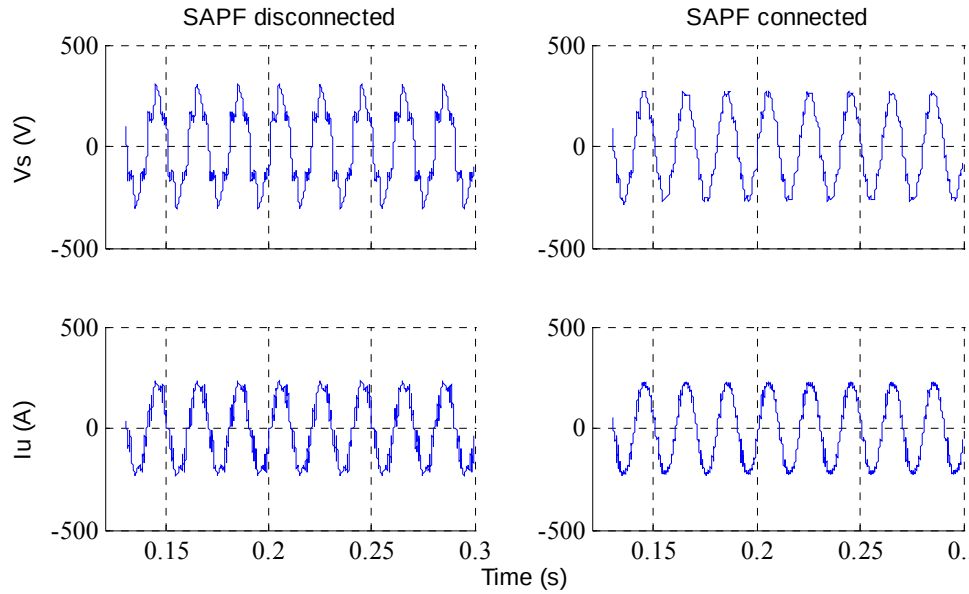

Figure 7.8 Damping of harmonic resonance by the proposed SAPF

Table 7.3 Simulated results in damping harmonic resonance

	Order	1	5 (%)	7 (%)	11 (%)	13 (%)	17 (%)	19 (%)
SAPF disconnected	Vs*	270V	19.3	8.93	5.30	2.07	2.22	1.52
	Iu*	220A	8.91	0.64	3.18	1.77	3.09	2.41
	Imp. (Ω)	1.2	2.7	**17.2**	2.0	1.4	0.9	0.8
SAPF connected	Vs	271V	2.55	3.58	2.99	2.07	0.74	0.89
	Iu	226A	1.24	0.22	1.77	1.90	1.11	1.19
	Imp. (Ω)	1.2	0.4	**6.9**	1.2	1.4	0.3	0.4

*: Vs is the phase voltage at the installation point, and Iu is the current in the upstream of the installation point

Figure 7.9 and Table 7.4 demonstrate the damping effect with the change of the control gains. The degree of resonance damping increases with the increasing control gain. Figure 7.10 shows the curves of system impedance against harmonic order under different values of the control gain. In this figure, the impedance of the 7^{th} harmonic is scaled down by a factor of 17.21 in order to show the trend of the impedance variation against harmonic order. These curves

show clearly the damping effect by the filter at order 7. With the proposed SAPF the harmonic impedance around the resonance frequency is reduced dramatically.

However, at order 17 and 19 harmonic distortion is slightly increased with the increase of the control gain. This increased harmonic distortion might be caused by upward shifting of the resonance frequency. Figure 7.10 clearly shows the local peak of system impedance is slightly moved upwards when the control gain is increased.

By comparing the equivalent harmonic impedance in Table 7.4 with those in Table 7.3, it can be seen that the filtering results shown in Table 7.3 are better than those in Table 7.4. All settings are similar in both configurations but the control gain is set to be different. In the case of Table 7.3, different values of the control gain at different orders are adopted while in those of Table 7.4 the same values are adopted for different harmonic orders. It is indicated that the multi-channel control-gain controller provides a great flexibility in damping harmonic resonance.

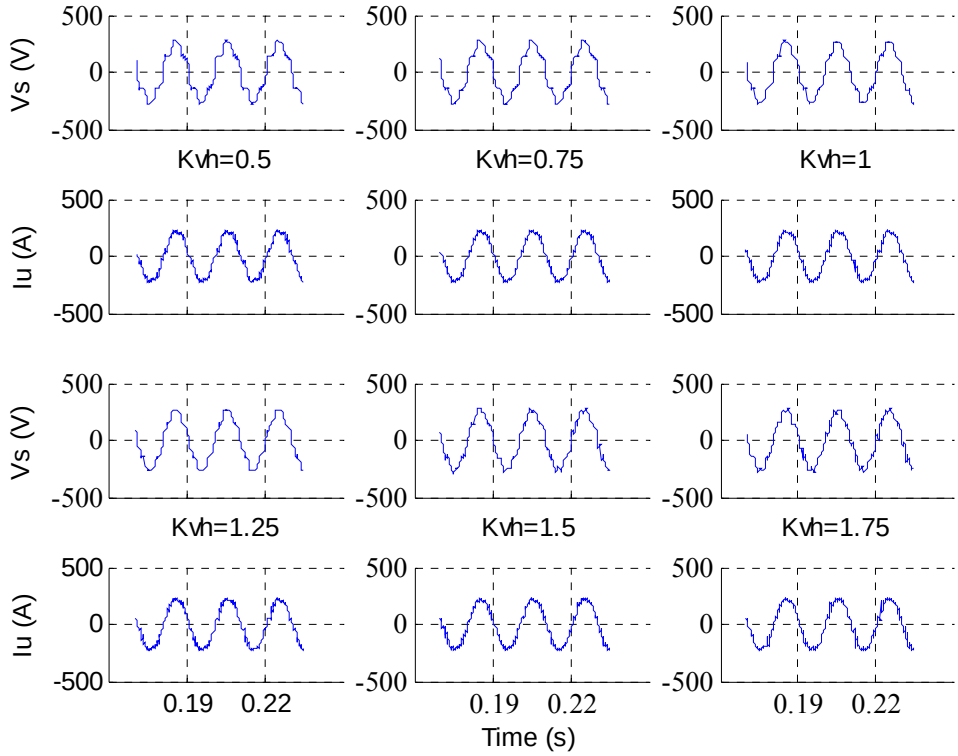

Figure 7.9 Damping effect of the proposed SAPF with Kvh at 0.5, 0.75, 1.0, 1.25, 1.5, and 1.75

Table 7.4 Results of the spectrum analysis of Case II with different control gains

	Order	1	5 (%)	7 (%)	11 (%)	13 (%)	17 (%)	19 (%)
Ref. (SAPF disconnected)	Vs	270V	19.2	8.93	5.37	2.19	2.19	1.44
	Iu	220A	9.00	0.64	3.36	1.95	3.00	2.27
	Imp. (Ω)	*1.23*	*2.62*	*17.21*	*1.96*	*1.37*	*0.89*	*0.78*
kvh=0.5	Vs	271V	16.2	9.52	4.91	**2.73**	0.30	0.63
	Iu	220A	7.64	0.68	3.14	**2.41**	0.41	1.05
	Imp. (Ω)	*1.23*	*2.22*	*18.43*	*1.80*	*1.72*	*0.12*	*0.34*
kvh=0.75	Vs	271V	14.1	8.01	4.28	**2.92**	**0.70**	**0.89**
	Iu	221A	6.65	0.54	2.58	**2.67**	**1.00**	**1.45**
	Imp. (Ω)	*1.23*	*1.93*	*15.50*	*1.57*	*1.84*	*0.29*	*0.48*
kvh=1.0	Vs	270V	9.93	7.26	3.85	**3.48**	**1.11**	**0.96**
	Iu	222A	4.77	0.50	2.30	**3.20**	**1.62**	**1.62**
	Imp. (Ω)	*1.23*	*1.35*	*14.00*	*1.41*	*2.19*	*0.45*	*0.52*
kvh=1.25	Vs	272V	7.43	6.21	3.31	**3.75**	**1.36**	0.81
	Iu	223A	3.50	0.45	2.06	**3.23**	**1.84**	1.30
	Imp. (Ω)	*1.24*	*1.02*	*12.07*	*1.22*	*2.37*	*0.56*	*0.44*
kvh=1.5	Vs	269V	5.54	5.72	3.16	**3.98**	**3.05**	0.74
	Iu	224A	2.50	0.40	1.92	**3.39**	**3.97**	1.25

	Imp. (Ω)	*1.22*	*0.75*	*11.00*	*1.15*	*2.49*	*1.24*	*0.40*
kvh=1.75	Vs	270V	1.44	3.00	2.41	**3.48**	**3.81**	**1.07**
	Iu	226A	0.66	0.22	1.86	**2.88**	**4.96**	**1.68**
	Imp. (Ω)	*1.23*	*0.20*	*5.79*	*0.88*	*2.19*	*1.56*	*0.58*

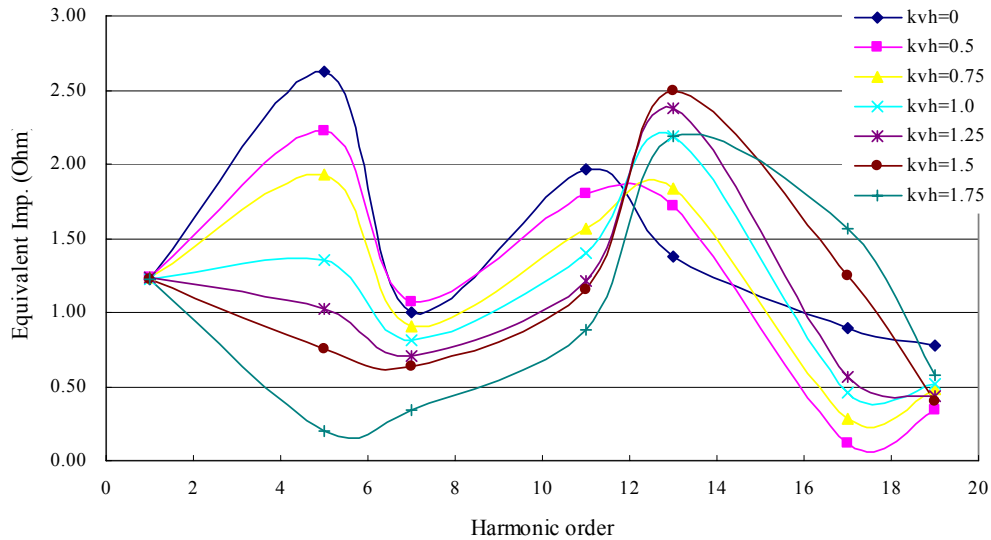

Figure 7.10 Upward shifting of resonance frequency

7.5 System Stability

7.5.1 Impact of the Digital Low Pass Filter on System Stability

The cutoff frequency of a digital low pass filter has a significant impact on the system stability. In this section, the configuration (II) with the capacitor bank installed at the end of the circuit is adopted for the investigation. Figure 7.11 shows the phase and DC voltages and the compensating current in an instable system. The control gain is at 8, and the cutoff frequency of the digital low pass filter is set at 10 Hz. It is seen from the figure that both the phase voltage and the compensating current oscillate and the DC-bus voltage is also

uncontrollable as the reference voltage is set at 600 V.

By increasing the cutoff frequency up to 3 Hz and retaining other settings in the SAPF the system turns stable, as shown in Figure 7.12. All the curves in Figure 7.12 indicate the SAPF functions well. It is noted that the magnitude of the compensating current takes a long to get stable. This is because that the step response time of the digital low pass filter increases when its cutoff frequency is reduced.

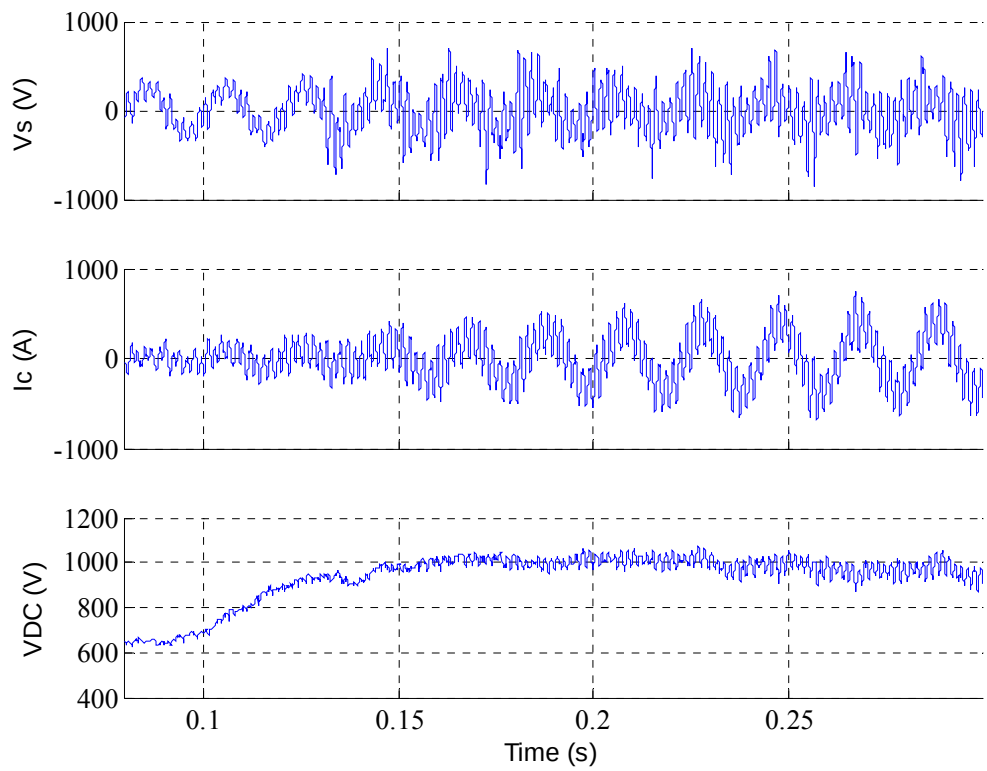

Figure 7.11 An unstable system with the cutoff frequency at 10 Hz

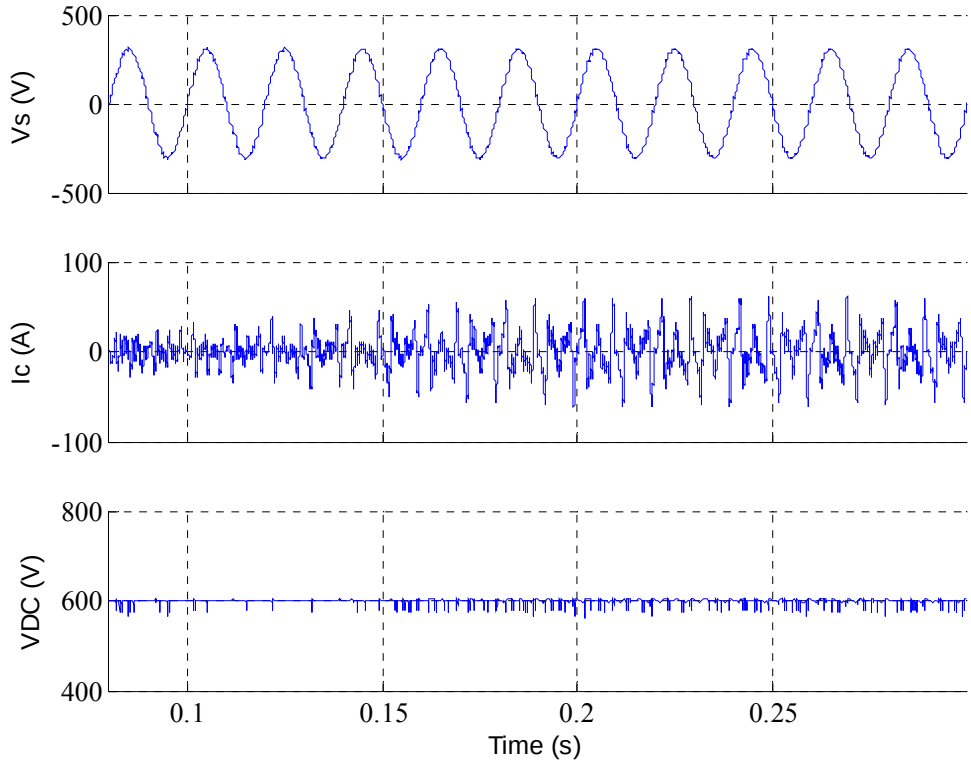

Figure 7.12 A stable system with the cutoff frequency at 3 Hz

7.5.2 Impact of the Angle of the Complex Control Gain on System Stability

In this section the impact of the phase angle of the control gain on system stability is studied. In order to clearly show the role of the phase angle, the control gain is set at 1 with zero angles for all channels, except one at order 19. The system configuration (I) is again selected for the investigation. Figure 7.13 shows the simulated results of the phase and DC-bus voltage as well as the compensating current when the control gain at order 19 set to be 35 and the control gain at other orders set at 1. All phase angles of the gain values are set to be zero in this case. It is clearly seen from the figure that the system is

unstable. Both the phase voltage and the compensating current oscillate and the DC-bus voltage is not stable either.

From the discussion in Chapter 6, it is known that the proportional control in the current regulator introduced a phase delay especially at high frequencies. It is well-known that the phase delay of a close loop may result in the decrease of the stability margins and even the instability. Therefore, it is necessary to compensate the phase delay in order to make the system stable. The phase delay at order 19 is 100°, which is obtained from the frequency response of the current regulator. With the leading compensation of 100° at order 19, the system turns stable, as shown in Figure 7.14.

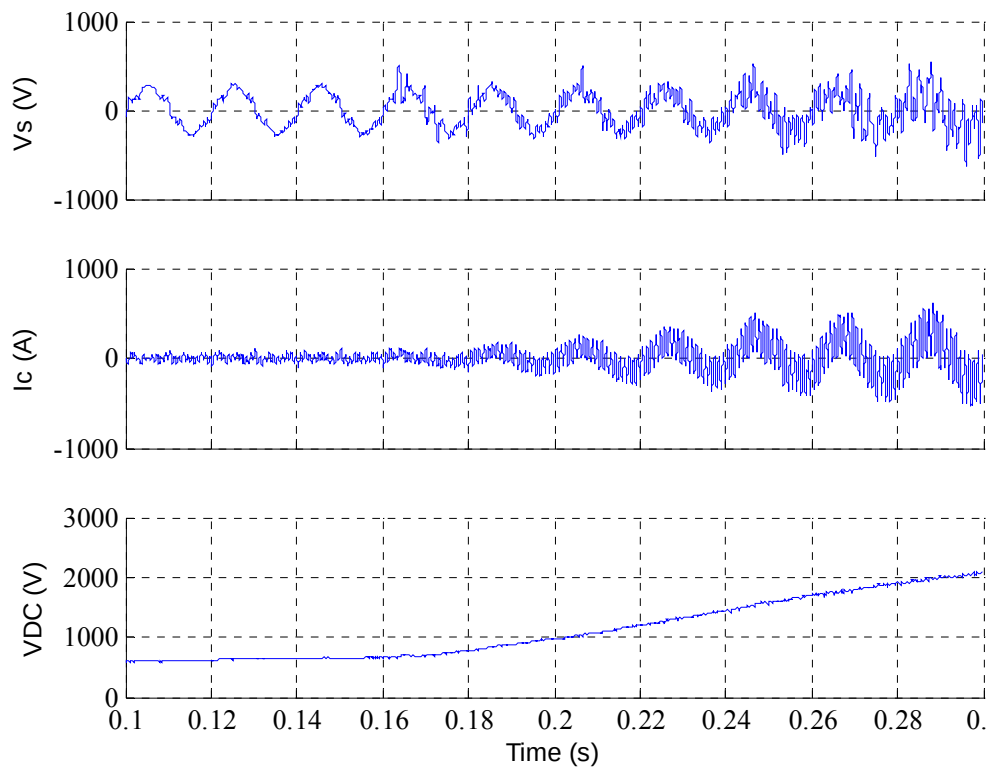

Figure 7.13 Results of an unstable system without leading compensation

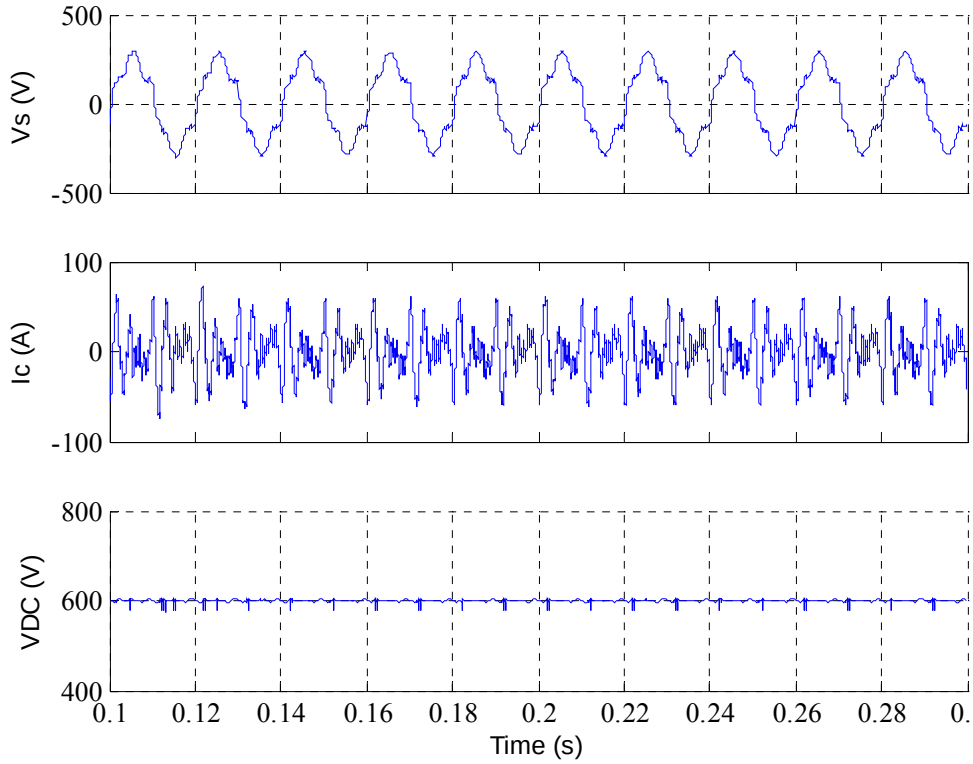

Figure 7.14 Results of a stable system with leading compensation

7.6 Application of the Proposed SAPF in the Building Distribution System

In this section, the proposed SAPF is applied in a typical building LV distribution system to control harmonics over the system. The simulation is conducted on the SINMULIK platform.

7.6.1 Description of the Distribution System

This is a typical building distribution found in Hong Kong. The utility provides the power supply at the transformer secondary side on the ground floor of the building. The short circuit capacity (SCC) at 11kV is approximately equal to

350MVA. Three three-phase distribution transformers are employed, which have the power rating of 1500kV and the impedance of 6% each. The ratio of the inductance to the resistance for these transformers is equal to 15. The short-circuit current at the secondary side of the transformer is equal to 38kA, which results in a short-circuit capacity of 25MVA. A figure of 25MVA is adopted here.

The electric power is transmitted to the final circuits through feeder or sub-main circuits connected to the main switchboard. There are three groups of sub-main circuits, which feed loads in low zone, middle zone and high zone of the building, respectively. In this case, one of sub-main circuits for the high zone is selected. The sub-main circuit is made by one 4-core armored XLPE-insulated cable with the size of 240mm^2 to BS 6346. The capacitor bank is installed at the main LV switchboard located on the ground floor. The harmonic sources in the building are distributed over the whole building. To demonstrate the worst cases, the linear loads in the building are disconnected. The information of the whole system is listed in Table 7.5. The floor height in the building is 4 meters and the number of floors is 36.

Table 7.5 The information of the studied building LV distribution system

Power source	11kV, 50Hz	No. of floors	36
11kV SCC	350MVA	Capacitor for PFC	250μF
Transformer	1500kVA, 11kV/380V, 6%	Linear loads	Disconnected
Riser imp.	Resistance: 0.66mOhms/floor	Harmonic loads	Multi-harmonic sources
	Inductance: 1.656μH/floor		

7.6.2 Harmonic Voltage Control on the Distribution Circuit

Digital simulation for the system configuration shown in Figure 7.15 is conducted on the platform of MATLAB/SIMULINK. In order to identify the ability of the proposed SAPF in harmonic voltage control over the circuit, multi-harmonic sources are considered in the simulation. Although it may be possible of the harmonic injection into the sub-main circuit on each floor, the source configuration is simplified by combining these sources and injecting the harmonic currents at three different locations, that is, on the 12^{th}, 24^{th}, and the 36^{th} floor, as shown in Figure 7.15. Subsequently, the sub-main circuit is represented by three sections in the simulation. Table 7.5 shows the parameters of the system shown in Figure 7.15.

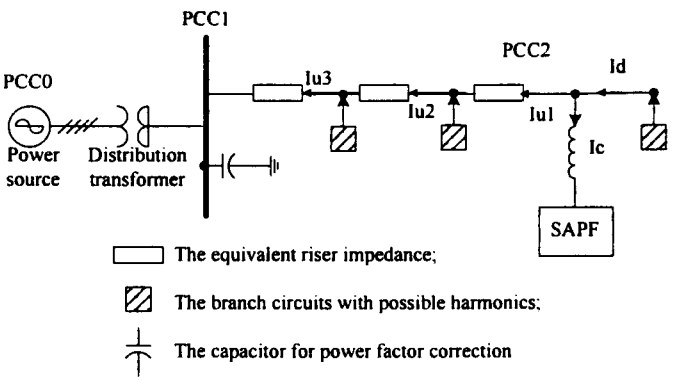

Figure 7.15 Configuration of a typical building distribution system

Table 7.6 provides both the phase voltage at the point of connection and the currents in three different sections of the sub-main circuit when the proposed SAPF is switched off. It is noted that the maximum harmonic voltage distortion

occurs at order 5 and reaches 4.2%. The total harmonic voltage distortion is up to 6.4%. As the harmonic currents from non-linear laods accumulate in the sub-main circuit, the harmonic current at the PCC1 reaches the maximum value at each order.

Table 7.6 Harmonic voltages and the currents with the SAPF being disconnected

Order	1	5	7	11	13	17	19
Vs (V)	305	**12.7**	**7.9**	**8.7**	**5.8**	**6.7**	**2.3**
Iu1 (A)	180	39.1	21.4	14.6	10.6	9.9	4.6
Iu2 (A)	361	80.0	39.4	29.1	17.6	16.6	6.2
Iu3 (A)	544	120.9	55.7	41.6	22.2	18.7	7.3

Table 7.7 shows the simulation results when the proposed SAPF with the control gain of 32 or 40 is switched on. No phase compensation is made in the simulation. Compared with the results without the proposed SAPF, the harmonic voltages in this case are significantly reduced. In general, the larger control gain results in better harmonic mitigation. The voltage harmonics at orders 17 and 19 slightly increase with the increasing control gain. This may because the difference of two control gains is not significant for higher harmonic orders as well as the small values of the currents of the 17^{th} and 19^{th} harmonics.

The proposed SAPF is capable of absorbing harmonic currents from the sub-main circuit. The harmonic currents originally flow towards the utility network. When the SAPF is switch on, part of these currents flow upwards and

is absorbed by the proposed SAPF. Subsequently, the harmonic voltage at the point of the connection is reduced. This phenomenon is proved by the results shown in Table 7.7. It is noted from the table that current harmonics $I_{u1,h}$ increase with increasing control gain while current harmonics $I_{u2,h}$ and $I_{u3,h}$ decrease. This absorbing effect becomes strong at lower harmonic orders. Figure 7.16 presents the corresponding waveforms of the voltages and currents. It is clearly seen that the harmonic currents in the different sections of the sub-main circuit are mitigated and the voltage distortion is reduced.

Table 7.7 Harmonic voltages and the currents with the SAPF being connected

Order	1	5	7	11	13	17	19
kvh	32	32	32	32	32	32	32
Vs (V)	305	**2.9**	**3.0**	**3.8**	**1.3**	**2.8**	**1.1**
Iu1 (A)	284	29.1	18.6	9.9	8.7	2.9	3.6
Iu2 (A)	463	12.4	17.8	9.5	4.9	4.9	2.3
Iu3 (A)	647	54.2	28.3	25.5	8.8	12.5	4.9
kvh	40	40	40	40	40	40	40
Vs (V)	305	**2.1**	**2.0**	**3.5**	**1.2**	**3.1**	**1.4**
Iu1 (A)	317	33.6	20.2	9.8	8.7	3.3	3.5
Iu2 (A)	496	7.7	16.1	8.9	4.5	4.6	2.4
Iu3 (A)	679	49.9	25.1	24.9	8.5	12.5	4.9

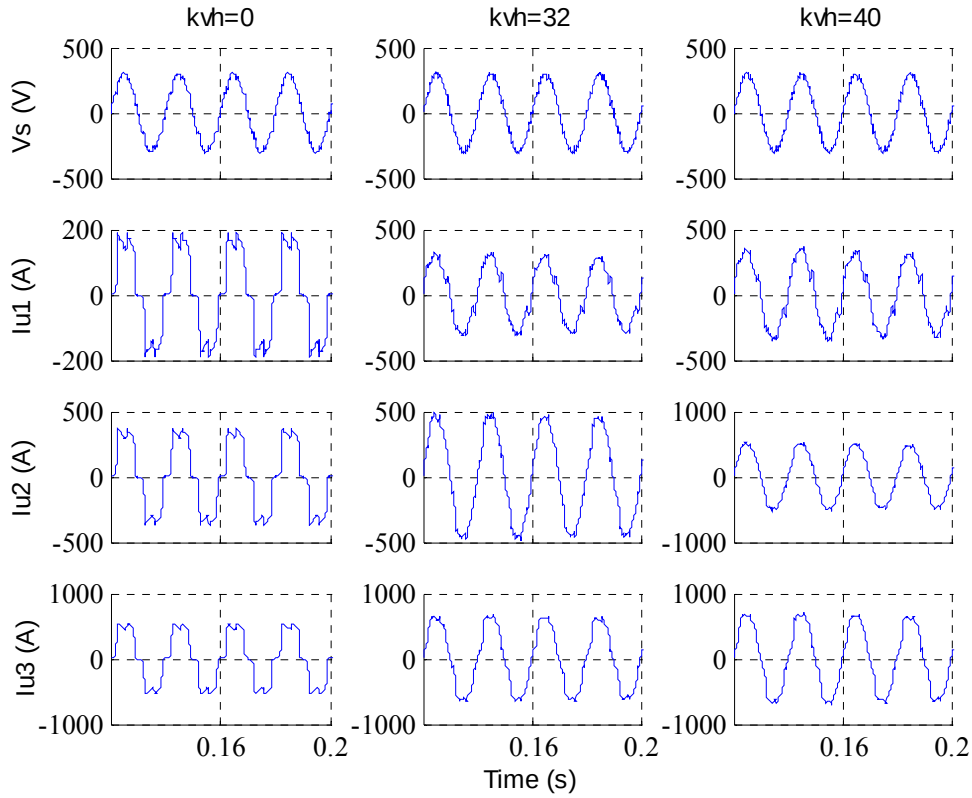

Figure 7.16 Harmonic mitigation by the proposed SAPF in a distribution system

7.7 Summary

This chapter investigated the characteristics and the performance of the proposed SAPF by performing computer simulations. The system modeling and computer simulation were conducted on the platform of MATLAB/SIMULINK. The simulation validated the control method of the proposed SAPF.

With the developed simulation models in the SIMULINK, the characteristics of the proposed SAPF were investigated, including DC-bus charging, the transient response and tracking of the reference currents. The results indicated that the proposed control strategy resulted in good performance of the system. The

application of the proposed SAPF in a typical building distribution system showed the potential capability of the SAPF in harmonic voltage control in buildings. The impact of the low pass filter and the phase angle of the control gain on system stability were investigated as well using the simulation. It was shown that a small cutoff frequency of the low pass filter and an appropriate phase angle of the control gain can increase the stability margins of the SAPF connected to a building distribution system.

Chapter 8

Implementation of the Proposed SAPF

8.1 Introduction

A prototype of the proposed SAPF was developed in the laboratory. This prototype was tested on a laboratory testing system, which includes a line simulator representing a building distribution circuit. In this chapter, both hardware and software of the prototype are described. The testing results of the prototype in the laboratory testing system are presented. The characteristics and the performance of the proposed SAPF are demonstrated, and the control strategy of the proposed SAPF and the capability of harmonic control in the system are validated.

8.2 Hardware Implementation of the Proposed SAPF

The hardware of the prototype was implemented in the laboratory in order to test the proposed control strategy as well as the filtering performance. It includes the main circuit, the signal conditioning circuit, the control chip, the drive of switching pulses and the switching ripple filter. These hardware parts are described in the following sections

8.2.1 Main Circuit

The main circuit of the proposed SAPF consists of three major parts, that is, two DC capacitors, a DC bus loop and a three-phase four-pole voltage-fed inverter, as shown in Figure A.8.1.

The capacitors are applied on the DC bus to maintain a stable DC voltage on the DC bus loop. Two series-connected capacitors rating at 4700μF, surge 450VDC are adopted in the prototype of the proposed SAPF. The equivalent capacitor has the capacitance of 2350μF and the voltage rating of 900VDC. In order to minimize the parasitic inductance of the DC bus loop, the DC bus is made by using two paralleled aluminum plates, instead of the cables. These two plates, serving as the positive pole and the negative pose of the DC bus, are insulated with a thin insulating level.

The voltage-fed inverter was made by IGBTs, which serve as the switching devices in the main circuit. An IGBT is a device with MOS input (voltage controlled or voltage drive), which greatly decreases the loss of the switching and reduces the risk of coupling or interference compared with the current-drive device. It is usually adopted in the application with the switching frequency below 20 kHz. This device is suitably used as a witching device in an active power filter as harmonics at order of less than 25 are usually of concern in

electrical systems. IGBTs are capable of carrying large current, compared with other similar devices. Some products can reach more than one thousand ampere current rating. In the application of harmonic mitigation in a LV distribution system, IGBTs with a few hundred ampere rating are considered adequate. In this prototype, the module of SKM200GB123D, a product by SEMIKRON, was adopted. This module consists of two series-connected IGBTs with fast and soft inverse-connected diodes in parallel. The rated current of the module is 200A and the collector-emitter breakdown voltage (V_{ces}) is at 1200V. Four modules are used to form a three-phase four-pole circuit and are mounted on a heat sink.

During active turn-off of an IGBT module as well as during reverse-recovery of paralleled diodes, switching over-voltages are generated in the module due to high di/dt caused by the commutation inductances. This will increase turn-off power dissipation and voltage stress of the power semiconductors. This effect is especially critical with regards to short-circuits and overload.

In addition, together with parasitic capacitances unwanted high frequency oscillations may be generated on the IGBT module. Therefore, it is of major importance to minimize the total inductance in the commutation circuit of hard-switching devices. The tight bus structure reduces the bus inductance down to 20-50nH. While the snubber circuit, which can be a capacitor- (C-), resistor-capacitor- (RC) or resistor-capacitor-diode- (RCD-) circuit, reduces the

inductance of an IGBT module. In most cases, a simple C-circuit with non-inductive capacitors of 0.1-2 μF is sufficient. In the prototype one capacitor of 1μF was applied each of four IGBT modules. This measure reduces the equivalent inductance of the main circuit and improves the transient condition during switching-off operation, which may effectively reduce the switching-off surge voltage.

8.2.2 Signal Conditioning

The proposed SAPF needs dynamic system information in order to generate updated compensating currents into the system. Such information includes the phase voltages, the DC-bus voltage and the compensating currents, which are measured by potential transformers (PTs), current transformers (CTs) and a hall-effect DC-voltage sensor in the prototype.

A signal conditioning circuit was designed to condition these detected voltages and currents into the desired signals, which can be processed in the control system. Firstly these voltages and currents are converted to electrical signals, and scaled down into a range of 0 - 2.5 V with an offset of 1.25V. The voltage signals are then converted into digital signals by using an analogue-to-digital converter (AD) of the module ADS8364, a product from Taxes Instruments (TI).

In a data-sampling system, frequency components greater than half of the sampling rate "alias" (shift) into the frequency band of interest. In most of the time aliasing effect results in an undesirable side effect. So the under-sampled higher frequencies are filtered out before the AD stage. But sometimes, the under-sampling is deliberate and the aliasing causes the A/D system to function as a mixer. An anti-aliasing filter is required. Its goal is to provide a cutoff frequency that removes unwanted signals from the AD input or at least attenuates them to the point that they will not adversely affect the circuit. It is a low-pass filter. In the prototype, an anti-aliasing filter with the cutoff frequency of 5 kHz was adopted.

8.2.3 DSP-Based Control System

DSP (digital signal processor) is the highly integrated, high-performance solution for demanding control applications. TMS320F2812, a powerful product from TI, was selected as the platform for the implementation of control strategies adopted in the proposed SAPF. The detailed features of TMS320F2812 are listed in Table 8.1. The high speed of this chip makes it possible to accomplish more algorithms within one limited period. This also may increase the maximum switching frequency of the designed system. EVA (event manager A) and EVB (event manager B) provide hardware resources for

the designer to easily arrange more functions such as the realization of PWM, interrupt etc.. The internal AD makes the data acquisition more convenient. This 12-bit AD was used to process DC-bus voltage. As the harmonic components of phase voltages are relatively small compared with those of the load currents, a 16-bit high-precision ADC (ADS8364) was adopted to process signals of the phase voltages and compensating currents.

Table 8.1 The main features of TMS320F2812

FEATURE	**F2812**
Instruction Cycle (at 150 MHz)	6.67 ns
Single-Access RAM (SARAM) (16-bit word)	18K
3.3-V On-Chip Flash (16-bit word)	128K
Code Security for On-Chip Flash/SARAM/OTP/ROM	Yes
Boot ROM	Yes
OTP ROM (1K x 16)	Yes
External Memory Interface	Yes
Event Managers A and B (EVA and EVB)	EVA, EVB
General-Purpose (GP) Timers	4
Compare (CMP)/PWM	16
Capture (CAP)/QEP Channels	6/2
Watchdog Timer	Yes
12-Bit AD	Yes
Channels	16
32-Bit CPU Timers	3
SPI	Yes
SCIA, SCIB	SCIA, SCIB
CAN	Yes
McBSP	Yes
Digital I/O Pins (Shared)	56
External Interrupts	3
Packaging	179-ball GHH and ZHH 176-pin PGF

ADS8364 is, also a product from TI company, includes six, 16-bit, 250 kHz

ADs (Analog to Digital converters) with 6 fully differential input channels grouped into two pairs for high-speed simultaneous signal acquisition. Inputs to the sample-and-hold amplifiers are fully differential and are maintained differential to the input of the AD. This provides excellent common-mode rejection of 80dB at 50 kHz that is important in high-noise environments. The ADS8364 offers a flexible high-speed parallel interface with a direct address mode, a cycle, and a FIFO mode. The output data for each channel is available as a 16-bit word.

ADS8364 is an external AD to TMS320F2812. To ensure reliable data transfer between these two chips, synchronous communication was adopted using the CMP output of Timer 2 in EVA of TMS320F2812. This output provides an external clock to ADS8364 to control the conversion rate inside. The PWM2 output in EVA of TMS320F2812 is connected to the three hold signals which initiate the conversion on the specific channels. A simultaneous hold on all six channels can occur with all three hold signals strobe together. The Address/Mode signals which select how the data is read from the ADS8364 are connected to the least three bits of the XINTF address bus of TMS320F2812.

For synchronization in the proposed SAPF the phase information of supply voltage is required in the control algorithm of the SAPF system. The method based on zero-crossing detection is used to provide the phase information. In the

hardware implementation, a comparator LM339 was used to detect the zero crossing. A high-speed s logic gate optocoupler was adopted to generate the phase information to the DSP.

8.2.4 Driver of Switching Pulse for IGBTs

The intelligent double IGBT driver SKHI 23/12, a product of SEMIKRON, is a standard driver for all power IGBTs in the market. It drives both IGBTs with V_{ce} up to 1200 V. The high power outputs capability was designed to switch high current double, single modules or paralleled IGBTs. The output buffers have been improved to make it possible to switch up to 200 A IGBT modules at frequencies up to 20 kHz.

A new function has been added to the short circuit protection circuitry, this automatically increases the IGBT turn-off time and hence reduces the DC voltage overshoot enabling the use of higher DC-bus voltages. Also, the possible adjustment of the gate condition makes it possible to reduce the losses during the switching-on operation.

A high-frequency DC/DC converter avoids the requirement of external isolated power supplies to obtain the necessary gate voltage. It ensures that the user is protected from the high voltage in the secondary side. An isolated ferrite

transformer in half-bridge configuration supplies the necessary power to the gate of the IGBT.

An interlock circuit prevents the two IGBTs of the half bridge to switch-on at the same time, and a dead-time can be preset by adjusting additional resistors. The available dead-time may be from 0.9 μs up to 10 μs. The setting of dead-time by the hardware circuit makes the switching of IGBTs on the half bridge more reliable. In the application, the dead-time is preset at 2.5 μs.

Short circuit protection is provided by measuring the collector-emitter voltage with a V_{ce} monitoring circuit. An additional circuit detects the short circuit after a delay of the IGBT, which can be adjusted in the hardware. Soft turn-off under fault conditions is necessary as it reduces the voltage overshoot and allows for a faster turn off during normal operation. In the application of the three-phase four-pole active power filter, the detections of all the IGBTs can be “wired-or”.

8.2.5 Switching Ripple Filter

The output voltages generated by switching operation of IGBTs contain significant noises at or above the switching frequency. These noises are the major source of EMI to the control system. Generally, a switching ripple filter should be installed at the output of the active power filter. The objective is to

prevent switching frequency currents flowing into the building distribution systems. Also, the filter can provide attenuation for other higher harmonic currents in the system.

A broad-band passive filter was designed to fulfill the function of the switching ripple filter. The topology is shown as in Figure 8.1. As indicated in the topology, this switching ripple filter provides two separate paths, one is for the switching frequency currents from the main circuit and the other is for broad-band damping of higher frequencies currents. The branch Lr-Cr-Rr is tuned at the switching frequency to sink dominant switching frequency ripple currents from main circuit. The path Rb-Cb provides broad-band damping to higher frequencies currents that is slightly lower than switching frequency. Also, Rb can damp out the possible resonances in the system.

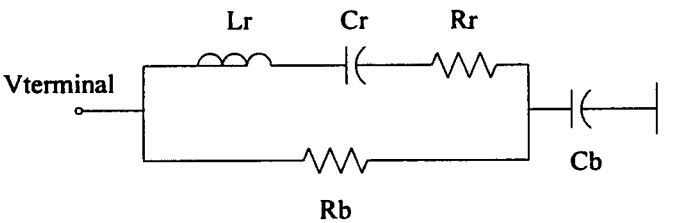

Figure 8.1 Topology of a switching ripple filter

The selection of the filter parameters are based on two principles, one is to ensure the two paths of the switching ripple filter working independently and the other is to limit the fundamental frequency current flowing through the filter. The first one is achieved by setting proper values of two capacitors. It is noted

that if Cb>>Cr, Cb does not change the filtering characteristics of Lr-Cr-Rr branch. Consequently, the switching ripple frequency current flows through Lr-Cr-Rr branch and other components mainly flow through Rb-Cb branch. The second principle is achieved by selecting proper Cb and Rb. Cb is the main parameter determining the fundamental frequency current. This current in the real application is limited by the power rating of the resistor Rb. The tradeoff is increased losses and rating of Rb. In order to achieve good performance, non-inductive resistor is preferred. At higher frequencies, the resistor Rb determines equivalent impedance of the branch which affects the switching ripple filtering branch. Therefore, a careful calculation of these values should be done.

In the prototype, the system is rated 220 V, and the switching frequency of the IGBTs is equal to 10 kHz. The designed values of the switching ripple filter are presented in Table 8.2. Rr is the equivalent series resistor (ESR) of the inductance Lr, generally around several mohms. Figure 8.2 shows the frequency response of the switching ripple filter. A laboratory setup is presented in Figure A.8.2.

Table 8.2 Design values of the switching ripple filter

Lr	115 μH	Rb	0.9
Cr	2.2 μF	Cb	30 μF
Rr	ESR		

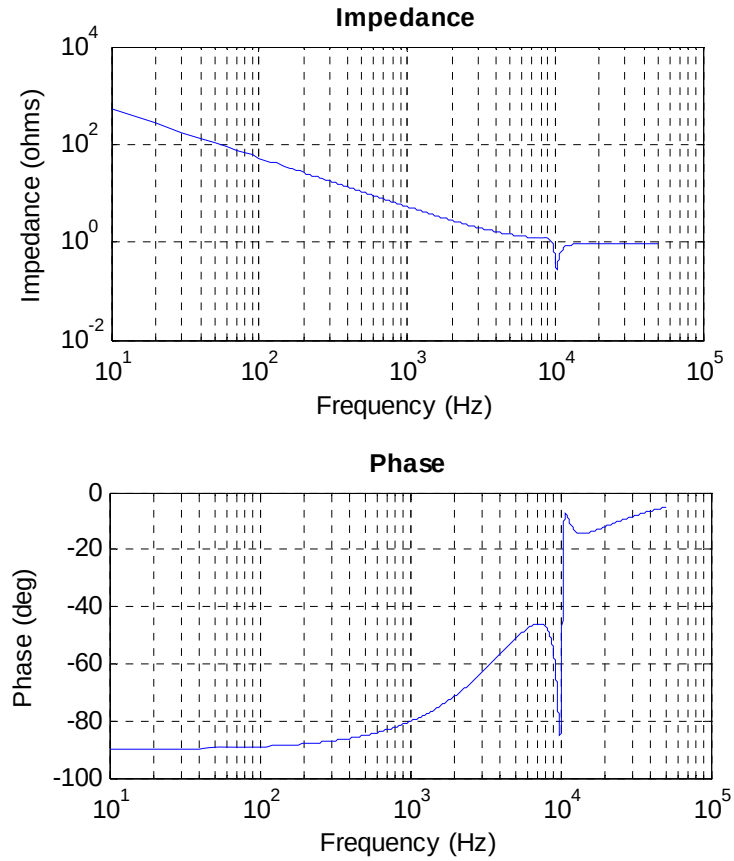

Figure 8.2 Frequency response of the switching ripple filter

8.3 Software Implementation of the Proposed SAPF

8.3.1 Timing Schedule, Program Flow and Numeric System

Shown in Figure 8.3 is the timing schedule of the control system adopted in the prototype. Figure 8.3 (a) shows the timing schedule in one period of 50 Hz. Time counting is used to record the phase information referred to system voltage in phase A. One of four timers in TMS320F2812 is set with the clock rate of 2.5MHz. As long as the zero-crossing point in a fundamental cycle is detected in the DSP, the phase counter is reset with zero then starting counting.

With the 10 kHz switching frequency, there are two hundred switching periods in each period of 50 Hz.

Figure 8.3 (b) presents the timing schedule during each switching period. At the beginning of each switching period, required signals are sampled. At the meanwhile, the switching pulses for IGBTs, which are computed at last switching period, are sent to the drives. The switching pulses computed at current switching period are sent at the beginning of next switching period, which is re-executed by each period. It is noted that the beginning of sampling which contains the hardware operation of ADs and data transmission is same as the start of the switching period. These result in no additional time for the sampling and ensure the switching frequency at 10 kHz. Although there exists one switching period of time delay, this can be compensated in the software.

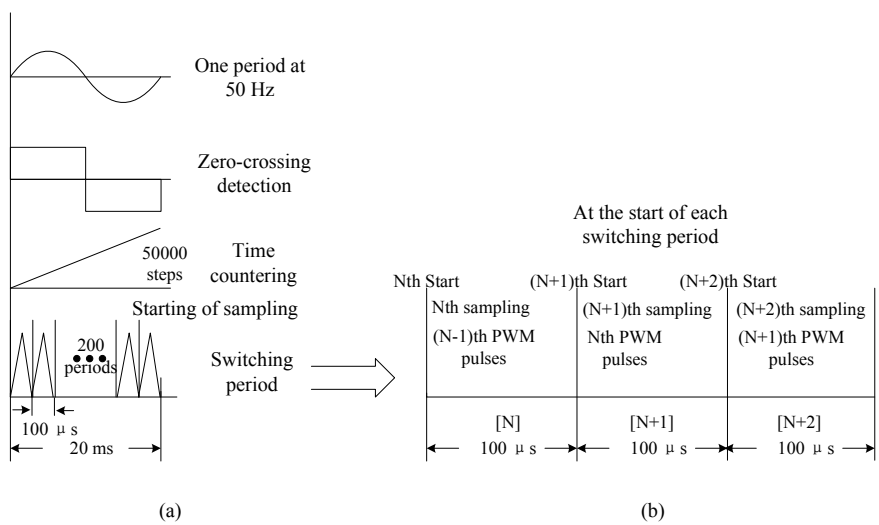

Figure 8.3 Timing schedule of the controller with
(a) 50 Hz period timing schedule, (b) 10 kHz switching period timing schedule

Figure 8.4 illustrates the flowchart of the program used in the prototype. The

whole program is divided into two parts, one for system initiation and the other for computation in one switching period. The system initiation includes initializing the setting of basic system environment, the setting of some required resources such as internal AD, EVA, EVB and interrupt service etc.. After detecting the first positive slope of the phase voltage which means the system is powered on, the program enters the computation of the control algorithm. It includes the data acquisition, the numeric transformation, the harmonic extraction, the multi-channel complex gain control, the current regulation and the computation of the driving pulses. A waiting module as well as the interruption of Time 3 underflow is adopted to ensure the switching period of 100 μs. All the algorithms are coded on per unit (pu) quantities. This may make it easy to set up the numeric system in the program.

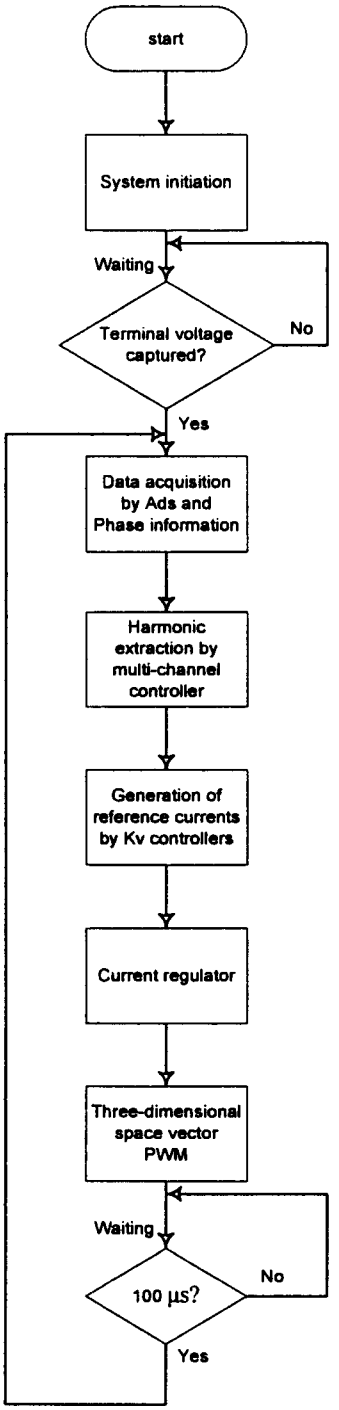

Figure 8.4 Flowchart of the control program

8.3.2 Digital Low-pass Filter

A digital low pass filter (LPF) was designed to extract harmonic components in the controller. When the signals are passed to the LPF, the output signals will

have no distortion in magnitude and phase at DC, but have attenuation at other frequencies. The Butterworth digital low pass filter is used in the control controller as it provides the maximum flatness within the pass-band. In this prototype, the assembly language is used to realize the function of a two-order Butterworth digital low pass filter. This is for the consideration of reducing computation time as this LPF function is frequently called in each switching period in the control algorithm. The coefficients of this digital filter are listed in the Table 8.3.

Table 8.3 The coefficients of a two-order digital low pass filter

a0	-1.9911142922016536	b0=b2	0.000009825916820482 0344
a1	0.99115359586893537	b1	0.000019651833640964 0688
y(n) = b2*x(n-2)+b1*x(n-1)+b0*x(n)-a1*y(n-2)-a0*y(n-1)			

Shown in Figure 8.5 is the frequency response of the selected digital low pass filter. For the digital filter with the cutoff frequency of 10 Hz, the attenuation in magnitude reaches more than 96% at 50 Hz. In the proposed controller, the signals applied to the digital filter are in the synchronous reference frame. The fundamental signals are transformed to those at 100 Hz in the 3rd order synchronous reference frame, or more in other-order synchronous reference frames. Hence, the attenuation is enough to attenuate the fundamental component which is normally dominant in the signals. In addition, the gain at DC frequency is perfectly 1. This means the harmonic components of concern can be extracted in the corresponding channels.

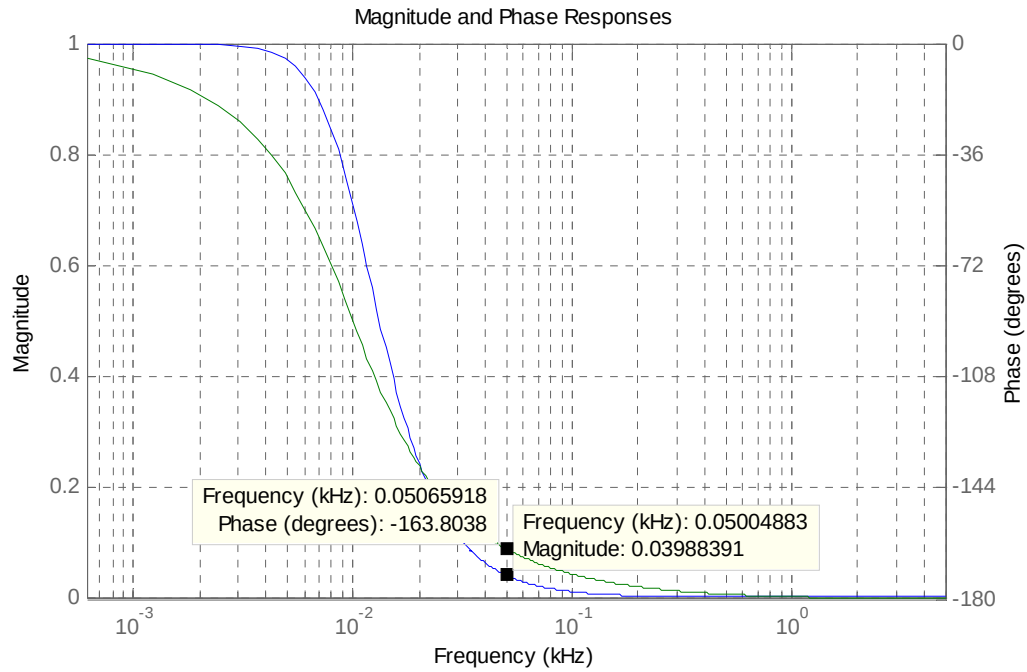

Figure 8.5 Frequency response of a digital low pass filter

Shown in Figure 8.6 is the step response of the selected digital low pass filter. Tit is noted that the rising time is about 0.06 second, and the signal remains stable after 0.1 second. The rising time is inversely proportional to the cutoff frequency. Therefore, if harmonic currents or voltages in the system change significantly and frequently, the cutoff frequency may be set at a large value.

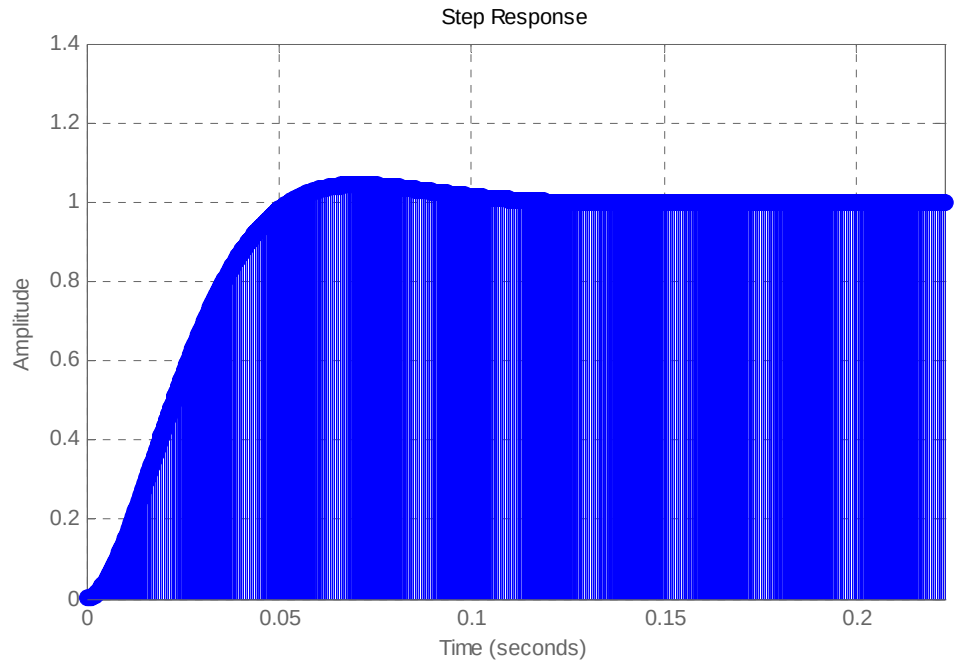

Figure 8.6 Step response of the digital low pass filter

8.4 Setup of the Laboratory Testing System

The laboratory testing system was developed for testing the performance of the proposed SAPF. It includes a line simulator simulating the building distribution system, a three-phase rectifier simulating the non-linear loads, and the prototype of the proposed SAPF.

System components such as the distribution transformer, the sub-main cable and the capacitor bank are represented by inductors, resistors and capacitors. The inductors were constructed by using the laminated silicon steel core wired by the enamel conductors. Pieces of silicon steel were assembled to form a U-shaped part. Each inductor is made of two U-shaped parts forming a

close-loop magnetic path. An adjustable air gap is introduced in the close loop to avoid saturation of the inductor when it carries out a large current. The thickness of the air gap was adjusted to obtain the desired inductance. Capacitors with the value of 35 μF were installed to represent the capacitor bank for the power factor correction. These capacitors are also employed to create harmonic resonance tuned at 280 Hz in order to test the damping performance of the proposed SAPF. The three-phase rectifier with resistive loads was employed as the harmonic source.

The objective of this experiment is to validate the control strategy of the proposed SAPF. Two cases presented in Chapter 7 for computer simulation are selected to demonstrate the performance of the proposed SAPF. The configuration of the cases is shown in Figure 8.7. The configuration shown in Figure 8.7 (a) is the distribution system without the capacitor bank. It is used to test the performance of the proposed filter on harmonic mitigation. The configuration shown in Figure 8.7 (b) represents the distribution system with the harmonic resonance being present. It is used to test the damping effect of the proposed SAPF in the distribution system. The parameters of the laboratory testing system are listed in Table 8.4.

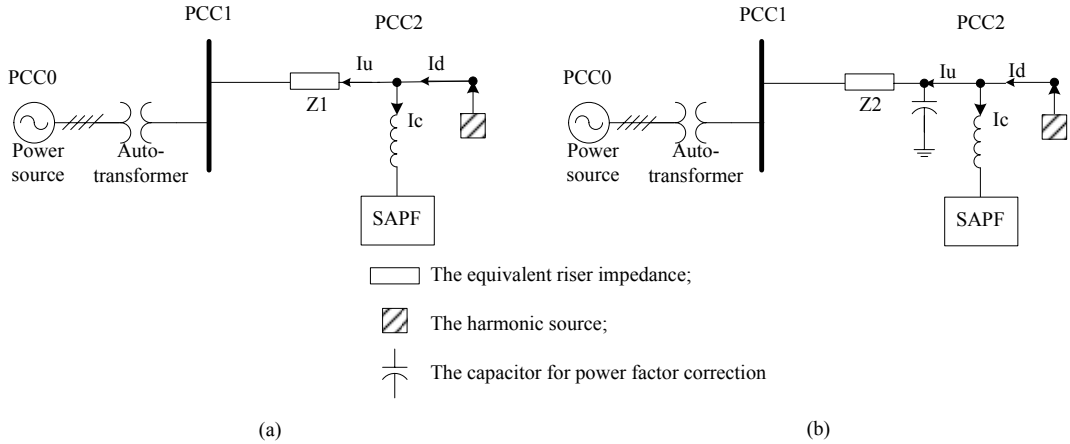

Figure 8.7 Configuration of two cases for laboratory testing of the proposed SAPF

Table 8.4 Parameters of the laboratory testing system

The electrical system:			The proposed SAPF:	
Power source (phase)		220V, 50Hz	Switching frequency	10kHz
Auto-transformer		380/380V, 20kVA	DC-bus capacitor	2350μF
The riser impedance	Z1	5.24mH	Output smoothing inductance	1mH
	Z2	9.12mH	Configuration	3-phase, 4-wire
Capacitor for PFC		35μF	DC-bus voltage setting	600V
Harmonic source		3-phase rectifier		

8.5 Results of the Experiment

The laboratory experiment was conducted based on the laboratory testing system. The proposed SAPF is set up as shown in Figure A.8.3. Both the characteristics of the proposed SAPF and the performance on harmonic mitigation are tested. The results are presented as follows.

8.5.1 DC-bus Voltage

Figure 8.8 shows the waveform of both the charging current (top curve) and the

DC-bus voltage (bottom curve) in DC capacitor changing. In the experiment, a resistor was in series with the input circuit of the prototype in order to reduce the current when switching on the SAPF. In fact, for the SAPF itself, this is same as the situation with reduced voltage starting. It is seen from the figure that the DC-bus voltage increases gradually and the charging current is moderate. The charging current is reduced to a low level when the DC-bus voltage tends to be stable. Figure 8.9 shows a portion of the DC-bus voltage when it is stable. The reference DC voltage is set at 600V.

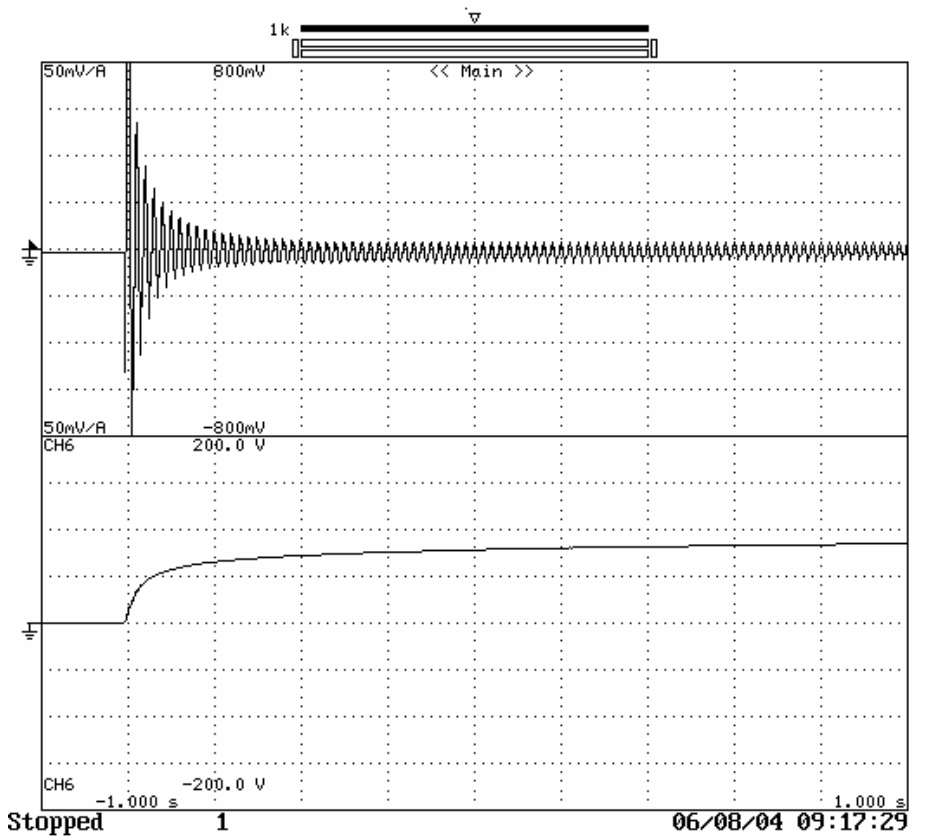

Figure 8.8 Input current (the upper curve) and the DC voltage (the lower curve) when charging the DC bus capacitors

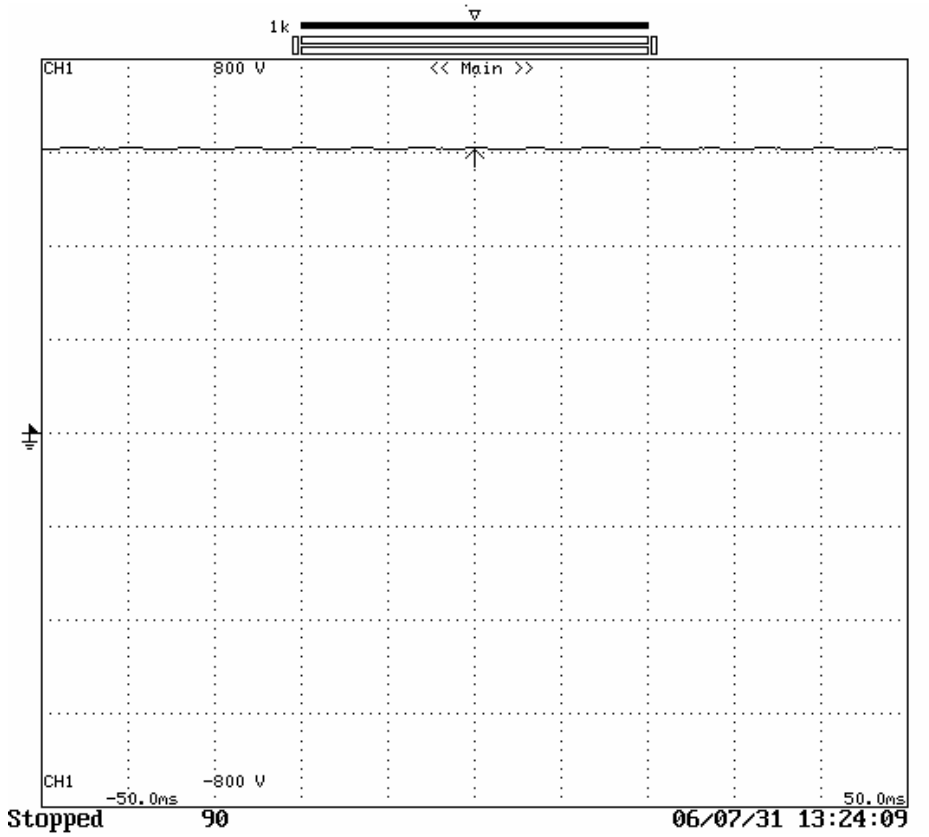

Figure 8.9 Steady-state DC-bus voltage

8.5.2 Compensating Current

Figure 8.10 presents the compensating current coming from the prototype in the experiment with the configuration shown in Figure 8.7 (a). It can be seen that there are some high-frequency noises in the curve. This mainly results from the switching operation of the IGBT modules. These high-frequency noises may be filtered out by using the switching ripple filter.

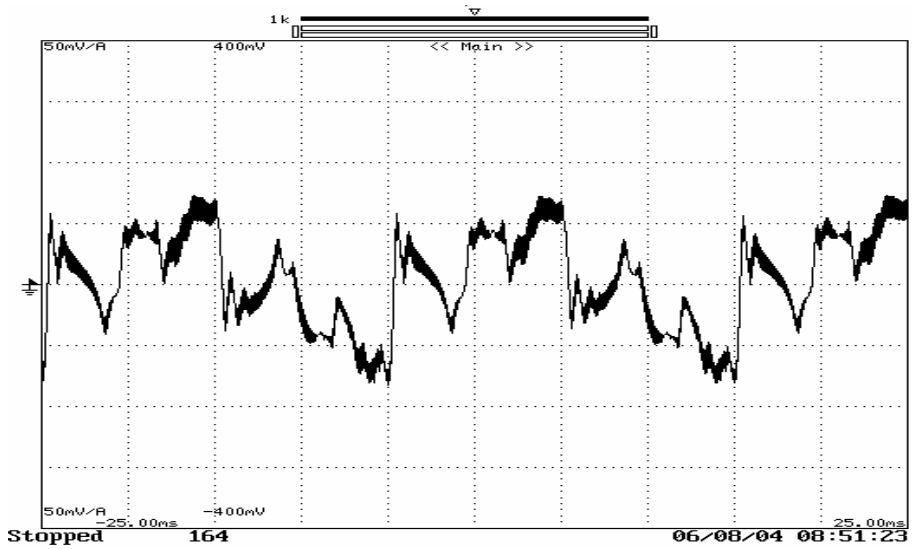

Figure 8.10 Compensating current from the prototype

8.5.3 Transient Response

Figure 8.11 shows the transient response of the prototype in the experiment when another harmonic-producing load is switched on. The phase voltage at the point of connection, the compensating current and the DC-bus voltage are presented in the figure. The harmonic-producing load is switched-on at the 3rd fundamental period. The phase voltage is distorted in the following period, and is recovered within two-three fundamental periods. This was because the compensating current is in the adjustment according to the transient conditions. Also, the compensating current has a response time of two and half periods. The DC-bus voltage was basically stable. There may be a little ripple in the DC voltage curve.

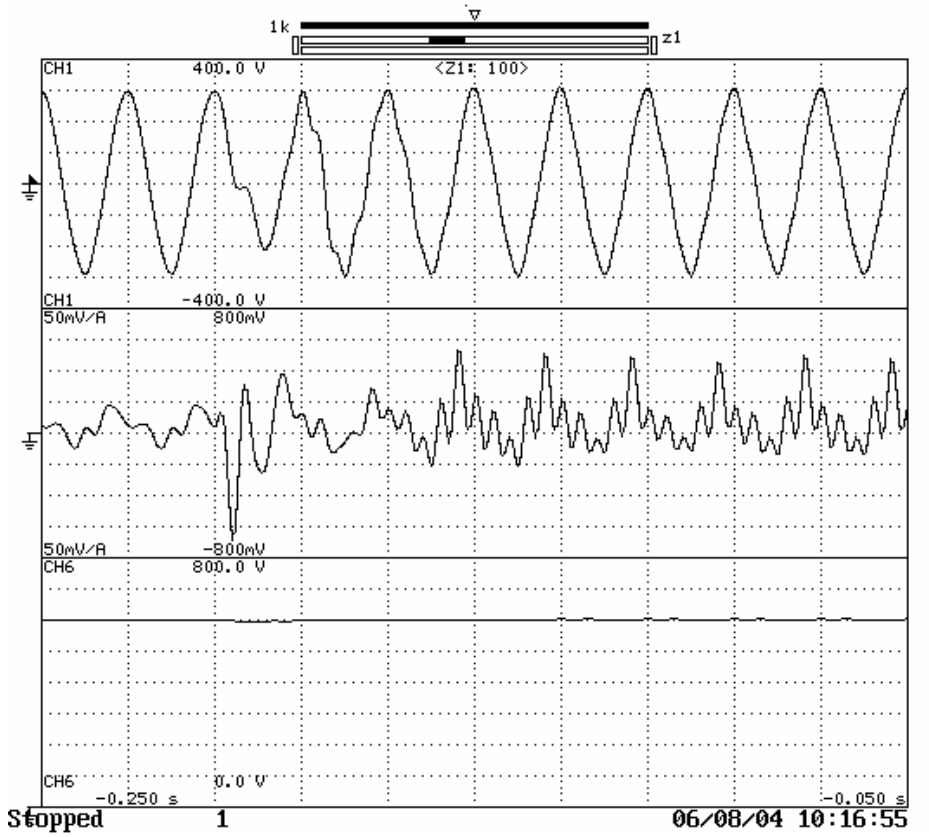

Figure 8.11 Transient response of the proposed SAPF
top curve: the phase voltage at the installation point
middle curve: the compensating current from the SAPF
bottom curve: the DC-bus voltage

8.5.4 Harmonic Mitigation by the Proposed SAPF

The laboratory experiment is conducted to test mitigation performance on the system with the configuration given in Figure 8.7 (a). In the experiment the control gain was adjusted in order to validate the effect of the control gain on the harmonic mitigation. The control gain kvh varied from 0 – 6 wit ha step of 2. When the control gain is equal to 0 it simply means the SAPF is switched off. The phase voltage at the point of connection is presented in Figures 8.12-8.15 for different values of the control gain,. It can be seen that the voltage distortion is reduced after the SAPF is switched on. The total harmonic voltage distortion

is 12.8% for Kvh=0, 8.53% for Kvh=2, 6.1% for Kvh=4 and 3.4% for Kvh=6. The corresponding spectrum under different gain values are listed in Table 8.5. It is indicated from the table that harmonic mitigation at the lower orders is better than that at the higher orders. This may because the contents at the higher orders are too low so that the mitigation effect is not significant. The histogram is presented in Figure 8.16 using the percentage of the fundamental voltage. When the control gain has the value of 6, the harmonic voltage distortion at each order is below 2%. These results show that the proposed SAPF has the capability of mitigating harmonics in the distribution system.

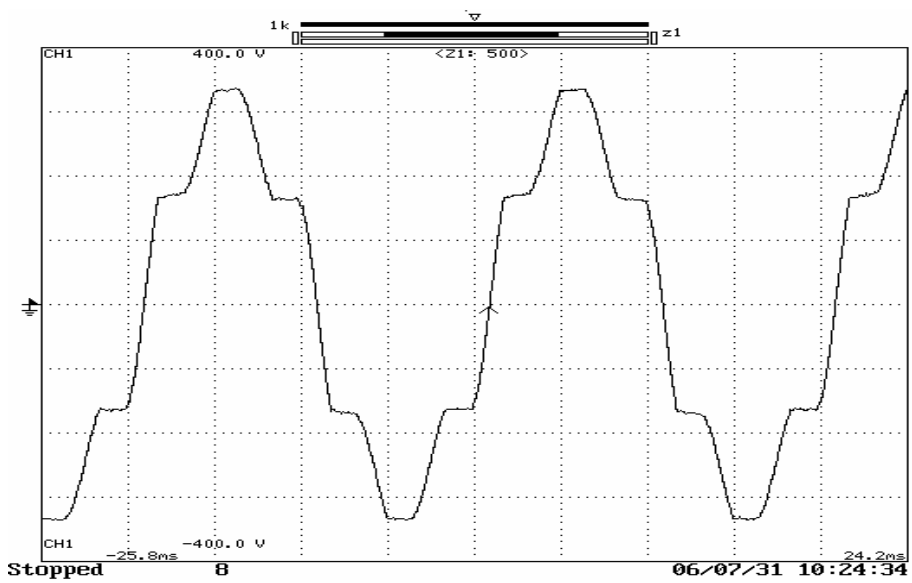

Figure 8.12 Phase voltage with kvh=0

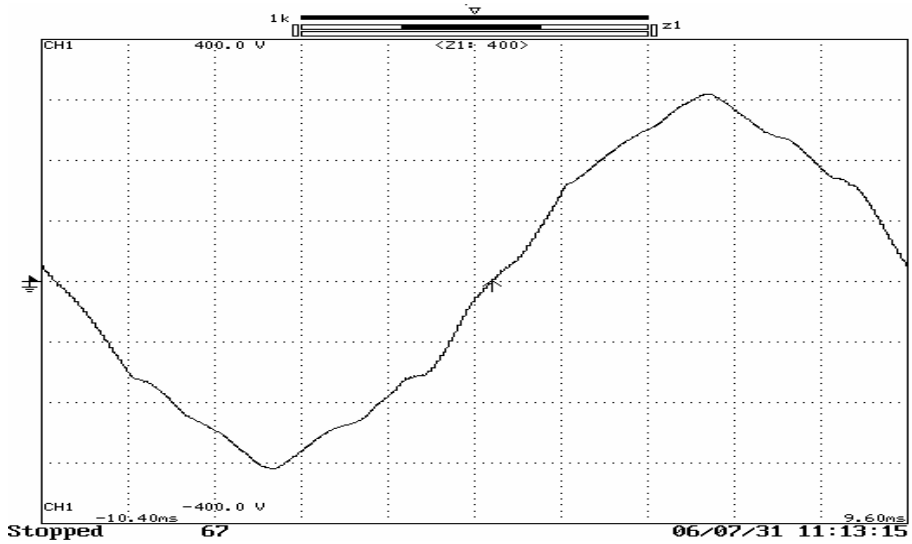

Figure 8.13 Phase voltage with kvh=2

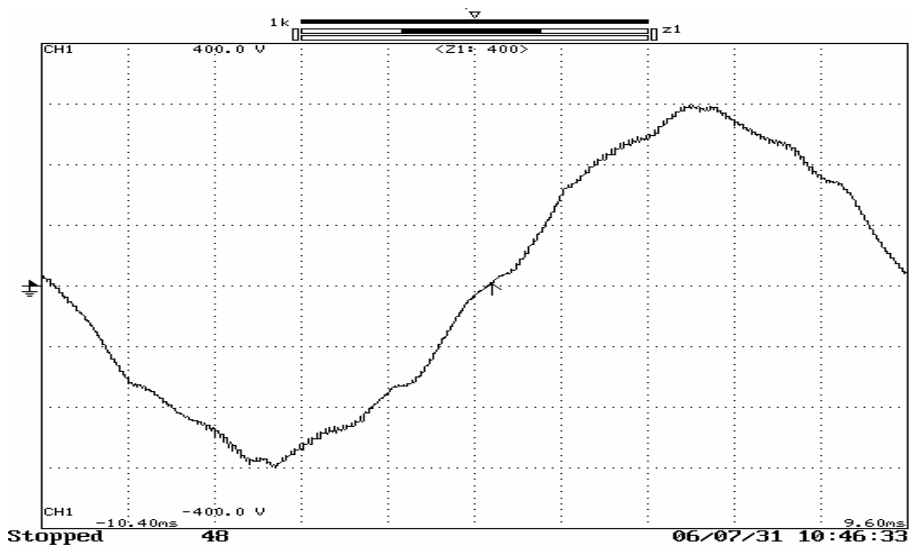

Figure 8.14 Phase voltage with kvh=4

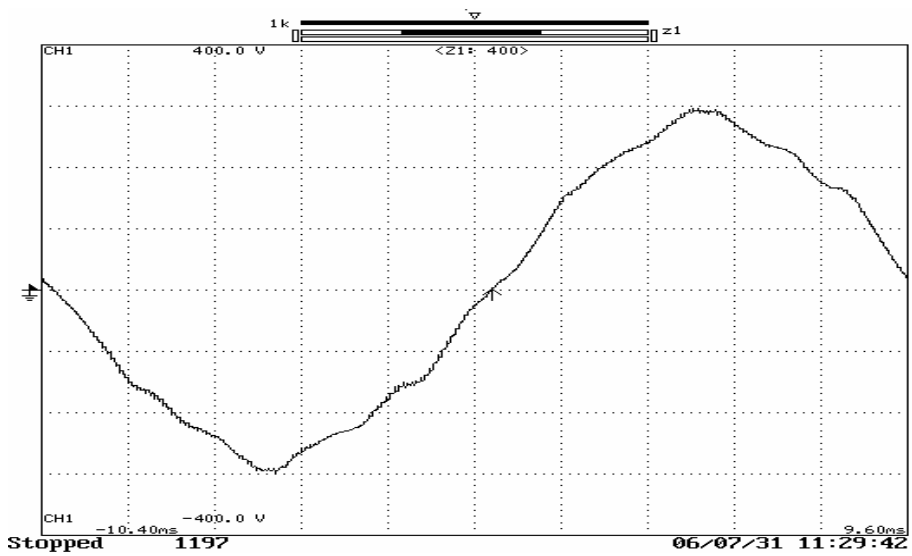

Figure 8.15 Phase voltage with kvh=6

Table 8.5 Spectrum of the phase voltage with different gain values

Case	Order	1	5	7	11	13	17	19
kvh=0	Voltage (V)	212	22.89	9.03	1.60	1.66	0.84	0.84
kvh=2	Voltage (V)	210	16.72	4.81	1.25	1.50	0.59	0.52
kvh=4	Voltage (V)	211	8.32	4.37	1.04	1.08	0.60	0.77
kvh=6	Voltage (V)	208	3.95	3.54	1.25	0.89	0.50	0.79

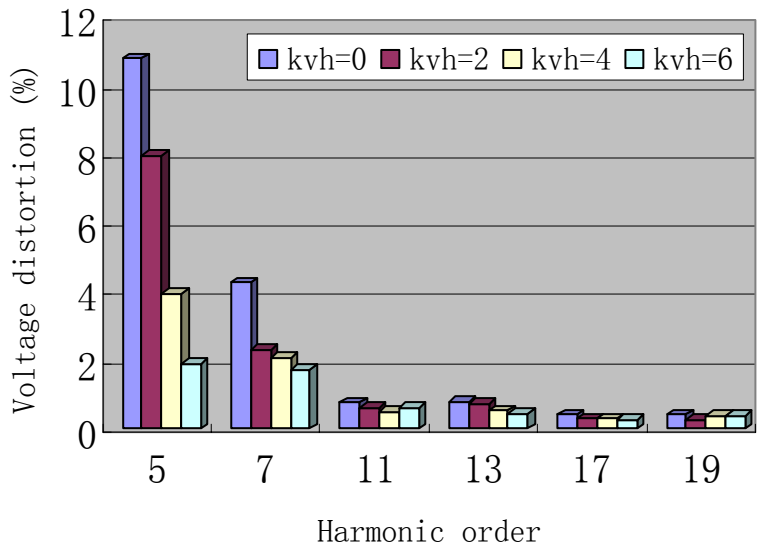

Figure 8.16 Spectrum of the phase voltage with different gain values in percentage

8.5.5 Damping of Harmonic Resonance

To test the damping effect of the proposed SAPF, the laboratory testing system with the configuration shown in Figure 8.7 (b) was tuned to produce harmonic resonance at 280 Hz when the proposed SAPF was disconnected. Similarly, the control gain varied from 0 – 6 with a step of 2 to show the damping effect of the SAPF. Again the case where the SPAF is switched off is denoted by a zero value for Kvh, that is, Kvh=0. The phase voltage at the point of connection is shown in Figure 8.17-8.20. The equivalent impedance of each order is presented in

Table 8.6 and plotted in Figure 8.21, which was calculated by dividing the harmonic voltage over the corresponding current measured. From these results, it can be drawn that the damping effect at the resonance frequency is significant and the SAPF with the large control gain has better performance. And it is also shown in Figure 8.21 that the possible harmonic resonance frequency is upward shifted.

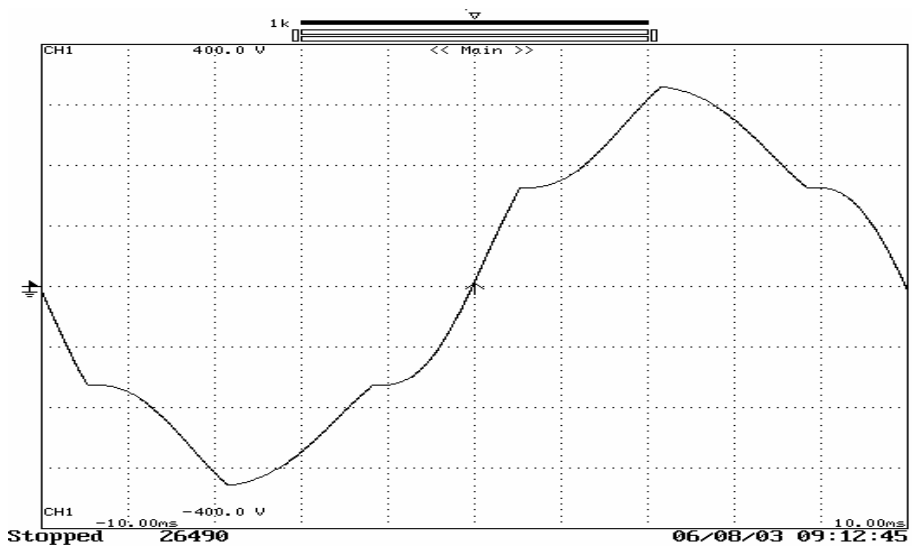

Figure 8.17 Phase voltage with kvh=0

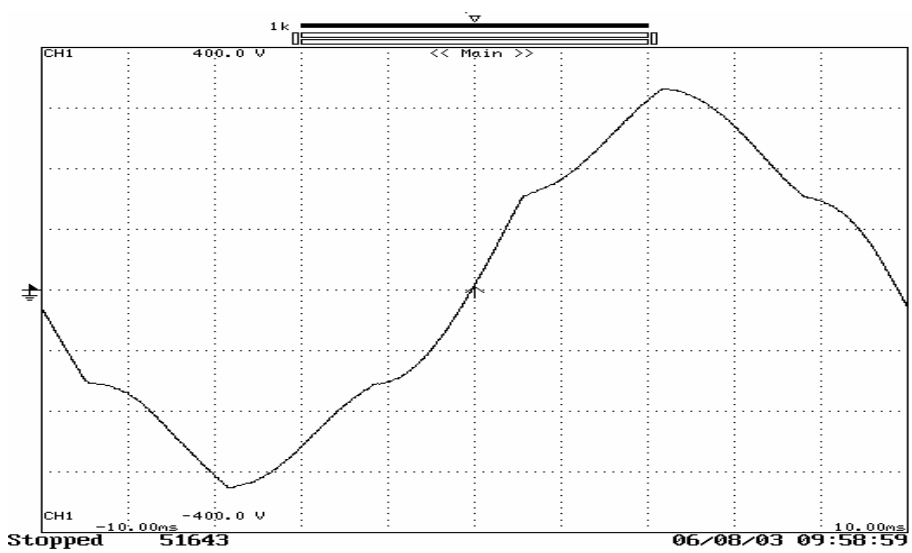

Figure 8.18 Phase voltage with kvh=2

Figure 8.19 Phase voltage with kvh=4

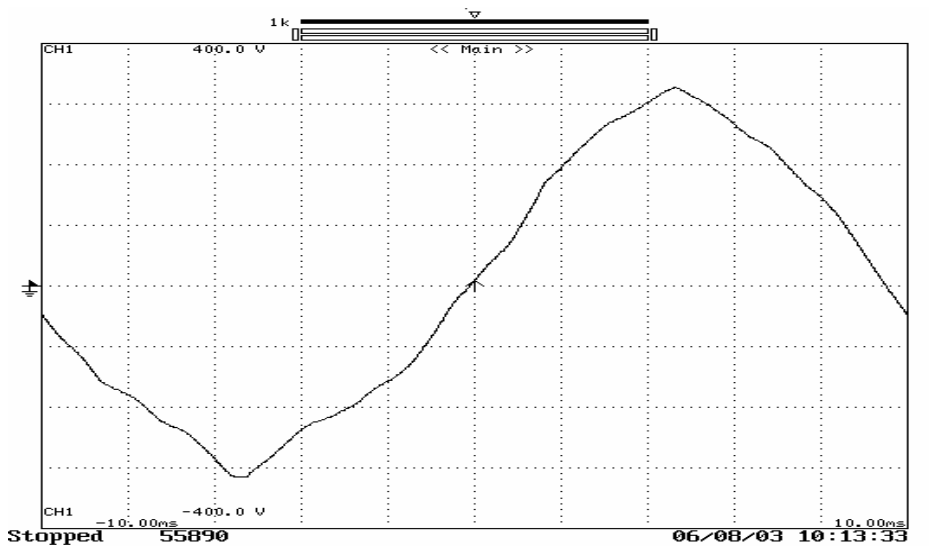

Figure 8.20 Phase voltage with kvh=6

Table 8.6 The spectrum analysis of the voltage for the cases with the capacitor bank

Case	Order	1	5	7	11	13	17	19
kvh=0	Current (A)	5.38	0.49	0.23	0.24	0.22	0.16	0.16
	Voltage (V)	216	21.27	7.56	2.52	1.68	0.84	0.84
kvh=2	Voltage (V)	209	14.63	3.76	1.86	1.25	0.63	0.27
kvh=4	Voltage (V)	208	7.49	4.37	2.12	1.00	0.10	0.77
kvh=6	Voltage (V)	208	4.99	5.47	1.77	0.69	0.33	0.60
kvh=0	Imp (Ω)	1.86	43.71	33.35	10.50	7.64	5.25	5.25
kvh=2	Imp (Ω)	2.04	30.06	8.02	7.75	5.70	3.92	1.70
kvh=4	Imp (Ω)	2.23	15.39	19.27	8.84	4.54	0.65	4.81
kvh=6	Imp (Ω)	2.23	10.26	24.13	7.37	3.12	2.08	3.77

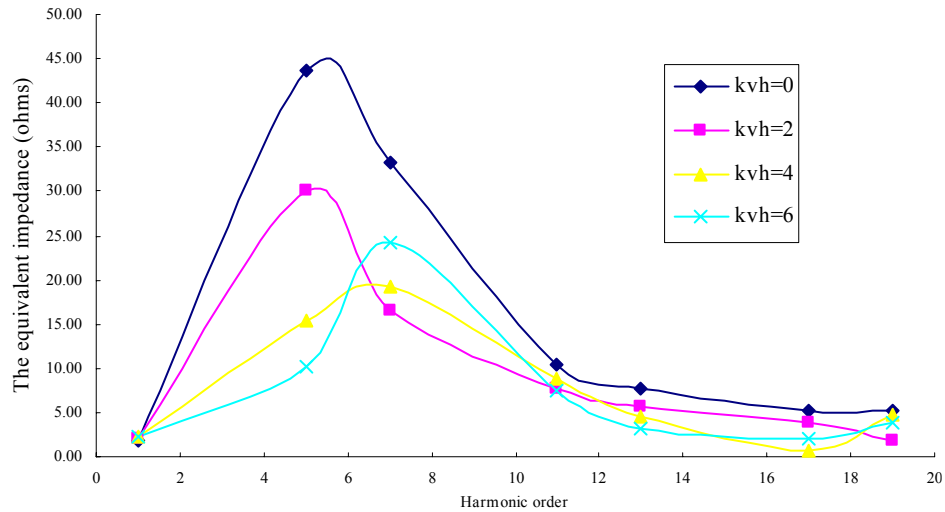

Figure 8.21 Equivalent harmonic impedance with different gain values

8.5.6 Application of the Proposed SAPF in the Equivalent Building Distribution System

A laboratory experiment was conducted to validate the harmonic mitigation effect by the proposed SAPF in a building distribution system. The system with the configuration presented in Chapter 7 was adopted and listed in Table 8.7. The equivalent impedance of the sub-main circuit was increased in order to decrease the system current to a level that the laboratory testing system can tolerate. The harmonic source was only installed at the end of the circuit. The capacitor for the PFC was installed at the beginning of the circuit, as seen in Figure 7.15.

Table 8.7 Information of the building distribution system

Equivalent capacitor for PFC	35μF	Linear loads	Disconnected
Equivalent riser impedance	Resistance: 0.3Ohms	Harmonic loads	One harmonic sources
	Inductance: 0.78mH		

Similar to the procedure used in the simulation, the test was conducted with different values of the control gain. Because the impedance of the circuit in the laboratory testing system increased, the control gain correspondingly decreased. The numerical results are shown in Table 8.8. Figures 8.22-8.25 presented the waveforms of the phase voltage at point of connection with the control gain increasing from 0 to 6. It can be seen that the harmonic voltage distortion at the point of connection is gradually reduced as the control gain is increased from 0 to 6. Especially harmonic voltage at low orders, such as the 5^{th}, 7^{th}, 11^{th}, 13^{th} orders, harmonic mitigation by the SAPF is significant.

Table 8.8 Harmonic mitigation with different values of the control gain

kvh	1 (V)	5 (%)	7 (%)	11 (%)	13 (%)	17 (%)	19 (%)
0	213	7.21	1.92	1.61	0.31	0.43	0.21
2	215	5.53	1.30	1.44	0.25	0.38	0.20
4	216	3.41	1.25	1.31	0.19	0.34	0.25
6	214	1.89	1.14	1.07	0.08	0.25	0.21

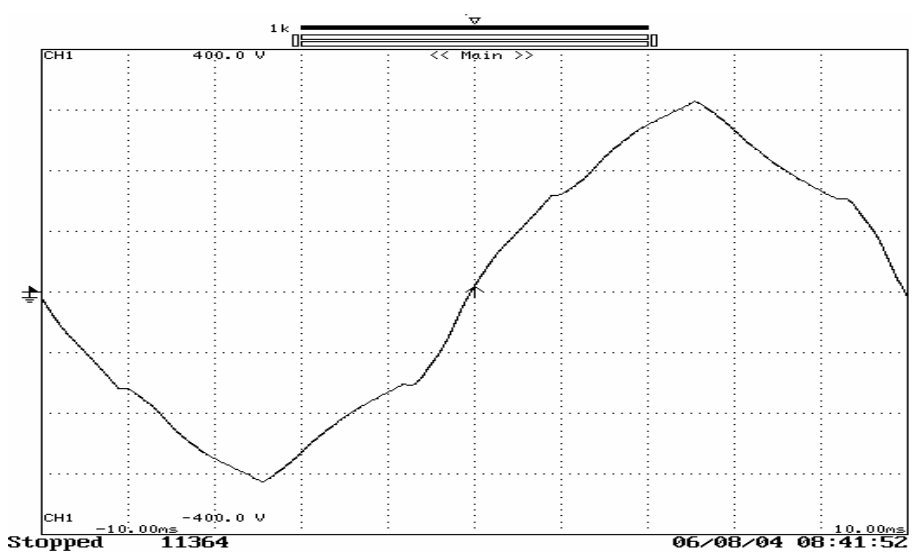

Figure 8.22 Phase voltage with Kvh=0

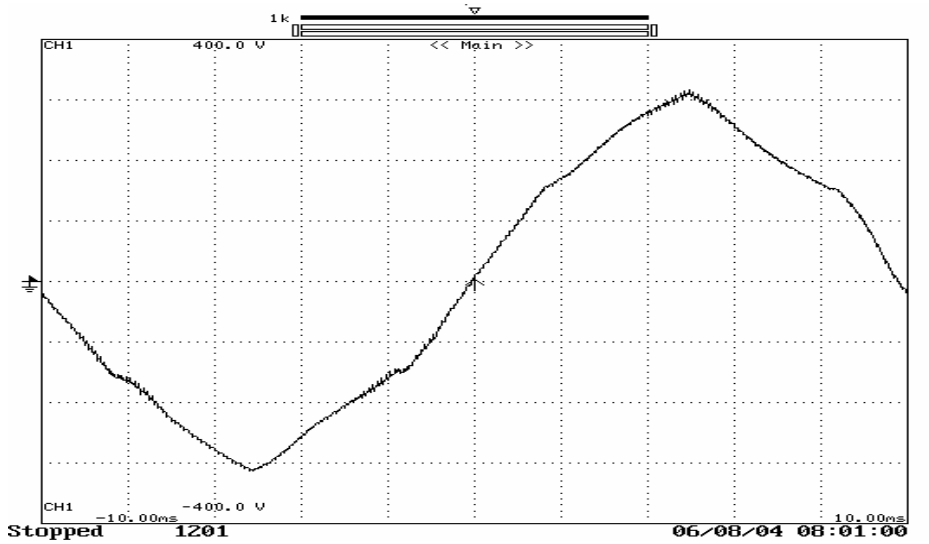

Figure 8.23 Phase voltage with Kvh=2

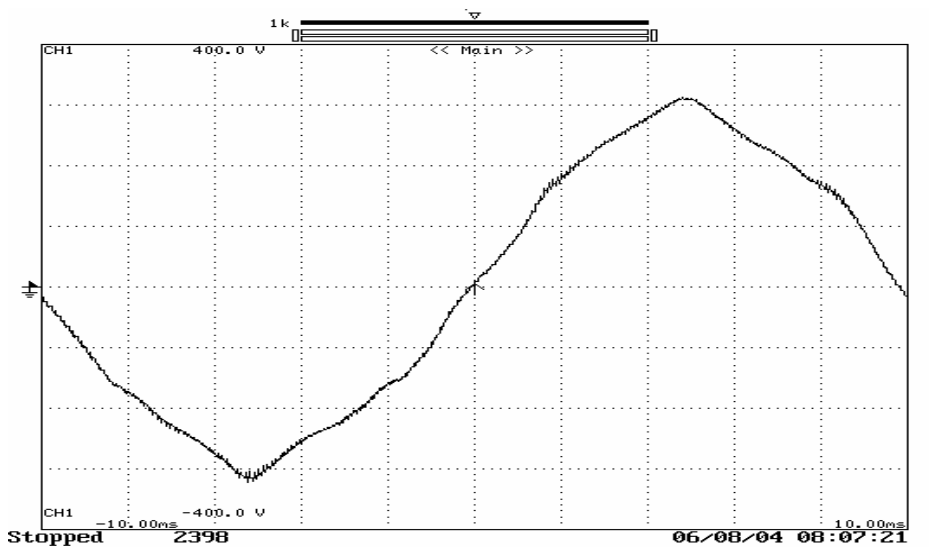

Figure 8.24 Phase voltage with Kvh=4

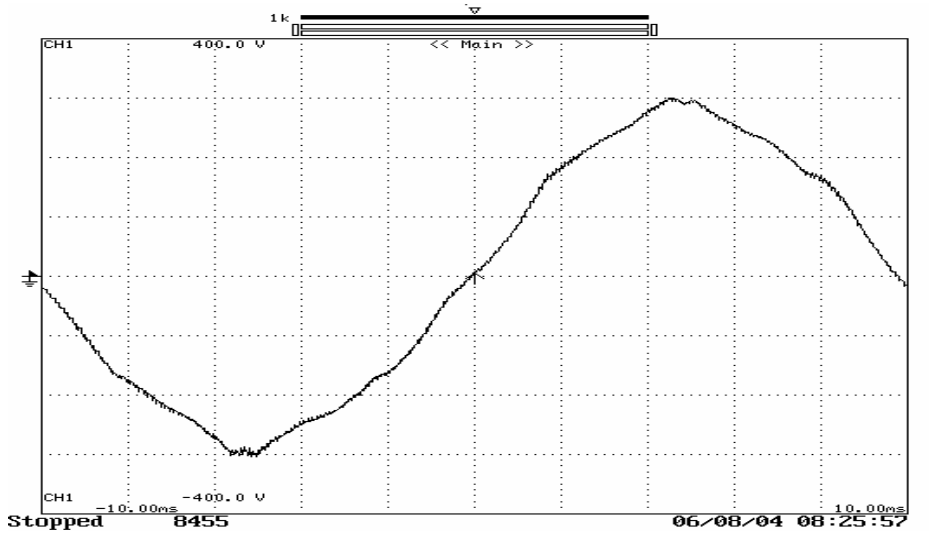

Figure 8.25 Phase voltage with Kvh=6

8.6 Summary

This chapter discussed the hardware and software implementation of the proposed SAPF. A laboratory testing system including the building distribution system and the harmonic source was set up. A prototype of the proposed SAPF was developed. The hardware and software implementation was described in the chapter. Two system configurations were adopted for the laboratory experiment. The characteristics of the SAPF were presented, such as charging of DC-bus voltage, the state-steady compensating current, and the transient response of the proposed SAPF. Finally, the performance of the proposed SAPF on harmonic mitigation and resonance damping was investigated. The results validated the control strategy of the proposed SAPF and the potential in harmonic voltage control.

It is showed that the better mitigation effect was obtained with the larger control

gain. The experiment on the damping of harmonic resonance indicated the proposed SAPF had the ability of damping harmonic resonance.

The application of the proposed SAPF in the building distribution system was conducted in the laboratory system. The results verified that the proposed SAPF may be installed on the feeder or sub-main circuit to improve the harmonic voltage distortion.

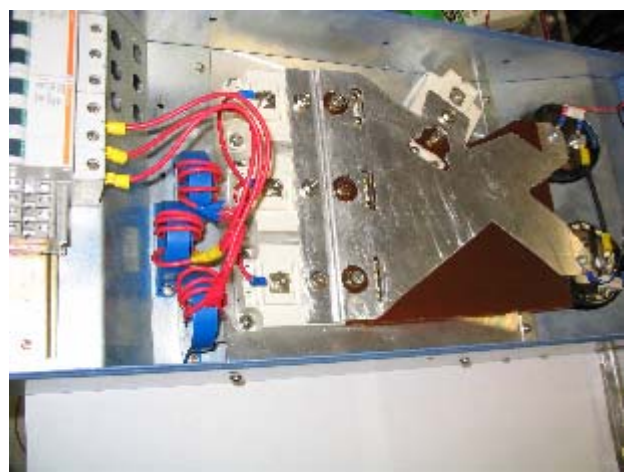

Figure A.8.1 The main circuit of the proposed SAPF in the laboratory system

Figure A.8.2 The switching ripple filter used in the laboratory system

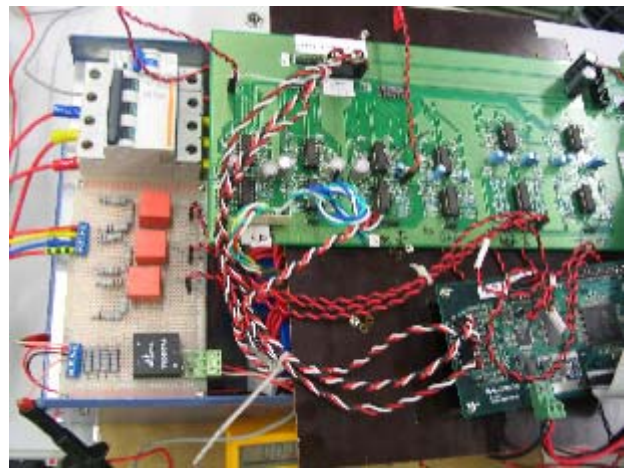

Figure A.8.3 The setup of the proposed SAPF in the laboratory system

Chapter 9

Conclusions and Future Work

9.1 Conclusions

I. Characteristics of harmonics in high-rise commercial buildings

In this thesis the characteristics of harmonics in high-rise commercial buildings were revealed. Harmonics in such buildings has unique features. Firstly, there is a mass of harmonic sources located in a small-scale low-voltage distribution system. It is impossible to compensate harmonic currents from individual sources one by one. Although most of harmonic sources are in small size, the total harmonic current generated can be significant.

Secondly, harmonics in the buildings are produced by both landlord loads and tenant loads. Harmonic current sources in the building distribution systems are generally unpredictable. This feature indicates that the solution should have a capability of responding the dynamically changing harmonics in the system.

Thirdly, cables, transformers as well as capacitor banks may exacerbate the harmonics in the distribution system due to their non-trivial impedance. The influx of harmonic currents from the distributed loads on different floors to the rising main circuit leads to unexpected harmonic voltage distortion. In some

cases, the harmonic voltage distortion on the upper floors may reach up to 17-20%. In addition, the capacitor banks installed may bring harmonic resonance in the distribution system.

II. Cabling in high-rise commercial buildings

Harmonic impedance of the distribution components has a significant impact on harmonics in the distribution system. Electric cables are one of the components, which are commonly used for rising main circuits. This thesis investigated the harmonic impedance of commonly-used electric cables using an experimental approach. An impedance database was built for single-core and multi-core armored cables with the cross-section areas of 95mm^2, 120mm^2, 150mm^2, 185mm^2, 240mm^2, 300mm^2, 400mm^2 and 630mm^2.

The revealed harmonic impedance under different conditions may serve as a reference to designers or engineers in selecting appropriate cables as well as installation methods to minimize harmonic distortion in the building distribution systems.

Firstly, for the multi-core armored cables, it was concluded that,

a) The resistance of the cables increases as the harmonic order or the cable size increases due to the skin and proximity effects of the cable conductors, as well as to eddy current losses within the steel wire armor.

b) The inductance of the cables is frequency-dependent.

c) Empirical formulas were derived, which reveals the rule of harmonic impedance of cables and may be used to estimate the harmonic impedance for other sizes of cables with the same types.

Secondly, for the single-core aluminum-armored cables, it was concluded that

a) The resistance with a solid boding system is larger than that with single point bonding. It is noted that the spare capacity of the cable should be considered due to increasing resistance if the solid bonding system is used. The inductance with solid bonding is smaller than that with single point bonding because of existence of the mutual inductance between the armor loop and the conductor loop.

b) Under the single-point bonding configuration, the descending orders of the impact of formations on the cable impedance are as follows: for the resistance, flat-and-touching, trefoil and flat-and-spacing, for the reactance, flat-and-spacing, flat-and-touching and trefoil. Under the bonding configuration, the impact of the different formations is greatly reduced.

c) Under the single-point bonding configuration, the descending sequence of the reactance is in-trunking, on-tray and in-free-air. Under the bonding condition, the impedance is not sensitive to the formation of the cables.

Thirdly, for the single-core non-armored cables, it was concluded that

a) The resistance the sequence of the impact of the different formations is flat-and-touching, trefoil and flat-and-spacing that is the minimum. The descending trend is flat and spacing, flat and touching, and then trefoil.

b) The condition of in-trunking has most significant impact on the impedance of the cables, and the condition of on-tray is less, and the condition of free-air has the minimum impact.

III. Harmonic management in high-rise commercial buildings

Harmonic management in high-rise commercial buildings was discussed and proposed in this thesis. Firstly, harmonic limits and a harmonic assessment procedure were presented using ER G5/4 and other harmonic standards for the building distribution system in commercial buildings.

Secondly, it was concluded that responsibility sharing in harmonic control was critical for effective harmonic management in a commercial building. The utility is responsible for the quality of the voltage at the secondary of distribution transformers. The landlord as a virtual customer at PCC1 is responsible for harmonic management inside the building. On one hand, the landlord controls the harmonic current injection into the utility network within the consultative limits. On the other hand, the landlord monitors the harmonics inside the building and may be responsible for mitigating excessive harmonics to provide qualified power supply to the tenants. Correspondingly, the tenants

are required to limit their harmonic current injection to the building distribution system. A tariff scheme may be possibly implemented. The tenants may pay for excessive harmonic current injection if they cannot reduce the harmonic current emission from their equipment.

IV. Harmonic voltage mitigation by the proposed SAPF

As an effective tool for harmonic control, a novel SAPF based on voltage detection was proposed and designed to achieve harmonic voltage mitigation within a building distribution system. The voltage-detection SAPF is suitable for applications in the distribution system of commercial buildings. In order to damp harmonic resonance effectively in a system, it was recommended to install the proposed SAPF at the end of a rising main circuit located on the upper floor of the buildings.

In order to solve the instability problem of the SAPF based on voltage detection, a novel multi-channel complex-gain controller was proposed. The control algorithms were implemented in the harmonic synchronous reference frames. The harmonics signals were processed in their corresponding channels. The adjustment of the control gain in either magnitude or phase angle or a combination of both helped to improve the stability margins, as well as the adjustment of the cutoff frequency in the low pass filters. The response time of the low pass filter, however, may be increased.

The feature of multiple channels in the controller makes it possible to set different values of the control gain in different channels. With this feature the upper limit of the control gain can be raised, and the control gain can be set with large values in specific channels to filter out dominant harmonics in a distribution system.

The feature of complex gain in the controller makes it possible to adjust the phase angle of the control gain independently at each harmonic order. Apart from the stability margins, the adjustment of phase angle can also help to change the equivalent impedance of the proposed SAPF, i.e. the resistance, the capacitance, inductance, or a combination of them.

The simulation and experiment results showed that the proposed SAPF can be applied in high-rise commercial buildings to control harmonic voltage distortion within the distribution system.

9.2 Future Works

I. Auto-adaptive control gain

According to the discussions in this thesis, it would be better if the proposed SAPF has the capability of real-time adjustment of the control gain in the

multi-channel complex-gain controller. This may improve the dynamic response of the SAPF to the harmonic loading, and help to keep the harmonic voltage distortion in the system at acceptable levels with a minimum filter rating. In addition, the SPAF may have the capability of real-time tuning to damp the harmonic resonance, which may arise from a sudden change in the distribution system.

II. Operation of multiple APFs

With the proposed SAPF, the harmonic voltage along a distribution circuit can be controlled. When the distribution system has multiple rising main circuits, a single SAPF is not sufficient to control harmonic voltage and current distortion in all circuits. It is necessary to install a number of APFs within the building to control harmonics effectively in the system. The issues of APF type, the APF location and cooperation strategy among these APF need to be addressed in detail.

Reference

[1] A. Ghosh etc. 2000
A. Ghosh and A. Joshi
A new approach to load balancing and power factor correction in power distribution system
IEEE Trans. Power Delivery, Vol. 15, No. 1, Jan. 2000, pp. 417-422

[2] Ahmed E.E. etc. 2005
Ahmed E.E., Xu W., Guibin Zhang
Analyzing systems with distributed harmonic sources including the attenuation and diversity effects
IEEE Transactions on Power Delivery, Volume 20, Issue 4, Oct. 2005 Page(s):2602 - 2612

[3] Akagi.H etc. 1984
Akagi.H, Kanazawa.Y, and Nabae.A
Instantaneous reactive power compensators comprising switching device without energy storage components
IEEE Trans. on Industry Applications, (20), 3, 1984, pp. 625-630

[4] Akagi.H etc. 1999
Akagi, H.; Ogasawara, S.; Hyosung Kim
The theory of instantaneous power in three-phase four-wire systems: a comprehensive approach
Industry Applications Conference, Thirty-Fourth IAS Annual Meeting, Vol. 1, 3-7 Oct. 1999 Page(s): 431 – 439

[5] Bhim Singh etc. 1999
Bhim Singh, Kamal Al-Haddad, Ambrish Chandra
A review of active filters for power quality improvement
IEEE Transactions on Industrial Electronics, Vol. 46, No. 5, October, 1999, pp. 960-971

[6] BS EN 1993
BS EN 61000-4-7
EMC, Part 4, Testing and measurement techniques, section 7, General guide on harmonics and interharmonics measurements and instrumentation, for power supply systems and equipment connected thereto

[7] BSI 1992
British Standard Institution
BS 7671: Requirements for Electrical Installations – IEE wiring Regulations

1992

[8] Burgos R.P. etc. 1998
Burgos R.P., Zapata F.F., Wiechman E.P., Salazar L.D.
Power converter analysis and design using Matlab: a transfer function approach
Industrial Electronics, Proceedings ISIE '98 IEEE International Symposium on Volume 2, 7-10 July 1998 Page(s):552 - 557

[9] Bor-Ren Lin etc. 2001
Bor-Ren Lin, Zong-Liang Hung, Shuh-Chuan Tsay, Mu-Shan Liao
Shunt active filter with sliding mode control
Electrical and Electronic Technology, TENCON Proceedings of IEEE Region 10 International Conference on Volume 2, 19-22 Aug. 2001 Page(s):884 - 889

[10] Cardenas V. etc. 1998
Cardenas V., Vazquez N., Herndndez C.
Sliding mode control applied to a 3Φ shunt active power filter using compensation with instantaneous reactive power theory
Power Electronics Specialists Conference, PESC 98 Record 29th Annual IEEE, Volume 1, 17-22 May 1998 Page(s):236 – 241

[11] Chang Y.N. etc. 1993
Chang Y.N., Moo C.S. and Jeng J.C.
Harmonic analysis of fluorescent lamps with electromagnetic ballasts
IEEE Proceedings of Computer, Communication, Control and Power Engineering, TENCON, 1993

[12] Chin Lin Chen etc. 1994
Chin Lin Chen, Chen E. Lin, Huang, C.L.
An active filter for unbalanced three-phase system using synchronous detection method
Power Electronics Specialists Conference, PESC '94 Record, 25th Annual IEEE 20-25 June 1994 Page(s):1451 - 1455

[13] D. G. Holmes etc. 1996
D. G. Holmes and D. A. Martin
Implementation of direct digital predictive current controller for single and three phase voltage source inverters
Conf. Rec. IEEE-IAS Annu. Meeting, 1996, pp. 906–913

[14] Energy Advisory Committee 1998
The energy advisory committee (Hong Kong)

Code of practice for energy efficiency of electrical installations

[15] F. Abrahmsen 2000
Energy optimal control of induction motor drives
Ph.D. dissertation, Aalborg University, Institute of Energy Technology, 2000, ISBN 87-89179-26-9

[16] Fang Zheng Peng 1998
Application issue of active power filters
IEEE Industry Applications Magazine, Vol. 4, Issue 5, pp. 21-30, September/October 1998

[17] Fang Zheng Peng etc. 1996
Fang Zheng Peng, Jih-sheng Lai
Application considerations and compensation characteristics of shunt active and series active filters in power systems
Proceeding of ICHQP, Las Vegas, Nevada, October, 1996, pp.12-20

[18] Fang Zheng Peng etc. 1998
Fang Zheng Peng, Ott G.W. Jr., Adams D.J.
Harmonic and reactive power compensation based on the generalized instantaneous reactive power theory for 3-phase 4-wire systems
Power Electronics, IEEE Transactions on Volume 13, Issue 6, Nov. 1998 Page(s):1174–1181

[19] FSD 1998
Fire Service Department
Codes of practice for minimum fire service installations and equipment and inspection and testing o installations and equipment
June, 1998

[20] F. Z. Peng etc. 1996
F. Z. Peng, J. S. Lai
Generalized instantaneous reactive power theory for three-phase power systems
IEEE Trans. On Instrumentation and Measurement, Vol. 45, No. 1, Feb. 1996, pp. 293-297

[21] Gawlik W.H.M. 2003
Time domain modeling of active filters for harmonic compensation
Power Tech Conference Proceedings, IEEE Bologna Volume 2, 23-26 June 2003 Page(s):

[22] George J. Anders 1997

Rating of Electric Power Cables---Ampacity Computations for Transmission, Distribution, and Industrial Applications
The Institute of Electrical and Electronics Engineers, Inc., New York

[23] G.J. Wakileh 2001
Power systems harmonics: fundamentals, analysis, and filter design
New York, Springer, 2001

[24] G. –K. Hung etc. 2001
G. –K. Hung, C. –C. Chang and C. –L. Chen
Analysis and implementation of a delay-compensated deadbeat current controller for solar inverters
IEE Proceeding of Circuits Devices System, vol. 148, No. 5, October 2001, Page(s): 279 - 286

[25] Graovac D. etc. 2001
Graovac D., Katic V.
Online control of current-source-type active rectifier using transfer function approach
Industrial Electronics, IEEE Transactions on Volume 48, Issue 3, Jun 2001 Page(s):526 – 535

[26] Hamadi A. etc. 2004
Hamadi A., Al-Haddad K., Rahmani S., Kanaan H.
Comparison of fuzzy logic and proportional integral controller of voltage source active filter compensating current harmonics and power factor
Industrial Technology, IEEE ICIT '04. 2004 IEEE International Conference on Volume 2, 8-10 Dec. 2004 Page(s):645 - 650

[27] Hamasaki S. etc. 2003
Hamasaki S., Kawamura A.
Improvement of current regulation of line-current-detection-type active filter based on deadbeat control
Industry Applications, IEEE Transactions on Volume 39, Issue 2, March-April 2003 Page(s):536 - 541

[28] H.-H. Kuo etc. 2001
H.-H. Kuo, S.-N. Yeh and J.-C. Hwang
Novel analytical model for design and implementation of three-phase active power filter controller
IEE Proceeding on electric Power Applications, Vol. 148, Issue 4, , July 2001, pp. 369-383

[29] Hirofumi Akagi 1996

New trends in active filters for power conditioning
IEEE Transaction on Industry Applications, Vol. 32, No. 6, November/December, 1996, pp. 1312-1322

[30] Hirofumi Akagi etc. 1999
Hirofumi Akagi, Hideaki Fujita, Keiji Wada
A shunt active filter based on voltage detection for harmonic termination of a radial power distribution line
IEEE Transaction on Industry Applications, Vol. 35, No. 3, May/June, 1999, pp. 638-645

[31] HKE 1995
The Hong Kong Electric Company Ltd.
Guide to connection of supply
GCS 2nd Edition, December, 1995

[32] Hongyu Li etc. 2005
Hongyu Li, Fang Zhuo, Zhaoan Wang, Lei W., Wu L.
A novel time-domain current-detection algorithm for shunt active power filters
Power Systems, IEEE Transactions on Volume 20, Issue 2, May 2005 Page(s):644 – 651

[33] Hosseini S.H. etc. 1998
Hosseini S.H., Aghagolzadeh A., Javidnia H., Zareeipoor H.R.
Deadbeat control of a power line conditioner
Electrical and Computer Engineering, IEEE Canadian Conference on Volume 1, 24-28 May 1998 Page(s):81 – 84

[34] H. Yang etc. 1996
H. Yang, P. Pirotte, E.D. Jaeger and A. Robert
Harmonic Emission Levels of Industrial Loads – Statistical Assessment
CIGRE Report 36-306, Paris, 1996

[35] IEC 1993
IEC Standard 1000-2-2
IEC Electromagnetic compatibility (EMC) Part 2: Environment Section 2: Compatibility levels for low-frequency conducted disturbances and signalling in public power supply systems

[36] IEC 1995
IEC Standard 1000-3-2
Part 3-2: Limits-Section 2: Limits for harmonic current emission (equipment input current <= 16A per phase)

[37] IEC 1996a
IEC Standard 1000-3-6
Part 3 Limits-Section 6 Assessment of emission limits for distorting loads in MV and HV power systems-Basic EMC publication

[38] IEC 1996b
IEC standard 61000-5-1
EMC, Part 5, Installation and mitigation guidelines, Section 1, General considerations, Basic EMC publication

[39] IEC 1997a
IEC standard 61000-6-1
EMC, Part 6, Generic standards-Section 1, Immunity for residential, commercial and light-industrial environments

[40] IEC 1997b
IEC standard 61000-5-2
EMC, Part 5, Installation and mitigation guidelines, Section 2, Earthing and cabling

[41] IEC 1998
IEC Standard 61000-3-4
Part 3-4: Limits-Limitation of emission of harmonic currents in low-voltage power supply systems for equipment with rated current greater than 16A

[42] IEC 2002
IEC standard 61000-2-4
EMC, Part 2-4, Environment-Compatibility levels in industrial plants for low-frequency conducted disturbances

[43] IEC 2003a
IEC standard 61000-4-30
EMC, Part 4-30, Testing and measurement techniques-power quality measurement methods

[44] IEC 2003b
IEC standard 61000-2-12
EMC, Part 2-12, Environment-Compatibility levels for low-frequency conducted disturbances and signaling in public medium-voltage power supply systems

[45] IEEE Task Force 1985
The Effects of Power System Harmonics on Power System Equipment and

Loads
IEEE Trans. on PAS, Vol. 104, Sept. 1985, pp. 2555-2563

[46] IEEE Task Force 1996a
Task Force on Harmonics Modeling and Simulation
Modeling and simulation of the propagation of harmonics in electric power networks, Part I: concepts, models, and simulation techniques
IEEE Trans. on Power Delivery, Vol. 11, No. 1, Jan. 1996, pp. 452-465

[47] IEEE Task Force 1996b
Task Force on Harmonics Modeling and Simulation
Modeling and simulation of the propagation of harmonics in electric power networks, Part II: sample systems and examples
IEEE Trans. on Power Delivery, Vol. 11, No. 1, Jan. 1996, pp. 466-474

[48] IEEE 1988
IEEE Guide for the Application of Sheath-bonding Methods for Single-conductor Cables and the Calculation of Induced Voltages and Currents in Cable sheaths
ANSI/IEEE Std. 575-1988

[49] IEEE 1990
Electric Power Systems in Commercial Buildings
IEEE Std. 241-1990

[50] IEEE 1992
IEEE Recommendation Practices and Requirements for Harmonic Control in Electric Power Systems
IEEE Std. 519-1992

[51] Joos G. etc. 2000
Joos G., Chen S., Haddad K.
Four Switch Three Phase Active Filter with Reduced Current Sensors
Proceedings of IEEE Annual Power Electronics Specialists Conference, (3), 2000, pp. 1318-1323

[52] Jou H.-L. 1995
Performance comparison of the three-phase active-power-filter algorithms
Generation, Transmission and Distribution, IEE Proceedings- Volume 142, Issue 6, Nov. 1995 Page(s):646 – 652

[53] Karimi-Ghartemani M. etc. 2005
Karimi-Ghartemani M., Iravani M.R., Katiraei F.
Extraction of signals for harmonics, reactive current and

network-unbalance compensation
Generation, Transmission and Distribution, IEE Proceedings- Volume 152, Issue 1, Jan 2005 Page(s):137 – 143

[54] Keiji Wada etc. 2002
Keiji Wada, Hideaki Fujita, Hirofumi Akagi
Considerations of a shunt active filter based on voltage detection for installation on a long distribution feeder
IEEE Transactions on Industry Applications, Vol. 38, No. 4, July/Aug. 2002, pp. 1123-1430

[55] K. Ferkal etc. 1996
K. Ferkal, M. Poloujadoff, E. Dorison
Proximity Effect and Eddy Current Losses in Insulated Cables
IEEE Transactions on Power Delivery, Vol. 11, No. 3, July 1996, pp. 1171-1178

[56] Lam J. 1994
Survey of harmonics in high-rise building
Research paper, BE4, 1994

[57] Lee K.K. 1989
Evaluation on the performance of three phase core type and single phase transformers
Hong Kong Polytechnic University, Department of Electrical Engineering, May, 1989

[58] L. Malesani etc. 1990
L. Malesani and P. Tenti
A novel hysteresis control method for current controlled VSI PWM inverters with constant modulation frequency
IEEE Trans. Ind. Application, Jan./Feb. 1990, vol. 26, pp. 88–92

[59] L. Malesani etc. 1995
L. Malesani, P. Mattavelli, and P. Tomasin
Improved constant frequency hysteresis current control of VSI inverters with simple feed forward bandwidth prediction
IEEE IAS Annu Meeting Conf. Rec., Orlando, FL, Oct. 1995, pp. 2633–2640

[60] L. Sonaglioni 1995
Predictive digital hysteresis current control
Conf. Rec. IEEE-IAS Annu. Meeting, Lake Buena Vista, FL, Oct. 1995, pp.1879–1886

[61] Luigi Malesani etc. 1997
Luigi Malesani, Paolo Mattavelli and Paolo Tomasin
High-performance hysteresis modulation technique for active filters
IEEE Trans. on Power Electronics, Vol. 12, No. 5, September 1997, pp. 876-884

[62] Luigi Malesani etc. 1999
Luigi Malesani, Paolo Mattavelli and Simone Buso
Robust dead-beat current control for PWM rectifiers and active filters
IEEE Trans. on Industry Applications, Vol. 35, No. 3, May/June 1999, pp. 613-620

[63] Mahesh K. Mishra etc. 2001
Mahesh K. Mishra, Avinash Joshi, Arindam Ghosh
A new compensation algorithm for balanced and unbalanced distribution systems using generalized instantaneous reactive power theory
Electric Power Systems Research, (60), 2001, pp. 29–37

[64] Malesani L. etc. 1997
Malesani L., Mattavelli P., Tomasin P.
High-performance hysteresis modulation technique for active filters
Power Electronics, IEEE Transactions on Volume 12, Issue 5, Sept. 1997 Page(s):876 – 884

[65] Manuel A. Perales etc. 2003
Manuel A. Perales, M. M. Prats, Ramon Portillo, Jose L. Mora, Jose I. Leon, and Leopoldo G. Franquelo
Three-dimensional space vector modulation in abc coordinates for four-leg voltage source converters
IEEE Power Electronics Letters, 2003

[66] Marian P. Kazmierkowski etc. 2002
Marian P. Kazmierkowski, R. Krishnan and Frede Blaabjerg
Control in power electronics
Academic Press, Elsevier Science (USA), 2002

[67] Massey G.W. 1994
Estimation methods for power system harmonic effects on power distribution transformers
IEEE Transactions on Industry Applications, Volume 30, Issue 2, March-April 1994 Page(s):485 - 489

[68] Mendalek N. etc. 2002

Mendalek N., Al-Haddad K., Fnaiech F., Dessaint L.A.
Sliding mode control of 3-phase shunt active filter in the d-q frame
Power Electronics Specialists Conference, 2002 IEEE 33rd Annual, Volume 1, 23-27 June 2002 Page(s):369 - 375

[69] M. EI-Habrouk etc. 2001
M. EI-Habrouk and M. K. Darwish
Design and implementation of a modified Fourier analysis harmonic current computation technique for power active filters using DSPs
Proc. Inst. Elect. Eng.—Elect. Power Appl., vol. 148, no. 1, pp. 21–28, Jan. 2001

[70] Mishra M.K. etc. 2000
Mishra M.K., Joshi A., Ghosh, A.
A new algorithm for active shunt filters using instantaneous reactive power theory
Power Engineering Review, IEEE Volume 20, Issue 12, Dec. 2000 Page(s):56 – 58

[71] Nash H.O. 1997
More about standby generator grounding
IEEE Trans. on Industry Applications, May/June, 1997

[72] Nishida K. etc. 2004
Nishida K., Rukonuzzman M., Nakaoka, M.
Advanced current control implementation with robust deadbeat algorithm for shunt single-phase voltage-source type active power filter
Electric Power Applications, IEE Proceedings, Volume 151, Issue 3, 8 May 2004 Page(s):283 – 288

[73] Nishida K. etc. 2002
Nishida K., Konishi Y., Nakaoka M.
Current control implementation with deadbeat algorithm for three-phase current-source active power filter
Electric Power Applications, IEE Proceedings, Volume 149, Issue 4, July 2002 Page(s):275 – 282

[74] Phipps J.K. 1997
A transfer function approach to harmonic filter design
Industry Applications Magazine, IEEE, Volume 3, Issue 2, March-April 1997 Page(s):68 – 82

[75] Quinn C.A. etc. 1992
Quinn C.A., Mohan N.

Active filtering of harmonic currents in three-phase, four-wire systems with three-phase and single-phase nonlinear loads
Applied Power Electronics Conference and Exposition, APEC '92. Conference Proceedings 1992, Seventh Annual, 23-27 Feb. 1992 Page(s):829 – 836

[76] Q. Yao etc. 1993
Q. Yao and D. G. Holmes
A simple, novel method for variable hysteresis-band current control of a three phase inverter with constant switching frequency
IEEE IAS Annu Meeting Conf. Rec., Toronto, Canada, Oct. 1993, pp. 1122–1129

[77] Rastogi M. etc. 1995
Rastogi M., Mohan. N., Edris A.-A.
Filtering of harmonic currents and damping of resonances in power systems with a hybrid-active filter
Applied Power Electronics Conference and Exposition, APEC '95 Conference Proceedings 1995., Tenth Annual, Issue 0, Part 2, 5-9 March 1995 Page(s):607 – 612

[78] Richard Zhang etc. 2002
Richard Zhang, V. Himamshu Prasad, Dushan Boroyevich and Fred C. Lee
Three-dimensional space vector modulation for four-leg voltage-source converters
IEEE Trans. on Power Electronics, Vol. 17, No. 3, May 2002, pp. 314-326

[79] S. Bhattacharya etc. 1996
S. Bhattacharya, D.M. Divan, A. Veltman, R.D. Lorenz
Flux-based active filter controller
IEEE Trans. on Industry Applications, (32), no.3, May/June 1996, pp. 491-501

[80] S. Bhattacharya etc. 1998
S. Bhattacharya, T.M. Franke, D.M. Divan, B. Banerjee
Active filter system implementation
IEEE Industry Applications Magazine, September/October, 1998, pp.47-63

[81] S. Buso etc. 1997
S. Buso, L. Malesani, P. Mattavelli and R. Veronese
Design and fully digital control of parallel active filters for thyristor rectifiers
Conf. Rec. IEEE-IAS Annu. Meeting, 1997, pp. 1360–1367

[82] Simone Buso etc. 1998
Simone Buso, Luigi Malesani and Paolo Mattavelli
Comparison of current control techniques for active filter applications
IEEE Trans. on Industrial Electronics, Vol. 45, No. 5, October 1998, pp. 722-729

[83] Singh B.N. etc. 1998
Singh B.N., Chandra H., Al-Haddad K.
Fuzzy control algorithm for universal active filter
Power Quality '98, 1998 Page(s):73 – 80

[84] S. Luo etc. 1991
S. Luo, Z. Lu, and Y. Zhou
A novel real-time harmonics and reactive power current detection method
Chongqing Univ. Trans., vol. 14, no. 6, pp. 28–31, Jun. 1991

[85] S. Mariethoz etc. 2002
S. Mariethoz, Alfred C. Rufer
Open loop and closed loop spectral frequency active filtering
IEEE Trans. on Power Electronics, (17), no.4, July 2002, pp. 564-573

[86] Sozanski K. etc. 2002
Sozanski K., Strzelecki R. and Kempski A.
Digital control circuit for active power filter with modified instantaneous reactive power control algorithm
Proceedings of IEEE Annual Power Electronics Specialists Conference, (2), 2002, pp. 1031-1036

[87] Suarez J.A. etc. 2005
Suarez J.A., di Mauro, G. Anaut D., Aguero C.
Analysis of the Harmonic Distortion and the Effects of Attenuation and Diversity in Residential Areas
Latin America Transactions, IEEE (Revista IEEE America Latina), Volume 3, Issue 5, Dec. 2005 Page(s):53 - 59

[88] Torrey D.A. etc. 1995
Torrey D.A., Al-Zamel and A.M.A.M.
Single-phase active power filters for multiple nonlinear loads
Power Electronics, IEEE Transactions on Volume 10, Issue 3, May 1995 Page(s):263 – 272

[89] Ting M.W. 1988
高層建築電氣 (Electrical design in high rise building)
水利電力出版社, 1988

[90] UK Electricity Association 2001
Engineering Recommendation G5/4
2001

[91] Wagner V.E. etc 1993
Wagner V.E., Balda J.C., Griffith D.C., McEachern A., Barnes T.M., Hartmann D.P., Phileggi D.J., Emannuel A.E., Horton W.F., Reid W.E., Ferraro R.J., Jewell W.T.
Effects of harmonics on equipment
IEEE Transactions on Power Delivery, Volume 8, Issue 2, April 1993 Page(s):672 - 680

[92] Wu J. C. 1996
Simplified control method for the single phase active power filter
Proc. of IEE –Elect. Power Application (143), 3, 1996, pp. 219-224

[93] Y. Du etc. 1998a
Y. Du, J. Burnett and Z.C. Fu
Harmonic characteristics, limits and design strategies for compliance in office buildings
Hong Kong Polytechnic University, 1998

[94] Y. Du etc. 1998b
Y. Du, J. Burnett
Harmonic characteristics and design compliance in large office buildings
Proc. of IEEE 36th IAS Annual Meeting, 1998, Vol. 3, pp. 2313 -2320

[95] Y. Du etc. 2001
Y. Du, J. Burnett
Current distribution in single-core cables connected in parallel
IEEE proceedings on Generation, Transmission, Distribution, Vol. 148, No. 5, September, 2001, pp. 406-412

[96] Young-Gook Jung etc. 1999
Young-Gook Jung, Ha-Suk Kim, Seung-Hak Yang, Young-Cheol Lim, Harashima F.
A simple instantaneous power theory and compensation performance evaluation for active power filters
TENCON 99. Proceedings of the IEEE Region 10 Conference, Vol. 2, 15-17 Sept. 1999 Page(s):1466 – 1470

[97] Young-Gook Jung etc. 2003
Young-Gook Jung, Woo-Yong Kim, Young-Cheol Lim, Seung-Hak Yang,

Harashima, F.
The algorithm of expanded current synchronous detection for active power filters considering three-phase unbalanced power system
TENCON 99 Proceedings of the IEEE Region 10 ConferenceIndustrial Electronics, IEEE Transactions on Volume 50, Issue 5, Oct. 2003 Page(s):1000 – 1006

[98] You Xiaojie etc. 2003
You Xiaojie, Li Yongdong, Hao Ruixiang, Cheng Zhiguang
A new synchronous frame current reference generation for hybrid active filter and system stability analysis
Industrial Electronics Society, 2003 IECON '03. The 29th Annual Conference of the IEEE Volume: 3, page(s): 2011- 2016

Appendix I

Publications Arising from the Thesis

1. ZH Yuan and Y. Du, "A Novel Shunt Active Power Filter Based on Voltage Detection for Harmonic Voltage Mitigation", IEEE Industry Applications Conference 2007, Accepted.
2. Zhenhuan Yuan and Yaping Du, "Active Control of Harmonic Voltage in an Electrical Distribution System", Proceedings of 2006 Sichuan-Hong Kong Joint Symposium, 30 June-July 1 2006, Chengdu China, Page(s): 189-197.
3. ZH Yuan and Y. Du, "Analytical Analysis of Shunt Active Power Filters Based on Voltage Detection", Proceeding of IEEE Industry Applications Conference and Fourtieth IAS Annual Meeting, Volume 2, 2-6 Oct. 2005, Hong Kong Page(s):1241 – 1245.
4. Y. Du and ZH Yuan, "Harmonic Impedance of Armored Cables for Low-voltage Power Distribution in Buildings", Proceeding of IEEE Industry Applications Conference and Fourtieth IAS Annual Meeting, Volume 3, 2-6 Oct. 2005 Page(s):2259 – 2263.
5. ZH Yuan and Y. Du, "A Shunt Active Harmonic Filter Based on a Voltage Detection Method for Harmonic Voltage Control", Proceedings of IEEE International Conference on Electric Utility Deregulation, Restructuring and Power Technologies, Volume 2, 5-8 April 2004 Page(s):763 – 768.

6. ZH Yuan and Y. Du, “Harmonics in a traction power supply system”, Proceeding (379-090) Power and Energy Systems - 2003.
7. ZH Yuan, Y. Du and J. Burnett “Harmonic assessment in high-rise buildings”, Proceedings of the CIBSC International Symposium 2003, Hong Kong, 26-27 September, 2003, page(s): 247-253.
8. Z.H. Yuan and Y. Du, “Harmonic impedance of single-core armored cables”, Proceeding of 2003 IEEE PES Transmission and Distribution Conference and Exposition, Vol.1, 7-12 Sept. 2003, Page(s): 45-48.

Appendix II

Parts of Source Codes

```
void pick_harmonics(void)
{
    int32 tmpcur32=0;
    int32 tmpvol32=0;
    vatmp=acq_a0-vadcoffset;
    vbtmp=acq_a1-vbdcoffset;
    vctmp=acq_b0-vcdcoffset;
    icatmp=acq_b1-icadcoffset;
    icbtmp=acq_c0-icbdcoffset;
    icctmp=acq_c1-iccdcoffset;
    ilatmp=acq_a0_2-iladcoffset;
    ilbtmp=acq_a1_2-ilbdcoffset;
    ilctmp=acq_b0_2-ilcdcoffset;

    ica=icatmp;
    tmpcur32=ica*kica;
    ica=(tmpcur32>>12);
    icb=icbtmp;
    tmpcur32=icb*kicb;
    icb=(tmpcur32>>12);
    icc=icctmp;
    tmpcur32=(icc*kicc);
    icc=(tmpcur32>>12);
    ila=ilatmp;
    tmpcur32=ila*kila;
    ila=(tmpcur32>>12);
    ilb=ilbtmp;
    tmpcur32=ilb*kilb;
    ilb=(tmpcur32>>12);
    ilc=ilctmp;
    tmpcur32=ilc*kilc;
    ilc=(tmpcur32>>12);

//the following is the set of the vdc and va,vb,vc

    vdc=vdc_ad;
    va=vatmp;
    tmpvol32=va*kva;
```

```
va=((tmpvol32)>>12);
vb=vbtmp;
tmpvol32=vb*kvb;
vb=((tmpvol32)>>12);
vc=vctmp;
tmpvol32=vc*kvc;
vc=((tmpvol32)>>12);

vdcerr = vdcref - vdc;    //q4.12
vdcpitmp32= vdckp*vdcerr;
vdcup=(vdcpitmp32>>12);
vdcpitmp32=vdcki*vdcerr;
vdcpitmp16=(vdcpitmp32>>12);
vdcpitmp32_2=vdckc*vdcsaterr;
vdcpitmp16_2=(vdcpitmp32_2>>12);
vdcui = vdcui +vdcpitmp16+vdcpitmp16_2;
vdcoutpresat = vdcup + vdcui;//
if (vdcoutpresat >vdcoutmax)
   {vdcout =    vdcoutmax;}
else if (vdcoutpresat < vdcoutmin)
   {vdcout =    vdcoutmin;}
else
   vdcout = vdcoutpresat;
vdcsaterr = vdcout - vdcoutpresat;

//the clark and park transformation of connect point voltage
//through va,vb to calculate the valpfa and vbeta
 tmpgp32_2=va;
 tmpgp32_3=vb;
 tmpgp32_4=vc;
 tmpgp32_2=((tmpgp32_2*0xaaa)>>12);
 tmpgp32_3=((((tmpgp32_3+tmpgp32_4)*0x555))>>12);
 valpha =tmpgp32_2-tmpgp32_3;

 tmpgp32_2=va;
 tmpgp32_3=vb;
 tmpgp32_4=vc;
 tmpgp32_3=((tmpgp32_3*0x93c)>>12);
 tmpgp32_4=((tmpgp32_4*0x93c)>>12);
 vbeta=tmpgp32_3-tmpgp32_4;

// Using look-up iQ sine table
   sine=sin[phase_index];
   cosine_index=phase_index+(sin_length>>2);
```

```
        if(cosine_index>=sin_length)
        {
            cosine_index-=sin_length;
        }
        cosine=sin[cosine_index];
        sin5_phase_index=phase_index*5;
        for    (;sin5_phase_index>=sin_length;)
        {
           sin5_phase_index-=sin_length;
        }
        sin5 =-sin[sin5_phase_index];
        cos5_phase_index=sin5_phase_index+(sin_length>>2);
        if (cos5_phase_index>=sin_length)
        {
            cos5_phase_index=cos5_phase_index-sin_length;
        }
        cos5=sin[cos5_phase_index];

        sin7_phase_index=phase_index*7;
        for    (;sin7_phase_index>=sin_length;)
        {
           sin7_phase_index-=sin_length;
        }
        sin7 =sin[sin7_phase_index];
        cos7_phase_index=sin7_phase_index+(sin_length>>2);
        if (cos7_phase_index>=sin_length)
        {
            cos7_phase_index=cos7_phase_index-sin_length;
        }
        cos7=sin[cos7_phase_index];

//through va,vb,vc to extract harmonics
        tmpgp32=cos5;
        parktmp32=valpha*tmpgp32;
       tmpgp32=sin5;
        parktmp32_2=vbeta*tmpgp32;
        parktmp16=(parktmp32>>15);
        parktmp16_2=(parktmp32_2>>15);
        vd5 = parktmp16+parktmp16_2;

       tmpgp32=cos5;
        parktmp32=vbeta*tmpgp32;
       tmpgp32=sin5;
        parktmp32_2=valpha*tmpgp32;
```

```
        parktmp16=(parktmp32>>15);
        parktmp16_2=(parktmp32_2>>15);
        vq5 =parktmp16-parktmp16_2;

       tmpgp32=cos7;
        parktmp32=valpha* tmpgp32;
       tmpgp32=sin7;
        parktmp32_2=vbeta*tmpgp32;
        parktmp16=(parktmp32>>15);
        parktmp16_2=(parktmp32_2>>15);
        vd7 = parktmp16+parktmp16_2;

        tmpgp32=cos7;
        parktmp32=vbeta*tmpgp32;
       tmpgp32=sin7;
        parktmp32_2=valpha*tmpgp32;
        parktmp16=(parktmp32>>15);
        parktmp16_2=(parktmp32_2>>15);
        vq7 =parktmp16-parktmp16_2;

  //through ica,icb to calculate the icalpfa and icbeta of the compensating current,
  //these are real value of the system used in the current regulator
      tmpgp32_2=ica;
      tmpgp32_3=icb;
      tmpgp32_4=icc;
      tmpgp32_2=((tmpgp32_2*0xaaa)>>12);
      tmpgp32_3=((((tmpgp32_3+tmpgp32_4)*0x555))>>12);
      icalpha =tmpgp32_2-tmpgp32_3 ;

      tmpgp32_2=ica;
      tmpgp32_3=icb;
      tmpgp32_4=icc;
      tmpgp32_3=((tmpgp32_3*0x93c)>>12);
      tmpgp32_4=((tmpgp32_4*0x93c)>>12);
      icbeta=tmpgp32_3-tmpgp32_4;

// lowpass filter used to filter the Ds and Qs to get the dc component
      lpfd5();
      lpfd7();
      lpfq5();
      lpfq7();
      vd5dc=outputd5buffer[2];
      vd7dc=outputd7buffer[2];
      vq5dc=outputq5buffer[2];
```

```
        vq7dc=outputq7buffer[2];

// kv and phase shift control
//the 5th
        tmpgp32_2=kv5;
        tmpgp32_3=vd5dc;
        tmpgp32_4=tmpgp32_2*tmpgp32_3;
        vd5dc=(tmpgp32_4>>12);
        tmpgp32_3=vq5dc;
        tmpgp32_4=tmpgp32_3*tmpgp32_2;
        vq5dc=(tmpgp32_4>>12);

        tmpgp32_3=tmpgp32_3*tmpgp32_2;
        tmpgp32_2=(tmpgp32_4>>12)*3784+(tmpgp32_3>>12)*1567;
        //cos22.5,sin22.5
        vd5dc=(tmpgp32_2>>12);
        tmpgp32_2=(tmpgp32_3>>12)*3784-(tmpgp32_4>>12)*1567;
        vq5dc=(tmpgp32_2>>12);

        tmpgp32_2=kv5;
        tmpgp32_3=vd5dc;
        tmpgp32_4=tmpgp32_2*tmpgp32_3;
        ild5dcfinal=(tmpgp32_4>>12);

        tmpgp32_2=kv5;
        tmpgp32_3=vq5dc;
        tmpgp32_4=tmpgp32_2*tmpgp32_3;
        ilq5dcfinal=(tmpgp32_4>>12);

//the 7th, no phase adjustment
        tmpgp32_2=kv7;
        tmpgp32_3=vd7dc;
        tmpgp32_4=tmpgp32_2*tmpgp32_3;
         ild7dcfinal=(tmpgp32_4>>12);

        tmpgp32_2=kv7;
        tmpgp32_3=vq7dc;
        tmpgp32_4=tmpgp32_2*tmpgp32_3;
         ilq7dcfinal=(tmpgp32_4>>12);

//inverse dq transformation of 5 order harmonics
        tmpgp32=cos5;
        gptmp32=ild5dcfinal*tmpgp32;
        tmpgp32=sin5;
```

```
        gptmp32_2=ilq5dcfinal*tmpgp32;
        iref5alpha=((gptmp32-gptmp32_2)>>15);

        tmpgp32=cos5;
        gptmp32=ilq5dcfinal*tmpgp32;
        tmpgp32=sin5;
        gptmp32_2=ild5dcfinal*tmpgp32;
        iref5beta =((gptmp32+gptmp32_2)>>15);

//inverse dq transformation of 7 order harmonics
        tmpgp32=cos7;
        gptmp32=ild7dcfinal*tmpgp32;
        tmpgp32=sin7;
        gptmp32_2=ilq7dcfinal*tmpgp32;
        iref7alpha=((gptmp32-gptmp32_2)>>15);

        tmpgp32=cos7;
        gptmp32=ilq7dcfinal*tmpgp32;
        tmpgp32=sin7;
        gptmp32_2=ild7dcfinal*tmpgp32;
        iref7beta =((gptmp32+gptmp32_2)>>15);

//inverse dq transform of the id charging current
        tmpgp32=-sine;
        ivdctmp32=vdcout*tmpgp32;
        ivdcdalpha=(ivdctmp32>>15);
        tmpgp32=cosine;
        ivdctmp32=vdcout*tmpgp32;
        ivdcdbeta=(ivdctmp32>>15);

//the final reference current of the compensating current
        ifin_ref_al=ivdcdalpha+iref7alpha+iref5alpha;
        ifin_ref_beta=ivdcdbeta+iref7beta+iref5beta;

//the following is the current regulator of the whole system
//the p control of ifin_al and ifin_be
        ialfaerr =icalpha-ifin_ref_al;
        gptmp32=ialphakp;
        gptmp32_2=ialfaerr;
        ialfout=((gptmp32*gptmp32_2)>>12);

// saturate the output
         if (ialfout >ialphapoutmax)
            {ialfout=ialphapoutmax;}
```

```
        else if (ialfout < ialphapoutmin)
            {ialfout=ialphapoutmin;}
        else
        {;}
       valpharef=ialfout+valpha;

       ibetaerr =icbeta-ifin_ref_beta;
       gptmp32=ibetakp;
       gptmp32_2=ibetaerr;
       ibetaout=((gptmp32*gptmp32_2)>>12);

      // saturate the output
        if (ibetaout >ibetapoutmax)
            {ibetaout =    ibetapoutmax;}
        else if (ibetaout < ibetapoutmin)
            {ibetaout =    ibetapoutmin;}
        else
        {;}
       vbetaref=ibetaout+vbeta;
}

void pwm_update(void)
{
        int32 pwmtmp32=0;
        int16 pwmtmp16=0;
        int16 d1=0;
        int16 d2=0;
        int16 d3=0;
        float pwmfloat=0.0;
        float d1_float=0.0;
        float d2_float=0.0;
        float d3_float=0.0;
        float tempfolat1=0.0;
        float tempfolat2=0.0;
        float tempfolat3=0.0;
        float tempfolat4=0.0;
        Uint16 taontmp=0;
        Uint16 tbontmp=0;
        Uint16 tcontmp=0;
        Uint16 tdontmp=0;
        Uint16 taon=0;
        Uint16 tbon=0;
        Uint16 tcon=0;
        Uint16 tdon=0;
```

```
        int32 tmp32=0;
        int32 tmp32_2=0;
       int32 tmp32_3=0;
       int32 tmp32_4=0;
// reference voltage for prism determination
        vref1 = vbetaref;
        tmp32 = valpharef;
        pwmtmp32 = tmp32*0xddb;    //0xddb in the q4.12 =sqrt(3)/2
        vref2 = (pwmtmp32>>12)-(vbetaref>>1);
        vref3 = -(pwmtmp32>>12)-(vbetaref>>1);

//reference voltage for tetrahedron determination
        vrefa = valpharef+vzeref;
        tmp32 = vbetaref;
        pwmtmp32 = tmp32*0xddb;
        vrefb = (pwmtmp32>>12)-(valpharef>>1)+vzeref;
        vrefc = -(pwmtmp32>>12)-(valpharef>>1)+vzeref;

//prism determination
       if (vref1>0)
            sector = 1;
       if (vref2>0)
            sector = sector + 2;
       if (vref3>0)
            sector = sector + 4;

//tetrahedron determination
         if (vrefa>0)
            subsector = 1;
         if (vrefb>0)
            subsector = subsector + 1;
         if (vrefc>0)
            subsector = subsector + 1;

// d1,d2,d3,dz calculation
      tmp32_2=valpharef;
      tmp32_3=vbetaref;
      tmp32_4=vzeref;
      tmp32=((tmp32_3*0xddb)>>12);
      tmppwm=EvbRegs.T3PR;

//sector=0, or 7
      if (sector==0|sector==7)
      {
```

```
        d1=(tmppwm>>1);
        d2=(tmppwm>>1);
        d3=(tmppwm>>1);
    }

    if (sector==1)
    {
        if (subsector==0)
        {
            d1=(tmp32_2>>1)-tmp32-tmp32_4;
            d2=-((tmp32_2*0x1800)>>12)+tmp32;
            d3=((tmp32_2*0x1800)>>12)+tmp32;
        }

        else if (subsector==1)
        {
            d1=-(tmp32_2>>1)+tmp32+tmp32_4;
            d2=-tmp32_2-tmp32_4;
            d3=((tmp32_2*0x1800)>>12)+tmp32;
        }

        else if (subsector==2)
        {
            d1=-((tmp32_2*0x1800)>>12)+tmp32;
            d2=tmp32_2+tmp32_4;
            d3=(tmp32_2>>1)+tmp32-tmp32_4;
        }

        else if (subsector==3)
        {
            d1=-((tmp32_2*0x1800)>>12)+tmp32;
            d2=((tmp32_2*0x1800)>>12)+tmp32;
            d3=-(tmp32_2>>1)-tmp32+tmp32_4;
        }
    }

    else if (sector==2)
    {
        if (subsector==0)
        {
            d1=-tmp32_2-tmp32_4;
            d2=((tmp32_2*0x1800)>>12)+tmp32;
            d3=-((tmp32*0x2000)>>12);
        }
```

```
        else if (subsector==1)
        {
            d1=tmp32_2+tmp32_4;
            d2=(tmp32_2>>1)+tmp32-tmp32_4;
            d3=-((tmp32*0x2000)>>12);
        }

        else if (subsector==2)
        {
            d1=((tmp32_2*0x1800)>>12)+tmp32;
            d2=-(tmp32_2>>1)-tmp32+tmp32_4;
            d3=(tmp32_2>>1)-tmp32-tmp32_4;
        }

        else if (subsector==3)
        {
            d1=((tmp32_2*0x1800)>>12)+tmp32;
            d2=-((tmp32*0x2000)>>12);
            d3=-(tmp32_2>>1)+tmp32+tmp32_4;
        }
    }
    else if (sector==3)
    {
        if (subsector==0)
        {
            d1=-tmp32_2-tmp32_4;
            d2=((tmp32_2*0x1800)>>12)-tmp32;
            d3=((tmp32*0x2000)>>12);
        }
        else if (subsector==1)
        {
            d1=tmp32_2+tmp32_4;
            d2=(tmp32_2>>1)-tmp32-tmp32_4;
            d3=((tmp32*0x2000)>>12);
        }
        else if (subsector==2)
        {
            d1=((tmp32_2*0x1800)>>12)-tmp32;
            d2=-(tmp32_2>>1)+tmp32+tmp32_4;
            d3=(tmp32_2>>1)+tmp32-tmp32_4;
        }
        else if (subsector==3)
        {
```

```
            d1=((tmp32_2*0x1800)>>12)-tmp32;
            d2=((tmp32*0x2000)>>12);
            d3=-(tmp32_2>>1)-tmp32+tmp32_4;
        }
    }
    else if (sector==4)
    {
        if (subsector==0)
        {
            d1=(tmp32_2>>1)+tmp32-tmp32_4;
            d2=-((tmp32*0x2000)>>12);
            d3=-((tmp32_2*0x1800)>>12)+tmp32;
        }
        else if (subsector==1)
        {
            d1=-(tmp32_2>>1)-tmp32+tmp32_4;
            d2=(tmp32_2>>1)-tmp32-tmp32_4;
            d3=-((tmp32_2*0x1800)>>12)+tmp32;
        }
        else if (subsector==2)
        {
            d1=-((tmp32*0x2000)>>12);
            d2=-(tmp32_2>>1)+tmp32+tmp32_4;
            d3=-tmp32_2-tmp32_4;
        }
        else if (subsector==3)
        {
            d1=-((tmp32*0x2000)>>12);
            d2=-((tmp32_2*0x1800)>>12)+tmp32;
            d3=tmp32_2+tmp32_4;
        }
    }

    else if (sector==5)
    {
        if (subsector==0)
        {
            d1=(tmp32_2>>1)-tmp32-tmp32_4;
            d2=((tmp32*0x2000)>>12);
            d3=-((tmp32_2*0x1800)>>12)-tmp32;
        }
        else if (subsector==1)
        {
            d1=-(tmp32_2>>1)+tmp32+tmp32_4;
```

```
            d2=(tmp32_2>>1)+tmp32-tmp32_4;
            d3=-((tmp32_2*0x1800)>>12)-tmp32;
        }
        else if (subsector==2)
        {
            d1=((tmp32*0x2000)>>12);
            d2=-(tmp32_2>>1)-tmp32+tmp32_4;
            d3=-tmp32_2-tmp32_4;
        }
        else if (subsector==3)
        {
            d1=((tmp32*0x2000)>>12);
            d2=-((tmp32_2*0x1800)>>12)-tmp32;
            d3=tmp32_2+tmp32_4;
        }
    }

    else if (sector==6)
    {
        if (subsector==0)
        {
            d1=(tmp32_2>>1)+tmp32-tmp32_4;
            d2=-((tmp32_2*0x1800)>>12)-tmp32;
            d3=((tmp32_2*0x1800)>>12)-tmp32;
        }
        else if (subsector==1)
        {
            d1=-(tmp32_2>>1)-tmp32+tmp32_4;
            d2=-tmp32_2-tmp32_4;
            d3=((tmp32_2*0x1800)>>12)-tmp32;
        }
        else if (subsector==2)
        {
            d1=-((tmp32_2*0x1800)>>12)-tmp32;
            d2=tmp32_2+tmp32_4;
            d3=(tmp32_2>>1)-tmp32-tmp32_4;
        }
        else if (subsector==3)
        {
            d1=-((tmp32_2*0x1800)>>12)-tmp32;
            d2=((tmp32_2*0x1800)>>12)-tmp32;
            d3=-(tmp32_2>>1)+tmp32+tmp32_4;
        }
    }
```

```
if (d1<0)
{d1=-d1;}
if (d2<0)
{d2=-d2;}
if (d3<0)
{d3=-d3;}

tmp32_2=vdcinvt;
tmp32_3=d1;
tmp32_4=tmp32_3*tmp32_2;
d1=(tmp32_4>>12);
tmp32_3=d2;
tmp32_4=tmp32_3*tmp32_2;
d2=(tmp32_4>>12);
tmp32_3=d3;
tmp32_4=tmp32_3*tmp32_2;
d3=(tmp32_4>>12);

//anti-saturation and dz calculation
pwmtmp16=d1+d2+d3;
test_c=pwmtmp16;
if (pwmtmp16>tmppwm)
{    tempfolat1=d1;
     tempfolat2=d2;
     tempfolat3=d3;
     tempfolat4=tmppwm;
     pwmfloat=tempfolat4/(tempfolat1+tempfolat2+tempfolat3);
     d1_float=tempfolat1*pwmfloat;
     d1=(Uint16)d1_float;
     d2_float=tempfolat2*pwmfloat;
     d2=(Uint16)d2_float;
     d3_float=tempfolat3*pwmfloat;
     d3=(Uint16)d3_float;
     t=1;
}
     else
     {t=0;}
     taontmp=((tmppwm-d1-d2-d3)>>1);
     tbontmp=taontmp+d1;
     tcontmp=tbontmp+d2;
     tdontmp=tcontmp+d3;

//allocation of CMPRx registers
```

```
if (sector==0|sector==7)
{
    taon=0;
    tbon=0;
    tcon=0;
    tdon=0;
}

if (sector==1)
{
    if (subsector==0)
    {
        taon=tcontmp;
        tbon=tbontmp;
        tcon=tdontmp;
        tdon=taontmp;
    }

    else if (subsector==1)
    {
        taon=tcontmp;
        tbon=taontmp;
        tcon=tdontmp;
        tdon=tbontmp;
    }

    else if (subsector==2)
    {
        taon=tbontmp;
        tbon=taontmp;
        tcon=tdontmp;
        tdon=tcontmp;
    }

    else if (subsector==3)
    {
        taon=tbontmp;
        tbon=taontmp;
        tcon=tcontmp;
        tdon=tdontmp;
    }
}

else if (sector==2)
```

```
{
    if (subsector==0)
    {
        taon=tbontmp;
        tbon=tdontmp;
        tcon=tcontmp;
        tdon=taontmp;
    }

    else if (subsector==1)
    {
        taon=taontmp;
        tbon=tdontmp;
        tcon=tcontmp;
        tdon=tbontmp;
    }

    else if (subsector==2)
    {
        taon=taontmp;
        tbon=tdontmp;
        tcon=tbontmp;
        tdon=tcontmp;
    }

    else if (subsector==3)
    {
        taon=taontmp;
        tbon=tcontmp;
        tcon=tbontmp;
        tdon=tdontmp;
    }
}
else if (sector==3)
{
    if (subsector==0)
    {
        taon=tbontmp;
        tbon=tcontmp;
        tcon=tdontmp;
        tdon=taontmp;
    }
    else if (subsector==1)
    {
```

```
            taon=taontmp;
            tbon=tcontmp;
            tcon=tdontmp;
            tdon=tbontmp;
        }
        else if (subsector==2)
        {
            taon=taontmp;
            tbon=tbontmp;
            tcon=tdontmp;
            tdon=tcontmp;
        }
        else if (subsector==3)
        {
            taon=taontmp;
            tbon=tbontmp;
            tcon=tcontmp;
            tdon=tdontmp;
        }
    }
    else if (sector==4)
    {
        if (subsector==0)
        {
            taon=tdontmp;
            tbon=tcontmp;
            tcon=tbontmp;
            tdon=taontmp;
        }
        else if (subsector==1)
        {
            taon=tdontmp;
            tbon=tcontmp;
            tcon=taontmp;
            tdon=tbontmp;
        }
        else if (subsector==2)
        {
            taon=tdontmp;
            tbon=tbontmp;
            tcon=taontmp;
            tdon=tcontmp;
        }
        else if (subsector==3)
```

```
        {
            taon=tcontmp;
            tbon=tbontmp;
            tcon=taontmp;
            tdon=tdontmp;
        }
    }

    else if (sector==5)
    {
        if (subsector==0)
        {
            taon=tdontmp;
            tbon=tbontmp;
            tcon=tcontmp;
            tdon=taontmp;
        }
        else if (subsector==1)
        {
            taon=tdontmp;
            tbon=taontmp;
            tcon=tcontmp;
            tdon=tbontmp;
        }
        else if (subsector==2)
        {
            taon=tdontmp;
            tbon=taontmp;
            tcon=tbontmp;
            tdon=tcontmp;
        }
        else if (subsector==3)
        {
            taon=tcontmp;
            tbon=taontmp;
            tcon=tbontmp;
            tdon=tdontmp;
        }
    }

    else if (sector==6)
    {
        if (subsector==0)
        {
```

```
            taon=tcontmp;
            tbon=tdontmp;
            tcon=tbontmp;
            tdon=taontmp;
        }
        else if (subsector==1)
        {
            taon=tcontmp;
            tbon=tdontmp;
            tcon=taontmp;
            tdon=tbontmp;
        }
        else if (subsector==2)
        {
            taon=tbontmp;
            tbon=tdontmp;
            tcon=taontmp;
            tdon=tcontmp;
        }
        else if (subsector==3)
        {
            taon=tbontmp;
            tbon=tcontmp;
            tcon=taontmp;
            tdon=tdontmp;
        }
    }

    EvbRegs.CMPR4 = taon;
    EvbRegs.CMPR5 = tbon;
    EvbRegs.CMPR6 = tcon;
    EvaRegs.CMPR3 = tdon;
}

#include "DSP281x_Device.h"         // DSP281x Headerfile Include File
#include "DSP281x_Examples.h"      // DSP281x Examples Include File
// ADC start parameters
#define ADC_MODCLK      0x3         // HSPCLK = SYSCLKOUT/2*ADC_MODCLK2 = 150/(2*3)      = 25MHz
#define ADC_CKPS        0x1         // ADC module clock = HSPCLK/2*ADC_CKPS    = 25MHz/(1*2) = 12.5MHz
#define ADC_SHCLK       0xf         // S/H width in ADC module periods = 16 ADC clocks
//#define AVG             1000    // Average sample limit
```

```
#define ZOFFSET        0x00    // Average Zero offset
#define BUF_SIZE      200    // Sample buffer size
extern int16 sine;
// Global variable for this example
//Uint16 SampleTable0[BUF_SIZE];
int16 SampleTable1[BUF_SIZE];
int16 SampleTable2[BUF_SIZE];
//Uint16 SampleTable3[BUF_SIZE];
int16 SampleTable3[BUF_SIZE];
//Uint16 SampleTable5[BUF_SIZE];
//Uint16 SampleTable6[BUF_SIZE];
//Uint16 SampleTable7[BUF_SIZE];
//Uint16 SampleTable8[BUF_SIZE];
//Uint16 SampleTable9[BUF_SIZE];
Uint16 ad_index=0;
Uint16 ad_index2=0;
Uint16 cap6_flag_old=0;
#define ADC_usDELAY    8000L
#define ADC_usDELAY2 20L

int16 acq_a0=0;
int16 acq_a1=0;
int16 acq_b0=0;
int16 acq_b1=0;
int16 acq_c0=0;
int16 acq_c1=0;

int16 acq_a0_2=0;
int16 acq_a1_2=0;
int16 acq_b0_2=0;
int16 acq_b1_2=0;
int16 acq_c0_2=0;
int16 acq_c1_2=0;

//global variables
Uint16    delay_counter=0;
Uint16    t3interruptflag=0;
Uint16    adcfinishflag=0;
Uint16    capcount=0;     //provide the pll information,0 means 0 ,399 means
360
Uint16    va_crozero_flag=0;    //when it is set the capcount return to 0
Uint16    enableflag=0;
Uint16    vdc_ad=0;
Uint16    va_ad=0;
```

```
Uint16    vb_ad=0;
Uint16    vc_ad=0;
Uint16    vasign=0;
Uint16    vbsign=0;
Uint16    vcsign=0;
Uint16    phaseb_index=0;
Uint16    phasec_index=0;
extern Uint16 icasign;
extern Uint16 icbsign;
extern Uint16 iccsign;
extern int16    cosine;
extern int16    sine;
extern Uint16 ilasign;
extern Uint16 ilbsign;
extern Uint16 ilcsign;
extern int32 outputd5buffer[3];
extern int32 inputd5buffer[3];
extern int32 outputd7buffer[3];
extern int32 inputd7buffer[3];
extern int32 outputq5buffer[3];
extern int32 inputq5buffer[3];
extern int32 outputq7buffer[3];
extern int32 inputq7buffer[3];

extern Uint16 cosine_index;
Uint16    phase_index=0; //this is the index of the sin&cos tab
Uint16    cap6_flag=0; //to indentify whether the cap6 detects a rising edge
Uint16    t4cnt_tmp=0; //store the value of the t4 cnt

#define ADS8364_base    0x80000

// Prototype statements for functions found within this file.
interrupt void evb_timer3_isr(void);
void init_eva_timer1(void);
void init_eva_timer2(void);
void init_evb_timer3(void);
void Gpio_select(void);
void InitAdc(void);

// Global counts used in this example
Uint32    EvbTimer3InterruptCount;

void delayn(Uint16 n)
{ while(n--);
```

```
}
void delayad(Uint16 n)
{ while(n--);
}

void main(void)
{

    Uint16 i=0;
    InitSysCtrl();
    InitGpio();
    DINT;
    InitPieCtrl();
    IER = 0x0000;
    IFR = 0x0000;
    InitPieVectTable();
    EALLOW;
    SysCtrlRegs.HISPCP.all = ADC_MODCLK;
    EDIS;
    InitAdc();  // For this example, init the ADC
    AdcRegs.ADCTRL1.bit.ACQ_PS = ADC_SHCLK;
    AdcRegs.ADCTRL3.bit.ADCCLKPS = ADC_CKPS;
    AdcRegs.ADCTRL1.bit.SEQ_CASC = 1;            // 1    Cascaded mode
    AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 0x6;
    AdcRegs.ADCCHSELSEQ1.bit.CONV01 = 0x1;
    AdcRegs.ADCCHSELSEQ1.bit.CONV02 = 0x3;
    AdcRegs.ADCCHSELSEQ1.bit.CONV03 = 0x4;
    AdcRegs.ADCTRL1.bit.CONT_RUN = 1;
    AdcRegs.ADCMAXCONV.bit.MAX_CONV1 = 0x3;
    init_eva_timer1();
    init_eva_timer2();
    init_evb_timer3();
    EvbTimer3InterruptCount = 0;
    PieCtrlRegs.PIEIER4.all = M_INT6;
    IER |= M_INT4;
    EINT;   // Enable Global interrupt INTM
    ERTM;   // Enable Global realtime interrupt DBGM
    AdcRegs.ADCTRL2.all = 0x2000;
    GpioDataRegs.GPACLEAR.bit.GPIOA1=1;   //CLEAR   THE   PWM2
OUTPUT
    delayn(300); //can be modified
    GpioDataRegs.GPASET.bit.GPIOA1=1;//SET THE PWM2 OUTPUT
    delayn(300); //can be modified
    outputd5buffer[0]=0;
```

```
    outputd5buffer[1]=0;
    outputd5buffer[2]=0;
    inputd5buffer[0]=0;
    inputd5buffer[1]=0;
    inputd5buffer[2]=0;
    outputd7buffer[0]=0;
    outputd7buffer[1]=0;
    outputd7buffer[2]=0;
    inputd7buffer[0]=0;
    inputd7buffer[1]=0;
    inputd7buffer[2]=0;
    outputq5buffer[0]=0;
    outputq5buffer[1]=0;
    outputq5buffer[2]=0;
    inputq5buffer[0]=0;
    inputq5buffer[1]=0;
    inputq5buffer[2]=0;
    outputq7buffer[0]=0;
    outputq7buffer[1]=0;
    outputq7buffer[2]=0;
    inputq7buffer[0]=0;
    inputq7buffer[1]=0;
    inputq7buffer[2]=0;
//the default value of the mux control pin
    GpioDataRegs.GPFSET.bit.GPIOF10=1;
    GpioDataRegs.GPFSET.bit.GPIOF12=1;
    GpioDataRegs.GPGSET.bit.GPIOG4=1;
    GpioDataRegs.GPFCLEAR.bit.GPIOF6=1;
    GpioDataRegs.GPFSET.bit.GPIOF4=1;
    GpioDataRegs.GPFSET.bit.GPIOF8=1;
    while (1)
    {
        if ((adcfinishflag==1)&&(enableflag==1))
        {
                process(); //it will finish the function of the apf ;
                adcfinishflag=0;
        }
        else
        {
          asm("nop;");
        }

    }
}
```

```
interrupt void evb_timer3_isr(void)
{
     EvaRegs.T1CNT = EvbRegs.T3CNT;
    delay_counter++;
    cap6_flag=GpioDataRegs.GPBDAT.bit.GPIOB10;

  if ((cap6_flag==1)&&(cap6_flag_old==0))
  {
     if (delay_counter>=190)
    {
    enableflag=1;    //this is the whole start of the program
     ad_index++;      //test
          if (ad_index==200)
              {
                 ad_index=0;
              }

     EvbRegs.T4CNT = 0x0000;
     t4cnt_tmp=0;
     delay_counter=0;
   }
   else
   {;}
  }
  else
  {
    t4cnt_tmp=EvbRegs.T4CNT;
  }

  EvbRegs.T4CNT = 0x0;
  t4cnt_tmp=0x0;
  delay_counter=0;
  }

  cap6_flag_old=GpioDataRegs.GPBDAT.bit.GPIOB10;
  phase_index=t4cnt_tmp>>3;
  if (phase_index>=484)
  {
   phase_index=483;
  }
  phaseb_index=phase_index+322;
  phasec_index=phase_index+161;
  GpioDataRegs.GPACLEAR.bit.GPIOA1=1;      //CLEAR      THE      PWM2
```

```
OUTPUT
   delayn(100); //can be modified

   GpioDataRegs.GPASET.bit.GPIOA1=1;//SET THE PWM2 OUTPUT
   EvaRegs.T2PR = 0xf;              // Period
   EvaRegs.T2CMPR = 0x7;          // Compare Reg
   EvaRegs.T2CNT = 0x0000;
   EvaRegs.GPTCONA.all = 0x48;
   EvaRegs.T2CON.all = 0x1042;
   acq_a0 = *(unsigned volatile int *)(ADS8364_base+0);
   acq_a1 = *(unsigned volatile int *)(ADS8364_base+1);
   acq_b0 = *(unsigned volatile int *)(ADS8364_base+2);
   acq_b1 = *(unsigned volatile int *)(ADS8364_base+3);
   acq_c0 = *(unsigned volatile int *)(ADS8364_base+4);
   acq_c1 = *(unsigned volatile int *)(ADS8364_base+5);
   while (AdcRegs.ADCST.bit.INT_SEQ1== 0) {} // Wait for interrupt
   asm(" RPT #11 || NOP");
   AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1;
   vdc_ad=((AdcRegs.ADCRESULT0>>4) );
   acq_a0_2=((AdcRegs.ADCRESULT1>>4) );
   acq_a1_2=((AdcRegs.ADCRESULT2>>4) );
   acq_b0_2=((AdcRegs.ADCRESULT3>>4) );
   adcfinishflag=1;
   EvbRegs.EVBIFRA.all = BIT9;
   PieCtrlRegs.PIEACK.all |= PIEACK_GROUP4;
}

void    InitGpio(void)
{
       Uint16 var2;
       Uint16 var3;
       var2= 0x0000;          // sets GPIO DIR as inputs
       var3= 0x0002;
       EALLOW;
      GpioMuxRegs.GPAMUX.bit.PWM1_GPIOA0=0; //pwm1 is used as 1o,
      GpioMuxRegs.GPAMUX.bit.PWM2_GPIOA1=0;
      GpioMuxRegs.GPAMUX.bit.PWM3_GPIOA2=0; //pwm3 is used as io
      GpioMuxRegs.GPAMUX.bit.PWM4_GPIOA3=0;
      GpioMuxRegs.GPAMUX.bit.PWM5_GPIOA4=1;
      GpioMuxRegs.GPAMUX.bit.PWM6_GPIOA5=1;
      GpioMuxRegs.GPAMUX.bit.T1PWM_GPIOA6=0;
      GpioMuxRegs.GPAMUX.bit.T2PWM_GPIOA7=1;      //provide    the    bit
signal
      GpioMuxRegs.GPAMUX.bit.CAP1Q1_GPIOA8=0; //test the polarity of va
```

```
    GpioMuxRegs.GPAMUX.bit.CAP2Q2_GPIOA9=0; //test the polarity of vb
    GpioMuxRegs.GPAMUX.bit.CAP3QI1_GPIOA10=0;   //test the polarity
of vc
    GpioMuxRegs.GPAMUX.bit.TDIRA_GPIOA11=0;
    GpioMuxRegs.GPAMUX.bit.TCLKINA_GPIOA12=0;
    GpioMuxRegs.GPAMUX.bit.C1TRIP_GPIOA13=0;
    GpioMuxRegs.GPAMUX.bit.C2TRIP_GPIOA14=0;
    GpioMuxRegs.GPAMUX.bit.C3TRIP_GPIOA15=0;

    GpioMuxRegs.GPBMUX.all=0x003f;
    GpioMuxRegs.GPDMUX.all=0x0000;
    GpioMuxRegs.GPEMUX.all=0x0000;
    GpioMuxRegs.GPFMUX.all=0x0000;
    GpioMuxRegs.GPGMUX.all=0x0000;

     GpioMuxRegs.GPADIR.all=0x0002;
     GpioMuxRegs.GPBDIR.all=var2;          // GPIO DIR select GPIOs as
input
     GpioMuxRegs.GPDDIR.all=var2;
     GpioMuxRegs.GPEDIR.all=var2;
     GpioMuxRegs.GPFDIR.all=0x1550;
     GpioMuxRegs.GPGDIR.all=0x0010;

     GpioMuxRegs.GPAQUAL.all=var3;          // Set GPIO input qualifier
values
     GpioMuxRegs.GPBQUAL.all=var3;
     GpioMuxRegs.GPDQUAL.all=var3;
     GpioMuxRegs.GPEQUAL.all=var3;

     GpioDataRegs.GPACLEAR.all=0xffff;
     GpioDataRegs.GPBCLEAR.all=0xffff;
     GpioDataRegs.GPDCLEAR.all=0xffff;
     GpioDataRegs.GPECLEAR.all=0xffff;
     GpioDataRegs.GPFCLEAR.all=0xffff;
     GpioDataRegs.GPFCLEAR.all=0xffff;
     EDIS;
}

void init_eva_timer1(void)
{
     EvaRegs.T1PR = 0x04e2;          // Period
     EvaRegs.T1CNT = 0x0000;
     EvaRegs.ACTRA.all = 0x0600;
     EvaRegs.CMPR3 = 0x0400;
```

```
    EvaRegs.DBTCONA.all = 0x0fe4; // enable deadband,x/8.and the multifier
is 8
    EvaRegs.COMCONA.all = 0x8600;
    EvaRegs.T1CON.all = 0x0840;
    EvaRegs.EVAIFRA.all=0xFFFF ;//clear the flag bit of ev interrupt register
    EvaRegs.EVAIFRB.all=0xFFFF ;//clear the flag bit of ev interrupt regi
    EvaRegs.EVAIFRC.all=0xFFFF ;//cle


    EvaRegs.EVAIMRA.all=0x0000;                 //DISABLE    ALL    THE
INTERRUPT OF EVA 1
    EvaRegs.EVAIMRB.all=0x0000;
    EvaRegs.EVAIMRC.all=0x0000;
}

void init_eva_timer2(void)
{
    EvaRegs.T2PR = 0x1f;            // Period
    EvaRegs.T2CMPR = 0xf;           // Compare Reg
    EvaRegs.T2CNT = 0x0000;
    EvaRegs.GPTCONA.all = 0x48;
    EvaRegs.T2CON.all = 0x1042;
}

void init_evb_timer3(void)
{
  EvbRegs.GPTCONB.all = 0;
  EvbRegs.T3PR = 0x04e2;            // Period
  EvbRegs.EVBIMRA.bit.T3UFINT = 1;
  EvbRegs.EVBIFRA.bit.T3UFINT = 1;
  EvbRegs.T3CNT = 0x0000;
  EvbRegs.ACTRB.all = 0x0666;

  EvbRegs.CMPR4 = 0x0100;
  EvbRegs.CMPR5 = 0x0300;
  EvbRegs.CMPR6 = 0x0200;
  EvaRegs.CMPR3 = 0x0400;

  EvbRegs.DBTCONB.all = 0x0fe4; // enable deadband,x/8.and the multifier is
8
  EvbRegs.COMCONB.all = 0x8600;

  EvbRegs.T4PR = 0xFFFF;                            // Set up timer period
  EvbRegs.T4CNT = 0x0000;
```

```
   EvbRegs.CAPCONB.all=0x1404;
   EvbRegs.CAPFIFOB.all = 0x0000;
   EvbRegs.T3CON.all = 0x0840;
   EvbRegs.T4CON.all = 0x1740;
   EvaRegs.EVAIFRA.all=0xFFFF ;//clear the flag bit of ev interrupt register
   EvaRegs.EVAIFRB.all=0xFFFF ;//clear the flag bit of ev interrupt regi
   EvaRegs.EVAIFRC.all=0xFFFF ;//cle
   EvaRegs.EVAIMRA.all=0x0000;       //DISABLE ALL THE INTERRUPT
OF EVA 1
   EvaRegs.EVAIMRB.all=0x0000;
   EvaRegs.EVAIMRC.all=0x0000;
}
// This function initializes ADC to a known state.
void InitAdc(void)
{
     AdcRegs.ADCTRL3.bit.ADCBGRFDN = 0x3; //          Power          up
bandgap/reference circuitry
     delayad(10000);                        // Delay before powering up rest of
ADC
     AdcRegs.ADCTRL3.bit.ADCPWDN = 1;        // Power up rest of ADC
     delayad(10000);               // Delay after powering up ADC
}
```