INTEGRATED ON-CHIP INDUCTORS FOR RADIO FREQUENCY CMOS CIRCUITS

SUBMITTED BY

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CERTIFICATE OF ORIGINALITY

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Abstract

The project is concerned with the study of integrated on-chip inductors for RF CMOS circuits. On-chip inductors were fabricated and characterized using standard 0.6μm CMOS process with 3 metal layers. The research is targeted on the optimization of on-chip inductors by varying the layout parameters including metal width, metal layer topology and number of turns. Planar (1 metal layer), 3D (3 metal layers) and stacked (2 metal layers) inductor structures were investigated. The scattering parameters of the samples were measured by a network analyzer up to 10 GHz. The effective resistance, effective inductance and quality factor were then extracted from the *S* parameters. The results were verified by numerical simulation with MicroWave Office software. Simulation was used to study the performance of the samples after the Si substrate was removed by etching.

Our results show that inductors with different metal widths have optimum Q factor at different operation frequencies. The inductor with wider metal width benefits at lower frequencies. On the other hand, the inductor with narrower metal width has comparatively lower effective resistance at higher frequencies. This is the consequence of combined skin and proximity effects in the metal lines and the eddy current loss in the substrate. In addition, it is found that after the substrate removal the planar inductor has the largest improvement in Q factor. The proximity effect from adjacent metal layers limits the performance of the 3D and stacked back-etched inductors as compared with the planar inductor.

Different topologies of the 2-layer stacked inductors have been studied. The result proves that the proximity effect from adjacent metal layers acts as a major loss affecting the Q factor of this type of inductor. Further interlayer distance leads to further increase of Q factor. Simulation shows that the substrate eddy current loss in stacked inductors plays a minor role because of the reduced size.

Comparing the three types of inductors, it is found that the back-etched planar inductor has the highest Q factor. It suffers from least proximity effect from adjacent metal lines after etching of the substrate. The drawback is its large size. The 3D inductor has comparatively high Q factor as well as small inductor size. It also has the highest peak Q frequency and self-resonant frequency.

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Acronyms

RF	Radio frequency
IC	Integrated circuit
CMOS	Complementary metal-oxide-semiconductor
PCB	Printed circuit board
CAD	Computer-aided design
MMIC	Monolithic microwave integrated circuit
3D	Three dimensional
EM	Electromagnetics

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Chapter 1

Introduction

1.1 Introduction

Progress in wireless communication induces great interest in the development of radio transceivers. On-chip passive components like inductors, capacitors and transformers integrated into RF ICs play an important role in minimizing the size of radio transceivers. In this project, on-chip inductors fabricated on CMOS ICs will be studied.

In past years, there has been much progress in the active devices in ICs. The size of the active devices has kept on diminishing, resulting in the development of complex system-on-chips (SOC). But passive devices are still often connected externally on PCBs rather than built on-chip.

Due to the explosive growth of wireless technology, the operation frequency range rises from below 5 MHz to 1 - 10 GHz [1]. The tank inductance value at 100 MHz will be of the order of 100nH, while that at 10GHz will be of the order of 1nH. It is impossible to construct the 1nH inductor externally since the package pin and bond wire inductances almost exceed this value. These lead to great interest in integrated passive devices.

In circuit building blocks, inductors perform an integral role, especially at high frequencies. At low frequencies, inductors can be replaced by simulated inductors using gyrator circuit principles. On the other hand, the simulated inductors are difficult to realize as active device gain drops at high frequencies. Also, they have finite dynamic range, require extra voltage headroom to operate, and import additional noise into the circuits. The limitations restrict their application, especially in highly sensitive performance.

In this project, passive inductors formed by spirals in the metallization layers in CMOS ICs will be investigated. In this Chapter, a brief introduction on the on-chip inductors and the related parameters will be given. Chapter 2 presents a short literature review on the past researches. In Chapter 3, the methodology of experimental processes and simulation will be described. Chapter 4 presents and discusses the results measured. The last chapter gives the conclusion on this project and suggestions for future work.

1.2 Applications of Inductors

Fig. 1.1 shows some common applications of inductors together with capacitors in wireless circuits. In Fig. 1.1(a), an inductor is used as a series-feedback element that increases the input impedance, stabilizes the gain, and lowers the non-linearity of the amplifier. The inductor has more benefits in consuming less voltage headroom and less injection of extra noise into the circuit compared with using a resistor. Real input impedance can be also obtained by the inductance at a particular frequency, hence

providing an impedance match to the amplifier.

Fig. 1.1(b) shows a LC tuned load used to replace a resistive load at high frequency operation. It benefits from less noise, less voltage headroom and larger impedance at high frequencies. In addition, the LC load also tunes the centre frequency of the oscillator and minimizes power injection from the driving transistor.

Fig. 1.1(c) shows inductors and capacitors functioning as a low-pass filter. Performance of this filter is better than that of other active filters due to its high operation frequencies, high dynamic range by the intrinsic linearity of the passive devices, and less injection noise.

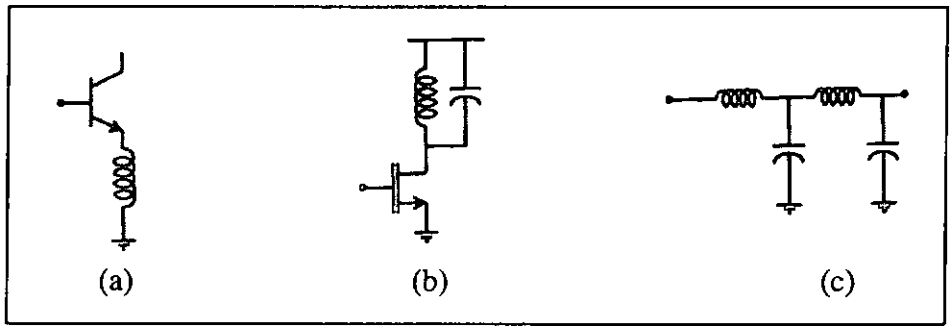


Figure 1.1. Some applications of inductors in IC building blocks [1]. (a) Series-feedback element. (b) Tuned load. (c) Low-pass filter.

1.3 Monolithic Inductor Realizations

There are several parameters that will affect the inductance and other characteristics of an on-chip spiral inductor. They can be classified as

design-controlled parameters and process-controlled parameters [1].

Design-controlled parameters include

- Number of turns, N
- Metal width, w
- Spacing between two adjacent metals, s
- Inductor shape
- Side length, ℓ
- Outer and inner diameter, d_{out} and d_{in}

Usually, the fill ratio, defined as $\frac{d_{out}-d_{in}}{d_{out}+d_{in}}$, is used instead of the outer and inter diameters. These parameters, which affect the construction of the inductor, can also be called "lateral" parameters. Meanwhile, process-controlled parameters will be controlled during the fabrication process. These can be also called "vertical" parameters, like

- Metal thickness t_{met}
- Oxide thickness t_{ox}
- Metal resistivity ρ_{met}
- Substrate resistivity ρ_{sub}
- Number of metal layers

Fig. 1.2 shows some of parameters of the on-chip inductor. These lateral and vertical parameters of the spiral inductor can be used to determine the inductance and

other parasitic elements, such as

- Metal line resistance, R_s

- Metal-to-substrate capacitance, C_{ox}

- Substrate loss R_{sub}

This issue is addressed in a later section.

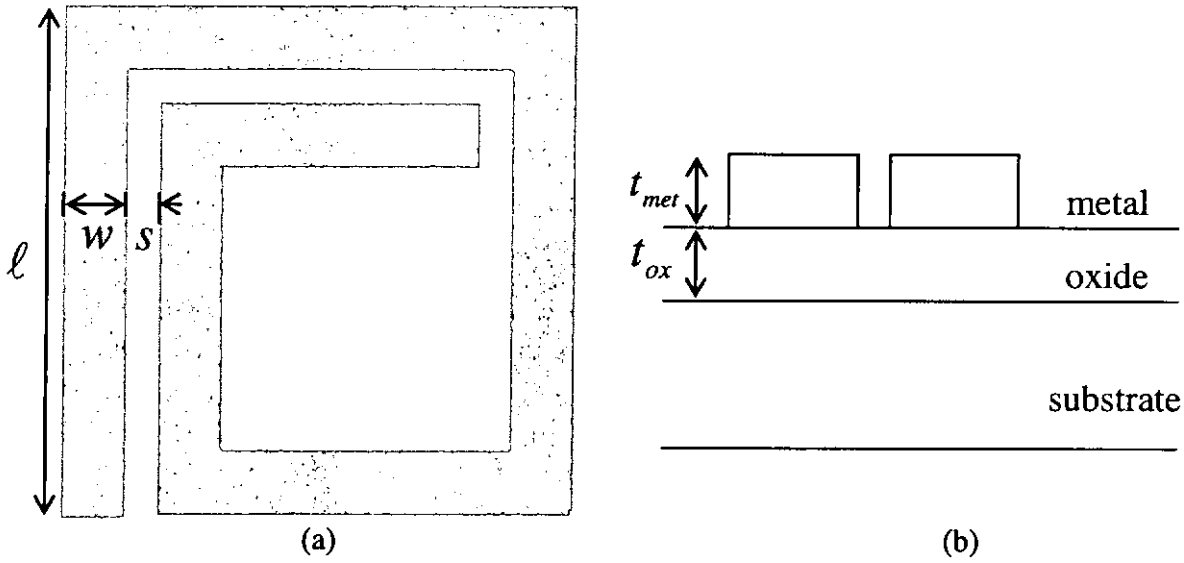


Figure 1.2. Some layout parameters of an on-chip inductor. (a) Top view. (b) Cross-section view.

Traditionally, spiral inductors are often in square form due to its ease of design and support from drawing tools. Although the most optimum pattern is a circular spiral form because it suffers less resistive and capacitive loss, only a few commercial layout tools support circular drawing feature. Hexagonal and octagonal structures are the other choices which are approximate to the circular structure but easier to construct and supported by most CAD tools.

1.4 Inductor Models

There are three extraction techniques that are used to develop inductor models [2]. They are EM solvers, distributed models and lumped circuit models.

The EM solvers are the most accurate tools to model inductors. The method depends on the numerical solution of Maxwell's equations by applying appropriate boundary conditions. However, the drawback is that the simulation time is too long for each simulation.

The second approach models each metal segment of the spiral inductor as an individual transmission line network, therefore forming a distributed model for the entire inductor. Fig. 1.3 shows a four-section distributed inductor model including all parasitic inductive and capacitive coupling elements [2]. However, it is still time consuming and complex in handling the resulting model. The simulation time greatly increases due to the size of the multi-turn polygon structure.

Most circuit designers prefer the last approach namely, the lumped model where the spiral inductor is represented by an equivalent π-network with the inductance L_s in series with a resistance R_s and parasitic losses shunted to ground. The model is shown in Fig. 1.4 C_f is the parasitic capacitance between metal segments; C_{ox1}, C_{ox2} are oxide capacitances between metal layers and Si substrate; C_{sub1}, C_{sub2} are capacitances of the Si substrate; R_{sub1}, R_{sub2} are the resistance of the Si substrate. The benefit of this model is its short simulation time together with an acceptable accuracy.

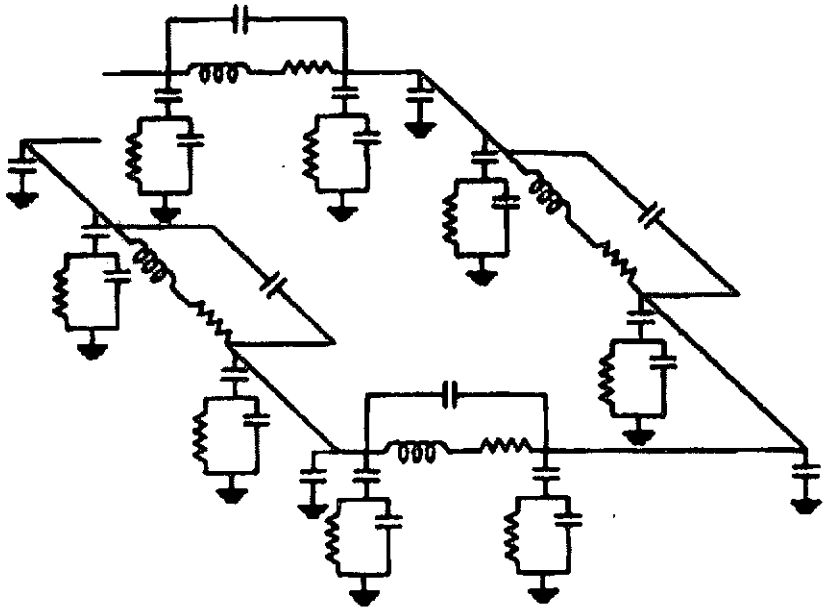


Figure 1.3. 4-section distributed inductor model [1].

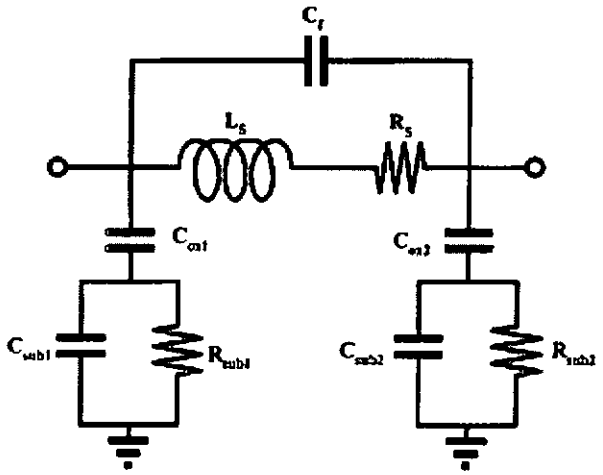


Figure 1.4. Lumped model for a monolithic inductor [1].

1.5 Inductance

1.5.1 Self-Inductance Calculation

The self-inductance L_i of the metal line in i-th segment can be calculated by the Greenhouse's method in [3]

$$L_i = 0.2\ell_i\left[\ln\left(\frac{2\ell_i}{GMD}\right) - 1.25 + \frac{AMD}{\ell_i} + \frac{\mu}{4}T\right] \ \mu\text{H} \qquad (1.1)$$

where ℓ_i is the metal length in i-th segment in meters. *GMD* and *AMD* represent the geometric and arithmetic mean distances of the metal cross section. μ is the metal permeability, and T is a frequency-correction parameter. *GMD* of the metal cross section [4] is equal to $0.2235(w+t)$, where w and t are the metal width and thickness, respectively. In case of a single metal cross section, the *AMD* of the metal line equals the average of distances between all possible pairs of points within the cross section, which can be written as $\frac{(w+t)}{3}$. The magnetic permeability of the metal is 1 and the T in (1.1) for microwave frequencies should also be 1. Therefore, (1.1) can be reduced to

$$L_i = 0.2\ell_i\left[\ln\left(\frac{2\ell_i}{w+t}\right) + 0.5 + \frac{w+t}{3\ell_i}\right] \ \mu\text{H} \qquad (1.2)$$

Fig. 1.5 shows a conventional three-turn spiral inductor which has 12 metal

segments. The total self-inductance L_0 of the inductor is $L_1 + L_2 + L_3 + ... + L_{12}$.

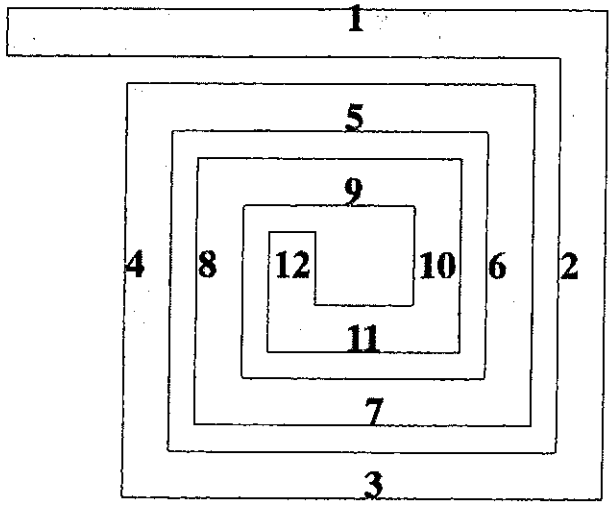


Figure 1.5. 3-turn spiral inductor.

1.5.2 Mutual Inductance Calculation

Mutual inductances between the metal segments also contribute to the total inductance of the inductor. Mutual inductance between two conductors is caused by the phenomenon that a current flowing in another nearby conductor induces a current flow in a conductor. For two parallel conductors, A and B, the mutual inductances between the two conductors are

$$M_{A,B} = \frac{d\phi_{A,B}}{di_A} \quad (1.3) \qquad \text{and} \qquad M_{B,A} = \frac{d\phi_{B,A}}{di_B} \quad (1.4)$$

where $\phi_{A,B}$ is the flux generated by current in conductor A, i_A, linking conductor B.

$\phi_{B,A}$ is the flux generated by current in conductor B, i_B, linking conductor A.

The mutual inductances between any two parallel metal segments of an inductor can be expressed as

$$M_{i,j} = 0.2\ell\left[\ln\left(\frac{\ell}{d_{i,j}} + \sqrt{1+\frac{\ell^2}{d_{i,j}^2}}\right) - \sqrt{1+\frac{d_{i,j}^2}{\ell^2}} + \frac{d_{i,j}}{\ell}\right] \ \mu\text{H} \qquad (1.5)$$

where ℓ is the length of both metal lines, $d_{i,j}$ is the distance between the centers of two segments [5]. For any two segments where the currents are flowing in the same direction, their mutual inductances are positive. On the other hand, the opposite flowing currents will lead to negative mutual inductance. The mutual inductances between two segments should be the same, i.e. $M_{i,j} = M_{j,i}$.

For the above three-turn inductor, the total positive mutual inductance, M_+ is

$$\begin{aligned} M_+ = 2(&M_{1,5} + M_{1,9} + M_{2,6} + M_{2,10} + M_{3,7} + M_{3,11} + M_{4,8} \\ &+ M_{4,12} + M_{5,9} + M_{6,10} + M_{7,11} + M_{8,12}) \end{aligned} \qquad (1.6)$$

The total negative mutual inductance, M_- is

$$\begin{aligned} M_- = 2(&M_{1,3} + M_{1,7} + M_{1,11} + M_{5,3} + M_{5,7} + M_{5,11} + M_{9,3} + M_{9,7} + M_{9,11} \\ &+ M_{2,4} + M_{2,8} + M_{2,12} + M_{6,4} + M_{6,8} + M_{6,12} + M_{10,4} + M_{10,8} + M_{10,12}) \end{aligned} \qquad (1.7)$$

1.5.3 Total Inductance Calculation

The general equation for the total inductance is

$$L_T = L_0 + \sum M \tag{1.8}$$

where L_T is the total inductance, and $\sum M$ is the sum of all the mutual inductances. From the expanded Grover formula given in [3], the total inductance of an on-chip square spiral inductor can be rewritten to

$$L_T = L_0 + M_+ - M_- \tag{1.9}$$

By (1.9), the total inductance of the 3-turn inductor shown in Fig 1.5 is

$$\begin{aligned} L_T &= L_1 + L_2 + L_3 + L_4 + L_5 + L_6 + L_7 + L_8 + L_9 + L_{10} + L_{11} + L_{12} \\ &+ 2(M_{1,5} + M_{1,9} + M_{2,6} + M_{2,10} + M_{3,7} + M_{3,11} + M_{4,8} \\ &+ M_{4,12} + M_{5,9} + M_{6,10} + M_{7,11} + M_{8,12}) \\ &- 2(M_{1,3} + M_{1,7} + M_{1,11} + M_{5,3} + M_{5,7} + M_{5,11} + M_{9,3} + M_{9,7} + M_{9,11} \\ &+ M_{2,4} + M_{2,8} + M_{2,12} + M_{6,4} + M_{6,8} + M_{6,12} + M_{10,4} + M_{10,8} + M_{10,12}) \end{aligned} \tag{1.10}$$

An analytical inductance of a planar inductor can be found by the above calculation. There are also other simple empirical approaches. Ronkainen derived a semi-empirical expression for the inductance of rectangular inductors [6]:

$$L = 1.5\mu_0 N^2 \ell e^{-\frac{3.7(N-1)(w+s)}{\ell}} \left(\frac{\ell}{w}\right)^{0.1} \tag{1.11}$$

Jenei has also presented a closed-form inductance expression for compact modeling of integrate inductors [7]. His formula to estimate the inductance is

$$L=\frac{\mu_0}{2\pi}\ell\left(\ln\frac{\ell}{w+t}-0.2-0.447N+(N-1)\cdot\left(\begin{array}{l}\ln\left(\sqrt{1+\left(\frac{\ell}{4Nd^+}\right)^2}+\frac{\ell}{4Nd^+}\right)\\-\sqrt{1+\left(\frac{4Nd^+}{\ell}\right)^2}+\frac{4Nd^+}{\ell}\end{array}\right)\right) \quad (1.12)$$

where d^+ is the average distance corresponding to $(w+s)\frac{(3N-2N_i-1)(N_i+1)}{3(2N-N_i-1)}$ and N_i is the integer part of N.

Lee derived an empirical formula for the inductance of planar inductors with different structures [8].

$$L=\frac{\mu_0 N^2 d_{avg} c_1}{2}\left[\ln\left(\frac{c_2}{\rho}\right)+c_3\rho+c_4\rho^2\right] \quad (1.13)$$

where d_{avg} is the arithmetic mean of the inner and outer diameters, and ρ is the fill ratio. The various c_n coefficients are functions of geometry.

The expanded Grover formula is the most accurate mathematical equation to find the inductance of an on-chip inductor and eqn. (1.10) can also be applied to all kinds

of inductor structure. The equation, however, will be more complicated when the structure becomes more complex. Comparing to eqn. (1.10), eqns. (1.11) - (1.13) is simpler, so the inductance can be found by just substituting the layout parameters to the equations. The discrepancy between mathematical and experimental inductance reported of eqns. (1.11) and (1.13) is around 2 - 4% and that of eqn. (1.12) is less than 2 %.

1.6 Scattering Parameters (*S* Parameters)

1.6.1 Definition

Fig. 1.6 shows the voltages and currents in a two-port network. The parameters set used to characterize the performance of the network is related to a set of four variables, two of which represent the excitation of the network and the remaining two represent the response of the network to the excitation. Scattering parameters, which are commonly called *S* parameters, involve the traveling waves that are scattered or reflected when a network is inserted into a transmission line.

At radio-frequency range, it is hard to measure voltage, current or impedance in a direct manner. On the other hand, *S* parameters which represent the voltage reflection coefficient and transmission gain can be readily measured and converted to more familiar network parameters.

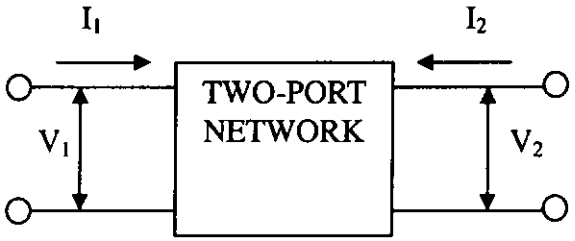


Figure 1.6. General two-port network.

To derivate S parameters, a new set of variables (a_i, b_i) is used [9]. The variables a_i and b_i are normalized complex voltage wave incident on and reflected from the i^{th} port of the network. For a two-port network shown in Fig. 1.6, the definition of the variables (a_1, a_2, b_1, b_2) in terms of the terminal voltage (V_1, V_2), the terminal current (I_1, I_2), and a reference impedance (Z_0) is shown as follows:

$$a_1 = \frac{V_1 + I_1 Z_0}{2\sqrt{Z_0}} = \frac{V_{i1}}{\sqrt{Z_0}} \quad (1.14)$$

$$a_2 = \frac{V_2 + I_2 Z_0}{2\sqrt{Z_0}} = \frac{V_{i2}}{\sqrt{Z_0}} \quad (1.15)$$

$$b_1 = \frac{V_1 - I_1 Z_0}{2\sqrt{Z_0}} = \frac{V_{r1}}{\sqrt{Z_0}} \quad (1.16)$$

$$b_2 = \frac{V_2 - I_2 Z_0}{2\sqrt{Z_0}} = \frac{V_{r2}}{\sqrt{Z_0}} \quad (1.17)$$

where V_{i1} and V_{i2} are the incident voltages on port 1 and 2, and V_{r1} and V_{r2} are the reflected voltages from port 1 and 2, respectively. The linear equations describing the network are then:

$$b_1 = S_{11}a_1 + S_{12}a_2 \quad (1.18)$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \quad (1.19)$$

The S parameters, S_{11}, S_{22}, S_{21} and S_{12} are:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} = \text{Input reflection coefficient with the output port terminated by a match load} \tag{1.20}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} = \text{Output reflection coefficient with the input terminated by a matched load} \tag{1.21}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} = \text{Forward transmission (insertion) gain with the output port terminated in a matched load.} \tag{1.22}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} = \text{Reverse transmission (insertion) gain with the input port terminated in matched load.} \tag{1.23}$$

Notice that

$$S_{11} = \frac{b_1}{a_1} = \frac{\frac{V_1}{I_1} - Z_0}{\frac{V_1}{I_1} + Z_0} = \frac{Z_1 - Z_0}{Z_1 + Z_0} \tag{1.24}$$

then

$$Z_1 = Z_0 \frac{1 + S_{11}}{1 - S_{11}} \tag{1.25}$$

where $Z_1 = \frac{V_1}{I_1}$ is the input impedance at port 1. The coefficients are usually plotted by Smith charts, and the input impedances can be readily derived.

1.6.2 Extraction of Inductor Impedance

The parameters of an inductor can be extracted by two-port S parameters measurements. Fig. 1.6 shows the terminal quantities of a two-port device. The input-output relations at any frequency are

$$V_1(\omega) = A(\omega)V_2(\omega) + B(\omega)[-I_2(\omega)] \tag{1.26}$$

$$I_1(\omega) = C(\omega)V_2(\omega) + D(\omega)[-I_2(\omega)] \tag{1.27}$$

and

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix} \tag{1.28}$$

where A, B, C and D are called $ABCD$ parameters or chain parameters. The measured S parameters can be converted into $ABCD$ matrix and π representation (Fig. 1.6) [10] by

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \frac{\Delta_{1\pm S}}{2S_{21}} & \frac{Z_0\Delta_{1+S}}{2S_{21}} \\ \frac{\Delta_{1-S}}{2Z_0S_{21}} & \frac{\Delta_{1\mp S}}{2S_{21}} \end{bmatrix} = \begin{bmatrix} 1+\frac{Z_2}{Z_3} & Z_2 \\ \frac{1}{Z_1}+\frac{1}{Z_3}\left(1+\frac{Z_2}{Z_1}\right) & 1+\frac{Z_2}{Z_1} \end{bmatrix} \tag{1.29}$$

where
$$\begin{aligned}\Delta_{1+s} &= (1+S_{11})(1+S_{22}) - S_{12}S_{21} \\ \Delta_{1-s} &= (1-S_{11})(1-S_{22}) - S_{12}S_{21} \\ \Delta_{1\pm s} &= (1+S_{11})(1-S_{22}) + S_{12}S_{21} \\ \Delta_{1\mp s} &= (1-S_{11})(1+S_{22}) + S_{12}S_{21}\end{aligned},$$

Z_0 is the reference impedance, Z_1, Z_2 and Z_3 are the branch impedances shown in Fig. 1.7.

Usually the inductor is operated with one of its ports short-circuited [11]-[14]. The two-terminal device can be replaced by a single-ended excitation circuit shown in Fig. 1.8. The input impedance at port 1 becomes the combination of two parallel impedances, Z_1 and Z_2. Z_2 is due to the inductance L_s, the series resistance R_s, and the parasitic capacitance between metal segments C_f. Z_1 is due to the oxide capacitance C_{ox}, and the shunt R-C parasitic elements in the substrate. So the effective impedance of the inductor (with port 2 short-circuited) is

$$Z_{eff} = \frac{Z_1 Z_2}{Z_1 + Z_2} \tag{1.30}$$

$$= R_{eff} + jX_{eff} \tag{1.31}$$

where R_{eff} is the effective resistance, X_{eff} is the effective reactance. The effective inductance L_{eff} and quality factor Q can be found by

$$L_{eff} = \frac{X_{eff}}{2\pi f} \tag{1.32}$$

$$Q = \frac{X_{eff}}{R_{eff}} \tag{1.33}$$

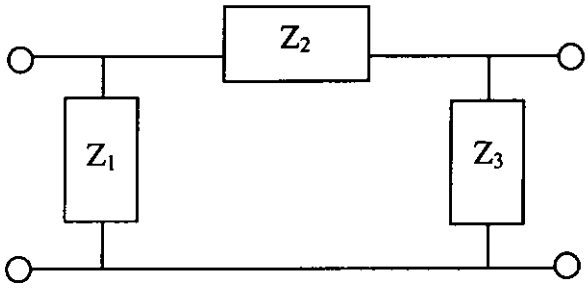


Figure 1.7. two-terminal device with three branch impedances (π representation).

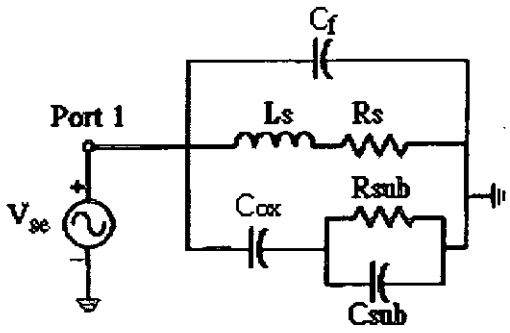


Figure 1.8. Single-ended excitation model.

1.7 Quality Factor Q

The quality factor is an important parameter determining the performance of inductors. Q factor is defined as

$$Q = 2\pi \bullet \frac{energy \quad stored}{energy \quad loss \quad in \quad one \quad oscillation \quad cycle} \tag{1.34}$$

For an inductor, the equation can be rewritten as

$$Q = 2\pi \bullet \frac{peak\ \ magnetic\ \ energy}{energy\ \ loss\ \ in\ \ one\ \ oscillation\ \ cycle} \tag{1.35}$$

There are also popular ways to calculate Q factor by the input admittance (Y_{11}) or input impedance (Z):

$$Q = -\frac{imag(Y_{11})}{real(Y_{11})} \tag{1.36}$$

$$Q = \frac{imag(Z)}{real(Z)} \tag{1.37}$$

The optimization of the Q factor of an inductor is maximizing the magnetic or electromagnetic energy stored in it as well as minimizing the energy dissipation. For an on-chip spiral inductor, at the frequencies, from dc to 15 GHz range, the metal layers as well as the bulk Si substrate play the most important roles in affecting the Q factor [15]. The losses in the inductor include metal losses and substrate losses.

1.8 Self-Resonant Frequency

The self-resonant frequency f_{SR} of the inductor is defined as

$$f_{SR} = \frac{1}{2\pi\sqrt{L_{eq}C_{eq}}} \tag{1.38}$$

where L_{eq} and C_{eq} are the equivalent inductance and capacitance of the structure in series [5]. At self-resonant frequency, X_{eff} in (1.31) is zero. Fig. 1.9 shows a typical graph of Q factor against frequency of an inductor. The Q factor of the inductor will increase with the frequency and has a maximum value at $f = f_{max}$. f_{max} represents the peak Q frequency. Then Q factor will drop due to higher energy dissipation at high frequency operation. The Q factor will continuously fall to zero at the self-resonant frequency. Increasing f_{SR} can increase the frequency band of the device operation.

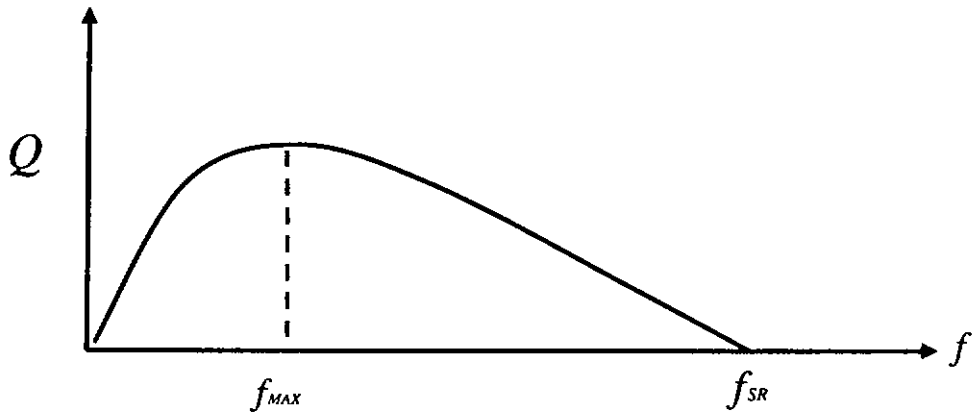


Figure 1.9. Typical Q-f graph of an inductor.

The equivalent inductance can be found by the Greenhouse's method [3] or electromagnetic field solvers. The equivalent capacitance is dependent on the structure of the inductor. It involves the metal-to-metal C_f and metal-to-substrate C_{ox} capacitances. In order to increase f_{SR}, C_f and C_{ox} should be minimized. For a multi-layer inductor, the capacitance between the metal layers will dominate and would be the limitation of f_{SR} [16]-[17].

1.9 Losses in Metal Lines

Losses in metal lines of inductors can be caused by two factors: dc series resistance and non-uniform current distribution by skin and proximity effects.

At low frequencies, the loss of the on-chip inductor is mainly dc resistance of the metal lines. The dc series resistance of each segment is determined by $R_{DC} = \rho \frac{\ell}{w \cdot t}$ and is independent of operating frequency.

At higher frequencies, the current distribution in the metal traces becomes non-uniform due to the eddy currents formed by skin and proximity effects, which increase the effective resistance of the inductor [18]. The magnetic fields penetrating a particular metal segment can be separated into two parts, the self-magnetic field and the neighborhood magnetic fields. At any given frequency, the magnetic field penetrating the metal line produces currents flowing near the surface of the metal. This is called the skin effect. As the frequency increases, the effective cross-section area of the metal line decreases, thus leading to increase of power loss. The skin effect loss is determined by the skin depth δ,

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} \quad \text{(for an infinite metal plane)} \tag{1.39}$$

where ρ is the resistivity, μ is the permeability of the metal. In the proximity

effect, the magnetic fields from the adjacent metal lines penetrate the metal trace. Eddy current loops are produced within the trace as shown in Fig. 1.10. These induced currents add to the excitation current on the inner edge but subtract from the excitation current on the outer edge. Increase of the effective resistance is due to the non-uniform current distribution in the metal trace.

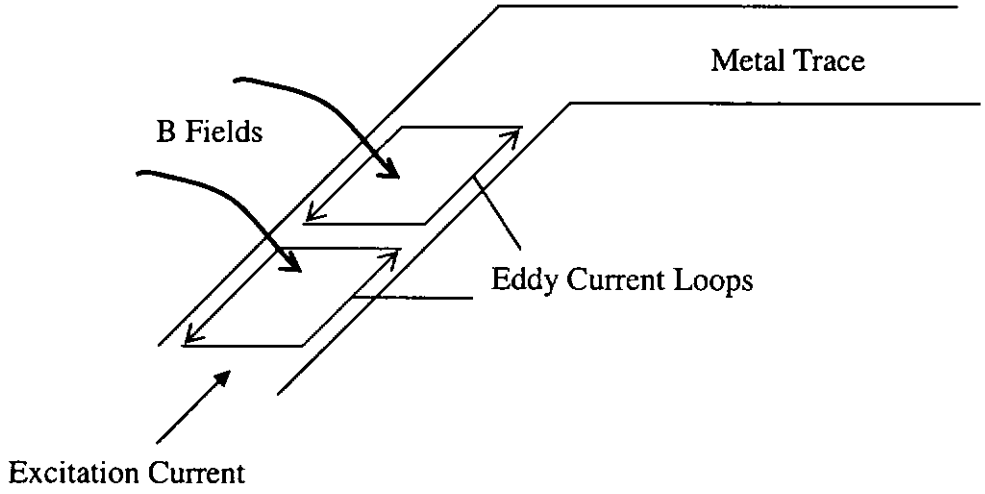


Figure 1.10. Eddy current loops formed in the metal trace [18].

1.10 Substrate Loss

The on-chip inductors are normally built on a conductive Si substrate layer. The substrate losses are mainly due to two mechanisms, the capacitive and inductive coupling.

The capacitive coupling from the bottom metal layer to the substrate through displacement current changes the substrate potential. This displacement current then

flows through around the substrate, and therefore energy is dissipated.

The inductive coupling is formed due to the time-varying magnetic fields penetrating the substrate. They form time varying electrics fields and induce eddy current flow in the substrate.

Fig. 1.11 shows the currents existing in the substrate. The electrically induced currents flow perpendicular to the metal segments while the magnetically induced currents flow parallel to the metal segments. The eddy current loss is usually more important than the displacement current loss at high frequencies.

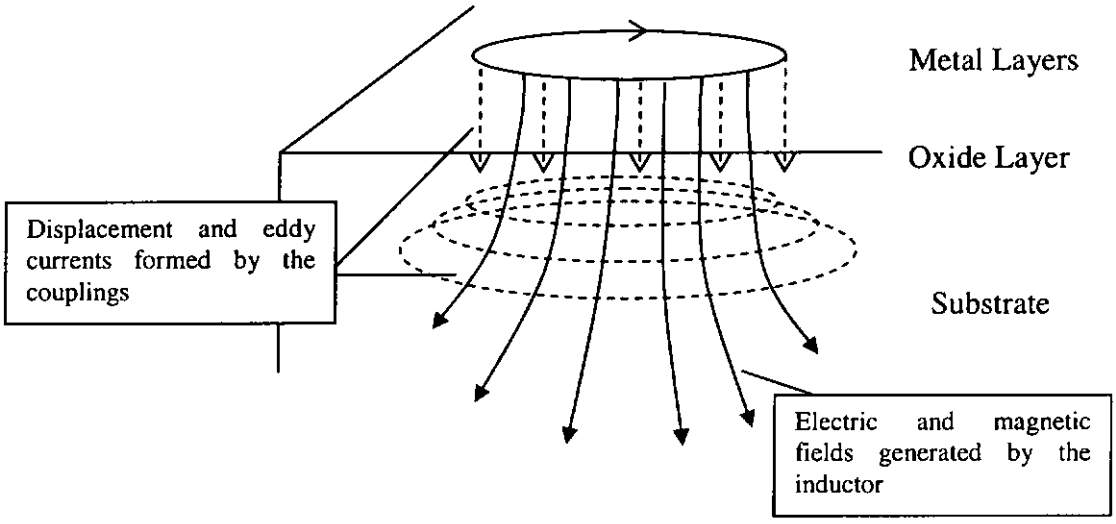


Figure 1.11. Schematic diagram showing the electrically and magnetically induced currents.

Chapter 2

Literature Review

In order to reduce the losses and improve the performance of on-chip inductors, many research efforts have been made in the optimum design of inductor. This chapter will give a brief review on some past researches in this area.

2.1 Fabrication Process

2.1.1 Metal-to-Substrate Spacing

The substrate loss is the major loss of on-chip inductors which operate at a frequency range above gigahertz. There are several methods to reduce the substrate loss in the CMOS process. In early 90s', the pattern of the on-chip inductor used was usually in planar structure. The large area of the spiral structure leaded to large capacitive coupling between the metal turns and the substrate. On way to reduce this coupling is to place the spiral further from the substrate, by using the uppermost metal layer [19-[20]. The capacitance is inversely proportional to the distance between two conductors. Increasing the metal-to-substrate spacing can reduce this capacitive coupling loss. In addition, recently the CMOS process allows multi-metal levels fabrication. The metal layers used are mostly three or four layers and sometimes more than six layers. The increase of metal layers can also help increasing the metal-to-substrate spacing. Therefore, using many metal layers can reduce the substrate loss. Moreover, Erzgraber and his partners proposed an oxide isolation

technique to reduce the parasitic capacitance [21]. They suggested a thick buried oxide isolated from the substrate to increase the distance between the metal spiral and the low resistivity Si substrate, and found that the peak Q value was increased almost twice.

2.1.2 Metal Conductivity and Multilevel Interconnection

The material used for fabricating the metal lines is also important. Aluminum metallization is typically used in CMOS technology due to its ease of fabrication and low cost. However, in order to further reduce the series resistance of the inductor, a thick gold metallization with higher conductivity is preferred [22], especially in GaAs technology. As mentioned before, the inductor is usually built on the upper layers of the device. The metal used in the upper layers should have low metal resistivity and/or with large metal thickness.

Special multilevel interconnect technology is also a way to achieve higher performance of the on-chip inductors [19], [23]. By shunting neighboring metal layers through via arrays, the effective thickness of the spiral inductor increases, thus reducing the series resistance. Fig. 2.1 shows a model with four metal layers. M2 to M4 forming the spiral pattern are linked together by via arrays. The effective thickness after the metal layers are shunted is increased more than 5 times. The series resistance can be reduced by the thick multilevel interconnect.

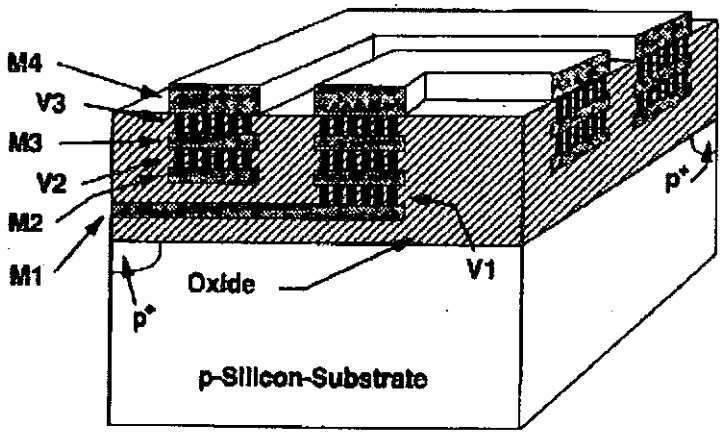


Figure 2.1. Cross-section view of the 4-level interconnect model [19].

2.1.3 Substrate Resistivity

Many researches are targeted on investigating the effect of substrate loss. The modification of the silicon fabrication process has been explored, such as silicon-on-insulator (SOI) [45], silicon-on-sapphire (SOS), high-resistivity silicon (HRS), and use of glass [24]. The methods for improving the loss mainly include using high resistivity substrate, building ground shields and back-etched micromachining.

Long and Danesh fabricated microstrip lines on substrates with resistivity of 1 Ω-cm and 10 Ω-cm [25]. A dramatic increase in series resistance was found at the lower resistivity substrate as the frequency increased. In the conductive substrate, more currents are induced by the inductive and capacitive coupling. This "image" eddy current will produce an opposing magnetic field and leads to eddy currents flowing in the metal strip, and then cause current crowding in the metal line, hence

increasing the series resistance. Proton addition to the substrate surface can also produce a high resistivity layer on the substrate [26], [46]. Lee proposed high energy proton bombardment to create semi-insulting silicon regions on IC wafers [27]. He reported that the increase of proton fluence can increase the substrate resistivity. The substrate resistivity which was originally at the value of 15 Ω-cm could increase to about $5x10^5$ Ω-cm after the proton radiation.

The on-chip spiral inductors have been used commonly in gallium arsenate (GaAs) RF MMIC [28]. The resistivity of Si substrate used in MMIC technology typically varies from 0.1 Ω-cm to 200 Ω-cm. However, in order to overcome the problem of substrate loss, it was found that the substrate resistivity should be at least greater than 1000 Ω-cm [29]. It is difficult for common Si MMIC to achieve this value. On the other hand, the semi-insulting GaAs can reach the resistivity of 10^6 Ω-cm. The value is sufficiently high to eliminate the parasitic elements from substrate. This is one of the reasons GaAs becomes popular for microwave technologies.

2.1.4 Shielded Structures

Researchers have proposed some shielded structures inserted in between the inductor and substrate to block the electromagnetic energy from the coil. The reduction in Si parasitics by ground shielding included solid ground shield (SGS) [30]-[31] and patterned ground shield (PGS) [32]-[36]. The shield is usually built with lower metal or polysilicons layer and provides a short to ground.

SGS consists of a solid metal or polysilicon layer inserted between the spiral inductor and the substrate. The solid plate blocks the electric fields of the inductor flowing to the substrate. However, the magnetic fields from the spiral still penetrate into the solid shield and induce a current flowing in it. The induced current in the shield opposes the current in the inductor. The negative magnetic coupling reduces the overall magnetic fields and decreases the inductance of the inductor.

The structure of patterned ground shield is shown in Fig. 2.2. The slots between the strips act as a "cut-off" to the induced current flowing on the strips. The "cut-off" pattern only allows the shielded current to flow perpendicular to the metal line of the spiral and minimizes most of eddy current loss. Since one of the purposes of PGS is to give a good medium to short the electric field from spiral to ground, the width of the slots should be sufficiently small so that the electric fields will not leak through the shield to the substrate. The major drawback of the PGS is the reduction in self-resonant frequency.

Yue compared the shielded structures built by aluminum and polysilicon [32]. He found a strong frequency dependence of the series resistance and inductance in aluminum SGS due to large "image" current formed by the conductive shield. The polysilicon SGS has properly solved this problem. In addition, a higher peak Q value and lower self-resonant frequency of the PGS has been also reported [32]. Yim also proposed using an n+ buried/n-well PGS so that the peak Q value has increased about 25% [36]. He also found that there is an optimum area of PGS to obtain a maximum Q factor.

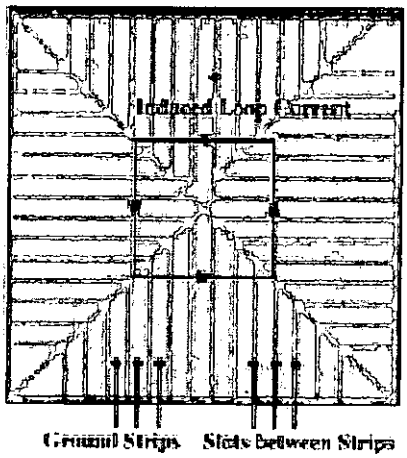


Figure 2.2. PGS photo [32].

2.1.5 Backside Micromachining

Backside micromachining is an effective method to eliminate all the eddy current effect from the lossy substrate (Fig. 2.3). In the post-processing of CMOS fabricated chips, the substrate under the spiral inductor is selectively removed by the etching process. As a result, the induced current under the inductor will no longer exist, thus achieving a higher inductance and Q factor. The major drawback of this technique is the device's mechanical weakness. Since most of the substrate is etched away, there are only thin metal layers and oxide layers remained. The chips will be broken easily during the measurement or operation due to the weak support of the device. Ozgur proposed a new post-processing procedure to reduce mechanical problems of the chips [10]. An adhesive-superstrate layer was attached on the top of substrate. After the back-etched process, the inductor was fabricated on the micromachined area. The superstrate layer provided enough internal stresses to the inductor and supported the device properly. The peak Q factor of the back-etched inductor has been increased about 90%. Low-k polyimide was also used as the stress-compensation to improve the

mass-fabrication problems and reduce the large parasitic capacitances [37].

Figure 2.3. Backside micromachined sample [37].

2.1.6 Surface Structure Micromachining

Besides the back-etching of the substrate, lifting out the spiral coils from the substrate is also an effective way to eliminate the substrate loss. Zou and Liu suggested a microstructure lifting technique, namely plastic deformation magnetic assembly (PDMA) [47], [48]. In PDMA, when an external magnetic field is applied, the flexible region of the device is plastically deformed and the surface structure is rotated by an angle off the substrate. It finally stays vertically as shown in Fig. 2.4. They found that the Q factor was improved about 3 times after the PDMA process.

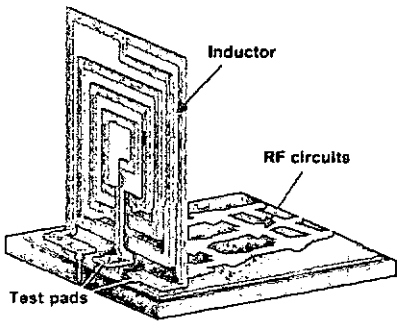


Figure 2.4. Schematic diagram of building a vertical spiral inductor using PDMA.

2.2 Inductor Structure

2.2.1 Planar Inductor

The simplest on-chip spiral inductor is constructed in planar form. The circular spiral inductor, shown in Fig. 2.5(a), is believed to have a high Q factor and low resistance loss [28]. Since the circular shape has the shortest perimeter for a given area, it gets highest number of turns for a given metal length, thus giving the highest inductance and Q value. However, as mentioned in section 1.3, not many layout design tools support the circle drawing feature, so that a square spiral pattern, shown in Fig. 2.5(b) and (c), is a popular alternative. Hexagonal and octagonal patterns [49], shown in Fig. 2.5(d) are also choices which are similar to the circular structure but more supportable by the CAD tools. Kuhn proposed centre-tapped spiral inductors (Fig. 2.6) which obtained better performance and occupied less chip area than the conventional planar inductor [38].

The conventional planar inductors are designed and fabricated with constant metal line width. However, researches found that the magnetically induced losses are serious problems in the inner turns of the spiral where the strongest magnetic field exists. Since the spacing between the opposite sides of the inner spiral of the inductor is small, it leads to decrease of inductance because of the negative mutual coupling. Long and Copeland suggested the spacing of the opposite sides of the inner turns should be greater than five metal line widths ($5w$) to reduce the parasitic electric and magnetic coupling [39]. Lopez-Villegas proposed a planar inductor with different strip width in each turn of the spiral, shown in Fig. 2.7 [40]. Narrower metal widths at

inner turns reduce the magnetically induced losses. Wider metal widths at outer turns minimize the series resistance losses. The total loss of the inductor is therefore minimized. He also suggested an optimum width for any turn of the spiral. The inductors with optimized metal widths were found to have a 60% better Q than the inductors with constant metal width.

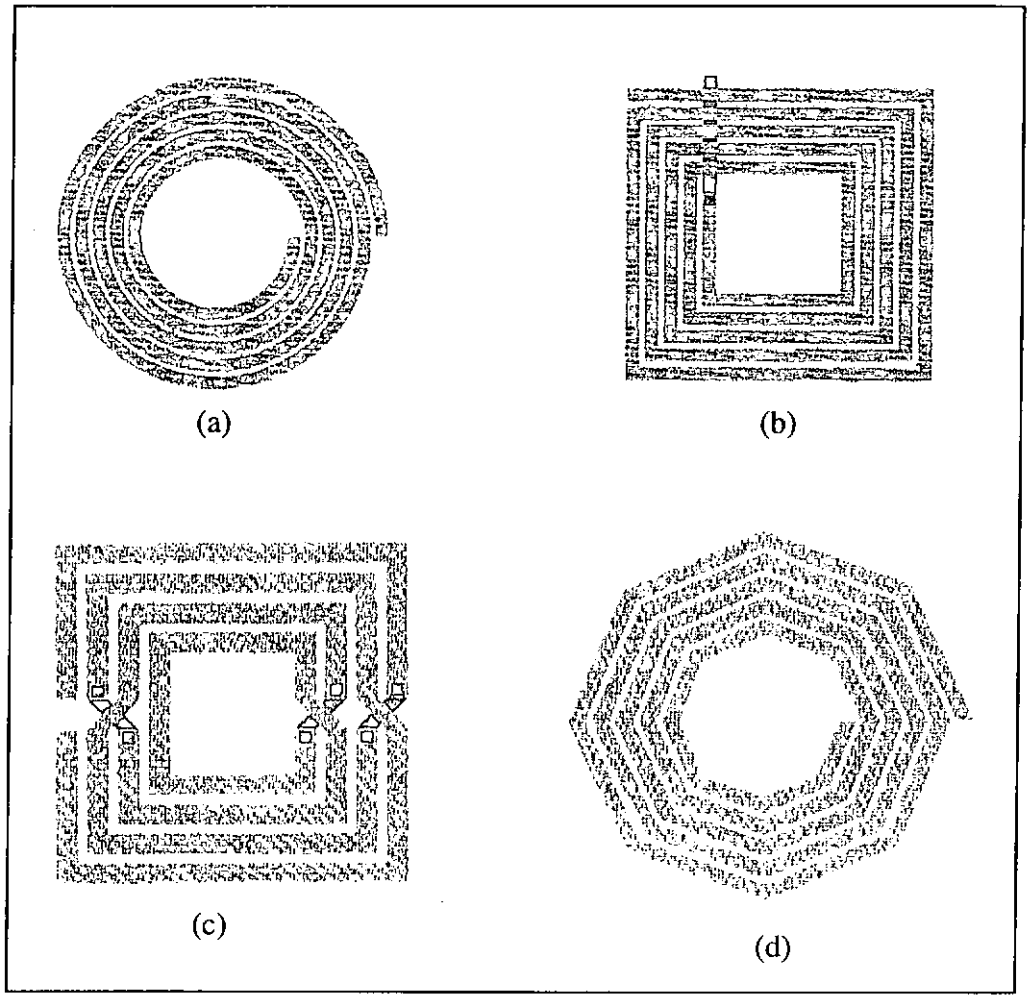
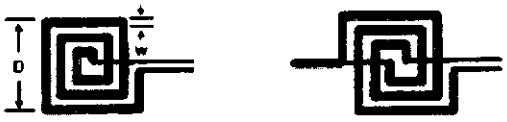


Figure 2.5. Common planar inductor structures. (a) Circular inductor. (b) Square inductor. (c) Symmetric planar inductor. (d) Octagonal inductor [1].



(a) (b)

Figure 2.6. (a) Conventional planar inductor .vs. (b) Centre-tapped inductor [38].

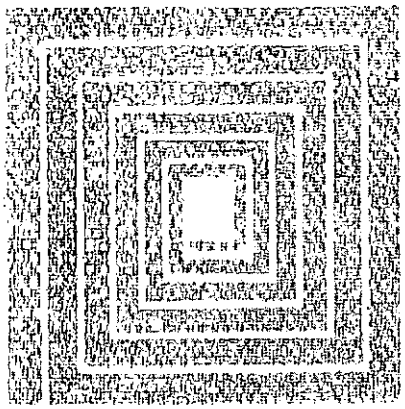


Figure 2.7. Planar inductor with variable metal width [1].

2.2.2 Multilayer Inductor

Modern IC processes support the fabrication of many metal layers. Multilayer inductors where the spirals are connected in series or in shunt in different metal layers are promoted. The benefit of the spirals connected in shunt is to increase the effective thickness and reduce the series resistance loss. The spiral connected in series can increase the total inductance and maintain the same Q factor while occupying the same area as the planar inductor. The area of this stacked inductor can also be reduced in the same ratio by keeping the inductance constant [41].

The input impedance of the two-layer stacked inductor [42], shown in Fig. 2.8 is

$$Z = j\omega(L_1 + L_2 + 2M) \tag{2.1}$$

The mutual coupling of the stacked inductor is strong and $M \approx \sqrt{L_1 L_2} = L$. So, the inductance is increased by four times compared to the single spiral. In other words, an n-layer stacked inductor has n^2 times increase of total inductance than one spiral. He also showed that the equivalent capacitance of the two-layer stacked inductor was

$$C_{eq} = \frac{1}{12}(4C_1 + C_2) \tag{2.2}$$

where C_1 is the capacitance between the two metal layers, and C_2 is the capacitance between the bottom metal layer and the substrate. The equivalent capacitance of the n-layer inductor was

$$C_{eq} = \frac{1}{3n^2}(4\sum_{i=1}^{n-1} C_i + C_n) \tag{2.3}$$

Form the above equation, the self-resonant frequency can be estimated by (1.38). Moreover, the upper interlayer capacitances contribute a factor of 4 to the effective capacitance than the bottom one. Putting the metal layers further from each other can achieve a high self-resonant frequency (Fig. 2.9). The interlayer capacitance reduction can also raise the Q value.

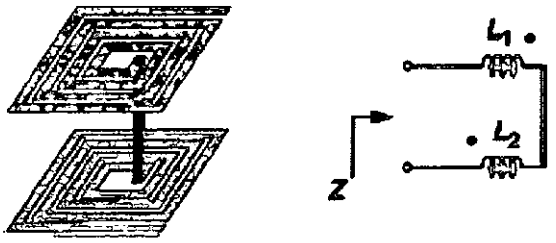


Figure 2.8. Double-layer stacked inductor. [42]

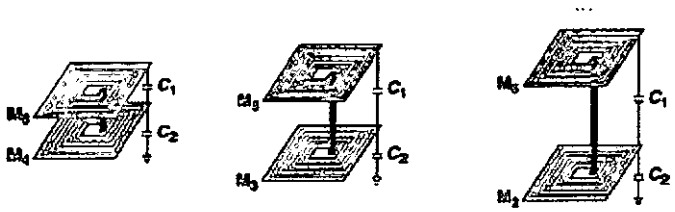


Figure 2.9. Modification of double-layer inductor [42].

Tang proposed a miniature 3D structure as shown in Fig. 2.10 [16]. The miniature 3D inductor involved more than two stacked inductors connected in series and each stacked inductor only got one turn in each metal layer. He found the self-resonant frequency of the miniature inductor was 34% higher than the conventional stacked inductor, and occupied only 16% of the area of the planar inductor and at the same time had higher Q value than both inductors.

Chen proposed a structure of symmetric 3D inductor as shown in Fig. 2.11 [17]. The structure consisted of a metal line winding downwardly (upwardly) with right-half (left-half) turn to the left-half (right-half) turn of the adjacent layer and finally maintaining the symmetry of input and output. The outer radii of the adjacent layers were different so that the mutual coupling was minimized. He found that the

inductor area was saved for about 30% compared to the symmetric planar inductor.

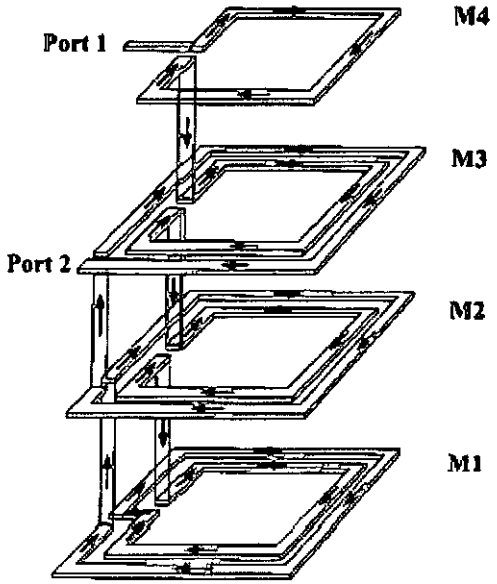


Figure 2.10. Miniature 3D inductor structure [16].

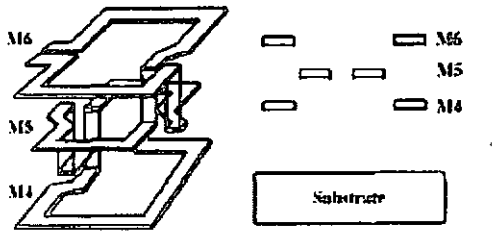


Figure 2.11. Symmetric 3D inductor structure and its cross-sectional view [17].

Chapter 3

Methodology

Despite past research efforts, there is still a need to clarify the various factors determining the Q factor in on-chip inductors, especially in multi-layer structures. Our research is targeted on the optimization of on-chip inductors by varying the layout parameters including metal width, metal layer topology, number of turns and overall layout. All inductors were designed to have the same inductance in order to provide a systematic comparison.

3.1 Sample details

In our research, inductors were fabricated using standard 0.6 μ m CMOS technology with 3 metal layers. Samples included 3D inductors (M05, M10, M15 and M20), planar inductors (P05, P10, P15, P20, T6.0 and T7.5) and double layer (D31 and D32) inductors. The layout of the samples is summarized in Table 3.1. All spiral patterns were in square form. The inductance of all inductors was fixed at 5 nH as determined by eqns. (1.1) - (1.10) and then verified by numerical simulation. It was found that the spacing between the metal lines should be as narrow as possible to maximize the magnetic coupling between the lines [39], [42]. According to the design rule of the fabrication process, the minimum spacing between two metal strips should be 1.8 μ m. The metal line separation in the samples used was set to be 2 μ m for

convenience.

Sample	Width(μm)	Side Length (μm)	Turns	Metal Layer involved
M05	5	113	2	M3 - M1
M10	10	143	2	M3 - M1
M15	15	169	2	M3 - M1
M20	20	191	2	M3 - M1
P05	5	163	4.5	M3
P10 / T4.5	10	212	4.5	M3
P15	15	256	4.5	M3
P20	20	299	4.5	M3
T6.0	10	198	6	M3
T7.5	10	191	7.5	M3
D31	10	123	4.5	M3, M1
D32	10	123	4.5	M3, M2

Table 3.1. Samples dimensions.

A 3D inductor structure is illustrated in Fig. 3.1. A single-turn stacked inductor from M3 to M1 combines with another single-turn stacked inductor from M2 to M3 to form a 2-turn 3D inductor. Since the metal lines for input and output signal are designed on the same layer, the bottom metal layer just consists of only one-turn spiral. Since wider metal lines will increase the overall inductor area, M20 is the largest 3D inductor.

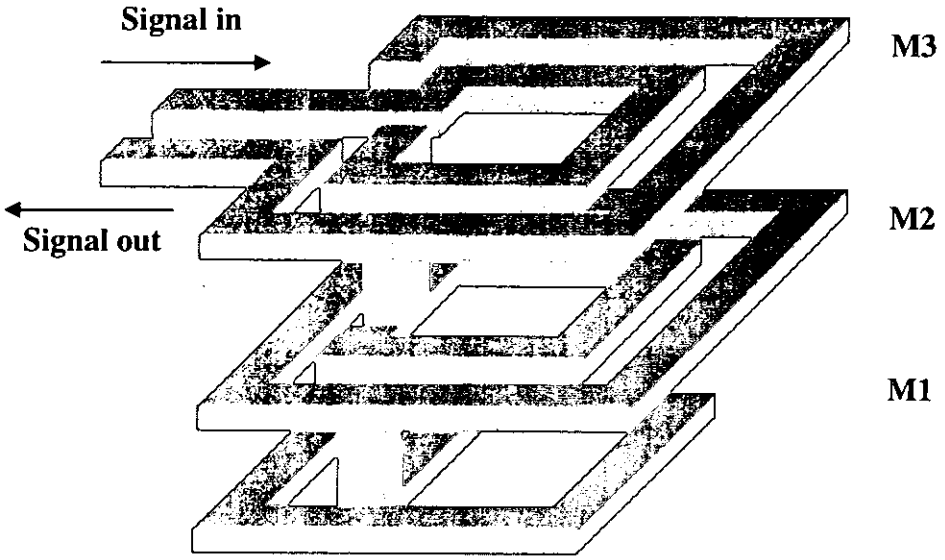


Figure 3.1. 3D inductor.

A planar inductor consists of a spiral top layer which acts as the main spiral structure to contribute inductance, and a bottom layer with a single metal line which acts as an exit for signal out. Just similar to 3D pattern, P05 to P20 have a variable metal line width from 5 to 20 μm but in planar structure. The sample name, T4.5, is also assigned to the planar inductor with the metal width of 10 μm. This is due to a further comparison between T4.5, T6 and T7.5 to study the effect of different number of turns. Since only one spiral layer contributes to the inductance, this type of inductor is always comparative large in size.

The stacked inductor used in this research is a double layer inductor. It consists of a 4.5-turn spiral-in pattern at the top metal layer and a 4.5-turn spiral-out pattern at the bottom layer. Since both metal layers of the inductor contribute to the inductance together with high mutual coupling between the layers, the size of the stacked

inductor is usually small and almost 3-4 times smaller than the planar inductor with the same inductance.

3.2 Sample Design

The layout of the samples in Table 3.1 was done by Cadence design tool. The samples were constructed within a 2.5 x 2.5 mm^2 die which is shown in Fig. 3.3. There were S-G pads (Fig. 3.2) used to probe the inductor structure. "Open" pads were also included to extract the pad impedance during the measurement [43]-[44].

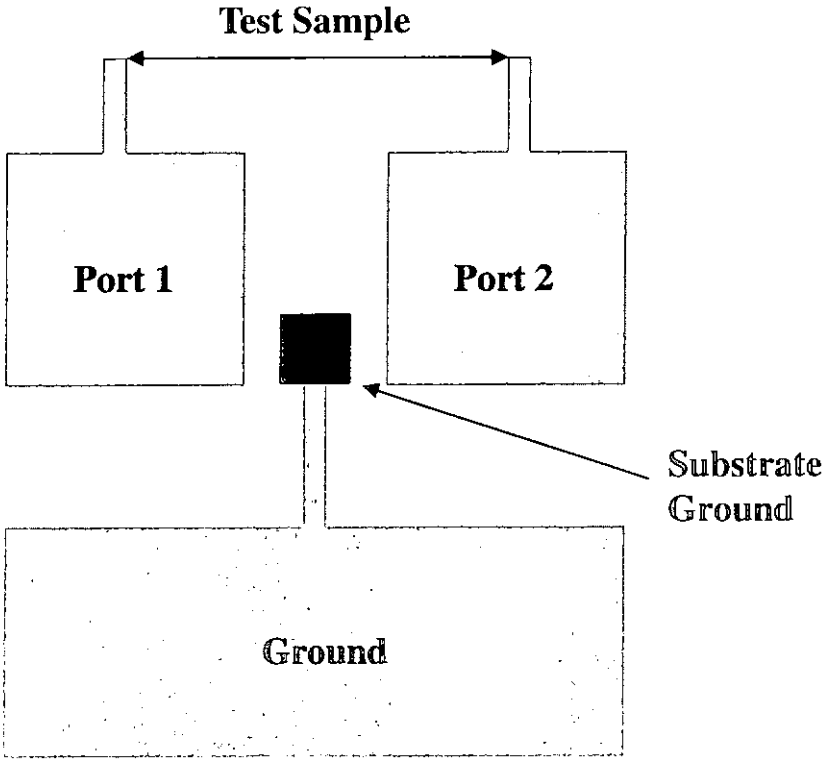


Figure 3.2. S-G pad structure.

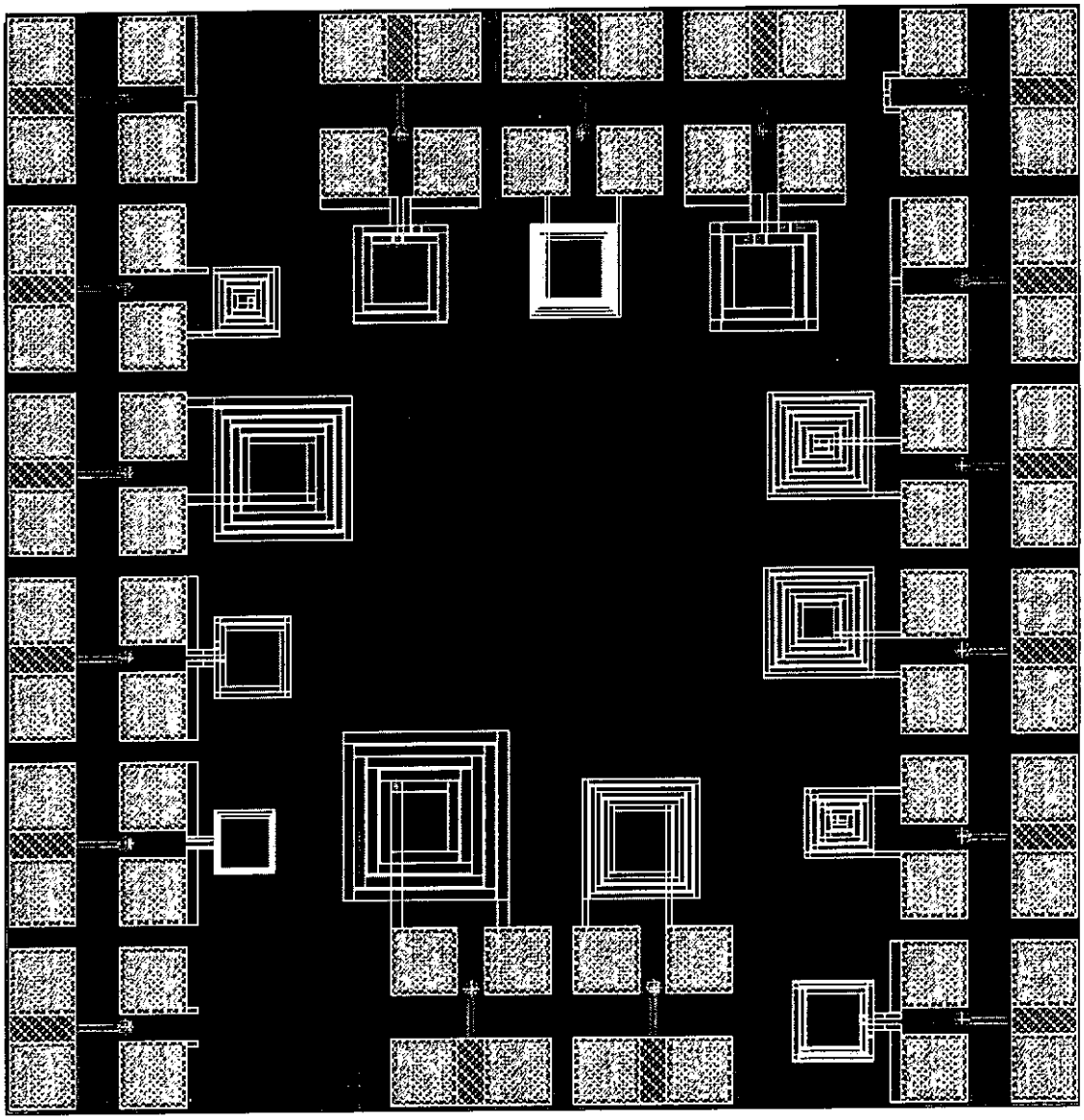


Figure 3.3. Inductor structures in Cadence.

As shown in Fig. 3.3, the spiral inductors were fabricated using Austria Mikro Systeme International AG's (AMS) 0.6 μm CMOS process. A bulk substrate with resistivity of $13\times10^{-3}\,\Omega$-cm was used. However, the Si epi-layer is fairly resistive at about $20\,\Omega$-cm, with a thickness of more than $10\,\mu$m. The CMOS process parameters are shown in Table 3.2

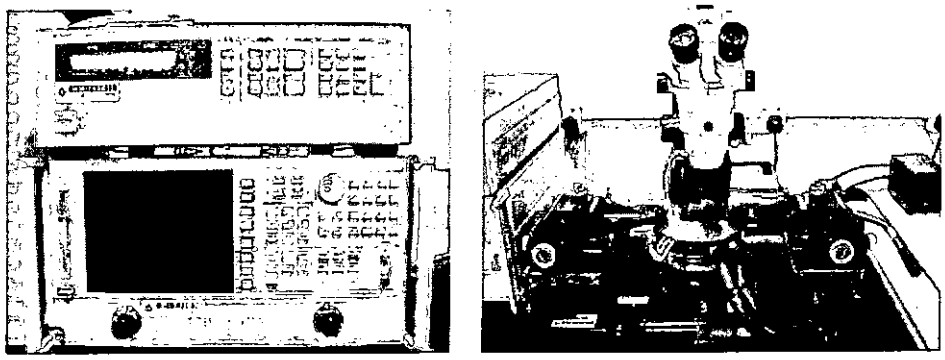
Metal 3	R_{sh} = 40 mΩ/sq	t = 0.94 μm	C_{sub} = 9.28 aF/μm^2 C_{M2} = 53.1 aF/μm^2 C_{M1} = 17.7 aF/μm^2
Metal 2	R_{sh} = 100 mΩ/sq	t = 0.65 μm	C_{sub} = 14.3 aF/μm^2 C_{M1} = 53.1 aF/μm^2
Metal 1	R_{sh} = 100 mΩ/sq	t = 0.72 μm	C_{sub} = 32.9 aF/μm^2
Epi- Substrate	ρ = 18.76 Ω-cm	t = 14.5 μm	p^+ Si
Bulk Substrate	ρ = 0.013 Ω-cm	t = 530 μm	p Si

Table 3.2. CMOS process parameters.

C_{sub} is the capacitance with the substrate, C_{M1} is the capacitance with Metal 1, C_{M2} is the capacitance with Metal 2.

3.3 Device Measurement

The inductor measurement was performed by a network analyzer 8720ES (Agilent), shown in Fig. 3.4 (a), from the frequency range of 50 MHz to 10 GHz with a standard probe station Microtech RF-1 (Cascade), shown in Fig. 3.4 (b). The probes used were a pair of air coplanar signal-ground (SG) microprobes (Cascade) (Fig. 3.5(a)).



(a) (b)

Figure 3.4. Measuring equipment. (a) Network analyzer. (b) Probe station.

3.3.1 Calibration

After the analyzer was set up and connected to the probe station, the planarity positioners on the probe station were adjusted to planarize the microprobes so that the tips in each probe (Fig. 3.5(b)) were at identical vertical level. The planarization was performed by a gold contact substrate. To ensure that the level of the tips was the same, the microprobes were kept adjusting and probing on the contact substrate until two even probing marks on the contact substrate shown in Fig. 3.5(c) were found. The microprobes were then cleaned to get the accurate measurement result. To clean the probes, it was skated up and down the gold part of the contact substrate. The substrate is a rough surface which will provide enough resistance to enable the mess, such as aluminum accumulated by last measurement, to come off.

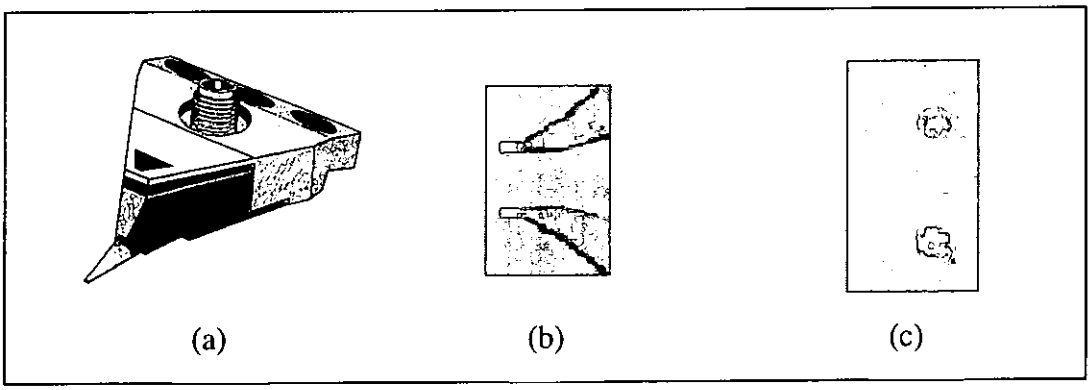


Figure 3.5. Graphs about microprobe. (a) Outlook. (b) Tips. (c) Probe marks on contact substrate.

The system was calibrated by short-open-load-through (SOLT) calibration to remove the parasitic element from the connections and the probes. The calibration kit of impedance standard substrates (ISS) had a number of "short", "load" and "through" standards. The whole calibration process was controlled by the automatic Cascade Microtech calibration software, *WinCal*. It provided a step-by-step guideline (open→load→short→thru) (Fig. 3.6) to achieve the calibration. After the calibration, a number of load resistors trimmed to 50 Ω on the ISS were re-measured in order to verify the calibration.

After the calibration, the sample were then probed and measured. The measured data represented by *S* parameters was recorded by the analyzer. To ensure the repeatability of the inductors, the device was re-measured several times. Fig. 3.7(a) shows a layout of spiral and probe pads for the measurement. The open-pad two-port network, shown in Fig. 3.7(b) was also measured in order to de-embed the impedance between the pad structure and the substrate.

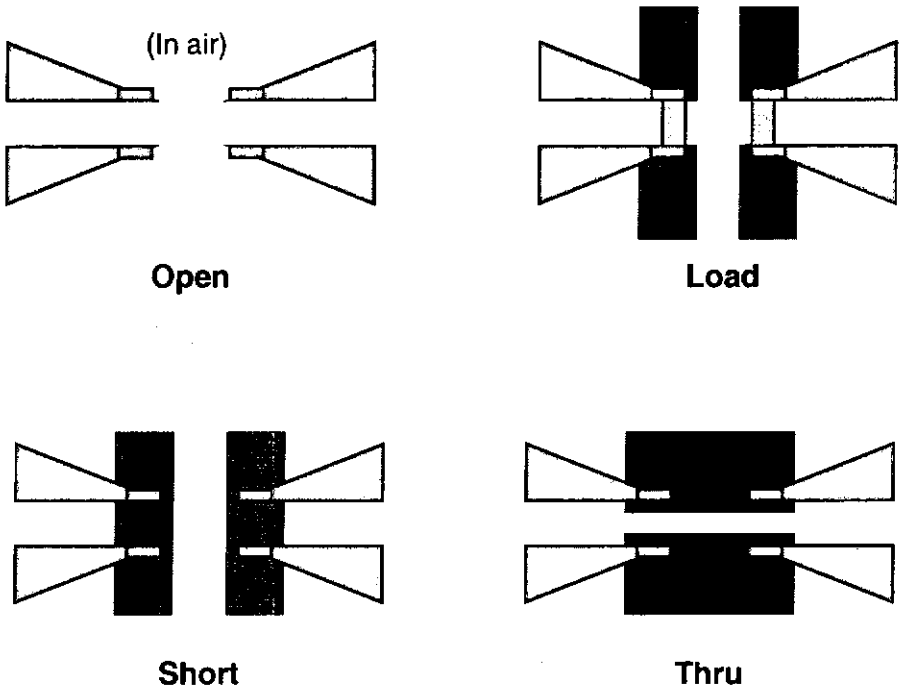
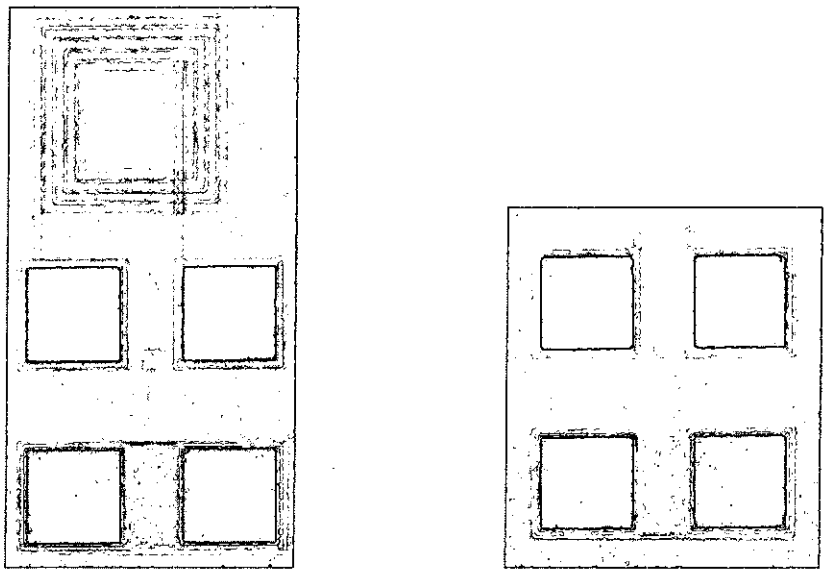


Figure 3.6. Calibration Steps (open, load, short and thru).



(a) (b)

Figure 3.7. Fabricated structures. (a) Spiral and probe pads. (b) Open-pad.

3.3.2 Data extraction

The real and imaginary parts of the S parameters of the samples were collected by the network analyzer. The branch impedances in the π representation (Fig. 1.6) were found by (1.29). The inductor is usually operated with one port shorted (port 2 short-circuited). In addition, the measured inport impedance is the combination of the pad impedance and the input impedance of the device. The impedance model can be represented by Fig. 3.8.

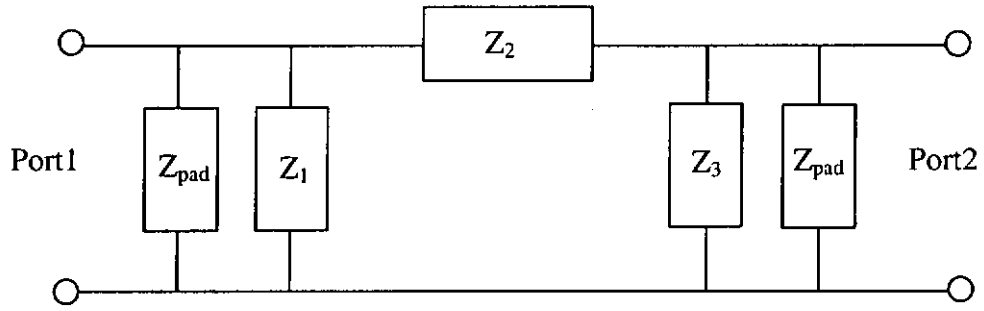


Figure 3.8. Equivalent circuit including pad impedance.

Z_{pad} represents the pad impedance. After eliminating the Z_{pad}, the effective resistance and reactance of the device were calculated by (1.31), and the effective inductance and Q factor were then determined by (1.32) and (1.33), respectively. The results from the measurement are presented in the next chapter.

3.4 Simulation

The simulation of the performance of the inductor was done by an electromagnetic analysis design suite, MicroWave (MW) Office. MW Office is a powerful EM numerical analysis tool. It integrates 3D planar electromagnetic simulation with the circuit simulation and layout tools, allowing arbitrary structures to be embedded within linear and nonlinear circuit simulations. After designing the layout patterns of the inductors and supplying the process parameters to the tool, the simulation can be carried out.

The samples shown in Table 3.1 were simulated. Firstly, the size (X and Y coordinate) of the platform was input. The platform size of a planar inductor was $350\,\mu$m x $350\,\mu$m large. Then, the process parameters such as the number of layers of the device, the layer thickness with the resistivity and dielectric constant, and the thickness and conductivity of the metal layers were entered. The process parameters used in the simulation are shown in Table 3.2.

Before the layout drawing, the cell size should be considered. Larger cell size means fewer cells for constructing the simulated inductor, hence improving the simulation time. However the currents in the metal lines, like the eddy currents from proximity effects, would not be accurately simulated. The cell size used in the simulation is $1\,\mu$m x $1\,\mu$m. This size makes sure that there are at least 5 cells within the metal line width. This allows the current redistribution in the metal strip recognized by simulation process, thus, improving the simulation accuracy. This size

also ensures that the simulation time and memory used for the simulation are within an acceptable range.

After entering the process parameters, the layout of the inductor could be designed by the drawing tools provided. Fig. 3.9 and 3.10 show the plan and 3D view of a 4.5-turn planar inductor designed, respectively. The spiral pattern was designed on the top layer while the exit metal line was designed on the second layer. The metal lines should be extended to the edge of the platform, and ports were added to each exit. The simulation time varied from half hour to one day depending on the structure's complexity. The *S* parameters could be generated after the simulation. The magnitude and phase angle of simulated *S* parameters for P10 are shown in Fig. 3.11 and Fig 3.12. The effective resistance, inductance and *Q* factor were extracted from the simulated *S* parameters as in Section 1.6.2.

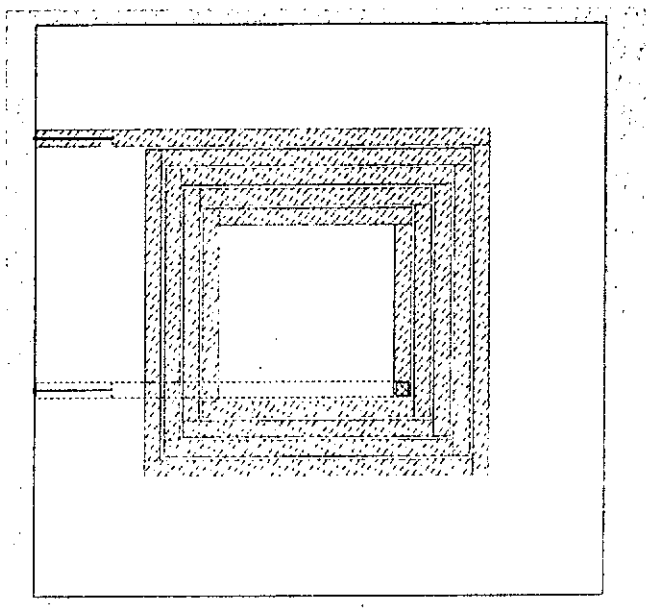


Figure 3.9. Plan view of planar inductor in MW Office.

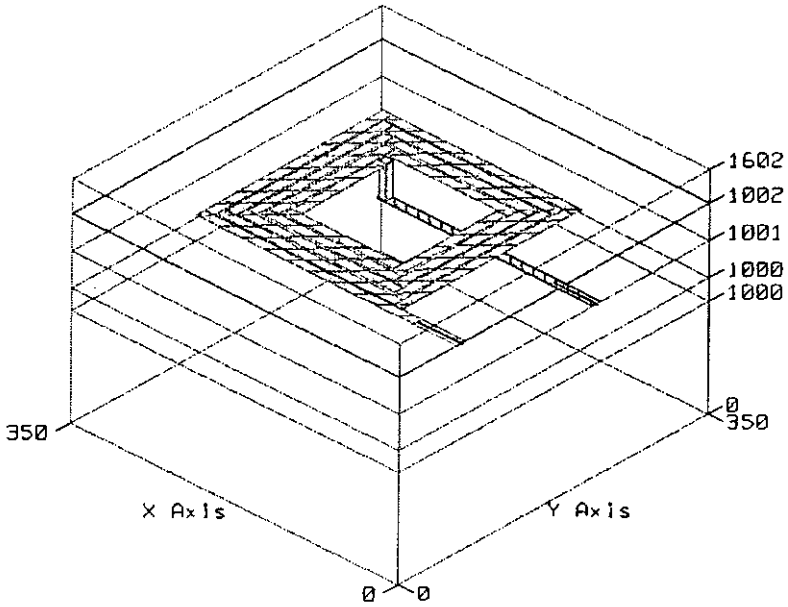


Figure 3.10. 3-D view of planar inductor in MW Office.

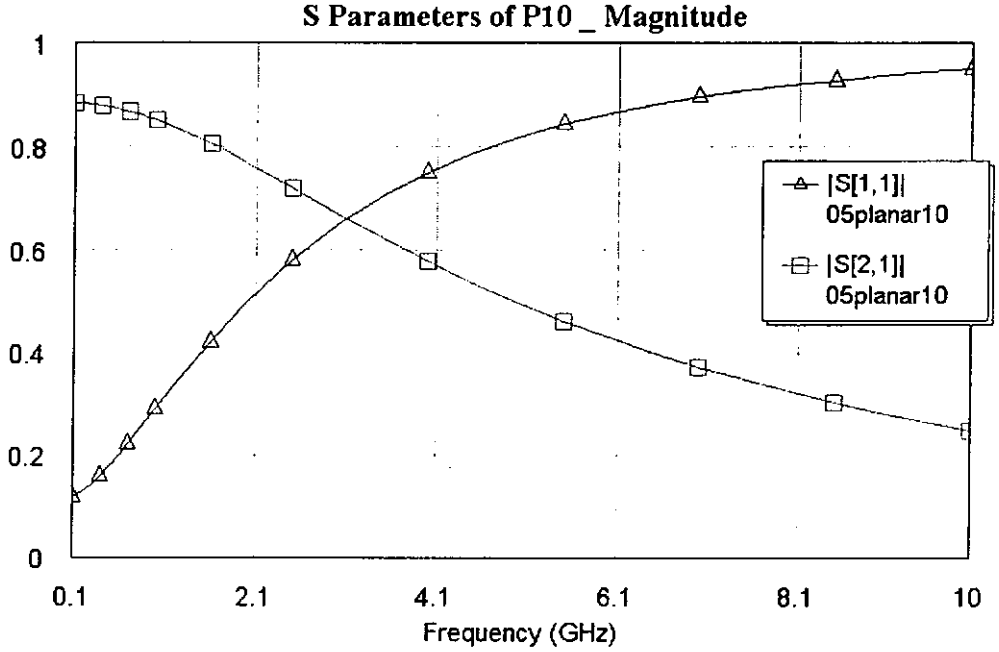


Figure 3.11. Magnitude of simulated *S* parameters for P10.

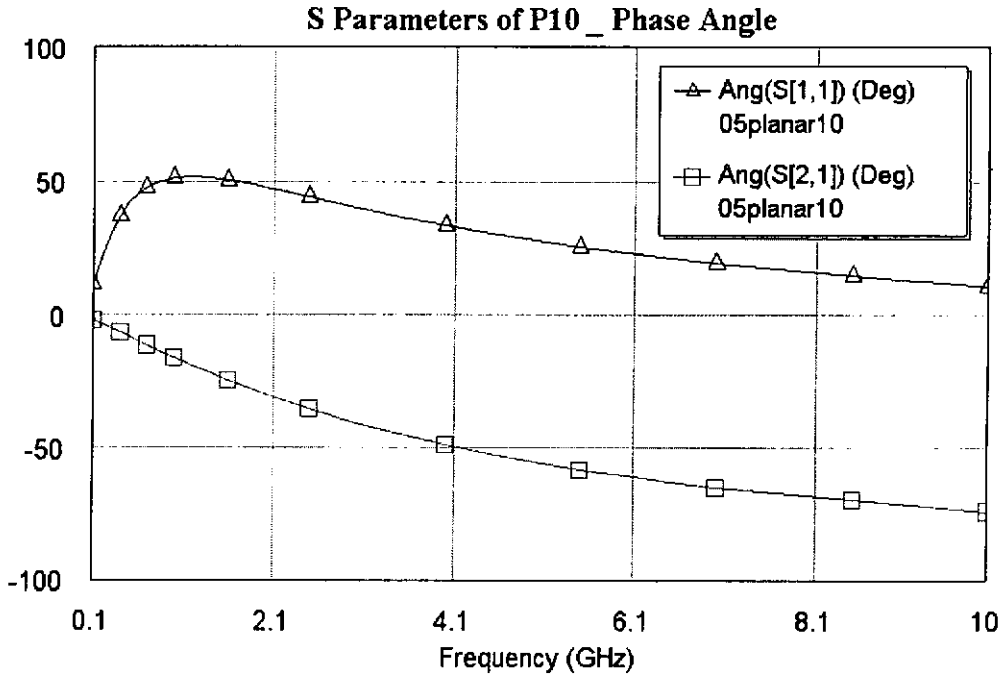


Figure 3.12. Phase Angle of simulated *S* parameters for P10.

Chapter 4

Results and Discussions

4.1 3D Inductors with Different Metal Widths

The experimental results of 3D inductors with various metal widths are shown below. Fig. 4.1 represents the effective series resistance of these inductors from 100 MHz to 5 GHz. Fig. 4.2 and 4.3 show the effective inductance and Q factors of the inductors as a function of frequency.

Below 500 MHz, the skin and proximity effects in the metal lines, and the substrate eddy current loss are not dominant. The main loss of the inductor is the dc resistance of metal line. The dc resistance of the metal line is theoretically inversely proportional to the metal width. The theoretically calculated dc resistance of the 3D samples was 26.6, 15.8, 11.4 and 9.2 Ω respectively. The measured result is almost the same as the theoretical result as observed in Fig. 4.1. At frequencies below 1 GHz, all inductors exhibit an effective inductance of 5nH, the designed inductor value as described to Chapter 3.

As the frequency increases, the effective resistance increases because of the skin and proximity effects in the metal lines. Both effects produce non-uniform current distribution in the metal line due to induced eddy currents, hence increasing the effective resistance. Skin effect is caused by the magnetic field from the current

flowing in the metal line itself. Proximity effect is due to the magnetic field from current in neighboring metal lines. These effects cause the ac resistance to increase with $\sqrt{f}$. Besides, the substrate eddy current loss also becomes dominant as the frequency increases. The resistance due to substrate effect is related to the area of the inductor and it increases with a factor of f^2 . The inductor areas of the four 3D inductors are $(113)^2$, $(143)^2$, $(169)^2$ and $(191)^2 \mu m^2$. M20 is about nearly two times larger than M05, and so suffers from more substrate loss than the others.

Fig. 4.1 shows that at frequencies below about 2 GHz, sample M20 with the widest metal width of $20 \mu m$ has the lowest resistance, and M05 with the smallest metal width of $5 \mu m$ has the highest resistance. But the rate of increase of the resistance with frequency depends strongly on the area of the inductor. The resistance rises most steeply as the frequency increases for M20 which has the largest inductor area. Its resistance increases dramatically above 1 GHz due the domination of substrate loss. Since M05 occupies the smallest inductor area, the resistance is only slightly increased due to less substrate loss.

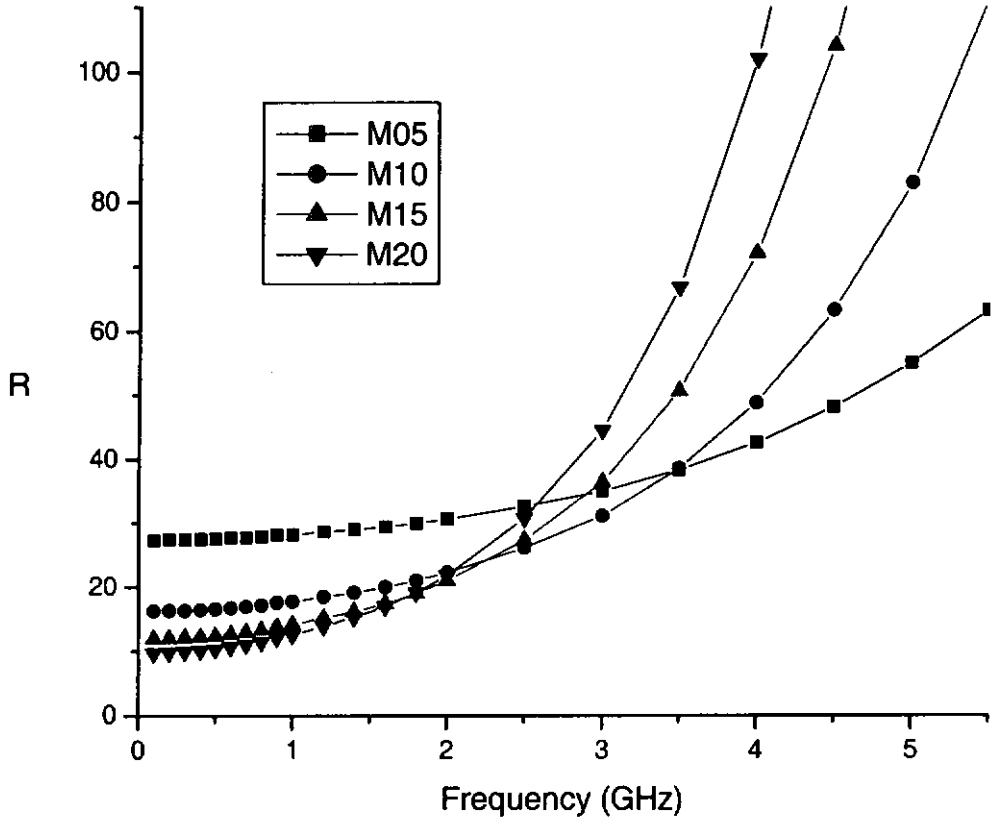


Figure 4.1. Measured effective resistance of the 3D samples from 100 MHz to 5 GHz.

Fig. 4.2 shows the effective inductance of the 3D inductors. The effective inductance of the inductors almost remains constant at low frequencies below 2 GHz. Then it increases gradually to its maximum value and then drops to negative value, meaning that the inductor becomes capacitive after passing the self-resonant frequency. The reason is that the coupling capacitances between metal lines and metal-to-substrate capacitance convert the effective impedance into capacitive at high enough frequencies. The self-resonant frequency f_{SR}, therefore sets a limit to the maximum operation frequency of the inductor. It is highest for M05, and is lowest for

M20. Therefore f_{SR} is increased as the inductor area is reduced.

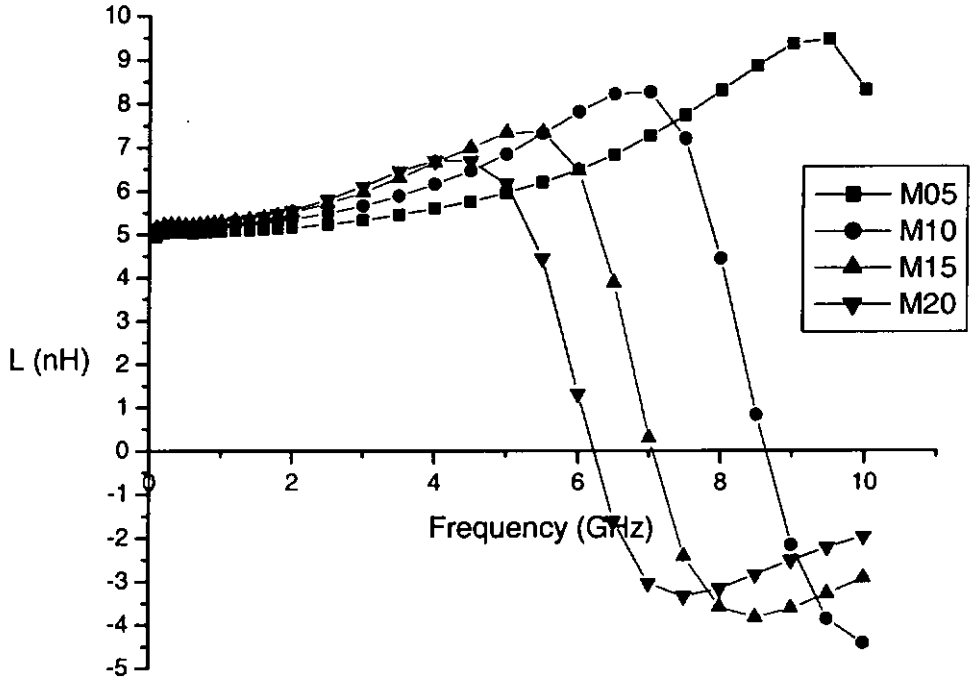


Figure 4.2. Measured effective inductance of the 3D samples.

M05 has the highest Q value of 3.57 at 5.5 GHz. The others samples, M10, M15 and M20 have their maximum Q values of 4.1, 3.95 and 3.9 at 3.1, 2.5 and 1.85 GHz respectively.

At low frequencies, as mentioned before, due to the domination of the dc resistance of the inductor, the samples with larger metal width benefit with having higher Q factors. As the frequency increases, the eddy current in the metal trace due to the skin and proximity effects increases the effective resistance. Samples with

larger metal width result in higher loss because of greater eddy currents in the metal trace by proximity effect. The inductor area is also greater in these samples, so the substrate loss increases with larger metal width. At frequencies above 4 GHz, sample M05 always has the highest Q factor. At any other frequency, there is a certain value of metal width which yields maximum Q value. This maximum represents the compromise between the dependence of dc resistance and eddy current loss on the metal width. Therefore the choice of metal width for optimum Q factor depends on the operation frequency.

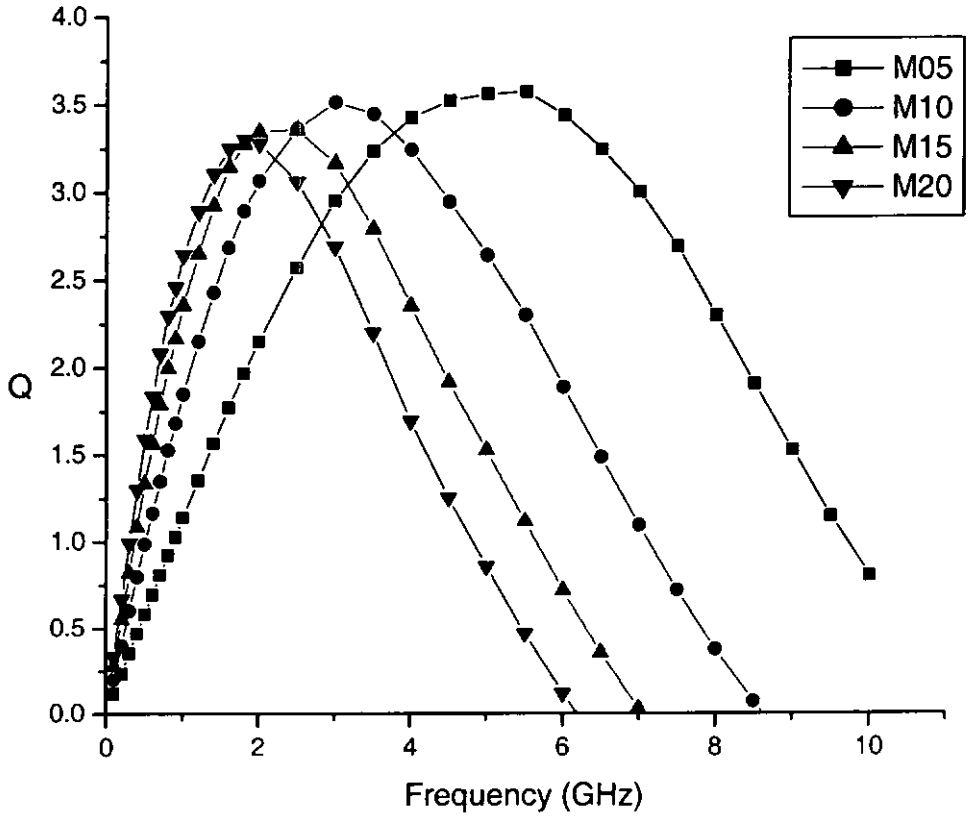


Figure 4.3. Measured Q factors of the 3D samples.

The inductor characteristics were simulated by a numerical program, Microwave Office. Fig. 4.4 shows the experimental and simulation result of Q factors of M05 and M20. A fairly good match between the simulated and measured results with the discrepancies of different samples around 7 – 12 % is observed. This is acceptable in view of the accuracy of numerical simulation. Further discussion would be made based on the simulation results.

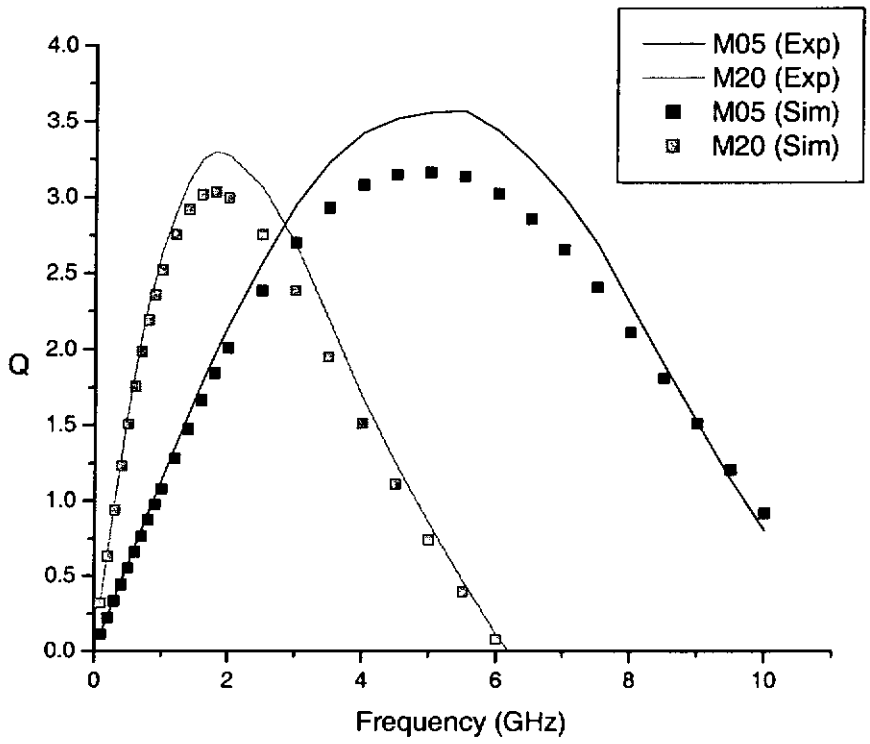


Figure 4.4. Measured and simulated result of 3D samples.

Simulation was done for the 3D samples assuming the substrate was removed by etching. Fig. 4.5 shows the effective resistance up to 5 GHz. Fig. 4.6 and 4.7 show the

effective inductance and Q factors of the back-etched inductors.

Fig. 4.5 shows the effective series resistance of the back-etched inductors from 100 MHz to 5 GHz. Below 500MHz, the resistance of the back-etched samples is almost the same as that of the normal samples. As the frequency is increased, the resistance increases gradually. At 3 GHz, the resistance of M05 is only increased by 10% compared with that at 300 MHz. The resistance of M05 with normal substrate rises almost one-third for the same case. For M20, the resistance is increased by 2 times for the back-etched sample while it is almost 4 times for a normal sample with the frequency rising from 300 MHz to 3GHz.

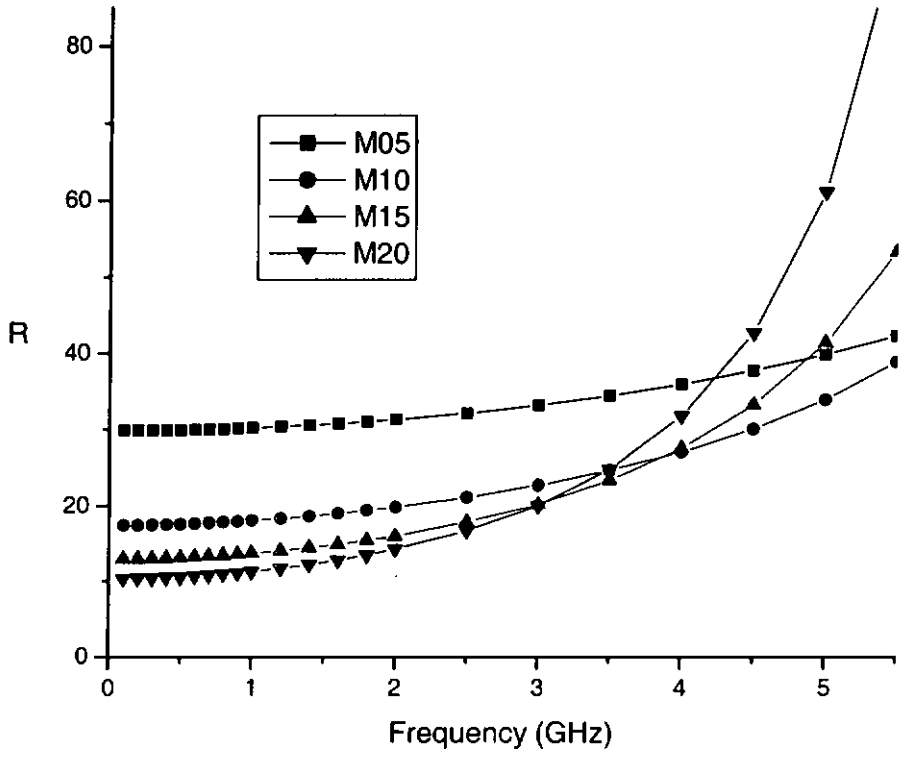


Figure 4.5. Simulated effective resistance of the 3D back-etched samples.

In back-etched samples, the substrate loss does not exist. The only losses are dc resistance and eddy current loss from skin and proximity effects in the meal lines. The dc resistance is a constant and the eddy current loss is proportional to $\sqrt{f}$.

From Fig. 4.6, the self-resonant frequency of the back-etched samples is higher than the normal samples. As the substrate of the samples is removed, the capacitive and inductive coupling between the metal and substrate no longer exists. The remaining couplings are from the capacitance between metal lines.

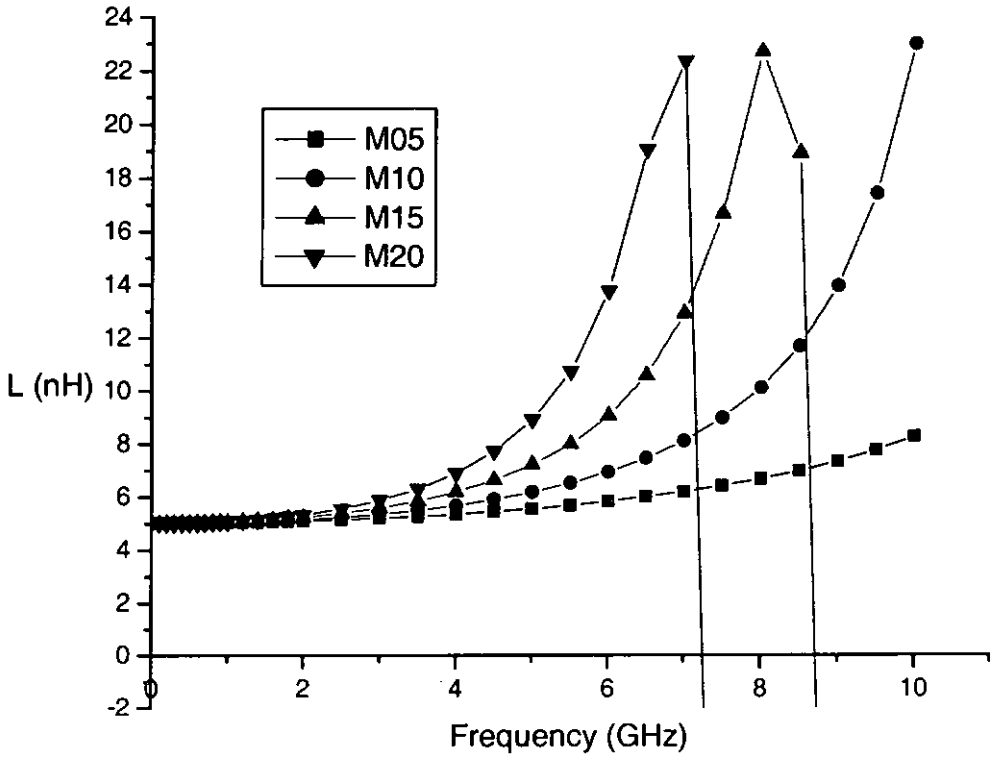


Figure 4.6. Simulated effective inductance of the 3D back-etched samples.

Fig. 4.7 shows the Q factors of the back-etched 3D samples from 100 MHz to 10

GHz. Compared with the normal samples, the peak Q factors of the back-etched inductors is improved by 70-80% from the range of 3 - 3.16 to that of 5.3-5.6. The self-resonant frequencies are also increased more than 15% after removing the substrate.

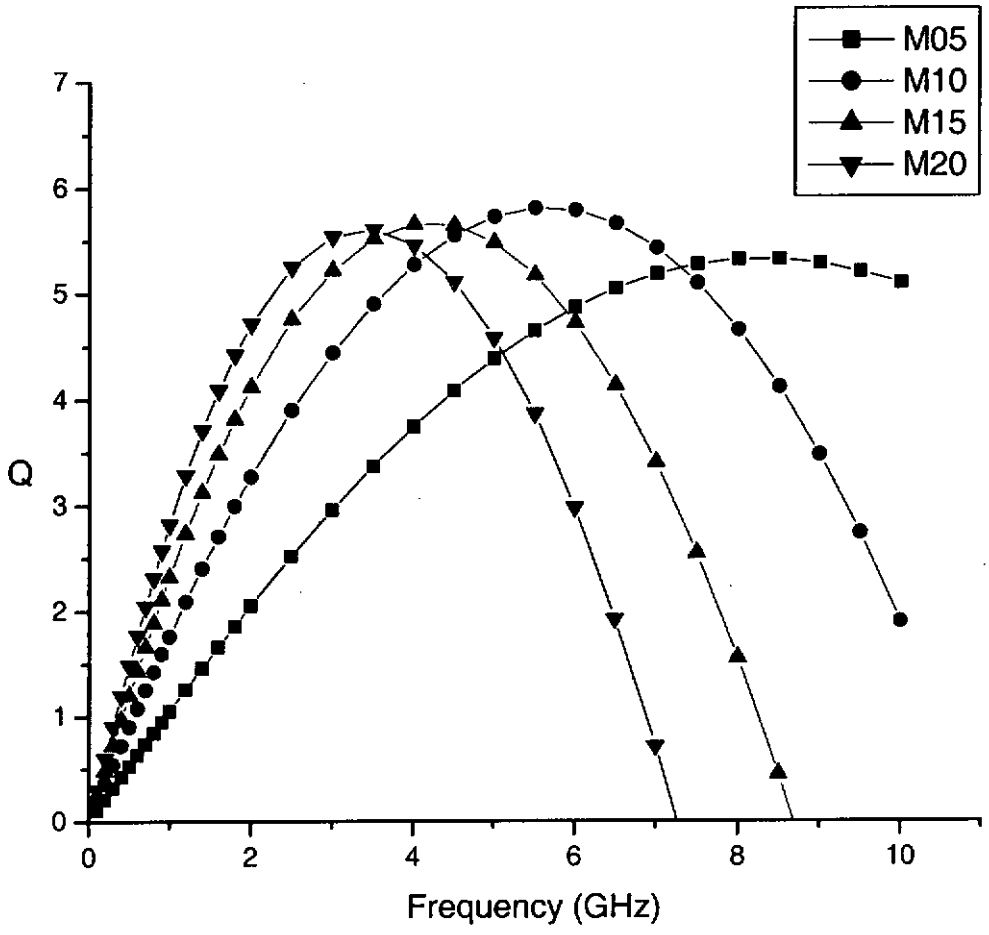


Figure 4.7. Simulated Q factors of the 3D back-etched samples.

4.2 Planar Inductors with Different Metal Widths

Measurement on traditional planar inductors with different metal widths was also made. Fig. 4.8 to 4.10 shows the results from measurement. The trend of the graphs representing the comparison of samples with different metal widths is similar to that of 3D inductors.

At low frequency range, the dc resistance is dominant in the operation. The samples with smaller metal width have more loss. From Fig. 4.8, P05, with the smallest metal width, has a resistance of 23 Ω below 500 MHz, and P10, P15 and P20 have resistance of about 13.5, 10 and 9 Ω respectively at the same frequency.

As the frequency increases, the effective resistances are increased due to the skin and proximity effects and substrate eddy current loss. The effective resistances of samples, P15 and P20 are increased more rapidly as compared with M15 and M20 in 3D inductors (Fig. 4.1). Thus, the planar inductors suffer from more losses as the frequency increases.

The area of planar inductors is 2 to 2.5 times of the 3D inductors with the same metal width in order to obtain the same inductance. Because of the larger inductor size, the planar samples suffer from more substrate eddy current loss.

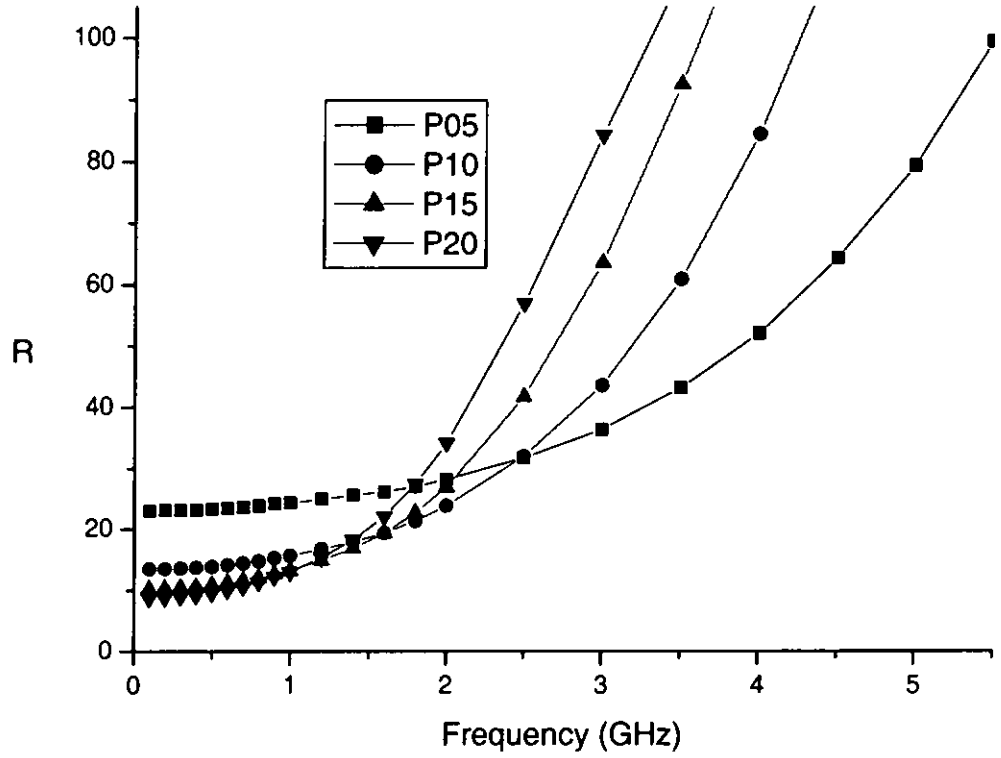


Figure 4.8. Measured effective resistance of the planar samples.

The effective inductance of the samples is shown in Fig. 4.9. The inductances are 5 nH as designed at low frequency. The inductances then increases as the frequency increases due to the metal-to-metal and metal-to-substrate capacitive and inductive couplings. Large capacitive coupling from the substrate finally causes the drop of the inductance at very high frequencies.

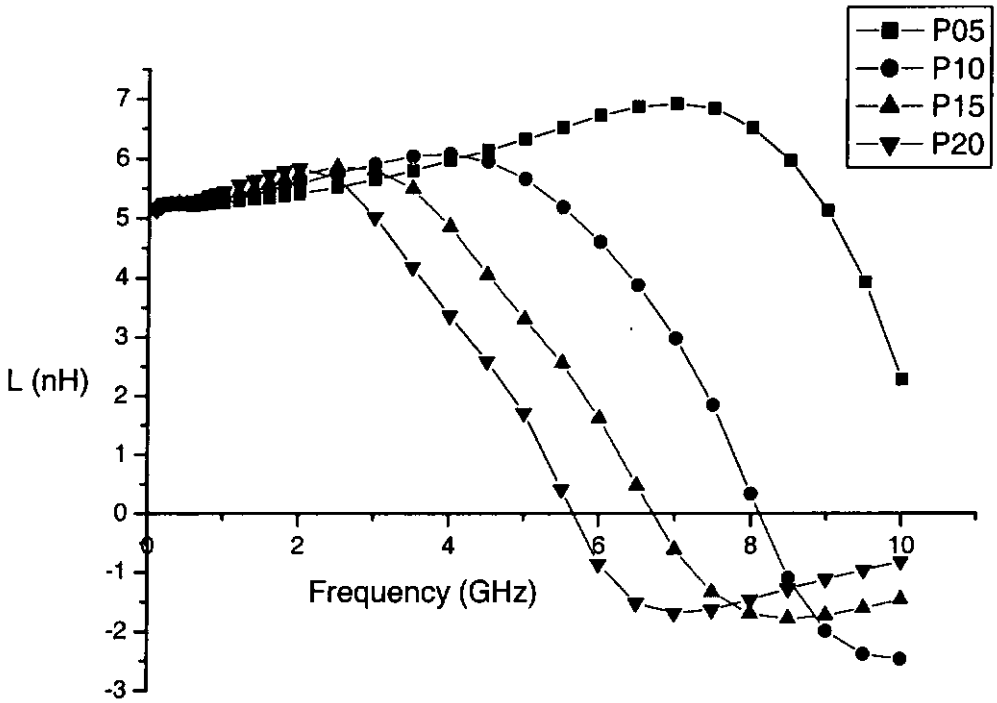


Figure 4.9. Measured effective inductance of the planar samples.

Fig. 4.10 shows the Q factors of the planar samples. Samples with comparatively wider metal line have higher Q factors at lower frequencies. Samples with smaller metal width have higher Q factors at high frequencies. Comparing to the 3D samples, the maximum Q factors of planar samples are about 20 – 30% lower. The self-resonant frequencies of the samples are also reduced by 10 – 15 %.

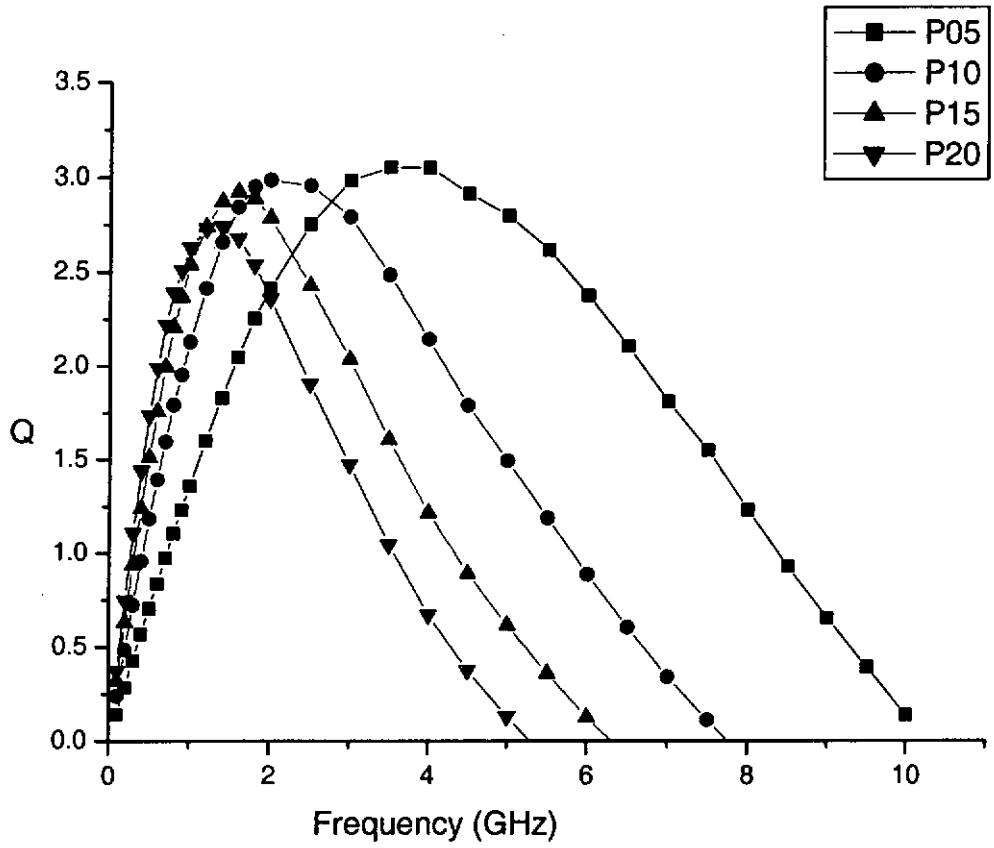


Figure 4.10. Measured Q factors of the planar samples.

The substrate loss plays a main role in affecting the performance of planar inductors. The removal of the substrate will greatly enhance the performance of planar inductors. Fig. 4.11 to 4.13 show the simulation result of the back-etched planar inductors with different metal widths. A huge improvement with resistance reduction, and increase of Q factor and self-resonant frequency is found.

The effective resistances of the planar samples without substrates shown in Fig. 4.11 are almost kept in constant below 2 GHz. At 4 GHz, the effective resistance of

P05 only rises 10% to 24 Ω compared to its resistance at low frequency. The resistance of P20 at 4 GHz is about twice of that at low frequency. It is almost a ten-fold reduction as compared to the same inductor with normal substrate. The removal of substrate could improve greatly the loss problem in the planar inductor.

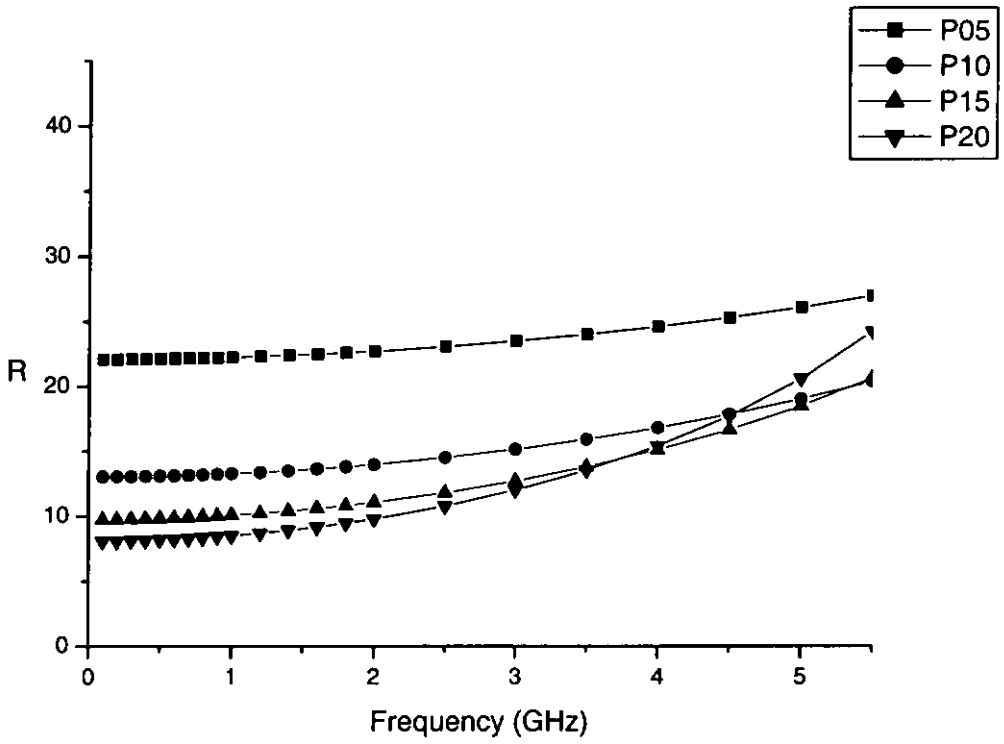


Figure 4.11. Simulated effective resistance of the back-etched planar samples.

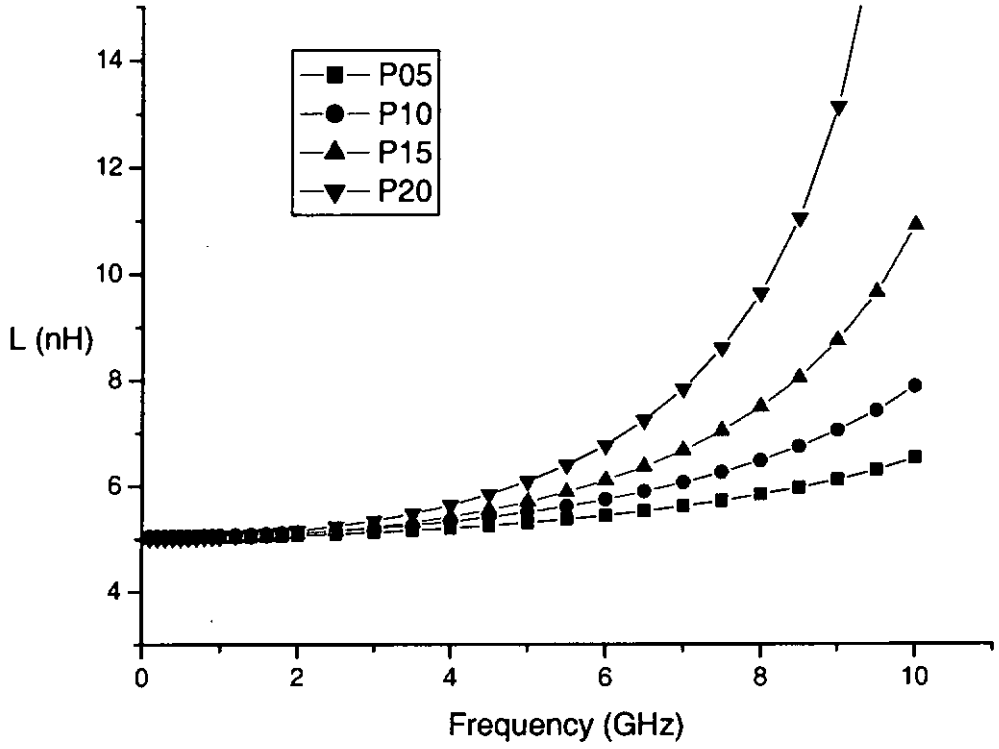


Figure 4.12. Simulated effective inductance of the back-etched planar samples.

The Q factors of the back-etched planar samples shown in Fig. 4.13 are increased more than 200% as compared with samples with substrates. Whereas for 3D samples, the corresponding improvement of Q factors is only 70 - 80%. In addition, the self-resonant frequencies of the samples are increased more than two times of the normal samples.

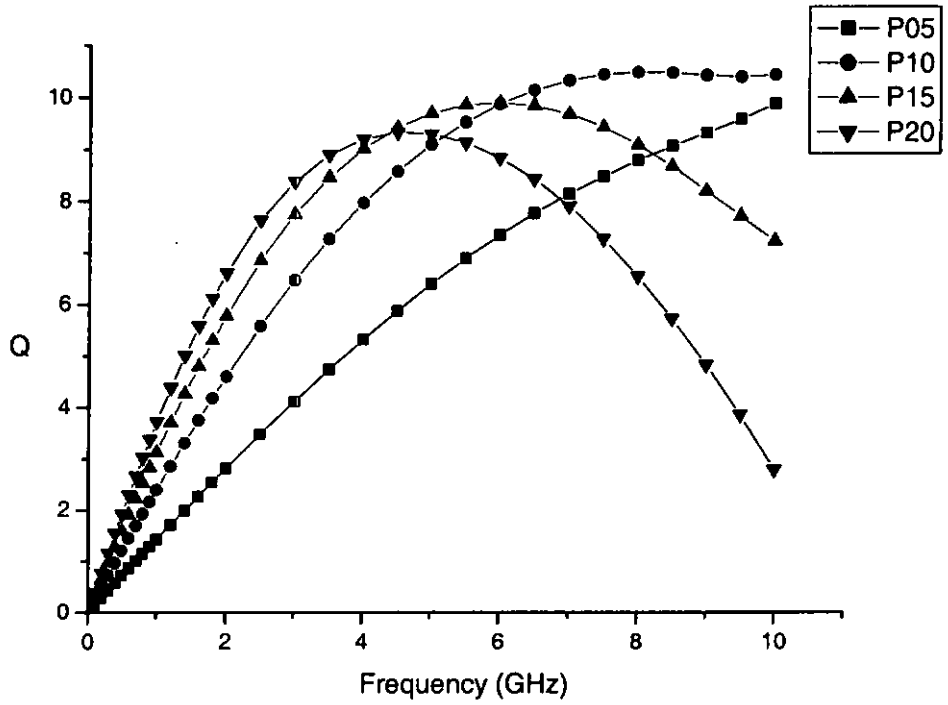


Figure 4.13. Simulated Q factors of the back-etched planar samples.

It is useful to compare the maximum Q factor which can be obtained from planar and 3D inductor. In both type of inductors, Q factors are increased after back-etching of the Si substrate because the eddy current loss in the substrate is eliminated. But the maximum Q factors of the back-etched planar inductors are much higher than that of back-etched 3D inductors with the same inductance. In back-etched samples the loss is only due to the skin and proximity effects in the metal lines. Our results can be explained by that the proximity effects in 3D inductors are more serious than that in planar inductors. This is obviously because in 3D inductor, some metal lines in adjacent layers are closer to each other (separated by SiO_2), as compared to the spacing between metal lines in planar inductors.

4.3 Planar Inductors with Different Turns

The experimental results of three planar inductors with the same inductance but different turns are shown in this section. The samples, T4.5, T6 and T7.5, are planar inductors with 4.5 turns, 6 turns and 7.5 turns respectively. The ratios of their center hole to overall inductor area are 26, 8.6 and 0.6% respectively.

Fig. 4.14 and 4.15 show the effective inductance and Q factors of the three samples. The inductance and Q factors of the samples are very close to each other. The maximum Q factor of T7.5 is slightly lower than that of T4.5 and T6.

In order to maintain the same inductance, T7.5 has more turns and shorter side length compared with other two samples. In all samples, their total length of metal line is about the same. Since the samples are planar inductors with the same metal width, their effective resistance values at low frequencies are almost the same. At higher frequencies, the magnetic field in the center of the spiral is stronger than the field in other parts of the inductor. Thus, the eddy current in the metal lines due to proximity effect will be higher near the center. As sample T7.5 has only 0.6% center-hole ratio, it suffers from more eddy current loss at high frequencies due to more magnetic fields penetrating to the center of the spiral. On the other hand, area of T7.5 is about 7% and 19% smaller than that of T6 and T4.5 respectively. It suffers from less substrate eddy current loss as compared to the others. The combined results of the proximity effect in the metal lines and the substrate loss therefore produce a Q factor which is nearly independent of the number of turns.

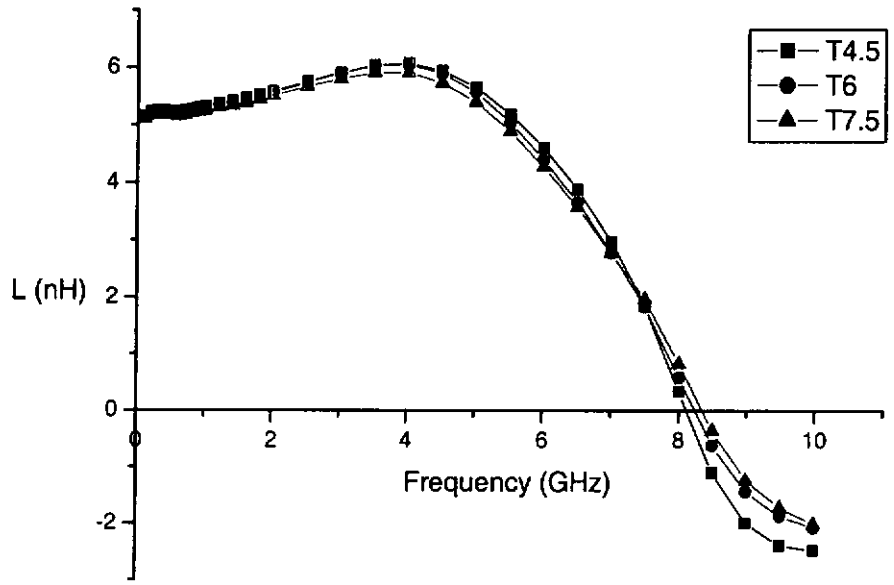


Figure 4.14. Measured effective inductance of the planar samples with different turns.

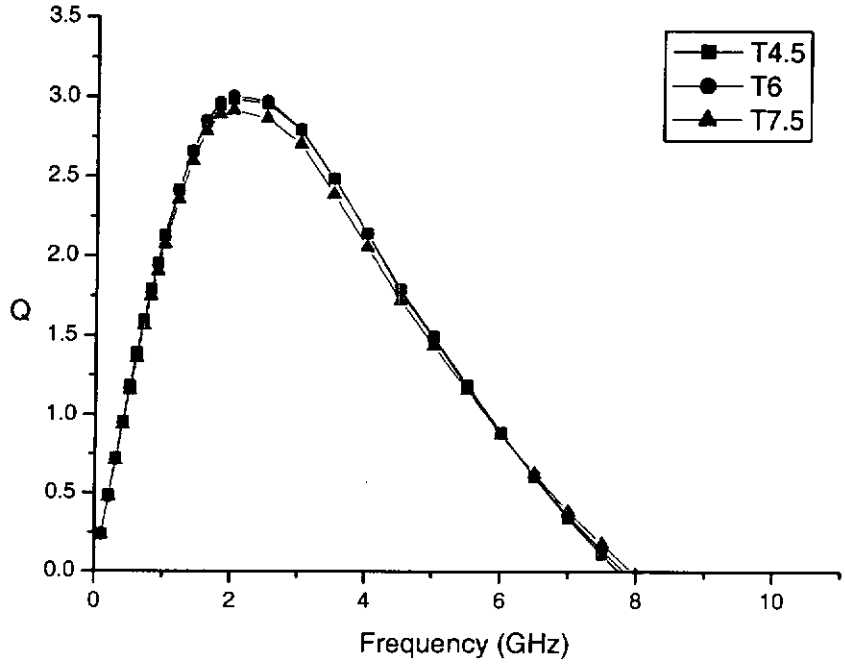


Figure 4.15. Measured Q factors of the planar samples with different turns.

Fig. 4.16 shows the simulated effective resistance of the inductors after the removal of the substrate. The resistance of T7.5 exceeds that of T4.5 and T6 throughout the frequency range. Since the substrate is removed, the substrate eddy current loss is eliminated. The eddy current loss from the skin and proximity effects in the metal lines is the dominated source of resistance loss at high frequency. Since the center-hole ratio of T7.5 is small, more magnetic fields penetrate in the metal turns in the center part of the inductor. The eddy currents at the center metal traces hence increase the overall effective resistance.

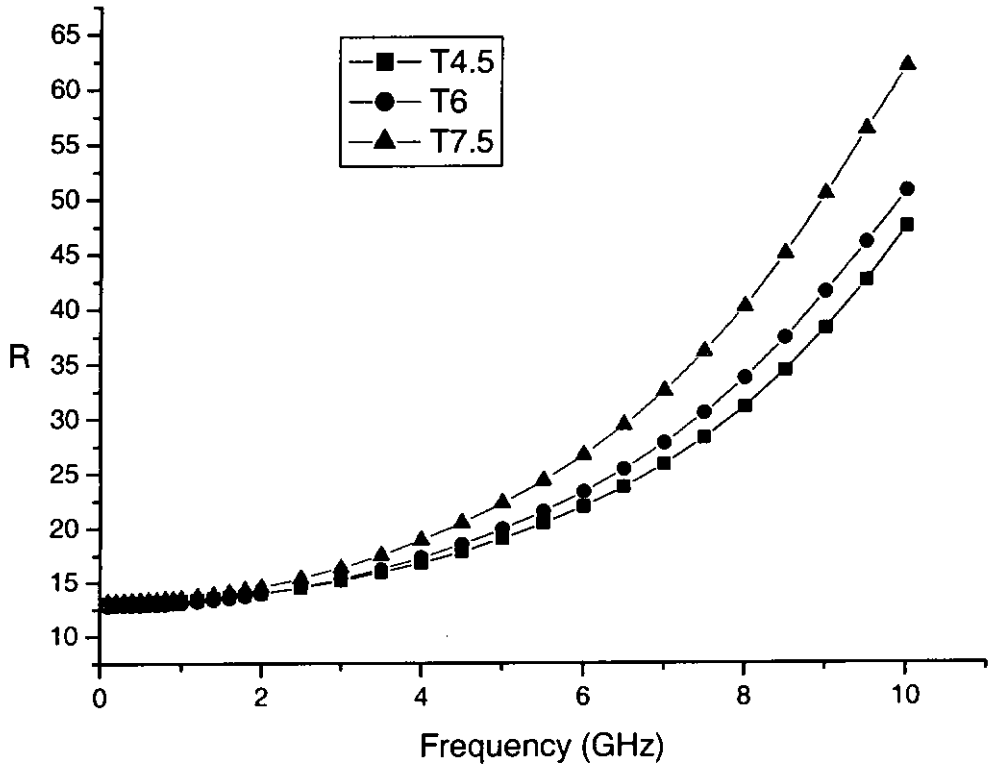


Figure 4.16. Simulated effective resistance of the planar samples with different turns.

The Q factors of the back-etched samples with different turns are shown in Fig. 4.17. T7.5 reaches the peak at about 6 GHz, while T6 and T4.5 reach the peak at 7 and 8 GHz respectively. The peak value of T4.5 and T6 after removing the substrate is 30% and 19% larger than T7.5. T7.5 has the lowest Q factor because of the higher eddy current loss in the metal lines near the center of the inductor.

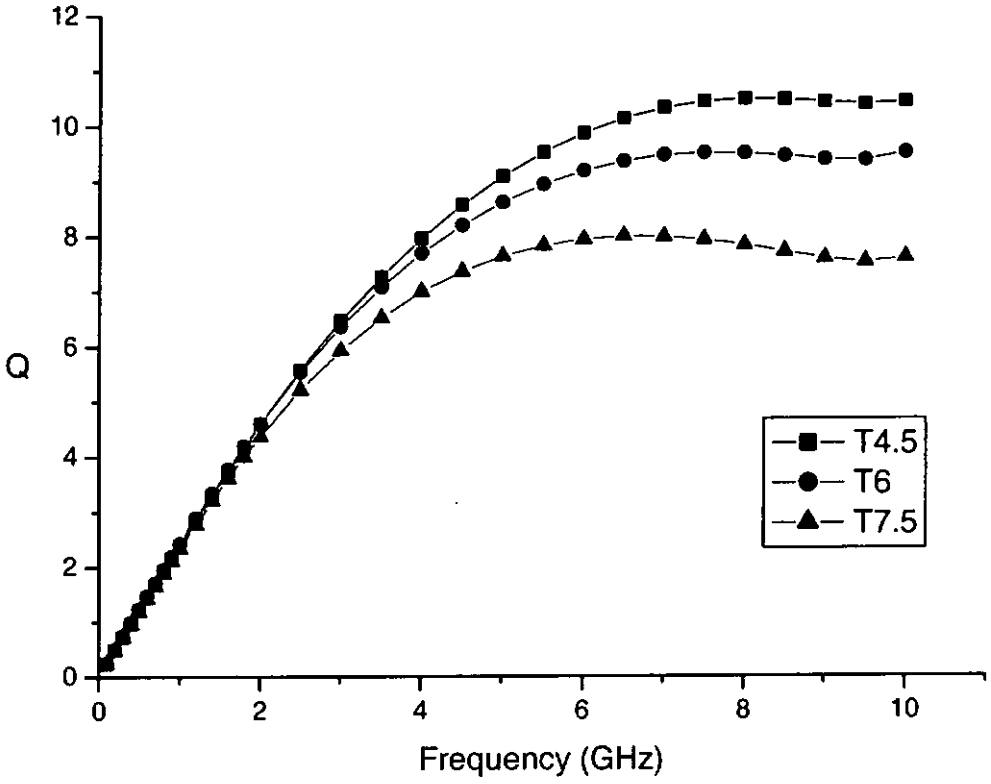


Figure 4.17. Simulated Q factors of the planar samples with different turns.

4.4 Double Layer Inductors with Different Layer Topology

The major benefit of the stacked inductor is its small size. The double layer inductors designed have smaller area compared with the 3D and planar inductors with the same metal width and designed inductance. Its area is about third quarter of the 3D inductors and almost one-third of the planar inductors. The double layer inductors have two 4.75-turn spiral patterns, with the top layer a spiral-in pattern and the bottom layer a spiral-out pattern. The overlapping area of the metal lines between the two layers causes large capacitive coupling between the layers.

Fig. 4.18 shows the effective inductance of the double layer inductors with different layer topology. In sample D31, metal layers M1 and M3 are used. In sample D32, metal layers M2 and M3 are used. Below 1.5 GHz, the effective inductances of D32 and D31 are the same and keep constant at 5 nH. Above 1.5 GHz, the inductance of D32 increases more sharply than D31 and reaches its peak at 3.5 GHz. The inductance of D31 rises gently to its maximum at about 5 GHz. After reaching the peak, they fall rapidly to zero at the self-resonant frequency.

Zolfaghari, as mentioned in Chapter 2, stated that the capacitances of a two-layer inductor can be classified as interlayer capacitance C_1 and bottom-layer capacitance C_2. The equivalent capacitance depends on $(4C_1+ C_2)$ according to his model [42]. Therefore, keeping the spirals further from each other can reduce the capacitive coupling of the inductor. The interlayer capacitance, thus, is important in affecting the effective inductance as well as the self-resonant frequency. In D31, the interlayer

distance was about double of that in D32. From Fig. 4.18, the effective inductance of D32 reaches a peak at 3.5 GHz. Sample D31 with a further interlayer separation has a maximum at 5 GHz.

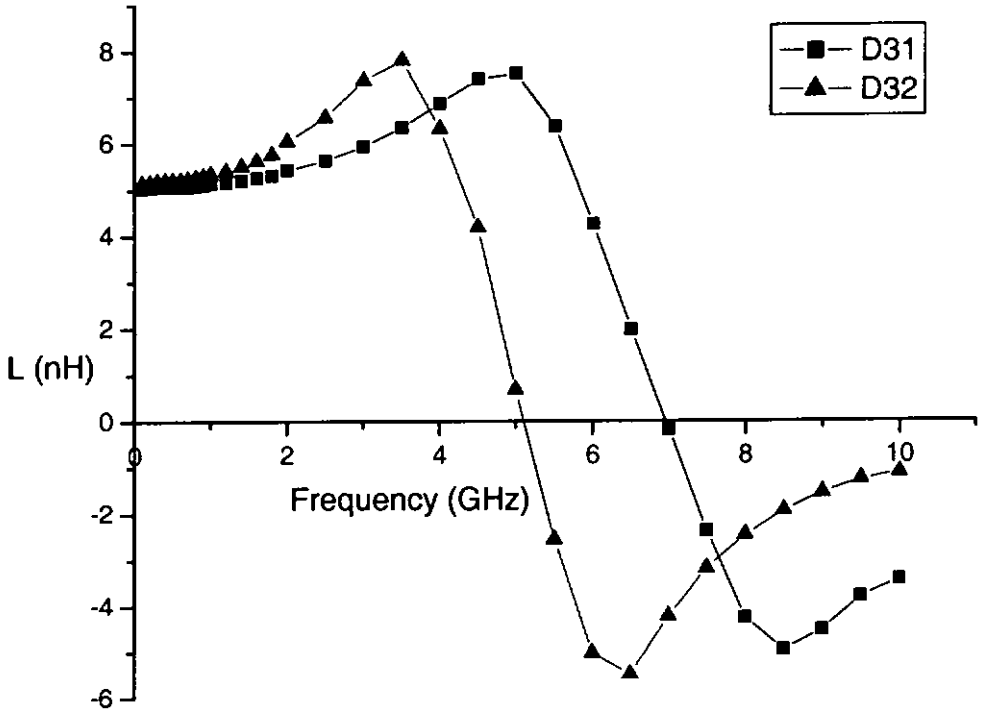


Figure 4.18. Measured effective inductance of double layer inductors with different layer topology.

Fig. 4.19 shows the Q factors of D32 and D31 as a function of frequency. The peak value of Q factor of D31 is slightly larger than that of D32. It also shows that the self-resonant frequency of D31 is about 40% greater than that of D32.

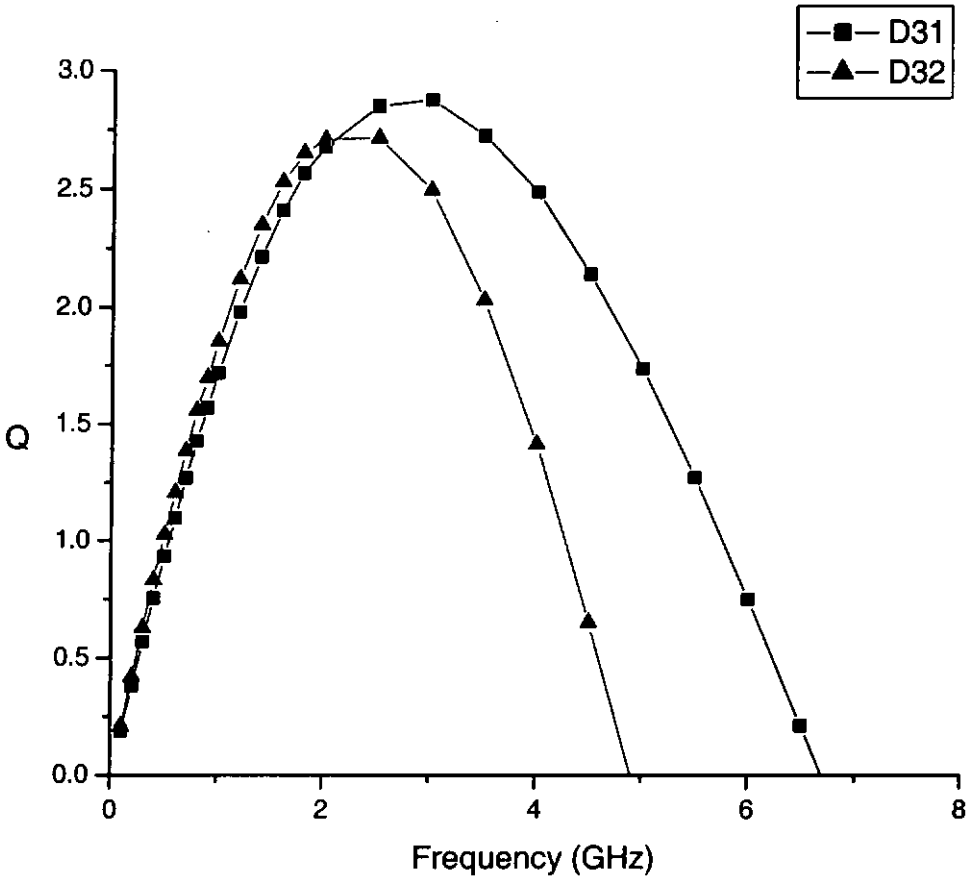


Figure 4.19. Measured Q factors of double layer inductors with different layer topology.

Fig. 4.20 shows the comparison of Q factors of the back-etched and normal double layer samples from the simulation. The Q factors of the samples only increase about 20% after the substrate is removed. The self-resonant frequencies are slightly increased by about 5 %.

Compared to 70 - 80% improvement of Q factors in 3D samples and 200%

improvement of Q factors in planar samples after substrate removal, the substrate eddy current loss is obviously less dominant in the stacked samples. Hence, the proximity effect in metal lines from the adjacent layer is the main loss in the stacked inductor. In addition, the interlayer capacitance is several times larger than the metal-to-substrate capacitance. The removal of substrate eliminates the metal-to-substrate capacitance. However, the interlayer capacitance, which contributes mainly to the effective capacitance, still remains. As a result, there is only a slight increase in f_{SR}.

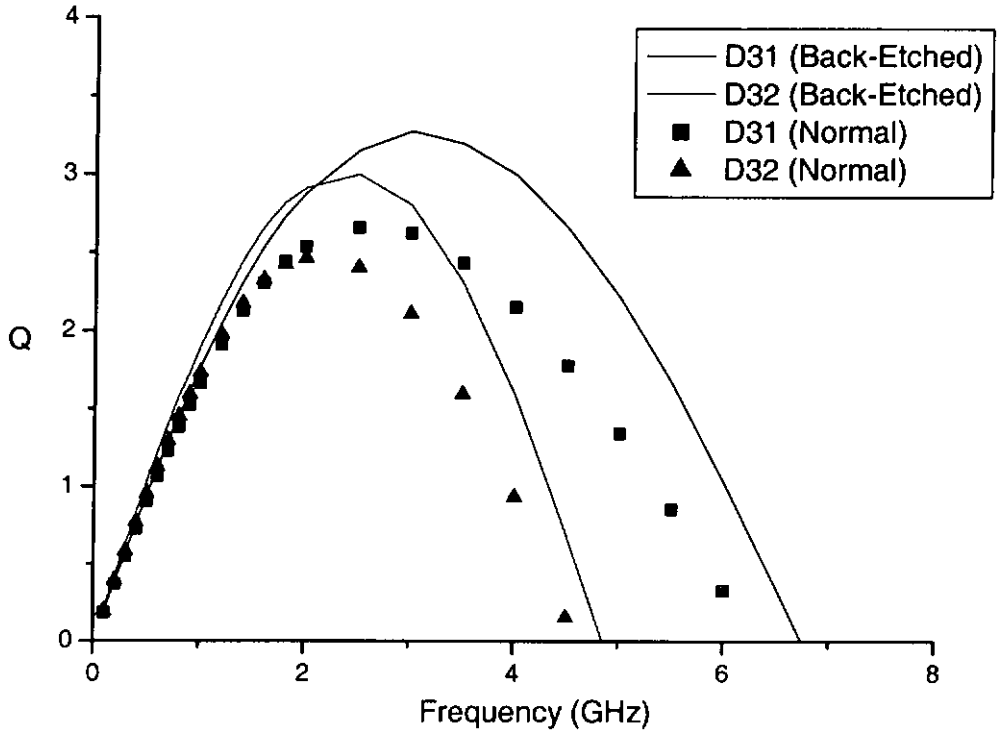


Figure 4.20. Simulated Q factors of back-etched and normal double-layer inductors.

Double-layer inductors with different layer topology constructed on five metal layers CMOS were also simulated. Fig. 4.21 shows the Q factors of the samples from the simulation. For example, in S53, M5 is the metal layer where the double-layer inductor spirals in and M3 is the metal layer where it spirals out.

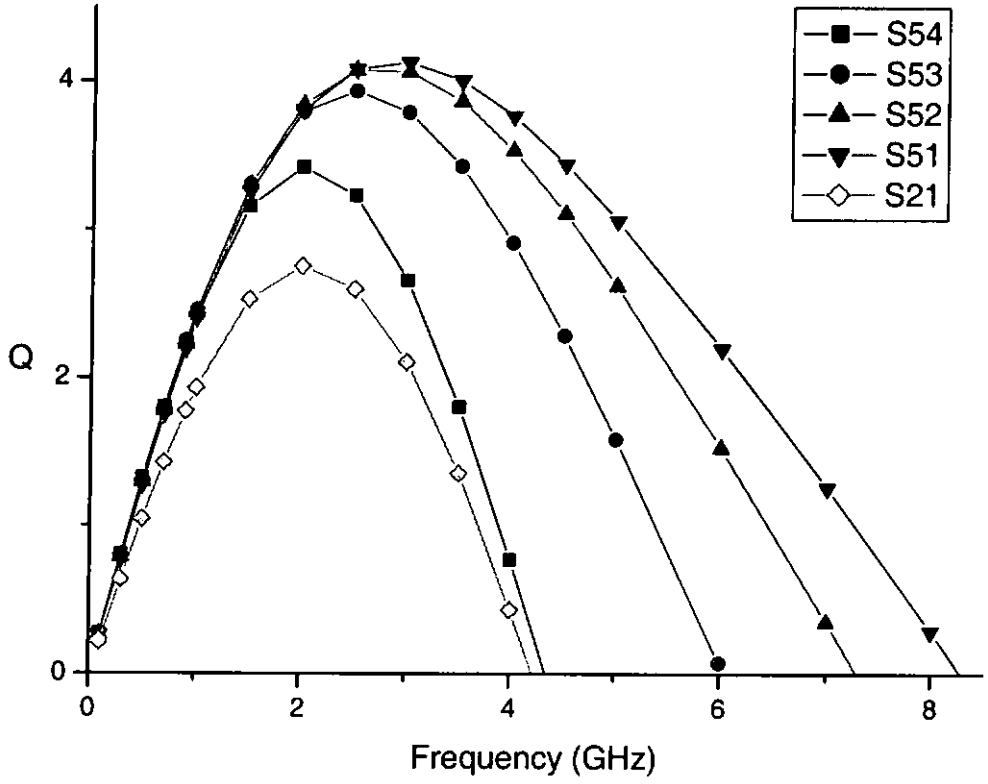


Figure 4.21. Simulated Q factors of double-layer inductors with different layer topology.

Since shorter interlayer distance will result in larger loss due to the proximity effect in metal lines from the adjacent layer, S21 and S54 have low Q factor. Although

the interlayer distances in S21 and S54 are same, the spiral layers of S21 are closer to the substrate, therefore producing higher substrate eddy current loss. Hence, the Q factor of S21 is smaller than that of S54. The highest Q factor occurs in S51, which has the largest interlayer distance but one layer is closest to the substrate. So it infers that the proximity effect in metal lines is a more dominant loss compared to the substrate eddy current loss.

4.5 Comparison between Different Structures

Table 4.1 shows the comparison of 3D, planar and double layer inductor with the same metal line width of $10\,\mu m$. The peak Q, peak Q frequency and self-resonant frequency of the normal and back-etched samples from simulation are presented. All samples have an inductance of 5 nH at low frequencies.

	M10	P10	D31
Area (μ m)	$(143)^2$	$(212)^2$	$(123)^2$
Peak Q (Normal)	3.2	2.94	2.58
Peak Q (Back-etched)	5.32	10.48	3.27
% Increase	66%	256 %	26.7 %
f_{max} (Normal) (GHz)	2.9	1.9	2.5
f_{max} (Back-etched) (GHz)	8.3	7.9	3
% Increase	186%	315 %	20 %
f_{SR} (Normal) (GHz)	8.7	6.9	5.9
f_{SR} (Back-etched) (GHz)	>10	>10	6.7
% Increase	>100%	>100 %	13.6 %

Table 4.1. Simulation results of the inductors with different structures.

The planar inductor, P10, gets great improvement in performance after the substrate is removed. The Q factor and peak Q frequency in the back-etched P10 sample increase about 3 to 4 times compared to the normal sample. Unlike 3D and

double layer inductor, the size of the planar inductor is large so that it suffers from large substrate eddy current loss at high frequencies. Removing the substrate totally eliminates this loss. At the same time, because of the structure of the planar inductor, the proximity effect from adjacent metal lines is smaller. Hence it has the highest Q factor after back-etching. However, the disadvantage of the planar inductor is its large size. Extending the spiral pattern to the center of the inductor can slightly reduce the inductor size. Nevertheless, the eddy current in the metal lines due to proximity effect produced at the center will lower the Q factor of the back-etched planar inductor.

For the double layer inductor, D31, the main loss in the inductor is the interlayer proximity effect. The substrate eddy current loss is only minor due to its small inductor size. This can be observed by the results when the substrate is removed. The Q factor and the peak Q frequency only increase by 20 % and the self-resonant frequency is almost the same.

The 3D inductor, M10, benefits both from small inductor size and high Q factor. Its structure fully uses the three metal layers, thus it has only about half the size of the planar inductor. Hence, it suffers from less substrate eddy current effect. In addition, the 3D inductor has only two turns for each layer. Its center-hole ratio is large to avoid most of the proximity effects of the metal line at the center of the inductor. As a result, it gets the highest Q factor, peak Q frequency and self-resonant frequency in normal samples. The size of the 3D inductor can further diminish as the number of metal layers increases. After the substrate is removed, the substrate loss is eliminated. The proximity effect from adjacent layers becomes dominant. Its Q factor increases about

66% and is just about a half of the planar inductor. The peak Q frequency is also the highest among all the structures.

Chapter 5

Conclusions

5.1 Conclusions

The project is aimed at studying the different factors which optimize the performance of integrated on-chip inductors for RF CMOS circuits. The inductors investigated include planar, stacked and 3D structures with varied metal widths, layer topology and number of turns. The inductor samples were fabricated using standard $0.6\,\mu$m CMOS process with 3 metal layers, and then characterized by a network analyzer up to 10 GHz. The S parameters exported from the analyzer were used to extract the effective resistance, effective inductance and Q factor. The measured results agreed well with those from a numerical simulation program, MicroWave Office. Simulation was also used to study the performance of the samples after the Si substrate was removed.

We show that both planar and multi-layer inductors with varied metal widths have optimum Q factors at different operation frequencies. Inductors with narrower metal width suffer from higher series resistance at low frequencies but have better performance at higher frequencies. However, inductors with wider metal width suffer from larger eddy current loss at high frequencies, but benefit at lower frequencies. This is the consequence of two combined effects: on one hand, the series resistance of metal lines is lowered as the width is increased; and on the other hand, the losses due

to proximity effect of metal lines and eddy current in the substrate increase with the metal width.

Planar inductors with different number of turns designed to have the same inductance were found to have similar performance. Sample with less turns have lower ratio of outer to inner radius, but this is offset by the disadvantage of larger inductor areas.

Simulations were used to analyze the inductors after the substrate removal. It shows that Q factor is improved for all types of inductor due to the absence of the eddy current loss in the substrate. Planar inductors have the greatest improvement of Q factor. Multilayer inductors get less improvement since the proximity effect from adjacent metal layers is still a main cause of loss in the inductors. In addition, different topologies of the double-layer stacked inductors have been studied. The result shows that increasing the interlayer spacing can improve the Q factor by reducing the proximity effect from adjacent metal layers.

Comparing the three types of inductors, it is found that the back-etched planar inductor has the highest Q factor. It suffers from least proximity effect from adjacent metal lines after etching of the substrate. The drawback is its large size. The 3D inductor has comparatively high Q factor as well as small inductor size. It also has the highest peak Q frequency and self-resonant frequency.

5.2 Suggestions for future work

In order to design inductors with optimized performance, analytical models are very useful for fast evaluation. However, analytical models which can represent accurately the losses in the metal lines and the substrate, especially in multi-layer structures are still not well developed. Further work is needed in this direction to enhance the design of on-chip inductors.

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