Design of Integrated Circuits for Switching Power Supply with Power Factor Correction

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ABSTRACT

This is a Teaching Company Scheme between The Hong Kong Polytechnic University and ON Semiconductor Ltd.

In this project two new circuits of AC-DC regulators with power factor correction have been proposed and thoroughly studied. Hardware prototypes of both circuits have been constructed, evaluated and compared with ordinary circuits.

The first circuit, "A novel ZVS switching mode power supply with Power Factor Correction", employs a special converter topology and a unique gate drive sequence (for MOS switches) to achieve both power factor correction and soft switching. The new circuit is capable of regulating the output for a wide range of loading current and has a fast transient response. A patent application on this design has been filed.

The second circuit, "A Pulse Skip Modulation PFC controller", uses a pulse skip method to control the average input current and to reduce the voltage stress of both active and passive components (e.g., electrolytic capacitors and switching transistors). In this way a high power factor, a better reliability and a lower cost can be obtained simultaneously. The power factor correction function is well maintained over a wide range of loading current.

Both of the two new circuits operate at fixed switching frequency. This makes the design of EMI filters much easier, when compared with a variable-frequency converter.

As an important objective of this Teaching Company Scheme, the controllers for the above-mentioned new circuits are to be integrated into IC form. Therefore the controller and driver circuits have been designed in such a way that they can be readily fabricated as ICs using existing technologies.

ACKNOWLEDGEMENTS

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It has been my pleasure to associate with the faculty, staff, and graduate students at The Hong Kong Polytechnic University (PolyU). I thank all of them for their friendship, which made my staying in PolyU enjoyable.

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CHAPTER 1
INTRODUCTION

Due to the rapid increase in the number of electronic equipment / appliances, the related power consumption is always increasing. In many countries, one of the reasons that cause power failures is that too many appliances with poor power factor (P.F.) are connected to the power line (e.g. televisions and personal computers). As a result, unexplained power failures occur, even if the power consumption is not overloaded. This is due to the poor power factor of electronic equipment / appliances. For example, if the power factor of an electronic product is 0.5, it means the apparent power is two times as large as the real power.

Electronic appliances usually employ switching mode power supplies (SMPS), because they have small size and can achieve high efficiency. The power factor of a switching mode power supply without power factor correction (PFC) is low, typically 0.65. Therefore the power factor of the power system becomes low.

To solve this problem, several regulations have been introduced. The European Union published its Directive 89/336/EEC for electromagnetic compatibility (EMC) in 1989. One of the key requirements for European Community (CE) approval is to limit the harmonic emissions that couple into the AC line supply. This requirement has been effective since January 1, 2001 in the form of European Normative (EN) EN61000-3-2 [1]. Although earlier and similar standards such as EN60555-2 targeted the domestic environment, EN61000-3-2 extends its scope to include common office equipment. It also tightens limits for devices that draw maximum power around the crest of the sine wave in the AC line supply.

In this chapter, the definition of power factor, its relation to the harmonic distortion and the limitation of the IEC1000-3-2 standard [1], will be introduced. Regarding the current harmonic distortion problems in power line, different circuits for improving the harmonic current have been designed [2][3][5]. These circuits reduce the losses of the power transmission line, increase the power transmission line capacity and

maintain a better voltage regulation. Major findings include solutions using active or passive power factor correction circuits, which will be introduced in Chapter 2.

1.1 Definition of power factor and total harmonic distortion

The power factor is defined as the ratio of the power P (averaged over a line cycle) to the product of the rms line voltage, V_{rms}, and the rms line current, I_{rms}.

$$PF = \frac{P}{V_{rms} I_{rms}} \tag{1-1}$$

A poor power factor can be due to a phase shift between the voltage (assumed sinusoidal) and the fundamental component of the current. It can also be due to the presence of harmonics in the current. The power factor can be written as

$$PF = PF_{disp} PF_{dist} \tag{1-2}$$

where PF_{disp} is the displacement factor and PF_{dist} is the distortion factor.

For a sine wave current , the power factor can be expressed as

$$PF_{disp} = \cos\phi = \frac{P}{V_1 I_1} \tag{1-3}$$

where P is the average power, PF_{disp} is the displacement factor, V_1 is the rms value of the fundamental voltage , I_1 is the rms value of fundamental current, and ϕ is the phase angle between voltage and current. The harmonic distortion can be due to the nonlinear nature of the rectifier and/or the discontinuous switching waveform. The total harmonic distortion (THD) is defined as

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \tag{1-4}$$

where I_1 is the rms value of the fundamental current, and I_n is the rms current of the nth harmonic current. The distortion factor has the following relationship with the total harmonic distortion (THD):

$$PF_{dist} = \frac{1}{\sqrt{(1 + THD^2)}} \tag{1-5}$$

For example, a power factor of 90 % corresponds to a THD of 48.4 %.

1.2 Classification of equipment

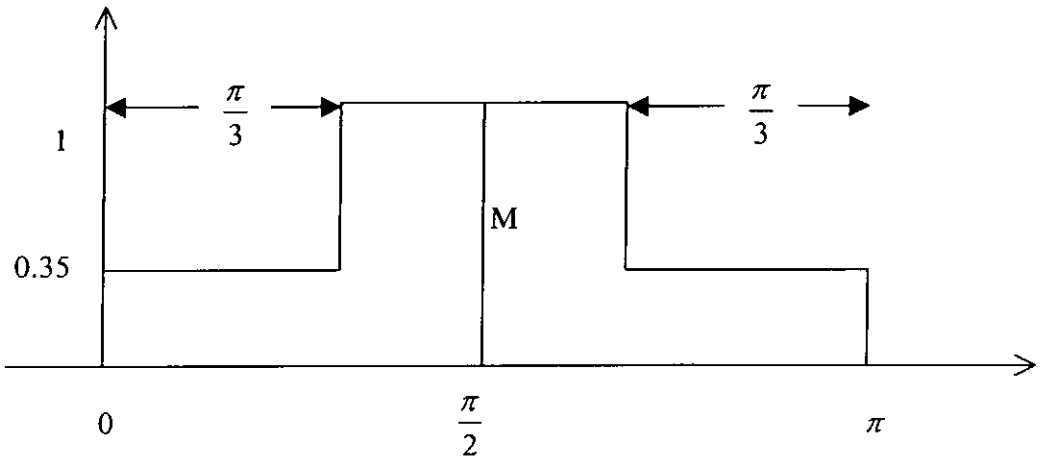
In the European Standard EN 61000-3-2 [1], there are four classes of equipment:

Class A: Balanced three-phase equipment and all other equipment, except those stated in one of the following classes.

Class B: Portable tools

Class C: Lighting equipment, including dimming devices.

Class D: Equipment having an input current with a "special wave shape" as defined in Figure 1 and an active input power, $P \leq 600$ W, measured under the type test conditions given in the relevant clause of the European standard publication.



Each half cycle of the input current is within the envelope for at 95% of the time.

The centerline, M, coincides with the peak value of the input current.

Figure 1 Envelope of the input current with "special wave shape", which is defined as Class D

For each of the four classes of equipment there is a specific set of requirements on the harmonic current emission.

1.3 Harmonic current emission limits

The harmonic limits are applicable to electrical and electronic equipment having an input current up to 16A per phase, and intended to be connected to public low-voltage distribution system.

1.3.1 Limits for Class A equipment

For the Class A equipment. The harmonics of the input current shall not exceed the absolute values given in Table 1.

Harmonic order	Maximum permissible harmonic current [A]
3	2.30
5	1.14
7	0.77
9	0.40
11	0.33
13	0.21
$15 \le n \le 39$ (odd harmonic only)	$0.15 \times \frac{15}{n}$
2	1.08
4	0.43
6	0.3
$8 < n < 40$	$0.23 \times \frac{8}{n}$

Table 1 Limits for Class A equipment.

1.3.2 Limits for Class B equipment

For Class B equipment, the harmonic of the input current shall not exceed the maximum permissible values give in Table 1 multiplied by a factor of 1.5.

1.3.3 Limits for Class C equipment

The harmonic current limits of the light equipment and dimming devices should not exceed the limits given in Table 2.

Harmonic order N	Maximum permissible harmonic current expressed as percentage of the input current at the fundamental frequency
2	2
3	30λ*
5	10
7	7
9	5
$11 \leq n \leq 39$ (odd harmonics only)	3
*λ is the circuit power factor	

Table 2 Limits for Class C equipment

1.3.4 Limits for Class D equipment

For Class D equipment, the limits of harmonic current are defined for the rated load condition. The harmonic current shall not exceed the values that can be derived from Table 3.

Harmonic order	Maximum permissible harmonic current per watt [mA/W]	Maximum permissible harmonic current [A]
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.4
11	0.35	0.33
13	0.296	0.21
$15 \le n \le 39$ (odd harmonic only)	$\frac{3.85}{n}$	$0.15 \times \frac{15}{n}$

Table 3 Limits for Class D equipment.

CHAPTER 2

POWER FACTOR CORRECTION CIRCUITS

Most off-line switching mode power supplies use the bridge rectifier with a bulk input filter capacitor to obtain a DC voltage from the AC line. The diagram of an SMPS and its associated waveforms are shown in Figure 2. The bulk capacitor is used to reduce the ripple of the rectified voltage and to meet the holdup requirement.

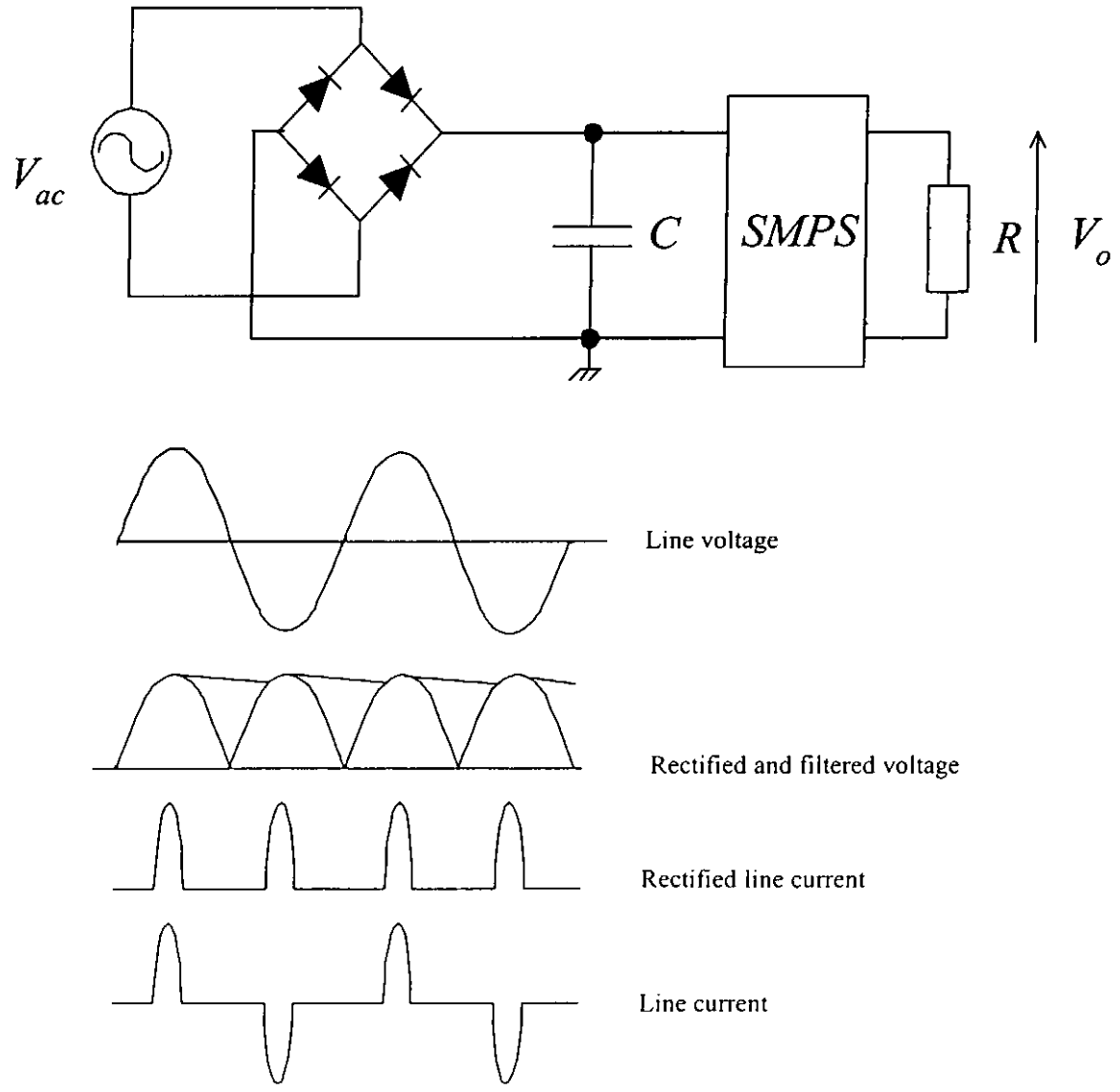


Figure 2 Block diagram of an SMPS and its associated waveforms

Figure 2 shows that a conventional SMPS will draw a pulsing line current. It will generate a lot of harmonic contents in the transmission line and increase the loss of the transmission line. The reasons for which the harmonic contents of the load current should be minimized are as follows:

- High peak currents will make the power supply inefficient. The power supply will have to be over-rated to deliver the peak current even if the mean current is well below the peak. This limits the power that can be drawn from the power supply to well below its full potential.
- The high peak currents cause problems with electronic circuit breakers (ELCBs). Such circuit breakers tend to trip out when the mains current becomes badly distorted.
- The high harmonic contents increase the neutral current in a three-phase system, which can cause safety trips to be activated.

To improve the above mentioned harmonic distortion problems, a power factor correction circuit can be added to the conventional SMPS. In general, there are two approaches to improve the harmonic contents, namely the passive approach and the active approach. In this chapter both approaches for power factor correction in line-fed power supplies will be introduced. The advantages and disadvantages of both approaches will also be discussed.

2.1 Passive methods

The simplest approach to improve the power factor of a power supply and to reduce the harmonic content is to use a passive filter. This can be done by adding a large inductance L between the AC mains and the diode bridge circuit [10], as shown in Figure 3. This circuit may increase the power factor up to 90% [1].

The optimal inductance and capacitance values are

$$L_{opt} = 0.03\frac{V^2_{ac(rms)}}{f \cdot P} \tag{2-1}$$

$$C_{opt} = 0.12\frac{P}{fV^2_{ac(rms)}} \tag{2-2}$$

where $V_{ac(rms)}$ is the line voltage, f is the line frequency, and P is the output power. With the optimal inductance, the output voltage is about 72% of peak the voltage [11].

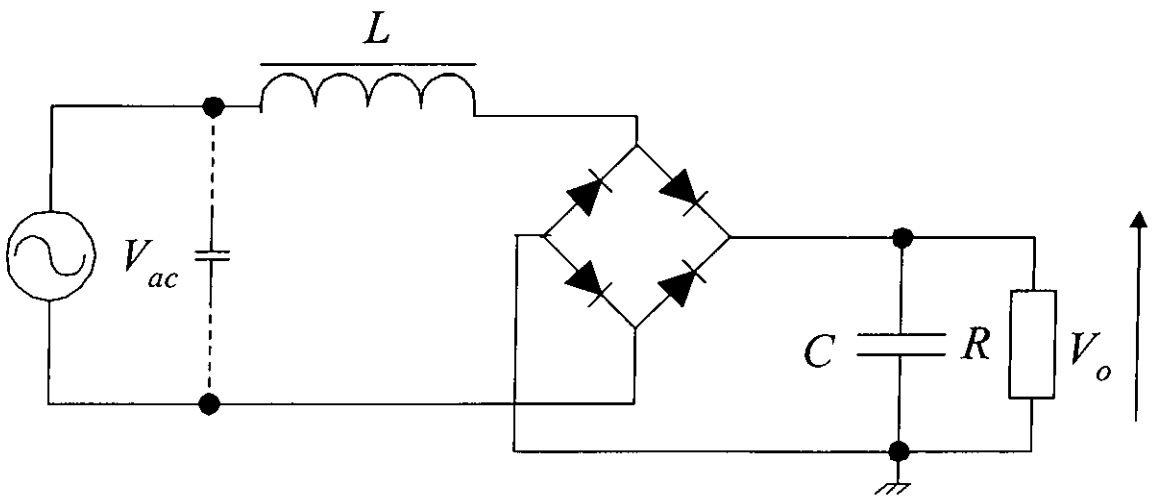


Figure 3 Rectifier with filter inductor.

To improve the performance of the circuit, a C_2 can be added as shown in Figure 4. Here inductor L and capacitor C_2 form a parallel resonator, which is tuned at the third harmonic for improving the power factor. By using a suitable component in this approach, this circuit can achieve a power factor of 0.96.

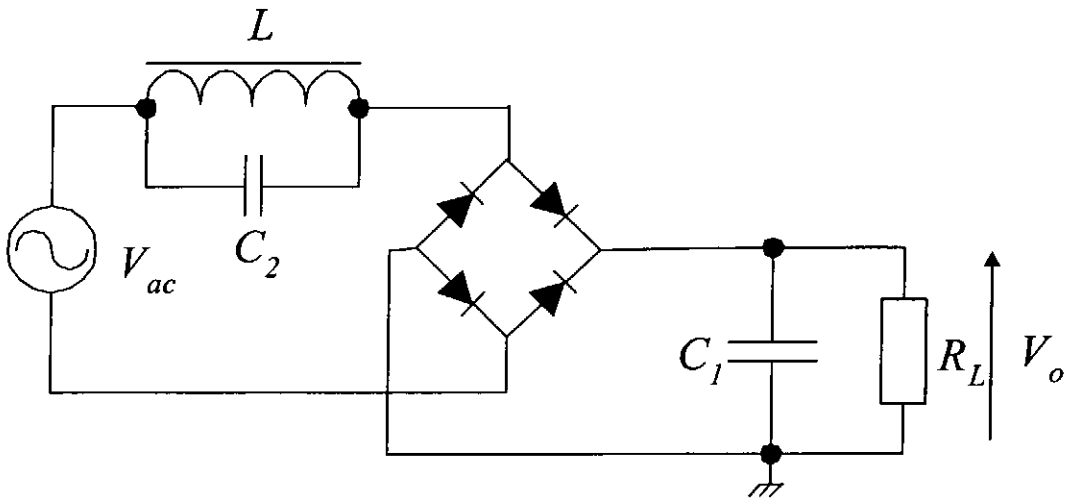


Figure 4 Rectifier with parallel resonant filter

Another passive method to solve the harmonic problems is to use a "valley fill" circuit, which is shown in Figure 5. This circuit uses two output capacitors C_1 and C_2, connected in series. During operation, one of the capacitors will be discharged first. When the line voltage drops below 50% from its peak value, then the other capacitor fills the valley and preventing the output voltage from going to zero. Under this condition, the input current becomes less pulsating (i.e., less harmonic components). This circuit can reduce about 75% of the harmonic distortion. It offers a simple solution for those applications in which the a high ripple voltage can be tolerated, e.g., electronic ballasts.

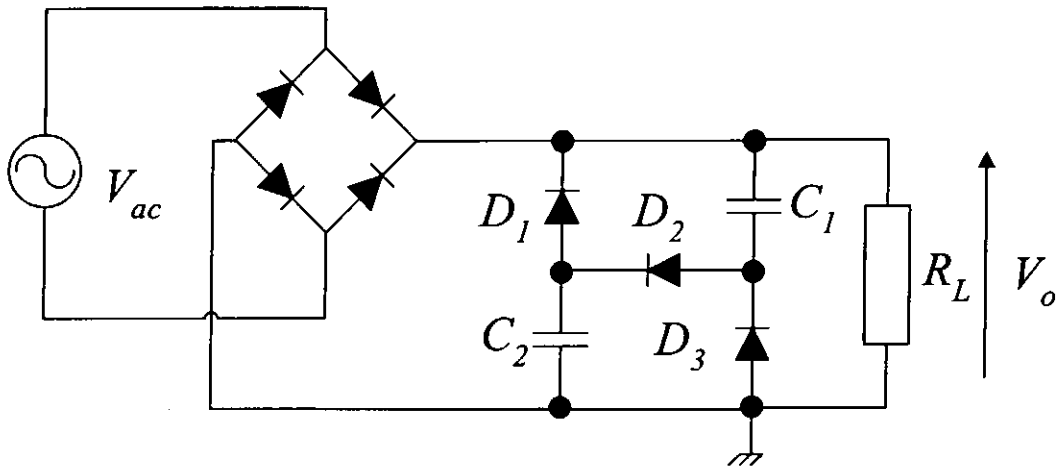


Figure 5 Valley fill circuit

The passive filter method is simple and reliable, and it produces less electromagnetic interference (EMI). However, the disadvantages are large size, load-dependent power factor, and poor dynamic response.

2.2 Active methods

Although passive PFC can help solve the harmonic problems, practically it is only suitable for low power applications below 30 W. For higher power applications, the passive methods need a bulky magnetic device. Also, it is not a suitable solution for appliances operating with wide input voltage range.

High switching frequency (over 30 kHz) active PFC circuits provide a possible solution to reduce the harmonic current emissions in high power applications. High switching frequency can increase the power density, reduce the size/weight of magnetic devices, and reduce the size of the output capacitor. Therefore, for high power applications, active PFC is a better solution. In active PFC methods, an AC-DC pre-regulator is added between the bridge and the DC-DC converter, as shown in Figure 6. Using the current feedback control, the input current is controlled so that it will follow the input sine wave voltage. Active PFC can reduce the total harmonic distortion to less than 5 % and increase the power factor up to 0.99 or higher.

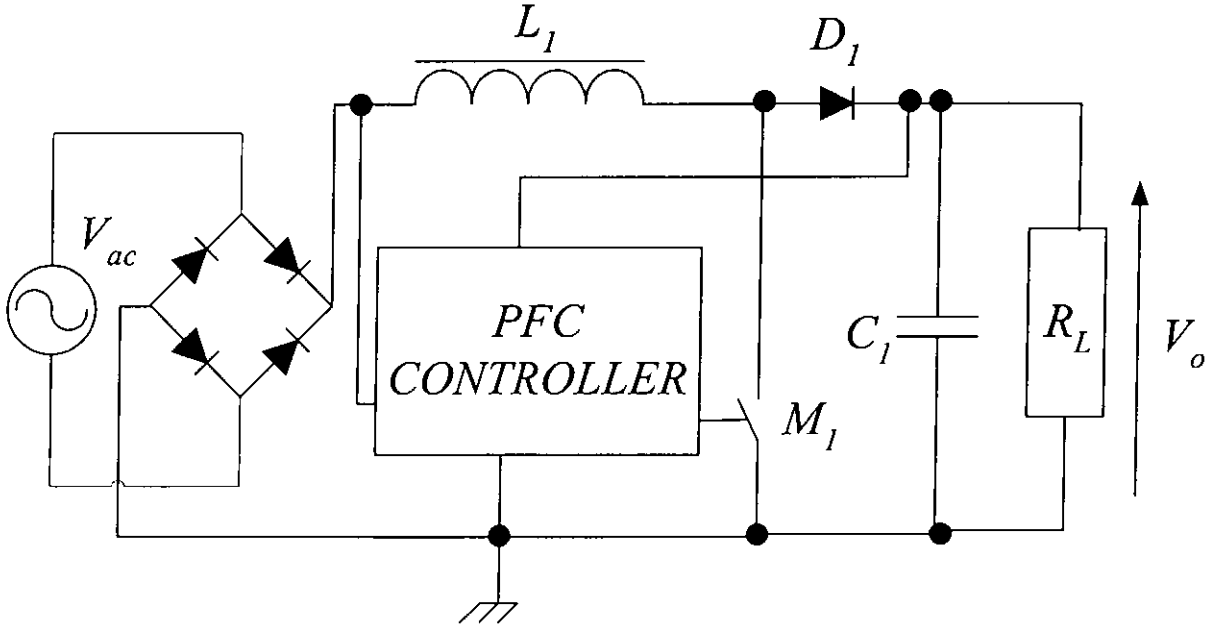


Figure 6 Basic boost power-factor corrector.

Another advantage of active power factor correction is that it can provide a wide input voltage range (90 - 240 V_{ac}) and a DC output voltage, which is stabilized to nearly constant value for large variations of line voltage. However, active PFC generates higher electromagnetic interference (EMI). A typical non-isolated power factor correction circuit is shown in Figure 7.

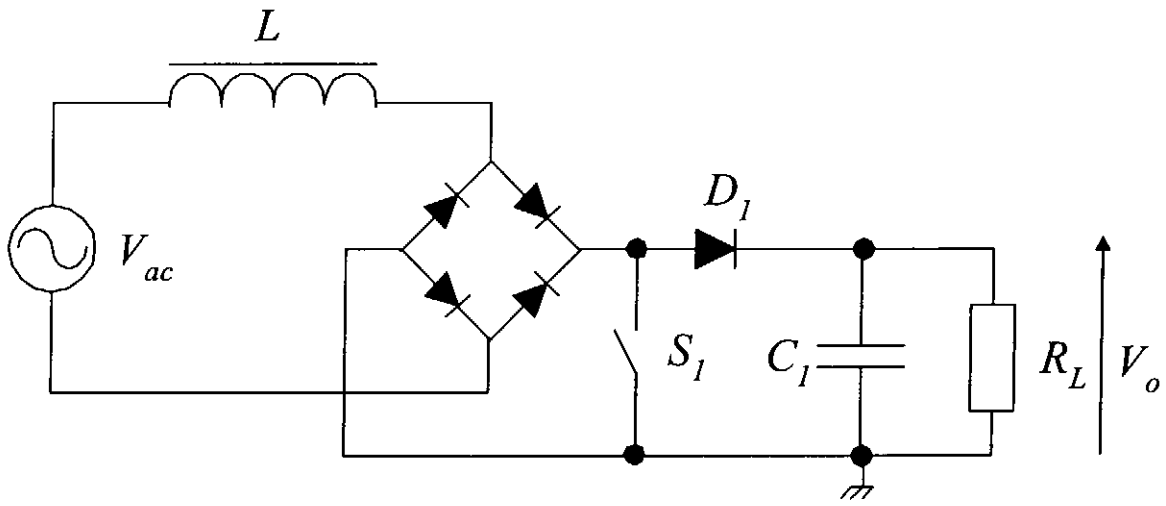


Figure 7 Non-isolation power factor correction circuit.

2.2.1 Review of previous works for active PFC

Today, active PFC is widely used in AC-DC switching power supplies, electronic ballasts, and uninterrupted power supplies (UPS). In general, power factor correctors are divided into two categories, isolated power factor correctors and non-isolated power factor correctors. Both non-isolated correctors and isolated correctors will be discussed.

2.2.2 Non-isolated correctors

When comparing with the isolated correctors, a non-isolated corrector can provide a higher efficiency and has less component count. Here five types of correctors, boost corrector, buck corrector, buck-boost corrector, Ćuk and SEPIC corrector will be briefly introduced.

2.2.2.1 Boost corrector

The circuit of a boost power-factor corrector is shown in Figure 8. It is the most popular non-isolated topology. A boost corrector can provide a high efficiency and a tight control over the line-current waveform. It requires a small storage capacitor and uses ground-referenced switch. The main drawback of the boost converter is that it is difficult to provide over current protection. Moreover, the output voltage is always higher than the peak input voltage.

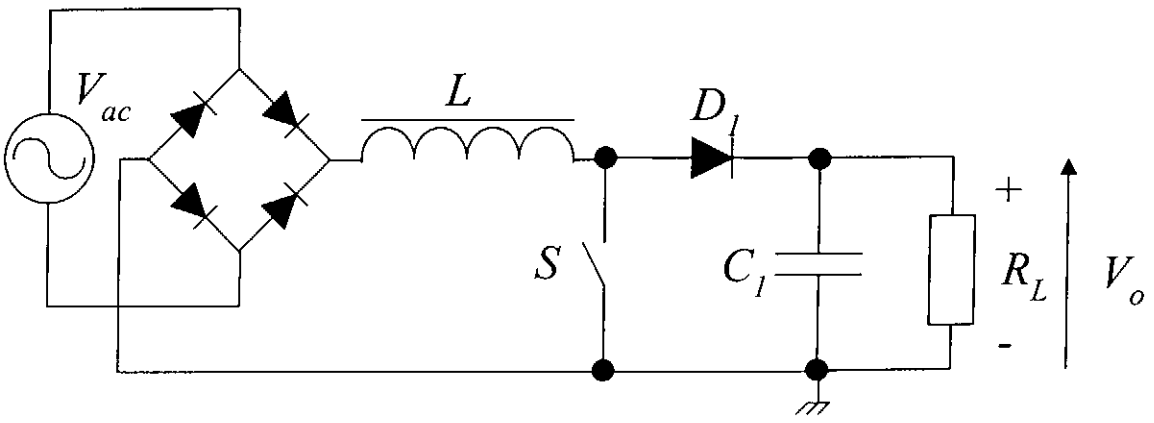


Figure 8 Boost power-factor corrector.

2.2.2.2 Buck corrector

The circuit of a buck power-factor corrector is shown in Figure 9. A buck corrector can provide a lower output voltage compared with the boost corrector. Although the circuit does not have the two drawbacks of the boost converter, it has the disadvantage of requiring a floating switch. The switch RMS current is also higher than that of the boost corrector for a given output power. Another major disadvantage of the buck corrector is that it stops drawing line current form the source when the input voltage is lower than the output voltage. This results in an imperfect power factor correction.

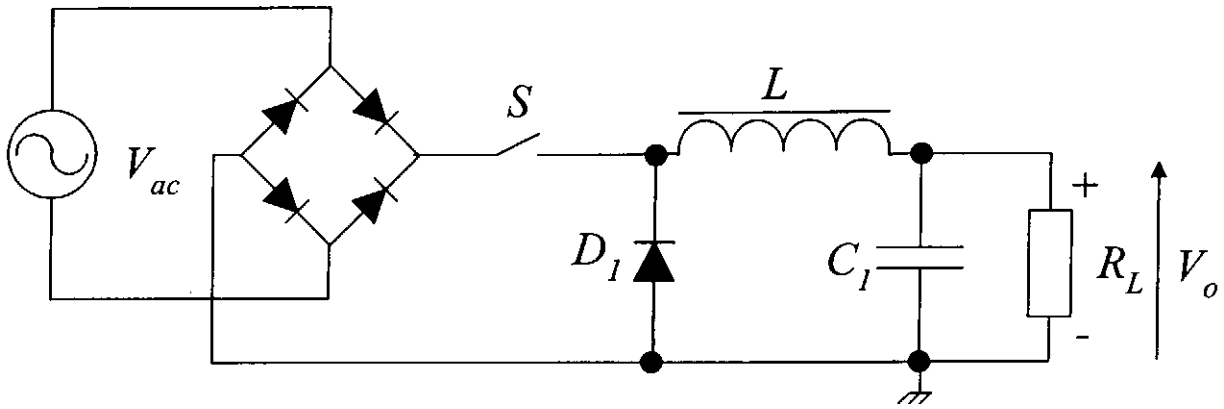


Figure 9 Buck power-factor corrector.

2.2.2.3 Buck-boost corrector

The circuit of a buck-boost corrector is shown in Figure 10. The advantage of the buck-boost corrector is its ability to achieve low line-current distortion and low output voltage similar to a buck corrector. But a buck-boost corrector needs a floating switch. Another problem of this circuit is the high EMI and RMS current. Also the circuit is inefficient.

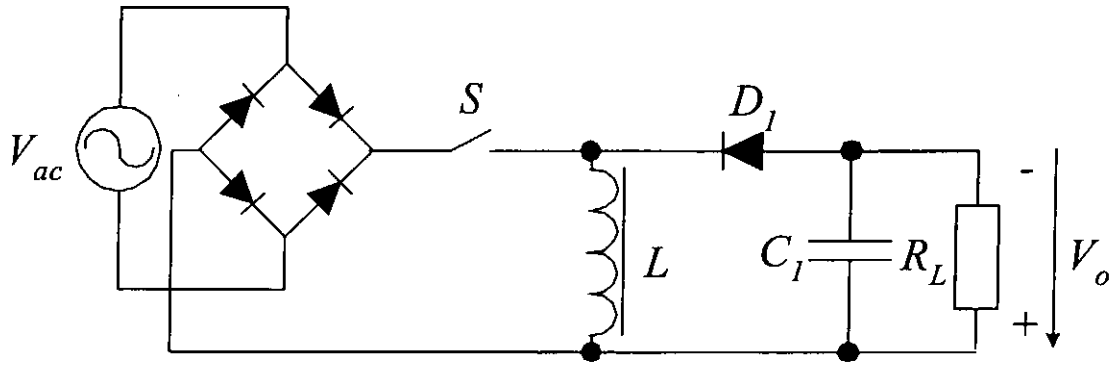


Figure 10 Buck-boost power-factor corrector.

2.2.2.4 Ćuk and SEPIC correctors

The circuits of Ćuk and SEPIC correctors are shown in Figure 11 and Figure 12. The voltage-boosting capability of these converters is desirable in some corrector applications. However, these correctors use more components and have higher voltage and current stresses.

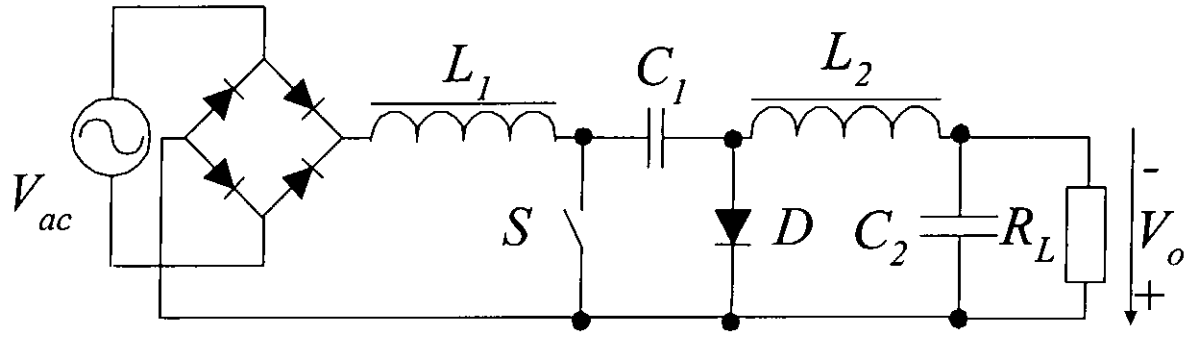


Figure 11 Power-factor corrector (Ćuk)

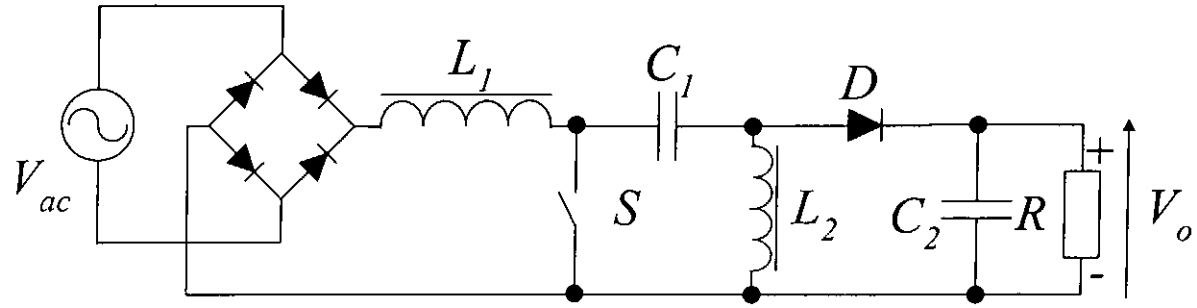


Figure 12 Power-factor corrector (SEPIC)

2.2.3 Isolated correctors

2.2.3.1 Basic isolated converters

An example of boost isolated power factor corrector is shown in Figure 13 [19]. For isolated power factor correctors, transformers are used to isolate the input and output stage. However, there are some disadvantages for this approach. For example, the energy storage requires a large capacitor at low output voltage. Also, the leakage inductance of the isolating transformer will cause a high voltage overshoot across the main switch. It needs a suitable snubber to reduce the overshoot.

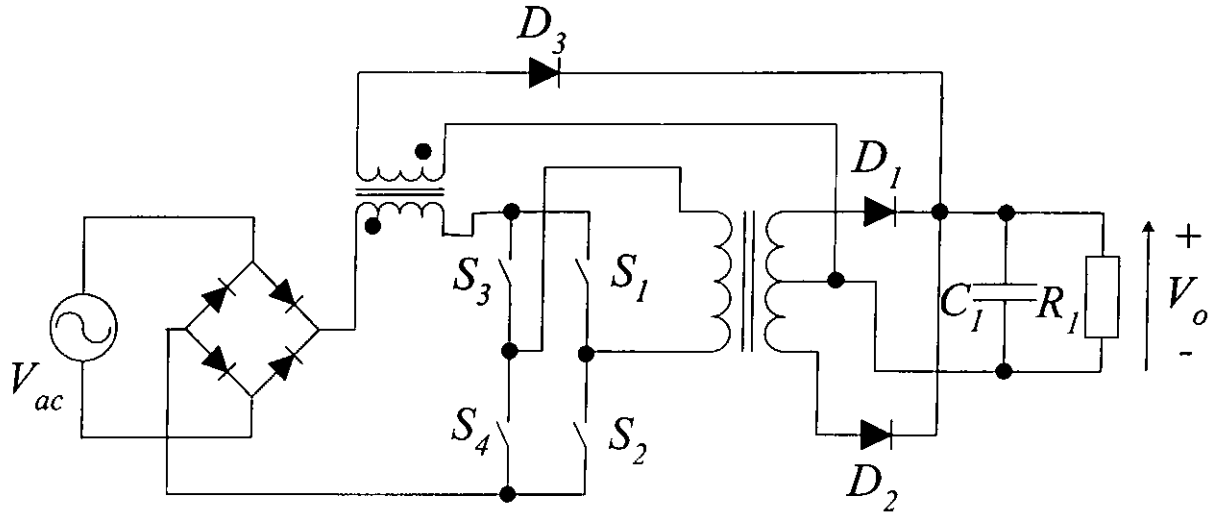


Figure 13 Isolated boost power-factor corrector.

2.2.3.2 Isolated correctors using resonant converter

An example of isolated corrector using a resonant converter is shown in Figure 14[16][13]. This circuit uses an inductor-capacitor-capacitor (LCC) resonant converter. Due to the natural voltage-boost capability of the converters, the converter can achieve a high power factor without a line current control. However, the circuit is complex.

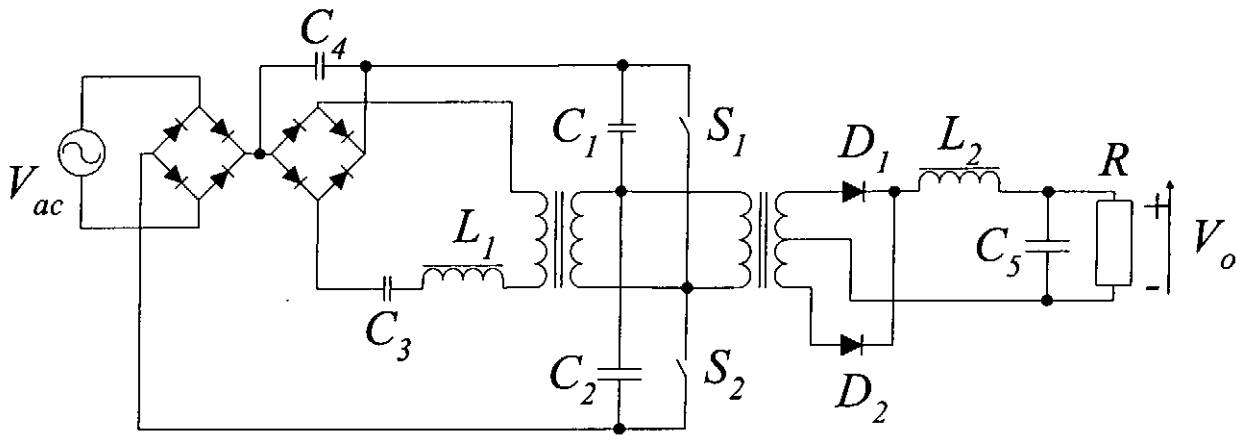


Figure 14 Isolated power factor corrector using a dual-control converter.

2.2.4 Dual-control converters

2.2.4.1 Single-switch dual-control converters with two conduction modes

In single switch dual-control converters, each converter can be divided into two segments, a boost segment and a DC/DC converter segment. The boost segment operates in discontinuous current mode (DCM). As a result, a high power factor is achievable without active control. Many circuit have been reported, e.g. the 'Dither rectifier' as shown in Figure 15 [17], the 'Russian circuit' as shown in Figure 16 [18], the 'BIFRED' circuit as shown in Figure 17 [14], and the 'BIBRED' as shown in Figure 18 [14]. All of these circuits are suitable for low cost applications.

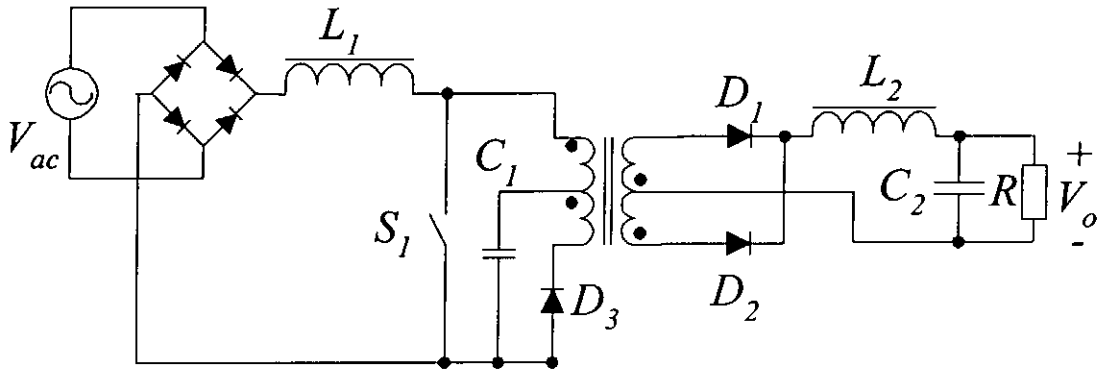


Figure 15 Dither rectifier

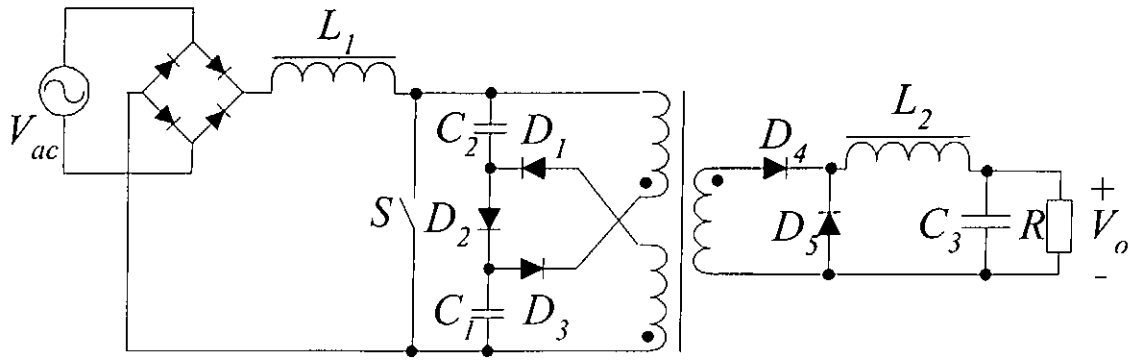


Figure 16 Russian circuit

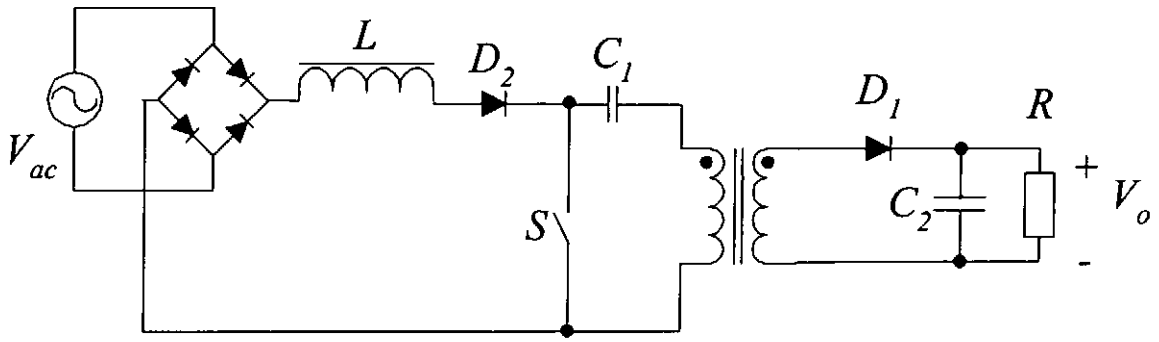


Figure 17 BIFRED

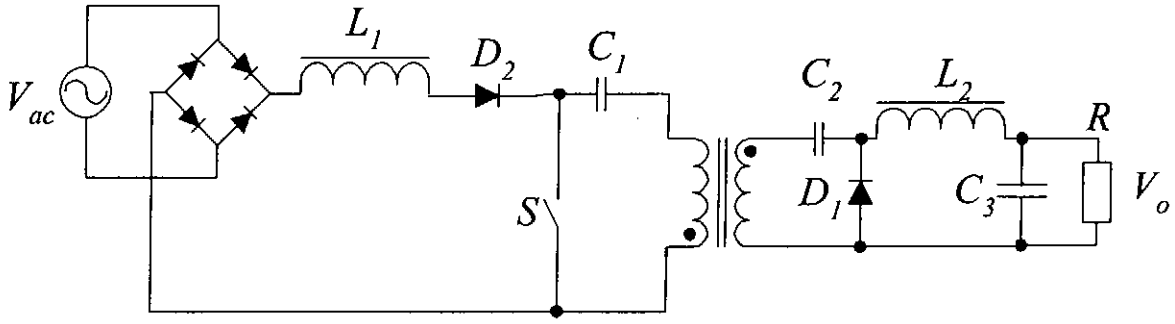


Figure 18 BIBRED

2.2.4.2 Single-stage single-control corrector with fast regulation.

A single-stage single-control corrector is shown in Figure 19 [4]. This circuit uses a single fast control loop to control the output voltage and provide a fast regulation. It has the advantages of low cost and complex design. For applications below 125 W, this is a possible optimum solution to the 110 V_{ac} market.

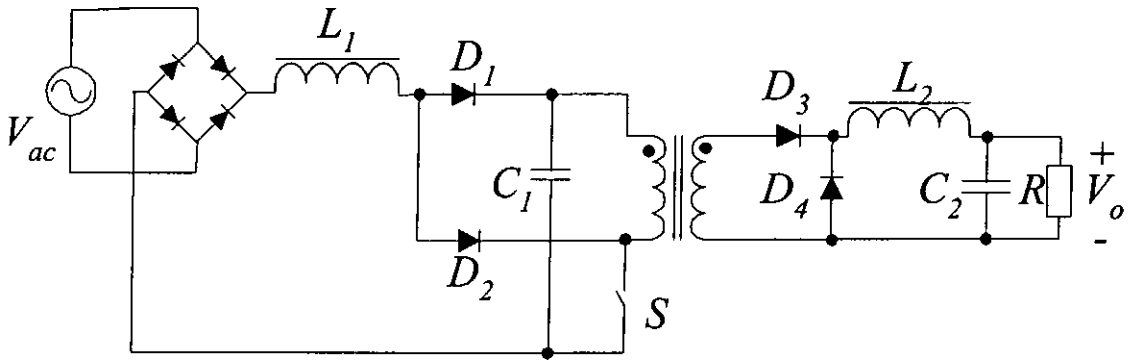


Figure 19 Single-stage single-control with fast regulation corrector.

2.3 Control methods for active PFC:

A typical boost PFC converter is shown in Figure 20.

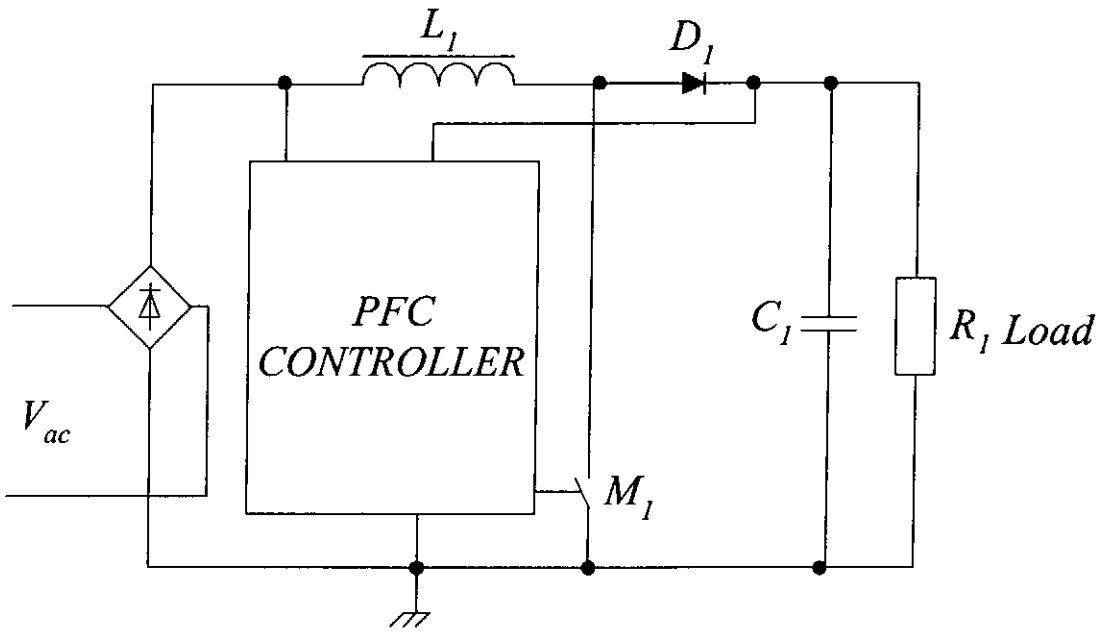


Figure 20 A typical Boost PFC converter circuit.

A typical boost PFC converter consists of a rectified AC source, a boost inductor, a main switch and a diode. By controlling the mark space ratio of the switch M_1, it is possible to shape the current to a sine wave. Generally, there are two modes of operation in the power factor correction converter. They are the continuous current mode CCM and the discontinuous current mode DCM. In CCM operation, the controller uses either peak current control, average current control or hysteretic band control. In DCM operation, the average input current is inherently close to a sine wave without control when the output voltage is enough high (1.5 times of the input voltage).

2.3.1 Peak current control

A circuit with peak current control is shown in Figure 21. When MOSFET M_1 is turned on, the input current i_s is compared with the current reference signal Z, which is obtained by multiplying signal x and signal y. Signal x is the output signal of the error amplifier *VA* , which is the amplified error signal between output voltage *Vo/H* and the voltage reference signal *Vref*. Signal y is the input voltage *Vdc/K*. *Vdc* is the rectified input voltage. When the current in MOSFET M_1 tends to become higher than the reference signal *Z*, MOSFET M_1 will be turned off. As a result, the inductor current *iL* will follow the input voltage and will be in phase with the input sine wave. A typical waveform of *iL* is shown in Figure 22. In this control method, a possible problem is that the average current may have a large error.

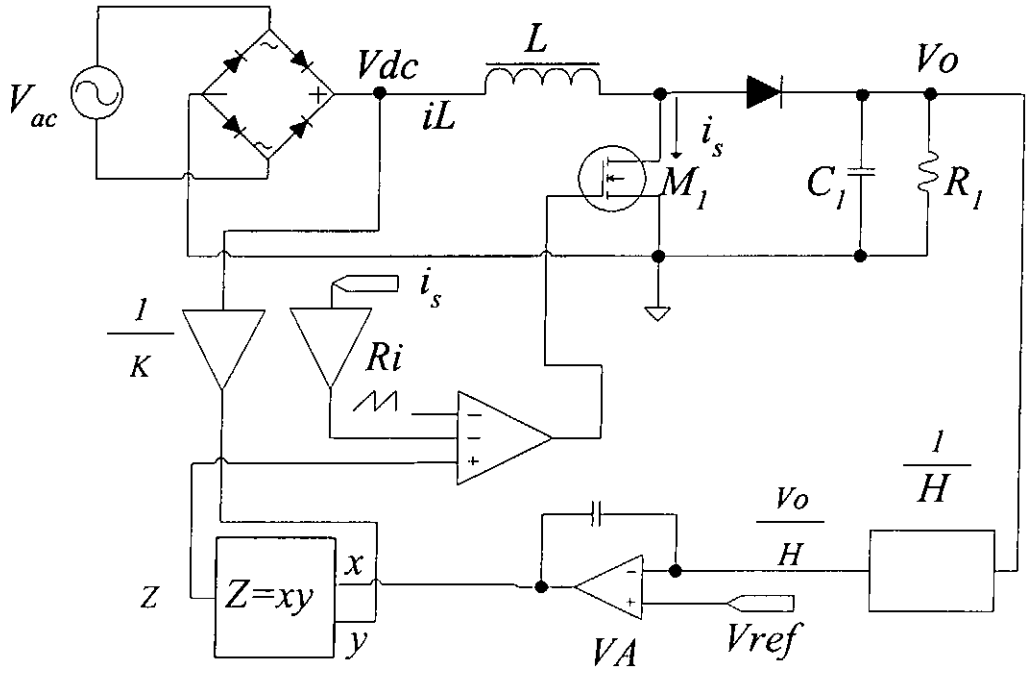


Figure 21 The peak current control.

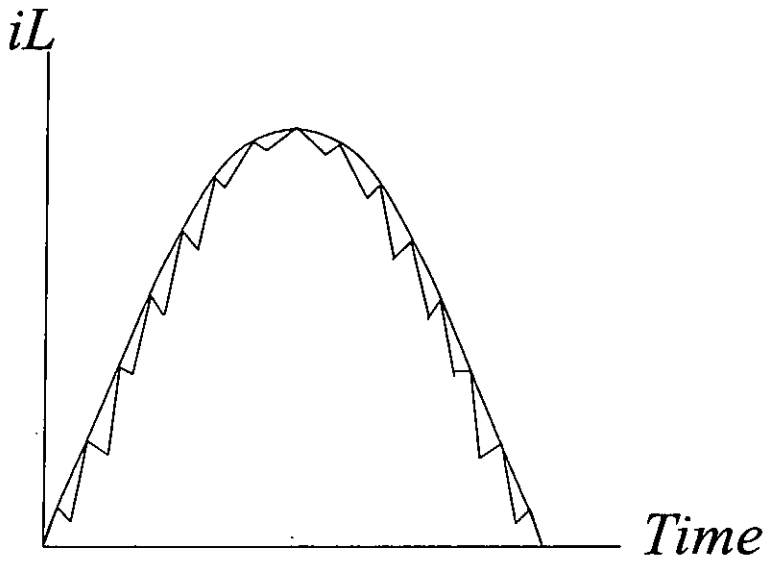


Figure 22 The typical waveform of input inductor with peak current control.

2.3.2 Hysteretic current control

A circuit with hysteretic current control is shown in Figure 23. The main difference between hysteretic current control and peak current control is that the hysteretic current control has an additional logic circuit which controls the hysteretic band current. The switching frequency of this circuit is not a constant. During normal operation if the input inductor current *iL* is lower than the minimum limit current I_{min}, the MOSFET will be turned on, and the input inductor current *iL* will increase. On the other hand, if the input inductor current *iL* is higher than the upper limit I_{max}, the MOSFET will be turned off, and the inductor current *iL* will decrease. The input inductor current will vary within the upper and lower bound. A typical waveform of *iL* is shown in Figure 24. The disadvantage of hysteretic current control is that it needs a wide range of operation frequencies for different loading conditions. Moreover, when designing the input inductance *L*, the minimum frequency requirement should be take into consideration. As a result, the minimum size and weight are limited.

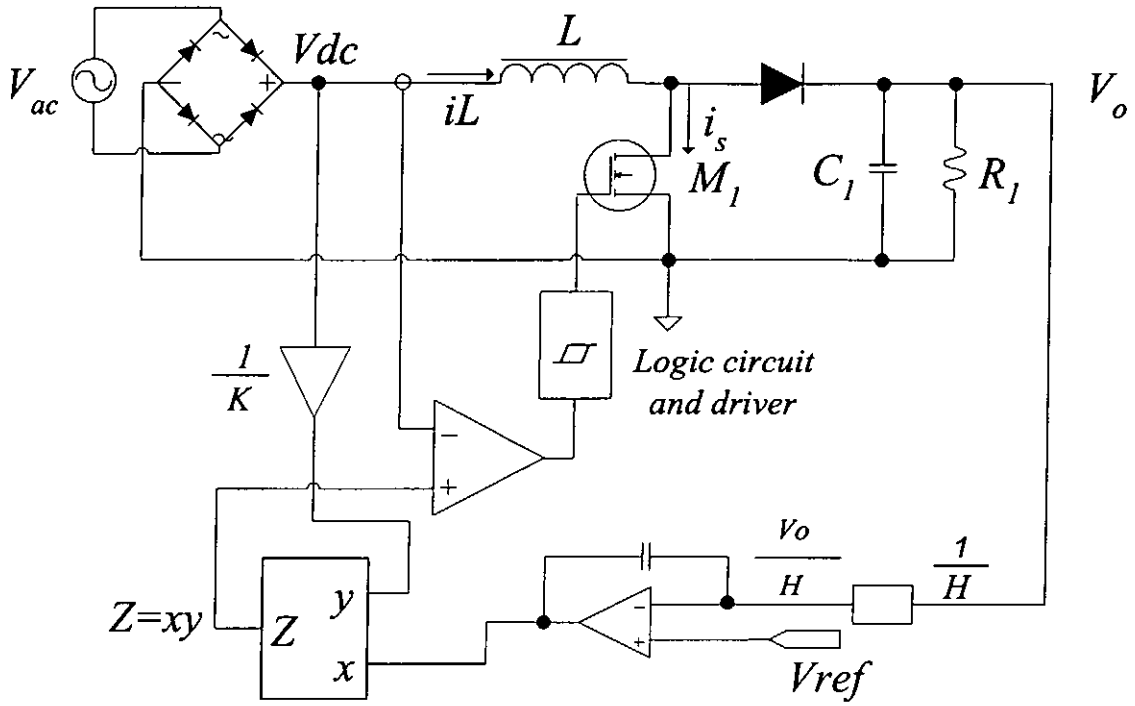


Figure 23 The hysteretic current control.

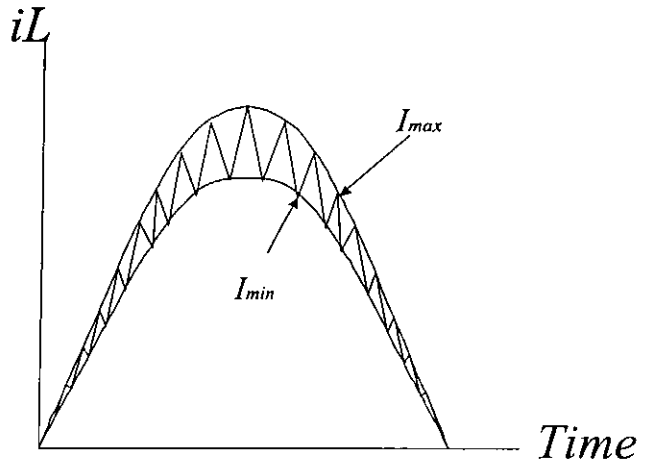


Figure 24 Typical waveform of input inductor current with hysteretic current control.

2.3.3 Average current control

A typical PFC circuit with average current control is shown in Figure 25. The main difference between the average current control and the peak current control is that the average current control method uses a current error amplifier, shown as *CA*, to replace the current comparator. The current reference *Z* is obtained by multiplying a voltage derived from the input, *Vdc/K*, and the error voltage, *Verr*. Through the current comparator, the pulse width modulator (PWM) will generate a suitable duty cycle to control the input inductor current. Because this control method uses a current amplifier, it can correct the current waveform very quickly. By using this method, the power factor can be made very close to unity. In addition, the average current control can operate in either DCM or CCM. The control methodology is applicable to both boost converter and flyback converter.

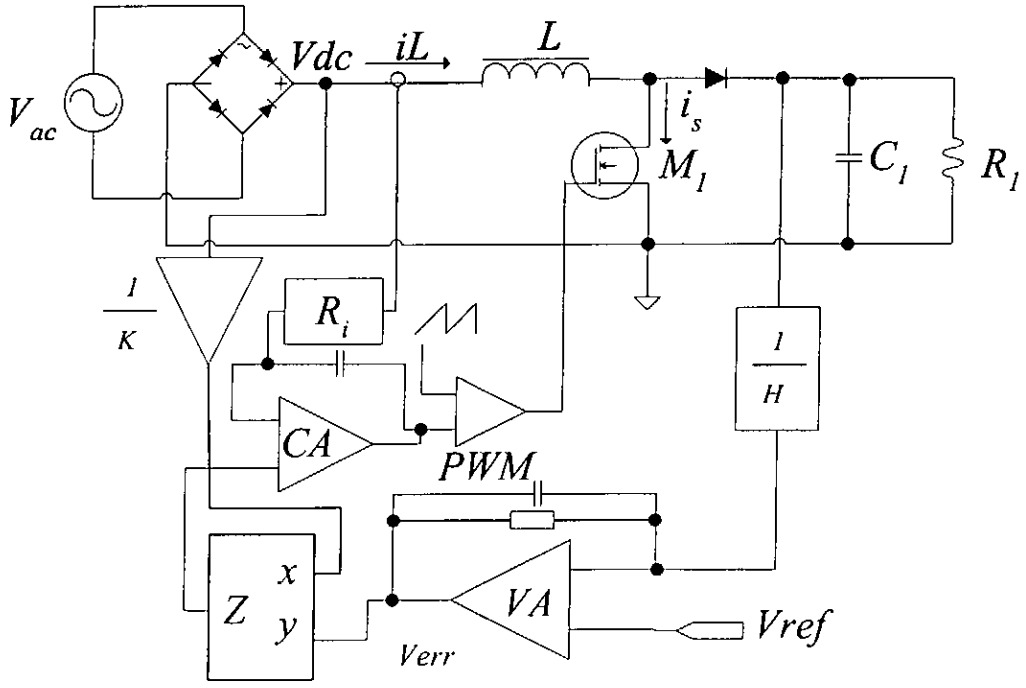


Figure 25 The average current control.

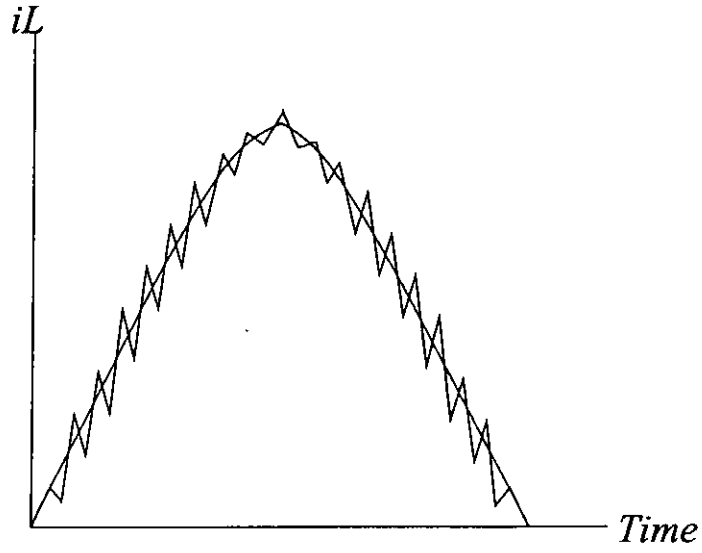


Figure 26 The typical waveform of input inductor with average current control.

2.4 Control requirement and techniques of general voltage regulators

Generally, a power supply should be designed to have good line regulation, good load regulation and fast transient response to system disturbances. It should remain stable under all operation conditions. When there are sudden changes in input voltage or output current the output voltage should settle down quickly, with minimal oscillations. A simple forward regulator with feedback control is shown in Figure 27. Figure 28 is a control block diagram of the regulator.

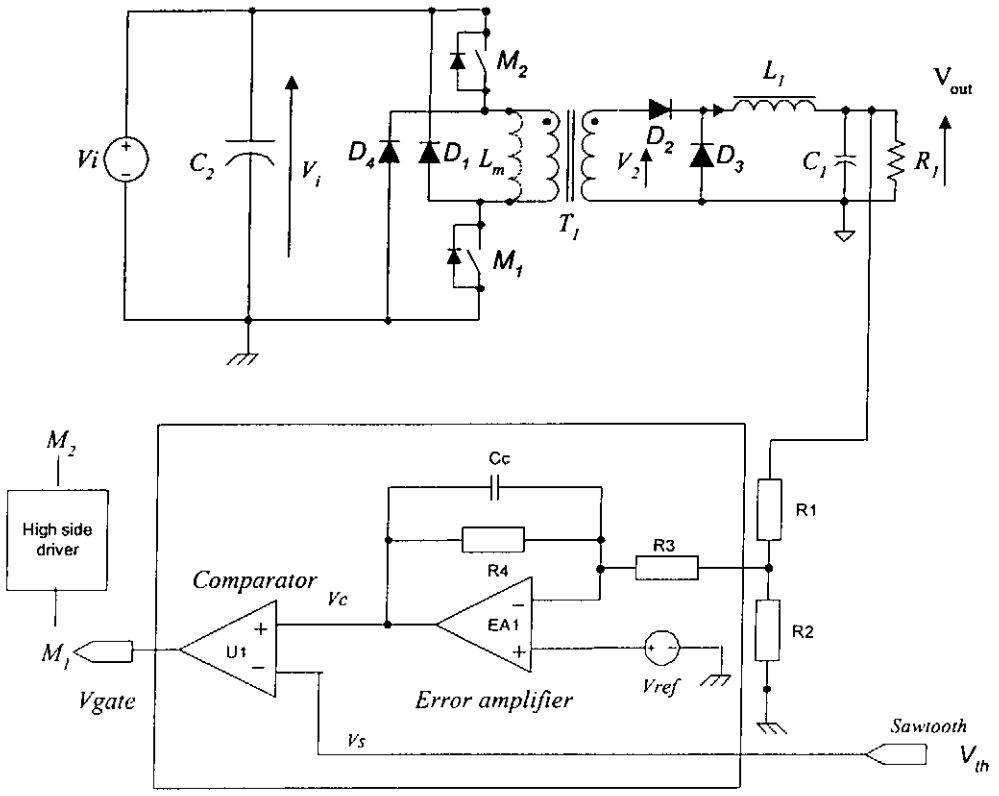


Figure 27 The block diagram of two switches forward SMPS.

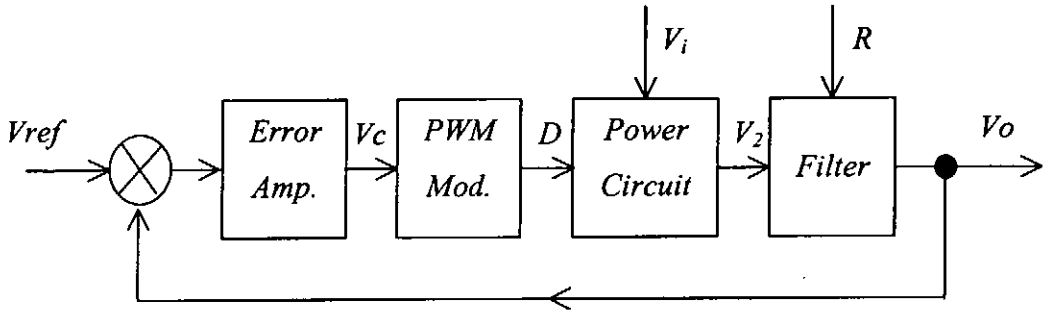


Figure 28 Power supply PWM control diagram.

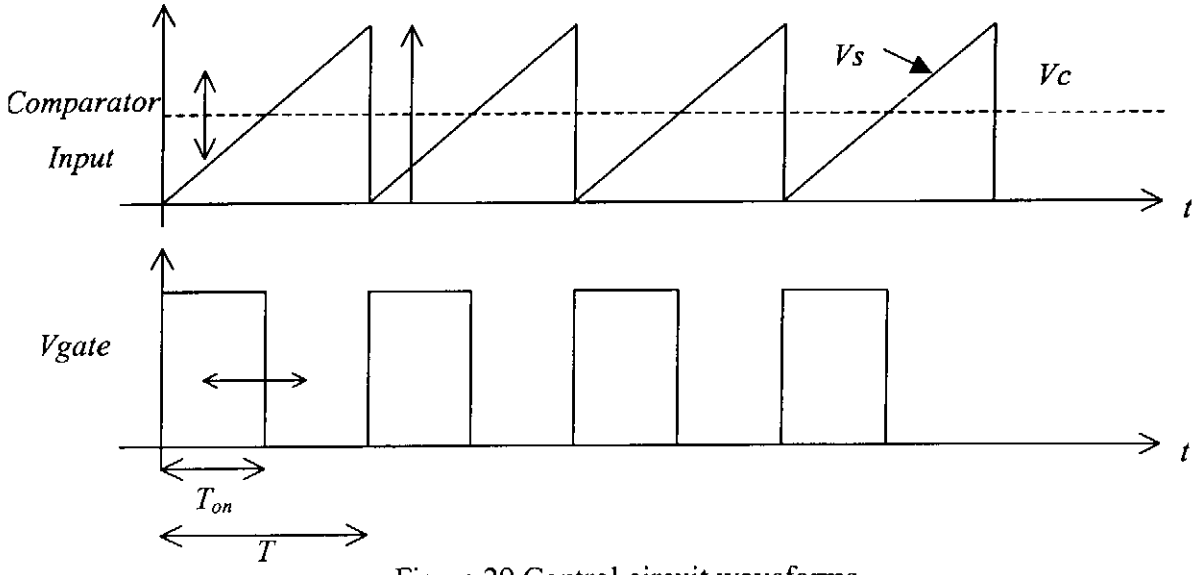


Figure 29 Control circuit waveforms.

2.4.1 Direct duty control

In the control circuit of a switching mode power supplies (SMPS), the output voltage V_o is first compared with a reference voltage. The resulting error voltage is used to adjust the duty cycle D. In direct duty cycle control, D is obtained by comparing the control voltage V_c with a fixed frequency sawtooth voltage, as shown in Figure 27. As a result, $D = \frac{T_{on}}{T} = \frac{V_c}{V_s}$. This technique uses a sawtooth waveform with a fixed amplitude and fixed frequency. The duty cycle D is adjusted by a change in the output voltage which alters the control voltage V_c.

This technique is very popular as it is very simple, but it does have drawbacks. The main problem is poor open loop line regulation, i.e. if the control loop is broken, a change in V_i will cause a significant change into the output voltage V_o. Also, direct duty control has a poor closed loop transient response to the changes in V_i. This is due to the delay in the output L-C filter.

2.4.2 Voltage feed forward control

To solve the drawback of direct duty control method, voltage feed forward control is used. An example of a power supply with feed forward control is shown in Figure 30. Some control circuit waveforms are shown in Figure 31. Here the sawtooth waveform Vs is made proportional to the input voltage Vi, so that

$V_s = \frac{V_i}{K}$ where K is a constant.

However, since

$$D = \frac{V_c}{V_s} \tag{2-3}$$

we have

$$D = K \cdot \frac{V_c}{V_i} \tag{2-4}$$

Assume that transformer ratio is 1:1. When operating in the continuous mode, the output voltage is

$$Vo = DVi = \left(K\frac{Vc}{Vi} \right) Vi = KVc \tag{2-5}$$

Under this condition (i.e. with voltage feed forward), the output voltage Vo will be independent of Vi.

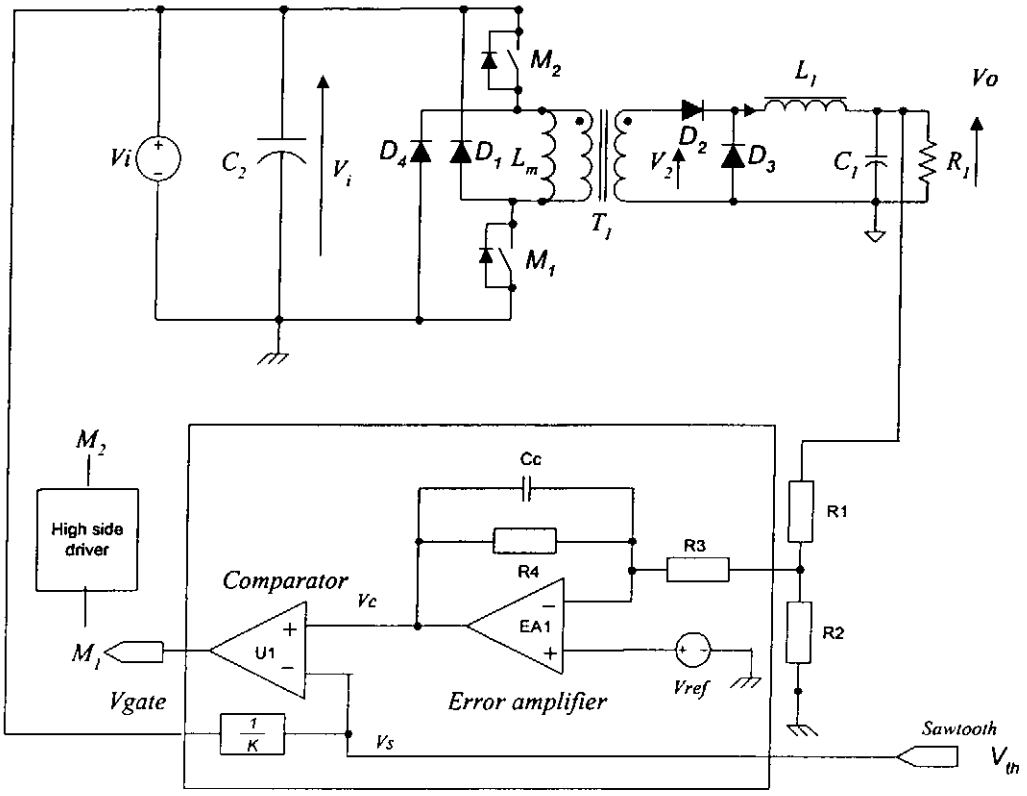


Figure 30 Power supply with feed forward control.

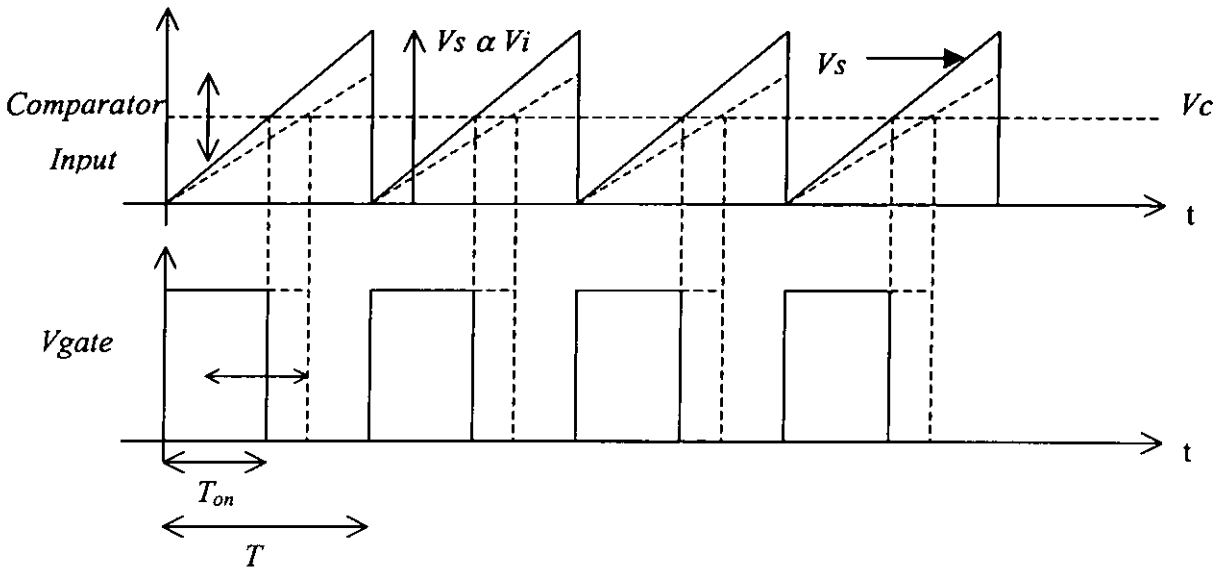


Figure 31 Control circuit waveforms.

The relationships among *Vi, D* and *Vo* for various converters are shown in Table 4.

Converter Type	**DC gain of the converter**
Buck, Continuous	$\frac{Vo}{Vi} = D$
Buck, Discontinuous	$\frac{Vo}{Vi} = \frac{2D}{D + \sqrt{D^2 + (8L/RT)}}$
Buck-Boost, Continuous	$\frac{Vo}{Vi} = \frac{D}{1-D}$
Buck-Boost, Discontinuous	$\frac{Vo}{Vi} = D \times \sqrt{\frac{RT}{2L}}$
Boost, Continuous	$\frac{Vo}{Vi} = \frac{1}{1-D}$
Boost, Discontinuous	$\frac{Vo}{Vi} = \frac{1 + \sqrt{2D^2TR/L}}{2}$

Table 4 The DC gain of the different types of converters

From equation (2-5), it can be seen that *Vi* disappears from the DC gain. The feedforward control is suitable for the buck (continuous mode) and buck-boost (discontinuous mode) regulators. As a result, the voltage feedforward control is a very useful and easily implemented technique. Since feedforward is an open loop technique, proper design of the scaling factor is important.

2.5 Electromagnetic interference (EMI)

Switching mode power conversion has many advantages that makes it very desirable, or even essential in some applications. Its major drawback is the generation of high frequency electrical noise associated with fast switching waveforms in the power regulator. In most applications, it is necessary to filter out this noise and prevent it from interfering other equipment or appliances.

Rapidly changing electric or magnetic fields generate EMI. Common sources of EMI are electric motors, relays and switches where rapid changes of current produce a broad range of interference frequencies. As switching mode power supplies contain high frequency switching currents, they are potentially major sources of EMI.

2.5.1 EMI reduction at source

In order to provide high conversion efficiency in a switch mode power supply (SMPS), the power converter requires rapid switching of current and voltage by the main switch. This gives rise to high $\frac{di}{dt}$ and $\frac{dv}{dt}$, which cause EMI problem. The major source of EMI is the main switching device, which produces oscillation in the parasitic capacitance and leakage inductance. In order to reduce this interference at the source, a slight trade-off can be made with efficiency, by reducing the speed the change of $\frac{di}{dt}$ and $\frac{dv}{dt}$ at the main switches. A possible arrangement is shown in Figure 32

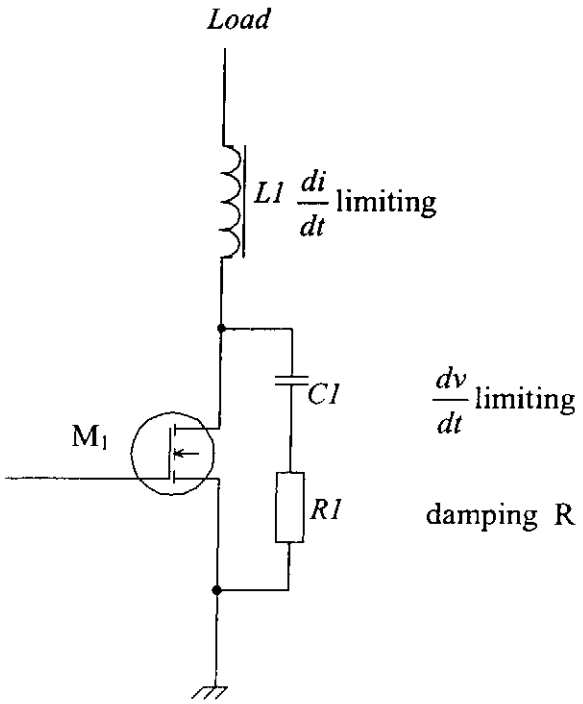


Figure 32 $\frac{di}{dt}$ and $\frac{dv}{dt}$ limiting components

2.5.2 Wire layout

In order to reduce EMI, the PCB layout must be carefully designed. All wires carrying rapidly switching currents and voltages should be kept as short as possible to minimize radiation. Excessive wiring length increases inductance and capacitance, producing unwanted ringing and voltage drops. It is particularly important to pay attention to the switching paths in the supply. Examples of good and bad wiring layouts are shown in Figure 33. In practice the main switching device must be close to the transformer and choke. Sensitive circuits, such as the voltage reference and error amplifier, should be kept away from circuits carrying high currents or voltage.

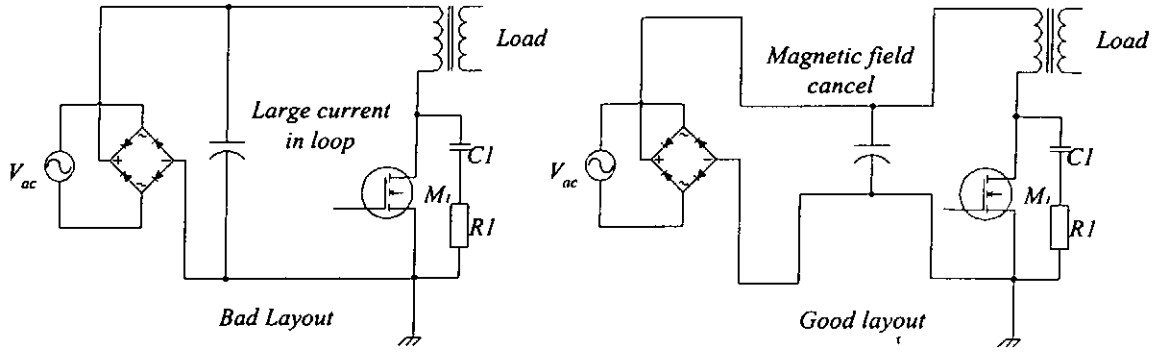


Figure 33 Examples of good and bad wiring layout.

CHAPTER 3
PROPOSED ZVS SMPS WITH POWER FACTOR CORRECTION

3.1 Introduction

Non-linear electronic loads such as switching mode power supplies in personal computers draw non-sinusoidal line current from the mains. This deteriorates the quality of the power line. As a preventive measure, EU countries require all off-line electronic equipment/appliances over 50 W to comply with the EN 61000-3-2 [1] standard after the year 2001. Hence, power-factor-correction circuits must be employed in most of the off-line equipment appliances. There are two types of power-factor-correction (PFC) circuits, namely passive type and active type. It is clear that active PFC circuits can achieve high power factor, high power density and high efficiency. Therefore, active PFC circuits are most popular used.

Today, Very High Voltage Integrate Circuit (VHVIC) technology can achieve a breakdown voltage of 700 V. Therefore, the controller circuit and the high voltage MOSFET can be integrated into a single-chip package. Based on this technology, theoretically, the cost and size of a power supply could be greatly reduced. However, the amount of size reduction in practice is limited by the temperature rise resulting from thermal dissipation on the signal-chip module. The objective of this project is to develop a new power-factor-corrected switching mode power supply with soft switching to reduce the chip temperature, and to design corresponding controller circuits using VHVIC technology.

3.2 Circuit description

The proposed PFC circuit is shown in Figure 34. Compared with the more conventional circuit shown in Figure 35, the proposed circuit has actually less component count. In the circuit shown in Figure 34, inductor L_1 is directly connected to transformer T_1. Here the body diodes of MOS switches M_1 and M_2 are used to replace diodes D_5 and D_1 in the conventional circuit (shown in Figure 35.)

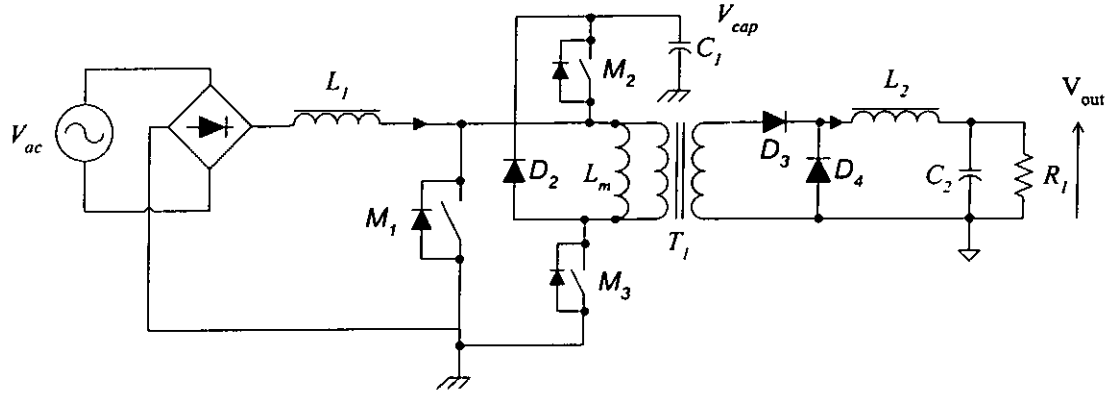


Figure 34 The proposed PFC circuit.

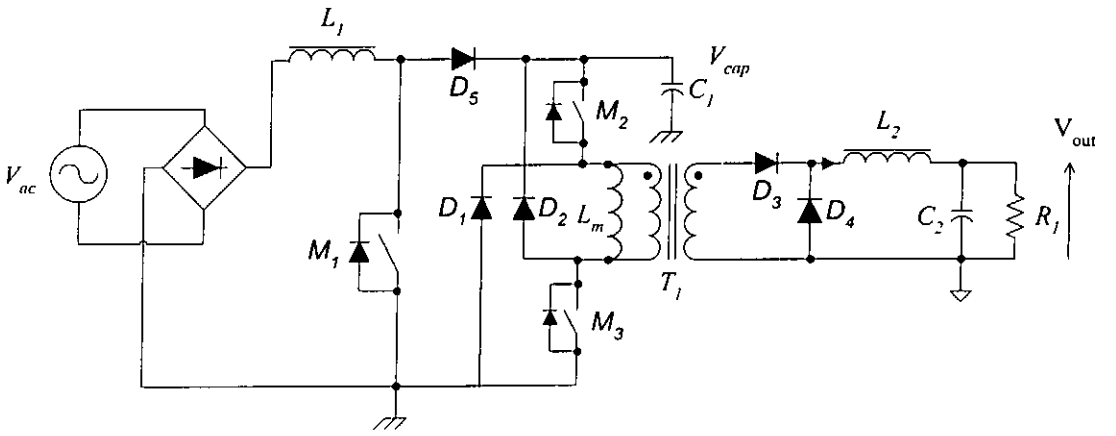


Figure 35 The conventional PFC circuit.

3.3 The mode of operation

For the proposed circuit shown in Figure 34, a special set of gate drive signals is required. Figure 36 shows the details of the gate drivers for M_1, M_2 and M_3. Through this synchronization switching sequences, the converter can gain soft switching operation on M_2 and M_3.

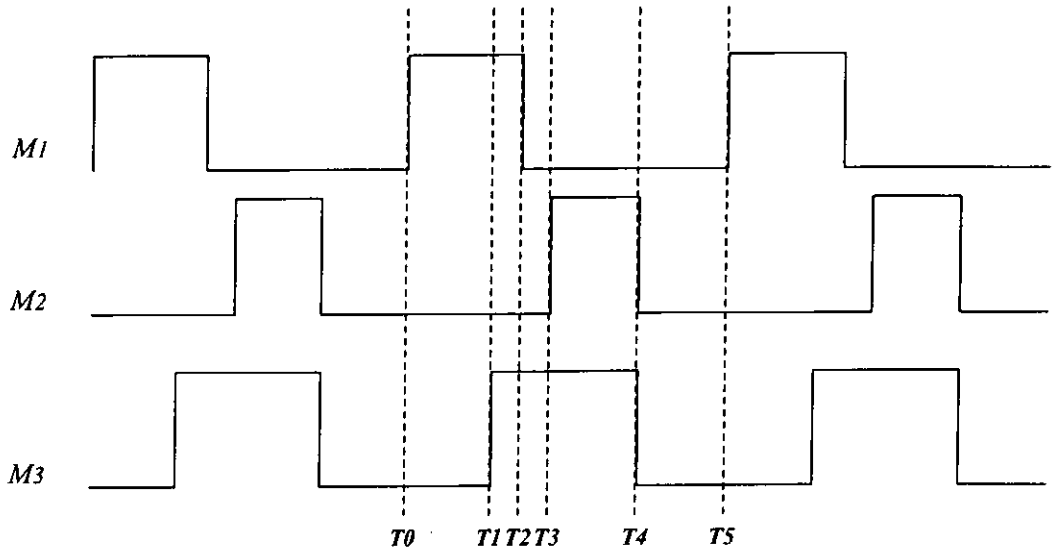


Figure 36 Gate drive signals of the proposed converter.

In this proposed converter, there are three operation stages:

- The stage in which the energy from the AC mains is transferred to the inductor (under the controller of M_1),
- The stage in which the energy from L_1 is transferred to C_1 and transformer T_1, and some energy from C_1 is also transferred to T_1.
- The stage in which the inductor L_2 and the transformer T_1 are operating under a freewheeling mode.

3.3.1 Energy input stage *(T0-T2)*

During the energy input stage, MOSFET M_1 is turned on. MOSFET M_2 and M_3 are turned off. The input current passes through the voltage source (V_{ac}) to inductor L_1. The input current is governed by equation (3-1).

$$di_{L_1} = \frac{V_{ac} - 0}{L_1} dt \tag{3-1}$$

When the boost converter circuit is operated in discontinuous mode (DCM), the waveform of averaged input current has a shape similar to that of the input voltage. Therefore, it can provide power factor correction.

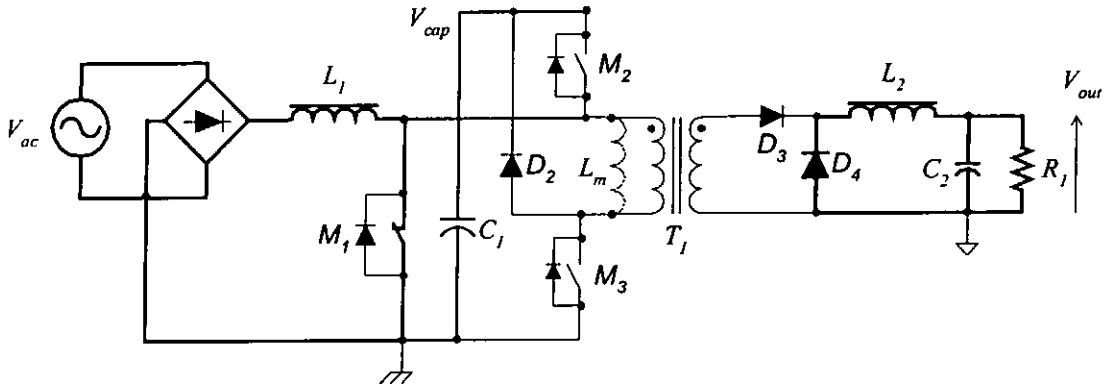


Figure 37 Energy input stage *T0-T1*

At the end of this stage M_3 is turned on before M_1 is turned off. Therefore M_3 is turned on under zero-voltage condition turned on, i.e., soft switched.

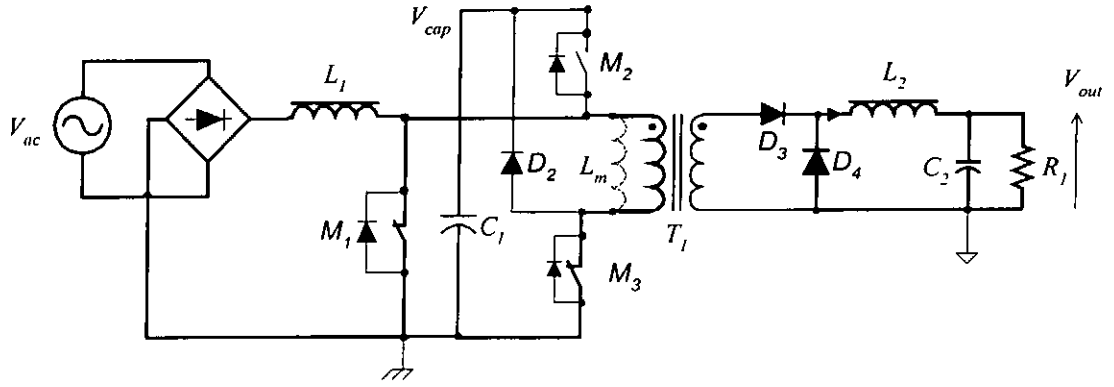


Figure 38 Energy input stage *T1-T2*

3.3.2 Energy transfer stage *(T2-T4)*

In this energy transfer stage, when the M_1 is turned off at *T2*, inductor L_1 current flows through the body diode of MOSFET M_2 to capacitor C_1, as shown in Figure 39. After

some delay (about 300ns), switches at M_2 and M_3 are turned on at *T3*. The energy stored in interval *T0-T2* (referring to Figure 37) is transferred from L_1 to C_1 and T_1, as shown in Figure 39. Note that later on some energy is also transferred from C_1 to T_1, as shown in Figure 40. At the same time, the energy transferred into transformer T_1 induces a current in the output stage. At this moment, diode D_3 is turned on and inductor L_2 current is governed according to equation (3-2).

$$di_{L_2} = \frac{\frac{V_{cap}}{N} - V_{out}}{L_2} dt \tag{3-2}$$

where N is the turns ratio of transformer T_1. Moreover, the input inductor L_1 current is decreasing at the rate of

$$di_{L_1} = \frac{|V_{ac}| - V_{cap}}{L_1} dt \tag{3-3}$$

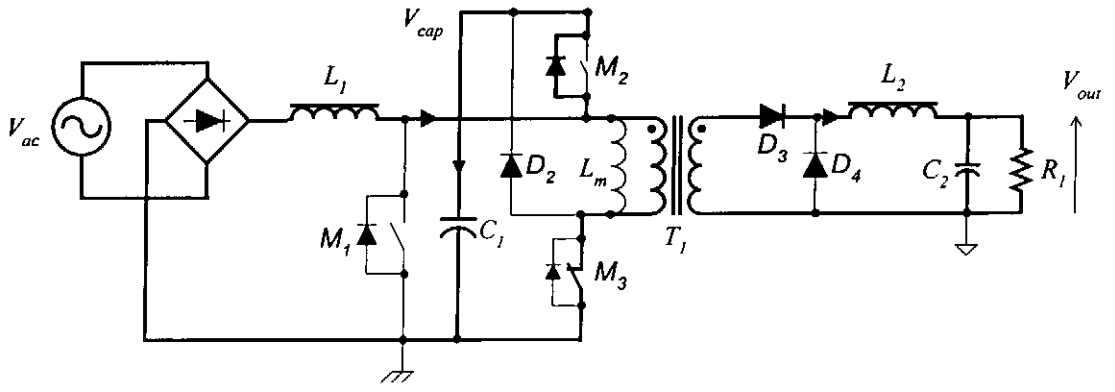


Figure 39 Energy transfer stage *T2-T3*

Since the input voltage V_{ac} is changing with line cycle, sometimes the input inductor energy is not enough to provide the output power (when the input voltage is low). At this moment, the bulk capacitor C_1 will provide most of the power to transformer T_1 , as shown in Figure 40.

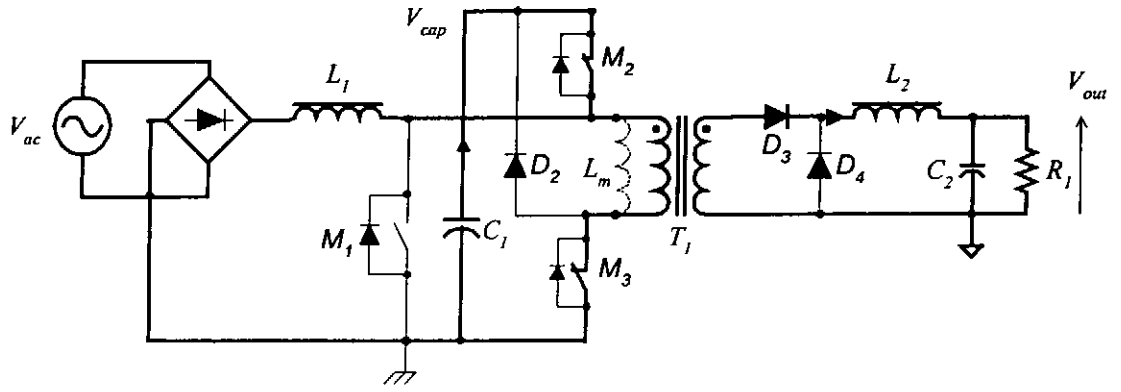


Figure 40 Energy transfer stage *T3-T4*

3.3.3 Freewheeling stage *(T4-T5)*

The operation of the circuit in the freewheeling stage is shown in Figure 41. The transformer reset current flows from the AC mains via bridge diode, inductor L_1, transformer T_1, diode D_2 into capacitor C_1. In the output stage, freewheeling diode D_4 is turned on and the capacitor is discharged. The inductor L_2 current is governed by equation (3-4).

$$di_{L2} = \frac{-V_{out} + 0.7}{L2} \tag{3-4}$$

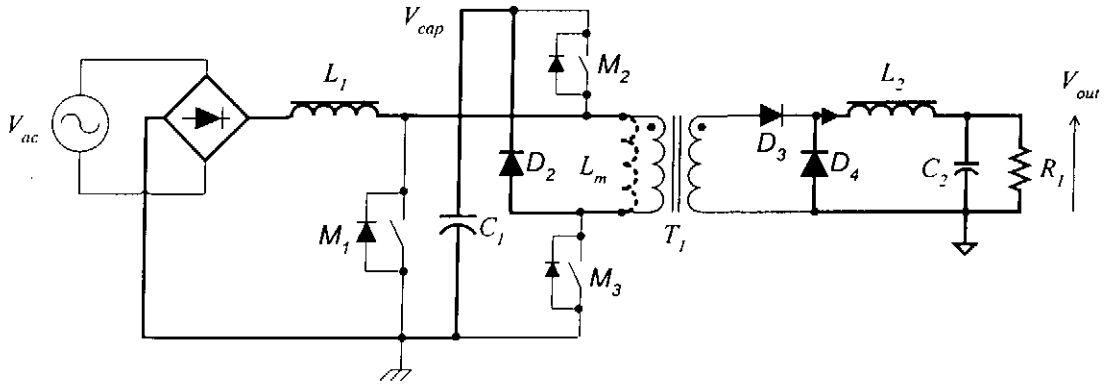


Figure 41 Freewheeling stage *T4-T5*

3.4 Circuit analysis

Assume that the boost converter circuit is operated in discontinuous mode (DCM) and the turn on time of M_3 is longer than the resetting time of the transformer T_1 in the freewheel mode. The waveform of current iL_1 then appears like the one shown in Figure 42.

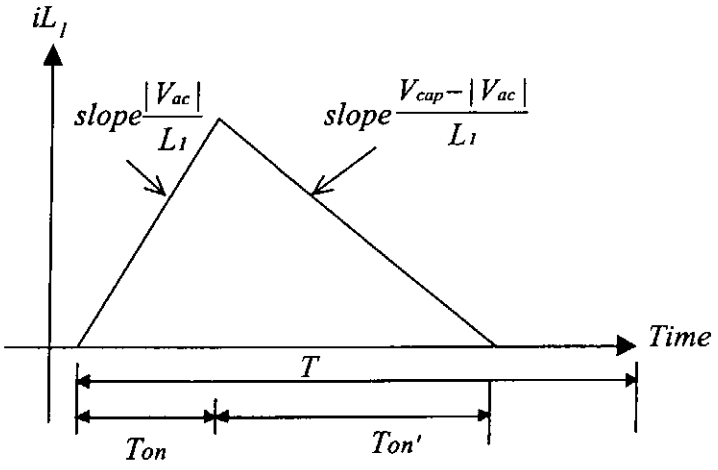


Figure 42 The input inductor waveform.

The input current iL_1 has a triangular shape.

$$\frac{|V_{ac}|-0}{L_1}T_{on}=\frac{V_{cap}-|V_{ac}|}{L_1}T_{on}' \tag{3-5}$$

where Ton' is the turn on time of the body diode of M_2.

To simplify the analysis, assume that the input voltage is a full-wave rectified sine wave $|V_{ac}|$. If the period of a switching cycle, T_s is much smaller than that of the mains, then the voltage of capacitor C_1, (referring to Figure 34), V_{cap}, is more or less constant. Also assuming that the power transformer T_1 does not have leakage inductances, the average boost inductor current is obtained as (3-6).

$$I_{avg}=\frac{V_{cap}\,T_{on}^{\,2}}{2\,L_1 T_s}\cdot\frac{\frac{|V_{ac}|}{V_{cap}}}{1-\frac{|V_{ac}|}{V_{cap}}} \tag{3-6}$$

From the equation (3-6), it is found that the waveform of the average current is similar to that of a typical boost PFC corrector operated in DCM. As an example, the waveform of the average current for a bulk capacitor voltage of 550 V (across C_1) and an input power of 250 W is shown in Figure 43.

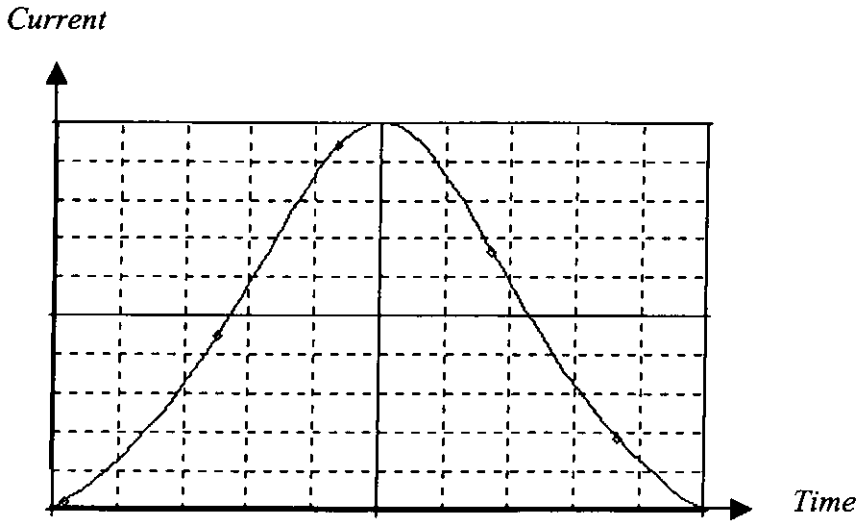


Figure 43 The input average current waveform.

Based on the simulation results, it is also found that the DCM operation in the boost converter has a power factor close to unity. The total harmonic distortion (THD) can meet EN 61000-3-2 standard requirement. Figure 44 shows the relation between input inductor L_1 and the maximum output power with 220 V_{ac} voltage input. In order to provide 230 W output power at 220 V_{ac} voltage input, the input inductor L_1 must be smaller than 183 μH as shown in Figure 44.

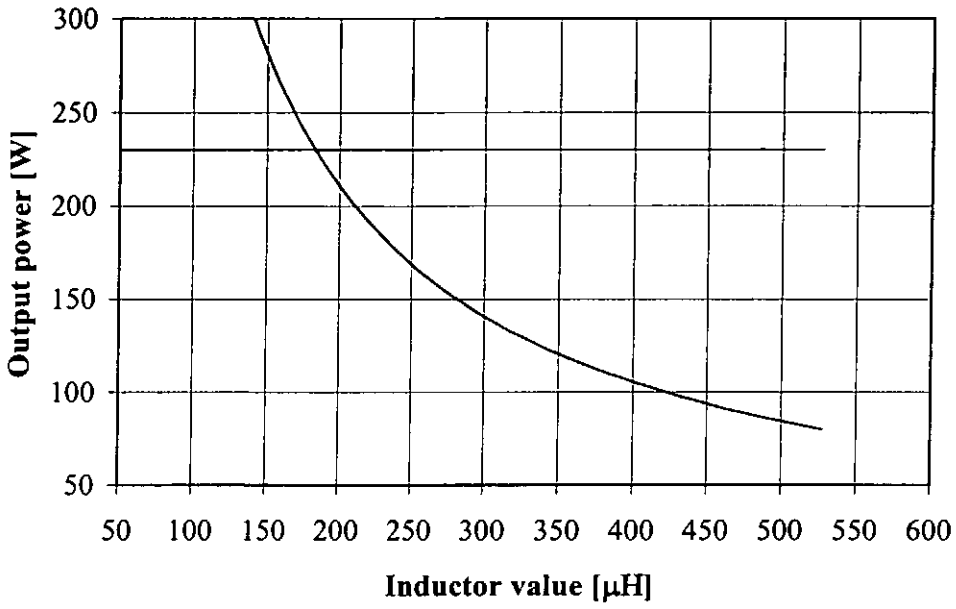


Figure 44 The relation between inductor L_1 and the maximum output power.

The selection criteria for the output capacitor and inductor L_2 are similar to those for conventional converters. The switching frequency, output inductor ripple current, DC output voltage and output ripple voltage are the determining factors. The total current through capacitor C_1 is the rms value of the switching frequency ripple current and the second harmonic of the line frequency current. The selection of capacitor C_1 is based on the allowable range of the duty cycle in the forward converter and the energy storage requirement of a PFC voltage regulator which is governed by

$$C_1 > \frac{P_o}{2\pi f \Delta V_{cap} V_{cap}} \tag{3-7}$$

where P_o is the output power, ΔV_{cap} is the ripple voltage across C_1, and f is the mains frequency. For example, if the variation in the duty cycle of the forward converter has a range from 0.297 to 0.303 (±1% change at 0.3), and V_{cap} is chosen to be 550 V, then the corresponding ΔV_{cap} has a value of 11 V. For a power supply with an output power of 230 W, the minimum value of C_1 must be greater than 121 μF. In our hardware prototype, capacitor C_1 has a value of 330 μF.

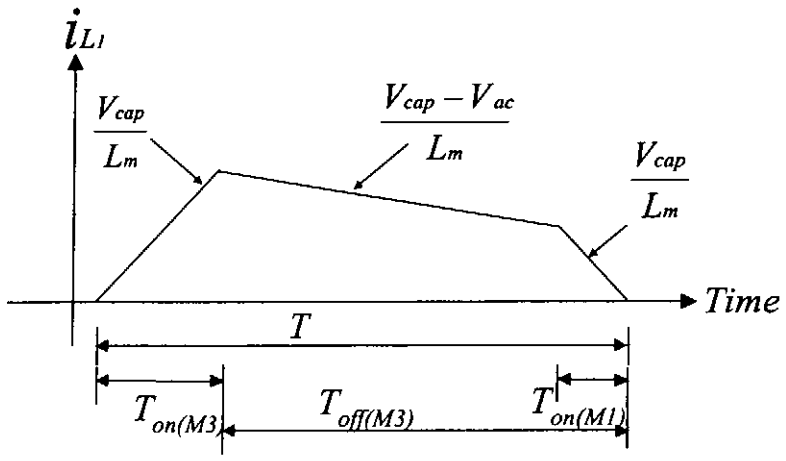


Figure 45 Reset current waveform of transformer T_1.

The magnetization current of transformer T_1 is governed by

$$\frac{V_{cap}}{L_m} T_{on(M3)} = \frac{V_{cap} - |V_{ac}|}{L_m} (T_{off(M3)} - T_{on(M1)}) + \frac{V_{cap}}{L_m} T_{on(M1)} \tag{3-8}$$

In the worst case, (low output power), the duty cycle of the MOSFET M_1 will be small. It means the $T_{on(M1)} \approx 0$. Equation (3-8) can be rewritten as

$$\frac{V_{cap}}{L_m} T_{on(M3)} = \frac{V_{cap} - |V_{ac}|}{L_m} T_{off(M3)} \tag{3-9}$$

Therefore, whether the magnetization current of the transformer can be completed reset in every switching cycle depends on the bulk capacitor voltage. In order to avoid magnetic saturation, it is necessary that

$$V_{cap} \geq |V_{ac}| \left(\frac{1-D}{1-2D} \right) \tag{3-10}$$

where D is the duty cycle of M_3. Based on equation (3-10), the relationship between bulk capacitor voltage and duty cycle are found, as shown in Figure 46. For example, if the capacitor voltage of C_1 is 550 V and the input voltage is 220 V_{ac} and 270 V_{ac}, the duty cycle of M_3 must be smaller than 0.3 and 0.23.

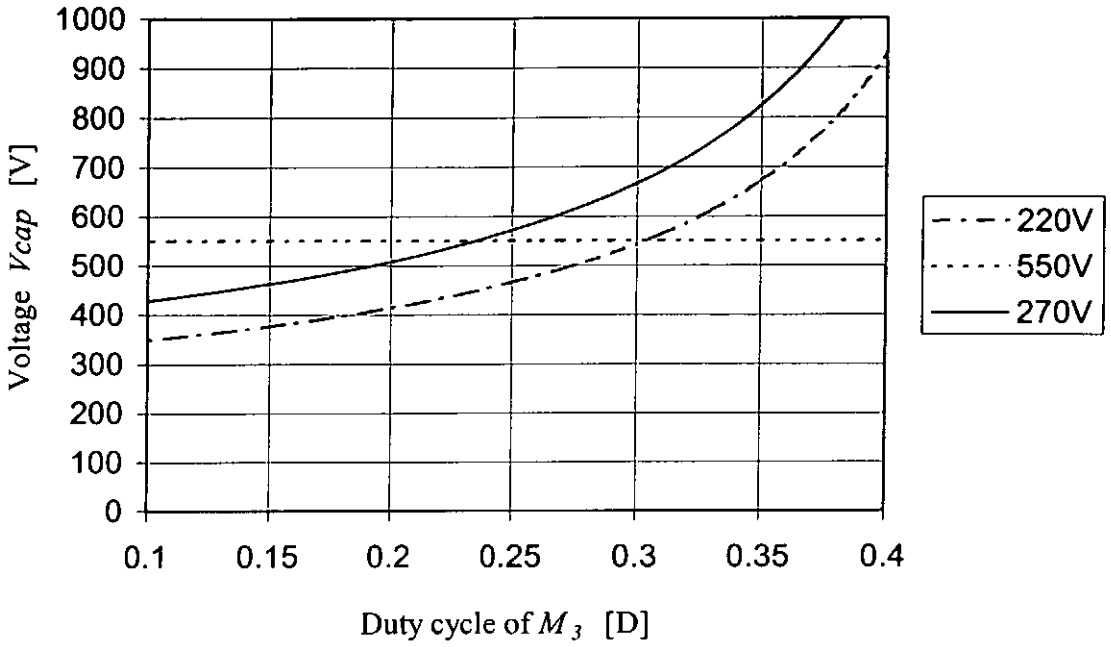


Figure 46 Relationship between Vcap and duty cycle of M_3.

3.5 Design of the controller

The block diagram of the controller for the proposed converter is shown in Figure 47. The controller consists of a triangular wave generator, an error amplifier, and a logic control block. It has a fixed switching frequency.

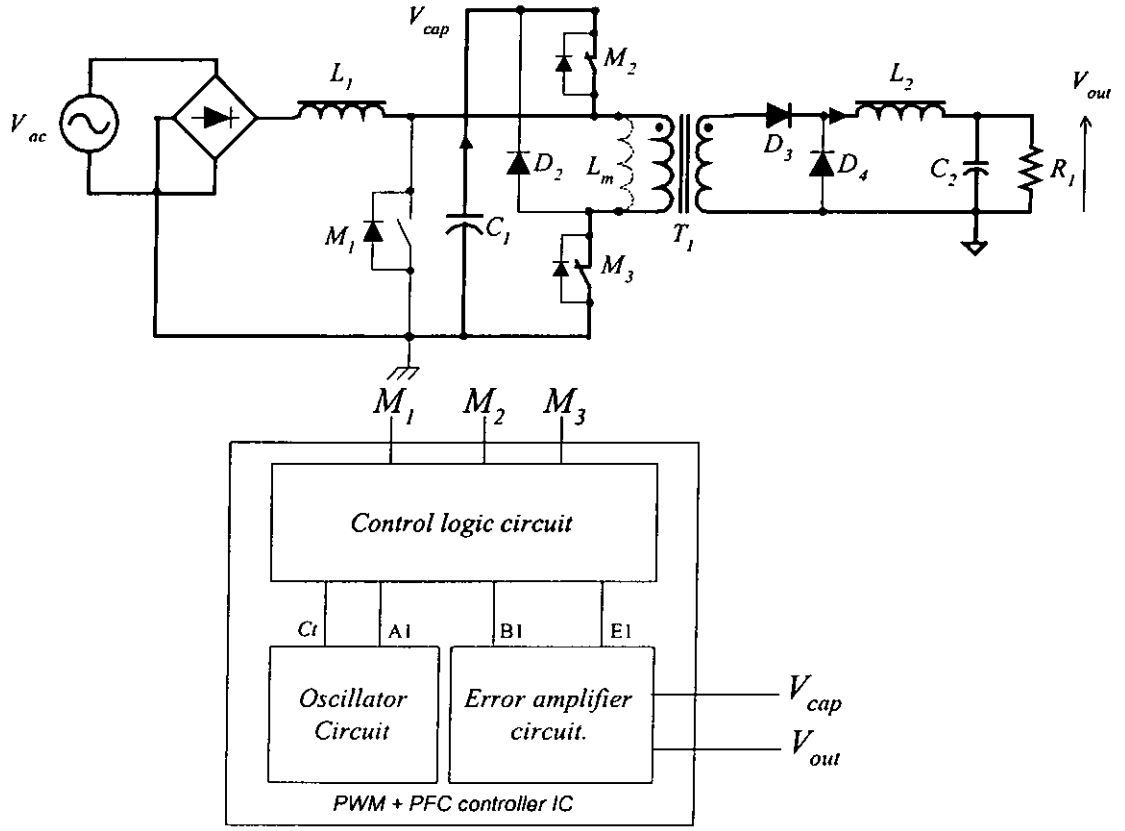


Figure 47 Block diagram of the proposed control circuits.

3.5.1 Oscillator and triangular waveform generator

Figure 48 shows the detailed circuits of the "Oscillator Circuit" block in Figure 47. The internal oscillator MC33363 can generate a triangular signal and a square wave with a 50% duty cycle. Transistors Q8 and Q9 and resistors R29 and R30 are used to form a buffer circuit to reduce the output impedance of the circuit. The oscillation frequency is determined by resistor *Rt* and capacitor *Ct*.

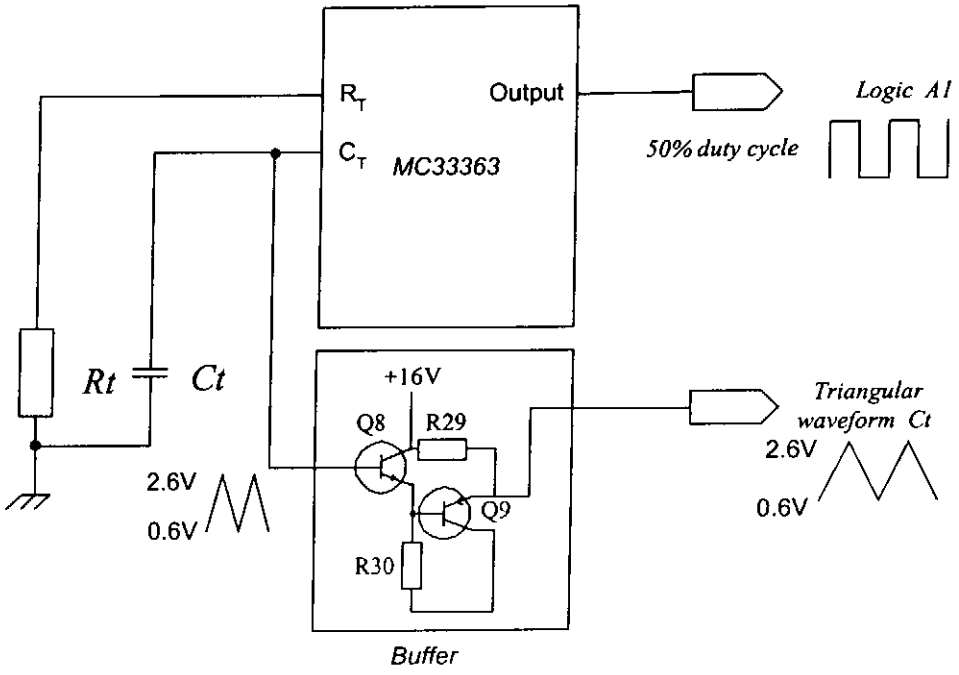


Figure 48 Oscillator circuit.

The oscillator frequency of MC33363 is governed by

$$f \cong \frac{5.4}{4CtRt} \tag{3-11}$$

For example, the oscillator frequency is 100 kHz, the value of the resistor *Rt* is 18 kΩ and capacitor *Ct* is 750 pF. The output pin *Ct* is a triangular wave signal. The voltage of this

pin is between 0.6 V and 2.6 V. The output at the pin *Logic* A1 is a square wave with a duty cycle of 50 %, which is synchronized to the triangular wave signal *Ct*.

3.5.2 Design of Error amplifier circuits

General-purpose operational amplifiers are used in the design of the error amplifiers in the controller (shown in Figure 47.) The detailed circuit of the error amplifiers is shown in Figure 49. The error amplifiers provide voltage mode negative feedback on both the output voltage and storage-capacitor voltage. The non-inverting inputs of both error amplifiers EA1 and EA2 are internally biased at 2.5 V. These error amplifiers are used for external loop compensation. Resistors R9 and R7 and capacitor C4 are used to control the gain and frequency compensation of the output voltage feedback path. The resistors R2 and R5 form a divider circuit to sample the output voltage. Resistors R16 and R18 and capacitor C7 are used to control the gain and frequency compensation of the storage-capacitor voltage feedback path. The resistors R10 and R14 form a divider circuit to sample the storage-capacitor voltage. The duty cycles of the boost converter and the forward converter will be controlled by the output signals B1 and E1.

In the regulation of the output voltage, if the sampled output voltage is higher than the reference voltage *Vreg*, the output of error amplifier *EA2*, $Eo_{(Vout)}$, will decrease as shown in Figure 50. The high-to-low transition edge of the output signal E1 then occurs at an earlier time. This change in E1 will be eventually result a shorter on turn-on time for switches M_2, M_3 and a lower output voltage. Therefore the output voltage is regulated.

In the regulation of the storage-capacitor voltage, if the sampled storage-capacitor voltage is lower than the reference voltage *Vreg*, then the output of error amplifier EA1, $Eo_{(Vcap)}$, will increase as shown in Figure 50. The low-to-high transition edge of the output signal B1 then occurs at an earlier time. This change in B1 will eventually result in a longer on time for switch M_1 and a higher storage-capacitor voltage. Therefore the storage-capacitor voltage is also regulated.

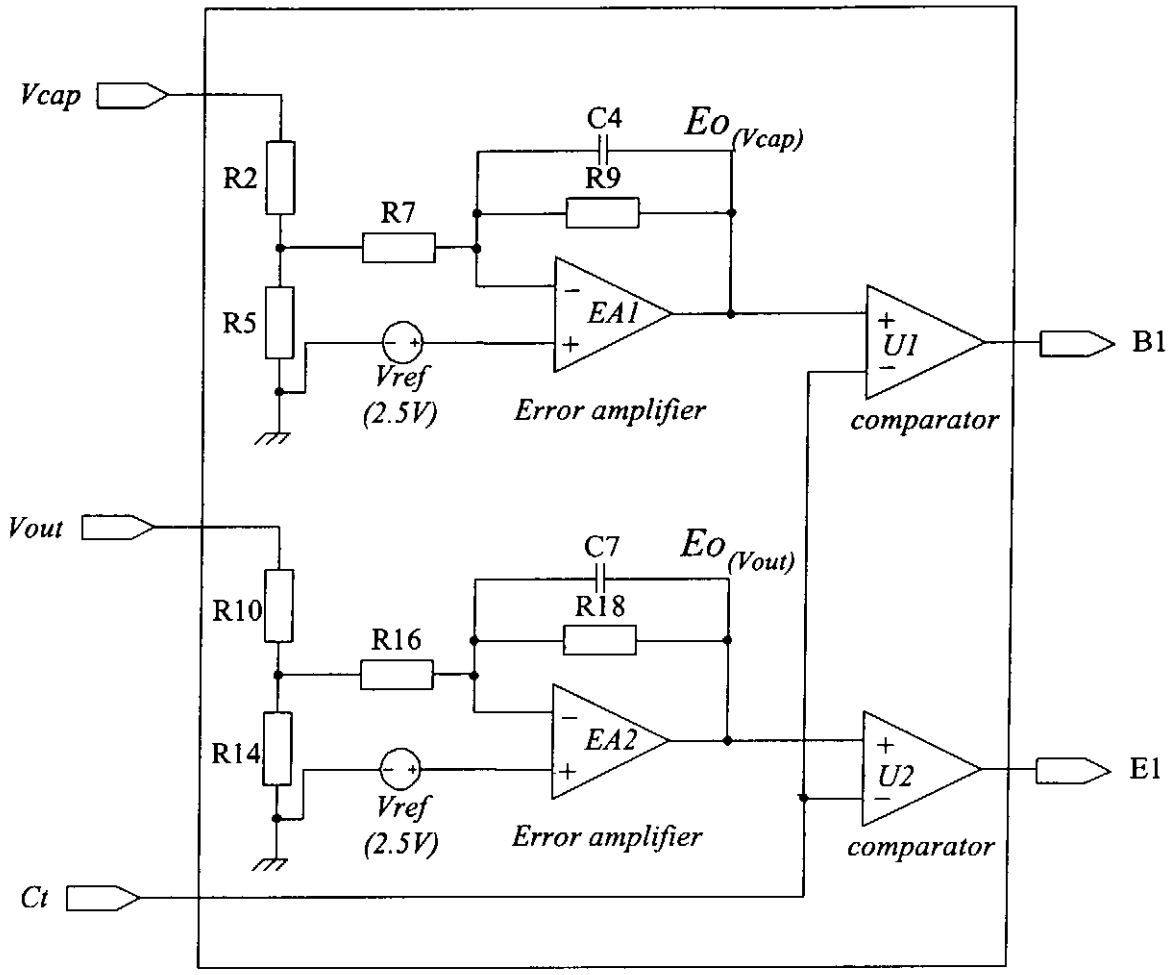


Figure 49 Error amplifier circuits.

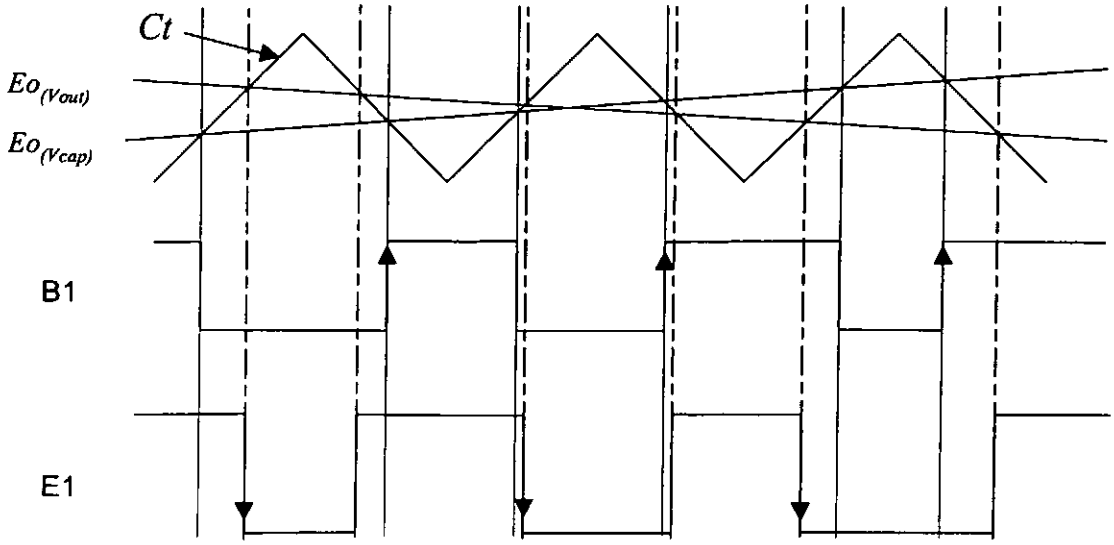
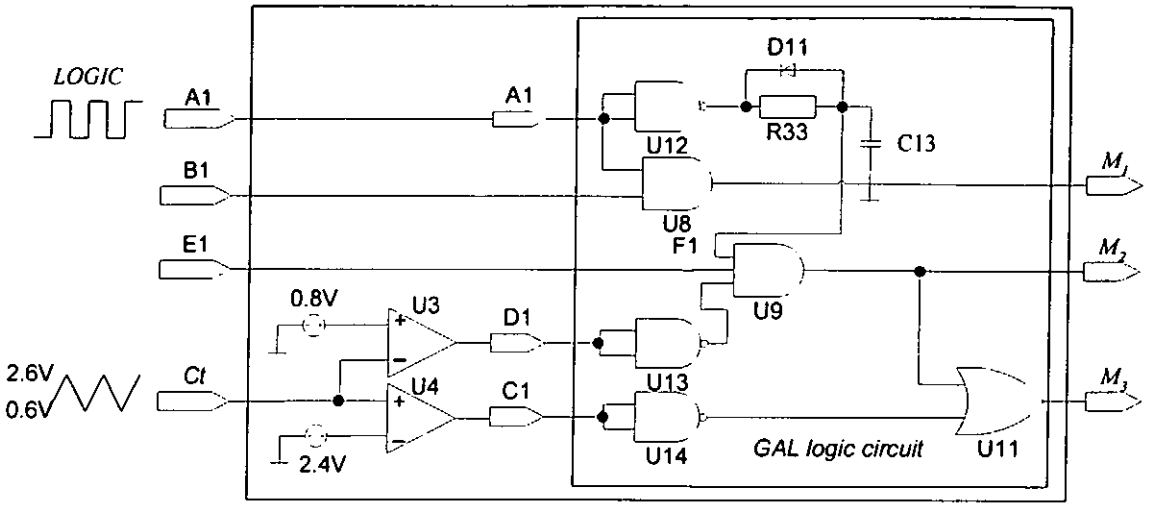


Figure 50 The detail waveforms of the error ampilifer circuits.

3.5.3 Design of logic control circuit

The logic control circuit is implemented by a GAL logic block, as shown in Figure 51. The signal at pin A1 is a square-wave signal with a 50 % duty cycle and the signal at pin B1 is the feedback control signal of the boost converter. The signal at pin E1 is the feedback control signal of the forward converter. These signal are generated by the circuit shown in Figure 50 as described in Section 3.5.2. The signal at pin D1 is a narrow pulse of a width of 600 ns. The narrow pulse is generated from comparer U3 by comparing triangular wave *Ct* with a 0.8 V reference level and it is used to ensure that switch M_3 is turned on before the switch M_1 has been turned off. In the proposed circuit, the boost stage is operated in discontinuous mode. The logic gate U8 is used to generate the gating signal of M_1 of the boost converter. The logic gates U9, U12, and U13 are used to control the gating signal of M_2 of the forward stage. Diode D11 and capacitor C13 generate a delay time (≈300 ns) to ensure that M_2 is turned on after its diode has been turned on by the current from inductor L_1 (after M_1 has been switched off). Signal C1 is used to give a limit on the maximum on time of M_1.



$M_1 = A1 \& B1,\ M_2 = F1 \& E1 \& !D1,\ M_3 = F1 \& E1 \& !D1 + !C1.$

Figure 51 Logic control circuit.

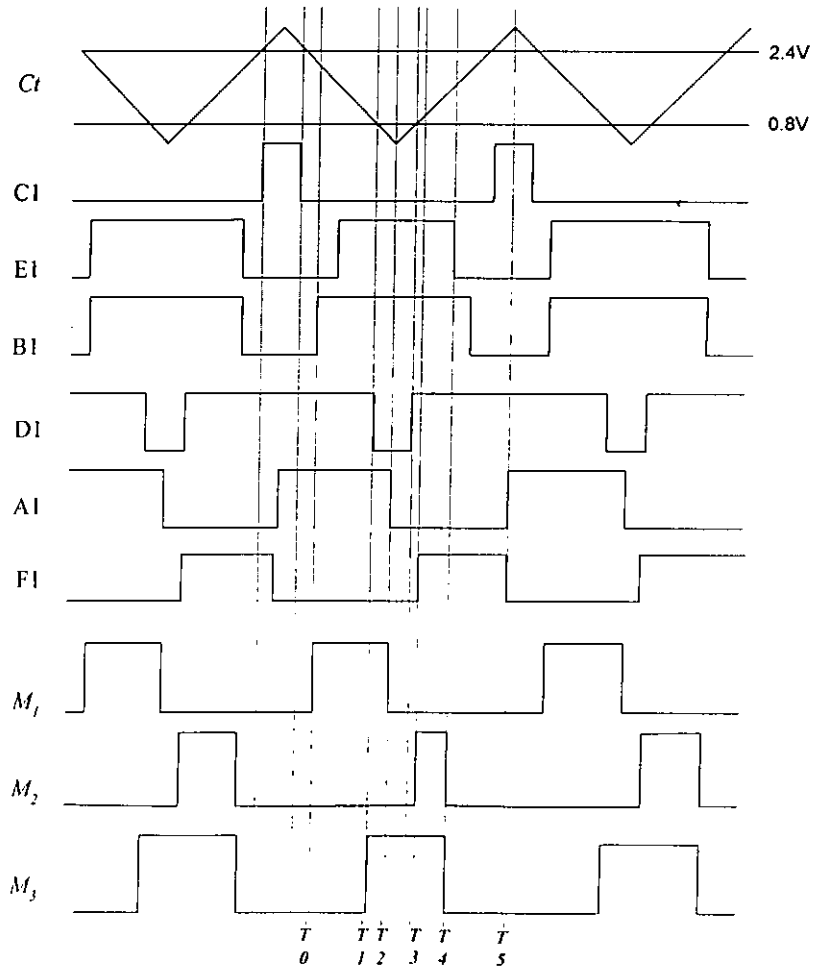


Figure 52 The logic control waveform.

3.6 Steady state analysis

3.6.1 Calculation of power factor

The proposed boost converter is operating in DCM operation. The average behavior model can be used to analyse the power factor performance of the proposed converter as what have been shown in [2]. The following shows the derivation of the average behavior model of the boost regulator. The averaged input current is given by

$$\bar{i}_i = \frac{d^2 T_s}{2L_1} \frac{|V_{ac}|}{1 - \frac{|V_{ac}|}{vc}} \tag{3-12}$$

where vc is the voltage of capacitor C_1, $|V_{ac}|$ is the input voltage, d is the duty cycle, T_s is the switching period and L_1 is the inductance of the input inductor.

Putting $|V_{ac}| = \hat{E}\,|\sin\omega t|$ becomes

$$\bar{i}_i = \frac{d^2 T_s}{2L_1} \frac{\hat{E}\,|\sin\omega t|}{1 - \frac{\hat{E}\,|\sin\omega t|}{vc}} \tag{3-13}$$

Under the steady-state operation, vc can be considered as a DC voltage and denoted by Vc. Hence, for the purpose of maintaining a regulated output voltage, the duty cycle can be assumed to be constant and denoted by D. The *rms* value of the averaged input current is

$$\overline{i_{irms}} = \frac{D^2 \hat{E} T_s^2}{2\sqrt{\pi} L_1} \sqrt{\int_0^{\pi} \frac{\sin^2\theta}{\left(1 - \frac{\hat{E}\sin\theta}{Vc}\right)^2} d\theta} \tag{3-14}$$

The input power is

$$Pi = \frac{\omega}{\pi} \int_0^{\frac{\pi}{\omega}} e(t)\,\bar{i}_i(t)\,dt \tag{3-15}$$

where t has been substituted by $\frac{\theta}{\omega}$.

$$= \frac{1}{\pi}\int_0^{\pi} \hat{E}\sin\theta \frac{D^2 T_s}{2L_1} \frac{\hat{E}\sin\theta}{1-\frac{\hat{E}\sin\theta}{Vc}} d\theta \tag{3-16}$$

$$= \frac{D^2 \hat{E}^2 T_s}{2\pi L_1}\int_0^{\pi} \frac{\sin^2\theta}{1-\frac{\hat{E}\sin\theta}{Vc}} d\theta \tag{3-17}$$

Hence, the power factor (*p.f.*) of the boost regulator is

$$p.f. = \frac{P_i}{e_{rms}\, \bar{i}_{irms}} \tag{3-18}$$

$$p.f. = \sqrt{\frac{2}{\pi}} \frac{\int_0^{\pi} \frac{T_s \sin^2\theta}{1-\frac{\hat{E}\sin\theta}{Vc}} d\theta}{\sqrt{\int_0^{\pi} \frac{T_s \sin^2\theta}{\left(1-\frac{\hat{E}\sin\theta}{Vc}\right)^2} d\theta}} \tag{3-19}$$

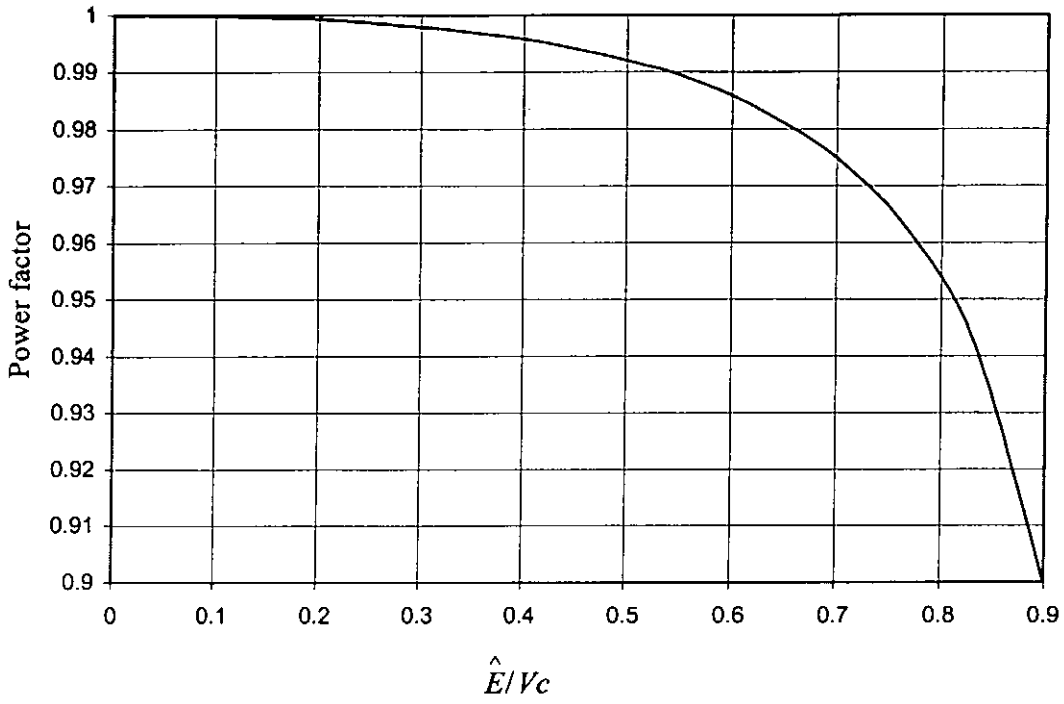


Figure 53 Power Factor versus $\hat{E}/Vc$.

In general the total harmonic distortion (*THD*) can be found as

$$THD = \sqrt{\frac{1}{\left(\frac{p.f.}{\cos\phi}\right)^2} - 1} \tag{3-20}$$

where $\cos\phi$ is the displacement factor. In the boost switching regulator the $\cos\phi = 1$.

Figure 54 shows the plot of THD versus $\hat{E}/Vc$.

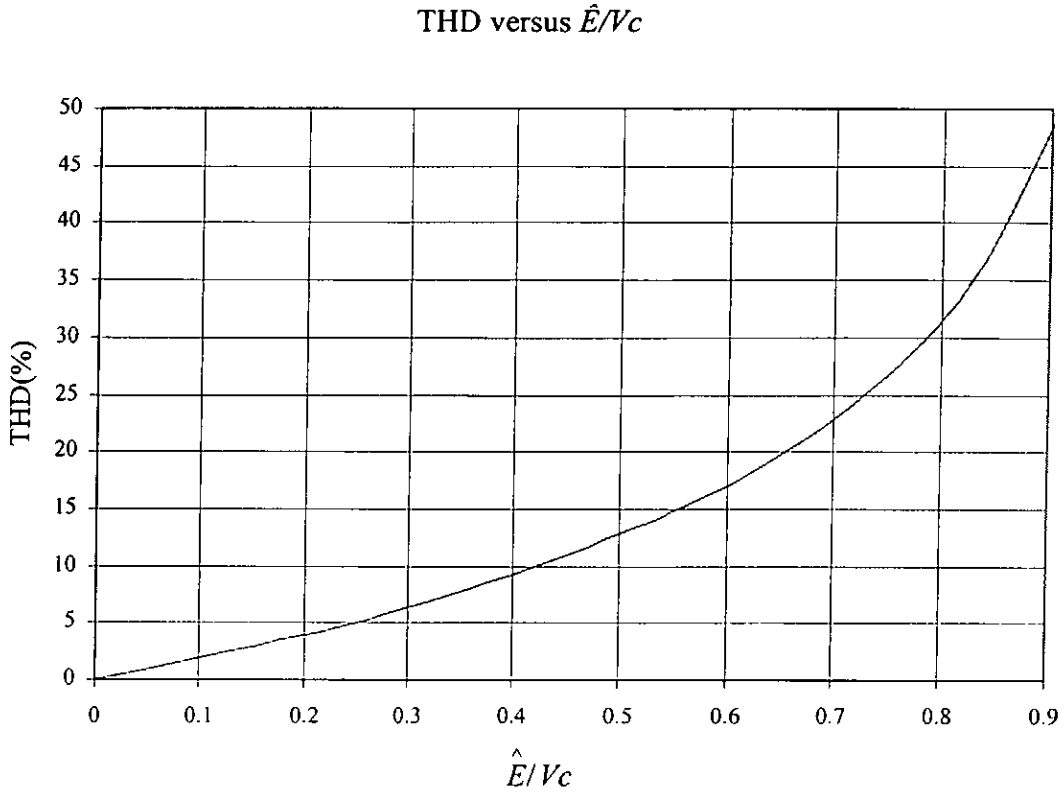


Figure 54 The $\hat{E}/Vc$ versus THD.

Based on the above analysis, the proposed circuit can provide a power factor correction.

3.7 Experimental result and verification

Implementation:

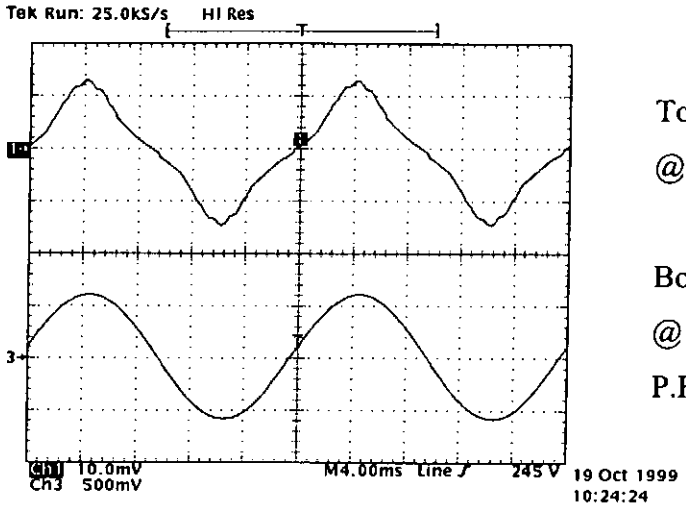
A 230 W experimental prototype has been built. The specifications of the prototype and the related components are shown in Table 5.

Parameter	Components/Values
Ê	$220\times\sqrt{2}$
Vo	38 V
Io	0.6-6 A
fs	100 kHz
C_1	330 μF
Co	1000 μF
L_1	180 μH
L_2	220 μH
Transformer Core	EDT-29 3C85
Transformer Lm	2 mH
Primary Winding	80 T
Second Winding	22 T
D1-D8	MUR460
L_1 core	*Kool Mu 77930-A7
L_2 core	*Kool Mu 77894-A7
M_1, M_2, M_3	IRF840

Table 5 Specifications and components for the proposed ZVS SMPS with PFC.

3.7.1 Input Current waveform

The waveform of the input line current and input line voltage are shown in Figure 55.

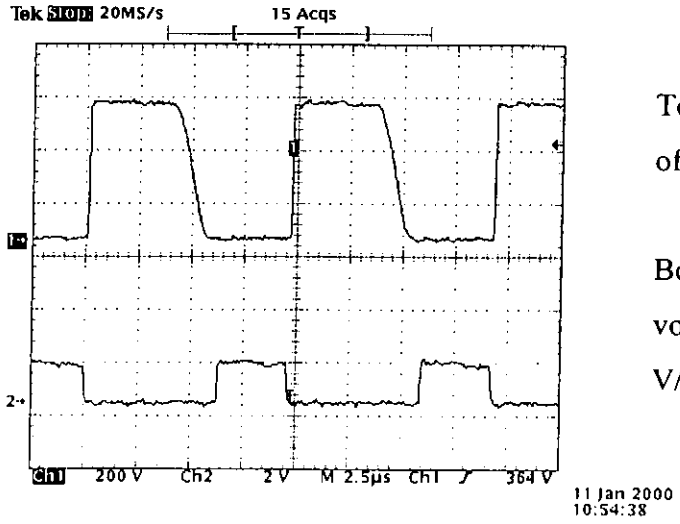


Top trace: Line current
@ 1 A/div

Bottom trace: Line voltage
@ 250 V/div
P.F. = 0.985

Figure 55 Line voltage and current.

The waveform of the drain voltage and gate drive voltage are shown in Figure 56.



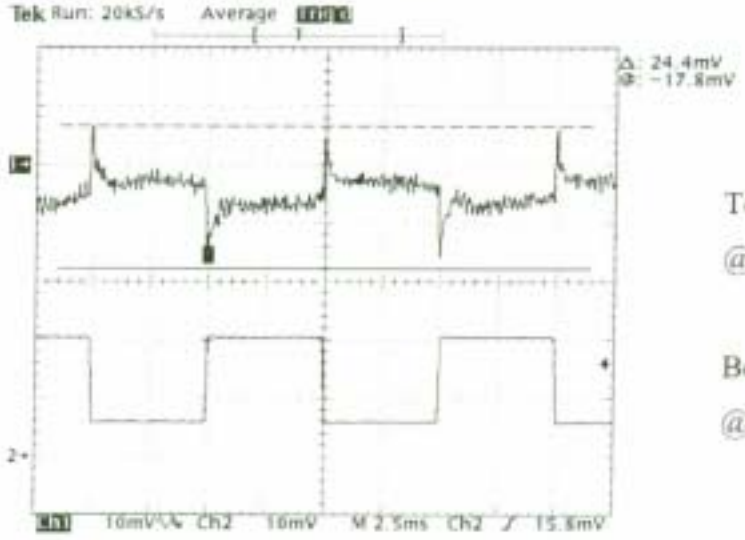
Top trace: The drain to source voltage of MOSFET M_3@ 200 V/div

Bottom trace: The gate to source votlage of the MOSFET M_3 @ 20 V/div

Figure 56 Drain voltage and gate drive voltage.

3.7.2 Dynamic load response

Experimental result of the dynamic load response is shown in Figure 57, where the load current is changed from 1 A to 4 A .



Top trace: The output voltage @10 mV/div

Bottom trace: The load current @ 2 A/div

Figure 57 Load current from 1 A to 4 A.

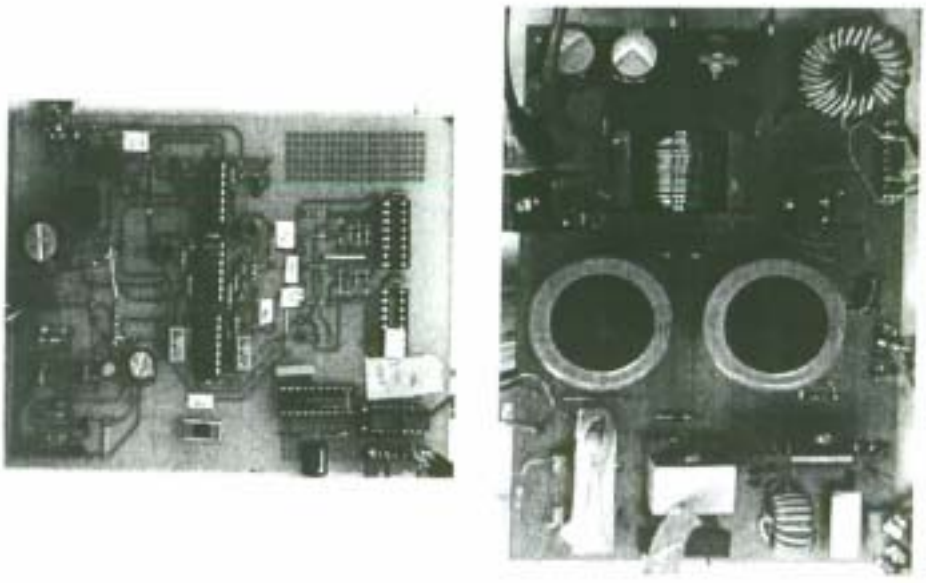


Figure 58 Hardware prototype

3.7.3 Harmonic distortion measurement result

In IEC1000-3-2 regulation [1], the general-purpose switching mode power supply belongs to class D equipment. The maximum allowable harmonic limits and the measured result are given in Table 6.

Harmonic order N	Relative harmonic limits mA(rms)/W	Measured result mA(rms)/W
	Class D Limit, mA(rms)/W	
3	3.4	1.060
5	1.9	0.145
7	1	0.008
9	0.5	0.002
11	0.35	0.001
13	0.296	0.14
15<N<39	3.85/N	

Table 6 Class D harmonic limits and measured result

According to the experimental result of the proposed circuit in Table 6, the input line current of the proposed circuit meets the limits of IEC1000-3-2 [1] regulatory requirement. The experimental result and the requirement are shown in Figure 59.

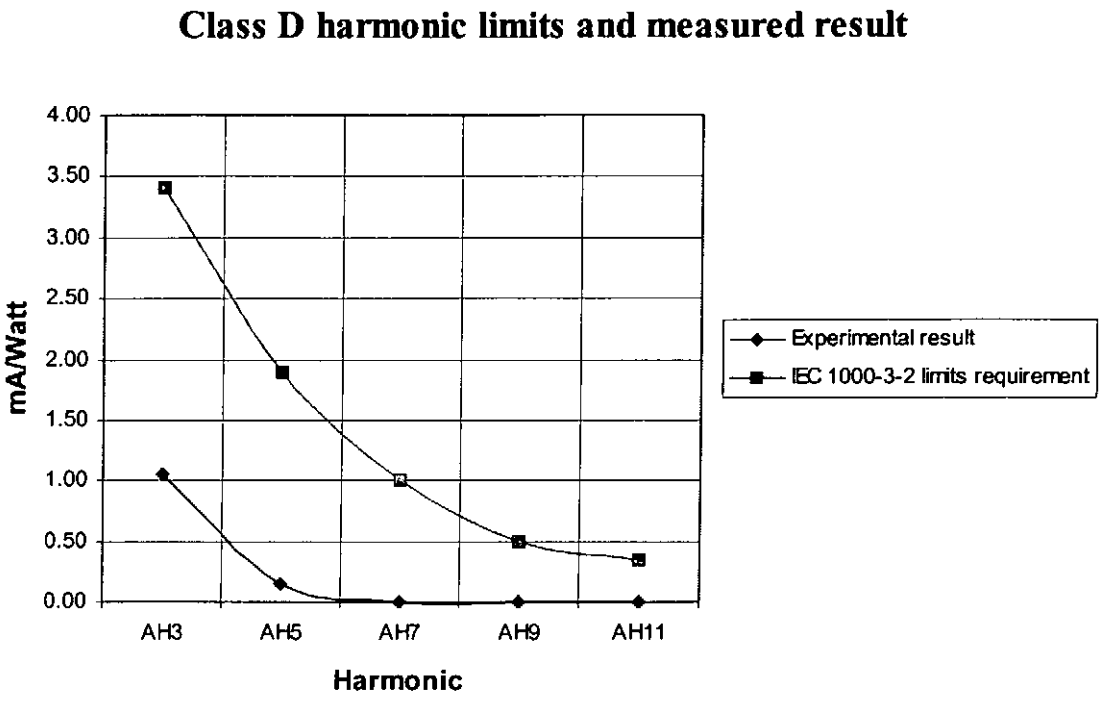
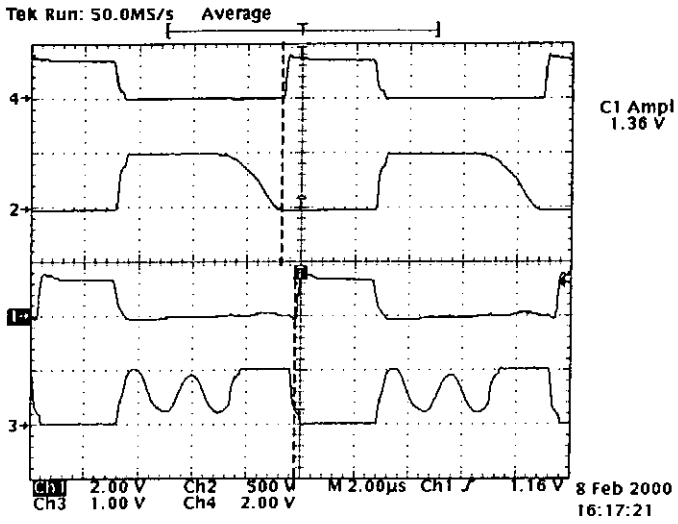


Figure 59 The prototype harmonic current and Class D harmonic limit.

3.7.4 Measured waveforms which demonstrate soft switching operation



Channel 2 Vds MOSFET M_3

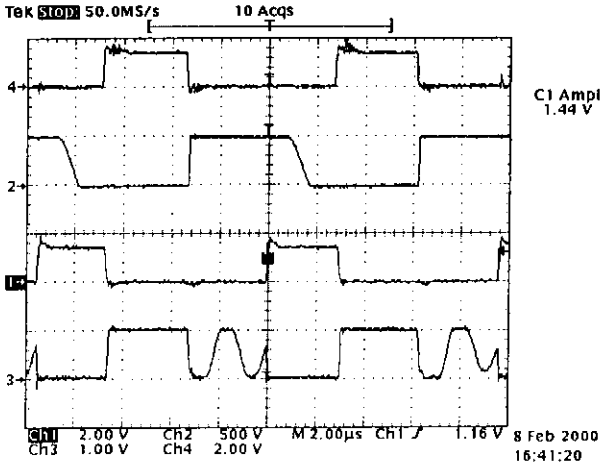
Channel 1 Vgs MOSFET M_2

Channel 3 Vds MOSFET M_2

Channel 4 Vgs MOSFET M_3

Pout=38 Vdc@ 4 A

Figure 60 The switching waveform of the *M3* and M_2.



Channel 4 Vgs of the MOSFET M_3

Channel 2 Vds of the MOSFET M_3

Channel 1 Vgs of the MOSFET M_1

Channel 3 Vds of the MOSFET M_1

Load 4 A 38 Vdc

Figure 61 The switching waveform of the M_1 and M_2.

Based on the waveforms shown in Figure 60 and Figure 61, MOSFET M_2 and MOSFET M_3 clearly have zero-voltage-switching operation.

3.7.5 Reduction in dissipations on active switches

The conventional circuit and the proposed circuit are compared at an output level of 150 W. The temperatures of switches in both implementations are shown in Figure 62. The result indicates that the temperature of active switch M_3 of the proposed circuit becomes 11 °C lower as compared to that of conventional implementation. However, there is an increase of 5 °C in active switch M_2. The temperature of M_1 remains unchanged. The slightly increase in temperature of switch M_2 is due to the fact that the body diode in the switch M_2 is being used as the part of boost converter in the proposed circuit. In the conventional circuit, an external diode is employed. In order words, the actual dissipation in M_2 has been reduced. An arrangement to measure the heat dissipation of switch M_2 (without the influences from its body diode) is shown in Figure 64.

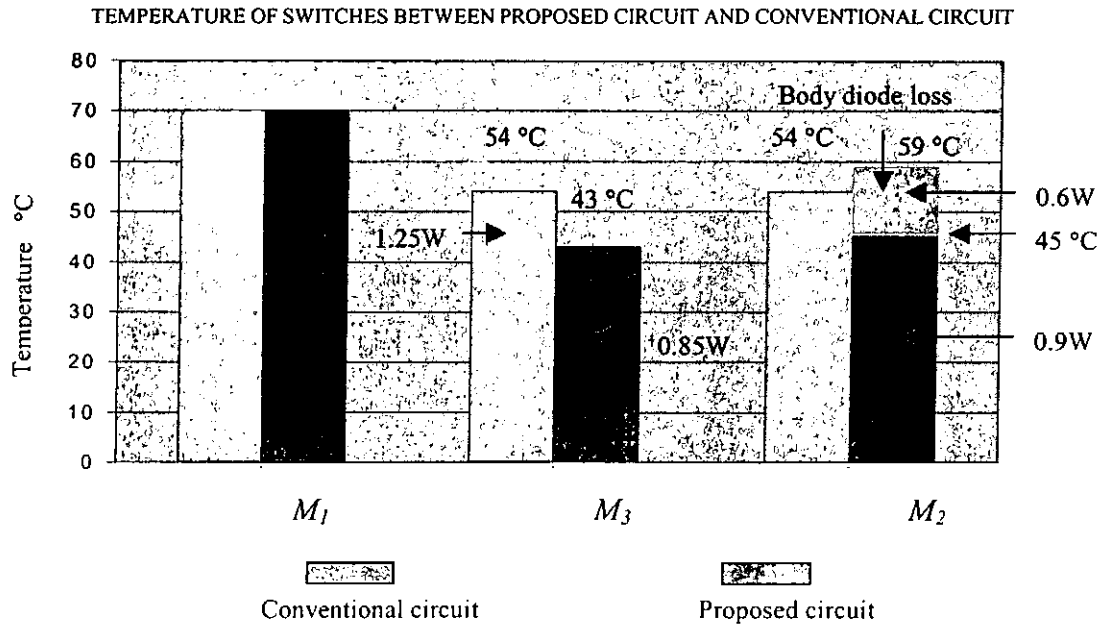


Figure 62 Dissipations in different topologies

In order to find out the amount of dissipation in W, a given amount of DC power is applied to switch M_3 under similar thermal condition and the temperature of switch M_3 is measured and plotted against power dissipation as shown in Figure 63. Based on

Figure 62 and Figure 63, the power dissipations of M_3 in the proposed and conventional circuits are estimated as 1.25 W and 0.85 W respectively. From the result of Figure 62, it is clear that the proposed circuit can provide soft switching function to switches M_2 and M_3 . The amount of reduction in switching loss in M_2 is about 32 %.

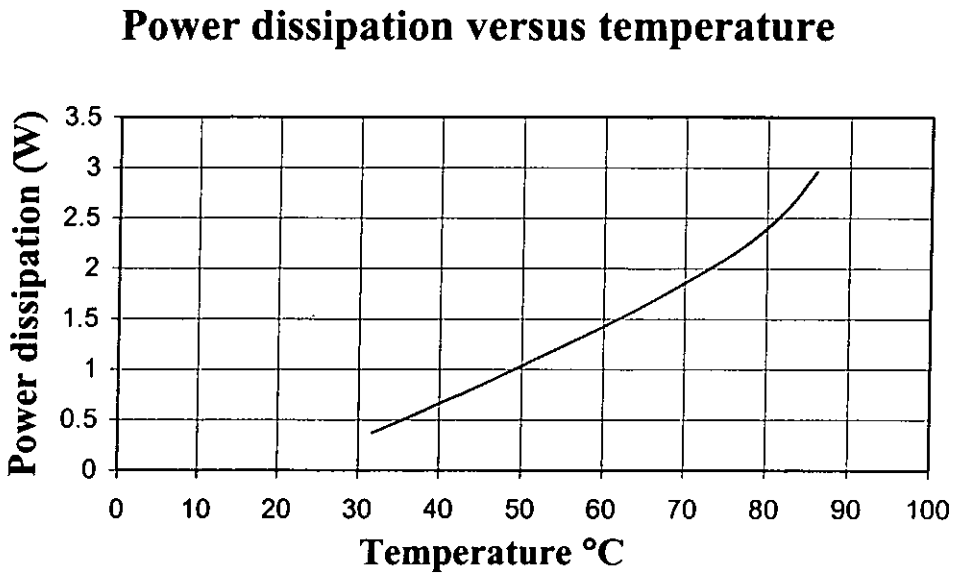


Figure 63 Power dissipation versus the temperature.

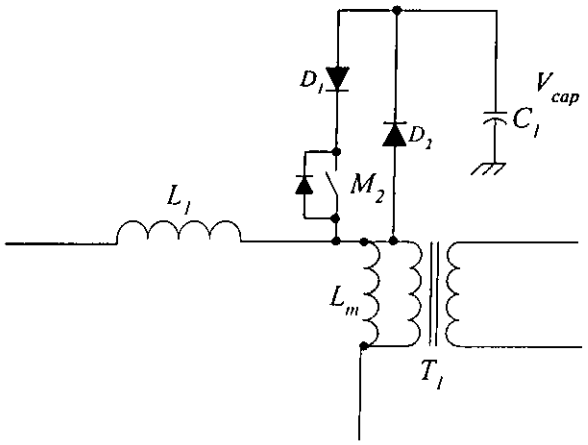


Figure 64 The way to isolate the body diode of M_2.

3.8 Summary

An active boost power factor correction circuit with soft switching is proposed. It is based on a new proposed converter and a controller with specially designed gating sequence. The proposed circuit can provide a high efficiency and low harmonic distortion solution for power factor correction applications. A regulated 230 W, 220 V_{ac} input and 38 V output power factor correction circuit has been implemented. The proposed circuit reduces about 32 % power loss in some of active switches. Compared with the conventional circuits, the proposed circuit can reduce the component count and provide a higher efficiency. Also, it can reduce the EMI noise. Since the proposed circuit can reduce the power loss of the main switch M_3 by about 32 %, this design is suitable for integrating the main switch and the controller circuit into a single package. The only drawback of the proposed circuit is that it needs a higher bulk capacitor voltage for the main transformer to reset the magnetizing current. Therefore, it may impose a higher voltage stress on the active switches.

CHAPTER 4

PROPOSED PULSE-SKIP MODULATION SMPS WITH PFC

4.1 Introduction

A conventional PFC switching regulator consists of a PFC corrector and a DC-DC converter. For low-power applications, PFC regulators usually operate in DCM operation. The advantage of DCM PFC regulators is that PFC function can be obtained inherently without employing complex controlling method, e.g., current sensing.

Generally, PFC correctors in DCM operation under constant switching frequency are very simple in terms of controller design. However, they impose higher voltage stress on the energy-storage capacitor. They are generally also less efficient and limited to low-power applications. It is possible to reduce both the voltage stress on the energy-storage capacitor and the dissipaton on the active switch if critical mode operation is employed in a boost PFC corrector. However, this results in a continuous variation of the switching frequency (in critical mode operation), which may produce visually noticeable interference in some applications, e.g., TVs and computer monitors.

This chapter proposes a new approach to the control method for DCM boost PFC correctors. In this approach, the on time of the active switch of a DCM boost PFC corrector is kept constant while its switching frequency is varied according to the input voltage in a quantised manner. Based on this new approach, the voltage stress on the energy-storage capacitor in the DCM boost PFC corrector can be kept to a minimal because the corrector is operated close to a critical mode. In addition, the duty cycle of the active switch in the DCM boost PFC corrector becomes very small when the input line voltage is reaching to its high value, i.e., most of the input current goes through the diode instead of the active switch in the DCM boost PFC corrector. Therefore the dissipation of the active switch is very low when the input line current is at its peak. In addition, the quantised variation in the switching frequency will not cause visually noticeable interference on applications like TVs or computer monitors because the

switching frequency always changes in an integer multiple fashion (and therefore the interference spectrum falls into a set of multiple lines which are the harmonics of the switching frequency). The interference in a conventional critical mode operation has a continuous spectrum between the highest and lowest switching frequencies. We coin this approach as "Pulse-Skip Modulation".

In the following sections, we will discuss how the switching frequency should be controlled such that the DCM PFC corrector can achieve "near" harmonic-free input line current as well as low voltage stress operation. A practical prototype has also been built to show that this approach can achieve a low dissipation on the active switch.

4.2 Circuit operation

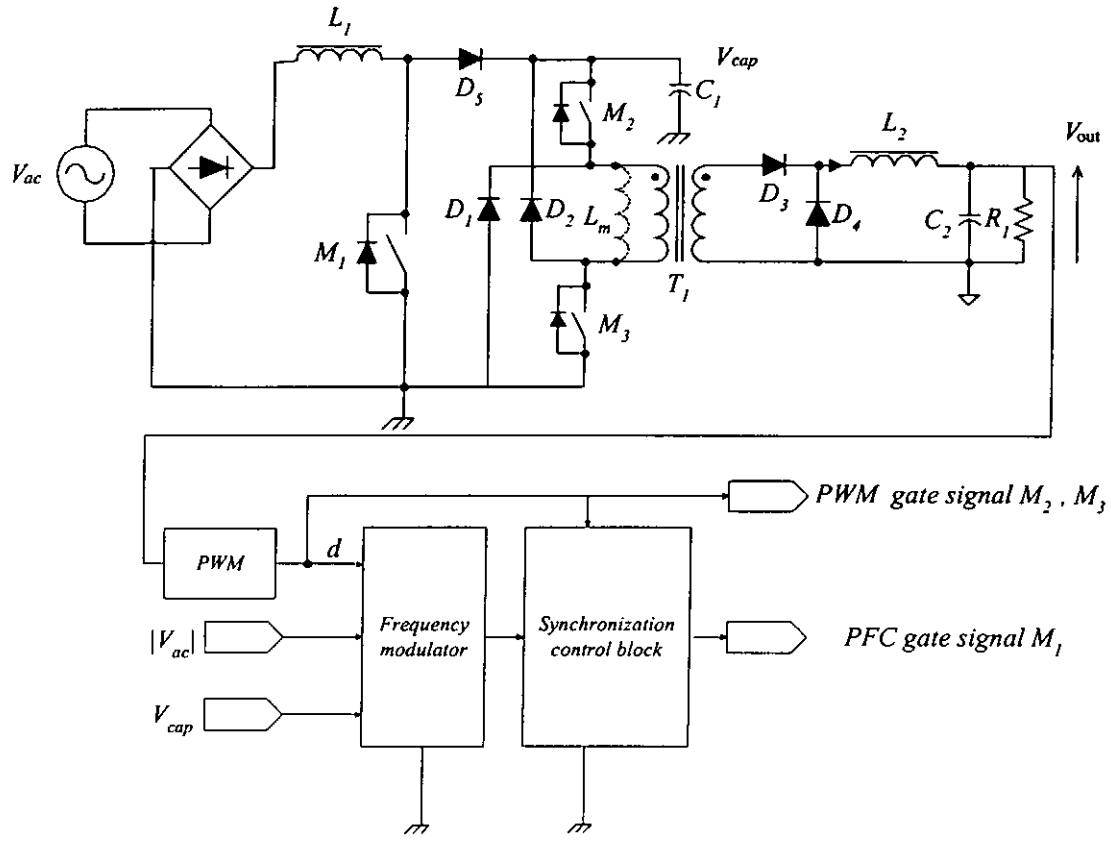


Figure 65 The schematic of the proposed pulse-skip modulation PFC SMPS

The proposed power supply circuit has a DCM boost PFC corrector in cascade with a two-switch forward converter. The controller in the proposed consists of two parts: one part is the PWM circuit for controlling the forward converter to achieve output voltage regulation; the another part is a frequency modulator and a synchronization control block for controlling the DCM boost PFC corrector to achieve an unity input power factor.

Under the full load condition, the on time of switches M_2, M_3 in the forward converter is roughly constant and can be determined by the voltage across the energy-storage capacitor C_1, i.e, the duty cycle of the PWM controller is roughly constant. The on time of switch M_1 in the DCM PFC corrector is set to be equal to the on time of switches M_2, M_3 . However, the off time of switch M_1 is varied according to the control of both frequency modulator and pulse-skip control logic block. Basically the frequency

modulator controls the off time of switch M_1 according to the rectified input voltage $|V_{ac}|$ and the voltage V_{cap} on the energy-storage capacitor. The off time becomes longer and longer when $|V_{ac}|$ is approaching V_{cap} as what is shown in Figure 66. If the off time is properly controlled in a manner which is described in the later section, the DCM boost PFC corrector can achieve unity input power factor. In fact, the PFC boost corrector and the two-switch forward converter have the same amount of on time but very different off time, i.e., they operate at different switching frequencies, and the PFC boost corrector can remain turnoff while the two-switch forward converter are being switched on for several times. This phenomena can be easily observed when the input is at a high voltage. The typical waveforms of the proposed circuit is shown in Figure 66 .

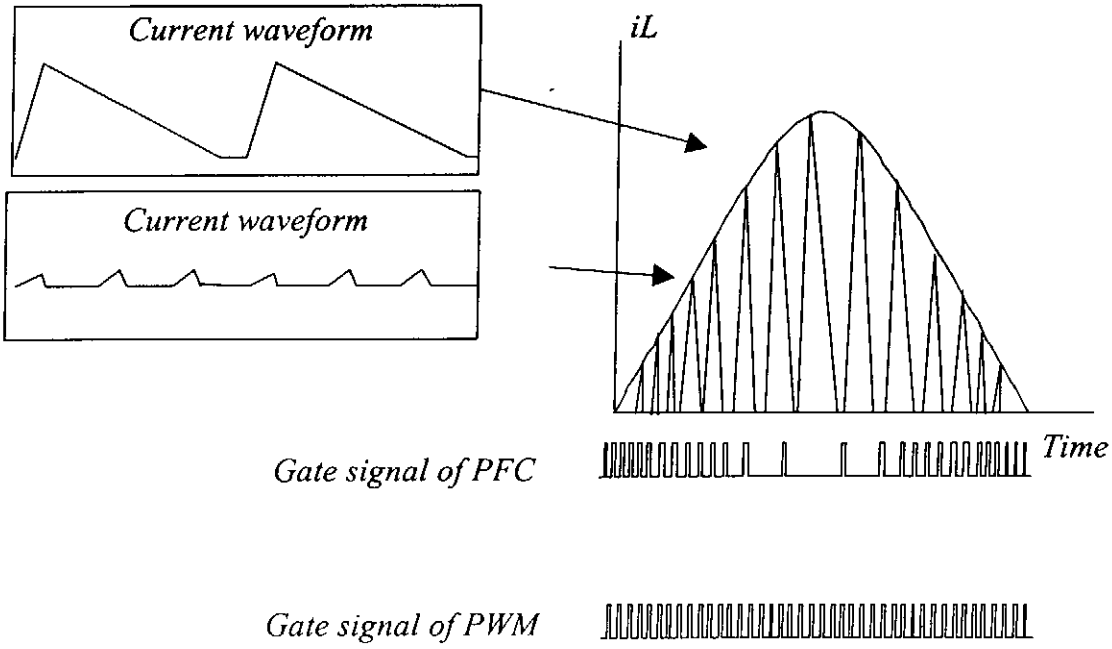


Figure 66 Typical waveforms of the proposed PFC boost corrector

The function of the synchronization control block is used to make sure that the on times of the PFC boost corrector and two-switch forward converter occur at the same moment, i.e, their switching frequencies have harmonic relationship. The proposed controller can be easily integrated into an 8-pin PFC + PWM combo chip.

4.3 Circuit analysis

4.3.1 Output voltage regulation

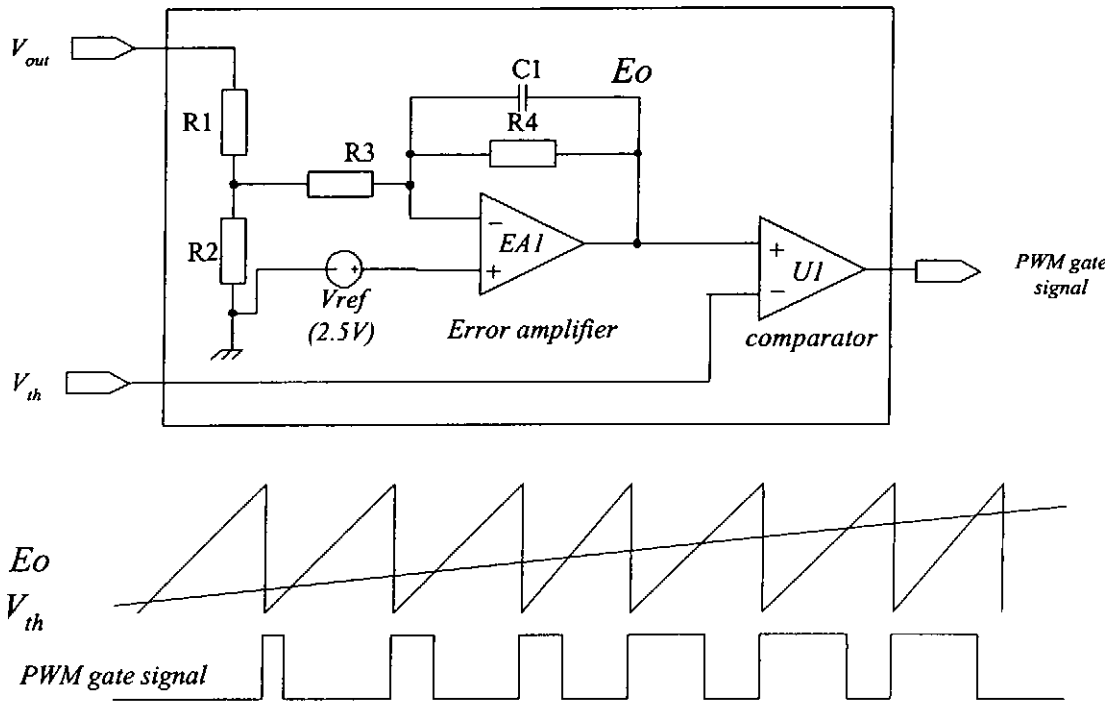


Figure 67 PWM controller block

The output voltage regulation is achieved by a conventional PWM voltage mode feedback control. The PWM control circuit is shown in Figure 67. In this circuit, V_{out} is the output voltage and V_{th} is a sawtooth waveform. Resistors R1 and R2 are used to sample of the output voltage. Resistors R3, R4 and capacitor C1 form the gain control and compensation network which control the loop gain of the two-switch forward converter and the phase and gain margin of its feedback control loop. When V_{out} is smaller than the internal voltage V_{ref} (2.5V), the output E_o of error amplifier $EA1$ will increase, then sawtooth signal V_{th} meets E_o at a later time. Therefore, the duty cycle of PWM gate signal will increase and the output voltage becomes higher and regulated against the reference voltage. The typical waveforms of the PWM controller are shown in Figure 67.

4.3.2 Unity power factor operation

When a PFC boost corrector operates in DCM with constant switching frequency, its input current has a near sinuoidal shape (good power factor) as shown in Figure 43 if the voltage of the energy-storage capacitor V_{cap} is relatively high compared with the input line voltage. The voltage stress can be reduced at the expanse of input power factor. However, if the PFC boost corrector operates at a variable frequency and the voltage stress can be reduced without deteriation of the input power factor.

The average of the input current of a PCF boost corrector operating in DCM is

$$i_{avg} = \frac{d^2 T_s}{2L_1} \frac{\hat{E}\left|\sin\omega t\right|}{1 - \frac{\hat{E}\left|\sin\omega t\right|}{V_{cap}}} \tag{4-1}$$

where d is the duty cycle, T_s is the switching period, L_1 is the input inductor, and $\hat{E}|sin\omega t|$ is the rectified input voltage.

If the on time of the active switch is fixed, i.e., $T_{on} = dT_s$, equation (4-1) becomes

$$i_{avg} = \frac{T_{on}^2}{2L_1 T_s} \frac{\hat{E}\left|\sin\omega t\right|}{1 - \frac{\hat{E}\left|\sin\omega t\right|}{V_{cap}}} \tag{4-2}$$

If the switching period can be changed according to the following expression

$$T_s = T_s' \left(\frac{V_{cap}}{V_{cap} - \hat{E}\left|\sin\omega t\right|} \right) \tag{4-3}$$

where T_s' is a constant, then the average current becomes

$$i_{avg} = \frac{T_{on}^2 \hat{E}\left|\sin\omega t\right|}{2L_1 T_s'} \tag{4-4}$$

where the average input current is proportional to the input line voltage, i.e., unity input power factor. It is clear that this variable frequency scheme may cause undesirable interference to certain applications, e.g., TVs and computer monitor. However, the synchronization control block in Figure 65 can make sure that the actual switching frequency is changed in a quantized manner, i.e., the interference appears in harmonics of the switching frequency in a discrete line spectrum which is similar to that of conventional fixed switching frequency scheme.

4.4 Controller hardware implementation

The controller is constructed by two conventional PWM controllers. One PWM controller is used for controlling the output voltage V_{out} by means of the duty cycle of its PWM waveform through voltage-mode negative feedback. The other PWM controller is used to contruct the pulse-skip frequency modulator. The oscillation frequency of the sawtooth waveform generator in this PWM controller is under feedforward control of the rectified input voltage such that unity input power factor operation can be achieved.

4.4.1 Pulse-skip modulator

The pulse-skip modulator consists of two blocks, namely a frequency modulator block and a synchronization control block. The block diagram of the pulse-skip modulator is shown in Figure 68.

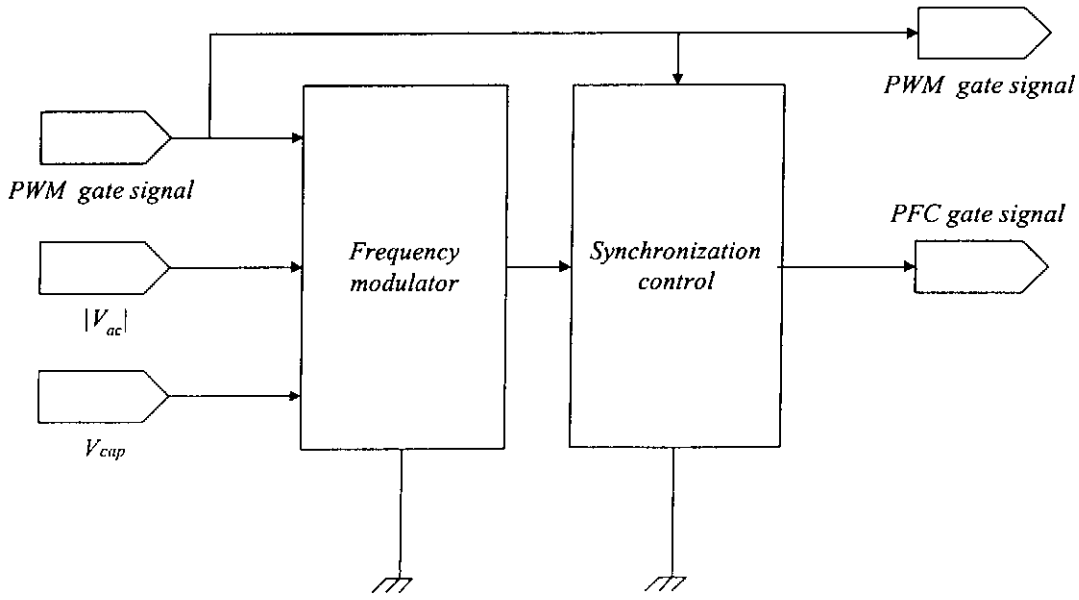


Figure 68 Block diagram of Pulse-Skip Modulator

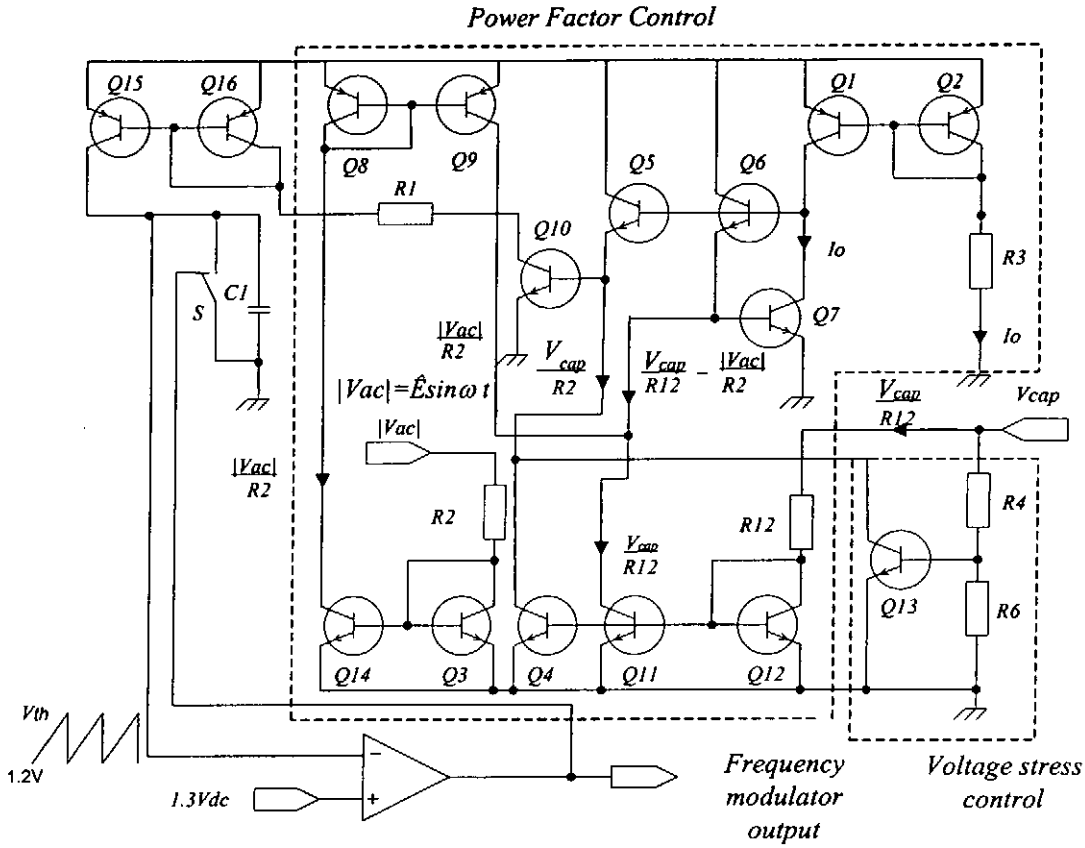


Figure 69 The proposed circuit of the frequency modulator.

The frequency modulator circuit is implemented by means of a translinear circuit and the sawtooth waveform generator of a UC3844 PWM controller and the detailed circuit diagram is shown in Figure 69. The period of oscillation of the sawtooth generator is governed by

$$T_s = \frac{CV_{th}}{I_{C15}} \tag{4-5}$$

The translinear circuit consists of a product-quotient circuit and six current mirrors. All transistors have a high current gain and same V_{be} voltage, therefore all current mirrors can be considered as ideal. In Figure 69, transistors *Q1* and *Q2* form a current mirror to provide collector current for *Q7*. The value of the collector current *Io* is controlled by resistor *R3*. Transistors *Q3*, *Q14* are connected as a current mirror to provide *Q8* and *Q9* with a collector current of $|\hat{E}\sin\omega t|/(R2)$. Transistors *Q11*, *Q12* are connected as a current mirror to provide *Q11* and *Q4* with a collector current of $|V_{cap}|/(R12)$. The product-quotient circuit is constructed with transistors *Q6*, *Q7*, *Q5* and *Q10*.

Based on the translinear circuit principle

$$I_{C6}I_{C7} = I_{C5}I_{C10} \tag{4-6}$$

$$I_{C10} = \frac{I_{C6}I_{C7}}{I_{C5}} \tag{4-7}$$

putting $R2 = R12$, $I_{C6} = \frac{V_{cap} - \hat{E}\left|\sin\omega t\right|}{R2}$, $I_{C7} = Io$, and $I_{C5} = \frac{V_{cap}}{R2}$,

then we have

$$I_{C10} = Io\frac{V_{cap} - \hat{E}\left|\sin\omega t\right|}{V_{cap}} \tag{4-8}$$

Because $I_{C10} = I_{C16} = I_{C15}$, then the period of oscillation T_s becomes

$$T_s = T_s'\left(\frac{V_{cap}}{V_{cap} - \hat{E}\left|\sin\omega t\right|}\right) \tag{4-9}$$

where $T_s' = CV_{th}/Io$. The maximum switching frequency occurs at the input voltage is zero or when I_{C10} is at its maximum. The function of resistor $R1$ is used to set the upper limit on the switching frequency. V_{cap} is sampled through resistor R4 and R6 to the base of $Q13$ for feedback comparison

$$V_{b13} = \frac{R6}{R4 + R6}V_{cap} \tag{4-10}$$

This feedback comparison provides a means to keep the voltage of the energy-storage capacitor V_{cap} at a constant value even at light load condition. For example, if V_{cap} increases at light load and this change will eventually decrease I_{C10} or increase the switching period such that the corresponding input current is reduced, i.e., V_{cap} is loosely regulated against load changes. The maximum voltage stress V_{cap} on the energy-storage capacitor can be estimated by

$$V_{cap_{\max}} \approx (\frac{R4 + R6}{R6})(V_{BE}) \tag{4-11}$$

The logic circuit of the synchronization control block is shown in Figure 68. The logic circuit consists of two D-type Flip-Flops, two NOT gates and a gate-drive buffer. The synchronization control block has two inputs which are the trigger pulse generated from the frequency modulator and the PWM gate signal from the PWM controller that controls the output voltage regulation. The output of the synchronization control block is a PFC gate pulse. The function of the synchronization block is to make sure that the PFC gate pulse occurs after there is an FM trigger pulse. The waveforms of the synchronization control block in Figure 70 shows two cases of this situation: the set of upper waveforms is the case where the FM trigger pulse has a high frequency, whereas the set of lower waveforms is the case where the FM trigger pulse has a lower frequency and it is clear that the PFC gate pulse has a lower frequency and PFC gate pulse and PWM gate pulse are always in synchronization.

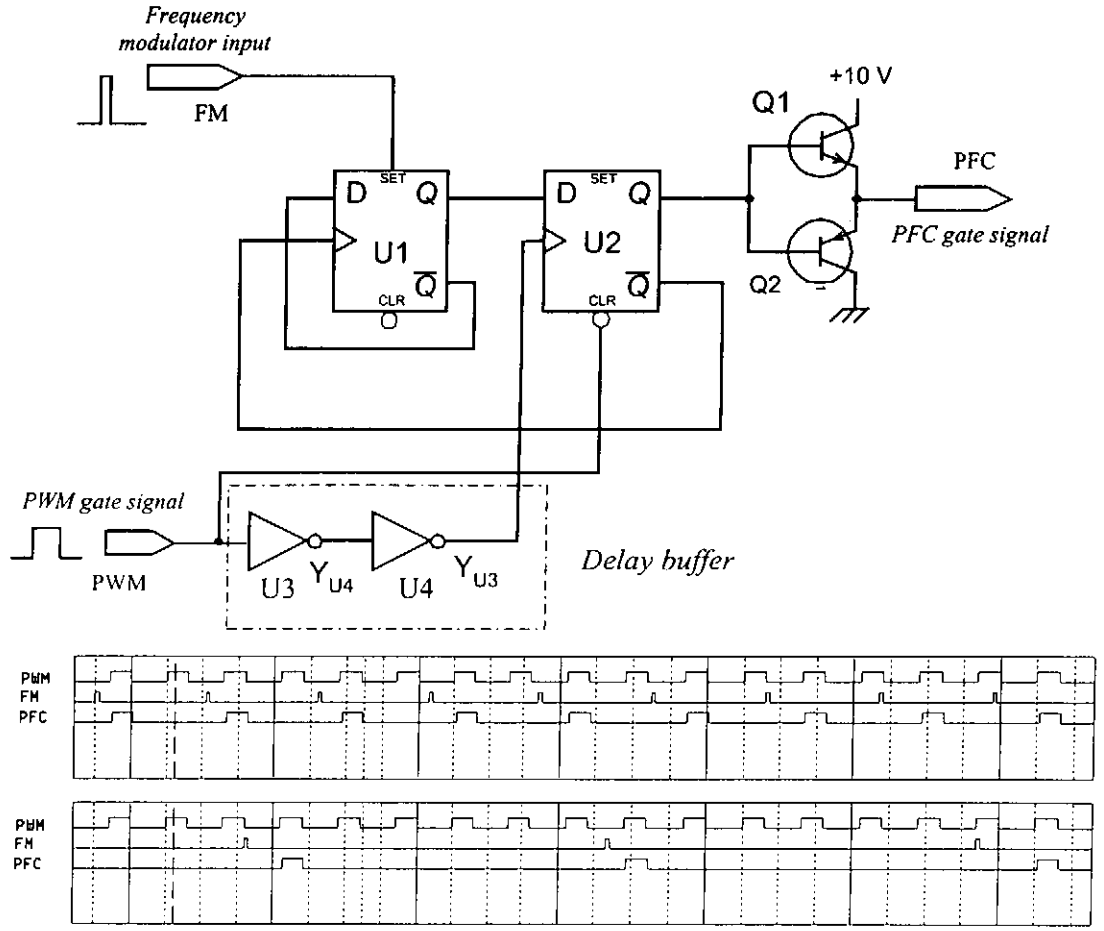


Figure 70 The synchronization control block and its typical waveforms

When the synchronization block detects an FM trigger signal, D type Flip-Flop U1 is set to a logic "high", i.e., Q_{U1} is logic "high". After this, when the PWM signal has a "low to high" transition, the signal on Q_{U1} will be passed to D type Flip-Flop U2 and PFC gate signal will be at high level. If the PWM signal returns to a "low" level, D type Flip-Flop U2 will be cleared and the PFC gate signal is changed back to low. The function of NOT gates is to provide some delay between the trigger pulse and clear signal of U2.

4.5 Design considerations

In this proposed Pulse-Skip Modulated PFC power supply circuit, the switching frequency of the PFC boost corrector is varied for maintaining a unity input power factor operation and keeping the voltage of the energy-storage capacitor at a low value even at a light load condition. The maximum switching frequency is set to 200 kHz. In order to avoid the switching frequency varied down to an audible range, the control scheme used in the pulse-skip modulation limits has to set a limit on the minimum switching frequency.

Based on the required operation frequency, the value of R3 are determined as follows. Suppose that a UC3844 PWM controller is employed to build the sawtooth waveform generator. There is an internal Flip-Flop in the UC3844, therefore the actual oscillation frequency of the sawtooth waveform generator has to be designed at 400 kHz. The period of the sawtooth waveform is governed by

$$Ts' = \frac{CV_{th}}{I_{C10}} \tag{4-12}$$

The maxmium switching frequency is 200 kHz. Based on equation (4-12), the value of the timing capacitor C is found to be 1.5 nF (Assuming I_{R3} = 1 mA and V_{th} =1.6 V). If we set the minimum switching frequency to 40 kHz (Ts' = 25 μs), then the corresponding I_{C10} should be 200 μA when the input voltage is at its peak value. If the peak voltage of the input voltage is 311 V, then the voltage of the energy-storage capacitor can be estimated by

$$\left(\frac{V_{cap}}{V_{cap} - \hat{E}\sin\theta} \right) = 5 \tag{4-13}$$

and the value is to be 388 V.

4.5.1 Implementation

A 200 W experimental prototype has been built. The specifications and component list are shown in Table 7. The prototype employs two UC3844 as the PWM controller for the two-switch forward converter and the pulse-skip modulator for the PFC boost corrector. The current-mode product-quotient circuit and all current mirrors are implemented by transistor arrays CA3096 in the experiment.

Parameter	Component values
E	$220\times\sqrt{2}$
Vo	36 V
Io	0.6-6 A
fs	40-200 kHz
C_1	330 uF
C_2	1000 uF
L_1	180 uH
L_2	220 uH
Transformer Core	EDT-29 3C85
Transformer Lm	2 mH
Primary Winding	80 T
Second Winding	22 T
D1-D10	MUR460
L_1 core	*Kool Mu 77930-A7
L_2 core	*Kool Mu 77894-A7
M_1, M_2, M_3	IRF840

Table 7 Specifications and components of pulse-skip modulation PFC power supply.

4.6 Experimental verification

4.6.1 Input current waveform

The input line current waveforms at heavy load and light load are shown in Figure 71 and Figure 72. At heavy load operation with less skip cycle, the input line current is partially harmonic-free with a measured THD of 15% and P.F. of 0.99. In the light load condition, the THD of proposed circuits is 30% and the P.F. of 0.95. It shows that the proposed pulse skip control can provide a significant reduction in the harmonic distortion. The voltage stress on the storage capacitor against output power is shown in Figure 76. It can be seen that the maximum voltage stress across the active switch is kept below the 400 V.

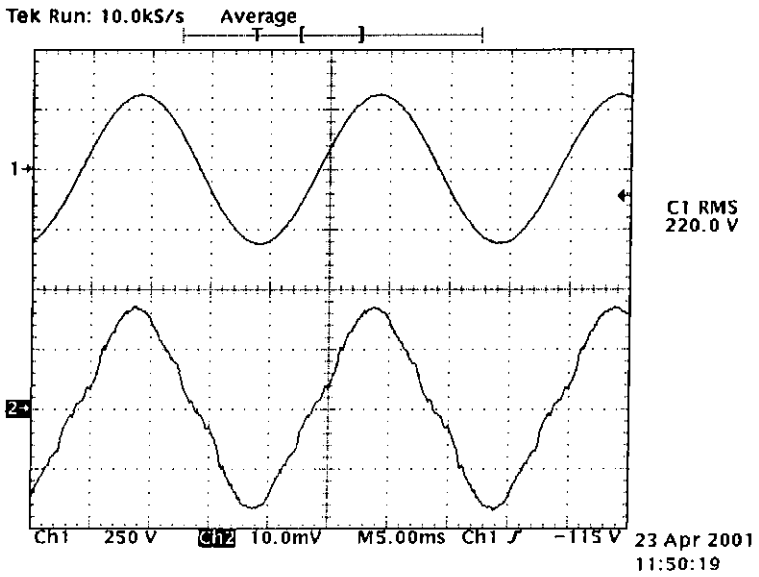


Figure 71 Input line voltage versus input line current.

Upper trace: Line voltage (100 V/div, 5 ms/div).

Bottom trace: Average line current (1 A/div, 5 ms/div, Po = 250 W).

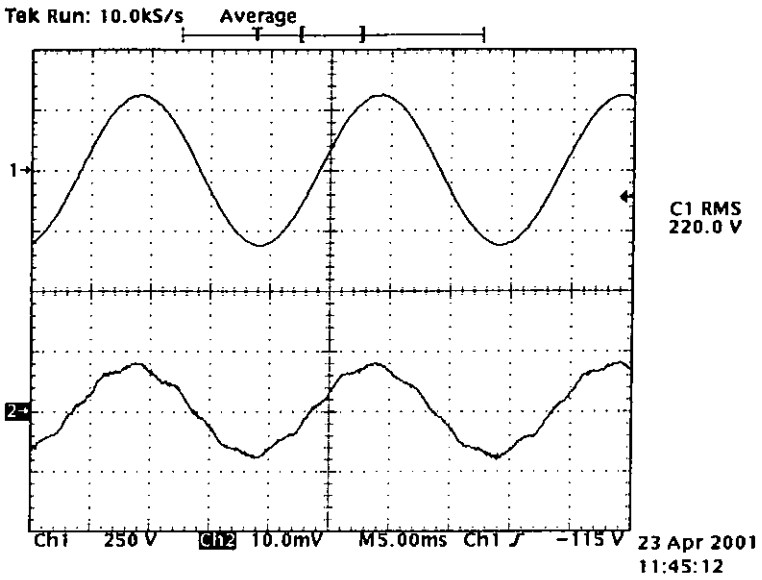


Figure 72 Input line voltage versus input line current.

Upper trace: Line voltage (100 V/div, 5 ms/div).

Bottom trace: Average line current (1 A/div, 5 ms/div, Po = 25 W).

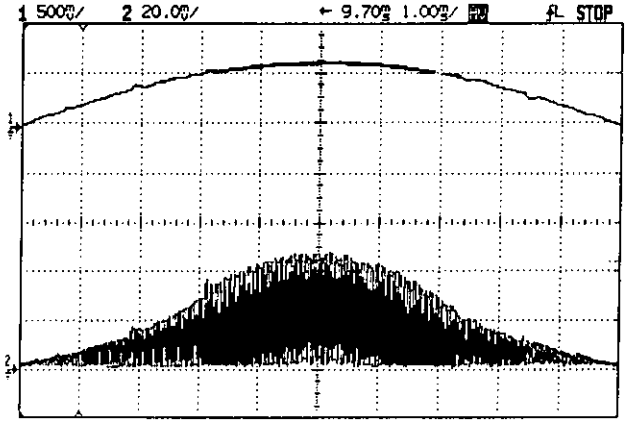


Figure 73 The input inductor waveform versus input voltage

Upper trace: The AC voltage 250 V/div.

Bottom trace: The input inductor current 1 A/div

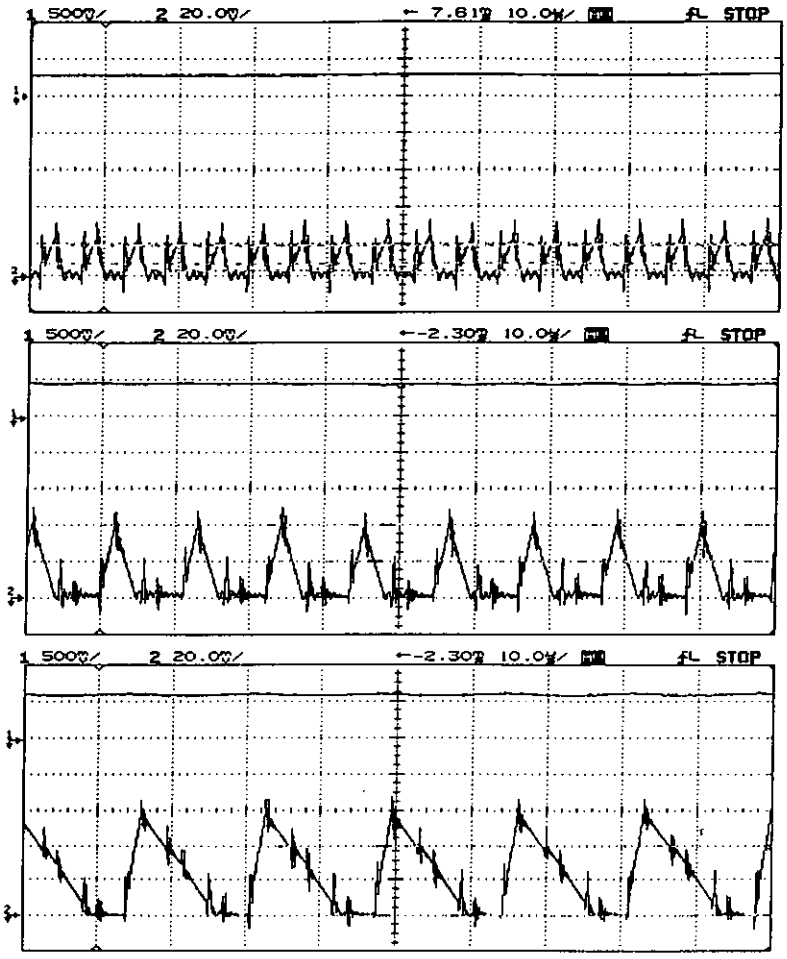


Figure 74 The input inductor waveform and voltage waveform

Channel 1 The AC voltage 250 V@div

Channel 2 The input inductor current 1 A@div

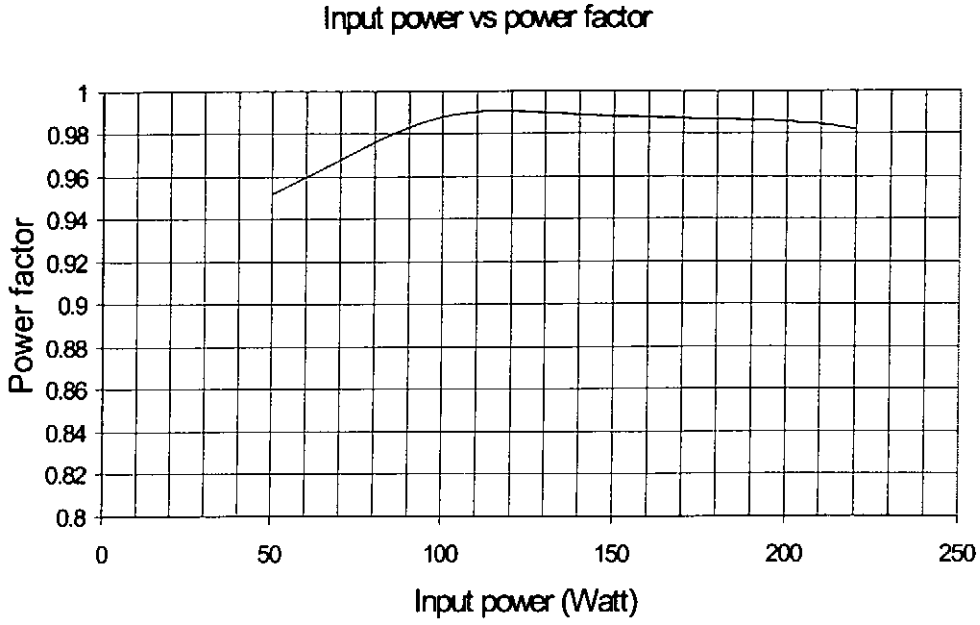


Figure 75 Measured result of the line input power versus the P.F.

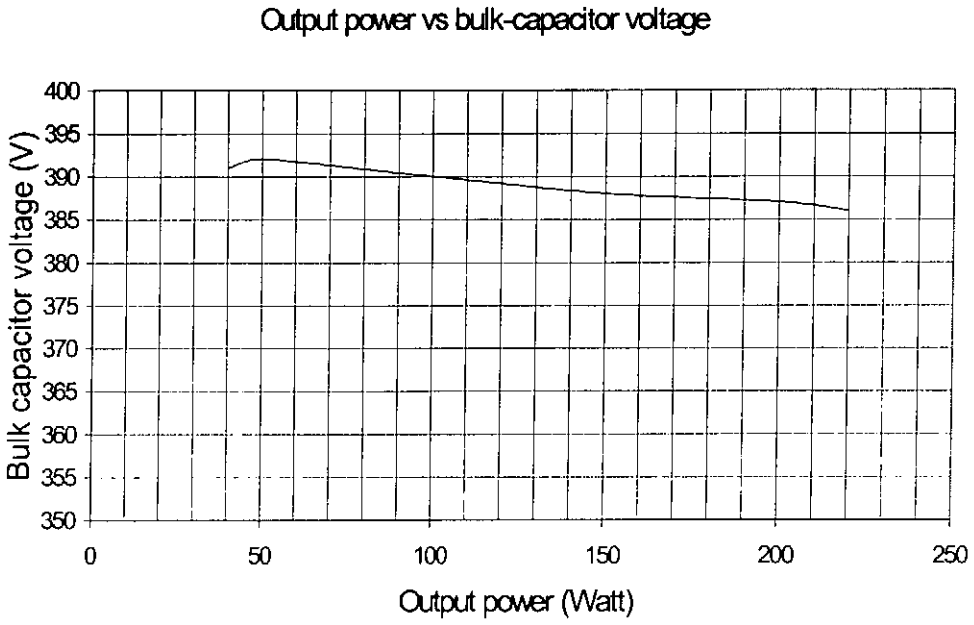


Figure 76 Measured result of voltage stress on the bulk capacitor versus output power

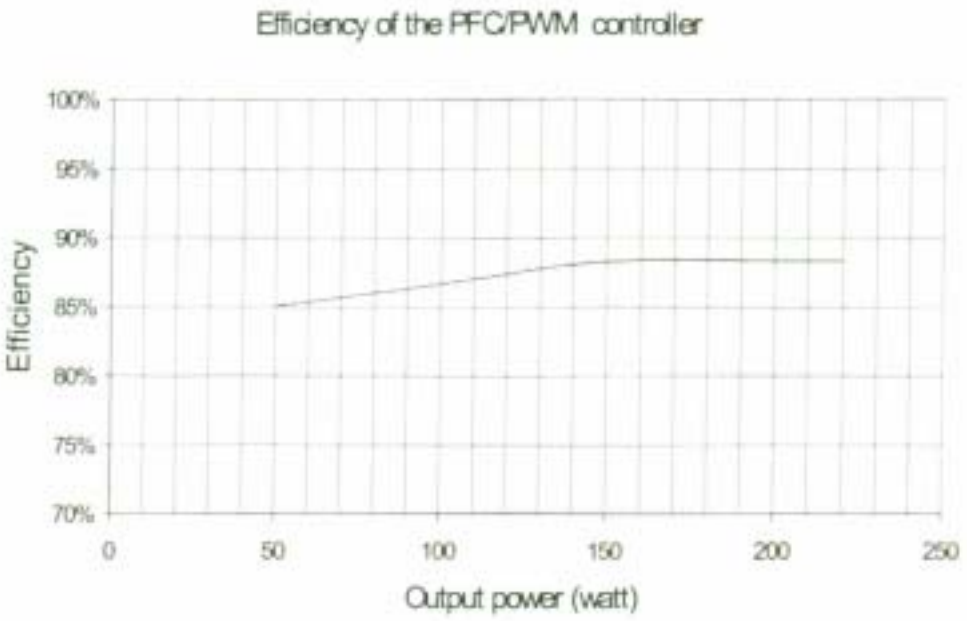


Figure 77 Measured overall efficiency

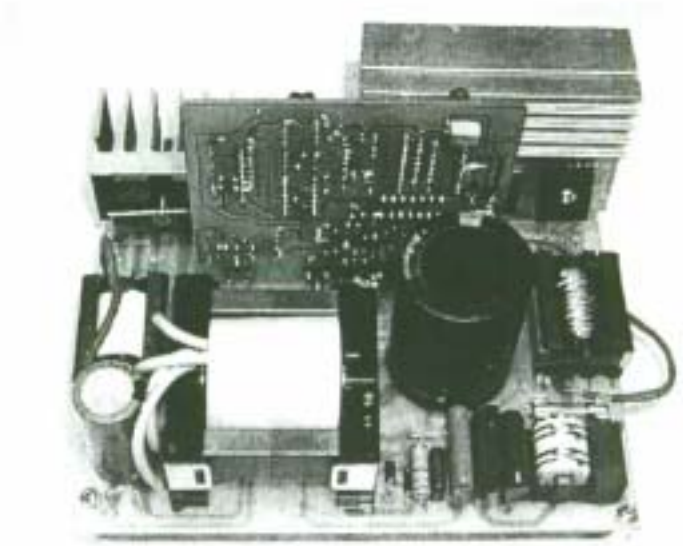


Figure 78 Hardware prototype

4.6.2 Summary

In this chapter, a pulse skip modulator PFC control method is presented for a two stage isolated PFC regulator that can achieve nearly unity power factor and fast output regulation. The role of varying the duty cycle is mainly to regulate the output voltage. By changing the skip cycle time, a unity power factor operation can be achieved. Moreover, it provides a low voltage stress, under 400 V, and reduces the switching loss of the PFC stage and interference generated in comparison with what can be achieved in the conventional frequency modulation scheme. An experimental prototype circuit is presented to verify the controller's functions. The prototype meets the harmonic requirements of IEC1000-3-2[6]. The proposed analog translinear circuit in the controller allows customer IC implementation and the proposed circuit is suitable for implementing as a low-cost solution for PFC + PWM combo-chip controller for PFC switching regulators. The drawback of the proposed circuit is that this circuit is not easy to design for universal line input.

CHAPTER 5

CONCLUSION

In order to reduce the size and weight of power supplies, high frequency operation of dc-dc converters has been widely pursued in the power electronic field. However, high-frequency operation can magnify the inherent problems of the conventional PWM converters, such as high switching loss and severe EMI noise.

In this thesis, two configurations of new converters are presented, both can provide high efficiency, and high power factor solution for PWM AC-DC converter. These two power factor correctors are operated in DCM mode. The first converter uses a special synchronization method to provide a ZVS function, while having a reduced component count. By using a synchronization control method in the proposed converter, it can also reduce the bulk capacitor ripple voltage and the switching loss. The drawback of this proposed converter is that the output PFC stage voltage of bulk capacitor is higher than conventional PFC converter. The second converter uses pulse skip control method to reduce the switching loss and provide a PFC function. These two proposed methods can provide higher efficiency, through the ZVS or pulse skip function, and good power factor correction function. The detailed operation of the proposed converter is analyzed. A number of experimental converters have also been implemented to demonstrate the feasibility of the proposed techniques. These two proposed converters use discontinuous current mode operation (DCM) in the power factor correction (PFC) stage. They are more suitable for low to medium power applications (<250 W). As the regulations contained in IEC1000-3-2 [1] have been legally enforced in the European market, low-cost solution for low harmonic and high power factor correction is becoming more and more important.

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