Test Methodologies for Analogue Cores of System-On-Chip

by

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Certificate of Originality

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Abstract

Three built-in self-test (BIST) techniques were developed during this research project. These testing techniques are: Weighed Sum of Selected Node Voltages (WSSNV), Summations of Cores' Test Output Voltages (SOCTOV) and Full Range Window Comparator (FRWC) BIST techniques. The first one is proposed for the effective testing of embedded analogue cores while the later two are proposed for that of the analogue portion of System-On-Chip (SOC). All these BIST techniques have the major advantages of high fault coverage, small hardware overhead and fast test application time.

The WSSNV BIST technique makes use of the weighted sum of a pre-selected small set of circuit node voltages to detect faults. When compared with the voltage scan approach, the WSSNV BIST technique is verified to have higher fault coverage while at the same time hardware overhead is much less. It needs only an extra pin for testing output and a single DC stimulus is needed to feed at the primary input of the circuit (or core) under test (CUT). Studies have been carried out to apply the proposed BIST technique to an analogue active low pass filter; a mixed-signal threshold detector of a telephone ringer IC; and a simulated mathematical functional block of a SOC to verify its effectiveness and efficiency. Test architecture of the WSSNV BIST technique for embedded cores is also proposed.

SOCTOV BIST technique is a unified BIST approach to SOC testing that is based on weighted and non-weighted sums of cores' test output voltages. It is developed in conjunction with the WSSNV BIST technique. Under test mode, all the test output

voltages of the cores are summed together (weighted and non-weighted). By observing these weighted and non-weighted summing outputs and those known nominal values, the faulty condition of the SOC and the location of the faulty core can be uniquely identified. The WSSNV BIST technique provides high fault coverage for individual cores while the SOCTOV BIST technique provides a 100% fault diagnosis resolution for the location of faulty cores.

FRWC BIST technique is based on Window Comparator of Cores' Test Output Voltages for the effective testing of embedded analogue cores. This BIST technique is also developed in conjunction with the WSSNV BIST technique. The resultant testing response is a binary bit stream which can be easily incorporated with the existing testing technique for the digital portion of the SOC such that a single digital Automatic Test Equipment (ATE) is all that required for the testing of a mixed-signal SOC. By reading the bit stream of the testing response, the health status of the SOC, location of the faulty core(s), and even the faults within the faulty core(s) can be identified. In contrast with the SOCTOV BIST technique, it has the major advantage of the capability to locate the unique faults (or equivalent fault sets) within the faulty core(s).

Author's Publications

[1] K.Y. Ko, M.W.T. Wong, and Y.S. Lee, "Built-In Self-Test Technique Based on Weighted Sum of Selected Node Voltages," *Proceedings, 9th International Symposium On Integrated Circuits, Devices & Systems (ISIC-2001)*, pp.186-189, 3-5 September 2001, Singapore.

[2] M.W.T. Wong, K.Y. Ko, and Y.S. Lee, "Study of Test Approach for IP Cores Applicable to SOC Designs," *Proceedings, the 4th International Conference on ASIC (ASICON'01)*, pp.612-615, 22-25 October 2001, Shanghai, China.

[3] M.W.T. Wong, K.Y. Ko, and Y.S. Lee, "Analog and Mixed-signal IP Cores Testing," *Proceedings, the 1st International Workshop on Electronic Design, Test & Applications (DELTA 2002)*, pp.3-7, 29-31 January 2002, Christchurch, New Zealand.

[4] K.Y. Ko, M.W.T. Wong, and Y.S. Lee, "Testing Embedded Cores by Weighted Sum of Selected Node Voltages," *the 19th IEEE Instrumentation and Measurement Technology Conference (IMTC2002)*, pp.595-599, 21-23 May 2002, Anchorage, AK, USA.

[5] K.Y. Ko, M.W.T. Wong, and Y.S. Lee, "Testing System-On-Chip by Summations of Cores' Test Output Voltages," *The Eleventh Asian Test Symposium (ATS'02)*, pp.350-355, 18-20 November 2002, Guam, USA.

[6] K.Y. Ko, M.W.T. Wong, and Y.S. Lee, "Testing Analogue and Mixed-Signal Integrated Circuits By Weighted Sum of Selected Node Voltages," *International Journal of Electronics*. (Accepted, to appear)

[7] K.Y. Ko, M.W.T. Wong, and Y.S. Lee, "Built-In Self-Test Technique for System-On-Chip Based on Summations of Cores' Test Output Voltages," Submitted to *IEEE Transactions on Instrumentation and Measurement*.

[8] K.Y. Ko, M.W.T. Wong, and Y.S. Lee, "Testing analogue cores using full range window comparator," Submitted to *Journal of Circuits, Systems, and Computers*.

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Abbreviations

ATE	Automatic Test Equipment
ATPG	Automatic Test Pattern Generation
BIST	Built-In Self-Test
CUT	Circuit Under Test or Core Under Test
FC	Fault Coverage
FRWC	Full Range Window Comparator
NVSP	Node Voltage Summation Pattern
Op-amp	Operational Amplifier
SOC	System-On-Chip
SOCTOV	Summations of Cores' Test Output Voltages
WC	Weighting Coefficient
WSSNV	Weighted Sum of Selected Node Voltages

Chapter 1

Introduction

As technology advances the size of integrated circuits (ICs) scales up dramatically and even a system can be fabricated on a single chip. The utilization of re-useable Intellectual Property (IP) cores for System-on-Chip (SOC) design can shorten the time-to-market and thus reducing the design cost. These system chips offer higher performance, lower power consumption, smaller volume, lighter weight and even cheaper cost, when compared to their multi-chip counterpart. An example block diagram of a SOC consisting of hierarchical cores and User Defined Logic (UDL) [Zorian 97] is shown in Figure 1.1.

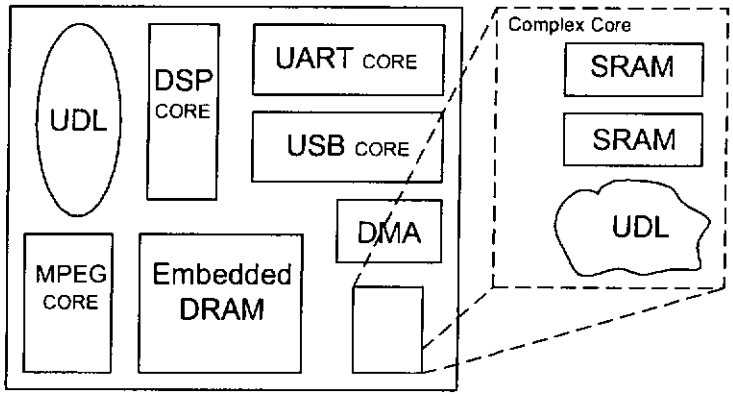

Figure 1.1 System-On-Chip consisting of hierarchical cores and User Defined Logic (UDL)

Three main types of circuitry used in system chips today, namely: logic, memory, analog and mixed-signal. Simple cores consist of one circuitry type only; Hierarchical Cores, also called complex cores, consist of one or more simple cores,

possibly of different circuitry type.

Testing of such IP cores is a challenge issue since the core vendors may not provide any information about the internal logic or circuitry of the cores and especially when these IP cores are deeply embedded in the system chip. The growing trend of mixed-signal cores embedded in a single SOC further makes the testing complicated since testing of both digital and analog parts cannot be accomplished in a single testing approach, either digital or analog.

The initiation of P1500 testing standard [Zorian 97, Zorian 98, Marinissen 99] can facilitate the testing of SOC. To make these deeply embedded cores more controllable and observable, accessible to every I/O pins and even internal nodes of the embedded cores is required. The core test wrapper and Test Access Mechanism (TAM) of the P1500 standard provide such facilities. However, a full size core test wrapper and TAM consume a large chip area and thus a higher cost results. This might not be cost effective in many of the cases. Researchers have proposed different algorithm [Xu 00], design for testability techniques [Ghosh 99, Hamzaoglu 99], test control [Lee 00] and access architectures [Touba 97, Aerts 98, Nourani 99, Iyengar 00], reconfigurable access wrapper [Koranne 02] and reuse of system bus [Hwang 01] either to reduce the hardware overhead of test access mechanism and/or to speed up the test application time in addition to satisfactory fault coverage.

On the other hand, if the testing requirements of embedded cores are considered and be able to reduce to a minimum during the design stage, SOC designers will not need to put much effort into the testing issue of the embedded cores. This aims of

this thesis are to derive Built-In Self-Test techniques (BIST) for the analogue IP cores embedded in a SOC such that the test I/O pins requirements are reduced to minimum, the test circuitry and the test architecture are simple and hence small chip area overhead results in addition to the essential requirements of high fault coverage and fast test application time. The achievements reported in this thesis are summarized as follows:

1.1 Built-in self-test technique for embedded analogue cores based on weighted sum of selected node voltages

The BIST technique based on weighted sum of selected node voltages (WSSNV) [Ko 01] is proposed for the effective testing of these embedded cores. This technique makes use of the weighted sum of a pre-selected small set of circuit node voltages in response to a DC stimulus applied at the primary input to detect faults. When compared with the voltage scan approach, the WSSNV BIST technique is verified to have higher fault coverage while at the same time hardware overhead is much less. It needs only an extra pin for testing output and a single DC stimulus is needed to feed at the primary input of the circuit/core under test (CUT). Hence, the size and design of the test architecture for SOC can be reduced and simplified respectively. Studies have been carried out to apply the proposed BIST technique to an analogue active low pass filter; a mixed-signal threshold detector of a telephone ringer IC; and a simulated mathematical functional block of a SOC to verify its effectiveness and efficiency. Test architecture of the WSSNV BIST technique for embedded cores is also proposed [Wong 01, Ko 02a, Wong 02]. The WSSNV BIST technique for embedded cores also forms an essential part of the succeeding

proposed BIST techniques based on summations of cores' test output voltages (SOCTOV) and by full range window comparator (FRWC) of cores' test output voltages. Details of the WSSNV BIST technique will be given in Chapters 3 and 4, and its demonstration will be given in Chapter 5.

1.2 Built-in self-test technique for analogue portion of system-on-chip based on summations of cores' test output voltages

A unified approach to SOC testing that uses a BIST technique based on weighted and non-weighted sums of cores' test output voltages is proposed. It is referred as the Summations of Cores' Test Output Voltages (SOCTOV) BIST technique [Ko 02b]. It is developed in conjunction with the WSSNV BIST technique mentioned in section 1.1. Under test mode, all the test output voltages of the analogue cores are summed together (weighted and non-weighted). By observing these weighted and non-weighted summing outputs and those known nominal values, the faulty condition of the analogue portion of a SOC and the location of the faulty core can be uniquely identified. The WSSNV BIST technique provides high fault coverage for individual cores while the SOCTOV BIST technique provides a 100% fault diagnosis resolution for the location of faulty cores. The details of the SOCTOV BIST technique will be given in Chapter 6.

1.3 Built-in self-test technique for analogue portion of system-on-chip by using full range window comparator

Another BIST technique based on Window Comparator of Cores' Test Output Voltages for the effective testing of embedded analogue cores of a SOC is proposed,

which is referred as Full Rang Window Comparator (FRWC) BIST technique. It is also developed in conjunction with the WSSNV BIST technique. The proposed window comparator has full adjustable ranges between VSS and VDD. The resultant testing response is a binary bit stream which can be easily incorporated with the existing testing technique for the digital portion of the SOC such that a single digital Automatic Test Equipment (ATE) is all that required for the testing of mixed-signal SOC. By reading the bit stream of the testing response, the health status of the SOC, location of the faulty core(s), and even the fault (or equivalent fault set) within the faulty core(s) can be identified. Besides, only one extra testing output pin is needed in addition to the two pins of reference voltages.

However, the effectiveness and performance of the FRWC BIST technique can be affected by the variations of CMOS process, the op-amp input offset, and the accuracy of the reference voltages used. Future works are proposed based on existing available techniques and/or to develop novel approaches to eliminate/minimize all these adverse factors. Besides, a FRWC chip is also proposed to be fabricated in order to evaluate the effectiveness and performance of the FRWC BIST technique in a practical manner. The details of the FRWC BIST technique and the proposed future works will be given in Chapters 7 and 8 respectively.

Chapter 2

A Review of Previous Works

The initiation of IEEE P1500 Standard for Embedded Core Test (SECT) eases the test interoperability between the core provider and core user by standardizing the test-related elements [Marinissen 99]. The P1500 Standard is not intended to standardize the internal test method(s) for individual cores and not intended to adopt a common SOC level test integration and optimization solution, but to standardize the interface between the core and the SOC by creating a common core test control and peripheral access mechanism to make core test plug-and-play possible [Zorian 97].

Direct physical access to cores is not available by default since the cores are often deeply embedded in a system chip. Electronic access mechanism, wrapper and TAM are needed. Wrapper is the logic circuit around the core and TAM is used to connect the core peripheries to the test sources and sinks. The wrapper performs switching between normal and test modes and for core isolation such that the CUT is free from external interference which come from neighbouring cores or user-defined logic (UDL). The test pattern source generates the test stimuli for the embedded core, and the test pattern sink compares the response(s) to the expected response(s). [Zorian 99].

Researchers have proposed different algorithms and techniques to reduce the chip area overhead of core test wrapper and TAM; and/or to speed up the test application

time. Some of them are reviewed and according to their nature of proposals, the following categories are identified:

2.1 Reducing chip area overhead by modification of hardware

The test methodology, Reuse of Addressable System Bus for SOC Testing (RASBuS), proposed in [Hwang 01] is based on the reuse of the existing system bus and/ or peripheral bus as the TAM to access the ports of deeply embedded cores, and use the embedded microprocessor as the test source and sink. Additional logic is only needed for the address decoding and the core I/O registers. The reuse of existing system and/ or peripheral buses eliminates the area overhead for TAM. When compared the RASBuS with the boundary scan method, the former introduces only 56% – 66% area overhead for those of the cores.

The test technique for core-based system proposed in [Ghosh 99] involves the modifications of original circuits to achieve low area overhead. It consists of two phases. In the first phase, each core is made testable and transparent. If a core is not highly testable, a small amount of hardware like test multiplexers may be needed to make it highly testable. The transparent property implies the propagation of test data through the core without information loss. In the second phase, the core-based system consisting of an interconnection of testable and transparent cores is made testable with some global test hardware, and the test schedule is derived for testing each embedded core with its precomputed test set. The fault coverage obtained is > 99.6% and the area overhead is only 6.3% with negligible penalty of testing delay.

A hierarchical test control architecture for SOC is proposed in [Lee 00]. The proposed architecture is compatible with the P1500 standard. It can handle both IEEE P1500 and IEEE 1149.1 cores. It provides hierarchical test capability. For a SOC chip whose DFT circuitry is integrated with this proposed architecture can be plug-and-play into a larger SOC as a hierarchical core. It supports both serial and parallel TAM and it needs only 10 test pins for the serial TAM irrespective of the complexity of the SOC.

2.2 Speeding up test application time by modification of hardware

The size of the test vector set defines the test application time and the required pin memory size of the test equipment. In [Aerts 98], the design of scan chains as transport mechanism to bring test stimuli from IC input pins to embedded cores and propagate test responses to IC output pins is introduced. Three different scan chain architectures: multiplexing architecture, daisychain architecture and distribution architecture for core-based ICs are introduced. These architectures aim at a minimum test vector set size. The multiplexing architecture assigns the full scan bandwidth to every core and multiplexes the scan chains per core onto the IC pins. Because of the pin sharing, the cores can only be tested sequentially, and the total test time is the sum of the individual test times. In the daisychain architecture, a bundle of scan chains as wide as can be accommodated at the IC pins is routed through all cores. The daisychain can be used to simultaneously scan test patterns in and out all cores. Multiplexers in the daisychain allow cores which run out of test patterns before other cores to be bypassed. The distribution architecture divides the

available scan chains over the cores, based on the amount of test data that has to be transported to each individual core. The architecture allows to test all cores in parallel and hence the total time is determined by the maximum test time of the individual cores. A trade-off between the number of scan chains and the number of scan control pins may be rewarding with respect to test time. In practice combinations of the architectures can be used to design the scan chains.

Another test methodology for testing a core-based system is proposed in [Nourani 99]. A "bypass" mode circuitry is added to each core such that the data can be transferred from a core input port to the output port without interfering the core circuitry itself. The interconnections are thoroughly tested because they are used to propagate test data in the system. The system is modeled as a directed weighted graph in which the accessibility (of the core input and output ports) is solved as a shortest path problem. The test data distribution and collection of signatures are scrambled in a pipelined fashion to minimize test time. Higher fault coverage and shorter test time are achieved from experimental results.

A full size wrapper is expensive but necessary to enhance the controllability and observability of the embedded core. One of the approaches to remove part of these wrappers is using controllability and observability evaluation via random inputs at the high level (i.e. no gate-level information needed). To achieve better results than the random input vectors, genetic algorithm is used in [Xu 00] to justify the test patterns provided by the core vendor. Genetic algorithm is an adaptive method which can be used to solve search and optimization problems. Experiments were conducted for two synthesized benchmark circuits. With the test patterns generated

by the genetic algorithm, both the wrapper size and the test application time are further reduced, while the fault coverages of the cores remain the same for most cases.

Another design for testability technique, Parallel Serial Full Scan (PSFS) is proposed in [Hamzaoglu 99] for reducing the test application time for full scan embedded cores without using any additional test access pins other than the ones used for the full scan technique. Test application time reduction is achieved by dividing the scan chain into multiple partitions and shifting in the same vector to each scan chain through a single scan input. The experimental results for a sequential benchmark circuit showed that PSFS technique significantly reduces both the test application time and the amount of test data for full scan embedded cores.

2.3 Reducing chip area overhead and speeding up test application time by modification of hardware

A reconfigurable wrapper design is proposed in [Koranne 02]. Test wrapppers around cores are usually designed assuming static width of test rail or test access bits. Since a core can have a variety of tests, assigning a core a wider than required TAM can increase the test time while some other cores might needed a wider TAM. If the wrapper can be adjusted dynamically to fulfil the bitwidth requirements of the various tests of cores, optimum test time and little area overhead can be achieved. The proposed method here is to use multiplexers at the head of each reconfigurable scan chain. The set of reconfigurable scan chains can be calculated using graph theoretic methods.

TAM and cores test wrapper are integral parts of a SOC test architecture. Researches usually focus on only one aspect of the TAM/wrapper design issue at a time, either optimizing the TAM for a set of predesigned wrappers for the cores or optimizing the wrapper for a given TAM width. In [Iyengar 00], a more general problem is addressed, in which the TAM design and wrapper optimization are carried out in conjunction. An efficient technique is introduced to construct test wrapper that reduce scan-in time for cores, and which requires minimum TAM width. New models for TAM optimization based on the precomputation of core testing times is also presented. Base on experimental results for an example SOC, testing time and TAM width are significantly reduced.

When a core is deeply embedded in a SOC, the set of test vectors provided by the core vendor can be applied to the core via a full isolation ring placed around the core. The isolation ring is essentially a boundary scan that provides full controllability of the inputs of the core and full observability of the outputs of the core as well as providing full observability of the logic driving the core and full controllability of the logic that is driven by the core. However, the area and performance overhead for this may not be acceptable in many applications. A systematic method for designing a partial isolation ring that provides the same fault coverage as a full isolation ring is proposed in [Touba 97]. ATPG techniques are used for efficiently checking whether a particular partial isolation ring will degrade fault coverage. Exact and heuristic search strategies are used for selecting a partial isolation ring for both the inputs and outputs of the core. Experimental results show that significant area and performance overhead reduction is achieved by using a partial isolation ring compared with a full isolation ring.

The above proposals can be adopted for the testing of SOC either to reduce the chip area overhead of test access mechanism, speed up the test application time, or both. But none of them is a universal approach and can only be applied to some or a particular case. On the other hand, if the testing requirements of embedded cores are considered and reduced to a minimum during the core design, SOC designers will not need to put much effort into the testing issue of the embedded cores. The minimum number of testing I/O pins is two, one for test input while the other for test output response. Applying a DC voltage at the primary input and observing the voltage at the primary output of a CUT is a simple testing technique. In general, its fault coverage is not satisfactory. If all the internal circuit nodes can be observed instead of only the primary output node, the fault coverage will be significantly improved to a satisfactory level. However, it is not economical and practical to bring all the internal nodes externally, very large area overhead will be incurred. Alternatively, Techniques like voltage scan [Wey 90, Wurtz 93, Shieh 98] can be adopted to achieve this purpose.

2.4 Voltage scan techniques

An analogue BIST (ABIST) structure was proposed in [Wey 90] to allow access to some internal nodes so that the fault diagnosis process can be simplified significantly while still keeping low pin overhead. Under the ABIST structure, each test point is equipped with a test point buffer, a pass switch, an analog pass buffer and a sample and hold (S/H) circuit. The ABIST structure operates in two modes: the normal operation mode and the test mode. In the normal mode, the ABIST structure is isolated from the circuit under test. During test mode, all the test data at

the various test points are simultaneously loaded to the corresponding S/H circuit. Then by the operation of pass switches, the test data held on S/H circuit are shifted out to the scan output serially in the last stage first out manner.

A BIST structure for mixed-mode circuits is presented in [Wurtz 93] applicable to both analogue and digital circuits. When compared with Wey's proposal, the new mixed-mode BIST structure does not require the S/H circuit and uses the transmission gates instead of pass switches. Hence the new structure requires less hardware to implement and does not suffer from the error introduced by nonideal buffer and S/H capacitor charge loss. But it does not allow simultaneously sampling of test points.

Another control and observation structures for analogue circuits are proposed in [Shieh 98]. The two structures are referred as COS1 and COS2. COS1 is a modified version of Wurtz's proposal. Each stage has two switches, one observation point and one control point. A random logic is employed for each stage to generate the control signals for respective switches. All random logic blocks receive the same broadcast signal. Designation signals will be sent to their respective stages. Depends on the combinations of status of the broadcast and designation signals and the positions of switches controlled by the random logic, the circuit under test will be put in either normal, sample and control operations. COS1 allows sampling or control of one test point at a time. COS2 reliefs this problem with the additional of one more broadcast signal, three more switches and one capacitor for analogue memory for each stage. Similarly, depends on the combinations of status of the two broadcast and one designation signals and the positions of switches controlled by the random logic, the

CUT will be put in one of the five states: normal, sample, scan out, scan in and control operations. All test points can be sampled at the same time and reading out their voltage levels one by one. All test points can also be controlled simultaneously. The dc voltage of each test point is scanned in one by one by scan-in instruction, then apply the control instruction to control all stages simultaneously.

Although these techniques provide a high observability and controllability of internal circuit nodes, though their hardware overheads are not the same, in general, a considerable hardware overhead, including the shift registers; timing and synchronization circuits are still incurred. Practically, not all of the circuit nodes are necessary to achieve the maximum fault coverage. Hence, a BIST technique based on weighted sum of selected node voltages (WSSNV) is proposed in this thesis for the effective testing of analogue and mixed-signal cores. Moreover, two succeeding BIST techniques for the effective testing of analogue cores of SOC are developed in conjunction with the WSSNV BIST technique, one is based on the Summations of Cores' Test Output Voltages (SOCTOV) while the other is based on a Full Range Window Comparator (FRWC) of cores' test output. There is the possibility of jointly application of these proposed BIST techniques with the above introduced proposals (in Sections 2.1-2.3) to achieve even less chip area overhead and faster test application time.

Chapter 3

Built-In Self-Test Technique Based on Weighted Sum of Selected Node Voltages

3.1 Introduction

Applying a DC voltage at the primary input and observing the voltage at the primary output of a CUT is a simple testing technique. Although no modification of the CUT is needed and no hardware overhead is incurred, in general, its fault coverage and fault diagnosis resolution is not satisfactory. For a faulty circuit different faults may cause different patterns of circuit node voltages due to the sensitivity of different node voltages with respect to different faults. To make use of the node voltages to detect and/or isolate faults, access to the internal circuit nodes is required. Techniques like voltage scan [Wey 90, Wurtz 93, Shieh 98] can be adopted to achieve this purpose. Although these techniques provide a high controllability and observability of internal circuit nodes, a considerable hardware overhead, including the shift registers, timing and synchronization circuits are incurred.

Practically, not all but a pre-selected small set of the circuit nodes' voltages is needed to be observed to achieve the highest fault coverage. This pre-selected small set of circuit nodes is referred as the optimum set of nodes, which is the least number of circuit nodes needed to be observed to achieve the highest fault coverage equal to that obtained by observing all the circuit nodes.

However, it is still necessary for the traditional scan techniques to observe this optimum set of internal node voltages externally and considerable area overhead results. Experimental data obtained suggests that the summation of this optimum set of circuit node voltages could be used to detect faults by comparing the deviation of the summed voltages between fault-free and faulty conditions. Based on fault simulation results, its fault coverage is comparable to voltage scan techniques while the hardware overhead is much less since it only needs an extra testing output pin and only a single DC stimulus is needed to feed at the primary input of the CUT.

Moreover, by adding appropriate weighting coefficients to each of the optimum set of node voltages before they are summed up, also based on simulation results the fault coverage achieved is higher than that obtained by observing all the circuit node voltages. In fact, the fault coverage can be further pushed to 100% of maximum achievable fault coverage. The reason is that by applying appropriate weighting coefficients to each of the nodes in the optimum set will change the sensitivity of some nodes with respect to some faults and has the possibility to make it much easier to differentiate the faulty and fault-free conditions. This is the underlying principle of the proposed BIST technique based on Weighted Sum of Selected Node Voltages (WSSNV). The working principle of the proposed BIST technique is illustrated in the following section.

3.2 Working principle of the WSSNV BIST technique

Under the assumption that only single catastrophic faults (open and short circuits) are considered and for notational convenience, we define the following notations to be used hereafter.

N - a set of circuit nodes, where $N=\{1,2,...,i,...,n\}$,

X - a set of faults, where $X=\{1,2,...,f,...,x\}$;

V_i - fault-free node voltage;

V_{if} - node voltage under fault f condition.

Consider a core under test, which has an optimum set of n nodes. For a particular fault f, assume the following conditions exist:

$(V_{1f}-V_1) >$ tolerance band of V_1 (say, $\pm$ 5% of V_1)

$(V_{2f}-V_2) <$ tolerance band of V_2 (say, $\pm$ 5% of V_2)

$(V_{3f}-V_3) >$ tolerance band of V_3 (say, $\pm$ 5% of V_3)

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$(V_{(n-1)f}-V_{n-1}) <$ tolerance band of V_{n-1} (say, $\pm$ 5% of V_{n-1})

$(V_{nf}-V_n) >$ tolerance band of V_n (say, $\pm$ 5% of V_n)

The sum of the fault-free voltages,

$$V_{sum} = (V_1 + V_2 + V_3 + \cdots + V_{n-1} + V_n) \tag{3.1}$$

The sum of the voltages under faulty condition,

$$V_{sumf} = (V_{1f} + V_{2f} + V_{3f} + \cdots + V_{(n-1)f} + V_{nf}) \tag{3.2}$$

Let the deviation of voltage between faulty and fault-free conditions,

$$\Delta V = V_{sumf} - V_{sum} \tag{3.3}$$

Based on simulation results, in most cases, ΔV will be beyond the tolerance band of V_{sum} and detectability of fault f is maintained. However in some cases, due to the

polarity of node voltages that can be either positive or negative, the summing process will reduce the deviation of the voltages between faulty and the fault-free conditions, thus making the corresponding fault undetectable. Hence, for a particular fault *f*, the maximum deviation of summed selected node voltages between faulty and fault-free conditions may be obtained by

$$\begin{aligned}\Delta V_{max} &= V_{sumf} - V_{sum} \\ &= (V_{1f} - V_{2f} + V_{3f} + \cdots - V_{(n-1)f} + V_{nf}) \\ &\quad - (V_1 - V_2 + V_3 + \cdots - V_{n-1} + V_n) \\ &= (1 \cdot V_{1f} - 1 \cdot V_{2f} + 1 \cdot V_{3f} + \cdots - 1 \cdot V_{(n-1)f} + 1 \cdot V_{nf}) \\ &\quad - (1 \cdot V_1 - 1 \cdot V_2 + 1 \cdot V_3 + \cdots - 1 \cdot V_{n-1} + 1 \cdot V_n)\end{aligned} \tag{3.4}$$

The set of coefficients (1, -1, 1) with respect to nodes 1, 2, 3, · · · n-1, n are referred as the node voltage summation pattern (NVSP), both fault-free and faulty summed node voltages follow the same summation pattern. However, due to the sensitivity of different node voltages with respect to different faults is not the same. The weighting of each node of the optimum set of nodes corresponding to a particular fault will be different. For the proposed WSSNV BIST technique,

$$\begin{aligned}\Delta KV_{max} &= KV_{sumf} - KV_{sum} \\ &= (k_1 V_{1f} + k_2 V_{2f} + k_3 V_{3f} + \cdots + k_{(n-1)} V_{(n-1)f} + k_n V_{nf}) \\ &\quad - (k_1 V_1 + k_2 V_2 + k_3 V_3 + \cdots + k_{(n-1)} V_{(n-1)} + k_n V_n)\end{aligned} \tag{3.5}$$

In general,

$$\Delta KV_{max} = \sum_{i=1}^{n} k_i V_{if} - \sum_{i=1}^{n} k_i V_i \tag{3.6}$$

Where - k_i represents the weighting coefficient (WC), which can be any values between and inclusive of −1 and +1, apply to node i. The whole set of WCs forms the node voltage summation pattern (NVSP) in corresponding to the optimum set of nodes.

- V_i represents fault-free voltage at node i;
- V_{if} represents node i voltage under fault f condition.

If the deviation of the summed optimum set of node voltages between faulty and fault-free conditions beyond the tolerance band, the particular fault f is said to be detectable. The values of WCs are determined during the summing process such that the maximum achievable fault coverage is achieved. Moreover, the summing process may further reduce the number of nodes in the optimum set. The detail of summing process will be described in Chapter 4.

3.3 Implementation of the WSSNV BIST technique

The block diagram of the WSSNV BIST architecture for an embedded core is shown in Figure 3.1. The weighted summer circuit is implemented based on the finalized optimum set of nodes and the appropriate node voltage summation pattern of maximum achievable fault coverage. The optimum set of node voltages is summed up with appropriate weighting coefficients. The summer output forms the test output. Under test mode, the primary input of the original core becomes the test input where DC test stimulus is applied. The final circuit of the embedded core with

the WSSNV BIST technique is then implemented with the weighted summer built in.

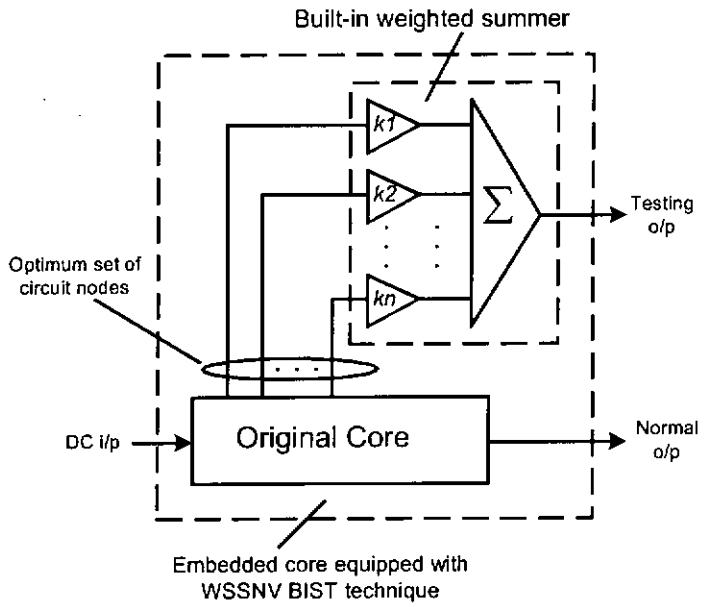

Figure 3.1 Block diagram of the WSSNV BIST architecture

3.4 Summary

The proposed WSSNV BIST technique has the advantages of high fault coverage, small hardware overhead, simple circuit structure and testing architecture. Test application procedure is simple and time is fast since DC test stimulus and test response are applied and observed simultaneously. The verification of the effectiveness and performance of the WSSNV BIST technique will be illustrated in Chapter 5 through its applications to an analogue circuit, a mixed-signal circuit and two example cores of a simulated mathematical functional block.

Chapter 4

Algorithm of the Weighted Sum of Selected Node Voltages BIST Technique

4.1 Introduction

The WSSNV BIST technique comprises five different phases and each phase has its specific function to perform. The process flow chart of the proposed BIST technique is shown in Figure 4.1.

Identification of node voltages with respect to fault-free and faulty conditions is performed in phase 1 by fault simulations. The data obtained is used to generate the fault dictionary. In phase 2, the optimum set of nodes is derived from the fault dictionary. Summing process is performed in phase 3 to determine the node voltages summation pattern(s) (NVSPs) of maximum achievable fault coverage. Based on the final set(s) of NVSP(s), the number of nodes in the optimum set is finalized in phase 4. The circuit implementation is performed in phase 5 based on the finalized optimum set of nodes and the appropriate NVSP(s) of maximum achievable fault coverage. Detailed description of the individual phases is given below.

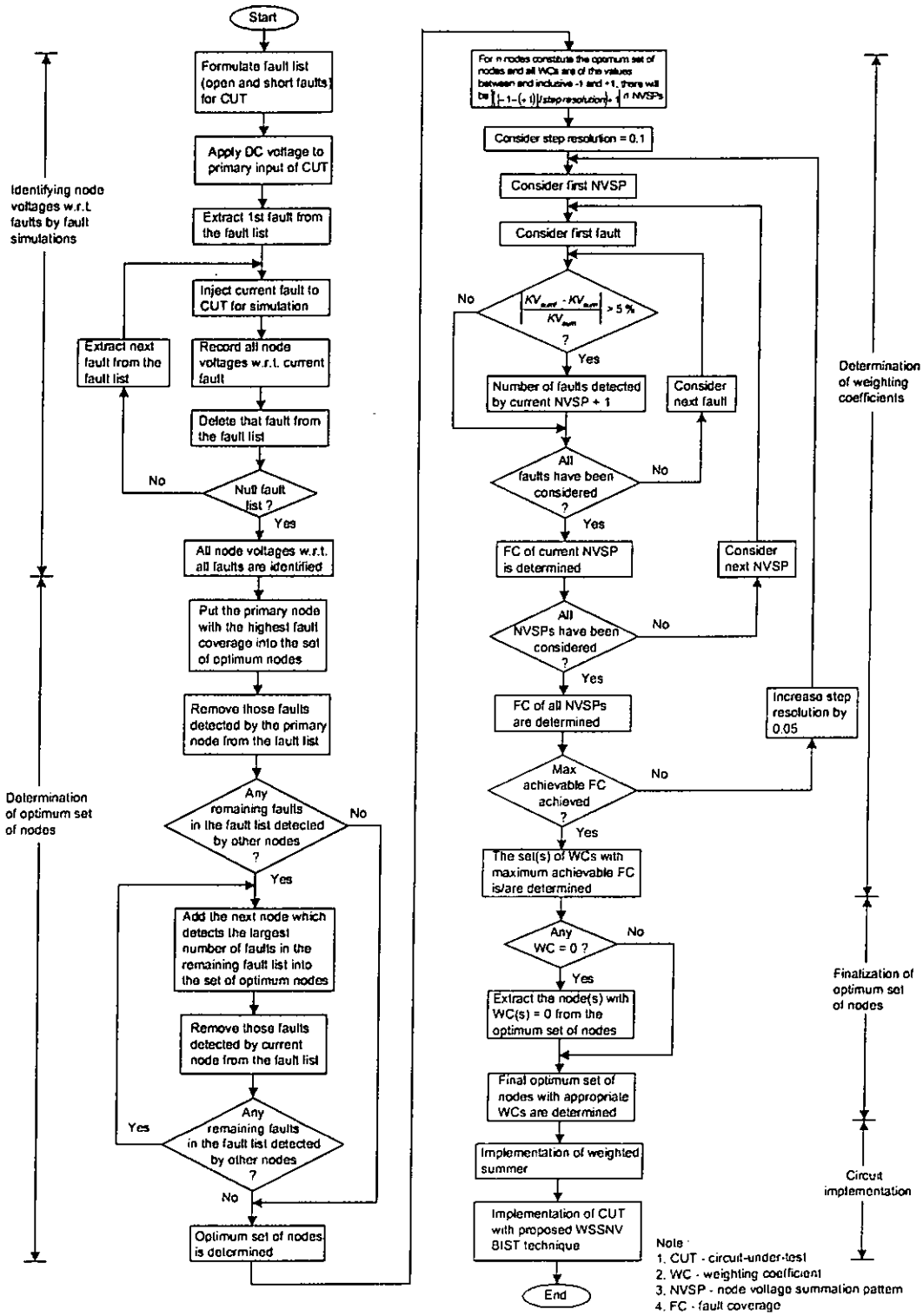

Figure 4.1 Process flow chart of the WSSNV BIST technique

4.2 Phase 1 : Identifying node voltages with respect to faults by fault simulations

The following tasks including:

- formation of fault list,
- modeling the faults,
- choice of CMOS process parameters,
- definition of tolerance band, and
- fault simulation are performed in this phase to generate the fault dictionary.

4.2.1 Formation of fault list

In order to evaluate the effectiveness of the WSSNV BIST technique, an accurate fault list for CUT is required. For analog circuits, faults can be either Catastrophic (hard) or Parametric (soft) [Milor 89, Arabi 97]. Parametric faults, consists of small deviation of process parameters (e.g. oxide thickness and lateral junction depth), caused by statistical fluctuations in the manufacturing process. Catastrophic faults are random defects and cause various components failure. They may be initiated by dust particle on photolithographic mask and then cause structural deformations like open or short circuits.

Research results claim that 80-90% of observed analogue faults are catastrophic faults which consist of shorts or opens in diodes, transistors, resistors, and capacitors [Arabi 97]. Moreover, the yield losses in CMOS process are primarily due to catastrophic faults [Milor 89]. It was also known that when 100% of catastrophic faults were

detected by a test method, the majority of parametric faults, depending on the deviation value of the parametric faults, could also be identified [Arabi 97].

Hence, all possible catastrophic faults of the CUT are being considered. Faults are injected one at a time, multiple faults are not considered. The open circuit faults of the inverting and non-inverting inputs of operational amplifiers (op-amps) are equivalent to the gate terminal open faults of MOSFETs, and because of the rare occurrence of such device failure [Milor 89] and the restriction of SPICE program, gate open faults will not be considered in the simulations. The occurrence probability of faults of a MOS transistor in CMOS process [Milor 89, Arabi 97] is shown in Table 4.1.

Class	Device failures	Interconnect failures
Most likely	Gate-drain short Gate-source short	Short between diffusion lines
Less likely	Drain contact open Source contact open	Aluminum polysilicon cross-over broken
Least likely	Gate-substrate short Gate contact open	Short between Aluminum lines

Table 4.1 Occurrence probability of CMOS faults

4.2.2 Fault modeling

Although there are different fault models proposed in literature [Milor 89, Meixner 91, Bell 95, Soma 96, Arabi 97], there is no single or universally applicable fault model for analogue circuits [Bell 95]. In this study, we choose a relatively simple

and commonly used model using appropriate values of resistance to represent the open and short circuits of devices and connections [Milor 89, Bell 95, Arabi 97]. This is thought to be more realistic than complete open and direct short circuits and it is necessary to enable simulation in some cases. Open fault is modeled as a 10 MEG ohms resistor while short fault is modeled as a 10 ohms resistor [Arabi 97]. Taking the MOSFET as an example, the implementation of fault models is shown in Figure 4.2.

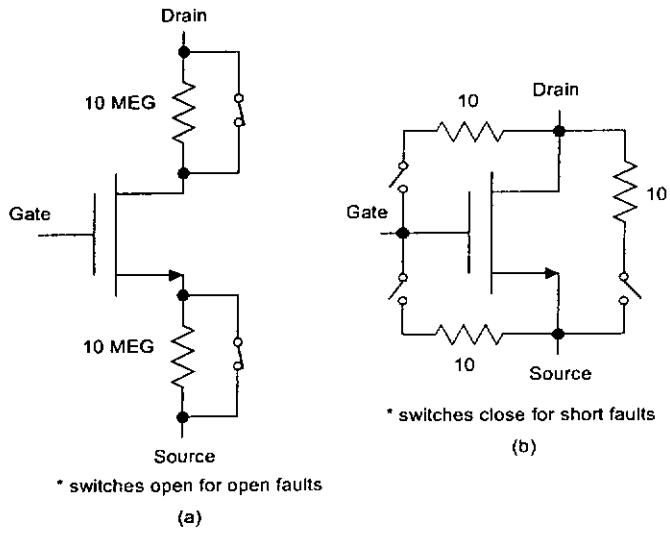

Figure 4.2 Implementation of fault models (a) open faults (b) short faults

4.2.3 Choice of CMOS process parameters and definition of tolerance band

A set of 2 μm CMOS process parameters taken from [Jacob 98] is used for simulation. Due to fluctuation of the CMOS process parameters and taking

parametric faults into our consideration, a tolerance band of ± 5% is assumed. The set of 2 μm CMOS process parameters is shown below:

```
.MODEL CMOSN NMOS(LEVEL=2 PHI=0.600000 TOX=4.3500E-08
+ XJ=0.200000U TPG=1 VTO=0.8756 DELTA=8.565E+00 LD=2.3950E-07
+ KP=4.5494E-05 UO=573.1 UEXP=1.5920E-01 UCRIT=5.9160E+04
+ RSH=1.0310E+01 GAMMA=0.4179 NSUB=3.3160E+15 NFS=8.1800E+12
+ VMAX=6.0280E+04 LAMBDA=2.9330E-02 CGDO=2.8518E-10
+ CGSO=2.8518E-10 CGBO=4.0921E-10 CJ=1.0375E-04 MJ=0.6604
+ CJSW=2.1694E-10 MJSW=0.178543 PB=0.800000)
*
.MODEL CMOSP PMOS(LEVEL=2 PHI=0.600000 TOX=4.3500E-08
+ XJ=0.200000U TPG=-1 VTO=-0.8889 DELTA=4.8720E+00 LD=2.923E-07
+ KP=1.5035E-05 UO=189.4 UEXP=2.7910E-01 UCRIT=9.5670E+04
+ RSH=1.8180E+01 GAMMA=0.7327 NSUB=1.0190E+16 NFS=6.1500E+12
+ VMAX=9.9990E+05 LAMBDA=4.2290E-02 CGDO=3.4805E-10
+ CGSO=3.4805E-10 CGBO=4.0305E-10 CJ=3.2456E-04 MJ=0.6044
+ CJSW=2.5430E-10 MJSW=0.244194 PB=0.800000)
```

4.2.4 Fault simulation and formation of the fault dictionary

Fault simulation is performed by using SPICE. The fault dictionary is generated by the following procedure:

- A DC voltage is applied to the primary input of the CUT.
- All the node voltages are recoded under fault-free condition.
- Each single fault is injected one at a time to the CUT for simulation.
- Record all node voltages of the CUT with respect to each of the individual faults.
- The recoded data forms the fault dictionary.

4.3 Phase 2 : Determination of optimum set of nodes

The fault dictionary just created will be used to generate the detectable fault list. Then the optimum set of nodes can be deduced from the detectable fault list.

4.3.1 Formation of detectable fault list

With reference to the fault dictionary, all the recorded node voltages with respect to a fault are compared with their nominal values. If one or more of the node voltages deviated from their nominal values and beyond the tolerance band, this fault is considered as a detectable fault. This process repeats for the rest of the faults. A detectable fault list with respect to the circuit nodes is then formulated. As an example, a simulated detectable fault list is shown below:

Fault	Node					
	1	2	3	4	5	6
f1			√		√	
f2				√		√
f3		√	√		√	
f4	√					
f5			√	√	√	√
f6		√		√	√	√
f7				√	√	√

Table 4.2 An example detectable fault list

Where √ denotes the node that a particular fault can be detected. For example, fault *f1* can be detected by nodes 3 and 5.

4.3.2 Determination of optimum set of nodes

Once the detectable fault list is generated, the optimum set of circuit nodes can also be determined. With reference to the detectable fault list, the primary node with the highest fault coverage among all the nodes is selected. The highest fault coverage here is referred as the largest number of faults, except those electrically but not physically redundant faults, faults cause no output deviation from normal response, and faults cause output deviation from normal response but within the tolerance band, can be detected. The next node to be chosen should cover the largest number of faults that cannot be detected by observing the primary node. This process repeats until the highest fault coverage is obtained. If more than one node possess the identical fault coverage, only one of them will be selected.

With reference to the example detectable fault list Table 4.2, the primary node is node 5 which has the highest fault coverage. The next node should be chosen is node 4 or node 6. Node 1 is the last node to be selected. Since node 4 and node 6 possess the identical fault coverage, hence the optimum set should consists of nodes (1, 4, 5) or (1, 5, 6).

4.4 Phase 3 : Determination of weighting coefficients for optimum set of node voltages

Weighting coefficients for the optimum set of nodes is determined in such a way that the maximum achievable fault coverage is obtained. Maximum achievable fault coverage here is referred as all the faults except those electrically but not physically redundant faults and faults cause no output deviation from normal response, can be detected.

4.4.1 Node voltages summation pattern

For an optimum set consists of n nodes, there will be n corresponding weighting coefficients (WCs) of any values between and inclusive of –1 and +1, and the possible number of node voltages summation patterns (NVSPs) is determined by the equation:

$$[(|\text{-1-(+1)}|/\textit{ step resolution}) + 1]^n \qquad (4.1)$$

For example, if an optimum set consists of 3 nodes, step resolution is 0.1, there will be 9,261 sets of NVSPs. The smaller the step resolution, the more the NVSPs and the more iterations have to be performed in the summing process. However, if maximum achievable fault coverage cannot be obtained under step resolution of, say 0.1, summing process has to be repeated with smaller step resolution, say 0.05.

4.4.2 Summing process

Summing process is performed to sum up all the optimum set of node voltages, each of them with an appropriate WC, with respect to the fault-free condition and each of the individual faults. All possible combinations of all values, in between and inclusive of –1 and +1, of the WCs are considered. For the ease of computation, all WCs are initially incremented in steps resolution of 0.1. All possible sets of the NVSPs are applied to the optimum set of node voltages with respect to each of the individual faults one by one during the summing process. Mathematical software may be used to facilitate the summing process. Table 4.3 shows some of the 9,261 sets of NVSPs for an optimum set of 3 nodes under step resolution of 0.1.

NVSP Set	Node No.		
	1	2	3
1	-1.0	-1.0	-1.0
2	-1.0	-1.0	-0.9
3	-1.0	-1.0	-0.8
4	-1.0	-1.0	-0.7
. . .	. . .	. . .	. . .
4631	0	0	0
. . .	. . .	. . .	. . .
9259	0.8	1.0	1.0
9260	0.9	1.0	1.0
9261	1.0	1.0	1.0

Table 4.3 Part of the 9261 sets of NVSPs

For a particular set of NVSP, all the weighted sums of optimum set of node voltages under faulty conditions (consider all catastrophic faults) are compared with the fault-free value one by one. If any of these summed voltages deviate from the fault-free value and beyond the tolerance band, the corresponding fault is said to be detectable. The fault coverage of this particular set of NVSP is then derived. As an example, Table 4.4 shows the fault coverage of 6 sets of NVSPs with respect to 10 faults.

Fault	NVSP Set					
	1	2	3	4	5	6
f1		√		√		
f2	√	√	√	√	√	
f3			√	√	√	√
f4		√		√		
f5	√	√		√	√	
f6		√		√	√	
f7	√		√	√		
f8		√		√		
f9		√		√	√	
f10	√			√		√
F.C. (%)	40	70	30	100	50	20

Table 4.4 Fault coverage of different NVSPs

Where,

F.C. – denotes fault coverage

√ - denotes the corresponding fault detected by the particular NVSP

Among all sets of NVSPs, the one or probably more than one set with the maximum achievable fault coverage can be identified. Maximum achievable fault coverage here is referred as all the faults except those electrically but not physically redundant faults and faults cause no output deviation from normal response, can be detected. Those undetectable faults that cause output deviate from normal response but within the tolerance band can now be detected by applying the appropriate NVSP to the optimum set of node voltages. If maximum achievable fault coverage cannot be achieved with step resolution of 0.1, summing process can be repeated by increasing the step resolution, say 0.05.

4.5 Phase 4 : Finalization of the optimum set of nodes

If there is any WC(s), in the final set(s) of NVSP(s) equal to zero which imply that the corresponding node(s) can be eliminated from the final optimum set of nodes.

For example, if the original optimum set consists of five nodes (1, 4, 10, 20, 33) and one of the NVSPs which can be used to obtain maximum achievable fault coverage is (0.1, 0, 0.4, 0, 1), then the final optimum set of nodes can be only consisted of three nodes (1, 10, 33).

4.6 Phase 5 : Circuit implementation with the WSSNV BIST technique

The built-in summer circuit is implemented based on the finalized optimum set of nodes and the appropriate NVSP of maximum achievable fault coverage. The final circuit with the proposed WSSNV BIST technique is then implemented with the weighted summer built in.

The summer can be built with op-amp. Examples of weighted summer circuit will be given in Chapter 5.

4.7 Computational complexity analysis of the proposed BIST technique

Refer to the five phases of the proposed WSSNV BIST algorithm; computational cost mainly depends on the stages of fault simulations and especially the determination of weighting coefficients while not much computational effort will be incurred in the determination of optimum set of nodes, finalization of optimum set of nodes and implementation of weighted summer. The computational cost can be approximated in terms of the number of iterations.

4.7.1 Computational effort for the fault simulations

For a CUT with x circuit nodes and y branches, if all possible catastrophic faults are considered the total numbers of

$$\text{Short circuit faults} = {}^{x}C_2 \tag{4.2}$$

$$\text{Open circuit faults} = y \tag{4.3}$$

All the node voltages with respect to the fault-free and faulty conditions used for the determination of optimum set of nodes and weighting coefficients, are obtained by fault simulations using SPICE. In practice, not all of the catastrophic faults are needed to be injected to the CUT for fault simulations since there must be some sets of equivalent faults and/or equivalent fault sets formed by schematically but not physically redundant branches of the CUT. Consequently a much smaller number of faults are needed to be injected into the CUT for simulations. The number of reduction of injected faults depends on the number of schematically redundant branches. Detailed discussion will be given in Sections 5.2.1, 5.3.1, 5.4.2 and 5.4.3 for the four example CUTs.

4.7.2 Computational effort for the determination of weighting coefficients

For an optimum set consists of n nodes, the possible number of node voltages summation patterns (NVSPs) is determined by (4.1). Moreover, if there are m faults or equivalent fault sets in the fault dictionary of the CUT, the total number of

computational iterations required for the summing process is given by

$$\left[\left(\left|-1-(+1)\right|/\,step\ resolution\right)+1\right]^{n} \times m \tag{4.4}$$

Consider a CUT, which has an optimum set of 3 nodes, step resolution is 0.1, and the fault dictionary consists of 100 faults/equivalent fault sets, there will be 9,261 sets of NVSPs and totally 926,100 computational iterations are needed to be performed in the summing process. The smaller the step resolution, the more the NVSPs and the more iterations have to be performed in the summing process. However, if the maximum achievable fault coverage cannot be obtained under step resolution of, say 0.1, summing process has to be repeated with smaller step resolution, say 0.05.

In order to achieve the maximum achievable fault coverage and reduce the number of optimum set of nodes and hence to simplify the circuitry of the weighted summer, the NVSPs for the summing process can be chosen in the following way:

By (4.1), for an optimum set of n nodes there are $[(|\ -1-(+1)|/\ step\ resolution) + 1]^n$ NVSPs. Each NVSP has n WCs. If there are p WC(s) out of the n WCs is/are equal to zero, the corresponding node voltage(s) is/are neglected and the number of NVSPs could be reduced to

$$\{[(|\ -1-(+1)|/\ step\ resolution) + 1]^{n-p}\} \times n \tag{4.5}$$

and the total number of computational iterations is given by

$$\{[(|-1-(+1)|/\ step\ resolution) + 1]^{n-p}\} \times n \times m \tag{4.6}$$

As shown before, for an optimum set of 3 nodes, step resolution is 0.1, there are 9,261 sets of NVSPs. Under the same step resolution, if one of the WCs is equal to zero (i.e. (k_1, k_2, 0), (k_1, 0, k_3), or (0, k_2, k_3)) then the number of NVSPs reduces to

$$\{[(|-1-(+1)|/\ 0.1) + 1]^{3-1}\} \times 3 = 1{,}323$$

Moreover, if two of the WCs are equal to zero (i.e. (k_1, 0, 0), (0, k_2, 0), or (0, 0, k_3)), the number of NVSPs will be further reduces to

$$\{[(|-1-(+1)|/\ 0.1) + 1]^{3-2}\} \times 3 = 63$$

If the maximum achievable fault coverage cannot be obtained under the step resolution of 0.1, summing process has to be repeated with smaller step resolution, say 0.05. Using the above-mentioned CUT as an example, the relationship among the number of optimum set of nodes, step resolutions, number of NVSPs and the total number of computational iterations is shown in Table 4.5.

No. of nodes in the optimum set (n)	Step Resolution			
	0.1		0.05	
	NVSPs	Iterations	NVSPs	Iterations
3	9,261	926,100	68,921	6,892,100
2	1,323	132,300	5,043	504,300
1	63	6,300	123	12,300

Table 4.5. Relationship among the optimum set of nodes, step resolutions, number of NVSPs and the number of computational iterations

Different hardware configurations of computer will have different computational power. For example, with a personal computer equipped with Pentium 4 1.6GHz processor, the time taken to complete 926,100 computational iterations for the summing process is about 39 seconds while about 291 seconds is required for that of the 6,892,100 computational iterations.

4.8 Summary

The algorithm of the WSSNV BIST technique comprises of 5 phases. Following the first 4 phases, the fault dictionary, the detectable fault list, the optimum set of nodes, the NVSP(s) of maximum achievable fault coverage and finalized optimum set of nodes for a circuit/core are generated and derived consecutively. In the final phase, based on the final optimum set of nodes and NVSP, the weighted summer can be built and incorporated into the original circuit/core to complete the WSSNV BIST architecture. Moreover, the computational complexity of the WSSNV BIST technique is analyzed.

Chapter 5

Demonstration of the Weighted Sum of Selected Node Voltages BIST Technique

5.1 Introduction

In the following, three case studies are given to verify and demonstrate the effectiveness of the WSSNV BIST technique. An analogue active low pass filter, a mixed-signal threshold detector of a telephone ringer IC and a mathematical functional block consists of seven cores will be used as the example CUTs.

Analysis of the effectiveness of the WSSNV BIST technique is based on data obtained from fault simulations which are performed mainly based on the criteria, parameters and assumptions as stated in Section 4.2 of Chapter 4.

5.2 Testing an analogue circuit by the WSSNV BIST technique

An analogue active low pass filter circuit taken from [Chen 93] as shown in Figure 5.1 is used as one of the CUTs to demonstrate the effectiveness of the WSSNV BIST technique. The verification is performed following the 5 different phases algorithm as introduced in Chapter 4.

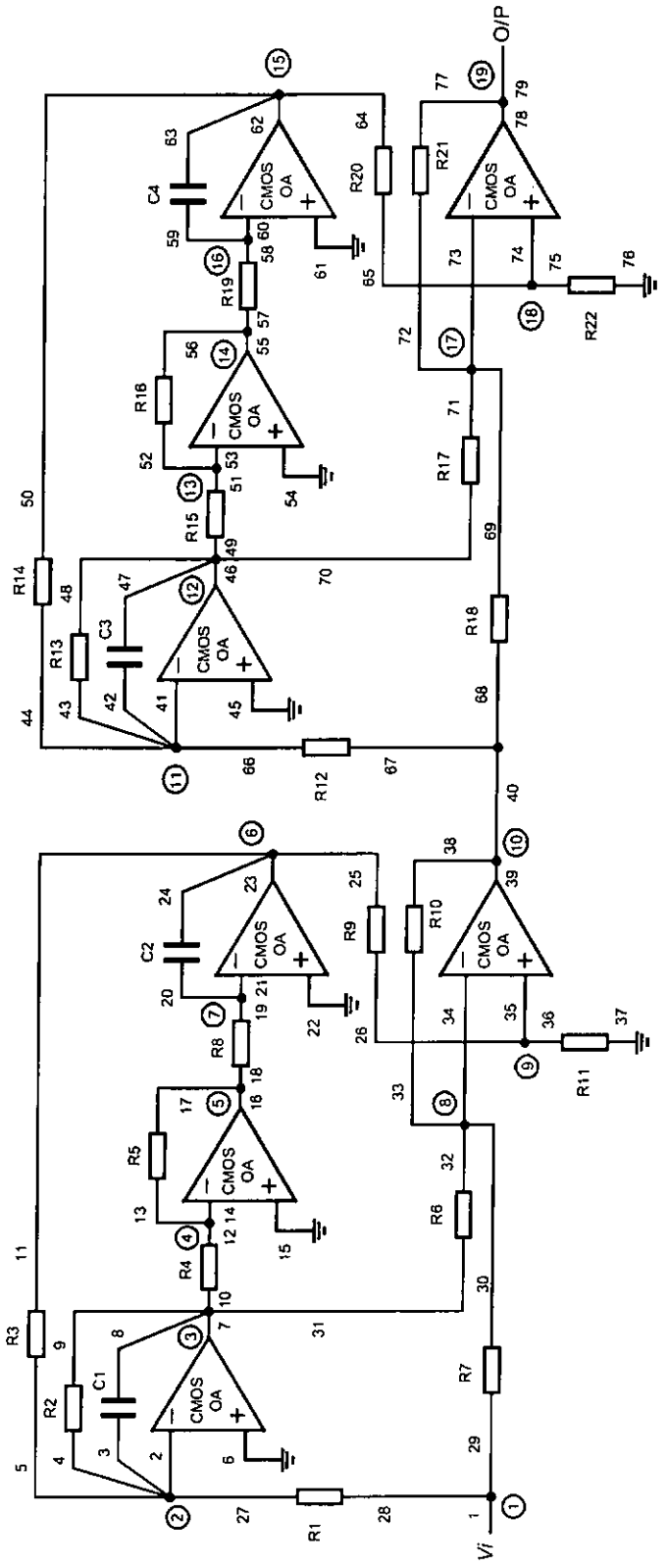

Figure 5.1 Schematic of the actve low pass filter

5.2.1 Additional simulation conditions for the active low pass filter

In addition to the simulation parameters and assumptions stated in Section 4.2 of Chapter 4, the following conditions are applied to the fault simulations of the active low pass filter:

- All the op-amps of the active low pass filter are assumed fault-free to start with.
- With reference to the schematic of the active low pass filter as shown in Figure 5.1, if all possible catastrophic faults are considered, there will be 3,240 single short faults and 63 single open faults. But referring to the schematic, 20 sets of schematically, but not physically redundant branches, are identified. Consequently, only 231 single short faults and 63 single open faults are injected to the CUT for simulations.

5.2.2 Simulation procedure

Fault simulations are carried out in phase 1. A DC voltage of 5 volts (See Section 5.8 Appendix : Determination of DC stimulus) is applied at the primary input of the active low-pass filter. Each single fault, open or short, is injected one by one to the CUT for simulation. All circuit node voltages with respect to each single fault, marked from 1 to 19 as shown in Figure 5.1, are recorded. Then a fault dictionary is generated from these recorded data.

5.2.3 Analysis of simulation results

In phase 2 operation, the detectable fault list is generated from the fault dictionary. Then an optimum set of circuit nodes is derived from the detectable fault list. For the active low pass filter, the optimum set of nodes consists of nodes (5, 13, 14, 19) or nodes (7, 13,14,19) since nodes 5 and node 7 possess the identical fault coverage.

The next step is the summing process used to sum up all these four node voltages, each of them with an appropriate Weighting Coefficient (WC), with respect to the fault-free condition and each of the individual faults. In this case, there are four WCs, k_1, k_2, k_3, and k_4 corresponding to nodes 5 (or 7), 13, 14, and 19 respectively. The four WCs (k_1, k_2, k_3, k_4) forms the node voltages summation pattern (NVSP). In this study, for the active low pass filter under the step resolution of 0.1, and the optimum set consists of 4 nodes. By (4.1), there are $[(|-1-(+1)|/0.1)+1]^4 = 194{,}481$ NVSPs.

As described in Section 4.4.2, all WCs are initially incremented in steps of 0.1. The summing process can be carried out with the help of some mathematical software packages.

All possible combinations of all values, in between and inclusive of –1 and +1, of the WCs are considered. All possible sets of the NVSPs are applied to the optimum set of circuit node voltages one by one during the summing process. For a particular set of NVSP, all the weighted sum of the optimum set of node voltages under faulty conditions are compared with the fault-free value one by one. If any of the summed

voltages deviates from the fault-free value and beyond the tolerance band, its corresponding fault is said to be detectable. The fault coverage for that particular set of NVSP is then derived.

Among 194,481 sets of NVSPs, there are 2,558 sets possess the same maximum achievable fault coverage of 94.88% are identified. Table 5.1 shows 10 examples out of the 2,558 sets of the NVSPs. The fault coverage of NVSPs of reverse polarity are the same because their absolute resultant amplitudes are identical.

NVSP			
Node 5(7)	Node 13	Node 14	Node 19
k_1	k_2	k_3	k_4
1	1	0.6	0.9
0.9	1	0.6	1
0.8	-0.7	0.2	0.5
0.6	0.2	0.3	0.6
-0.5	0.9	-0.2	-1

NVSP			
Node 5(7)	Node 13	Node 14	Node 19
k_1	k_2	k_3	k_4
-0.4	1	-0.1	-0.7
0.2	-0.5	-0.1	-0.4
0.1	-1	-0.3	-1
-0.7	0	0	0.9
-0.5	0	0	0.7

Table 5.1 Part of the sets of NVSPs which provide the maximum achievable fault coverage

It is interesting to note that there are two sets of NVSPs with k_2=k_3=0, which imply that nodes 13 and 14 can be eliminated from the optimum set of selected nodes. Hence the final optimum set of nodes will only consist of nodes 5 (or 7) and 19.

The fault coverage of the WSSNV BIST technique and its comparison with the voltage scan approach is tabulated in Table 5.2.

Faults	Fault Coverage	
	by Voltage Scan	By WSSNV
Open	77.78%	80.95%
Short	94.54%	95.15%
Overall	94.22%	94.88%

Table 5.2 Comparison of fault coverage between the voltage scan approach and the WSSNV BIST technique

As can be seen, for the example CUT, the fault coverage of the proposed testing technique is better than the voltage scan approach.

If inherently undetectable faults (which including the schematically but not physically redundant short circuit faults and those faults that cause no output deviation with respect to normal condition) were not considered, the fault coverage achieved by the WSSNV BIST technique would have been 100%.

5.2.4 Implementation of weighted summer for the active low pass filter

A weighted summing circuit is necessary to sum up the voltages at the selected circuit nodes and output to an accessible pin. As an example, consider the set of weighting coefficients (-0.5, 0, 0, 0.7), the proposed summer circuit for the active low pass filter is implemented and the complete schematic is shown in Figure 5.2. The unity gain buffers are added to minimize the possible loading effect caused by the additional circuitry.

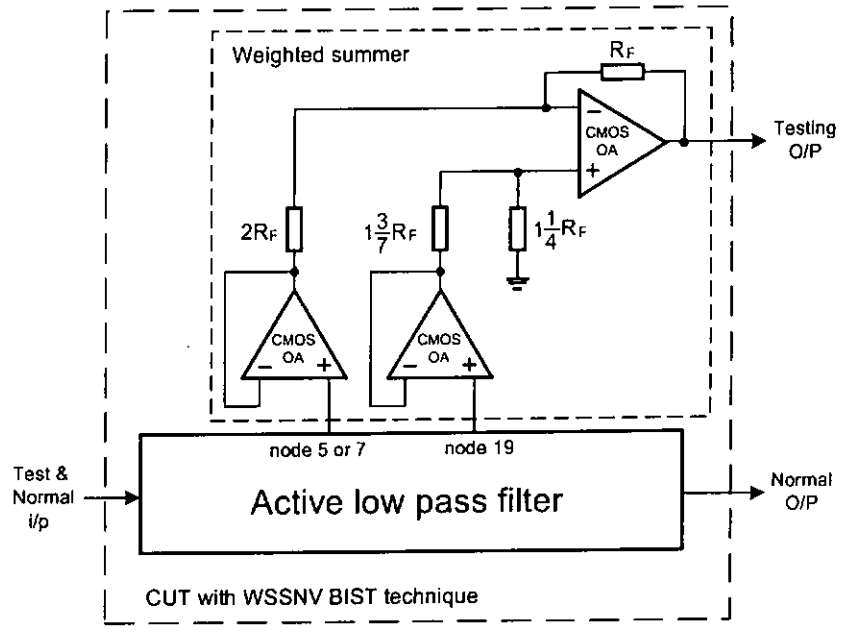

Figure 5.2 Active low pass filter equipped with WSSNV BIST technique

5.3 Testing a mixed-signal circuit by the WSSNV BIST technique

A mixed-signal circuit, the threshold detector circuit of a telephone tone ringer IC as shown in Figure 5.3 is also used as the CUT to demonstrate the WSSNV BIST technique.

5.3.1 Additional simulation conditions for the threshold detector

In addition to the simulation parameters and assumptions as stated in Section 4.2 of Chapter 4, the following conditions are applied to the fault simulations of the threshold detector:

- Similar to the former case, all possible catastrophic faults, except the gate open faults, of MOSFTEs, are being considered.
- Referring to Figure 5.3, there are totally 6,328 single short faults and 81 single open faults but 18 sets of schematically, but not physically redundant branches are identified. Consequently, only 231 single short faults and 81 single open faults are injected to the threshold detector circuit for simulations.

5.3.2 Simulation procedure

A DC voltage of 2.5 volts is applied at the detection (DET) input of the threshold detector. One single fault, open or short, is injected one by one to the CUT for simulation. All circuit node voltages, marked from 1 to 21 as shown in Figure 5.3, are recorded.

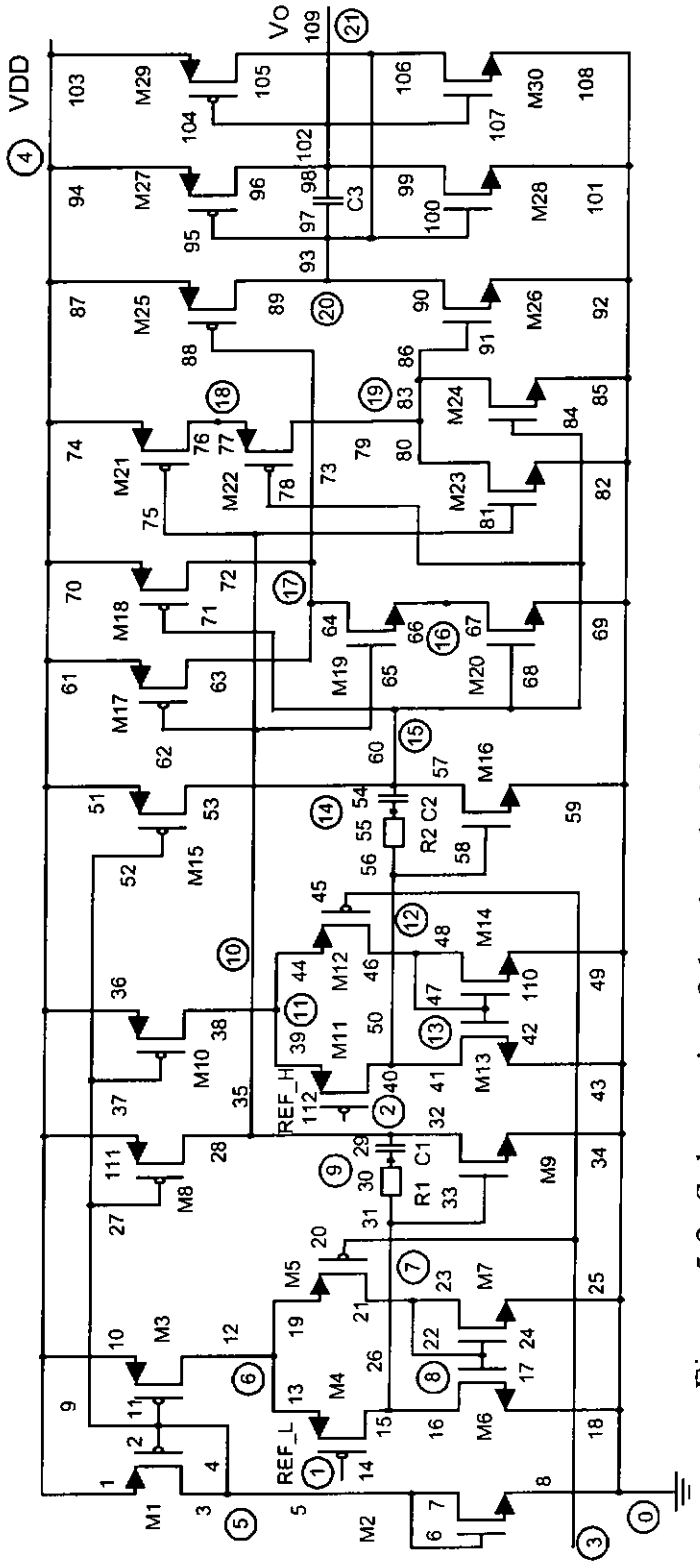

Figure 5.3 Schematic of the threshold detector of a telephonic ringer IC

5.3.3 Analysis of simulation results

A detectable fault list with respect to the circuit nodes is then formulated after the simulations are completed. An optimum set of circuit nodes which consists of nodes 8, 10, 13, 16, 20 are then determined to achieve highest fault coverage.

Like the former case, the next step is to sum up all these 5 node voltages, each of them with a WC. In this case, there are five WCs, k_1, k_2, k_3, k_4 and k_5 corresponding to nodes 8, 10, 13, 16, and 20 respectively. Under the step resolution of 0.1, by (4.1), there are $[(|-1-(+1)|/0.1)+1]^5 = 4{,}084{,}101$ NVSPs.

However, since the set(s) of NVSP(s) with maximum achievable fault coverage cannot be found at the step resolution of 0.1, the summing process is repeated with a step resolution of 0.05. Finally, 26 sets of NVSPs which can provide the same maximum achievable fault coverage of 89.31% are determined. Table 5.3 shows 10 examples out of the 26 sets of NVSPs.

NVSP				
Node 8	Node 10	Node 13	Node 16	Node 20
k_1	k_2	k_3	k_4	K_5
-0.9	0.05	0.8	0.75	0.3
-0.85	0.85	0.7	0.9	0.95
-0.8	-0.8	0.85	-0.15	-0.85
-0.8	-0.05	0.9	-0.75	-0.75
-0.6	-0.7	0.6	0.2	0.95

NVSP				
Node 8	Node 10	Node 13	Node 16	Node 20
k_1	k_2	k_3	k_4	K_5
-0.55	-0.4	0.5	0.5	-0.8
-0.55	0.35	0.55	-0.1	-0.7
-0.35	-0.3	0.25	0.85	1
-0.2	0.4	0.25	-0.5	0.6
-0.05	-0.8	0.1	-0.15	-0.65

Table 5.3 Part of the sets of NVSPs which provide the maximum achievable fault coverage

Unlike the former case, with reference to the NVSPs of maximum achievable fault coverage, there is no WC equal to zero which implies that no nodes can be eliminated from the final optimum set of nodes. The fault coverage of the WSSNV BIST technique and its comparison with the voltage scan approach is tabulated in Table 5.4.

Faults	Fault Coverage	
	by Voltage Scan	by WSSNV
Open	64.20%	77.78%
Short	81.45%	89.46%
Overall	81.23%	89.31%

Table 5.4 Comparison of fault coverage between the voltage scan approach and the WSSNV BIST technique

When compare with the voltage scan approach, a very significant improvement in fault coverage can be observed. Also, same as the former case, the fault coverage achieved is 100% of the maximum achievable fault coverage.

5.3.4 Implementation of weighted summer for the threshold detector of telephone ringer IC

Similar to former case, a weighted summing circuit is necessary to sum up the voltages at the selected circuit nodes and output to an accessible pin. Consider the node voltage summation pattern (-0.2, 0.4, 0.25, -0.5, 0.6), the proposed summer circuit for threshold detector of telephone ringer IC is implemented and the complete schematic is shown in Figure 5.4.

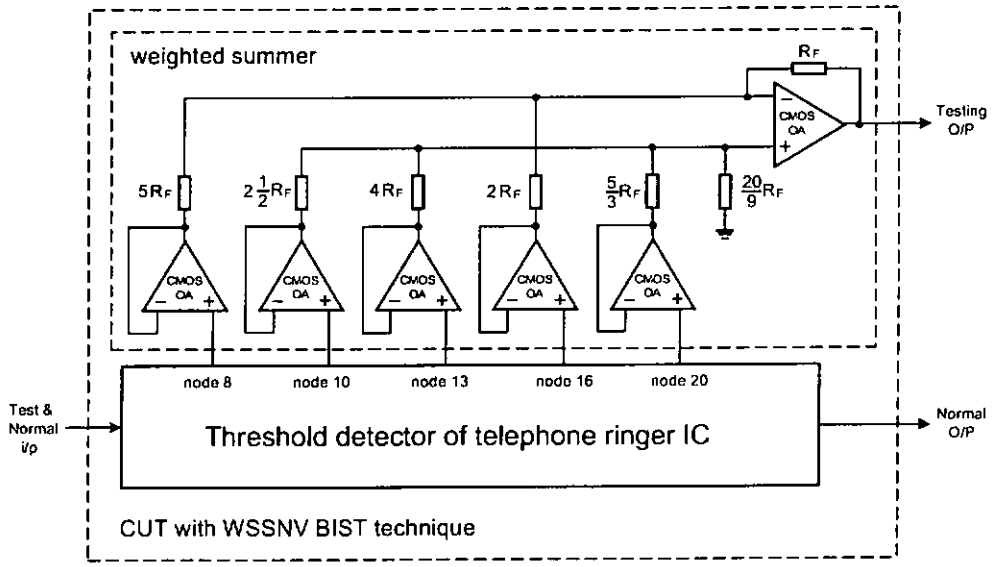

Figure 5.4. Threshold detector equipped with WSSNV BIST technique

5.4 Testing the embedded cores by the WSSNV BIST technique

As an example a mathematical functional block, which performs root mean square function for two inputs, is also used to illustrate the feasibility and effectiveness of the WSSNV BIST technique. The test architecture for the embedded cores of a SOC will also be proposed.

5.4.1 Structure of the mathematical functional block

The mathematical functional block consists of three 'square function' cores (SQ1-3) and four 'operational amplifier' cores (OA1-4). The block diagram of the mathematical functional block is shown in Figure 5.5. The schematics of the squaring (SQ) core, which is based on the multiplier circuit taken from [Song 90], and the OA core are shown in Figures 5.6 and 5.7 respectively.

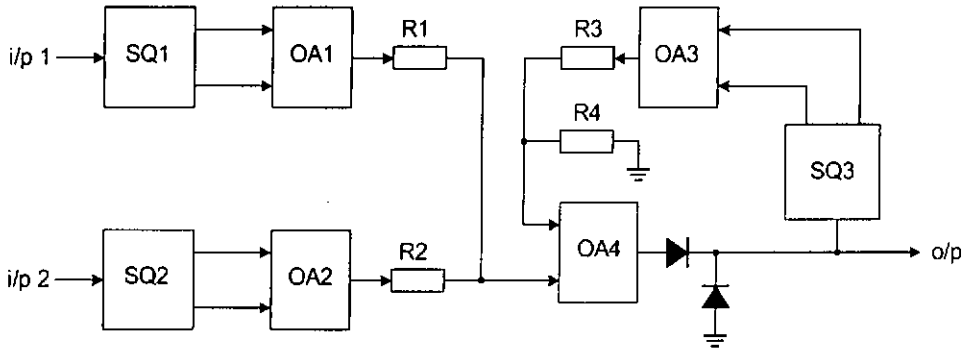

Figure 5.5 Block diagram of the mathematical functional block

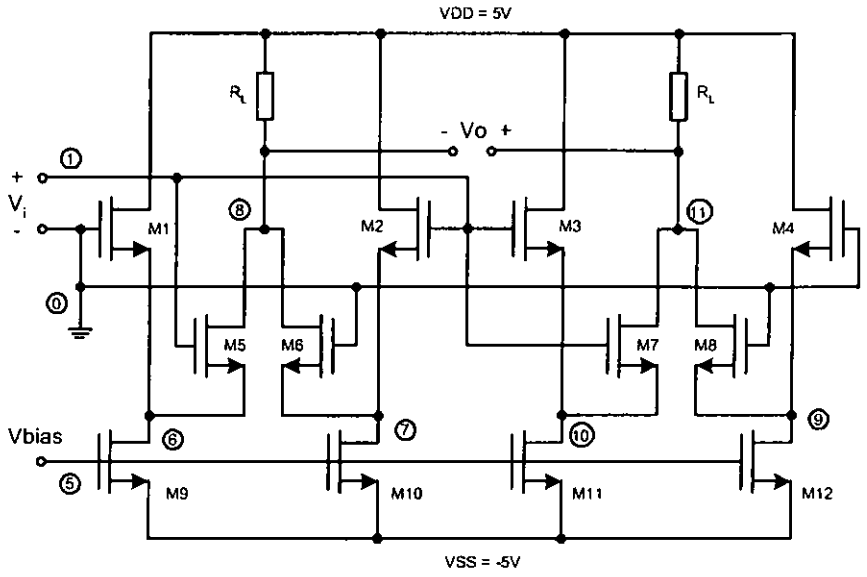

Figure 5.6 Schematic of the SQ core

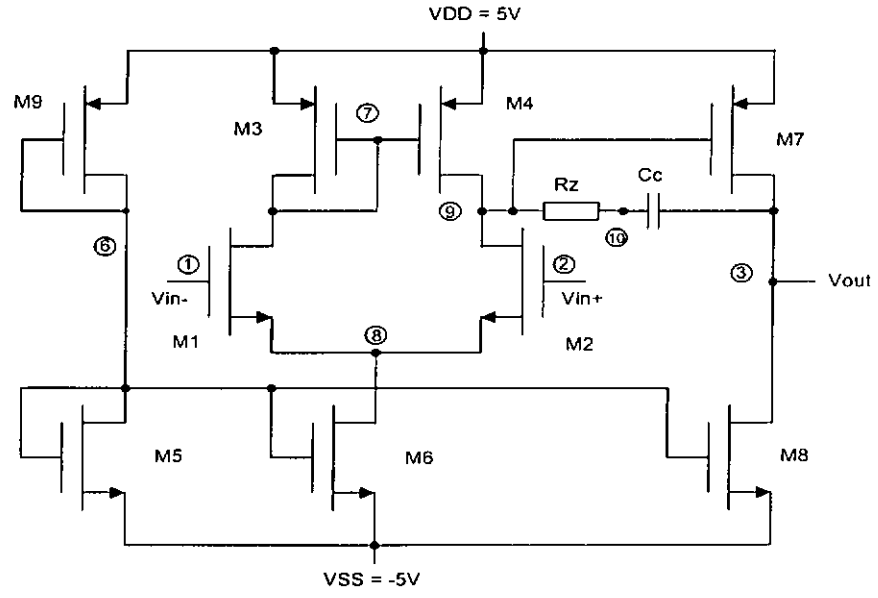

Figure 5.7 Schematic of the OA core

Fault simulations for the SQ and OA cores are carried out based on the parameters and assumptions described in Section 4.2 of Chapter 4.

5.4.2 Apply WSSNV BIST technique for the SQ core

A DC voltage of 2.5 volts is applied at the primary input of the SQ core. Totally, there are 780 single short faults and 28 single open faults. But referring to Figure 5.6, 11 sets of schematically but not physically redundant branches are identified. Consequently, only 55 single short faults and 28 single open faults are injected to the SQ core for simulations.

Like the former cases, all circuit node voltages are recorded and then a detectable fault list with respect to the circuit nodes is generated. Once the detectable fault list is formulated, the optimum set of circuit nodes can also be determined. For the SQ core, there are 3 nodes (7, 8 and 11) that constitute the optimum set of nodes.

Next step is to sum up all these node voltages, each of them with an appropriate WC, with respect to the fault-free condition and each of the individual faults. Under the step resolution of 0.1, by (4.1), there are $[(|-1-(+1)|/0.1)+1]^3 = 9{,}261$ NVSPs.

By the summing process, there are 114 sets of NVSPs can provide the maximum achievable fault coverage. Part of these sets of NVSPs is tabulated in Table 5.5.

NVSP		
Node 7	Node 8	Node 11
k_1	K_2	K_3
-1	-0.8	-0.7
-0.8	0.6	-0.2
-0.4	1	0.1
0.4	-1	-0.1
0.8	-0.6	0.2
1	0.8	0.7

NVSP		
Node 7	Node 8	Node 11
k_1	K_2	k_3
-0.1	0.9	0.2
0	-1.0	-0.3
0	-0.7	-0.2
0	0.7	0.2
0	1.0	0.3
0.1	-0.9	-0.2

Table 5.5 Part of the sets of NVSP with maximum achievable fault coverage for SQ core

It can be observed that, for some sets of NVSPs, the WC corresponds to node 7 is equal to zero which implies that node 7 can be eliminated from the final optimum set of nodes and hence it consists of nodes 8 and 11 only. The fault coverage of the WSSNV BIST technique and its comparison with the voltage scan approach for SQ core is tabulated in Table 5.6.

Faults	Fault Coverage	
	by Voltage Scan	by WSSNV
Open	92.86%	100.00%
Short	87.44%	88.59%
Overall	87.62%	88.99%

Table 5.6 Comparison of fault coverage between the WSSNV BIST technique and the voltage scan approach for SQ core

Same as previous cases, the fault coverage of WSSNV BIST technique is better than the voltage scan approach and the former has the advantages of much less hardware overhead and much faster testing time. Consider the set of NVSP, (1, 0.3) for SQ core, the corresponding weighted summer is proposed and shown in Figures 5.8.

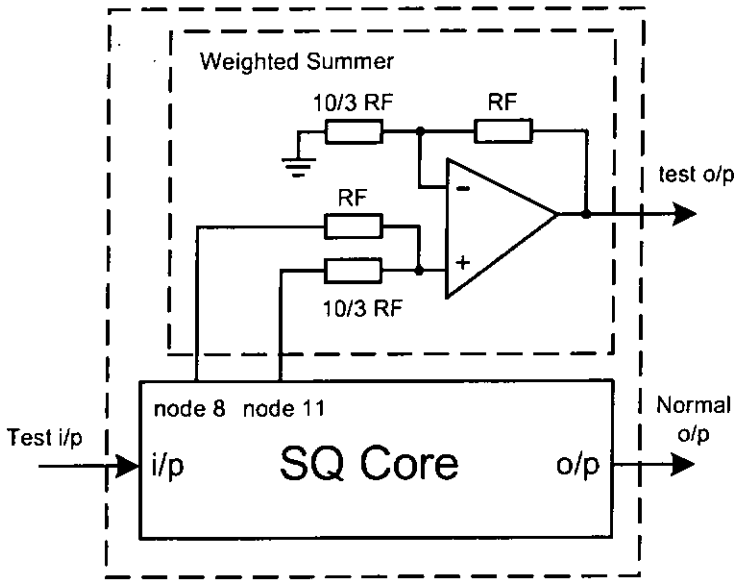

Figure 5.8 SQ Core equipped with WSSNV BIST technique

5.4.3 Apply WSSNV BIST technique for the OA core

Under test mode, the configuration of the OA core is shown in Figure 5.9. A DC voltage of 2.5 volts is applied at the non-inverting input while the inverting input is connected to ground.

Fault simulations for the OA core is carried out based on the parameters and assumptions described before. Totally, there are 465 single short faults and 22 single open faults. But referring to Figure 5.7, 11 sets of schematically but not physically redundant branches are identified. Consequently, only 55 single short faults and 22 single open faults are injected to the OA core for simulations.

Like the previous cases, all possible catastrophic faults are injected one at a time to the OA core for simulations. All circuit node voltages are recorded and, by the process as described before, are used to formulate a detectable fault list with respect to circuit nodes.

Once the detectable fault list is formulated, the optimum set of circuit nodes correspond to highest fault coverage can also be determined. For the OA core, there are 2 nodes (3 and 9) that constitute the optimum set of nodes.

Summing process then follows, under step resolution of 0.1, by (4.1), there are $[(|-1-(+1)|/0.1)+1]^2 = 441$ NVSPs. Out of 441, there are 12 sets of NVSPs can provide the maximum achievable fault coverage. Unlike the previous case studies (ALPF and SQ core), there is no WC equals zero which implies that no nodes can be

eliminated from the final optimum set of nodes. These sets of WCs are tabulated in Table 5.7.

NVSP	
Node 3	Node 9
k_1	k_2
-0.4	-1
-0.3	-0.9
-0.3	-0.8
0.3	0.8
0.3	0.9
0.4	1

NVSP	
Node 3	Node 9
k_1	k_2
-0.2	-0.6
-0.2	-0.5
-0.1	-0.3
0.1	0.3
0.2	0.5
0.2	0.6

Table 5.7 Complete sets of NVSP with maximum achievable fault coverage for OA core

The fault coverage of the WSSNV BIST technique and its comparison with the voltage scan approach for OA core is tabulated in Table 5.8.

Faults	Fault Coverage	
	by Voltage Scan	by WSSNV
Open	72.73%	81.82%
Short	81.09%	89.46%
Overall	80.69%	89.12%

Table 5.8 Comparison of fault coverage between the WSSNV BIST technique and the voltage scan approach for OA core

Same as before, for the OA core, the fault coverage of WSSNV BIST technique is also better than the voltage scan approach with the advantages of much less hardware overhead and much faster testing time.

Consider the set of NVSP (0.4, 1) for OA core, the corresponding weighted summer is proposed and shown in Figure 5.9.

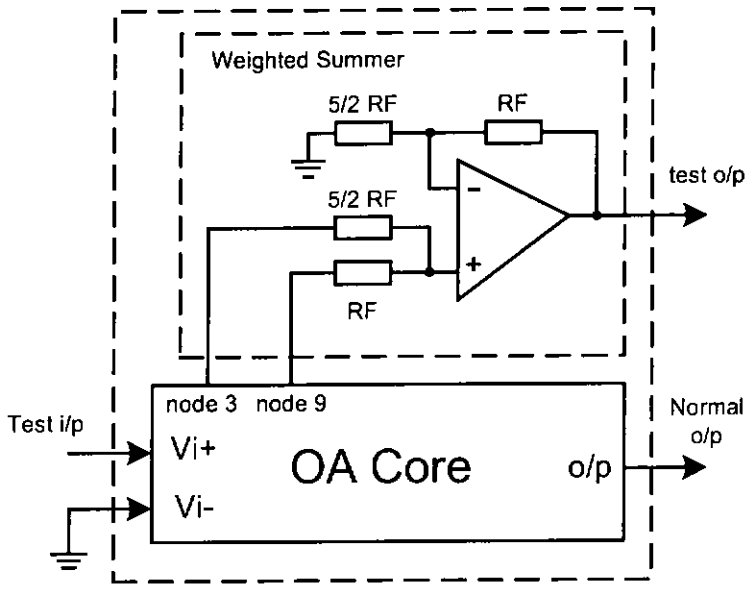

Figure 5.9 OA core equipped with WSSNV BIST technique

5.5 Fault detection of the weighted summers

The catastrophic faults of the weighted summers can also be detected by observing the test output. The fault coverage of the CUTs (the active low pass filter, threshold detector, SQ core and the OA core) and their respective weighted summers are shown in Table 5.9.

	Fault coverage (%)			
	Active low pass filter	Threshold detector	SQ core	OA core
CUT	94.88	89.31	88.99	89.12
Summer	88.30	88.53	87.64	88.76
Overall	94.53	89.25	88.85	89.06

Table 5.9 Fault coverage of the CUTs and their respective weighted summers

5.6 Proposed test architecture for the embedded cores with WSSNV BIST technique

Consider the mathematical functional block as part of the SOC design, the proposed test architecture for SQ and OA cores is shown in Figure 5.10.

Since there is still no standardized test wrapper for analog core proposed by the IEEE P1500 working group. But analogue signals are considered as one of the 'Special care' signals by the IEEE P1500 Standard Proposal [Marinissen 99]. For these types of signals, both [Marinissen 98, Marinissen 99] have proposed 'direct test access' which implies that these signals can be fed through the wrapper without intervention.

For those cores equipped with the WSSNV BIST technique, they have only one test input and one test output, no boundary scan facility is required. The wrappers simply provide two connection paths, one is the interface between the analogue cores and the Test Access Mechanism under test mode and the other is the connection between the analogue cores and the adjacent cores/circuitry under normal mode. Of its simplest form, these wrappers only consist of switches to toggle the analogue cores between normal and test modes under the control of the operation mode control logic.

Under test mode, the DC stimuli are applied to cores through the TAM while test responses from cores are also fed through the TAM to sink under the control of Control Logic. The width of the TAM can be designed depends on tolerable area overhead. For a wide enough TAM, the DC stimuli can be applied to all cores simultaneously and test responses from all cores can also be observed simultaneously. For a narrow TAM, the DC stimuli may have to be applied and the cores' test responses may have to be shifted out serially to/from cores through TAM.

Furthermore, if all the analogue cores of the SOC are equipped with the WSSNV BIST technique, the size and architecture of the Wrapper and TAM could be greatly reduced and simplified.

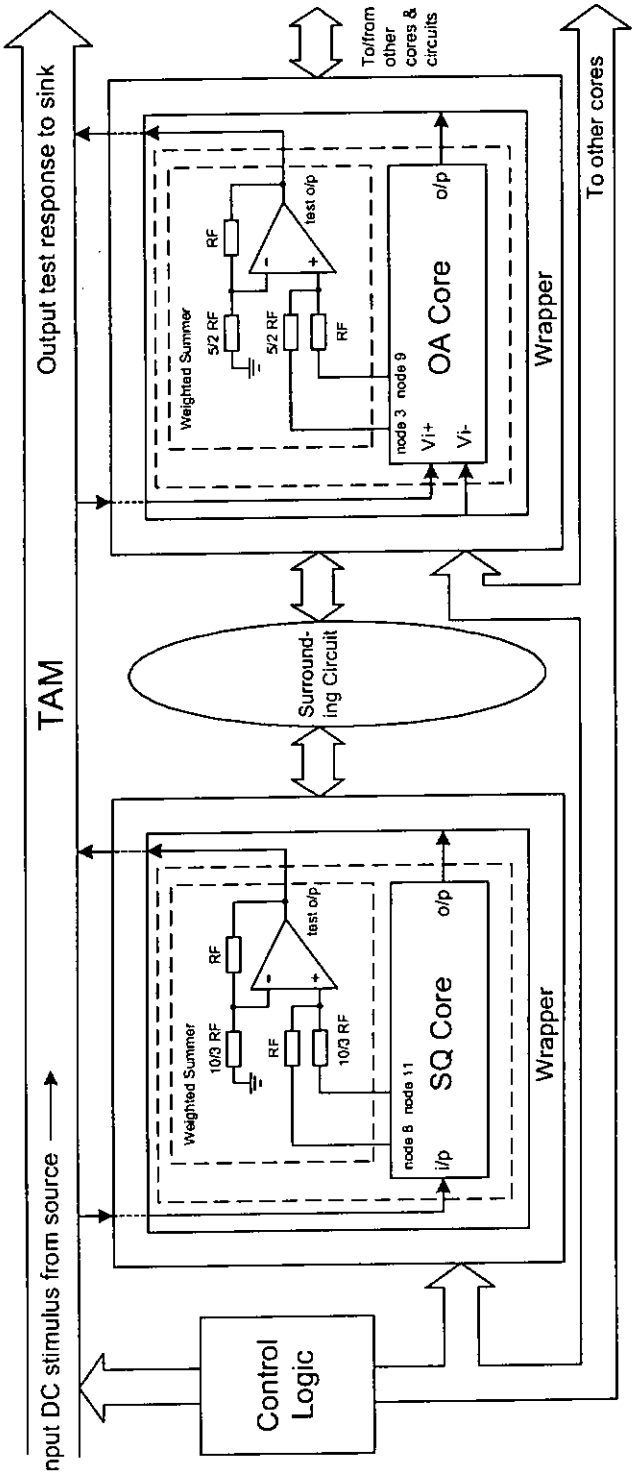

Figure 5.10 Proposed test architecture of WSSNV BIST technique for embedded cores

5.7 Summary

The WSSNV BIST technique has been applied to an analogue active low pass filter, a mixed-signal threshold detector of a telephone ringer IC, and two core of a simulated mathematical functional block to verify and demonstrate its feasibility, effectiveness and efficiency. In general, the WSSNV BIST technique can be applied to analogue or mixed-signal circuits, it has higher fault coverage than the voltage scan testing approach and a much simpler circuit structure in addition to the simple test procedure and fast test application time. Moreover, test architecture of the WSSNV BIST technique for embedded cores is also proposed. A simple TAM and wrapper design for the SOC will be benefited from those core equipped with the WSSNV BIST technique.

5.8 Appendix : Determination of DC stimulus

The SQ core will be used as the example to illustrated the relationship among test input voltage, fault coverage, original optimum set of nodes, finalized optimum set of nodes, number of NVSPs of maximum achievable fault coverage, number of NVSPs of maximum achievable fault coverage with minimum optimum set of nodes, final optimum set of nodes and appropriate NVSP.

5.8.1 Relationship between fault coverage and test input voltages

Based on fault simulations, the relationship between fault coverage (by observing all the nodes' voltages and optimum set of node (O.S.N.) voltages) and the DC stimului of the SQ core is shown in Table 5.10.

DC Stimulus (V)	Fault coverage (%)	
	By observing all nodes	By observing O.S.N.
-5.0	81.93	81.93
-4.5	85.40	85.40
-4.0	85.40	85.40
-3.5	85.64	85.64
-3.0	84.65	84.65
-2.5	87.62	87.62
-2.0	87.75	87.75
-1.5	87.87	87.87
-1.0	87.87	87.87
-0.5	85.64	85.64
0	81.19	81.19
0.5	82.67	82.67
1.0	87.87	87.87
1.5	87.87	87.87
2.0	86.39	86.39
2.5	87.62	87.62
3.0	88.74	88.74
3.5	88.74	88.74
4.0	88.74	88.74
4.5	87.62	87.62
5.0	84.65	84.65

Table 5.10 Fault coverage against DC stimului

As can be seen, same fault coverage obtained by observing all the nodes' voltages or the optimum set of node voltages. The highest fault coverage achieved is 88.74% when DC stimulus is 3, 3.5 or 4 volts.

5.8.2 Determination of DC stimulus

DC stimuli of highest fault coverage and stimulus of 2.5 volts are used as the examples to illustrated the relationship among DC stimulus, optimum set of nodes, node voltage summation patterns and fault coverage. All these relationships are shown in Table 5.11.

DC Stimulus (V)	2.5	3.0	3.5	4.0
O.S.N.	7, 8, 11	7, 8, 11	7, 8, 10, 11	7, 8, 11
F.C. by O.S.N. (%)	87.62	88.74	88.74	88.74
No. of NVSPs of M.A.F.C.	114	584	2446	892
Corresponding step resolution	0.1	0.05	0.1	0.05
No. of NVSPs with min. O.S.N.	4	2	2	2
Final NVSP	0, 1, 0.3	0, 0.95, -0.4	-0.3, 0, 0.8, 0	0.95, 0, -0.15
Final O.S.N.	8, 11	8, 11	7, 10	7, 11
F.C. by WSSNV (%)	88.99	88.99	88.99	88.99

Note : O.S.N. denotes optimum set of nodes
F.C. denotes fault coverage
M.A.F.C. denotes maximum achievable fault coverage

Table 5.11 Relationship among DC stimuli, O.S.N., NVSP, M.A.F.C., and F.C.

The optimum set of nodes may be different in respect to different DC stimuli. The figures under the heading 'No. of NVSPs of M.A.F.C.' are of especially important

since they indicate the possibility of elimination of node(s) in the finalized optimum set of nodes.

For DC stimuli of 2.5 and 3.5 volts, NVSPs of maximum achievable fault coverage obtained in summing process under step resolution of 0.1. For DC stimuli of 3 and 4 volts, the step resolution has to be increased to 0.05 to achieve the same coverage.

Nevertheless, the resultant fault coverage and the number of nodes in the final optimum set of nodes for all these four DC stimuli are the same no matter how they are different before the application of WSSNV BIST technique to the SQ core. Hence, the voltage of the DC stimulus is not important to the final result.

Chapter 6

Built-In Self-Test Technique for Analogue Cores of System-On-Chip Based on Summations of Cores' Test Output Voltages

6.1 Introduction

This chapter presents a unified BIST approach for the analogue portion of a SOC that is based on summations (weighted and non-weighted) of analogue cores' test output voltages (SOCTOV) and results in a much less hardware overhead and fast test application time. The proposed BIST technique is developed in conjunction with the WSSNV BIST technique for embedded cores. The WSSNV BIST technique provides high fault coverage for individual cores while the SOCTOV BIST technique provides a 100% fault diagnosis resolution for location of the faulty core. It is an alternative solution to the testing of analogue cores especially when chip area overhead is a critical concern.

6.2 Working principle of the SOCTOV BIST technique

Under the SOCTOV BIST approach, all the test output voltages of the analogue cores equipped with the WSSNV BIST technique are summed together (weighted and non-weighted). By observing these weighted and non-weighted summing outputs, those known nominal values and the weighting coefficients, the faulty condition of the SOC and the location of the faulty core can be uniquely identified.

6.3 Configuration of the SOCTOV BIST technique

The mathematical functional block will be used again to illustrate the configuration of the SOCTOV BIST technique. Assume all the other analogue cores of the SOC, like the cores of the mathematical functional block are equipped with the WSSNV BIST architecture.

Under test mode all the cores should be connected similar to the cores SQ1 and OA1 of the mathematical functional block as shown in Figure 6.1. Surrounding circuitry can be formed into groups and be tested just like a core. As an example, R1 – R4 of the mathematical functional block are grouped and reconfigured as a voltage divider by the core test wrapper under test mode. Since the test stimuli are DC voltages and can be simply obtained from the VDD, and the test output responses are directly observed from the weighted or non-weighted circuitry of the SOCTOV BIST architecture, the TAM can has a much simple structure. The SOC will be toggled between normal and test modes by the control logic and in turn by the wrapper and TAM.

All the analogue cores' test output voltages are fed to the weighted or non-weighted summers of the SOCTOV BIST architecture as shown in Figure 6.2.

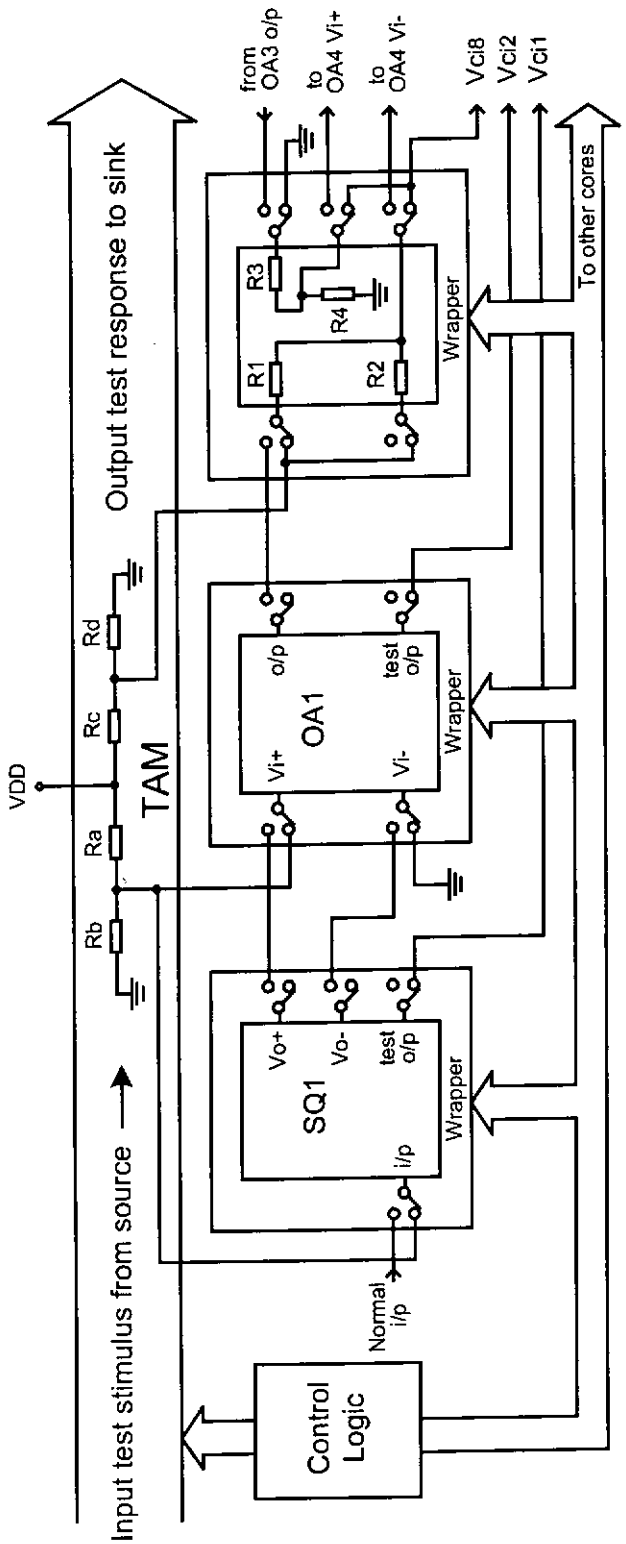

Figure 6.1 Configuration of part of the mathematical functional block under test mode

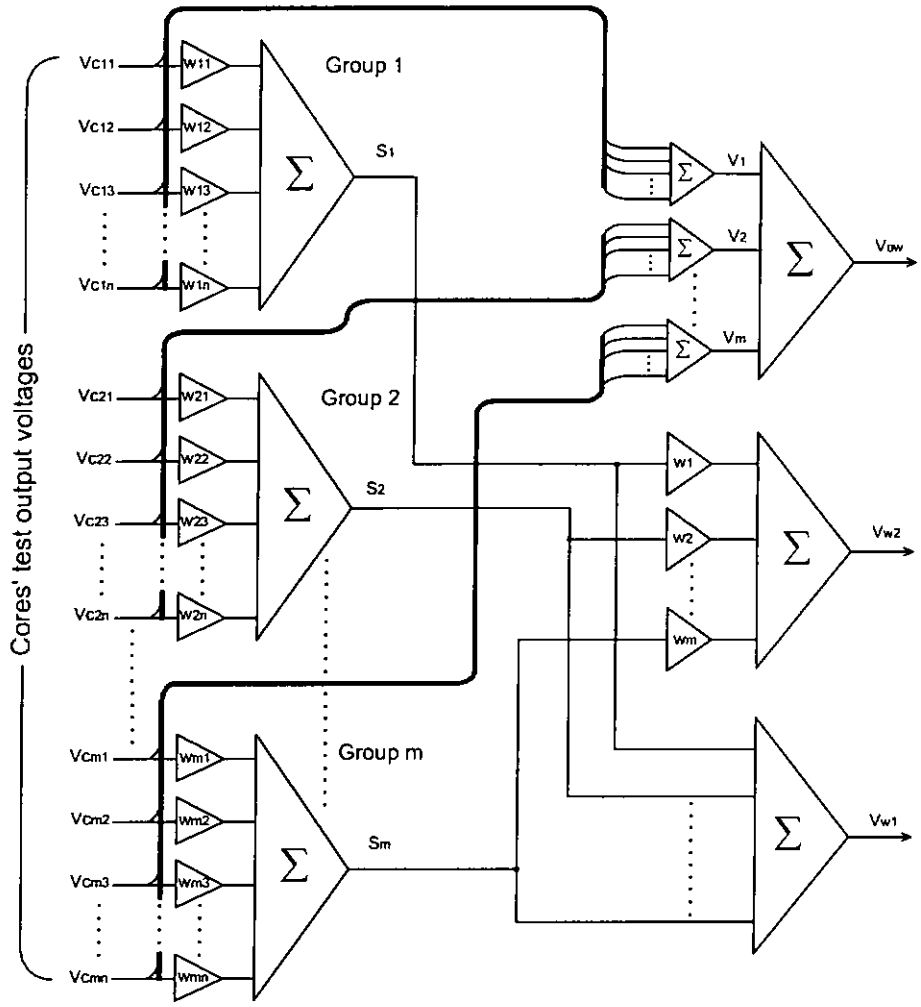

Figure 6.2 Proposed test architecture for SOC with SOCTOV BIST technique

6.4 Algorithm of the SOCTOV BIST technique

The SOCTOV BIST architecture is shown in Figure 6.2. The algorithm of the SOCTOV BIST technique is developed based on the following conditions and assumptions:

- cores are separated into groups;
- cores are isolated from each others during the test mode;
- consider single catastrophic faults;
- the cores' test output voltages are summed (weighted and non-weighted);
- test stimuli are applied to the cores' test inputs simultaneously under test mode;
- all the weighted and non-weighted test output voltages are observed simultaneously.

Referring to Figure 6.2, the notations are defined as follows:

Vc_{ij} represents test output voltage from core ij (core j of group i), for i=1 to m, j=1 to n

W_{ij} represents weighting coefficient for test output voltage of core ij, for i=1 to m, j=1 to n

S_i represents weighted sum of group i cores' test output voltages, for i=1 to m

V_i represents non-weighted sum of group i cores' test output voltages, for i=1 to m

V_{ow} represents non-weighted sum of all V_i, for i=1 to m

V_{w1} represents non-weighted sum of all S_i, for i=1 to m

W_i represents weighting coefficient for S_i, for i=1 to m

V_{w2} represents weighted sum of all S_i, for i=1 to m

Assuming that the SOC under faulty condition, the faulty values of V_{ow}, V_{w1} and V_{w2} are denoted by V_{owF}, V_{w1F}, and V_{w2F} respectively.

$$V_{w2F} = \sum_{i=1}^{m} W_i S_i \tag{6.1}$$

$$V_{w1F} = \sum_{i=1}^{m} S_i \tag{6.2}$$

To identify the faulty Group *i*, the following process is used:

For i = 1 to m

{

Eq(6.1)/W_i – Eq(6.2) = $V_{w2F}/W_i - V_{w1F}$;

Sub nominal values of S_i into L.H.S;

Compare ($V_{w2F}/W_i - V_{w1F}$) and ($V_{w2}/W_i - V_{w1}$);

Are they equal ?

If equal, Group *i* is faulty, then break;

If not equal, next *i*;

}

Determination of the faulty value S_{iF} of faulty Group *i* is based on the following expression:

$$S_{iF} = S_i + (V_{w1F} - V_{w1}) \tag{6.3}$$

Since S_i, V_{w1F}, and V_{w1} are known, S_{iF} can be determined.

To identify the faulty Core *ij* of faulty Group *i*:

$$S_{iF} = \sum_{j=1}^{n} W_{ij} Vc_{ij} \qquad \text{for } i=1 \text{ to } m \tag{6.4}$$

$$V_{iF} = \sum_{j=1}^{n} Vc_{ij} \qquad \text{for } i=1 \text{ to } m \tag{6.5}$$

Since the corresponding faulty group number i is identified with previous procedures, for clarity, group 1 is assumed to be the faulty group in describing the succeeding procedures. Hence we have,

$$S_{1F} = \sum_{j=1}^{n} W_{1j} Vc_{1j} \tag{6.6}$$

$$V_{1F} = \sum_{j=1}^{n} Vc_{1j} \tag{6.7}$$

To identify the faulty Core 1j, the following process is used:

For j = 1 to n

{

Eq(6.6)/W_{1j} – Eq(6.7) = $S_{1F}/W_{1j} - V_{1F}$;

Sub nominal values of Vc_{1j} into L.H.S;

Compare ($S_{1F}/W_{1j} - V_{1F}$) and ($S_1/W_{1j} - V_1$);

Are they equal ?

If equal, Core 1j is faulty, then break;

If not equal, next j;

}

Determination of the faulty value Vc_{1jF} of the faulty Core 1j is based on the following expression:

$$Vc_{1jF} = Vc_{1j} + (V_{1F} - V_1) \tag{6.8}$$

Since Vc_{1j} and V_1 are known and V_{1F} can be found by the following equation

$$V_{1F} = V_1 + (V_{owF} - V_{ow}) \tag{6.9}$$

Hence Vc_{1jF} can be determined. All the faults come from the cores can then be detected and the faulty core can also be identified.

6.5 Summary

A unified BIST approach for the analogue portion of a SOC is presented, which is the union of two BIST techniques, WSSNV and SOCTOV. The WSSNV BIST technique provides high fault coverage for each of the individual cores while the SOCTOV BIST technique provides a 100% fault diagnosis resolution to locating the faulty core. In addition to high fault coverage, high faulty core locating capability and small hardware overhead, the proposed single pass BIST approach provides an extremely fast test time for the analogue cores under test. During the test mode, test stimuli are applied to all cores and test outputs are observed simultaneously. Consequent analysis can be performed by an automatic test equipment (ATE) setup. Overall, the proposed BIST technique has the major advantages of simple circuit structure, small chip area overhead, high fault coverage and fast test application time. It provides an alternative solution to the testing of analogue cores especially when chip area overhead is a critical concern.

Chapter 7

Built-In Self-Test Technique for Analogue Cores of System-On-Chip by Using Full Range Window Comparator

7.1 Introduction

The full range window comparator (FRWC) BIST technique is also developed in conjunction with the WSSNV BIST technique for the effective testing of mixed-signal SOC. The essential component of the FRWC BIST technique is a FRWC. The FRWC is used to evaluate the analogue cores' test output voltages to determine whether the core(s) is/are faulty and to locate the fault (or equivalent fault set) within the faulty core(s).

Under the FRWC BIST architecture, all the analogue cores are equipped with the WSSNV BIST technique and their test output voltages are fed to a common FRWC consecutively through the analogue scan paths. DC test stimuli are applied to all cores simultaneously. The FRWC will examine the test output voltage of each core one by one and then output the test results to a test control unit. The control unit will, depends on the test results from FRWC, instruct a test output unit to output a corresponding bit pattern to indicate whether the core under test is faulty and the location of fault (or equivalent fault set) if the core is under faulty condition. Hence, the resultant response of test application is a binary bit stream which can be easily incorporated into the existing testing architecture for the digital portion of the

mixed-signal SOC such that a single digital Automatic Test Equipment (ATE) is all that required.

7.2 Working principle of the full range window comparator

There are many window comparators proposed in literature. In [Franca 91], a mixed-analogue-digital window comparator whose boundaries can be programmed independently is introduced. By converting the existing op-amps or OTAs into two-mode comparators to monitor specific internal node voltages on-chip is described in [Venuto 00]. In [Venuto 02], a digital window comparator implemented with standard digital gates to monitor analogue voltages on-chip is presented. However, the first proposal has a relatively complex circuit and operating procedure while the second and third proposals are targeted on on-chip monitoring of specific node voltages with predetermined window boundaries. A new window comparator is proposed here, which has a simple circuit structure and window boundaries can be freely adjusted in between and inclusive of VSS and VDD.

7.3 Inverter gate with adjustable switching threshold

As shown in Figure 7.1, the basic element of the FRWC is an inverter gate with adjustable switching threshold. It is constructed with a CMOS inverter and an operational amplifier (op-amp). It can be switched at any desired input voltage Vi, in between and inclusive of VSS and VDD.

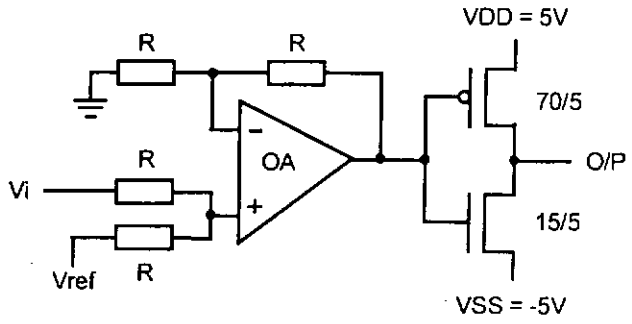

Figure 7.1 Schematic of an inverter gate with adjustable switching threshold

The switching threshold of a CMOS inverter gate is given by [Weste 93]:

$$V_{sw} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \tag{7.1}$$

where β_n/β_p and V_{tn}/V_{tp} are transistor gain and threshold voltages of N/P transistors respectively. The inverter can never be switched at any desired input voltages other than the switching threshold. The op-amp is employed to offset the switching threshold such that the inverter can be effectively switching at any desired input voltages. By adjusting the reference voltage V_{ref} in such a way:

$$V_{ref} = V_{sw} - V_i \tag{7.2}$$

Where V_i is the desired switching voltage of inverter. By simulation with a 2μm CMOS process parameters, the example inverter of transistor sizing shown in Figure 7.1 has a switching threshold of 0.5743V. By adjusting the reference voltages V_{ref} of the op-amp, the inverter can be switched at any desired voltages, in between V_{DD} and V_{SS}, of V_i. Based on simulation results, the switching behavior of the inverter was obtained and shown in Figure 7.2.

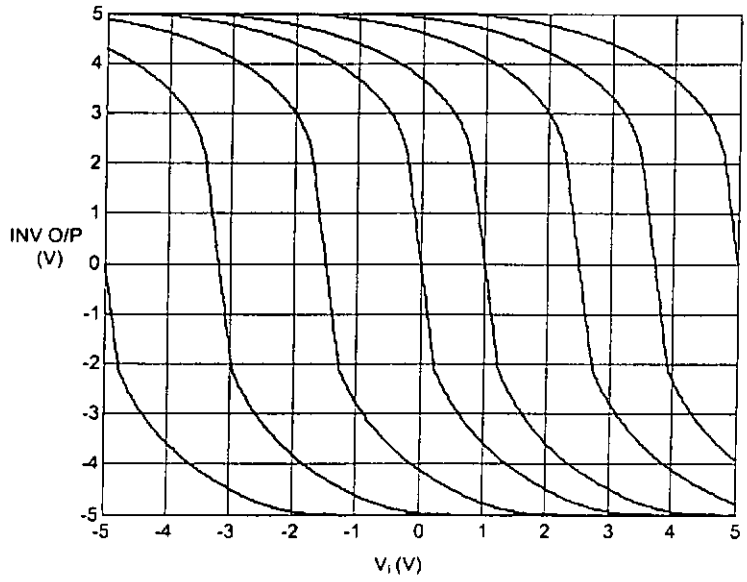

Figure 7.2 Simulation results of the inverter with adjustable switching threshold

7.4 Implementation of the full range window comparator

As shown in Figure 7.3, the FRWC is constructed with two inverters of adjustable switching threshold and a XOR logic gate.

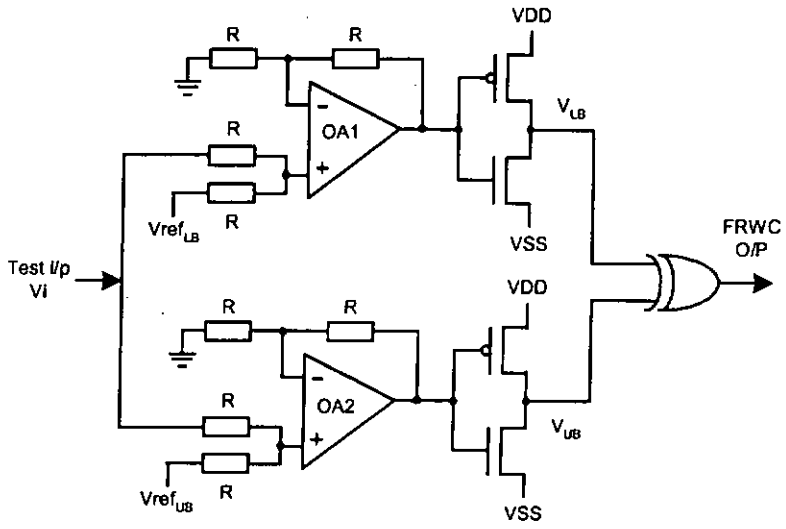

Figure 7.3 Schematic of the full range window comparator

One set of switching threshold adjustable inverter is responsible for the detection of lower boundary V_{LB} of the window range while another set is responsible for that of the upper boundary V_{UB}. Outputs from these inverters are XORed. The test resultant output from the XOR gate would be at logic '1', if either of its inputs V_{LB} or V_{UB} is at logic '1'. Figure 7.4 shows the simulation results of the FRWC with window width of 2.96V (V_{LB} = -0.5V, V_{UB} = 2.46V).

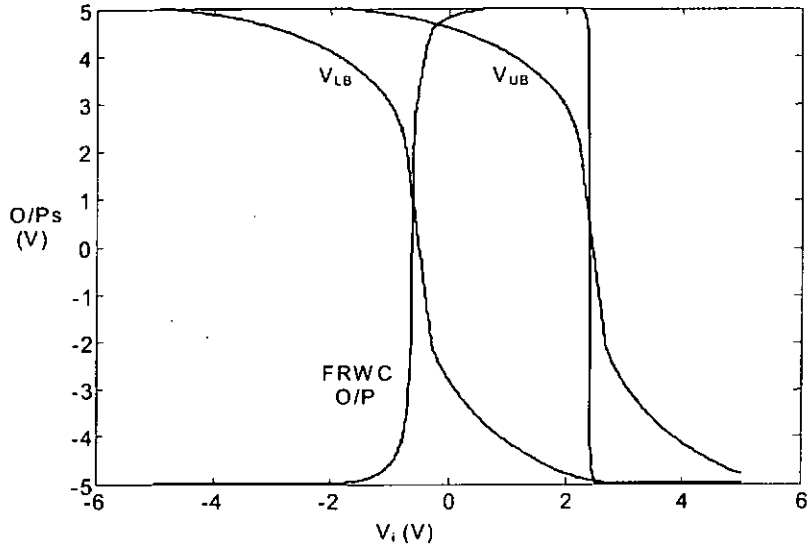

Figure 7.4 Simulation results of the full range window comparator

The relationship between the two logic levels of XOR output and the inverter outputs is shown in Table 7.1.

Case	Logic level		
	V_{UB}	V_{LB}	XOR O/P
1	0	0	0
2	0	1	1
3	1	0	1
4	1	1	0

Table 7.1 Relationship of logic levels between outputs of inverters and XOR gate

The width of the window represents the tolerance range of a core's test output voltage to be detected. Whenever the core's test output voltage lies beyond the window slot, a faulty condition is detected. With reference to the simulation results of the FRWC (as shown in Figure 7.4), the condition of case 2 will never exist.

When input voltage lies within the window slot, V_{LB} will be at logic '0', V_{UB} will be at logic '1' and the output of XOR gate will be at logic '1' to indicate the CUT is fault free. The proposed application of the FRWC in conjunction with the WSSNV BIST technique for the testing of analogue cores of a SOC, is referred as the FRWC BIST technique, will be described in the next section.

7.5 Proposed FRWC BIST technique for the testing of analogue cores of a SOC

The configuration, algorithm, and the structure of test output bit pattern of the FRWC BIST technique will be introduced in this section.

7.5.1 Configuration of the analogue portion of a SOC with FRWC BIST technique

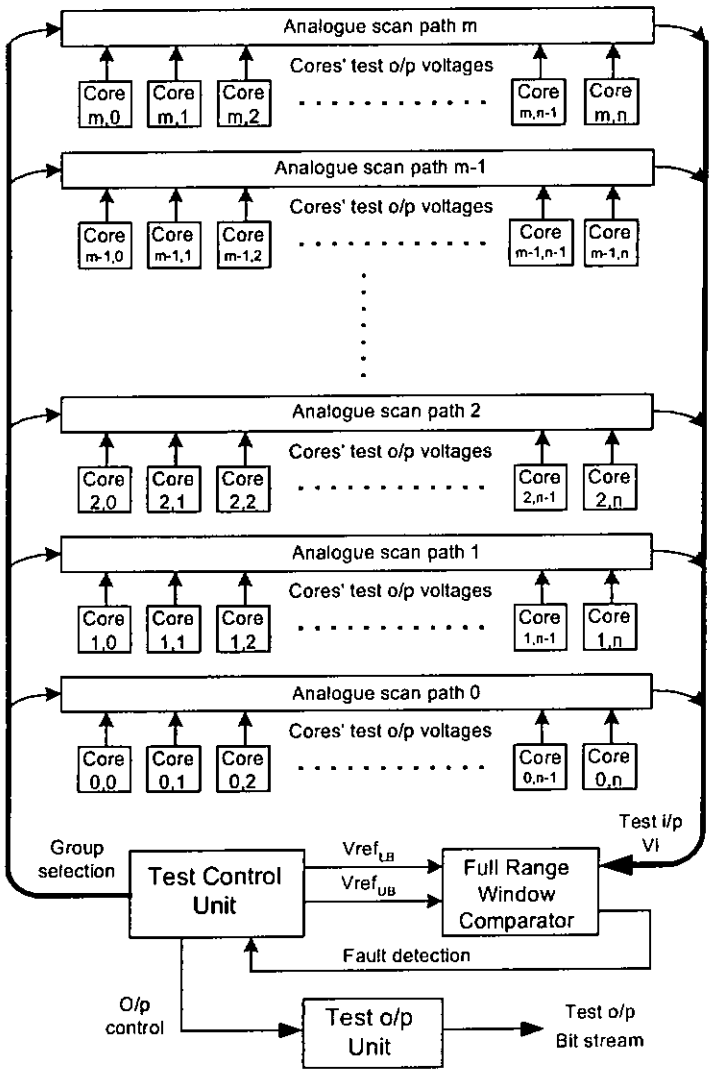

Figure 7.5 Configuration of the FRWC BIST architecture

The configuration of the analogue portion of a SOC under test is shown in Figure 7.5. The architecture and function of various part of the configuration is summarized as follows:

(i) All the analogue cores are equipped with the WSSNV BIST technique. Hence, the cores' test output voltages are the weighted sum of their selected node voltages with respect to fault-free and faulty conditions.

(ii) Due to a large number of cores will be involved in a SOC design, to facilitate the testing and to make the FRWC BIST technique a scalable structure, cores are separated into groups. Each group is equipped with an analogue scan path where all cores' test output voltages are connected. Cores are isolated from each other during the test mode.

(iii) All the analogue scan paths are connected to a common FRWC. The window comparator is used to identify the faulty core(s) and the unique fault (or equivalent fault set) within the faulty core(s) in phases 1 and 2 operations respectively.

(iv) A test control unit is employed to coordinate all the testing facilities, including the tasks of cores' group and core selection, the appropriate window width adjustment, and to control the test output unit to output the corresponding bit patterns in response to the test results.

7.5.2 Testing algorithm of the FRWC BIST technique

The testing algorithm is divided into two phases, identification of faulty cores and location of faults within faulty cores.

Phase 1: Identification of faulty cores

(i) DC test stimuli are applied to all cores simultaneously.

(ii) Select the first group in the group list.

(iii) Select the first core from the current core list of current selected group.

(iv) Test Output Unit output header bits to show current core's number.

(v) Adjust window width of FRWC according to the tolerable test output voltage ranges of the current core under test.

(vi) If the core's test output voltage lies within the window width (i.e. tolerable range of current core's test output voltage), which implies that the core is fault-free and the FRWC output will be at logic '1'. This test result is passed to the Test Control Unit which in turn to control the Test Output Unit to output the corresponding fault-free bit pattern (the structure of bit pattern will be introduced in Section 7.5.3). If the FRWC output is logic '0' implies a faulty core is detected, then go to Phase 2.

(vii) Delete current core from current core list.

(viii) If current core list is not exhausted, return to step (iii) else delete current group from group list.

(ix) If group list is not exhausted, return to step (ii) else end.

Phase 2: Location of faults within a faulty core

(i) Select the first fault from the fault list of the current faulty core.

(ii) Adjust window width of FRWC according to the error range of core's test output voltage of the current fault.

(iii) If the core's test output voltage lies within the window width of the FRWC, which implies that the corresponding fault (or equivalent fault set) is existed and the output of FRWC will be at logic '1' which will be used by the Test Control Unit to control the Test Output Unit to output the next bit as logic '1'. If the current fault is not existed the next output bit will be of logic '0'.

(iv) Delete current fault from fault list.

(v) If fault list is not exhausted, go back to step (i) else return to step (Vii) of Phase 1.

7.5.3 Structure of the test output bit stream

The structure of the test output bit stream is shown in Figure 7.6.

Figure 7.6 Structure of the test output bit stream

The test output bit patterns for all cores are of equal length. Start from core (0,0) until core (m,n), corresponding test output bit patterns are shifted out consecutively

and continuously to form a bit stream. The bit pattern, corresponding to a CUT, consists of two components, Header and Status Bits.

- Header – consist of x bits used to represent the core number. Where x is given by

$$x = \lceil \log w / \log 2 \rceil \tag{7.3}$$

where w denotes the total number of cores attached to the FRWC BIST architecture.

- Status Bits – used to indicate the health status of the corresponding fault (or equivalent fault set) of the respective core. One bit represents one catastrophic fault of the CUT. All the status bits will be at logic '0' to indicate the core is under fault-free condition. The length of the Status Bits will be equal to y bits. Where y is the largest number of catastrophic faults that, among all the cores, a particular core has. For those cores have less number of catastrophic faults, the reminder bits will be inserted with '0's.

7.6 Summary

The FRWC BIST technique for the testing of analogue cores of a mixed-signal SOC has been illustrated. It is a unified BIST technique, developed in conjunction with the WSSNV BIST technique. A FRWC design is demonstrated that can be used to monitor the analogue cores' test output voltages effectively. With the FRWC BIST technique, the analogue portion of a mixed-signal SOC can be tested with a digital tester without the necessity of any analogue I/Os. Therefore, from the view of testing, the whole mixed-signal SOC can be treated as a digital system. By reading the bit stream at the test output, whether the analogue portion of the SOC is healthy or one or more of its embedded analogue cores is/are under faulty conditions can be determined. It also has the capability to locate the unique faults or equivalent fault sets within the faulty core.

Chapter 8

Conclusions and Proposed Future Works

8.1 Conclusions

Three different BIST techniques for the analogue cores of SOC have been developed. These BIST techniques can either be used in isolation or in a combined ways to achieve effective and efficient testing of the analogue cores of SOC. All these BIST techniques are verified to be effective by simulations. The salient points and major advantages of the three techniques are summarized as follows:

The WSSNV BIST technique was developed based on the weighted sum of selected node voltages (WSSNV) for the effective testing of analogue circuits/embedded cores. An analogue active low pass filter, a mixed-signal threshold detector of a telephone ringer IC, and two example cores were used as CUTs to evaluate the effectiveness and performance of the WSSNV BIST technique. From the simulation results obtained, if inherently undetectable faults (which including the schematically but not physically redundant short circuit faults and those faults that cause no output deviation with respect to normal condition) are not considered, then the fault coverage acquired is already 100% of their respective maximum achievable fault coverage. Moreover, the optimum set of nodes may be further fine-tuned during the evaluation process of node voltage summation patterns (NVSPs), just like in the cases of the active low pass filter and the SQ core.

The major advantages of the WSSNV BIST technique are two-fold: (i) the requirement of testing I/O pins is reduced to the minimum; and (ii) also the hardware overhead is substantially reduced. This results in a much simplified design of TAM and the core test wrapper circuitry. Also the testing procedure is simplified and the testing time is reduced due to the fact that only one test output response needs to be observed. In general, the WSSNV BIST technique is verified to be an effective testing technique with high fault coverage; applicable to both analogue and mixed-signal circuits; simple circuit structure and small hardware overhead.

SOCTOV is a unified BIST approach proposed for the testing of analogue cores of a SOC, which was developed in conjunction with the WSSNV BIST techniques and is based on the summations of cores' test output voltages (SOCTOV). The WSSNV BIST technique provides 100% maximum achievable fault coverage for each of the individual cores while the SOCTOV BIST technique provides a 100% fault diagnosis resolution to locating the faulty core. In addition to high fault coverage, high faulty core locating capability and small hardware overhead, the unified single pass BIST technique provides an extremely fast test time for the testing of analogue cores of a SOC. During the test mode, test stimuli are applied to all analogue cores and test outputs are observed simultaneously. Consequent analysis can be performed by an automatic test equipment (ATE) setup. Overall, the unified BIST technique has the major advantages of simple circuit structure, small chip area overhead, high fault coverage and fast testing time. It provides an alternative solution to the analogue cores testing especially when chip area overhead is a critical concern.

Finally, another BIST technique based on Window Comparator of Cores' Test Output Voltages for the effective testing of analogue cores of a mixed-signal SOC was proposed, which is referred as Full Range Window Comparator (FRWC) BIST technique. It is also a unified BIST technique, developed in conjunction with the WSSNV BIST technique. The testing output is a binary bit stream. With FRWC BIST technique, the analogue portion of a mixed-signal SOC is tested with a digital tester without the necessity of any analogue I/Os. In the view of testing, the whole mixed-signal SOC can be treated as a digital system. By reading the binary patterns of the bit stream, whether the SOC is healthy or one or more of its embedded cores is/are under faulty conditions can be determined. In contrast with the SOCTOV BIST technique, it has the major advantage of not only capable to locate the faulty core(s) but also has the capability to locate the unique faults or equivalent fault sets within the faulty cores.

By using the analogue cores equipped with these proposed BIST techniques, a SOC designer needs not to put much effort on the testing issue of the analogue cores. The small I/O pins requirements and simple test circuitry lead to less chip area overhead and result in the ease of wrapper and TAM designs. The simple test procedure enables a fast test application time. With the data of test output response provided by the IP core designer, the SOC designer can easily design the ATE setup to utilize the test output data such that the faulty core and/or even the unique fault (or equivalent fault set) within the faulty core can be identified.

8.2 Proposed further works

For the FRWC BIST technique, its effectiveness and performance are affected by the effective implementation of the FRWC. The proposed FRWC is verified to be effective by simulations. In practice, the effective implementation of the FRWC depends on the control of CMOS process variation, the offset of op-amps and the accuracy of reference voltages within acceptable range. Future works are proposed as follows:

- To study the implications of CMOS process variation, op-amp offset, and the accuracy of reference voltages against error rate of the window width of the window comparator. Based on existing available techniques and/or to develop novel approaches to eliminate/minimize all these adverse factors.

- The performance of digital circuits critically depends on I-V characteristics of MOS transistors and the parasitics in interconnection lines, both of which can vary due to process variations [Kang 99]. The drain current of an MOS transistor can be described by

$$I_d = \mu C_{ox} \frac{W}{L} f(V_{DS}, V_{Gs}, V_T) \qquad (8.1)$$

where μ is the mobility of electrons in nMOS (holes in pMOS) transistors,

$C_{ox} = \varepsilon_{ox}/t_{ox}$ is the gate oxide capacitance per unit area,

W/L is the ratio of the channel width to channel length, and

V_T is the threshold voltage of the transistor.

Among the parameters in (8.1), the only designable parameter under the jurisdiction of the designer is the nominal value of the aspect ratio, *W/L*. Thus in order to make the circuit performance less sensitive to process variations is to determine the optimal values of *W* and *L* for various MOS transistors in the circuit. Also, a more careful layout with proper orientation of transistors can be done to make the processed circuit less sensitive to process variations. This is even more important for analog circuits. Cad tools may be used to simulate and verify the effects regarding this issue.

- With some existing techniques like median-based offset cancellation circuit technique [Shoval 92]; systematic offset minimization circuit [Dowlatabadi 95]; and by using the voltage gain in a feedback loop [Chan 00] to modify the op-amp circuit, minimization of the input offset of op-amp may be achieved.

- Existing technique like CMOS bandgap voltage references [Chin 91] may be employed to obtain the precise reference voltages.

- To design the practical circuits of Test Control Unit, Scan paths, test output unit and associated circuits with BIST facilities such that the whole SOC is testable.

Finally, with the help of CAD tools from Cadence a FRWC chip is proposed to be fabricated in order to evaluate the effectiveness and performance of the FRWC BIST technique in a practical manner.

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