Advanced Control of SPWM dc/ac Inverters

by

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CERTIFICATE OF ORIGINALITY

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Abstract

of the thesis entitled 'Advanced Control of SPWM dc/ac Inverters'
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There is a growing need for sinusoidal inverters that can supply power to nonlinear loads and still maintain precise regulation of the output voltage magnitude, phase and total harmonic distortion (THD). Also, with the ever-increasing demand for power, UPS systems may have to be paralleled to form a multi-inverter system. A multi-inverter system can have many desirable features such as N+X redundancy operation, improved reliability, modularity and expandability.

This thesis studies the control methodologies that enable inverter systems to deal with nonlinear loads and be paralleled easily with high performance. Starting with a brief introduction to the basics of sinusoidal PWM inverter in Chapter 2, neural network (NN) control of the inverters is introduced in Chapter 3. Benefited from abilities of nonlinear functional mapping and fault tolerance, simulation and experiment results show superior performance of the proposed NN controller compared with a traditional PI controller. In Chapter 4 and 5, parallel operation of multi-inverters is discussed. An instantaneous average-current-sharing scheme is modeled and analyzed in Chapter 4. Based on the model established, some key issues of the parallel multi-inverter system are discussed, including stability of the current-sharing controller, impedance characteristics and voltage regulation. A full-state feedback controller for parallel multi-inverter systems based on optimal control methodology is presented in Chapter 5. Having a global view of the whole system, the proposed full-state feedback controller is easy to design. The robustness of the controller to the change of number of parallel inverters has also been investigated. The hardware implementation of the controller is simple. All modeling and theoretical analyses are verified by simulation and experiment results. Finally, suggestions for future research are addressed.

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Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Motivation

As modern society continues to increase its reliance on electrical and electronic equipment, there is a growing demand for a clean and reliable ac power to keep these devices operating regardless of weather, location or other conditions adverse to nominal utility power supply [1]. Traditionally, backup generators have been used to meet this need, and they continue to be installed in great numbers in hospitals, data processing centers, recreational & emergency vehicles, communication centers and the like. However, backup generators have an unavoidable lag of several seconds from the beginning of a power outage to the time that the generator can be started and switched in. While this was once a minor inconvenience, there now exists a growing class of "critical loads" that demand uninterrupted power at all times. Such loads include:

- Computer Systems
- Security Systems
- Communication Systems
- Hospital Equipment

- Critical Process Control Equipment

As such, power electronic inverters have been developed that can synthesize sinewave ac voltage from a backup power source, traditionally a bank of batteries. These inverters can be activated almost instantaneously in case of a power outage, and thus can provide uninterrupted ac power. Hence, the phrased "Uninterruptible Power Supply" (UPS) was coined.

Furthermore, UPSs can protect their loads from disturbances of the mains supply. These disturbances can be divided into different categories [2]:

- Radio-frequency (rf) voltages,
- Voltage spikes,
- Harmonic voltages,
- Dips, surges, brown-outs, flickers and failure.

As an alternative of the main supplies, UPSs are required to produce constant sinusoidal output voltage with minimum Total Harmonic Distortion (THD) for a wide load range: from resistive to reactive (inductive or capacitive), and from linear to nonlinear. At the same time, fast transient response, good stability and high reliability are also required.

Nowadays, more and more power electronic converters are employed to provide electrical power. Most of converters use diode rectifiers (followed by a filtering capacitor) as an interface with the mains supply, which draws non-sinusoidal current with high spike when fed with a sinusoidal voltage. When serving the nonlinear loads, like diode rectifiers, UPSs should have much higher dynamic stiffness and much lower output impedance. It is becoming more difficult (but essential) to design a suitable

controller for a dc/ac inverter, the core of a UPS, to maintain a sinusoidal voltage, especially for the cases of nonlinear loads.

Parallel operation is tendency of power supplies [3]. The power capability of the system can be easily expanded by adding more modules into system. Reliability, redundancy and modularity are also improved by parallel operation. Technologies for Parallel operation of dc/dc converter have been developed for last two decades. Some successful technologies [4] and mature commercial products [5] provide very convenient method to parallel connect converters with high performance.

As a backup power supply system, the reliability and redundancy of the UPSs are remarkable. Parallel operation can provide a good solution to improve reliability and redundancy. More and more researchers put their focuses on parallel operation of UPSs.

1.2 Background

As the technology of power electronics has progressed over the years, so has the technology of UPS inverters: as far back as 1981 there were UPS systems referred to as "5th generation". A complete history of UPS inverter development is beyond the scope of this thesis. In general, as better power electronic switching devices and techniques became available, they were subsequently incorporated into UPS inverter designs. It should be noted that UPS inverter designs incorporated ferroresonant transformers, though quite prevalent in the past, will not be considered as they are becoming obsolete. It should also be noted that the scope of the research reported in this thesis is limited to the ac output voltage synthesis and control of UPS-style inverters. Other issues pertaining to UPS inverter systems, such as battery maintenance, startup-shutdown, line-synchronization, etc. will not be addressed.

Today, the vast majority of UPS inverters incorporate transistors (IGBTs or MOSFETs). They are of the voltage source inverter (VSI) type, with a DC link supplying voltage to the inverter bridge. These types of UPS inverters can be classified into two broad categories based on their output voltage synthesis:

1). **Stepped-wave output**: Here a sinusoidal waveform is approximated by a series of voltage "steps". The RMS magnitude of the output voltage is usually controlled by varying the width, or duty-cycle, of the steps. The peak of the output voltage steps are determined by the dc link (or bus) voltage level [6].

2). **Sinewave output**: These inverters produce a "smooth" sinusoidal output voltage by passing the output of the inverter bridge through an LC filter. To minimize the size and rating of the filter components, the inverter bridge is usually pulse-width-modulated (PWM) at a switching frequency much higher than the fundamental of the synthesized output voltage. Output voltage control can be controlled either on an RMS or instantaneous basis [7].

Early UPS inverters were dominated by the stepped-wave design (also referred to as "quasi-sinewave"). They were simple to implement and had a high efficiency due to the low switching frequency. The drawbacks of these inverters included poor output voltage quality, as measured by THD, and rather slow response to load transients. While many types of loads (such as lighting and heating) function properly with stepped-wave inverters, the harmonics of the output voltage waveform tend to heat up motors, and adversely affect some other types of electronic equipment. Today, these types of UPS inverters are found mostly in low-cost systems where waveform quality is not a major concern.

As with all electronic equipment, better performance is continually being sought, and thus sinewave output UPS inverters are increasingly in demand. With advances in power electronic device performance, high-frequency PWM inverters can deliver up to 100KVA and beyond [8]. These types of sinewave inverters are compatible with all types of ac-powered equipment. They can also offer fast-speed regulation and low THD (better than what is generally supplied by the utility). In addition, since the inverter comprises an electronic converter, a much wide range of dc bus voltage can be utilized. This thesis is concerned with Sinusoidal Pulse-Width-Modulated (SPWM) UPS inverter systems with LC filters intended for sinewave output voltage waveforms, as these are seen to be the most dominant design for current and future UPS systems.

In a SPWM inverter, the switching frequency is usually several orders higher than the fundamental frequency of the output voltage. The dynamics of the switching can therefore be ignored. An averaged time-continuous model of the SPWM inverter can be easily derived. Such a model is quite precise within half the switching frequency. Generally, the frequency domain analysis is applied to the controller design of SPWM inverters. The Bode plots are powerful tools, which make system analysis and controller evaluation visable and straightforward. The derived controller, mostly PI controllers, have been widely used in SPWM inverters. However, because the design is based on the linearized model under a specific loading condition, the performance of PI controllers is often far from ideal for extreme loading conditions. For example, under nonlinear loading conditions, PI controllers often have poor ability to maintain a low THD in the output voltage.

Parallel operation of the UPS inverters can bring many desirable advantages. However, for the following reasons, the parallel operation of voltage source inverters is

very sensitive to disturbance, and therefore extremely careful consideration should be given when planning and designing the system [9].

- An inverter has an overload capacity of only 150-200 percent, and if the output current exceeds this limit, even for a fraction of a cycle, this will result in a commutation failure or a damage of the switching device.
- Because of its low-impedance and quick-response characteristics, the inverter output current changes very rapidly and thereby easily reaches an overload condition.
- There are many different configurations of inverter circuits with various operating principles, and each configuration has its own characteristics and weakness.

Therefore, some addition mechanisms are required to deal with the current balance among the inverters. However, not much research work had been reported on the parallel operation of dc/ac inverters.

1.3 Objectives

The performance of the UPS inverters under nonlinear loads is quite essential since more and more electrical loads are becoming nonlinear and generate harmonics. However, the design of most controllers for UPS inverters is based on linearized models. Although linear models make the design quite simple and direct, the performance of the systems degrades in a wide load range. The intelligent control, like fuzzy logic or neural networks, shows its advantages to deal with nonlinear systems, and attracts efforts on research and development. In this thesis, neural networks are applied to the control of UPS inverters. The focuses are put on trying to find a simple and low-cost solution of

neural-network controller for the UPS inverter, which is expected to have superior performance under nonlinear loading conditions.

Due to the shortage of knowledge of parallel multi-inverter system, when we design such a system, some questions arise. Can we apply the methodology of design of a single inverter to the design of a parallel multi-inverter system? Are the characteristics of the inverters changed when they are paralleled together? How to model a parallel multi-inverter system? Can we predict the performance of the parallel multi-inverter system when we design the controllers? This thesis tries to answer these questions.

1.4 Outline of the Thesis

Chapter 2 gives a brief introduction to the basics of SPWM dc/ac inverters. The circuit topology, PWM operation, and linear model of the SPWM dc/ac inverters are addressed. The linear model developed will be used in other chapters to analyze and synthesize the SPWM dc/ac inverters.

In Chapter 3, neural-network-based control is introduced into SPWM dc/ac inverters. The proposed neural-network controller is benefited from the nonlinear-functional-mapping ability of the neural networks. Design procedures of the proposed controller are given. Simulation and experimental results show its superior performance to a PI controller with optimized parameters. The implementation of the analogue neural-network controller using integrated circuits is also discussed.

In Chapter 4, a parallel multi-inverter system with instantaneous average-current-sharing scheme is discussed. A model that describes the whole system's performance is built. Based on this model, some key issues of parallel multi-inverter systems are discussed, including stability of the current-sharing controller, impedance characteristics

and voltage regulation. Three experimental 110Vac/1.1KVA inverters are built and paralleled to verify the theoretical predictions.

Chapter 5 further discusses the parallel multi-inverter system. The optimal theory is employed to design a state feedback controller for the system. The robustness of the controller to the change of the number of parallel inverters has also been investigated. Simulation and experimental results are provided.

Finally, Chapter 6 presents conclusions and discusses opportunities for further research.

Chapter 2

Basics of Sinusoidal PWM dc/ac Inverters

2.1 Introduction

As mentioned in Chapter 1, the scope of this thesis is limited to single-phase high frequency SPWM voltage source inverters with LC output filters. In general, this type of sinusoidal inverter is well suited for producing tightly regulated sinusoidal output voltage waveforms. Since most modern sinusoidal inverters are operated above the audible range (≥18kHz) to alleviate human discomfort (as well as to reduce filter component size), the inverter harmonics have frequencies well above that of the output voltage fundamental, and are easily filtered out. This chapter presents a brief introduction to the basics of sinusoidal PWM inverters. The popular circuit topologies, PWM operation and linearized models of inverters are included.

2.2 Topologies of a dc/ac Inverter

A sinusoidal inverter typically consists of a dc power source, a PWM inverter and an LC filter, as shown in Figure 2.1. The inverter, which is the core of the system, chops

the dc input into a series of PWM pulses according to modulation signal u_m. The function of the second-order LC filter is to remove the high frequency components of the chopped output voltage u_i. R_f represents the resistance of the filter inductor. The effective series resistance (ESR) of the filter capacitor is ignored since it only has a small effect within the frequency range concerned. The dc power source is considered as an ideal constant-voltage supply. The load shown in Figure 2.1 can be of any type: resistive, inductive, capacitive or nonlinear.

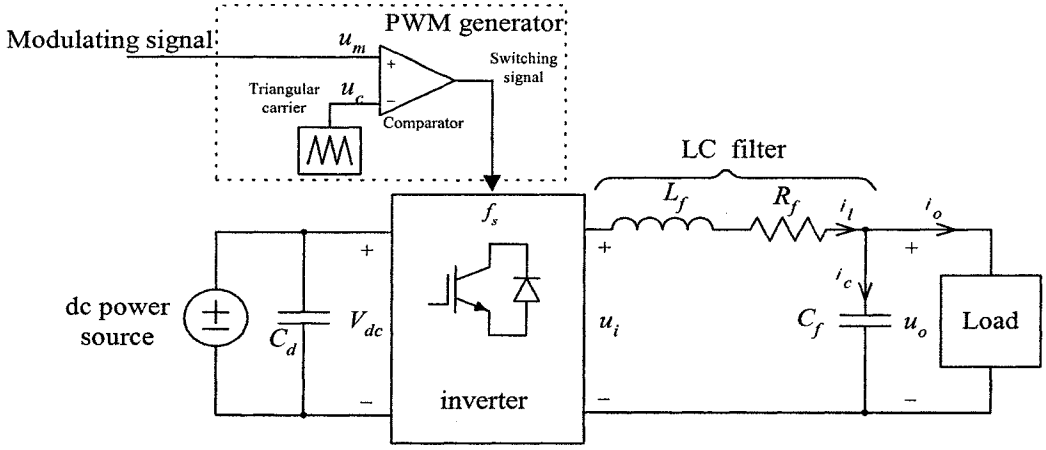


Figure 2.1 Single-phase Sinusoidal PWM inverter.

The most obvious and popular configurations for the inverter, shown in middle of Figure 2.1, are half-bridge and full-bridge inverters [10][11]. The following two sub-sections give a brief introduction to both of them.

2.2.1 Half-Bridge Inverter

Figure 2.2 shows a half-bridge inverter. Here, two equal capacitors are connected in series across the dc input. Their junction is at a midpotential, with a voltage V_{dc} across each capacitor. Sufficiently large capacitances should be used such that it is reasonable to assume that the potential at point O remains essentially constant with

respect to the negative dc bus N. The two switches, S_1 and S_2, are switched in such a way that when one of them is on, the other is off. The two switches are never turned on simultaneously. In practice, they can also be both off for a short time interval (known as the blanking time) to avoid short circuit of the dc input. Because of the anti-parallel diodes of the switches, when a switch is turned on, it may or may not conduct a current, depending on the direction of the output current i_l. Therefore, a half-bridge inverter such as shown in Figure 2.2 can operate in all four quadrants of the i_l-u_l plane, and the power flow through the inverter can be in either direction.

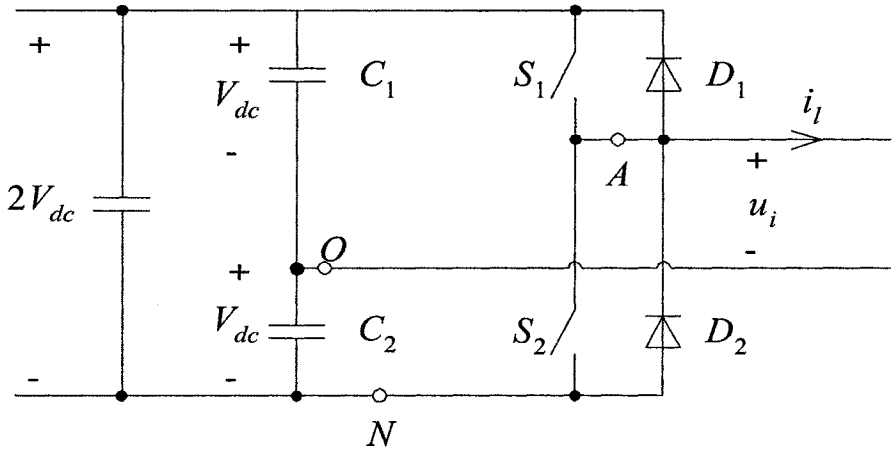


Figure 2.2 Half-bridge inverter.

2.2.2 Full-Bridge Inverter

A full-bridge inverter is shown in Figure 2.3. This inverter consists of two legs, A and B. The number of switches is twice that of the half-bridge inverter. Full-bridge is the preferred arrangement for higher power applications. With the same output voltage, the minimum dc input voltage of the full-bridge inverter is half that of the half-bridge inverter. This implies that for the same power, the voltage stresses of the switches are

one-half of those for a half-bridge inverter. At high power levels, this is a distinct advantage.

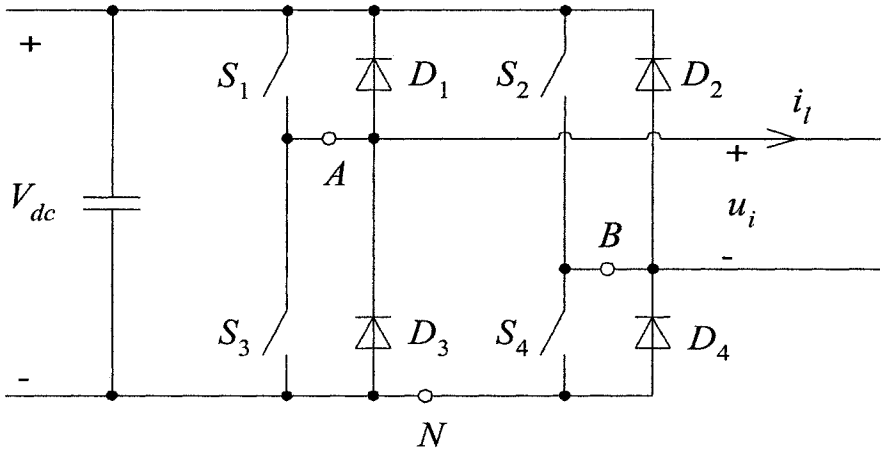


Figure 2.3 Full-bridge inverter.

2.3 PWM Operation of Inverters

Pulse-width-Modulation (PWM) provides a way to decrease the Total Harmonic Distortion (THD) of load current. A PWM inverter output, with some filtering, can meet THD requirements easily. The unfiltered PWM output will have a relative high THD, but the harmonics will be at much higher frequencies, making filtering easier.

In PWM, the amplitude of the output voltage can be controlled by the modulating waveform. Reduced filter requirements for harmonics and easier control of the output voltage amplitude are two distinct advantages of PWM. Disadvantages include more complex control circuits for the switches and increased losses due to high frequency switching.

The control of the switches for sinusoidal PWM output requires (1) a reference signal, sometime called a modulating or control signal (u_m as shown in Figure 2.1),

which is a sinewave; and (2) a carrier signal (u_c as shown in Figure 2.1), which is a triangular wave that controls the switching frequency.

Before discussing the PWM behavior, it is necessary to define a few terms. The triangular carrier u_c in Figure 2.1 has amplitude of $\hat{U}_c$ and frequency of f_s, which establishes the switching frequency of the inverter. The modulating signal u_m is used to modulate the switch duty ratio and has a frequency of f_1, which is the desired fundamental frequency of the inverter voltage output. The amplitude modulation ratio m_a is defined as

$$m_a = \frac{\hat{U}_m}{\hat{U}_c} \tag{2-1}$$

where $\hat{U}_m$ is the peak amplitude of the modulating signal. The amplitude $\hat{U}_c$ of the triangular carrier is generally kept constant.

The frequency modulation ratio m_f is defined as

$$m_f = \frac{f_s}{f_1} \tag{2-2}$$

Bipolar and unipolar switch schemes are introduced in following two sub-sections.

2.3.1 Bipolar Switching

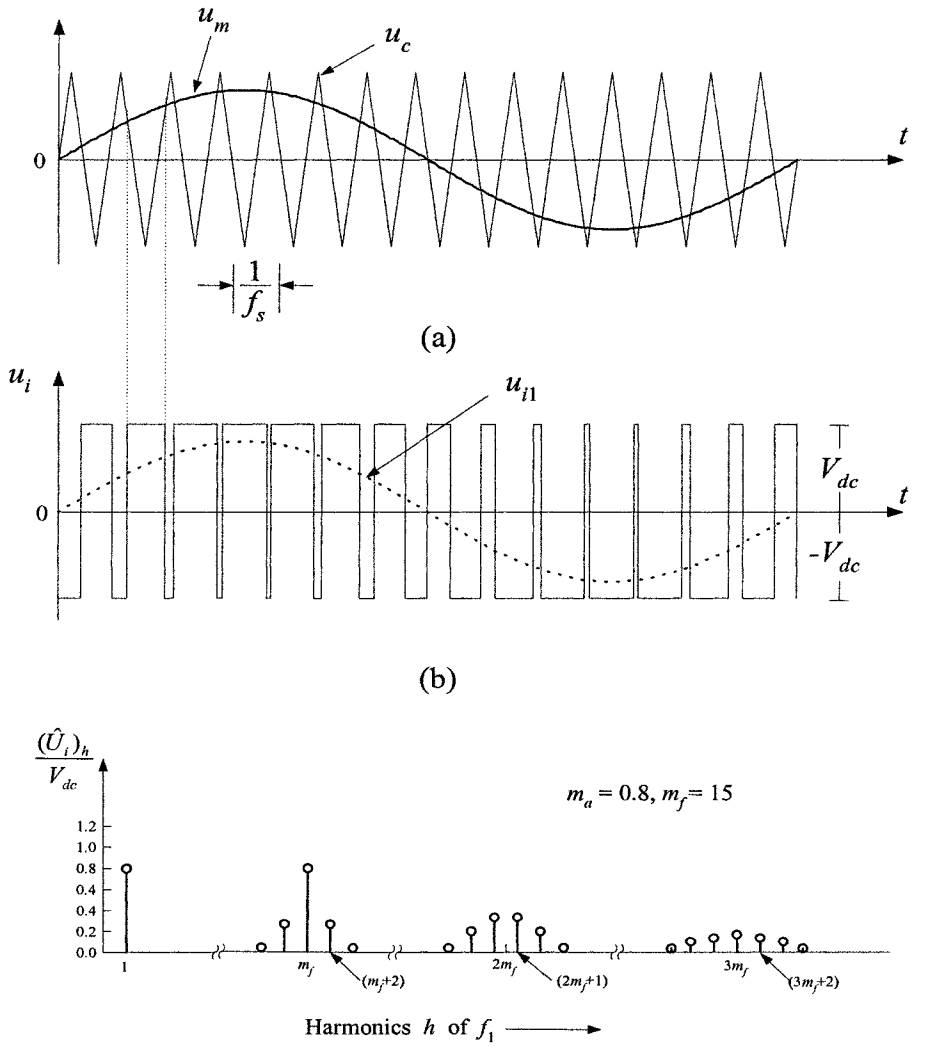


Figure 2.4 Bipolar pulse-width modulation.

Figure 2.4 illustrates the principle of sinusoidal bipolar pulse-width modulation. Figure 2.4a shows a sinusoidal reference signal and a triangular carrier signal. When the instantaneous value of the sine reference is larger than the triangular carrier, the output is at $+V_{dc}$, and when the reference is less than the carrier, the output is at $-V_{dc}$ as shown in Figure 2.4b.

The fundamental of the output voltage u_i of the inverter is a sinusoidal waveform, whose magnitude and frequency can be controlled by the reference (modulating signal). This version of PWM is bipolar because the output alternates between the positive and the negative of the dc supply voltage.

The switching schemes that will implement bipolar switching using the half-bridge inverter of Figure 2.2 and the full-bridge inverter of Figure 2.3 are

$u_m > u_c$: S_1 on ; $u_i = V_{dc}$,

$u_m < u_c$: S_2 on ; $u_i = -V_{dc}$.

and

$u_m > u_c$: S_1 and S_4 on ; $u_i = V_{dc}$,

$u_m < u_c$: S_2 and S_3 on ; $u_i = -V_{dc}$.

The harmonic spectrum of u_i under the bipolar PWM switching is shown in Figure 2.4c, where the normalized harmonic voltages $\frac{(\hat{U}_i)_h}{V_{dc}}$ are plotted. The harmonics in the inverter output voltage waveform appears as sidebands, centered around the switching frequency and its multiples, that is, around harmonics m_f, $2m_f$, $3m_f$, and so on. Therefore, if m_f is large, the harmonics of the output voltage will appear at high frequency, the size of filter can be reduced significantly.

2.3.2 Unipolar Switching

Unipolar switching is for full-bridge inverter only, because the switches in the two legs of the full-bridge inverter of Figure 2.3 are not switched simultaneously as in the bipolar switching scheme. Here, the legs of A and B of the full-bridge inverter are controlled separately by comparing u_c with u_m and $-u_m$, respectively.

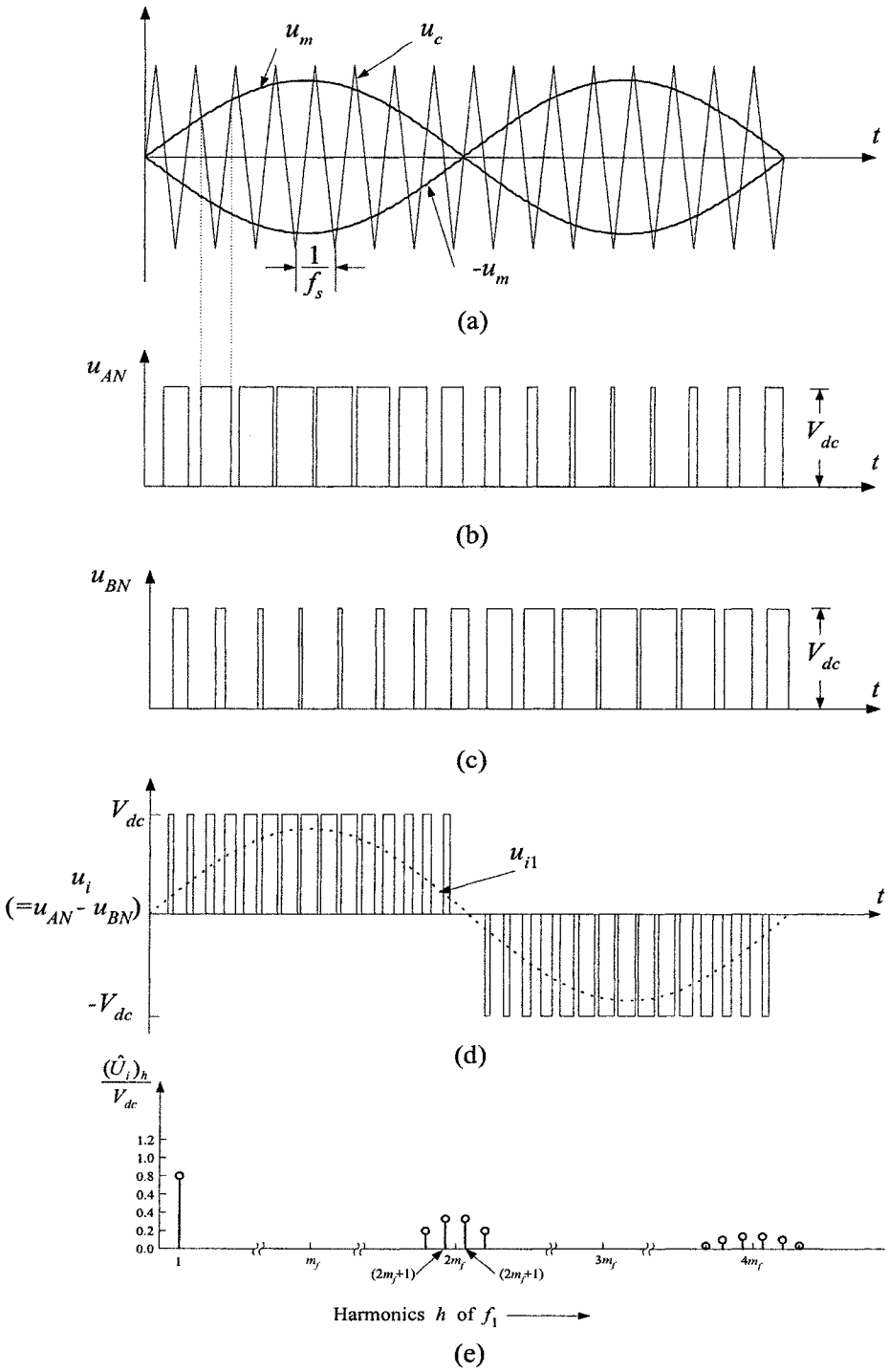


Figure 2.5 Unipolar pulse-width modulation.

As shown in Figure 2.5a, the comparison of modulating signal u_m with the triangular carrier u_c results in the following switching scheme in leg A:

$u_m > u_c$: S_1 on and $u_{AN} = V_{dc}$,

$u_m < u_c$: S_4 on and $u_{AN} = 0$.

The output voltage of inverter leg A with respect to the negative dc bus N is shown in Figure 2.5b. For controlling the leg B switches, $-u_m$ is compared with the same triangular carrier u_c, which yields the following:

$(-u_m) > u_c$: S_2 on and $u_{BN} = V_{dc}$,

$(-u_m) < u_c$: S_3 on and $u_{BN} = 0$.

Because there are antiparallel diodes across the switches, the voltages at u_{AN} and u_{BN} are independent of the direction of the output current i_l. The waveforms of Figure 2.5 show that there are four combinations of switch on-states and the corresponding voltage levels:

1. S_1, S_4 on: $u_{AN} = V_{dc}$, $u_{BN} = 0$; $u_i = V_{dc}$
2. S_2, S_3 on: $u_{AN} = 0$, $u_{BN} = V_{dc}$; $ui = -V_{dc}$
3. S_1, S_2 on: $u_{AN} = V_{dc}$, $u_{BN} = V_{dc}$; $u_i = 0$
4. S_3, S_4 on: $u_{AN} = 0$, $u_{BN} = 0$; $u_i = 0$

In this type of PWM scheme, when a switching occurs, the output voltage changes between zero and $+V_{dc}$, or between zero and $-V_{dc}$. For this reason, this type of PWM scheme is called PWM with a unipolar voltage switching, as opposed to the PWM with bipolar (between + V_{dc} and $-V_{dc}$) voltage switching scheme, as described in last sub-section. This scheme has the advantage of "effectively" doubling the switching frequency as far as the output harmonics are concerned, compared to the bipolar voltage-switching scheme. Figure 2.5e shows the harmonic spectrum of the output voltage u_i, where the lowest harmonics (in the idealized circuit) appear as sidebands of twice the switching frequency.

There is yet another unipolar switching scheme which has one pair of switches operating at the carrier frequency and another pair operating at the ac reference frequency, thus having two high-frequency switches and two low-frequency switches [11]. The switching losses of those two switches with low switching frequency are greatly reduced. Furthermore, they can be implemented using slow power semiconductor devices (e.g., GTO thyristors), which usually have lower conduction losses than the corresponding fast power semiconductor devices (e.g., MOSFET's).

2.4 Linear Model of a Sinusoidal dc/ac Inverter

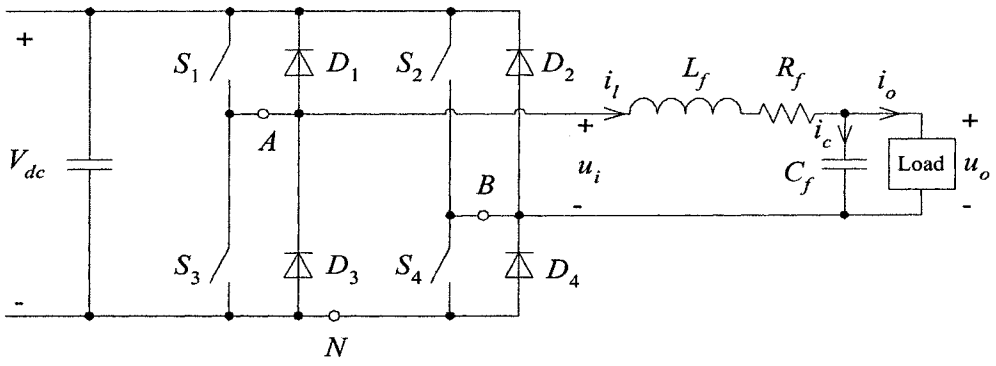


Figure 2.6 Full-bridge inverter with LC filter.

Figure 2.6 shows a full-bridge inverter with LC filter. Assuming that the bipolar PWM scheme is used, the output voltage u_i of the bridge changes between $+V_{dc}$ and $-V_{dc}$. With the foregoing discussion, a switching function is defined as follows:

$$S^* = \begin{cases} 1 & u_m > u_c : S_1 \text{ and } S_3 \text{ on} \\ 0 & u_m < u_c : S_2 \text{ and } S_4 \text{ on} \end{cases} \tag{2-3}$$

Therefore, the output voltage u_i of the bridge can be described as

$$u_i = V_{dc}(2S^* - 1) \tag{2-4}$$

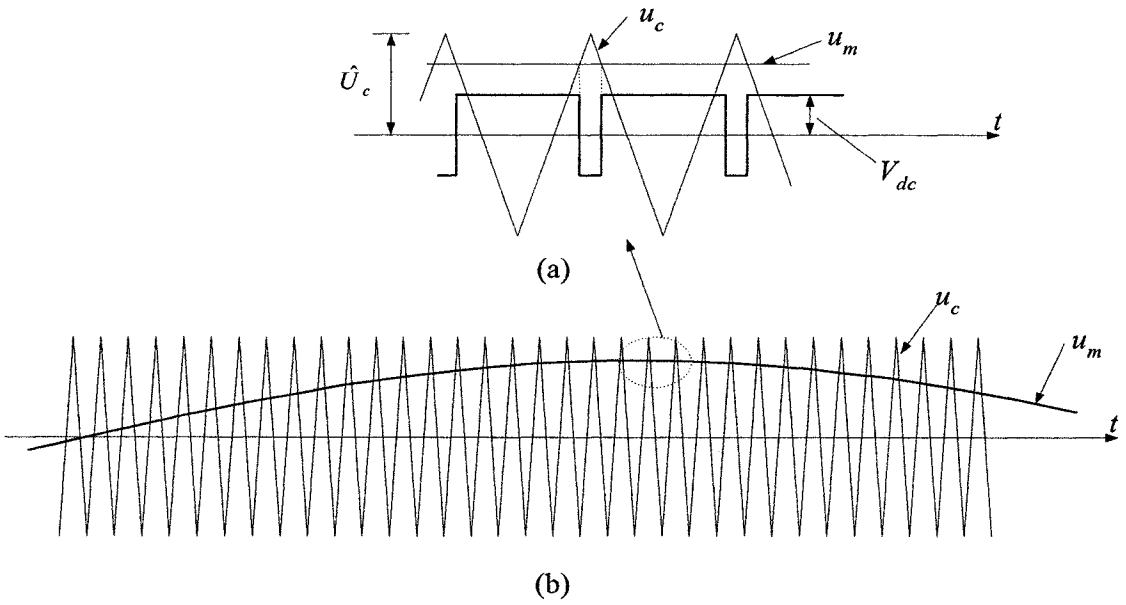


Figure 2.7 Sinusoidal PWM.

Let us assume (though this assumption is not necessary) that the carrier frequency f_s is much high than the frequency f_1 of the modulating signal u_m, meaning that the frequency modulation ratio m_f is large, as shown in Figure 2.7b. Therefore, u_m can be considered as constant over a switching time period. Consequently, for $m_a \leq 1$ ($\hat{U}_m \leq \hat{U}_c$), the discontinuous switching function S^* can be replaced by its time-dependent duty cycle $d(t)$ [13], as

$$d(t) = \frac{1}{2}\left(\frac{u_m(t)}{\hat{U}_c} + 1\right) \tag{2-5}$$

where $\hat{U}_c$ is amplitude of the triangular carrier.

By inserting (2-5) as S^* into (2-4), an averaged time-continuous model of the sinusoidal PWM inverter can be obtained as

$$u_i = V_{dc}\frac{u_m(t)}{\hat{U}_c} = Mu_m(t) \tag{2-6}$$

where $M = \frac{V_{dc}}{\hat{U}_c}$ is the modulating gain. Therefore, the bridge inverter in Figure 2.6 can be modeled as a controlled voltage source with the gain of M, as described in (2-6). The equivalent circuit of the averaged sinusoidal PWM inverter with LC filter is shown in Figure 2.8.

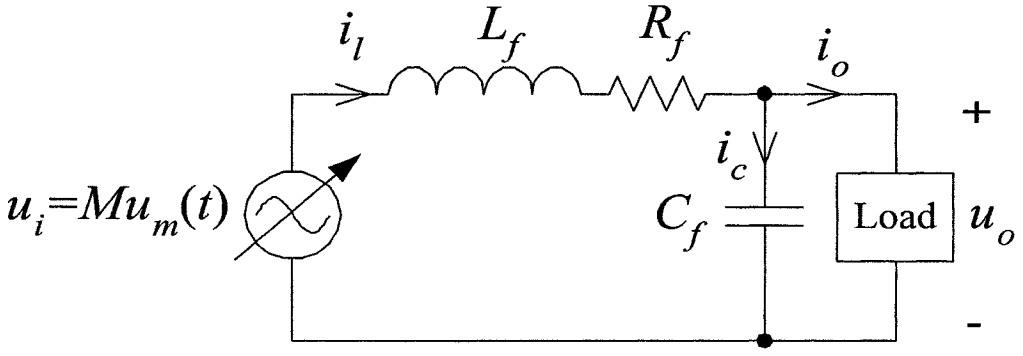


Figure 2.8 Equivalent circuit of the averaged sinusoidal PWM inverter.

Thus, we can use state-space function to describe the sinusoidal PWM inverter as (2-7). Here, the load is assumed to be a pure resistance, represented by R_L.

$$\frac{d}{dt}\begin{bmatrix} i_l \\ u_o \end{bmatrix} = \begin{bmatrix} -\frac{R_f}{L_f} & -\frac{1}{L_f} \\ \frac{1}{C_f} & -\frac{1}{R_L C_f} \end{bmatrix}\begin{bmatrix} i_l \\ u_o \end{bmatrix} + \begin{bmatrix} \frac{M}{L_f} \\ 0 \end{bmatrix} u_m \tag{2-7}$$

By applying Laplace transform, a linearized model can be easily derived as shown in Figure 2.9.

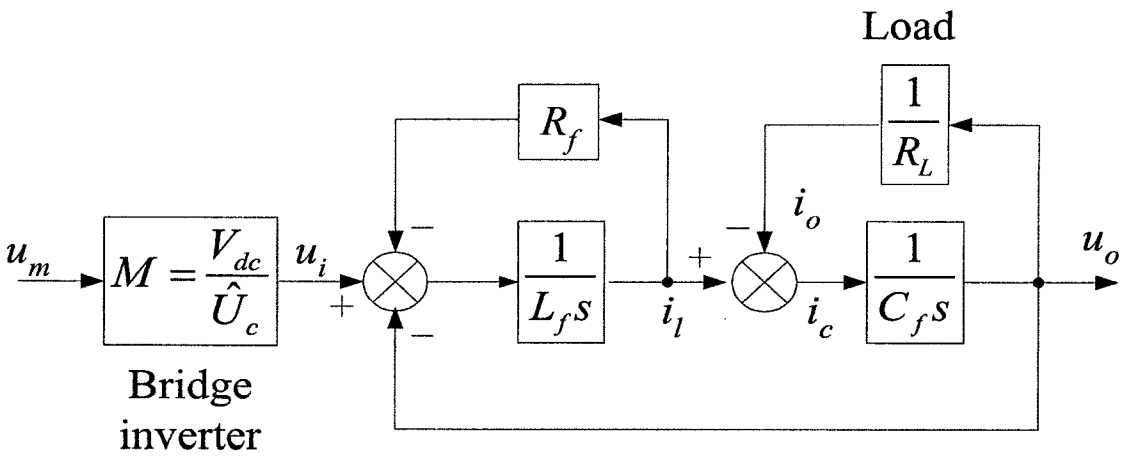


Figure 2.9 Linearized model of sinusoidal PWM inverter.

2.5 Summary

In this chapter, the basics of the sinusoidal PWM inverter are introduced. The focus is put on high frequency PWM, where the frequency of the triangular carrier is much higher than that of the modulating signal. The popular circuit topologies and PWM switching schemes are discussed briefly. Moreover, a linearized model of the sinusoidal PWM inverter is established. This model will be used in the later parts of the thesis.

Chapter 3

Neural Network Based Control for SPWM Inverter

3.1 Introduction

The objective of UPS inverters is to provide a pure sinusoidal voltage with constant frequency and constant amplitude. Various controllers were used to achieve regulation. The controllers can be classified into two groups: analog-based and digital-based.

Most of the analog-based controllers were designed based on linearized model and traditional frequency-domain analysis. Some multiple-feedback-loop control strategies were proposed in [14][15]. Such schemes sense the current in the inductor (or capacitor) of the LC filter as the control signal of an inner feedback loop. An outer voltage feedback loop is incorporated to ensure a sinusoidal output voltage. Owing to the introduction of the inner current feedback loop, the output impedance of the inverter filter is decreased and the dynamic stiffness enhanced. The controlled inverter can produce a satisfactory sinusoidal output voltage within a certain load range. However, uniform performance cannot be obtained under extreme loading conditions, and THD

increases significantly when there is a nonlinear load. In addition, such schemes are analog-based. As a result, they have all the drawbacks of analog circuits, such as limited accuracy, uncompensated thermal drift, and need of recalibration.

Digital control schemes are all realized by software. They bring more flexibility than analog schemes. Microprocessor-based deadbeat control scheme was proposed in [16][17]. In this scheme, the capacitor voltage and its derivative (or capacitor current) are used to calculate the duration of the ON/OFF state of the switching devices, so that the capacitor voltage is forced to be equal to the reference voltage at each sampling instant. Although this technique can achieve good performance when the switching frequency is low (a few kHz), it has two major disadvantages: 1) high sensitivity to parameter variations; 2) high THD under nonlinear load conditions.

Modern Digital Signal Processors (DSP) are capable of executing over 50 million instructions per second (MIPS). Some complicated control algorithms, which are almost impossible to be realized by analog circuitry, can be flexibly implemented by DSP. In addition, there are many advantages in using DSP, e.g. the system parameters are free from the effects of aging and temperature drift. References [18]-[21] proposed different DSP-based control algorithms of inverters. However, although these algorithms could achieve good transient response and low THD under nonlinear loading conditions, the high computation demand increases the implementation difficulty as well as expense.

Numerous advances have been made in developing intelligent system, some inspired by biological neural networks. Researchers from many scientific disciplines are designing artificial neural networks to solve a variety of problems in pattern recognition, prediction, optimization, associative memory, and control. Conventional

approaches have been proposed for solving these problems. Although successful applications can be found in certain well-constrained environments, none is flexible enough to perform well outside its domain. Neural network (NN) provides exciting alternatives, and many applications could benefit from using them. An NN is a massively parallel computing systems consisting of an extremely large number of simple processors with many interconnections that simulates a real biological brain system. Therefore, the NN possesses the features of distributed representation and computation, learning ability, adaptability, inherent contextual information processing, and fault tolerance [22].

Power electronic systems are nonlinear indeed. Although there are many approaches to model power electronic circuits as low frequency behavior models [23] and hence various control methodologies can be applied to power electronic systems, the performance of the system against nonlinear loads is still poor. With specific reference to NN in control the following characteristics and properties of NN are important [24]:

- Nonlinear system,
- Parallel distributed processing,
- Hardware implementation,
- Learning and adaptation,
- Data fusion,
- Multivariable system.

From the control theory viewpoint, the ability of the NN to deal with nonlinear systems is perhaps most significant. This stems from its theoretical ability to

approximate arbitrary nonlinear mapping. The NN is, thus, very attractive for electronic to tackle strong nonlinearity of power electronic systems. It has already been employed in various control and signal processing applications in power electronics [25]-[27].

The NN is employed to perform waveform estimations of power electronics. Due to its strong abilities of parallel processing and data fusion, the NN is successfully applied to estimate distorted waveform generated by power electronic circuits [28]-[31]. Harmonic estimation or prediction also benefit from the NN [32]-[36].

In the control of dc/ac inverters, the NN has been introduced in the current control of inverters for ac motor drives [35]-[39], where the NN receives a phase-current error and generates PWM logic signals to drive the inverter switches. [40]-[42] presented a neural network application in the harmonic elimination of PWM inverter where the NN replaced a large and memory-demanding look-up table to generate the switching angles of the PWM inverter for a given modulation index.

Many architectures of NN have been reported. Although they have different elements and connections, they can be classified into two categories: dynamic (feedback, recurrent) and static (feedforward). Dynamic networks have feedback connections, which produce several stable points in networks. Dynamic networks are vital in many applications, like pattern recognition, signal processing and optimization. Static networks may have more than one layer. However, a neuron in one layer receives inputs only from neurons in the previous layer (or, in the case of the first layer, from the network input). The connection of several layers gives the possibility of more complex nonlinear mapping between the inputs and outputs. A number of results have been published showing that a feedforward network of multi-layer type can approximate arbitrarily well a continuous function. To be specific, it is proved that a continuous function can be arbitrarily well approximated by a feedforward network with only one

single internal hidden layer [24]. With these properties, static (feedforward) networks have great application potential in the modeling and control of nonlinear systems.

The loading conditions of a SPWM inverter can be quite complicated. The range may cover linear and nonlinear regions. When we attempt to introduce NN control to an inverter, an obvious difficulty is that not all the loading conditions that the inverter may encounter can be included into the model. A complete model of the control objectives, therefore, cannot be established. If a dynamic NN were employed, it would be very hard to describe the prescribed equilibrium (or steady-state matching) in the network. Our attention naturally turns to static NN, which has the property of nonlinear functional mapping. Our idea is to present an almost-perfect teacher, which can perform very well in simulation under all loading conditions, to a static (feedforward) NN. The teacher is actually a database composed of idealized input-output patterns. The training of the NN is a classical supervised training problem. Training an NN using a set of input-output data from a nonlinear plant can be considered as a nonlinear functional approximation problem. The training can be performed either on-line or off-line.

In on-line training, since the weights and biases of the NN are adaptively modified during the control process, it has better adaptability to nonlinear systems. The most popular gradient decent algorithm is back propagation. It is attractive because it is stable, robust and efficient. However, the back propagation algorithm involves a great deal of multiplication. If implemented in software, it needs a very fast digital processor. If implemented in hardware, it results in a rather complex circuitry and expensive solution [43].

Possible alternatives of the back propagation are perturbation-based algorithms, such as weight perturbation [44], chain-rule perturbation learning [45] or random weight change [46]. In these algorithms, the weights are perturbed and the gradients are

evaluated from the errors generated (instead of calculating the derivatives in back propagation). They are feasible for analogue VLSI implementation [47]. However, in real-time control of the power electronic system, there are no desired outputs to be presented to the NN since we have no a priori knowledge about the loading conditions. We can employ an NN emulator to identify the system behavior in order to determine the output error of the NN controller [48], but this NN emulator also need to be pre-trained with data obtained from simulations or experiments. Therefore, in short, on-line training of the NN has better adaptability to the system, but at the cost of complicated computation and expensive implementation. Moreover, it is difficult to directly introduce on-line training into the control of UPS inverters. We consider that the on-line training of the NN does not fit the requirement of fast response of the real-time control of the UPS inverters.

Off-line training of the NN requires a large number of example patterns, which may be obtained through simulations. Although the weights and biases are fixed during the control process, the NN is a nonlinear system that has much better robustness than a linear system. Moreover, the forward calculation of the NN just involves addition, multiplication and sigmoidal-function waveshaping that can be implemented with simple and low-cost analogue hardware [49]. The fast response and low-cost implementation of the off-line trained NN are suitable for UPS inverter applications.

Simulations of an NN controller with off-line training for PWM inverter were reported in [50]. The NN learned the control law through simulations off-line. The inputs of the NN are time, present output voltage and last sampled output voltage. This NN may not have enough information to ensure a sinusoidal output voltage under various loading conditions. Moreover, only computer simulation, but no experimental results are reported.

In this chapter, an analogue NN controller with off-line training for UPS inverter applications is proposed. It is a trial of applying NN in a quite simply way. The proposed NN controller is of feedforward type with supervised training. Example patterns are obtained from two simulation models, one is a traditional multi-loop controller for linear loads, the other is an idealized load-current-reference controller specially for nonlinear loads. A selected feedforward NN is trained to model this controller using back propagation algorithm. After training, the NN is used to control the inverter on-line. Simulation results show that the proposed NN controller can achieve low THD under nonlinear loading conditions and good dynamic response under transient loading conditions. To further verify the performance of the proposed NN controller, a hardware inverter with an analogue NN controller (constructed using operational amplifiers and resistors) is built. A PI controller with optimized parameters is built as well for comparison purposes. Experiment results confirm the simulation results and show the superior performance of the proposed NN controller. A discussion about the integrated circuit implementation of the proposed analogue NN controller will also be given.

3.2 Feedforward Neural Network

Neural networks are interconnections of artificial neurons that tend to emulate the human brain. One structure of the artificial neuron is shown in Figure 3.1.

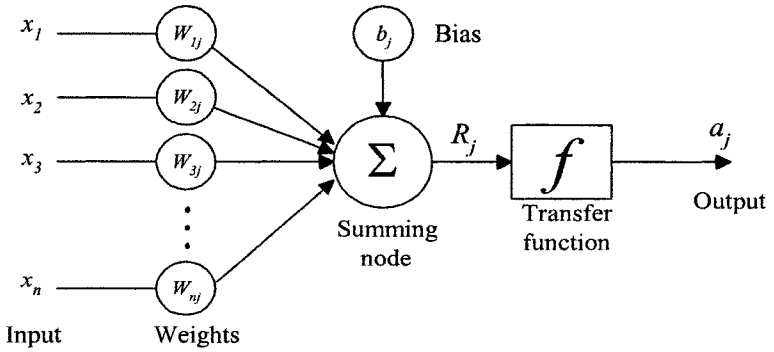


Figure 3.1 Structure of an artificial neuron.

Here the individual element inputs, x_1, x_2, x_3, ... x_n, are multiplied by weights, W_{1j}, W_{2j}, W_{3j}, ... W_{nj}, and the weighted values are fed to the summing node. The neuron has a bias b, which is summed with the weighted inputs to form the net input R_j. R_j is then used as the argument of the transfer function f. Therefore, the output of the neuron can be written as:

$$a_J = f(\sum_i W_{ij} x_i + b_j) \tag{3-1}$$

The transfer function can be of threshold type, sigmoid type, linear type and etc. Figure 3.2 shows the structure of a feedforward multi-layer network that has one hidden layer. The circles represent neurons, which have the structure as shown in Figure 3.1. A weight-adjustment feature is included when the back propagation is implemented. There can be more than one hidden layer. The number of hidden layers and the number of neurons on each layer depend on the complexity of the problem being solved and the desired accuracy.

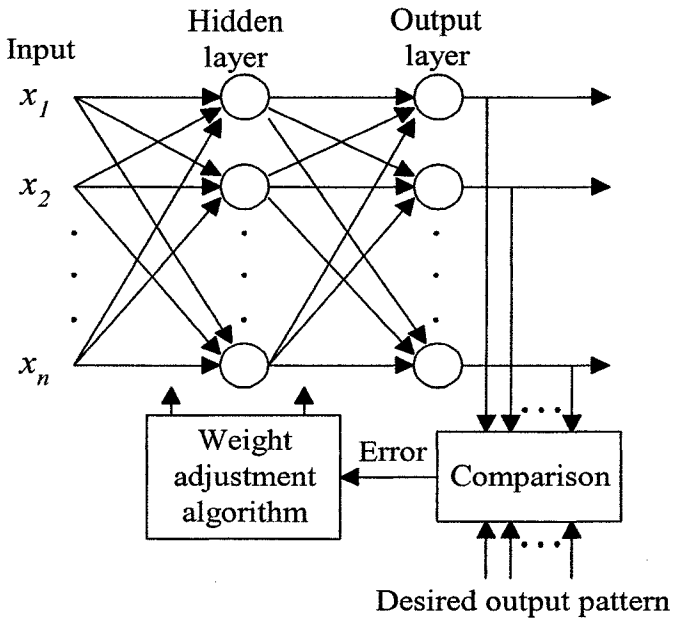


Figure 3.2 Structure of a two layer feedforward neural network showing the back propagation training.

Neural networks can compute very fast in a parallel and distributed manner, and can approximate any complicate nonlinear functions by multi-compounding simple nonlinear functions through a training process, which is realized by repeated adjustments of weights and biases. The back propagation training algorithm is the most commonly used one for feedforward neural networks [51]. It updates the network weights and biases in such a direction that the performance function, usually the sum of square errors, will decrease most rapidly. A properly trained network tends to give a reasonable output when presented with inputs that have never been seen. The training is usually done by an off-line computer simulation program using a large number of example patterns. The example patterns can be obtained from analysis, simulation or directly from experiments if the model is totally unknown.

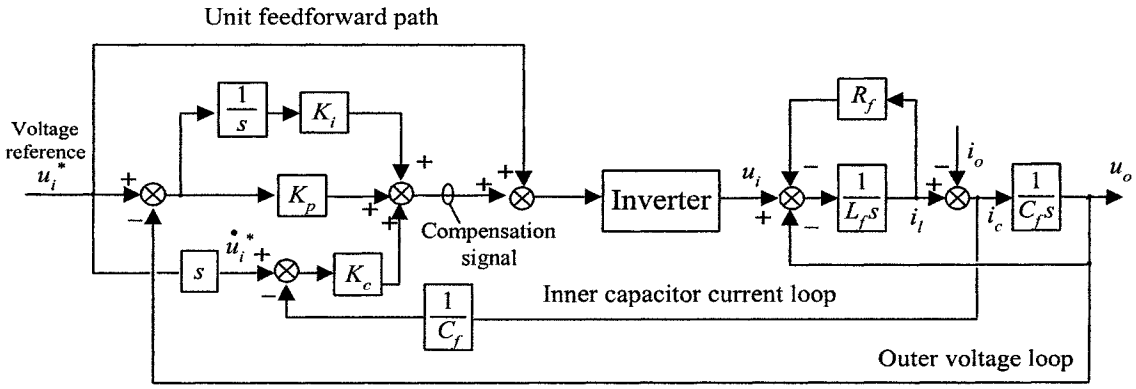
3.3 Proposed Neural Network Control of Inverter

To realize the proposed neural network control scheme on inverters, we have to present a large number of example patterns obtained under various loading conditions, and train the neural network properly to implement control law. Two controllers, one for linear loads, the other for nonlinear loads, are built and simulated using MATLAB [52] and SIMULINK [53].

3.3.1 Obtaining Example Patterns Under Linear Loading Conditions

The control scheme for linear loads is shown in Figure 3.3. Under linear load conditions (resistive, capacitive, or inductive), a multiple-feedback-loop control scheme can give good performance [14][15]. Based on the traditional frequency-domain theory, an inner capacitor-current feedback loop is designed to reduce the phase lag caused by the filter inductor, so that the gain and phase margin can be improved. An outer voltage feedback loop can easily enable the output voltage to track the reference with small error and low THD. Different from the strategy proposed in [14][15], there is a unit feedforward path from the reference voltage (shown at the top of Figure 3.3), which is found to have advantages of reducing steady-state error and providing a high tracking accuracy to the reference. Although it may cause large overshoot in the dynamic response, the drawback can be overcome by optimizing the parameters of the voltage feedback loop. The whole modulation signal to PWM generator can be divided into two parts, one is a sinusoidal signal, and the other is called compensation signal (as marked in the middle of Figure 3.5) produced by feedback loops. Another important reason to

introduce the voltage feedforward loop is that the neural network can then use compensation signal as its desired output. During the training process of the neural network, we find that, as compared with the method using the net modulation signal as the desired output, the method using the compensation signal can greatly improve effectiveness of the training.



Variables marked with * are reference variables

Figure 3.3 Multiple feedback loop control scheme to obtain example patterns under linear loads.

An inverter system with multiple-feedback-loop control scheme is modeled using MATLAB and SIMULINK. The full-bridge inverter is described by the following equation in SIMULINK:

$$u_i = \begin{cases} V_{dc} & (u_m \geq u_c) \\ -V_{dc} & (u_m < u_c) \end{cases} \tag{3-2}$$

where u_m is the instantaneous voltage of the modulating signal and u_c is the instantaneous voltage of the triangular carrier wave in the PWM. By using S-Function provided by SIMULINK, the full-bridge inverter can be easily built. The model of

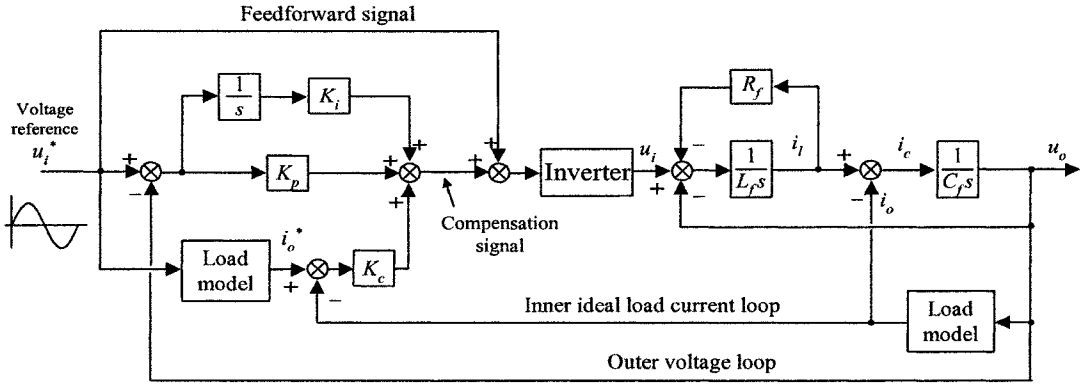
Figure 3.3 in SIMULINK and the S-Function described the full-bridge inverter are listed in Appendix A.

It should be noted that a controller with fixed parameters could not be good for all kinds of linear loads. Each load is associated with a set of optimal parameters. We design the parameters for each load using frequency-domain analysis to ensure enough stability margin and small steady-state error, and fine-tune the parameters in the simulations for good transient responses. The compensation signal as shown in Figure 3.3 is collected as the desired output of the neural network. The output voltage and output currents (including load current, capacitor current) of the inverter are collected as the inputs to the neural network. Dozens of example patterns are obtained from the simulation results under different load conditions and controller parameters.

3.3.2 Obtaining Example Patterns Under Nonlinear Loading Conditions

Many electrical loads nowadays are nonlinear. It is therefore essential to maintain the performance of a UPS inverter under nonlinear loading conditions. The nonlinear load in this Chapter is chosen to be a full-wave diode bridge rectifier with an output filter. The input current of the nonlinear load, namely the output current of the inverter, is usually non-sinusoidal with a rather large slope. The multiple-feedback-loop control scheme used under the linear loading conditions cannot perform satisfactorily. Thus, we should find another control scheme especially for nonlinear loads in order to obtain example patterns.

If the loading current of the inverter can be predicted, we can design a controller to keep trace of the output current. Following the control scheme used under the linear loading conditions, we change the inner capacitor-current loop to a load-current loop whose reference is obtained from an idealized load-current feedback control scheme (as shown in Figure 3.4), where a sinusoidal voltage is fed to a nonlinear load model to obtain a load-current reference. The actual load current is compared with this reference, and the error signal is used as the controller input. Although such a scheme is impossible to implement practically, it is actually an excellent teacher for the NN to learn to achieve the idealized performance. Figure 3.5 shows an example of the output waveform of an inverter controlled by an idealized load current feedback scheme. It can be seen that the performance of such a scheme is very good under nonlinear load conditions.



Variables marked with * are reference variables

Figure 3.4 Idealized load-current feedback control scheme to obtain example patterns under nonlinear loads.

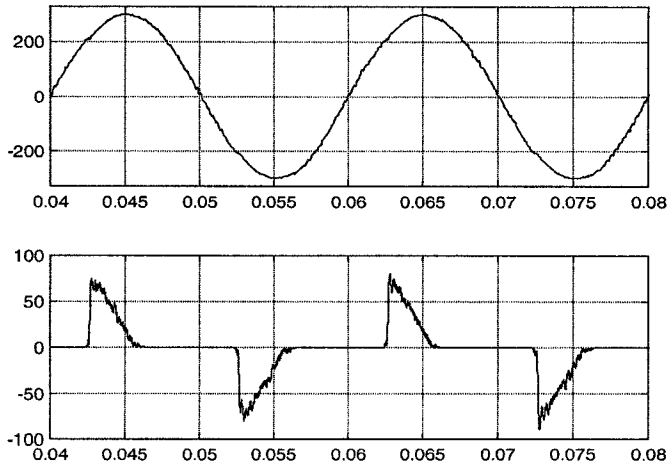


Figure 3.5 Example waveform of idealized load-current feedback control scheme.

A model of such an idealized load-current feedback control scheme is built using MATLAB and SIMULINK. The PWM full-bridge inverter is modeled in the way as mentioned in the last subsection. The core of modeling a full-wave diode bridge rectifier in MATLAB is the model of the power diode. We describe a diode using the following equation:

$$i_d = \begin{cases} 0 & u_d < 0.7 \\ (u_d - 0.7)/0.1 & u_d \geq 0.7 \end{cases} \tag{3-3}$$

where u_d is the instantaneous forward voltage across the diode and i_d is the instantaneous forward current in diode. Using (3-3), we can easily build a rectifier-type load using S-Function provided by SIMULINK. The model of Figure 3.4 in SIMULINK and the S-Function described the rectifier-type load are listed in Appendix A.

It should be noted that a fixed set of controller parameters (K_p, K_i, and K_c) is not good for every loading condition. Each loading condition has a set of optimal parameters, which can be determined from simulation that produce an output voltage

with a low THD and a small enough steady-state error. The output voltage, load current, and capacitor current of the inverter are collected as the inputs to the NN. The compensation signal (as marked in the middle of Figure 3.4), instead of the whole modulation signal, is collected as the desired output of the NN. By using this compensation signal as the desired output of the NN, more effective learning and better control performance can be achieved.

3.3.3 Training of the Neural Network

The off-line training of an NN needs a large database that contains input-output relationships. In the case of UPS inverters, the database should include the input-output patterns under all possible loading conditions. We classify the loading condition into two types, linear and nonlinear. The linear loads are further separated into resistive, capacitive, and inductive categories. The nonlinear loads are full-wave bridge rectifiers followed by a capacitor filter and a resistor load, in which we further classify them according to different output power ratings and different current crest factors. A new example pattern is obtained each time the load model is changed. The patterns for linear loads are obtained by running the simulation model shown in Figure 3.3, while the patterns for nonlinear loads are obtained by running the simulation model shown in Figure 3.4. The pattern database contains hundreds of patterns, in which two-thirds are for linear loading condition, and the other one-third is for nonlinear loading condition. it should be noted, in Figure 3.4, the nonlinear load models are involved into the controller. We can say that the example patterns contain our knowledge of the nonlinear loading conditions.

In the selection of an NN for the inverter, we believe the NN should be as simple as possible (with fewer inputs and fewer hidden nodes) so as to speed up the control process and to reduce the controller cost, but it should be sufficient enough to represent the required nonlinear functional mapping. The training of the NN is automated by a computer program that presents a randomly selected example pattern from the pattern database to the NN a large number of times (approximately one thousand and five hundred times). During each time, the weights and biases of the NN are updated using the back propagation algorithm to make the mean square error between the desired output and the actual output of the NN less than a predefined value.

The following is a summary of the design steps for the proposed NN controller for UPS inverter applications:

(1) Build the simulated model, as shown in Figure 3.3 (for linear loads) and Figure 3.4 (for nonlinear loads).

(2) For each of the loading conditions, tune the parameters of the controller to the optimal values. Then collect the output voltage, load current, and capacitor current as the inputs of the NN, and the compensation signal as the desired output of the NN. These patterns form a pattern database for the training of the NN.

(3) Select an NN structure that is simple and yet sufficient to represent the nonlinear functional mapping based on the pattern database.

(4) Train the NN using software tools (e.g. MATLAB with Neural Network Toolbox).

3.4 Simulation Results, Analogue Hardware Implementation and Experimental Results

To verify the ideas described above, we have designed an NN controller for a UPS inverter, whose parameters are listed in Table 3.1.

Parameter	Value	Units
Switching frequency, f_s	20	KHz
Nominal DC source voltage, V_{dc}	48	V
Rated Output Voltage	25	V_{rms}
Rated Output Frequency	50	Hz
Rated Output Current	5	A_{rms}
Rated output impedance	5	Ω
Filter Inductor, L_f	250	μH
Inductor Resistance, R_f	0.2	Ω
Filter Capacitor, C_f	30	μF

Table 3.1 Inverter Parameters.

For the purpose of obtaining training data, a simulated controller, as shown in Figure 3.3 and Figure 3.4, is built using MATLAB. Hundreds of example patterns are collected to form a pattern database for linear and nonlinear loads. Figure 3.6 shows the complete system diagram. The NN controller has a 5-3-1 structure (five inputs, three nodes in a hidden layer and one output node). The nodes on the hidden layer have a sigmoid transfer function, and the output node has a linear transfer function. This NN

structure is the result of many repeated trials. The structure is found to be simple but sufficient. Its inputs are capacitor current, delayed capacitor current, load current, output voltage, and error between the reference voltage and the output voltage. The delay time of the delayed capacitor current (i_{cd}) is one switching period. Such a time-delay is obtained from a simple R-C low-pass filter. The training of the NN is done using the Neural Network toolbox of MATLAB. The weights and biases of the trained NN are listed in Appendix B.

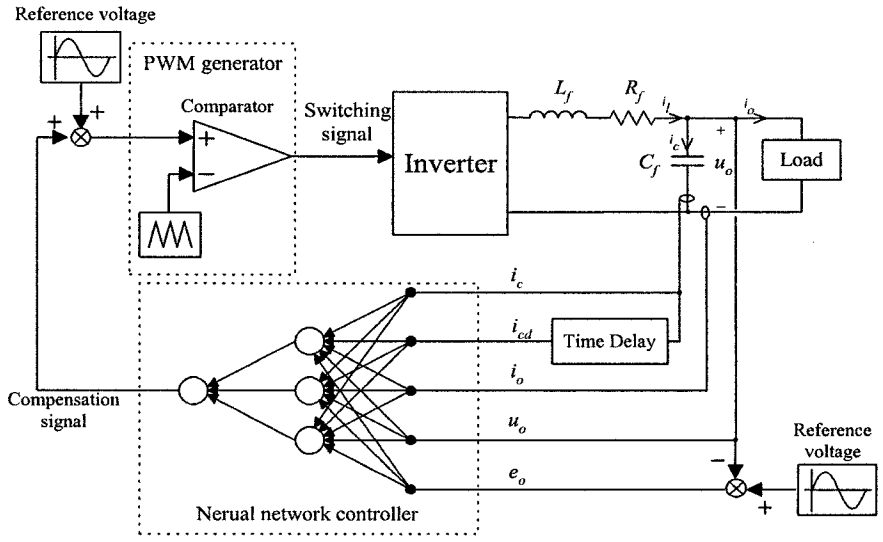


Figure 3.6 Proposed neural network control scheme for UPS inverter.

3.4.1 Simulation Results

We simulate the proposed NN controller using PSpice, which has accurate models of switching components and diodes. The weights and biases from MATLAB simulations are put into the PSpice model. The steady-state response and the dynamic response of the proposed neural network controlled inverter are investigated using PSpice. The output voltage and current waveforms of inverter system for full resistive

load (5Ω) are depicted in Figure 3.7. The figure shows that the proposed neural network control scheme is capable of producing a sinusoidal output voltage. Figure 3.8 shows the simulation result of the dynamic response when the load changes from no load to full load (5Ω). The figure shows that the system exhibits very fast dynamic response with little change in the output voltage at the point of applying the full load, indicating that the neural network control scheme ensures a "stiff" load voltage. Figure 3.9 shows the output voltage and current of the inverter for a nonlinear load consisting of a full-wave diode bridge rectifier following by a 3200μF capacitor in parallel with a 5Ω resistor. Note that although the current has high spikes, the voltage waveform is distorted only slightly. The THD of the output voltage is found as,

$$\%\text{THD} = 100 \times \sqrt{\sum_{h \neq 1} \left(\frac{h\text{th harmonic component}}{\text{the fundamental component}}\right)^2} = 1.76\% \qquad (3\text{-}4)$$

Table 3.2 lists the THD of the output voltage under various load conditions. The proposed neural-network-controlled inverter can achieve quite low THD under various load conditions.

Load Conditions	No load	Resistive load		
		5Ω	10Ω	20Ω
THD (%)	1.36	1.54	1.52	1.52
Load Conditions	Inductive load with 20Ω impedance			
	0.6 PF	0.7 PF	0.8 PF	0.9 PF
THD (%)	1.35	1.37	1.38	1.33
Load Conditions	Capacitive load with 20Ω impedance			
	0.6 PF	0.7 PF	0.8 PF	0.9 PF
THD (%)	1.29	1.33	1.33	1.36
Load Conditions	Full –wave diode bridge with C and R Load			
	500μF 20Ω	1000μF 20Ω	2000μF 20Ω	3300μF 20Ω
THD (%)	2.71	2.82	2.97	3.09

Table 3.2 THD of Output Voltage under Various Load Conditions.

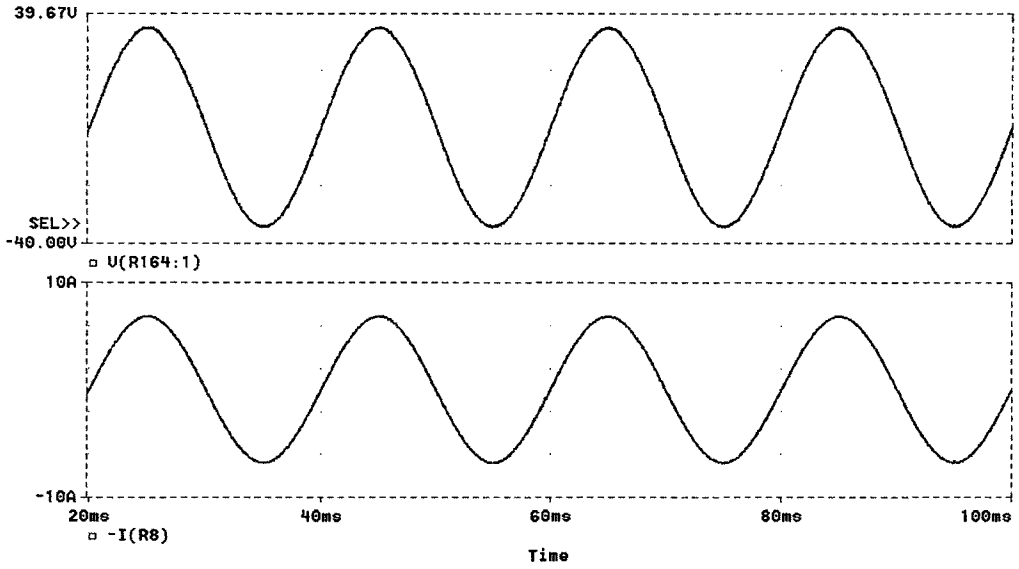


Figure 3.7 Simulation result of the steady-state response of the proposed NN controlled UPS inverter for full resistive load (5Ω).

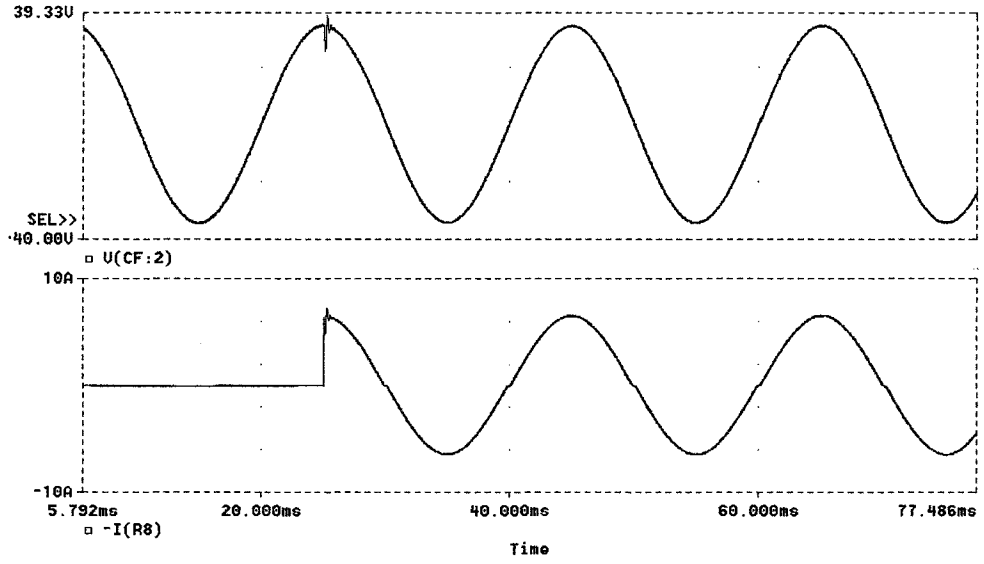


Figure 3.8 Simulation result of the transient response of the proposed NN controlled UPS inverter when the load changes from no load to full load.

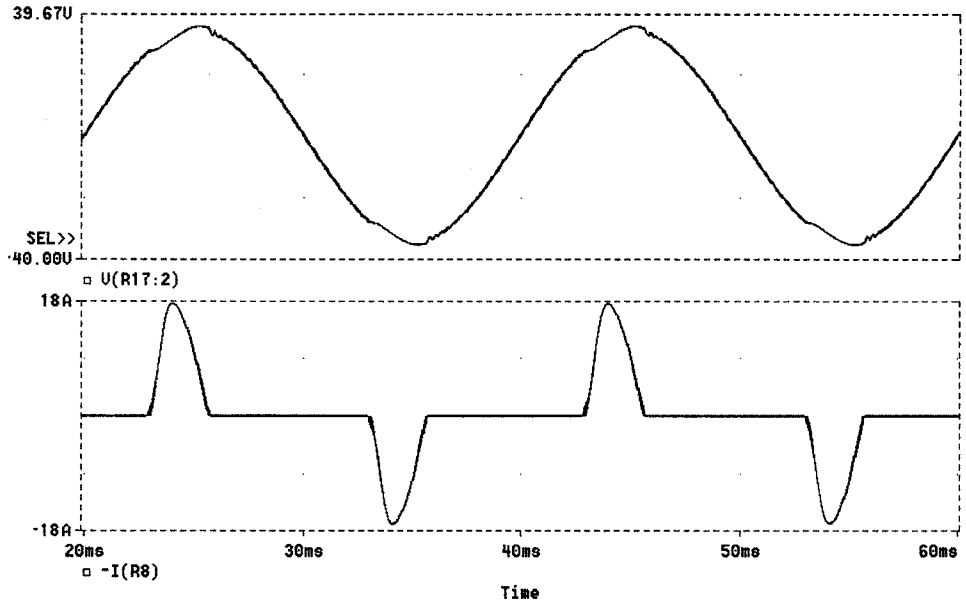


Figure 3.9 Simulation result of the proposed NN controlled UPS inverter for a full-wave diode bridge rectifier load (3200μF 10Ω).

3.4.2 Analogue Hardware Implementation

After off-line training is completed, the weights and biases will not be changed during the control process. Since the forward propagation of the NN involves just multiplication, addition, and sigmoid waveform shaping, a simple analogue circuit can be used to implement the proposed NN controller. To further verify the performance of the proposed NN controller, an experimental inverter system is built with the parameters listed in Table 3.1. We design a simple analogue circuit to implement the proposed NN controller. Figure 3.10 shows the schematic of the circuit, which is composed of mainly operational amplifiers and resistors. The nonlinear sigmoidal function is realized by a differential pair. The weights and the biases of neural network are represented by resistors. The output voltage of the first node in hidden layer u_{node1} can be described as:

$$u_{node1} = Sigmoid[-(\frac{R_f}{R_1}u_{in1} + \frac{R_f}{R_2}u_{in2} + \frac{R_f}{R_3}u_{in3} + ... + \frac{R_f}{R_b}u_b)] \quad (3\text{-}5)$$

where: $Sigmoid(x) = \frac{2}{1+e^{-2x}} - 1$.

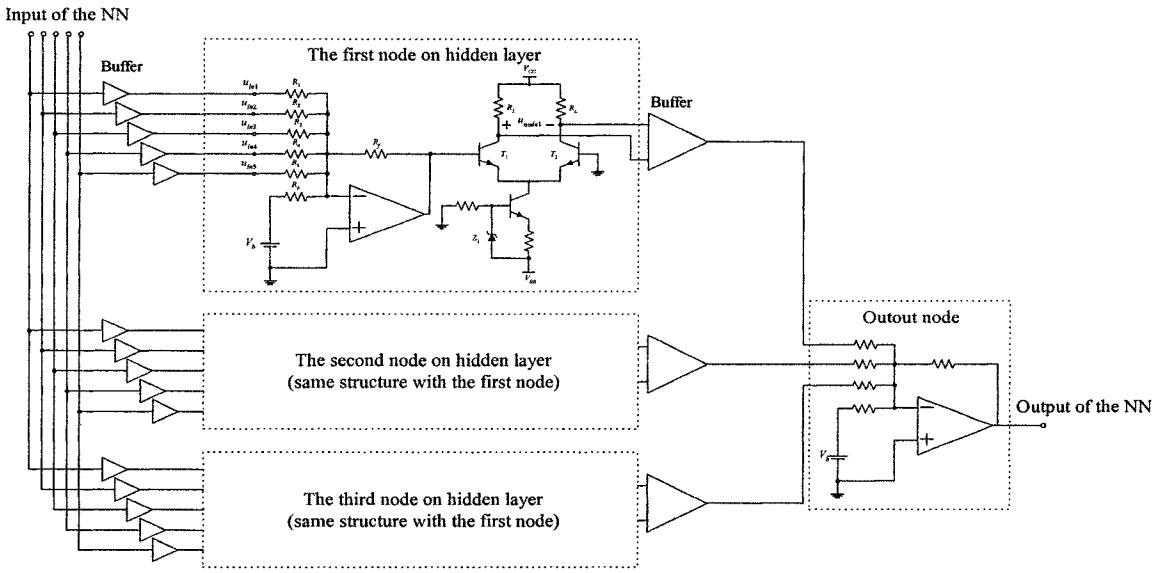


Figure 3.10 An analog circuit realization of the proposed NN controller.

Here it should be noted that analogue circuits have limited precision. It is therefore essential to assess how closely the analogue circuit can approximate the NN. The largest deviation between the analogue implementation and the NN is introduced by the inaccurate weights represented by resistors. In order to study the effect of inaccurate weights, the following experiment is performed:

(1) A network is well trained with the pattern database. The accurate values of the required weights are stored.

(2) Randomly-varying offsets are added to the accurate weights to perturb the NN.

(3) The root mean square (RMS) error between the output of the original NN and the output of the perturbed NN is evaluated.

(4) The procedure is repeated 50 times for each level of relative offset with different inputs and the RMS error is averaged over the 50 runs.

Figure 3.11 shows the average RMS error as a function of the relative offset. The error increases with the relative offset almost linearly. With 3% relative offset of the weights, which can be achievable in most analogue circuitry, the RMS error of output is about 6.6%. Such an error is tolerable in the control system of a UPS inverter.

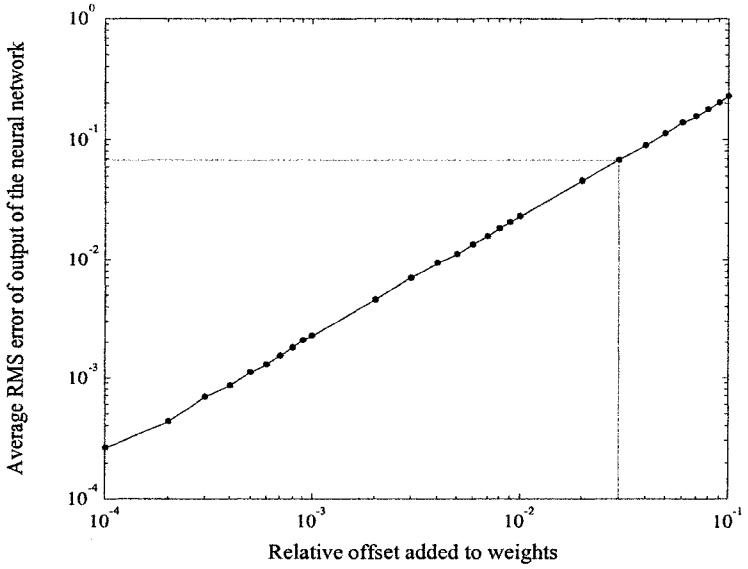


Figure 3.11 Effect of limited precision in the weights.

3.4.3 Experimental Results

A dc/ac inverter system was implemented in the laboratory, which had the parameters listed in Table 3.1. For the purpose of comparison, an inverter with a PI controller has also been built. The PI controller has the structure as shown in Figure 3.3 with K_p=3.1, K_i=2200 and K_c=5.8e-5. The parameters of the PI controller have been optimized for a resistive full-loading condition using frequency domain design techniques.

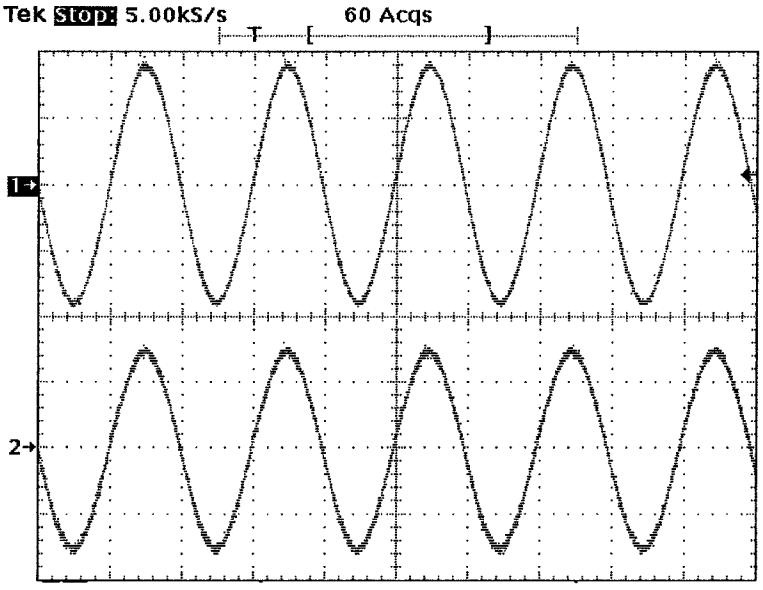
Figure 3.12~Figure 3.15 show the experimental results. Figure 3.12 shows the experimental steady-state output voltage and load current of the NN controlled UPS inverter for a full resistive load. The analog circuit is capable to implement the function of the proposed neural network controller.

Figure 3.13 compares the output voltage and load current waveforms of the NN controlled inverter with those of the PI controlled inverter for a full-wave bridge-rectifier load, whose output is connected directly to a 3200μF capacitor in parallel with a 10Ω resistor. The figure shows that the output voltage of the NN controlled inverter has lower distortion than that of the PI controlled inverter. Figure 3.14 compares the THD of the output voltage of the NN controlled inverter with that of the PI controlled inverter under different rectifier-type loads. It is found that the NN controller significantly outperforms the PI controller.

Figure 3.15 shows the output voltage and load current waveforms for a step change of load from no load to 5Ω resistive load. Compared with the PI controller, the NN controller achieves a smaller overshoot in the output voltage. The NN controller also has an improved dynamic response.

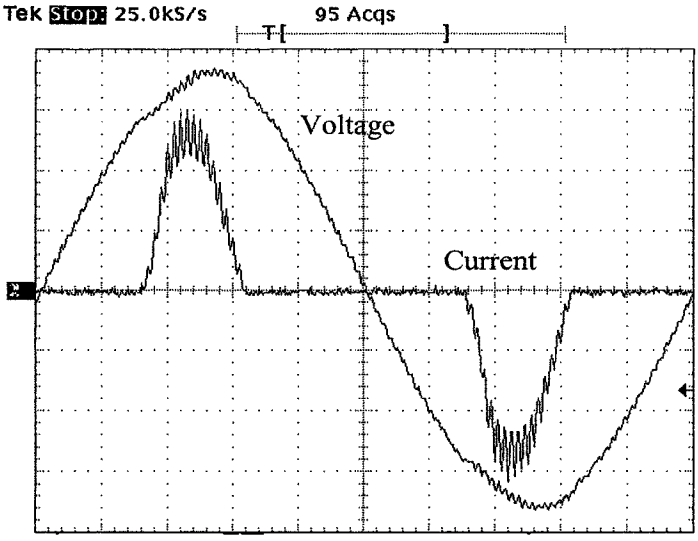
In the NN controller, the input-output mapping of the NN is stored in the pattern database, which includes many cases of rectifier-type loads. The NN learns the control laws from this database. Therefore, the NN stores the knowledge of the characteristics of these rectifier-type loads. It is for this reason that the NN controller can achieve lower distortion in the output voltage than the PI controller.

The experimental results given above confirm that the proposed NN controller can be easily realized by analogue circuit. The NN controller is capable of maintaining good steady-state and fast dynamic responses, and has significant improvement in reducing the THD of the output voltage under nonlinear loading condition. It is very suitable for applications where the load introduces periodic distortions.

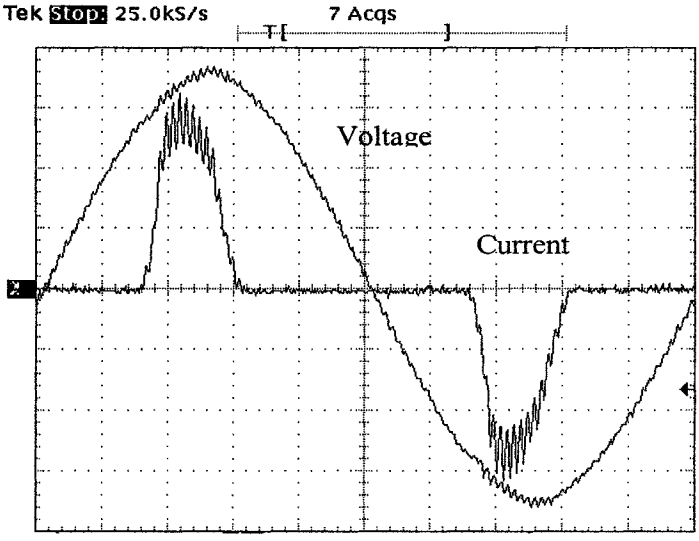


Upper trace: voltage (20V/div, 10ms/div); lower trace: current (4A/div, 10ms/div)

Figure 3.12 Experimental result of the steady-state response of the proposed NN controlled UPS inverter for full resistive load (5Ω).



(a)



(b)

Voltage (10V/div, 2ms/div) Current (5A/div, 2ms/div)

Figure 3.13 Experimental result for a full-wave diode bridge rectifier load (3200μF 10Ω) (a). The PI controlled UPS inverter; (b). The proposed NN controlled UPS inverter.

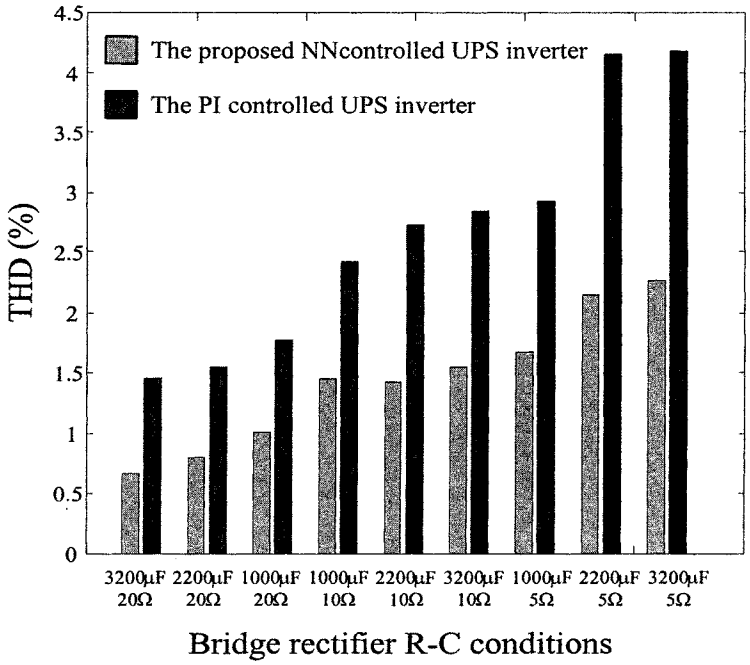
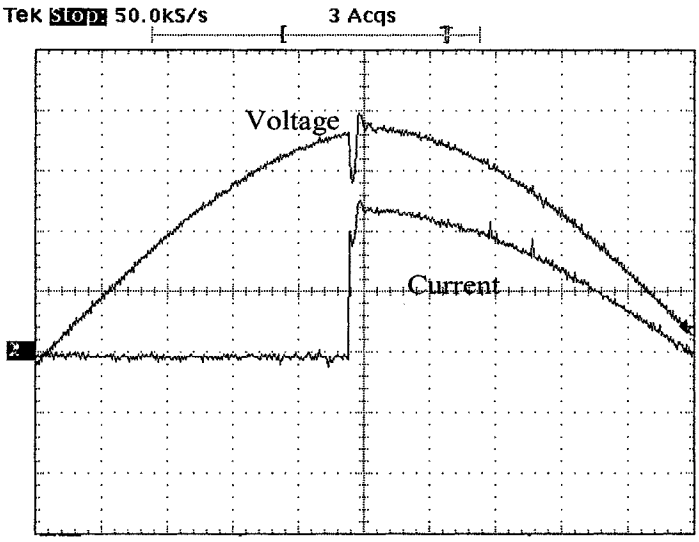
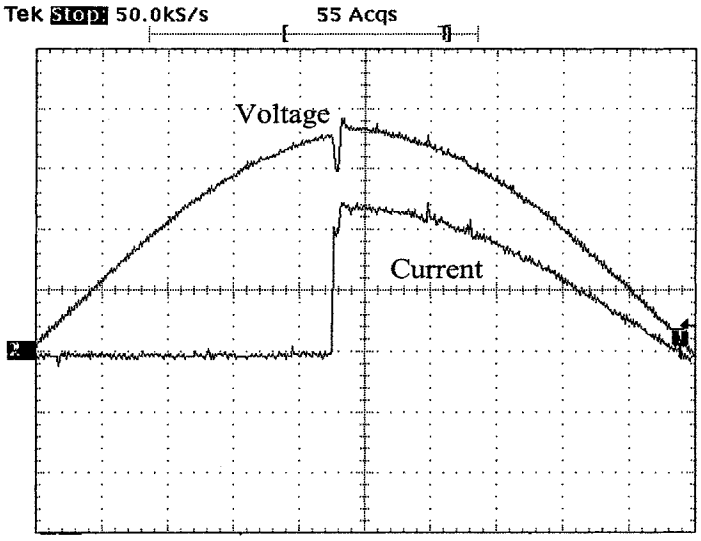


Figure 3.14 The THD of the output voltage for bridge rectifier loads feeding different R-C loads.



(a)



(b)

Voltage(10V/div, 1ms/div) Current(2.5A/div, 1ms/div)

Figure 3.15 Experimental results with a step-change of load from no load to 5Ω (a). The PI controlled UPS inverter; (b). The proposed NN controlled UPS inverter.

3.5 Implementation of the Proposed NN Controller Using Integrated Circuits

For the analogue NN controller described in last section, if the weights and biases of the network have to be changed, the corresponding weighting and biasing resistors have to be replaced. This brings in inconvenience in the fabrication of the controller circuit. We therefore suggest a mixed analogue/digital circuit, which can be implemented in IC (integrated circuit) form, to implement the proposed NN controller. Thus, the whole controller can be integrated into a single chip. The size and cost of the controller could be further reduced. Figure 3.16 shows the block diagram of the proposed integrated circuit, which consists of three parts: EPROM (for weight storage), synapses, and neurons. The following is a brief description of the functions of the building blocks shown in Figure 3.16.

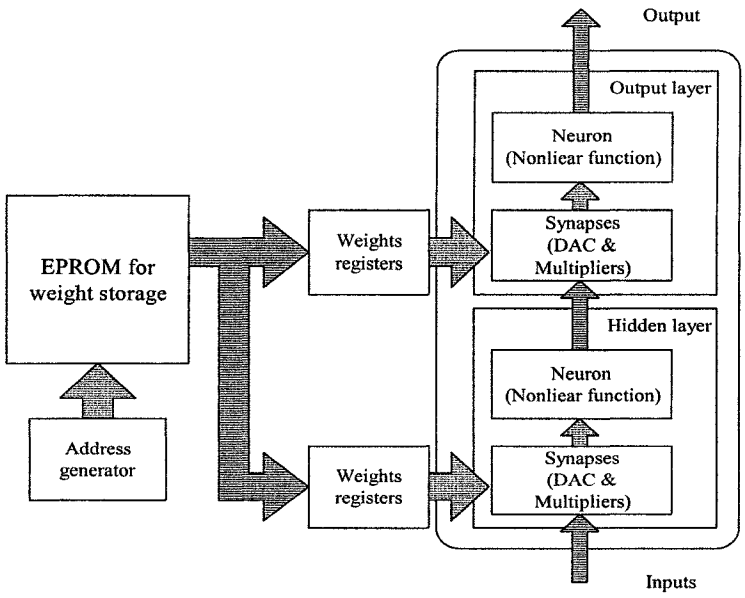


Figure 3.16 Block diagram of the integrated circuit implementation of the proposed NN controller.

3.5.1 EPROM

The EPROM is used to store (digitally) the values of the weights and biases. The values stored in EPROM can be programmed. The maximum error of each weight is Least Significant Bit (LSB). On the contrary, the error in the analogue circuit is unexpectable and suffered from uncompensated thermal drift. From Figure 3.11, we have found that a five-bit resolution is already adequate. The maximum quantization error is 3%. Thus a weight register needs only six bits each. (The extra bit is for the sign.)

3.5.2 Synapse

Synapse is the interconnection between neurons. It is the most important part in hardware implementation of NN. In trainable NN hardware, the function of a synapse includes weight storage, weight adjustment, and multiplication [47]. In this case, due to the off-line training, the weights are not changed after downloaded to the hardware. Therefore, the function of the synapse is simplified. Moreover, the weights and biases are stored in EPROM digitally. The synapses need to transfer the values of the weights to an analogue value and multiply it to the outputs of the neurons in the last layer.

Figure 3.17 shows a circuit to perform the function of the synapse. This circuit is based on a bi-directional current mirror (in the left of Figure 3.17) [54]. The input of the synapse i_{in} is current signal representing the inputs of the NN or the output of the neuron in last layer. The digitally stored weight $B_4B_3B_2B_1B_0$ binary weights the input current to output current. Thus, the output current is the product of the weight and the input current. Figure 3.18 shows the simulation result of the circuit in Figure 3.17 built in PSpice. $B_5B_4B_3B_2B_1B_0$ is set as 10110, namely 22. From Figure 3.18, it is obvious that

the circuit in Figure 3.17 functions as a DAC and a multiplier. Such a circuit is mainly constructed by transistors, it is available for IC implementation.

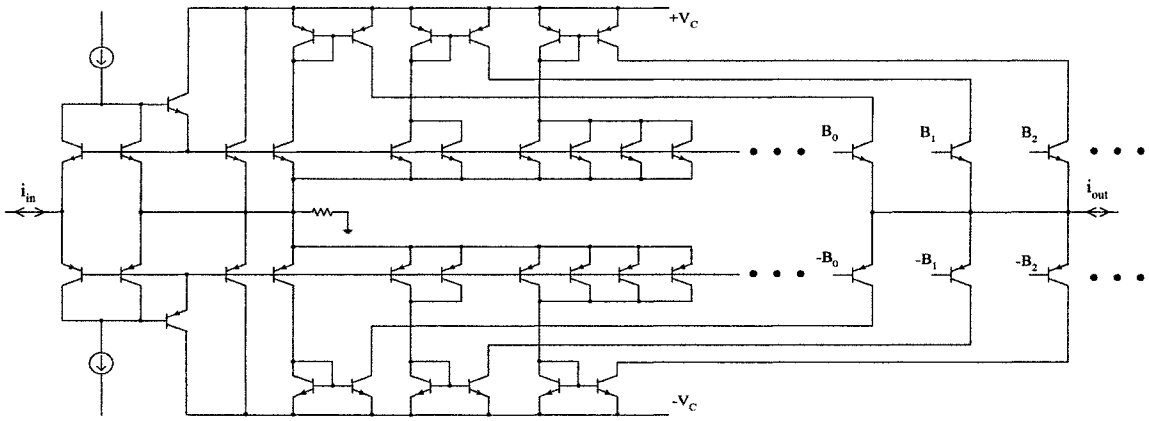


Figure 3.17 The circuit of a synapse.

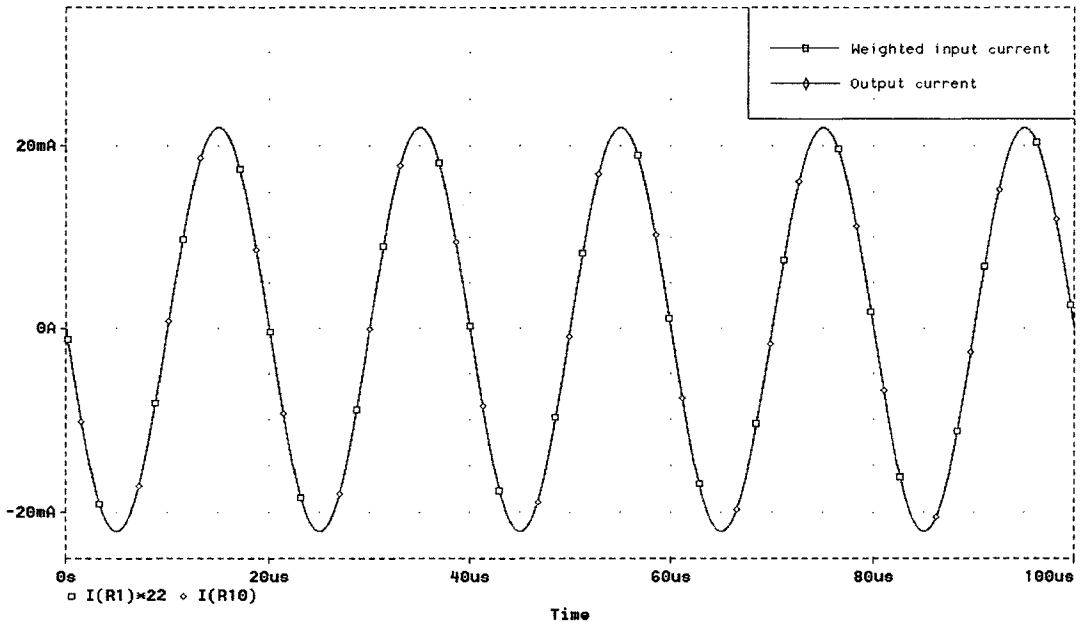


Figure 3.18 Simulation results to show the function of the circuit in Figure 3.17.

3.5.3 Neuron

The summing of the synapses' outputs and the non-linear function mapping are proceeded in the neurons. Here non-linear function is selected to be sigmoid, so that the circuit shown in Figure 3.10 can be used, except for some modification to meet the requirement for IC implementation. Figure 3.19 shows the circuit of a neuron. The main part is a differential pair composed of two transistors and a current source. B_5 is the sign bit of the weight corresponding to the synapse. $!B_5$ is the inverse of B_5. Current switching logic controlled by B_5 enables the output to be changed in sign if a negative weight is desired. The output currents of the synapses are converted to voltage using linear resistors R_s, which also have the function of scaling.

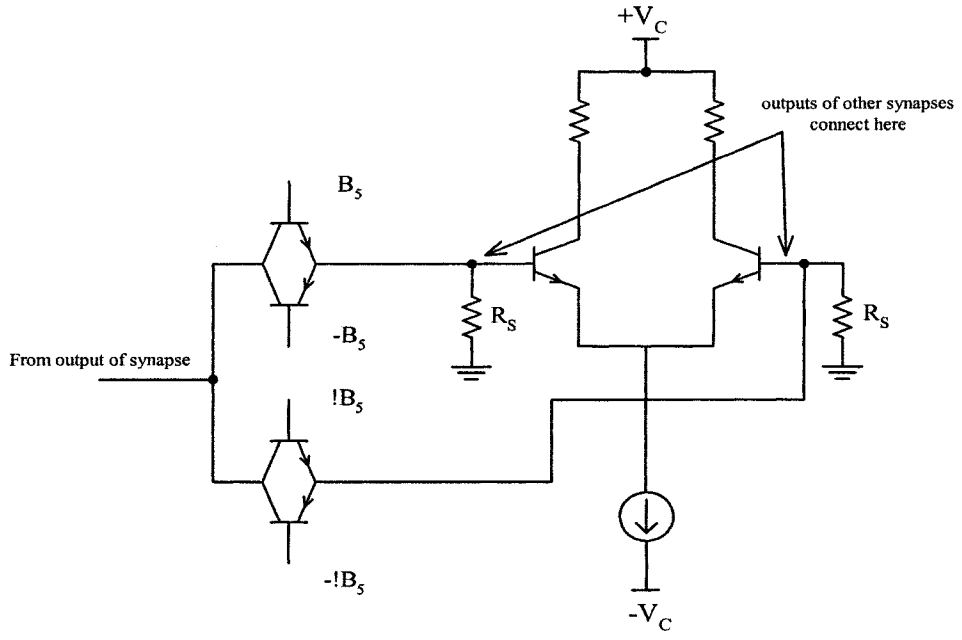


Figure 3.19 The circuit of a neuron.

This proposed programmable controller employs only resistors and transistors. So it can be easily implemented using integrated circuits. Such a scheme has the feature of fast computation and low cost, which can meet the requirement of real-time controller for power converters.

3.6 Conclusion

An analogue NN controller for UPS inverter has been presented in this Chapter. The NN controller is a feedforward network with off-line supervised training. Training patterns for the NN controller are obtained from a simulated controller. After training, the NN can be used to control the UPS inverter on-line. Simulation results show that the proposed NN controller can achieve low THD under nonlinear loading condition and good dynamic response under transient loading condition. The proposed NN controller is implemented using a simple analogue circuit. A traditional PI controller with optimized parameters is also built for comparison purposes. Experimental results confirm the simulation results and show the superior performance of the proposed NN controller, especially under rectifier-type loading condition. The proposed NN controller is particularly suitable for nonlinear load that introduces periodic distortion. Finally, The implementation of the proposed analogue NN controller using programmable integrated circuits has also been discussed.

Chapter 4

Modeling and Analysis of Parallel Multi-Inverter Systems with Average-Current-Sharing Scheme

4.1 Introduction

In recent years, there has been a considerable increase in the use of uninterruptible power supplies (UPS) to provide continuous electrical power to loads which cannot afford to have unexpected power failure [55]. Moreover, with the ever-increasing power demand, a UPS should be expandable. The power capability as well as the reliability can be increased by connecting UPS units in parallel [56]. Such a parallel multi-inverter system could also have other desirable features, such as N+X redundancy operation and modularity [57]. However, output characteristic of the inverters is voltage source, the system could be damaged without proper current-sharing mechanism. A current-sharing control scheme has to be employed to enable the paralleled inverters to share the load current equally.

To connect inverters in parallel, the simplest method is to employ a coupled inductor at the output end of the inverter [58][59]. The coupled inductor can reasonably balance the output currents among the inverters. However, the working frequency of the inductors is quite low. Such a bulky inductor greatly increases the size and cost of the system. In case the load current contains harmonics, the output voltage will be strongly distorted by the inductors. In addition, it is inconvenient to add more inverters to the system.

A traditional current-sharing control method is the frequency and voltage droop method [9], [60]-[63]. Such a method has been used in utilities for decades to share the power among distributed power plants. The basic idea is that the real power flow is mainly influenced by the power angle. On the contrary, the reactive power flow is mostly dependent on the amplitude of the output voltage. A notable advantage of this method is simplicity, because no extra interconnections among inverters are required. Thus, high modularity and good reliability can be easily achieved. However, the voltage regulation and transient responses are sacrificed. In addition, the harmonic currents cannot be shared properly. Some reports are presented to solve the harmonic currents sharing based on droop method [64]-[66]. Due to the inherent "droop" nature, all those schemes only try to set a compromise between the current-sharing precision and the voltage regulating precision.

To improve the voltage regulation and the current-sharing characteristics, interconnections among inverters are required to transfer/share certain common information. The objective of sharing information among inverters is to determine the deviation of the individual output current from the desired value.

At the early development of the parallel multi-inverter system, due to the limitation of the switching frequency of the switching components, the sharing

information is either the average RMS value of the output current [9],[67][68], or the average output active/passive power [69] to compensate the RMS value and frequency of the output voltage. The voltage regulation is improved. However, the response of the sharing loop is slow, only the RMS value of the output current of each inverter is assured to be equal. The harmonic current unbalances among the inverters can still be large.

With the development of semi-conductor technologies, high-speed switching components appeared. To improve the instantaneous current-sharing characteristics, instantaneous current-sharing schemes have been proposed [70]-[78]. These schemes employ different mechanisms to share information among the inverters. The reported instantaneous current-sharing schemes can be classified as: master-slave current-programming method [70]-[72], average current-programming method [73]-[77], and circular-chain current –programming method [78]. Since the output currents of the inverters are regulated at every switching cycle, instantaneous current-sharing scheme has very good performance in both current sharing and voltage regulation. Even if the output currents contain many harmonics, the inverters can share the output currents equally. However, the interconnections between the inverters are necessary. This limits the flexibility of the multi-inverter system and degrades redundancy of the system.

Besides the above-mentioned ones, a method called frequency-based current-sharing technique was also reported [79]. This technique is attractive and interesting. It does not need any interconnection. The sharing information is transferred through the output bus using a frequency to represent the value. Such a technique has the advantages of both the frequency/voltage droop method and the sharing bus method. However, it could be very sensitive. If some noise within the frequency bandwidth used

by the sharing signal were coupled to the output bus, an unbalance of power distribution could be caused. When the situation is serious, the whole system can become unstable.

In this Chapter, a multi-inverter system with instantaneous average-current-sharing scheme is presented. By introducing a disturbance source to represent all the sources that may cause current unbalances, a model of the system can be easily built. Some key issues of the parallel multi-inverter system are discussed based on the model, including stability of the current-sharing controller, impedance characteristics and voltage regulation. Three experimental 110Vac/1.1KVA inverters are built and paralleled to verify the theoretical predictions.

4.2 System Configuration of Parallel Multi-Inverter System

Figure 4.1 shows a block diagram that describes the instantaneous current-sharing scheme for a multi-inverter system with n inverters paralleled. The output of jth inverter is connected through an impedance Z_{pj} to load Z_L. Each inverter has three control loops, which are the inner current feedback loop, the voltage feedback loop, and the outer current-sharing loop. The control scheme consists of the voltage feedback loop and the inner current-feedback loop, which is proved to have good performance on both steady-state and transient responses on single inverter system [14][15]. The reference of the voltage-feedback loop u_j^* should be synchronized to make the output voltages of all inverters in phase. An outer current-sharing loop is added to enable each inverter to contribute equal power to the load. Each inverter provides a measurement of its output current i_j to the current-sharing bus, which generates a common current reference i_s.

According to different mechanisms, the reference i_s can be the averaged output current [73]-[77], the highest output current [71], or the output current of the one with fastest clock [72]. The error between i_s and inverter's own output current i_j is first processed by the current-sharing controller H_j, and then added onto the voltage reference to feed to the control input of the inverter concerned. With the high gain of H_j, the error between i_s and i_j tends to zero. All inverters' output current will be the same. The equal current sharing is therefore achieved.

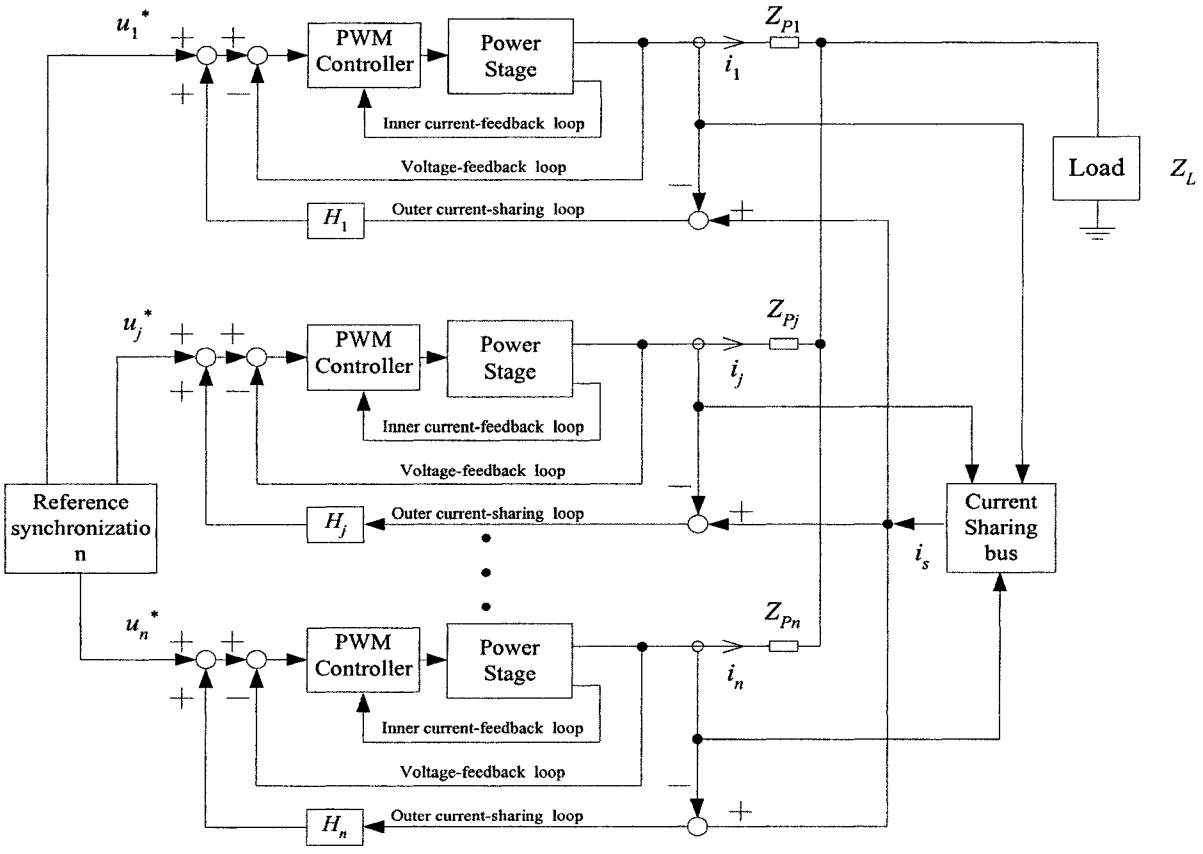


Figure 4.1 A block diagram of parallel multi-inverter system.

4.3 Modeling of Parallel Multi-Inverter System

In this section, a model of parallel multi-inverter system is built for analyzing and evaluating system's performance and stability. The current-sharing loop is outside of the voltage-feedback loop. It is a very natural thought to treat voltage-feedback loop as a control objective of the current-sharing loop. Therefore, the modeling of the system starts from a single inverter integrated with the inner current-feedback loop and the voltage-feedback loop. Sub-section 4.3.1 describes modeling of a single inverter. Then, a model for n paralleled-inverter system is derived in sub-section 4.3.2, which will be used to analyze and assess the performance and stability of the multi-inverter system in Section 4.4.

4.3.1 Model of a Single dc/ac Inverter

An inverter typically consists of a dc power source, a bridge type (full-bridge or half-bridge) PWM inverter and an LC output filter, as shown in Figure 2.1. Using the linear model of a dc/ac inverter introduced in section 2.4, the inverter with a multi-loop feedback controller can be described by Figure 4.2, where the controller consists of an inner capacitor-current-feedback loop, an outer voltage-feedback loop, and a voltage-feedforward loop. By introducing the capacitor-current-feedback loop, the sensitivity to parameter variations is reduced and the robustness is much improved. Moreover, the system can have a fast dynamic response [14][15]. Here, the voltage-feedback loop employs a traditional PI controller to regulate the output voltage. Since the PI controller will introduce phase errors, a voltage-feedforward loop is employed to reduce the phase error and to provide a high tracking accuracy to the reference. Although this

arrangement may cause large overshoot in the dynamic response, the drawback can be overcome by optimizing the parameters of the voltage-feedback loop. K_c is the gain of the capacitor-current-feedback loop. K_p and K_i are the proportional and integrated gains of the voltage-feedback loop. K_f is gain of the voltage-feedforward loop. For the simplicity of analysis, we let the modulation gain of inverter $M = 1$.

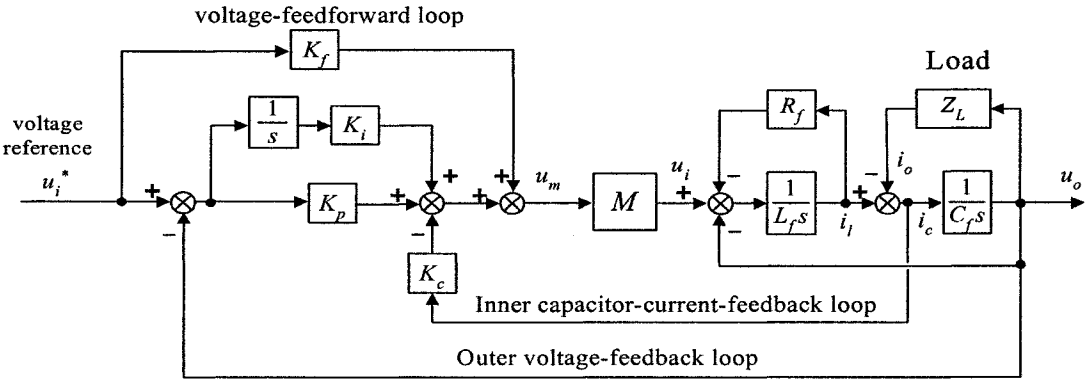


Figure 4.2 Linear model of inverter with multi-loop feedback control.

According to Thévenin theorem, all two-terminal networks can be treated as a voltage source in series with an output impedance. Therefore, a closed-loop inverter can be represented by the equivalent circuit shown in Figure 4.3, where Gu_i^* is a controlled voltage source and Z is the output impedance of the inverter. Z_L is the impedance of the load. Z_P is the impedance of the line that connects the output of the inverter to the load.

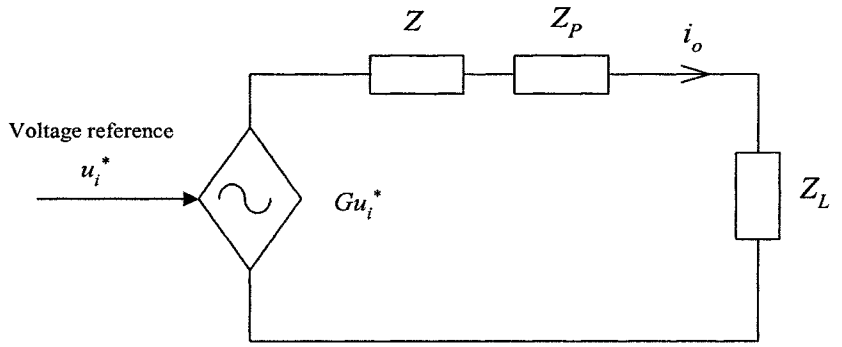


Figure 4.3 Thévenin equivalent circuit of a closed-loop inverter.

From Figure 4.2, the closed-loop voltage gain G and the output impedance Z are derived. (M=1)

$$G = \left.\frac{u_o}{u_i^*}\right|_{i_o=0} = \frac{[(K_f + K_p)s + K_i]}{C_f L_f s^3 + C_f(R_f + K_c)s^2 + (1 + K_p)s + K_i} \tag{4-1}$$

$$Z = -\left.\frac{u_o}{i_o}\right|_{u_i^*=0} = \frac{L_f s^2 + R_f s}{C_f L_f s^3 + C_f(R_f + K_c)s^2 + (1 + K_p)s + K_i} \tag{4-2}$$

Figure 4.4 shows the typical Bode plots of G and Z. We set the parameters of the inverter to the values listed in Table 4.1.

Parameter	Value	Parameter	Value	Parameter	Value
L_f	1mH	R_f	0.2Ω	C_f	20μF
K_f	1	K_p	4.5	K_i	2780
K_c	6.5				

Table 4.1 Inverter parameter list.

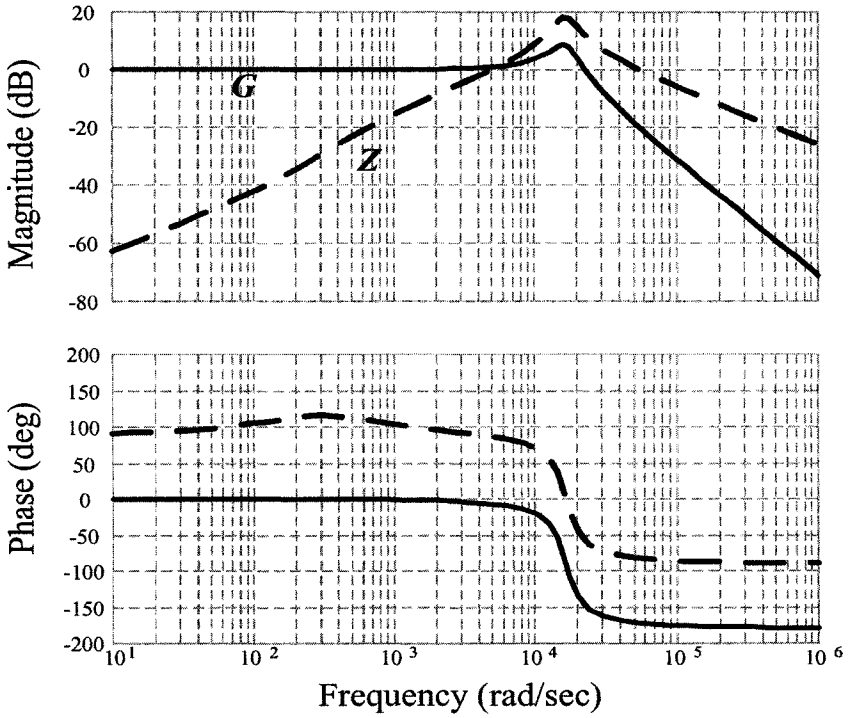


Figure 4.4 Typical Bode plots of the closed-loop gain G and the output impedance Z.

Based on the individual dc/ac inverter model given above, a model of parallel multi-inverter systems will be developed in next sub-section.

4.3.2 Model of Parallel Multi-Inverter Systems

In a parallel multi-inverter system, each inverter acts as a voltage source. If all the inverters are identical, the output current will be equally shared automatically. However, in practical circuits, the parameters of the inverters have deviations. These parameter deviations cause the output current of the inverter to change from the nominal one. Thus, we can consider the parameter deviations as disturbances to the inverter. For simplicity, we assume that the effects of the parameter deviations and other external disturbances are collected and presented at the output of the inverter as shown in Figure 4.5, where i_d

represents the disturbance source. Therefore, the current-sharing problem becomes a disturbance-rejection problem [80][81]. The objective of the current sharing control is now to minimize the influence of the disturbance source.

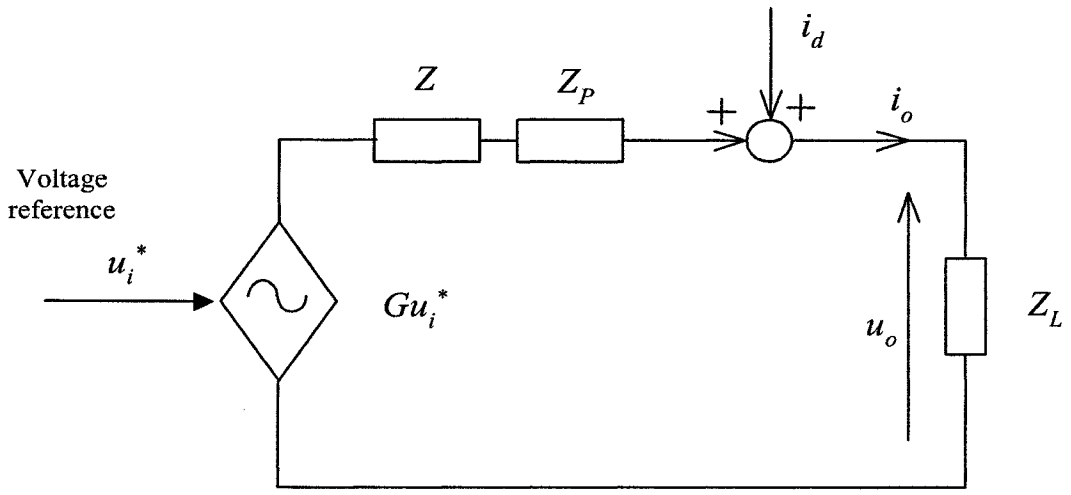


Figure 4.5 Inverter model showing disturbance source.

By introducing a disturbance source to represent all parameter deviations, all the inverters in the parallel multi-inverter system can be considered as identical. Therefore, we have

$$\begin{aligned} &G_1 = \cdots = G_j = \cdots = G_n = G \\ &Z_1 = \cdots = Z_j = \cdots = Z_n = Z \\ &Z_{P1} = \cdots = Z_{Pjl} = \cdots = Z_{Pn} = Z_P \\ &u_{i1}^* = \cdots = u_{ij}^* = \cdots = u_{in}^* = u_i^* \\ &H_1 = \cdots = H_j = \cdots = H_n = H \end{aligned} \tag{4-3}$$

By using (4-3) and Figure 4.5, the parallel multi-inverter system illustrated by Figure 4.1 can be modeled as shown in Figure 4.6. All inverters are identical except i_{dj}, which is the disturbance source.

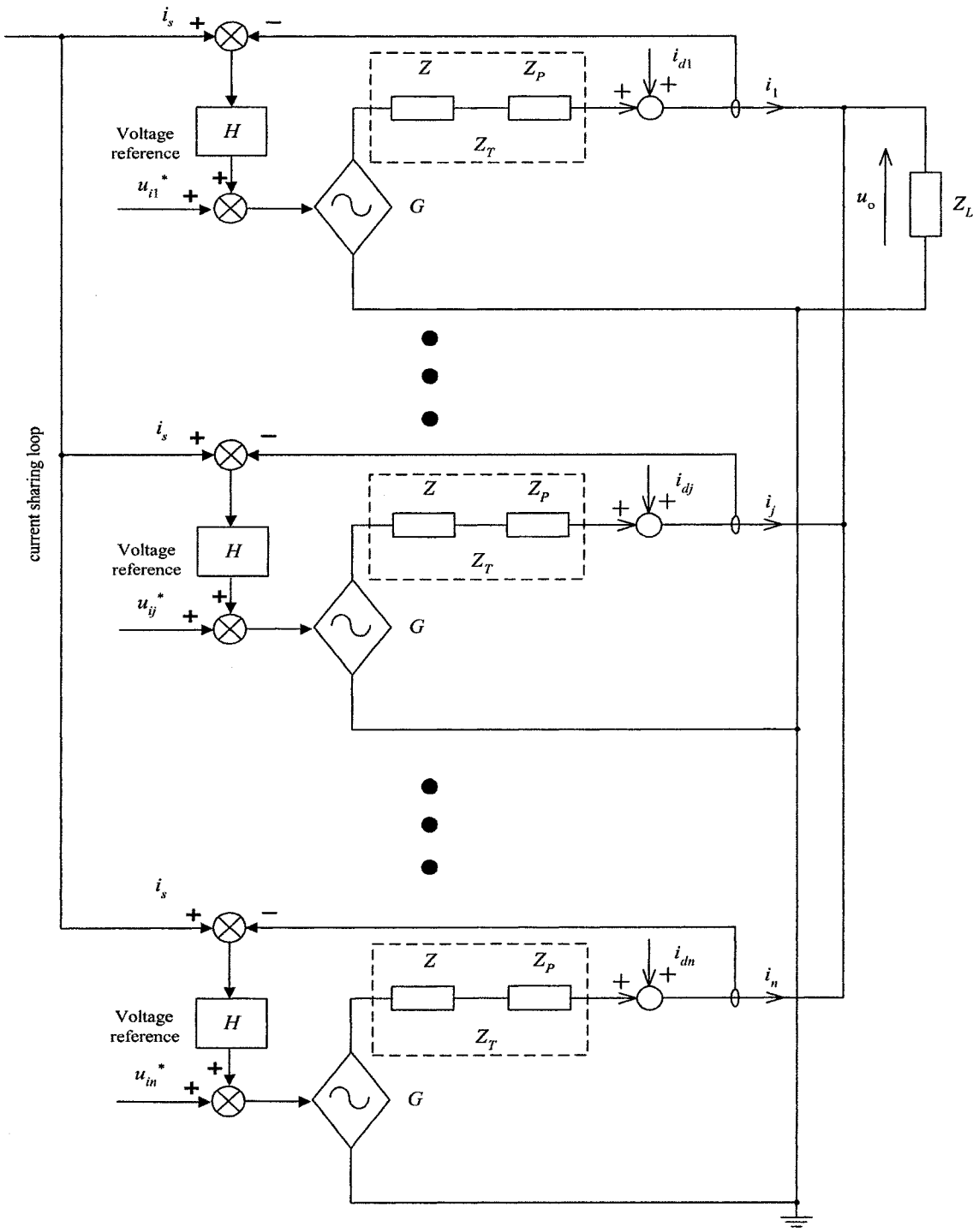


Figure 4.6 Model of a parallel multi-inverter system.

From Figure 4.6, a set of equations to describe the parallel multi-inverter system can be obtained:

$$\begin{cases} (i_1+\cdots+i_j+\cdots+i_n)Z_L = u & (5-4.1) \\ G[u_i^* + (i_s - i_1)H] - u_o = (i_1 - i_{d1})Z_T & (5-4.2) \\ \vdots & \vdots \\ G[u_i^* + (i_s - i_j)H] - u_o = (i_j - i_{dj})Z_T & (5-4.j+1) \\ \vdots & \vdots \\ G\,[u_i^* + (i_s - i_n)H] - u_o = (i_n - i_{dn})Z_T & (5-4.n+1) \end{cases}$$

where Z_T=Z+Z_P.

We consider an average-current-sharing control scheme. The shared information is the average current. Therefore, we have

$$i_s = \frac{\sum_{j=1}^{n} i_j}{n} \tag{4-5}$$

Adding (4-4.2), (4-4.3), …, and (4-4.n+1) together, we have

$$nGu_i^* + [ni_s - \sum_{j=1}^{n} i_j]GH - nu_o = (\sum_{j=1}^{n} i_j - \sum_{j=1}^{n} i_{dj})Z_T \tag{4-6}$$

Replacing i_s by (4-5), and inserting (4-4.1) into (4-6), the following is obtained.

$$u_o = \frac{G}{1+Z_T/nZ_L}u_i^* + \frac{Z_T/n}{1+Z_T/nZ_L}\sum_{j=1}^{n} i_{dj} \tag{4-7}$$

Inserting (4-7) into (4-4.k+1), we have

$$i_k = \frac{G/nZ_L}{1+Z_T/nZ_L}u_i^* + \frac{1}{n}\frac{(n-1)+Z_T/Z_L+GH/nZ_L}{(1+Z_T/nZ_L)(1+GH/Z_T)}i_{dk} + \frac{1}{n}\frac{GH/nZ_L-1}{(1+Z_T/nZ_L)(1+GH/Z_T)}\sum_{\substack{j=1 \\ j\neq k}}^{n} i_{dj} \tag{4-8}$$

(4-7) and (4-8) show the characteristics of the voltage regulation and current sharing of the system, respectively. The stability of the system is decided by the positions of the roots of the denominators in (4-7), (4-8). The Bode plots can be employed to examine whether any roots are located in the right half of the complex plane.

4.4 Analysis and Simulations

In this section, a detailed analysis of the parallel multi-inverter system shown in Figure 4.6 will be given. PSspice simulations are used to verify the results. In these simulations, full bridge inverters are used. The control scheme within each individual inverter is the same as the one shown in Figure 4.2. The dc input of the inverter is 300V. The switching frequency is 40kHz. The rated output voltage of the inverter is $110V_{rms}$@50Hz. The rated output current is $11A_{rms}$. Other inverter parameters are the same as those listed in Table 4.1. In order to perturb the system, different LC filters and line impedances are used in different inverters. One has the nominal values as listed in Table 4.1, the others have deviated values. These values are list in Table 4.2, which will be used in following sub-sections.

	Inductance of filter L_f	Resistor of the filter R_f	Capacitance of filter C_f	Line Impedance Z_p
First inverter	1mH	0.2Ω	20μF	0.03Ω
Second inverter	1.2mH	0.24Ω	17μF	0.01Ω
Third inverter	1.4mH	0.28Ω	13μF	0.02Ω
Fourth inverter	0.8mH	0.16Ω	23μF	0.015Ω

Table 4.2 The parameter lists of L-C filter and line impedance that used in the simulation.

4.4.1 Current-Sharing Controller

In (4-7) and (4-8), it is clear that the stability of the system is decided by the roots of the denominators. Thus, the stability condition reduces to the requirement that $(1+Z_T/nZ_L)$ and $(1+GH/Z_T)$ have all roots on the left half of the complex plane. The contribution of the current-sharing controller H to the system stability is discussed in this sub-section.

In the term of $(1+GH/Z_T)$, G is the closed-loop voltage gain (while the current-sharing loop is opened), Z_T is the equivalent output impedance (plus line impedance), and H is the gain of current-sharing controller. The term GH/Z_T can be considered as the loop gain of the current-sharing loop. Bode plots of this loop gain can be used to assess the stability and to evaluate the performance of the current-sharing loop.

Here, G and Z_T are both stable. Figure 4.7 shows the Bode plots of G/Z_T (dashed line). We need to design H to compensate the Bode plots of GH/Z_T to a desirable shape. The gain in the low-frequency region should be large enough, but in the high-frequency region, the gain should be attenuated. The gain at intermediate frequencies typically controls the gain and phase margins. Near the crossover frequency, the slope of the log-magnitude curve in the Bode plots should be close to –20dB/decade. Therefore, the transfer function of H is selected as

$$H = \frac{40(1.6\times10^{-4}s+1)}{(1\times10^{-3}s+1)(1\times10^{-5}s+1)} \tag{4-9}$$

This is a one-zero, two-pole controller with a zero at 994Hz, and two poles at 154Hz and 15.92kHz. The Bode plots of GH/Z_T are also shown in Figure 4.7 (solid line). The crossover frequency is 5381Hz and the phase margin is 61°. The Bode plots of loop

gain (GH/Z_T) have high crossover frequency and large phase margin. The performance of this current sharing controller is expected to be satisfacted.

Now, we apply the current-sharing controller H, with the transfer function of (4-9), to a two-inverter system. The two inverters have the L-C filter and line impedance parameters as listed in the top two rows of Table 4.2. In our case, Z_L (= 5Ω) and Z_T are both stable. Figure 4.8 shows the Bode plots of Z_T/nZ_L. It shows that $(1+Z_T/nZ_L)$ has its roots in the left-half plane. Since both $(1+GH/Z_T)$ and $(1+Z_T/nZ_L)$ have left-half-plane roots, the parallel two-inverter system is predicted to be stable. The transient response of the system is simulated. In order to perturb the system, a 5A pulse lasting 100μs is injected into the output current of the first inverter at 45ms. Figure 4.9 shows the response. It shows that response of the output currents of the two inverters quickly settle to their steady state. The variations in these two currents are also seen to be out of phase with each other, so that the output voltage remains a good sinusoidal waveform (The total output current remains essentially sinusoidal). Note from Figure 4.9 that the damped oscillation frequency of the transient response is approximately the same as the crossover frequency shown in Figure 4.7 (5381Hz).

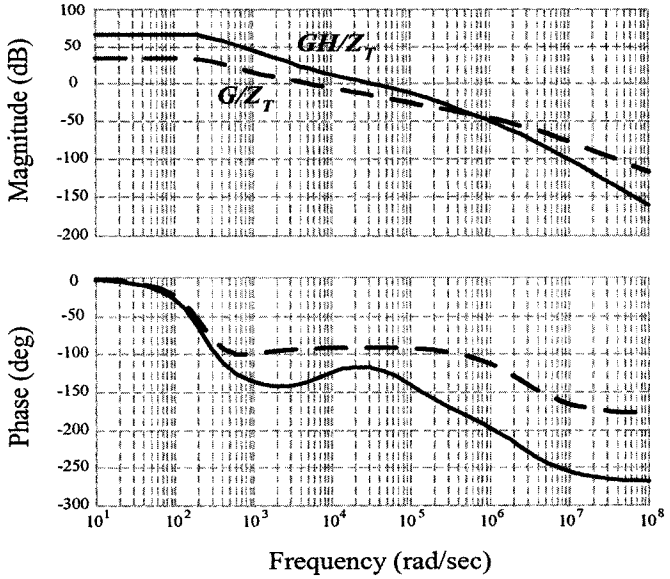


Figure 4.7 Bode plots of G/Z_T and GH/Z_T (H have the transfer function of (4-9)).

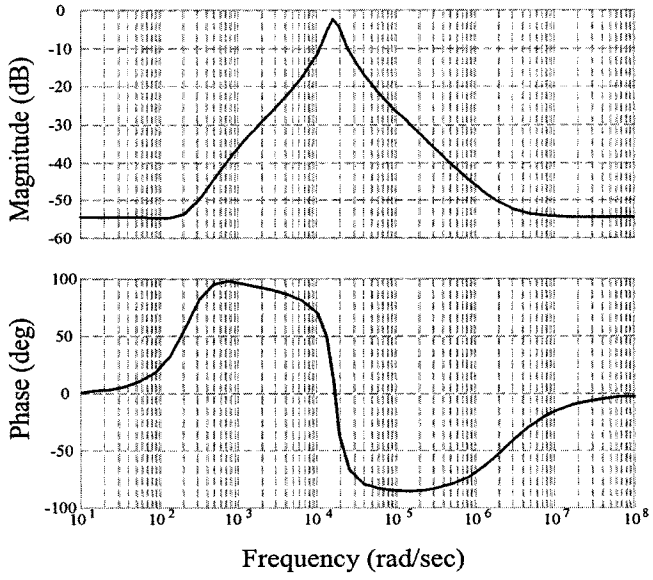
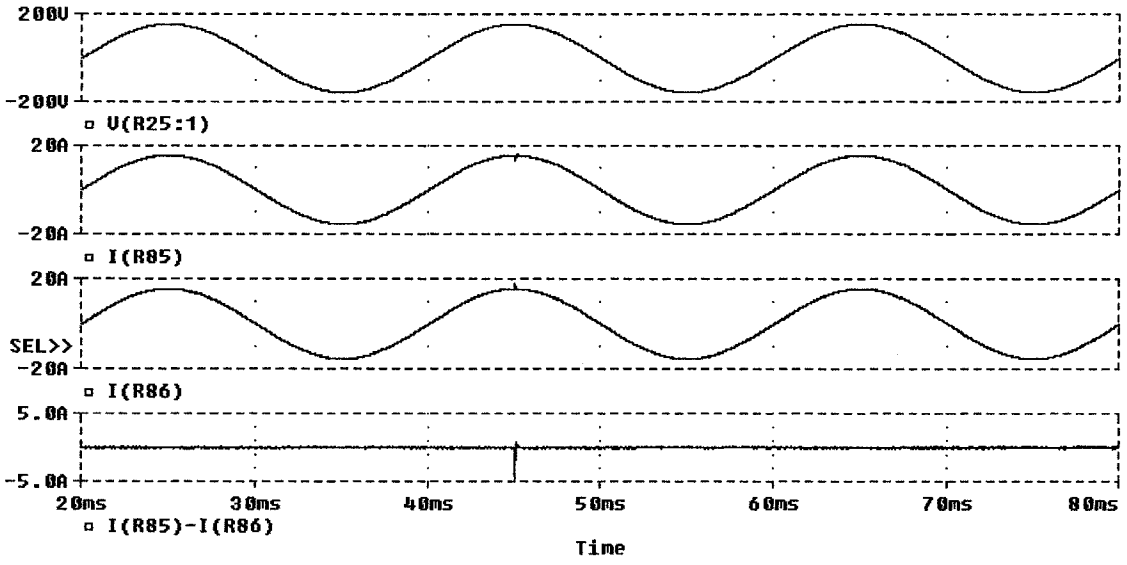
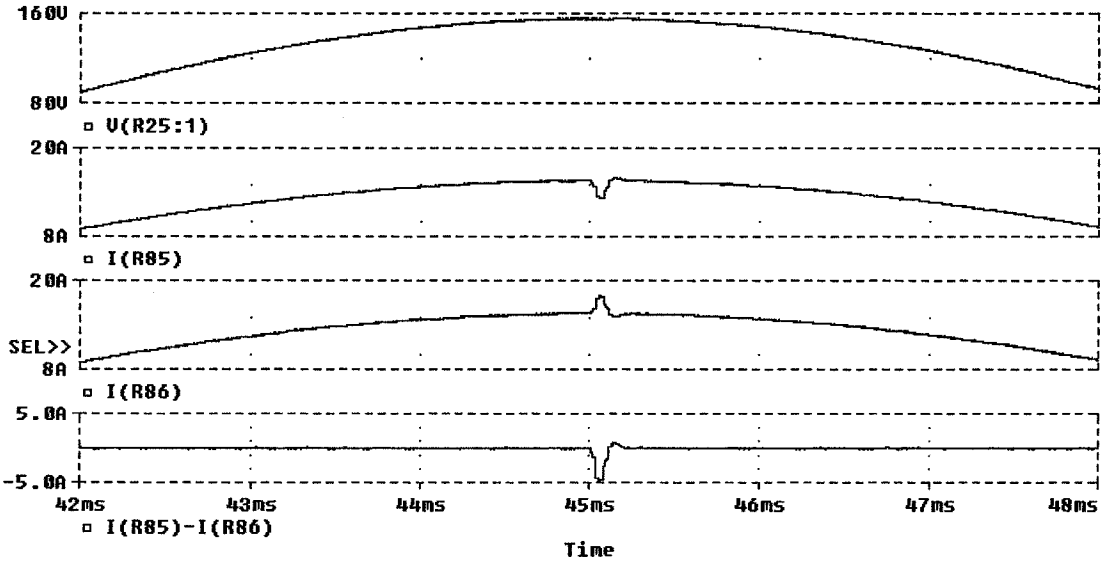


Figure 4.8 Bode plots of Z_T / nZ_L. (Total load is 5Ω, number of paralleled inverters is 2).



(a)



(b)

Figure 4.9 PSpice simulation results of transient response of two-inverter system with H of (4-9). (a). global view. (b). detailed view. First: output voltage; Second: output current of the first inverter; Third: output current of the second inverter; Fourth: error between the output current of the two inverters.

In order to illustrate the contribution of H to the system stability and performance, we move the pole at 154Hz of (4-9) to 32Hz. Thus, H is changed to

$$H = \frac{40(1.6\times10^{-4}s+1)}{(5\times10^{-3}s+1)(1\times10^{-5}s+1)} \tag{4-10}$$

The resulting Bode plots of GH/Z_T are shown in Figure 4.10. The crossover frequency is now 1375Hz and the phase margin is 49°, indicating a stable system. However, now the crossover frequency is lower than that of Figure 4.7. The response of the current sharing controller of (4-10) is expected to be slower than that of the current sharing controller of (4-9). Figure 4.11 shows the results. It is found that, after the perturbation, the output currents of the two inverters can settle to their steady states. However, the settling time is much longer compared with the responses shown in Figure 4.9. Note again that the oscillatory frequency of the damped response closely matches the crossover frequency shown in Figure 4.10.

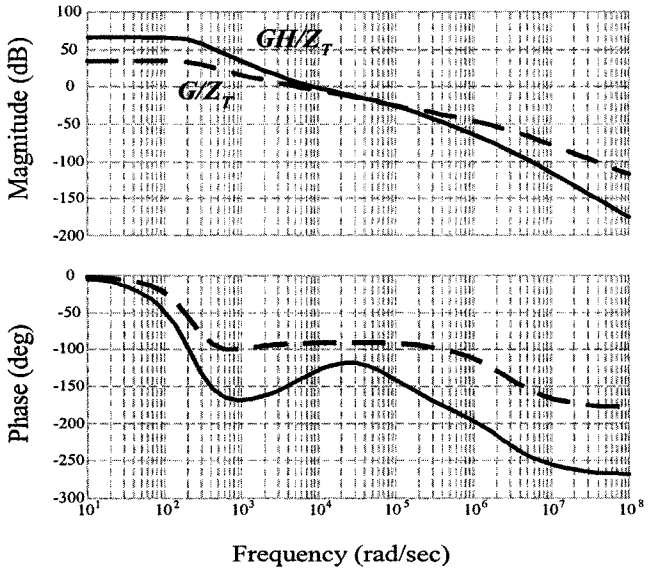
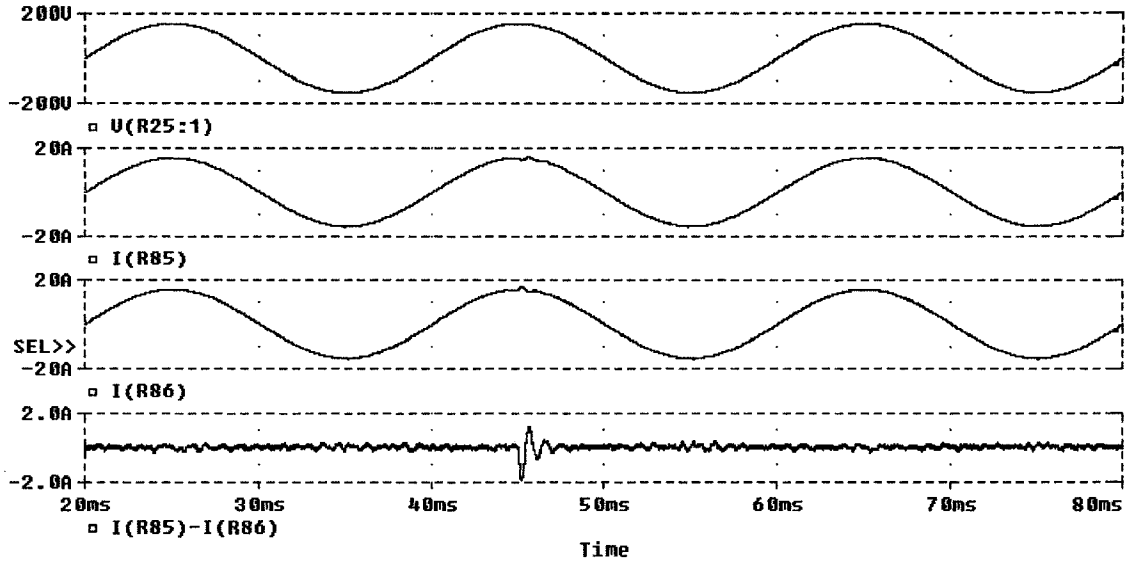
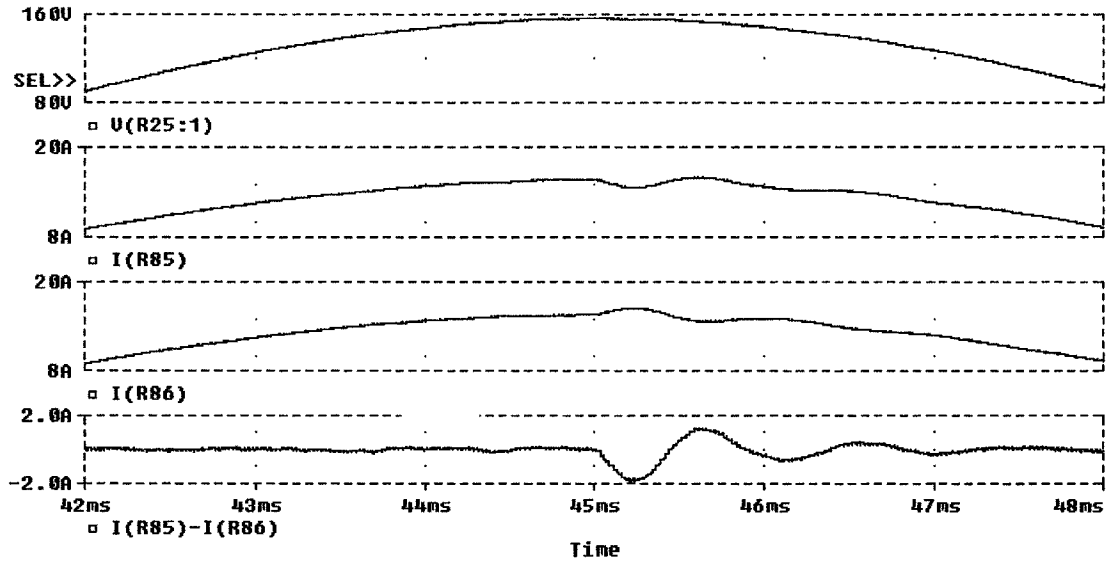


Figure 4.10 Bode plots of G/Z_T and GH/Z_T (H has the transfer function of (4-10)).



(a)



(b)

Figure 4.11 PSpice simulation results of transient response of two-inverter system with H of (4-10). (a). global view. (b). detailed view. First: output voltage; Second: output current of the first inverter; Third: output current of the second inverter; Fourth: error between the output current of the two inverters.

Next, we will demonstrate an unstable operation of the two-inverter system caused by the current-sharing controller. We remove the zero at 994Hz of (4-9). Thus, H is changed to

$$H = \frac{40}{(1\times10^{-3}s+1)(1\times10^{-5}s+1)} \tag{4-11}$$

The resulting Bode plots of GH/Z_T are shows in Figure 4.12. The crossover frequency is 1925Hz and the phase margin is –9°, indicating instability. The simulation results are given in Figure 4.13. The output currents of the two inverters oscillate with increasing amplitude, confirming the system instability. It should be noted that the two output currents are out of phase with each other. Although the system is instable, the total current is still essentially sinusoidal, thus the output voltage is also sinusoidal. Externally, the system fails to display the instability until it collapses.

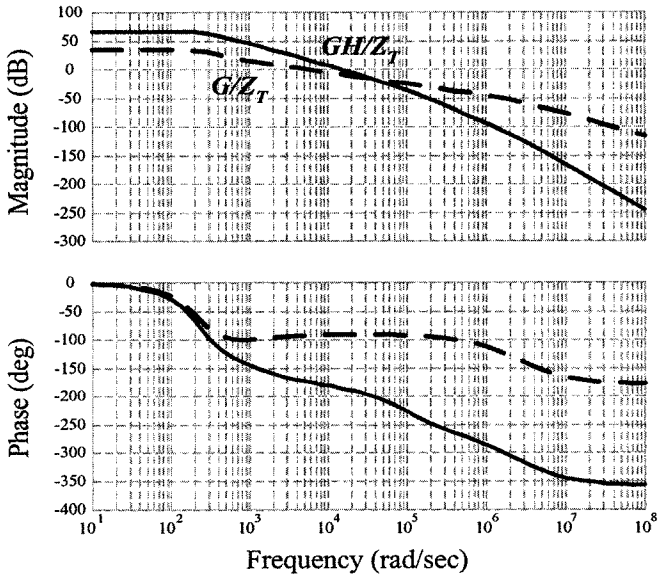


Figure 4.12 Bode plots of G/Z_T and GH/Z_T (H have the transfer function of (4-11)).

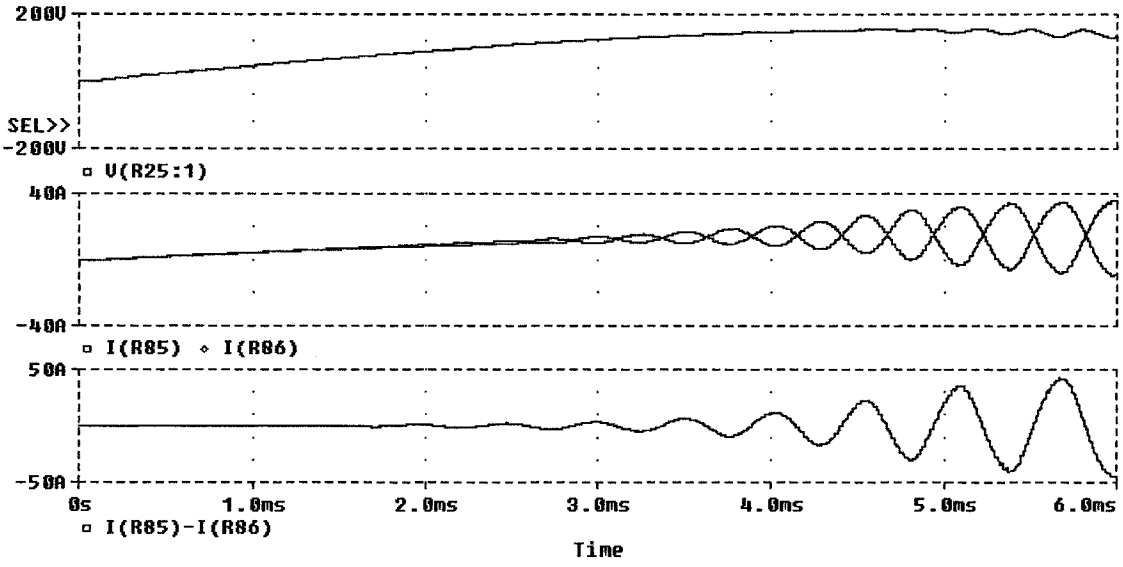
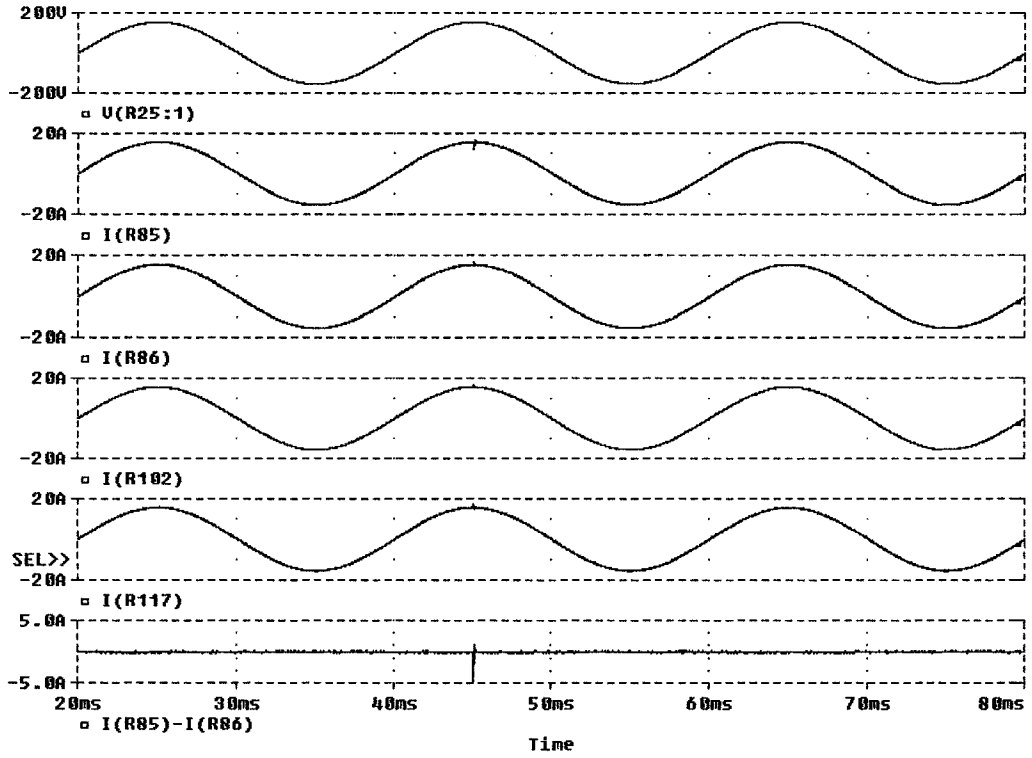


Figure 4.13 PSpice simulation results of transient response of two-inverter system with H of (4-11). First: output voltage; Second: output currents of both inverters; Third: error between the output current of the two inverters.

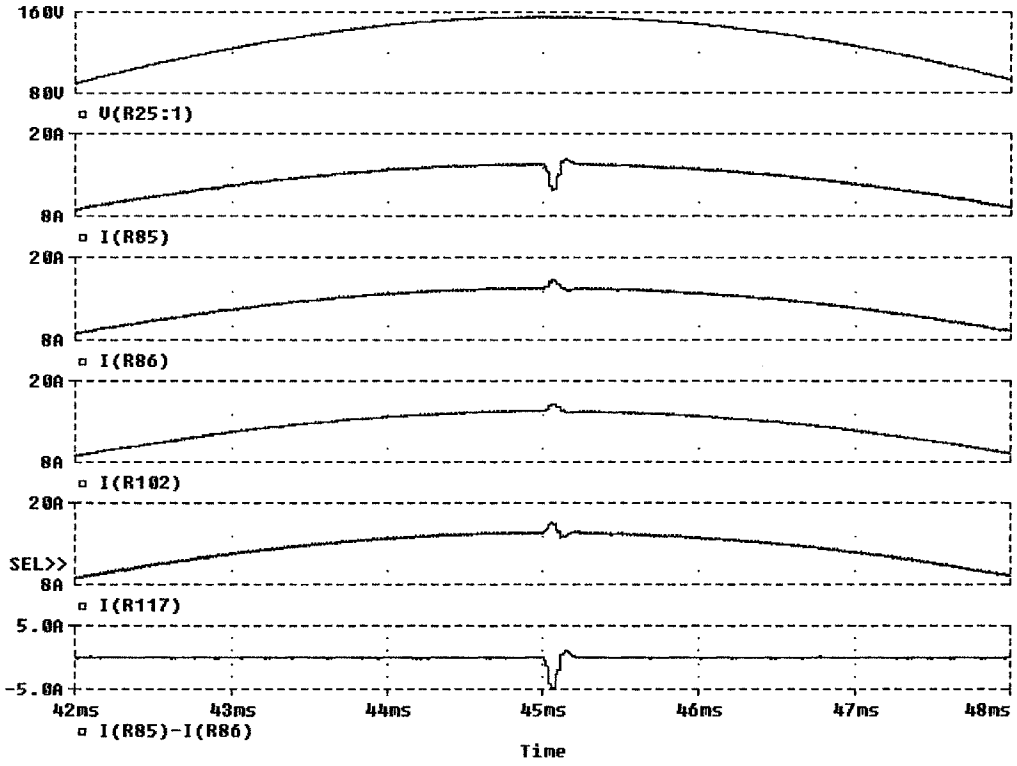
From the analysis and simulation results given above, it is found that the term of GH/Z_T can be treated as loop gain of the current-sharing loop. Thus, the stability and performance of the current-sharing loop can be predicted by examining its Bode plots.

It should be noted that the number of the paralleled inverter, n, does not appear in GH/Z_T. Therefore, the stability of the current-sharing loop is not related to n. For the purpose of verification, a simulation is run for a four-inverter system, where the inverters have L-C filters and line impedances as listed in Table 4.2. Now, the total load for the case of the four-inverter system is 2.5Ω. The current-sharing controller of (4-9) is employed to equalize the output currents. Again, a 5A pulse lasting 100μs is injected into the output current of the first inverter at 45ms. Figure 4.14 shows the responses. It is found that the transient response of the four-inverter system (shown in Figure 4.14) is

essentially the same as that of the two-inverter system (shown in Figure 4.9). It is demonstrated that the number of the paralleled inverter has no influence on the stability and performance of the current-sharing loop.



(a)



(b)

Figure 4.14 PSpice simulation results of transient response of four-inverter system with H of (4-9). (a). global view. (b). detailed view. First: output voltage; Second: output current of the first inverter; Third: output current of the second inverter; Fourth: output current of the third inverter; Fifth: output current of the fourth inverter; Sixth: error between the output current of the first and the second inverters.

4.4.2 Impedance Characteristics

The term $(1+{GH}/{Z_T})$ in denominator of (4-8) that we discuss in the last sub-section is directly determined by the design of the current-sharing loop. In contrast, another term $(1+{Z_T}/{nZ_L})$, which appears in the denominator of (4-7) and (4-8), is

unaffected by the current-sharing controller H and depends only on: 1) the equivalent output impedance of the inverters; 2) the load impedance; and 3) the number of paralleled inverters. To guarantee the stability of the system, $(1+Z_T/nZ_L)$ should have all its roots on the left-half plane. Therefore, we can examine the Nyquist or Bode plot of Z_T/nZ_L to assess the stability of the system.

As we assume that the paralleled inverters are the same (they have equal equivalent output impedance Z_T), so that the term of Z_T/n can be treated as the output impedance of the source system, whereas Z_L is the input impedance of the input impedance of the load system. The ratio of these two impedances has been used to evaluate the stability of the DC distributed power systems [82]-[84]. Although our case is a multi-inverter system, it can be found from term $(1+Z_T/nZ_L)$ that the relationship between the source and the load is also reflected by the ratio of the output impedance of the source and the input impedance of the load. Therefore, the conclusions and methodologies that were found in DC distributed power systems can be applied to the multi-inverter systems. Here, the criteria to ensure system stability are:

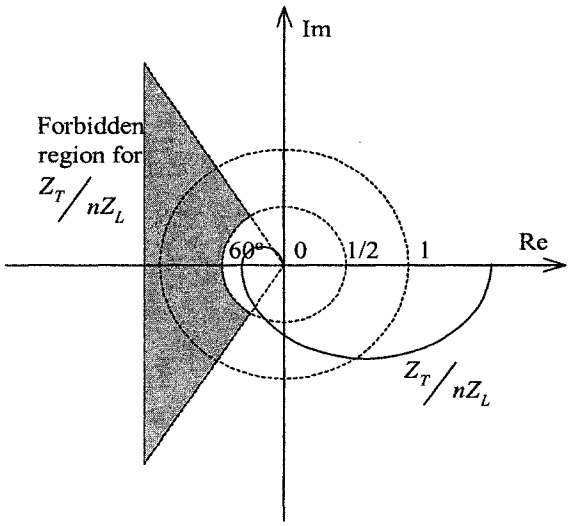
- If the output impedance of the source system is much smaller than the input impedance of the load system within all frequency ranges, i.e., $Z_T/n \ll Z_L$, then the system stability is guaranteed.

  or

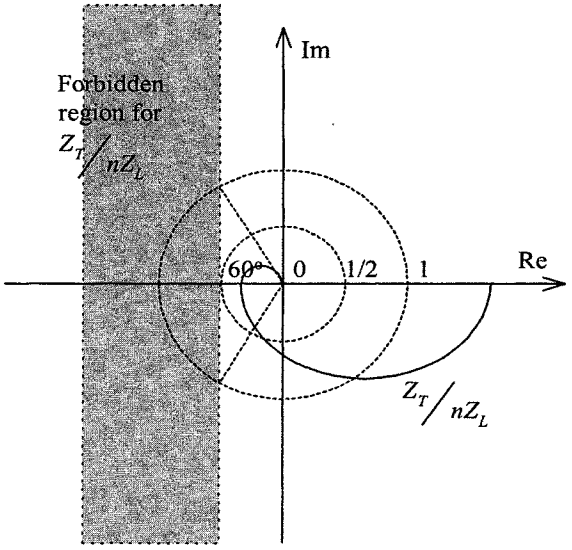
- In [83] and [84], a less conservative impedance specification is provided. By keeping Z_T/nZ_L out of the forbidden region shown in Figure 4.15, the

system stability is guaranteed with a GM (gain margin) of 6dB and PM (phase margin) of 60°.

For more details, the readers may like to refer to references [82], [83], and [84].



(a)



(b)

Figure 4.15 Forbidden regions of Z_T/nZ_L.

The output impedance of the source system is usually very low. In general, the requirement of $Z_T/n << Z_L$ can be met. However, there are applications in which the load is a negative resistance (*-R)*, which is generated by the closed-loop control of the load. In case that the output impedance of the source system is larger than close loop controlled load (*-R*), the whole system may become unstable. To illustrate the role of the Z_T/nZ_L, we change the load of the former multi-inverter system to be a negative resistance, -4Ω. The Nyquist plots of $Z_T/2Z_L$ and $Z_T/4Z_L$ are shown in Figure 4.16. The curve of two-inverter system covers the point of –1, while the curve of four-inverter does not, indicating that the two-inverter system will be unstable, and the four-inverter system will be stable. To verify these results, transient simulations are run, with the results shown in Figure 4.17 and Figure 4.18. Figure 4.17 is a two-inverter case, the current oscillate with increasing amplitude, indicating unstable operation. Note that unlike the results shown in Figure 4.13, the inverter currents oscillate in phase, suggesting that the instability is not caused by the current-sharing loop. Figure 4.18 is a four-inverter case. Due to the larger number paralleled inverters, the output impedance of the source system is reduced, and the system becomes stable.

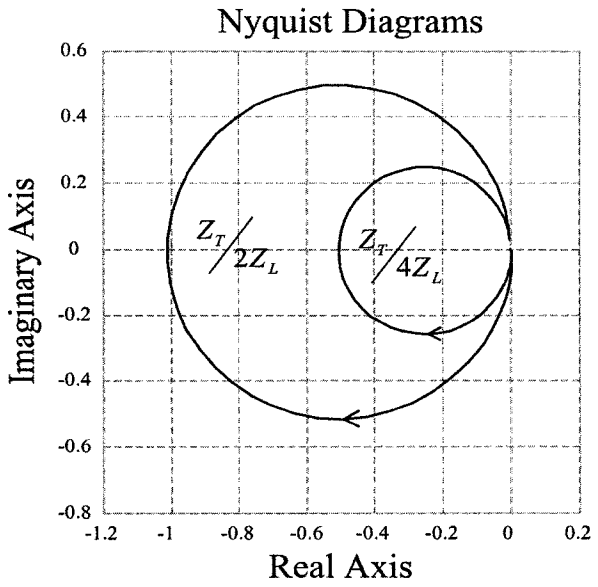


Figure 4.16 Nyquist plots of $Z_T/2Z_L$ and $Z_T/4Z_L$.

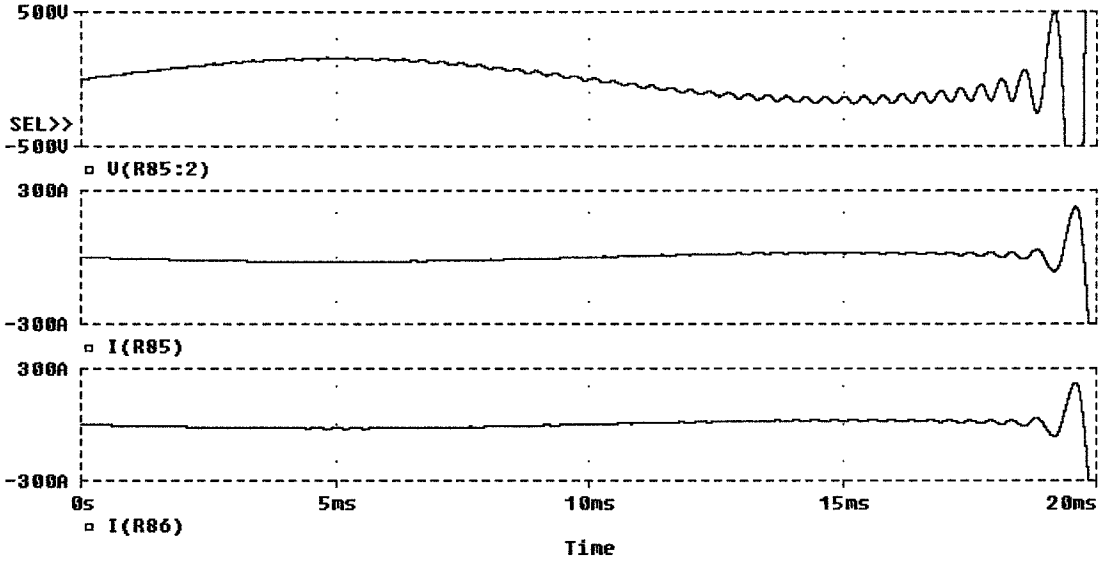


Figure 4.17 PSpice simulation results of transient response of two-inverter system with negative resistance, -4Ω. First: output voltage; Second: output current of the first inverter; Third: output current of the second inverter.

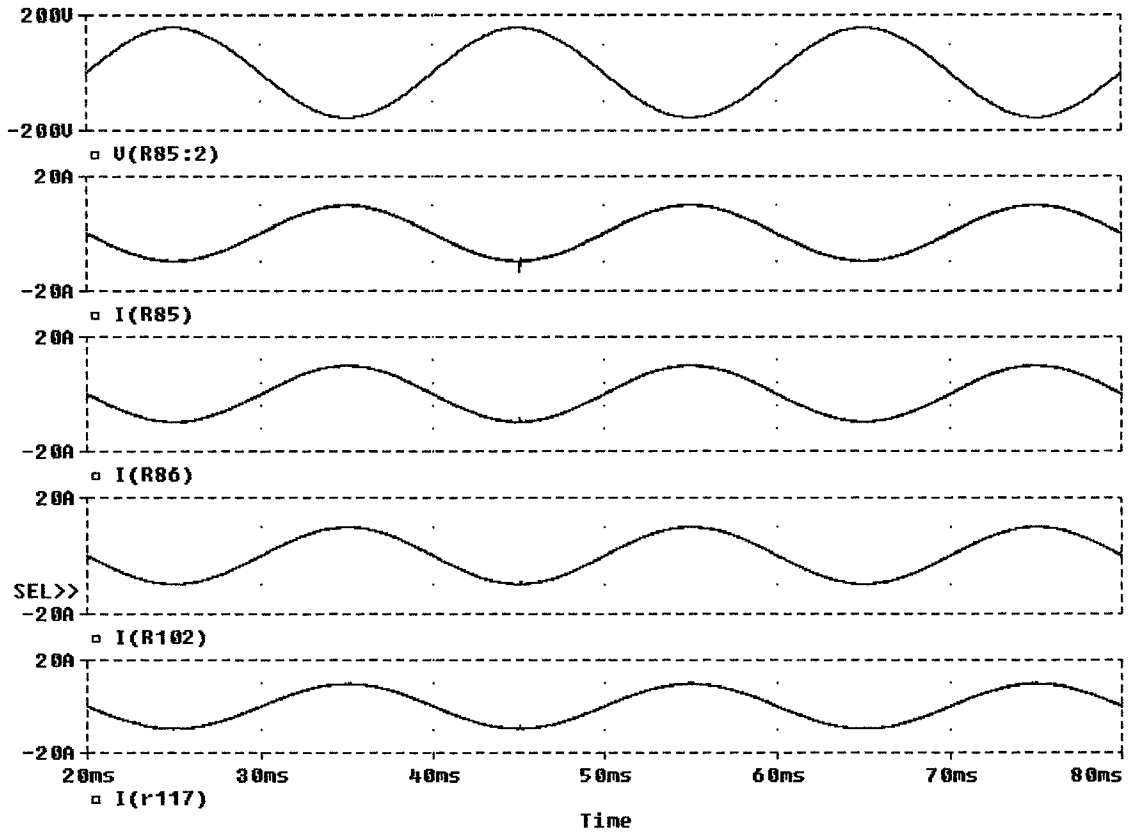


Figure 4.18 PSpice simulation results of transient response of four-inverter system with negative resistance, -4Ω. First: output voltage; Second: output current of the first inverter; Third: output current of the second inverter; Fourth: output current of the third inverter; Fifth: output current of the fourth inverter.

4.4.3 Voltage Regulation

Equation (4-7) is an expression showing the relationship among the output voltage, the voltage reference, and the disturbance source. Since (4-7) is independent of H, the output voltage is not affected by the current-sharing controller.

Equation (4-7) shows that the output voltage depends on only G, Z_T and the disturbance source i_d. Under a stable parallel operation, i.e., GH/Z_T is stable and Z_T/n << Z_L, (4-7) can be simplified to

$$u_o = \frac{G}{1+\frac{Z_T}{nZ_L}} u_i^* + \frac{Z_T/n}{1+\frac{Z_T}{nZ_L}} \sum_{j=1}^{n} i_{dj} \approx G u_i^* + \frac{Z_T}{n} i_d \qquad (4\text{-}12)$$

In order to achieve a small steady-state error of output voltage, the closed loop gain G should be constant and have no phase shift within the operating frequency. To achieve good disturbance rejection and good load regulation, the equivalent output impedance Z_T should be as small as possible. These requirements are the same as those of a single inverter. G and Z_T are the parameters that are determined in the design of the individual inverter. Therefore, under stable parallel operation, the voltage regulation of the whole system depends on the voltage-regulating capability of the individual inverter.

4.5 Experimental Results

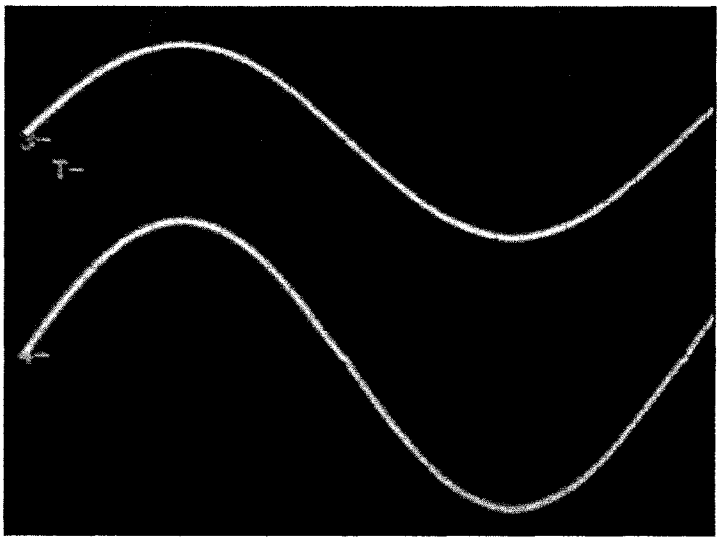
Three 110Vac/1.1KVA dc-ac inverters are built for parallel operation. The arrangement of the system is same as the one shown in Figure 4.6. Each inverter has a structure as shown in Figure 4.2, and has the parameters as listed in Table 4.1. The dc input of the inverter is 300V. The switching frequency is 40kHz. The rated output voltage of the inverter is $110V_{rms}$@50Hz. The rated output current is $11A_{rms}$. In order to investigate the influence of the current sharing controller H to the multi-inverter system, we apply different transfer function of current sharing controller (H) to the system.

Figures 4.19~21 are the steady-state responses, Figures 4.22~24 are the dynamic responses, and Figure 4.25 is the response for a rectifier-type load.

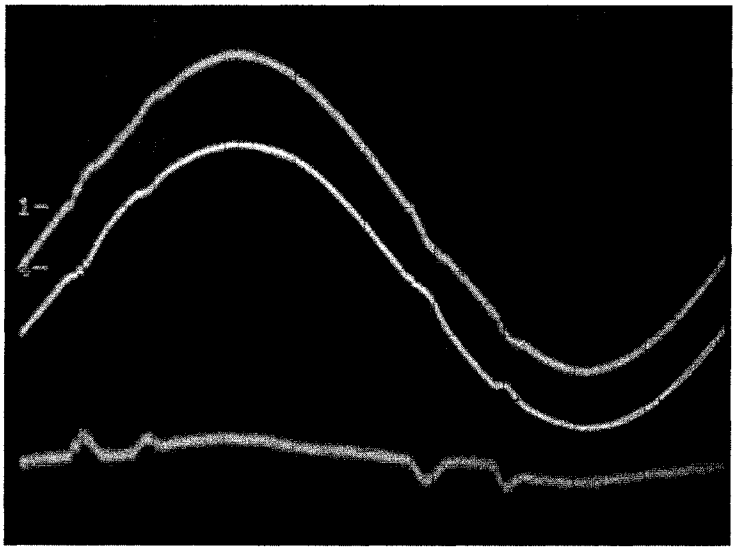
Comparing Figure 4.19 with Figure 4.20, we can find the influence of the current sharing controller to the system. Due to lower crossover frequency of loop gain of the current sharing controller of (4-10), the output currents of both inverters shown in Figure 4.19 have slow response to the disturbance, thus the waveforms of the output currents have obvious perturbation. On the contrary, the waveforms of the output currents shown in Figure 4.20 are smoother because we apply a faster current sharing controller on the system. Figure 4.21 is the waveforms of the three-inverter system. We can see that the current sharing controller of (4-11) also has good current sharing performance on the three-inverter system. These results are coincident with the simulation results shown in Figure 4.9, Figure 4.11, and Figure 4.14.

From Figure 4.22 to Figure 4.24, we can find that although the current sharing controllers are different, and the numbers of the parallel inverters are different, the dynamic responses of the system's output voltage and current are similar. This confirms that under stable parallel operation, the voltage regulation of the whole system depends on voltage-regulating capability of the individual inverter.

Even under nonlinear loading condition, the multi-inverter system with instantaneous average-current-sharing scheme also shows its good performance. The waveforms are shown in Figure 4.25. The load is a full-wave bridge-rectifier connected directly to a 660μF capacitor in parallel with a 50Ω resistor. Although the load current draws a very high strike and generates many harmonics, the load current is shared by two inverters equally.

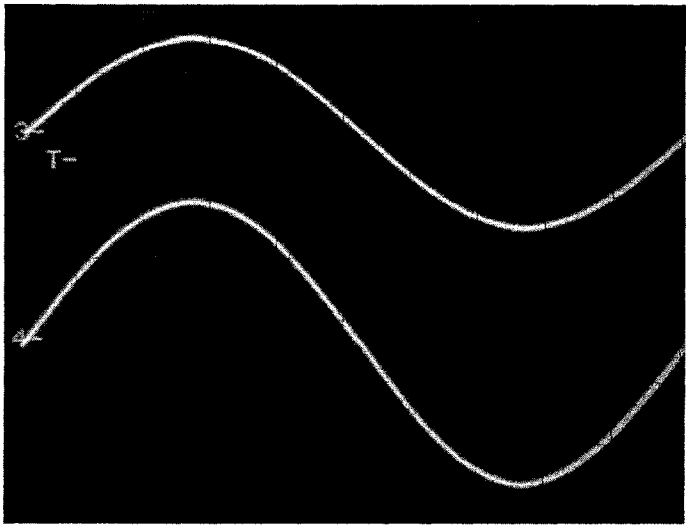


(a)

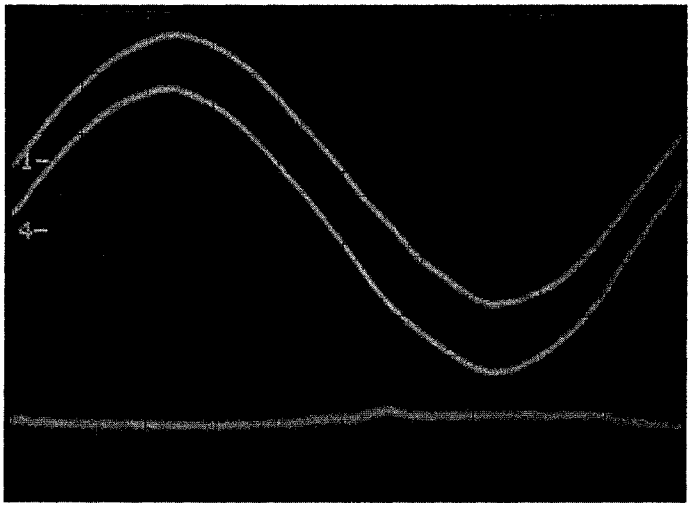


(b)

Figure 4.19 Steady-state response of the two-inverter system with the current sharing controller of (4-10). (a). output voltage (upper: 100V/div) and output current (lower: 10A/div); (b). current of both inverters (upper: 5A/div) and current error between them (bottom: 5A/div).

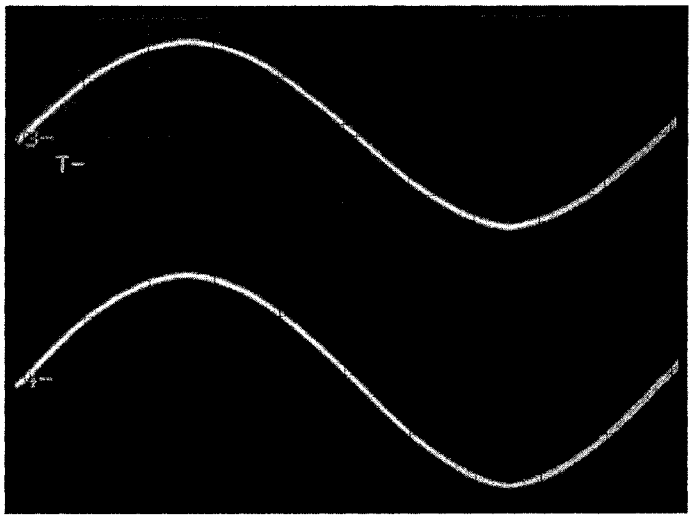


(a)

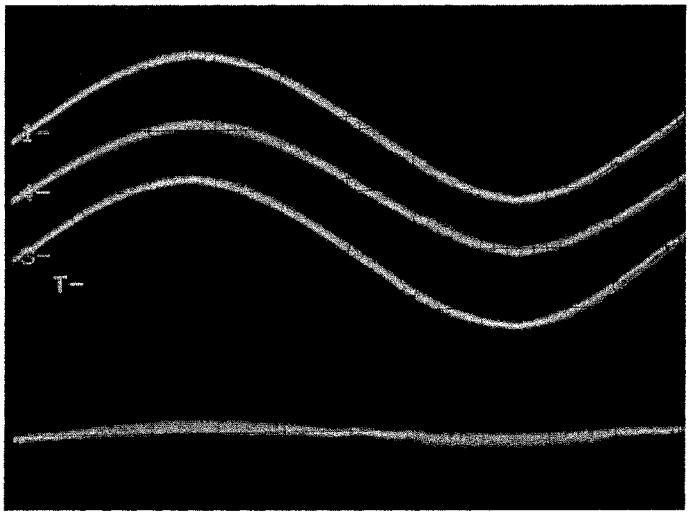


(b)

Figure 4.20 Steady-state response of the two-inverter system with the current sharing controller of (4-9). (a). output voltage (upper: 100V/div) and output current (lower: 10A/div); (b). current of both inverters (upper: 5A/div) and current error between them (bottom: 5A/div).

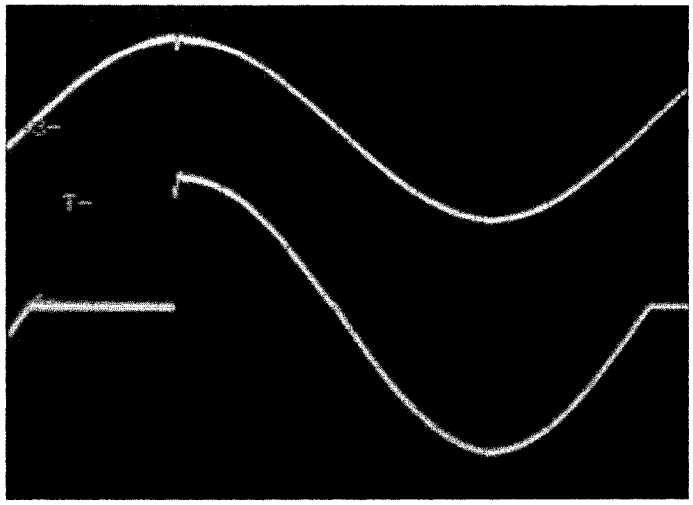


(a)

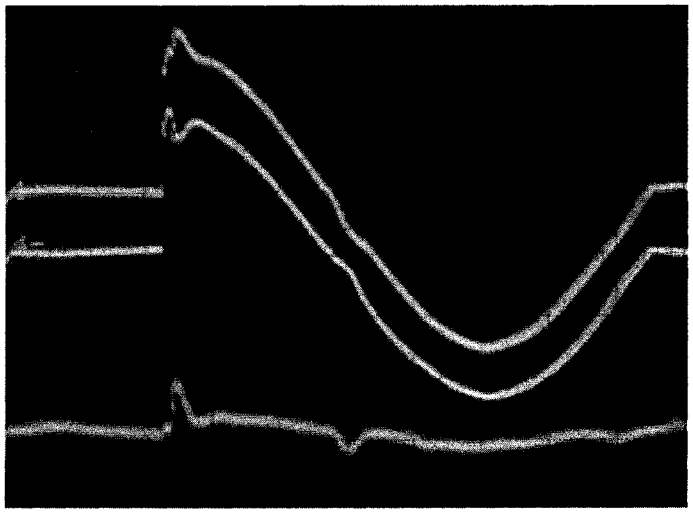


(b)

Figure 4.21 Steady-state response of the three-inverter system with the current sharing controller of (4-9). (a). output voltage (upper: 100V/div) and output current (lower: 20A/div); (b). current of all inverters (upper: 10A/div) and current error between first and second inverter (bottom: 10A/div).

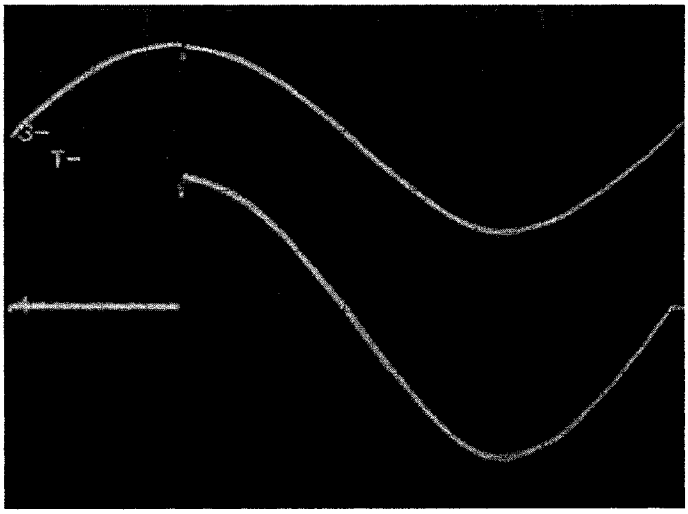


(a)

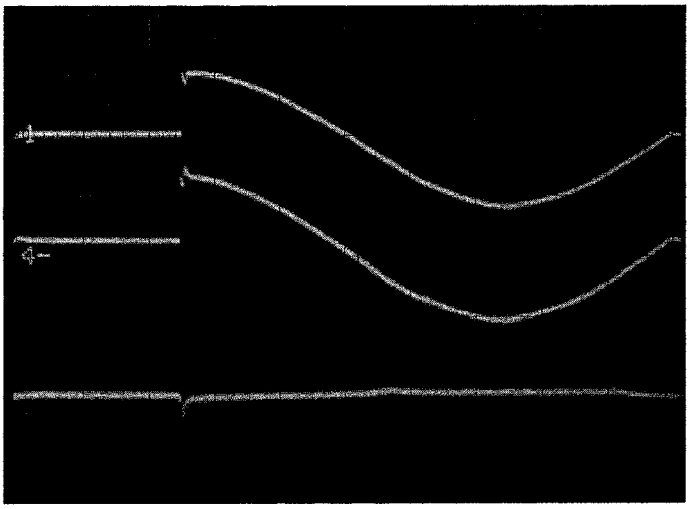


(b)

Figure 4.22 Dynamic response of the two-inverter system with the current sharing controller of (4-10). (a). output voltage (upper: 100V/div) and output current (lower: 10A/div); (b). current of both inverters (upper: 5A/div) and current error between them (lower: 5A/div).

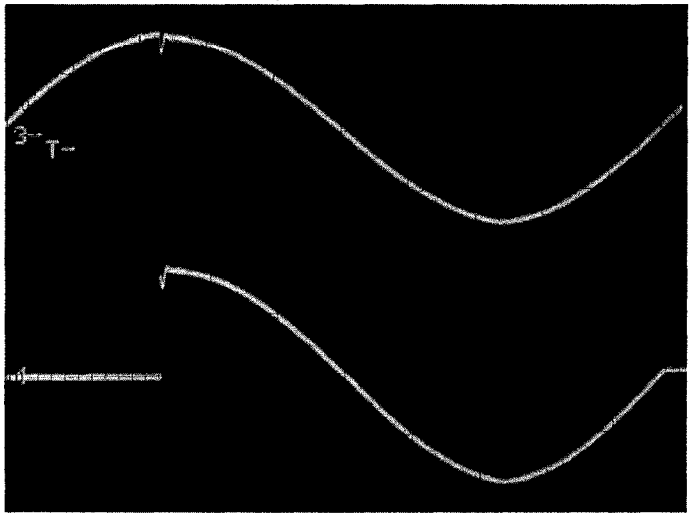


(a)

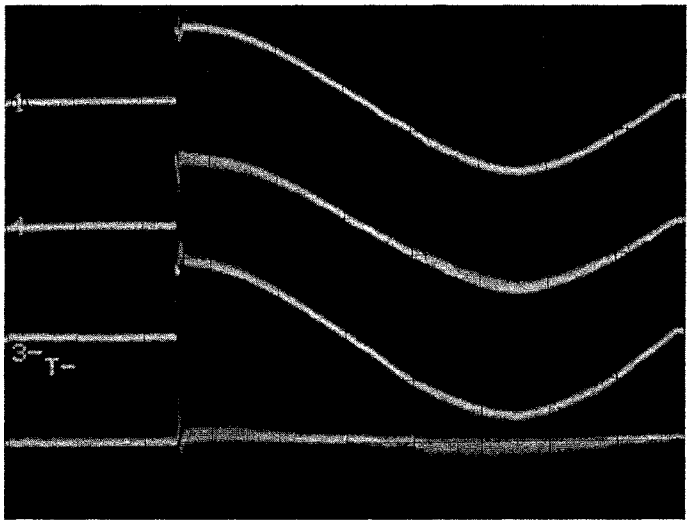


(b)

Figure 4.23 Dynamic response of the two-inverter system with the current sharing controller of (4-9). (a). output voltage (upper: 100V/div) and output current (lower: 10A/div); (b). current of both inverters (upper: 10A/div) and current error between them (lower: 10A/div).

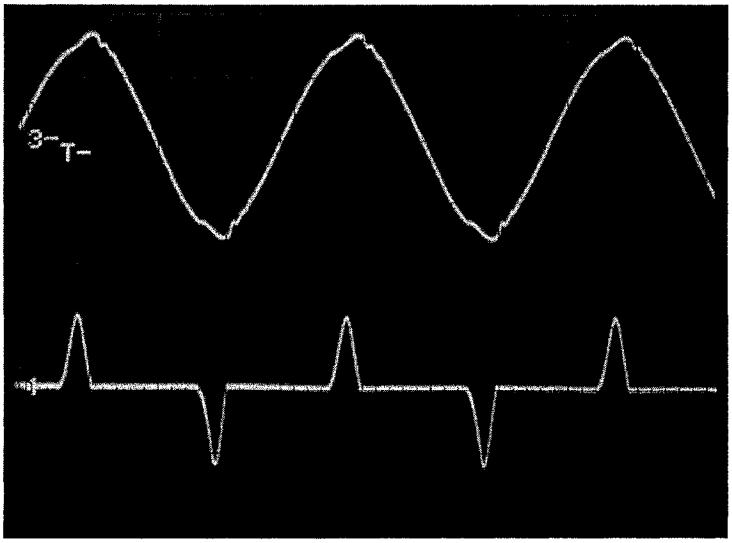


(a)

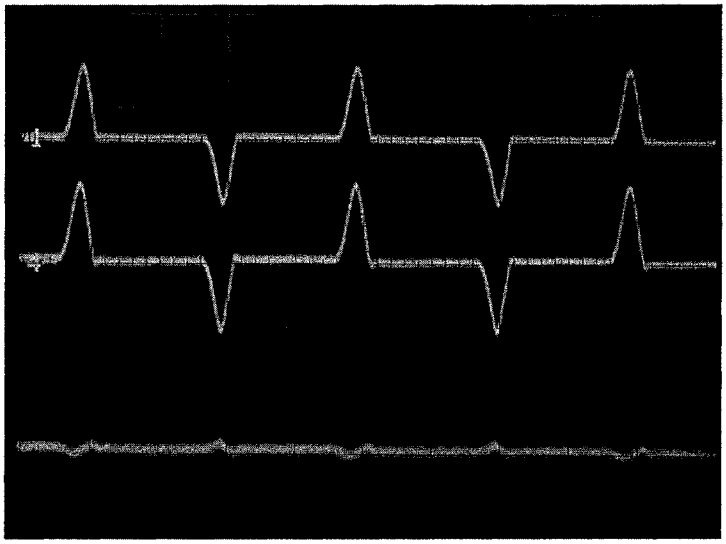


(b)

Figure 4.24 Dynamic response of the three-inverter system with the current sharing controller of (4-9). (a). output voltage (upper: 100V/div) and output current (lower: 20A/div); (b). current of both inverters (upper: 10A/div) and current error between first and second inverter (lower: 10A/div).



(a)



(b)

Figure 4.25 Response of the three-inverter system with the current sharing controller of (4-9) for rectifier-type load. (a). output voltage (upper: 100V/div) and output current (lower: 20A/div); (b). current of both inverters (upper: 10A/div) and current error between first and second inverter (lower: 10A/div).

4.6 Conclusion

In this Chapter, a multi-inverter system with instantaneous average-current-sharing scheme is discussed. By introducing a disturbance source to represent all the sources that may cause the current unbalance, a model of the system can be easily built. Through the analysis of the model, the following conclusions are drawn.

- GH/Z_T can be treated as the loop gain of the current-sharing loop in the evaluation of the stability and performance of the current-sharing controller, where G is the transfer function of individual inverter with voltage-feedback loop closed but current-sharing loop opened, H is the transfer function of the current-sharing controller, and Z_T is the equivalent output impedance of individual inverter, plus the line impedance that connects the output of the inverter to the common connection point.

- Z_T/nZ_L is the impedance characteristic of the multi-inverter system. The term $(1+Z_T/nZ_L)$ should have all its roots on the left-half plane to ensure system stability. A conservative requirement is that Z_T/n should be much smaller than Z_L at all frequencies.

- Under stable parallel operation, the voltage regulation of the whole system depends on the voltage-regulating capability of the individual inverter.

Three experimental 110Vac/1.1KVA inverters are built. The experimental results show a good performance and verify the theoretical predictions.

Chapter 5

A State Feedback Controller for Parallel Multi-Inverter Systems

5.1 Introduction

A multi-inverter system consists of several inverters. With an increasing number of paralleled inverters, the dimension of the system increases rapidly. This brings difficulties to the modeling, design, and evaluation of e the system. In this Chapter, we apply the optimal control methodology, developed by Anderson and Moore [85], to the design of the feedback loops of parallel multi-inverter systems. The control signals thus obtained will minimize a performance index, which is a function of the output voltage error, the inductor currents of all inverters and the reference signals. This enables the controller to achieve some desired objectives like minimization of the circulating current and reduction of error of the output voltage.

We find that the proposed controller has the following advantages: 1). It is robust to the change in the number of inverters. By applying the frequency domain analysis to the multi-inverter system with the proposed controller, the performances on current sharing and transient output voltage (indicated by the output impedance) depend only

slightly on the number of inverters. Thus, we can design a state feedback controller based on a fixed number of inverters and use the controller for systems with variable number of paralleled inverters without re-designing the controller. 2). It requires only one common signal line to share the information on the total current. The common circuits of the system are shrunken to be a current sense and a conducting wire. Thus, the state feedback controller for the multi-inverter system is simple not only in design but also in hardware implementation. The reliability of the whole system is greatly improved compared with methodologies in which the sharing bus carries information on the average current or the highest current. Simulations are carried out to investigate the performance of the system and to verify the analytical results. Three experimental 110Vac/1.1KVA inverters are built and paralleled to verify the theoretical predictions.

5.2 Modeling of a Multi-Inverter System

A voltage source SPWM inverter can be modeled as a controlled ac source followed by an output LC filter as introduced in Chapter 2. It is assumed that the switching frequency of the inverter is much higher than the fundamental frequency of the output voltage, so that the switching-frequency component can be ignored in the low frequency analysis. Therefore, n paralleled inverters can be modeled as shown in Figure 5.1. In this model, M_i is the gain of the SPWM. d_i is the duty ratio. L_i, R_i and C_i, are the inductance, resistance and capacitance of the output filter of the ith inverter, respectively (i=1, 2, ..., n). Z_{pi} is impedance of the cable between the output point of the ith inverter and the common connection point. For simplicity of analysis and design, the line impedances Z_{pi} are set to zero in the following equations. However, in the simulation, different values of Z_{pi} will be introduced to the inverters to verify the

performance of the optimal controller. Assuming a resistive load R_L, the state-space form of an n paralleled inverters system is:

$$\frac{d}{dt}\begin{bmatrix} i_{l1} \\ i_{l2} \\ \vdots \\ i_{ln} \\ v_o \end{bmatrix} = \begin{bmatrix} -\frac{R_1}{L_1} & 0 & \cdots & 0 & -\frac{1}{L_1} \\ 0 & -\frac{R_2}{L_2} & \cdots & 0 & -\frac{1}{L_2} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \cdots & -\frac{R_n}{L_n} & -\frac{1}{L_n} \\ \frac{1}{C_L} & \frac{1}{C_L} & \cdots & \frac{1}{C_L} & -\frac{1}{C_L R_L} \end{bmatrix} \begin{bmatrix} i_{l1} \\ i_{l2} \\ \vdots \\ i_{ln} \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{M}{L_1} & 0 & \cdots & 0 \\ 0 & \frac{M}{L_2} & \cdots & 0 \\ \vdots & & \ddots & \vdots \\ 0 & 0 & \cdots & \frac{M}{L_n} \\ 0 & 0 & \cdots & 0 \end{bmatrix} \begin{bmatrix} d_1 \\ d_2 \\ \vdots \\ d_n \end{bmatrix} \quad (5\text{-}1)$$

where $C_L = C_1 + C_2 + \cdots + C_n$. In order to improve the steady-state performance of the output voltage, an integrator is inserted into the system. Let e_v be the state describing the integration of output error, that is

$$\dot{e}_v = v_r - v_o \quad (5\text{-}2)$$

where $v_r = V_m \sin \omega_r t$ is the voltage reference in an inverter system, which is a sinusoidal wave with amplitude V_m and angular frequency ω_r. Hence, the state-space equation of the n paralleled multi-inverter system can be described as

$$\dot{x} = Ax + Bu + B_w$$

$$y = v_o = Cx \quad (5\text{-}3)$$

where $x = \begin{bmatrix} e_v \\ i_{l1} \\ i_{l2} \\ \vdots \\ i_{ln} \\ v_o \end{bmatrix}$, $u = \begin{bmatrix} d_1 \\ d_2 \\ \vdots \\ d_n \end{bmatrix}$, $A = \begin{bmatrix} 0 & 0 & 0 & \cdots & 0 & -1 \\ 0 & -\frac{R_1}{L_1} & 0 & \cdots & 0 & -\frac{1}{L_1} \\ 0 & 0 & -\frac{R_2}{L_2} & \cdots & 0 & -\frac{1}{L_2} \\ \vdots & \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & \cdots & -\frac{R_n}{L_n} & -\frac{1}{L_n} \\ 0 & \frac{1}{C_L} & \frac{1}{C_L} & \cdots & \frac{1}{C_L} & -\frac{1}{C_L R_L} \end{bmatrix}$,

$B = \begin{bmatrix} 0 & 0 & \cdots & 0 \\ \frac{M}{L_1} & 0 & \cdots & 0 \\ 0 & \frac{M}{L_2} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \frac{M}{L_n} \\ 0 & 0 & \cdots & 0 \end{bmatrix}$, $B_w = \begin{bmatrix} v_r \\ 0 \\ \vdots \\ 0 \end{bmatrix}$, $C = \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 0 \\ 1 \end{bmatrix}$.

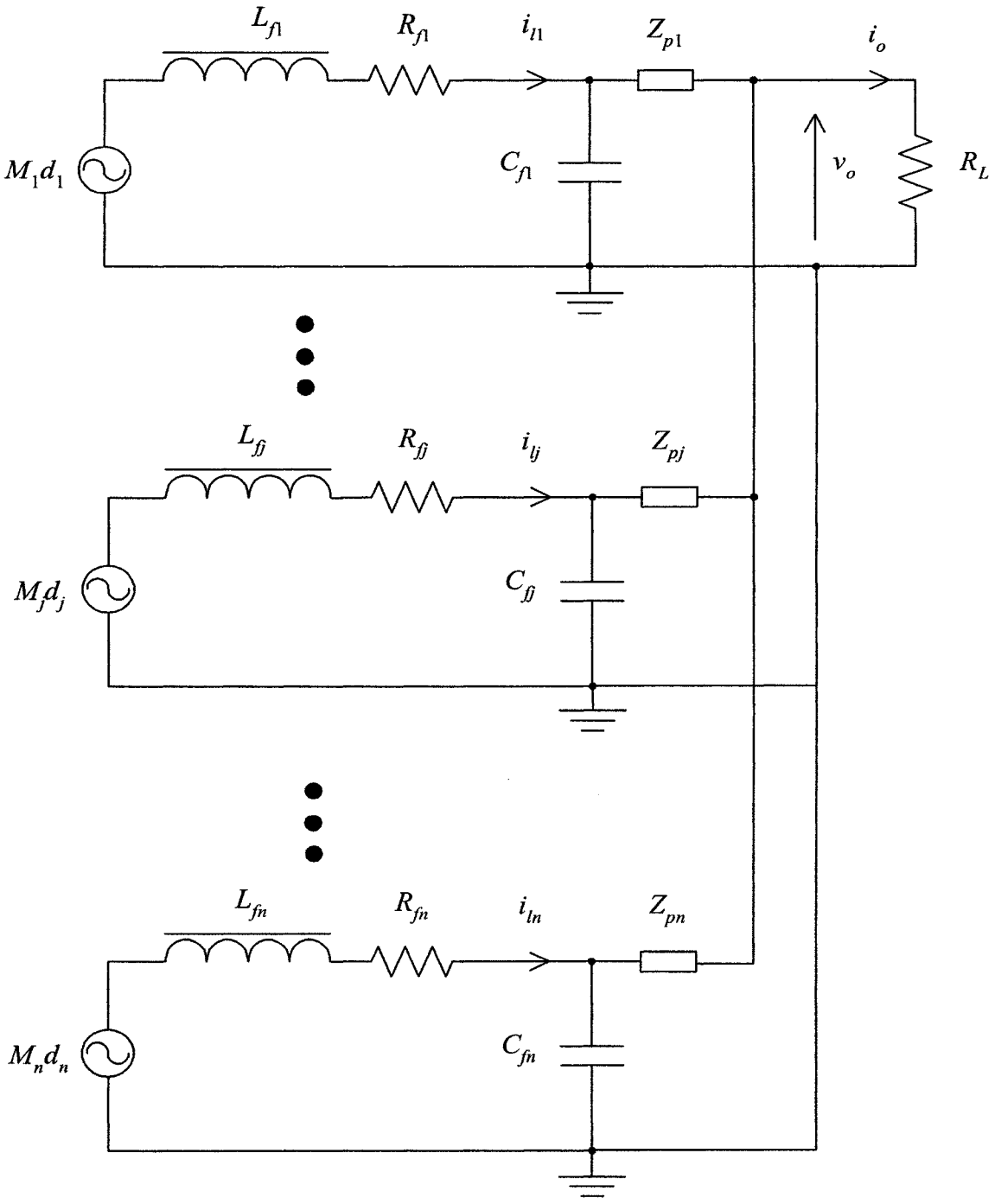


Figure 5.1 Model of n paralleled inverters.

(5-2) and (5-3), together with Figure 5.1, form a complete model of the multi-inverter system.

5.3 Optimal Control

The goal of the proposed optimal controller is to optimize the performance of the output voltage and inductor currents of the multi-inverter system as described by (5-3), with respect to a performance index selected by the designer. By solving a Riccati equation, which is determined by the matrix of the system equation and the performance index, a set of feedback gains can be obtained. By using a common state-feedback controller with these feedback gains, the closed-loop system can achieve an optimal control. In this section, the equations required to determine the feedback gains will be found. Then the relationship between the performance index and the performance of the output voltage and inductor currents will be examined in Sub-section 5.3.3. The selection of the performance index to minimize the circulating current will be discussed in Sub-section 5.3.4.

5.3.1 Augmented System

If the optimal control methodology is directly applied to the *n*-paralleled multi-inverter system described by (4-3), the performance index can be

$$J_p = \frac{1}{2}\int_0^\infty \left[u^T W u + x^T Q_1 x + (v_r - y)^T Q_2 (v_r - y)\right] dt \tag{5-4}$$

where $W \in \Re^{n\times n}$, $Q_1 \in \Re^{(n+2)\times(n+2)}$, and $Q_2 \in \Re^{1\times 1}$ are symmetric matrices with non-negative eigenvalues fixed by the designer (as discussed in Sub-section 5.3.3). However, the above method is for the regulator problem only. Since the output voltage of an inverter system should follow a sinusoidal wave, its control is a tracking problem. Therefore, the first step in the design is to reduce this tracking problem to a regulator

problem. In addition to the n paralleled multi-inverter system described by (5-3), we introduce an augmented system describing the voltage reference as follows:

$$\dot{z} = A_Z z \tag{5-5}$$

$$v_r = C_Z^T z \tag{5-6}$$

where $z = \begin{bmatrix} v_r \\ \dot{v}_r \end{bmatrix}$, $A_Z = \begin{bmatrix} 0 & 1 \\ -\omega_r^2 & 0 \end{bmatrix}$, $C_Z = \begin{bmatrix} 1 \\ 0 \end{bmatrix}$. By combining the augmented system with the n-paralleled multi-inverter system described by (5-3), we have

$$\dot{z}_C = A_C z_C + B_C u \tag{5-7}$$

where $z_C = \begin{bmatrix} x \\ z \end{bmatrix}$, $A_C = \begin{bmatrix} A & A_1 \\ 0 & A_Z \end{bmatrix}$, $B_C = \begin{bmatrix} B \\ 0 \end{bmatrix}$. $A_1 = \begin{bmatrix} C_Z & A_2 \end{bmatrix}^T$, $A_2 = \begin{bmatrix} 0 & 0 & \cdots & 0 \\ 0 & 0 & \cdots & 0 \end{bmatrix}$.

Now, with reference to the new system (5-7), it has been derived in [85] that the performance index is

$$J = \frac{1}{2}\int_0^\infty \left[u^T W u + z_C^T Q_C z_C\right] dt \tag{5-8}$$

where $Q_C = \begin{bmatrix} Q & -QC(C^TC)^{-1}C^T \\ -C_Z(C^TC)^{-1}C^TQ & C_Z(C^TC)^{-1}C^TQC(C^TC)^{-1}C_Z^T \end{bmatrix}$,

$Q = \left[I - C(C^TC)^{-1}C^T\right]^T Q_1 \left[I - C(C^TC)^{-1}C^T\right] + CQ_2C^T$.

The standard result of optimal control can be obtained from [85] as follows,

$$u = -K_a z_C \tag{5-9}$$

$$K_a = W^{-1}B_C P$$

where P is the solution of the Riccati equation,

$$PA_C + A_C^T P - PB_C W^{-1} B_C^T P + Q = 0 \tag{5-10}$$

5.3.2 Solving for the Riccati Equation

Although the Riccati equation is of high order and appears complex, it can be easily solved by numerical tools like MATLAB, which already has built-in functions[1] to find the solution P. (A new function dedicated to the proposed optimal control for a multi-parallel inverter system has been written and included in the Appendix C.) However, since A_C is not asymptotically stable due to the presence of a pair of poles lying on the imaginary axis introduced by A_Z, in order to use MATLAB, we have to modify A_z to

$$A_Z = \begin{bmatrix} 0 & 1 \\ -\omega_r^2 & -\varepsilon \end{bmatrix}, \tag{5-11}$$

where ε is a small positive constant. Here, the reference signal will eventually decay to zero and the system will become asymptotically stable. By setting ε small, the decay is made slow. Although the gains found for this modified system have a discrepancy as compared with that of using the unmodified system, the discrepancy results in only negligible effect.

5.3.3 Relationship Between Performance Index and Performance

This sub-section aims at exploring the relationship between the performance index J and the performance of the output voltage and inductor currents. If the interactions among the states are not considered, (i.e., J is a function of x_i^2 but not $x_i x_j$ for $i, j \in [1,$

[1] Use the MATLAB function "are.m" in the control system toolbox to solve for the algebraic Riccati equation.

n+2]), the matrix Q of the performance can be decomposed into three matrices which are related to the performance of the output voltage and inductor currents.

First, we decompose Q_1 as follows:

$$Q_1 = \begin{bmatrix} Q_{11} & Q_{21} \\ Q_{12} & Q_{22} \end{bmatrix},$$

where $Q_{11} \in \Re^{(n+1)\times(n+1)}$, $Q_{21} \in \Re^{(n+1)\times 1}$, $Q_{12} \in \Re^{1\times(n+1)}$, and. $Q_{22} \in \Re^{1\times 1}$. Substitute C = [0 0 ... 0 1]^T and C_z = [1 0]^T into (5-8), we have

$$Q = \begin{bmatrix} Q_{11} & 0 \\ 0 & Q_2 \end{bmatrix}. \tag{5-12}$$

We further decompose Q_{11} as follows:

$$Q_{11} = \begin{bmatrix} Q_e & 0 \\ 0 & Q_i \end{bmatrix}, \; Q_e \in \Re^{1\times 1}, \; Q_i \in \Re^{n\times n}. \tag{5-13}$$

Substituting (5-12), (5-13), $C = [0 \; 0 \; \ldots \; 0 \; 1]^T$ into (5-8),

$$\begin{aligned} J &= \frac{1}{2}\int_0^\infty \left[u^T W u + x^T Q x + v_r Q_2 v_r - 2Q_2 v_r y\right] dt \\ &= \frac{1}{2}\int_0^\infty \left[u^T W u + e_v Q_e e_v + [i_1 \;\; i_2 \;\; \ldots \;\; i_n] Q_i [i_1 \;\; i_2 \;\; \ldots \;\; i_n]^T + y Q_2 y + v_r Q_2 v_r - 2Q_2 v_r y\right] dt \\ &= \frac{1}{2}\int_0^\infty \left[u^T W u + e_v Q_e e_v + [i_1 \;\; i_2 \;\; \ldots \;\; i_n] Q_i [i_1 \;\; i_2 \;\; \ldots \;\; i_n]^T + (v_r - y) Q_2 (v_r - y)\right] dt \end{aligned} \tag{5-14}$$

It can be seen from the above performance index J that Q_i specifies the performance of i_{l1}, i_{l2}, ..., i_{ln}. Q_e and Q_2 specify the output regulation performance of the system. Hence, designers can make a trade-off to weight the performance between good voltage regulation and good current control by selecting Q_e and Q_2 (which are scalar quantities).

5.3.4 Minimize Circulating Current

One design objective of the multi-inverter system is to share currents equally among all inverters. One method to design a system to achieve this objective is to select Q_i as an identity matrix, as be shown in the following derivation.

Let f be a function consisting of all current components within the performance index, that is,

$$\begin{aligned} f &= [i_{l1} \quad i_{l2} \quad \cdots \quad i_{ln}]Q_i[i_{l1} \quad i_{l2} \quad \cdots \quad i_{ln}]^T \\ &= i_{l1}^2 + i_{l2}^2 + \cdots + i_{ln}^2 \end{aligned} \tag{5-15}$$

From Figure 5.1,

$$i_{l1} + i_{l2} + \cdots + i_{ln} = \frac{v_o}{R_L} + C_L \frac{dv_o}{dt} = i \tag{5-16}$$

where i is equal to the load current plus currents in all the filter capacitors. Then let

$$g = i_{l1} + i_{l2} + \cdots + i_{ln} - i\,.$$

To minimize f subject to a constraint g, we apply the Lagrange multiplier method [86]. Let λ be a Lagrange multiplier so the following equation can be obtained,

$$\frac{\partial}{\partial i_{lk}}(f + \lambda g) = 0,$$

$$2i_{lk} + \lambda = 0 \tag{5-17}$$

for $k = 1, 2, \ldots, n$.

$$\frac{\partial}{\partial \lambda}(f + \lambda g) = 0$$

$$i_{l1} + i_{l2} + \cdots + i_{ln} - i = 0\,. \tag{5-18}$$

Summing up all equations of (5-17),

$$2(i_{l1} + i_{l2} + \cdots i_{ln}) + n\lambda = 0$$

From (5-18),

$$\lambda = -\frac{2i}{n} \tag{5-19}$$

Substitute (5-19) into (5-17), we obtain $2i_{lk} - \frac{2i}{n} = 0$, so

$$2i_{lk} = \frac{2i}{n}. \tag{5-20}$$

The solution that (5-15) is of minimum subjects to the constrain (5-16) is

$$i_{l1} = i_{l2} = \cdots = i_{ln} = \frac{1}{n} i \tag{5-21}$$

Recall that the aim of the optimal controller is to minimize the performance index. Thus, by selecting Q_i=I, where I is the identity matrix, we can obtain (5-21) which implies a minimization of the circulating current.

5.4 Design Example and Simulation

5.4.1 Design Step

(5-9) is the control law of the proposed controller, we rewrite (5-9) as

$$u = -K_a z_C = -K_a \begin{bmatrix} x \\ z \end{bmatrix} = -K_a \begin{bmatrix} e_v & i_{l1} & i_{l2} & \cdots & i_{ln} & v_o & v_r & \dot{v}_r \end{bmatrix}^T \tag{5-22}$$

The term $\dot{v}_r$ is for augmented system and its coefficient is very small so that it can be omitted. Considering $u = [d_1 \quad d_2 \quad \cdots \quad d_n]^T$, we can obtain the expression of the duty ratio of the switches of each inverter in the multi-inverter system, as described in (5-23).

$$d_j = -K_{ev} e_v - K_v v_o - \sum_{m=1}^{n} K_{im} i_{lm} - K_r v_r \tag{5-23}$$

where K_{ev}, K_r, K_{ij} ($j = 1, \cdots, n$), and K_v are elements of K_a.

The solution of K_a can be obtained easily by using software tools like MATLAB [52]. A MATLAB function is written to find the feedback gain matrix K, which is listed in Appendix C.

As a summary, the design steps for a state-feedback controller of a multi-inverter system are as follows:

1. Model the multi-inverter system. According to the parameters of the system, set up the state-space description of the system (5-3).
2. Build up the augmented system based on the model set up in step 1. The augmented system is described by (5-5) and (5-6).
3. According to the desired performance, select proper W, Q_1 and Q_2 to determine the performance index described by (5-8).
4. Solve the Riccati equation (5-10) to find the gain matrix K_a (using the function listed in Appendix C). The controller of the j-th inverter has the structure of (5-23). Because the feedback gains for the inductor currents of other inverters are the same (K_{ilo}), the control law for the j-th inverter can be described as (assuming that the currents in the filter capacitors are very small):

$$
\begin{aligned}
d_j &= -K_{ev}e_v - K_r v_r - K_v v_o - K_{ij} i_j - K_{ilo} \sum_{\substack{m=1 \\ m \neq j}}^{n} i_{lm} \\
&= -K_{ev}e_v - K_r v_r - K_v v_o - (K_{ij} - K_{ilo}) i_j - K_{ilo} \sum_{m=1}^{n} i_{lm} \\
&\approx -K_{ev}e_v - K_r v_r - K_v v_o - (K_{ij} - K_{ilo}) i_j - K_{ilo} (\sum_{m=1}^{n} i_{lm} + C_L \frac{dv_o}{dt}) \\
&= -K_{ev}e_v - K_r v_r - K_v v_o - K_i i_j - K_{io} i_o
\end{aligned}
\tag{5-24}
$$

From (5-24), it is found that only a common signal line that carries a signal of the load current is needed. The complex interconnections among the inverters are avoided. Such a structure has notable advantages — simplicity and reliability. The reliability of the whole system is increased as well. A diagram of the controller of *j-th* inverter is depicted in Figure 5.2.

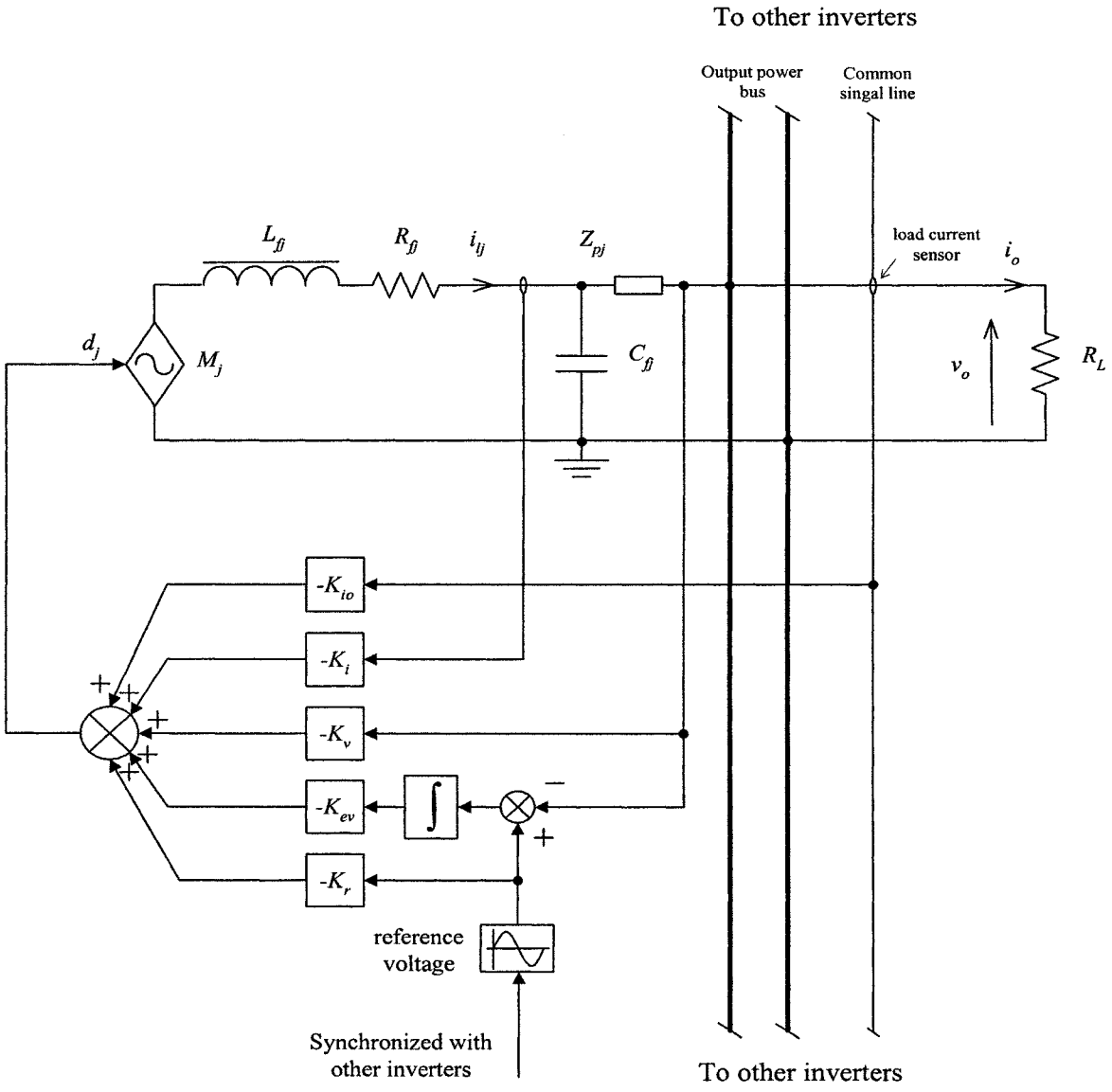


Figure 5.2 Diagram of proposed state-feedback controller for j-th inverter of the multi-inverter system.

5.4.2 Simulations

In this sub-section, we use PSpice to simulate a parallel multi-inverter system to investigate the performance of the proposed controller. The individual inverter of the parallel multi-inverter system has the nominal parameters as listed in Table 5.1. These

parameters will be used throughout the last part of this Chapter. A full-bridge inverter is employed as the core of the ac/dc inverter.

Parameters	Values	Unit
Output filter inductor, $L_{f1,2}$	1	mH
Resistance of the filter inductor, $R_{f1,2}$	0.2	Ω
Output filter capacitor, $C_{f1,2}$	20	μF
Switching frequency of the inverter, f_s	40	kHz
Input dc voltage, V_{dc}	300	V
Rated load of a single inverter	10	Ω
Rated output voltage, v_o	110	Vrms
Output voltage frequency	50	Hz

Table 5.1 Parameter list

Following the design step introduced in Sub-section 5.4.1, let us consider a two-inverter system, with W=2, $Q_1 = \begin{bmatrix} 2e7 & 0 & 0 \\ 0 & 50 & 0 \\ 0 & 0 & 50 \end{bmatrix}$, and Q_2=50. The gain matrix is calculated as $K_a = \begin{bmatrix} -2236 & 9.1 & 4.3 & 1.6 & -3.9 & -8.1^{-4} \\ -2236 & 4.3 & 9.1 & 1.6 & -3.9 & -8.1^{-4} \end{bmatrix}$. Thus, the control law can be described as

$$d_j = \frac{2236}{s}(v_r - v_o) - 4.8i_j - 4.3i_o - 1.6v_o + 3.9v_r \qquad (5\text{-}25)$$

We simulate a two-inverter system with the proposed controller using PSpice. In order to perturb the system, the two inverters are assumed to have different L-C filters. One had the nominal values as listed in Table 5.1, and the other has an inductance of 1.2mH and a capacitance of 17μF. In addition, different line impedances are added into the inverters. Because the fundamental (AC) frequency of the output voltage is quite low (50Hz), the line impedance is mainly resistive. We set Z_{p1}=0.03Ω for the first inverter, and Z_{p2}=0.01Ω for the second inverter. Without current-sharing control, the output currents of the two inverters would be largely different due to the different parameters and line impedances.

Figure 5.3 shows PSpice simulation results of the proposed controller. When the output is open-circuited (no load), the RMS value of the output voltage is 115.3V. At t = 45ms, a 5Ω load (rated load) is connected. The RMS of the output voltage then falls to 109.7V. The voltage regulation from no load to the rated load is within ±5%. The transient response from no load to full load is quite fast. The peak value of the current unbalance is about 1.1A, which is about 7.2% of the output current of the individual inverter.

From the simulations, the performance of the proposed controller has been verified. The proposed controller can achieve not only good voltage regulation, but also good current sharing among the inverters.

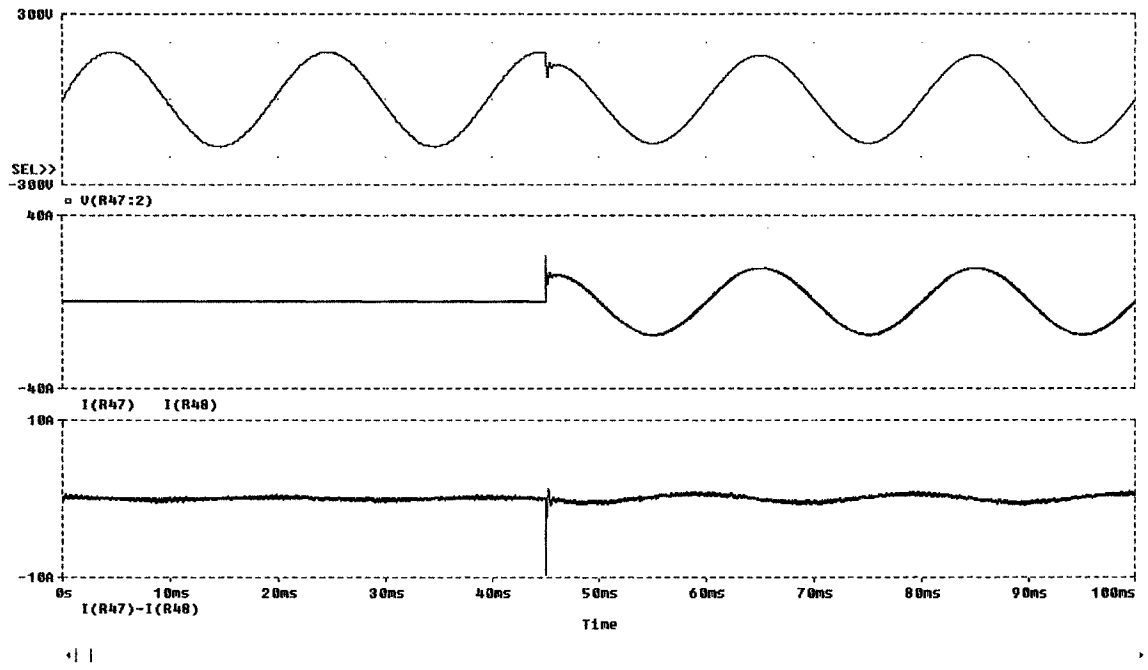


Figure 5.3 Simulation results of a two-inverter system when load changes from open circuit (no load) to 5Ω. Top: the output voltage, Middle: the output currents of individual inverter. Bottom: the output current difference between two inverters.

5.5 Robustness of the Proposed Controller

During the normal operation of the multi-inverter system, the number of paralleled inverters may be changed. For example, if one inverter fails, it may be removed from the system. Additional inverters may also be added into the system. In this section, we shall show that the proposed state-feedback controller is robust to the change in the number of paralleled inverters. Despite of the fact that the feedback gains are designed for a fixed number of inverters, the system can still perform well for different numbers of paralleled inverters. A frequency domain analysis will be carried out to analyze the multi-inverter system. It is proved that with the specified gains of the

proposed controller (e.g., a set of gains designed for a two-inverter case), increasing or decreasing the number of the paralleled inverters will produce little effect on the performance of the multi-inverter system.

The control laws derived in last section can be described as

$$d_j = -\frac{K_{ev}}{s}(v_r - v_o) - K_r v_r - K_v v_o - K_i i_j - K_{io} i_o \tag{5-26}$$

The following equations then describe the system shown in Figure 5.1.

$$\begin{aligned}
&M[-\frac{K_{ev}}{s}(v_r - v_o) - K_r v_r - K_v v_o - K_i i_{l1} - K_{io} i_o] - v_o = i_{l1}(L_{f1}s + R_{f1}) \\
&M[-\frac{K_{ev}}{s}(v_r - v_o) - K_r v_r - K_v v_o - K_i i_{l2} - K_{io} i_o] - v_o = i_{l2}(L_{f2}s + R_{f2}) \\
&\qquad\qquad \vdots \\
&M[-\frac{K_{ev}}{s}(v_r - v_o) - K_r v_r - K_v v_o - K_i i_{ln} - K_{io} i_o] - v_o = i_{ln}(L_{fn}s + R_{fn}) \\
&i_{l1} + i_{l2} + \cdots + i_{ln} - v_o C_L s = i_o
\end{aligned} \tag{5-27}$$

Two key issues of the multi-inverter system, current sharing and voltage regulation, are investigated in following two sub-sections based on the model (5-27).

5.5.1 Current Sharing

By introducing the concept of disturbance source raised in last Chapter, we can use a disturbance source to represent all the deviations of an inverter from the nominal one, then other parameters can be considering as the same. Therefore, (5-27) becomes

$$
\begin{aligned}
&M[-\frac{K_{ev}}{s}(v_r - v_o) - K_r v_r - K_v v_o - K_i i_{l1} - K_{io} i_o] - v_o = (i_{l1} - i_{d1})(L_f s + R_f) \\
&M[-\frac{K_{ev}}{s}(v_r - v_o) - K_r v_r - K_v v_o - K_i i_{l2} - K_{io} i_o] - v_o = (i_{l2} - i_{d2})(L_f s + R_f) \\
&\qquad\qquad \vdots \\
&M[-\frac{K_{ev}}{s}(v_r - v_o) - K_r v_r - K_v v_o - K_i i_{ln} - K_{io} i_o] - v_o = (i_{ln} - i_{dn})(L_f s + R_f) \\
&\qquad\qquad i_{l1} + i_{l2} + \cdots + i_{ln} - v_o C_L s = i_o
\end{aligned}
\tag{5-28}
$$

where $i_{d1}, \cdots i_{dn}$ are the disturbance source.

Subtracting the k-th from the j-th equation in (5-28), we obtain

$$
i_{lk} - i_{lj} = (i_{dj} - i_{dk}) \frac{L_f s + R_f}{L_f s + R_f + K_i}, (1 \le j, k \le n, j \ne k) \tag{5-29}
$$

It shows that the current unbalance between any two inverters is independent of the number of paralleled inverters, and is related to the statuses of these two inverters. For a given set of feedback gains, the current unbalance is fixed (independent of the number of parallel inverters).

5.5.2 Voltage Regulation

The equivalent output impendence is an important specification of a UPS. An ideal UPS inverter should have zero output impendence so that the output voltage would have zero steady-state error under all loading conditions, and have fast transient response under transient loading conditions. In this sub-section, the equivalent output impendence of the system is discussed. The objective is to investigate the voltage regulation when the number of paralleled inverters is changed.

We first assume that the parameters of all the inverters in the system are the same. Namely, $L_{f1} = L_{f2} = \cdots = L_{fn} = L_f$, $R_{f1} = R_{f2} = \cdots = R_{fn} = R_f$, and $C_{f1} = C_{f2} = \cdots = C_{fn} = C_f$.

In (5-27), by inserting the summation of the first n equations into the last equation, and letting $v_r = 0$, the equivalent output impendence of the system (5-27) is derived.

$$-\frac{v_o}{i_o}\bigg|_{v_r=0} = \frac{1}{n}\left(\frac{s(L_f s + K_i + nK_{io} + R_f)}{L_f C_f s^3 + C_f(R_f + K_i)s^2 + (K_v + 1)s - K_{ev}}\right) \tag{5-30}$$

Let $D(s) = L_f C_f s^3 + C_f(R_f + K_i)s^2 + (K_v + 1)s - K_{ev}$ be the denominator of (5-30). We then have

$$-\frac{v_o}{i_o}\bigg|_{v_r=0} = \frac{K_{io}s}{D(s)} + \frac{s(L_f s + K_i + R_f)}{nD(s)} \tag{5-31}$$

It is obviously that the equivalent output impendence is not strictly inversely proportional to the number of paralleled inverters. Here we use an example to show the relationship between the equivalent output impendence and the number of paralleled inverters. This example is the same as the one used in Sub-section 5.4.2. Originally the multi-inverter system is a two-inverter system, where individual inverter has the nominal parameters as listed in Table 5.1, and has the control law of (5-25). We now add new inverters into the system one after another (each assumed to have the same nominal parameters as shown in Table 5.1) and plot the output impedance in a Bode form. Figure 5.4 shows the results for $n = 2, \cdots, 9$.

In Figure 5.4, in the low frequency band (around 314rad/sec or 50Hz), the equivalent output impendence varies only slightly when the number of paralleled inverters changes. What this means is that, even with a significant change in the

number of parallel inverters, the steady-state error of the output voltage would not vary significantly.

In Figure 5.4, in the high frequency band, the equivalent output impendence varies more significantly. The larger is the number of inverters, the lower is the equivalent output impendence. A lower equivalent output impendence in high frequency band implies a faster transient response.

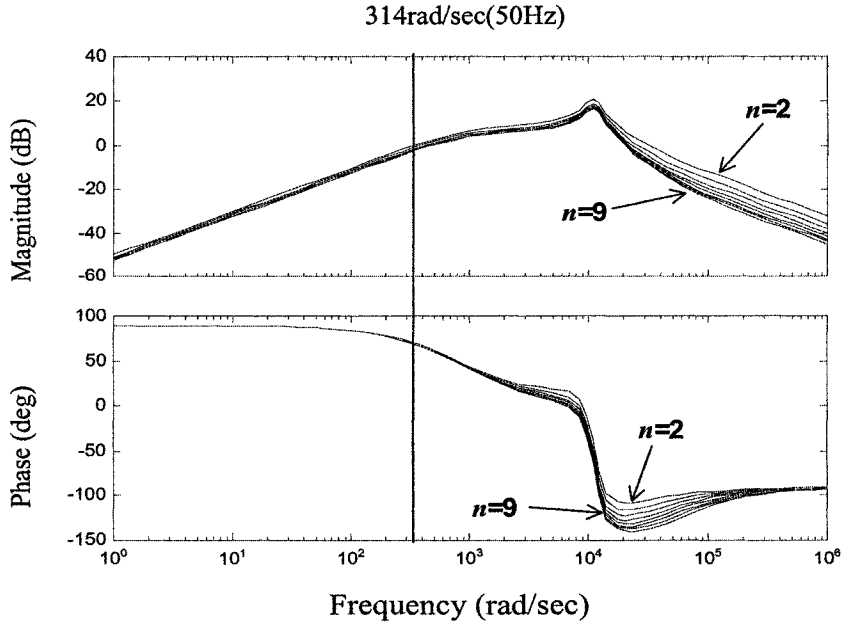


Figure 5.4 Bode plot of the equivalent output impendence of multi-inverter system ($n = 2, \ldots, 9$)

In (5-31), *D(s)* is the characteristic equation of the whole system when there is no load (output open-circuited). The roots of *D(s)* are the closed-loop poles of the whole system. Note that n does not appear in *D(s)*. Increasing or decreasing the number of paralleled inverters would, therefore, not influence the stability of the whole system.

Summarizing the results, it may be concluded that, as the number of parallel inverters is increased, the equivalent output impendence of the whole system decreases

slightly in low frequency band, but significantly in the high frequency band. Therefore, while a larger number of inverters will result in little change in the steady-state error of the output voltage, it will actually improve the transient response. In addition, the change in the number of the paralleled inverters would not influence the stability of the whole system.

5.5.3 Simulations

In this sub-section, PSpice simulations are performed to verify the analysis. The simulated multi-inverter system is composed of three inverters that have the nominal parameters as listed in Table 5.1 (except the L-C filters). The system employs a controller with the control law of (5-25). In order to perturb the system, different L-C filters are used in different inverters. Different line impedances are also added into the inverters. The actual parameters of the filters and the line impendences are:

	Inductance of filter L_f	Capacitance of filter C_f	Line Impedance Z_p
First inverter	1mH	20μF	0.03Ω
Second inverter	1.2mH	17μF	0.01Ω
Third inverter	0.8mH	22μF	0.02Ω

Figure 5.5 and Figure 5.6 are the PSpice simulation results. In the example shown in Figure 5.5, initially only two inverters are paralleled. Then, at t = 60ms, an inverter is added to the system. At t = 120ms, the additional inverter is removed. It is found that the adding or removing of an inverter does not have much effect on current sharing between the first inverter and the second inverter. (It is remains at about 7~8%.) This verifies the conclusion of (5-29). Figure 5.6 shows the waveforms of a three-inverter

system when the load changes from open circuit (no load) to 5Ω (rated load for the 2-inverter system). When there is no load, the RMS of the output voltage is 115.5V. With a 5Ω load, the RMS of the output voltage is 110.7V. Compared with the simulation result for a two-inverter system (shown in Figure 5.3), the three-inverter system has a smaller steady-state error in the output voltage and a faster transient response. This is due to the fact that the three-inverter system has smaller equivalent output impendence than the two-inverter system at high frequency.

The analysis and simulations results given in the last three sub-sections prove that the proposed controller, designed for a fixed number of paralleled inverters, can be used satisfactorily in systems with different number of paralleled inverters.

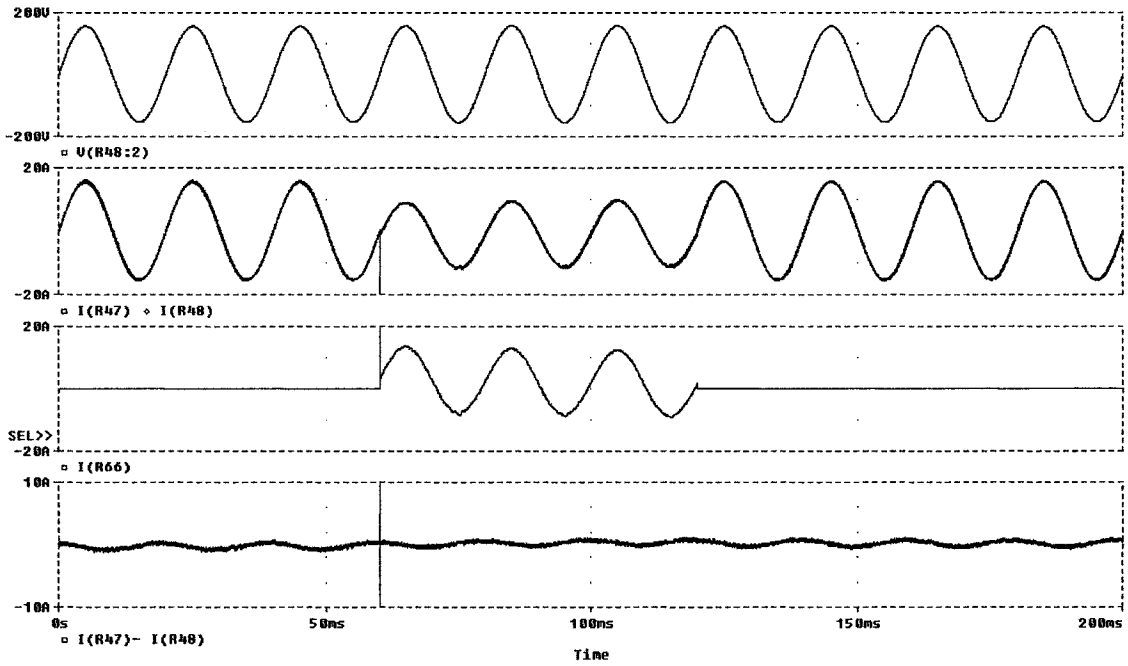


Figure 5.5 Simulation results of a three-inverter system (the third inverter is added, then removed). Top: the output voltage. Second: the output currents of the first and second inverter. Third: the output current of the third inverter. Bottom: the output current difference between the first and second inverters.

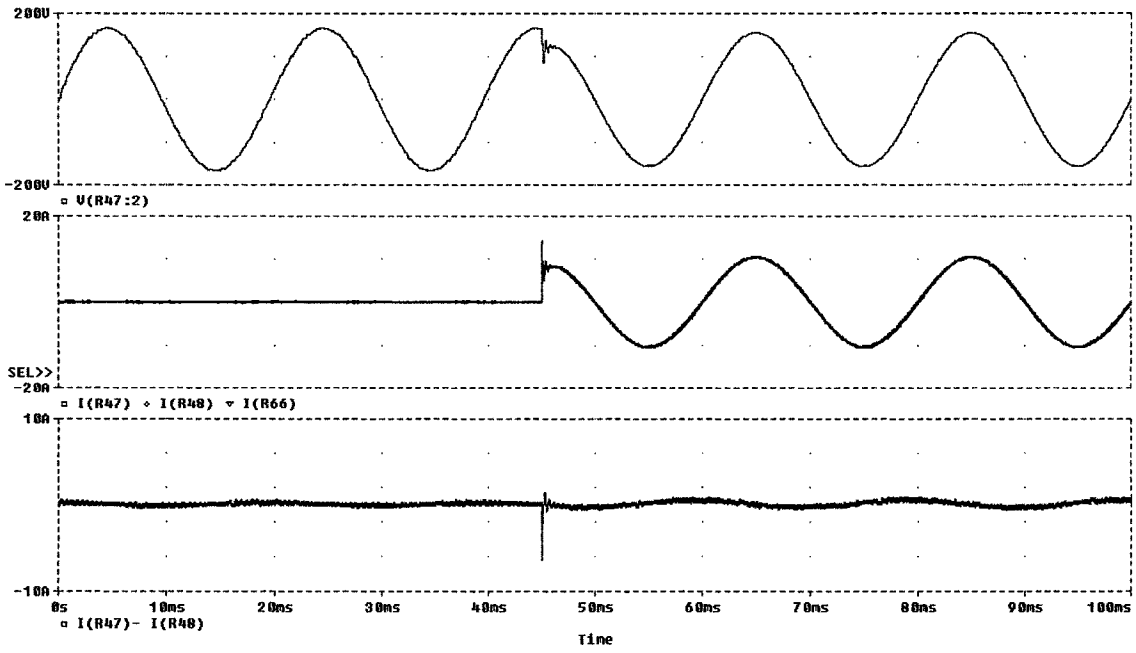


Figure 5.6 Simulation results of a three-inverter system when load changes from open circuit (no load) to 5Ω. Top: the output voltage. Middle: the output currents of the first, second and third inverter. Bottom: the output current difference between the first and second inverters.

5.6 Experimental Results

Three 110Vac/1.1KVA dc-ac inverters are built for parallel operation to verify the performance of the proposed control scheme. Each inverter has the parameters as listed in Table 4.1, and the controller has the structure as shown in Figure 5.2, and with the parameters of (5-25).

Figure 5.7 and Figure 5.8 are the experimental results of the two-inverter system. Figure 5.7 shows the waveforms under the rated load of 5Ω. It shows that the load current can be shared properly. Figure 5.8 is the waveforms when load changes from

open circuit (no load) to 5Ω. It shows that the transient response is fast. Even under dynamic load, the load current is shared properly.

Figures 5.9~12 are the experimental results of a three-inverter system. Figure 5.9 shows the waveforms for a load of 5Ω. It shows that, even using the same controller as the two-inverter system, the load current is equally shared among the three inverters. Figure 5.10 shows the waveforms when the load changes from open circuit (no load) to 5Ω. The response is similar to the one of the two-inverter system shown in Figure 5.8. It proves that the controller performs equally well in systems with different number of paralleled inverters. Figure 5.11 shows the waveforms when a third inverter is added into the system. Figure 5.12 shows the waveforms when the third inverter is removed from the system. Under all conditions, the load current can be shared properly.

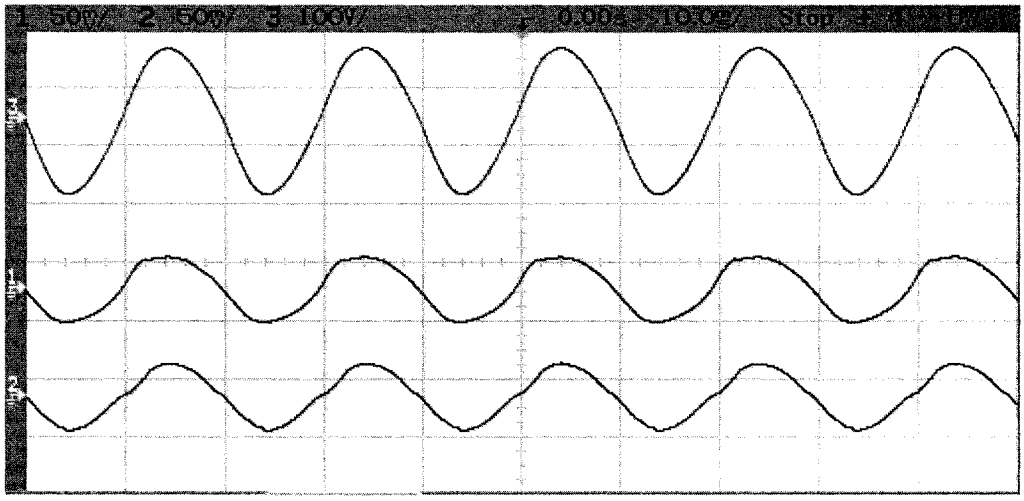


Figure 5.7 Experimental results of a two-inverter system under rated load of 5Ω. Top: the output voltage (100V/div). Middle: the output currents of the first inverter (25A/div). Bottom: the output current of the second inverter (25A/div).

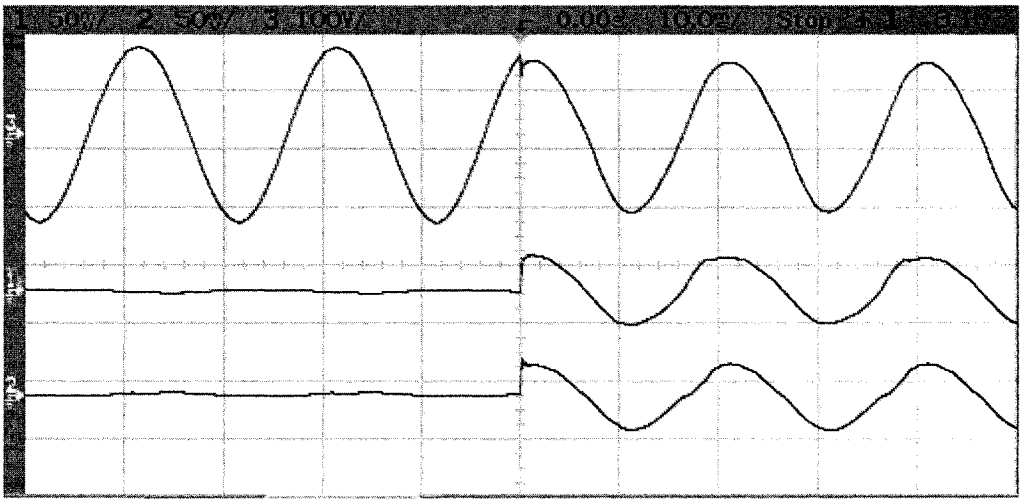


Figure 5.8 Experimental results of a two-inverter system when load changes from open circuit (no load) to 5Ω. Top: the output voltage (100V/div). Middle: the output currents of the first inverter (25A/div). Bottom: the output current of the second inverter (25A/div).

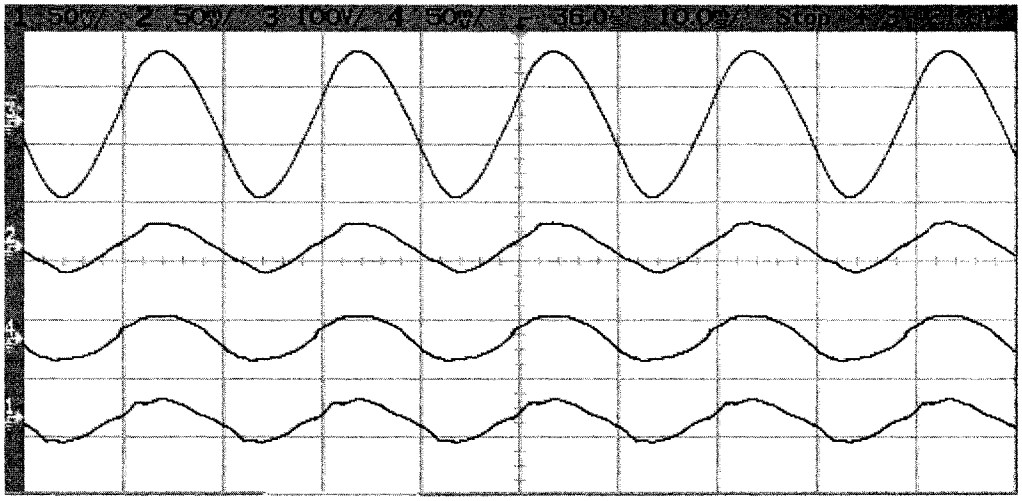


Figure 5.9 Experimental results of a three-inverter system under load of 5Ω. Top: the output voltage (100V/div). Second: the output currents of the first inverter (25A/div). Third: the output currents of the second inverter (25A/div). Bottom: the output current of the third inverter (25A/div).

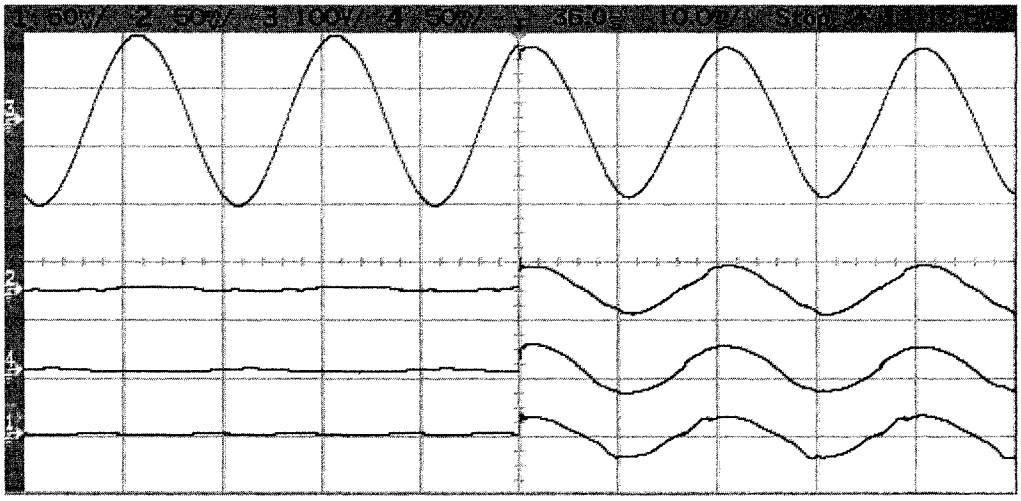


Figure 5.10 Experimental results of a three-inverter system when load changes from open circuit (no load) to 5Ω. Top: the output voltage (100v/div). Second: the output currents of the first inverter (25A/div). Third: the output currents of the second inverter (25A/div). Bottom: the output current of the third inverter (25A/div).

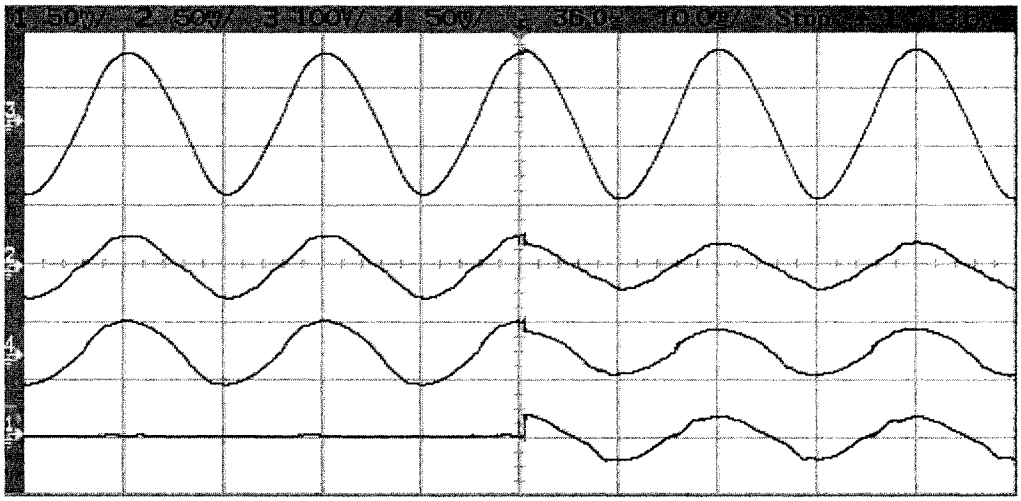


Figure 5.11 Experimental results of a three-inverter system when an inverter is added (load of 5Ω). Top: the output voltage (100v/div). Second: the output currents of the first inverter (25A/div). Third: the output currents of the second inverter Bottom (25A/div): the output current of the third inverter (25A/div).

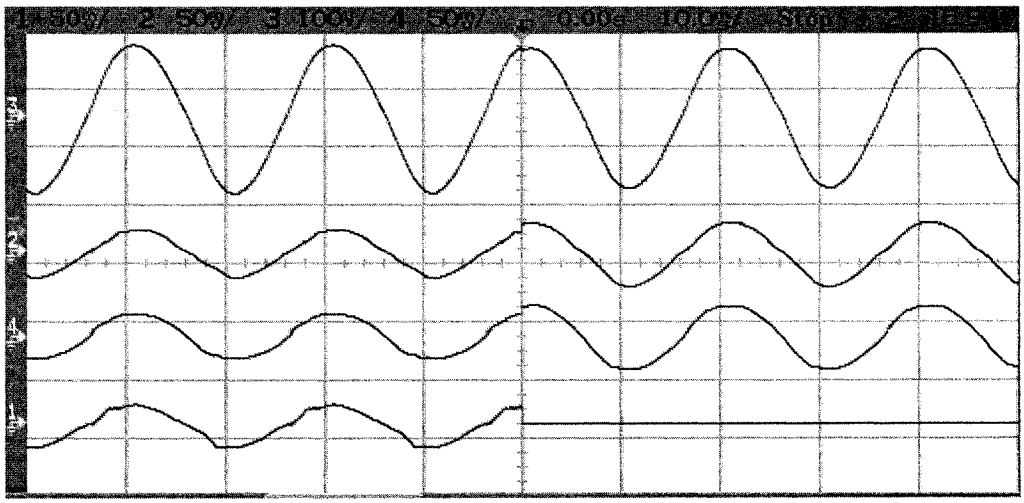


Figure 5.12 Experimental results of a three-inverter system when an inverter is removed (load of 5Ω). Top: the output voltage (100v/div). Second: the output currents of the first inverter (25A/div). Third: the output currents of the second inverter (25A/div). Bottom: the output current of the third inverter (25A/div).

5.7 Conclusion

In this chapter, a state-feedback controller is proposed for parallel multi-inverter systems. The optimal control methodology is used to determine the feedback gain matrix. The resultant state-feedback controller gives good performance on output voltage regulation and output current sharing. The hardware implementation of the controller is also simple. The common circuit of the system consists of only a current sensor (for each inverter) and a single signal wire. Therefore, the reliability of the whole system is greatly improved. The robustness of the controller has also been investigated. Through frequency domain analysis, it has been proved that the variation of the number of paralleled inverters has only small influence on the performance of the system. Therefore, a state-feedback controller designed for a fixed number of inverters can function well for systems with a variable number of paralleled inverters. PSpice

simulation results and experimental results are given to verify the theoretical analysis and prediction.

Chapter 6

Conclusions and Suggestions for Future Research

This thesis presents a research on the control of both single inverters and multi-inverter systems. Such inverter systems are commonly used in uninterruptible power supply (UPS) applications. For the single inverter system, focus is put on the improvement of quality of output voltage by introducing the intelligent control. For the multi-inverter system, focus is put on the investigation of the characteristic of the parallel operation, and the synthesis of the controller design. In this concluding chapter, important results that have been obtained in the study are summarized, along with some suggestions for future work on inverter systems.

6.1 Contributions of the Thesis

In this section, we summarize the main contributions of the thesis in following three main topics:

1). Intelligent control of single dc/ac inverter.

The flexibility of neural-network control on dc/ac inverters has been investigated. It is found that, due to its nonlinear function-mapping ability, the neural-network control is suitable for the control of the inverters especially in cases where nonlinear loads are involved. A neural-network controller for dc/ac inverters has been proposed to improve the quality of the output voltage. The neural-network controller is trained off-line using the example patterns obtained from computer simulations. Simulation and experimental results show the superiority of the neural-network controller to traditional PI controller.

The integrated-circuit implementation of the proposed neural-network controller is discussed. It is shown that the proposed neural-network controller can be integrated into a single chip, thus making it a low-cost high-performance solution to the inverter system.

2). Modeling and analysis of the multi-inverter system with instantaneous average-current-sharing scheme.

By introducing a disturbance source to represent all the sources that may cause the current unbalance, a model of the system with instantaneous average-current-sharing scheme can be easily built. An extensive analysis has revealed the following: 1) A loop gain expression can be developed to evaluate the stability and performance of the current-sharing loop. 2) The impedance characteristic of the multi-inverter system can be used to investigate the stability of the system. 4) Under stable parallel operation, the voltage regulation of the whole system depends on voltage-regulating capability of the individual inverter. Simulation and experimental results confirm the theoretical predictions.

3). State-feedback control design for the multi-inverter system.

Optimal control is introduced to control the current in multi-inverter systems. By minimizing a performance index, the feedback gains of the voltage loop and current-sharing loop are easily designed. In order to verify the robustness of the proposed optimal controller, frequency domain analysis is applied to the multi-inverter system with the proposed optimal controller. The advantages of the proposed optimal controller include easy design and simple hardware implementation. The common circuits of the system are shrunken to be a current sense and a conducting wire. Simulations and experiments are carried out to investigate the performance of the system and to verify the analytical results.

6.2 Suggestions for Future Research

In the area of control of single inverter, the following opportunities for further research are noted:

1). Development of the proposed neural-network controller to three-phase system.

The UPS is a backup power supply system. As the power level increases to about 10KVA or higher, it becomes advantageous to use a three-phase inverter. The majority of industrial/commercial sine-wave inverters are of this type. The control of the three-phase inverters is more complicated than that of the single-phase inverter. Not only the individual output, but also the balance among the three phases should be controlled carefully. In order to introduce the proposed neural-network controller into the three-phase system, it is necessary to investigate the characteristics of the complete system.

2). Application of computational intelligence in control of dc/ac inverter systems.

Recently the computational intelligence (CI) attracts many research interests. CI is an emerging area of fundamental and applied research exploiting a number of advanced information processing technologies. The main components of CI encompass neural network, fuzzy set and evolutionary computation [87]. Actually, this thesis has explored some areas of application of CI in the control of inverter systems.

Neural network offers a powerful and distributed computing architecture, which is equipped with significant learning abilities. Fuzzy set is a logical system that is much closer in spirit to human thinking and natural language than traditional logical systems. Evolutionary computation embraces genetic algorithms, evolutionary computation and evolutionary strategies which are biologically-inspired methodologies aiming at global optimization. Combination of them thus molds a powerful weapon to solve the nonlinear and parameter uncertainty problems [88]. The inverter system, itself, is a nonlinear system. Unknown loading condition makes the control problem more complex. In addition, parameter sensitivities, robustness and disturbance rejection all should be taken into consider. It is therefore meaningful to explore more in the area of the application of CI in the control of inverter systems.

In the area of parallel multi-inverter systems, the following opportunities for further research are noted:

1). Modeling and analysis of other current-sharing schemes for multi-inverter systems.

In Chapter 4, the instantaneous average-current-sharing scheme is discussed. A useful and simple model is provided to analyze and evaluate parallel multi-inverter

systems. If the sharing scheme is changed to master-slave mode or circular chain mode, the model will be different. It is worthwhile to extend the model and analysis to all types of sharing schemes, and to assess their performance.

2). Decentralized control and analysis for multi-inverter systems.

A multi-inverter system can be considered as a large-scale system. A system is considered to be large-scale if it can be decoupled or partitioned into a number of interconnected subsystems or "small-scale" systems for either computational or practical reasons [89]. Decentralized control assigns system inputs to a given set of local controllers, which observe only local system outputs. Therefore, the concept of large-scale system and decentralized control are useful to help solve the current sharing problem of multi-inverter systems.

Appendix A

SIMULINK Model to Obtain Example Patterns

This appendix presents the models built in SIMULINK to obtain example patterns for training of the neural network controller. The block diagrams of the models are depicted in Figure 3.3 and Figure 3.4.

Figure A.1 illustrates the SIMULINK model of Figure 3.3. Figure A.2 is the detail of the subsystem named "model of inverter" in the middle of Figure A.1.

Figure A.3 illustrates the SIMULINK model of Figure 3.4. Figure A.4 is the detail of the subsystem named "model of inverter" in the middle of Figure A.3.

In Figure A.1, a S-Function named "pwm_inverter" is used to describe the behavior of the full-bridge inverter. In Figure A.3 and Figure A.4, another S-Function named "rectifier" is used to describe the behavior of the rectifier type load. The sources files of both are listed below.

```
function[sys,x0,str,ts]=pwm_inverter(t,x,u,flag,E)

% model of PWM Inverter.
%
% Input definiation:
% u(1,:) is the modulation signal;
% u(2,:) is the carrier wave, usually a triangular wave;
%
% When u(1,:)>u(2,:), output voltage equel to E;
% When u(1,:)<=u(2,:), output voltage equel to –E.

switch flag,

case 0
sizes=simsizes;
sizes.NumContStates=0;
sizes.NumDiscStates=0;
sizes.NumOutputs=1;
sizes.NumInputs=2;
sizes.DirFeedthrough=0;
sizes.NumSampleTimes=1;

sys=simsizes(sizes);
x0=[];
str=[];
ts=[-1,0];

case 3
if u(1,:)>u(2,:)
  sys=E;
else
  sys=-E;
end

case {1,2,4,9}
 sys=[];

otherwise
  error(['Unhandled falg=',num2str(falg)]);

end

% end of function PWM_inverter
```

```
function [sys,x0,str,ts]=rectifier(t,x,u,flag,Rd,Cd,Rl)

% Model of full-wave rectifier load
% State-space description.
%
% Input is the input voltage of rectifier.
% Output is the load voltage and current of rectifier.
%
% Rd is equivalent resistor of rectifier;
% Cd is the capacitor paralleled as filter after rectifier.
% Rl is the resistor paralleled with Cd as a load.


A=-(1/Rl+1/Rd)/Cd;

B=1/Rd/Cd;
AA=-1/Rl/Cd;

C=[1;-1/Rd];
D=[0;1/Rd];
CC=[1;1/Rd];
CCC=[1;0];

switch flag,

case 0
sizes=simsizes;
sizes.NumContStates=1;
sizes.NumDiscStates=0;
sizes.NumOutputs=2;
sizes.NumInputs=1;
sizes.DirFeedthrough=0;
sizes.NumSampleTimes=0;

sys=simsizes(sizes);
x0=zeros(1,1);
str=[];
ts=[];

case 1
  if(abs(u)>abs(x(1,:)+0.75))
    if(u>0)
      sys=A*x+B*(u-0.75);
    else
      sys=A*x-B*(u+0.75);
    end

  else
    sys=AA*x;
  end
```

```
 case 3
   if(abs(u)>abs(x(1,:)+0.75))
     if(u>0)
       sys=C*x+D*(u-0.75);
     else
       sys=CC*x+D*(u+0.75);
     end

   else
     sys=CCC*x;
   end


case {2,4,9}
  sys=[];

otherwise
  error(['Unhandled flag=',num2str(flag)]);

end

% end of function rectifier.
```

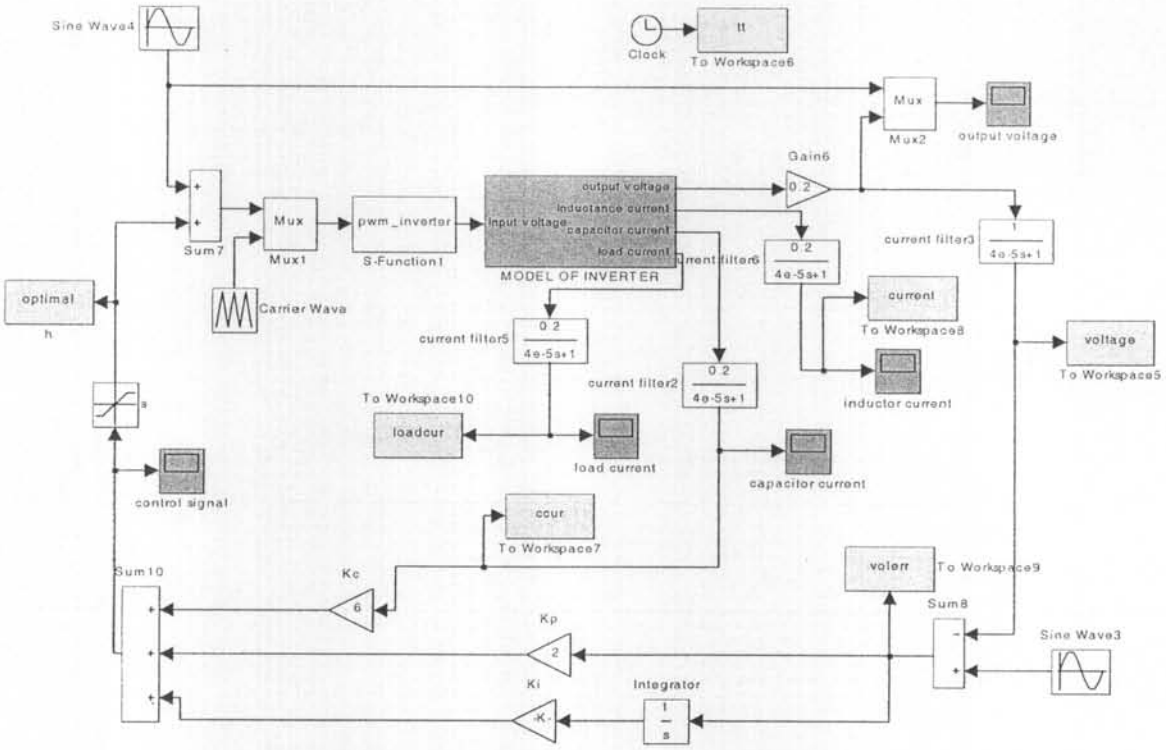


Figure A.1. SIMULINK model of Figure 3.3.

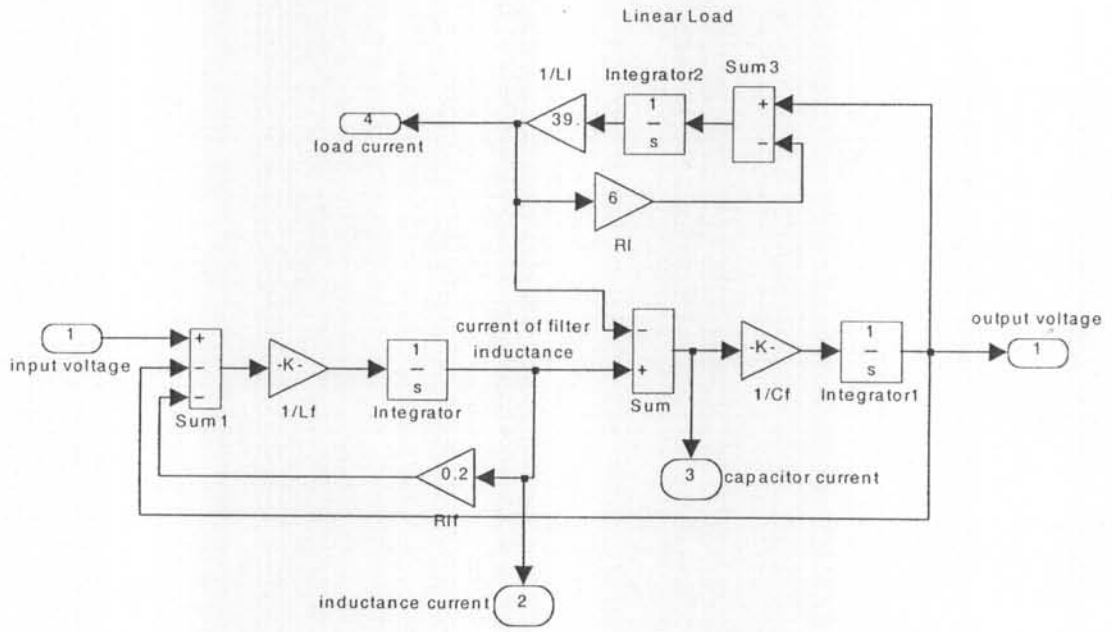


Figure A.2. Details of the subsystem of "model of inverter" in Figure A.1.

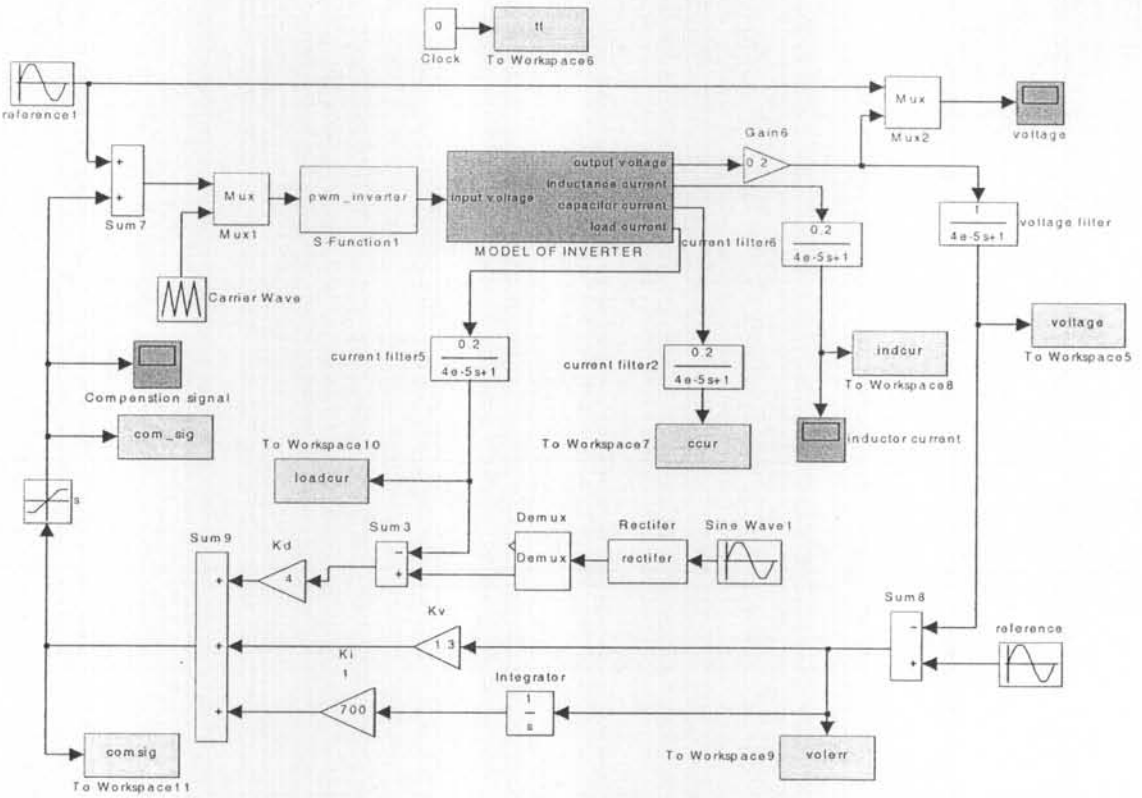


Figure A.3. SIMULINK model of Figure 3.4.

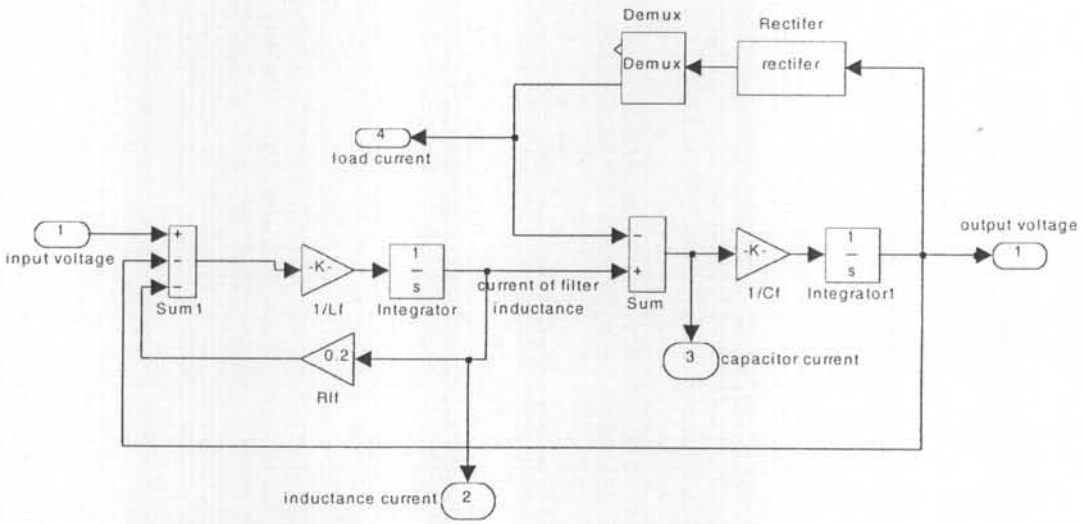


Figure A.4. Details of the subsystem of "model of inverter" in Figure A.2.

Appendix B

Weights and Biases of Well-Trained Neural Network

$W_{jk}^{(i)}$ is the weight that connects the j-th node on the (i-1)-th layer with the k-th node on the i-th layer (if i=1, then the (i-1)-th layer refers to the inputs).

$b_k^{(i)}$ is the bias of the k-th node on the i-th layer.

$W_{11}^{(1)} = 0.065$ $W_{12}^{(1)} = 1.023$ $W_{13}^{(1)} = -45.179$

$W_{21}^{(1)} = -0.076$ $W_{22}^{(1)} = -7.926$ $W_{23}^{(1)} = 40.474$

$W_{31}^{(1)} = 0.001$ $W_{32}^{(1)} = 97.383$ $W_{33}^{(1)} = -12.053$

$W_{41}^{(1)} = -0.001$ $W_{42}^{(1)} = 58.484$ $W_{43}^{(1)} = -44.747$

$W_{51}^{(1)} = 0.065$ $W_{52}^{(1)} = 45.695$ $W_{53}^{(1)} = 33.124$

$b_1^{(1)} = 0.092$ $b_2^{(1)} = 12.468$ $b_3^{(1)} = 203.781$

$W_{11}^{(2)} = -54.116$

$W_{21}^{(2)} = -0.0273$

$W_{31}^{(2)} = 0.0744$

$b_1^{(2)} = 5.229$

Appendix C

MATLAB Function to Calculate the Feedback Gain

```
function K=calgain(A,B,C,Qe,Q2,Qi,W,f)

% CALGAIN caculates gains for optimal control of multi-inverter system.
%
%  Syntax
%
%      K = CALGAIN(A,B,C,Qe,Qi,Q2,W,f)
%
%  Description
%      CALGAIN(A,B,C,Qe,Qi,Q2,W,f)takes
%          A, B, C - State space description of the multi-inverter system.
%          Qe - Weight of integration of output voltage error in performance
%          index, default = 20.
%          Qi – Weight matrix of inductor currents for each inverter in
%          performance index. default = I.
%          Q2 – Weight of output voltage error in performance index.
%          default = 20.
%          W  - Weight of input duty ratio in performance index. Default = 2.
%          f  - The fundament frequency of output voltage, default = 50Hz.
%      and returns a gain matrix K.
%
%      With the gain matrix K, the input of the multi-inverter sytem can
%      be describe as,
%                              u = K*zc,
%      where u = [d1, d2, ..., dn]', di is duty ratio of ith inverter.
%              zc = [ev, il1, il2, ..., iln, vo, vr].
```

```
% Input argument.
if nargin < 3
  error('Not enough input arguments.')
end

if size(A,1) ~= size(A,2)
  error('First argument must be square matrix.')
end

N = size(A,1)-2;
if size(B,1) ~= N+2
  error('Second argument must have same number of rows as first argument
has.')
end
if size(C,1) ~= N+2
  error('Third argument must have same number of rows as first argument has.')
end

% Default
if nargin < 4, Qe = 20; end
if nargin < 5, Q2 = 20; end
if nargin < 6, Qi = eye(N); end
if nargin < 7, W = 2*eye(N); end
if nargin < 8, f = 50; end

Q11 = eye(N+2); Q11(1,1) = Qe; Q11(2:N+1,2:N+1)=Qi; wf = 2*pi*f;

% Calculate gain
Az = [0          1;
      -wf*wf   -1e-3];

Cz = [1 0]';

      Ac = [A                  [Cz';  zeros(N+1, 2)];
            zeros(2, N+2)   Az;];

Bc = [B; zeros(2, N)];

Q = (eye(N+2)-C*inv(C'*C)*C')'*Q11*(eye(N+2)-C*inv(C'*C)*C')+C*Q2*C';

Qc = [Q                                -Q*C*inv(C'*C)*Cz';
      -Cz*inv(C'*C)*C'*Q       Cz*inv(C'*C)*C'*Q*C*inv(C'*C)*Cz'];

P = are(Ac,   Bc*inv(W)*Bc',   Qc);
K = inv(W)*Bc'*P;

% end of calgain.
```

Publications

Journal papers

[1] X. Sun, M.H.L. Chow, F.H.F. Leung, D.H. Xu, Y.S. Lee, and Y.S. Wang, "Analogue Implementation of a Neural Network Controller for UPS Inverter Applications", *IEEE Trans. Power Electron.*, vol. 17, no. 3, pp. 305-313, May, 2002.

[2] X. Sun, Y.S. Lee, and D. Xu, "Modeling, analysis, and implementation of parallel multi-inverter systems with instantaneous average-current-sharing scheme," *IEEE Trans. Power Electron.*, vol. 18, no 3, pp. 844-856, May, 2003.

[3] X. Sun, L.K. Wong, Y.S. Lee, and D. Xu, "Design and analysis of an optimal controller for parallel multi-inverter systems," submitted to *IEEE Trans. Circuit and Systems - I: Fundamental Theory and Applications.*

Conference papers

[1] X. Sun, D. H. Xu, F. H. F. Leung, Y. S. Lee, and Y. S. Wang, "Neural-network-controlled single-phase UPS inverters with improved transient response and adaptability to various loads," *Proceedings, of IEEE PEDS'99*, vol. 2, pp. 865-870, July 1999, Hong Kong.

[2] X. Sun, D. H. Xu, F. H. F. Leung, Y. S. Lee, and Y. S. Wang, "Design and implementation of a neural-network-controlled UPS inverter", *Proceedings, 25th annual conference of the IEEE Industrial Electronics Society (IECON' 99)*, pp. 779-784, December 1999, San Jose, USA.

[3] X. Sun, Martin H. L. Chow, F. H. F. Leung, D. H. Xu, Y. S. Lee, and Y. S. Wang, "An analogue-neural-network-controller for UPS inverter applications," *Proceedings, China Fifteenth Conference on Circuits and Systems*, pp. 1-10, November, 1999, Guangzhou, CHINA. (Keynote presentation).

References

[1] R. Billinton, G. Wacker, "Cost of electrical service interruptions to industrial and commercial consumers," *IEEE/IAS Annu. Meet. Conf. Rec.,* 1985, pp. 289-294.

[2] G.P. Hicks, *A review of ac UPS technology*, ERA project 49-01-2304, final report, ERA technology Ltd., 1992.

[3] W.A. Tabisz, M. M. Jovanovic, and F.C. Lee, "Present and future of distributed power system," in *IEEE-APEC Conf. Rec.* 1992, pp. 11-18.

[4] M.M. Jovanovic, "A novel, low-cost implementation of 'democratic load-current sharing of parallel converter modules," *IEEE Trans. Power Electron.*, vol. 11, no. 4, pp. 604-611, July, 1996.

[5] L. balogh, "The UC3902 load sharing controller and its performance in distributed power systems," *Unitrode application note U-163*, 1999.

[6] B.D. Berford and R.G. Hoft, *Principle of inverter circuits*, Wiley, New York, 1964.

[7] G. Séguier and F. Labrique, *Power electronic converters: DC-AC conversion*, Springer-Verlag, Berlin Heidelberg, 1993.

[8] D.M. Divan, "Inverter topologies and control techniques for sinusoidal output power supplies,: in *IEEE-APEC Conf. Rec.* 1991, pp. 81-87.

[9] T. Kawabata and S. Higashono, "Parallel operation of voltage source inverters," *IEEE Trans, on Ind. Applicat.*, vol. 24, no. 2, pp. 281-287, 1988.

[10] D.W. Hart, *Introduction to Power Electronics*, Prentice-Hall, USA, 1997.

[11] N. Mohan, T.M. Undeland, and W.L. Robbins, *Power Electronics: Converters, Applications, and Design*, 2nd Edition, Wiley, New York, 1995.

[12] R.S. Lai and K.D.T. Ngo, "A PWM method for reduction of switching loss in a full-bridge inverter", *IEEE Trans. Power Electron.*, vol.10, no.3, pp.326-332, 1995.

[13] R. Wu, S.B. dewan, and G.R. Slemon, "Analysis of an ac-to-dc voltage-source converter using PWM with phase and amplitude control", *IEEE Trans. Ind. Applicat.* , vol.27, no.2, pp.355-364, 1991.

[14] N.M. Abdel-Rahim, J.E. Quaicoe, "Analysis and design of a multiple feedback loop control strategy for single-phase voltage-source UPS inverters", *IEEE Trans. Power Electron.*, vol.11, no.4, pp.532-541, 1996.

[15] M.J. Ryan, W. E. Brumsickle, and R.D. Lorenz, "Control topology options for single-phase UPS inverter", *IEEE Trans. Ind. Applicat.* , vol.33, no.2, pp.493-501, 1997.

[16] A. Kawamura, R. Chuarayapratip, and T. Haneyoshi, "Deadbeat control of PWM inverter with modified pulse patterns for uninterruptible power supply", *IEEE Trans. Ind. Electron.* , vol.35, no.2, pp.295-300, 1988.

[17] T. Kuwabata, T. Miyashita, and Y. Yamamoto, "Deadbeat control of three PWM inverter", *IEEE Trans. Power Electron.*, vol.5, no.1, pp.21-28, 1990.

[18] Y.Y. Tzou, S.L. Jung, and H.C. Yeh, "Adaptive repetitive control of PWM inverter for very low THD AC-voltage regulation with unknown load," *IEEE Trans. Power Electron.*, Vol. 14, no. 5, pp. 973-981, 1999.

[19] S.L. Jung and Y.Y. Tzou, "Sliding mode control of a closed-loop regulated PWM inverter under large load variations", in Proc. *IEEE-PESC'93, 1993*, pp.616-622.

[20] B.J. Kim, J.H. Choi, J.S. Kim, and C.H. Choi, " Digital control scheme of UPS inverter to improve the dynamic response", *IEEE Electrical and Computer Engineering, 1996 Canadian conference on* 1996, pp.318-321.

[21] A.V. Jouanne, P.N. Enjeti, and D. Lucas, " DSP control of high–power UPS systems feeding nonlinear loads", *IEEE Trans Ind. Applicat.* , vol.43, no.1, pp.121-125, 1996.

[22] A.K. Jain, J. Mao, and K.M. Mohiuddin, "Artificial neural networks: a tutorial", *Computer*, vol. 29, issue 3, pp. 33-44, 1996.

[23] Y.S. Lee, *Computer-aided analysis and design of switch-mode power supplies,* Dekker, New York, 1993.

[24] K.J. Hunt, D. Sbarbaro, R. Zbikowski and P. J. Gawthrop, "Neural networks for control system — a survey" *Automatica*, vol.28, no.6, pp.1083-1112, 1992.

[25] B.K. Bose, " Expert system, fuzzy logic, and neural network applications in power electronics and motion control", *Proceeding of the IEEE*, vol.82, no.8, pp.1303-1323, 1994.

[26] B.R. Lin, " Analysis of neural and fuzzy-power electronic control", *IEE Proc.- Sci. Meas. Technol.,* Vol.144, No.1, pp.25-33, 1997.

[27] Y. Dote and R. G. Hoft, *Intelligent control power electronic systems*, Oxford University Press, New York, 1998.

[28] M-H. Kim, M.G. Simões, and B.K. Bose, "Neural network-based estimation of power electronic waveform", *IEEE Trans. Power Electron.*, vol.11, no.2, pp.383-389, 1996.

[29] A. Cichocki and T. Lobos, "Adaptive analogue network for real-time estimation of basic waveforms of voltage and currents", *IEE Proceeding-C*, vol. 134, no. 9, pp. 343-350, 1992.

[30] P.K. Dash, S.K. Panda, B. Mishra, and D.P. Swain, "Fast estimation of voltage and current phasors in power networks using an adaptive neural network", *IEEE Trans. Power Systems*, vol. 12, no. 4, pp. 1494-1499, 1997.

[31] P. Kostyla, T. Lobos, and Z. Waclawek, "Neural networks for real-time estimation of signal parameters", *Proceedings of the IEEE International Symposium on Industrial Electronics, ISIE'96*, 1996, vol. 1, pp. 380-385.

[32] M. Rukonuzzaman and M. Nakaoka, "Magnitude and phase determination of harmonic currents by adaptive learning back-propagation neural network", *Proceedings of IEEE 1999 international conference on Power Electronics and Drive Systems, PEDS'99*, 1999, pp. 1168-1173.

[33] L.L. Lai, W.L. Chan, C.T. Tse, and A.T.P. So, "Real-time frequency and harmonic evaluation using artificial neural networks", *IEEE Trans. Power Delivery*, vol. 14, pp. 52-59, 1999.

[34] H. Mori, K. Itou, H. Uematsu, and S. Tsuzuki, "An artificial neural-net based method of predicting power system voltage harmonic", *IEEE Trans. Power Delivery*, vol. 7, no.1, pp. 402-409, 1992.

[35] Y. Ito, T. Furuhashi, S. Okuma, Y. Uchikawa, "A digital current controller for a PWM inverter using a neural network and its stability", *IEEE-APEC Conf. Rec.*, 1990, pp.219-224.

[36] K. Tazume, T. Aoki, Y. Nozaki, Y. Kuwata, and T. Koyashiki, "Harmonic current suppression in an interconnection inverter by using neural network," in *Proc. of Proc. of the Power Conversion Conference, IPEC'95*, Yokohama, 1995, pp. 1260-1265.

[37] M.R. Buhl, R.D. Lorenz, "Design and implementation of neural networks for digital current regulation of inverter drives", in *IEEE/IAS Annu. Meet. Conf. Rec.*, 1991, pp415-423.

[38] B.R. Lin, R.G. Hoft, " Power electronics inverter control with neural networks", in *IEEE-APEC Conf. Rec.*, 1993, pp.128-134.

[39] M.P. Kazmierkowski, D. Sobczuk, "Improved neural network current regulator for VS-PWM inverters", in *Proc. IEEE–IECON'94,* 1994, pp.1237-1241.

[40] A.M. Trzynadlowski, S. Legowski, "Application of neural networks to the optimal control of three-phase voltage-controlled inverters", *IEEE Trans. Power Electronics*, vol.9, no.4, pp.397-404, 1994.

[41] M. Mohaddes, A.M. Gole, and P.G. McLaren, "Harmonic Elimination in PWM inverters using neural networks", *Proceedings of Electrical and Computer Engineering Conference*, 1994 Canadian Conference, vol. 1, pp.64-67.

[42] D. Daniolos, M.K. Darwish and P. Mehta, "Optimised PWM inverter control using artificial neural networks", *Electronics Letters*, vol.31, no.20, pp.1739-1740, 1995.

[43] T. Morie and Y. Amemiya, "An all-analog expandable neural network LSI with on-chip backpropagation learning", *IEEE Journal of Solid-State Circuits,* Vol. 29, No. 9, pp. 1086-1093, 1994.

[44] M. Jabri and B. Flower, "Weight perturbation: an optimal architecture and learning technique for analog VISI feedforward and recurrent multilayer network", *IEEE Trans. on Neural Networks,* Vol. 3, No. 1, pp.154-157, 1992.

[45] P.W. Hollis and J.J. Paulos, "A neural network learning algorithm tailored for VLSI implementation", *IEEE Trans. on Neural Networks*, Vol. 5, No. 5, pp. 784-791, 1994.

[46] F. Kamran, R.G. Harley, B. Burton, and T.G. Habetler, "An on-line trained neural network with an adaptive learning rate for a wide range of power electronic applications", *IEEE-PESC'96 Conf. Rec.*, 1996, pp. 1499-1505.

[47] A.J. Montalvo, R.S. Gyurcsik, and J. Paulos, "Toward a general-purpose analog VLSI neural network with on-chip learning", *IEEE Trans. on Neural Networks*, Vol. 8, No. 2, pp. 413-423, 1997.

[48] H.C. Chan, K.T. Chau, and C.C. Chan, "A neural network controller for switching power converters", *IEEE-PESC'93 Conf. Rec.*, 1993, pp. 887-892.

[49] P.H.W. Leong and M.A. Jabri, "A low-power VLSI arrhythmia classifier", *IEEE Trans. On Neural Networks,* Vol. 6, No. 6, pp. 1435-1445, 1995.

[50] R.C. Hwang, T.J. Liang, and J. W. Chen, "Neural networks controlled PWM inverter", *Proc. IEEE-INTELEC'97,* 1997, pp.201-206.

[51] D.E. Rumelhart, J.L. McClelland, and PDP Research Group, *Parallel Distributed Processing: Exploration in the Microstructure of Cognition*, MIT Press, Cambridge, Mass., 1986.

[52] *Using MATLAB*, The MathWorks, Inc. Natick, MA.

[53] *Using SIMULINK*, The MathWorks, Inc. Natick, MA.

[54] C. Toumazou, F.J. Lidgey, and D.G. Haigh, *Analogue IC design: the current-mode approach*, Peter Peregrinus Ltd, London, UK, 1990.

[55] H. Yamashita, "Uninterruptible power supply systems in NTT," in *Proc. IEEE-INTELEC'90*, 1990, pp. 412-418.

[56] U. De Pra, D. Baert, and H. Kuyken, "Analysis of the degree of reliability of a redundant modular inverter structure," in *Proc. IEEE-INTELEC'98*, 1998, pp543-548.

[57] C. Fontaine, "On the paralleling of UPS systems," in *Proc. IEEE-INTELEC'86*, 1986, pp. 651-658.

[58] J.F. Chen, C.L. Chu, and C.L. Huang, "The parallel operation of two UPS by the coupled-inductor method," in *Proceedings of the IEEE International Symposium on Industrial Electronics 1992*, vol. 2, pp. 733 –736.

[59] F. Ueda, K. Matsui, M. Asao, and K. Tsuboi, "Parallel-connections of pulsewidth modulated inverters using current sharing reactors," *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 673-679, Nov. 1995.

[60] M.C. Chandorkar, D.M. Divan, and R. Adapa, "Control of parallel connected inverters in standalone ac supply systems," *IEEE Trans. Ind. Applicat.*, vol. 29, pp. 136-143, 1993.

[61] Y.B. Byun, T.G. Koo, K.Y. Joe, and etc. "Parallel operation of three-phase UPS inverters by wireless load sharing control," in *Proc. IEEE INTELEC'00*, 2000, pp. 526-532.

[62] Y. Meng, S. Duan, Y. Kang, and J. Chen, "Research on voltage source inverters with wireless parallel operation," in *Proc. IEEE IPEMC'00*, 2000, pp. 808-812.

[63] K. Wallace and G. Mantov, "Wireless load sharing of single phase telecom Inverters," in *Proc. IEEE-IETELEC'99*, 1999.

[64] S.J. Chiang, C.Y. Yen, and K.T. Chang, "A multimodule parallelable series-connected PWM voltage regulator," *IEEE Trans. Ind. Electron.*, vol. 48, no.3, pp. 506-516, June 2001.

[65] U. Borup, F. Blaabjerg, and P.N. Enjeti, "Sharing of nonlinear load in parallel-connected three-phase converters," *IEEE Trans. Ind. Applicat.*, vol. 37, no. 6, pp.1817-1823, Nov/Dec. 2001.

[66] Tuladhar, H. Jin, T. Unger, and K. Mauch, "Control of parallel inverters in distributed AC power systems with consideration of line impedance effect," *IEEE Trans. Ind. Applicat.*, vol. 36, no. 1, pp. 131-138, 2000.

[67] J. Holtz, W. Lotzkat, and K-H. Werner, " A high-power multitransistor-inverter uninterruptible power supply system," *IEEE Trans. Power Electron.*, vol. 3, no. 3, pp. 278-235, 1988.

[68] S. Oshima, Y. Miyazawa, and A. Hirata, "Parallel redundant UPS with instantaneous PWM control," in *Proc. IEEE INTELEC'91*, 1991, pp. 436-442.

[69] S. Duan, Y. Meng, J. Xiong, Y.Kang, and J. Chen, "Parallel operation control technique of voltage source inverters in UPS," in *Proceedings of IEEE 1999 International Conference on Power Electronics and Drive Systems, PEDS' 99*, 1999, pp. 883-887.

[70] J.F. Chen and C.L. Chu, "Combination voltage-controlled and current-controlled PWM inverters for UPS parallel operation," *IEEE Trans. Power Electron.*, vol. 10, no. 5, pp. 547-558, 1995.

[71] C.S. Lee, S. Kim, C.B. Kim, and etc. "Parallel U.P.S. with an instantaneous current sharing control," in *Proc. IEEE-IECON'98*, 1998, vol. 1, pp.568-573.

[72] H. Broeck and U. Boeke, "A simple method for parallel operation of inverters," in *Proc. IEEE-INTELEC'98*, 1998, pp. 143-150.

[73] Y. Ito and O, Iyama, "Parallel redundant operation of UPS with robust current minor loop," in *Proc. of the Power Conversion Conference, IPEC'97*, Nagaoka 1997. pp. 489-494.

[74] A.P. martins, A.S. Carvalho, and A. S. Araújo, "Design and implementation of a current controller for the parallel operation of standard UPSs," in *Proc. IEEE IECON'95*, 1995, pp. 584-589.

[75] R. Xiong, W. Hao, and J. Chen, "A study of parallel operation control technique of DC/AC SPWM inverter," in *Proceedings of IEEE 1999 International Conference on Power Electronics and Drive Systems, PEDS' 99*, 1999, pp. 1027-1032.

[76] Y.-K. Chen, T.-F. Wu, Y.-E. Wu, and C.-P. Ku, "A current sharing control strategy for paralleled multi-inverter systems using microprocessor-based robust control," in *Proceedings of IEEE Region 10 international conference on Electrical and Electronic Technology, TENCON' 2001*, pp. 647-653.

[77] Y. Xing, L. Huang, S. Sun, and Y. Yan, "Novel control for redundant parallel UPSs with instantaneous current sharing," in *Proc. of the Power Conversion Conference, IPEC'02*, Osaka, 2002, pp. 959-963.

[78] T.-F. Wu, Y.-K. Chen, and Y.-H. Huang, "3C strategy for inverters in parallel operation achieving an equal current distribution," *IEEE Trans. Ind. Electron.*, vol. 47, no. 2, pp. 273-281, 2000.

[79] D.J. Perreault, R.L. Selders, Jr., and J.G. Kassakian, "Frequency-based current-sharing techniques for paralleled power converters," *IEEE Trans. Power Electron.*, vol. 13, no. 4, pp. 626-634, 1998.

[80] W.S. Levine (editor), *The Control Handbook*, Boca Raton, Florida, CRC Press, 1996, ch. 10.

[81] J.J. D'Azzo and C.H. Houpis, *Linear Control System Analysis and Design: Conventional and Modern*, New York, McGraw-Hill, Inc., 1995.

[82] R. D. Middlebrook, "Input filter consideration in design and application of switching regulators," in *Proc. IEEE Ind. Applicat. Soc. Annu. Meeting*, 1976.

[83] C.M. Wildrick, F.C. Lee, B.H. Cho, and B.Choi, "A Method of defining the load impedance specification for a stable distributed power system", *IEEE Trans. Power Electron.*, vol. 10, no. 3, pp. 280-285, 1995.

[84] X. Feng, J. Liu, and F.C. Lee, "Impedance specifications for stable DC distributed power systems", *IEEE Trans. Power Electron.*, vol. 17, no. 2, pp. 157-162, 2002.

[85] B. D. O. Anderson and J. B. Moore, *Linear Optimal Control.* Englewood Cliffs, Prentice-Hall, N.J., 1971.

[86] A. G. Bajpai, L. R. Mustoe, and D. Walker, *Advanced Engineering Mathematics*, John Wiley & Sons, Ltd. 1978.

[87] W. Pedrycz, *Computational Intelligence: An Introduction.* Boca Raton, CRC Press, New York, 1997.

[88] H.K. Kam, S.L. Ling, F.H.F. Leung, and P.K. Tam, "Optimal and stable fuzzy controllers for nonlinear systems subject to parameter uncertainties using genetic algorithm," *Proceedings of the 10th IEEE International Conference on Fuzzy Systems, FUZZ-IEEE'2001*, Australia, Dec 2001, pp. 908-911.

[89] M. Jamshidi, *Large-scale systems: modeling, control and fuzzy logic*, Prentice-Hall, N.J., 1997.