Analysis of Single-Phase Single-Stage Power-Factor-Corrected Switching Converters

by

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Abstract

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The distorted input-current waveforms of nonlinear electronic loads cause interference and lead to poor utilization of the utility power system. This is rapidly becoming a serious problem due to the wide proliferation of electronic loads. *Input-current shaping* or power-factor-correction (PFC) addresses the techniques of reducing the distortion of input-current waveforms drawn from the power line. There are many methods of input-current shaping. This thesis focuses on the analysis and comparison of single-stage cascaded switching power converters which can provide simultaneous power factor correction and tight output-voltage regulation.

The study begins with a detailed review of the concept of power factor and the methods of input-current shaping. At the reviewing stage, the automatic PFC is chosen as the subject of the thesis. Topologically there are many ways of realizing automatic PFC. After a detailed comparison between two-switch and single-switch cascaded topologies, the single-switch cascaded version is identified as a suitable candidate for low-power applications. All possible topologies based on pure cascade of the basic second-order converters are derived by using the grafted tree technique. A new buck based topology which is not based on the pure cascade is also derived. Some existing and new rules are used for determining whether a particular cascaded converter is suitable for use as a PFC regulator. Then, the converters which are found suitable are compared against their RMS, peak and average diode, inductor and switch currents. Small-signal dynamical analysis of some well known cascaded converters are also studied in detail. The results from small-signal analysis provide important insights into the dynamics of cascaded PFC converters, which have not been reported in the power electronics literature.

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Chapter 1

Introduction

1.1 Motivation and Objectives

Raw electric power obtained from utilities, batteries and other sources must be converted to a usable form before today's sophisticated machinery and electronics equipment can operate. There is a bewildering variety of electrical loads with different specifications and requirements of the supplied power including low to high voltage, AC and DC waveforms, etc. For example, a variable speed induction motor may require a power source whose voltage and frequency vary during operation. In very few applications is the available power source suited ideally for the load at hand. This is the job of power processing equipment such as the *switching converter*, which processes electric power from one form into another using some minimal number of switches.

One of the most common switching converters is the *AC-DC converter*, which supplies a DC load with power drawn from an AC source. The popularity of AC-DC converters results from the fact that AC power sources and DC loads are so common. The most widely available source of electrical power is the utility grid, which supplies power in the form of low-frequency sinusoidal voltage. Virtually all electronic systems, including equipment for instrumentation, communication and computers, require DC voltage. AC-DC converters range from extremely simple circuits to complicated microprocessor controlled systems. In low-power applications a simple rectifier bridge is often followed by a DC-DC converter to smooth and regulate the output voltage. At high-power levels, phase-controlled rectification provides a regulated DC output voltage using rugged semiconductor devices.

All these methods of generating a DC voltage from an AC power line suffer from the following drawbacks resulting from the poor input-current waveform.

- Distortion of the line voltage affecting both the offending equipment and other equipment connected to the same power line.

- Conducted and radiated electromagnetic interference resulting from harmonic currents drawn from the power source causing impaired performance of nearby electronic systems.
- Poor utilization of the capacity of power source.
- Higher losses and reactive voltage drops in the power distribution network.
- Crawling or cogging in motors.

Due to the proliferation of electronic equipment using DC power, these drawbacks have raised a lot of concern among the electrical power engineers and the users resulting in stringent requirements on power quality. Now several international standards require that the harmonics of the line-current of an electronic equipment stay below certain specified levels. The designer of a utility fed AC-DC converter must now consider the effects of the converter not only on the DC load, but also on the AC power source and any other equipment supplied by that source. In essence, the design has to consider the quality of the input current as well as of the output voltage.

Input-current shaping is the process of improving the input-current waveform of an AC-DC converter, with an intention of mitigating the above mentioned drawbacks. While both single-phase and three-phase AC-DC converters may need current shaping, this project focuses on switching converters supplying a DC load from a **single-phase** source of sinusoidal (AC) voltage for low-power applications. In such applications, cascaded single-stage Power-Factor-Corrected (PFC) converter topologies have been proposed recently [1]-[6]. However, a rigorous analysis of all these topologies and their design aspects are not yet available in the literature. This is the principal motivation of the thesis, which analyzes and compares all the existing and other possible single-stage PFC topologies in respect of their performance and dynamics.

1.1.1 Objectives of the Thesis

As mentioned above, the primary objective of this thesis is to examine the various types of PFC converters and in particular the cascade configuration that can result in high power factor and tight output-voltage regulation. The specific objectives are

1. to derive the possible cascade circuit configurations and their single-switch versions;
2. to study their steady-state performance;
3. to compare their voltage and current stress; and
4. to study their dynamical behaviour.

1.2 Outline of the Thesis

Chapter 2 briefly reviews the concept of power factor and some techniques used for input-current shaping.

Chapter 3 derives all the possible combinations of single-stage converters based on cascading the second-order pulse-width modulated (PWM) converters sharing a single active switch. Nine cascaded converters along with two special topologies are analyzed to determine their suitability as a PFC regulator against some preliminary requirements and criteria. Then some converters are found unsuitable to function as a PFC regulator.

Chapter 4 compares all the cascaded converters which are found suitable against their switch stresses, average and peak currents in inductors, diodes and capacitors. Voltage conversion ratios and operating mode boundary determination are also derived and tabulated.

Chapter 5 gives a detailed small-signal analysis of the cascaded boost-and-buck converter for different operating modes [4].

Chapter 6 gives a detailed small-signal analysis and comparison of the Boost Integrated Flyback Rectifier Energy storage DC-DC Converter (BIFRED) [1] and single-stage cascaded boost-and-flyback converter [2, 3] for different operating modes.

Conclusion is given in Chapter 7.

1.3 Terminology

Some conventions and terms which will be used throughout this thesis should be noted.

A single-stage cascaded converter or simply cascaded converter refers to a system of two converters connected in cascade sharing the same active switch. Single-stage cascaded converters are also referred to as single-switch cascaded converters. For example, single-switch or single-stage cascaded boost-and-buck converter will be referred as cascaded boost-and-buck converter or simply as boost-and-buck converter.

The term PWM converter is used to distinguish "conventional, hard switched" or pulse-width modulated converters from resonant or quasi-resonant converters. A PWM converter, for the present purposes, is a converter with approximately rectangular waveforms.

For brevity, DCM is used to denote discontinuous conduction mode and CCM is used to denote continuous conduction mode. The terms "discontinuous mode" and "continuous mode" will be avoided.

Chapter 2

Review of Power Factor and Input-Current Shaping Techniques

This chapter reviews the concept of power factor and the existing methods of input-current shaping. The "automatic" and "nonautomatic" approaches for shaping input-current will be briefly reviewed. In particular, the automatic shaping method based on the use of discontinuous-conduction-mode converter will be discussed in depth.

2.1 Power Factor

Power factor (PF) is one of the common measures of input-current quality. It is a dimensionless quantity connecting both the input current and voltage. In this section, PF is analyzed from different avenues, and important observations are made.

2.1.1 Definitions

2.1.1.A Time-domain Interpretation

Consider a load drawing a current i_l from the utility power line with voltage v_l. Both i_l and v_l are periodic waveforms with period T_l. The load draws an average power given by

$$P = \frac{1}{T_l}\int_{T_l} v_l i_l \, dt \tag{2.1}$$

where $\int_{T_l}$ represents the integral over any continuous interval of length T_l (a single period of the line-voltage). The power factor (PF) is defined by

$$\mathrm{PF} \equiv \frac{P}{V_{l,rms} I_{l,rms}}, \tag{2.2}$$

where the *RMS* line-voltage and current are given by

$$V_{l,rms} \equiv \sqrt{\frac{1}{T_l}\int_{T_l} v_l^2 \, dt} \tag{2.3}$$

$$I_{l,rms} \equiv \sqrt{\frac{1}{T_l}\int_{T_l} i_l^2\, dt} \tag{2.4}$$

Hence, from (2.2), (2.3) and (2.4), it can be observed that PF is actually a ratio of the average power P to the total power $V_{l,rms}I_{l,rms}$.

2.1.1.B *Vector-algebra Interpretation*

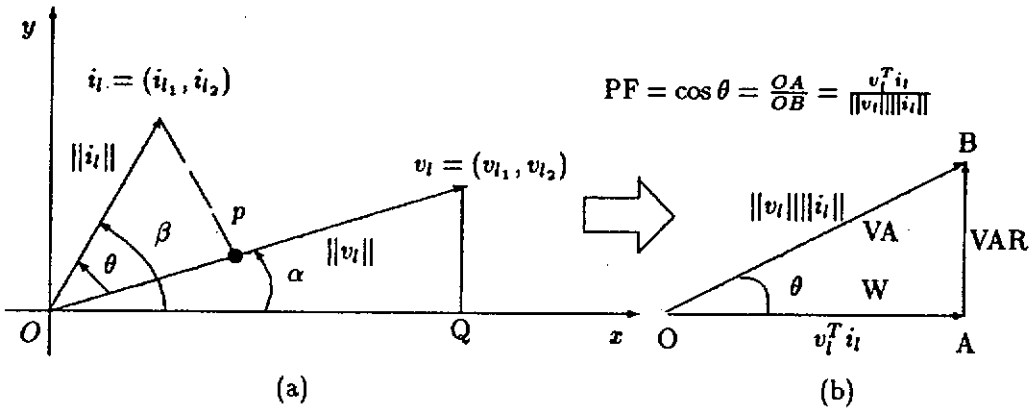

Figure 2.1: (a) The cosine of angle $\theta = \beta - \alpha$; (b) Power triangle

From Fig. 2.1(a), it can be easily shown that

$$\cos\theta = \cos\beta\cos\alpha + \sin\beta\sin\alpha = \frac{v_{l_1}i_{l_1} + v_{l_2}i_{l_2}}{\|v_l\|\|i_l\|} = \frac{v_l^T i_l}{\|v_l\|\|i_l\|} \tag{2.5}$$

In Fig. 2.1(a), $\|v_l\|$ represents the length of the vector v_l. For example, $\|v_l\|$ is the hypotenuse of the triangle of Ov_lQ. The arrow between Figs. 2.1(a) and (b) indicates that the information obtained from Fig. 2.1(a) is used in Fig. 2.1(b). For example, $v_l^T i_l$, which is the projection (Op) of i_l onto vector v_l in Fig. 2.1(a) is used in Fig. 2.1(b) to denote active power. The following useful observations are immediately apparent from (2.5):

- The term $v_l^T i_l$, also known as inner or scalar or dot product of $\|v_l\|\|i_l\|$, will be zero if they are orthogonal [8].
- $v_l^T i_l \leq \|v_l\|\|i_l\|$.

Furthermore, from the avenue of linear circuit theory, the above observations can be translated as follows:

- From Figs. 2.1(a) and (b), the real power ($v_l^T i_l$ W) will be zero if $\|v_l\|$ and $\|i_l\|$ are orthogonal.
- $v_l^T i_l \leq \|v_l\|\|i_l\|$ which gives PF = $\cos\theta \leq 1$. In other words, PF can never be greater than unity.

- From Fig. 2.1(b), power factor is the ratio of active or real or true power to the total or apparent power ($\|v_l\|\|i_l\| = V_{l,rms}I_{l,rms}$ VA). The total power will be equal to the real power, if PF is unity.

2.1.1.C *Frequency-domain Interpretation*

Let the periodic functions v_l and i_l be represented by Fourier series as shown below:

$$\mathcal{FS}[v_l] = V_0 + \sum_{k=1}^{\infty} \sqrt{2}V_k \sin(k\omega + \gamma_k) \tag{2.6}$$

$$\mathcal{FS}[i_l] = I_0 + \sum_{k=1}^{\infty} \sqrt{2}I_k \sin(k\omega + \phi_k) \tag{2.7}$$

The magnitudes V_k and I_k, phase angles γ_k and ϕ_k and coefficients a_k, b_k, c_k and d_k are given by

$$\left.\begin{array}{rclcrcl} a_k &=& \frac{2}{T_l}\int_{T_l} v_l \cos(k\omega_l t)\, dt & & V_k &=& \sqrt{\frac{a_k^2+b_k^2}{2}} \\ b_k &=& \frac{2}{T_l}\int_{T_l} v_l \sin(k\omega_l t)\, dt & \text{and} & I_k &=& \sqrt{\frac{c_k^2+d_k^2}{2}} \\ c_k &=& \frac{2}{T_l}\int_{T_l} i_l \cos(k\omega_l t)\, dt & & \gamma_k &=& \tan^{-1}\frac{a_k}{b_k} \\ d_k &=& \frac{2}{T_l}\int_{T_l} i_l \sin(k\omega_l t)\, dt & & \phi_k &=& \tan^{-1}\frac{c_k}{d_k} \end{array}\right\} \quad k = 1, 2, \ldots \tag{2.8}$$

The values of V_0 and I_0 are defined as the DC values (averages) of v_l and i_l respectively. The coefficients of V_k and I_k, for $k = 1, 2, \ldots$ are the *RMS* values of the kth voltage and current harmonics. The Parseval's equality for this form of the series can be written as

$$v_{l,rms} = \|v_l\| = \sqrt{\left(V_o^2 + \sum_{k=1}^{\infty} V_k^2\right)} \tag{2.9}$$

$$i_{l,rms} = \|i_l\| = \sqrt{\left(I_o^2 + \sum_{k=1}^{\infty} I_k^2\right)} \tag{2.10}$$

$$P = \langle v_l i_l \rangle = V_0 I_0 + \sum_{k=1}^{\infty} V_k I_k \cos(\phi_k - \gamma_k) \tag{2.11}$$

From (2.8) to (2.11), the following can be concluded:

- A current harmonic component can produce active power only if it is matched by a voltage harmonic component of the *same* frequency and $\phi_k - \gamma_k \neq 90^0$.
- From (2.5) and (2.11), it can be observed that presence of unmatched components either in the voltage or current reduces PF below unity.
- Further from (2.5), (2.9), (2.10) and (2.11), it can be noticed that unity PF occurs if $\phi_k = \gamma_k$.

2.1.2 Power Factor for Sinusoidal Voltage

Although in practice the input-voltage profile is distorted and generally not known exactly, for analytical convenience, it can be assumed to be a pure sinusoid when analyzing utility supplied power converters. Therefore $V_k = 0$ for $k \neq 1$. Thus, PF can be expressed as

$$\mathrm{PF} = \frac{V_1 I_1 \cos\phi_1}{V_1 \left(I_0^2 + \sum_{k=1}^{\infty} I_k^2\right)^{1/2}} = \frac{I_1}{I_{l,rms}} \cos\phi_1 \tag{2.12}$$

which contains two terms. The first term, $I_1/I_{l,rms}$, is called *distortion factor*. If i_l contains no DC component, then distortion factor can be written as

$$\frac{I_1}{I_{l,rms}} = \frac{1}{\sqrt{1 + (\mathrm{THD})^2}} \tag{2.13}$$

where THD is the Total Harmonic Distortion. This factor represents only the harmonic content but provides no phase information. The harmonics present in i_l (other than the fundamental) cannot contribute any average power. Therefore, the distortion factor is less than unity and PF is correspondingly reduced.

The second term, $\cos\phi_1$, is called the *displacement factor*, and is the cosine of the angle between the fundamental components of the line-current and voltage. This term reduces the PF when the fundamental components are not in phase. In the case of pure linear load, the line-current contains only a fundamental component and PF is solely determined by the displacement factor.

If the load is reactive and nonlinear the input current can be both phase shifted (displaced) and distorted. Fragmenting the PF into two different factors is useful because these two problems require entirely different solutions. For instance, if a power system is heavily loaded with inductive (reactive) load, it will be compensated by installing suitable parallel capacitor banks near the distribution point of common coupling or by sometimes (rarely) using series compensation of transmission lines. However, a nonlinear load requires a different solution as will become clear in the next section.

2.2 The Capacitor-Input Filter

At low to medium-power levels, the most common method of producing DC power from the AC line uses a *capacitor-input filter* as shown in Fig. 2.2 [9]. The capacitor-input filter is a bridge rectifier followed by a filter capacitor. The bridge converts the AC voltage to DC while the capacitor forces the DC voltage to have a small ripple. The capacitor-input filter is a cheap, simple, and rugged system which is often used with a post-regulator to provide a well-regulated DC voltage. Switching post-regulators which are often used also provide a convenient place to introduce isolation.

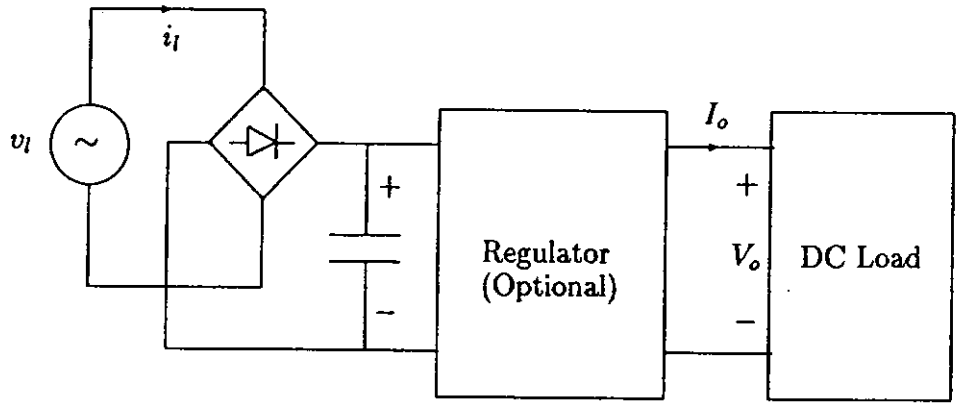

Figure 2.2: A capacitor-input filter AC-DC conversion system

Unfortunately, the capacitor-input filter suffers from a poor line-current waveshape. Since the output capacitor is large and maintains a nearly constant voltage, the diode bridge turns on only for a short time when the input voltage is close to its peak resulting in peaky input pulses of short duration as shown in Fig. 2.3. Although both Figs. 2.3(a) and (b) represent

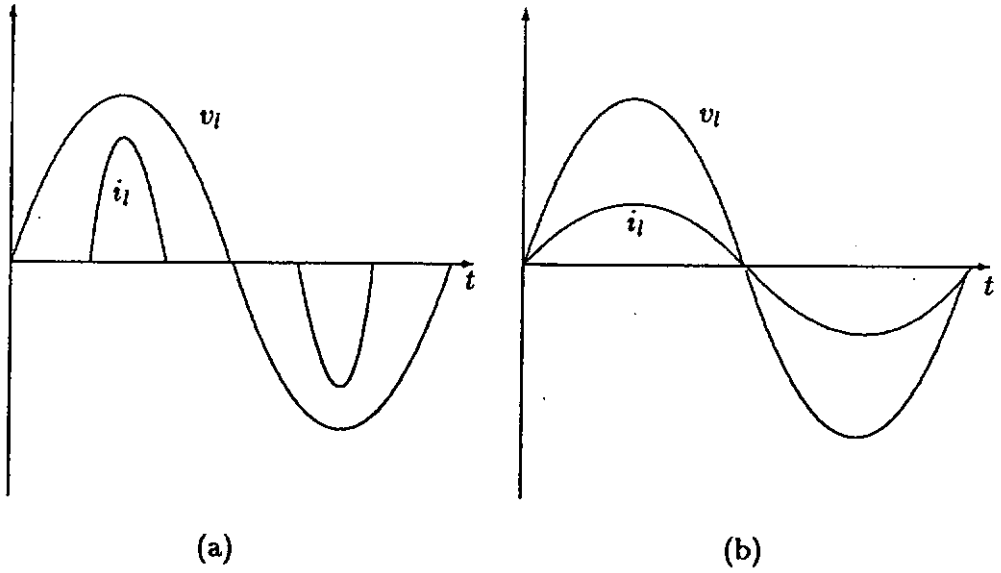

Figure 2.3: Capacitor input-filter (a) Line voltage and current waveforms (b) Line-voltage and current waveforms with a linear resistor connected directly across the line

the same consumption of average power for any given resistance R, the peak and RMS line-current shown in Fig. 2.3(b) is smaller than that shown in Fig. 2.3(a). Compared to the pure linear resistive case, the capacitor-input filter case shown in Fig. 2.3(a) demands a higher peak current resulting in a higher demand on the generators, transformers, circuit breakers and transmission lines in order to supply the same amount of average power for a given R. Hence, all the elements of a power distribution system should be designed for a higher rating, resulting in greater size, weight and cost.

The peaky input-current of the capacitor-input filter also leads to harmonic currents in the line, thus causing problems both to the power system and electronic systems. Therefore, an AC-DC conversion system is required to deliver power to a DC load like the capacitor-input filter and draw a *proportional* current like a pure linear resistive load. The circuits, which perform that function, will be the subject of the subsequent chapters. Before proceeding to the next chapter, some input-current shaping methods will be reviewed in the next section.

2.3 Input-current Shaping Methods

There are many methods of input-current shaping. They can be broadly classified as passive current-shaping and active current-shaping methods as shown in Table 2.1.

Input-current Shaping Methods		
Passive Shaping	Active Shaping	
Inductor-input filters	Automatic	Nonautomatic
Resonant-input filters	DCM PWM Converters	CCM PWM Converters
Tuned input filters	DCVM PWM Converters	Resonant Converters
	Half-wave Quasi-Resonant Converters	

Table 2.1: Classification of input-current shaping methods

A switching converter is said to operate in continuous conduction mode (CCM), if its inductor current never falls to zero and it is said to operate in discontinuous conduction mode (DCM), if its inductor current becomes zero for a portion of a switching period. In Table 2.1, DCVM denotes discontinuous capacitor voltage mode for which the voltage across a certain capacitor becomes zero for a portion of a switching period [10].

2.3.1 Nonautomatic Power-Factor-Correctors (PFCs)

Before the advent of average current-mode control (AMC) [11, 12] the CCM boost converter was considered to be the ideal topology for input-current shaping. However, due to the advantages of AMC, all the basic converters operating in CCM can be used as PFCs. Since the CCM input-current shapers need a separate control loop for input-current shaping, they are referred to as "nonautomatic" PFCs. Recently, some resonant converters were also proposed as nonautomatic PFCs [13]. However, the design and circuit operation are more complicated when compared to any other basic PWM PFC converter. Apart from this, when the load variation is large, there will be a wide range of frequency variation involved if they are operating in half-wave mode [13, 14].

2.3.2 Automatic PFCs

It has been well understood [15]-[18] that the basic PWM converters operating in DCM offer a near unity PF (UPF) *automatically* (absence of a separate control circuit) due to the inherent resistive input impedance. From the previous chapter, it is clear that UPF can be achieved if v_l and i_l have a strict linear relationship. However, theoretically UPF can be achieved in the case of the buck-boost converter without any constraints [16]. All the basic second-order converters are shown in Fig. 2.4 and their corresponding input-current waveforms are shown in Fig. 2.5. The waveforms are averaged over a switching period T to give the averaged input-current

$$I_{in} = \frac{1}{T}\left(\int_0^{DT} i_{in}(t)dt + \int_{DT}^{(D+D_1)T} i_{in}(t)dt + \int_{(D+D_1)T}^{T} i_{in}(t)dt\right) \tag{2.14}$$

where $i_{in}(t)$ is a function of both input and output voltage. According to the waveforms shown in Figs. 2.5(a), (b) and (c), the switching frequency averaged input-currents are given by

$$\text{Buck converter:} \quad I_{in} = \frac{D^2T}{2L}(\hat{e} - v_o) \tag{2.15}$$

$$\text{Buck-boost converter:} \quad I_{in} = \frac{D^2T}{2L}\hat{e} \tag{2.16}$$

$$\text{Boost converter:} \quad I_{in} = \frac{D^2T}{2L}\left(\frac{v_o\hat{e}}{\hat{e}-v_o}\right) \tag{2.17}$$

where $\hat{e} = E_p \sin\theta$. Then, the input impedances $\hat{e}/I_{in}$ are calculated and listed in Table 2.2 for constant duty-ratio and switching period, where M denotes the conversion ratio $M = V_o/E_p$.

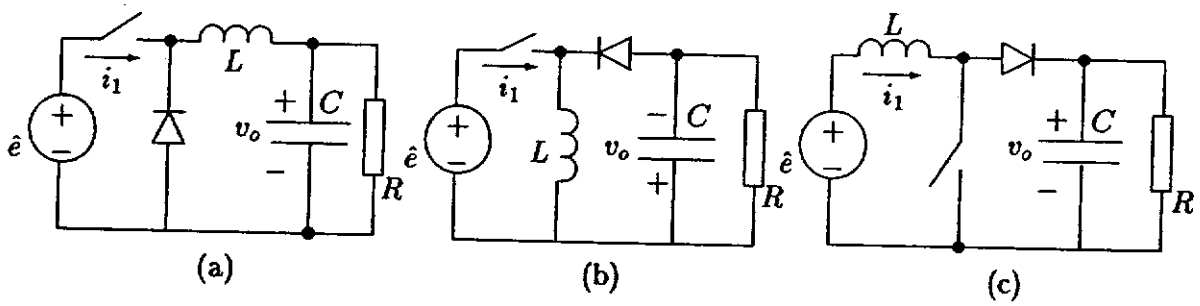

Figure 2.4: (a) Buck converter ; (b) Buck-boost converter ; (c) Boost converter

Input Resistance		
Converter	$Z_{in} = \frac{\hat{e}}{I_1}$	Nature of Z_{in}
Buck	$\frac{2L}{D^2T}\left(\frac{\sin\theta}{\sin\theta - M}\right)$	Nonlinear
Buck-Boost	$\frac{2L}{D^2T}$	Linear
Boost	$\frac{2L}{D^2T}\left(\frac{M-\sin\theta}{M}\right)$	Nearly linear if $M \gg 1$

Table 2.2: Comparison of input resistances of second-order DCM PFC converters ($M = V_o/E_p$)

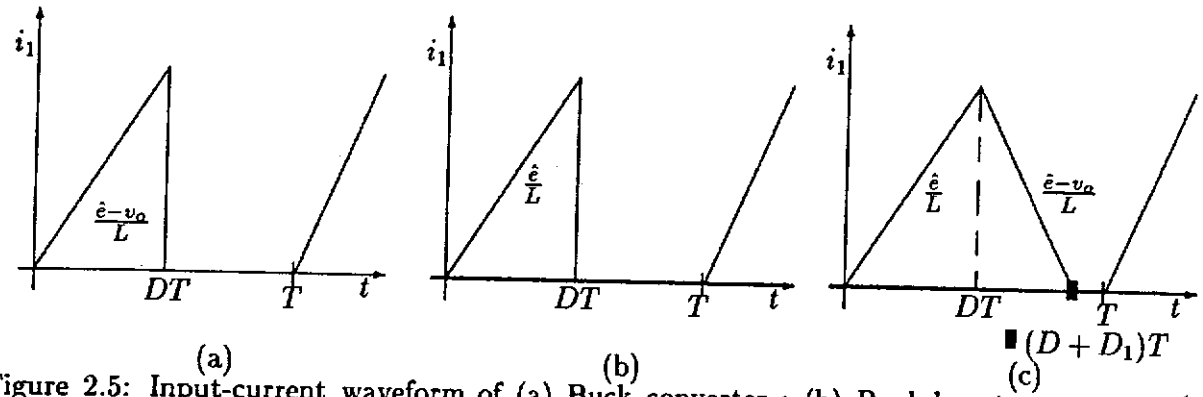

Figure 2.5: Input-current waveform of (a) Buck converter ; (b) Buck-boost converter ; (c) Boost converter (The entries on the waveforms represent current slopes.)

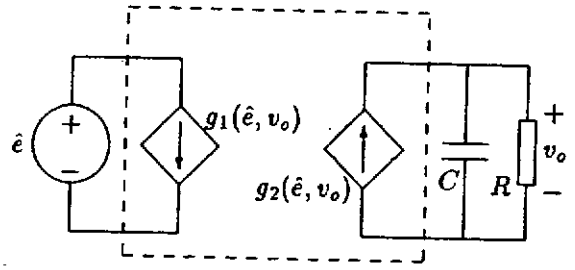

Figure 2.6: (a) General averaged model of a second-order converter operating in DCM

Table 2.2 suggests that to obtain a maximum PF the best choice among second-order converters is the buck-boost converter because the input impedance is purely linear and devoid of dynamics. It can be noticed that the next possible alternative is the boost converter wherein the input impedance can be made nearly linear if the voltage conversion ratio M is made sufficiently greater than 1. A detailed analysis of Total Harmonic Distortion and PF of all these basic DCM second-order converters can be found in Freeland [16] and in Liu *et al.* [17].

Fourth-order converters, namely Ćuk [19], SEPIC [20, 21] and Zeta [22] converters, can also be used as automatic PFCs. It can be noticed that especially for low-power applications i.e. for less than 200W, the second-order converters, having less components, seem to outweigh the fourth-order converters. This is the main reason for limiting the focus of study to second-order PWM DCM converters.

2.4 Concluding Remarks

In this chapter all the basic PWM second-order converters are examined to determine their suitability as automatic PFC regulators. None of the converters, irrespective of their switching techniques and/or operating modes, can serve as a modular PFC power supply since fast output-voltage regulation and PFC cannot be achieved in a single converter [16], [23]. At this stage, this important commercial requirement provides a strong motivation for deriving the single-stage cascaded topologies which will be the subject of the next chapter.

Chapter 3

Single-stage Cascaded PWM PFC Converters

In the previous chapter it can be gleaned that all the second-order and fourth-order converters provide *automatic* current-shaping when operating in DCM under some constraints whereas the converters operating in CCM require a separate input-current shaping control loop. For applications requiring both PFC and fast output-voltage regulation, a line-frequency storage element is mandatorily required to buffer the difference between the varying input power and constant DC output power. Thus, in the absence of a line-frequency storage element, any simple converter cannot satisfactorily provide good PFC and fast output-voltage regulation, irrespective of the operating modes [16], [23, 24]. Now an obvious question arises:
Can any other topology provide both high PF and voltage regulation ?
This chapter presents and compares the existing and new buck-based topology which are derived by cascading the basic second-order converters.

3.1 Requirements of a PFC Regulator

Any PFC regulator intended for commercial applications must have the following features:

- **Near linear input resistor emulation**
  From chapter 2, it is clear that the instantaneous line-current should be proportional to the line-voltage to achieve unity PF. This function can be achieved automatically or by using a separate current-shaping circuit. However, the main concern here is to achieve a high PF automatically, and to ensure that the emulated input resistance is nearly linear and devoid of any dynamics.

- **Internal line-frequency energy storage**
  It is clear that a line-frequency energy storage is needed to buffer the difference between the varying input power and the constant DC output power. Extra energy may be needed if there is any hold-up requirement. This line-frequency energy storage has to be *internal* in order to avoid any second-harmonic line-frequency ripple appearing across the

DC load thus eliminating the need for a large output capacitor across the load. Therefore, when low-frequency energy is stored internally, fast output-voltage regulation is possible. Hence, internal energy storage is preferable rather than external energy storage.

- **Fast regulation of load-voltage**
  The PFC converter's input-voltage and the internal energy storage capacitor contain the line second-harmonic component ($2\omega_l$). This harmonic component should be reduced to a minimum or should be ideally made absent at the load by a suitable design of capacitors and inductors. This facilitates the designer to provide a wide bandwidth i.e., a high crossover frequency sufficiently greater than the second-harmonic line-frequency [1]. It should be noted that fast regulation of load-voltage is possible if internal low-frequency energy storage is present.

There are many ways to incorporate the above features, *e.g.*,

- Conventional two-stage cascaded scheme ;
- Single-stage cascaded scheme [1]-[4], [25, 26] ;
- Single-stage parallel scheme [28, 29].

Here the focus is only on the single-stage cascaded scheme which cascades two simple converters sharing a single active switch. In this system, the input converter stage is used for PFC and the output converter stage for output-voltage regulation, as shown in the block diagram of Fig. 3.1. Such converters can operate in a number of operating modes. Essentially, the PFC

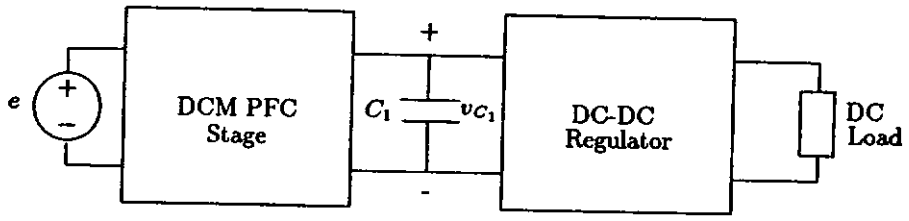

Figure 3.1: Block diagram of a cascaded PFC regulator

converter (input) stage and the DC-DC converter (output) stage can operate in either DCM or CCM. For brevity, DCM-CCM will be used to denote the operation of PFC regulator in which the PFC stage operates in DCM while the DC-DC converter stage operates in DCM-CCM. Likewise, DCM-DCM is used to denote the operation in which both the PFC stage and the DC-DC converter stage are in DCM, etc. Table 3.1 summarizes some properties of common cascaded PFC converters. Circuit complexity implies the number of components. For example, a two-switch cascade has a larger number of components when compared to a single-switch cascade. Control complexity implies the number of control loops required to achieve both PFC

when compared to a single-switch cascade. Control complexity implies the number of control loops required to achieve both PFC and fast output-voltage regulation. For example, a single-switch cascaded converter operating in CCM-DCM requires more than one loop whereas it requires just a single control loop for output-voltage regulation when operating in DCM-DCM. From Table 3.1, it can be concluded that for low-power applications, the single-switch cascaded topology is the most suitable.

3.2 Cascaded PFC Converters

Based on pure cascade combination of the basic second-order converters, nine topologies are derived as shown in Figs. 3.2 to 3.10. The two-switch nonisolated version of the cascaded converters are shown in Figs. 3.2(a) to 3.10(a) and nonisolated single-switch versions are shown in Figs. 3.2(b) to 3.10(b) where some have been derived by using the grafted tree technique [6, 7]. Some of the isolated versions are shown in Figs. 3.11 and 3.12. However, the BIFRED [1], decoupled Zeta and the new topology shown in Figs. 3.13(a),(b) and 3.14 respectively are not pure cascaded topologies since the input and output ports form a loop during a subinterval of a switching period.

Topology	DCM-DCM		DCM-CCM	CCM-DCM	CCM-CCM
2-switch cascade OR parallel scheme	Circuit complexity	yes	yes	yes	yes
	Control complexity	yes	yes	yes	yes
	Input filter	yes	yes	no	no
	Medium and high power	no	no	no	yes
1-switch cascade	Circuit complexity	no	no	no	Difficult to provide both PFC and fast regulation
	Control complexity	no	no	yes	
	Input filter	yes	yes	no	
	Medium and high power	no	no	no	

Table 3.1: Comparison of two-switch and single-switch cascaded PFC converters

In Table 3.1, input filter is the filter which is used to filter out DCM switching frequency ripples of input current and it does *not* refer to an input EMI filter which is invariably used to filter out the conducted EMI.

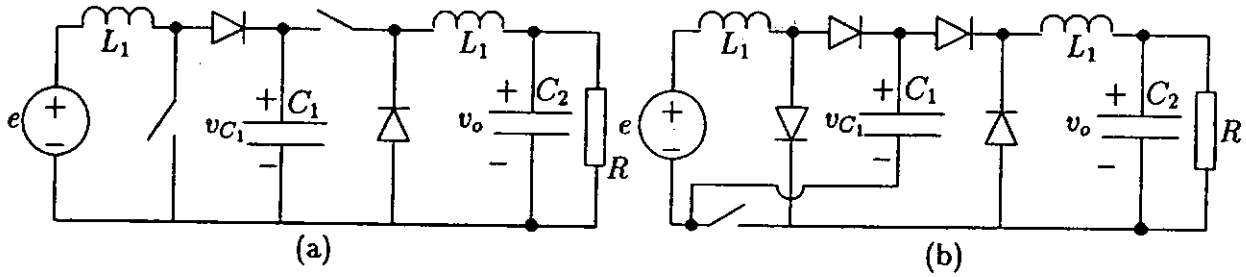

Figure 3.2: Cascaded boost-and-buck converter (a) Two-switch ; (b) Single-switch

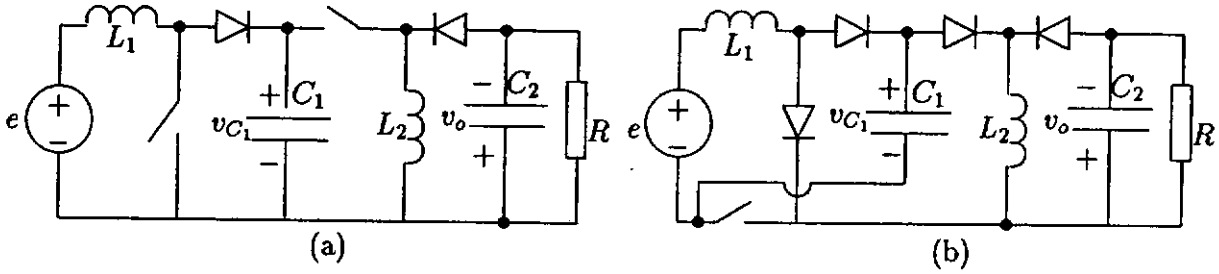

Figure 3.3: Cascaded boost-and-flyback converter (a) Two-switch ; (b) Single-switch

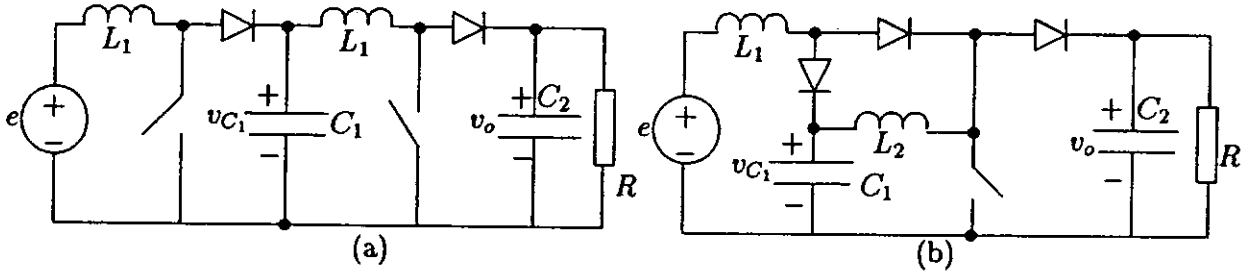

Figure 3.4: Cascaded boost-and-boost converter (a) Two-switch ; (b) Single-switch

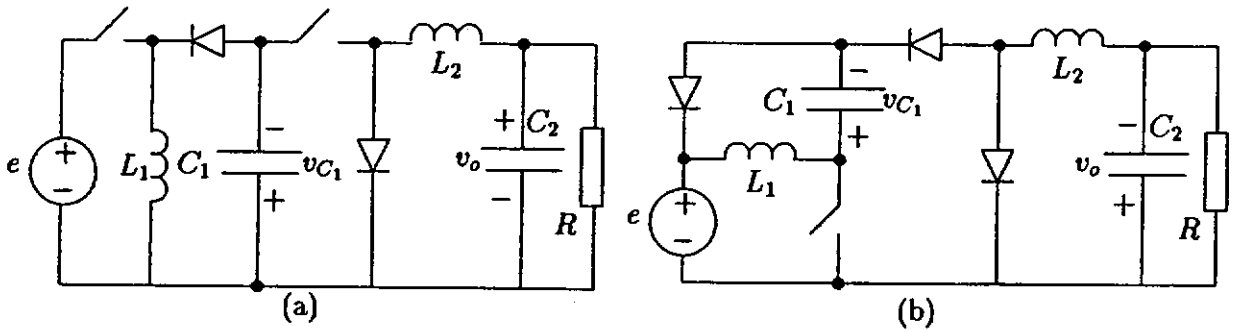

Figure 3.5: Cascaded flyback-and-buck converter (a) Two-switch ; (b) Single-switch

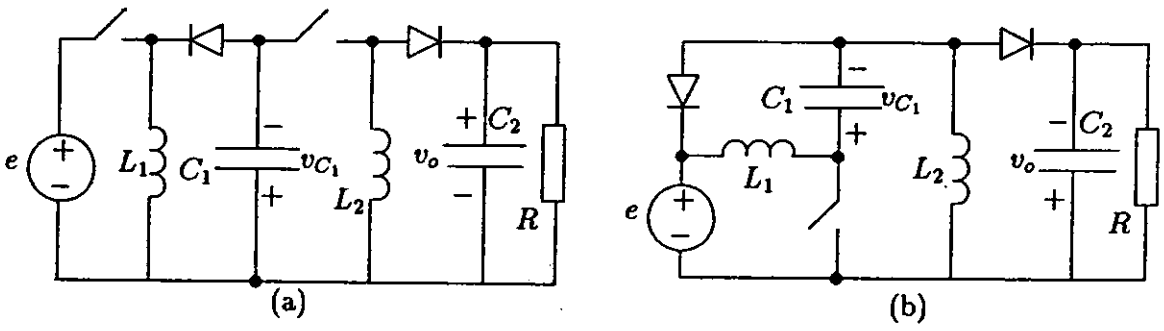

Figure 3.6: Cascaded flyback-and-flyback converter (a) Two-switch ; (b) Single-switch

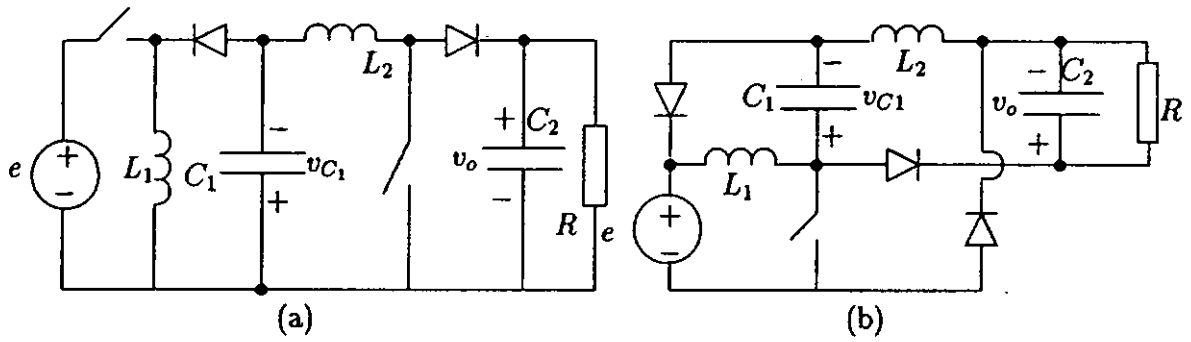

Figure 3.7: Cascaded flyback-and-boost converter (a) Two-switch ; (b) Single-switch

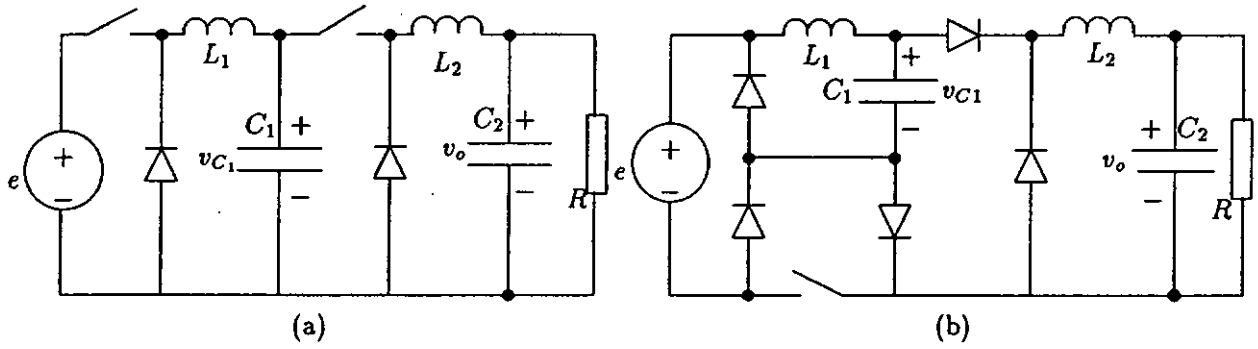

Figure 3.8: Cascaded buck-and-buck converter (a) Two-switch ; (b) Single-switch

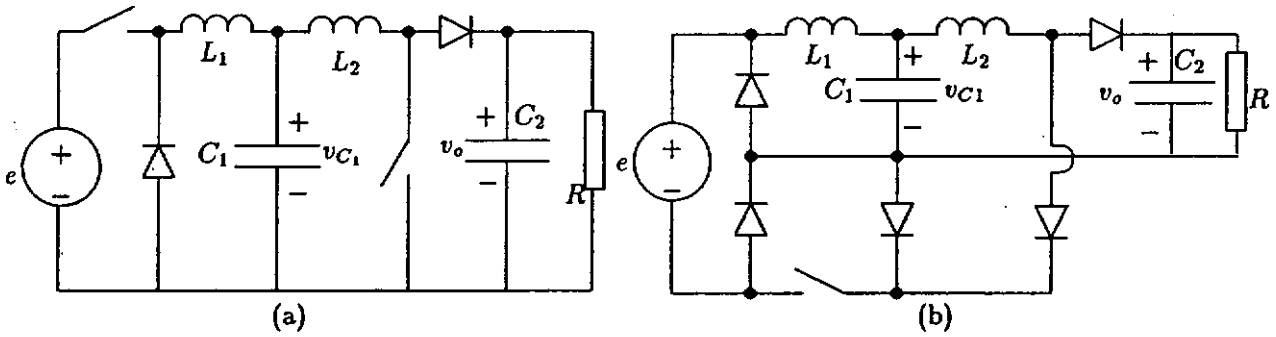

Figure 3.9: Cascaded buck-and-boost converter (a) Two-switch ; (b) Single-switch

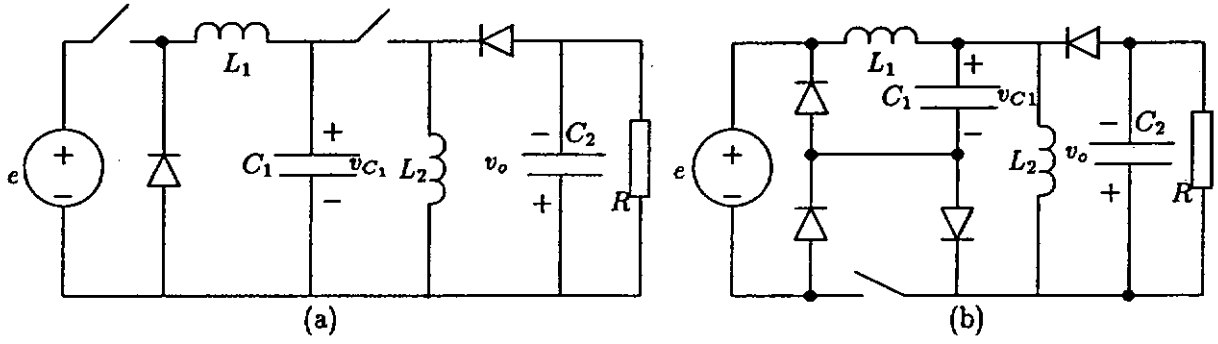

Figure 3.10: Cascaded buck-and-flyback converter (a) Two-switch ; (b) Single-switch

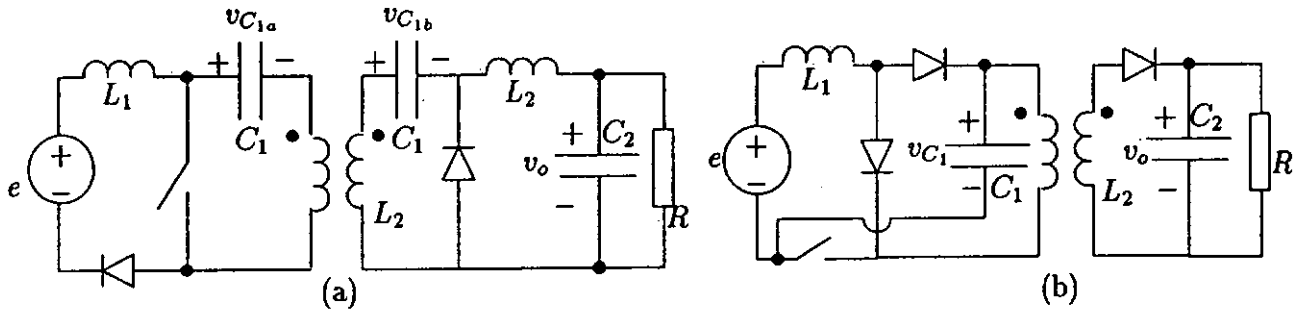

Figure 3.11: Isolated version of (a) Cascaded boost-and-buck converter (b) Cascaded boost-and-flyback converter

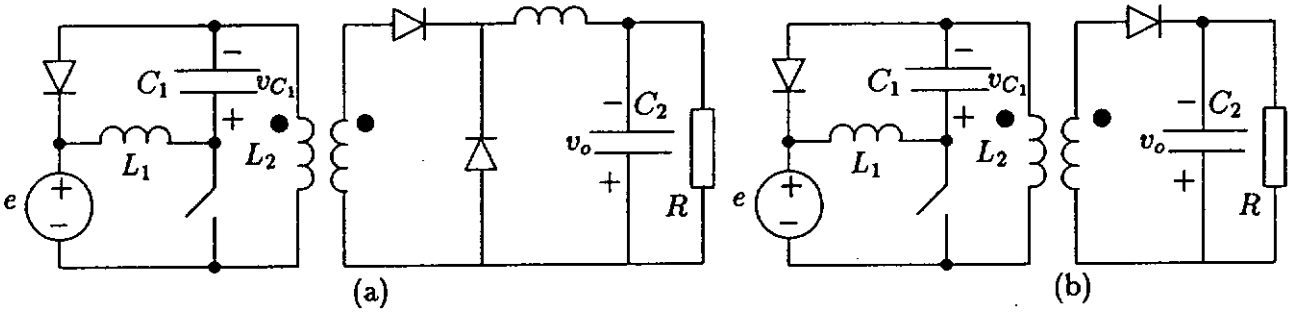

Figure 3.12: Isolated version of (a) Cascaded flyback-and-buck converter (b) Cascaded flyback-and-flyback converter

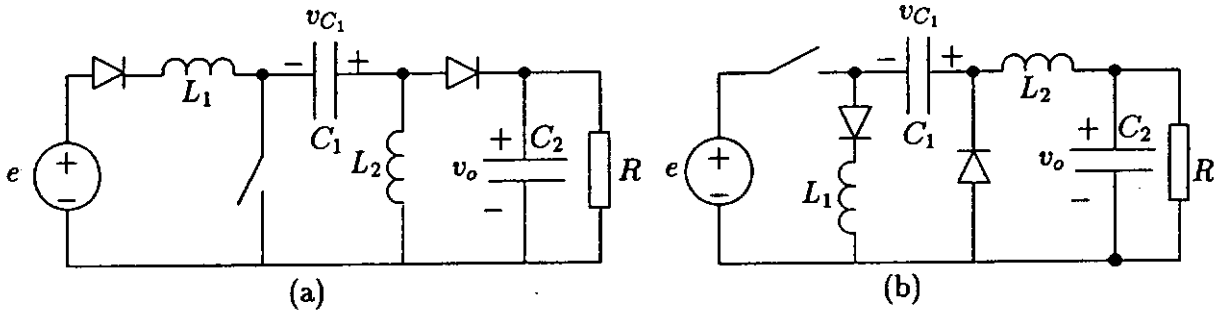

Figure 3.13: Nonisolated version of (a) BIFRED ; (b) Decoupled Zeta converter

3.3 Feasibility of Single-switch Cascaded Converters

As mentioned earlier, the most important preliminary requirements for a converter to function as a PFC regulator are

1. near linear input resistor emulation;
2. internal line-frequency energy storage; and
3. fast regulation of output-voltage.

The topological requirements to incorporate the above features are outlined as follows:

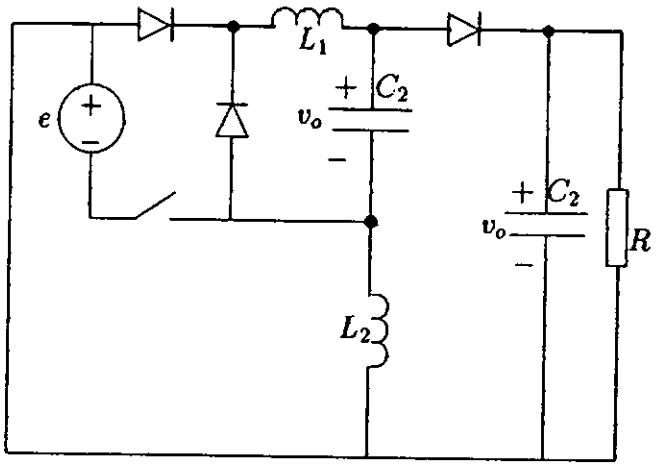

Figure 3.14: Buck based topology

Cascaded converter	Reasons
Boost-&-boost (Fig. 3.4(b))	Cannot operate properly for $D > 0.5$ Difficult to introduce isolation
Flyback-&-flyback (Fig. 3.6(b))	Cannot operate properly for $D > 0.5$
Buck-&-buck (Fig. 3.8(b))	Requires a large C_1
Buck-&-flyback (Fig. 3.10(b))	Requires a large C_1
Buck-&-boost (Fig. 3.9(b))	Requires a large C_1 Difficult to introduce isolation
BIFRED (Fig. 3.13(a))	Requires a large C_2

Table 3.2: Reasons for single-switch cascaded converters not capable of serving as PFC regulators

1. In Tse [18] the details of incorporating the first feature are analyzed. It has been proved that the input impedance of a switching converter operating under constant duty-ratio and switching frequency will be purely linear and resistive, if no loop is formed that contains both the input port and the output port during the entire switching period. Hence, the analysis easily identifies the buck-boost converter as the ideal choice for pure input resistance emulation.

2. In Madigan *et al.* [1] the details of incorporating the second feature are given. It was recognised that the key to development of integrated high quality rectifier-regulators is that the low-frequency components of the input-voltage e, the energy storage capacitor voltage v_{C_1} and the load-voltage v_o must all be independent and hence the converter topology must possess sufficient degrees of freedom to allow these voltages to vary arbitrarily. This was realized by placing high-frequency switching elements between e, v_{C_1} and v_o to block the low-frequency components of these voltages.

and v_o to block the low-frequency components of these voltages.

3. The third feature can be *partially* incorporated by ensuring:

   I. *Absence of any loop containing input and output ports during any portion of switching interval.*

   For example, in the case of BIFRED shown in Fig. 3.13 during the discharging interval of inductor L_1, the input and output ports form a loop. This causes the input second-harmonic line-frequency to appear across the load capacitor C_2. This necessitates a large C_2 which makes the converter unsuitable as a PFC regulator with the conventional duty-ratio control scheme.

   II. *Absence of any high-frequency reactive element belonging to either of the converter stage, which may charge itself directly from the input, and discharge its energy directly to the output.*

   For example in the new topology shown in Fig. 3.14, unlike BIFRED there is no loop formation involving both the input and output ports. However, the high-frequency reactive element L_2 which forms a loop with the input port discharges all its energy to the output port. This again necessitates a large C_2 which makes the converter unsuitable as a PFC regulator with the conventional duty-ratio control scheme.

   The above mentioned criteria ensure the elimination of the AC second-harmonic component of the line-voltage across the output port, thus enabling the designer to choose a small C_2 which is enough to filter the switching frequency ripples and to give a fast response.

Apart from the above three requirements, electrical isolation may be needed, if the converter is expected to operate as an off-line power supply. Among the nine single-stage PFC converters, boost-and-buck, boost-and- flyback, flyback-and-buck PFC converters are the readily feasible converters since they satisfy all the above mentioned requirements including the requirement of electrical isolation. With the above three basic requirements borne in mind, the phrase ***readily feasible*** implies further that the converter does not need any sophisticated control such as simultaneous duty-ratio and switching frequency control and/or a complicated electrical isolation. The converters which are not readily feasible are tabulated in Table 3.2. with the associated reasons, which are elaborated as follows:

- In all the buck based topologies of Table 3.2, large C_1 is generally required, which is due to two reasons.

  1. In Tse [18], the peak-to-peak ripple is derived as $\Delta v_{C_1} = P_o/4\pi f_i C V_{C_1}$. In the case of the buck converter, $V_{C_1} < E$. So Δv_{C_1} will be larger when compared to a boost converter.

2. *Near linear input resistance emulation* dictates that $V_{C_1} \ll E$ [18]. This further requires a larger C_1.

- In the case of BIFRED, there is a loop formation involving both the input and output ports during a portion of switching interval. This necessitates a large C_2 at the load to provide a low ripple voltage at the load. This impairs the dynamical response.

3.4 Concluding Remarks

At this stage, it is well understood that linear input resistor emulation, internal low-frequency energy storage and fast output-voltage regulation are the the fundamental requirements for any converter topology to function as PFC regulator. Fast dynamical response is partially ensured by internal low-frequency energy storage. Consequently, two new topological criteria are proposed which can easily determine whether a given topology is *readily* feasible as a PFC regulator. Hence, the above mentioned preliminary requirements and topological conditions are used to determine whether the cascaded single-switch converter can function as a PFC regulator. In the next chapter, all the feasible converters will be compared against the switch, inductor and diode RMS, peak and average currents, steady-state voltage relationships and operating mode boundaries.

Chapter 4

Comparison of Cascaded PWM PFC Converters

In the previous chapter, nine different topologies along with some special topologies were analyzed and some of them were found not to be readily feasible based on the preliminary requirements and some new topological criteria. In this chapter, the converters, which were found to be suitable as PFC regulator, will be compared against the switch and diode RMS, peak and average currents, steady-state voltage relationships and conduction mode boundaries. This information is extremely useful for the design of the single-stage cascaded PFC converters.

4.1 Calculation of Average, RMS and Specific Switch Stress

4.1.1 Average Value

Average value or the DC value of a given periodic function $i(t)$ can be defined in terms of the following integral [30]:

$$I = \frac{1}{T}\int_0^T i(t)\ dt \tag{4.1}$$

where T is the period of $i(t)$. The average value is used in evaluating the low-frequency behaviour of switching converters.

4.1.1.A Average Switch Current in a Cascaded Converter Operating in DCM-CCM

Consider the switch current of a cascaded boost-and-buck converter operating in DCM-CCM. In general, the waveform of a switch current i_{sw} is shown in Fig. 4.1(a) from which the average switch current I_{sw} can be found as

$$I_{sw} = \frac{1}{T}\int_0^{DT}\left[\frac{E}{L_1}t + DI_0 - DT\frac{(V_{C_1} - V_o)}{L_2} + \frac{(V_{C_1} - V_o)}{L_2}t\right]dt = \frac{D^2T}{2L_1}E + DI_o \tag{4.2}$$

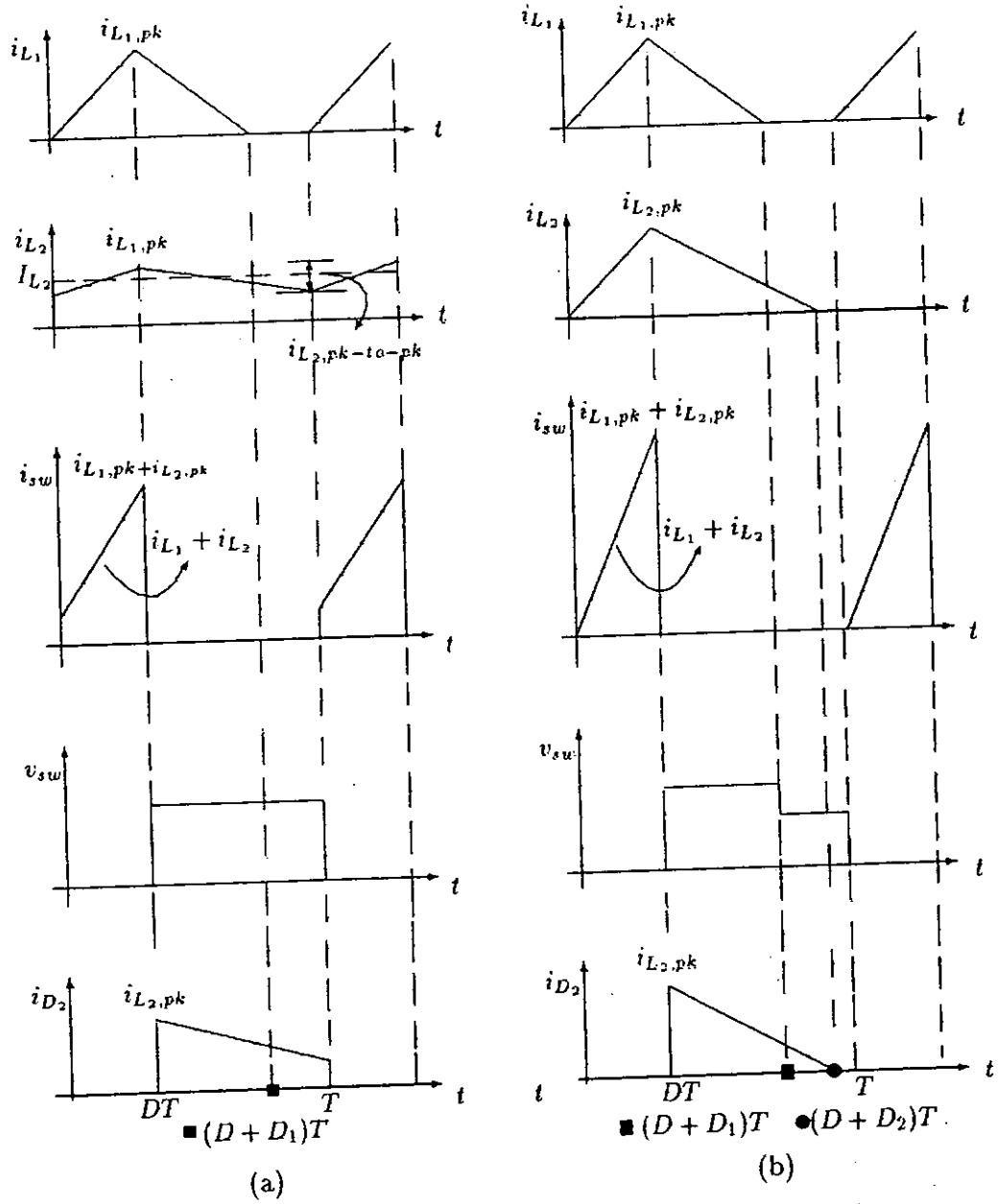

Figure 4.1: Switching waveforms of cascaded converter (a) DCM-CCM ; (b) DCM-DCM

4.1.1.B Average Switch Current in a Cascaded Converter Operating in DCM-DCM

Consider the switch current of a cascaded boost-and-flyback converter operating in DCM-DCM. In general, the waveform of a switch current i_{sw} is shown in Fig. 4.1(a).

$$I_{sw} = \frac{1}{T}\int_0^{DT}\left[\frac{Et}{L_1} + \frac{V_{C_1}}{L_2}t\right]dt = \frac{D^2T}{2}\left(\frac{E}{L_1} + \frac{V_{C_1}}{L_2}\right) \tag{4.3}$$

Likewise, the average current of other converters can be found as tabulated in Table 4.1.

4.1.2 Root Mean Square (RMS) Value

RMS value can be defined in terms of the following integral [30]:

$$I_{rms} = \left[\frac{1}{T}\int_0^T i^2(t)dt\right]^{\frac{1}{2}} \tag{4.4}$$

where $i(t)$ is a periodic function with period T. RMS values are used in the calculation of losses and efficiency.

4.1.2.A RMS Value of the Inductor Current in CCM

Consider the RMS value of the CCM inductor current i_{L_2} of a buck converter. In general, the waveform is shown in Fig. 4.1(a).

$$I^2_{L_2,rms} = \frac{1}{T}\int_0^T [i_{ch}(t) + i_{disch}(t)]^2\, dt = \frac{1}{T}\int_0^T [i_{ch}(t) + i_{disch}(t) + 2i_{ch}(t)i_{disch}(t)]^2\, dt \tag{4.5}$$

At any instant of time both the charging current $i_{ch}(t)$ and discharging current $i_{disch}(t)$ cannot have a nonzero value [31]-[33]. This implies that the third term $2i_{ch}(t)i_{disch}(t)$ of RHS of (4.5) is zero. Hence, the RMS inductor current can be expressed as the sum of its RMS charging current and RMS discharging current. Then $I^2_{L_2,rms}$ can be expressed as

$$I^2_{L_2,rms} = I^2_{ch,rms} + I^2_{disch,rms} = I^2_{ch,rms} + I^2_{D_2,rms} \tag{4.6}$$

The RMS charging current is given by

$$I^2_{ch,rms} = \frac{1}{T}\int_0^{DT}\left[I_o - \left(\frac{V_{C_1} - V_o}{2L_2}\right) + \frac{(V_{C_1} - V_o)t}{L_2}\right]^2 dt = D\left[I_o^2 + D^2T^2\frac{(V_{C_1} - V_o)}{12L_2^2}\right] \tag{4.7}$$

where I_o is the average (DC) inductor or load current V_o/R which is equal to I_{L_2} shown in Fig. 4.1(a). Also, $i_{sw}(t) \neq i_{ch}(t)$ because the buck converter is assumed to be cascaded with an input converter stage. The RMS discharging current is given by

$$I^2_{D_2,rms} = \frac{1}{T}\int_{DT}^{T}\left[I_o + \left(\frac{V_{C_1} - V_o}{2L_2}\right)DT - \frac{V_o(t - DT)}{L_2}\right]^2 dt = (1 - D)\left[I_o^2 + D^2T^2\frac{(V_{C_1} - V_o)}{12L_2^2}\right] \tag{4.8}$$

Substituting (4.7) and (4.8) in (4.5) results in

$$I^2_{L_2,rms} = I^2_{ch,rms} + I^2_{D_2,rms} = I_o^2 + D^2T^2\frac{(V_{C_1} - V_o)}{12L_2^2} = I_o^2 + \frac{i^2_{L_2,pk-to-pk}}{12} \tag{4.9}$$

where $i_{L_2,pk-to-pk}$ is the peak-to-peak ripple of the inductor current i_{L_2} shown in Fig. 4.1(a). Then normalizing (4.9) with I_o^2 as the base value results in

$$I^2_{L_2,rms,n} = \frac{I^2_{L_2,rms}}{I_o^2} = 1 + D^2T^2\frac{(V_{C_1} - V_o)}{12I_o^2L_2^2} \tag{4.10}$$

where subscript n denotes normalized value. Putting $I_o = V_o/R$, $K_2 = 2L_2/RT$ and $(V_{C_1} - V_o)D = V_o(1-D)$ in (4.10) and simplifying give

$$I^2_{L_2,rms,n} = 1 + \frac{(1-D)^2}{3K_2^2} \tag{4.11}$$

In Tables 4.3, 4.4, 4.5 and 4.6 the following new quantities have been introduced for brevity of notation:
$M_1 = V_{C_1}/E$, $M_2 = V_O/V_{C_1}$, $K_1 = 2L_1/RT$, $K_2 = 2L_2/RT$.

4.1.2.B RMS Value of the Inductor Current in DCM

Consider the RMS value of a DCM inductor current i_{L_1} of a boost converter. In general, the waveform is shown in Fig. 4.1(b). Using the same definition of RMS value given previously, the RMS charging current is given by

$$I^2_{ch,rms} = \frac{1}{T}\int_0^{DT}\left(E\frac{t}{L_1}\right)^2 dt = E^2\frac{D^3T^2}{3L_1^2} \tag{4.12}$$

The RMS discharging current is given by

$$I^2_{disch,rms} = \frac{1}{T}\int_{DT}^{(D+D_1)T}\left[E\frac{DT}{L_1} - (E - V_{C_1})\left(\frac{t-DT}{L_1}\right)\right]^2 dt = \frac{D^3T^2}{3L_1^2}\left[\frac{E^2}{M_1 - 1}\right] \tag{4.13}$$

where $D_1 = DE/(V_{C_1} - E)$. The RMS value of inductor current i_{L_1} in DCM can be written as

$$I^2_{L_1,rms} = I^2_{ch,rms} + I^2_{disch,rms} = \frac{D^3T^2E^2}{3L_1^2}\left[\frac{M_1}{(M_1-1)}\right] \tag{4.14}$$

Then normalizing (4.14) with I_o^2 as the base value results in

$$I^2_{L_1,rms,n} = \frac{I^2_{L_1,rms}}{I_o^2} = \frac{D^3T^2E^2}{3I_o^2L_1^2}\left[\frac{M_1}{(M_1-1)}\right] \tag{4.15}$$

Substituting $D = M_2\sqrt{K_1M_1(M_1-1)}$ [36], $I_o = V_o/R$ and $K_1 = 2L_1/RT$ in (4.15) and simplifying give

$$I^2_{L_1,rms,n} = \frac{4D}{3K_2} \tag{4.16}$$

Similarly, the inductor RMS and diode RMS currents of other converters are calculated and listed in Table 4.3.

4.1.2.C Specific Switch Stress in a Cascaded Converter Operating in DCM-CCM

Consider the RMS value of the switch current in a cascaded boost-and-buck converter where the input boost stage is operating in DCM and the output buck stage is operating in CCM.

From Fig. 4.1(a) it can observed that switch current i_{sw}, is essentially the sum of the charging currents of the inductors of both the stages.

$$I_{sw,rms}^2 = \frac{1}{T}\int_0^{DT} [i_{L_1,ch}(t) + i_{L_2,ch}(t)]^2\, dt \tag{4.17}$$
$$= \frac{1}{T}\int_0^{DT} \left[\frac{E}{L_1}t + I_o - \left(\frac{V_{C_1} - V_o}{2L_2}DT\right) + \frac{(V_{C_1} - V_o)}{L_2}t\right]^2 dt$$

The normalized RMS switch current $I_{sw,rms,n}$ is given by

$$I_{sw,rms,n}^2 = \frac{D^3T^2(L_1(V_{C_1}-V_o)+L_2E)^2}{3I_o^2L_1^2L_2^2} + \frac{D(2I_oL_2-DTV_{C_1}+D^2TV_{C_1})^2}{4I_o^2L_2^2} + \frac{D^2T(2I_oL_2-DTV_{C_1}+D^2TV_{C_1})(L_1(V_{C_1}-V_o)+L_2E)}{2I_o^2L_1L_2^2} \tag{4.18}$$

The normalized specific switch stress $P_{ss,n}$, is defined as $V_{sw,off}I_{sw,rms}/P_o$. Putting $P_o = V_oI_o$ and $V_{sw,off} = V_{C_1}$ in (4.18) and simplifying yields

$$P_{ss,n} = \frac{1}{M_2}\sqrt{D + \frac{D(1-2D)}{3K_2^2} + \frac{D}{3}\left(\frac{2}{K_1M_1} + \frac{D}{K_2}\right)^2 + \frac{2D}{K_1M_1}\left(1 + \frac{1-3D}{3K_2}\right)} \tag{4.19}$$

4.1.2.D Specific Switch Stress in a Cascaded Converter Operating in DCM-DCM

Consider the RMS value of the switch current in a cascaded boost-and-buck converter where both the input boost stage and output buck stage are operating in DCM as shown in Fig. 4.1(b). Using a similar approach as in section 4.1.2.C, the RMS value can be written as

$$I_{sw,rms}^2 = \frac{1}{T}\int_0^{DT} [i_{L_1,ch}(t) + i_{L_2,ch}(t)]^2\, dt = \frac{1}{T}\int_0^{DT} \left[E\frac{t}{L_1} + \frac{(V_{C_1} - V_o)}{L_2}t\right]^2 dt \tag{4.20}$$

The normalized RMS switch current is given by

$$I_{sw,rms,n}^2 = \frac{D^3T^2(L_1(V_{C_1}-V_o)+L_2E)^2}{3I_o^2L_1^2L_2^2} \tag{4.21}$$

Putting $P_o = V_oI_o$ and $V_{sw,off} = V_{C_1}$ in (4.21) and simplifying, the normalized specific switch stress $P_{sw,rms,n}$ is given by

$$P_{sw,rms,n} = \sqrt{\frac{D}{3}}\left[\frac{2D}{M_2^2}\left(\frac{1}{K_1M_1} + \frac{1}{K_2} - \frac{M_2}{K_2}\right)\right] \tag{4.22}$$

Similarly, the normalized specific switch stresses of other cascaded converters are calculated and they are listed in Table 4.4. Though the cascaded converters listed in Table 3.2 are deemed unfeasible, they can be still used if

- transformer isolation could be provided in the case of cascaded flyback-and-boost and cascaded boost-and-boost PFC converters;
- a complicated control like the *simultaneous duty-ratio and switching frequency control* can be applied especially for the case of BIFRED operating in DCM-CCM [1], [34].

This control is suitable only if the converter is operating in DCM-CCM because any variation of switching frequency will not affect the output-voltage regulation. Hence, switching frequency modulation is used exclusively for achieving unity PF and duty-ratio modulation is used for output-voltage regulation; and

- a complicated control which uses load-current and duty-ratio as the feedback signals can be applied, especially for the case of BIFRED operating in DCM-DCM [5]. In Table 4.3, $I^2_{L,rms,n}$ of the input stage of BIFRED is the same as that of the boost (input stage) converter and $I^2_{L,rms,n}$ of the output stage of BIFRED is the same as that of the flyback (output stage) converter.

Cascaded converter	$I_{sw,dc}$		I_{pk}	$V_{sw,off}$
	DCM-DCM	DCM-CCM		
Boost-&-Buck,	$D^2T\left(\frac{E}{2L_1}+\frac{V_{C_1}-V_o}{2L_2}\right)$	$\frac{D^2TE}{2L_1}+DI_o$ BIBRED	$\frac{EDT}{L_1}+\frac{V_{C_1}-V_o}{L_2}$	V_{C_1}
Flyback-&-buck	same as above	same as above	same as above	$V_{C_1}+E$
Boost-&-flyback	$D^2T\left(\frac{E}{2L_1}+\frac{V_{C_1}}{2L_2}\right)$	$\frac{D^2TE}{2L_1}+DI_{L2}$	$\frac{EDT}{L_1}+\frac{V_{C_1}}{L_2}$	V_{C_1}
BIFRED	same as above	same as above	same as above	$V_{C_1}+V_o$
Boost-&-Boost	same as above	same as above	same as above	V_{C_1}
Flyback-&-Boost	same as above	same as above	same as above	$V_{C_1}+E$
Flyback-&-flyback	same as above	same as above	same as above	$V_{C_1}+E$

Table 4.1: Average and peak expressions of switch current

In order to visualize the variation of the specific switch stresses with input DC voltage ratios and to compare the stress values of different converters, the normalized stresses are plotted in Figs. 4.2 to 4.13. Figs. 4.2 to 4.7 show the specific normalized switch stresses $P_{ss,n}$ of the cascaded converters operating in DCM-CCM for different values of parameter K_2. Figs. 4.8 to 4.13 show the specific normalized switch stresses of the cascaded converters operating in DCM-DCM for different values of K_2. All these plots are drawn for the duty-ratios ranging from 0.1 to 0.9. Computer programs have been written to draw these plots. These computer programs can be found in Appendix C. The programs essentially used the expressions given in Tables. 4.4, 4.5 and 4.6. In the case of cascaded boost-and-boost, flyback-and-boost and flyback-and-flyback converters, the plots are drawn assuming that the duty-ratio varies from 0.1 to 0.5. Observations about the plots of specific switch stresses which can also be analytically gleaned from Table. 4.4 are as follows :

- The flyback based converters have higher stresses when compared to boost based converters irrespective of the operating modes.

Cascaded converter	$I^2_{sw,rms}$	
	DCM-DCM	DCM-CCM
Boost-&-buck, BIBRED	$\frac{D^3T^2(L_1(V_{C_1}-V_o)+L_2E)^2}{3L_1^2L_2^2}$	$\frac{D^3T^2(L_1(V_{C_1}-V_o)+L_2E)^2}{3L_1^2L_2^2} + \frac{D(2I_oL_2-DTV_{C_1}+D^2TV_{C_1})^2)^2}{4L_2^2}$ $+\frac{D^2T(2I_oL_2-DTV_{C_1}+D^2TV_{C_1})(L_1(V_{C_1}-V_o)+L_2E)}{2L_1L_2^2}$
Flyback-&-Buck	same as boost-&-buck	same as boost-&-buck
Boost-&-flyback, BIFRED	$\frac{D^3T^2(L_1V_{C_1}+L_2E)^2}{3L_1^2L_2^2}$	$\frac{D^3T^2(L_1V_{C_1}+L_2E)^2}{3L_1^2L_2^2} + \frac{D(2I_{L2}L_2-DTV_{C_1})^2}{4L_2^2}$ $+\frac{D^2T(2I_{L2}L_2-DTV_{C_1})(L_1V_{C_1}+L_2E)}{2L_1L_2^2}$
Boost-&-boost	same as boost-&-flyback	same as boost-&-flyback
Flyback-&-flyback	same as boost-&-flyback	same as boost-&-flyback
Flyback-&-boost	same as boost-&-flyback	same as boost-&-flyback

Table 4.2: RMS expressions of switch current

- Figs. 4.2 to 4.7 show that the converters operating in DCM-CCM have lower normalized specific switch stress when compared to converters operating in DCM-DCM shown in Figs. 4.8 to 4.13.
- Fig. 4.3 also shows the slight increase of switch stress in cascaded boost-and-flyback converter operating in DCM-CCM when compared with cascaded boost-and-buck converters as shown in Fig. 4.2.

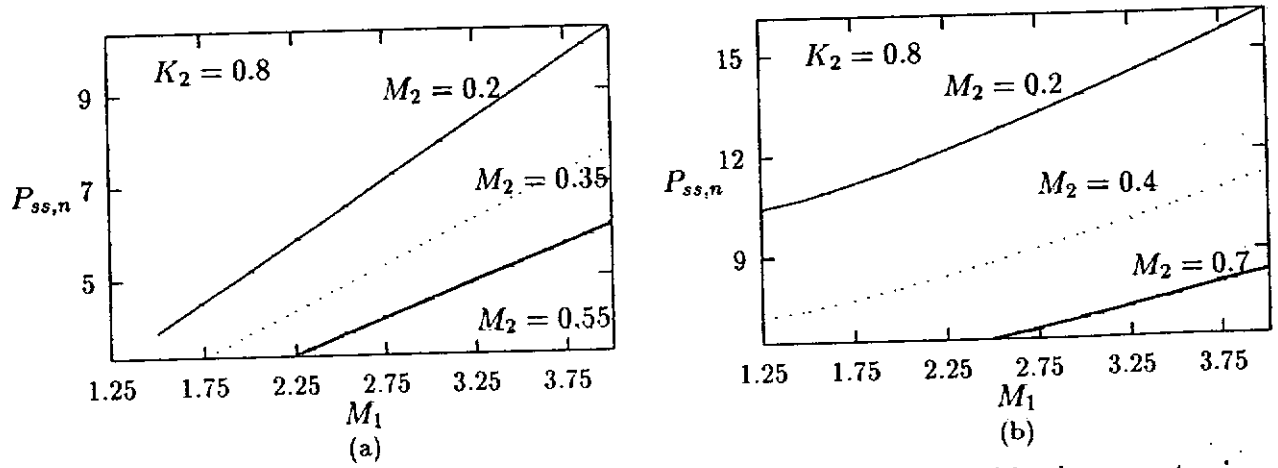

Figure 4.2: Normalized specific switch stress of cascaded (a) Boost-and-buck converter in DCM-CCM; (b) Flyback-and-buck converter in DCM-CCM

Converter	$I^2_{L,rms,n}$		$I^2_{D,rms,n}$	
	DCM	CCM	DCM	CCM
Boost input stage	$\frac{4D}{3K_1}$	-N/A-	$\frac{4D}{3K_1M_1}$	-N/A-
Boost output stage	$\frac{4D}{3K_2}$	$\frac{1}{(1-D)^2}+\frac{D^2}{3K_2^2M_2^2}$	$\frac{4D}{3K_2M_2}$	$(1-D)I^2_{L,rms,ccm,n}$
Flyback input stage	$\frac{4D}{3K_1}\left(1+\frac{1}{M_1}\right)$	-N/A-	$\frac{4D}{3K_1M_1}$	-N/A-
Flyback output stage	$\frac{4D}{3K_2}\left(1+\frac{1}{M_2}\right)$	$\frac{1}{(1-D)^2}+\frac{(1-D)^2}{3K_2^2}$	$\frac{4D}{3K_2M_2}$	$(1-D)I^2_{L,rms,ccm,n}$
Buck output stage	$\frac{4D}{3K_2}\left(1+\frac{1}{M_2}\right)$	$1+\frac{(1-D)^2}{3K_2^2}$	$\frac{4D}{3K_2M_2}\left(\frac{1}{1-M_2}\right)$	$(1-D)I^2_{L,rms,ccm,n}$
BIFRED $I^2_{D_2,rms,ccm}$	$\int_{DT}^{(D+D_2)T}\left(\frac{EDT}{L_1}+\frac{(V_{C_1}+V_o-E)(t-DT)}{L_1}+I_{L_2}+\frac{V_{C_1}DT}{2L_2}-\frac{V_o(t-DT)}{L_2}\right)^2 dt+$ $\int_{(D+D_2)T}^{T}\left(I_{L_2}+\frac{V_{C_1}DT}{2L_2}-\frac{V_oD_2T}{2L_2}-\frac{V_o(t-(D+D_2)T)}{L_2}\right)^2 dt$			
BIFRED $I^2_{D_2,rms,dcm}$	$\int_{DT}^{(D+D_2)T}\left(\frac{EDT}{L_1}+\frac{(V_{C_1}+V_o-E)(t-DT)}{L_1}+\frac{V_{C_1}DT}{L_2}-\frac{V_o(t-DT)}{L_2}\right)^2 dt+$ $\int_{(D+D_2)T}^{T}\left(\frac{V_{C_1}DT}{L_2}-\frac{V_oD_2T}{L_2}-\frac{V_o(t-(D+D_2)T)}{L_2}\right)^2 dt$			

Table 4.3: Normalized RMS expressions of inductor and diode currents

Cascaded converter	Specific Switch Stress $= P_{ss,n} = I_{rms}V_{sw,off}/P_O$	
	DCM-DCM	DCM-CCM
Boost-&-buck, BIBRED	$\sqrt{\frac{D}{3}}\left[\frac{2D}{M_2^2}\left(\frac{1}{K_1M_1}+\frac{1}{K_2}-\frac{M_2}{K_2}\right)\right]$	$\frac{1}{M_2}\sqrt{D+\frac{D(1-2D)}{3K_2^2}+\frac{D}{3}\left(\frac{2}{K_1M_1}+\frac{D}{K_2}\right)^2+\frac{2D}{K_1M_1}\left(1+\frac{1-3D}{3K_2}\right)}$
Boost-&-flyback	$\sqrt{\frac{D}{3}}\left[\frac{2D}{M_2^2}\left(\frac{1}{K_1M_1}+\frac{1}{K_2}\right)\right]$ BIFRED: $M_2 = V_O/(V_O+V_{C_1})$	$\frac{1}{M_2}\sqrt{\frac{D}{(1-D)^2}+\frac{D^3}{3M_2^2}\left(\frac{1}{K_2}+\frac{1}{K_1M_1}\right)^2+\frac{D^2}{M_1M_2K_1}\left(1+\frac{D}{K_1M_1M_2}\right)}$ BIFRED: $M_2 = V_O/(V_O+V_{C_1})$
Boost-&-boost	$P_{ss,n}$ of boost-&-flyback	$P_{ss,n}$ of boost-&-flyback
Flyback-&-buck	$\left(1+\frac{1}{M_1}\right)$ ($P_{ss,n}$ of boost-&-buck)	$\left(1+\frac{1}{M_1}\right)$ ($P_{ss,n}$ of boost-&-buck)
Flyback-&-flyback	$\left(1+\frac{1}{M_1}\right)$ ($P_{ss,n}$ of boost-&-flyback)	$\left(1+\frac{1}{M_1}\right)$ ($P_{ss,n}$ of boost-&-flyback)
Flyback-&-boost	$\left(1+\frac{1}{M_1}\right)$ ($P_{ss,n}$ of boost-&-flyback)	$\left(1+\frac{1}{M_1}\right)$ ($P_{ss,n}$ of boost-&-flyback)

Table 4.4: Normalized specific switch stress

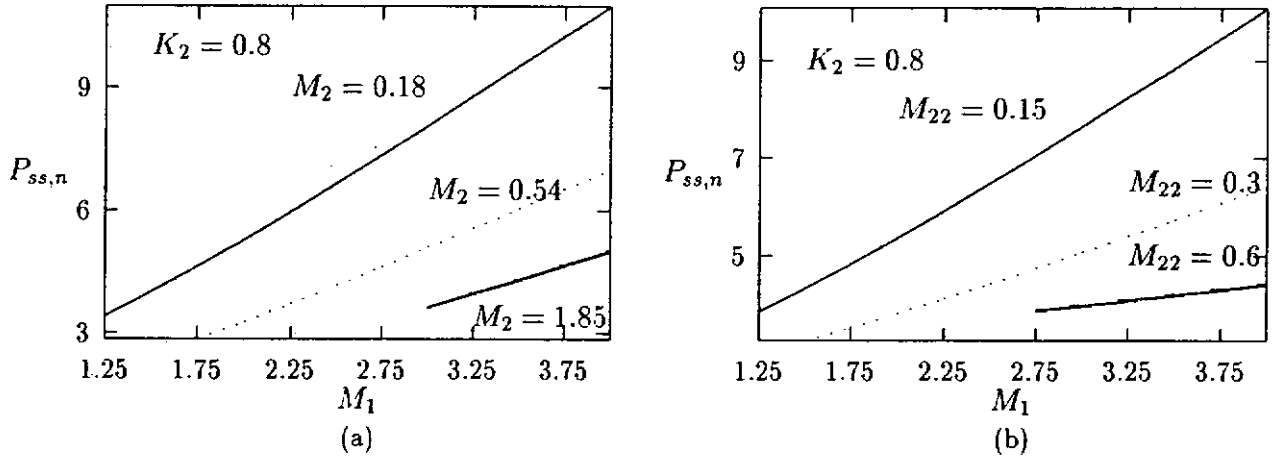

Figure 4.3: Normalized specific switch stress of cascaded (a) Boost-and-flyback converter in DCM-CCM; (b) BIFRED in DCM-CCM

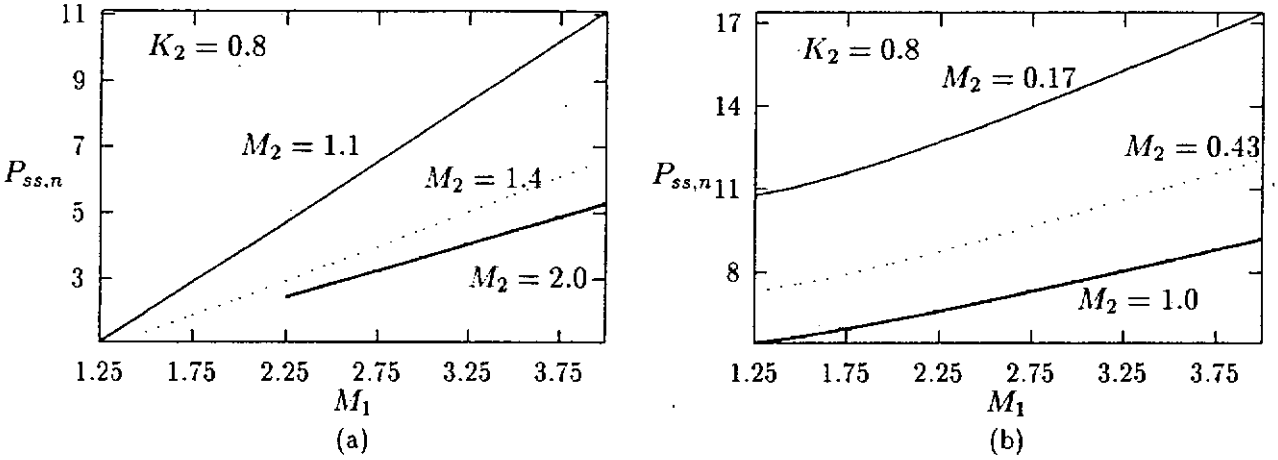

Figure 4.4: Normalized specific switch stress of cascaded (a) Boost-and-boost in DCM-CCM; (b) Flyback-and-flyback converter in DCM-CCM

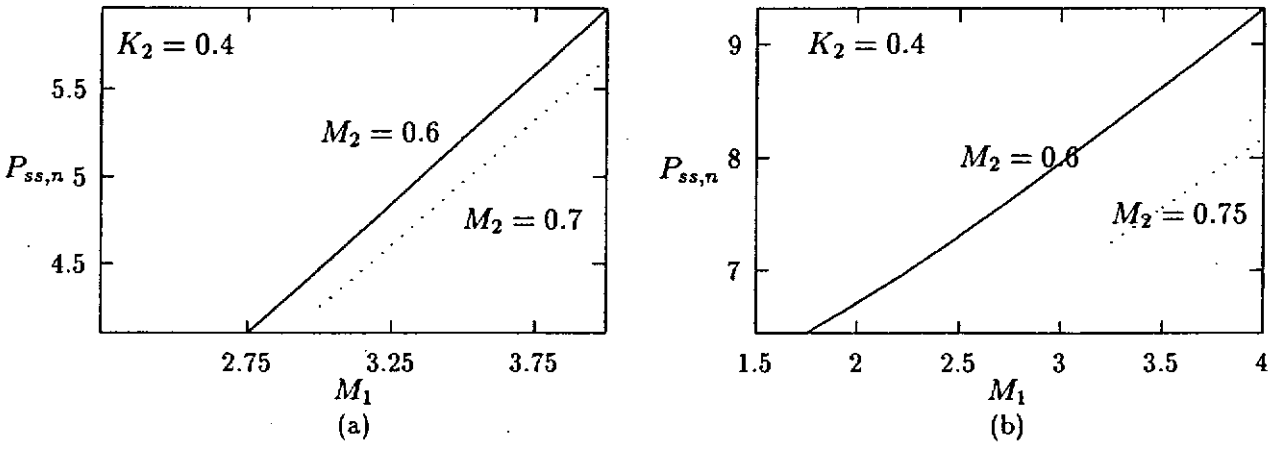

Figure 4.5: Normalized specific switch stress of cascaded (a) Boost-and-buck converter in DCM-CCM; (b) Flyback-and-buck converter in DCM-CCM

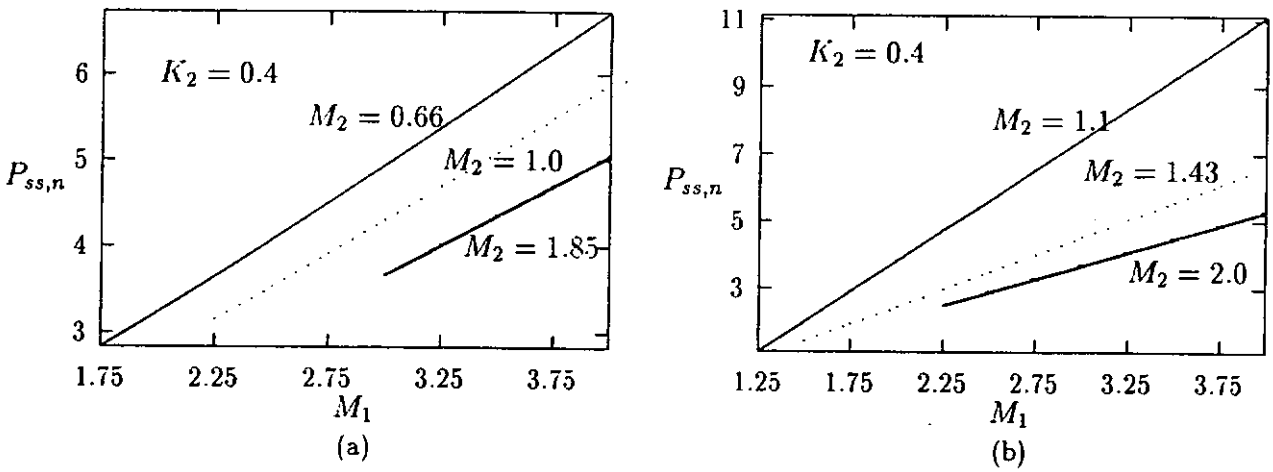

Figure 4.6: Normalized specific switch stress of cascaded (a) Boost-and-flyback converter in DCM-CCM; (b) Boost-and-boost converter in DCM-CCM

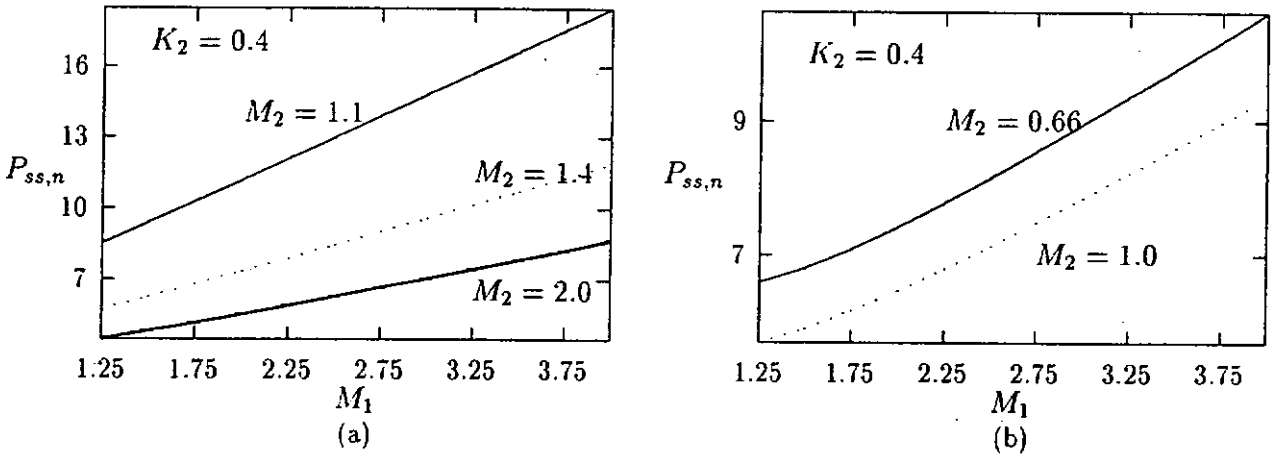

Figure 4.7: Normalized specific switch stress of cascaded (a) Flyback-and-boost in DCM-CCM; (b) Flyback-and-flyback converter in DCM-CCM

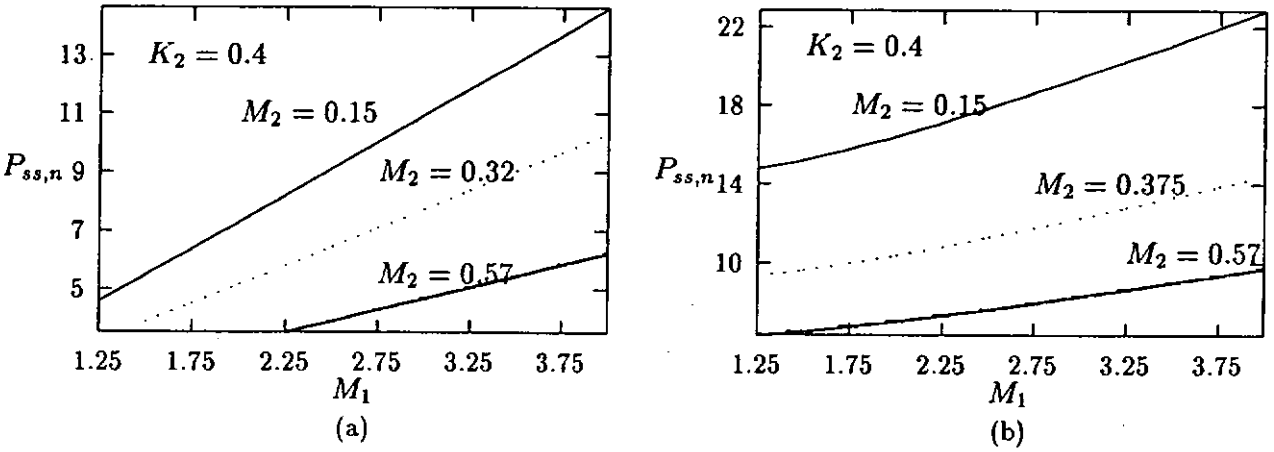

Figure 4.8: Normalized specific switch stress of cascaded (a) Boost-and-buck converter in DCM-DCM ; (b) Flyback-and-buck converter in DCM-DCM

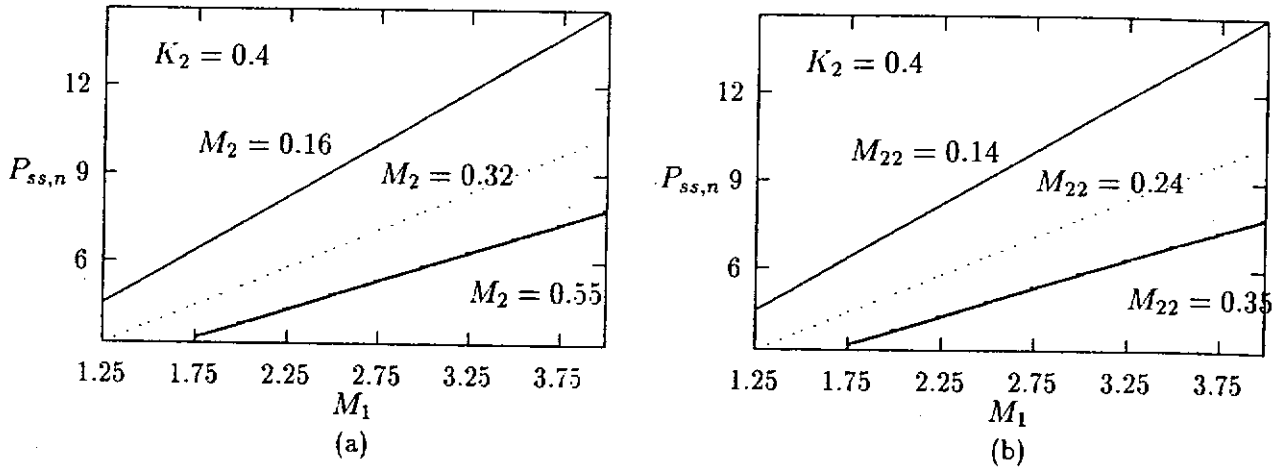

Figure 4.9: Normalized specific switch stress of cascaded (a) Boost-and-flyback converter in DCM-DCM ; (b) BIFRED in DCM-DCM

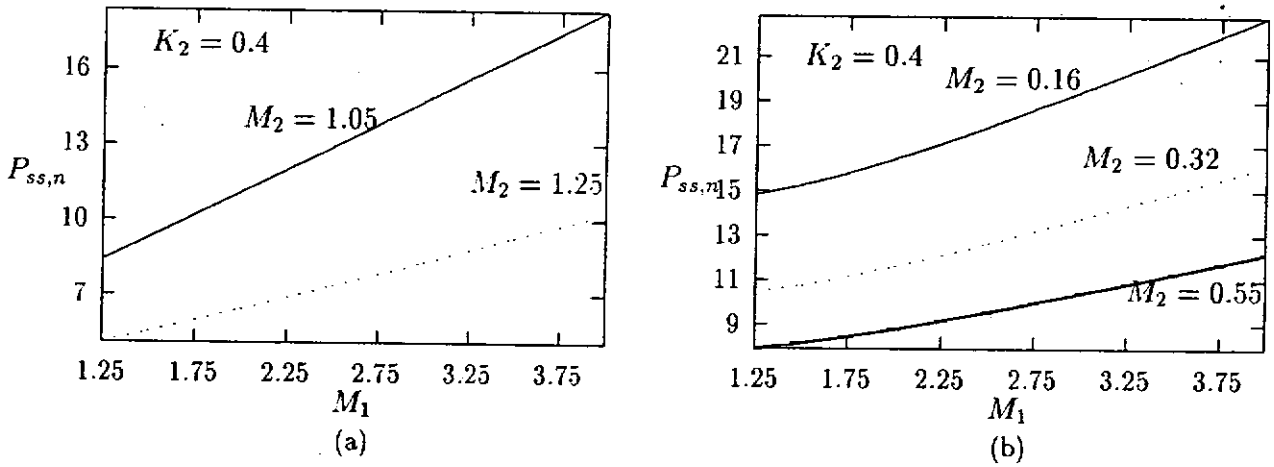

Figure 4.10: Normalized specific switch stress of cascaded (a) Flyback-and-boost in DCM-DCM ; (b) Flyback-and-flyback converter in DCM-DCM

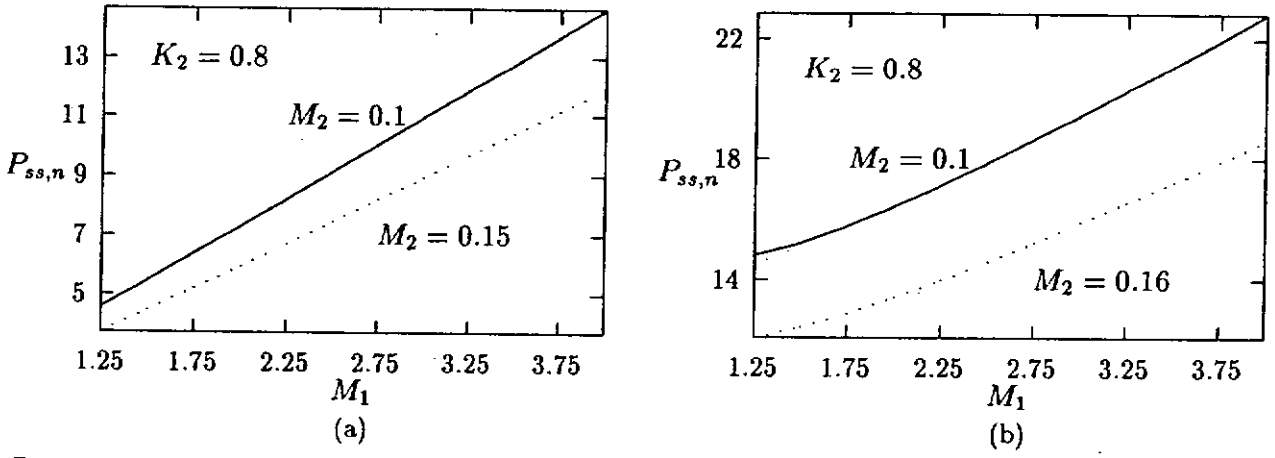

Figure 4.11: Normalized specific switch stress of cascaded (a) Boost-and-buck converter in DCM-DCM ; (b) Flyback-and-buck converter in DCM-DCM

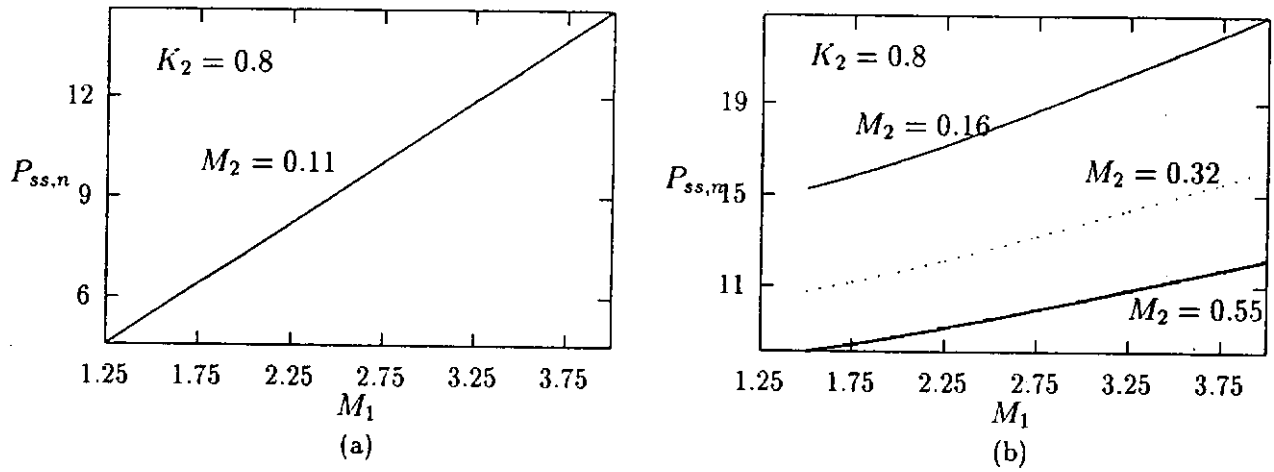

Figure 4.12: Normalized specific switch stress of cascaded (a) Boost-and-flyback converter in DCM-DCM ; (b) Flyback-and-flyback converter in DCM-DCM

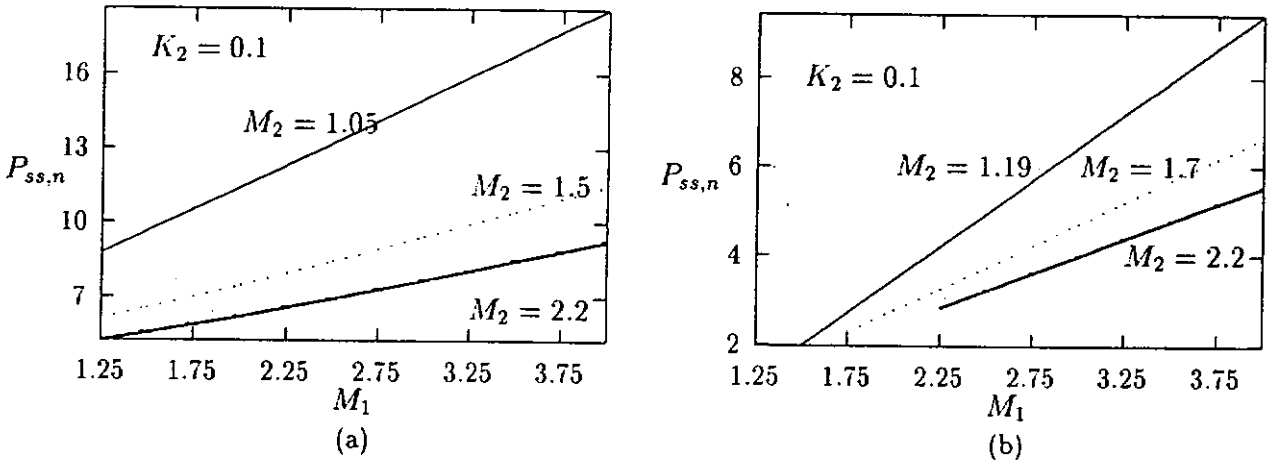

Figure 4.13: Normalized specific switch stress of cascaded (a) Flyback-and-boost in DCM-DCM ; (b) Boost-and-boost converter in DCM-DCM

4.2 Calculation of DC Voltage Conversion Ratios and Operating Mode Boundaries

4.2.1 Calculation of DC Voltage Conversion Ratio

Voltage conversion ratio is an important parameter especially in the case of PFC regulators based on automatic PFC. This is because the THD of the input-current waveform is dependent on the voltage conversion ratio of input converter stage especially when boost converter is employed as the input PFC stage. Consider the boost converter operating in DCM. In general, the switching waveform of the DCM inductor current is shown in Fig. 4.14(b).

For $0 < t < DT$,

$$i_L = \frac{t}{L}E \tag{4.23}$$

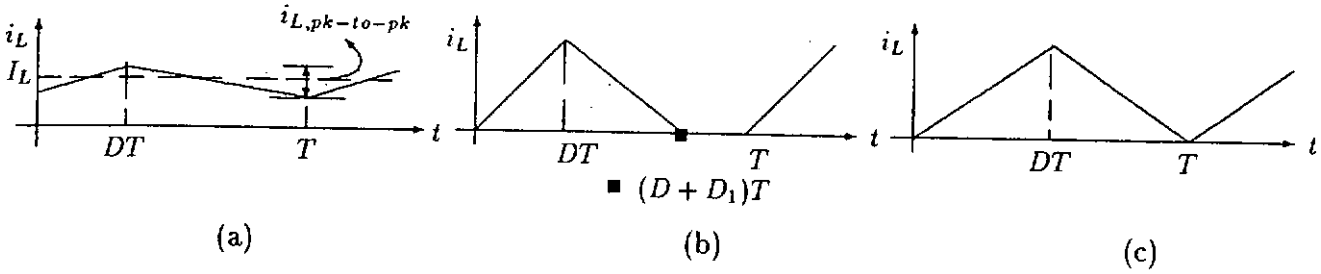

Figure 4.14: Switching waveforms of inductor operating in (a) CCM ; (b) DCM ; (c) Critical mode

For $DT < t < (D + D_1)T$,

$$i_L = \frac{DT}{L}E - \left(\frac{V_o - E}{L}\right)(t - DT) \tag{4.24}$$

where $D_1 = DE/(V_o - E)$. For $(D + D_1)T < t < T$:

$$i_L = 0 \tag{4.25}$$

From (4.23) to (4.25), the averaged value of i_L denoted as I_L is given by

$$I_L = \frac{DTE}{2L}(D + D_1) \tag{4.26}$$

By conservation of power, I_L can be expressed as

$$I_L = \frac{DTE}{2L}(D + D_1) = \frac{MV_o}{R} \tag{4.27}$$

where $M = V_o/E$ is the DC voltage conversion ratio. Putting $M = V_o/E$ in $D_1 = DE/(V_o - E)$ yields

$$D_1 = \frac{D}{(M - 1)} \tag{4.28}$$

Solving for D from (4.27) and (4.28) yields

$$D = \sqrt{M(M - 1)\frac{2L}{RT}} \tag{4.29}$$

Let $2L/RT$ be denoted by K. Note that K is a dimensionless quantity. Then solving for M from (4.29) results in

$$M = \frac{1 + \sqrt{1 + \frac{4D^2}{K}}}{2} \tag{4.30}$$

which is the steady-state voltage conversion ratio of the boost converter operating in DCM. Putting (4.30) in (4.28) and solving for D_1 yield

$$D_1 = \frac{K}{D}\left(\frac{1 + \sqrt{1 + \frac{4D^2}{K}}}{2}\right) \tag{4.31}$$

Similarly, the DC voltage conversion ratios and the discharging interval D_1 of other converters are calculated. They can also be found in Ćuk-Middlebrook [36] and Lee [41].

4.2.2 Calculation of Operating Mode Boundary

Some of the most important characteristics of DC-DC converters (small-signal transfer functions, stresses in power transistor and diode, switching losses, EMI levels, current stress in capacitor, etc.) depend on the operating mode, which is one of the important considerations in the design of PFC regulators especially in the case of converters operating as automatic PFCs. It is therefore important to know the condition for the converter to operate in a certain operating mode. From the previous section, it can be gleaned that the crucial parameter is K which is given by $2L/RT$. The converter's operating mode can be determined from Figs. 4.14(a), (b) and (c). Analytically, for CCM (from Fig. 4.14(a)), the requirement is:

$$D_1 > 1 - D \tag{4.32}$$

For DCM (from Fig. 4.14(b)), the requirement is:

$$D_1 < 1 - D \tag{4.33}$$

Thus, at the boundary between the two operating modes (from Fig. 4.14(c)):

$$D_1 = 1 - D \tag{4.34}$$

Substitution of RHS of (4.34) in LHS of (4.31) gives an expression for the critical value of K, expressed as K_{crit}. Hence, K_{crit} for the case of the boost converter is given by

$$K_{crit} = D(1 - D)^2 \tag{4.35}$$

The converter will operate in CCM, if $K > K_{crit}$. The converter will operate in DCM if $K < K_{crit}$ and in boundary mode if $K = K_{crit}$. The DC voltage conversion ratio of the boost converter operating in CCM is given by

$$M = \frac{1}{1 - D} \tag{4.36}$$

Substitution of (4.36) in (4.35) gives the expression of K_{crit} in terms of M which is given by

$$K_{crit} = \frac{M - 1}{M^3} \tag{4.37}$$

Similarly, the critical values of K of other basic converters can be calculated. They can also be found in Ćuk-Middlebrook [36].

4.2.3 Calculation of DC Voltage Conversion Ratios of a Cascaded Converter

Consider the cascaded boost-and-buck converter operating in DCM-CCM. Since the buck converter is operating in CCM, its voltage conversion ratio is $M_2 = V_o/V_{C_1} = D$. By conservation

Cascaded converter	$M_1 = V_{C_1}/E$	$M_2 = V_O/V_{C_1}$		$M = M_1 M_2 = V_O/E$	
	DCM	DCM	CCM	DCM-DCM	DCM-CCM
Boost-&-Buck, BIBRED	$\frac{1+\sqrt{1+\frac{4D^2}{K_{e1}}}}{2}$, $K_{e1} = K_1 M_2^2$	$\frac{2}{1+\sqrt{1+\frac{4K_2}{D^2}}}$	D	$\frac{1+\sqrt{1+\frac{D^2}{K_1}\left(1+\sqrt{1+\frac{4K_2}{D^2}}\right)^2}}{1+\sqrt{1+\frac{4K_2}{D^2}}}$	$D\left(\frac{1+\sqrt{1+\frac{4}{K_1}}}{2}\right)$
Boost-& -flyback	$\frac{1+\sqrt{1+\frac{4D^2}{K_{e1}}}}{2}$	$\frac{D}{\sqrt{K_2}}$	$\frac{D}{1-D}$	$\frac{D\left(1+\sqrt{1+\frac{4K_2}{K_1}}\right)}{2\sqrt{K_2}}$	$\frac{D\left(1+\sqrt{1+\frac{4(1-D)^2}{K_1}}\right)}{2(1-D)}$
BIFRED	$\frac{V_O}{E} - \frac{1+\sqrt{1+\frac{4D^2}{K_{e1}}}}{2}$, $K_{e1} = K_1\left(\frac{V_o}{V_o+V_{C_1}}\right)^2$	$\frac{D}{\sqrt{K_2}}$	$\frac{D}{1-D}$	$\frac{1+\sqrt{1+\frac{D^2}{K_1}\left(1+\sqrt{1+\frac{4K_2}{D^2}}\right)^2}}{1+\sqrt{1+\frac{4K_2}{D^2}}}$	$D\left(\frac{1+\sqrt{1+\frac{4}{K_1}}}{2}\right)$
Boost-& -boost	$\frac{1+\sqrt{1+\frac{4D^2}{K_{e1}}}}{2}$	$\frac{1+\sqrt{1+\frac{4D^2}{K_2}}}{2}$	$\frac{1}{1-D}$	$M_1\frac{1+\sqrt{1+\frac{16D^2}{K_1\left(1+\sqrt{1+\frac{4D^2}{K_2}}\right)^2}}}{2}$	$\frac{1+\sqrt{1+\frac{4D^2(1-D)^2}{K_1}}}{2}$
Flyback-&-buck	$\frac{D}{\sqrt{K_{e1}}}$	$\frac{2}{1+\sqrt{1+\frac{4K_2}{D^2}}}$	D	$\frac{D\left(1+\sqrt{1+\frac{4K_2}{D^2}}\right)}{2\sqrt{K_1}}$	$\frac{D}{\sqrt{K_1}}$
Flyback-&-flyback	$\frac{D}{\sqrt{K_{e1}}}$	$\frac{D}{\sqrt{K_2}}$	$\frac{D}{1-D}$	$\frac{D}{\sqrt{K_1}}$	$\frac{D}{\sqrt{K_1}}$
Flyback-&-boost	$\frac{D}{\sqrt{K_{e1}}}$	$\frac{1+\sqrt{1+\frac{4D^2}{K_2}}}{2}$	$\frac{1}{1-D}$	$\frac{D}{\sqrt{K_1}}$	$\frac{D}{\sqrt{K_1}}$

Table 4.5: DC voltage conversion ratios

of power, the equivalent load resistance R_e and K_{e1} of the input stage are given by

$$R_e = \frac{R}{M_2^2} \tag{4.38}$$

$$K_{e1} = K_1 M_2^2 \tag{4.39}$$

Putting K_{e1} instead of K_1 in (4.30) results in the DC voltage conversion ratio of input boost DCM stage of the cascaded boost-and-buck converter operating in DCM-CCM:

$$M_1 = \frac{1+\sqrt{1+\frac{4}{K_1}}}{2} \tag{4.40}$$

Similarly, the DC voltage conversion ratio of input boost DCM stage of the cascaded boost-and-buck converter operating in DCM-DCM can be found as

$$M_1 = \frac{1+\sqrt{1+\frac{D^2}{K_1}\left(1+\sqrt{1+\frac{4K_2}{D^2}}\right)^2}}{1+\sqrt{1+\frac{4K_2}{D^2}}} \tag{4.41}$$

Likewise, the DC voltage conversion ratios of other cascaded converters are calculated and listed in Table 4.5.

4.2.4 Calculation of Operating Mode Boundaries of a Cascaded Converter

From (4.39) and (4.35), the condition for the input boost stage of a cascaded boost-and-buck converter to operate in DCM can be written as

$$K_1 < \frac{D(1-D)^2}{M_2^2} \tag{4.42}$$

where $K_1 = 2L_1/RT$. The cascaded boost-and-buck converter can operate in DCM-CCM if the following conditions are satisfied

$$K_1 < \frac{(1-D)^2}{D} \tag{4.43}$$

and

$$K_2 > 1-D \tag{4.44}$$

where $K_2 = 2L_2/RT$. Similarly, the cascaded boost-and-buck converter can operate in DCM-DCM if the following conditions are satisfied

$$K_1 < \frac{D(1-D)^2}{4}\left(1+\sqrt{1+\frac{4K_2}{D^2}}\right)^2 \tag{4.45}$$

and

$$K_2 < 1-D \tag{4.46}$$

Likewise, the operating mode boundaries of other cascaded converters are calculated and listed in Table 4.6.

4.3 Concluding Remarks

Knowledge of RMS and average currents is essential for calculating efficiency, estimating EMI and analyzing low-frequency behaviour of switching converters. Information about peak currents can be used for selecting the semiconductor devices and for inductor design. All the feasible cascaded converters are compared against their inductor, diode and switch average,

Cascaded converter	$K_1 < K_{1,crit}$			$K_2 <_{DCM}$ or $>_{CCM} K_{crit}$	
	DCM-DCM	DCM-CCM	$K_{1,crit}(M_1, M_2)$	$K_{2,crit}(D)$	$K_{2,crit}(M_2)$
Boost-&-buck, BIBRED	$\frac{D(1-D)^2}{4}\left(1+\sqrt{1+\frac{4K_2}{D^2}}\right)^2$	$\frac{(1-D)^2}{D}$	$\frac{M_1-1}{M_1^3M_2^2}$	$1-D$	$1-M_2$
Boost-&-flyback	$\frac{K_2(1-D)^2}{D}$	$\frac{(1-D)^4}{D^2}$	$\frac{M_1-1}{M_1^3M_2^2}$	$(1-D)^2$	$\frac{1}{(M_2+1)^2}$
BIFRED	$\frac{D(1-D)^2}{4}\left(1+\sqrt{1+\frac{4K_2}{D^2}}\right)^2$	$\frac{(1-D)^2}{D}$	$\frac{M_1-1}{M_1^3M_{22}^2}$, $M_{22}=V_o/(V_{C_1}+E)$	$(1-D)^2$	$\frac{1}{(M_2+1)^2}$
Boost-&-boost	$\frac{4D(1-D)^2}{\left(1+\sqrt{1+\frac{4D^2}{K_2}}\right)^2}$	$D(1-D)^4$	$\frac{M_1-1}{M_1^3M_2^2}$	$D(1-D)^2$	$\frac{M_2-1}{M_2^3}$
Flyback-&-buck	$\frac{(1-D)^2}{4}\left(1+\sqrt{1+\frac{4K_2}{D^2}}\right)^2$	$\frac{(1-D)^2}{D^2}$	$\frac{1}{M_2^2(M_1+1)^2}$	$1-D$	$1-M_2$
Flyback-&-flyback	$\frac{K_2(1-D)^2}{D^2}$	$\frac{(1-D)^4}{D^2}$	$\frac{1}{M_2^2(M_1+1)^2}$	$(1-D)^2$	$\frac{1}{(M_2+1)^2}$
Flyback-&-boost	$\frac{4(1-D)^2}{\left(1+\sqrt{1+\frac{4D^2}{K_2}}\right)^2}$	$(1-D)^4$	$\frac{1}{M_2^2(M_1+1)^2}$	$D(1-D)^2$	$\frac{M_2-1}{M_2^3}$

Table 4.6: Operating mode boundary determination between DCM and CCM

RMS and peak currents. Normalized specific switch stresses are plotted for all the feasible converters operating in DCM-CCM and DCM-DCM. It is found that the specific switch stresses of boost based converters are lesser than flyback based converters. Cascaded boost-and-buck converters are found to have lower specific switch stress when compared to cascaded boost-and-flyback converters. Steady-state voltage conversion ratios and operating mode boundaries are also given. The details concerning the efficiencies of some of these single-stage converters can be found in Redl [2, 3]. In the next two chapters, small-signal dynamical analyses of cascaded boost-and-buck converter, BIFRED and cascaded boost-and-flyback converters are dealt with in detail.

Chapter 5

Dynamical Analysis of Single-Stage Cascaded Boost-and-Buck PFC Converters

In the previous chapter all the feasible single-stage topologies were compared in terms of their switching stresses. RMS, peak and average currents in inductors, capacitors and diodes. The mode boundaries and steady-state voltage conversion ratios were tabulated. In this chapter the small-signal dynamical analysis of single-stage PFC converters based on cascade combination of a DCM boost converter and a buck converter will be rigorously analyzed. This chapter gives a detailed analysis of the dynamical response of this type of converters, e.g., Boost Integrated with Buck Rectifier Energy storage DC-DC converter (BIBRED) [1], Single-Stage Isolated PFC Power Supply (SSIPP) [2] and *decoupled* Ćuk converter [4], and explains how the relative sizes of the storage and output capacitors affect the dynamics. The term *decoupled* implies that voltages e, v_{C_1} and v_o are independent. Complete sets of small-signal transfer functions are derived for all common operating modes. Conditions for order reduction will also be derived which is important for achieving fast response. Throughout the chapter, uppercase letters are used for steady-state values, and letters with *tilde* ($\tilde{}$) for small-signal variables. For simplicity, the single-stage cascaded boost-and-buck converter will be referred to as cascaded boost-and-buck converter or simply as boost-and-buck converter. In particular, the duty-ratio-to-output voltage transfer function $\tilde{v}_o/\tilde{d}$, output impedance Z_o, line-to-output voltage transfer function $\tilde{v}_o/\tilde{e}$, and input impedance Z_i will be derived and analyzed. Since the line-frequency is assumed

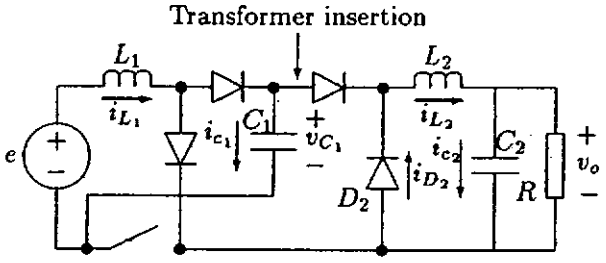

Figure 5.1: Cascaded boost-and-buck converter

to be a very small fraction of switching frequency, the input voltage is assumed to be constant within a switching period. Hence the same analysis of the DC-DC converter is used here.

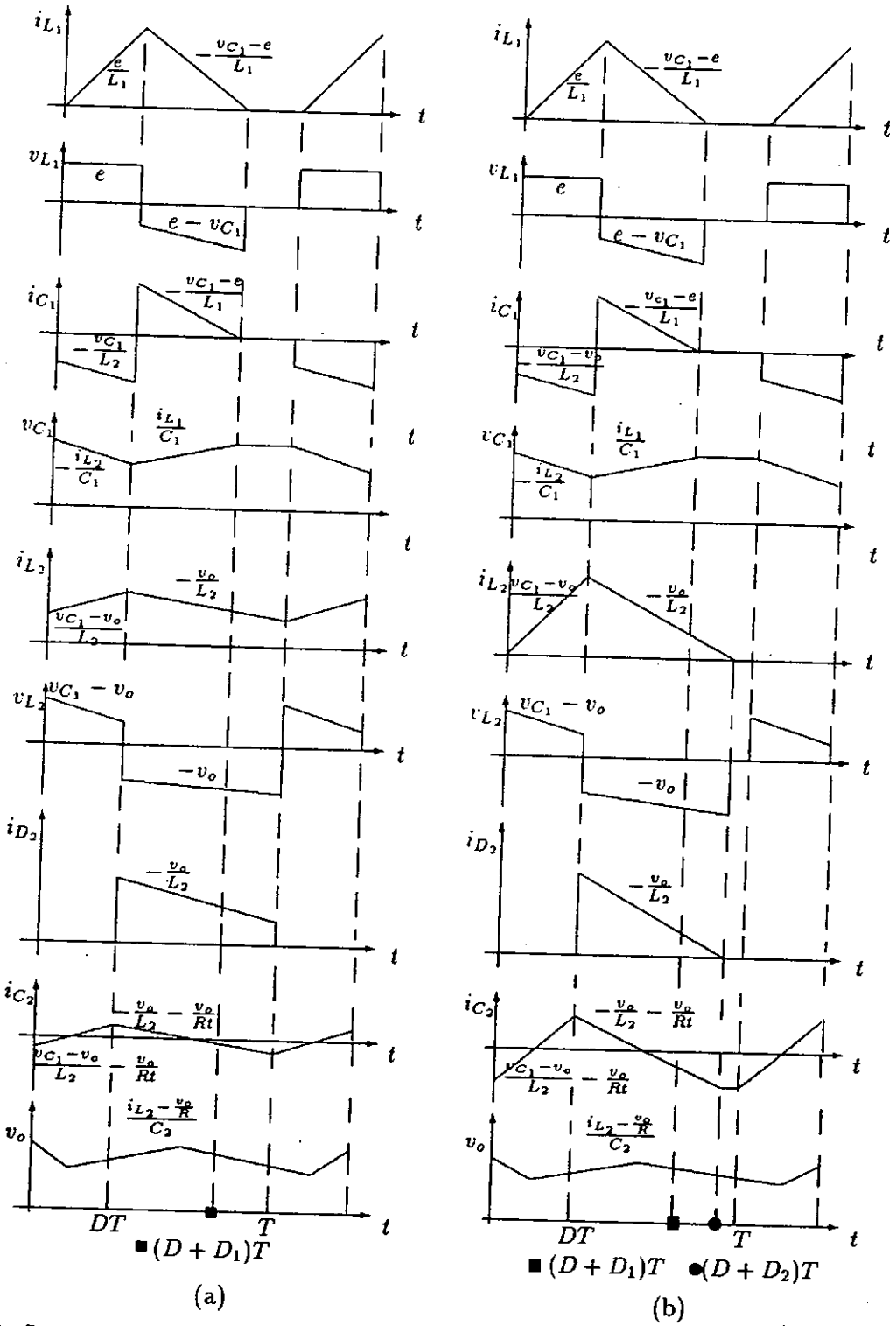

Figure 5.2: Switching waveforms of boost-and-buck converter (a) DCM-CCM ; (b) DCM-DCM
(All the entries on the waveforms represent slopes except the inductor voltage waveforms.)

5.1 Dynamical Analysis of Boost-and-buck Converter in DCM-CCM

The basic equivalent form is shown in Fig. 5.1. Usually for PFC applications, the boost part operates in DCM while the buck part can operate in either DCM or CCM. In this section, the boost-and-buck converter operating in DCM-CCM is considered.

5.1.1 Derivation of Small-signal Transfer Functions

The switching waveforms of cascaded boost-and-buck converter operating in DCM-CCM is shown in Fig. 5.2(a). By averaging the inductor and capacitor current and voltage waveforms over a switching cycle [35], the following equations are derived:

$$i_{L_1} = \frac{d^2 T e}{2L_1(1 - e/v_{C_1})} \tag{5.1}$$

$$C_1 \frac{dv_{C_1}}{dt} = i_{C_1} = \frac{d^2 T e}{2L_1(v_{C_1}/e - 1)} - di_{L_2} \tag{5.2}$$

$$L_2 \frac{di_{L_2}}{dt} = v_{L_2} = dv_{C_1} - v_o \tag{5.3}$$

$$C_2 \frac{dv_o}{dt} = i_{C_2} = i_{L_2} - \frac{v_o}{R} \tag{5.4}$$

which provide an analytical basis to derive the averaged model shown in Fig. 5.3. The

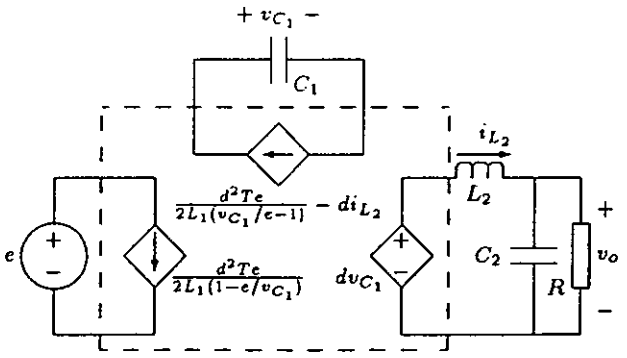

Figure 5.3: Averaged model for DCM-CCM operation

small-signal parameters are found as

$$\begin{array}{lll} G_{11} = \frac{\partial i_{L_1}}{\partial e} & G_{12} = \frac{\partial i_{L_1}}{\partial v_{C_1}} & K_{13} = \frac{\partial i_{L_1}}{\partial i_{L_2}} \\ G_{21} = \frac{\partial i_{C_2}}{\partial e} & G_{22} = \frac{\partial i_{C_2}}{\partial v_{C_1}} & K_{23} = \frac{\partial i_{C_2}}{\partial e} \\ K_{31} = \frac{\partial v_3}{\partial e} & K_{32} = \frac{\partial v_3}{\partial v_{C_1}} & Z_{33} = \frac{\partial v_3}{\partial i_{L_2}} \\ J_1 = \frac{\partial i_{L_1}}{\partial d} & J_2 = \frac{\partial i_{C_2}}{\partial d} & J_3 = \frac{\partial i_{L_2}}{\partial d} \\ G_{23} = \frac{\partial i_{C_2}}{\partial v_o} & G_{32} = \frac{\partial i_{L_2}}{\partial v_{C_1}} & U_3 = \frac{\partial v_3}{\partial d} \end{array} \tag{5.5}$$

where $v_3 = v_{L_2} + v_o$, and i_{L_1}, i_{C_1}, i_{L_2} and i_{C_2} are given in (5.1) to (5.4). Using the standard

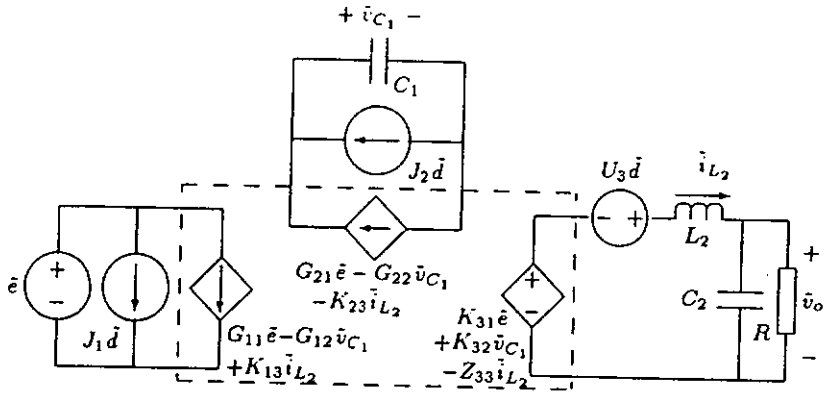

Figure 5.4: Small-signal model for DCM-CCM operation

procedure of small-signal linearization [35]-[37], [37] the small-signal model shown in Fig. 5.4 is derived. For brevity and convenience, the following new quantities have been introduced :

$$M_1 = V_{C_1}/E,\ M_2 = V_o/V_{C_1},\ K_1 = 2L_1/RT,\ K_2 = 2L_2/RT,\ R_e = R/M_2^2,\ K_e = K_1 M_2^2$$

The small-signal parameters given in (5.5) are derived and tabulated in Table 5.1 which can be used to derive all transfer functions of interest.

5.1.1.A *Duty-ratio-to-output Voltage Transfer Function*

In deriving the $\tilde{v}_o/\tilde{d}$ transfer function, the input $\tilde{e}$ is set to zero. The circuit model thus reduces to the one shown in Fig. 5.5. Application of nodal analysis to this circuit yields

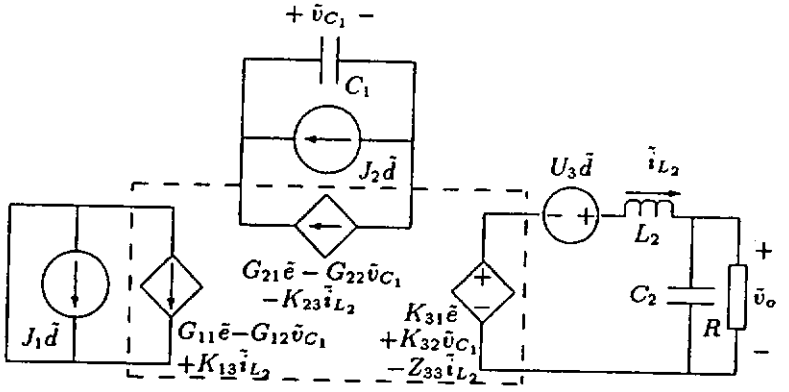

Figure 5.5: Model for calculation of $\tilde{v}_o/\tilde{d}$

$$\begin{bmatrix} G_{22}+sC_1 & K_{23} \\ -K_{32} & sL_2 + \frac{R}{1+sRC_2} \end{bmatrix} \begin{bmatrix} \tilde{v}_{C_1} \\ \tilde{i}_{L_2} \end{bmatrix} = \begin{bmatrix} J_2\tilde{d} \\ U_3\tilde{d} \end{bmatrix} \tag{5.6}$$

Solving (5.6) for i_{L_2} results in

$$\frac{\tilde{i}_{L_2}}{\tilde{d}} = \frac{V_{C_1}(1+sRC_2)\left[sC_1 + G_{22} + \frac{K_{32}J_2}{U_3}\right]}{R\left[(s^2L_2C_2 + \frac{sL_2}{R} + 1)(sC_1 + G_{22}) + (sC_2 + \frac{1}{R})K_{32}K_{23}\right]} \tag{5.7}$$

Para-meters	DCM-CCM		DCM-DCM	
	$f(E, V_{C_1}, I_{L_2})$	$f(M, K, R)$	$f(E, V_{C_1}, V_o)$	$f(M, K, R)$
G_{11}	$\frac{D^2T}{2L_1}\frac{1}{(V_{C_1}/E-1)^2}$	$\left(\frac{M_1^3}{M_1-1}\right)\frac{1}{R_e}$	$\frac{D^2T}{2L_1}\frac{1}{(V_{C_1}/E-1)^2}$	$\left(\frac{M_1^3}{M_1-1}\right)\frac{1}{R_e}$
G_{12}	$\frac{D^2T}{2L_1}\frac{1}{(V_{C_1}/E-1)^2}$	$\left(\frac{M_1}{M_1-1}\right)\frac{1}{R_e}$	$\frac{D^2T}{2L_1}\frac{1}{(V_{C_1}/E-1)^2}$	$\left(\frac{M_1}{M_1-1}\right)\frac{1}{R_e}$
G_{13}	-N/A-	-N/A-	0	0
K_{13}	0	0	-N/A-	-N/A-
J_1	$\frac{DTE}{L_1(1-E/V_{C_1})}$	$\frac{2V_{C_1}}{R_e}\sqrt{\frac{M_1}{K_e(M_1-1)}}$	$\frac{DTE}{L_1(1-E/V_{C_1})}$	$\frac{2V_{C_1}}{R_e}\sqrt{\frac{M_1}{K_e(M_1-1)}}$
G_{21}	$\frac{D^2T}{2L_1}\frac{(2V_{C_1}/E-1)}{(V_{C_1}/E-1)^2}$	$\frac{M_1(2M_1-1)}{(M_1-1)R_e}$	$\frac{D^2T}{2L_1}\frac{(2V_{C_1}/E-1)}{(V_{C_1}/E-1)^2}$	$\frac{M_1(2M_1-1)}{(M_1-1)R_e}$
G_{22}	$\frac{D^2T}{2L_1}\frac{1}{(V_{C_1}/E-1)^2}$	$\left(\frac{M_1}{M_1-1}\right)\frac{1}{R_e}$	$\frac{D^2T}{2L_1}\frac{1}{(V_{C_1}/E-1)^2}+\frac{D^2T}{2L_2}$	$\frac{1}{R_e}\left(\left(\frac{M_1}{M_1-1}\right)+\frac{1}{(1-M_2)}\right)$
G_{23}	-N/A-	-N/A-	$\frac{D^2T}{2L_2}$	$\left(\frac{1}{1-M_2}\right)\frac{1}{R_e}$
K_{23}	D	M_2	-N/A-	-N/A-
J_2	$\frac{DTE}{L_1(V_{C_1}/E-1)}-I_{L_2}$	$\frac{2V_{C_1}/R_e}{\sqrt{K_eM_1(M_1-1)}}-\frac{V_o}{R}$	$\frac{DTE}{L_1(V_{C_1}/E-1)}-\frac{D^2T(V_{C_1}-V_o)}{L_2}$	$\frac{2V_{C_1}/R_e}{\sqrt{K_eM_1(M_1-1)}}-\frac{2V_o}{R}\sqrt{\frac{1-M_2}{K^2}}$
G_{31}	-N/A-	-N/A-	0	0
G_{32}	-N/A-	-N/A-	$\frac{D^2T}{2L_2}\left(\frac{2V_{C_1}}{V_o}-1\right)$	$\frac{M_2}{R}\left(\frac{2-M_2}{1-M_2}\right)$
G_{33}	-N/A-	-N/A-	$\frac{D^2T}{2L_2}\left(\frac{V_{C_1}}{V_o}\right)^2$	$\frac{1}{R(1-M_2)}$
K_{31}	0	0	-N/A-	-N/A-
K_{32}	D	M_2	-N/A-	-N/A-
Z_{33}	0	0	-N/A-	-N/A-
U_3	V_{C_1}	V_{C_1}	-N/A-	-N/A-
J_3	-N/A-	-N/A-	$\frac{DTV_{C_1}}{L_1}\left(\frac{V_{C_1}}{V_o}-1\right)$	$\frac{2V_o}{RM_2}\sqrt{\frac{1-M_2}{K_2}}$

Table 5.1: Small-signal parameters

Substituting $\tilde{i}_{L_2}=\tilde{v}_o((1+sRC_2)/R)$ in RHS of (5.7) results in

$$\frac{\tilde{v}_o}{\tilde{d}}=\frac{V_{C_1}\left[sC_1+G_{22}+\frac{K_{32}J_2}{U_3}\right]}{\left[(s^2L_2C_2+\frac{sL_2}{R}+1)(sC_1+G_{22})+(sC_2+\frac{1}{R})K_{32}K_{23}\right]} \tag{5.8}$$

5.1.1.B *Output Impedance Transfer Function*

In deriving the output impedance, the inputs $\tilde{e}$ and $\tilde{d}$ are set to zero. A test current source $\tilde{i}_s$ is injected to the output terminal as shown in Fig. 5.6 [38]. Application of nodal analysis to the circuit shown in Fig. 5.6 yields

$$\begin{bmatrix} 0 & G_{22}+sC_1 & K_{23} \\ \frac{1+sRC_2}{R} & 0 & -1 \\ -1 & K_{32} & -sL_2 \end{bmatrix}\begin{bmatrix} \tilde{v}_o \\ \tilde{v}_{C_1} \\ \tilde{i}_{L_2} \end{bmatrix}=\begin{bmatrix} 0 \\ \tilde{i}_s \\ 0 \end{bmatrix} \tag{5.9}$$

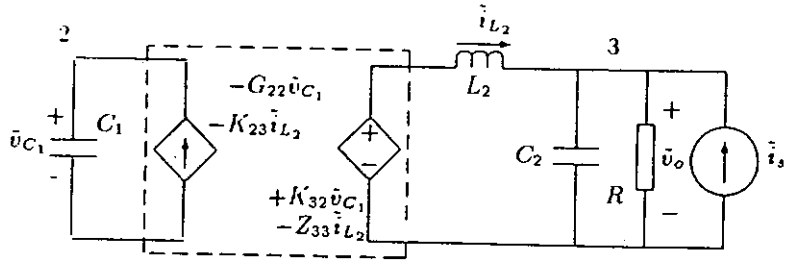

Figure 5.6: Model for calculation of Z_o

Solving (5.9) for $\tilde{v}_o$ gives

$$Z_o = \frac{\tilde{v}_o}{\tilde{i}_s} = \frac{s^2 L_2 C_1 + sL_2 G_{22} + K_{23}K_{32}}{\left(sC_2 + \frac{1}{R}\right)(s^2 L_2 C_1 + sL_2 G_{22} + K_{23}K_{32}) + sC_1 + G_{22}} \tag{5.10}$$

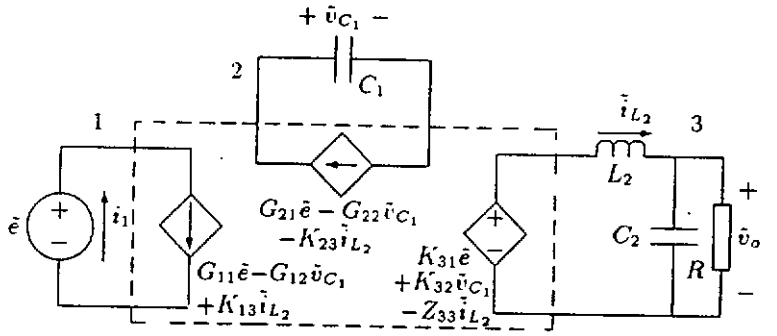

Figure 5.7: Model for calculation of $\tilde{v}_o/\tilde{e}$ and Z_i

5.1.1.C Line-to-output Voltage Transfer Function

In deriving the line-to-output voltage transfer function, the duty-ratio $\tilde{d}$ is set to zero. Thus, the circuit model reduces to the one shown in Fig. 5.7. Application of nodal analysis to this circuit yields

$$\begin{bmatrix} G_{22} + sC_1 & K_{23} \\ -K_{32} & sL_2 + \frac{R}{1+sRC_2} \end{bmatrix} \begin{bmatrix} \tilde{v}_{C_1} \\ \tilde{i}_{L_2} \end{bmatrix} = \begin{bmatrix} G_{21}\tilde{e} \\ 0 \end{bmatrix} \tag{5.11}$$

Solving (5.11) for i_{L_2} results in

$$\frac{\tilde{i}_{L_2}}{\tilde{d}} = \frac{(1 + sRC_2)V_{C_1}\left[sC_1 + G_{22} + \frac{K_{32}J_2}{U_3}\right]}{R\left[(s^2 L_2 C_2 + \frac{sL_2}{R} + 1)(sC_1 + G_{22}) + (sC_2 + \frac{1}{R})K_{32}K_{23}\right]} \tag{5.12}$$

Substituting $\tilde{i}_{L_2} = \tilde{v}_o((1 + sRC_2)/R)$ in LHS of (5.12) yields

$$\frac{\tilde{v}_o}{\tilde{e}} = \frac{G_{21}K_{32}}{\left[(s^2 L_2 C_2 + \frac{sL_2}{R} + 1)(sC_1 + G_{22}) + (sC_2 + \frac{1}{R})K_{32}K_{23}\right]} \tag{5.13}$$

5.1.1.D *Input Impedance Transfer Function*

The same model shown in Fig. 5.7 is used again for the derivation of input impedance. The nodal equation is given by

$$\begin{bmatrix} 1 & G_{12} & 0 \\ 0 & G_{22}+sC_1 & K_{23} \\ 0 & -K_{32} & sL_2+\frac{R}{1+sRC_2} \end{bmatrix} \begin{bmatrix} \tilde{i}_1 \\ \tilde{v}_{C_1} \\ \tilde{i}_{L_2} \end{bmatrix} = \begin{bmatrix} G_{11}\tilde{e} \\ 0 \\ 0 \end{bmatrix} \tag{5.14}$$

Solving (5.14) for $\tilde{i}_1$ results in

$$Z_i = \frac{\tilde{e}}{\tilde{i}_1} = \frac{(s^2L_2C_2R+sL_2+R)(sC_1+G_{22})+D^2(sRC_2+1)}{[(s^2L_2C_2R+sL_2+R)(sC_1+G_{22})+(sC_2+\frac{1}{R})K_{32}K_{23}]-G_{12}G_{21}(s^2L_2C_2R+sL_2+R)} \tag{5.15}$$

All the transfer functions are further simplified in order to represent them in the conventional form and they are listed in Table 5.2. The transfer functions can also be derived by using the Extra Element Theorem (EET) [40]. To facilitate inspection, poles and zeros for $\tilde{v}_o/\tilde{d}$ and Z_o, are listed in Table 5.3.

Transfer function	Converter operating in DCM-CCM	Converter operating in DCM-DCM
$\frac{\tilde{v}_o}{\tilde{d}}$	$\frac{\frac{G_{22}V_{C_1}+K_{32}J_2}{G_{22}}\left(1+\frac{sC_1V_{C_1}}{G_{22}V_{C_1}+K_{32}J_2}\right)}{\left(1+\frac{sL_2}{R}+s^2L_2C_2\right)\left(1+\frac{sC_1}{G_{22}}\right)+\frac{K_{32}K_{23}}{RG_{22}}(1+sC_2R)}$	$\frac{RJ_3\left(\frac{1-M_2}{2-M_2}\right)\left[1+\frac{sC_1}{G_{22}}+\frac{J_2G_{32}}{J_3G_{22}}\right]}{\left[\left(1+sC_2R\left(\frac{1-M_2}{2-M_2}\right)\right)\left(1+\frac{sC_1}{G_{22}}\right)-\left(\frac{M_2^3}{1-M_2}\right)\frac{1}{RG_{22}}\right]}$
Z_o	$\frac{R\left(1+\frac{sL_2G_{22}}{K_{23}K_{32}}+\frac{s^2L_2C_1}{K_{23}K_{32}}\right)}{(1+sC_2R)\left(1+\frac{sL_2G_{22}}{K_{23}K_{32}}+\frac{s^2L_2C_1}{K_{23}K_{32}}\right)+\frac{G_{22}R}{K_{23}K_{32}}\left(1+\frac{sC_1}{G_{22}}\right)}$	$\frac{R\left(\frac{1-M_2}{2-M_2}\right)\left[1+\frac{sC_1}{G_{22}}\right]}{\left[\left(1+sC_2R\left(\frac{1-M_2}{2-M_2}\right)\right)\left(1+\frac{sC_1}{G_{22}}\right)-\left(\frac{M_2^3}{1-M_2}\right)\frac{1}{RG_{22}}\right]}$
$\frac{\tilde{v}_o}{\tilde{e}}$	$\frac{\frac{G_{21}K_{32}}{G_{22}}}{\left(1+\frac{sC_1}{G_{22}}\right)\left(1+\frac{sL_2}{R}+s^2L_2C_2\right)+\frac{K_{23}K_{32}}{RG_{22}}(1+sC_2R)}$	$\frac{\frac{G_{32}G_{21}}{G_{22}}\left(\frac{1-M_2}{2-M_2}\right)R}{\left[\left(1+sC_2R\left(\frac{1-M_2}{2-M_2}\right)\right)\left(1+\frac{sC_1}{G_{22}}\right)-\left(\frac{M_2^3}{1-M_2}\right)\frac{1}{RG_{22}}\right]}$
Z_i DCM-CCM	$\frac{1}{G_{11}-\frac{1}{\frac{G_{22}}{G_{12}G_{21}}\left(1+\frac{sC_1}{G_{22}}\right)+\frac{K_{23}K_{32}(1+sC_2R)}{RG_{12}G_{21}\left(1+\frac{sL_2}{R}+s^2L_2C_2\right)}}}$	
Z_i DCM-DCM	$\frac{\left(1+sC_2R\left(\frac{1-M_2}{2-M_2}\right)\right)\left(\frac{sC_1}{G_{22}}+1\right)-\left(\frac{M_2^3}{1-M_2}\right)\frac{1}{RG_{22}}}{G_{11}\left[\left(1+sC_2R\left(\frac{1-M_2}{2-M_2}\right)\right)\left(\frac{sC_1}{G_{22}}+1\right)-\left(\frac{M_2^3}{1-M_2}\right)\frac{1}{RG_{22}}\right]-\frac{G_{12}G_{21}}{G_{22}}\left(1+sC_2R\left(\frac{1-M_2}{2-M_2}\right)\right)}$	

Table 5.2: Small-signal transfer functions

5.1.2 Dynamical Analysis

The system is in general third-order [35],[36], with L_1 being disqualified as a state variable because of its DCM operation. The following important results can be analytically derived from the transfer functions:

Poles & zeros	$C_1 \gg M_2^2 C_2$ & $M_1 \gg 1$		$C_1 \ll M_2^2 C_2$ & $M_1 \gg 1$	
	DCM-CCM	DCM-DCM	DCM-CCM	DCM-DCM
$-s_{rp1}$ Real Pole	$\frac{G_{22}}{C_1} + \frac{D^2}{RC_1}$	$\frac{2M_2^2}{RC_1}$	$\frac{1}{RC_2} + \frac{G_{22}}{D^2C_2}$	$\left(\frac{2-M_2}{1-M_2}\right)\frac{M_2^2}{RC_1}$
$-s_{rp2}$ Real Pole	-N/A-	$\left(\frac{2-M_2}{1-M_2}\right)\frac{1}{RC_2}$	-N/A-	$\frac{2}{RC_2}$
$-s_{2,3}$ Complex Poles	$\frac{1}{2RC_2} \pm j\frac{1}{\sqrt{L_2C_2}}$	-N/A-	$\frac{G_{22}}{2C_1} \pm j\frac{D}{\sqrt{L_2C_1}}$	-N/A-
$-s_{rz}$ Real zero of $\tilde{v}_o/\tilde{d}$	$\frac{G_{22}}{C_1} + \frac{D^2}{RC_1}$	$\left(\frac{2-M_2}{1-M_2}\right)\frac{M_2^2}{RC_1}$	$\frac{G_{22}}{C_1} + \frac{D^2}{RC_1}$	$\left(\frac{2-M_2}{1-M_2}\right)\frac{M_2^2}{RC_1}$
$-s_z$ Zero of Z_o	$\frac{G_{22}}{2C_1} \pm j\frac{D}{\sqrt{L_2C_1}}$ Complex	$\left(\frac{2-M_2}{1-M_2}\right)\frac{M_2^2}{RC_1}$ Real	$\frac{G_{22}}{2C_1} \pm j\frac{D}{\sqrt{L_2C_1}}$ Complex	$\left(\frac{2-M_2}{1-M_2}\right)\frac{M_2^2}{RC_1}$ Real

Table 5.3: Comparison of poles and zeros

1. Pole-zero cancellation occurs in $\tilde{v}_o/\tilde{d}$ when $C_1 \gg D^2C_2$. The resulting simple second-order transfer function gives fast dynamic response. However, for $C_1 \approx D^2C_2$, the system remains third-order, and for $C_1 \ll D^2C_2$, the poles split and the real pole becomes dominant. Fig. 5.8 shows the second-order oscillatory response for $C_1 \gg D^2C_2$, and Fig. 5.9 shows the dominant pole response for $C_1 \ll D^2C_2$.

Pole-zero Cancellation

Consider the characteristic cubic equation of the duty-ratio-to-output voltage transfer function of (5.8)

$$s^3 + \left(\frac{L_2C_1 + L_2C_2G_{22}R}{L_2C_1C_2R}\right)s^2 + \left(\frac{D^2C_2R + G_{22}L_2 + C_1R}{L_2C_1C_2R}\right)s + \frac{D^2 + G_{22}R}{L_2C_1C_2R} = 0 \quad (5.16)$$

Using the approximate solution of the cubic equation of Appendix A, the roots of (5.16) can be written as

$$s_{rp1} \approx -\frac{D^2 + G_{22}R}{D^2C_2R + G_{22}L_2 + C_1R} \quad (5.17)$$

$$s_{2,3} \approx -\frac{1}{2}\left(\frac{L_2C_1 + L_2C_2G_{22}R}{L_2C_1C_2R} + s_{rp1}\right) \pm j\sqrt{\frac{D^2C_2R + G_{22}L_2 + C_1R}{L_2C_1C_2R}} \quad (5.18)$$

where s_{rp1} and $s_{2,3}$ are the real and complex roots of (5.16) respectively. Since $RC_1 + D^2RC_2 \gg G_{22}L_2$, s_{rp1} can be written as

$$s_{rp1} \approx -\frac{D^2 + G_{22}R}{D^2RC_2 + RC_1} \quad (5.19)$$

Further consider $RC_1 \gg D^2RC_2$ in (5.19). This inequality can also be expressed as

$$C_1 \gg D^2C_2 \quad (5.20)$$

Thus,

$$-s_{rp1} \approx \frac{D^2 + G_{22}R}{RC_1} \approx \frac{G_{22}}{C_1} + \frac{D^2}{RC_1} \tag{5.21}$$

Now consider the numerator of $\tilde{v}_o/\tilde{d}$ of (5.8). The zero is

$$-s_{rz} = \frac{G_{22}}{C_1}\left(1 + \frac{K_{32}J_2}{G_{22}V_{C_1}}\right) \tag{5.22}$$

For large V_{C_1}/E ratios, V_{C_1}/E can be approximated as $1/\sqrt{K_1}$. Substituting this approximation in J_2 and G_{22} of Table 5.1, then putting them in (5.22), yields

$$-s_{rz} \approx \frac{G_{22}}{C_1} + \frac{D^2}{RC_1} \tag{5.23}$$

Comparing (5.21) with (5.23) indicates the occurrence of pole-zero cancellation for $C_1 \gg D^2C_2$ and $\frac{V_{C_1}}{E} \gg 1$. Substituting $C_1 \gg D^2C_2$ in $s_{2,3}$ of (5.18) results in

$$s_{2,3} \approx -\frac{1}{2}\left(\frac{1}{RC_2}\right) \pm j\sqrt{\frac{1}{L_2C_2}} \tag{5.24}$$

Inspection of (5.24) reveals that they are the complex poles of a loaded LC filter. This suggests that $\tilde{v}_o/\tilde{d}$ of the cascaded boost-and-buck converter operating in DCM-CCM reduces to a simple CCM buck converter's duty-ratio-to-output voltage transfer function which can be written as

$$\frac{\tilde{v}_o}{\tilde{d}} \approx V_{C_1}\left(\frac{1}{1 + \frac{1}{Q}\left(\frac{s}{\omega_o}\right) + \left(\frac{s}{\omega_o}\right)^2}\right) \tag{5.25}$$

where $Q = R_o/R$, $R_o = \sqrt{L_2/C_2}$ and $\omega_o = 1/\sqrt{L_2C_2}$ [41]. Magnitude responses shown in Figs. 5.10 and 5.11 and the phase responses shown in Figs. 5.12 and 5.13 verify this fact for the case of $C_1 = 100\mu$F and $C_2 = 10\mu$F. They also verify the cubic root approximation proposed in Appendix A. Computer programs have been written to plot the frequency response curves shown in Figs. 5.10 and 5.12. These computer programs are given in Appendix C.

2. From the Z_o transfer function, the DC output impedance is

$$Z_o|_{s=0} = \frac{R}{1 + \frac{G_{22}R}{D^2}} \approx \frac{R}{2} \quad \text{if } V_{C_1}/E \gg 1 \tag{5.26}$$

which is undesirably high. (Note that $V_{C_1}/E \approx \sqrt{RT/2L_1}$ and hence $G_{22} \approx D^2/R$ for large V_{C_1}/E.) The output voltage is thus rather sensitive to load current variation contrary to a buck CCM converter. Also, as observed from Table 5.2, there is a complex zero pair at $G_{22}/2C_1 \pm jD/\sqrt{L_2C_1}$, causing a "glitch" in the frequency response of Z_o. However, if $C_1 \ll D^2C_2$ and $V_{C_1}/E \gg 1$, from Table 5.2, the complex poles and zeros cancel out (the "glitch" gets eliminated) resulting in a single-pole impedance: $Z_o \approx R/[2(1 + sC_2R/2)]$.

3. Unlike $\tilde{v}_o/\tilde{d}$, $\tilde{v}_o/\tilde{e}$ has no zeros in its transfer function.

4. When V_{C_1}/E is large, Z_i is devoid of any dynamics. This property is exploited for PFC applications as has been well understood [17],[18]. Specifically, putting $V_{C_1}/E \gg 1$ in Z_i in Table 5.2, gives

$$Z_i \approx \frac{1}{G_{11}} \approx \frac{2L_1}{D^2T} \tag{5.27}$$

which is consistent with the value found directly from the average model shown in Fig. 5.3.

5.1.3 Computer Simulations

In the foregoing analysis, the dynamical behaviour for different relative sizes of C_1 and C_2 was analyzed. Such is also partially illustrated in the form of root loci in Figs. 5.14 and 5.15 which essentially show the movement of the poles as either one of the capacitor values is varied. In this subsection, PSPICE is used to verify the qualitative behaviour as observed from the above analysis. The PSPICE netlists of all the small-signal models which are used to generate the frequency responses are given in Appendix B. The circuit parameters used for simulation are $L_1 = 0.2\text{mH}$, $L_2 = 0.5\text{mH}$, $D = 0.4$, $R = 100\Omega$, $f_s = 100\text{kHz}$, $E = 160\text{V}$. A series of frequency response curves corresponding to different relative sizes of C_1 and C_2 are given below.

1. Fig. 5.16 shows the frequency response of $\tilde{v}_o/\tilde{d}$. It is generally a third-order response with three LHP poles and one LHP zero, the phase response extending from $0°$ to $-180°$, as predicted from the analysis. Also, from Fig. 5.16, the response resembles a second-order filter for large C_1, with corner frequency at $1/2\pi\sqrt{L_2C_2}$.

2. The Z_o frequency response is shown in Fig. 5.17. It can be clearly noticed that the LHP complex zero pair whose corner frequency is $D/\pi\sqrt{L_2C_1}$, as predicted in Table 5.2. This is also confirmed by the phase response shown in Fig. 5.17 which shows the phase rising from $-90°$ to $+90°$ and back to $-90°$ due to the complex LHP pole pair $-s_{2,3}$. Fig. 5.17 also confirms the prediction of the elimination of the "glitch" for $C_1 \ll D^2C_2$ giving a single-pole response.

3. Fig. 5.18 shows the magnitude and phase responses of $\tilde{v}_o/\tilde{e}$. The absence of any zeros is clearly verified by the phase response being extending from $0°$ to $-270°$.

4. Fig. 5.19 verifies that the input impedance is equal to $2L_1/D^2T$ when V_{C_1}/E is large, and that the phase shift is negligible. Thus, the input of the converter emulates a resistor.

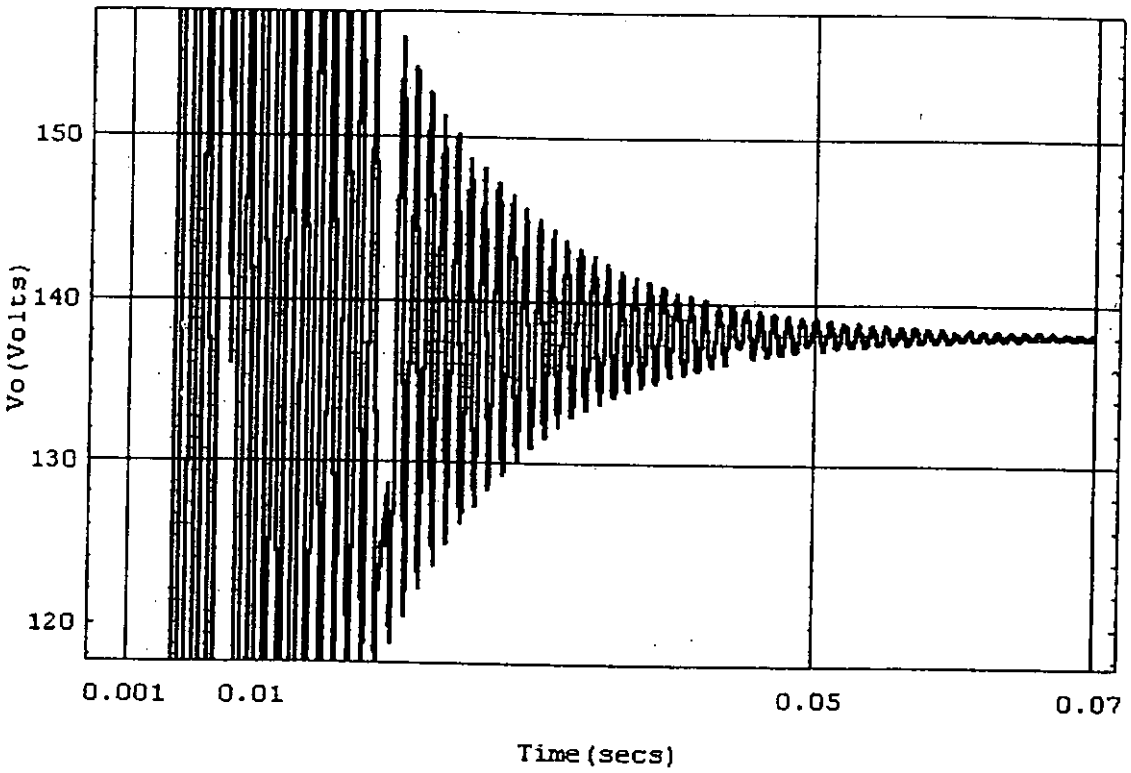

Figure 5.8: Output voltage transient response with pole-zero cancellation ($C_1 \gg D^2C_2$) for DCM-CCM operation showing damped oscillatory second-order response

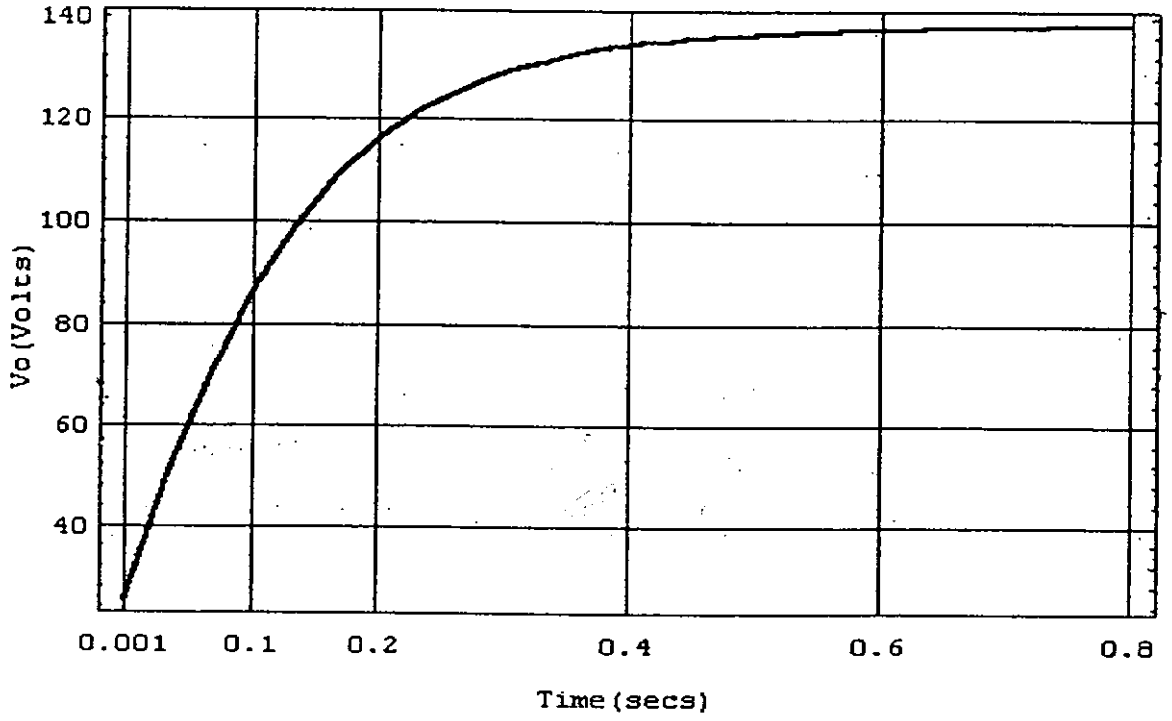

Figure 5.9: Output voltage transient response without pole-zero cancellation ($C_1 \ll D^2C_2$) for DCM-CCM operation showing dominant first-order response

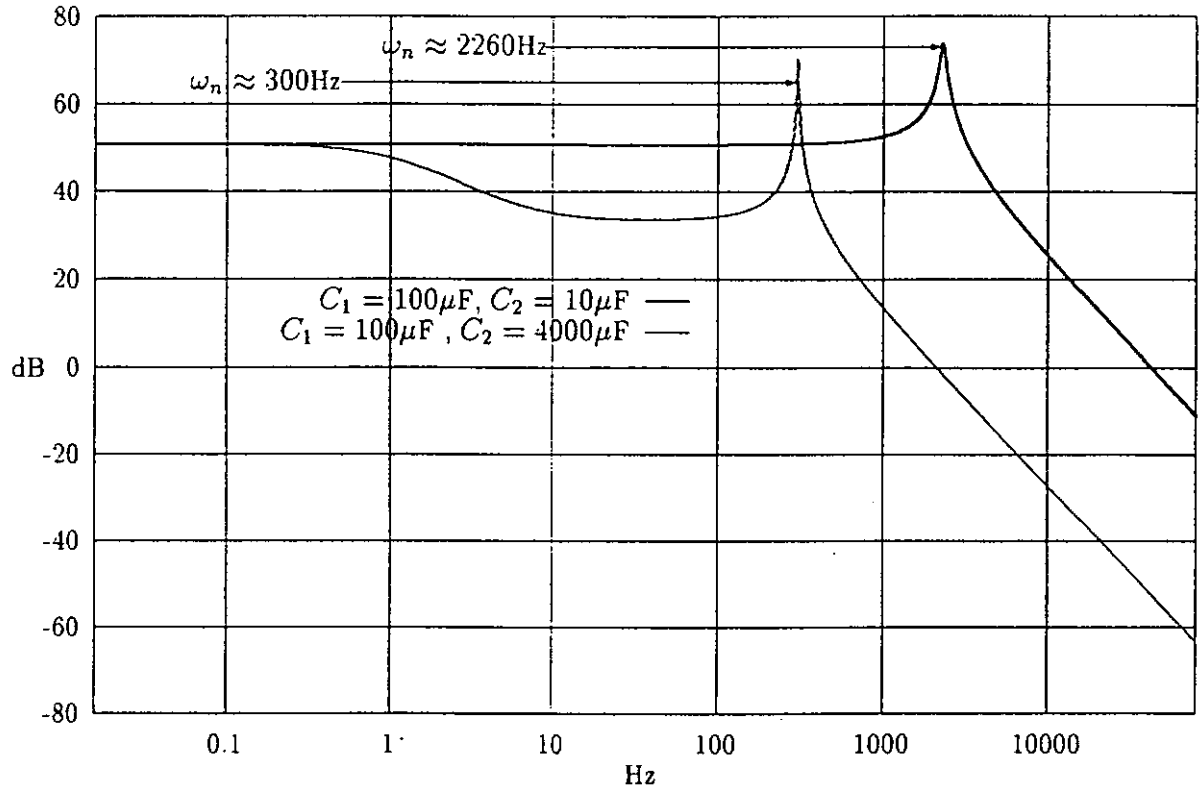

Figure 5.10: Magnitude response of duty-ratio-to-output voltage transfer function by using the proposed approximations

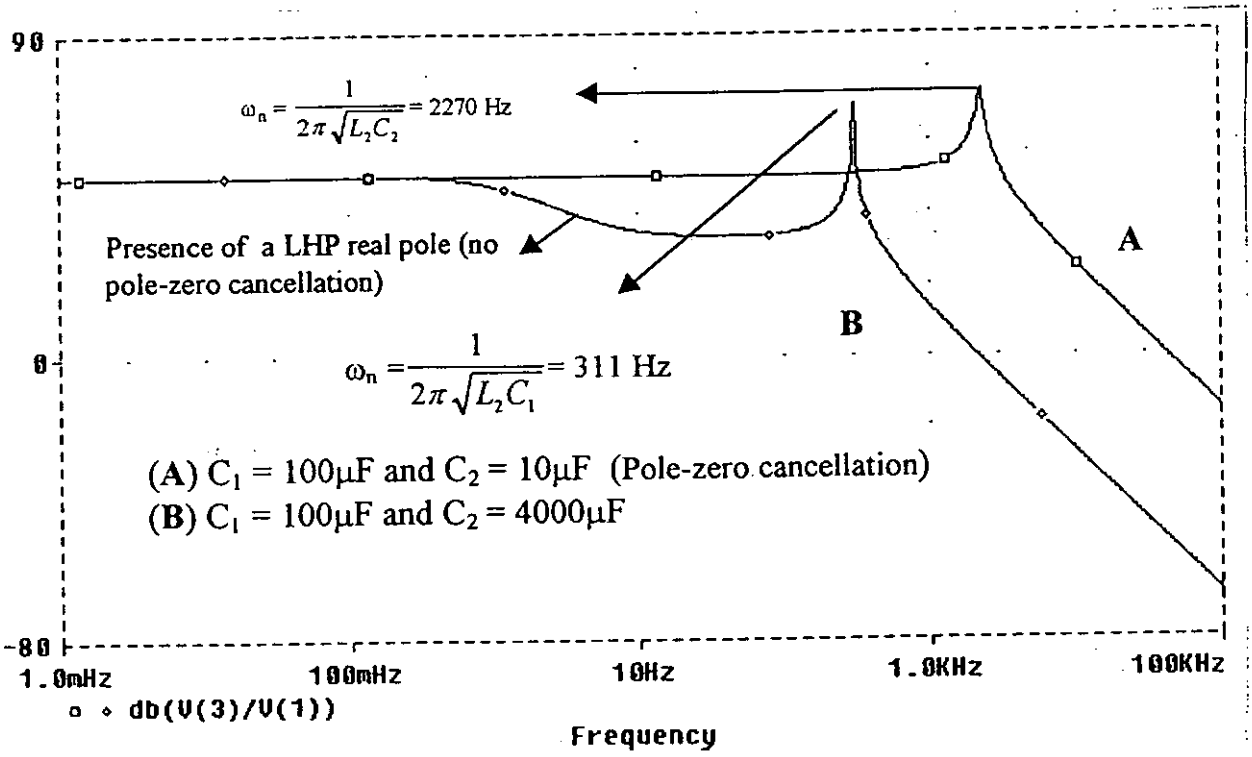

Figure 5.11: Magnitude response of duty-ratio-to-output voltage transfer function of PSPICE

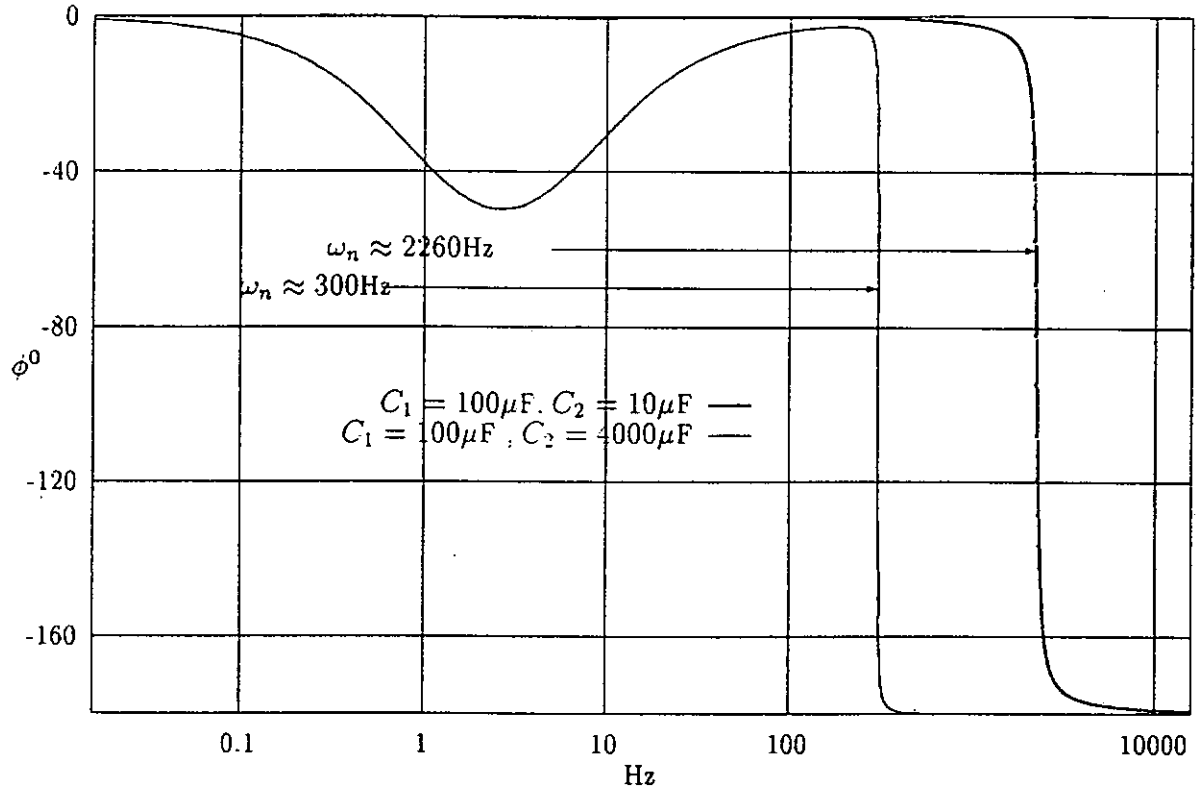

Figure 5.12: Phase response of duty-ratio-to-output voltage transfer function by using the proposed approximations

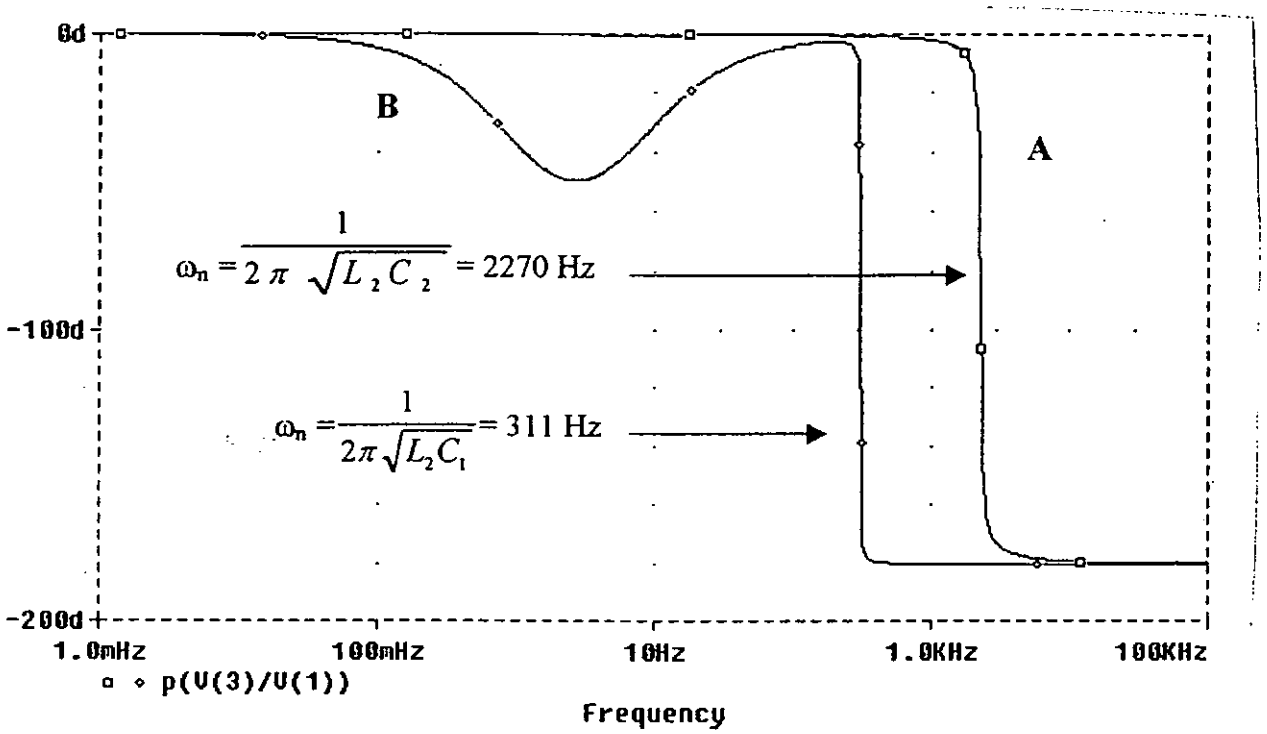

Figure 5.13: Phase response of duty-ratio-to-output voltage transfer function of PSPICE

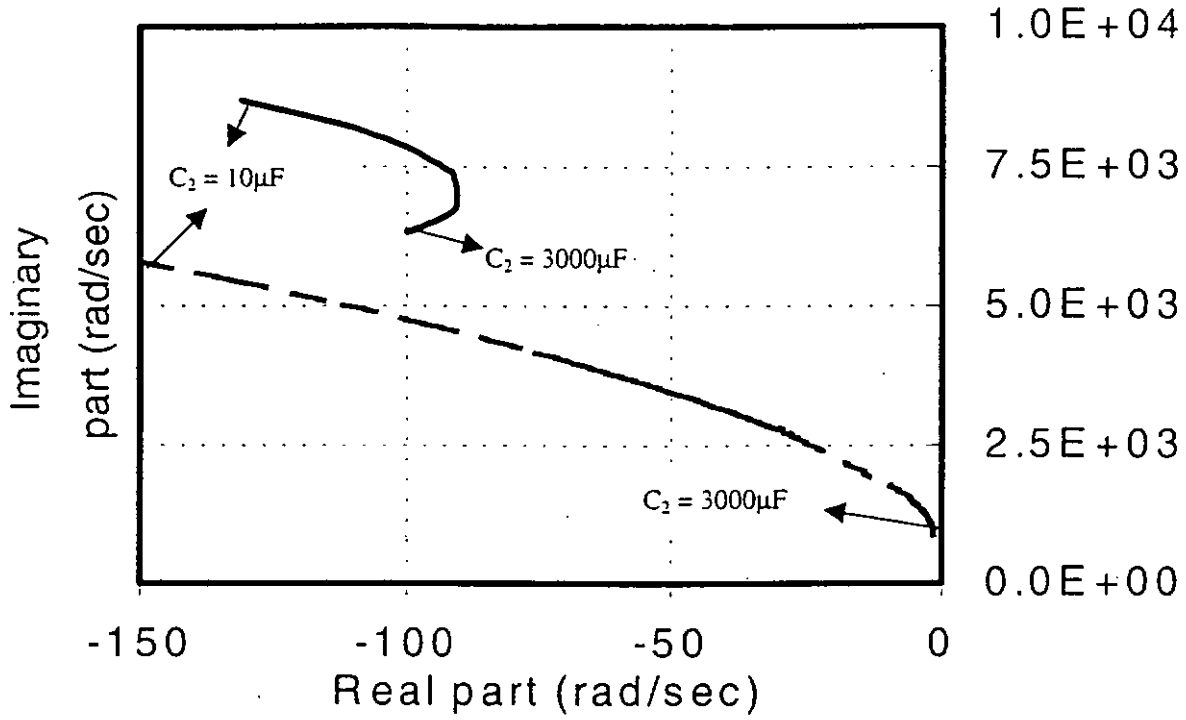

Figure 5.14: Comparison of root loci for DCM-CCM operation. Fixed C_2 and varying C_1 from 10 to 4000μF. Upper locus: $C_2 = 50\mu$F; Lower locus: $C_2 = 3000\mu$F

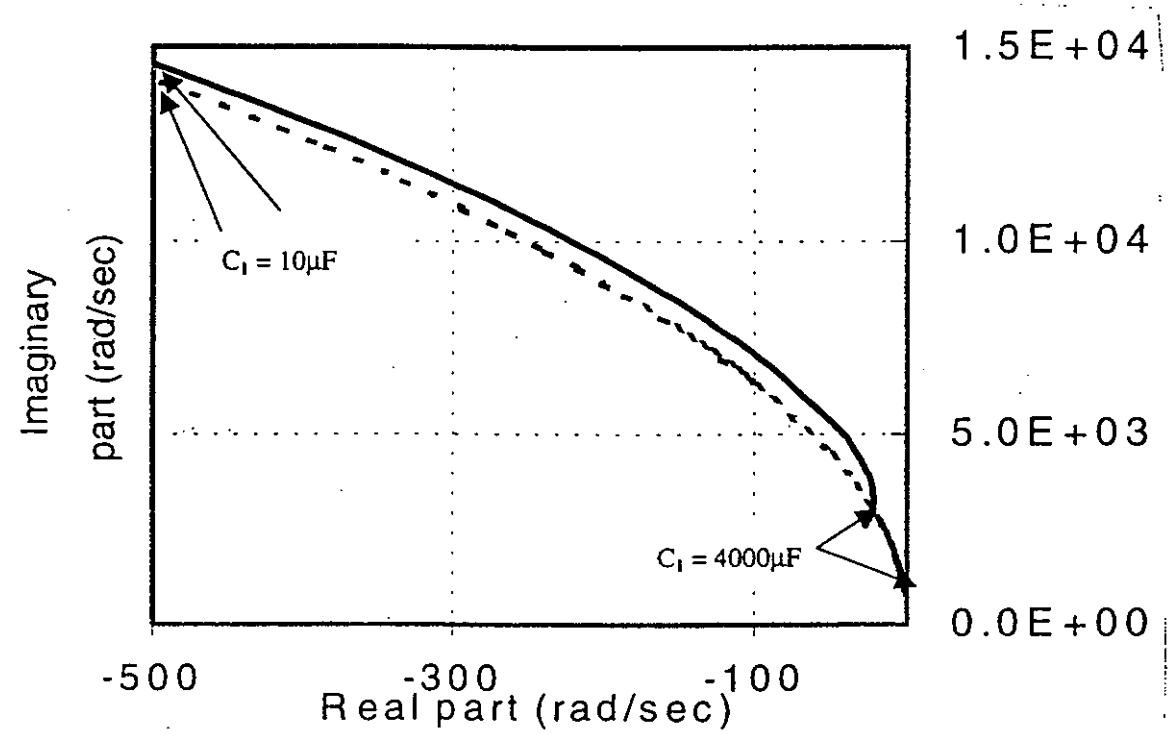

Figure 5.15: Comparison of root loci for DCM-CCM operation. Fixed C_1 and varying C_2 from 10 to 3000μF. Upper locus: $C_1 = 50\mu$F; Lower locus: $C_1 = 3000\mu$F

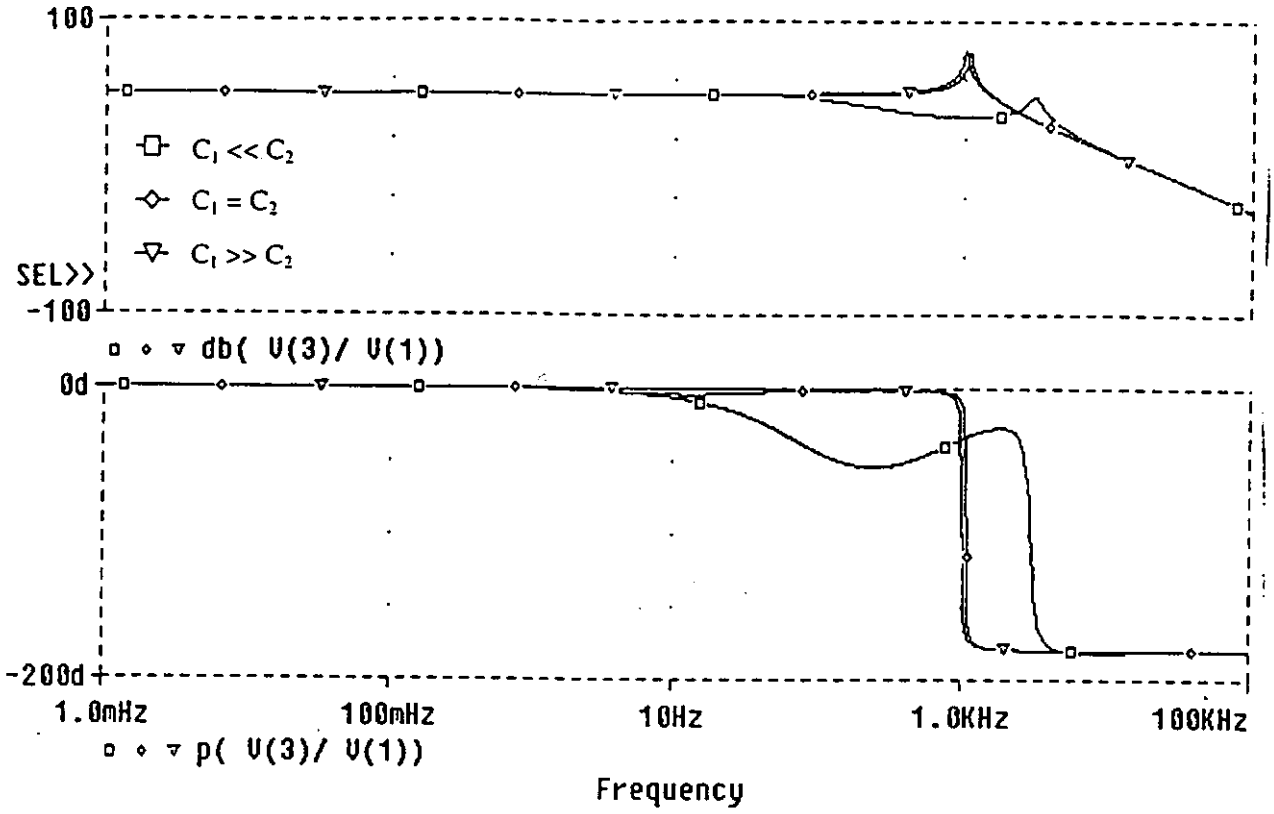

Figure 5.16: $\tilde{d}$-to-$\tilde{v}_o$ frequency responses for DCM-CCM operation for different relative sizes of capacitances. Upper plot: magnitude (dB); Lower plot: phase (deg)

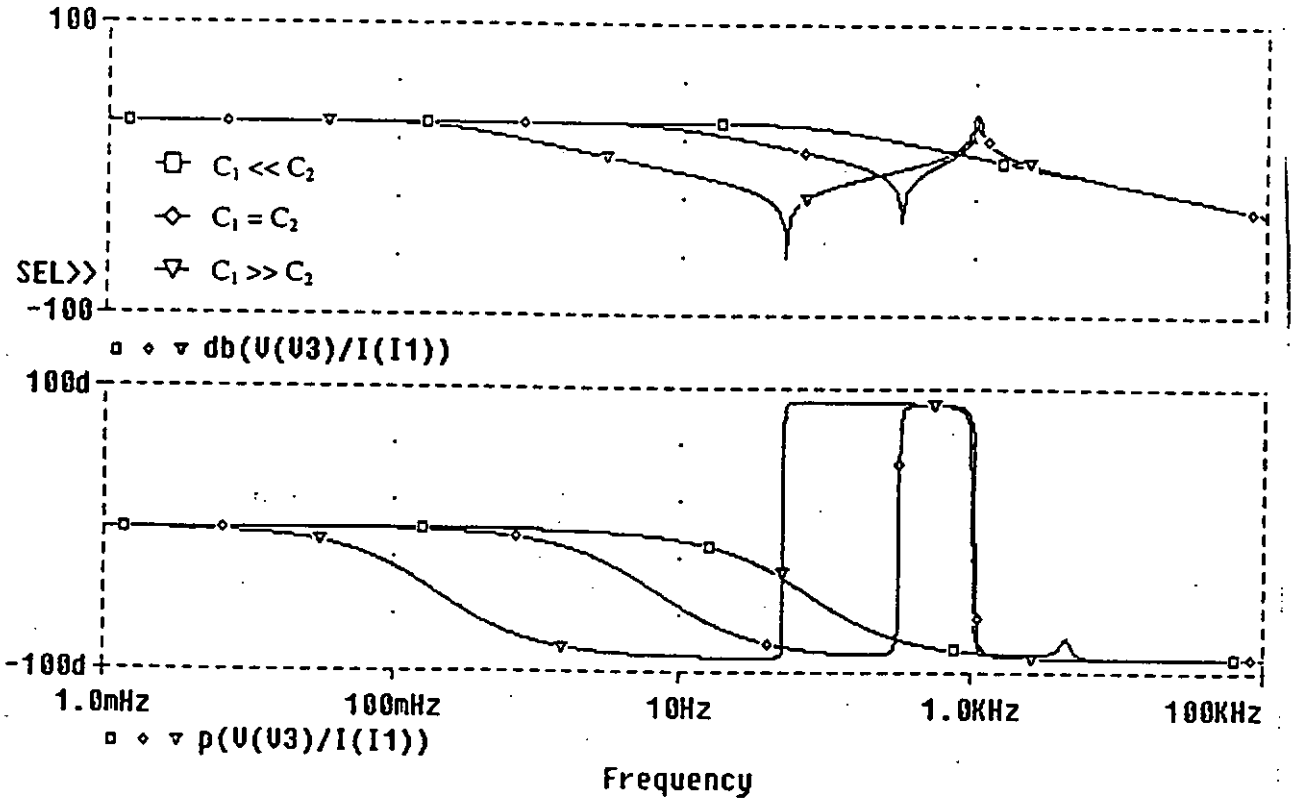

Figure 5.17: Z_o frequency responses for DCM-CCM operation for different relative sizes of capacitances. Upper plot: magnitude (dB); Lower plot: phase (deg)

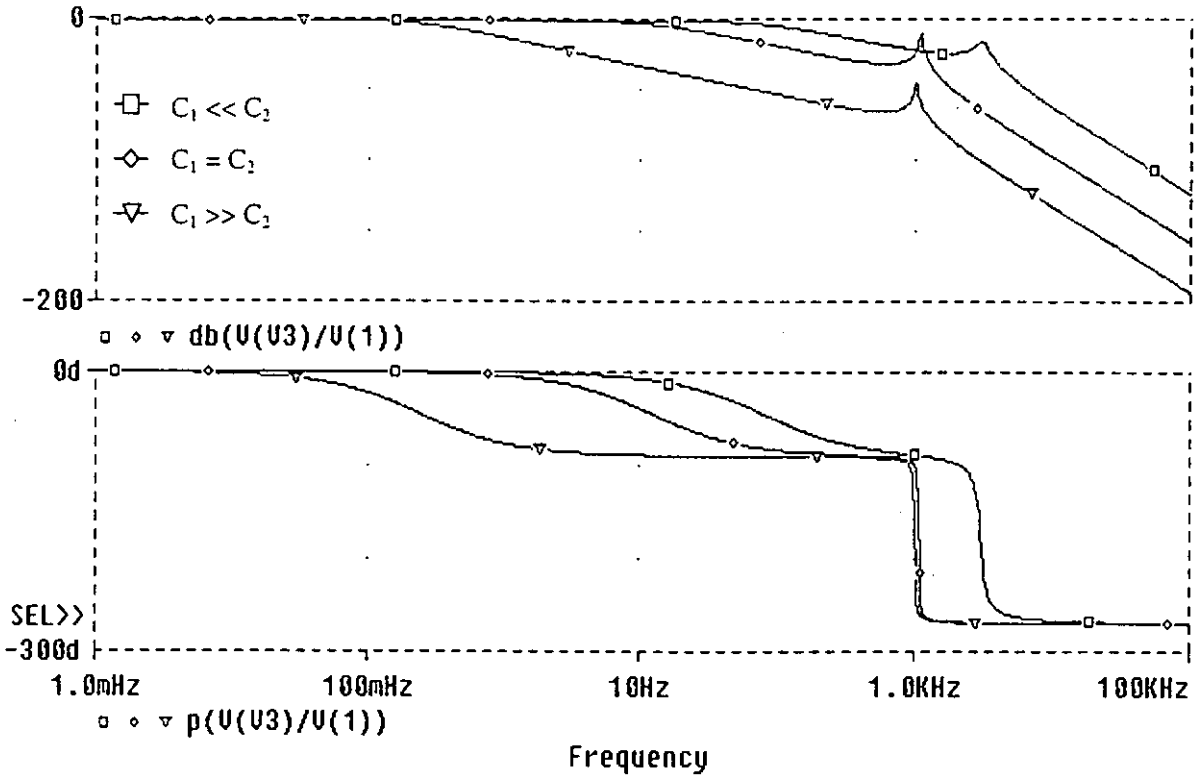

Figure 5.18: $\tilde{e}$-to-$\tilde{v}_o$ frequency responses for DCM-CCM operation for different relative sizes of capacitances. Upper plot: magnitude (dB); Lower plot: phase (deg)

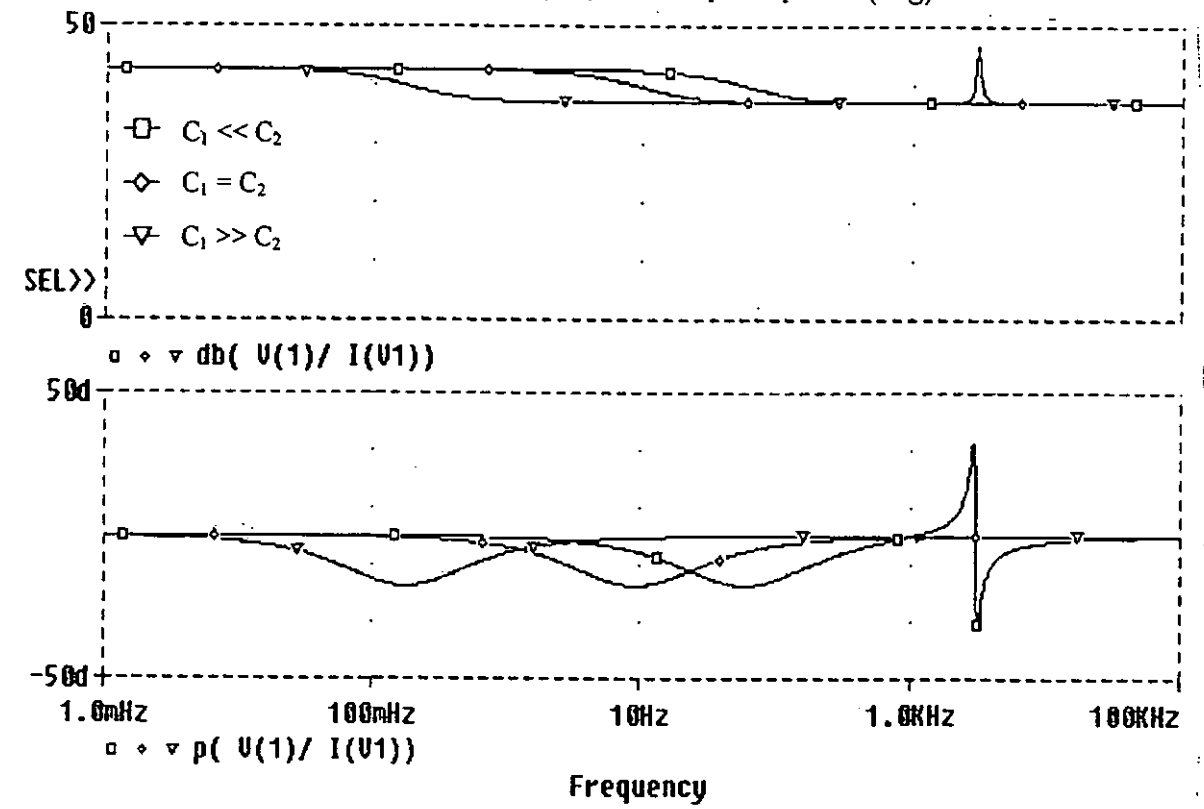

Figure 5.19: Z_i frequency responses for DCM-CCM operation for different relative sizes of capacitances. Upper plot: magnitude (dB); Lower plot: phase (deg)

5.2 Dynamical Analysis of Boost-and-buck Converter in DCM-DCM

The switching waveforms of cascaded boost-and-buck converter operating in DCM-CCM is shown in Fig. 5.2(b). By averaging the inductor and capacitor current and voltage waveforms over a switching cycle [36], the following equations are derived

$$i_{L_1} = \frac{d^2 T \epsilon}{2L_1(1-\epsilon/v_{C_1})} \tag{5.28}$$

$$C_1 \frac{dv_{C_1}}{dt} = i_{C_1} = \frac{d^2 T e}{2L_1(v_{C_1}/e-1)} - d^2 T \frac{v_{C_1}-v_o}{2L_2} \tag{5.29}$$

$$C_2 \frac{dv_o}{dt} = i_{C_2} = v_{C_1}\left(\frac{v_{C_1}-v_o}{v_o}\right)\frac{d^2 T}{2L_2} - \frac{v_o}{R} \tag{5.30}$$

which provide an analytical basis to derive the averaged model shown in Fig. 5.20.

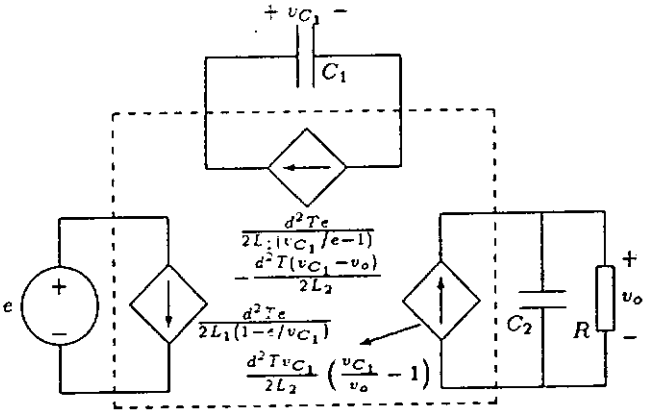

Figure 5.20: Averaged model of boost-and-buck converter operating in DCM-DCM

5.2.1 Derivation of Small-signal Transfer Functions

Application of small-signal linearization [36] results in the small-signal model shown in Fig. 5.21. The corresponding small-signal parameters are listed in Table 5.1. As the model shown in Fig. 5.21 clearly suggests, the dynamics is second-order, with two real poles determined by C_1/G_{22} and RC_2. Based on this model, all transfer functions of interest are derived.

5.2.1.A Duty-ratio-to-output Voltage Transfer Function

In deriving the $\tilde{v}_o/\tilde{d}$ transfer function, the input $\tilde{e}$ is set to zero. The circuit model thus reduces to the one shown in Fig. 5.22. Application of nodal analysis to this circuit gives

$$\begin{bmatrix} -G_{23} & G_{22}+sC_1 \\ \frac{1+sRC_2}{R}+G_{33} & -G_{32} \end{bmatrix} \begin{bmatrix} \tilde{v}_o \\ \tilde{v}_{C_1} \end{bmatrix} = \begin{bmatrix} J_2\tilde{d} \\ J_3\tilde{d} \end{bmatrix} \tag{5.31}$$

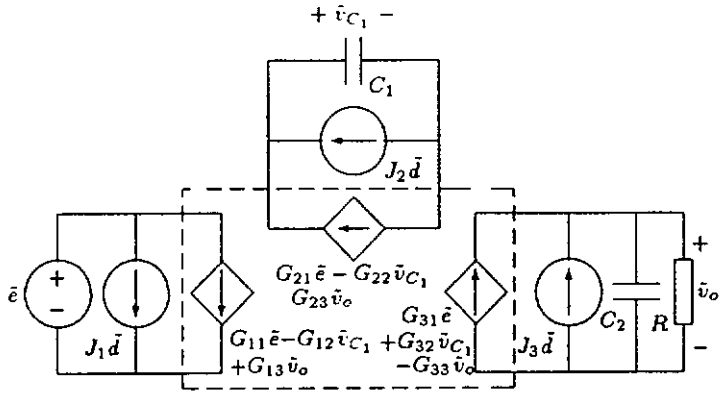

Figure 5.21: Small-signal model of boost-and-buck converter operating in DCM-DCM

Solving (5.31) for $\tilde{v}_o$ results in

$$\frac{\tilde{v}_o}{\tilde{d}} = \frac{RJ_3\left[1 + \frac{sC_1}{G_{22}} + \frac{G_{32}J_2}{J_3G_{22}}\right]}{\left(1 + \frac{sC_1}{G_{22}}\right)(1 + sRC_2 + RG_{33}) - \frac{RG_{23}G_{32}}{G_{22}}} \tag{5.32}$$

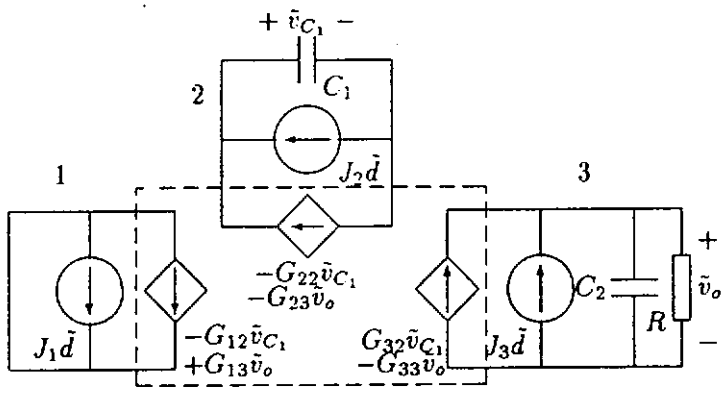

Figure 5.22: Model for $\tilde{v}_o/\tilde{d}$ calculation

5.2.1.B Output Impedance Transfer Function

In deriving the output impedance, the inputs $\tilde{e}$ and $\tilde{d}$ are set to zero. A test current source $\tilde{i}_s$ is injected to the output terminal as shown in Fig. 5.23. Application of nodal analysis to this circuit gives

$$\begin{bmatrix} -G_{23} & G_{22} + sC_1 \\ \frac{1+sRC_2}{R} + G_{33} & -G_{32} \end{bmatrix} \begin{bmatrix} \tilde{v}_o \\ \tilde{v}_{C_1} \end{bmatrix} = \begin{bmatrix} 0 \\ \tilde{i}_s \end{bmatrix} \tag{5.33}$$

Solving (5.33) for $\tilde{v}_o$ results in

$$Z_o = \frac{\tilde{v}_o}{\tilde{i}_s} = \frac{R\left[1 + \frac{sC_1}{G_{22}}\right]}{\left(1 + \frac{sC_1}{G_{22}}\right)(1 + sRC_2 + RG_{33}) - \frac{RG_{23}G_{32}}{G_{22}}} \tag{5.34}$$

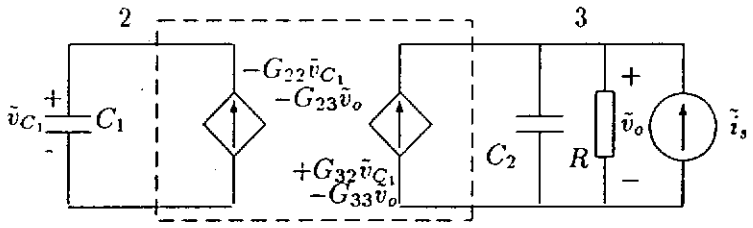

Figure 5.23: Model for calculation of Z_o

5.2.1.C *Line-to-output Voltage Transfer Function*

In deriving the line-to-output voltage transfer function, the duty-ratio $\tilde{d}$ is set to zero, Thus, the circuit model reduces to the one shown in Fig. 5.24. Application of nodal analysis to this circuit gives

$$\begin{bmatrix} -G_{23} & G_{22}+sC_1 \\ \frac{1+sRC_2}{R}+G_{33} & -G_{32} \end{bmatrix} \begin{bmatrix} \tilde{v}_o \\ \tilde{v}_{C_1} \end{bmatrix} = \begin{bmatrix} G_{21}\tilde{e} \\ 0 \end{bmatrix} \tag{5.35}$$

Solving (5.35) for $\tilde{v}_o$ results in

$$\frac{\tilde{v}_o}{\tilde{e}} = \frac{\frac{RG_{32}G_{21}}{G_{22}}}{\left(1+\frac{sC_1}{G_{22}}\right)(1+sRC_2+RG_{33}) - \frac{RG_{23}G_{32}}{G_{22}}} \tag{5.36}$$

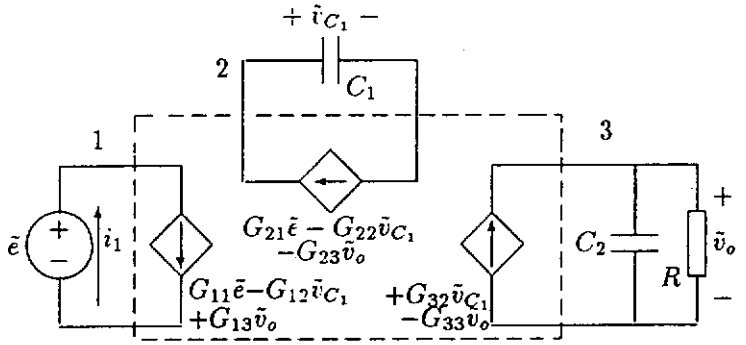

Figure 5.24: Model for calculation of $\tilde{v}_o/\tilde{e}$ and Z_i

5.2.1.D *Input Impedance Transfer Function*

The same model shown in Fig. 5.7 is used again for the derivation of input impedance. The nodal equation is given by

$$\begin{bmatrix} 1 & G_{12} & 0 \\ 0 & -G_{23} & G_{22}+sC_1 \\ 0 & G_{33}+\frac{1+sRC_2}{R} & -G_{32} \end{bmatrix} \begin{bmatrix} \tilde{i}_1 \\ \tilde{v}_o \\ \tilde{v}_{C_1} \end{bmatrix} = \begin{bmatrix} G_{11}\tilde{e} \\ G_{21}\tilde{e} \\ 0 \end{bmatrix} \tag{5.37}$$

Solving (5.37) for $\tilde{i}_1$ yields

$$Z_i = \frac{\tilde{e}}{\tilde{i}_1} = \frac{\left(1+\frac{sC_1}{G_{22}}\right)(1+sRC_2+RG_{33}) - \frac{RG_{23}G_{32}}{G_{22}}}{G_{11}\left[\left(1+\frac{sC_1}{G_{22}}\right)(1+sRC_2+RG_{33}) - \frac{RG_{23}G_{32}}{G_{22}}\right] - \frac{G_{12}G_{21}}{G_{22}}(1+sRC_2+RG_{33})} \tag{5.38}$$

All the transfer functions are further simplified in order to represent them in the conventional form and listed in Table 5.2. Locations of poles and zeros are also given in Table 5.3.

5.2.2 Dynamical Analysis

The system is generally second-order with two real poles. From the transfer functions, the following observations can be made:

1. Pole-zero cancellation occurs in $\tilde{v}_o/\tilde{d}$ and Z_o if either of the following is satisfied:

   (i) $V_{C_1}/E \gg 1$ and $C_1 \ll (V_o/V_{C_1})^2 C_2$; or

   (ii) $V_{C_1}/E \gg 1$ and $V_o/V_{C_1} \ll 1$, irrespective of the values of C_1 and C_2.

   Since none of these conditions is practical, pole-zero cancellation does not normally occur. Moreover, for $C_1 \gg (V_o/V_{C_1})^2 C_2$ and for any practical value of V_o/V_{C_1}, it can be observed from Table 5.3 that s_{rz} and s_{rp1} are close to each other, resulting in a quasi-pole-zero-cancellation and leaving a single-pole response:

$$\frac{\tilde{v}_o}{\tilde{d}} \approx \frac{A_{vd}|_{s=0}}{1+\left(\frac{s(2-M_2)}{RC_2(1-M_2)}\right)} \tag{5.39}$$

$$Z_o \approx \frac{A_{zo}|_{s=0}}{1+\left(\frac{s(2-M_2)}{RC_2(1-M_2)}\right)} \tag{5.40}$$

2. Like the DCM-CCM case, $\tilde{v}_o/\tilde{e}$ has no zeros. Moreover, the two real poles are determined by C_1/G_{22} and RC_2.

3. The input impedance Z_i has the same characteristics as in the DCM-CCM case, for $V_{C_1}/E \gg 1$.

5.2.3 Computer Simulations

In this subsection PSPICE simulations of the frequency responses based on the small-signal model are reported. The PSPICE netlists of all the small-signal models which are used to generate the frequency responses are given in Appendix B. The circuit parameters chosen for the simulation are $L_1 = 0.08\text{mH}$, $L_2 = 0.1\text{mH}$, $D = 0.25$, $R = 100\Omega$, $f_s = 100\text{kHz}$, and $E = 160\text{V}$. In particular, from what PSPICE reports, the previously derived analytical results are verified as follows:

1. Figs. 5.25 and 5.26 show the frequency response of $\tilde{v}_o/\tilde{d}$ and Z_o respectively. Both of these manifest a second-order response having an LHP zero and two LHP poles, as predicted in Table 5.3. Moreover, for the case of $C_1 \gg (V_o/V_{C_1})^2 C_2$, we see that the pole ($s_{rp1}$) is close to the zero (either s_z or s_{rz}), practically within a decade, giving effectively a single-pole response determined by RC_2.

2. Pole-zero cancellation occurs for $C_1 \ll (V_o/V_{C_1})^2 C_2$, as can be observed in the magnitude plots of $\tilde{v}_o/\tilde{d}$ and Z_o in Figs. 5.25 and 5.26.

3. Fig. 5.27 shows the frequency response of $\tilde{v}_o/\tilde{e}$. In this case, the phase response extends from 0° to −180°, from which the absence of zeros in the transfer function are verified.

4. Fig. 5.28 shows the input impedance Z_i. For $V_{C_1}/E \gg 1$, Z_i has the same characteristics as its counterpart in DCM-CCM.

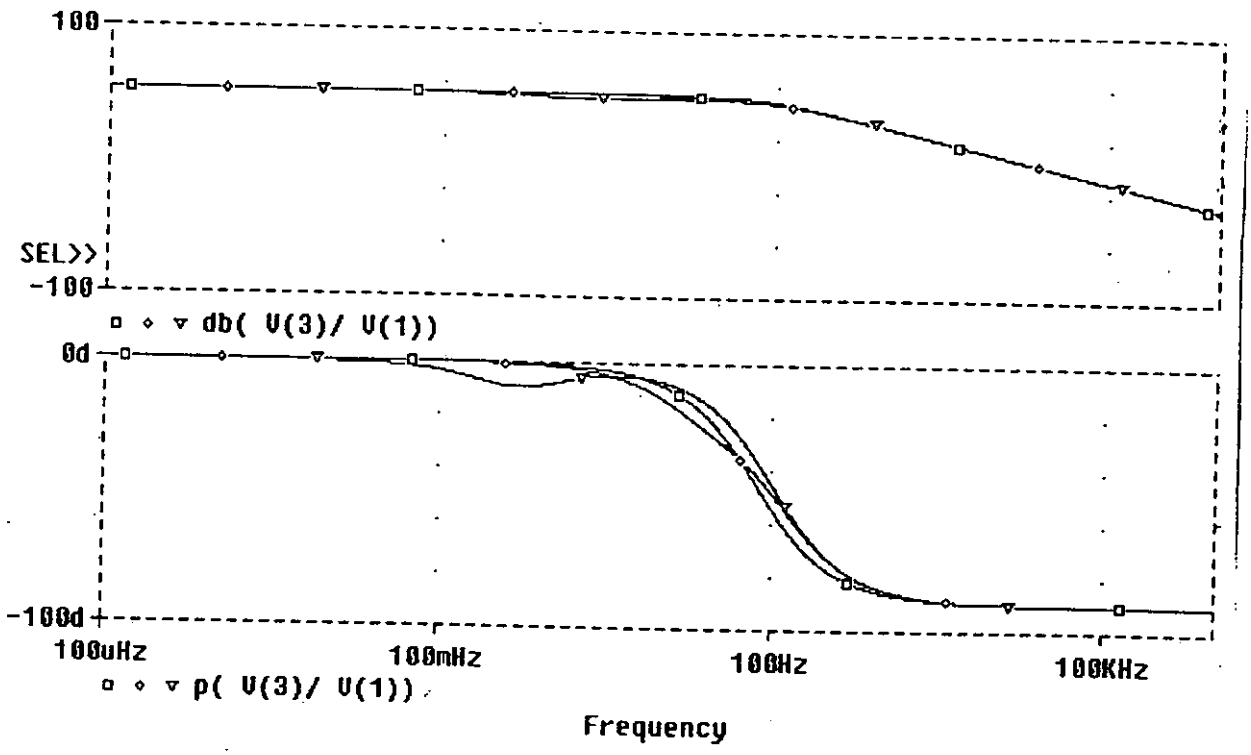

Figure 5.25: $\tilde{d}$-to-$\tilde{v}_o$ frequency responses for DCM-DCM operation for different relative sizes of capacitances. Upper plot: magnitude (dB); Lower plot: phase (deg)

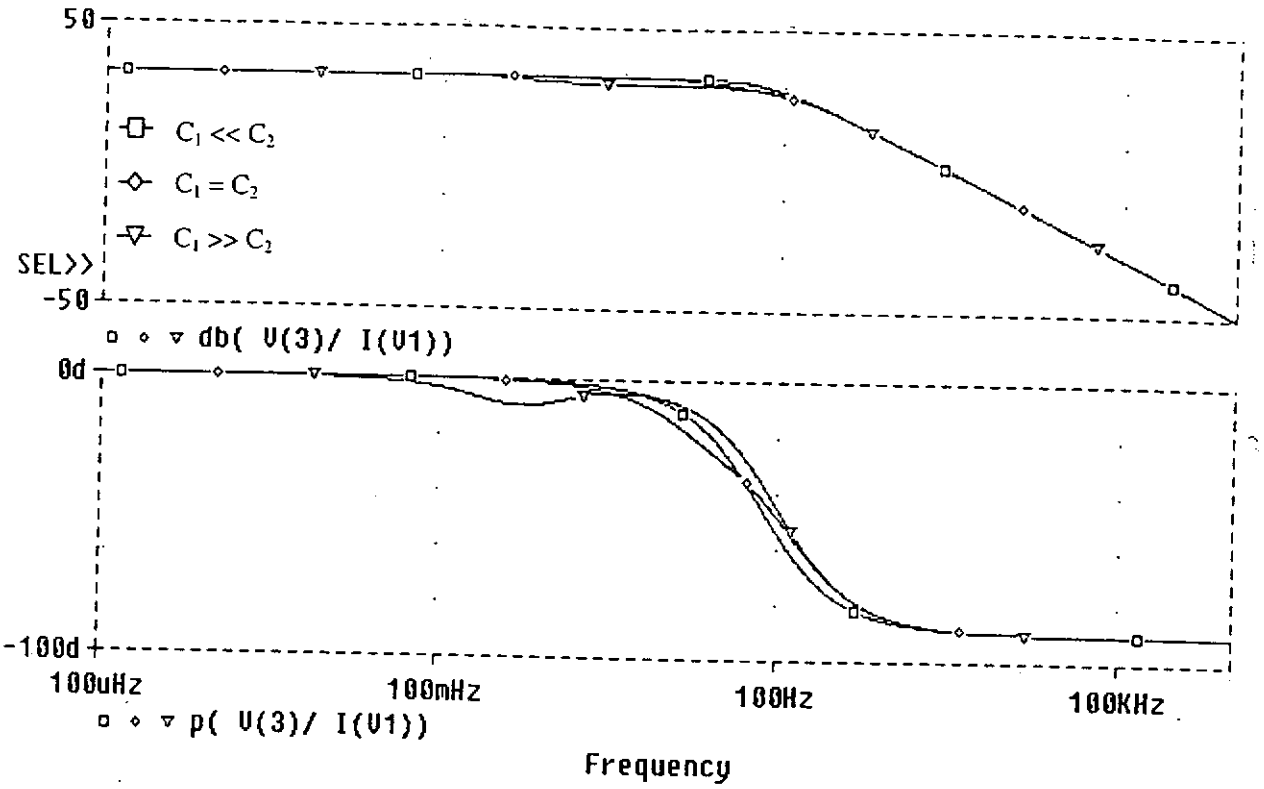

Figure 5.26: Z_o frequency responses for DCM-DCM operation for different relative sizes of capacitances. Upper plot: magnitude (dB); Lower plot: phase (deg)

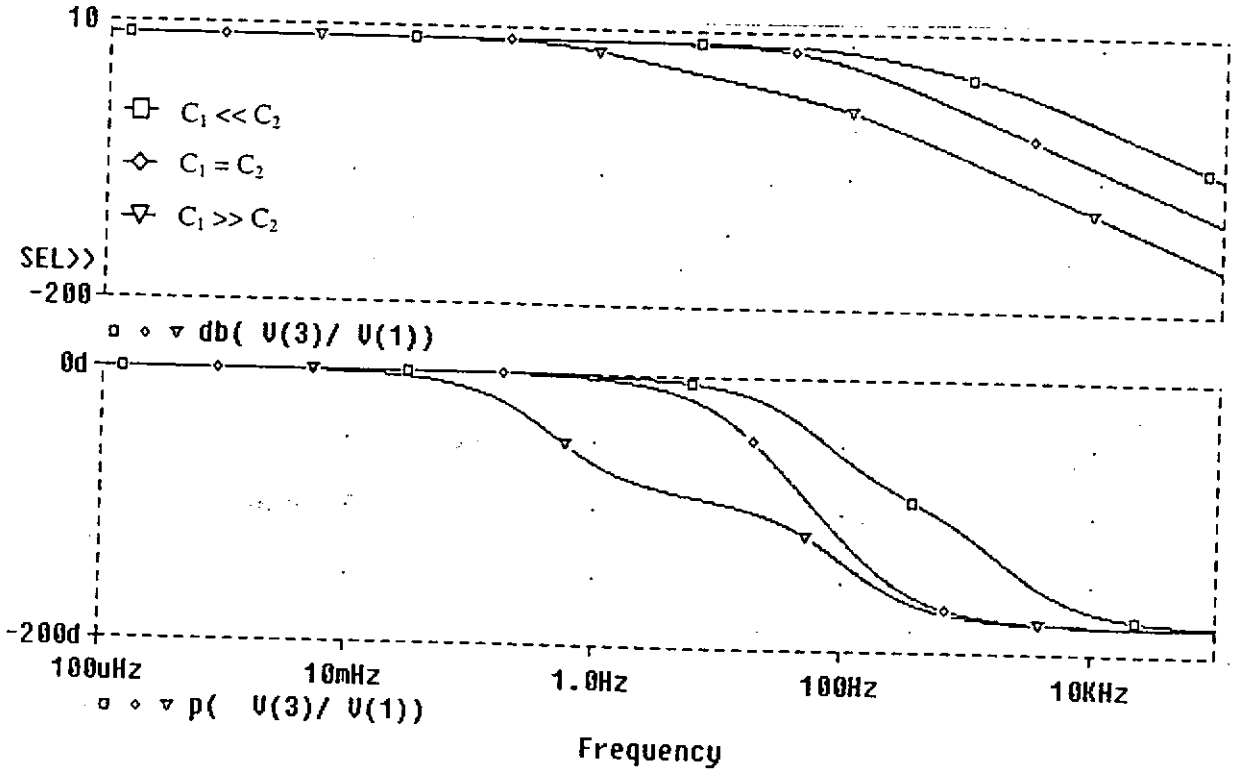

Figure 5.27: $\tilde{e}$-to-$\tilde{v}_o$ frequency responses for DCM-DCM operation for different relative sizes of capacitances. Upper plot: magnitude (dB); Lower plot: phase (deg)

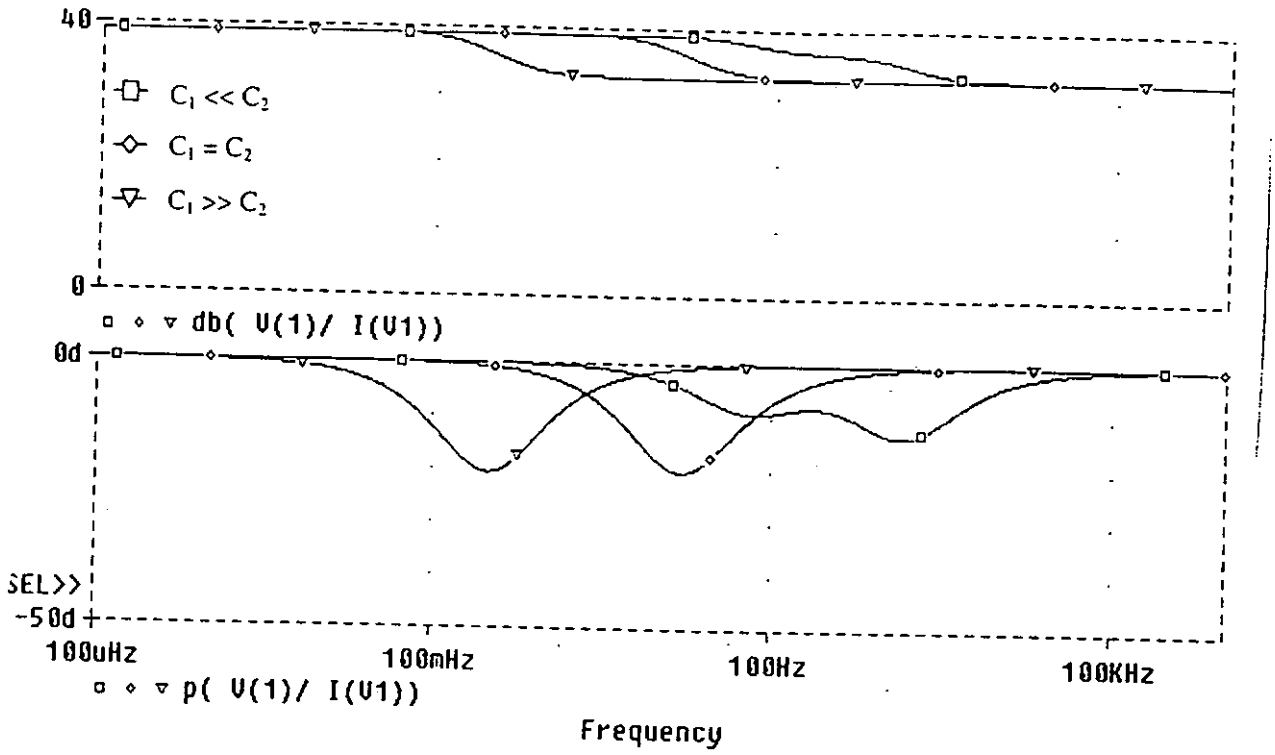

Figure 5.28: Z_i frequency responses for DCM-DCM operation for different relative sizes of capacitances. Upper plot: magnitude (dB); Lower plot: phase (deg)

5.3 Concluding Remarks

Complete sets of small-signal transfer functions for the cascaded boost-and-buck PFC converter are derived in this chapter. The results are important in understanding the dynamics of this kind of converter and the various factors that can affect the dynamical response of the converter.

In particular, it is shown that when the boost part operates in discontinuous mode and the buck part in continuous mode, the duty-ratio-to-output transfer function can be reduced to a simple second-order function when the storage capacitor is sufficiently large. Such order reduction (pole-zero cancellation) is important for achieving fast response. Though the output buck stage is operating in CCM (i.e.,when the converter is operating in DCM-CCM), steady-state output impedance is greater than the output impedance of a buck converter operating in CCM. Moreover, when both the boost and buck parts operate in discontinuous mode, the system can achieve fast response for most practical situations regardless of the occurrence of pole-zero cancellation. In the next chapter a detailed comparison of the dynamical analysis of BIFRED and cascaded boost-and-flyback converter is given.

Chapter 6

Comparison of Small-Signal Dynamics of BIFRED and Single-Stage Cascaded Boost-and-Flyback PFC Converters

In the previous chapter a detailed small-signal dynamical analysis of cascaded boost-and-buck converter operating in both DCM-CCM and DCM-CCM is given. This chapter gives a detailed analysis and comparison of the small-signal dynamical response of Boost Integrated with Flyback Rectifier Energy storage DC-DC converter (BIFRED) [1] and single-stage cascaded boost-and-flyback [2] converters [2], and explains how the relative sizes of the storage and output capacitors affect the dynamics. Complete sets of small-signal transfer functions are derived and compared for both the BIFRED and single-stage cascaded boost-and-flyback converter, for all common operating modes. Conditions for order reduction are also given. Throughout the chapter, uppercase letters will be used to denote steady-state values, and letters with *tilde* ($\tilde{}$) for small-signal variables. Also, for simplicity, single-stage cascaded boost-and-flyback converter will be referred to as boost-and-flyback converter. The non-isolated version of BIFRED and boost-and-flyback converter are shown in Figs. 6.1(a) and 6.1(b) respectively. Topologically BIFRED is an isolated version of *decoupled* SEPIC. The term *decoupled* implies that voltages e, v_{C_1} and v_o are independent. In particular, the duty-ratio-to-output voltage transfer function $\tilde{v}_o/\tilde{d}$, line-to-output voltage transfer function $\tilde{v}_o/\tilde{e}$, output impedance Z_o and input impedance Z_i will be derived and analyzed.

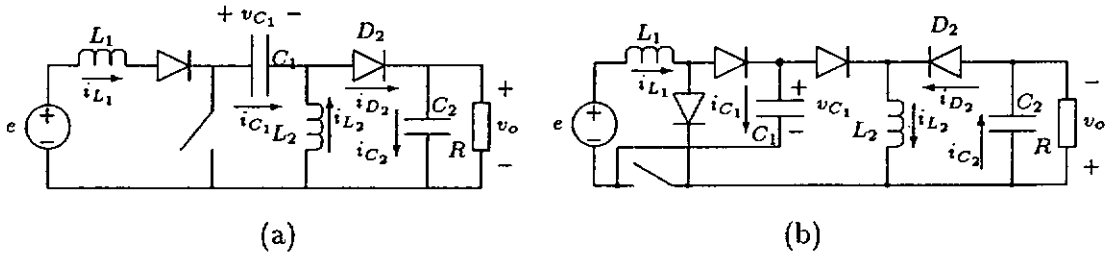

Figure 6.1: Non-isolated version of (a) BIFRED; (b) Boost-and-flyback converter

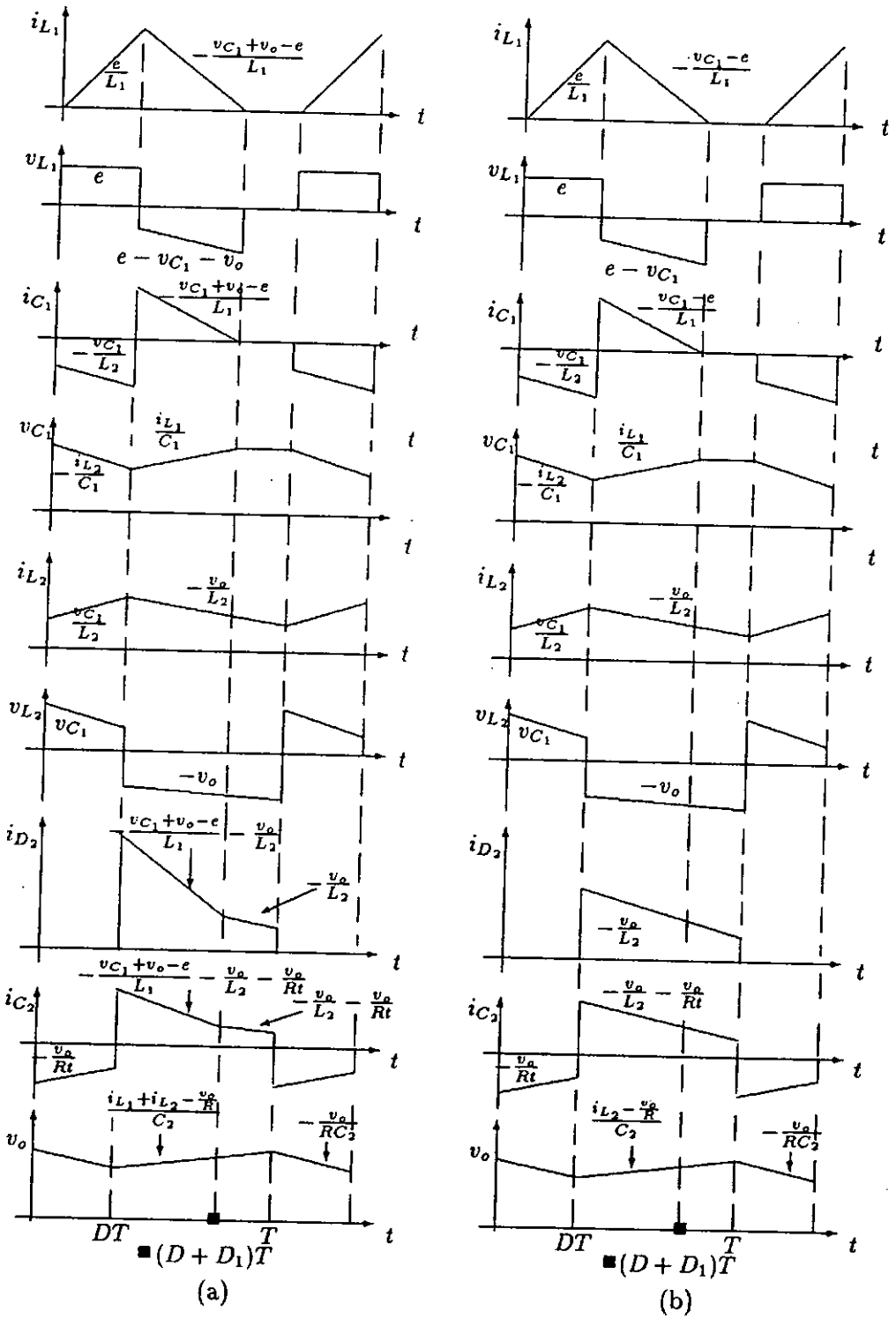

Figure 6.2: Switching waveforms of (a) BIFRED in DCM-CCM ; (b) Boost-and-flyback converter in DCM-CCM. (All the entries on the waveforms represent slopes except the inductor voltage waveforms.)

6.1 Dynamical Analysis of BIFRED Operating in DCM-CCM

The switching waveforms of BIFRED and boost-and-flyback converter operating in DCM-CCM are shown in Figs. 6.2(a) and (b) respectively. The main difference in the operations of the BIFRED and boost-and-flyback converter is observed in the discharging interval of L_1. During this interval, L_1 is subjected to $(v_o + v_{C_1}) - e$ in the case of BIFRED. In other words, the input and output ports form a loop, **unlike** any flyback converter, which causes the DCM inductor current of L_1 to discharge through both C_1 and $C_2 \| R$. This can be clearly observed by comparing the waveforms of i_{D_2} in Fig. 6.2(a) and 6.2(b). By averaging the inductor and capacitor current and voltage waveforms over a switching cycle [35, 36], the following equations are derived:

$$i_{L_1} = \frac{d^2 T \epsilon}{2L_1(1 - e/(v_{C_1} + v_o))} \tag{6.1}$$

$$C_1 \frac{dv_{C_1}}{dt} = i_{C_1} = \frac{d^2 T e}{2L_1((v_{C_1} + v_o)/e - 1)} - di_{L_2} \tag{6.2}$$

$$L_2 \frac{di_{L_2}}{dt} = v_{L_2} = dv_{C_1} - (1 - d)v_o \tag{6.3}$$

$$C_2 \frac{dv_o}{dt} = i_{C_2} = \frac{d^2 T e}{2L_1((v_{C_1} + v_o)/e - 1)} + (1 - d)i_{L_2} - \frac{v_o}{R} \tag{6.4}$$

which provide an analytical basis to derive the averaged model shown in Fig. 6.3. The small-signal parameters are found as

$$\begin{array}{llll} G_{11} = \frac{\partial i_{L_1}}{\partial e} & G_{12} = \frac{\partial i_{L_1}}{\partial v_{C_1}} & G_{14} = \frac{\partial i_{L_1}}{\partial v_o} & K_{13} = \frac{\partial i_{L_1}}{\partial i_{L_2}} \\ G_{21} = \frac{\partial i_{C_1}}{\partial e} & G_{22} = \frac{\partial i_{C_1}}{\partial v_{C_1}} & G_{24} = \frac{\partial i_{C_1}}{\partial v_o} & K_{23} = \frac{\partial i_{C_1}}{\partial e} \\ K_{31} = \frac{\partial v_{L_2}}{\partial e} & K_{32} = \frac{\partial v_{L_2}}{\partial v_{C_1}} & K_{34} = \frac{\partial v_{L_2}}{\partial v_o} & Z_{33} = \frac{\partial v_{L_2}}{\partial i_{L_2}} \\ G_{41} = \frac{\partial i_{C_2}}{\partial e} & G_{42} = \frac{\partial i_{C_2}}{\partial v_{C_1}} & G_{44} = \frac{\partial i_{C_2}}{\partial v_o} & K_{43} = \frac{\partial i_{C_2}}{\partial i_{L_2}} \\ J_1 = \frac{\partial i_{L_1}}{\partial d} & J_2 = \frac{\partial i_{C_1}}{\partial d} & J_4 = \frac{\partial i_{C_2}}{\partial d} & U_3 = \frac{\partial v_{L_2}}{\partial d} \end{array} \tag{6.5}$$

All the small-signal parameters are derived by using (6.5) and listed in Table 6.1.

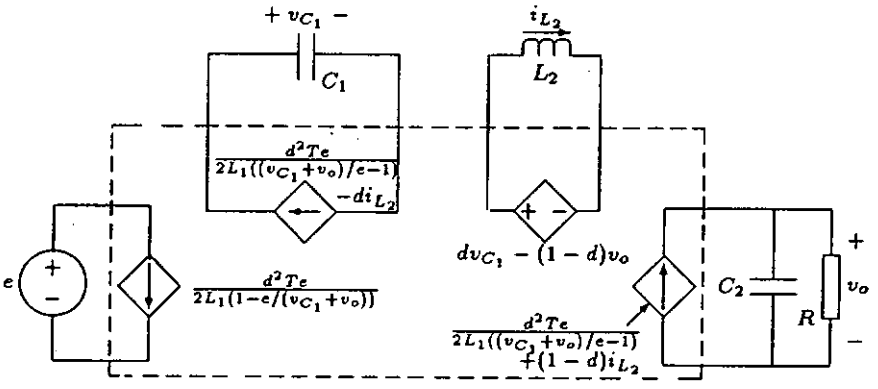

Figure 6.3: Averaged model of BIFRED operating in DCM-CCM

para-meters	BIFRED		Boost-and-flyback converter	
	DCM-CCM	DCM-DCM	DCM-CCM	DCM-DCM
G_{11}	$\left(\frac{M_1^3}{M_1-1}\right)\frac{1}{R_e}$	$\left(\frac{M_1^3}{M_1-1}\right)\frac{1}{R_e}$	$\left(\frac{M_{11}^3}{M_{11}-1}\right)\frac{1}{R_e}$	$\left(\frac{M_{11}^3}{M_{11}-1}\right)\frac{1}{R_e}$
G_{12}	$\left(\frac{M_1}{M_1-1}\right)\frac{1}{R_e}$	$\left(\frac{M_1}{M_1-1}\right)\frac{1}{R_e}$	$\left(\frac{M_{11}}{M_{11}-1}\right)\frac{1}{R_e}$	$\left(\frac{M_{11}}{M_{11}-1}\right)\frac{1}{R_e}$
G_{13}	-N/A-	$\left(\frac{M_1}{M_1-1}\right)\frac{1}{R_e}$	-N/A-	0
G_{14}	$\left(\frac{M_1}{M_1-1}\right)\frac{1}{R_e}$	-N/A-	0	-N/A-
J_1	$\frac{2V_{C_1}}{R_e}\sqrt{\frac{M_1}{k_e(M_1-1)}}$	$\frac{2V_{C_1}}{R_e}\sqrt{\frac{M_1}{K_e(M_1-1)}}$	$\frac{2V_{C_1}}{R_e}\sqrt{\frac{M_{11}}{K_e(M_{11}-1)}}$	$\frac{2V_{C_1}}{R_e}\sqrt{\frac{M_{11}}{K_e(M_{11}-1)}}$
K_{13}	0	-N/A-	0	-N/A-
G_{21}	$\frac{M_1(2M_1-1)}{(M_1-1)R_e}$	$\frac{M_1(2M_1-1)}{(M_1-1)R_e}$	$\frac{M_{11}(2M_{11}-1)}{(M_{11}-1)R_e}$	$\frac{M_{11}(2M_{11}-1)}{(M_{11}-1)R_e}$
G_{22}	$\left(\frac{M_1}{M_1-1}\right)\frac{1}{R_e}$	$\left(\frac{M_1}{M_1-1}\right)\frac{1}{R_e}+\frac{1}{R_e}$	$\left(\frac{M_{11}}{M_{11}-1}\right)\frac{1}{R_e}+\frac{M_{22}^2}{R}$	$\left(\frac{M_{11}}{M_{11}-1}\right)\frac{1}{R_e}+\frac{1}{R_e}$
G_{23}	-N/A-	$\left(\frac{M_1}{M_1-1}\right)\frac{1}{R_e}$	-N/A-	0
G_{24}	$\left(\frac{M_1}{M_1-1}\right)\frac{1}{R_e}$	-N/A-	0	-N/A-
J_2	$\frac{2V_{C_1}/R_e}{\sqrt{K_eM_1(M_1-1)}}-I_{L_2}$	$\frac{2V_{C_1}/R_e}{\sqrt{K_eM_1(M_1-1)}}-\frac{2V_O}{R\sqrt{K_2}}$	$\frac{2V_{C_1}/R_e}{\sqrt{K_eM_{11}(M_{11}-1)}}-I_{L_2}$	$\frac{2V_{C_1}/R_e}{\sqrt{K_eM_{11}(M_{11}-1)}}-\frac{2V_O}{R\sqrt{K_2}}$
K_{23}	D	-N/A-	D	-N/A-
G_{31}	-N/A-	$\frac{M_1(2M_1-1)}{(M_1-1)R_e}$	-N/A-	0
G_{32}	-N/A-	$\left(\frac{M_1}{M_1-1}\right)\frac{1}{R_e}-\frac{2M_{22}}{R}$	-N/A-	$\frac{2M_{22}}{R}$
G_{33}	-N/A-	$\left(\frac{M_1}{M_1-1}\right)\frac{1}{R_e}+\frac{1}{R}$	-N/A-	$\frac{1}{R}$
J_3	-N/A-	$\frac{2V_{C_1}/R_e}{\sqrt{K_eM_1(M_1-1)}}+\frac{2V_O}{RM_{22}\sqrt{K_2}}$	-N/A-	$\frac{2V_O}{RM_{22}\sqrt{K_2}}$
K_{32}	D	-N/A-	D	-N/A-
K_{34}	$1-D$	-N/A-	$1-D$	-N/A-
U_3	$V_{C_1}+V_O$	-N/A-	$V_{C_1}+V_O$	-N/A-
G_{41}	$\frac{M_1(2M_1-1)}{(M_1-1)R_e}$	-N/A-	0	-N/A-
G_{42}	$\left(\frac{M_1}{M_1-1}\right)\frac{1}{R_e}$	-N/A-	0	-N/A-
G_{44}	$\left(\frac{M_1}{M_1-1}\right)\frac{1}{R_e}$	-N/A-	0	-N/A-
J_4	$\frac{2V_{C_1}/R_e}{\sqrt{K_eM_1(M_1-1)}}-I_{L_2}$	-N/A-	I_{L_2}	-N/A-
K_{43}	$1-D$	-N/A-	$1-D$	-N/A-

Table 6.1: Small-signal parameters

For convenience the following new quantities are introduced:
$M_1 = (V_O + V_{C_1})/E, M_2 = V_O/(V_O + V_{C_1})$. $M_{22} = V_O/V_{C_1}$, $K_1 = 2L_1/RT, K_2 = 2L_2/RT$, $K_e = K_1 M_2^2$, $R_e = R/M_2^2, G_4 = G_{44} + 1/R$.

Using the standard procedure of small-signal linearization [35, 36] the small-signal model shown in Fig. 6.4 is derived. Based on this model, all transfer functions of interest can be derived.

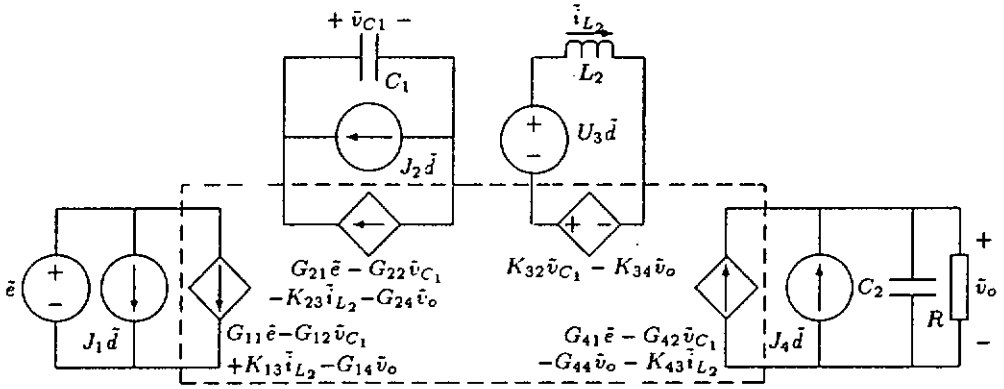

Figure 6.4: Small-signal model of BIFRED operating in DCM-CCM

6.1.1 Derivation of Small-signal Transfer Functions

6.1.1.A Duty-ratio-to-output Voltage Transfer Function

In deriving the $\tilde{v}_o/\tilde{d}$ transfer function, the input $\tilde{e}$ is set to zero. The circuit model thus reduces to the one shown in Fig. 6.5.

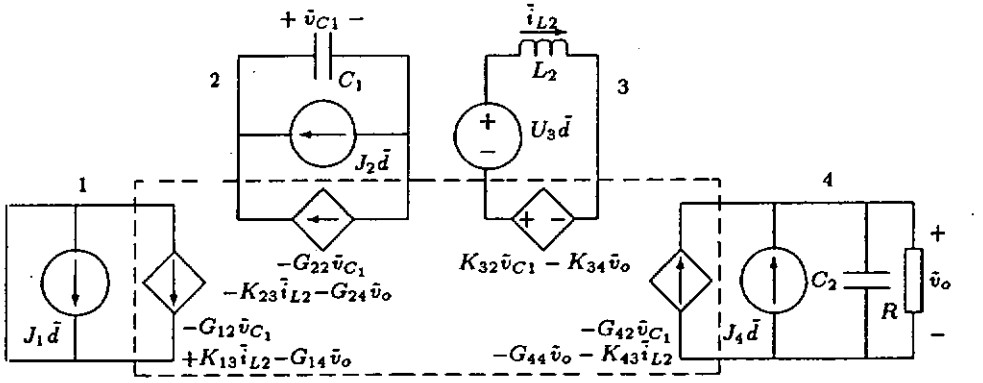

Figure 6.5: Model for calculation of $\tilde{v}_o/\tilde{d}$

Application of standard nodal analysis to the circuit shown in Fig. 6.5 gives

$$\begin{bmatrix} K_{34} & -K_{32} & sL_2 \\ G_{24} & G_{22} + sC_1 & K_{23} \\ G_{44} + sC_2 + \frac{1}{R} & G_{42} & -K_{43} \end{bmatrix} \begin{bmatrix} \tilde{v}_o \\ \tilde{v}_{C_1} \\ \tilde{i}_{L_2} \end{bmatrix} = \begin{bmatrix} N_1\tilde{d} \\ J_2\tilde{d} \\ J_4\tilde{d} \end{bmatrix} \tag{6.6}$$

Solving (6.6) for $\tilde{v}_o$ yields

$$\frac{\tilde{v}_o}{\tilde{d}} = \frac{s^2 L_2 C_1 J_4 + sC_1 N_1 K_{43} + G_{22} N_1 + J_2 K_{32}}{s^3 L_2 C_2 C_1 + s^2 L_2 C_1 G_{44} + sC_1 K_{34} K_{43} + s^2 L_2 G_{22} C_2 + sC_2 K_{32} K_{23} + \frac{sL_2 G_{22}}{R} + G_{44} + \frac{D^2}{R}} \tag{6.7}$$

6.1.1.B Output Impedance Transfer Function

In deriving the output impedance, the inputs $\tilde{e}$ and $\tilde{d}$ are set to zero. A test current source $\tilde{i}_s$ is injected to the output terminal as shown in Fig. 6.6.

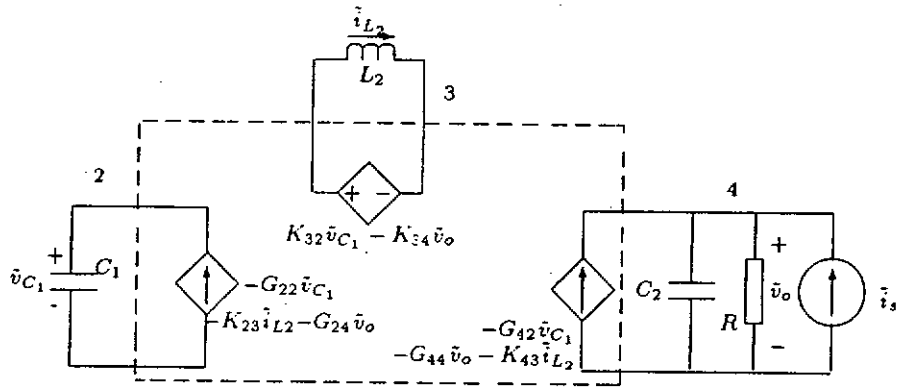

Figure 6.6: Model for calculation of Z_o

Application of nodal analysis to the circuit shown in Fig. 6.6 gives

$$\begin{bmatrix} K_{34} & -K_{32} & sL_2 \\ G_{24} & G_{22} + sC_1 & K_{23} \\ G_{44} + sC_2 + \frac{1}{R} & G_{42} & -K_{43} \end{bmatrix} \begin{bmatrix} \tilde{v}_o \\ \tilde{v}_{C_1} \\ \tilde{i}_{L_2} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ \tilde{i}_s \end{bmatrix} \tag{6.8}$$

Solving (6.8) for $\tilde{v}_o$ yields

$$Z_o = \frac{\tilde{v}_o}{\tilde{i}_s} = \frac{s^2 L_2 C_1 + sL_2 G_{22} + K_{23} K_{32}}{s^3 L_2 C_2 C_1 + s^2 L_2 C_1 G_{44} + sC_1 K_{34} K_{43} + s^2 L_2 G_{22} C_2 + sC_2 K_{32} K_{23} + \frac{sL_2 G_{22}}{R} + G_{44} + \frac{D^2}{R}} \tag{6.9}$$

6.1.1.C Line-to-output Voltage Transfer Function

In deriving the line-to-output voltage transfer function, the duty-ratio $\tilde{d}$ is set to zero, Thus, the circuit model reduces to the one shown in Fig. 6.7.

The linear equation resulting from the application of nodal analysis is

$$\begin{bmatrix} K_{34} & -K_{32} & sL_2 \\ G_{24} & G_{22} + sC_1 & K_{23} \\ G_{44} + sC_2 + \frac{1}{R} & G_{42} & -K_{43} \end{bmatrix} \begin{bmatrix} \tilde{v}_o \\ \tilde{v}_{C_1} \\ \tilde{i}_{L_2} \end{bmatrix} = \begin{bmatrix} 0 \\ G_{21}\tilde{e} \\ G_{41}\tilde{e} \end{bmatrix} \tag{6.10}$$

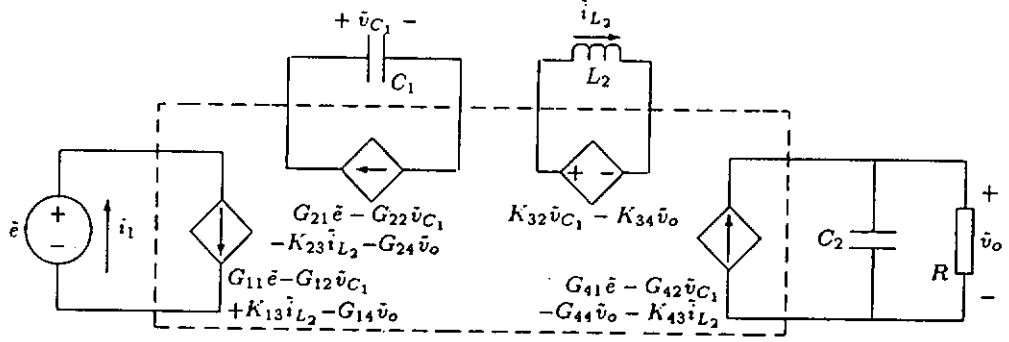

Figure 6.7: Model for calculation of $\tilde{v}_o/\tilde{e}$ and Z_i

Solving (6.10) for $\tilde{v}_o$ results in

$$\frac{\tilde{v}_o}{\tilde{e}} = \frac{G_{41}(s^2L_2C_1 + D)}{s^3L_2C_2C_1 + s^2L_2C_1G_{44} + sC_1K_{34}K_{43} + s^2L_2G_{22}C_2 + sC_2K_{32}K_{23} + \frac{sL_2G_{22}}{R} + G_{44} + \frac{D^2}{R}} \tag{6.11}$$

6.1.1.D Input Impedance Transfer Function

The same model shown in Fig. 6.7 is used again for the derivation of input impedance. The nodal equation is given by

$$\begin{bmatrix} 1 & G_{14} & G_{12} & 0 \\ 0 & K_{34} & -K_{32} & sL_2 \\ 0 & G_{24} & G_{22}+sC_1 & K_{23} \\ 0 & G_{44}+sC_2+\frac{1}{R} & G_{42} & -K_{43} \end{bmatrix} \begin{bmatrix} \tilde{i}_1 \\ \tilde{v}_o \\ \tilde{v}_{C_1} \\ \tilde{i}_{L_2} \end{bmatrix} = \begin{bmatrix} G_{11}\tilde{e} \\ 0 \\ G_{21}\tilde{e} \\ G_{41}\tilde{e} \end{bmatrix} \tag{6.12}$$

Solving (6.12) for $\tilde{i}_1$ yields

$$Z_i = \frac{\tilde{e}}{\tilde{i}_1} = \frac{sC_1\left(sL_2\left(sC_2 + G_{44} + \frac{1}{R} + K_{34}K_{43}\right)\right) + s^2L_2C_2G_{22} + sC_2K_{23}K_{32} + \frac{K_{23}K_{32}}{R}}{G_{11}\left[s^2L_2C_1(sC_2 + G_4 + K_{34}K_{43}) + s^2L_2C_2G_{22} + sC_2K_{23}K_{32} + \frac{K_{23}K_{32}}{R}\right] - G_{12}G_{21} - G_{12}G_{21}\left(sL_2\left(sC_1 + sC_2 + \frac{1}{R}\right) + 1\right)} \tag{6.13}$$

The transfer functions can also be derived by using the Extra Element Theorem (EET) [40]. To facilitate inspection, the poles and zeros for $\tilde{v}_o/\tilde{d}$, $\tilde{v}_o/\tilde{e}$ and Z_o are listed in Table 6.3.

6.1.2 Dynamical Analysis

The circuit shown in Fig. 6.4 is in general third-order, with L_1 being disqualified as a state variable because of its DCM operation. Specifically (except Z_i), there are two LHP zeros, $-s_{rz1}$ and $-s_{rz2}$, one real LHP pole $-s_{rp1}$ and one LHP complex pole pair $-s_{2,3}$ as shown in Table 6.3. The following results can be analytically derived from the transfer functions:

1. It can be observed from Table 6.3 that the pole, $-s_{rp1}$ and the zero, $-s_{rz1}$ of $\tilde{v}_o/\tilde{d}$ for $C_1 \gg (V_O/V_{C_1})^2C_2$ (note: $G_{22} \approx D^2/R$ for $M_1 \gg 1$) are close to each other but their

degree of proximity depends on the value of D since $s_{rz1} = (1-D)s_{rp1}$ for $M_1 \gg 1$. However, in the following subsection it is shown that pole-zero cancellation can occur in $\tilde{v}_o/\tilde{d}$ if $C_1 = (V_O/V_{C_1})C_2$ suggesting that C_1 cannot be very much greater than C_2 to achieve a fast response for any practical values of D.

Pole-zero Cancellation

Consider the characteristic equation of $\tilde{v}_o/\tilde{d}$ or $\tilde{v}_o/\tilde{e}$ or Z_o of BIFRED operating in DCM-CCM given in Table 6.2. Substituting for K_{23}, K_{32}, K_{34} and K_{43} from Table 6.1 in the characteristic equation results in

$$s^3 + \left(\frac{L_2C_1 + L_2C_2G_{22}R + L_2C_1G_{22}R}{L_2C_1C_2R}\right)s^2 + \left(\frac{D^2RC_2 + G_{22}L_2 + (1-D)^2RC_1}{L_2C_1C_2R}\right)s + \frac{D^2 + G_{44}R}{L_2C_1C_2R} = 0 \tag{6.14}$$

Using the approximate solution of the cubic equation of Appendix A, the roots of (6.14) can be written as

$$s_{rp1} \approx -\frac{D^2 + G_{44}R}{D^2C_2R + G_{22}L_2 + (1-D)^2C_1R} \tag{6.15}$$

$$s_{2,3} \approx -\frac{1}{2}\left(\frac{L_2C_1 + L_2C_2G_{22}R + L_2C_1G_{22}R}{L_2C_1C_2R} + s_{rp1}\right) \pm j\sqrt{\frac{D^2RC_2 + G_{22}L_2 + (1-D)^2RC_1}{L_2C_1C_2R}} \tag{6.16}$$

where s_{rp1} and $s_{2,3}$ are the real and complex roots of (6.14) respectively. Since $(1-D)^2RC_1 + D^2RC_2 \gg G_{22}L_2$ and for $(V_O + V_{C_1})/E \gg 1$, s_{rp1} can be written as

$$s_{rp1} \approx -\frac{2D^2}{D^2RC_2 + (1-D)^2RC_1} \tag{6.17}$$

Now consider the numerator of $\tilde{v}_o/\tilde{d}$ of BIFRED (see Table 6.2). For $(V_O + V_{C_1})/E \gg 1$. The numerator can be simplified as

$$s^2 + s\left(\frac{1-D}{D}\right)\frac{R}{L_2} + \frac{2D}{L_2C_1} = 0 \tag{6.18}$$

If $((1-D)/D)^2(R/L_2)^2 \gg 2D/L_2C_1$, then using the results of Section A.2 of Appendix A, the LHP zeros of (6.18) are found to be

$$-s_{rz1} \approx \frac{2D^2}{(1-D)RC_1} \tag{6.19}$$

$$-s_{rz2} \approx \left(\frac{1-D}{D}\right)\frac{R}{L_2} \tag{6.20}$$

Analytically, the condition for pole-zero cancellation can be found by equating s_{rp1} and s_{rz1}. Then, solving for C_1 or C_2 gives $C_1 \approx C_2\left(\frac{D}{1-D}\right)$. When $(V_O + V_{C_1})/E \gg 1$ and $C_1 \approx C_2\left(\frac{D}{1-D}\right)$, s_{rp1} and s_{rz1} get cancelled, and $\tilde{v}_o/\tilde{d}$ reduces to a simple second-order

minimum phase function

$$\frac{\tilde{v}_o}{\tilde{d}} \approx \frac{V_{C_1}}{(1-D)^2}\left(\frac{1+\frac{s}{s_{rz2}}}{1+\frac{1}{Q}\left(\frac{s}{\omega_o}\right)+\left(\frac{s}{\omega_o}\right)^2}\right) \tag{6.21}$$

where $Q = R_o/R$, $R_o = \frac{1}{1-D}\sqrt{\frac{L_2}{C_2}}$ and $\omega_o = (1-D)/\sqrt{L_2C_2}$. It is interesting to observe that the DC value and the characteristic polynomial of (6.21) is the same as that of the $\tilde{v}_o/\tilde{d}$ of a CCM flyback converter [41].

2. Though the output stage is a flyback converter, the $\tilde{v}_o/\tilde{d}$ has its zeros in LHP, i.e., a *minimum phase* system as seen from Table 6.3.

3. The DC output impedance ($\approx R/2$ for $M_1 \gg 1$) is undesirably high, as observed from Table 6.2. Thus, the output voltage is relatively sensitive to load-current change. This situation is different from a CCM flyback converter. Also, as observed from Table 6.2, there is a complex zero pair at $G_{22}/2C_1 \pm jD/\sqrt{L_2C_1}$, causing a "glitch" in the frequency response of Z_o. However, for $C_1 \ll (V_O/V_{C_1})^2C_2$, the complex poles and zeros cancel out ("glitch" gets eliminated) resulting in a single-pole response (see Table 6.3).

4. Unlike any other basic DC-DC converter, the $\tilde{v}_o/\tilde{e}$ transfer function, has a complex zero pair at $\sqrt{D/L_2C_1}$ causing a "glitch" in its frequency response.

5. When $M_1 \gg 1$, the input impedance Z_i is devoid of any dynamics. This property is exploited for PFC applications as has been well understood [17]. When $(V_O + V_{C_1})/E \gg 1$, Z_i in Table 6.2 can be simplified to $2L_1/D^2T$ which is consistent with the value found directly from the average model shown in Fig. 6.3.

6.1.2.A PSPICE Verifications

In this subsection, PSPICE simulations of the frequency responses of the transfer functions based on the small-signal models are reported. The PSPICE netlists of all the small-signal models which are used to generate the frequency responses are given in Appendix B. The circuit parameters used for simulation are $L_1 = 0.08$mH, $L_2 = 0.5$mH, $D = 0.3$, $R = 100\Omega$, $f_s = 100$kHz, $E = 160$V. A series of frequency response curves corresponding to different relative sizes of C_1 and C_2 will be plotted, from which the following observations are made:

1. Fig. 6.8 shows the frequency response of $\tilde{v}_o/\tilde{d}$ which shows the phase response extending from 0^0 to -90^0 since both the zeros are located in the LHP as predicted in the analysis. The magnitude response plot of Fig. 6.8 also shows the corner frequency due to the complex LHP pole pair, $-s_{2,3}$, at $(1-D)/2\pi\sqrt{L_2C_2}$ for $C_1 \gg M_{22}^2C_2$. Fig. 6.8 also shows the change in response for different relative sizes of C_1 and C_2.

2. The magnitude and phase responses of Z_o are shown in Fig. 6.12. As predicted in Table 6.2, the phase response rises from -90^0 to $+90^0$ due to the LHP complex zero pair at $D/2\pi\sqrt{L_2C_1}$, and falls back to -90^0 due to the LHP complex pole pair, $-s_{2,3}$ at $(1-D)/2\pi\sqrt{L_2C_2}$ for $C_1 \gg M_{22}^2C_2$. Fig. 6.12 also confirms the prediction of the elimination of "glitch" for $C_1 \ll M_{22}^2C_2$ giving a single-pole response.

3. Fig. 6.10 shows the magnitude and phase responses of $\tilde{v}_o/\tilde{e}$. The presence of the complex zero, (see Table 6.2) is verified by the phase response rising from -90^0 to $+90^0$ due to the complex zero pair at $(1/2\pi)\sqrt{D/L_2C_1}$ and falls back to -90^0 due to the LHP complex pole pair $-s_{2,3}$ at $(1-D)/2\pi\sqrt{L_2C_2}$ for $C_1 \gg M_{22}^2C_2$ as predicted in Table 6.3.

4. Fig. 6.16 verifies that input impedance is approximately equal to $2L_1/D^2T$ when $(V_O + V_{C_1})/E \gg 1$, and that the phase shift is negligible. Thus, the input of the converter emulates a resistor.

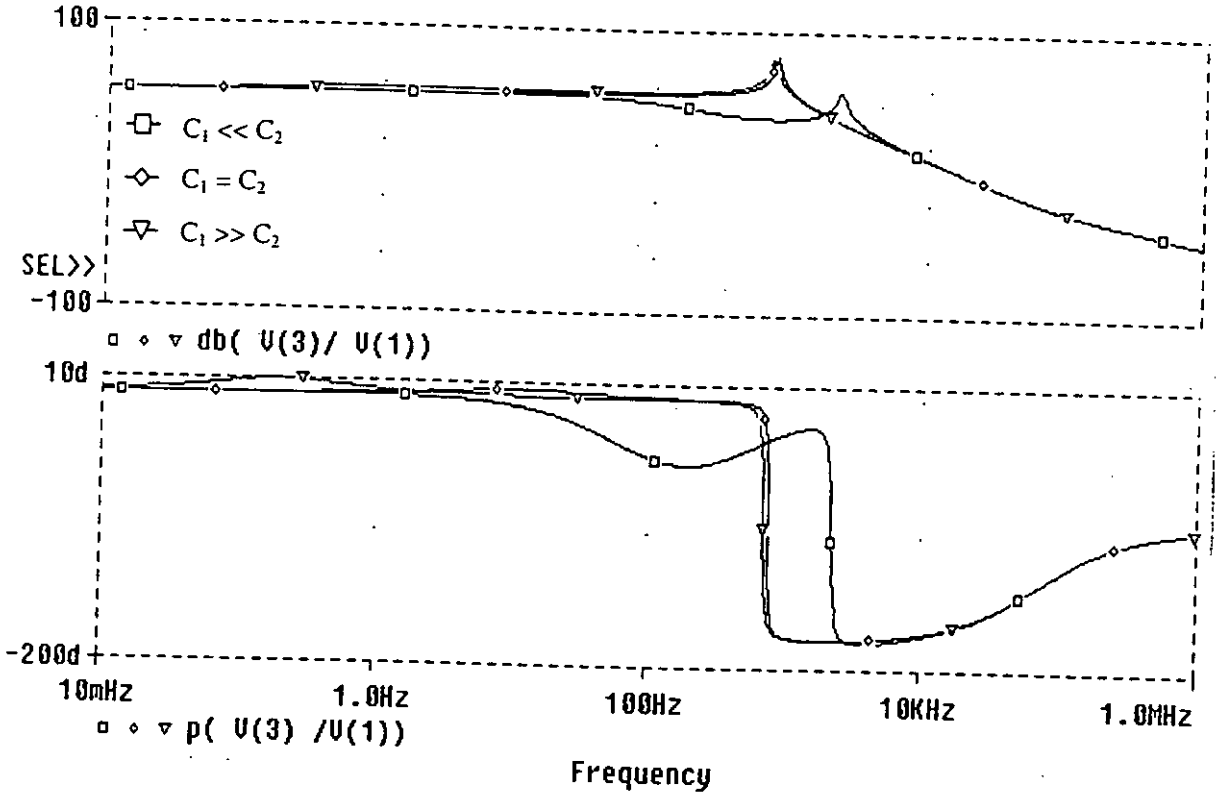

Figure 6.8: $\tilde{d}$-to-$\tilde{v}_o$ frequency responses of **BIFRED** operating in DCM-CCM for different relative sizes of capacitances. Upper plot: magnitude (dB); Lower plot: phase (deg)

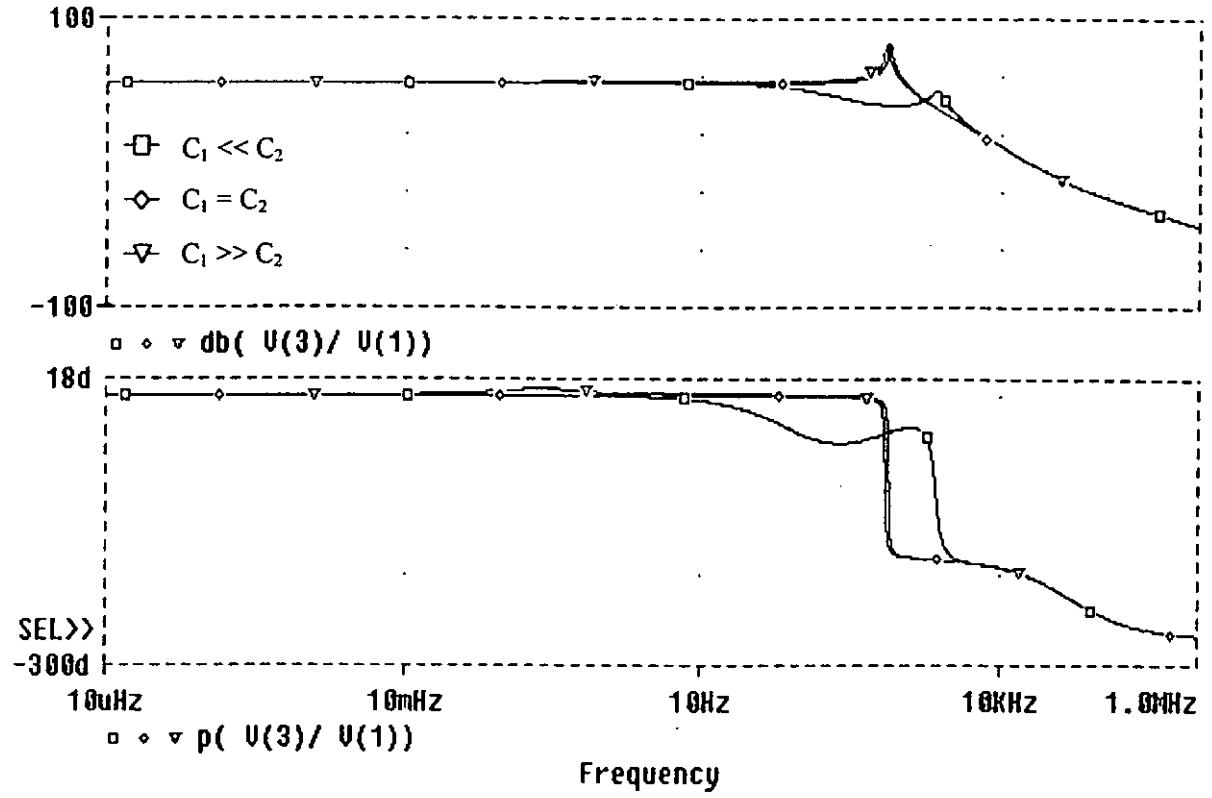

Figure 6.9: $\tilde{d}$-to-$\tilde{v}_o$ frequency responses of **boost-and-flyback converter** operating in DCM-CCM for different relative sizes of capacitances. Upper plot: magnitude (dB); Lower plot: phase (deg)

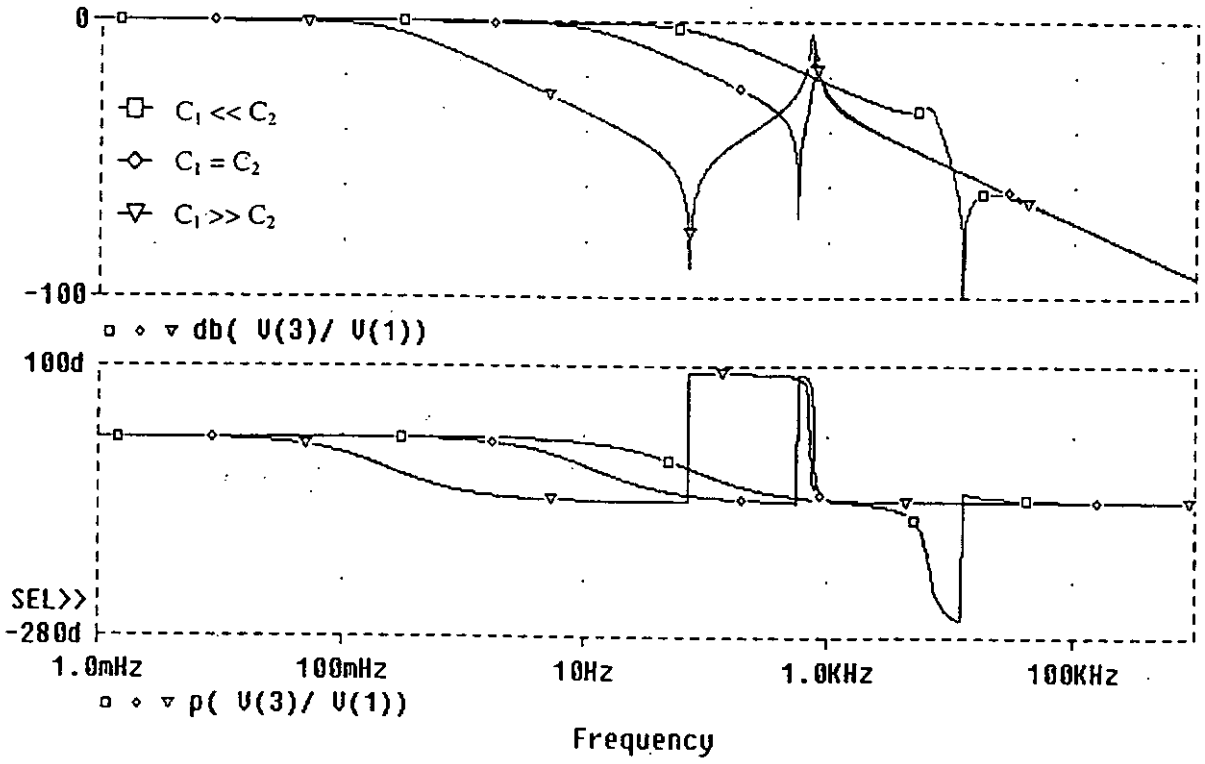

Figure 6.10: $\tilde{e}$-to-$\tilde{v}_o$ frequency responses of **BIFRED** operating in DCM-CCM for different relative sizes of capacitances. Upper plot: magnitude (dB); Lower plot: phase (deg)

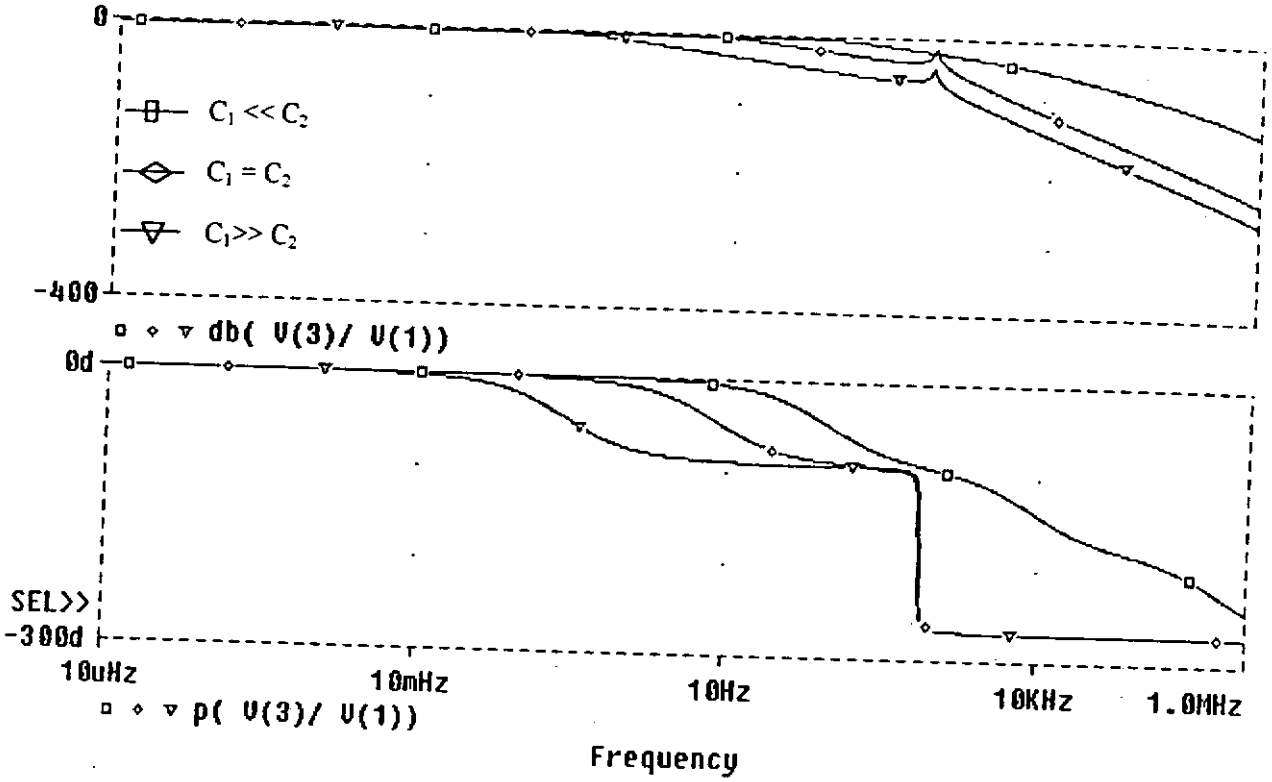

Figure 6.11: $\hat{e}$-to-$\hat{v}_o$ frequency responses of **boost-and-flyback converter** operating in DCM-CCM for different relative sizes of capacitances. Upper plot: magnitude (dB); Lower plot: phase (deg)

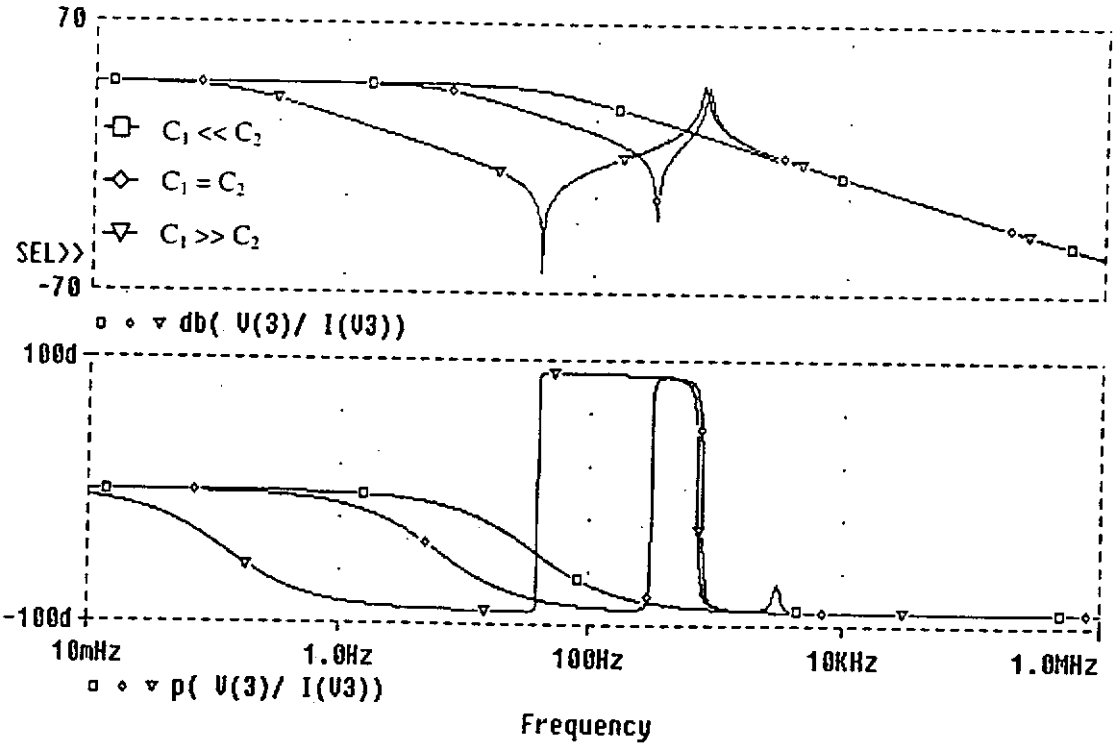

Figure 6.12: Z_o frequency responses of **BIFRED** operating in DCM-CCM for different relative sizes of capacitances. Upper plot: magnitude (dB); Lower plot: phase (deg)

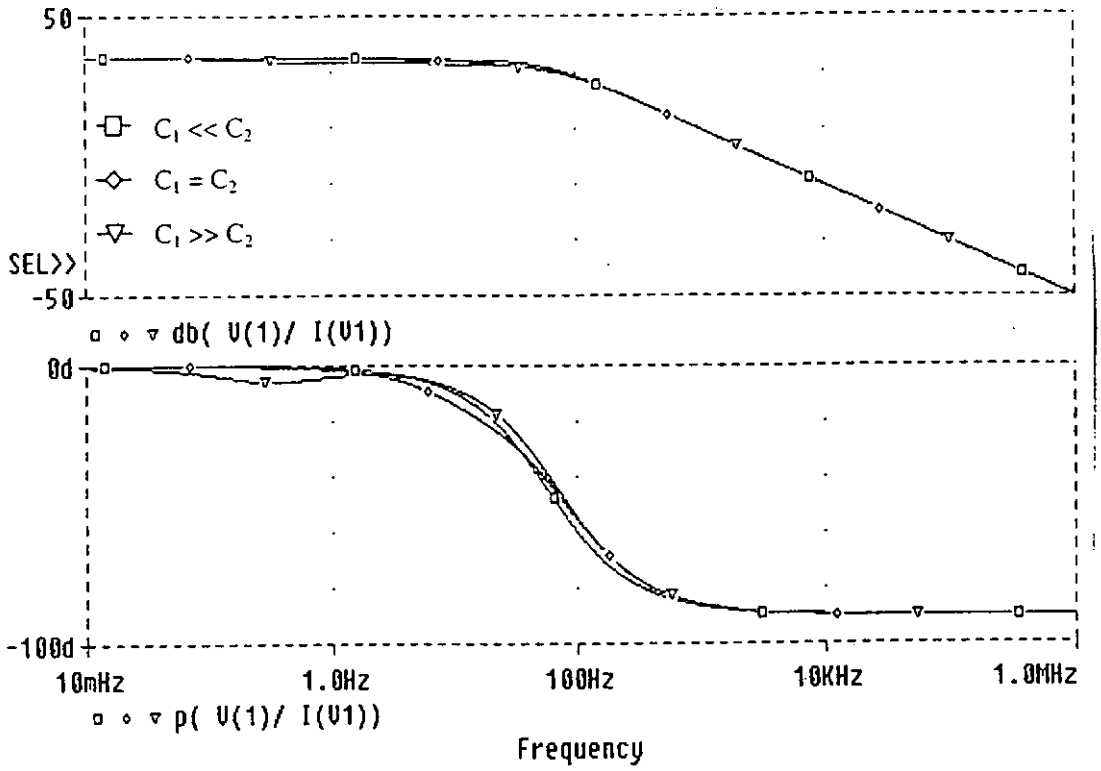

Figure 6.13: Z_o frequency responses of **BIFRED** operating in DCM-DCM for different relative sizes of capacitances. Upper plot: magnitude (dB); Lower plot: phase (deg)

6.2 Dynamical Analysis of Boost-and-flyback Converter in DCM-CCM

The switching waveforms of the boost-and-flyback converter operating in DCM-CCM are shown in Fig. 6.2(b). By averaging the inductor and capacitor current and voltage waveforms over a switching cycle [35, 36], the following equations are derived:

$$i_{L_1} = \frac{d^2Te}{2L_1(1-e/v_{C_1})} \tag{6.22}$$

$$C_1\frac{dv_{C_1}}{dt} = i_{C_1} = \frac{d^2Te}{2L_1(v_{C_1}/e-1)} - di_{L_2} \tag{6.23}$$

$$L_2\frac{di_{L_2}}{dt} = v_{L_2} = dv_{C_1} - (1-d)v_o \tag{6.24}$$

$$C_2\frac{dv_o}{dt} = i_{C_2} = (1-d)i_{L_2} - \frac{v_o}{R} \tag{6.25}$$

which provide an analytical basis to derive the averaged model shown in Fig. 6.14.

6.2.1 Derivation of Small-signal Transfer Functions

Small-signal parameters are derived using (6.5) and listed in Table 6.1. Again by applying the procedure of small-signal linearization [35, 36], the small-signal model is derived as shown in Fig. 6.15 which is used in the derivation of small-signal transfer functions.

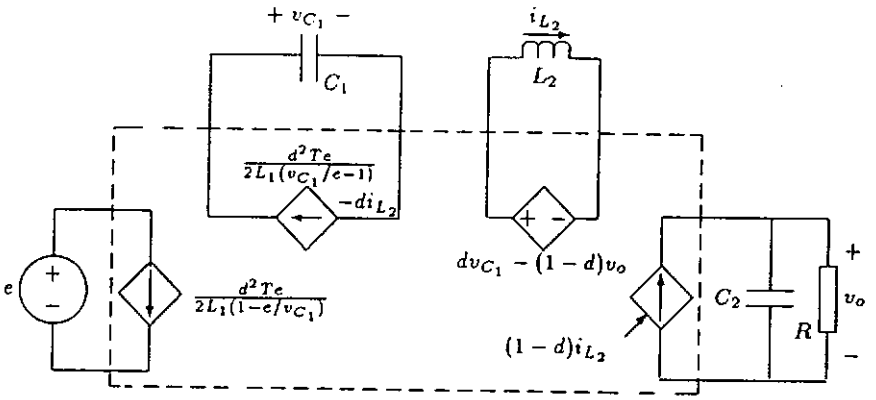

Figure 6.14: Averaged model of boost-and-flyback converter operating in DCM-CCM

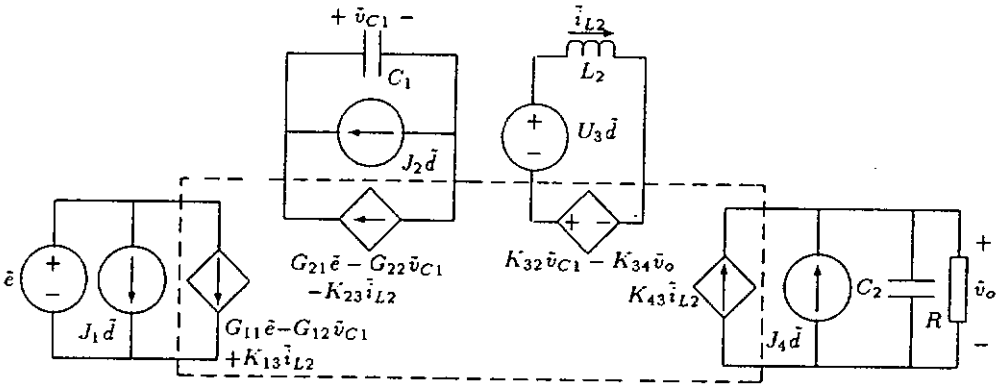

Figure 6.15: Small-signal model of boost-and-flyback converter operating in DCM-CCM

The small-signal transfer functions are tabulated for both operating modes in Table 6.4. To facilitate inspection, the poles and zeros of $\tilde{v}_o/\tilde{d}$, $\tilde{v}_o/\tilde{e}$ and Z_o are listed in Table 6.5. For convenience, the following new quantities are introduced: $M_{11} = V_{C_1}/E$, $R_e = R/M_{22}^2$, $K_e = K_1 M_{22}^2$

The associated models of small-signal transfer functions of BIFRED are used in the derivation of the small-signal transfer functions of boost-and-flyback converter.

6.2.1.A Duty-ratio-to-output Voltage Transfer Function

The model shown in Fig. 6.5 is again used here. Applying nodal analysis to the circuit shown in Fig. 6.5 gives

$$\begin{bmatrix} K_{34} & -K_{32} & sL_2 \\ 0 & G_{22}+sC_1 & K_{23} \\ sC_2+\frac{1}{R} & 0 & -K_{43} \end{bmatrix} \begin{bmatrix} \tilde{v}_o \\ \tilde{v}_{C_1} \\ \tilde{i}_{L_2} \end{bmatrix} = \begin{bmatrix} N_1\tilde{d} \\ J_2\tilde{d} \\ -J_4\tilde{d} \end{bmatrix} \tag{6.26}$$

Solving (6.26) for $\tilde{v}_o$ yields

$$\frac{\tilde{v}_o}{\tilde{d}} = \frac{-s^2 L_2 C_1 J_4 + sC_1 N_1 K_{43} - sG_{22} J_4 L_2 + G_{22} N_1 K_{43} + J_2 K_{32} K_{43} - J_4 K_{32} K_{23}}{\left(s^2 L_2 C_2 + \frac{sL_2}{R} + K_{34} K_{43}\right)(sC_1 + G_{22}) + sC_2 K_{32} K_{23} + \frac{K_{32} K_{23}}{R}} \tag{6.27}$$

6.2.1.B Output Impedance Transfer Function

The model shown in Fig. 6.6 is again used here. The nodal admittance matrix of the circuit shown in Fig. 6.6 is given by

$$\begin{bmatrix} K_{34} & -K_{32} & sL_2 \\ 0 & G_{22} + sC_1 & K_{23} \\ sC_2 + \frac{1}{R} & 0 & -K_{43} \end{bmatrix} \begin{bmatrix} \tilde{v}_o \\ \tilde{v}_{C_1} \\ \tilde{i}_{L_2} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ \tilde{i}_s \end{bmatrix} \tag{6.28}$$

Solving (6.28) for $\tilde{v}_o$ and simplifying yields

$$Z_o = \frac{\tilde{v}_o}{\tilde{i}_s} = \frac{s^2 L_2 C_1 + sL_2 G_{22} + K_{32} K_{23}}{\left(s^2 L_2 C_2 + \frac{sL_2}{R} + K_{34} K_{43}\right)(sC_1 + G_{22}) + sC_2 K_{32} K_{23} + \frac{K_{32} K_{23}}{R}} \tag{6.29}$$

6.2.1.C Line-to-output Voltage Transfer Function

Application of nodal analysis to the circuit shown in Fig. 6.7 gives

$$\begin{bmatrix} K_{34} & -K_{32} & sL_2 \\ 0 & G_{22} + sC_1 & K_{23} \\ sC_2 + \frac{1}{R} & 0 & -K_{43} \end{bmatrix} \begin{bmatrix} \tilde{v}_o \\ \tilde{v}_{C_1} \\ \tilde{i}_{L_2} \end{bmatrix} = \begin{bmatrix} 0 \\ G_{21}\tilde{e} \\ 0 \end{bmatrix} \tag{6.30}$$

Solving (6.30) for $\tilde{v}_o$ and simplifying yields

$$\frac{\tilde{v}_o}{\tilde{e}} = \frac{G_{21} D(1-D)}{\left(s^2 L_2 C_2 + \frac{sL_2}{R} + K_{34} K_{43}\right)(sC_1 + G_{22}) + sC_2 K_{32} K_{23} + \frac{K_{32} K_{23}}{R}} \tag{6.31}$$

6.2.1.D Input Impedance Transfer Function

The nodal matrix of the circuit shown in Fig. 6.7 is

$$\begin{bmatrix} 1 & 0 & -G_{12} & 0 \\ 0 & K_{34} & -K_{32} & sL_2 \\ 0 & 0 & G_{22} + sC_1 & K_{23} \\ 0 & sC_2 + \frac{1}{R} & 0 & -K_{43} \end{bmatrix} \begin{bmatrix} \tilde{i}_1 \\ \tilde{v}_o \\ \tilde{v}_{C_1} \\ \tilde{i}_{L_2} \end{bmatrix} = \begin{bmatrix} G_{11}\tilde{e} \\ 0 \\ G_{21}\tilde{e} \\ 0 \end{bmatrix} \tag{6.32}$$

Solving (6.32) for $\tilde{i}_1$ and simplifying yields

$$Z_i = \frac{\tilde{e}}{\tilde{i}_1} = \frac{\left(s^2 L_2 C_2 + \frac{sL_2}{R} + K_{34} K_{43}\right)(sC_1 + G_{22}) + sC_2 K_{32} K_{23} + \frac{K_{32} K_{23}}{R}}{G_{11}\left[\left(s^2 L_2 C_2 + \frac{sL_2}{R} + K_{34} K_{43}\right)(sC_1 + G_{22}) + sC_2 K_{32} K_{23} + \frac{K_{32} K_{23}}{R}\right] - G_{12} G_{21}\left(s^2 L_2 C_2 + \frac{sL_2}{R} + K_{34} K_{43}\right)} \tag{6.33}$$

All the transfer functions are rearranged and listed in Table 6.4 for reader's convenience.

6.2.2 Dynamical Analysis

The model shown in Fig. 6.15 is of third-order, with L_1 being disqualified as a state variable because of its DCM operation. They all have the same characteristics as BIFRED operating in DCM-CCM except for two important differences:

1. As in flyback converters, the zero $-s_{rz2}$ of $\tilde{v}_o/\tilde{d}$ is situated in the RHP, i.e., a *non-minimum phase* system as seen from Table 6.5. This is true even if pole-zero cancellation occurs because $-s_{rz1}$ and $-s_{rp1}$ get cancelled and $-s_{rz2}$ still remains which is shown as follows:

Pole-zero Cancellation

Consider the characteristic equation of $\tilde{v}_o/\tilde{d}$ or $\tilde{v}_o/\tilde{e}$ or Z_o of the boost-and-flyback converter operating in DCM-CCM given in Table 6.4 and substituting for K_{23}, K_{32}, K_{34} and K_{43} from Table 6.1 gives

$$s^3 + \left(\frac{L_2C_1 + L_2C_2G_{22}R}{L_2C_1C_2R}\right)s^2 + \left(\frac{D^2RC_2 + G_{22}L_2 + (1-D)^2RC_1}{L_2C_1C_2R}\right)s + \frac{D^2 + (1-D)^2G_{22}R}{L_2C_1C_2R} = 0 \tag{6.34}$$

Using the approximate solution of the cubic equation of Appendix A, the roots of (6.34) can be written as

$$s_{rp1} \approx -\frac{D^2 + (1-D)^2G_{22}R}{D^2RC_2 + G_{22}L_2 + (1-D)^2RC_1} \tag{6.35}$$

$$s_{2,3} \approx -\frac{1}{2}\left(\frac{L_2C_1 + L_2C_2G_{22}R}{L_2C_1C_2R} + s_{rp1}\right) \pm j\sqrt{\frac{D^2RC_2 + G_{22}L_2 + (1-D)^2RC_1}{L_2C_1C_2R}} \tag{6.36}$$

where s_{rp1} and $s_{2,3}$ are the real and complex roots of (6.14) respectively. Since $(1-D)^2RC_1 + D^2RC_2 \gg G_{22}L_2$ and for $(V_O + V_{C_1})/E \gg 1$, s_{rp1} can be written as

$$s_{rp1} \approx -\frac{2D^2}{D^2RC_2 + (1-D)^2RC_1} \tag{6.37}$$

Now consider the numerator of $\tilde{v}_o/\tilde{d}$ of the boost-and-flyback converter given in Table 6.4. For $V_{C_1}/E \gg 1$, it can be simplified as

$$s^2 - s\frac{(1-D)^2}{D}\frac{R}{L_2} + \left(\frac{D}{1-D}\right)^2\frac{s}{RC_1} + \frac{2D(1-D)}{L_2C_1} = 0 \tag{6.38}$$

For $\frac{(1-D)^2}{D}\frac{R}{L_2} \gg \left(\frac{D}{1-D}\right)^2\frac{1}{RC_1}$ and $((1-D^2)/D)^2(R/L_2)^2 \gg 2D(1-D)/L_2C_1$, the zeros of (6.38) are found to be

$$-s_{rz1} \approx -\frac{2D^2}{(1-D)RC_1} \tag{6.39}$$

$$-s_{rz2} \approx \left(\frac{(1-D)^2}{D}\right)\frac{R}{L_2} \tag{6.40}$$

based on the results of Section A.2 of Appendix A. Analytically, the condition for pole-zero cancellation can be found by equating s_{rp1} and s_{rz1}. Then solving for C_1 or C_2 results in $C_1 \approx C_2\left(\frac{D}{1-D}\right)$. When $V_{C_1}/E \gg 1$ and $C_1 \approx C_2\left(\frac{D}{1-D}\right)$, s_{rp1} and s_{rz1} get cancelled, and $\tilde{v}_o/\tilde{d}$ reduces to a simple second-order *non-minimum phase* function

$$\frac{\tilde{v}_o}{\tilde{d}} \approx \frac{V_{C_1}}{(1-D)^2}\left(\frac{1-\frac{s}{s_{rz2}}}{1+\frac{1}{Q}\left(\frac{s}{\omega_o}\right)+\left(\frac{s}{\omega_o}\right)^2}\right) \tag{6.41}$$

where $Q = R_o/R$, $R_o = \frac{1}{1-D}\sqrt{\frac{L_2}{C_2}}$ and $\omega_o = (1-D)/\sqrt{L_2C_2}$. It is interesting to observe that (6.41) is the same as the $\tilde{v}_o/\tilde{d}$ of a CCM flyback converter [41].

2. As in other basic DC-DC converters, $\tilde{v}_o/\tilde{e}$ has no zeros.

PSPICE Verifications

In this subsection, PSPICE simulations of the frequency responses based on the small-signal models are reported. The PSPICE netlists of all the small-signal models which are used to generate the frequency responses are given in Appendix B. The circuit parameters used for simulation are $L_1 = 0.08$mH, $L_2 = 0.1$mH. $D = 0.3$, $R = 100\Omega$, $f_s = 100$kHz, $E = 160$V. Frequency response curves corresponding to different relative sizes of C_1 and C_2 will be plotted, from which the following observations are made: All the characteristics of transfer functions are similar to BIFRED operating in DCM-CCM except for the two important differences as predicted earlier in this subsection are verified here,

1. Fig. 6.9 confirms the prediction of RHP and LHP zeros in $\tilde{v}_o/\tilde{d}$. Thus, its phase response extends from 0^0 to -270^0.

2. Fig. 6.11 confirms the absence of any zeros in $\tilde{v}_o/\tilde{e}$. Thus, its phase response also extends from 0^0 to -270^0.

Boost Integrated with Flyback Rectifier DC-DC converter (BIFRED)		
Transfer function	DCM-CCM	DCM-DCM
$\frac{\hat{v}_o}{\hat{d}}$	$\frac{R(G_{22}U_3+J_2K_{32})\left(\frac{s^2L_2C_1J_4}{(G_{22}U_3+J_2K_{32})}+\frac{sC_1U_3K_{43}}{(G_{22}U_3+J_2K_{32})}+1\right)}{sRC_1K_{34}K_{43}\left[\frac{s^2L_2C_2}{K_{34}K_{43}}+\frac{sC_2G_4}{K_{34}K_{43}}+1\right]+RG_{22}(sL_2G_4+1)+K_{23}K_{32}(sRC_2+1)}$	$\frac{\left(\frac{J_3}{G_3}\right)\left[1+\frac{sC_1}{G_{22}}-\frac{G_{32}J_2}{J_3G_{22}}\right]}{\left(1+\frac{sC_2}{G_3}\right)\left(1+\frac{sC_1}{G_{22}}\right)-\frac{G_{23}G_{32}}{G_{22}G_3}}$
Z_o	$\frac{RK_{23}K_{32}\left(\frac{s^2L_2C_1}{K_{23}K_{32}}+\frac{sL_2G_{32}}{K_{23}K_{32}}+1\right)}{sRC_1K_{34}K_{43}\left[\frac{s^2L_2C_2}{K_{34}K_{43}}+\frac{sC_2G_4}{K_{34}K_{43}}+1\right]+RG_{22}(sL_2G_4+1)+K_{23}K_{32}(sRC_2+1)}$	$\frac{\left(\frac{1}{G_3}\right)\left[1+\frac{sC_1}{G_{22}}\right]}{\left(1+\frac{sC_2}{G_3}\right)\left(1+\frac{sC_1}{G_{22}}\right)-\frac{G_{23}G_{32}}{G_{22}G_3}}$
$\frac{\hat{v}_o}{\hat{e}}$	$\frac{RDG_{41}\left(\frac{s^2L_2C_1}{D}+1\right)}{sRC_1K_{34}K_{43}\left[\frac{s^2L_2C_2}{K_{34}K_{43}}+\frac{sC_2G_4}{K_{34}K_{43}}+1\right]+RG_{22}(sL_2G_4+1)+K_{23}K_{32}(sRC_2+1)}$	$\frac{\frac{G_{31}}{G_3}\left[1+\frac{sC_1}{G_{22}}-\frac{G_{32}G_{21}}{G_{31}G_{22}}\right]}{\left(1+\frac{sC_2}{G_3}\right)\left(1+\frac{sC_1}{G_{22}}\right)-\frac{G_{23}G_{32}}{G_{22}G_3}}$
Z_i DCM-CCM	$\frac{sRC_1K_{34}K_{43}\left[\frac{s^2L_2C_2}{K_{34}K_{43}}+\frac{sC_2G_4}{K_{34}K_{43}}+1\right]+RG_{22}(sL_2G_4+1)+K_{23}K_{32}(sRC_2+1)}{G_{11}\left\{sRC_1K_{34}K_{43}\left[\frac{s^2L_2C_2}{K_{34}K_{43}}+\frac{sC_2G_4}{K_{34}K_{43}}+1\right]+RG_{22}(sL_2G_4+1)+K_{23}K_{32}(sRC_2+1)\right\}-RG_{12}G_{21}\left[s^2(L_2C_1+L_2C_2)+\frac{sL_2}{R}+1\right]}$	
Z_i DCM-DCM	$\frac{\left(1+\frac{sC_2}{G_3}\right)\left(1+\frac{sC_1}{G_{22}}\right)-\frac{G_{23}G_{32}}{G_3G_{22}}}{G_{11}\left\{\left(1+\frac{sC_2}{G_3}\right)\left(1+\frac{sC_1}{G_{22}}\right)-\frac{G_{23}G_{32}}{G_3G_{22}}\right\}+\frac{G_{13}G_{31}}{G_3G_{22}}(sC_1+sC_2-G_3+G_{23}+G_{32})}$	

Table 6.2: Small-signal transfer functions

Boost Integrated with Flyback Rectifier DC-DC converter (BIFRED)				
Poles & zeros	$C_1 \gg M_{22}^2C_2$		$C_1 \ll M_{22}^2C_2$	
	DCM-CCM	DCM-DCM	DCM-CCM	DCM-DCM
$-s_{rp1}$ Real Pole	$\frac{D^2}{RC_1(1-D)^2}+\frac{G_{22}}{C_1(1-D)^2}$	$\frac{G_{22}}{C_1}\left(1-\frac{G_{23}G_{32}}{G_3G_{22}}\right)$	$\frac{1}{RC_2}+\frac{G_{22}}{D^2RC_2}$	$\frac{G_3}{C_2}\left(1-\frac{G_{23}G_{32}}{G_3G_{22}}\right)$
$-s_{rp2}$ Real Pole	-N/A-	$\frac{G_3}{C_2}$	-N/A-	$\frac{G_{22}}{C_1}$
$-s_{2,3}$ Complex Poles	$\frac{1}{2RC_2}\pm j\frac{1-D}{\sqrt{L_2C_2}}$	-N/A-	$\frac{G_{22}}{2C_1}\pm j\frac{D}{\sqrt{L_2C_1}}$	-N/A-
$-s_{rz1}$ Real zero of $\hat{v}_o/\hat{d}$	$\frac{2D^2}{(1-D)RC_1}$	$\frac{G_{22}}{C_1}\left(1-\frac{G_{32}J_2}{J_3G_{22}}\right)$	$\frac{2D^2}{(1-D)RC_1}$	$\frac{G_{22}}{C_1}\left(1-\frac{G_{32}J_2}{J_3G_{22}}\right)$
$-s_{rz2}$ Real zero of $\hat{v}_o/\hat{d}$	$\left(\frac{1-D}{D}\right)\frac{R}{L_2}$	-N/A-	$\left(\frac{1-D}{D}\right)\frac{R}{L_2}$	-N/A-
$-s_z$ zero of $\hat{v}_o/\hat{d}$	$\left(\frac{1-D}{2D}\right)\frac{R}{L_2}\pm j\sqrt{\frac{2D}{L_2C_1}}$ Complex	-N/A-	$\left(\frac{1-D}{2D}\right)\frac{R}{L_2}\pm j\sqrt{\frac{2D}{L_2C_1}}$ Complex	-N/A-
$-s_z$ zero of Z_o	$\frac{G_{22}}{2C_1}\pm j\frac{D}{\sqrt{L_2C_1}}$ complex	$\frac{G_{22}}{C_1}$ Real	$\frac{G_{22}}{2C_1}\pm j\frac{D}{\sqrt{L_2C_1}}$ complex	$\frac{G_{22}}{C_1}$ Real

Table 6.3: Comparison of poles and zeros

Boost-and-flyback Converter		
Transfer function	DCM-CCM	DCM-DCM
$\frac{\hat{v}_o}{\hat{d}}$	$\frac{\left(1-\frac{sL_2J_4}{U_3K_{43}}\right)\left(1+\frac{sC_1}{G_{22}}\right)+\frac{J_2K_{32}K_{43}-J_4K_{32}K_{23}}{G_{22}U_3K_{43}}}{K_{34}K_{43}G_{22}\left[\frac{s^2L_2C_2}{K_{34}K_{43}}+\frac{sL_2}{RK_{34}K_{43}}+1\right]\left(\frac{sC_1}{G_{22}}+1\right)+\frac{K_{23}K_{32}}{R}(sRC_2+1)}$	$\frac{\frac{RJ_3}{2}\left[1+\frac{sC_1}{G_{22}}+\frac{G_{32}J_2}{J_3G_{22}}\right]}{\left(\frac{sRC_2}{2}+1\right)\left(\frac{sC_1}{G_{22}}+1\right)}$
Z_o	$\frac{K_{23}K_{32}\left(\frac{s^2L_2C_1}{K_{23}K_{32}}+\frac{sL_2G_{22}}{K_{23}K_{32}}+1\right)}{K_{34}K_{43}G_{22}\left[\frac{s^2L_2C_2}{K_{34}K_{43}}+\frac{sL_2}{RK_{34}K_{43}}+1\right]\left(\frac{sC_1}{G_{22}}+1\right)+\frac{K_{23}K_{32}}{R}(sRC_2+1)}$	$\frac{\frac{R}{2}}{\left(\frac{sRC_2}{2}+1\right)}$
$\frac{\hat{v}_o}{\hat{e}}$	$\frac{G_{21}K_{32}K_{43}}{K_{34}K_{43}G_{22}\left[\frac{s^2L_2C_2}{K_{34}K_{43}}+\frac{sL_2}{RK_{34}K_{43}}+1\right]\left(\frac{sC_1}{G_{22}}+1\right)+\frac{K_{23}K_{32}}{R}(sRC_2+1)}$	$\frac{G_{32}G_{21}\left(\frac{R}{2G_{22}}\right)}{\left(\frac{sRC_2}{2}+1\right)\left(\frac{sC_1}{G_{22}}+1\right)}$
Z_i DCM-CCM	$\frac{K_{34}K_{43}G_{22}\left[\frac{s^2L_2C_2}{K_{34}K_{43}}+\frac{sL_2}{RK_{34}K_{43}}+1\right]\left(\frac{sC_1}{G_{22}}+1\right)+\frac{K_{23}K_{32}}{R}(sRC_2+1)}{G_{11}\left\{K_{34}K_{43}G_{22}\left[\frac{s^2L_2C_2}{K_{34}K_{43}}+\frac{sL_2}{RK_{34}K_{43}}+1\right]\left(\frac{sC_1}{G_{22}}+1\right)+\frac{K_{23}K_{32}}{R}(sRC_2+1)\right\}-G_{12}G_{21}K_{34}K_{43}\left[\frac{s^2L_2C_2}{K_{34}K_{43}}+\frac{sL_2}{RK_{34}K_{43}}+1\right]}$	
Z_i DCM-DCM	$\frac{\left(\frac{sC_1}{G_{22}}+1\right)}{G_{11}\left(\frac{sC_1}{G_{22}}+1\right)-\frac{G_{12}G_{21}}{G_{22}}}$	

Table 6.4: Small-signal transfer functions

Boost-and-flyback Converter				
Poles & zeros	$C_1 \gg M_{22}^2C_2$		$C_1 \ll M_{22}^2C_2$	
	DCM-CCM	DCM-DCM	DCM-CCM	DCM-DCM
$-s_{rp1}$ Real pole	$\frac{D^2}{RC_1(1-D)^2}+\frac{G_{22}}{C_1}$	$\frac{2}{RC_2}$	$\frac{1}{RC_2}+\frac{G_{22}(1-D)^2}{D^2RC_2}$	$\frac{2}{RC_2}$
$-s_{2,3}$ Complex poles	$\frac{1}{2RC_2}\pm j\frac{1-D}{\sqrt{L_2C_2}}$	-N/A-	$\frac{G_{22}}{2C_1}\pm j\frac{D}{\sqrt{L_2C_1}}$	-N/A-
$-s_{rz1}$ Real zero of $\hat{v}_o/\hat{d}$	$\frac{2D^2}{(1-D)RC_1}$	-N/A-	$\frac{2D^2}{(1-D)RC_1}$	-N/A-
$-s_{rz2}$ Real zero of $\hat{v}_o/\hat{d}$	$-\left(\frac{(1-D)^2}{D}\right)\frac{R}{L_2}$	-N/A-	$-\left(\frac{(1-D)^2}{D}\right)\frac{R}{L_2}$	-N/A-
$-s_z$ zero of Z_o	$\frac{G_{22}}{2C_1}\pm j\frac{D}{\sqrt{L_2C_1}}$ complex	$\frac{G_{22}}{C_1}$ Real	$\frac{G_{22}}{2C_1}\pm j\frac{D}{\sqrt{L_2C_1}}$ complex	$\frac{G_{22}}{C_1}$ Real

Table 6.5: Comparison of poles and zeros

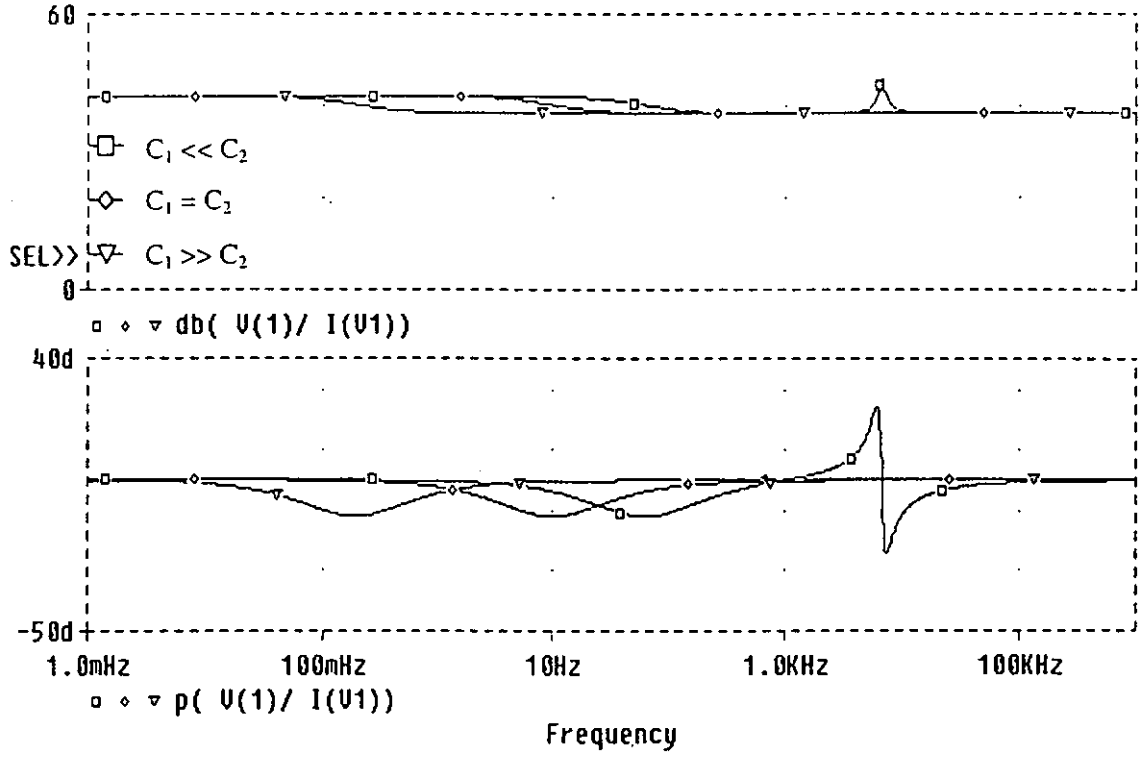

Figure 6.16: Z_i frequency responses of **BIFRED** operating in DCM-CCM for different relative sizes of capacitances. Upper plot: magnitude (dB); Lower plot: phase (deg)

6.3 Dynamical Analysis of BIFRED operating in DCM-DCM

The switching waveforms of BIFRED operating in DCM-DCM are shown in Fig. 6.17(a). Averaging the inductor and capacitor current and voltage waveforms over a switching cycle [36], the following equations are derived:

$$i_{L_1} = \frac{d^2 T e}{2L_1(1 - e/(v_{C_1} + v_o))} \tag{6.42}$$

$$C_1 \frac{dv_{C_1}}{dt} = i_{C_1} = \frac{d^2 T e}{2L_1((v_{C_1} + v_o)/e - 1)} - v_{C_1} \frac{d^2 T}{2L_2} \tag{6.43}$$

$$C_2 \frac{dv_o}{dt} = i_{C_2} = \frac{d^2 T e}{2L_1((v_{C_1} + v_o)/e - 1)} + v_{C_1}^2 \frac{d^2 T}{2v_o L_2} - \frac{v_o}{R} \tag{6.44}$$

provide an analytical basis to derive the averaged model shown in Fig. 6.18.

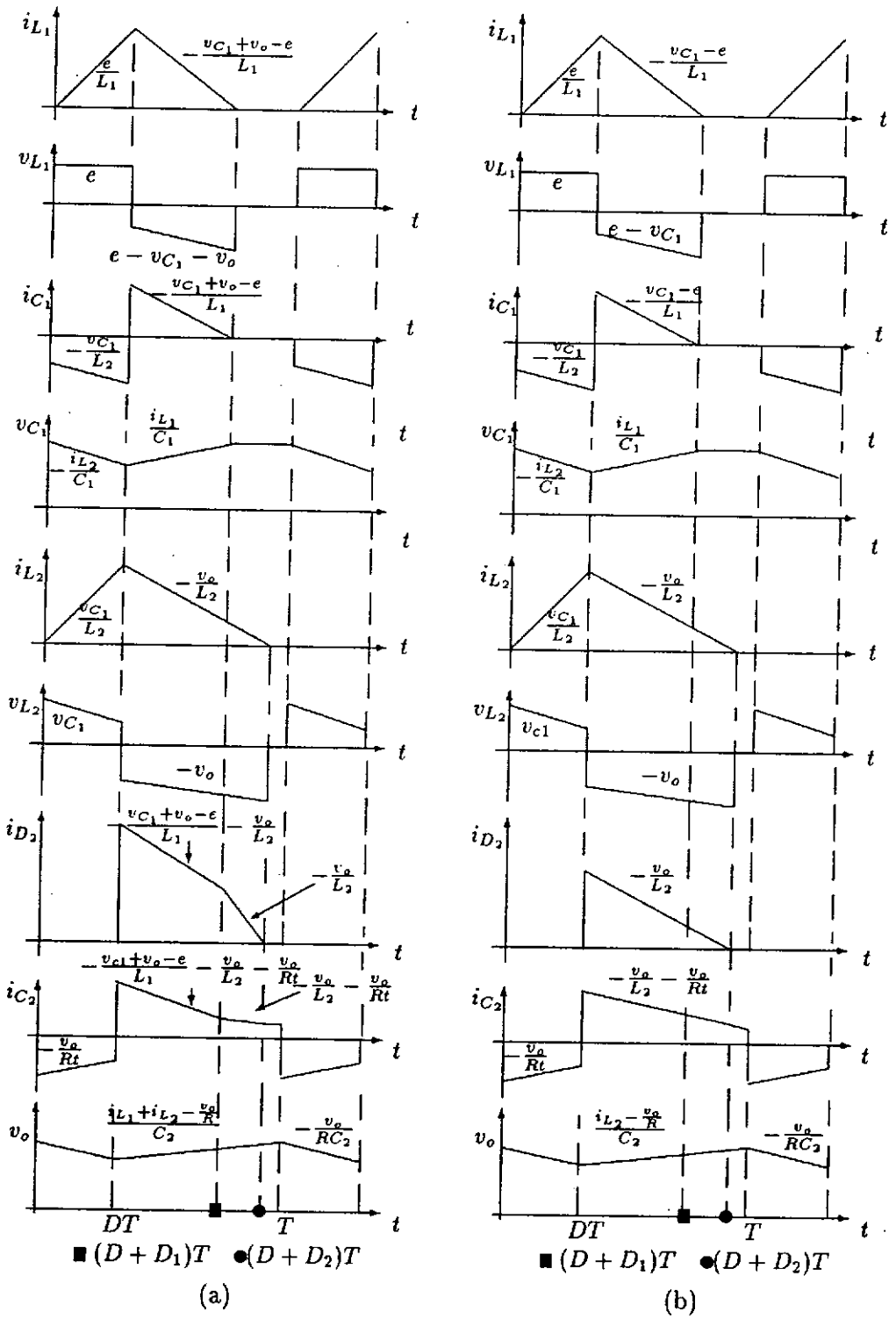

Figure 6.17: Switching waveforms of (a) BIFRED in DCM-DCM ; (b) Boost-and-flyback converter in DCM-DCM. (All the entries on the waveforms represent slopes except the inductor voltage waveforms.)

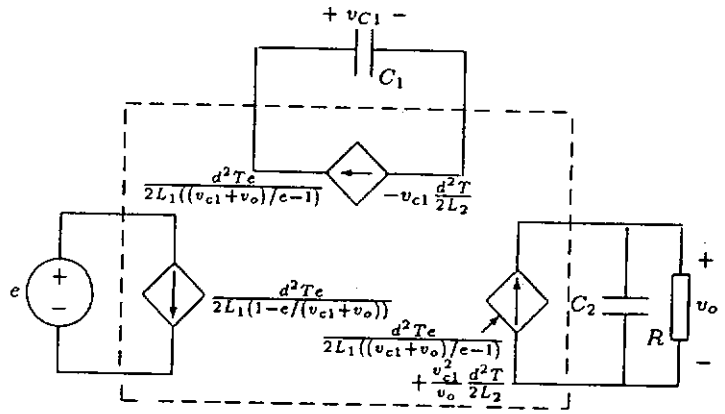

Figure 6.18: Averaged model of BIFRED operating in DCM-DCM

6.3.1 Derivation of Small-signal Transfer Functions

By applying small-signal linearization [36], the small-signal model shown in Fig. 6.19 is derived which is used in the derivation of small-signal transfer functions. The model shown in Fig. 6.19 suggests, the dynamics is of second-order, with two real poles determined by G_{22}/C_1 and G_3/C_2 where G_3 (introduced in Tables 6.2 and 6.3) denotes $G_{33} + 1/R$.

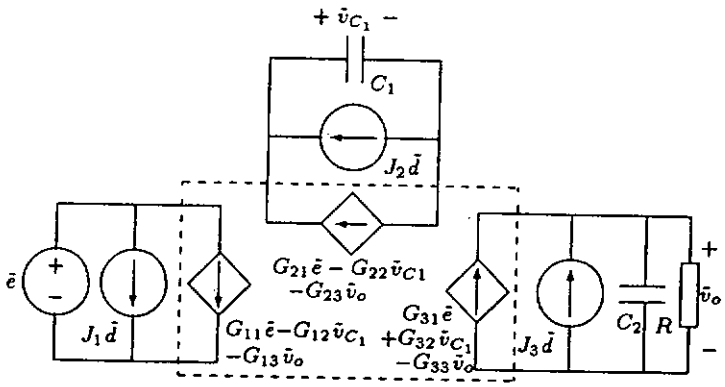

Figure 6.19: Small-signal model of BIFRED operating in DCM-DCM

6.3.1.A Duty-ratio-to-output Voltage Transfer Function

In deriving the $\tilde{v}_o/\tilde{d}$ transfer function, the input $\tilde{e}$ is set to zero. The circuit model thus reduces to the one shown in Fig. 6.20.

Application of nodal analysis to the circuit shown in Fig. 6.20 gives

$$\begin{bmatrix} -G_{23} & G_{22}+sC_1 \\ sC_2+G_3 & -G_{32} \end{bmatrix} \begin{bmatrix} \tilde{v}_o \\ \tilde{v}_{C_1} \end{bmatrix} = \begin{bmatrix} J_2\tilde{d} \\ J_3\tilde{d} \end{bmatrix} \tag{6.45}$$

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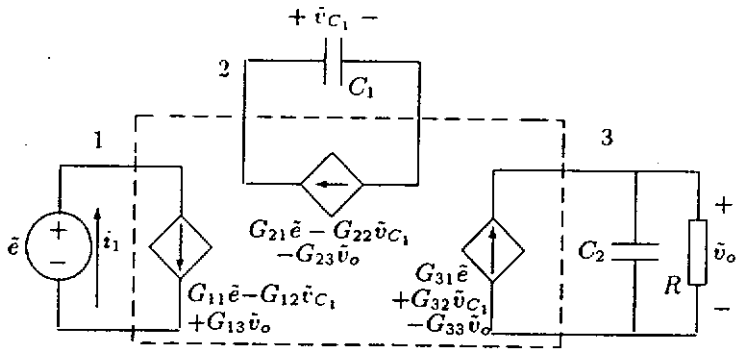

Figure 6.22: Model for calculation of $\tilde{v}_o/\tilde{e}$ and Z_i

Applying nodal analysis to the circuit shown in Fig. 6.22 given by

$$\begin{bmatrix} -G_{23} & G_{22}+sC_1 \\ sC_2+G_3 & -G_{32} \end{bmatrix} \begin{bmatrix} \tilde{v}_o \\ \tilde{v}_{C_1} \end{bmatrix} = \begin{bmatrix} G_{21}\tilde{e} \\ G_{31}\tilde{e} \end{bmatrix} \tag{6.49}$$

Solving (6.49) for $\tilde{v}_o$ results in

$$\frac{\tilde{v}_o}{\tilde{e}} = \frac{\frac{G_{31}}{G_3}\left[1+\frac{sC_1}{G_{22}}-\frac{G_{32}G_{21}}{G_{31}G_{22}}\right]}{\left(1+\frac{sC_1}{G_{22}}\right)\left(1+\frac{sC_2}{G_3}\right)-\frac{G_{23}G_{32}}{G_{22}G_3}} \tag{6.50}$$

6.3.1.D Input Impedance Transfer Function

The circuit of Fig. 6.22 is used again for calculating the input impedance. The nodal matrix of the circuit shown in Fig. 6.22 is

$$\begin{bmatrix} 1 & -G_{13} & -G_{12} \\ 0 & -G_{23} & G_{22}+sC_1 \\ 0 & sC_2+G_3 & G_{32} \end{bmatrix} \begin{bmatrix} \tilde{i}_1 \\ \tilde{v}_o \\ \tilde{v}_{C_1} \end{bmatrix} = \begin{bmatrix} G_{11}\tilde{e} \\ G_{21}\tilde{e} \\ G_{31}\tilde{e} \end{bmatrix} \tag{6.51}$$

Solving (6.51) for $\tilde{i}_1$ results in

$$Z_i = \frac{\tilde{e}}{\tilde{i}_1} = \frac{\left(1+\frac{sC_2}{G_3}\right)\left(1+\frac{sC_1}{G_{22}}\right)-\frac{G_{23}G_{32}}{G_3G_{22}}}{G_{11}\left[\left(1+\frac{sC_2}{G_3}\right)\left(1+\frac{sC_1}{G_{22}}\right)-\frac{G_{23}G_{32}}{G_3G_{22}}\right]+\frac{G_{13}G_{31}}{G_3G_{22}}\left(sC_1+sC_2-G_3+G_{23}+G_{32}\right)} \tag{6.52}$$

All the transfer functions can be rearranged in the conventional form which are listed in Table 6.2. To facilitate inspection, the poles and zeros are tabulated in Table 6.3.

6.3.2 Dynamical Analysis

From the transfer functions we can make the following observations:

1. It can be observed from Table 6.3 that $-s_{rp1}$ and $-s_{rz}$ are close to each other resulting in a single-pole response essentially determined by G_3/C_2 for $C_1 \gg M_{22}^2C_2$. However if $C_1 \ll M_{22}^2C_2$, then the pole and zero due to G_{22}/C_1 gets separated from pole due to G_3/C_1, resulting again in a single-pole response determined by G_3/C_2.

2. Similar to the DCM-CCM case, $\tilde{v}_o/\tilde{e}$ has a zero due to G_{22}/C_1 but has two real poles.

3. The input impedance Z_i has the same characteristics as in the DCM-CCM case, for $M_1 \gg 1$.

PSPICE Verifications

In this subsection PSPICE simulations of the frequency responses of the transfer functions on the small-signal models are reported. The PSPICE netlists of all the small-signal models which are used to generate the frequency responses are given in Appendix B. The circuit parameters used for simulation are $L_1 = 0.08\text{mH}$, $L_2 = 0.1\text{mH}$, $D = 0.3$, $R = 100\Omega$, $f_s = 100\text{kHz}$, $E = 160\text{V}$. Frequency response curves corresponding to different relative sizes of C_1 and C_2 will be plotted, from which the following observations are made:

1. Figs. 6.25 and 6.13 show the frequency responses of $\tilde{v}_o/\tilde{d}$ and Z_o respectively. They manifest a second-order response having an LHP zero and two LHP poles, as predicted in Table 6.3. A single-pole response is shown for the case of $C_1 \ll M_{22}^2 C_2$.

2. Fig. 6.27 confirms the presence of an LHP zero for $\tilde{v}_o/\tilde{e}$. Thus the phase extends from 0^0 to -90^0.

3. Z_i has the same characteristics as in the DCM-CCM case (Fig. 6.16), for $M_1 \gg 1$.

6.4 Dynamical Analysis of Boost-and-flyback Converter in DCM-DCM

The switching waveforms of the boost-and-flyback converter operating in DCM-DCM are shown in Fig. 6.17(b). By averaging the inductor and capacitor current and voltage waveforms over a switching cycle [36], the following equations are derived:

$$i_{L_1} = \frac{d^2 T e}{2L_1(1 - e/v_{C_1})} \tag{6.53}$$

$$C_1 \frac{dv_{C_1}}{dt} = i_{C_1} = \frac{d^2 T e}{2L_1(v_{C_1}/e - 1)} - v_{C_1}\frac{d^2 T}{2L_2} \tag{6.54}$$

$$C_2 \frac{dv_o}{dt} = i_{C_2} = v_{C_1}^2 \frac{d^2 T}{2v_o L_2} - \frac{v_o}{R} \tag{6.55}$$

which provide an analytical basis to derive the averaged model shown in Fig. 6.23.

6.4.1 Derivation of Small-signal Transfer Functions

In the following subsections, all the small-signal transfer functions are derived based on the model shown in Fig. 6.24.

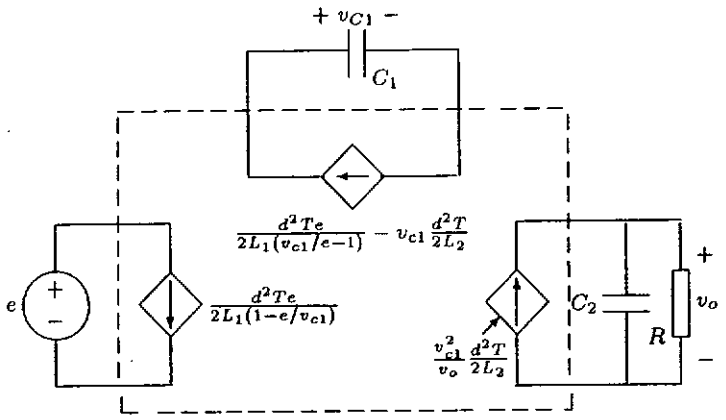

Figure 6.23: Averaged Model of boost-and-flyback converter operating in DCM-DCM

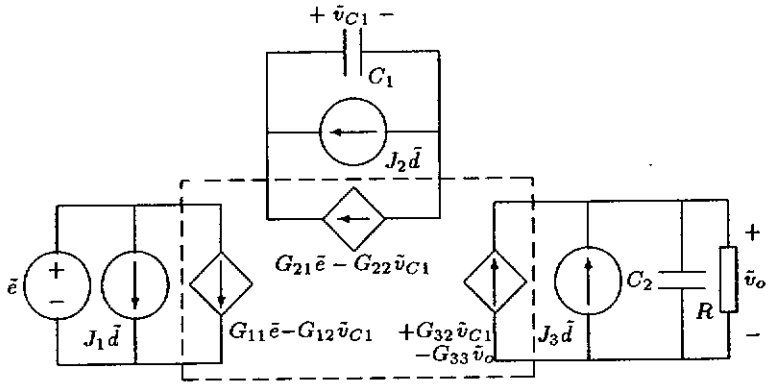

Figure 6.24: Small-signal model of boost-and-flyback converter operating in DCM-DCM

6.4.1.A Duty-ratio-to-output Voltage Transfer Function

Application of nodal analysis to the ciruit shown in Fig. 6.20 gives

$$\begin{bmatrix} 0 & G_{22}+sC_1 \\ sC_2+\frac{1}{R} & -G_{32} \end{bmatrix} \begin{bmatrix} \tilde{v}_o \\ \tilde{v}_{C_1} \end{bmatrix} = \begin{bmatrix} J_2\tilde{d} \\ J_3\tilde{d} \end{bmatrix} \tag{6.56}$$

Solving (6.56) for $\tilde{v}_o$ results in

$$\frac{\tilde{v}_o}{\tilde{d}} = \frac{\frac{RJ_3}{2}\left[1+\frac{sC_1}{G_{22}}+\frac{G_{32}J_2}{J_3G_{22}}\right]}{\left(1+\frac{sC_1}{G_{22}}\right)\left(1+\frac{sRC_2}{2}\right)} \tag{6.57}$$

6.4.1.B Output Impedance Transfer Function

Application of nodal analysis to the circuit shown in Fig. 6.21 gives

$$\begin{bmatrix} 0 & G_{22}+sC_1 \\ sC_2+\frac{1}{R} & -G_{32} \end{bmatrix} \begin{bmatrix} \tilde{v}_o \\ \tilde{v}_{C_1} \end{bmatrix} = \begin{bmatrix} 0 \\ \tilde{i}_s \end{bmatrix} \tag{6.58}$$

Solving (6.58) for $\tilde{v}_o$ results in

$$Z_o = \frac{\tilde{v}_o}{\tilde{i}_s} = \frac{\frac{R}{2}}{1 + \frac{sRC_2}{2}} \tag{6.59}$$

6.4.1.C Line-to-output Voltage Transfer Function

Application of nodal analysis to the circuit shown in Fig. 6.22 gives

$$\begin{bmatrix} 0 & G_{22} + sC_1 \\ sC_2 + \frac{1}{R} & -G_{32} \end{bmatrix} \begin{bmatrix} \tilde{v}_o \\ \tilde{v}_{C_1} \end{bmatrix} = \begin{bmatrix} G_{21}\tilde{e} \\ 0 \end{bmatrix} \tag{6.60}$$

Solving (6.60) for $\tilde{v}_o$ results in

$$\frac{\tilde{v}_o}{\tilde{e}} = \frac{\frac{RG_{21}G_{32}}{2}}{\left(1 + \frac{sRC_2}{2}\right)} \tag{6.61}$$

6.4.1.D Input Impedance Transfer Function

Application of nodal analysis to the circuit shown in Fig. 6.22 gives

$$\begin{bmatrix} 1 & 0 & G_{12} \\ 0 & 0 & G_{22} + sC_1 \\ 0 & sC_2 + \frac{1}{R} & -G_{32} \end{bmatrix} \begin{bmatrix} \tilde{i}_1 \\ \tilde{v}_o \\ \tilde{v}_{C_1} \end{bmatrix} = \begin{bmatrix} G_{11}\tilde{e} \\ G_{21}\tilde{e} \\ 0 \end{bmatrix} \tag{6.62}$$

Solving (6.62) for $\tilde{v}_o$ results in

$$Z_i = \frac{\tilde{e}}{\tilde{i}_1} = \frac{sC_1 + G_{22}}{G_{11}(sC_1 + G_{22}) - G_{21}G_{12}} \tag{6.63}$$

6.4.2 Dynamical Analysis

As the model shown in Fig. 6.24 suggests, the dynamics is of second-order, with two real poles determined by G_{22}/C_1 and RC_2. From the above derived transfer functions (see Table 6.4), the following observations can be made:

1. Unlike BIFRED, pole-zero cancellation occurs in $\tilde{v}_o/\tilde{d}$ transfer function irrespective of the sizes of C_1 and C_2 resulting in a simple single-pole response determined by RC_2 (see Table 6.5).

   Pole-zero Cancellation

   Consider the characteristic equation of $\tilde{v}_o/\tilde{d}$ or $\tilde{v}_o/\tilde{e}$ of boost-and-flyback converter operating in DCM-DCM given in Table 6.4:

$$\left(\frac{sRC_2}{2} + 1\right)\left(\frac{sC_1}{G_{22}} + 1\right) = 0 \tag{6.64}$$

The numerator of $\tilde{v}_o/\tilde{d}$ from Table 6.4 is

$$\frac{RJ_3}{2}\left[1+\frac{sC_1}{G_{22}}+\frac{G_{32}J_2}{J_3G_{22}}\right] \tag{6.65}$$

For $V_{C_1}/E \gg 1$, J_2 of (6.65) becomes zero, thus, $\left(\frac{sC_1}{G_{22}}+1\right)$ of (6.64) and (6.65) get cancelled, leaving just a single-pole response:

$$\frac{\tilde{v}_o}{\tilde{d}} \approx \frac{RJ_3}{2}\left[\frac{1}{\frac{sRC_2}{2}+1}\right] \tag{6.66}$$

(6.66) is the same as the $\tilde{v}_o/\tilde{d}$ transfer function of the DCM flyback converter.

2. Z_o is just a simple single-pole transfer function without any zero.

3. Similar to any other basic DC-DC converter, $\tilde{v}_o/\tilde{e}$ has no zeros.

4. Z_i has the same characteristics as in the BIFRED case for $M_{11} \gg 1$.

PSPICE Verifications

In this subsection, PSPICE simulations of the frequency responses based on the small-signal models are reported. The PSPICE netlists of all the small-signal models which are used to generate the frequency responses are given in Appendix B. The circuit parameters used for simulation are $L_1 = 0.08$mH, $L_2 = 0.1$mH, $D = 0.3$, $R = 100\Omega$, $f_s = 100$kHz, $E = 160$V. A series of frequency response curves corresponding to different relative sizes of C_1 and C_2 are plotted, from which the following observations are made:

1. Figs. 6.26 and 6.29 verify the single-pole response for $\tilde{v}_o/\tilde{d}$ and Z_o whose phase responses extend from 0^0 to -90^0 due to pole-zero cancellation irrespective of the relative sizes of C_1 and C_2, thus, having a common corner frequency of $1/\pi RC_2$.

2. Fig. 6.28 confirms the absence of zeros in $\tilde{v}_o/\tilde{e}$, thus, its phase response extends from 0^0 to -180^0.

3. For $M_{11} \gg 1$, Z_i has the same response as in the DCM-CCM case (see Fig. 6.16).

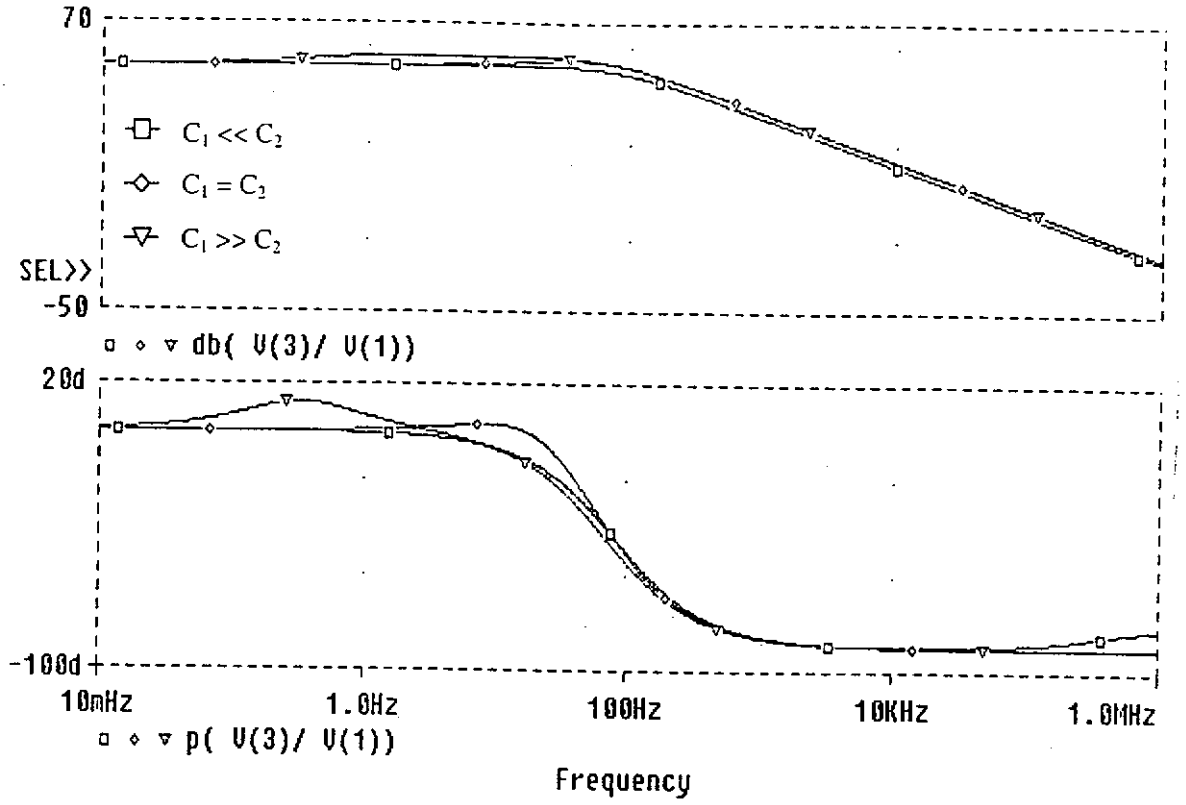

Figure 6.25: $\tilde{d}$-to-$\tilde{v}_o$ frequency responses of **BIFRED** operating in DCM-DCM for different relative sizes of capacitances. Upper plot: magnitude (dB); Lower plot: phase (deg)

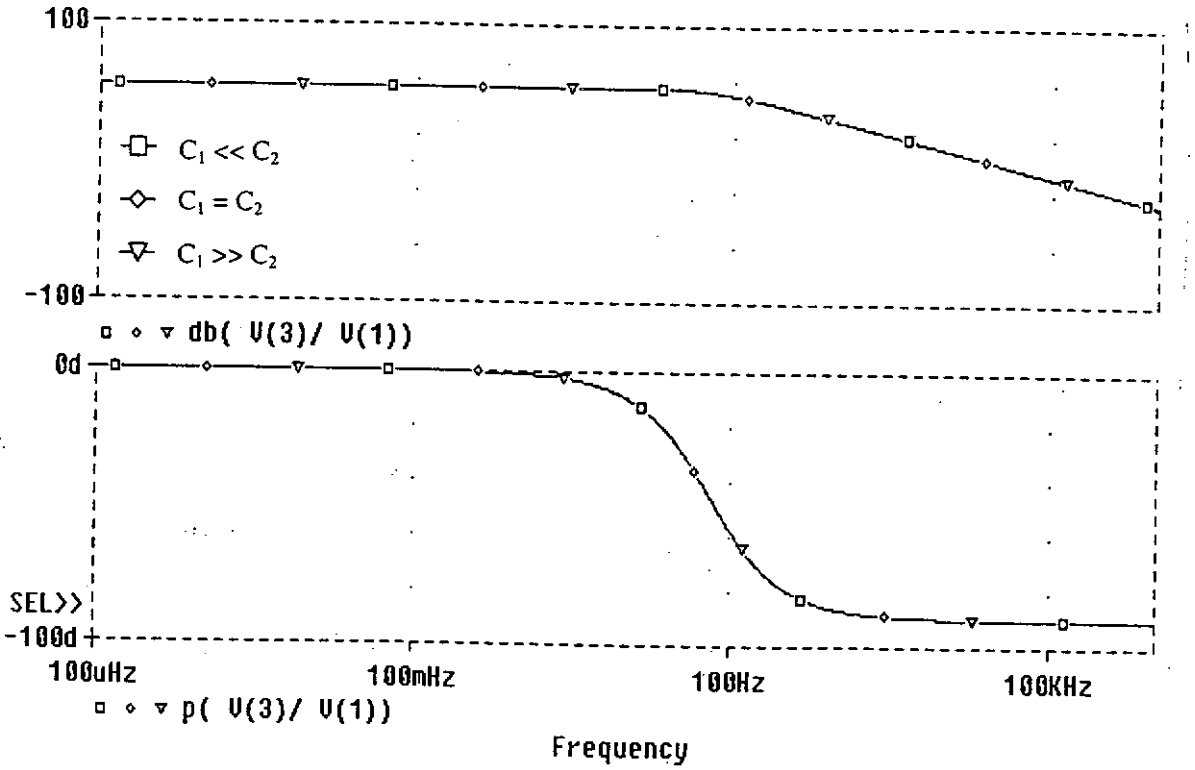

Figure 6.26: $\tilde{d}$-to-$\tilde{v}_o$ frequency responses of **boost-and-flyback converter** operating in DCM-DCM for different relative sizes of capacitances. Upper plot: magnitude (dB); Lower plot: phase (deg)

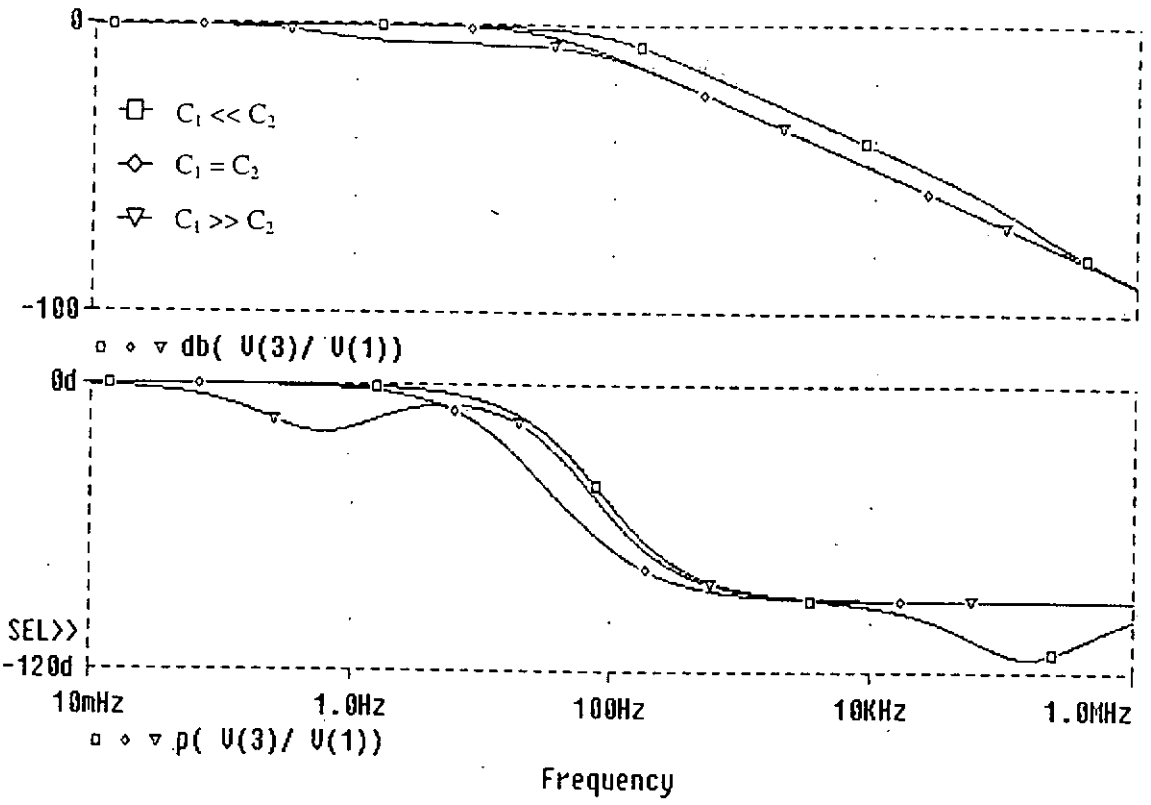

Figure 6.27: $\tilde{e}$-to-$\tilde{v}_o$ frequency responses of **BIFRED** operating in DCM-DCM for different relative sizes of capacitances. Upper plot: magnitude (dB); Lower plot: phase (deg)

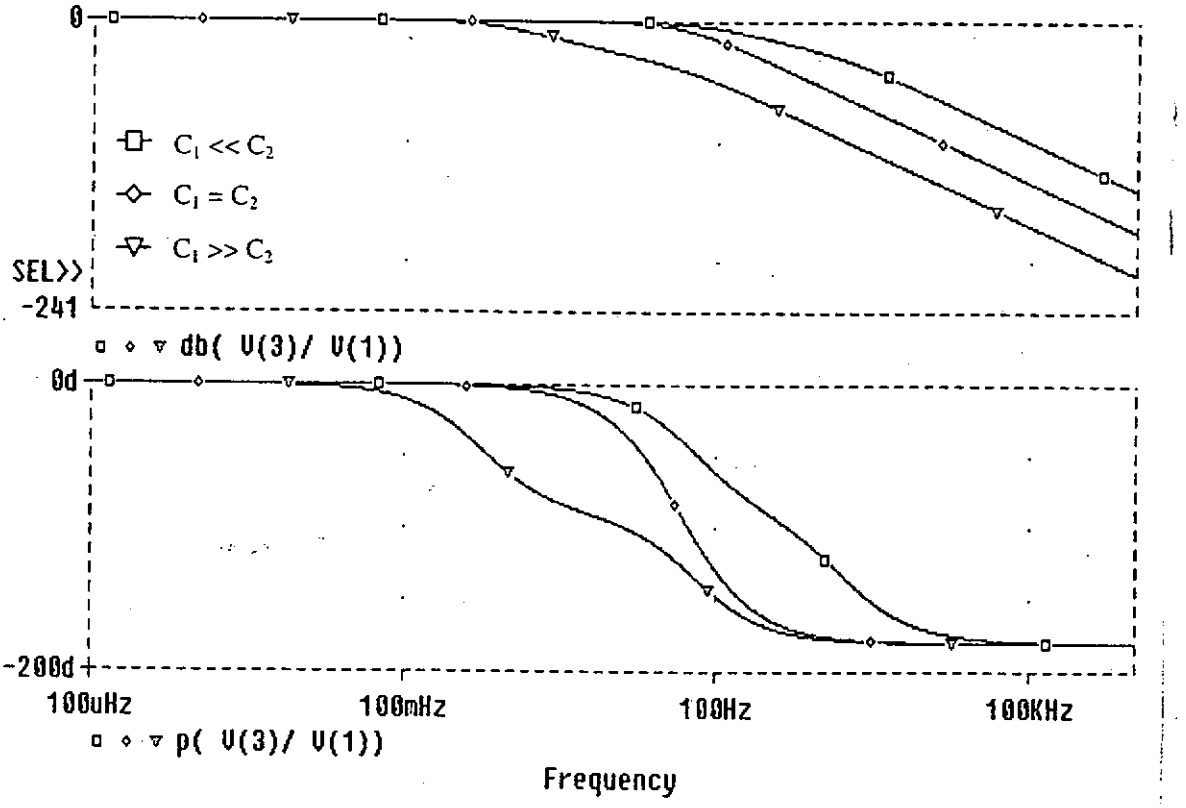

Figure 6.28: $\tilde{e}$-to-$\tilde{v}_o$ frequency responses of **boost-and-flyback converter** operating in DCM-DCM for different relative sizes of capacitances. Upper plot: magnitude (dB); Lower plot: phase (deg)

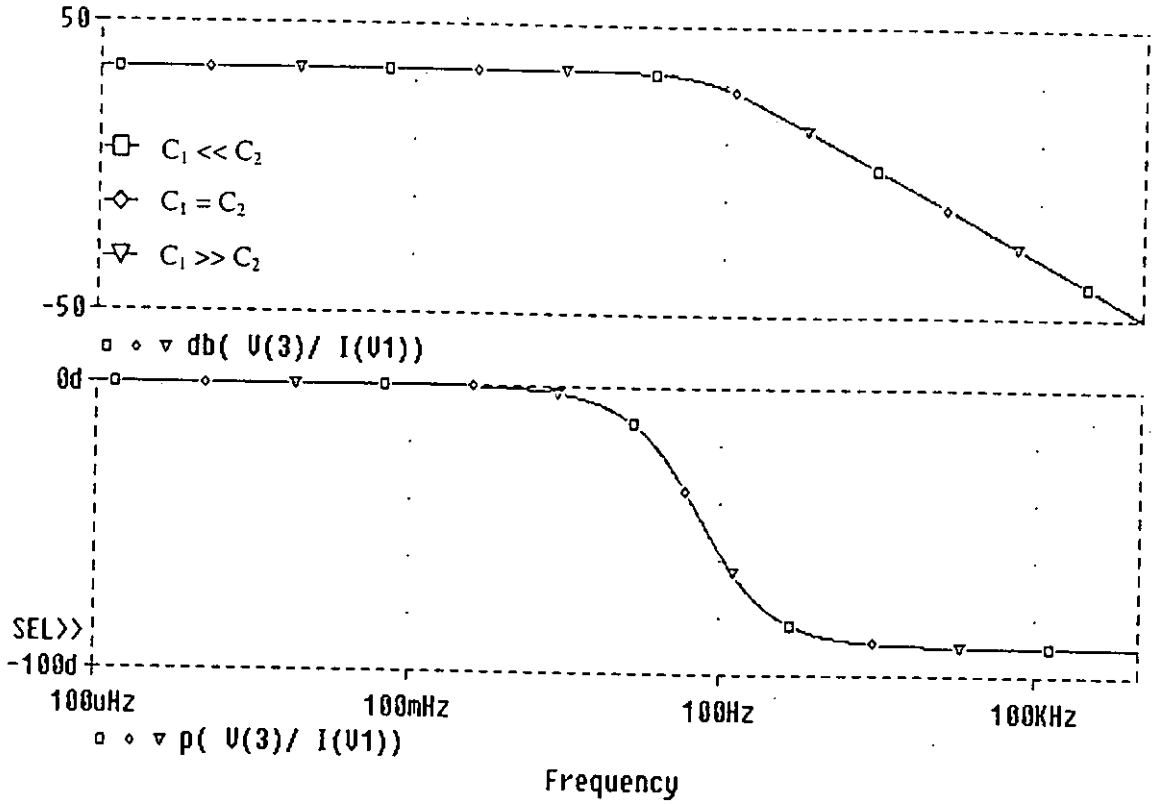

Figure 6.29: Z_o frequency responses of **boost-and-flyback converter** operating in DCM-DCM for different relative sizes of capacitances. Upper plot: magnitude (dB); Lower plot: phase (deg)

6.5 Concluding Remarks

Complete sets of small-signal transfer functions for BIFRED and cascaded boost-and-flyback PFC converters operating in DCM-CCM and DCM-DCM are derived and compared in this chapter. The results are important in understanding the dynamics of these types of converters and the various factors that can affect the small-signal dynamical response of the converter. In particular, it is shown that when the boost part operates in DCM and the flyback part in CCM, the duty-ratio-to-output transfer function of BIFRED can be reduced to a simple second-order *minimum phase* function whereas the SSIPP can be reduced to second-order *non-minimum phase* function under certain conditions. Such order reduction (pole-zero cancellation) is important for achieving fast response. Moreover, due to the occurrence of pole-zero cancellation, the boost-and-flyback converter can achieve fast (single-pole) response regardless of the size of the storage capacitor, when both the boost and flyback parts operate in DCM. Also, both the converters when operating in DCM-CCM have higher DC output impedance than that of a flyback converter operating in CCM. This provides some valuable insight in the design of control loop (compensation network) because the designer now knows the effect of sizes of the storage capacitor and output capacitor on the dynamical response.

Chapter 7

Conclusions

The delivery of electric power with a well regulated DC output voltage and in-phase sinusoidal input-current from a single-phase AC line is an important technical area in power electronics. Phase shifted and harmonic-rich line currents lead to poor utilization of the power line, reduced efficiency and interference problems. Hence, a current waveform with UPF can only offer a full utilization of the power line and reduce the interference problems.

Shaping circuits fall into two categories-passive and active. Since passive current-shapers suffer from excessive size and weight, active current-shapers are commonly used in practice which can be classified as - nonautomatic and automatic shapers. Non-automatic shapers use a separate current-shaping control loop as in the boost PFC converters operating in CCM. This thesis focuses on automatic input-current shapers based on DCM operation. These shapers draw proportional input-current when operating under fixed duty-ratio and switching frequency. Such DCM PFC converters are cascaded (in order to satisfy all the requirements of a PFC regulator) by using a single active switch with another DC-DC converter which may be operating either in DCM or CCM. Such cascaded topologies offer a reduction in weight, size and cost [2]. Usually they all use a simple voltage-mode (PWM) or a current-mode control loop for output-voltage regulation without any control loop for input-current shaping. Such cascaded converters are analyzed and compared.

Based on the preliminary requirements of linear input resistance emulation, internal line-frequency energy storage and fast regulation of load voltage and also some topological criteria, all the buck based single-switch topologies are found unsuitable to function as a PFC regulator. The BIFRED is found unsuitable to function as a PFC regulator, but can be still be used if a *simultaneous duty-ratio with load-current feedforward control* or *simultaneous duty-ratio and switching frequency control* is employed to shape the input-current and regulate the output-voltage [1], [5]. The new buck based topology and other buck based topologies are not considered for PFC regulator application even though a simultaneous duty-ratio and switching frequency control is applied. The main drawback that disqualifies buck based topologies from being employed as PFC regulators is that they require a relatively larger internal energy

storage capacitor C_1, when compared with boost or flyback based converters because of the low static voltage level of the buck stage.

The single-stage cascaded converters which are found suitable are compared against their switching stresses, RMS, peak and average currents in inductors, capacitors and diodes. The flyback based converters can theoretically provide a UPF but have higher switching stresses when compared to boost based converters. The converters which are operating in DCM-CCM have lower switch stresses when compared to converters operating in DCM-DCM. The RMS currents of inductors, diodes are also high when operating in DCM. However, when the output converter stage is operating in CCM there are some advantages:

- Lesser losses due to lower RMS and average currents.
- Size of the load capacitor C_2 in the case of buck output stage can be reduced.

Moreover, the loop compensation is slightly more complicated if the output stage is operating in CCM due to the presence of complex poles and RHP zero in the case of flyback or boost output stages. The static capacitor of the input PFC stage tends to vary with the load. Although a slightly larger output capacitance C_2 is needed when compared to the CCM output stage, the output converter stage operating in DCM offers some advantages:

- A single-pole response (hence a fast response) and a simpler loop compensation.
- The internal energy storage capacitor voltage V_{C_1} is load independent.

Since the input converter stage of these cascaded converters always operate in DCM, they are suited only for low-power applications. The work which could be done in the future is to develop a more efficient system which satisfies all the requirements of a PFC regulator and uses a simple control loop. Apart from the parallel power processing scheme, some work in this direction has been started elsewhere where the input power is not processed twice. This increases the efficiency. By suitably restructuring the topology and using an appropriate control method, a fast dynamical response can be achieved [43, 44].

Appendix A

Approximate Solution of Cubic Equation

A.1 Approximate Solution of the Cubic Equation

By using conventional method of solving a given cubic equation [45], it is almost impossible to gain any insight from the roots of the cubic equation. This provides a motivation to propose an approximate method to calculate the roots of a cubic equation under certain conditions. The conditions under which the approximate roots of the cubic equation are valid are given in the following theorems.

Theorem A.1 *Consider the cubic equation:* $s^3 + a_1 s + a_0 = 0$ *where* a_1 *and* a_0 *are positive real numbers. Let* s_r *be a real root of this cubic equation. If* $a_0^2 \ll a_1^3$ *then*

$$s_r \approx -\frac{a_0}{a_1} \tag{A.1}$$

Proof:
The approximate value of s_r given by (A.1) is valid if the cubic equation can be reduced to $a_1 s + a_0 = 0$. This requires that the s^3 term be much smaller than the other two terms in the original cubic equation, i.e.,

$$\left(-\frac{a_0}{a_1}\right)^3 \ll a_0 \tag{A.2}$$

and

$$\left(-\frac{a_0}{a_1}\right)^3 \ll a_1\left(-\frac{a_0}{a_1}\right) \tag{A.3}$$

Since a_0 and a_1 are positive, (A.2) and (A.3) can be written as

$$-a_0^2 \ll a_1^3 \quad \text{and} \quad a_0^2 \ll a_1^3 \tag{A.4}$$

which can be rewritten as $a_0^2 \ll a_1^3$.

Theorem A.2 *Consider the cubic equation:*

$$s^3 + a_2 s^2 + a_1 s + a_0 = 0 \tag{A.5}$$

Let s_r be a real root of this cubic equation. If

$$\frac{\left(\frac{a_0}{a_1}\right)^2\left(a_2-\frac{a_0}{a_1}\right)}{a_0} \ll 1 \tag{A.6}$$

then the approximate solution of the cubic equation is

$$s_r \approx -\frac{a_0}{a_1} \tag{A.7}$$

Moreover, the other roots, if complex, are given by

$$s_{2,3} \approx -\frac{a_2+s_r}{2} \pm j\sqrt{a_1} \tag{A.8}$$

Proof:

The approximate solution of the cubic equation given by (A.7) is valid if the cubic equation can be reduced to $a_1 s + a_0 = 0$. This requires that the $s^3 + a_2 s^2$ term be much smaller than the other two terms in the original cubic equation, i.e.,

$$\left(-\frac{a_0}{a_1}\right)^3 + a_2\left(-\frac{a_0}{a_1}\right)^2 \ll a_0 \tag{A.9}$$

and

$$\left(-\frac{a_0}{a_1}\right)^3 + a_2\left(-\frac{a_0}{a_1}\right)^2 \ll a_1\left(-\frac{a_0}{a_1}\right) \tag{A.10}$$

Since a_0 and a_1 are positive, (A.9) and (A.10) can be written as

$$\left(\frac{a_0}{a_1}\right)^2\left(a_2-\frac{a_0}{a_1}\right) \ll a_0 \tag{A.11}$$

Moreover, since the cubic equation can be written as

$$(s-s_r)(s^2+(a_2+s_r)s+a_1)=0 \tag{A.12}$$

The remaining roots can be found by solving the quadratic equation (A.12). Assuming the roots s_2 and s_3 to be complex, the approximate solution is

$$s_{2,3} \approx -\frac{a_2+s_r}{2} \pm j\sqrt{a_1} \tag{A.13}$$

Corollary Consider the characteristic cubic equation of $\tilde{v}_o/\tilde{d}$ or $\tilde{v}_o/\tilde{e}$ or Z_o of a cascaded boost-and-buck converter operating in DCM-CCM as given in Chapter 5:

$$s^3 + \overbrace{\left(\frac{L_2C_1+L_2C_2G_{22}R}{L_2C_1C_2R}\right)}^{a_2} s^2 + \overbrace{\left(\frac{D^2C_2R+G_{22}L_2+C_1R}{L_2C_1C_2R}\right)}^{a_1} s + \overbrace{\frac{D^2+G_{22}R}{L_2C_1C_2R}}^{a_0} = 0 \tag{A.14}$$

Inequality (A.6) can also be written as

$$\frac{a_0}{\left(\frac{a_0}{a_1}\right)^2\left(a_2-\frac{a_0}{a_1}\right)} \gg 1 \tag{A.15}$$

It can be concluded that if the roots (A.7) and (A.13) are valid then (A.15) is satisfied. Figs. A.1(a) and (b) illustrate this fact. It can be observed that even if (A.15) is *weakly* satisfied, the error introduced is significant. This can be clearly noticed in Fig. A.1(b). C_1C_2 is chosen as the independent (x-axis) variable instead of L_2 for various reasons such as,

- Analytical convenience.
- a_2 is not a function of L_2.
- C_1C_2 can be freely varied over a wide range.
- L_2 cannot be freely varied over a wide range like C_1C_2 because the converter has to operate in DCM-CCM for (A.14). However, it can be increased beyond its critical value (for example: $L_2 > (1-D)RT/2$ for the case of buck converter) so that the output converter stage will be operating in CCM for (A.14) to be valid. Fig. A.1(b) illustrates this fact by considering a very high value of L_2, (though impractical) to examine the validity of the condition (A.15).
- Unlike L_2 and C_1C_2, R cannot be varied since it alters the conduction mode of both the converter stages.

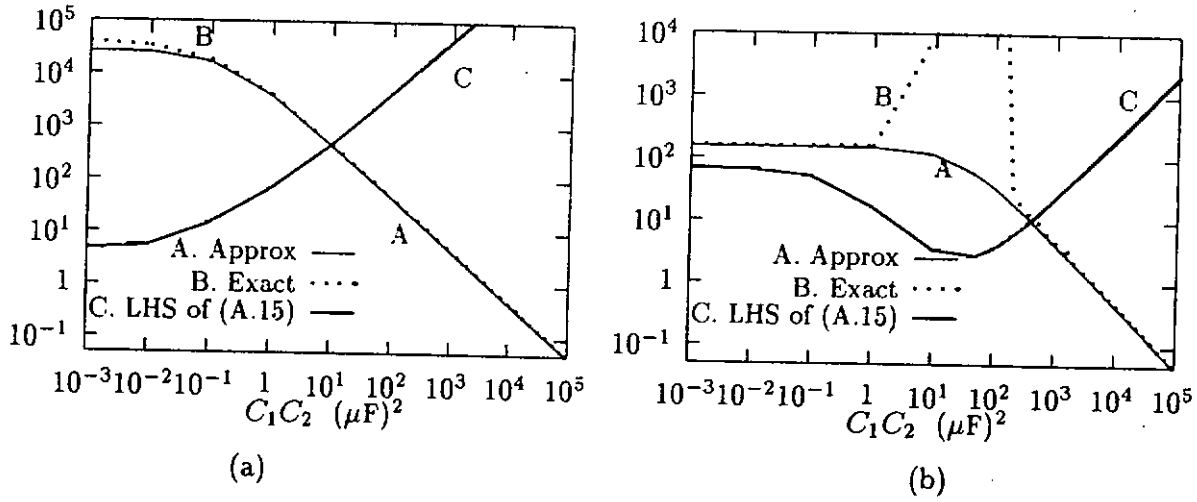

Figure A.1: Verification of the proposed approximation: (a) $L_2 = 0.5$mH (b) $L_2 = 1$H
Y-Axis of plots A & B: $-s_{rp1}$ (rad/sec) ; Y-Axis of plot C: LHS of (A.15)

Both the Figs. A.1(a) and (b) illustrate the fact that the condition (A.15) has to be rigorously satisfied, for the error to be negligible.

A.2 Approximate Solution of the Quadratic Equation

Consider the quadratic equation, $s^2 + a_1 s + a_0 = 0$, where a_1 and a_0 are real numbers. One of the real roots of the equation is given by $-a_0/a_1$ if $a_1^2 \gg a_0$

Proof:

In general, the roots of the quadratic equation, $s^2 + a_1 s + a_0 = 0$ are given by,

$$s_{1,2} = \frac{-a_1 \pm \sqrt{a_1^2 - 4a_0}}{2} \tag{A.16}$$

If $a_1^2 \gg a_0$, then approximately one of the roots is $-a_1$. The other root can be calculated by applying Taylor series expansion,

$$\frac{\sqrt{a_1^2 - 4a_0}}{2} = \frac{a_1}{2} - \frac{a_0}{a_1} - \mathcal{O}\left(\frac{a_0}{a_1}\right)^2 \tag{A.17}$$

Using the first and second terms of (A.17) in (A.16), the other root is $-a_0/a_1$. Hence, the result follows.

A.3 Circuit Components

In Chapters 5 and 6, the circuit components used in modelling and simulation have not been used according to any conventional design procedure since the main aim here is only to analyze the small-signal behaviour of the single-stage cascaded converter. The circuit component values namely L_1, L_2 and R are chosen based on the following criteria.
Input DCM PFC stage:

$$K_{crit,\ boost} = D(1-D)^2 > \frac{2M_2^2 L_1}{RT} \tag{A.18}$$

$$M_1 = \frac{V_{C_1}}{E} \gg 1 \tag{A.19}$$

Output CCM stage:

$$K_{crit,\ buck} = (1-D) < \frac{2L_2}{RT} \tag{A.20}$$

$$K_{crit,\ buck-boost} = (1-D)^2 < \frac{2L_2}{RT} \tag{A.21}$$

Output DCM stage:

$$K_{crit,\ buck} = (1-D) > \frac{2L_2}{RT} \tag{A.22}$$

$$K_{crit,\ buck-boost} = (1-D)^2 > \frac{2L_2}{RT} \tag{A.23}$$

Since it is a hard-switched PWM converter, a high switching frequency is not chosen. With the above criteria in mind, the output power of the converters are not allowed to exceed 200W.

Appendix B

Netlists of PSPICE

This Appendix gives the PSPICE netlists of small-signal models to generate the frequency response plots, which are used in Chapters 5 and 6.

B.1 Netlists of Small-signal Models of Cascaded Boost-and-Buck Converter operating in DCM-CCM

B.1.1 Duty-ratio-to-output Voltage Transfer Function

```
G_G8        0 2 VALUE { 1.38*V(1,0) }
R_R7        0 2  333.33
E_E3        4 0 VALUE { 0.4*V(2,0) + 345.3*V(1,0) }
L_L2        5 3  0.5mH
R_R9        0 3  100
R_R10        0 1  10G
V_V24        1 0 DC 0V AC 1V
F_F3        0 2 VF_F3 -0.4
VF_F3       4 5 0V
C_C2        0 3  {Cval}
C_C1        0 2  100UF
```

B.1.2 Output Impedance

```
R_R1        2 0  333.33
E_E3        4 0 VALUE { 0.4*V(2,0)  }
L_L2        5 V3  0.5mH
F_F3        0 2 VF_F3 -0.5
VF_F3       4 5 0V
R_R2        0 V3  100
C_C2        0 V3  50UF
I_I1        0 V3 DC 0 AC 0.01A
C_Cval      0 2  {Cval}
```

B.1.3 Line-to-output Voltage and Input Impedance Transfer Functions

```
G_G8        0 2 VALUE { 0.0099*V(1,0) }
```

```
R_R7        0 2  333.33
E_E3        4 0 VALUE { 0.4*V(2,0)  }
L_L2        5 V3  0.5mH
R_R9        0 V3  100
V_V1        0 1 DC 0V AC 1V
F_F3        0 2 VF_F3 -0.4
VF_F3       4 5 0V
C_C2        0 V3  50.0UF
C_C1        0 2  {Cval}
G_G9        1 0 VALUE { -0.003*V(2,0) }
R_R1        0 1  71.40
```

B.2 Netlists of Small-signal models of Cascaded Boost-and-buck converter operating in DCM-DCM

B.2.1 Duty-ratio-to-output Voltage Transfer Function

```
R_R1        0 3  57.6
R_R2        0 2  285
R_R3        0 2  320
R_R4        0 3  100
C_C1        0 3  50UF
C_C2        0 2  {Cval}
G_G1        0 3 VALUE { 0.011*V(2,0) }
G_G2        0 2 VALUE { 0.003*V(3,0)  }
R_R6        0 1  10G
G_G4        3 0 VALUE { -11.12*V(1,0) }
V_V1        1 0 DC 0V AC 1V
```

B.2.2 Output Impedance

```
R_R1        0 3  57.6
R_R2        0 2  285
R_R3        0 2  320
R_R4        0 3  100
C_C1        0 3  50UF
C_C2        0 2  {Cval}
G_G1        0 3 VALUE { 0.011*V(2,0) }
G_G2        0 2 VALUE { 0.003*V(3,0)  }
V_V1        0 3 DC 0V AC 1V
```

B.2.3 Line-to-output Voltage and Input Impedance Transfer Functions

```
R_R1        0 3  57.6
R_R2        0 2  285
R_R3        0 2  320
R_R4        0 3  100
C_C1        0 3  50UF
C_C2        0 2  {Cval}
G_G1        0 3 VALUE { 0.011*V(2,0) }
```

```
G_G2        0 2 VALUE { 0.003*V(3,0) +0.011*V(1,0) }
R_R6        0 1  67.5
G_G4        1 0 VALUE { -0.004*V(2,0) }
V_V1        0 1 DC 0V AC 1V
```

B.3 Netlists of Small-signal Models of BIFRED Operating in DCM-CCM

B.3.1 Duty-ratio-to-output Voltage Transfer Function

```
G_G3        0 2 VALUE { 1.46*V(1,0)-0.0013*V(3,0) }
R_R7        0 2  769
R_R8        0 3  769
R_R9        0 3  100
L_L2        $N_0001 $N_0002  0.5mH
E_E2        $N_0003 $N_0004 VALUE { 480*V(1,0)+0.3*V(2,0)-0.7*V(3,0) }
F_F3        0 3 VF_F3 0.7
VF_F3       $N_0003 $N_0002 0V
G_G4        0 3 VALUE { 1.46*V(1,0)-0.0013*V(2,0) }
C_C5        0 3  50UF
V_V2        1 0 DC 0V AC 1V
R_R10       0.1  10G
R_R11       0 $N_0004  0.000001
F_F4        0 2 VF_F4 -0.3
VF_F4       $N_0001 0 0V
C_C6        0 2  {Cval}
```

B.3.2 Output Impedance

```
G_G3        0 2 VALUE { 0.0013*V(3,0) }
R_R7        0 2  769
R_R8        0 3  769
R_R9        0 3  100
L_L2        $N_0001 $N_0002  0.5mH
E_E2        $N_0003 $N_0004 VALUE { 0.3*V(2,0)-0.7*V(3,0) }
F_F3        0 3 VF_F3 0.7
VF_F3       $N_0003 $N_0002 0V
G_G4        0 3 VALUE { 0.0013*V(2,0) }
C_C5        0 3  50UF
V_V3        3 0 DC 0V AC 1V
R_R11       0 $N_0004  0.000001
F_F4        0 2 VF_F4 -0.3
VF_F4       $N_0001 0 0V
C_C6        0 2  {Cval}
```

B.3.3 Line-to-output Voltage and Input Impedance Transfer Functions

```
G_G3        0 2 VALUE { 0.007*V(1,0)-0.0013*V(3,0) }
R_R7        0 2  769
R_R8        0 3  769
R_R9        0 3  100
```

```
L_L2        $N_0001 $N_0002  0.5mH
E_E2        $N_0003 $N_0004 VALUE { 0.3*V(2,0)-0.7*V(3,0) }
F_F3        0 3 VF_F3 0.7
VF_F3       $N_0003 $N_0002 0V
G_G4        0 3 VALUE { 0.007*V(1,0)-0.0013*V(2,0) }
C_C5        0 3  50UF
V_V1        0 1 DC 0V AC 01V
R_R10        0 1  83.3
R_R11        0 $N_0004  0.000001
F_F4        0 2 VF_F4 -0.3
VF_F4       $N_0001 0 0V
C_C6        0 2  {Cval}
G_G5        1 0 VALUE { -0.0013*V(2,0)-0.0013*V(3,0) }
```

B.4 Netlists of Small-signal Models of BIFRED Operating in DCM-DCM

B.4.1 Duty-ratio-to-output Voltage Transfer Function

```
G_G3        0 2 VALUE { -2.52*V(1,0)-0.003*V(3,0) }
R_R7        0 2  152
R_R8        0 3  80
R_R9        0 3  100
G_G4        0 3 VALUE { 14.5*V(1,0)+0.009*V(2,0) }
C_C5        0 3  50UF
V_V2        1 0 DC 0V AC 1V
R_R10        0 1  1G
C_C6        0 2  {Cval}
```

B.4.2 Output Impedance

```
G_G3        0 2 VALUE { 0.003*V(1,0) }
R_R7        0 2  152
R_R8        0 1  80
R_R9        0 1  100
G_G4        0 1 VALUE { 0.009*V(2,0) }
C_C5        0 1  50UF
V_V1        0 1 DC 0V AC 1V
C_C6        0 2  {Cval}
```

B.4.3 Line-to-output Voltage and Input Impedance Transfer Functions

```
G_G3        0 2 VALUE { 0.01*V(1,0)-0.003*V(3,0) }
R_R7        0 2  152
R_R8        0 3  80
R_R9        0 3  100
G_G4        0 3 VALUE { 0.01*V(1,0)+0.009*V(2,0) }
C_C5        0 3  50UF
V_V1        1 0 DC 0V AC 1V
R_R10        0 1  66.6
C_C6        0 2  {Cval}
G_G5        1 0 VALUE { -.003*V(2,0)-0.003*V(3,0) }
```

B.5 Netlists of Small-signal Models of Cascaded Boost-and-Flyback Converter Operating in DCM-CCM

B.5.1 Duty-ratio-to-output Voltage Transfer Function

```
G_G1        0 2 VALUE { 2.1*V(1,0) }
R_R1        0 2  294
R_R3        0 3  100
L_L1        $N_0001 $N_0002  0.5mH
E_E1        $N_0003 $N_0004 VALUE { 490*V(1,0)+0.3*V(2,0)-0.7*V(3,0) }
F_F1        0 2 VF_F1 -0.3
VF_F1       $N_0001 0 0V
F_F2        0 3 VF_F2 0.7
VF_F2       $N_0003 $N_0002 0V
G_G2        0 3 VALUE { -2.1*V(1,0) }
C_C2        0 3  50UF
V_V1        1 0 DC 0V AC 1V
R_R4        0 1  1G
R_R7        0 $N_0004  0.000001
C_C4        0 2  50UF
```

B.5.2 Output Impedance

```
G_G3        0 2 VALUE { 0.0037*V(3,0) }
R_R7        0 2  270.2
R_R8        0 3  270.2
R_R9        0 3  50
L_L2        $N_0001 $N_0002  0.5mH
E_E2        $N_0003 $N_0004 VALUE { 0.4*V(2,0)-0.6*V(3,0) }
F_F3        0 3 VF_F3 0.6
VF_F3       $N_0003 $N_0002 0V
G_G4        0 3 VALUE { -0.0037*V(2,0) }
C_C5        0 3  500UF
V_V3        0 3 DC 0V AC 0.1V
R_R11        0 $N_0004  0.000001
F_F4        0 2 VF_F4 -0.4
VF_F4       $N_0001 0 0V
C_C1        0 2  100UF
```

B.5.3 Line-to-output Voltage and Input Impedance Transfer Functions

```
G_G1        0 2 VALUE { 0.01*V(1,0) }
R_R1        0 2  294
R_R3        0 3  100
L_L1        $N_0001 $N_0002  0.5mH
E_E1        $N_0003 $N_0004 VALUE { 0.3*V(2,0)-0.7*V(3,0) }
F_F1        0 2 VF_F1 -0.3
VF_F1       $N_0001 0 0V
F_F2        0 3 VF_F2 0.7
VF_F2       $N_0003 $N_0002 0V
C_C2        0 3  50UF
```

```
V_V1        1 0 DC 0V AC 1V
R_R4        0 1  50
R_R7        0 $N_0004  0.000001
C_C4        0 2  {Cval}
G_G3        1 0 VALUE { -0.0034*V(2,0) }
```

B.6 Netlists of Small-signal Models of Cascaded Boost-and-Flyback Converter operating in DCM-DCM

B.6.1 Duty-ratio-to-output Voltage Transfer Function

```
R_R1        0 3  100
R_R2        0 2  320
R_R3        0 2  124
R_R4        0 3  100
C_C1        0 3  50UF
C_C2        0 2  {Cval}
G_G1        0 3 VALUE { 0.011*V(2,0) }
R_R6        0 1  10G
G_G4        3 0 VALUE { -12.3*V(1,0) }
V_V1        1 0 DC 0V AC 1V
```

B.6.2 Output Impedance

```
R_R1        0 3  100
R_R2        0 2  343
R_R3        0 2  640
R_R4        0 3  100
C_C1        0 3  50UF
C_C2        0 2  {Cval}
G_G1        0 3 VALUE { 0.008*V(2,0) }
V_V1        0 3 DC 0V AC 1V
```

B.6.3 Line-to-output Voltage and Input Impedance Transfer Functions

```
R_R1        0 3  100
R_R2        0 2  320
R_R3        0 2  135
R_R4        0 3  100
C_C1        0 3  50UF
C_C2        0 2  {Cval}
G_G1        0 3 VALUE { 0.011*V(2,0) }
R_R6        0 1  45.5
V_V1        1 0 DC 0V AC 1V
G_G5        0 2 VALUE { 0.018*V(1,0) }
G_G6        1 0 VALUE { -0.007*V(1,0) }
```

Appendix C

Computer Programs

This Appendix lists the programs used to plot the normalized specific switch stresses of cascaded converters, which are given in Chapter 4. C program used for plotting the frequency responses in order to verify the proposed cubic root approximation with that of the frequency responses generated by PSPICE is also given. These plots are used in Chapter 5.

C.1 Programs for Plotting Normalized Specific Switch Stresses

The plots generated by the programs of the following subsections are shown in Figs. 4.2 to Fig. 4.13.

C.1.1 Specific Switch Stress of Boost-and-Buck Converter in DCM-CCM

```
main()
 { float d, m1, k1, k2, m2, kc1, kc2,irms,ke, irms1[14][18],i1,i2,ia,ib,p;
  int t, n ;
  char str[11];
  printf("\n Enter the name of file:\n");
 scanf("%s" , str);
  FILE *fp;
  if ((fp = fopen( str , "w+")) == NULL) {
 printf("\n Cannot open file. \n");
 exit(1);   }
 fp = fopen(str , "w+");
  scanf("%f",&k2);
  fprintf(fp, "Boost & Buck converter operating in DCM-CCM  \n ");
  t = 0;   n = 1;
         for (m1= 1.25; m1 < 4.1 ; m1= m1 + 0.25){
  fprintf(fp,"\n %.3f ", m1);
  t = t+1;
for (d=0.1; d < 0.91; d = d + 0.05) {
 if (k2 < 1.0-d)  { goto desika;}
 else { k1 = 1.0/(m1*(m1-1.0));
 ke = k1*d*d;
  if (ke > d*(1.0-d)*(1.0-d)) {goto desika;}
else {   n = n+1;
```

```
irms = (sqrt(d + (d*(1.0-(2.0*d))/(3.0*k2*k2)) +
 (d/3.0)*((2.0/(k1*m1))+(d/k2))*((2.0/(k1*m1))+(d/k2))
 + (2.0*d/(k1*m1))*(1.0+((1.0-(3.0*d))/(3.0*k2)))))*(1.0/d);
irms1[t][n] = irms;
 ke, d*(1.0-d)*(1.0-d), k2; 1.0-d, irms);
       fprintf(fp,"\t %.3f ",irms1[t][n]);
 }  }
  desika: fprintf(fp,"\t NAN");  }  }
        fclose(fp);  }
```

C.1.2 Specific Switch Stress of Boost-and-Buck Converter in DCM-DCM

```
main()
 { float d, m1, k1, k2, m2, kc1, kc2,irms,ke, irms1, irms2;
  char str[11];
  printf("\n Enter the name of file:\n");
  scanf("%s" , str);
  FILE *fp;   if ((fp = fopen( str , "w+")) == NULL) {
 printf("\n Cannot open file. \n");
 exit(1);  }
 fp = fopen(str , "w+");
 printf("\n Enter the k2 of o/p stage :\n",k2);  scanf("%f",&k2);
  fprintf(fp, "Boost & Buck converter operating in DCM-DCM \n ");
  for (m1= 1.25; m1 < 4.1; m1= m1 + 0.25){
  fprintf(fp,"\n %.3f",m1);
  for (d = 0.1; d < 0.91; d = d + 0.05) {
  if ( k2 < 1.0-d){
  m2 = 2.0/(1.0 + sqrt(1.0+(4.0*k2/(d*d))));
  k1 = d*d/(m2*m2*m1*(m1-1.0));
  ke = k1*m2*m2;
 if (ke <= d*(1.0-d)*(1.0-d) ) {
   d*(1.0-d)*(1.0-d), 1.0-d );
irms = (sqrt((4.0*d*d*d/(3.0*k2*k2)) + (4.0*d*d*d/(3.0*k2*k2*m2*m2)) + (8.0*d*d*d/(3.0*k2*ke*m1))+
(4.0*d*d*d/(3.0*k1*k1*m2*m2*m1*m1)) - (8.0*d*d*d/(3.0*k2*k2*m2)) - ((8.0*d*d*d/(3.0*ke*k2))*(m2/m1))))*(1.0/m2) ;
  irms2 = sqrt(d/3.0)*((2.0*d/(m2*m2))*((1.0/k2)+(1.0/(k1*m1))));
  irms1 = sqrt(d/3.0)*((2.0*d/(m2*m2))*((1.0/(k1*m1))+(1.0/k2)-(m2/k2)));
  ke,d*(1.0-d)*(1.0-d), k2, 1.0-d, irms, irms1, irms2 ); */
  fprintf(fp,"\t %.3f",irms1);     }      }
  else { fprintf(fp,"\t NAN");
  goto desika; }
desika:  }  }
  fclose(fp);  }
```

C.1.3 Specific Switch Stress of Boost-and-Flyback Converter in DCM-CCM

```
main()
 { float d, m1, k1, k2, m2, kc1, kc2,irms,ke,irms1;
 char str[11];
 printf("\n Enter the name of file:\n");
scanf("%s" , str);
 FILE *fp;
 if ((fp = fopen( str , "w+")) == NULL) {
printf("\n Cannot open file. \n");  exit(1);  }
```

```
  fp = fopen(str , "w+");
  printf("\n Enter the k2 of o/p stage :\n",k2);
   scanf("%f",&k2);
   fprintf(fp, "Boost & Flyback converter operating in DCM-CCM \n ");
    for (m1= 1.25; m1 < 4.1; m1= m1 + 0.25){
   fprintf(fp,"\n %.3f ",m1);
   for (d = 0.1; d < 0.91; d = d + 0.05) {
   if (k2 > (1.0-d)*(1.0-d)) {
  m2 = d/(1.0-d);
   k1 = (1.0-d)*(1.0-d)/(m1*(m1-1.0)) ;   ke = k1*m2*m2;
   if (ke > d*(1.0-d)*(1.0-d) ) {goto desika;}
   else {  irms = (sqrt((4.0*d*d*d/(3.0*k1*k1*m1*m1*m2*m2)) +
   (2.0*d*(1.0-d)*(1.0-d)/(3.0*k1*k2*m1))
   + (d/((1.0-d)*(1.0-d))) + (d*(1.0-d)*(1.0-d)/(3.0*k2*k2)) + d/(k1*m1) ))*(1.0/m2) ;
   irms1 = (sqrt(  ( d/((1.0-d)*(1.0-d)) ) +
  (d*(1.0-d)*(1.0-d)/3.0)*( (1.0/k2)+ (1.0/(k1*m1)) )*( (1.0/k2)+ (1.0/(k1*m1)) )
   +(d/(m1*k1))*(1.0+ ((1.0-d)*(1.0-d)/(m1*k1)) ) ))*(1.0/m2);
   fprintf(fp,"\t %.3f \t %.3f \t %.3f",irms1,irms,m2);     } }
   else {  goto desika;}
desika: fprintf(fp,"\t NAN ");   } }
   fclose(fp);  }
```

C.1.4 Specific Switch Stress of Boost-and-Flyback Converter in DCM-DCM

```
 main()
{  float d, m1, k1, k2, m2, kc1, kc2,irms1[18][20], d1[20], ke,irms;
   int n, t,p;   char str[11];
   printf("\n Enter the name of file:\n");  scanf("%s" , str);
   FILE *fp;
   if ((fp = fopen( str , "w+")) == NULL) {
 printf("\n Cannot open file. \n"); exit(1);   }
 fp = fopen(str , "w+");
 printf("\n Enter the k2 of o/p stage :\n",k2);
  scanf("%f",&k2);
  printf("Boost & Flyback operating in DCM-DCM \n ");
  fprintf(fp, "Boost & Flyback converter operating in DCM-DCM \n ");
 n = 0;  t = 0;  p = 0;
for (m1= 1.25; m1 < 4.1; m1= m1 + 0.25){ fprintf(fp,"\n %.3f",m1);
t = t +1; for (d=0.1; d < 0.91; d = d + 0.05) {
  m2 = d/sqrt(k2);  k1 = k2/(m1*(m1-1.0));
ke = k1*m2*m2;
        if (k2 > (1.0-d)*(1.0-d) )  { goto desika;}
  else { m2 = d/sqrt(k2);
k1 = k2/(m1*(m1-1.0));
ke = k1*m2*m2;
  if (ke > d*(1.0-d)*(1.0-d)) {goto desika;}
else {   n = n + 1;
  irms = sqrt(d/3.0)*((2.0*d/(m2*m2))*((1.0/k2)+(1.0/(k1*m1))));
  irms1[t][n] = irms;
fprintf(fp,"\t %.3f \t %.3f",irms1[t][n],m2);   }
desika: fprintf(fp,"\t NAN"); } }
  fclose(fp); }
```

C.1.5 Specific Switch Stress of Flyback-and-Buck Converter in DCM-CCM

```
 main()
{ float d, m1, k1, k2, m2, kc1, kc2,irms,ke;
  char str[11];
  printf("\n Enter the name of file:\n");
 scanf("%s" , str);
  FILE *fp;
  if ((fp = fopen( str , "w+")) == NULL) {
 printf("\n Cannot open file. \n");
 exit(1);  }
 fp = fopen(str , "w+");
 printf("\n Enter the k2 of o/p stage :\n",k2);
  scanf("%f",&k2);
 fprintf(fp, "Flyback & Buck converter operating in DCM-CCM \n ");
   for (d =.0.1; d < 0.91; d = d + 0.05) {
  if (k2 > (1.0-d)*(1.0-d)) {  m2 = d/(1.0-d);
  fprintf(fp,"\n ");
  for (m1= 1.25; m1 < 4.1; m1= m1 + 0.25){
  k1 = (1.0-d)*(1.0-d)/(m1*(m1-1.0)) ;  ke = k1*m2*m2;
  if (ke > d*(1.0-d)*(1.0-d) ) {goto desika;} else {
 irms = sqrt((4.0*d*d*d/(3.0*k1*k1*m1*m1)) +  (2.0*d*d*d/(3.0*k1*k2*m1*m2*m2))
+ (d/((1.0-d)*(1.0-d))) + (d*d*d/(3.0*k2*k2*m2*m2)) + d*d/((1.0-d)*k1*m2*m1) ) ;
   fprintf(fp,"%.3f \t %.3f \t %.3f \t %.3f \t %.3f \t %.3f \t %.3f \t %.3f \n ", d,m1, m2,
ke, d*(1.0-d)*(1.0-d), k2,(1.0-d)*(1.0-d), irms );     }
      desika:   }   }
     else {goto desika1;}
desika1:  }
fclose(fp);   }
```

C.1.6 Specific Switch Stress of Flyback-and-Buck Converter in DCM-DCM

```
 main()
  { float d, m1, k1, k2, m2, kc1, kc2,irms,ke;
  char str[11];
  printf("\n Enter the name of file:\n");
 scanf("%s" , str);
  FILE *fp;
  if ((fp = fopen( str , "w+")) == NULL) {
 printf("\n Cannot open file. \n");
 exit(1);   }
 fp = fopen(str , "w+");
 printf("\n Enter the k2 of o/p stage :\n",k2);
  scanf("%f",&k2);
  fprintf(fp, "\n Flyback & Buck converter operating in DCM-DCM \n ");
   for (d = 0.1; d < 0.91; d = d + 0.05) {
  if ( k2 < 1.0-d){  m2 = 2.0/(1.0 + sqrt(1.0+(4.0*k2/(d*d))));
  fprintf(fp,"\n");
  for (m1= 1.25; m1 < 4.1; m1= m1 + 0.25){ k1 = d*d/(m2*m2*m1*m1);
  ke = k1*m2*m2;
 if (ke <= (1.0-d)*(1.0-d) ) {
  irms = (sqrt((4.0*d*d*d/(3.0*k2*k2)) + (4.0*d*d*d/(3.0*k2*k2*m2*m2)) + (8.0*d*d*d/(3.0*k2*ke*m1))+
  (4.0*d*d*d/(3.0*ke*ke*m1*m1)) - (8.0*d*d*d/(3.0*k2*k2*m2)) -
  ((8.0*d*d*d/(3.0*ke*k2))*(m2/m1))))*(1.0/m2)*(1.0+(1.0/m1)) ;
```

```
   fprintf(fp,"%.3f \t %.3f \t %.3f \t %.3f \t %.3f \t %.3f \t %.3f \t %.3f \n ",
  d,m1, 2.0/(1.0+ sqrt(1.0+(4.0*k2/(d*d)))), ke,(1.0-d)*(1.0-d), k2, 1.0-d, irms );  }
  else {goto desika; } desika:   }   }
  else {goto desika1;}  desika1:   }
    fclose(fp);   }
```

C.1.7 Specific Switch Stress of Flyback-and-Flyback Converter in DCM-CCM

```
   main()
    { float d, m1, k1, k2, m2, kc1, kc2,irms,ke,idrms1,idrms2,k1e;
    char str[11];
    printf("\n Enter the name of file:\n");
   scanf("%s" , str);
    FILE *fp;
    if ((fp = fopen( str , "w+")) == NULL) {
   printf("\n Cannot open file. \n");
   exit(1);  }
   fp = fopen(str , "w+");
   printf("\n Enter the k2 of o/p stage :\n",k2);
    scanf("%f",&k2);
    printf("Flyback & Flyback operating in DCM-CCM \n ");
    fprintf(fp, "Flyback & Flyback converter operating in DCM-CCM \n ");
     for (d = 0.1; d < 0.51; d = d + 0.05) {
    if (k2 > (1.0-d)*(1.0-d)) {  m2 = d/(1.0-d);
    fprintf(fp,"\n ");
    for (m1= 1.25; m1 < 4.1; m1= m1 + 0.25){
    k1 = (1.0-d)*(1.0-d)/(m1*m1) ;
 k1e = (1.0-d)*(1.0-d)/(m1*(m1-1.0)) ;
  ke = k1*m2*m2;
  (1.0-d)*(1.0-d), (1.0-d)*(1.0-d) );
  if (ke > (1.0-d)*(1.0-d) ) {goto desika;}
  else { irms = (sqrt(  ( d/((1.0-d)*(1.0-d)) ) +
  (d*(1.0-d)*(1.0-d)/3.0)*( (1.0/k2)+ (1.0/(k1*m1)) )*( (1.0/k2)+ (1.0/(k1*m1)) )
  +(d/(m1*k1))*(1.0+ ((1.0-d)*(1.0-d)/(m1*k1)) ) ))*(1.0/m2)*(1.0+(1.0/m1)) ;
   idrms1 = sqrt(4.0*d/(3.0*k1*m1));
   idrms2 = sqrt(1.0/((1.0-d)) + (1.0-d)*(1.0-d)*(1.0-d)/(3.0*k2*k2));
   fprintf(fp,"%.3f \t %.3f \t %.3f \t %.3f \t %.3f \t %.3f \t %.3f \t %.3f \t %.3f \t %.3f \n ", d,m1, m2,
ke, (1.0-d)*(1.0-d), k1e*m2*m2, k2,(1.0-d)*(1.0-d), idrms1,idrms2,irms );     }
   desika:   }   }
   else {goto desika1;}  desika1:  }
   fclose(fp);   }
```

C.1.8 Specific Switch Stress of Flyback-and-Flyback Converter in DCM-DCM

```
main()
  { float d, m1, k1, k2, m2, kc1, kc2,irms1[18][20], d1[20], ke,irms;
int n, t,p;
  char str[11];
  printf("\n Enter the name of file:\n");
 scanf("%s" , str);
  FILE *fp;
  if ((fp = fopen( str , "w+")) == NULL) {
 printf("\n Cannot open file. \n");
```

```
 exit(1);  }
 fp = fopen(str , "w+");
 printf("\n Enter the k2 of o/p stage :\n",k2);
  scanf("%f",&k2);
  fprintf(fp, "Flyback & Flyback converter operating in DCM-DCM \n ");
 for (m1= 1.25; m1 < 4.1; m1= m1 + 0.25){
fprintf(fp,"\n %.3f",m1);
for (d=0.1; d < 0.51; d = d + 0.05) {
 if (k2 > (1.0-d)*(1.0-d) )  { goto desika;}
  else { m2 = d/sqrt(k2);
k1 = k2/(m1*m1); ke = k1*m2*m2;
 if (ke > (1.0-d)*(1.0-d)) {goto desika;} else {
  irms = sqrt(d/3.0)*((2.0*d/(m2*m2))*((1.0/k2)+(1.0/(k1*m1))))*(1.0+(1.0/m1));
fprintf(fp,"\t %.3f \t %.3f",irms,m2);  }
desika: }  }
  fclose(fp);  }
```

C.1.9 Specific Switch Stress of Boost-and-Boost Converter in DCM-CCM

```
main()
 { float d, m1, k1, k2, m2, kc1, kc2,irms,ke,idrms1,idrms2,irms1;
 char str[11];
 printf("\n Enter the name of file:\n");
scanf("%s" , str);
 FILE *fp;
 if ((fp = fopen( str , "w+")) == NULL) {
printf("\n Cannot open file. \n");
exit(1);   }
fp = fopen(str , "w+");
printf("\n Enter the k2 of o/p stage :\n",k2);
 scanf("%f",&k2);
 fprintf(fp, "Boost & Boost converter operating in DCM-CCM \n ");
 for (m1= 1.25; m1 < 4.1; m1= m1 + 0.25){
 fprintf(fp,"\n %.3f",m1);
 for (d = 0.1; d < 0.51; d = d + 0.05) {
 if (k2 > d*(1.0-d)*(1.0-d)) { m2 = 1.0/(1.0-d);
 k1 = (1.0-d)*(1.0-d)*d*d/(m1*(m1-1.0)) ;
  ke = k1*m2*m2;
 if (ke > d*(1.0-d)*(1.0-d) ) {goto desika;}
else {  irms = (sqrt((4.0*d*d*d/(3.0*k1*k1*m1*m1*m2*m2)) +
(2.0*d*d*d*(1.0-d)*(1.0-d)/(3.0*k1*k2*m1))
 + (d/((1.0-d)*(1.0-d))) + (d*d*d*(1.0-d)*(1.0-d)/(3.0*k2*k2)) + d*d/(k1*m1) ))*(1.0/m2) ;
 irms1 = (sqrt(  (d/((1.0-d)*(1.0-d)) ) +
(d*d*d*(1.0-d)*(1.0-d)/3.0)*( (1.0/k2)+ (1.0/(k1*m1)) )*( (1.0/k2)+ (1.0/(k1*m1)) )
 +(d*d/(m1*k1))*(1.0+ ((1.0-d)*(1.0-d)*d/(m1*k1)) ) ))*(1.0/m2);
  fprintf(fp,"\t %.3f ",irms);   }
 else {goto desika;} desika: fprintf(fp,"\t NAN"); }}
 fclose(fp);  }
```

C.1.10 Specific Switch Stress of Boost-and-Boost Converter in DCM-CCM

```
main()
  {  float d, m1, k1, k2, x, m2, kc1,
```

```
    kc2,irms1[18][20], d1[20], ke,irms; int n, t,p;
  char str[11];
  printf("\n Enter the name of file:\n");
 scanf("%s" , str);
  FILE *fp;
  if ((fp = fopen( str , "w+")) == NULL) {
 printf("\n Cannot open file. \n");
 exit(1);   }
 fp = fopen(str , "w+");
 printf("\n Enter the k2 of o/p stage :\n",k2);
  scanf("%f",&k2);
  fprintf(fp, "Boost & boost converter operating in DCM-DCM \n ");
  for (m1= 1.25; m1 < 4.1; m1= m1 + 0.25){
fprintf(fp,"\n %.3f",m1);
for (d=0.1; d < 0.51; d = d + 0.05) {
if (k2 < d*(1.0-d)*(1.0-d) )  {
x = 1.0+(4.0*d*d/k2);
m2 = (1.0+sqrt(x))/2.0;
k1 = d*d/(m2*m2*m1*(m1-1.0));
ke = k1*m2*m2;
if (ke < d*(1.0-d)*(1.0-d))  {
fprintf(fp,"\t %.3f \t %.3f",irms,m2); }
 else{ goto desika;} desika: fprintf(fp,"\t BAM"); } }
  fclose(fp);  }
```

C.1.11 Specific Switch Stress of Flyback-and-Boost Converter in DCM-CCM

```
main(){
  float d, m1, k1, k2, m2, kc1, kc2,irms,ke,idrms1,idrms2,irms1;
  char str[11];
  printf("\n Enter the name of file:\n");
 scanf("%s" , str);
  FILE *fp;
  if ((fp = fopen( str , "w+")) == NULL) {
 printf("\n Cannot open file. \n");
 exit(1); }
 fp = fopen(str , "w+");
 printf("\n Enter the k2 of o/p stage :\n",k2);
  scanf("%f",&k2);
  fprintf(fp, "Flyback & Boost converter operating in DCM-CCM \n ");
  for (m1= 1.25; m1 < 4.1; m1= m1 + 0.25){
  fprintf(fp,"\n %.3f",m1);
  for (d = 0.1; d < 0.51; d = d + 0.05) {
  if (k2 > d*(1.0-d)*(1.0-d)) {
m2 = 1.0/(1.0-d);
 k1 = (d*d)/(m1*m1*m2*m2) ;
ke = k1*m2*m2;
if (ke > (1.0-d)*(1.0-d) ) {goto desika;}
 else {
irms = (sqrt((4.0*d*d*d/(3.0*k1*k1*m1*m1*m2*m2)) +
 (2.0*d*d*d*(1.0-d)*(1.0-d)/(3.0*k1*k2*m1))
 + (d/((1.0-d)*(1.0-d))) + (d*d*d*(1.0-d)*(1.0-d)/(3.0*k2*k2)) + d*d/(k1*m1)))*(1.0/m2)*(1.0+(1.0/m1));
 irms1 = (sqrt(  (d/((1.0-d)*(1.0-d)) ) +
(d*d*d*(1.0-d)*(1.0-d)/3.0)*( (1.0/k2)+ (1.0/(k1*m1)) )*( (1.0/k2)+ (1.0/(k1*m1)) )
```

```
  +(d*d/(m1*k1))*(1.0+ ((1.0-d)*(1.0-d)*d/(m1*k1)) ) ))*(1.0/m2)*(1.0+(1.0/m1));
    fprintf(fp,"\t %.3f ",irms);   }
  else {goto desika;} desika: } }
  fclose(fp);  }
```

C.1.12 Specific Switch Stress of Flyback-and-Boost Converter in DCM-DCM

```
main()  {
  float d, m1, k1, k2, m2, kc1, kc2,irms,ke, idrms1,idrms2 ;
  char str[11];
  printf("\n Enter the name of file:\n");
 scanf("%s" , str);
  FILE *fp;
  if ((fp = fopen( str , "w+")) == NULL) {
 printf("\n Cannot open file. \n");
 exit(1);  }
 fp = fopen(str , "w+");
 printf("\n Enter the k2 of o/p stage :\n",k2);
  scanf("%f",&k2);
  fprintf(fp, "Flyback & boost converter operating in DCM-DCM \n ");
   for (m1= 1.25; m1 < 4.1; m1= m1 + 0.25){
fprintf(fp,"\n %.3f",m1);.
   for (d=0.1; d <= 0.51; d = d + 0.05) {
 if (k2 > (1.0-d)*(1.0-d))  { goto desika;}
 else { m2 = (1.0+sqrt(1.0+4.0*d*d/k2))/2.0;
k1 = d*d/(m2*m2*m1*(m1));
  ke = k1*m2*m2;
if (ke > (1.0-d)*(1.0-d)) {goto desika;}
else {   irms = sqrt(d/3.0)*((2.0*d/(m2*m2))*((1.0/k2)+ (1.0/(k1*m1))))*(1.0+(1.0/m1));
 fprintf(fp,"\t %.3f \t %.3f ",irms,m2);   } }
  desika:  }}  fclose(fp);  }
```

C.2 Frequency Responses for Verification of Cubic Root Approximation

The curves generated by this program are used in Chapter 5 (see Figs. 5.10 and 5.12).

```
float pwr(float m, int n);
 main() {
float omega,m1,n1,f1,b1,d1,j2,a0,a1,a2,zero1,root1,root2,root3,f,g2,b,
d,r,l1,l2,c1,c2,vc,e,k,k1,k2,c,q,r1;
char str[11];
 FILE *fp;
printf("\n Enter the inductance of PFC stage in mH:\n",l1);  scanf("%f",&l1);
printf("\n Enter the inductance of O/P stage in mH:\n",l2);  scanf("%f",&l2);
printf("\n Enter the capacitance of O/P stage in UF:\n",c2); scanf("%f",&c2);
printf("\n Enter the capacitance of I/P stage in UF:\n",c1); scanf("%f",&c1);
printf("\n Enter the resistance of O/P stage:\n",r);  scanf("%f",&r);
printf("\n Enter the switching frequency in KHz;\n",f);  scanf("%f",&f);
printf("\n Enter the Steady state duty ratio:\n",d);  scanf("%f",&d);
printf("\n Enter the input voltage:\n",e);  scanf("%f",&e);
printf("\n Enter the name of file:\n");  scanf("%s" , str);
 if ((fp = fopen( str , "w+")) == NULL) {
```

```
printf("\n Cannot open file. \n");
exit(1);  }
fp = fopen(str , "w+");
       fprintf(fp,"\n The inductance of PFC stage is %.4f mH \n",l1);
fprintf(fp,"\n The inductance of O/P stage is %0.4f mH \n",l2);
fprintf(fp,"\n The capacitance of O/P stage is %.4f UF \n",c2);
fprintf(fp,"\n The capacitance of I/P stage is %.4f UF \n",c1);
fprintf(fp,"\n The resistance of O/P stage is %.4f ohm \n",r);
fprintf(fp,"\n The switching frequency is %.2f KHz;\n",f);
fprintf(fp,"\n The Steady state duty ratio is %.4f \n",d);
fprintf(fp,"\n The input voltage is %0.2f \n",e);
vc = (e/2.0)*(1.0 +sqrt(1.0 + ((2.0*r)/(f*l1)) )  );
c =  (vc/e)-1.0;
g2 = (d*d/(2.0*l1*f))*(1.0/(c*c));
 j2 = (d*e)/(c*f*l1) - d*vc/r ;
fprintf(fp,"\n Low frequency energy storage capacitor voltage: %0.2f volts\n",vc);
fprintf(fp,"\n G22: %.4f J2: %.2f \n",g2,j2);
  j2 = (d*e)/(c*f*l1) - d*vc/r ;
 k1=2.0*l1*f*d*d/r ;
 k2=2.0*l2*f/r ;
fprintf(fp,"\n zero's part: %.4f \n",(d*j2)/(g2*vc));
fprintf(fp,"\n c1 \t a2 \t a1 \t a0 \t zero1 \t root1 \t root2,3 \n");
omega = 0.0;
if (k1 < (d*(1.0-d)*(1.0-d)) && k2 > (1.0-d)){
for (omega = 0.01; omega <= 100001.0; omega = omega + 10.0){
  fprintf(fp,"\n %.3f",omega*7.0/44.0);
  for (c2 = 10.0; c2 < 4000.10; c2 = c2+ 3990.0) {
a2 = ((l2*c1 + l2*c2*g2*r)/(pwr(10.0,9)))/((l2*c2*c1*r)/pwr(10.0,15));
a1  = ((d*d*c2*r/pwr(10.0,6)) + g2*l2*0.001 + (c1*r/pwr(10.0,6)))/
 ((l2*c2*c1*r)/pwr(10.0,15));
 a0 = (d*d + g2*r)/((l2*c2*c1*r)/pwr(10.0,15));
  j2 = (d*e)/(c*f*l1) - d*vc/r ;
 root1 = -(d*d + g2*r)/((d*d*c2*r/pwr(10.0,6)) + g2*l2*0.001 + (c1*r/pwr(10.0,6)));
 b= root1 + a2;  k = b*b - 4.0*a1;
 zero1 = ((-g2*pwr(10,6))/c1)*(1.0 + (d*j2)/(g2*vc));
 f1 = ((a0/a1)*(a0/a1)*(a2 - (a0/a1)))/a1;
 if(k<0.0){ b1 = -b/2.0;
 d1 = sqrt(4.0*a1-b*b)/2.0;
 n1= 20.0*log10(1.0/(sqrt(pwr((b1*b1 + d1*d1 - omega*omega),2)+ pwr((-2.0*b1*omega),2))));
 m1 = 20.0*log10(vc) +  n1 + 20.0*log10(b1*b1 + d1*d1)
 + 20.0*log10(sqrt((zero1*zero1 + omega*omega)/(root1*root1 + omega*omega)))
  + 20.0*log10(-1.0*root1) + 20.0*log10(-1.0/zero1);
   fprintf(fp,"\t %.2f", m1); }
  else  { root2 = (-b/2.0)+ sqrt(-4.0*a1 + b*b)/2.0 ;
 root3 =  (-b/2.0)- sqrt(-4.0*a1 + b*b)/2.0 ;
 m1 = 20.0*log10(sqrt((zero1*zero1 + omega*omega)/(root1*root1 + omega*omega)))
 + 20.0*log10(vc) + 20.0*log10(1.0/sqrt(root2*root2 + omega*omega))
 + 20.0*log10(1.0/sqrt(root3*root3 + omega*omega));
   fprintf(fp,"\t %.2f", m1);     } } } }
 else { fprintf(fp,"\n The PFC-Converter is NOT operating in desired mode! \n");}
 fclose(fp);  }
 float pwr(float m, int n)
 {   float t=1.0;
 for(;n;n--) t = t*m;
 return t;  }
```

Publications

1. V. S. Murali and C. K. Tse, "Computer Based Implementation of Extra Element Theorem," *IEEE International Symposium on Circuits and Systems*, pp. 141-144, June 1997.

2. V. S. Murali, C. K. Tse and M. H. L. Chow, "Small-Signal Dynamical Analysis of Single-stage Cascaded Boost-and-Buck PFC Converters," *IEEE Power Electronics Specialists Conference Record*, May 1998, accepted.

3. V. S. Murali and C. K. Tse, "Comparison of Small-Signal Dynamics of BIFRED and Single-Stage Cascaded Boost-and-Flyback PFC Converters," *IEEE Power Electronics Specialists' Conference Record*, May 1998, accepted.

4. V. S. Murali and C. K. Tse, "Implementing Extra Element Theorem Using Nullor Approach," *International Journal of Circuit Theory and Applications*, revised on 5th Jan 1998.

5. V. S. Murali, C. K. Tse and M. H. L. Chow, "Small-Signal Dynamical Analysis of Single-stage Cascaded Boost-and-Buck PFC Converters," *IEEE Transactions on Power Electronics*, under preparation.

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