Analysis and Design of Switching Converters for Power Factor Correction Applications

by

Dylan Dah-Chuan LU

A thesis submitted in partial fulfillment of the

requirements for the Degree of

Doctor of Philosophy

in the Department of Electronic and Information Engineering

The Hong Kong Polytechnic University

Hong Kong SAR, China

February 2004

CERTIFICATE OF ORIGINALITY

I hereby declare that this thesis is my own work and that, to the best of my knowledge and belief, it reproduces no material previously published or written, nor material which has been accepted for the award of any other degree or diploma, except where due acknowledgement has been made in the text.

_____ (Signed)

_____ (Name of student)

Abstract

of the thesis entitled
"Analysis and Design of Switching Converters for Power Factor Correction Applications"
submitted by Dylan Dah-Chuan Lu
for the Degree of Doctor of Philosophy
at The Hong Kong Polytechnic University in February 2004

Switching converters for power factor correction (PFC) applications generally adopted a two-stage approach consisting of two individual power stages - PFC stage and DC/DC regulation stage. Depending on the output power level, the two stages are put together into either serially-connected individually-controlled or serially-connected integrated-control configuration. This thesis presents the analysis and design of some converter topologies and control circuits to improve the performance of the switching converters for both configurations.

For high power level, a PFC pre-regulation converter is connected in series with a DC/DC regulation converter and each power stage has its own control circuitry. Due to the continuous-conduction-mode (CCM) operation of the input inductor, the rectifier reverse-recovery transition causes switching loss and electromagnetic interference (EMI) problems. In this thesis, a CCM boost converter suitable for PFC application is studied. A passive low-loss snubber using a pair of coupled inductors is proposed so that all the rectifiers turn off softly. The power switch is also operating in low-voltage turn-on condition, further reducing the switching loss.

For low to medium power levels, the PFC pre-regulation converter and the DC/DC regulation converter are basically serially-connected but they share the common switch(es) to simplify the power stages and control circuitry (integrated-control). We refer to this arrangement as single-stage PFC approach. However, this configuration causes substantial voltage and current stresses on the passive and active components of the converter and results in low conversion efficiency. An improved converter topology is then presented using the direct power transfer approach to reduce the stresses on the components. We refer to this arrangement

as parallel-connected integrated-control configuration. Experimental results show that the conversion efficiency is improved. The approach is then extended to derive a flyback-topology based single-switch single-stage PFC converter to loosely regulate the storage capacitor voltage using the regulated output voltage. The range of change of storage capacitor voltage against change of line voltage is significantly reduced.

In an attempt to provide more rigorous regulation of the storage capacitor voltage and to provide stand-by mode operation, an auxiliary bi-directional switch is added to the single-stage PFC converter. This auxiliary switch is operated in zero-voltage-switching (ZVS) condition and is connected in series with the storage capacitor to control the storage capacitor voltage. Besides, this switch helps to create a direct power transfer path for input power to output load and reduce the storage capacitor voltage stress at light load condition. A simple single-loop control method is also proposed to achieve power factor correction, output voltage regulation and control of storage capacitor voltage simultaneously.

Experimental results to verify the operation and analysis of the proposed circuit topologies are given. Comparative results (based on calculation or experiment) are also given to prove the proposed approaches effective.

Publications

Journal Papers

1. D.D.C. Lu, D.K.W. Cheng and Y.S. Lee, "Reduction of Current and Voltage Stresses in Single-Stage AC/DC Power Factor Correction Converters with Reduced Repeated Power Processing and Inherent Input Current Control", *Journal of Circuits, Systems and Computers (Special Jubilee Issue on Power Electronics)*. (Accepted for publication)

2. D.D.C. Lu, D.K.W. Cheng and Y.S. Lee, "Analysis and Design of a Single-Stage Single-Switch Power-Factor-Corrected Converter with Direct Power Transfer", *IEICE Transactions on Communications*, vol. E86-B, no. 12, pp. 3606-3613, December 2003.

3. D.D.C. Lu, D.K.W. Cheng and Y.S. Lee, "A Single-Switch AC/DC Converter with Voltage Regulated Storage Capacitor", *IEEE Power Electronics Letters*, vol. 1, no. 3, pp. 78-82, September 2003.

4. D.D.C. Lu, D.K.W. Cheng and Y.S. Lee, "Single-Stage AC-DC Power-Factor-Corrected Voltage Regulator with Reduced Intermediate Bus Voltage Stress", *IEE Proc., Electric Power Applications*, vol. 150, no. 5, pp. 506-514, September 2003.

5. D.D.C. Lu, D.K.W. Cheng and Y.S. Lee, "A Single-Switch Continuous-Conduction-Mode Boost Converter with Reduced Reverse-Recovery and Switching Losses", *IEEE Transactions on Industrial Electronics*, vol. 50, no. 4, pp. 767-776, August 2003.

International Conference Papers

1. D.D.C. Lu, D.K.W. Cheng, and Y.S. Lee, "Storage Capacitor Voltage Control of Single-stage AC/DC PFC Converter", Proceedings, *IEEE Power Electronics Specialists Conference 2004 (PESC)*, June 2004, pp. 3794-3797, Germany.

2. D.D.C. Lu, D.K.W. Cheng, and Y.S. Lee, "A Single-Stage AC-DC High Power Factor Voltage Regulator with Reduced Intermediate Bus Voltage Stress", Proceedings, *IEEE Power Electronics Specialists Conference (PESC)*, June 2003, pp. 663-668, Mexico.

3. D.D.C. Lu, D.K.W. Cheng, and Y.S. Lee, "Single-Switch Flyback Power-Factor-Corrected AC/DC Converter with Loosely Regulated Intermediate Storage Capacitor Voltage", Proceedings, *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2003, pp. 264-267, Bangkok, Thailand.

4. D.D.C. Lu, D.K.W. Cheng, and Y.S. Lee, "A Single-Switch Power-Factor-Corrected Converter with Reduced Repeated Power Processing", Proceedings *IEEE Power Electronics and Drive Systems (PEDS)*, Oct 2001, pp. 26-32, Bali, Indonesia.

5. D.D.C. Lu, D.K.W. Cheng, and Y.S. Lee, "A Novel Single-Phase Power-Factor-Corrected Voltage Regulator", Proceedings, *IEEE Power Electronics Specialists Conference (PESC)*, 17-22 June 2001, pp. 936-941, Vancouver BC, Canada.

Acknowledgements

I would like to express my sincere thanks to my supervisor Dr. David Cheng, for his guidance and support during my studies. His encouragement has made undertaking this studies a pleasure. During the past four years working in his group, I have been given the opportunity to pursue my own scientific and engineering interests while learning to investigate complexity in power electronics systems through numerous discussions with him. His professional knowledge has guided me to think wider and deeper. I have learned much from him.

I would also like to thank my co-supervisor Prof. Y. S. Lee, for his constructive comments and suggestions throughout my studies. His enthusiasm for power electronics, and his commitment to his students have been an inspiration to me.

Thanks to my many friends and colleagues of the Power Electronics Research Centre: Mr. Adrian Wong, Dr. Alex Wong, Mr. Martin Cheung, Dr. Xiao Sun, Dr. Herbert Iu, Dr. J. Feng, Dr. K. W. Siu, Mr. S. H. Wong, Mr. C. P. Lee, Mr. Y. L. Cheng, Mr. Steve Ling, Mr. Eric Leung, Mr. Edward Ho, Mr. Wallace Ho, Mr. T. S. Chong, Ms. Yi Chen, Mr. Wen Wei, Ms. Ella Kan, and Mr. Leo Tung, for spending enjoyable hours with me, at different times, discussing technical issues, culture, life and religion. I especially thank my best friend Kenneth To, who has encouraged me over the past difficult years.

I gratefully acknowledge the Research Committee of The Hong Kong Polytechnic University for her financial support during the entire period of my candidature.

I thank my parents, my grandparents, my sister and brother-in-law, for their

love, care and patient over the years. I wish very much that my grandma could be present to witness the completion of this work. I will miss her greatly.

I thank my girlfriend Maria, who has stood with me and positively influenced my life. We have shared memorable happy times till now. Her encouragement has always been a comfort to me whenever I was undergoing hardships.

Thanks and praise be to God, who makes all things possible. He is my provider and His grace is sufficient for me. To Him be all the glory and love.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Background and Motivation

Power electronics is an enabling technology for all electrical and electronic apparatus requiring electric power to drive. Over the past twenty years, the power electronics industry has grown tremendously. Its growth is a result from increasing demand of reliable, efficient, compact and cost effective power supplies for telecommunication, computer, and motor drive industries as well as for medical equipments and military use. This growth is facilitated by the significant improvement in semiconductor technology in which smaller packaging and higher power handling devices have been marketed. In response to the advancement in semiconductor and magnetics technology, power electronics researchers and engineers have strived to thoroughly employ these technologies through new circuit design and topologies, optimized control and packaging techniques, in order to meet the industry demands.

At present, AC/DC power supplies share a large market because they are dominated by consumer products such as cellular phones, notebook and personal computers, power tools, flatbed scanners and digital cameras. In particular, for computer products which require power supplies with higher output power or output current are of increasing demand. This is mainly due to the increasing computational speed and power of the central processing unit (CPU) and the

increasing number of peripherals connected to the computer.

For the simplest and cost-effective design of AC/DC power supplies, a large capacitive filter is placed in between the bridge rectifier and the load. However, such power supplies introduce undesirable harmonic currents to the utility. These harmonic currents cause severe problems such as voltage distortion, heating, noise and reduced available power from the line. Agencies such as International Electrotechnical Commission (IEC) imposed limit (IEC 61000-3-2) to the harmonic currents drawn by the off-line power supplies. The restraint of harmonic currents promptly drives the direction of research to power factor correction (PFC) to improve the quality of input current.

Research on PFC generally falls into two categories: active and passive approaches. Passive PFC uses only passive elements such as inductors, capacitors and rectifiers while active PFC uses switching devices such as transistors in addition to the passive elements. The passive PFC approach enjoys high efficiency, low cost and low electromagnetic interference (EMI) at the expense of large volume and weight. The active PFC approach, having a higher power factor but larger noise, follows closely to the market trend of electronic equipment minimization and advanced technology of packaging.

For high power applications with PFC function, a continuous-conduction-mode (CCM) boost converter is the preferred topology. Due to its simple circuitry, low component stress and favourable placement of input inductor, the CCM boost converter becomes the standard PFC converter in most high power off-line power supplies. However, with CCM operation, the boost converter suffers from extra power dissipation and EMI due to the reverse-recovery current of the output rectifier. To reduce the reverse-recovery current, many have proposed passive or active snubbers to remedy this problem. Although much work has been done in this area, few have successfully shown improvement with minimum component count, soft turn-off of power devices, and least circulation current.

At present, a common practice to achieve high quality input current and tight output regulation is to connect a PFC converter circuit serially to a DC/DC

regulator circuit. This, the two-stage approach, is by far the best option in large AC/DC power supplies , due to the optimized DC/DC regulator stage and the controlled input current, output voltage and intermediate storage capacitor voltage. However, for low to medium power applications, the component count, size, and manufacturing cost of the two-stage approach are not well justified [1]. This motivated researchers to simplify the power-stage and control circuits by combining the two-stage circuits using the so-called single-stage approach.

The single-stage approach is developed by rebuilding the two-stage circuits using shared switch(es) and the so-called integrated control. Typical examples can be found from references [17]-[22]. In this way, however, the switch(es) can only control either two out of the three critical circuit parameters, input current, storage capacitor voltage and output voltage, through duty ratio and switching frequency modulations. In most cases, the output voltage is controlled by duty ratio to give tight output regulation. Although switching frequency modulation may be employed to control the voltage stress on the storage capacitor voltage, it is difficult to completely suppress the stress over a wide range of line and load changes. Besides, the common switch suffers from high current stress and low conversion efficiency due to repeated input power processing.

1.2 Objectives

This thesis is intended to systematically address the major technical issues in existing AC/DC switching converters with PFC applications (active PFC approach). Firstly, a low-loss passive snubber is proposed for a CCM boost converter suitable for high-power PFC applications. All the rectifiers can turn off softly and clamped to the output voltage. The power switch also operates on low-voltage turn-on condition to reduce switching loss. Secondly, an auxiliary transformer is added to the single-stage PFC converter to reduce the storage capacitor voltage stress. Thirdly, a dual-output flyback transformer is added to control the storage capacitor voltage by the output voltage feedback. The storage capacitor voltage is found loosely regulated throughout the line and load ranges.

Finally, a simple direct storage capacitor voltage control method is proposed. An auxiliary bi-directional switch is inserted serially with the storage capacitor. By controlling the on-time ratio of the auxiliary switch to that of the main switch according to change of line voltage, the control of storage capacitor voltage and output voltage can be achieved in a single-control loop. Extensive simulation and experimental results confirmed the proposed solutions effective. The organization of the thesis is summarized in the following section.

1.3 Contributions

In this section, we summarize the original contributions of this thesis to the field of power electronics. These contributions are related to the development of switching power converters with PFC applications. These includes the following:

1. Have proposed a passive snubber for CCM boost PFC converter using a pair of coupled inductors and two additional rectifiers. Not only all the rectifiers turn-off softly, their voltages are clamped to output voltage. The coupled inductors also assist low-voltage turn-on transition for the main power switch.

2. Have applied the direct power transfer approach on single-stage PFC (S^2PFC) converters to solve the high voltage and current stresses and low conversion efficiency problems. An auxiliary transformer is added to the input stage of a boost-flyback S^2PFC converter to achieve such purposes. A detailed analysis is performed on DCM and CCM operation.

3. Have derived a S^2PFC converter with a dual-output flyback transformer to further minimize the fluctuation of storage capacitor voltage against change of line voltage. By using a single switch, the proposed converter achieves simultaneously high power factor, loosely regulated storage capacitor voltage and tight output voltage.

4. Have proposed a direct control of the storage capacitor voltage for a S^2PFC converter. An auxiliary bi-directional switch is added in series to the storage

capacitor. This auxiliary switch also provides standby power mode feature for the converter to cutoff the PFC stage to save power.

1.4 Outline of the Thesis

Chapter 2 outlines the basics and potential problems of AC/DC switching converters. In this chapter, a boost converter for power factor correction (PFC) application is discussed. This includes the operating principle, modes of operation and control strategies issues. In particular, the continuous-conduction-mode (CCM) operation is mentioned due to the severe rectifier reverse-recovery problem. Based on the two-stage approach to implement PFC and output voltage regulation functions, the single-stage approach and its potential problems are explained. This chapter provides information about the problems associated with AC/DC converters for PFC and serves as an introduction to the techniques proposed in the subsequent chapters of this thesis.

Chapter 3 presents a technique to solve the reverse-recovery and switching losses in a CCM boost converter. A passive snubber using coupled inductors and two rectifiers is introduced. All the rectifiers are turned off softly and clamped to the output voltage. In addition, the power switch operates in low-voltage turn-on condition which reduces the switching loss. Detailed operating principle and analysis are presented. This chapter also considers the criteria to reduce the reverse-recovery loss and to design the required inductance for proper operation. Experiments are performed to verify the theoretical analysis and the effectiveness of the proposed approach.

Chapter 4 introduces a method to reduce the voltage and current stresses in the single-stage PFC approach. An auxiliary transformer is added to provide a direct power transfer path for input power to output load. The DCM and CCM operations of this transformer are discussed. Detailed analysis of reducing the stresses is given. Hardware prototypes are implemented and tested to confirm the proposed method. It is found from experiments that the conversion efficiency is also improved.

Chapter 5 proposes a technique to further control the voltage stress on the storage capacitor. By using a dual-output flyback transformer, the storage capacitor voltage is loosely regulated by the controlled output voltage. The transformer leakage inductance is considered in order to identify the discrepancy in the theoretical analysis. The analysis of input current due to the circuit operation is carried out. Experimental results on a 70W prototype verify the technique and the analysis.

Chapter 6 presents the direct control of the storage capacitor voltage. An auxiliary bi-directional switch is inserted in series with the storage capacitor to control its voltage. This switch works in zero-voltage-switching (ZVS) condition and assists the provision of direct power transfer feature. This chapter begins with neglecting the storage capacitor voltage control loop. It is found that the duty ratio is a function of the load so that the storage capacitor voltage decreases naturally when the load becomes light. The experimental results verify the theoretical analysis of this phenomenon. Further, a simple single control loop, which incorporates both the control of storage capacitor voltage and output voltage, is derived. The control concept is confirmed by simulation results.

Chapter 7 gives some suggestion for future work and concludes the thesis by summarizing the important results that have been established from the analysis and design for switching converters for PFC applications.

Chapter 2

Switching Converters for Power Factor Correction (PFC)

2.1 Introduction

In general, all DC/DC converters can implement AC to DC conversion. However, boost converter is a preferred topology among the basic DC/DC converters such as buck and buck-boost converters, especially for power factor correction (PFC) application. In this chapter, the operating principle of DC/DC boost converter is explained. Different control approaches to achieve PFC at three distinct modes of operation: discontinuous-conduction-mode (DCM), boundary-conduction-mode (BCM) and continuous-conduction-mode (CCM) for boost converter are discussed. Among the three modes of operation, the CCM operation causes the most severe rectifier reverse-recovery problem. Various snubber methods to reduce the reverse-recovery current are discussed. In order to achieve PFC and tight output regulation simultaneously, two power stages are required. This chapter further presents the basic concepts of single-stage PFC approach. It consists of functionally two power stages but integrates the PFC and DC/DC regulator circuits by sharing the same switch(es). The potential problems in single-stage approach for PFC are addressed.

2.2 Power Factor Correction (PFC)

2.2.1 Definitions

For a given voltage $v(t)$ with period T applying across a load Z_L, the current flowing through Z_L is $i(t)$. The power factor (PF) is then defined as the ratio of the average power $P_{average}$ to the apparent power $P_{apparent}$ flowing through Z_L.

$$PF = \frac{P_{average}}{P_{apparent}} \tag{2.1}$$

where

$$P_{average} = \frac{1}{T}\int_0^T v(t) \cdot i(t)dt \tag{2.2}$$

$$P_{apparent} = V_{rms} \cdot I_{rms} \tag{2.3}$$

where V_{rms} and I_{rms} represent the root mean square (rms) values of load voltage and current respectively. Active power is the power that is actually absorbed by the load, whereas apparent power is the power that would be absorbed by the load if it were resistive. Given a sinusoidal voltage $v(t)$,

$$v(t) = V_1 sin(\omega t + \theta_1) \tag{2.4}$$

If $v(t)$ is applied across a nonlinear load, the current waveform will be non-sinusoidal but can be expressed by Fourier series,

$$i(t) = I_o + \sum_{n=1}^{\infty} I_n sin(n\omega t + \theta_2) \tag{2.5}$$

Substituting (2.4) and (2.5) into (2.2) and assuming net $i(t)$ is zero (i.e. I_o=0), we get

$$P_{average} = \frac{V_1 I_1}{2} cos(\theta_1 - \theta_2) = V_{1,rms} I_{1,rms} cos(\theta_1 - \theta_2) \tag{2.6}$$

Putting (2.6) into (2.1), it becomes

$$PF = \frac{I_{1,rms}}{I_{rms}} \cdot cos(\theta_1 - \theta_2) \tag{2.7}$$

Note that V_{rms} in (2.3) equals $V_{1,rms}$ in (2.2) as the input voltage is purely sinusoidal. The latter term is called the displacement factor (DpF), which indicates the phase difference between the voltage and current waveform. The former term

in (2.7) is called the distortion factor (DtF), which indicates the non-sinusoidal property of the voltage waveform and/or current waveform (current only in this case). The total rms current I_{rms} can be expressed as the sum of harmonic currents,

$$I_{rms} = \sqrt{\sum_{n=0}^{\infty} I_{n,rms}^2} \tag{2.8}$$

The total harmonic distortion (THD) of the load current is given by,

$$THD = \sqrt{\frac{I_{rms}^2 - I_{1,rms}^2}{I_{1,rms}^2}} \tag{2.9}$$

For in this case, $v(t)$ is a pure sinusoidal voltage and is applied to a nonlinear load, DtF can be expressed as,

$$DtF = \sqrt{\frac{1}{1+THD^2}} \tag{2.10}$$

If the load current $i(t)$ is in phase with the voltage $v(t)$ (i.e. DpF = 1), THD can be related to PF as

$$THD = \sqrt{\frac{1-PF^2}{PF^2}} \tag{2.11}$$

For instance, a power factor of 0.95 would yield a THD of 32.9%. This implies a relatively high power factor can still yield a conceivably large THD.

2.2.2 Compliance Specifications

In order to limit the harmonic content of input current drawn from AC mains by the electrical and electronic equipment, compliance requirements for low AC current harmonic distortion are being enforced by national and international regulating bodies. The International Electrotechnical Commission (IEC) details the current harmonic limits in document IEC 61000-3-2. The IEC has representation in major nations, primarily in Europe. (For in the US presently, they adopted the IEEE 519-1992 standard.) The original version of IEC 61000-3-2 regulation was published in 1995 [2], but it has been recently modified since October 2001 [3].

The purpose of IEC 61000-3-2 is to deal with the limitation of harmonic currents injected into the public supply system. The requirements of IEC 61000-3-2 apply to electrical and electronic equipment having an input current up to

and including 16A per phase, and intended to be connected to public low-voltage distribution systems. For systems with nominal voltages less than 220V (line-to-neutral), the limits have not yet been considered. For the purpose of harmonic current limitation, equipment is classified as follows:

Class A: Balanced three-phase equipment;
Household appliances excluding equipment identified as class D;
Tools, excluding portable tools;
Dimmers for for incandescent lamps; audio equipment.

Class B: Portable tools;
Arc welding equipment which is not professional equipment.

Class C: Lighting equipment.

Class D: Personal computers and personal computer monitors;
Television receivers.

The major change in the new regulation is how to classify Class D equipment. In the first edition, Class D was applied to equipment with a special waveform that fitted a template defined by the regulation. In the modified version, this Class D line current waveform template has been removed. In addition, the Class D harmonic limit specifications must now be applied to equipment with a maximum input power less than or equal to 600W, relating personal computers and television receivers.

In order to aid in determining into which class a piece of equipment belongs, the IEC 61000-3-2 provides the flow chart of Figure 2.1. For Class A equipment, the harmonics of the input current shall not exceed the values given in Table 2.1. The limits for Class B equipment shall be 1.5 times the limits of Table 2.1. The limits for Class C are listed in Table 2.2. The limits for lighting equipment is subject to the type and range of input power of the lighting equipment, and is out of the scope of this dissertation. The limits for Class D equipment are defined according to the rated load, as listed in Table 2.3. It is noted that the limits are not specified in the standard for the equipment with a rated power of 75W or less, other than lighting equipment (This value may be reduced to 50W in the future) and professional equipment with a total rated power greater than 1kW.

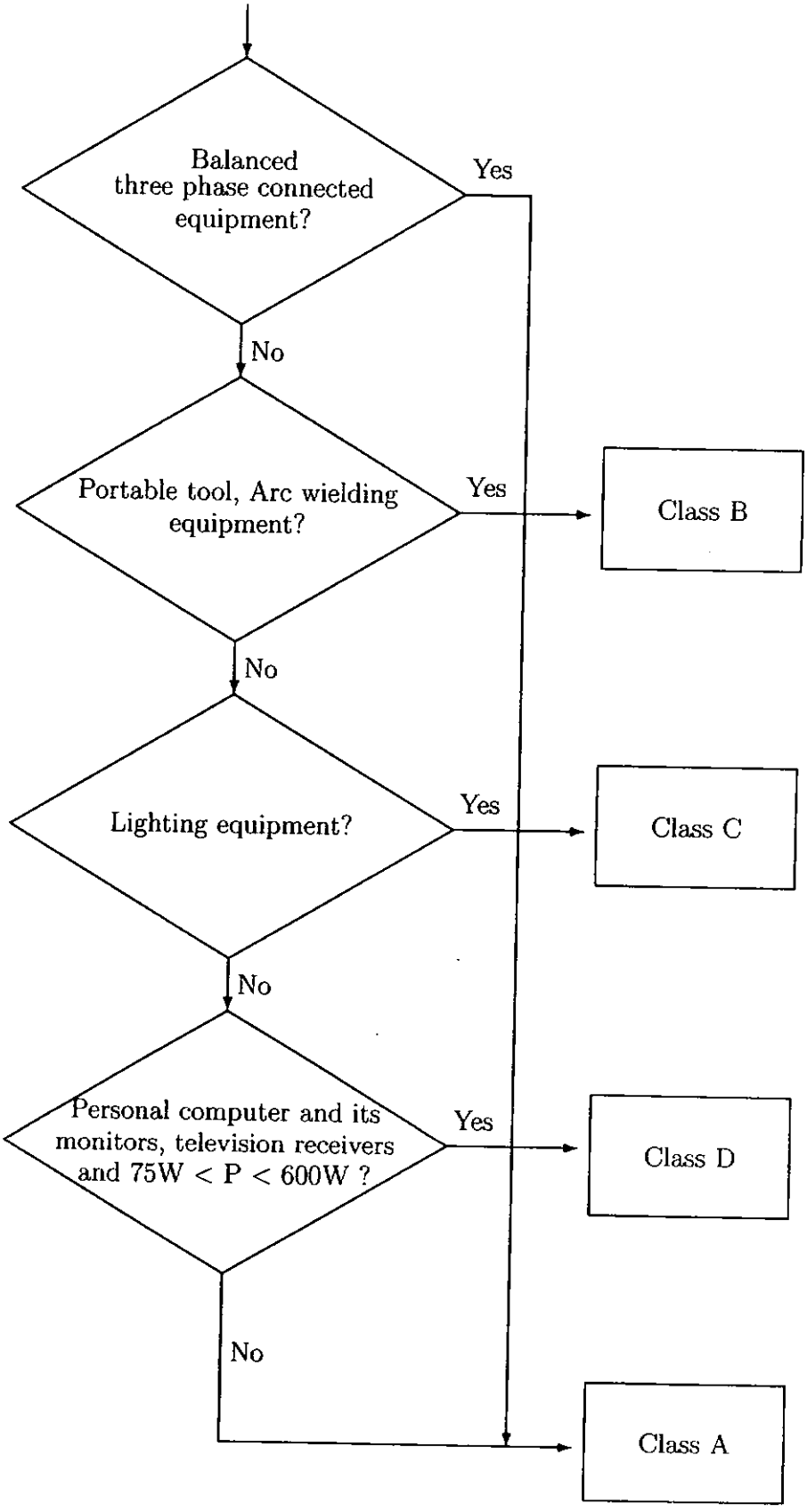


Figure 2.1: IEC 61000-3-2 equipment classification flowchart.

Harmonic order n	Maximum permissible harmonic current A
Odd harmonics	
3	2.30
5	1.14
7	0.77
9	0.40
11	0.33
13	0.21
$15 \leq n \leq 39$	$0.15\ (\frac{15}{n})$
Even harmonics	
2	1.08
4	0.43
6	0.30
$8 \leq n \leq 40$	$0.23\ (\frac{8}{n})$

Table 2.1: Limits for Class A equipment

Harmonic order n	Maximum permissible harmonic current expressed as a percentage of the input current at the fundamental frequency %
2	2
3	$30 \cdot \lambda^*$
5	10
7	7
9	5
$11 \leq n \leq 39$ (Odd harmonics only)	3
$^*\lambda$ is the circuit power factor	

Table 2.2: Limits for Class C equipment

Harmonic order n	Maximum permissible harmonic current per watt mA/W	Maximum permissible harmonic current A
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
$13 \leq n \leq 39$ (odd harmonics only)	$\frac{3.85}{n}$	see Table 2.1

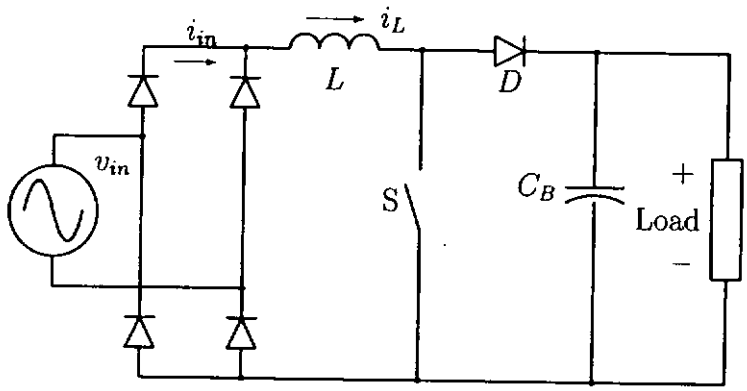
Table 2.3: Limits for Class D equipment

2.3 DC/DC Switching Converter Topologies for PFC Application

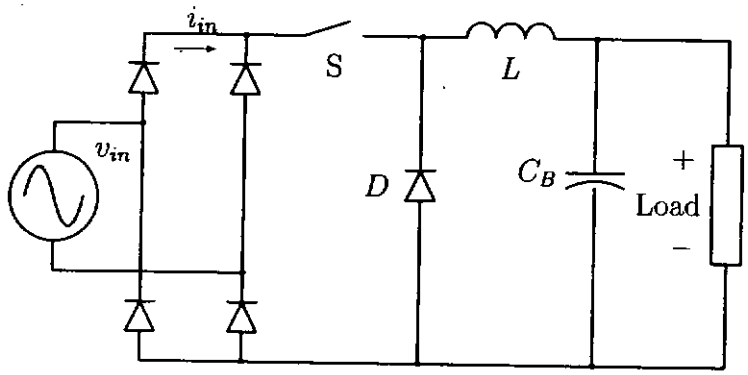
Although passive PFC approach using only inductors and capacitors can achieve fairly good power factor, the intention of this thesis is to focus on the active approach where switching transistors (using cutoff and saturation regions) and rectifiers are being used in addition to inductors and capacitors.

Generally, all switching DC/DC converters can use for implementing PFC function. The most commonly used basic DC/DC converters are boost, buck and buck-boost converters. They represent the simplest form of DC/DC converters as only one inductive storage element is needed to store and transfer energy from a voltage source to an output load. To implement PFC function, the input voltage source is just replaced by an AC voltage source and follows by a bridge-rectifier. Figure 2.2 shows the configuration of boost, buck and buck-boost PFC converters.

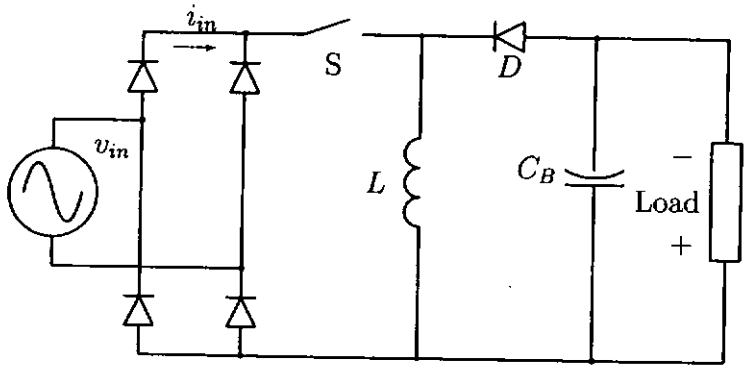
Among the three basic converters, the boost converter has the most desirable features for implementing PFC. Firstly, the input inductor of the boost converter is inserted serially with the bridge-rectifier and AC voltage source. This shapes the input current continuously and smoothly follows the input voltage when the inductor works in continuous conduction mode (CCM). For buck converter, the



(a) Boost



(b) Buck



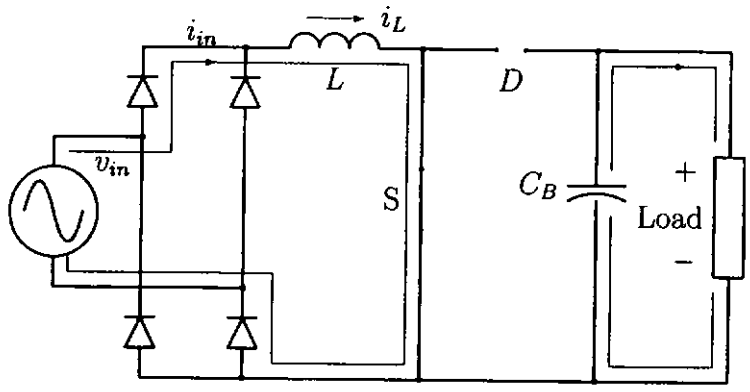
(c) Buck-boost

Figure 2.2: Circuit diagram of basic DC/DC converters for PFC implementation.

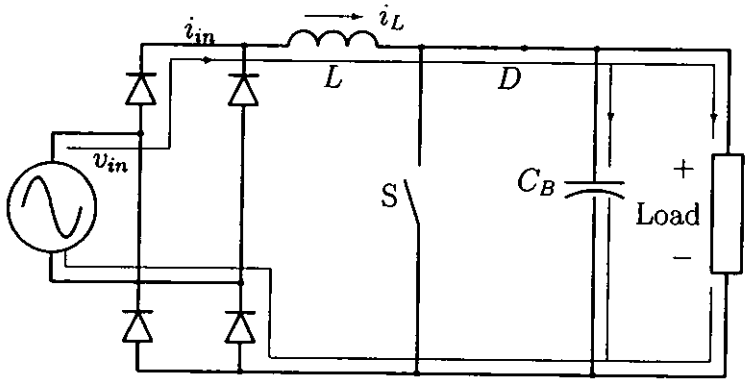
input current cannot flow during the line period where the input voltage is lower than the output voltage. This causes input current distortion and generate high current harmonics. Both buck and buck-boost converters draw pulsating input currents that generate high harmonic currents in any mode of operation. Secondly, due to the pulsating currents of the buck and buck-boost converters, the electromagnetic interference (EMI) noise is much larger than that of boost converter. A larger input filter is needed to attenuate the high frequency noise. Thirdly, after the switch S turns off, the drain-to-source voltage (say MOSFET is used) of the boost converter is clamped to the output voltage. The switching loss is reduced comparing to that of buck and buck-boost converters because their switches are subjected to parasitic oscillation due to the series LC arrangement. Fourthly, the source pin of the boost converter switch is connected to the common ground while the switch ends of buck and buck-boost converters are floating. Additional use of isolated gate drive or level-shift technique to drive the switch in buck and buck-boost converters is required and that increases the overall size and cost.

2.4 Modes of Operation of Boost Converter

The basic operating principle of the boost converter, as shown in Figure 2.3, is described as follows. When the switch S is turned on, it represents a short circuit or a small value resistance (usually a few hundred milli-ohms in MOSFET) and the inductor L is charged up linearly by the rectified input voltage. The anode of the rectifier D is shorted to ground and is reverse-biased. Therefore, the capacitor C_B powers the load and sustains the output voltage. When the switch S is turned off, the drain-to-source (if MOSFET is used) voltage quickly rises up to just above the output voltage to turn on the rectifier. After the rectifier is forward-biased, the drain-to-source voltage is clamped to the output voltage. Meanwhile, the inductor L is discharged through the rectifier. The stored energy in L is transferred to feed the capacitor C_B and output load. The switch S turns on again for some period to begin the next switching cycle. The switching stages as shown in 2.3 are identical for positive and negative states of AC input voltage.



(a) S is turned on.



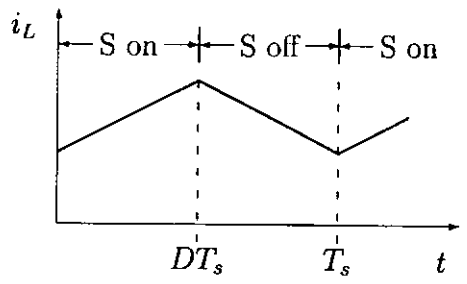
(b) S is turned off.

Figure 2.3: Equivalent circuits of the two switching stages of boost converter.

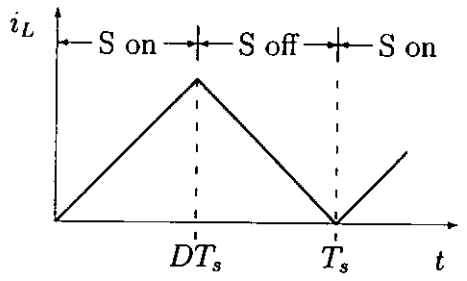
As being the same as other converters, boost converter can have different modes of operation depending on the switching frequency f_s (or switching period T_s), duty ratio of power switch D, inductance value L, output load R. These circuit parameters are related by

$$L \geq \frac{D(1-D)^2 R}{2f_s} \tag{2.12}$$

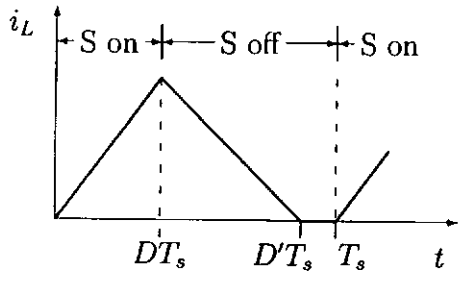
where L in (2.12) is the minimum inductance value required for continuous-conduction-mode (CCM) operation. This is the mode of operation when the inductor current i_L does not fall to zero at the instant the switch S is turned on,



(a) Continuous-conduction-mode (CCM) operation



(b) Boundary-conduction-mode (BCM) operation



(c) Discontinuous-conduction-mode (DCM) operation

Figure 2.4: Inductor current waveform of boost converter in different modes of operation.

as shown in Figure 2.4(a). This mode is sometimes referred to as the incomplete energy transfer mode.

When the boost inductance L equals the circuit parameters in right-hand side of (2.12), the converter is said to be operating in boundary-conduction-mode (BCM). In this mode, the inductor current i_L is just touching zero when the switch S is turned on to charge the inductor again, as shown in Figure 2.4(b). When either decrease in output power, duty ratio or increase in switching frequency, the converter runs into discontinuous-conduction-mode (DCM). In this mode, the inductor current i_L falls to zero for a while $(1 - D - D')T_s$, as shown in Figure 2.4(c), before the switch turns on and charges the inductor again. Both BCM and DCM are sometimes referred to as complete energy transfer mode.

2.5 Control of Boost Converter for PFC Application

The ideal target of switching converter for PFC application is to shape the input current such that it is of sinusoidal shape (i.e. distortion factor = 1) with sinusoidal input voltage and in phase with the input (i.e. displacement factor =1). That is, to achieve unity power factor because PF = DtF · DpF = 1. In other words, what the input side sees into the converter is a purely resistive load R_e, as shown in Figure 2.5, where ohms law applies.

$$i_{in} = \frac{v_{in}}{R_e} \tag{2.13}$$

With different modes of operation, the control strategy for a boost PFC converter is different. Figure 2.6 shows a block diagram of basic control of a boost PFC converter operating in CCM. It consists of basically two voltage loops and one current loop. In simple words, the voltage loops are used to generate a voltage reference template $v_{in,ref}$ for the current loop to follow to shape the input current of the boost converter as closely to a sine wave as possible, as shown in Figure 2.7. While the input voltage loop provides the template with

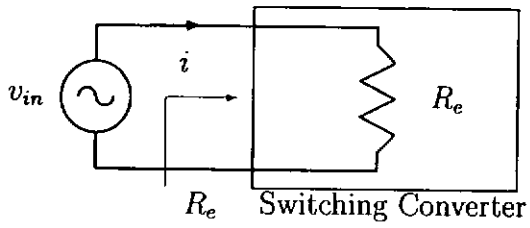


Figure 2.5: The switching converter emulates a purely resistive load for unity power factor.

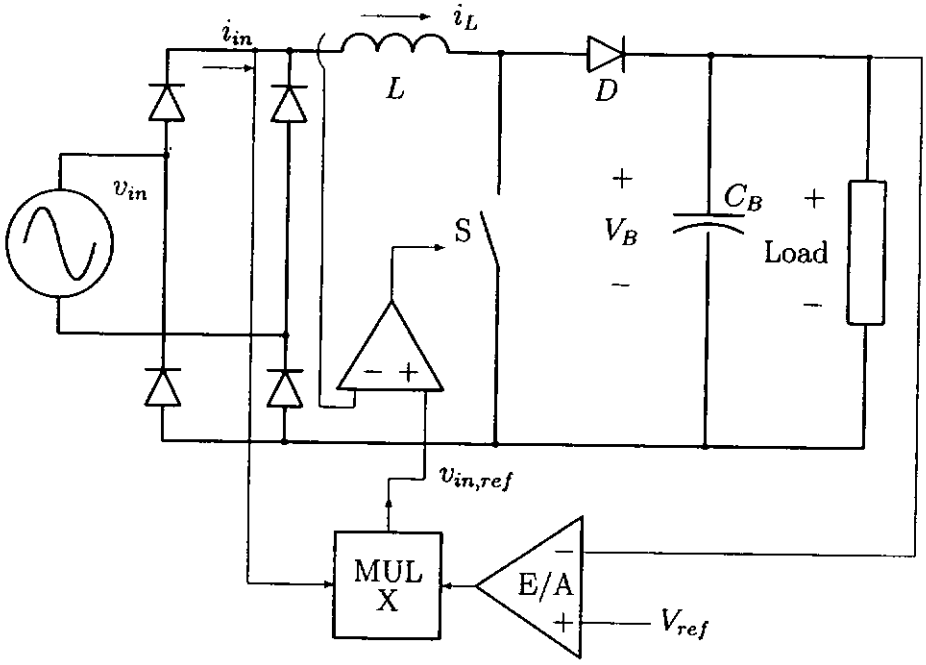


Figure 2.6: Basic control block diagram of a boost PFC converter in CCM.

required input current shape, the output voltage loop controls the output power by altering the height of the template. There are numerous control schemes to implement such PFC control, such as peak current mode control, average current mode control and hysteresis current control. Although in recent years researchers tried to simplify the control mechanism by reducing the number of loops involved [4]-[6], the idea of getting these three control parameters (i.e. input voltage, input current and output voltage) to implement PFC is fundamentally unchanged.

With BCM operation of the boost converter, a zero current detector is added to the current loop. When the inductor current falls to zero, the detector (actu-

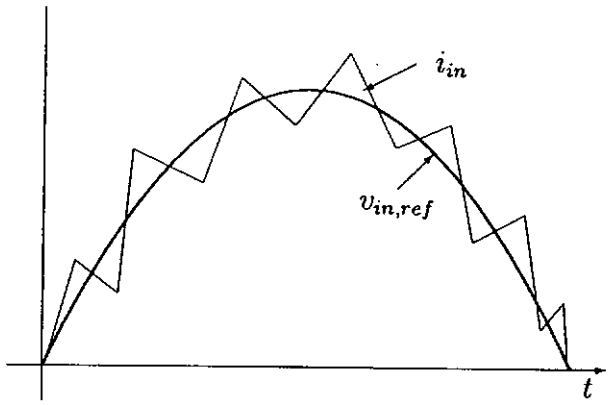


Figure 2.7: Use of voltage reference template to shape the input current.

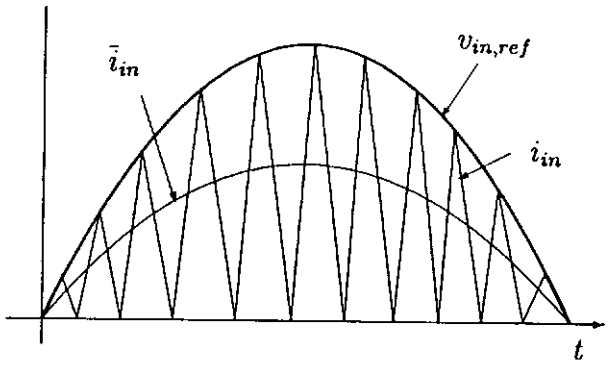


Figure 2.8: Input current of boost converter in BCM operation.

ally a comparator) is triggered to turn on the switch. When the inductor current touches the voltage reference template, the switch is turned off. Figure 2.8 shows the instantaneous and average input current. Using this current shaping technique, the average instantaneous input current $\bar{i}_{in}$ is given by

$$\bar{i}_{in} = \frac{v_{in}}{R_e} = v_{in}\frac{DT_s}{2L} \tag{2.14}$$

It can be seen from (2.14) that unity power factor can be achieved providing variable duty ratio and switching frequency modulations are used. In addition, the switch of the boost converter at BCM is operating under soft-switching condition: zero-current and low-voltage turn-on.

When the boost converter is operated in DCM, the average instantaneous

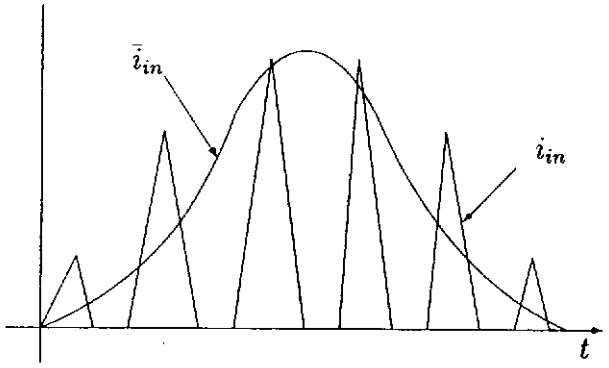


Figure 2.9: Input current of boost converter in DCM operation.

input current $\bar{i}_{in}$, as shown in Figure 2.9, is given by

$$\bar{i}_{in} = \frac{v_{in}}{R_e} = v_{in}\frac{D^2T_s}{2L}\frac{V_B}{V_B - v_{in}} \tag{2.15}$$

where V_B is the boost converter output voltage. It can be seen from (2.15) that unity power factor can be achieved only if conditions of fixed duty ratio and switching frequency modulation, and the output voltage V_B is much larger than the input voltage are both fulfilled. In practice, V_B is fixed by the design specification and high V_B will impose higher switching loss. As a result, distortion of input current will occur. To remedy this problem, the switching frequency can be set inversely proportional to the line voltage period [7]. Nevertheless, boost converter in DCM operation is the simplest current shaping technique among the others (BCM and CCM) because no voltage reference template is required. Therefore, to achieve high power factor (with acceptable degree of input current distortion) in DCM operation, only output voltage loop is needed.

With the fixed switching frequency and constant duty ratio to achieve high power factor in DCM operation, this opens room for development of single-stage PFC converters in which a DCM boost PFC converter is combined with a post-regulated DC/DC converter and they share the same switch(es). This will be detailed in Section 2.8.2.

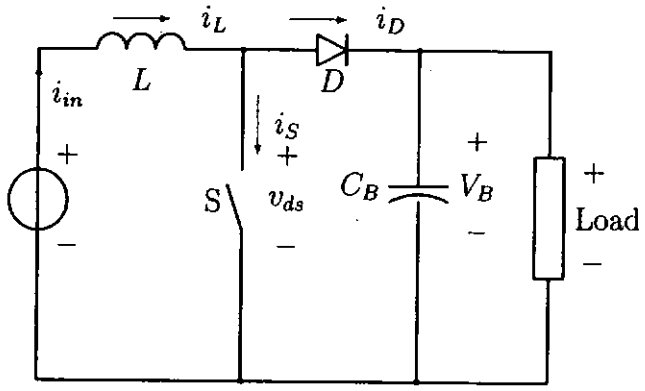
2.6 Rectifier Reverse-Recovery Problem in CCM Operation

In a boost converter, continuous-conduction-mode (CCM) is the preferred mode of operation for high power applications when compared to the discontinuous-conduction-mode (DCM), because CCM has lower conduction loss and smaller current stress on the semiconductor devices. But the large reverse-recovery current of the output rectifier in a CCM boost converter causes power dissipation and interference problems. This happens at the instant the switching transistor is turned on, forcing the output rectifier to be suddenly reverse-biased. Figure 2.10 illustrates the adverse effects of the rectifier reverse-recovery on a CCM boost converter. The large reverse-recovery current spike of the rectifier i_{rr} also flows into the switching transistor. This cross conduction of current i_S and voltage v_{ds} may cause excessive power dissipation and severe electromagnetic interference (EMI).

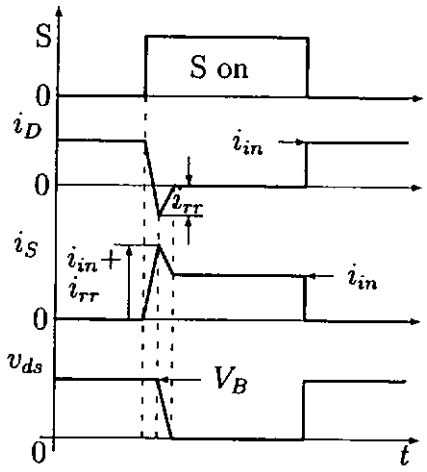
2.7 Reported Methodologies – Snubbers

To overcome the reverse-recovery related problems, various passive and active snubbers are proposed to reduce the current turn-off rate of rectifiers [8] - [16]. In general, the principle of these approaches is to insert a snubber inductor in series with the rectifier and the transistor to reduce the di/dt of the rectifier reverse-recovery current during the period of transistor turn-on. Some of the snubbers are regenerative and have the ability to recycle the reverse-recovery energy to the output load or to use it to create a soft-switching condition for the switching devices.

Active snubbers often employ auxiliary power switches to control the output rectifier turn-off rate di/dt. Zero-voltage-switching (ZVS) of power switches and rectifiers may also be achieved [8] - [11]. For instance, in the circuit proposed in [9], an additional boost converter is inserted across the output rectifier of a conventional boost converter. The main output current is shifted over to the



(a) CCM boost converter.



(b) Key switching transition waveforms.

Figure 2.10: Equivalent circuits of the two switching stages of boost converter.

added boost converter. The purpose of the additional inductor is to limit the turn-off rate of the rectifier which operates in CCM and to remove the charge stored in the parasitic capacitance of the auxiliary power switch for ZVS turn-on. The voltage and current stresses on the semiconductors are similar to those of a conventional boost converter. However, the main switch is turned on without soft-switching. The synchronization of the gate drivers for the main and auxiliary switches is yet another issue when using active snubbers to reduce the rectifier reverse-recovery loss.

Passive regenerative snubbers, which employs only inductors, capacitors and rectifiers, eliminate the use of auxiliary power switch. This increases the robustness and reliability of the converter. Many topologies have been introduced such as those proposed in [12] - [16]. A valley-fill circuit is added across the boost switch in [14] and across the boost rectifier in [15] to reduce the di/dt rate during rectifier turn-off. However, not all the additional rectifiers are turned off softly. As a large number of components are added, the components cost and conduction loss due to the circulating current are increased. In [12], the parasitic oscillation of the rectifiers would also cause extra power dissipation. Among the passive snubbers, the one proposed in [16] is more attractive because only a few additional components (a coupled pair of inductors and a rectifier) are required. However, the transient spikes caused by the coupled inductors and the parasitic capacitances of the boost switch during the turn-on transition result in extra loss and interference. Although a passive snubber can be added to reduce the transient spikes and to reduce the excessive voltage stress on the rectifier [16], it causes additional power loss.

2.8 Two-stage PFC Approaches

In Section 2.5, the control of PFC boost converter in different modes of operation has been discussed. The discussion is focused on how to shape the input current to achieve unity power factor. Since the average input current over a line cycle contains the line frequency component, the input power and so as the

output power also contain this line frequency component. Although a large bulk capacitor can use for smoothing out the output voltage, it contains substantial output voltage ripple at twice of the line frequency. In addition, for a boost converter, the output voltage is always higher than the input voltage. For universal input voltage application in which the high line voltage reaches $264V_{rms}$, the output voltage is loosely regulated at 380V to 400V. In many applications such as computer products where regulated low voltages are used (e.g. 3.3V, 5V, 12V, etc.), the output voltage of the boost converter certainly cannot meet the needs. Besides, an isolation transformer is usually required to provide sufficient safety measure for the power supply. Therefore, an additional stage using an isolation transformer with voltage step-down and regulated output is necessary to provide such features. This cascaded configuration of PFC converter with a DC/DC converter is called the two-stage PFC approach.

There are typically two approaches to implement two-stage PFC, depending on the output power level. For high power level (>300W), the serially-connected and individually-controlled two-stage PFC approach is used. For medium to low power levels ($\leq$ 300W), the serially-connected and integrated-control two-stage PFC approach is used under the consideration of control complexity and manufacturing cost and size.

2.8.1 High Power Level

In high power level application which requires PFC and tight output regulation, the serially-connected and individually-controlled two-stage PFC approach, as shown in Figure 2.11, is used. The PFC controller is dedicated to improve the power factor while the DC/DC controller is committed to remove the low frequency ripple on V_B and tightly regulated the output voltage. The advantage of this approach is the ease of optimization of individual power stages, especially the DC/DC regulation stage because the storage capacitor voltage V_B is loosely regulated at around 380Vdc-400Vdc for the entire input line voltage range. The commonly used converter topologies for DC/DC stage are two-transistor forward,

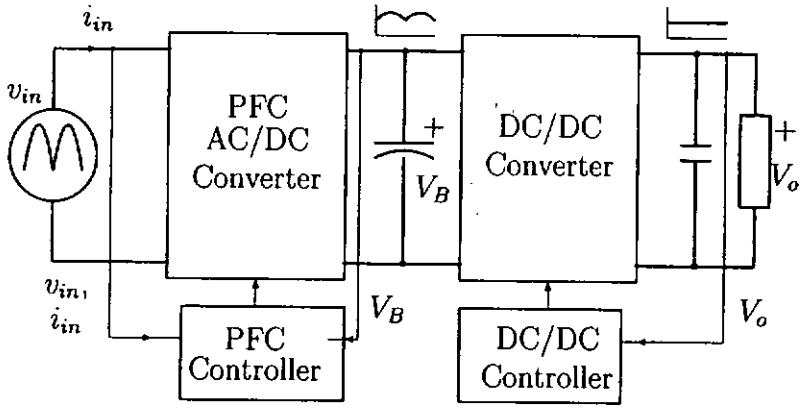


Figure 2.11: Serially-connected and individually-controlled two-stage PFC approach.

half-bridge and full-bridge converters.

2.8.2 Medium to Low Power Levels

In low power level application where cost is of prime concern, the control complexity and component count reduce stability and profit margin. In order to simply the power stages and control circuitry, single-stage PFC (S^2PFC) concept has been proposed. This concept was originated from some early work presented in [17]-[18]. The paper in [17] introduced a dual-output transformer in which one of the outputs is regulated DC load voltage (with fast response) and the other is used to boost up the input voltage to improve the power factor. The input boost stage is frequency-modulated and the output DC stage is PWM-controlled. Though the approach is effective, the implementation using a full-bridge converter only suitable for high power level and additional component used for resonant stage and boost-up voltage stage increased the converter complexity. In article [18], a boost PFC converter is connected serially with a DC/DC forward converter by sharing the same power switch. The duty cycle control is used to regulated the output voltage while the variable switching frequency control is used to regulated the storage capacitor voltage. High power factor is obtained by running the boost converter in DCM.

In 1992 Divan *et al* presented a cascaded connection of a CCM boost PFC

converter with a two-transistor forward DC/DC converter and shared the common bottom switch. Due to the sharing of common switch and different control constraints in input and output parameters, either one of the two parameters can be controlled over the entire line cycle. In the same year, Madigan *et al* [20] reported a new family of S^2PFC AC/DC converters, BIFRED and BIBRED, which are the integration of a DCM boost PFC converter with a buck or flyback converter and sharing of one power switch. It is noted that the storage capacitor is connected in series with the path of the input boost inductor and the transformer primary. Unlike the two-stage PFC approach, which processes the input power twice, the BIFRED and BIBRED inherit the parallel power processing or reduced redundant power processing feature which improves the conversion efficiency. Detailed about the power processing will be discussed in Sections 2.9.3, 2.10 and 2.11. In 1993, Brkovic and Cuk [21] reported the addition of a diode serially with the boost inductor in the Cuk topology performs the similar S^2PFC characteristics to that of BIFRED and BIBRED.

In 1994, Redl *et al* [22] reported a systematical approach to develop S^2PFC AC/DC converters with consideration of different topologies suitable for PFC and DC/DC stages. Apart from boost converter, other converters such as SEPIC, buck, buck-boost and Cuk are alternate practical choices for PFC stage implementation. For DC/DC stage, converters such as current-fed isolated DC/DC and two-transistor flyback topologies are also suitable for circuit integration. The paper also described the way to combine different converter topologies to form S^2PFC AC/DC converters. The combination is based on the assumption that the PFC stage is operated in DCM and the DC/DC stage can be operated either in DCM or CCM.

In the articles [20]-[22], the control strategy is further simplified by solely controlling the output voltage (i.e. single-loop voltage mode control). Although these converters share the common switch(es), two control parameters (input current and output voltage) are needed to shape the input current and give tight output regulation. Thanks to the DCM operation of PFC converter where constant duty cycle and fixed switching frequency are sufficient to achieve high power

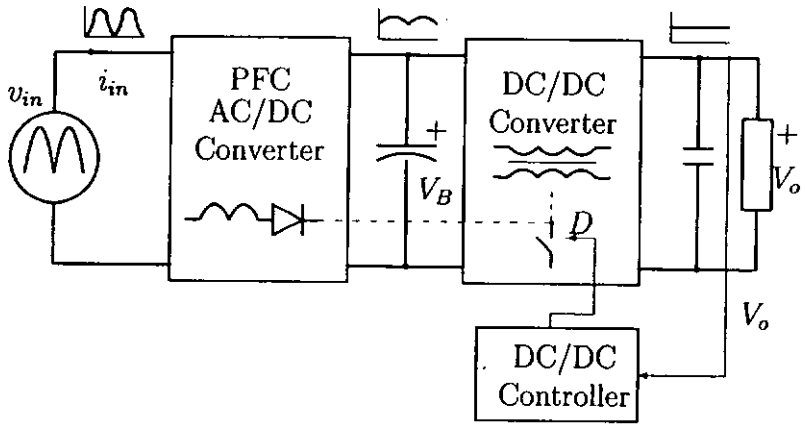


Figure 2.12: Integrated-controlled and serially-connected two-stage PFC approach (or single-stage PFC approach).

factor, as discussed in Section 2.5, a wide-bandwidth PWM control can be employed to monitor and control only the output voltage and to give fast transient response and improved power factor simultaneously, as shown in Figure 2.12.

It is noted that, apart from the BIFRED and BIBRED, the S^2PFC AC/DC concept and converters proposed in [17] to [22] belong to the two-stage PFC approach. It is because these converters consist of fundamentally two individual power stages but the configuration and control are simplified after sharing of the same switch(es).

2.9 Potential Problems in Single-stage PFC Converters

Although S^2PFC AC/DC converters enjoy simple converter structure and control circuitry, they presents more problems than that of individually-controlled serially-connected converters. In this section, we will investigate the causes of three important problems in S^2PFC approach including high voltage and current stresses and low conversion efficiency, which limit their practical in medium to low power level applications.

2.9.1 High Voltage Stress across the Storage Capacitor

Most of the S^2PFC converters employed a boost converter as the front-end power factor corrector due to its high power factor capability and ease of integration with DC/DC regulator. The energy stored in the boost inductor from the line voltage source will be transferred to the storage capacitor. Due to the input-output characteristic of the boost converter, the storage capacitor voltage is always higher than the peak input voltage. According to [24], the ratio of storage capacitor voltage to peak input voltage should be as high as 1.37 to achieve power factor of 0.97, that will be higher than 500V for high line input condition (i.e. $264V_{rms}$). In other words, better power factor is obtained at the expense of high voltage stress on the storage capacitor. This will also impose higher voltage stress on the semiconductor devices such as power switch and output diode.

In addition, the S^2PFC converters employ a single-loop feedback controller where only the change of output voltage is regulated, the storage capacitor will therefore vary according to line and load changes. It has been shown that the storage capacitor voltage of the S^2PFC converters where the DC/DC stage working in continuous conduction mode (CCM) is inversely proportional to the load current [23]. This voltage may even rise up higher (e.g. 1000V) at high line light load condition. The rise of storage capacitor voltage due to power imbalance has already been discovered and investigated [22]-[23]. But most of the analysis only based on mathematical calculation or from the power level standpoint. However, it is more profitable to look at the problem from the circuit level with supplementary equations.

Figure 2.13 shows an example circuit of a single-switch S^2PFC converter that combines a DCM boost PFC converter with a CCM flyback DC/DC converter. At the time t_0 (shown in Figure 2.14) when the power switch S1 is turned off, the secondary current i_s supplies the output capacitor and output load currents.

$$i_s = i_c + i_o \tag{2.16}$$

The rate of change of inductor current and capacitor voltage are given by, respec-

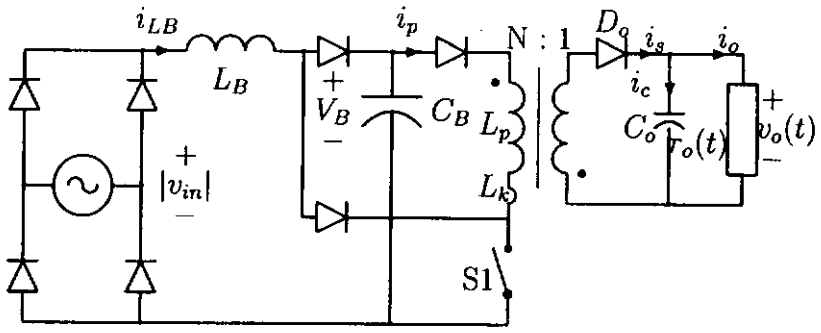


Figure 2.13: Single-switch single-stage power-factor-corrected converter combining boost and flyback converters.

tively,

$$\frac{di_s}{dt} = \frac{N^2 V_o}{L_p} \tag{2.17}$$

$$\frac{dv_o}{dt} = \frac{i_c}{C_o} \tag{2.18}$$

Substituting (2.17) and (2.18) into (2.16) and solving this second-order differential equation with the initial condition of $v_o(t_0) = V_1$, we finally get

$$v_o(t - t_0) = \frac{V_1}{2}\left[\left(1 + \frac{1}{k(t)}\right) e^{\frac{t(k(t)+1)}{2C_o r_o(t)}} + \left(1 - \frac{1}{k(t)}\right) e^{\frac{t(k(t)-1)}{2C_o r_o(t)}}\right] \tag{2.19}$$

where

$$k(t) = \left[1 + \frac{4N^2 C_o r_o(t)}{L_p}\right]^{\frac{1}{2}} \tag{2.20}$$

The output voltage $v_o(t)$ during the period $(t_1 - t_0)$ derived in (2.19) is plotted against loading resistance $r_o(t)$ with the following circuit parameters: V_1=15V, C_o=2200μF, L_p=50μH, N=2 and t=10μs. As shown in Figure 2.15, the output voltage increases when the load becomes light (i.e. $r_o(t)$ increases). If this happens, the rate of change of inductor current di_s/dt indicated in (2.17) will be faster (thick solid line in Figure 2.14). It takes i_s a shorter period to fall to zero (t_2' instead of t_2 at steady state) when S1 is turned on at t_1. The rate change of secondary current results in a steeper rate of change of the primary current i_p but with a smaller peak current comparing to that of the steady state (thin solid line). It is obvious to observe from the figure that the transformer current, i_p and i_s, is self-adjusted (current area A < current area B for decreasing load) to the change of load current. Consequently, after just a few switching cycles the

output voltage will be fallen to the regulation range, provided that the change of load is not severe. Since the compensation network of the converter has a cutoff frequency far below the switching frequency for stability reason, the compensation is not fast enough to response to this change of voltage and the duty cycle of S1 remains unchanged. The input current drawn into the converter also keeps the same amount. Therefore, with smaller demand than supply of current, the excess current will be stored as charge in the storage capacitor and its voltage will be increased.

2.9.2 High Current Stress on the Power Switch

Another problem arises in S^2PFC converters is the extra current stress on the switch (or a pair of switches) when compared with the individually-controlled serially-connected approach as shown in Figure 2.11 because it has to handle all the input currents from the line input voltage and the storage capacitor voltage at the same time. The current stress is maximum at full load condition and at the peak of input voltage. Conduction and switching losses are therefore increased which deteriorate the conversion efficiency and cause high temperature rise. The power switch becomes the major portion of total power losses and the hottest point comparing to other power devices in the converter. Larger EMI noise is another critical issue due to this high current stress.

2.9.3 Repeated Power Processing

In most of the S^2PFC converters, in [17]-[18],[21]-[22] for example, the input power has to be processed twice before transferring to output load. The more input power is repeatedly processed, the higher power is dissipated to the power devices. Conversion efficiency is limited to the product of individual efficiency of each stage.

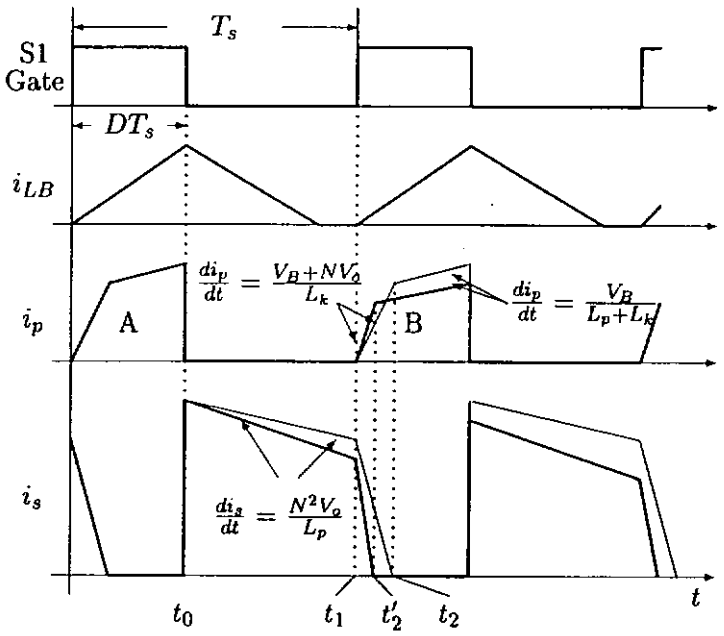


Figure 2.14: Key switching waveforms illustrating the influence of decreasing load.

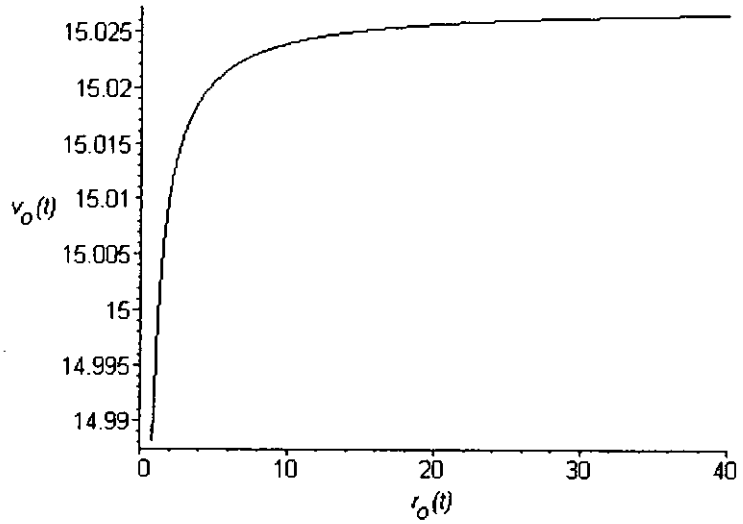


Figure 2.15: Calculated output voltage v_o against load change (r_o).

2.10 Reported Methodologies

To suppress the voltage stress across the storage capacitor, various approaches are introduced to reduce the energy feeding the storage capacitor. Variable switching

frequency (VSF) [25]-[26] limits the input power pumped to the storage capacitor by increasing the switching frequency at decreasing load. But large load variation results in wide variation range in switching frequency. The optimization of filtering is yet another issue when using VSF to cope with high voltage stress problem.

Recently, a number of circuits applying the negative voltage feedback technique have been introduced [27]-[29]. An extra coupled winding from the output transformer is inserted in series with the boost inductor so that the storage capacitor voltage information is brought forward to the input stage to reduce the input current when this voltage is increased. The authors attempted to remove the boost inductor in [30] to provide a direct control of input current. However, the input current ceases to flow into the circuit during the line cycle when the input voltage is smaller than the feedback voltage. This generates high input current harmonics. Consequently, the input power is concentrated near the peak of input voltage, resulting in high current stress on the power devices.

Series-charging-parallel-discharging technique [31] cannot reduce input power when load becomes light but it simply uses two storage capacitors to share the voltage stress. Balanced sharing of voltage stress becomes a critical design issue and two storage capacitors increase cost and size of the converters. DCM PFC + DCM DC/DC arrangement [32] does not suffer from high voltage stress at decreasing load but the storage capacitor voltage change largely according to the line voltage change.

Besides reduction of voltage stress on storage capacitor, the negative voltage feedback [33] and load current feedback [30] techniques found useful in reducing the switch current stress. But the reduction of current stress should be justified by the increase in input current harmonics.

Many new topologies have been developed [34]-[42] to reduce the number of times the input power is repeatedly processed by means of adding direct power transfer path(s) to the circuits. Using this concept the conversion efficiency is improved by the experimental work shown in [42]. Most of these converters consist of

two or more switches that require a sophisticated control to shape the input current and regulate the output voltage. Therefore single-switch AC-DC converters with this reduced repeated power processing feature have been proposed in [40] -[42] that simplified the control mechanism. Namely, these converters employ an parallel-connected integrated-control configuration. Another way to reduce control complexity is to introduce a simpler control system for the converters like the one in [37], but the control mechanism detail has not been described yet.

In 2000, Tse and Chow [43] reported a systematical approach for deriving basic converter configurations that achieve PFC and voltage regulation. Based on the presentation of power flow and three-port network model, there are sixteen configurations in total to achieve PFC and voltage regulation with reduced repeated (or redundant) power processing. The discussion in [43] is based on the parallel-connected individually-controlled configuration. Although unity power factor is the ideal objective, it is not necessary to meet nowadays regulations with unity power factor. By inspecting the current harmonics limits in IEC 61000-3-2 for instance, according to different classes they allow certain current harmonics in the design. In 2001, Garcia *et al* [44] presented a survey on different converter configurations to achieve such purpose.

Besides the rectifier reverse-recovery related problem, simple and cost-effective solutions to achieve high power factor, to reduce the high voltage and current stresses and to improve the conversion efficiency are the objectives of this dissertation.

2.11 Summary

In this chapter, a review of boost PFC converter operating in three distinct modes and associated control methods have been discussed. The rectifier reverse-recovery related problem and various solutions have been explained. Moreover, the two-stage approaches in achieving PFC and output regulation , in particular the single-stage PFC approach, have been presented. The main issues concerning single-stage PFC approach are the high voltage and current stresses and low

conversion efficiency, which need further work to resolve.

Chapter 3

Technique for Reducing Reverse-Recovery and Switching Losses

3.1 Introduction

Last chapter we discussed the use of CCM converters for PFC function and the associated reverse-recovery related losses of the rectifier. To provide an improved solution over the existing ones, a single-switch continuous-conduction-mode (CCM) boost converter with reduced reverse-recovery and switching losses is proposed in this chapter. By using the leakage inductances of a pair of coupled inductors and two additional rectifiers, the turn-off rates (di/dt) of the boost output rectifier and the additional rectifiers are slowed down to reduce the reverse-recovery loss. The boost power transistor is also operated under a low-voltage turn-on condition to reduce the switching loss. Experimental results are presented to confirm the theoretical analysis and the performance of the proposed converter.

The proposed CCM boost converter offers the following advantages:

- The leakage inductances of the coupled inductors are used to control the di/dt rate of the rectifier currents. All rectifiers are turned off softly and clamped to the output voltage afterwards. They do not require any extra snubber circuit to protect them from parasitic ringing.

- The boost switch operates under a low-voltage turn-on condition because the coupled inductors provide a path for the parasitic capacitance of the boost switch to discharge before the switch is turned on.

3.2 Proposed Circuit and Its Operation

3.2.1 Circuit Description

An improved CCM boost converter, as shown in Figure. 3.1, is formed by adding a coupled inductor-rectifier ($L_2 - D_2$) branch to the input and output nodes of a boost converter and inserting a rectifier (D_3) from ground to the common node of the coupled inductor-rectifier branch. Rectifier D_3 is employed to clamp the parasitic ringing caused by the output capacitance C_{oss} of the boost switch S1, the coupled inductors and the reverse-bias capacitance of rectifier D_2 during the turn-on transition of S1. The magnetic coupling coefficient between L_1 and L_2 is k. As will be shown in Chapter 3.2.2, a smaller value of k results in a better capability of achieving low-voltage turn-on of the boost switch S1. L_1 and L_2 are wound in the same orientation and are related by the turns ratio n where $n > 1$. In this proposed converter, all rectifier turn-off rates (di/dt) are controlled by the leakage inductances of the coupled inductors. The inductor currents i_{L1} and i_{L2} run in DCM. However, i_{L1} and i_{L2} combine to form a continuous input current. Comparing to a boost converter with discontinuous input current, the proposed converter possesses less EMI noise so that a smaller input filter can be used.

3.2.2 Circuit Operation Analysis

For the ease of analysis and explanation, an equivalent circuit model of the converter including the magnetizing inductance and the leakage inductances is developed, as shown in Figure. 3.2. Some equations relating the equivalent circuit are given below prior to the description of the converter operation stages.

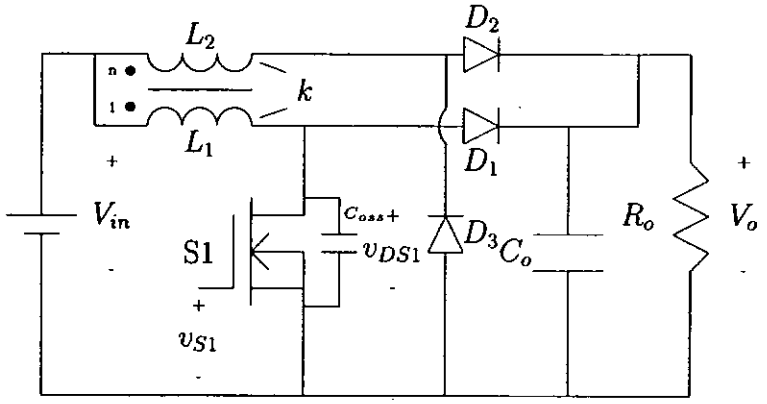


Figure 3.1: Circuit diagram of the proposed CCM boost converter.

$$n = \sqrt{\frac{L_2}{L_1}} \tag{3.1}$$

$$L_M = k\sqrt{L_1 L_2} \tag{3.2}$$

$$v_a = \left(L_1 - \frac{L_M}{n}\right)\frac{di_{L1}}{dt} \tag{3.3}$$

$$v_b = \frac{L_M}{n}\frac{d}{dt}(i_{L1} + ni_{L2}) \tag{3.4}$$

$$v_c = (L_2 - nL_M)\frac{di_{L2}}{dt} \tag{3.5}$$

$$v_d = nv_b \tag{3.6}$$

Here, L_M is the mutual inductance between L_1 and L_2. To facilitate the analysis of the steady-state operation, some assumptions are made (within each switching period): 1) The input voltage V_{in} is a dc voltage source; 2) The output capacitor C_o is large enough so that the output voltage ripple due to switching is negligible and V_o is essentially a constant; 3) Except for the reverse-recovery of the rectifiers and the output capacitance of the power switch C_{oss}, all circuit components have ideal characteristics. Referring to the equivalent circuit model shown in Figure. 3.2 and the switching waveforms shown in Figure. 3.3, the eight operation stages of the converter are discussed as follows.

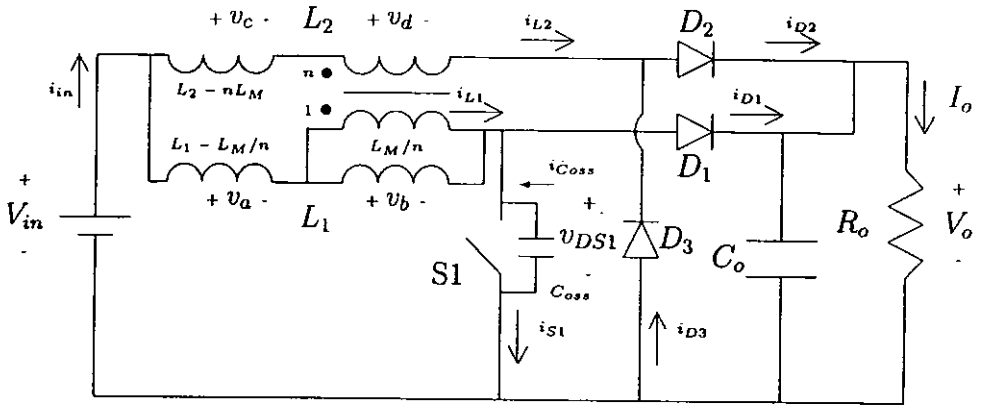


Figure 3.2: Equivalent circuit model of the proposed converter.

Stage 1 $(t_0 - t_1)$ [Figure. 3.4(a)]: At time $t = t_0$, the boost switch S1 is turned on. At the same time, the rectifiers D_1 and D_3 are turned off with reverse voltages both equal the output voltage V_o. The voltage across L_1, $(v_a + v_b)$, is equal to V_{in}. The current i_{L1} starts to increase linearly at the rate of (The detailed derivation is given in Appendix)

$$\frac{di_{L1}}{dt} = \frac{(L_2 - L_M)V_{in} + L_M V_o}{L_1 L_2 - L_M^2} \tag{3.7}$$

Substituting (3.1) and (3.2) into (3.7), we have

$$\frac{di_{L1}}{dt} = \frac{(n-k)V_{in} + kV_o}{nL_1(1-k^2)} \tag{3.8}$$

Rectifier D_2 is forward biased such that the input current i_{in} flows through L_2. The voltage across L_2, $(v_c + v_d)$, is $-(V_o - V_{in})$ and i_{L2} decreases linearly at the rate of

$$\frac{di_{L2}}{dt} = \frac{(1-nk)V_{in} - V_o}{n^2 L_1(1-k^2)} \tag{3.9}$$

This interval ends when i_{L2} and i_{D2} reach zero.

Stage 2 $(t_1 - t_2)$ [Figure. 3.4(b)]: This is the reverse-recovery period of D_2 to release its residual stored charge. The turn-off rate is governed by the decreasing rate of i_{L2} in (3.9). In order to remove the parasitic ringing caused by the reverse-bias capacitance of D_2 and the leakage inductance of the coupled

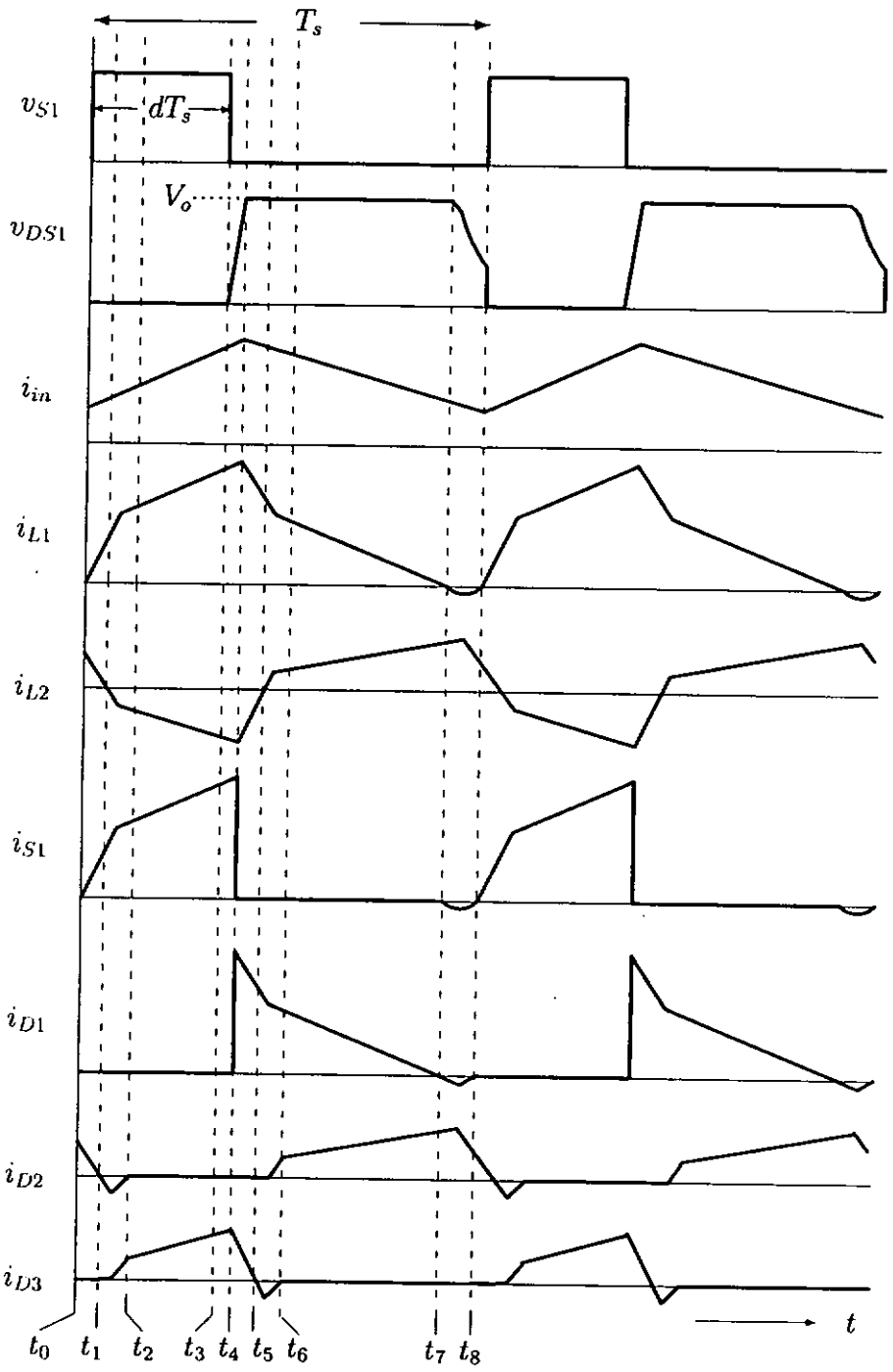


Figure 3.3: Key switching waveforms of the proposed converter.

inductors, D_3 has to turn on to clamp the anode of D_2 to ground. The induced emf in L_2 should therefore be sufficiently high to turn on D_3, namely

$$v_d > V_{in} \tag{3.10}$$

Substituting (3.1), (3.2) and (3.6) into (3.10), we come up with the requirement to forward bias D_3:

$$n^2 k > 1 \tag{3.11}$$

In practice, due to the imperfect coupling between the coupled inductors, there are leakage inductances. The leakage inductances are modeled as $(L_1 - L_M/n)$ in L_1, and $(L_2 - nL_M)$ in L_2, as shown in Figure. 3.2. Referring to (3.11), since the coupling coefficient k is always less than 1, the turns ratio n must be greater than 1. If the condition in (3.11) is fulfilled, the voltage applied on D_3 may decrease from V_o to zero and D_3 may conduct in Stage 2. The voltage across L_2, $(v_c + v_d)$, is then equal to V_{in}, and i_{L2} begins to flow in negative direction. Meanwhile, a reverse voltage is set up in D_2 from zero towards V_o and D_2 starts to turn off. This stage ends when D_2 is completely reverse-biased. Note that for the absence of D_3, D_2 will start ringing between the parasitic capacitance of D_2 and the leakage inductance of the coupled inductors once it is turned off at t_2.

Stage 3 $(t_2 - t_3)$ [Figure. 3.4(c)]: At $t = t_2$, D_3 conducts fully and $i_{D3} = i_{L2}$. The rate of change of i_{L2} (and thus i_{D3}) equals

$$\frac{di_{L2}}{dt} = \frac{(1 - nk)V_{in}}{n^2 L_1(1 - k^2)} \tag{3.12}$$

The current i_{L1} continues to ramp up. The rate of change of i_{L1} is

$$\frac{di_{L1}}{dt} = \frac{(n - k)V_{in}}{nL_1(1 - k^2)} \tag{3.13}$$

D_3 clamps the anode voltage of D_2 to ground and prevents it from ringing. This stage is completed when S1 is turned off.

Stage 4 $(t_3 - t_4)$ [Figure. 3.4(d)]: S1 is turned off at $t = t_3$. The current that was flowing through the drain to source channels of S1 is now being switched to C_{oss}. As a result, C_{oss} is charged up by i_{L1} in a resonant manner towards V_o. Since the charging time is short compared to the oscillation period, which is

given by $2\pi\sqrt{L_1 C_{oss}}$, v_{DS1} increases linearly. After v_{DS1} reaches V_o, the charging current will continue to charge up C_{oss}. v_{DS1} then rises above V_o. This stage ends when D_1 is forward-biased.

Stage 5 ($t_4 - t_5$) [Figure. 3.4(e)]: At $t = t_4$, D_1 turns on. A constant negative voltage, $-(V_o - V_{in})$, is applied across L_1. The current in L_1 decreases linearly from its peak value with a rate of

$$\frac{di_{L1}}{dt} = \frac{(n-k)V_{in} - nV_o}{nL_1(1-k^2)} \tag{3.14}$$

In the meantime, the rate of change of i_{L2} equals

$$\frac{di_{L2}}{dt} = \frac{(1-nk)V_{in} + nkV_o}{n^2 L_1(1-k^2)} \tag{3.15}$$

The energy stored in L_1 and L_2 are transferred to the load through D_1 and the source V_{in} respectively. This interval ends when i_{L2} and i_{D3} reach zero.

Stage 6 ($t_5 - t_6$) [Figure. 3.4(f)]: D_3 undergoes a reverse-recovery transition. The turn-off rate of D_3 is limited to the rate of change of i_{L2} in (3.15). The blocking voltage applied across D_3 begins to rise towards V_o. At the same time, the reverse voltage applied across D_2 starts to drop from V_o to zero. After that, D_2 enters conduction state. At the end of this interval, D_3 is completely reverse-biased.

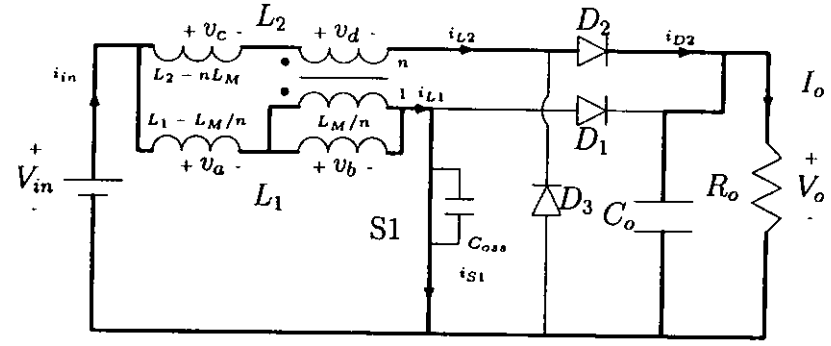
Stage 7 ($t_6 - t_7$) [Figure. 3.4(g)]: At $t = t_6$, D_3 recuperates from reverse-recovery period and ceases conducting. As D_2 conducts, a constant negative voltage, $-(V_o - V_{in})$, is applied across L_2. However, the current i_{L2} becomes positive to flow through D_2 to the output owing to the energy coupled from L_1.

$$\frac{di_{L2}}{dt} = \frac{(1-nk)(V_{in} - V_o)}{n^2 L_1(1-k^2)} \tag{3.16}$$

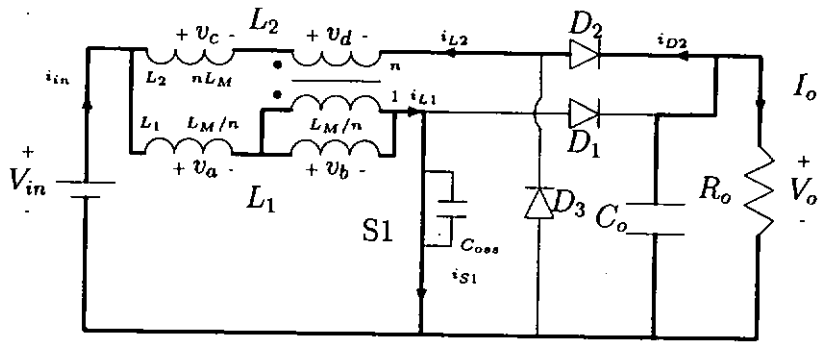
During this stage, the inductor current i_{L1} continues to decrease as the rest of the energy stored in L_1 continues to be delivered to output through D_1. The rate of change of i_{L1} is now equal to

$$\frac{di_{L1}}{dt} = \frac{(n-k)(V_{in} - V_o)}{nL_1(1-k^2)} \tag{3.17}$$

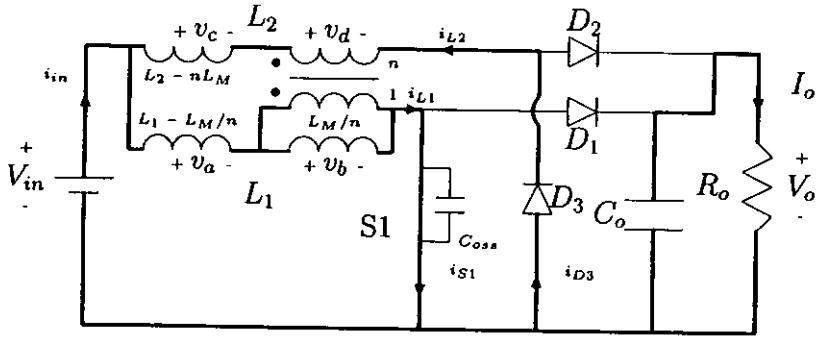
This mode ends when i_{L1} drops to zero.



(a) Stage 1 ($t_0 - t_1$)

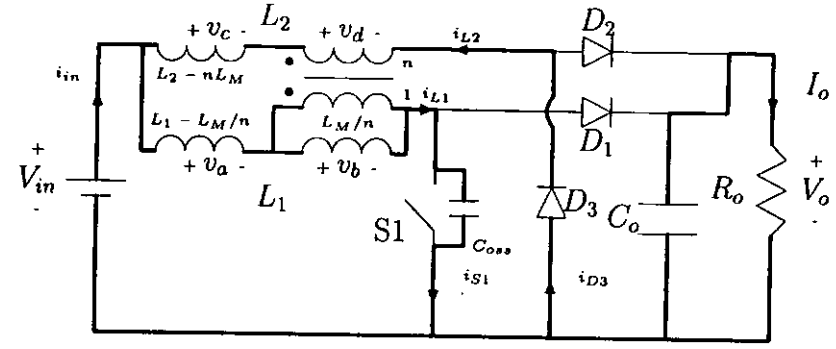


(b) Stage 2 ($t_1 - t_2$)

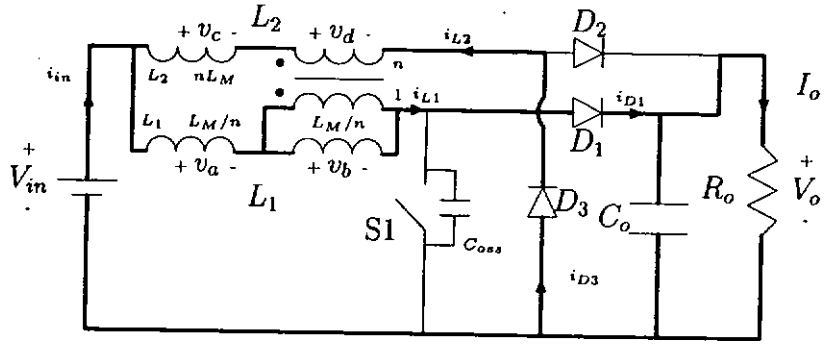


(c) Stage 3 ($t_2 - t_3$)

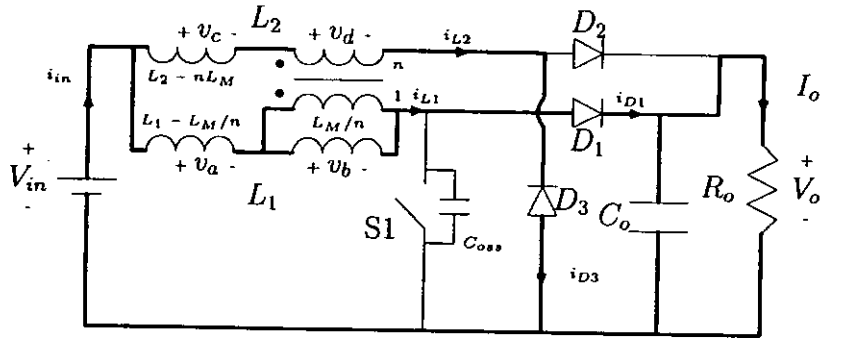
Figure 3.4: Eight operation stages of the converter during one switching period.



(d) Stage 4 ($t_3 - t_4$)

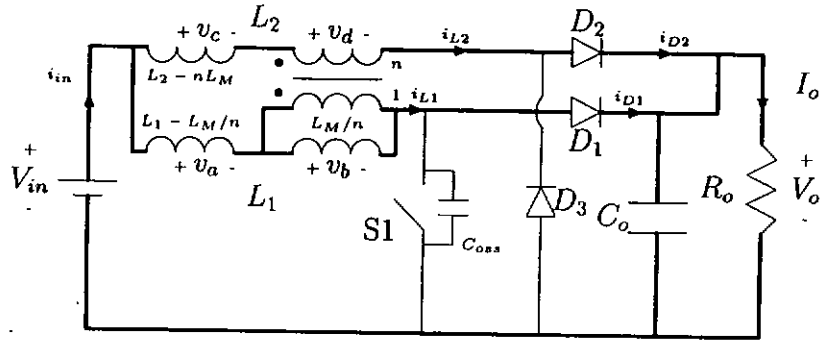


(e) Stage 5 ($t_4 - t_5$)

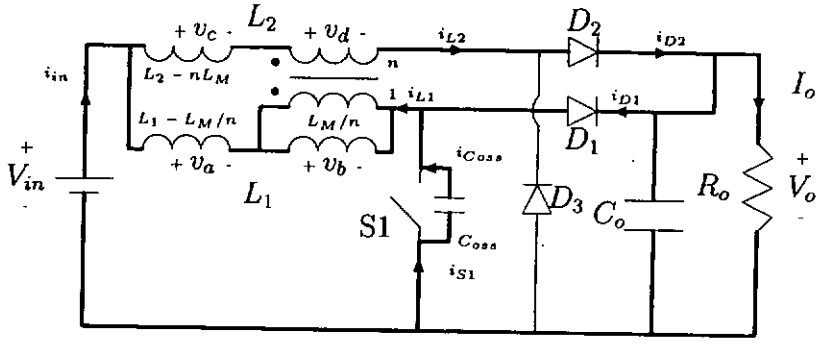


(f) Stage 6 ($t_5 - t_6$)

Figure 3.4: Eight operation stages of the converter during one switching period.



(g) Stage 7 ($t_6 - t_7$)



(h) Stage 8 ($t_7 - t_8$)

Figure 3.4: Eight operation stages of the converter during one switching period.

Stage 8 ($t_7 - t_8$) [Figure. 3.4(h)]: i_{L1} and i_{D1} drop to zero at $t = t_7$. Reverse-recovery of D_1 occurs at a turn-off rate limited to that of i_{L1} in (3.17). During this time interval, i_{L1} flows backward in a current loop consisting of L_1, V_{in}, C_o and D_1. At the same time, v_{DS1} decreases with a resonance frequency ω_r because the charge stored in C_{oss} is being transferred through L_1 back to the input source. At the end of this stage, v_{DS1} reaches a minimum value and S1 is then turned on at $t = t_8$ to begin the next switching cycle. The voltage and current of C_{oss} during this period are

$$v_{DS1}(t) = V_o + (V_o - V_{in})(1 - \beta)[cos\omega_r(t - t_7) - 1] \tag{3.18}$$

$$i_{Coss}(t) = (V_{in} - V_o)(1 - \beta)Z_r sin\omega_r(t - t_7) \tag{3.19}$$

where

$$\beta = \frac{k(n+1)}{n(k+1)} \tag{3.20}$$

$$\omega_r = \frac{1}{\sqrt{L_1 C_{oss}}} \tag{3.21}$$

$$Z_r = \sqrt{\frac{C_{oss}}{L_1}} \tag{3.22}$$

$$t_8 = t_7 + \frac{\pi}{\omega_r} \tag{3.23}$$

Substituting (3.23) into (3.18), the minimum drain-to-source voltage of S1 is written as

$$v_{DS1}(t_8) = V_o - 2(V_o - V_{in})(1 - \beta) \tag{3.24}$$

Define the voltage conversion ratio $M = V_o/V_{in}$ and let V_{in}=100V. Equation (3.24) can then be plotted as shown in Figure. 3.5. It is found that the smaller is the value of β, the lower is the drain-to-source voltage for the turn-on of S1. β reflects effectively the portion of magnetizing inductance of the coupled-inductors. Also, when M is smaller than 2, only non-ideal zero-voltage-switching (ZVS), or low-voltage turn-on, for S1 is obtainable. Based on (3.20), a plot of β against turns ratio n for different values of k is given in Figure. 3.6. It can be observed that β decreases when n is increased, or k is decreased.

It should be noted that the charge stored in C_{oss} is removed in a resonance manner by the leakage inductance of the coupled inductors. If S1 is not switched

on around the time when v_{DS1} is minimum (at $t = t_8$), the low-voltage turn-on property will be lost. This results in higher capacitive turn-on loss as residual energy in C_{oss} is being dissipated through the switch at the instant S1 is turned on. This capacitive loss, P_{Coss}, can be calculated as

$$P_{Coss} = \frac{1}{2T_s} C_{oss} v_{DS1}^2(t_8) \tag{3.25}$$

As shown in Figure. 3.7, v_{DS1} will tend to oscillate if S1 remains off. The oscillation frequency is ω_r, but the amplitude will gradually decrease as energy is being dissipated by the circuit devices along the oscillation path.

3.3 Design Criteria

3.3.1 Condition for Reduction of Reverse-Recovery Loss

Since all rectifier currents reach zero before undergoing the reverse-recovery transitions, the loss due to the reverse-recovery current will be significantly reduced compared to the case where a reverse voltage is suddenly applied to a rectifier while it is heavily conducting in the forward direction. Moreover, the reverse-recovery currents of the rectifiers in the proposed circuit are all controlled by the leakage inductances of the coupled inductors (di_{D1}/dt is controlled by leakage inductance $(L_1 - L_M/n)$, di_{D2}/dt and di_{D3}/dt are controlled by leakage inductance $(L_2 - nL_M)$). Soft turn-off of the rectifiers is thus ensured. However, in order to obtain the desired operation, the following inequality must be satisfied.

$$t_8 - t_3 \leq 1 - d \tag{3.26}$$

In general, it is preferable to keep the turn-off rate of ultra-fast rectifiers below 100A/μs in order to alleviate the reverse-recovery problem. As mentioned above, the turn-off rates of D_1, D_2 and D_3 are controlled by (3.17), (3.9) and (3.15) respectively. It is clear that the turn-off rates can be reduced by increasing the leakage inductance. In order to observe the effects of n and k on the turn-off rate, two normalized expressions (from (3.17)) for the turn-off rate of D_1, $r_{n,D1}(n)$

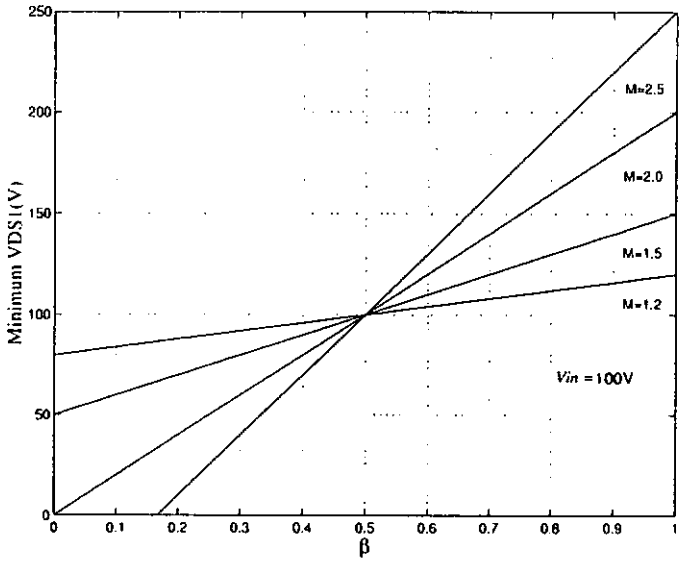


Figure 3.5: Minimum v_{DS1} attainable by the converter at different values of β.

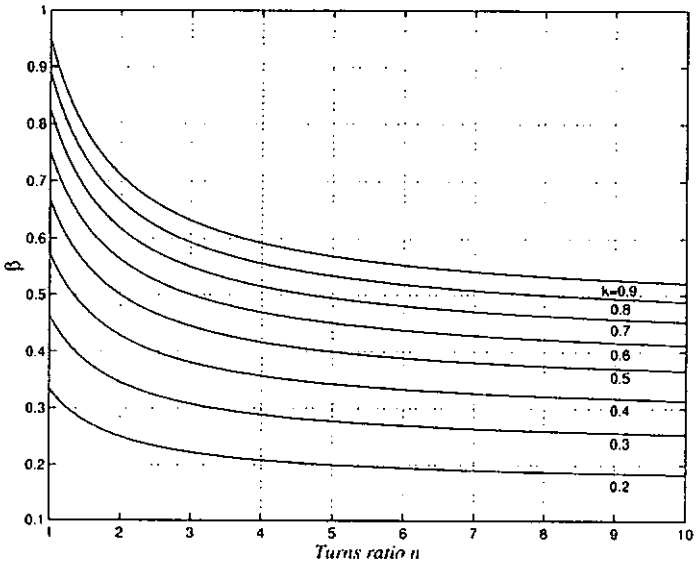


Figure 3.6: β versus turns ratio n for different values of k.

(as a function of n) and $r_{n,D1}(k)$ (as a function of k), are formed.

$$r_{n,D1}(n) = \frac{n_o(n - k_o)}{n(n_o - k_o)} \tag{3.27}$$

$$r_{n,D1}(k) = \frac{(1 - k_o^2)(n_o - k)}{(1 - k^2)(n_o - k_o)} \tag{3.28}$$

where n_o and k_o are the reference values of n and k. Similarly, for the turn-off

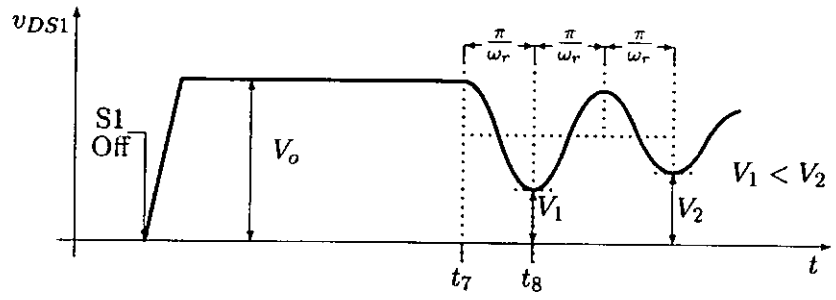


Figure 3.7: Drain-to-source voltage v_{DS1} of S1 after the switch is turned off.

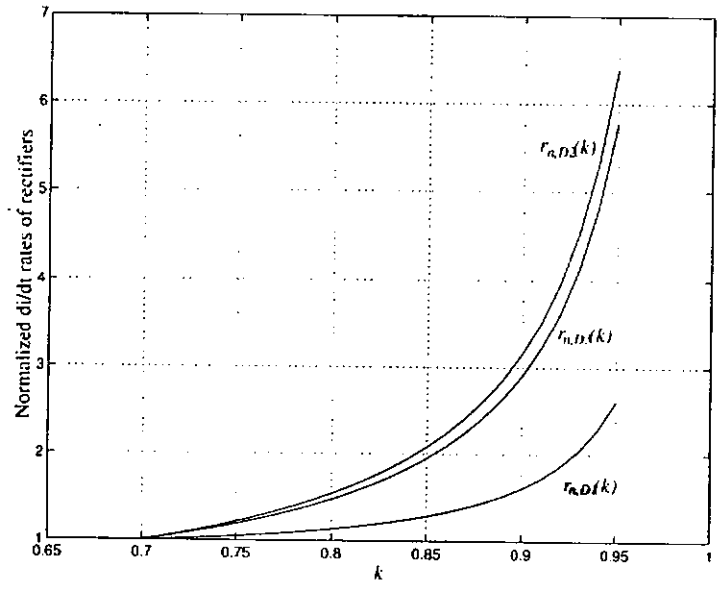


Figure 3.8: Normalized di/dt turn-off rates of rectifiers versus coupling coefficient k.

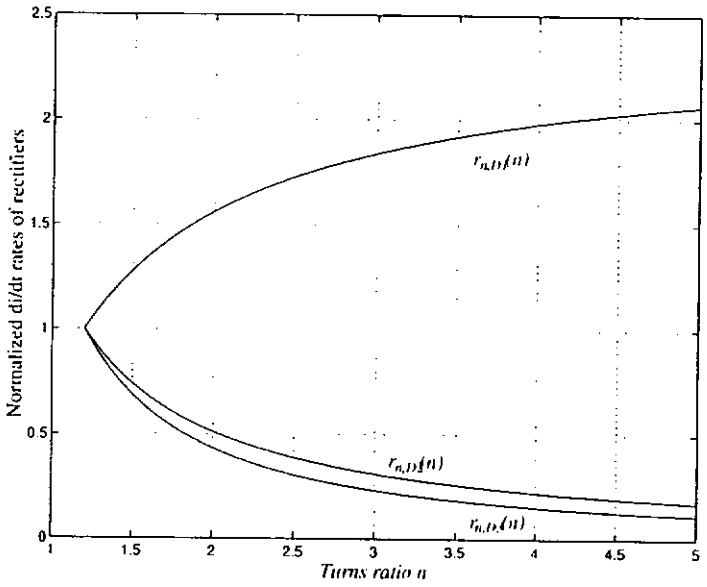


Figure 3.9: Normalized di/dt turn-off rates of rectifiers versus turns ratio n.

rates of D_2 in (3.9) and D_3 in (3.15), we have

$$r_{n,D2}(n) = \frac{n_o^2[(1-nk_o)-M]}{n^2[(1-n_ok_o)-M]} \tag{3.29}$$

$$r_{n,D2}(k) = \frac{(1-k_o^2)[(1-n_ok)-M]}{(1-k^2)[(1-n_ok_o)-M]} \tag{3.30}$$

$$r_{n,D3}(n) = \frac{n_o^2[(1-nk_o)+nk_oM]}{n^2[(1-n_ok_o)+n_ok_oM]} \tag{3.31}$$

$$r_{n,D3}(k) = \frac{(1-k_o^2)[(1-n_ok)+n_okM]}{(1-k^2)[(1-n_ok_o)+n_ok_oM]} \tag{3.32}$$

Define $k_o = 0.7$ and from (3.11) $n_o = 1.2$. Equations (3.27) to (3.32) are plotted and shown in Figures. 3.8 and 3.9. It can be seen that all the rectifier turn-off rates are reduced when k is decreased. However, when n is decreased, the di/dt rate of D_1 is reduced and those of D_2 and D_3 are increased. Since the main input current flows through D_1 and more residue charge will be stored in D_1, which has to be removed at the reverse-recovery period, it is better to choose a smaller n which is close to $1/\sqrt{k}$ (from (3.11)).

3.3.2 Voltage Conversion Ratio V_o/V_{in}

Referring to the switching waveforms in Figure. 3.3, it is assumed that S1 is turned on a little later after i_{L1} and i_{D1} fall to zero. The delay time should be

π/ω_r in order to achieve low-voltage turn-on. Since π/ω_r is much shorter than the switching period T_s, L_1 can be regarded as operating in boundary or critical mode (between DCM and CCM). Using the voltage-second balance either on L_1 or L_2, the relationship between the input and output voltages of the proposed converter is given by

$$M = \frac{V_o}{V_{in}} = \frac{1}{1-d} \tag{3.33}$$

where d is the duty ratio of S1. Equation (3.33) shows that the voltage conversion ratio is the same as that of the conventional CCM boost converter.

3.3.3 Determination of Critical Inductance of L_1

As the converter is designed to have L_1 operating in boundary mode, the critical value of L_1 has to be determined. The average output current I_o, which is the sum of average rectifiers currents of D_1 and D_2, is given by

$$I_o = i_{D1,avg} + i_{D2,avg} \tag{3.34}$$

Equating the voltage-second balances on leakage inductances $(L_1 - L_M/n)$ and $(L_2 - nL_M)$ and substituting (3.33) into the equality, the relationship between the time intervals is obtained,

$$t_5 - t_4 = t_1 - t_0 \tag{3.35}$$

Substituting (3.26) and (3.35) into (3.34), the critical inductance of L_1 is found as

$$L_{1,crit} = \frac{R_o T_s}{2} \frac{n^2-1}{n^2(1-k^2)} d(1-d)^2 \tag{3.36}$$

where R_o is the loading resistance.

3.3.4 Control of Input/Output Current

In order to control i_{L1}, the controller circuit should be designed in such a way that S1 will be turned off when i_{L1} reaches a pre-determined value. S1 will be turned on again when i_{L1} reaches zero. A slight delay may be necessary to ensure that C_{oss} has been discharged and v_{DS1} has reached a minimum before S1 is turned on.

In effect, as can be seen from (3.33) and (3.36), both duty-cycle and frequency modulation are used for the control of i_{L1}. Since i_{L1} can be well controlled, the circuit may be easily designed to operate as a power-factor-correction circuit.

At present a number of commercial PFC controller ICs such as UC3852 and MC34262, which operate in critical conduction mode, can achieve the control purpose. When the controller switches on S1, i_{L1} is charged up linearly until it reaches the rectified sine wave envelope. This envelope is generated from the controller with magnitude controlled by the output voltage and the input rectified voltage. Using this envelope as a reference, the converter draws input current that follows in-phase with the rectified input voltage, achieving unity power factor. Meanwhile, the output voltage is also loosely regulated because the input current, hence the input power, is limited by the envelope. The controller also monitors i_{D1}. After i_{D1} reaches zero, a time delay signal equals π/ω_r is introduced by the zero current detector of the controller. This is to ensure v_{DS1} has been reached to minimum before S1 is turned on again to reduce turn-on switching loss.

3.3.5 Voltage and Current Stresses of Rectifiers and Switch

To estimate the voltage rating of the boost switch S1, it is assumed that the voltage spike appearing on v_{DS1} is completely absorbed by the parasitic capacitance C_{oss}, so that no voltage overshoot will occur. By analysing the switching waveforms one can see that the maximum voltages across the rectifiers and S1 are clamped to V_o when they are turned off. Without the addition of D_3 to the circuit, the maximum voltage on D_2, V_{D2}, will no longer being clamped to V_o but it is given by [16]

$$V_{D2} = V_o + (L_2 - nL_M) * di(rec)M/dt \tag{3.37}$$

A snubber is necessary to avoid excessive voltage stress on D_2 but it introduces additional loss. In the proposed converter, D_2 is always clamped by D_3 to V_o after it is turned off (at t_2 of Figure. 3.3). Moreover, the undesirable resonance between the leakage inductance of the coupled inductors and the parasitic capacitance of D_2 is eliminated, reducing the EMI noise.

The maximum current of S1 (also the peak current of D_1) is equal to the maximum current of L_1 at $t = t_4$. Taking into account the converter efficiency η and assuming that the time interval of $t_0 - t_1$ is far shorter than dT_s (true if k tends to one), the peak current of S1 (or D_1) can be found by combining (3.8), (3.13), (3.33) and (3.36)

$$i_{S1,max} = i_{D1,max} = \frac{2P_{o,max}}{\eta}\frac{G(k,n)}{V_{in}} \tag{3.38}$$

where

$$G(k,n) = \frac{n(n-k)}{n^2-1} \tag{3.39}$$

and $P_{o,max}$ is the maximum output power. Based on the above consideration and assumption, the peak current of D_2 and D_3 are found by combining (3.13), (3.16), (3.33) and (3.36)

$$i_{D2,max} = i_{D3,max} = \frac{2P_{o,max}}{\eta}\frac{H(k,n)}{V_{in}} \tag{3.40}$$

where

$$H(k,n) = \frac{nk-1}{n^2-1} \tag{3.41}$$

$G(k,n)$ and $H(k,n)$ are plotted against turns ratio n for different values of k, as shown in Figs. 3.10 and 3.11. It is noted that, for a given value of k, there is a point where $G(k,n)$ reaches a minimum (which corresponds to the lowest values of $i_{S1,max}$ and $i_{D1,max}$). Almost simultaneously, $H(k,n)$ reaches a maximum (which corresponds to the highest values of $i_{D2,max}$ and $i_{D3,max}$).

3.3.6 Control of Leakage Inductance

From the above analysis in Section 3, the coupling of L_1 and L_2 is essential to the overall converter operation. A toroidal core can be used to separate the windings aside (as being used in this paper), and yet share the same core and hence achieve certain coupling. The coupling can be controlled through sliding the windings along the core. A partially overlapping of the coupled inductors may result in tighter coupling. A more accurate way to implement the magnetizing and leakage inductances is to wind the cores separately.

As shown in Figures 3.5, 3.7, and 3.8, the converter will benefit from lower di/dt and transistor voltage stress if k is decreased. However, if k is too small,

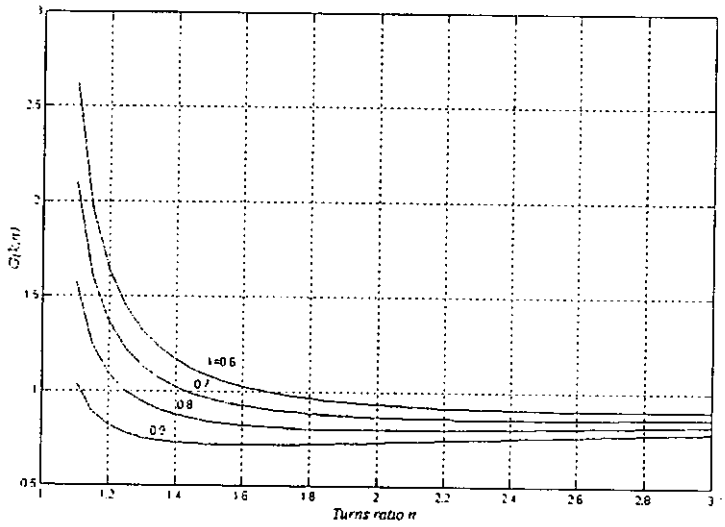


Figure 3.10: $G(k,n)$ versus turns ratio n for different values of k.

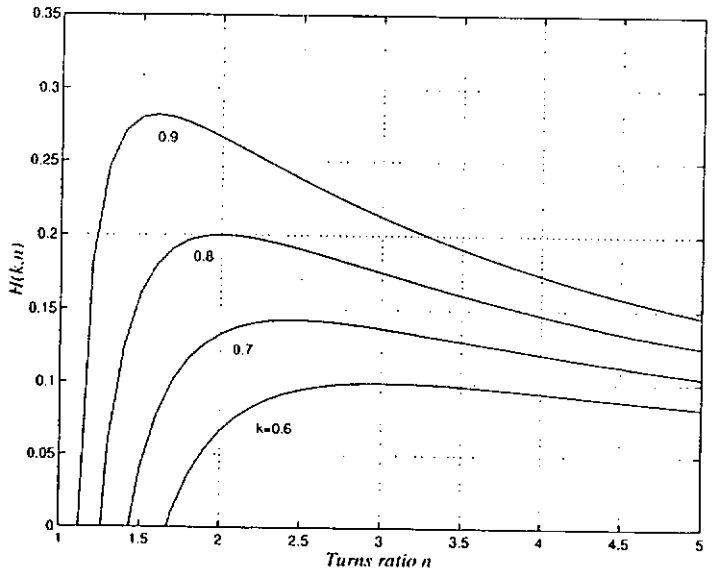


Figure 3.11: $H(k,n)$ versus turns ratio n for different values of k.

the current stress on S1 will then be increased. Moreover, the operation of Stage 2 which requires $n^2k > 1$ may not be guaranteed. D_3 will not conduct and achieve the clamping of D_2. Parasitic oscillation of D_2 with stray inductance and capacitance may occur as a result. Therefore, the optimal k obtained should be taken into account of voltage and current stresses of power components, di/dt of rectifiers, input current ripple, and switching frequency of the converter.

3.3.7 Design Considerations

As mentioned in circuit operation analysis, at Stages 3 to 5 D_3 is turned on and some energy is diverted back to the input source. This circulation energy should be kept to minimum in order to reduce overall conversion efficiency. Since the duration of i_{D3} is fixed by voltage conversion ratio, the di/dt and hence the average current can be reduced according to the inequality (3.10) or (3.11). That is, by making v_d small enough to just slightly be larger than V_{in}, the di/dt of D_3 can be reduced. This supports the analysis in Section 3.3.1.

Although the proposed converter is ideally fitted for high power applications, the RMS current of power devices should be noticed. Since the inductor currents operate either in critical or discontinuous conduction mode, the RMS currents increase as output power increases. The benefits of using the proposed converter may be diminished as compared to a standard CCM boost converter, which RMS current and conduction loss are the lowest among all operation modes.

3.4 Design Example

Based on the analysis in Section III, a design example will be presented. The specifications of the converter are as follows:

$$V_o = 150\text{V}$$
$$V_{in} = 100\text{V}$$
$$P_o = 40\text{W to } 200\text{W}$$
$$f_{s,min} = 50\text{kHz}$$

Here P_o is the output power and $f_{s,min}$ is the minimum switching frequency. The main design considerations are to find the optimized values of n and k, and the critical inductance of L_1, so that the soft-switching characteristic is preserved, the reverse-recovery currents are limited and the current stress on S1 is minimized. From the specifications the voltage conversion ratio is given by

$$M = \frac{150}{100} = 1.5 \tag{3.42}$$

The steady state duty ratio of the switch S1 can be obtained from (3.33) as

$$d = 1 - \frac{1}{1.5} = 0.33 \tag{3.43}$$

From Figure. 3.10, it can be seen that, n should be chosen to be around 2, where the current stress of S1 reaches its minimum value. Therefore the turns ratio is selected as

$$n = 2 \tag{3.44}$$

In the selection of k, it should be noted that a smaller value of k will result in a slower turn-off rate of D_1 and a lower turn-on voltage of S1. However, the current stress on S1 will then increase (for decreasing value of k). As a compromise, the coupling coefficient is chosen as

$$k = 0.8 \tag{3.45}$$

Substituting (3.43), (3.44), (3.45) and above specification parameters into (3.36), the critical inductance of L_1 is obtained as

$$L_{1,crit} = 347\mu H \tag{3.46}$$

Putting (3.44) and (3.45) into (3.11), we have

$$n^2 k = 3.2 > 1 \tag{3.47}$$

Equation (3.47) shows that the chosen values of n and k are valid to ensure a proper operation of the converter. Then from (3.17), the turn-off rate of D_1,

which is controlled by L_1, is given by $di_{D1}/dt = 2.4A/\mu s$. Supposing that the converter efficiency is 95%, we have $i_{S1,max} = 3.36$A at 200W output power. As the duty ratio is insensitive to load change according to (3.33), the switching frequency will be varied when the load is changed. The switching frequency f_s is maximum when the output power is minimum (i.e. R_o is maximum).

$$f_{s,max} = \frac{R_{o,max}}{2L_{1,crit}} \frac{n^2 - 1}{n^2(1 - k^2)} d(1 - d)^2 \tag{3.48}$$

In this example, the minimum output power is 40W (or $R_{o,max} = 562.5\Omega$). Therefore $f_{s,max}$=250kHz. Assuming the value of C_{oss} be 400pF, then from (3.20) we have $\beta = 0.67$. Substituting this value into (3.24) and (3.25), we can roughly estimate the capacitive turn-on loss as $P_{coss} = 0.68$W at minimum output power.

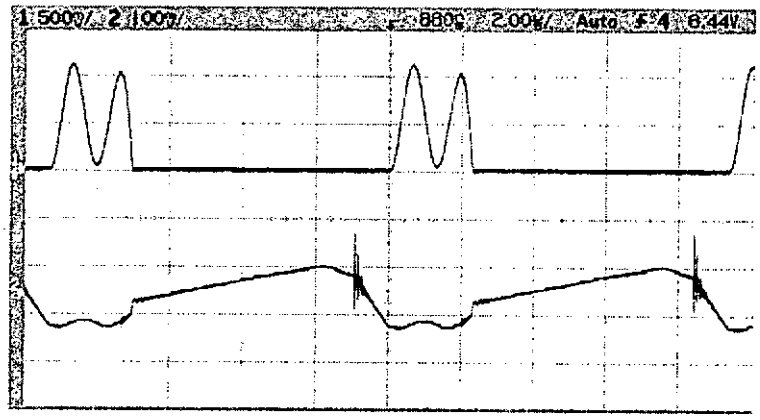
3.5 Experimental Results

Based on the design example described in the preceding section, an improved CCM boost converter is implemented. The hardware prototype has a 100Vdc input and a 200W (150V/1.33A) output. The duty ratio is kept at 0.33 to maintain the voltage conversion ratio. The switching frequency decreased from around 230kHz to 44kHz when the load current I_o increased from 0.25A to 1.33A. The details of the components used are tabulated in Table 1.

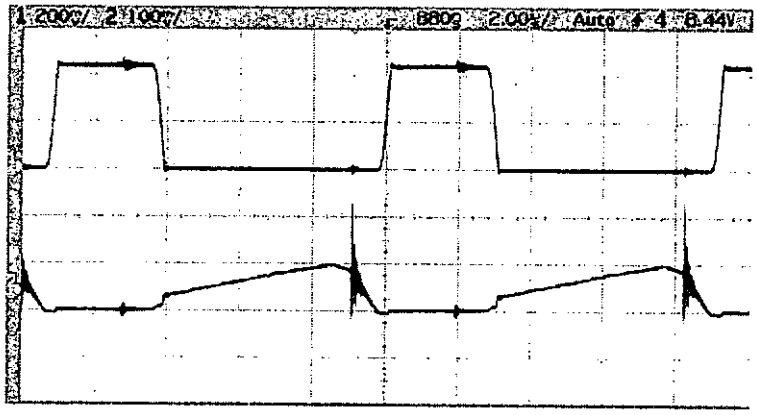
Figure. 3.12 shows the significant reduction of voltage stress and elimination of ringing caused by leakage inductance and parasitic capacitance of D_2 under same input-output condition (V_{in}=58V; V_o=80V; I_o=0.33A). Figure. 3.13 shows the waveforms of the drain-to-source voltage v_{DS1} of S1 and the currents of the rectifiers at a load current of 0.25A. Figure. 3.14 shows the waveforms at full

Component	Details
Coupled Inductors	$L_1 = 347\mu$H; $L_2 = 1.38$mH; $n = 2$; $k = 0.8$
MOSFET	MTW14N50E (for S1) with $C_{oss} = 280pF$
Rectifiers	MUR820 (for $D_1 - D_3$)
Capacitors	$C_o = 2 \times 220\mu F/250V$

Table 3.1: Details of components used in 150V-200W CCM boost converter.



(a) CH1: V_{D2} (100V/div); CH2: i_{D2} (200mA/div)



(b) CH1: V_{D2} (40V/div); CH2: i_{D2} (200mA/div)

Figure 3.12: Comparison of voltage stress on D_2: (a) Without D_3 added; (b) With D_3 added. Note the different voltage scale of CH1 of the two experimental setups under same measurement condition.

load (P_o=200W). As predicted, v_{DS1} is decreased in a resonant manner after i_{D1} has reached zero to provide a low-voltage turn-on of S1. It can be seen that all the rectifier turn-off rate are controlled and no reverse recovery current spikes appear in all the rectifiers at the turn-off instant. Notice that, as shown in Figs. 3.13 and 3.14, the parasitic ringing on i_{D2} is eliminated. Figure. 3.15 shows the detailed waveforms of v_{DS1} and i_{S1} at full load. Here it is found that no transient spike is observed at the instant of S1 turn-on. Figure. 3.16 shows the measured converter efficiency. It is found that the efficiency remains at 97% or higher for an output power of 80W to 150W.

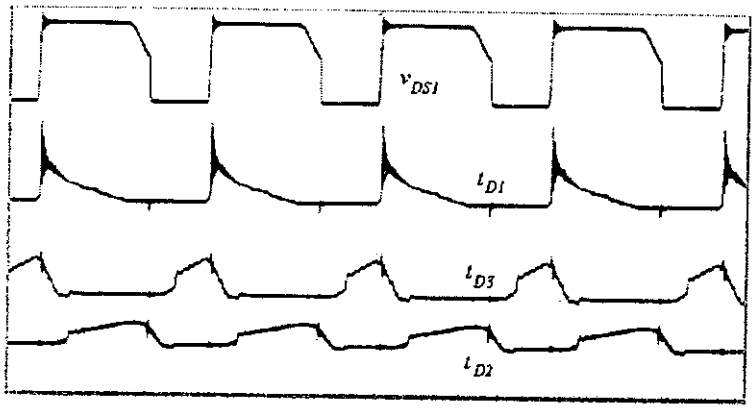


Figure 3.13: Measured drain-to-source voltage of S1 and rectifier currents at P_o=37.5W. (v_{DS1}: 100V/div; i_{D1}: 1A/div; i_{D3}: 200mA/div; i_{D2}: 500mA/div; time base: 2μs/div).

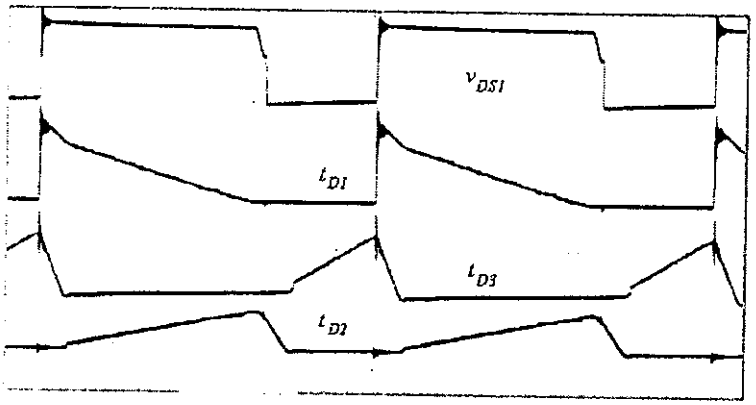


Figure 3.14: Measured drain-to-source voltage of S1 and rectifier currents at P_o=200W. (v_{DS1}: 100V/div; i_{D1}: 2A/div; i_{D3}: 500mA/div; i_{D2}: 1A/div; time base: 5μs/div).

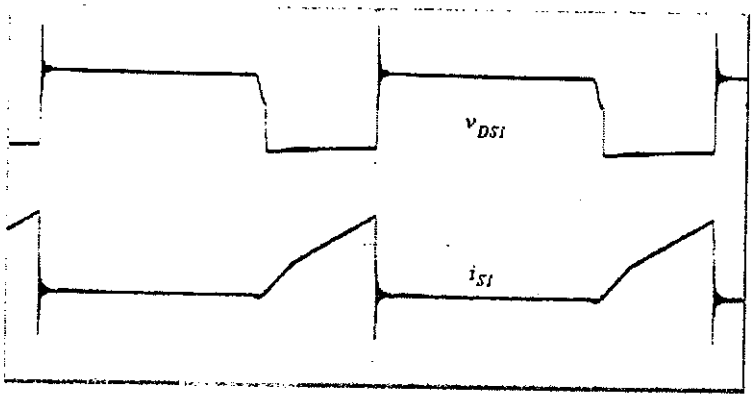


Figure 3.15: Measured drain-to-source voltage and current of S1 at P_o=200W. (v_{DS1}: 100V/div; i_{S1}: 2A/div; time base: 5μs/div).

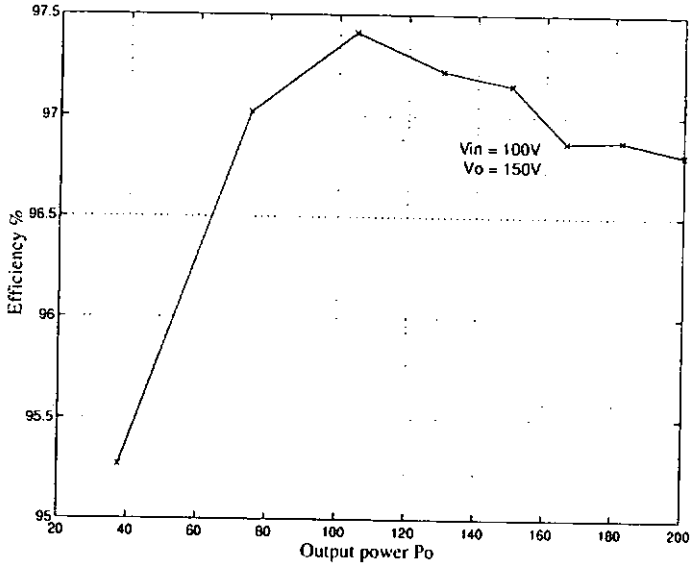


Figure 3.16: Measured efficiency of the proposed CCM boost converter at different output power levels.

3.6 Comparative Loss Analysis

A brief comparison of conduction loss of additional components of the proposed CCM boost converter to that of the conventional CCM boost converter is carried out and tabulated in Table 3.2. The conduction loss of diodes is calculated by integration of diode current according to experimental switching waveform and forward voltage drop provided by data sheet at particular forward current. It can be seen that the conduction losses are comparable. The conduction losses of D1 and D2 are due to the sharing of main output current of the proposed converter. Conduction loss of D3 is due to the circulation current.

3.7 Comparison with Saturable Inductor

A possible way to reduce the reverse-recovery related loss in CCM boost converter is to add a saturable inductor serially with the output rectifier. It is simple and no extra control is needed. However, this method does not eliminate reverse-recovery current but only convert this energy to hysteresis loss of saturable core with square-like BH loop. It is a dissipative method and the core grows very hot

Conduction Loss	Proposed CCM Boost	Conventional CCM Boost
D1	0.935	1.209
D2	0.198	N/A
D3	0.100	N/A
Total	1.233W	1.209W

Table 3.2: Comparison of components conduction losses at P_o=200W.

eventually. For the proposed converter, the reverse-recovery current of all rectifiers are reduced to minimum due to the limiting di/dt by the leakage inductance.

3.8 Summary

This chapter presents an improved single-switch CCM boost converter in which all the rectifiers are turned off softly. The turn-off rates of the rectifiers are controlled by the leakage inductances of the coupled inductors. Moreover, the boost switch can be operated under a low-voltage turn-on condition. The transient spike and parasitic ringing during the turn-on instant of the switch are successfully eliminated by the addition of a clamping rectifier. The theoretical analysis is verified by an experimental setup working at 200W output power. The concept depicted for the boost converter can also be extended to many other non-isolated converter topologies such as buck, buck-boost and Cuk. The converter is particularly useful for power factor correction applications.

Chapter 4

Voltage and Current Stresses Reduction Using an Auxiliary Transformer

4.1 Introduction

This chapter intends to solve the high storage capacitor voltage stress, high current stress on the power switch and limited conversion efficiency problems of single-stage power-factor-corrected (S^2PFC) converters, as mentioned in Chapter 2. The proposed method is to add an auxiliary transformer to the S^2PFC converter. This transformer provides a direct power transfer path for input line to output load after the first power process. The storage capacitor voltage and its range of voltage change against line voltage change are thus reduced. This also decreases the current stress and increases the conversion efficiency, due to this reduced repeated power processing. High power factor is maintained due to the elimination of dead angle of the input current. A similar idea has also been proposed at the same time [41], but the authors implemented the idea on a boost-forward converter working in continuous-conduction mode (CCM) with a discontinuous-conduction-mode (DCM) auxiliary transformer. The authors mainly concerned about the analysis of operation and the derivation of storage capacitor voltage. This chapter, however, presents comprehensive analysis and optimal design of a boost-flyback S^2PFC converter with the auxiliary

transformer working in both DCM and CCM. It is found that the auxiliary transformer with CCM operation reduces the voltage stress on decreasing load while it is not feasible in DCM operation. Experimental results of a 15V/60W prototype, with comparison to a S^2PFC converter without the auxiliary transformer, are given to show the proposed method effective.

4.2 Proposed S^2PFC Converter with DCM Auxiliary Transformer

4.2.1 Circuit Description

The proposed single-switch S^2PFC converter, which is formed by adding an auxiliary transformer (flyback transformer TR1) to a boost-flyback S^2PFC converter (with boost inductor L_B and flyback transformer TR2), is shown in Figure. 4.1. Both inductor and transformers are working in DCM. A low-loss snubber is added to the circuit for suppressing the transistor turn-off loss and recycling the leakage energy. The inductor L_B is used for improving the power factor and serving as a storage element for feeding the intermediate storage capacitor C_B. The flyback

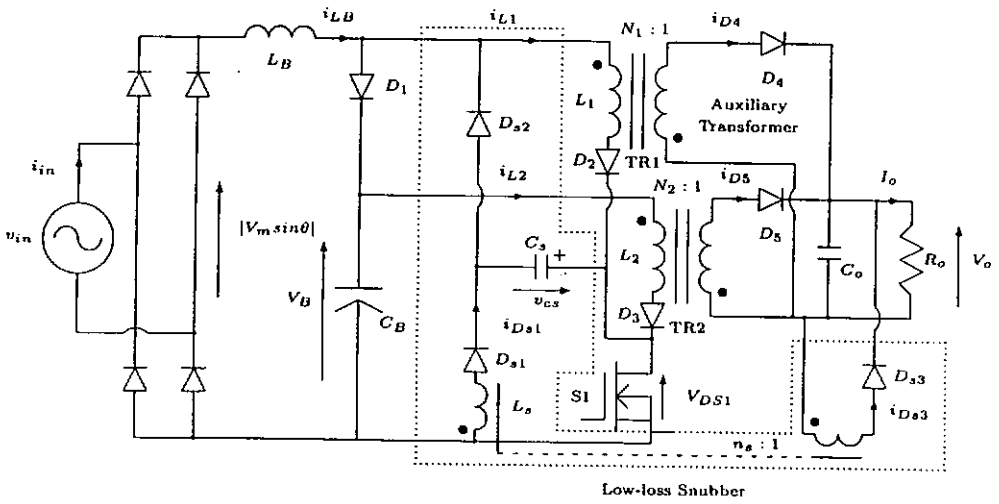


Figure 4.1: Proposed boost-flyback type single-switch single-stage power-factor-corrected (S^2PFC) converter with a low-loss snubber.

transformers TR1 and TR2 are used for transferring input power being processed once and twice, respectively, to the output. In the steady state, there are six modes of operation. The key theoretical waveforms within several switching periods are shown in Figure. 4.2.

4.2.2 Circuit Operation Analysis

To facilitate the analysis of the circuit, some assumptions are made. First, the capacitors C_B and C_o are large enough so that the voltage ripple on V_B and V_o are negligible; V_B and V_o are essentially dc voltage sources. Second, the switching frequency f_s (=$1/T_s$) is much faster than the line frequency so that the rectified input voltage $|V_m sin\theta|$ (V_m is the peak input voltage) within a switching interval is constant. Third, L_1 and L_2 represent the magnetizing inductances of transformers TR1 and TR2.

Mode 1 starts at $t = t_0$ when the power switch S1 is turned on. Since the storage capacitor voltage V_B is always higher than the rectified line voltage $|V_m sin\theta|$, D_1 is blocked and L_B and L_1 are linearly charged up by $|V_m sin\theta|$ at the same rate,

$$\frac{di_{LB}}{dt} = \frac{di_{L1}}{dt} = \frac{|V_m sin\theta|}{L_B + L_1} \tag{4.1}$$

Meanwhile, L_2 is linearly charged up by the bulk capacitor C_B. The charge stored in C_s is also discharging through L_s. The decreasing slope of the charging rate, di_{Ds1}/dt, indicates that the charge in C_s is being removed. The output capacitor C_o sustains the output voltage V_o. The mode ends when S1 is turned off.

In operation Mode 2 at $t = t_1$, S1 is turned off and the energy stored in the leakage inductance (not shown for brevity) of TR1 and TR2 is being transferred to C_s through paths $L_1 - D_2 - C_s - D_{s2}$ and $L_2 - D_3 - C_s - D_{s2} - D_1$ respectively. At the same time, the energy stored in L_s is diverted to the load. Note that the turns ratio of the snubber transformer is chosen such that the energy stored in L_s will not be dumped to C_B. Power loss will be reduced if energy is diverted to the load directly. Therefore the following inequality should be satisfied,

$$n_s V_o < V_B \tag{4.2}$$

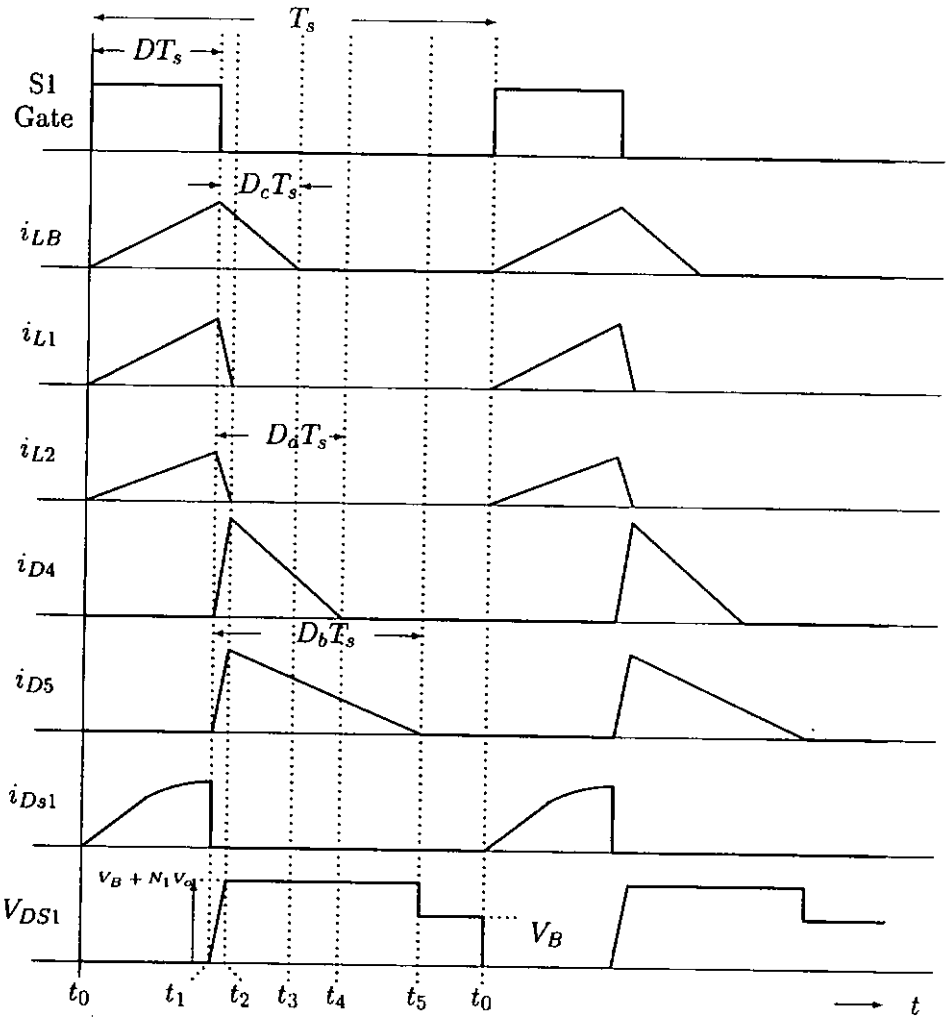


Figure 4.2: Key theoretical waveforms within several switching periods.

This interval ends when the leakage energy has been transferred to C_s.

Mode 3 starts at $t = t_2$. The energy stored in L_1 and L_2 are transferred to the output load through TR1-D_4 and TR2-D_5 respectively. At the same time, L_B delivers its stored energy to C_B with a rate of

$$\frac{di_{LB}}{dt} = \frac{V_B - |V_m sin\theta|}{L_B} \tag{4.3}$$

Note that L_B and L_1 form a power divider network for which some portion of input power is transferred to the output through L_1 directly to increase conversion efficiency and reduce the level of V_B. In (4.1) and (4.3), the effective inductance during charge and discharge periods of the input inductor are $L_B + L_1$ and L_B

respectively. The smaller effective inductance during discharge period gives a faster discharging rate. This reduces the input current distortion. The drain-to-source voltage of S1, V_{DS1}, rises to $V_B + N_2 V_o$. This interval ends when L_B has released all its energy.

During operation Mode 4 ($t_3 - t_4$), energy stored in TR1 and TR2 continue to discharge through D_4 and D_5 respectively. At the end of the interval, TR1 is reset. i_{D4} must reach zero before the next turn-on period of S1, otherwise the remnant current will reflect to the primary side of TR1 and add up to i_{LB} causing distortion to the input current. At the end of operation Mode 5 ($t_4 - t_5$), TR2 is reset. In operation Mode 6 ($t_5 - t_0$), there is no energy left either in the inductor or the transformers. C_o sustains the output voltage and V_{DS1} stays at the bulk capacitor voltage V_B. At the end of this mode, S1 turns on again to begin the next switching cycle.

4.3 Steady State Analysis

In this section, the voltage across the storage capacitor C_B, the power factor and power distribution under different inductance ratios of L_B/L_1 and L_1/L_2 will be investigated. To facilitate the analysis and design, some useful expressions such as the duty ratio, the voltage conversion ratio of V_B to V_m, and the average input current are derived.

4.3.1 Duty Ratio D

Since the boost converter operating in DCM corrects the power factor automatically, power factor correction and output voltage regulation of a S^2PFC converter can be achieved simultaneously by solely controlling the output voltage. Referring to Figure. 3.3, the time to charge up C_s (at $t_1 - t_2$) is far shorter than the period to discharge TR1 and TR2. Moreover, the leakage energy recycled by the snubber transformer only contributes to a tiny portion of the total output power. Therefore, the averaged output current can be approximated by the sum of i_{D4}

and i_{D5}

$$I_o = \frac{DT_s}{2}\left(\frac{N_1 V_m|sin\theta|}{L_B + L_1}D_a + \frac{N_2 V_B}{L_2}D_b\right) \tag{4.4}$$

where T_s is the switching frequency. D_a and D_b are the duty ratios as shown in Figure. 3.3 and they can be found by voltage-second balance on L_1 and L_2 respectively,

$$D_a = D\frac{V_m|sin\theta|L_1}{N_1 V_o(L_B + L_1)} \tag{4.5}$$

$$D_b = D\frac{V_B}{N_2 V_o} \tag{4.6}$$

Substitute (4.4), (4.5) and (4.6) into the following equation

$$V_o = I_o R_o \tag{4.7}$$

then yields the steady state equation of the duty ratio

$$D(\theta) = \sqrt{\frac{2M_1^2 L_2 \beta(1+\alpha)^2}{R_o T_s\left[|sin\theta|^2 + M_2^2\beta(1+\alpha)^2\right]}} \tag{4.8}$$

where $M_1 = V_o/V_m$, $M_2 = V_B/V_m$, $\alpha = L_B/L_1$ and $\beta = L_1/L_2$. It can be seen that the duty ratio of the proposed circuit varies according to the input voltage.

4.3.2 Voltage Conversion Ratio of V_B to V_m, M_2

Since the storage capacitor voltage V_B determines the inductor and transformers values, the power factor as well as the portion of power distribution by TR1 and TR2, it is necessary to derive an expression for V_B. Consider the energy stores in C_B during the off-state period of S1. The averaged L_B current during this period equals the averaged capacitor current. It is given by

$$i_{LBO,avg} = \frac{\alpha D(\theta)^2 T_s}{2L_2(\alpha+1)^2}\left[\frac{V_m^2|sin\theta|^2}{V_B - V_m|sin\theta|}\right] \tag{4.9}$$

While the on-state period of S1, the capacitor transfers energy to store in L_2 and its averaged capacitor current equals the averaged L_2 current

$$i_{L2,avg} = \frac{D(\theta)^2 T_s}{2L_3}V_B \tag{4.10}$$

In steady state, the averaged capacitor current over a half line cycle should be zero, that is

$$\int_0^\pi i_{LBO,avg}d\theta - \int_0^\pi i_{L2,avg}d\theta = 0 \tag{4.11}$$

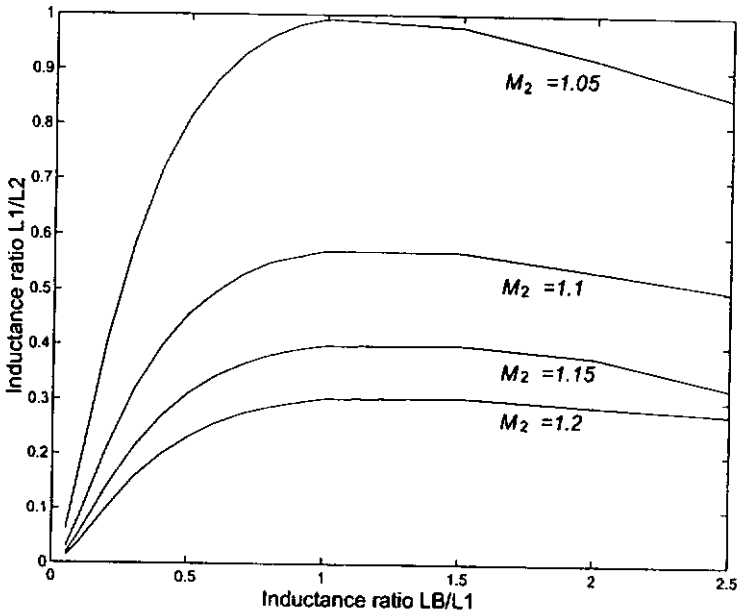


Figure 4.3: Inductance ratio of $L_1/L_2(=\beta)$ against $L_B/L_1(=\alpha)$ for values of different $M_2(=V_B/V_m)$.

Substituting (4.8), (4.9) and (4.10) into (4.11) and rearranging of terms, a transcendental expression of M_2 is found,

$$M_2 = \frac{V_B}{V_m} = \frac{\int_0^{\pi} \frac{|sin\theta|^2 \alpha\beta(\alpha+1)^2 d\theta}{(M_2-|sin\theta|)\left[|sin\theta|^2+M_2^2\beta(\alpha+1)^2\right]}}{\int_0^{\pi} \frac{\beta^2(\alpha+1)^4 d\theta}{|sin\theta|^2+M_2^2\beta(\alpha+1)^2}} \tag{4.12}$$

From (4.12) it can be seen that M_2 depends on α and β only and it can merely be solved by numerical method. According to (4.12), the inductance ratio $L_1/L_2(=\beta)$ is plotted against $L_B/L_1(=\alpha)$ for different values of $M_2(=V_B/V_m)$ and is shown in Figure. 4.3. It is shown in Figure. 4.3 that for a given value of α, V_B increases (or M_2 increases) with increasing value of L_2 (or a decreasing ratio of β). The increase in V_B can be explained as following. When L_2 becomes larger, the rate of change of i_{L2} and also the energy stored in L_2 will be decreased. The turn-on time of S1 is made longer by the feedback compensation network to maintain the output voltage constant. The energy stored in L_B and hence C_B will be increased. V_B is therefore shifted up to higher level. For a given value of β, V_B increases (or M_2 increases) with an increasing value of L_B (or an increasing ratio of α). It is because when L_B gets larger it will store a larger portion of input energy as L_B and L_1 are charged up in series when S1 is turned on. More

energy will be fed to C_B. However, when α continues to increase (or L_1 continues to decrease), TR1 will handle less output power than that of TR2. In addition, the increase in α also brings down the charging rate of L_B and L_1 and so as the energy stored in them. Therefore energy to be stored in C_B will be getting less and V_B will be shifted to a lower level. This explains the fall of the curves when α increases.

4.3.3 Condition of Good Power Factor PF

Since the input current i_{in} equals i_{LB}, the instantaneous average input current, $\bar{i}_{in}$, can be calculated by considering the area of the triangular waveform within a switching cycle, we have

$$\bar{i}_{in} = \frac{V_m D(D + D_c)T_s}{2(L_B + L_1)}|sin\theta| \tag{4.13}$$

where D_c is the ratio of time for L_B to discharge. From the voltage-second balance on L_B we obtain

$$D_c = D\frac{\alpha}{(\alpha+1)}\frac{|sin\theta|}{M_2 - |sin\theta|} \tag{4.14}$$

Substitute (4.14) into (4.13), the average input current over a half line cycle becomes

$$\bar{i}_{in} = \frac{V_m D^2 T_s}{2L_2(\alpha+1)}\int_0^{\pi} |sin\theta| F(\theta) d\theta \tag{4.15}$$

where

$$F(\theta) = \frac{(M_2 - |sin\theta|)(\alpha+1) + |sin\theta|}{M_2 - |sin\theta|)(\alpha+1)} \tag{4.16}$$

Moreover, the rms value of the input current is

$$I_{in,rms} = \frac{V_m T_s}{2\sqrt{\pi}L_1(\alpha+1)}\sqrt{\int_0^{\pi} D^4 |sin\theta|^2 F(\theta)^2 d\theta} \tag{4.17}$$

The input power is calculated from the product of $|V_m sin\theta|$ and $\bar{i}_{in}$, which is expressed by

$$P_{in} = \frac{V_m^2 T_s}{2\pi L_1(\alpha+1)}\int_0^{\pi} D^2 |sin\theta| F(\theta) d\theta \tag{4.18}$$

Since the power factor is the ratio of average input power to the apparent power, we have

$$PF = \frac{P_{in}}{V_{m,rms} I_{in,rms}} \tag{4.19}$$

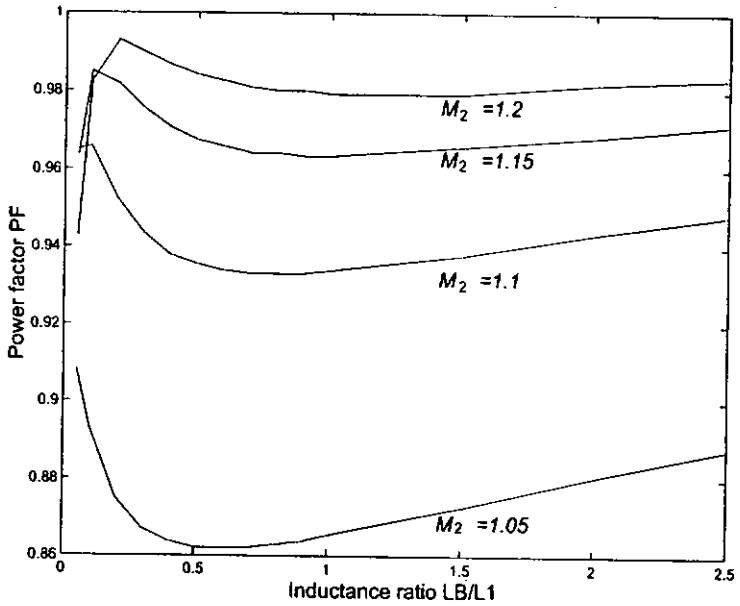


Figure 4.4: Calculated power factor against $L_B/L_1(=\alpha)$ for different values $M_2(=V_B/V_m)$.

Substitute (4.8), (4.17) and (4.18) into (4.19), we finally get the expression of the power factor, which is given by

$$PF = \sqrt{\frac{2}{\pi}} \frac{\int_0^\pi G(\theta)F(\theta)d\theta}{\int_0^\pi [G(\theta)F(\theta)]^2 d\theta} \tag{4.20}$$

where

$$G(\theta) = \frac{(\alpha+1)^2 sin^2\theta}{sin^2\theta + \beta(\alpha+1)^2 M_2^2} \tag{4.21}$$

From (4.20) a set of graphs showing the relationship between α and the power factor for different values of M_2 is shown in Figure. 4.4. It can be seen that the proposed circuit has already reached a power factor around 0.98 for only $M_2 = 1.2$ and when $\alpha \geq 0.2$. To compare the power factor capability to that of the S^{2}PFC converters [22], Figure. 4.5 shows the plot of V_B versus V_{in} at different values of power factor. It is clear that the proposed S^{2}PFC converter attains the same power factor with lower V_B. Moreover, the proposed circuit reduces the range of voltage change against the line voltage change. Note that the selection of storage capacitor is determined by the capacitance needed for hold-up time requirement at low line full load and by the maximum tolerable voltage at high line. From Figure. 4.5 again we can see that, as compared to the S^{2}PFC converters [22], the proposed S^{2}PFC converter needs a storage capacitor

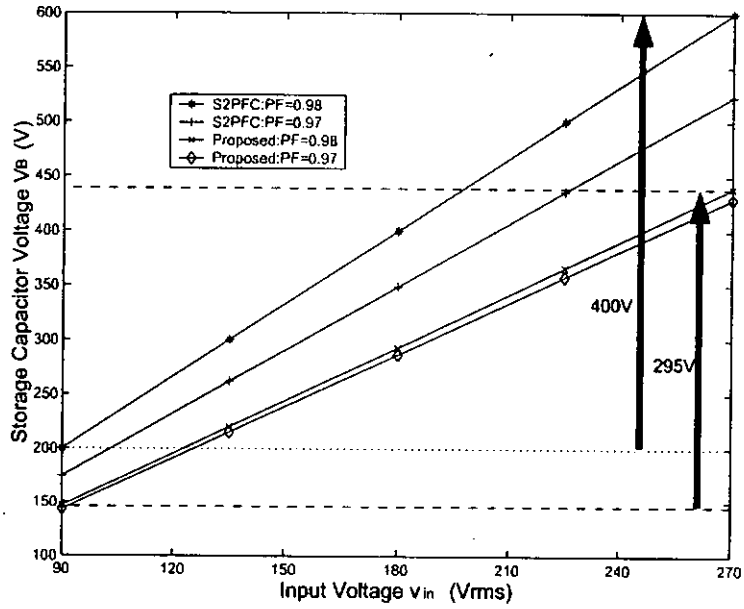


Figure 4.5: Comparison of storage capacitor voltage as a function of rms line voltage of the S^{2}PFC converter in [22] and the proposed S^{2}PFC converter for different values of power factor.

with slightly larger capacitance but with much smaller voltage rating. Therefore, it is possible for the proposed S^{2}PFC to select a smaller C_B.

4.3.4 Power Distribution by TR1 and TR2

For the proposed S^{4}PFC converter, the output power delivered by transformer TR1 is processed once, and that by transformer TR2 is processed twice. The output power is given by

$$Po = \frac{V_o^2}{R_o} = \frac{V_m^2 D^2 T_s}{2L_2}\left[\frac{|sin\theta|^2}{(\alpha+1)^2} + \beta M_2^2\right] \tag{4.22}$$

In the square blanket of (4.22), the first term and the second term represent the output power contributed by TR1 and TR2 correspondingly. By the assumption of constant duty ratio D for simplified analysis, the portion of output power handled by TR1 and TR2 are found as, respectively,

$$P_{o,TR1} = \frac{V_o^2}{R_o}\frac{\int_0^\pi |sin\theta|^2 d\theta}{\int_0^\pi \left[|sin\theta|^2 + \beta(\alpha+1)^2 M_2^2\right] d\theta} \tag{4.23}$$

$$P_{o,TR2} = \frac{V_o^2}{R_o}\frac{\beta(\alpha+1)^2 M_2^2}{\int_0^\pi \left[|sin\theta|^2 + \beta(\alpha+1)^2 M_2^2\right] d\theta} \tag{4.24}$$

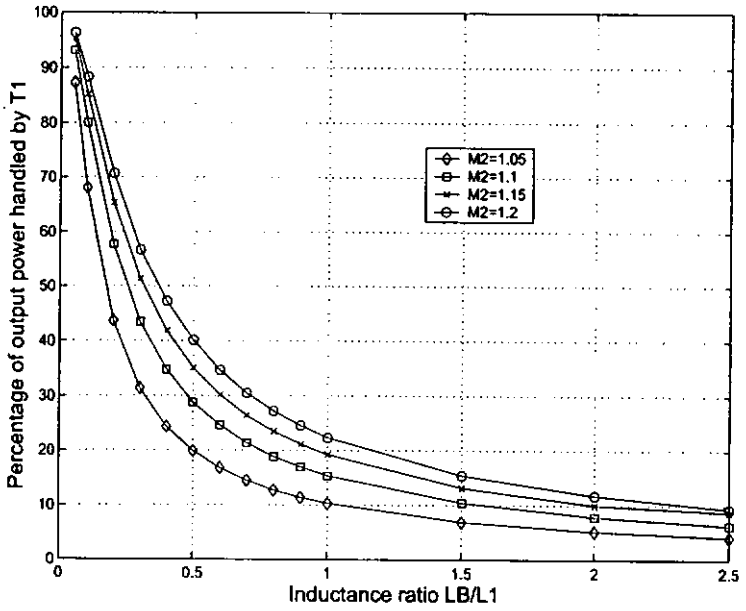


Figure 4.6: Percentage of output power delivered by TR1.

Figure 4.6 shows the percentage of output power delivered by TR1 at different α. It is seen that, with smaller value of α (M_2 also decreases as indicated in Figure 4.3), TR1 handles more input power to be processed once. This results in higher conversion efficiency as less input power will be processed twice. The re-process of input power causes extra loss to components in the form of heat. From Figure 4.6 it is also observed that, for a given value of α, higher M_2 increases the percentage of input power handled by TR1. Since the pre-determined power factor constrains the level of M_2, the only possible way to increase conversion efficiency is to select a smaller value of α. However, as will be discussed in next section, if α is chosen to a very small value, the inductances of L_B and L_1 will decrease rapidly such that high current stress will be imposed on the semiconductor devices.

4.4 Optimal Design of the Converter

The turns ratios N_1 and N_2 are critical parameters to determine the operation mode of the inductor and transformers, the peak currents on the devices and the voltage stress on the switch. The proposed S^{4}PFC converter should be designed such that i_{LB}, i_{D4} and i_{D5} become discontinuous before the start of the next turn-on period of S1.

For a given V_o, the discharging rates of i_{D4} and i_{D5} are determined by the square of turns ratios and the inductances. To prevent L_2 from entering into CCM, $D_b \leq (1-D)$ must be satisfied. The maximum value of L_2 can be found as (which can be determined when $sin\theta = 0$),

$$L_{2,max} = \frac{R_o T_s}{2}\left(\frac{N_2 M_2}{M_2 + N_2 M_1}\right)^2 \tag{4.25}$$

Take an example of a 15V-60W output S^{4}PFC converter with switching frequency of 75kHz and it is designed to operate over a wide range of line input voltage (90-140Vrms). From (4.25), L_2 reaches its maximum value when the peak input voltage V_m is at its minimum ($M_1 = V_o/V_m$), and $M_1 = 15/(90\sqrt{2})$=0.118. Figure. 4.7 shows the plot of $L_{3,max}$ against the turns ratio N_2 for different values of M_2 at minimum V_m. To reduce the current stress on the diodes and switch of the primary side, L_2 must be chosen with a larger N_2 and close to the maximum value since the switch current stress decreases with increasing value of L_2 (or N_2),

$$i_{S1,pk} = \frac{V_m D T_s}{L_2}\left[\frac{|sin\theta|}{\beta(\alpha+1)} + M_2\right] \tag{4.26}$$

The peak current of S1 also occurs at the peak input voltage, that is, $|sin\theta| = 1$. Considering the output section, the maximum current stress on D_5 occurs when $|sin\theta| = 0$ (for TR2 delivers the total output power). The peak current of D_5 is

$$i_{D5,pk} = N_2 V_o \sqrt{\frac{2T_s}{R_o L_{2,max}}} \tag{4.27}$$

Equation (4.27) shows that a small N_2 is preferred. The maximum peak current of D_4, which happens at the peak input voltage (i.e. $|sin\theta| = 1$) is given by,

$$i_{D4,pk} = N_1 V_o \sqrt{\frac{2T_s}{R_o L_2\left[\beta(\alpha+1)^2 M_2^2 + 1\right]}} \tag{4.28}$$

From (4.28), an increase in the value of L_1 and a decrease in the value of N_1 lower the peak current of D_4. Since $L_1(=\beta L_2)$ is selected from L_2, α and β for the desired power factor and the power distribution percentage of TR1, we need to use a minimum value for N_1. If TR1 is operated in DCM, $D_a \leq (1-D)$ must be fulfilled. The constraint for N_1 is

$$N_1 \geq \frac{|sin\theta|}{M_1(\alpha+1)}\frac{D}{1-D} \tag{4.29}$$

The value of L_2 chosen from (4.25) is used for defining the duty ratio D in (4.8). The minimum value of N_1, must be greater than the maximum value calculated in (4.29). For i_{LB} operating in DCM, we first consider the waveforms of i_{LB} and i_{D4} in Figure. 3.3. Assume i_{D4} works in DCM, the following inequality must be satisfied

$$\frac{D_c}{D_a} \leq 1 \tag{4.30}$$

Substituting the voltage-second balance of L_B and L_1 into (4.30), we obtain

$$N_1 \leq \frac{M_2 - sin\theta}{\alpha M_1} \tag{4.31}$$

N_1 will be a minimum value when $sin\theta = 1$ (as $M_2 \geq 1$), so (4.31) becomes

$$N_1 \leq \frac{M_2 - 1}{\alpha M_1} \tag{4.32}$$

Equation (4.32) provides the upper limit for N_1 to prevent L_B from operating in CCM. To understand the limits of N_1 for proper DCM operation of the converter, (4.29) and (4.32) are used to plot a set of curves, as shown in Figure. 4.8, illustrating the relationship between N_1 and α for different values of N_2 at $M_2 = 1.15$. M_2 is set to 1.15 for obtaining high power factor (>0.96) and keeping $V_B <$ 450V at high line. Note that the range of α for keeping L_B in DCM is narrowed with increasing value of N_2. Figure. 4.9 shows that the maximum voltage stress on the switch S1 is $V_B + N_2 V_o$ at high line voltage. It is obvious that $N_2 \leq 10$ is preferred to limit the voltage stress on S1 (<600V). Although a larger N_2 reduces the switch peak current, yet a higher voltage stress is imposed on the switch however. As the switching loss of S1 is the area of cross conduction of the current flowing through S1 and the voltage across it, it may not be an advantage of increasing N_2 to minimize the current stress on S1. However, a lower turns ratio reduces the current stresses on output diodes. It can be concluded that, a small turns ratio of N_2 is preferred for 15V-60W output ratings and should be chosen near the boundary mode of L_B to reduce the peak current of S1. Referring to Figure. 4.4 again, α should be selected to be 0.5 or smaller to keep the power factor around 0.97. And from Figure. 4.9, turns ratio $N_2 = 6$ is therefore chosen.

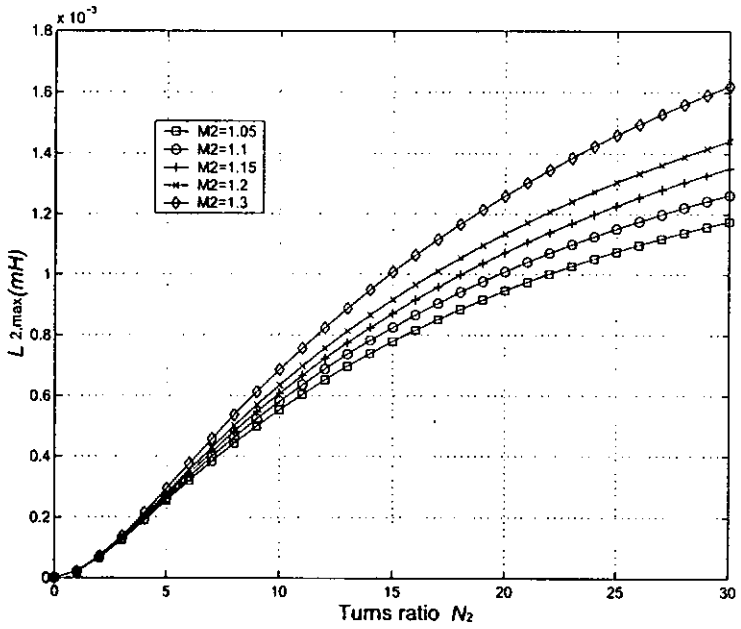


Figure 4.7: Maximum L_2 against turns ratio N_2 for values of different $M_2(= V_B/V_m)$.

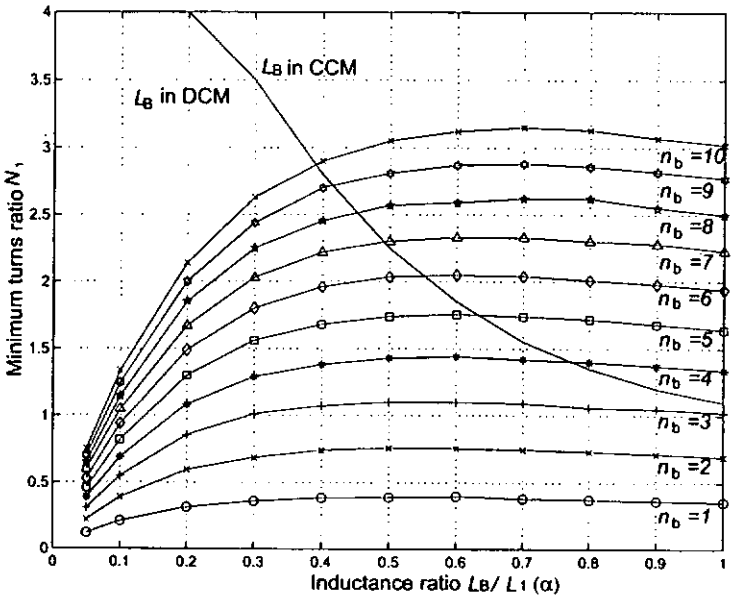


Figure 4.8: Minimum turns ratio N_1 of TR1 to operate in DCM for different values of $L_B/L_1(= \alpha)$ and turns ratio N_2 at $M_2 = 1.15$.

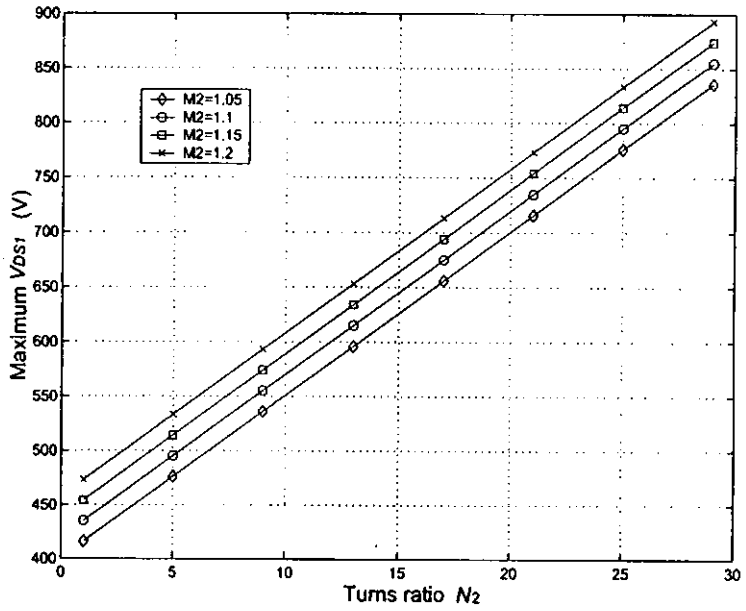


Figure 4.9: Maximum voltage stress on S1 at high line (v_{in} = 265$Vrms$) for different values of M_2 and N_2.

4.5 Controller Design

The controller used for the proposed single-switch S^{2}PFC converter resembles commonly used voltage-mode PWM controller. The input current will be automatically shaped for high power factor provided with DCM operation of input inductor. The controller shall only montior and control the output voltage according to line and load variations. Commercial voltage-mode PWM controller ICs such as TL494 and TL5001A can be used.

4.6 Experimental Results

In order to confirm the theoretical analysis of the proposed single-switch S^{2}PFC converter, the converter shown in Figure. 4.1 was implemented with an 15V-60W output for wide line voltage application (90-140Vrms) at a 75kHz switching frequency. The control circuit used a voltage-mode PWM controller IC TL494 for output voltage regulation. According to the design criteria in Section 3, the converter parameters are summarized as follows. L_B=53μH; L_1=106μH;

N_1=2.04; L_2=340μH and N_2=6. The power components used are: MT6N60E (S1); MUR460 (D_1-D_3) and MUR860 (D_4-D_5). The measured filtered (an input LC filter with inductance and capacitance equal 4mH and 680nF respectively) line-current waveform and the line-voltage is shown in Figure. 4.10. The measured power factor at this point is 0.953, which is close to the predicted value of 0.967. The discrepancy may be caused by the slight distortion of the line-voltage in the experimental setup while it is assumed to be a pure sinusoidal waveform in the theoretical analysis. The power factor and current total harmonic distortion (THD) of the converter at different line voltage and load conditions are shown in Figures. 4.11 and 4.12 respectively. Figure. 4.13 shows the measured converter efficiency, which rises gradually as load current increases. This may due to the decrease in diode forward voltage drop and increase in duty ratio. It can also be seen that as line voltage increases the converter efficiency drops lightly because the voltage snubber handles more recycle energy (v_{cs} increases as v_{in} increases) and power dissipation through snubber increases. It may be remedied by using a larger value of L_s. The maximum converter efficiency is recorded at 82% at low-line condition. A comparison between the proposed converter to the conventional one without the auxiliary transformer under the same condition is carried out. L_B/L_2 is set to 0.75 to give power factor of 0.97. Based on (4.25), L_2 in this case is the same as was designed in the proposed S^{2}PFC converter. The storage capacitor voltage for the proposed S^{2}PFC converter is always lower than converter without the auxiliary transformer with same power factor (around 0.96) as shown in Figure. 4.14. From Figure. 4.15, it can be seen that the proposed S^{2}PFC converter also has higher efficiency.

4.7 Proposed S^{2}PFC Converter with CCM Auxiliary Transformer

The circuit diagram of the proposed single-switch S^{2}PFC converter, which is the same in Figure 4.1 but without the low-loss snubber, is re-drawn in Figure. 4.16. The converter consists of a DCM boost inductor L_B to shape the input current

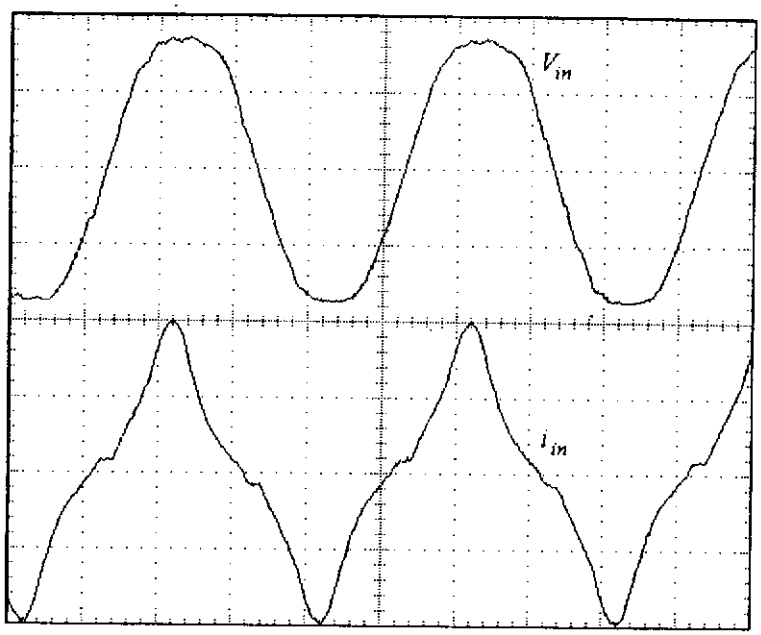


Figure 4.10: Measured filtered line-voltage v_{in} (100V/div) and filtered line-current i_{in} (2A/div) at $V_{in,rms} = 140V$ and full load ($I_o = 4A$). (Time bse: 5μs/div)

and to deliver energy to the storage capacitor. The auxiliary flyback transformer TR1, working mainly in CCM, is used to control the input current, to reduce the current stress of the power switch and to provide a direct power transfer path to the converter. Transformer TR2 mainly works in CCM and is used to maintain output voltage constant.

To simplify the analysis of the converter, all components are assumed ideal. The basic operation of the proposed converter is depicted as follows. When the power switch S1 is turned on, the boost inductor L_B and primary inductance of TR1 L_1 are charged up linearly in series by the rectified input voltage $|v_{in}|$. At the same time, the primary inductance of TR2 L_2 is also charged up linearly by the storage capacitor V_B. Diodes D_3 and D_4 are reverse biased due to the blocking voltage which equals the output voltage plus the reflected primary voltage on the secondary (dotted end is positive with respect to non-dotted end). The output capacitor sustains the output voltage V_o. After some time S1 turns off, diode D_1 is also reverse biased. Diode D_B conducts to maintain the current flow through L_B. Meanwhile, TR1 and TR2 deliver stored energy to output through D_3 and

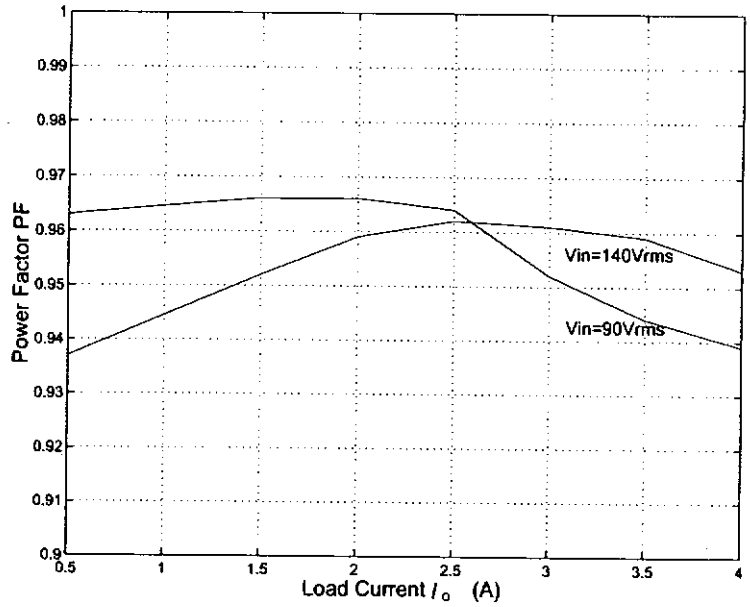


Figure 4.11: Measured power factor under line and load variations.

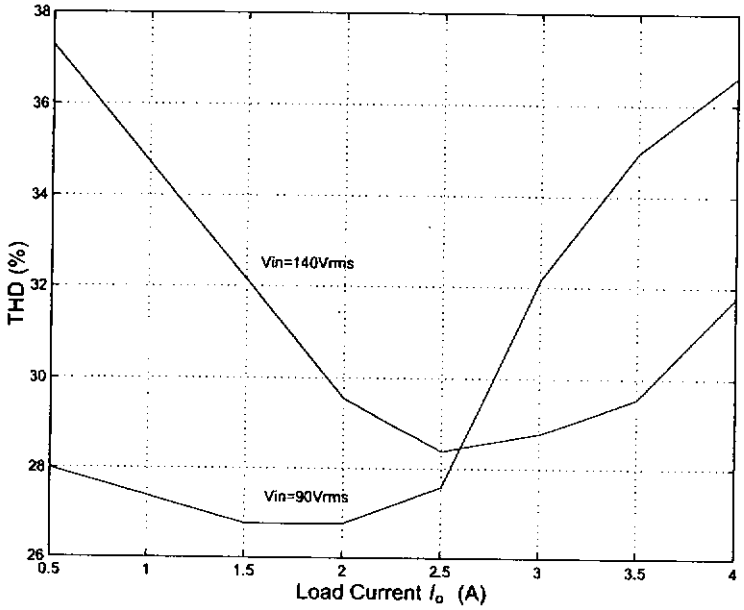


Figure 4.12: Measured current THD under line and load variations.

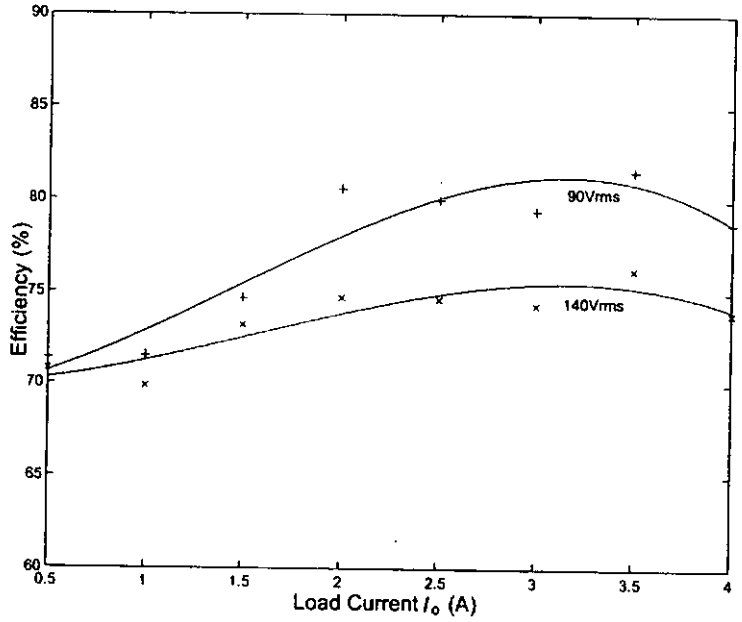


Figure 4.13: Measured converter efficiency under line and load variations.

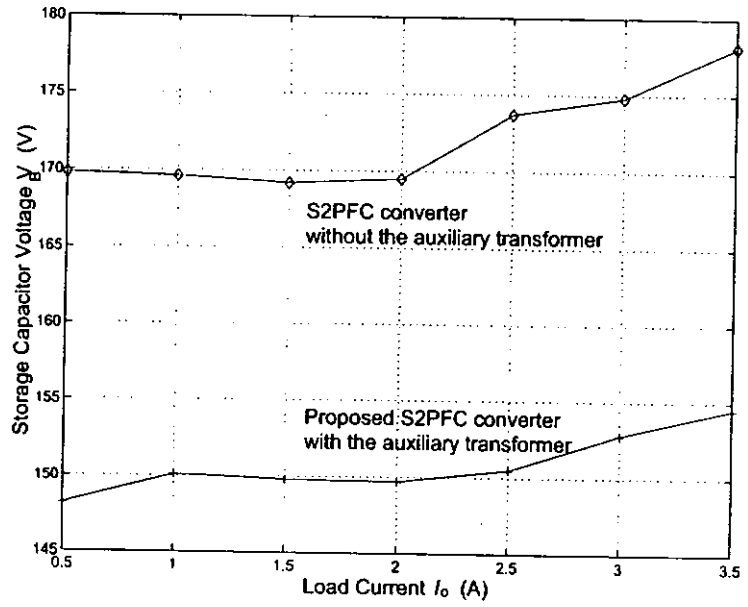


Figure 4.14: Comparison of storage capacitor voltage between the S^2PFC converters with and without the auxiliary transformer (with same power factor) at $V_{in,rms} = 90V$.

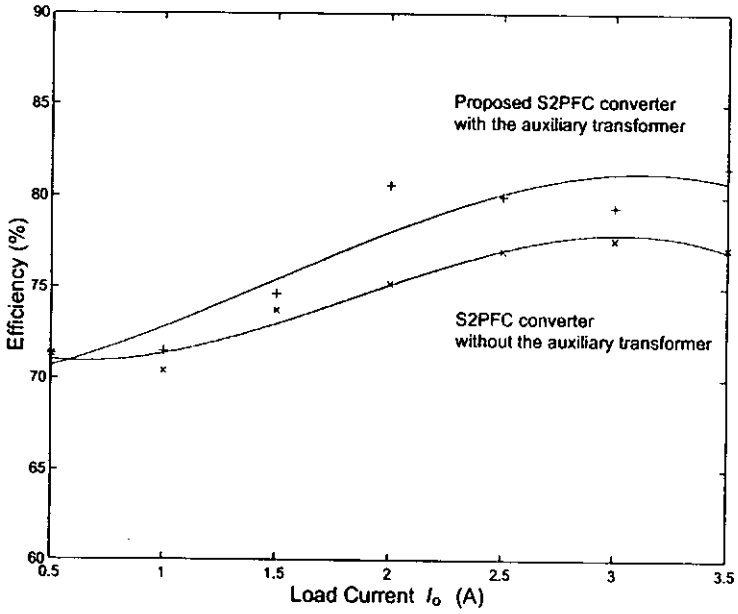


Figure 4.15: Comparison of converter efficiency between the S^{2}PFC converter with and without the auxiliary transformer at $v_{in} = 90Vrms$.

D_4 respectively (non-dotted end is positive with respect to dotted end). Before S1 is turned on again to begin the next switching cycle, all the energy stored in L_B is completely transferred to C_B. Otherwise L_B will operate in CCM and distort the input current.

When $|v_{in}|$ traverses a half line cycle, the currents of TR1 and TR2 enter different modes of operation, as shown in Figure. 6.3. Note that the current waveforms of i_{LB}, i_{L1} and i_{L2} shown in Figure. 6.3 are current envelops but not averaged values. Although TR2 mainly works in CCM, the change of energy transfer of TR1 due to line voltage variation alters the current level of TR2. There are three modes of operation (M1-M3), as shown in Figure. 4.18, throughout the half line cycle, which are described as follows:

Mode 1 [Figure. 4.18(a)]: During this mode (M1 in Figure. 4.17), TR2 runs in CCM. Since the input power is smaller than the output power, TR2 handles most the output power and TR1 operates in DCM. Considering the voltage-second

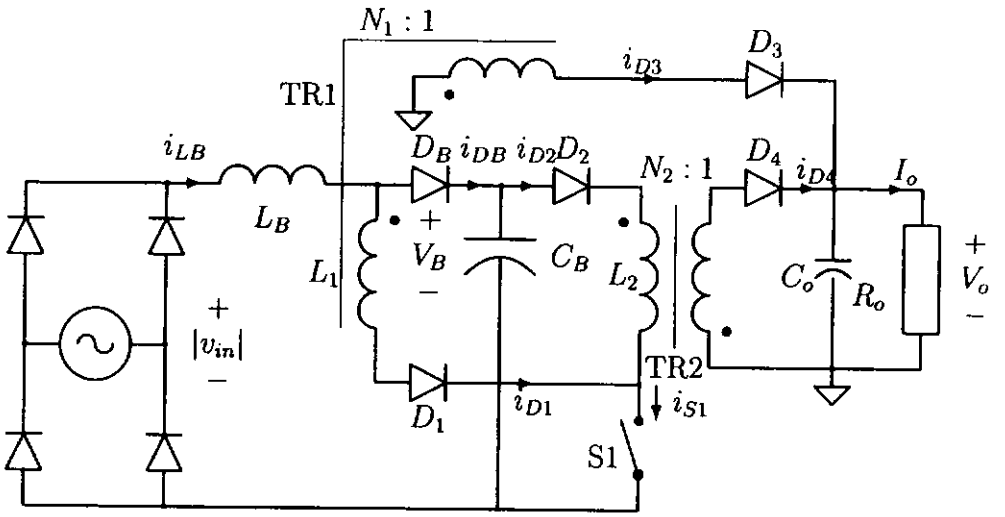


Figure 4.16: Proposed single-switch single-stage power-factor-corrected converter S^2PFC converter with auxiliary transformer TR1 in CCM.

balance of TR2, the duty ratio D of S1 is given by

$$D = \frac{N_2 V_o}{N_2 V_o + V_B} \tag{4.33}$$

which resembles a normal CCM flyback converter with a constant duty cycle and tight output regulation. As $|v_{in}|$ increases, more input power as well as output power will be handled by TR1. This pushes TR2 towards DCM as TR1 provides more output current.

Mode 2 [Figure. 4.18(b)]: In this mode (M2 in Figure. 4.17), TR2 still runs in CCM but with smaller magnitude of current through D_4. TR1 operates in CCM and handles most of the output power as $|v_{in}|$ increases further. The duty ratio of S1 remains constant (same as (4.33)) because TR2 automatically corrects the current difference between D_3 and D_4 to maintain a constant output current.

Mode 3 [Figure. 4.18(c)]: Within this mode (M3 in Figure. 4.17), TR2 is forced to run in DCM due to the increasing transfer of energy from TR1 as $|v_{in}|$ rises towards its peak value. The duty ratio of S1 can be derived from the

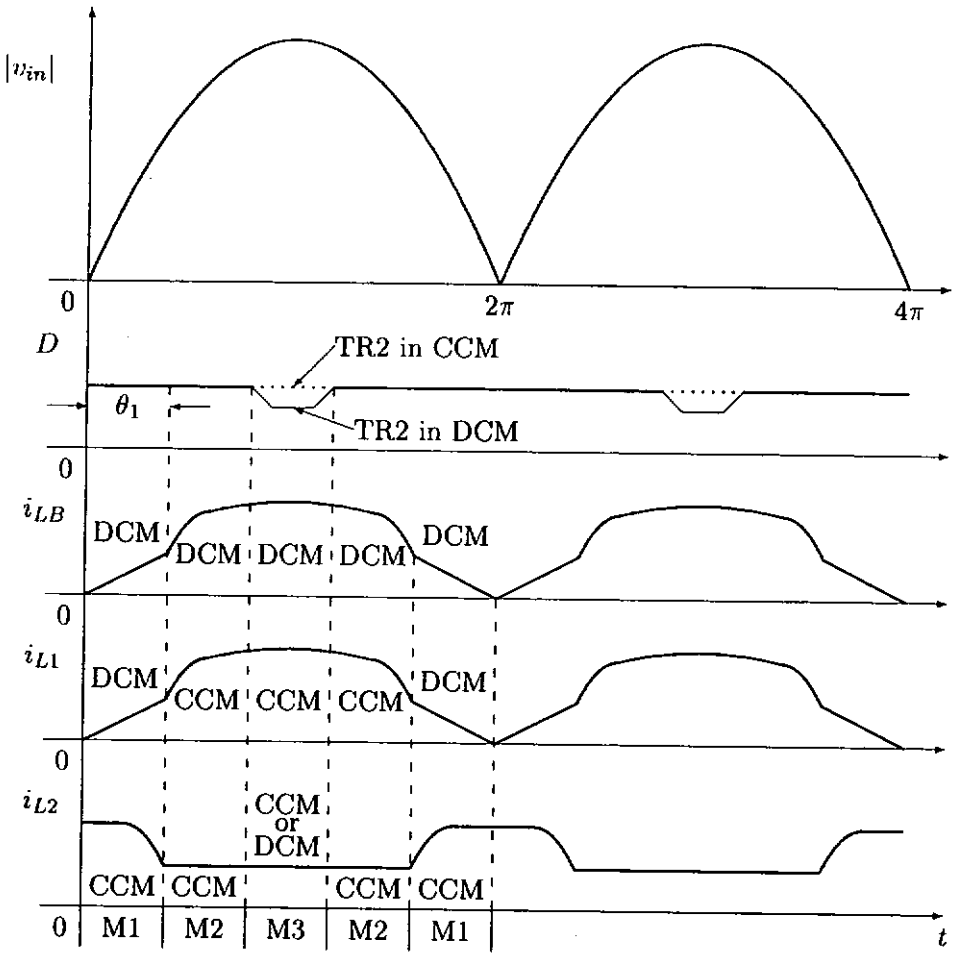
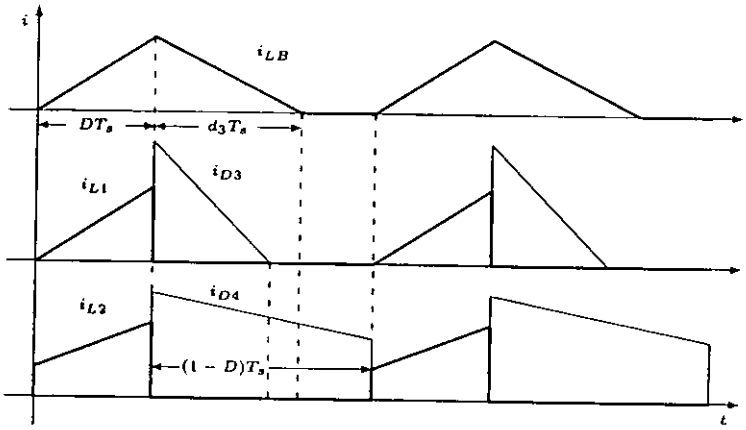


Figure 4.17: Key switching waveforms of the proposed S^{2}PFC converter at different modes of operation during a line cycle.

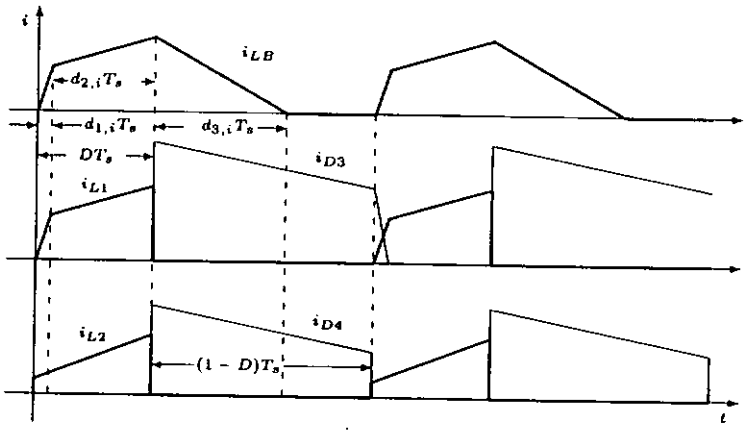
voltage-second balance of TR1 and is given by

$$D = (1 + d_1) - \frac{L_1}{L_1 + L_B} \frac{|v_{in}|}{N_1 V_o} d_2 \tag{4.34}$$

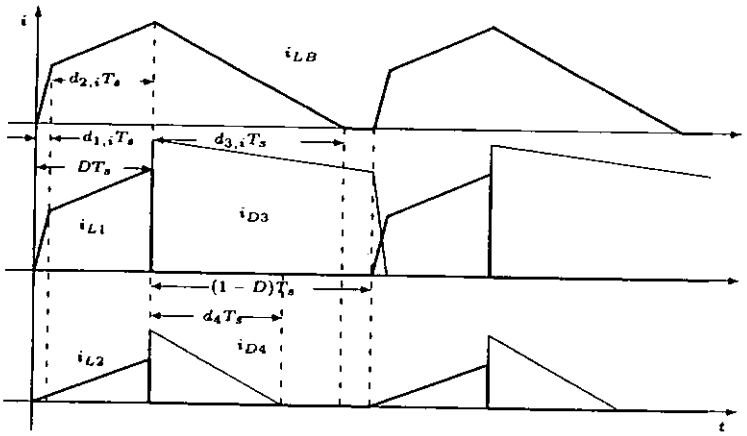
Note that the duty ratio now depends not only on the output voltage and circuit parameters, but also on the rectified line voltage. Since the power delivered from TR1 increases until peak input voltage is reached, D is decreased to maintain output power constant. When the line voltage decreases from its peak value, the operation of TR1 and TR2 go back to Mode 2 and then to Mode 1 when $|v_{in}|$ falls near the zero crossing region.



(a) Mode 1



(b) Mode 2



(c) Mode 3

Figure 4.18: Inductor and diode currents at different operation modes.

4.8 Expression of the Storage Capacitor Voltage

The derivation of the storage capacitor voltage expression is essential to modeling and design of the proposed S^{2}PFC converter. Figure. 4.18 shows the current waveforms of the boost inductor L_B and transformers TR1 and TR2 at different modes of operation. In Mode 1, the instantaneous average input current, which equals the averaged i_{LB} within a switching cycle T_s, is obtained from the area of triangular current waveform.

$$\bar{i}_{LB,M1} = \frac{D(D+d_3)T_s}{2(L_B+L_1)}|v_{in}| \tag{4.35}$$

The discharging time ratio d_3 is expressed as

$$d_3 = \frac{L_B}{L_B+L_1}\frac{D|v_{in}|}{V_B-|v_{in}|} \tag{4.36}$$

While in Mode 2, the boost current experiences an additional fast slope at the instant of switch turn-on due to the CCM operation of TR1. The instantaneous average input current is thus given by

$$\bar{i}_{LB,M2} = \frac{T_s}{2}\left[d_{1,i}(2D-d_{1,i}+d_{3,i})\frac{|v_{in}|+N_1V_o}{L_B} + (D-d_{1,i})(D-d_{1,i}+d_{3,i})\frac{|v_{in}|}{L_B+L_1}\right] \tag{4.37}$$

where

$$d_{3,i} = \left[\frac{L_1}{L_B+L_1}d_{1,i}(|v_{in}|+N_1V_o) + \frac{L_B}{L_B+L_1}D|v_{in}|\right](V_B-|v_{in}|)^{-1} \tag{4.38}$$

$$d_{1,i} = a_i\left[\frac{N_1^2V_o}{L_1} + \frac{N_1(|v_{in}|+N_1V_o)}{L_B}\right]^{-1} \tag{4.39}$$

$$a_i = N_1\left[b_{i-1} + \frac{(D-d_{1,i-1})T_s}{L_B+L_1}|v_{in}|\right] - \frac{N_1^2V_o}{L_1}(1-D)T_s \tag{4.40}$$

$$b_i = \frac{|v_{in}|+N_1V_o}{L_B}d_{1,i}T_s \qquad i=1,2,3,...,n \tag{4.41}$$

n is the number of switching period within the interval of Mode 2. The interest of study here is to find when Mode 2 starts as it helps to predict the voltage and current stresses, which will be investigated in Section V and VI respectively. At the transition period of Mode 1 to Mode 2, i_{D3} is operated just in the boundary mode (i.e. S1 turns on at the instant i_{D3} becomes zero). Consider the fall period

of i_{D3}, which equals $(1-D)T_s$, we obtain the angle of input voltage (θ_1 in Figure. 6.3) where Mode 2 starts,

$$\theta_1 = arcsin\left[\left(1+\frac{L_B}{L_1}\right)\frac{N_1 V_B}{N_2 V_m}\right] \tag{4.42}$$

where $|v_{in}| = V_m|sin\theta|$ and V_m is the peak input voltage. Due to the symmetrical property of $|v_{in}|$, Mode 2 ends at $\pi - \theta_1$. During Mode 3, the boost current is the same as that in Mode 2, though TR2 works in DCM and the duty ratio is changed from (4.33) to (4.34).

In the steady state, the energy absorbed by the converter during a half of line cycle is equal to the integral of the product of instant rectified input voltage and average input current (boost inductor current), which is given by

$$E_{in} = \int_0^{\theta_1} |v_{in}| \cdot \bar{i}_{LB,M1} d\theta + \int_{\theta_1}^{\pi-\theta_1} |v_{in}| \cdot \bar{i}_{LB,M2} d\theta + \int_{\pi-\theta_1}^{\pi} |v_{in}| \cdot \bar{i}_{LB,M1} d\theta \tag{4.43}$$

Assume in lossless condition that the energy absorbed equals the energy output during a half line cycle (i.e. $E_{in} = E_{out}$), the energy output can be expressed in terms of output power P_o and line period T_L.

$$E_{out} = P_o \cdot \frac{T_L}{2} \tag{4.44}$$

Therefore, the storage capacitor voltage expression can be found by equating (4.43) and (4.44), which is given by

$$\begin{gathered}\int_0^{\theta_1} |v_{in}|^2 \cdot \tfrac{D(D+d_3)T_s}{L_B+L_1} d\theta + \\ \int_{\theta_1}^{\pi-\theta_1} |v_{in}| \cdot T_s \left[d_{1,i}(2D - d_{1,i} + d_{3,i})\tfrac{|v_{in}|+N_1V_o}{L_B} + (D-d_{1,i})(D-d_{1,i}+d_{3,i})\tfrac{|v_{in}|}{L_B+L_1}\right] d\theta + \\ \int_{\pi-\theta_1}^{\pi} |v_{in}|^2 \cdot \tfrac{D(D+d_3)T_s}{L_B+L_1} d\theta - T_L \cdot P_o = 0\end{gathered} \tag{4.45}$$

It is noted that this expression is transcendental and can only be solved by specific circuit parameters. In addition, equation (4.45) solely concerns the modes of operation for either or both transformers working in CCM, which happens at heavy load. At light load condition, it is possible that both transformers operate in DCM for the entire line cycles. The equations derived above are then not valid to describe the storage capacitor voltage. The duty ratio and storage capacitor voltage for both transformers work in DCM have been found in (4.12).

If TR1 and TR2 operate in Mode 1 to Mode 3 at heavy load, the storage capacitor voltage V_B is determined by (4.45). In contrast to the existing S^{2}PFC converter topologies, even for those with the negative voltage feedback technique [27]-[29], V_B of the proposed converter decreases as load reduces. This will be proved analytically and experimentally in Section V and VIII respectively. When TR1 and TR2 are both run in DCM, V_B is independent of load, as shown in (4.12). In order to determine the mode of boundary, the discharging ratio d_4 of TR1 in DCM is considered at the peak of input voltage V_m. In this case, both transformers will be operated in DCM and $d_4 \leq 1 - D$. Substituting this inequality into (4.8) and relating it to the power-voltage equation, we come up with the critical output power $P_{o,crit}$ of the mode of boundary.

$$P_{o,crit} = V_o^2 \cdot \left\{ \left[1 + \frac{L_1 V_m}{(L_B + L_1) N_1 V_o} \right] \cdot \sqrt{\frac{2 L_1 L_2 (L_B + L_1)^2 V_o^2}{T_s \left[L_1 L_2 |v_{in}|^2 + V_B^2 (L_1 + L_B)^2 \right]}} \right\}^{-2} \tag{4.46}$$

4.9 Analysis of Voltage Stress Reduction

The voltage stress reduction on the storage capacitor of the proposed circuit is achieved in two ways : 1) energy split by boost inductor L_B and transformer TR1 and 2) input current reduction through transformer TR1 operating in CCM.

4.9.1 Energy Split by Inductor L_B and Transformer TR1

With the insertion of TR1 into the input stage of the converter, the input energy from $|v_{in}|$ is split into two portions. One portion is stored in L_B where energy will be fed to C_B. The rest is stored in TR1 where energy will be directly coupled to output. Figure. 4.19 shows the effect on V_B for different values of inductance ratios using the equations (4.45) to (4.46) derived in Section IV. On one hand, the ratio of boost inductance to auxiliary flyback magnetizing inductance (L_B/L_1) reduces, the storage capacitor voltage V_B will be decreased. This is due to the fact that more input energy will be diverted to the output through the auxiliary flyback transformer, without being stored in C_B. On the other hand, if the

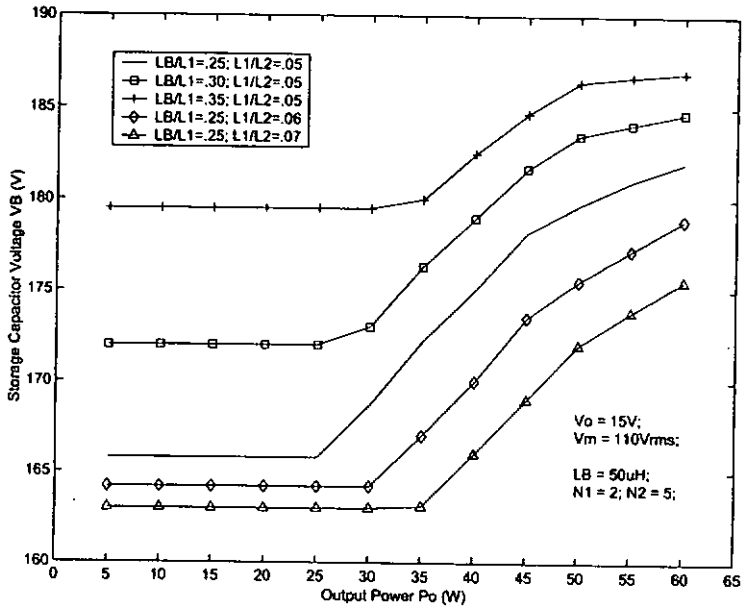


Figure 4.19: Estimated V_B for different values of inductance ratios.

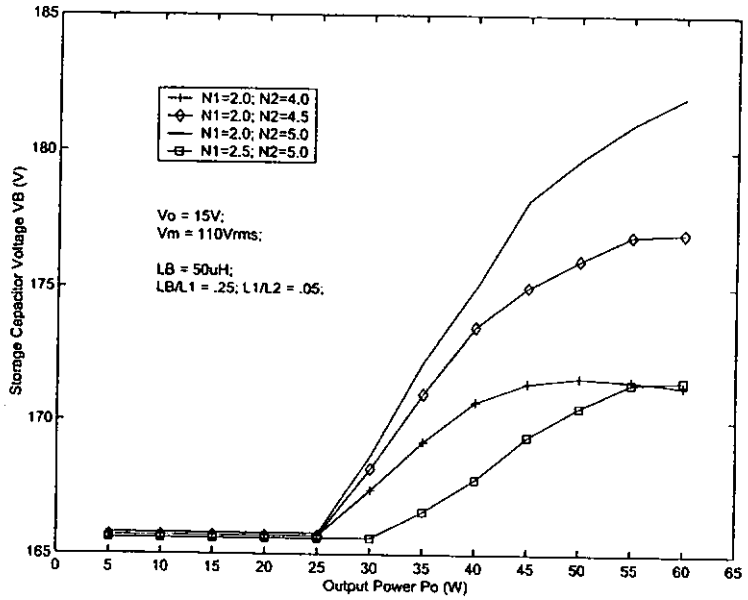


Figure 4.20: Estimated V_B for different values of turns ratios.

ratio of auxiliary flyback magnetizing inductance to main flyback magnetizing inductance (L_1/L_2) increases, the storage capacitor voltage V_B will be decreased as well. This is because, viewing from the output side, TR1 handles more output power when (L_1/L_2) increases. With less power handled by TR2, less energy will be stored in C_B and hence V_B is reduced. The turns ratios (N_1 and N_2) of the converter also affect the level of V_B. As shown in Figure. 4.20, when N_1 increases or N_2 decreases, V_B is reduced. With the increase of N_1 or decrease of N_2, more output current and hence output power will shifted to TR1. It is observed from Figure. 4.20 that N_1 has much greater impact on V_B than that of N_2. Besides, the fluctuation of V_B is reduced with decreasing value of N_2.

It is noted that when $L_B/L_1 = 0$ (i.e. absence of L_B), all input power will be processed by TR1. The voltage across C_B will be minimum for which V_B is clamped to the peak of input voltage. In this case, however, the current harmonics increases rapidly as it incurs dead angle of input current. This is equivalent to a capacitor-filtered converter without PFC control.

4.9.2 Input Current Control by CCM of TR1

The input current control begins when the converter enters Mode 2 where TR1 is operating in CCM. To illustrate the effect of input current control, Figure. 4.21 shows the instant when the load R_o becomes light. Assume the load reduces within the short period from t_p to t_0, the downslopes of the output diodes currents, i_{D3} and i_{D4}, will be increased (indicated in Figure. 4.21 as thin lines) due to the increase of output voltage as mentioned in Section II. When the switch S1 turns on at t_0, L_B and L_1 will both experience faster charging slopes (L_B and L_1 charge up in series). The rate of change of i_{LB} and i_{L1} are equal, which is given by

$$\frac{di_{LB}}{dt} = \frac{di_{L1}}{dt} = \frac{|v_{in}| + N_1 V_o}{L_B} \tag{4.47}$$

From (4.47), it is observed that the input current ($=i_{LB}$) carries the load information through the reflected output voltage, which contains the sudden change of load resistance. On one hand, the current in transformer TR2 will be automatically reduced due to this decrease of load, so that less energy will be taken

from C_B. On the other hand, with this slight increase of output voltage due to load reduction, the peak input current as well as the average input current will be reduced. Therefore, less energy is being stored up in C_B, preventing the rise in V_B.

In addition, in the steady state D_3 and D_4 will have higher peak currents at heavy load than that at light load. This results in a longer interval of t_0 to t_1 which allows the inductor currents (i_{LB}, i_{L1} and i_{L2}) to ramp up higher and store more energy even though the rate of change of currents at different loading conditions are the same. Therefore the duty ratio of S1 can remain roughly constant for wide load change. To verify the above analysis, a series of computer simulation of the circuit in Figure. 4.16 using PSpice circuit simulator is performed. The circuit parameters are $L_B = 50\mu$H, $L_1 = 200\mu$H, $N_1 = 2.2$, $L_2 = 1$mH, $N_2 = 5$, v_{in} = $90V_{rms}$ and 60W/15V$_{DC}$ output is tested. Figure. 4.22 shows the simulation results of the S^{2}PFC converter in Mode 2 at full load (60W) and half load (30W) conditions. It can be seen that the duty ratio remains roughly unchanged at different loading conditions. Although the preceding analysis is conducted for Mode 2 only, the input current reduction still performs in Mode 3 since TR1 continues to work in CCM.

As mentioned in [41]-[42], when the auxiliary transformer operates in DCM, voltage level on storage capacitor throughout the output power range is reduced. However, it cannot help reduce the rising voltage stress on light load condition. This is because the secondary current of the auxiliary transformer falls to zero before the end of each switching cycle. At the instant when the power switch is turned on, the magnetizing inductance is charging from zero. Thus, the state of load (represented as load current) will not be brought to the input stage. For the proposed converter with auxiliary transformer TR1 operated in CCM, however, V_B is reduced at light load due to the input current control feature. Mathematical estimation of V_B as plotted in Figures. 4.19 and 4.20 has been proved the proposed approach effective. Experimental verification will be given in Section VIII.

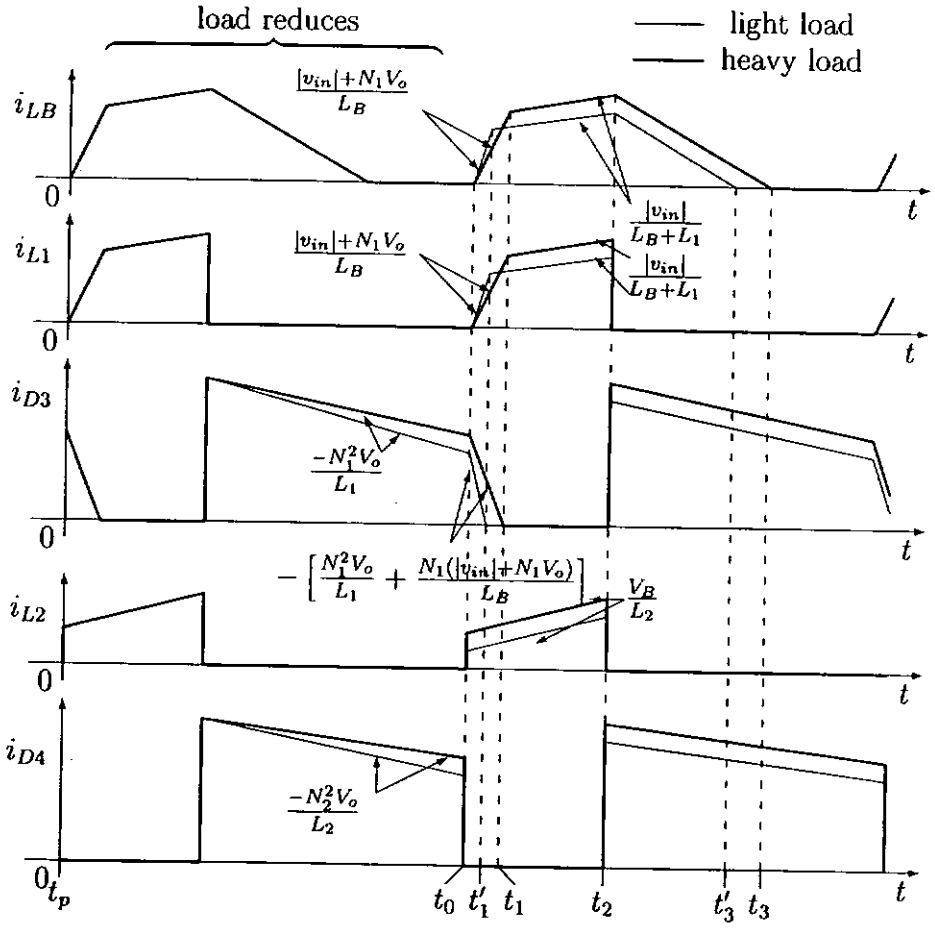


Figure 4.21: Input current control of the proposed S²PFC converter in sudden change of load current.

4.10 Analysis of Current Stress Reduction

The average switch current $\bar{i}_{S1}$ of the converter is the sum of boost charging and main flyback (TR1) primary currents, which is given by

$$\bar{i}_{S1} = (\bar{i}_{LB} - \bar{i}_{DB}) + \bar{i}_{L2} = (\bar{i}_{LB} - \bar{i}_{DB}) + \frac{V_o}{V_B}(I_o - \bar{i}_{D3}) \qquad (4.48)$$

It can be observed that if $i_{D3} = 0$ (i.e. absence of TR1), the converter resembles a normal single-switch S²PFC converter such that S1 has to handle all the currents from the line input $|v_{in}|$ and the storage capacitor C_B. With the increase of i_{D3}, more output current will be provided by TR1 and hence the average switch current will be reduced as anticipated from (4.48). However, as $\bar{i}_{L1} = \bar{i}_{LB} - \bar{i}_{DB}$, which increases when i_{D3} is increased, a more tangible comparison should be

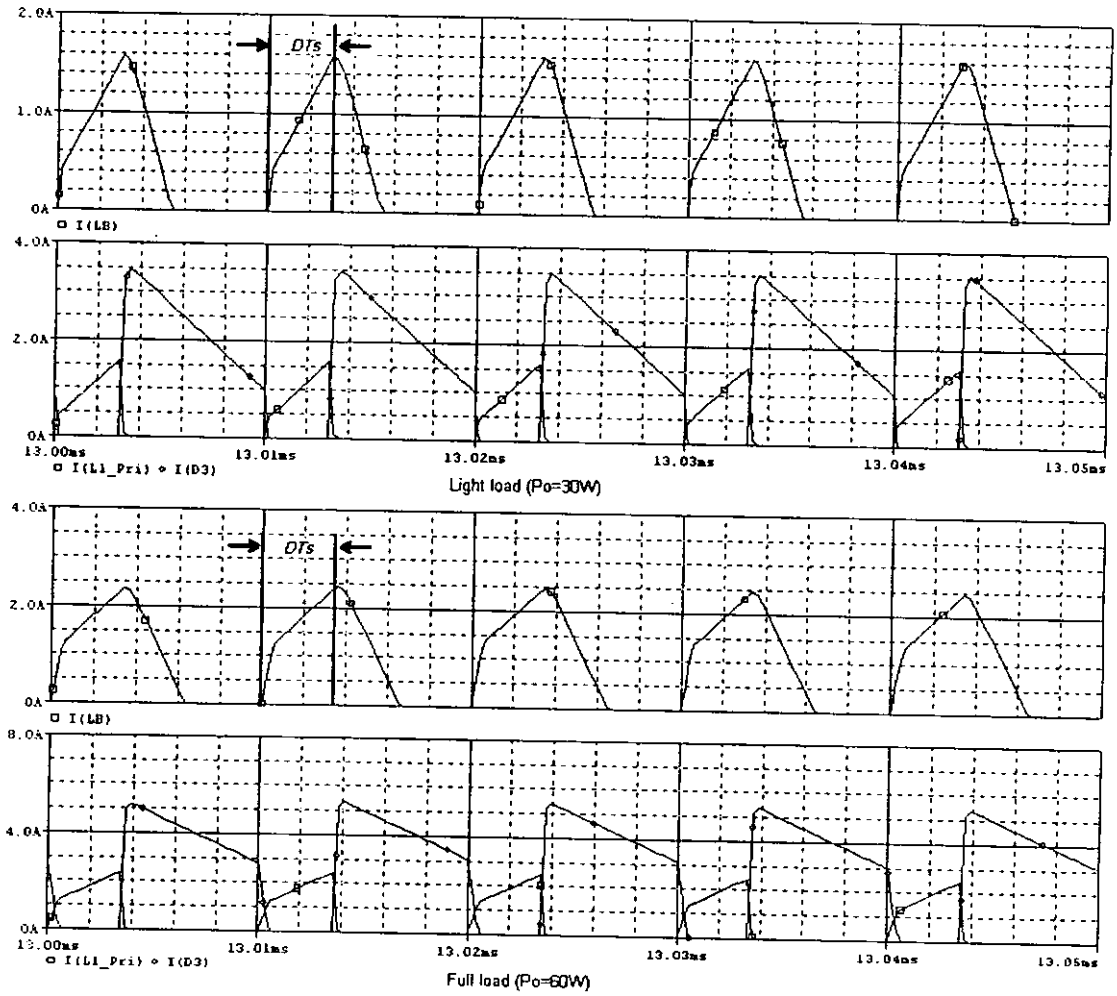


Figure 4.22: Simulation of the input current reduction in Mode 2 at (a) light load and (b) at full load in the steady state.

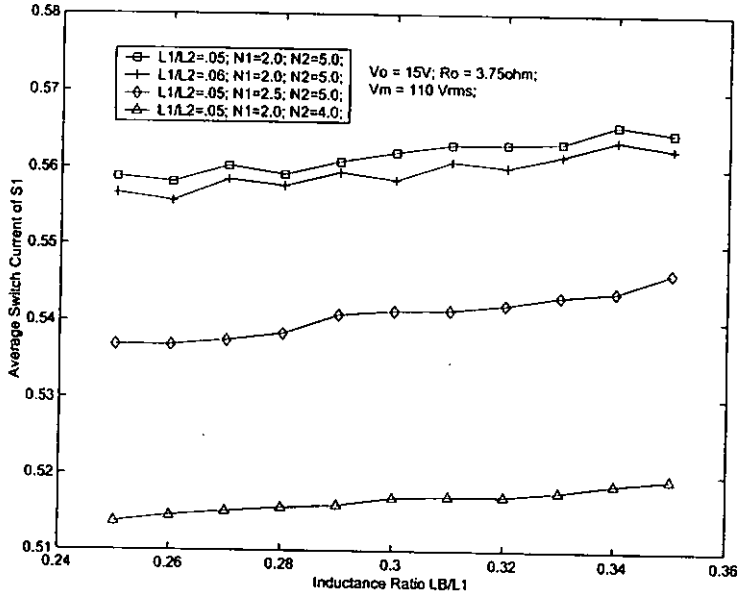


Figure 4.23: Estimated average switch current $\bar{i}_{S1}$ (averaged over half line cycle) for different values of inductance and turns ratios.

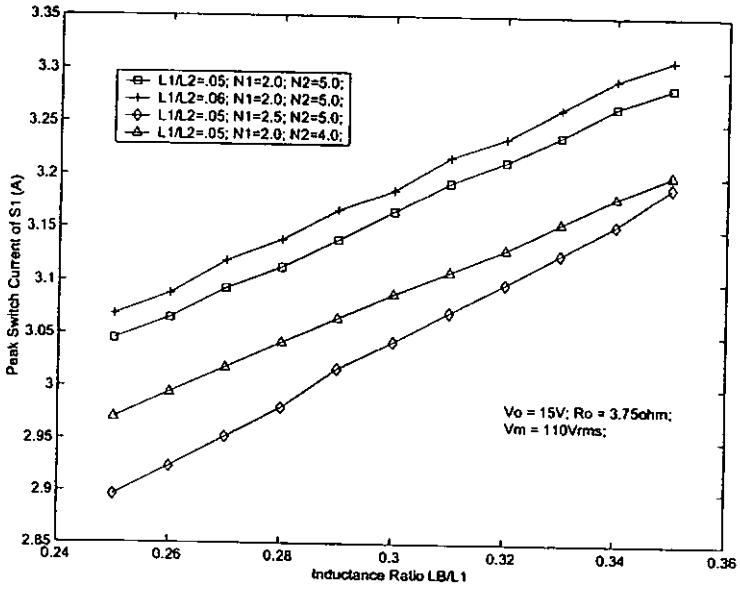


Figure 4.24: Estimated peak switch current $\hat{i}_{S1}$ (averaged over half line cycle) for different values of inductance and turns ratios.

	V_B	$\bar{i}_{S1}$	$\hat{i}_{S1}$
L_B/L_1 Decrease	Decrease	Decrease	Decrease
L_1/L_2 Increase	Decrease	Decrease	Increase
N_1 Increase	Decrease	Decrease	Decrease
N_2 Decrease	Decrease	Decrease	Decrease

Table 4.1: Comparison on current and voltage stresses for different values of inductance ratios and turns ratios.

made. Figure. 4.23 shows that the estimated $\bar{i}_{S1}$ using (4.48) over a half of line cycle. Consider the inductance ratios, it can be seen that the average switch current reduces when L_B/L_1 is decreased or L_1/L_2 is increased. For the turns ratios, the switch current reduces when N_1 is increased and N_2 is decreased.

Table 4.1 shows the comparison on current and voltage stress reduction for different values of inductance ratios and turns ratios. The average current on output diodes (D_3 and D_4) is not considered due to the fact that the average output current I_o will always equal the sum of diodes currents ($i_{D3} + i_{D4}$). From Table 5.1 it is interesting to notice that the decrease of voltage stress will bring about reduction of current stress, except for the slight increase of peak switch current $\hat{i}_{S1}$ when L_1/L_2 is increased. The reduction of current stress is due to the increase of output power handled by TR1, without being re-processed through the switch again. Despite the reduction of current and voltage stresses on the primary side (V_B and i_{S1}), the output diodes are expected to suffer from higher peak currents due to the increase of turns ratio and decrease of inductance.

4.11 Improvement of Input Current Distortion

This section studies the power factor correction capability of the proposed converter by investigating the linearity of the input current. Since the converter employs a boost converter (with boost inductor L_B) at the input stage, power factor correction is automatically achieved if L_B works in DCM and the duty ratio is roughly constant. In other words, the input stage of the converter will emulate a resistor (i.e. division of current to voltage results in a linear slope)

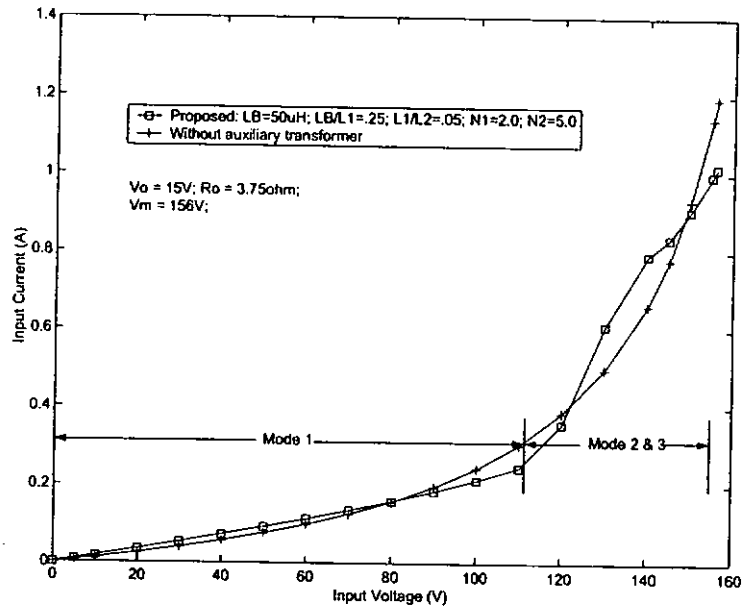


Figure 4.25: Comparison of linearity of input current between the S^2PFC converter with and without the auxiliary transformer under the same input-output condition.

if the above requirements are fulfilled. With the instantaneous average input current at Mode 1 and Mode 2/3 represented by (4.35) and (4.37) respectively, the input current is plotted against the input voltage, as shown in Figure. 4.25. To compare the performance of the proposed converter with the conventional S^2PFC converter without the auxiliary transformer, the input current of a single-switch boost-flyback S^2PFC converter under the same input-output condition is also shown in Figure. 4.25. It can be seen that in Mode 1, the input current of the proposed converter increases linearly when the input voltage increases (i.e. the input stage of the converter emulates a resistor). While for the one without the auxiliary transformer, the input current is much distorted due to the non-linearity of input current-voltage relationship. During the interval of Mode 2 and 3, the input current of the proposed converter is roughly linear but with different slope compared to Mode 1. For the conventional one, the input current keeps a parabolic relationship with the input voltage and shows a higher peak value at the peak input voltage. It can be concluded that the proposed converter can achieve lower input current distortion then the conventional one. Also, in order to improve the input current further, the duration of Mode 1 can be extended by increasing V_B as indicated in (4.42).

Component	Details
Inductor	$L_B = 50\mu$H
Transformers	TR1($L_1 = 200\mu$H; $N_1 = 2$)
	TR1($L_2 = 1m$H; $N_2 = 5$)
MOSFET	MTW14N50E (for S1) with C_{oss}=280pF
Diodes	MUR460 (for $D_B, D_1 - D_2$); MUR3040TP (for $D_3 - D_4$)
Capacitors	$C_B = 100\mu$F/400V; $C_o = 2 \times 1000\mu$F/25V

Table 4.2: Details of components used in 15V-60W proposed single-switch S^{2}PFC converter with CCM auxiliary transformer (Fig. 4.16).

The improvement in input current harmonics of the proposed circuit is due to the addition of TR1. When S1 turns on, L_B and L_1 charge up together in series. The effective charging inductance is $L_B + L_1$. After S1 turns off, L_1 is detached from the discharging path of L_B as the stored energy is coupled to output directly. The effective inductance when discharging becomes L_B which is much smaller then $L_B + L_1$ (as $L_B \ll L_1$). This reduces the discharging interval (d_3T_s), which is the main factor to reduce the input current distortion. Note that in (4.36) and (4.38), a $L_B/(L_B + L_1)$ term is added to reduce d_3 at both modes of operation.

4.12 Experimental Verifications

To verify the operation analysis and performance of the proposed single-switch S^{2}PFC, a hardware prototype with 110 V_{rms} AC input and 60W output (15Vdc/4A) working at 100kHz switching frequency is implemented. The details of the components used is tabulated in Table 4.2.

Figure. 4.26 shows the key switching waveforms of the proposed converter operating in Mode 2 in concert with the theoretical analysis. Figure. 4.27 confirms the analysis and simulation that the duty ratio of S1 remains unchanged during different loading conditions. The measured input voltage and current at full load are shown in Figure. 4.28. The input current contains no dead angle at the zero crossing region of input voltage. Figure 4.29 shows the output voltage

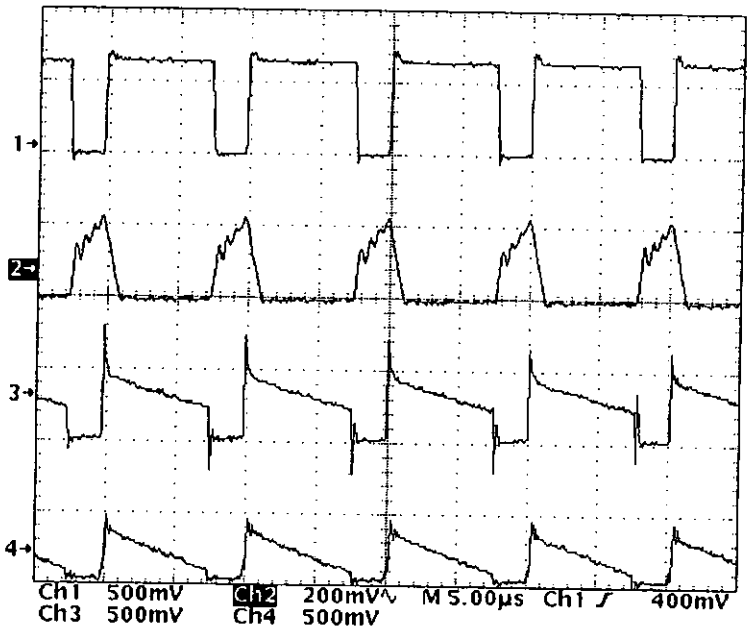


Figure 4.26: Experimental key switching waveforms of the proposed converter: drain-to-source voltage of S1 (CH1: 250V/div), i_{LB} (CH2: 2A/div), i_{D3} (CH3: 5A/div) and i_{D4} (CH4: 5A/div); time base (5μs/div).

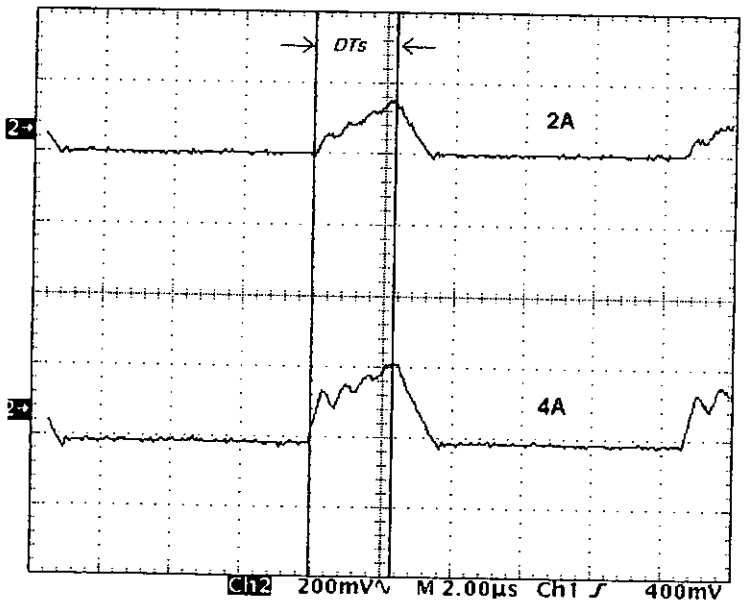


Figure 4.27: Measured inductor current at different loading conditions (2A and 4A), showing duty cycle (DT_s) remains roughly unchanged; time base (2μs/div).

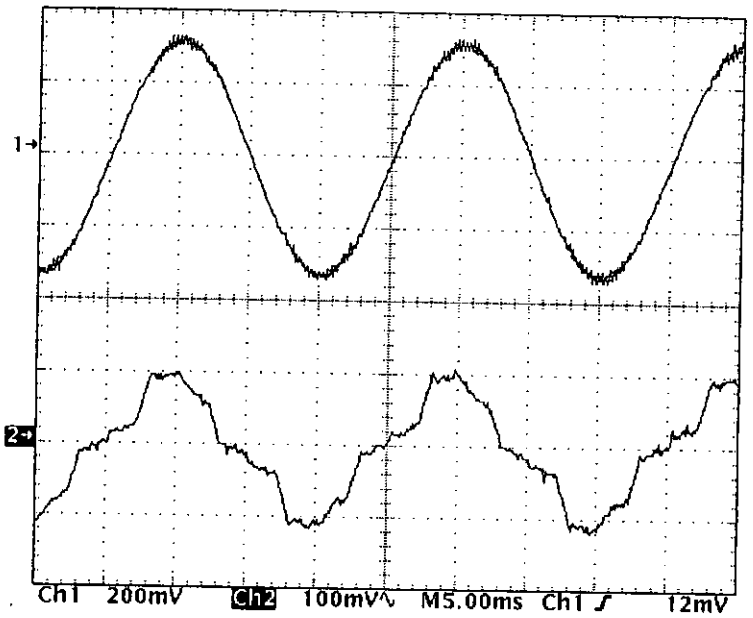


Figure 4.28: Measured line input voltage (CH1: 100V/div) and input current (CH2: 1A/div) at full load (15V/60W); time base (5ms/div).

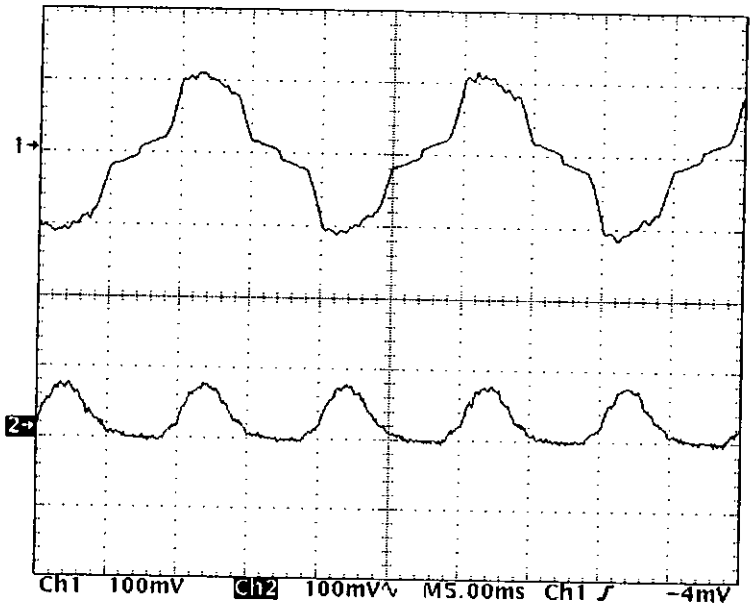


Figure 4.29: Measured line input current (CH1: 1A/div) and output voltage (CH2: 100mV/div) at full load (15V/60W); time base (5ms/div).

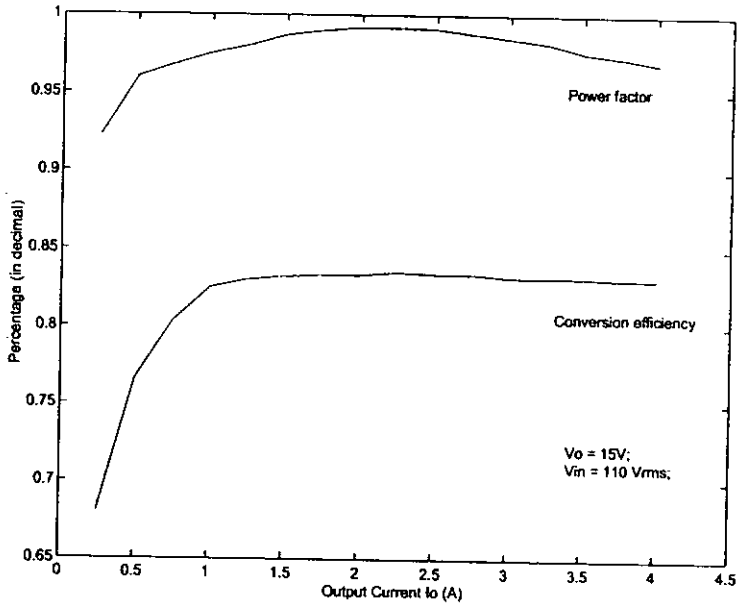


Figure 4.30: Measured power factor and conversion efficiency of the proposed converter.

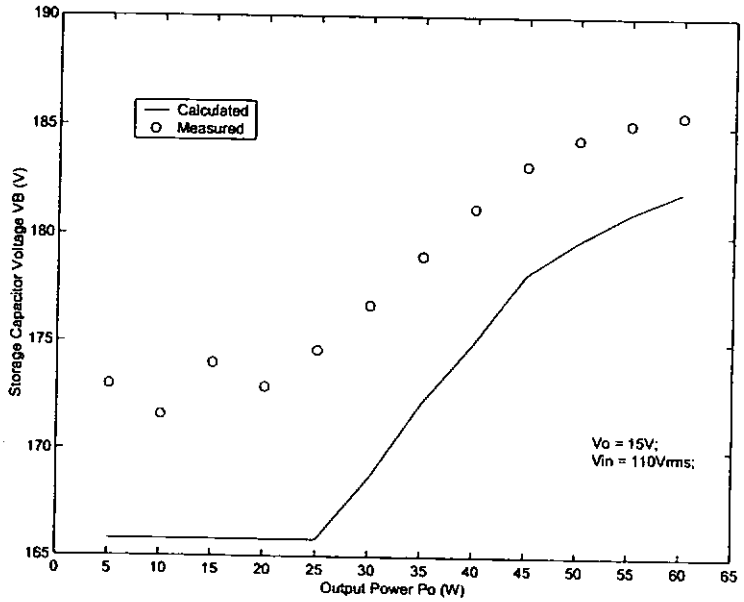


Figure 4.31: Measured and calculated storage capacitor voltage of the proposed converter.

I_o(A)	V_o (V)
0.5	15.14
1.0	15.08
1.5	15.05
2.0	15.03
2.5	15.01
3.0	15.00
3.5	15.00
4.0	14.94

Table 4.3: Load regulations of proposed converter at V_{in}=110Vrms.

ripple is about 80mV at full load condition. Figure. 4.30 shows both the measured power factor and conversion efficiency. It is shown that the power factor is above 0.97 and the conversion efficiency is around 83% at load current greater than 1A. Finally, in Figure. 4.31, it can be seen that the measured storage capacitor voltage V_B matches the trend of the calculation result. The storage capacitor voltage at light load is significantly reduced due to the input current control. The load regulation is within 1%, as shown in Table 4.3.

4.13 Discussion

In this section, the size and related cost of the proposed converter are compared with the conventional S^2PFC converter. Table 4.4 shows the brief comments on critical power components. From the table it can be seen that the size of transistor, inductor and storage capacitor are both reduced comparing to that of the conventional S^2PFC converter. This is due to the fact that part of the input power has been diverted to the output, these components handle less power. Less current and voltage stresses imply smaller size.

Although the proposed converter uses two transformers, they can be wound on the same core using integrated magnetics techniques. The core utilization is improved and size is reduced as a result. For the proposed converter, an additional diode is used due to the auxiliary output winding. However, the two

	Conventional S^2PFC	Proposed S^2PFC
Transistor	Larger	Smaller
Transformer	Single	Two shared
Inductor	Larger	Smaller
Diode	Two	Three
Storage Capacitor	Higher V & μF	Lower V & μF
Output Capacitor	Smaller	Slightly larger

Table 4.4: Comparison of component size between conventional and proposed S^2PFC converters.

flyback diodes share the total output power and so as the rated current of diodes. As both diode cathodes are connected to output, series diodes with common cathode in a package can be used. The size and cost will be pretty much the same as one with higher current. As a portion of input sinusoidal power will be coupled to output, a larger capacitor is necessary to attenuate the low frequency ripple. Since the proposed converter has higher conversion efficiency than that of the conventional ones, smaller heat sinks can be used. It is believed that the total size as well as the cost of the converter will be reduced.

4.14 Summary

It has been experimentally verified that after the insertion of an auxiliary transformer to the proposed DCM boost-flyback S^2PFC converter, the storage capacitor voltage and its range of voltage change when compared to the converter without the auxiliary transformer are reduced. The conversion efficiency is also improved as input power is processed less than twice. Expressions for the duty ratio, the storage capacitor voltage, the power factor and the percentage of output power handled by transformer are derived. It is found that these parameters are all controlled by the inductance ratio of the input inductor, the auxiliary and the flyback transformers. Optimal design criteria are then discussed in order to design a DCM S^2PFC converter at 15V-60W output with wide input voltage range. The results of the converter analysis have been confirmed by extensive experimental data.

Although the insertion of an auxiliary transformer operating in DCM to the input stage of the S^2PFC converter can reduce the level of storage capacitor voltage, this voltage still rises when load is reduced as a result from the imbalance between input and output powers. This chapter further presents an improved single-switch S^2PFC converter with an auxiliary transformer working mainly in CCM, which can control the input current and hence prevent excess charge being stored in the intermediate storage capacitor. The storage capacitor voltage decreases as load decreases, alleviating the high voltage stress at light load problem in the existing S^2PFC converter.

In addition to the reduction of voltage stress, the current stress of the power switch is also reduced. This is due to the fact that the auxiliary transformer, which directly couples a portion of input power to output after the first power process, reduces the input power to be re-processed by the switch again. High power factor is obtained due to the absence of dead angle of input current and smaller effective boost inductance during the discharge period. Experimental results show good agreement with the theoretical predictions.

Chapter 5

Storage Capacitor Voltage Control Using Output Voltage Feedback

5.1 Introduction

In Chapter 4, a S^2PFC converter based on the reduced repeated power processing approach have been developed to reduce the storage capacitor voltage stress. Nevertheless, the large storage capacitor voltage swing due to line voltage variation is still unresolved. The storage capacitor voltage also cannot fall below the peak input voltage due to the presence of boost converter, which steps up the storage capacitor voltage. The authors in [37] and [46] have made an attempt to reduce the storage capacitor voltage below the peak line voltage by using flyback-buckboost and flyback-boost converters respectively. But these converters require two switches, making them less attractive for low-power applications.

This chapter introduces a simple method to control the intermediate storage capacitor voltage of single-switch S^2PFC converter, while maintaining a high power factor. By employing a dual-output flyback converter in which one of the output ends is the regulated output voltage and the other is connected across the storage capacitor, the storage capacitor voltage swing due to line and load variations is narrowed. This voltage stress is also reduced, reaching below the

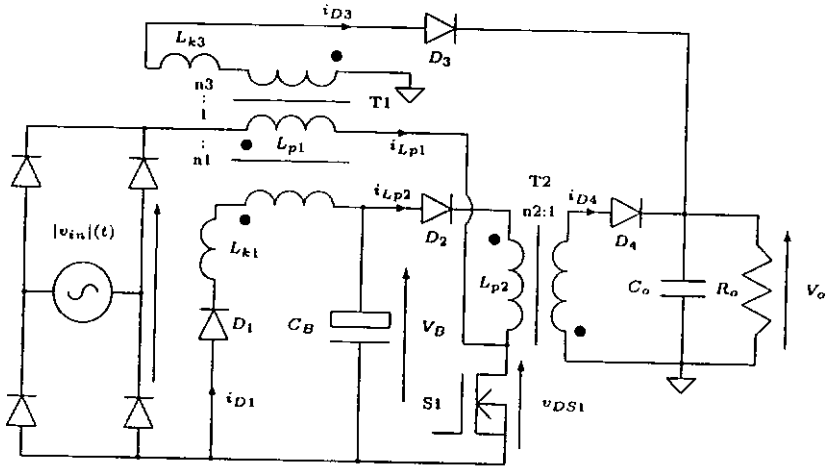


Figure 5.1: Proposed single-switch flyback power-factor-corrected AC/DC (S^2PFC) converter.

peak input voltage at high line.

5.2 Proposed Circuit and Its Operation

The proposed S^2PFC shown in Figure 5.1 is composed of two flyback converters sharing a single switch. A flyback converter with dual-output transformer T1 is connected to the line to shape the input current (works in discontinuous conduction mode (DCM) for inherent PFC function), to deliver energy to the intermediate storage capacitor C_B, to provide a direct power transfer path to output load and, most importantly, to control the voltage of C_B. C_B delivers power through another flyback converter with transformer T2, which operates in either DCM or CCM.

The basic operation of the flyback S^2PFC is depicted as follows. When the power switch S1 is turned on, L_{p1} and L_{p2} are charged up linearly by the rectified input voltage $|v_{in}|$ and the storage capacitor voltage V_B respectively. Diodes D_1, D_3 and D_4 are reverse biased and not conducting. The output capacitor C_o sustains the output voltage V_o. After period d_1T_s, as shown in Figure 5.3, S1 is turned off. Diode D_4 is forward biased and energy stored in T2 is coupled to the

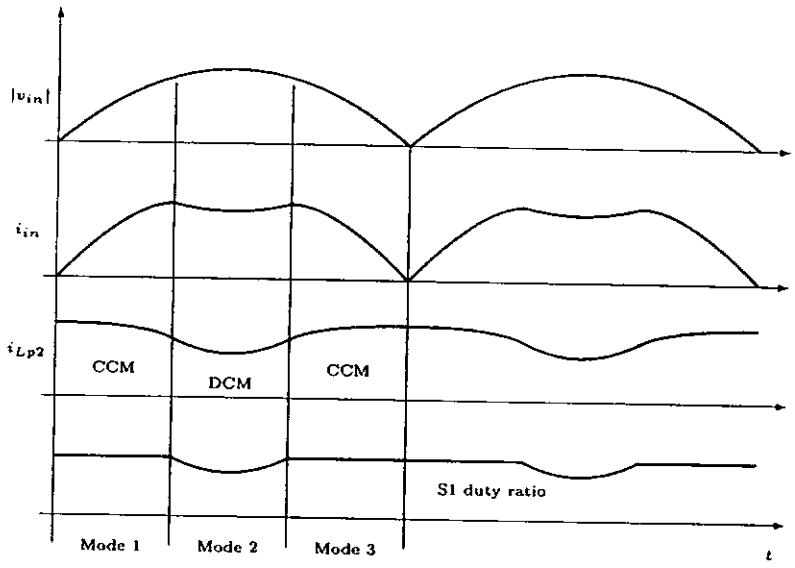


Figure 5.2: Operation analysis of the proposed flyback S^{2}PFC converter in a line cycle.

load. Meanwhile, the energy stored in T1 transfers to C_B and R_o through D_1 and D_3 respectively. Before S1 turns on again to begin the next switching cycle, all the energy stored in T1 is completely transferred to the load and C_B (i.e. i_{D1} and i_{D3} fall to zero). If T2 runs in CCM, V_o is maintained by the energy delivered from T2 through D4. If T2 operates in DCM, no current flows in T2 before the turn-on of S1. V_o is then sustained by C_o. To repeat the operation cycle, S1 is switched on again.

When $|v_{in}|$ is going through a half line cycle, the current of transformer T2 enters different conduction modes due to the varying output power from T1. In steady state, as shown in Figure 5.2, there are three modes of operation, which are described as follows:

Mode 1: During this mode, T2 runs in CCM. Since the input power is smaller than the output power, T2 handles most of the output power. The major portion of stored energy in T1 will be coupled to C_B through D_1. Since the duty ratio of S1 is constant within this interval, more input power as well as output power will be handled by T1 as input voltage increases. On one hand, this pushes T2 towards DCM as T1 provides more output current. On the other hand, the

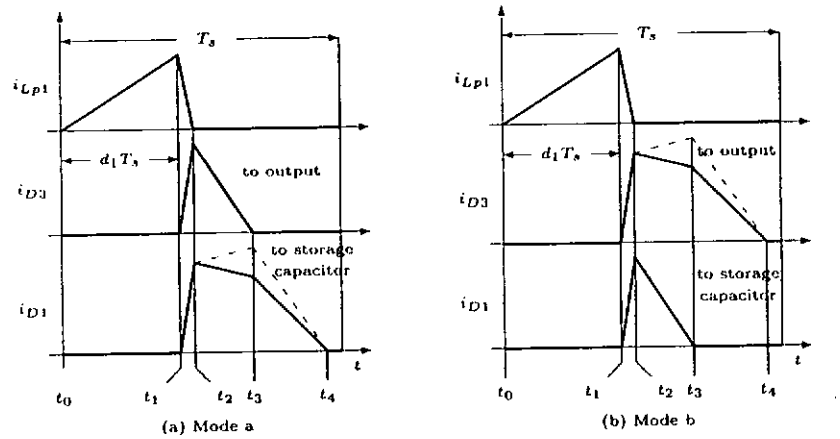


Figure 5.3: Key switching waveforms of T1 primary and secondary currents within a switching period T_s at different modes.

current in D_3 becomes larger.

Mode 2: In this mode, T2 runs in DCM. T1 handles most of the output power. When T2 runs in CCM, it automatically corrects the current difference in D_3 and D_4 by shifting the level of CCM. But when both transformers work in DCM, the duty ratio has to be decreased to maintain a constant output power, as the line voltage increases.

Mode 3: As input voltage reduces, T2 again handles the major part of output power as input power becomes smaller. The duty ratio remains constant as in Mode 1.

For an ideal transformer T1 where leakage inductance is absence, only the output with lower reflected output voltage (n_1V_B or n_3V_o) will receive energy from T1 primary. It is during turn-off of S1 and the rising v_{DS1}, which forward biases either D_1 or D_3 and clamps at the reflected voltage plus the input voltage $|v_{in}|$. In practice, the presence of unavoidable leakage inductances (L_{k1} and L_{k3}) in T1 will cause v_{DS1} to rise above both reflected output voltages and force D_1 and D_3 to turn on simultaneously. As a result, period $t_1 - t_2$ is introduced, as shown in Figure 5.3.

The peak current of i_{D1} and i_{D3} at t_2 is determined by i_{Lp1} which is a function

of $|v_{in}|$. Higher peak value of i_{Lp1} (due to higher $|v_{in}|$) will cause more current to flow through both i_{D1} and i_{D3}. T1 will then provide more output power but T2 will take less energy from C_B to output. Therefore, V_B will increase slightly but it is loosely regulated by short-circuiting it with the tightly regulated V_o, by means of T1. Moreover, V_B can only be loosely regulated (average value, not instant value) because it has to balance power between input and output. The differences between voltages $|v_{in}|$, V_B and V_o and the model of a "real" T1 determines current waveforms (Mode a or b in Figure 5.3), along the line cycle.

On one hand, when V_B is higher, current flowing through i_{D1} gets less because the reflected voltage on n_1 minus V_B is smaller to charge L_{k1} during $t_1 - t_2$. Since V_o is well-regulated, i_{D3} takes more current. The converter is then entered Mode b (in Figure 5.3). This phenomenon happens mostly at high line or when $|v_{in}|$ traverses to its peak value. On the other hand, at low line or at zero crossing region of $|v_{in}|$, the converter enters Mode a; i_{D1} has a trapezoidal waveform while i_{D3} has a triangular waveform.

Note that the rate of change of i_{D1} and i_{D3} at period $t_2 - t_3$, as shown in Figure 5.3, are given by

$$\frac{di_{D1}}{dt} = \frac{(L_{k3} + n_3^2 L_{p1}) \cdot V_B - n_1 n_3 L_{p1} \cdot V_o}{n_3^2 L_{k1} L_{p1} + L_{k3}(L_{k1} + n_1^2 L_{p1})} \tag{5.1}$$

$$\frac{di_{D3}}{dt} = \frac{(L_{k1} + n_1^2 L_{p1}) \cdot V_o - n_1 n_3 L_{p1} \cdot V_B}{n_3^2 L_{k1} L_{p1} + L_{k3}(L_{k1} + n_1^2 L_{p1})} \tag{5.2}$$

The upslope (thin dash line) or downslope (thick solid line) of i_{D1} and i_{D3} at period $t_2 - t_3$ is determined by the instantaneous value of V_B. Nevertheless, the slope within this period does not affect the operation mode (a or b).

It should be noted that V_o is free from low frequency components of the line voltage at both operation modes (DCM and CCM) of T2. When T2 runs in CCM, the duty ratio of S1 is constant due to the fast self-adjustment of transformer current. When T2 runs in DCM (Mode 2 in Figure 5.2), the transformer current adjustment disappears but the fast feedback loop of V_o gives a valley-shape duty ratio of S1 which maintains the output constant.

5.3 Analysis of Storage Capacitor Voltage

For perfect coupling of transformer (i.e. absence of leakage inductance), the storage capacitor voltage V_B is merely controlled by the turns ratio of transformer T1 as the output voltage V_o is tightly regulated and it is given by

$$V_B = \frac{n_1}{n_3} V_o \tag{5.3}$$

However, in practice, the wiring inductance and the leakage inductance of transformer degrade the cross regulation of converter. Equation (5.3) is no longer valid. By inspecting the current waveforms in Mode 1 and using input-output power balance between T1, T2 and V_o, the steady state expression of the storage capacitor voltage during this mode can be found.

$$V_B = \frac{n_1}{n_3} \frac{K_2 + \sqrt{K_2^2 - 4K_1K_3}}{2K_1} V_o \tag{5.4}$$

where

$$K_1 = \frac{1}{16}[16\pi n_3 M_1^2 k_c (2-k)^2/d_1^2 - 8n_1 M_1 (2-k)(3-2k) + \pi n_3 (1-k)(2-k)(3-k)] \tag{5.5}$$

$$K_2 = \frac{1}{16}[16\pi n_3 M_1^2 k_c (2-k)/d_1^2 - 8M_1 (3-k)^2 + \pi n_3 (1-k)(3-k)] \tag{5.6}$$

$$K_3 = \frac{1}{2}\left[2\pi n_3 M_1^2 k_c/d_1^2 - M_1 k\right] \tag{5.7}$$

M_1 is the ratio of output voltage to peak input voltage, k is the coupling coefficient of T1 and $k_c = L_{p1}/(R_o T_s)$. Equation (5.4) is valid provided that T2 operates in CCM throughout the entire line cycle. Otherwise, the equation of steady state V_B over a half line cycle will involve different modes of operation and complex calculation. However, from (5.4) it is enough for one to predict that V_B will be controlled not only by the turns ratio and V_o, but also by the peak input voltage. When the peak input voltage increases, V_B will also increase.

	v_{in}=90V$_{rms}$		v_{in}=140V$_{rms}$		v_{in}=240V$_{rms}$	
P_o(W)	PF	THD	PF	THD	PF	THD
10	0.867	57.5	0.768	83.4	0.501	153.8
30	0.932	38.9	0.830	67.2	0.660	113.8
50	0.983	18.7	0.906	46.7	0.717	97.2
70	0.997	7.8	0.932	38.9	0.770	82.9

Table 5.1: Measured power factor (PF) and total harmonic distortion (THD) at different line and load conditions.

$P_o(W)$	V_o at V_{in}=90V	V_o at V_{in}=240V
10	27.19V	27.49V
20	26.86V	27.30V
30	26.68V	27.14V
40	26.53V	27.11V
50	26.41V	26.98V
60	26.26V	26.84V
70	26.00V	26.72V

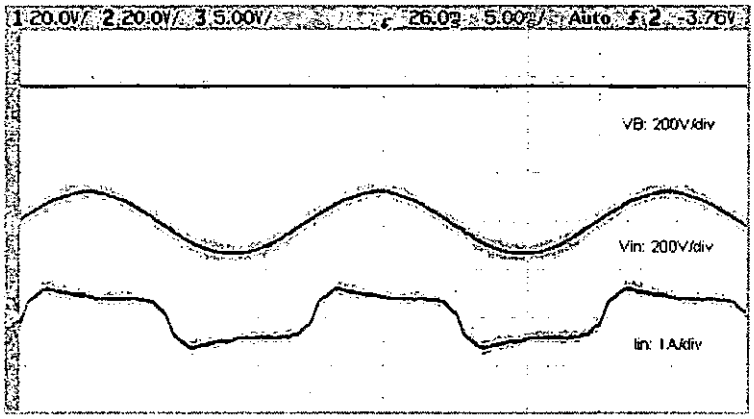
Table 5.2: Line and load regulations of proposed converter.

5.4 Analysis of Input Current

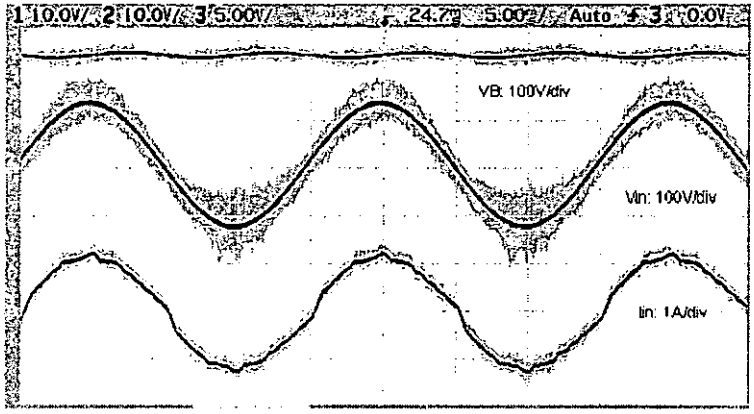
The average input current $\bar{i}_{in}$ of the proposed converter within one switching period equals the average primary current of T1 $\bar{i}_{Lp1}$ and is given by

$$\bar{i}_{in} = \frac{d_1^2 T_s}{2L_{p1}} |v_{in}(t)| \tag{5.8}$$

which resembles the input current of a normal flyback converter serving as a power factor correction circuit. Hence, the proposed flyback S^{2}PFC converter inherits unity power factor property provided that T2 is working in CCM throughout the line cycle so that the duty ratio d_1 can keep constant. It is observed from Figure 5.2 that T2 may enter DCM in Mode 2, resulting in distorted input current as the third current harmonic component increases (and higher odd harmonics but of smaller quantity). The longer the duration of Mode 2, the poorer the power factor will be. In fact when the output power becomes light, T2 has larger tendency to enter DCM.



(a) P_o=30W



(b) P_o=70W

Figure 5.4: Measured storage capacitor voltage V_B (upper), line input voltage (middle) and current (lower) at 90Vrms and different output power (time base=5ms/div).

5.5 Controller Design

The controller used for the proposed single-switch S^2PFC converter resembles commonly used voltage-mode PWM controller. The input current will be automatically shaped for high power factor provided with DCM operation of input inductor. The controller shall only montior and control the output voltage according to line and load variations. Commercial voltage-mode PWM controller ICs such as TL494 and TL5001A can be used.

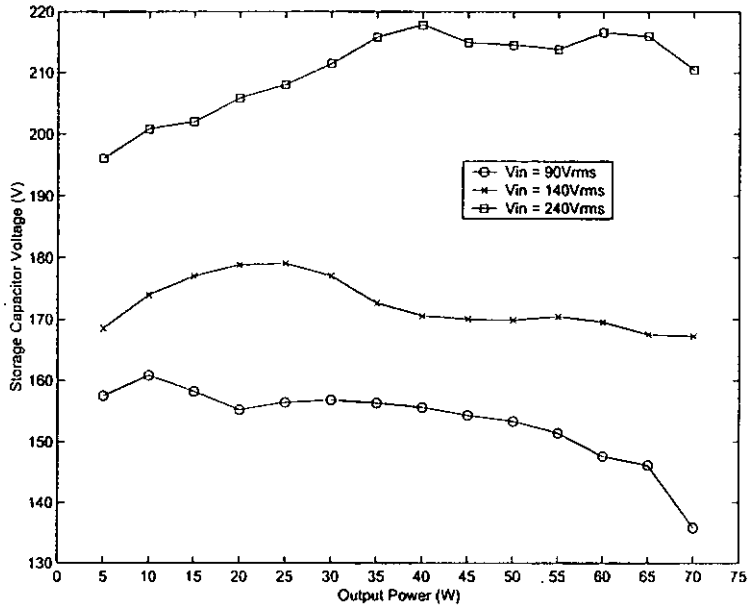


Figure 5.5: Measured storage capacitor voltage V_B versus output power at different v_{in}.

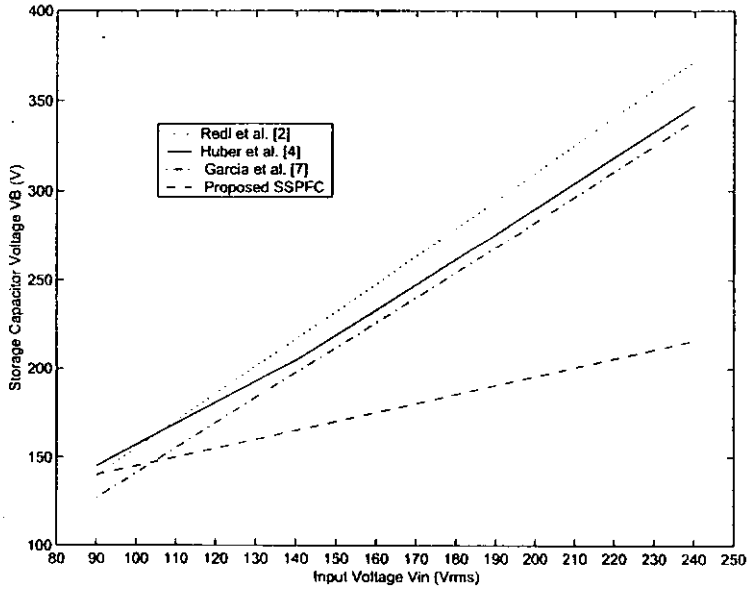


Figure 5.6: Comparison of V_B against v_{in} on different converter topologies.

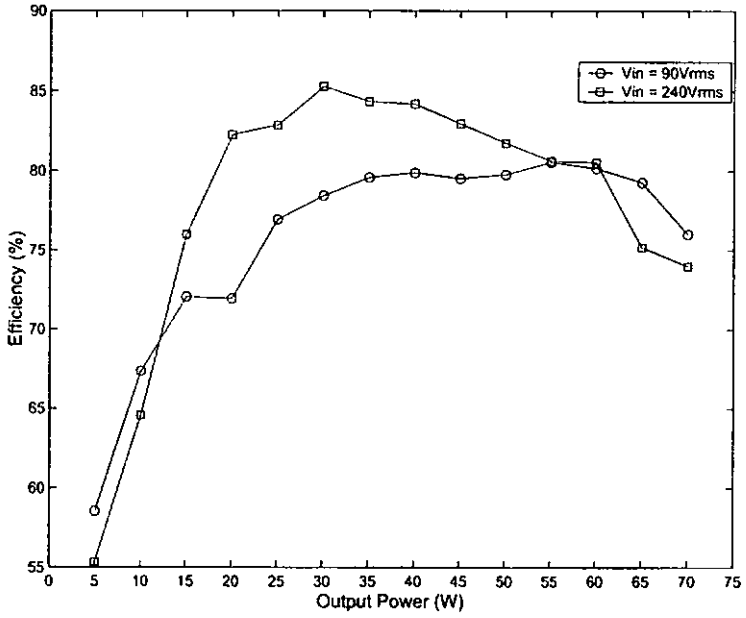


Figure 5.7: Measured efficiency against output power at different input line voltages.

5.6 Experimental Results

In order to verify the operation of the proposed S^2PFC converter shown in Figure 5.1, a 28Vdc-70W hardware prototype with input voltage range 90-240Vrms and 100kHz switching frequency has been implemented and tested. The control circuit employs a voltage-mode PWM controller IC TL494 for output voltage regulation. As only the output voltage is monitored, a voltage-mode PWM controller TL494 has been used for output voltage regulation. The circuit parameters used for the experiment are $L_{p1} = 70\mu$H, $n_1 = 0.31$, $n_3 = 1.54$; $L_{p2} = 900\mu$H, $n_2 = 3.3$; $C_B = 220\mu$F; $C_o = 1000\mu$F; S1: MTW14N50E, D_1: MUR4100E, D_2: MUR460, D_3 – D_4:MUR860. Figure 5.4 shows the waveforms of the storage capacitor voltage, the input line voltage and the line current at 90Vrms for light load (30W) and full load (70W). The measured power factor is 0.946 at 30W and 0.997 at 70W. Table 5.1 shows the performance of the SSPFC at different line and load conditions. It can be seen from Table 5.1 that when line voltage increases, the THD is also increased. This is because T2 runs in DCM at high line earlier than that at low line, resulting more distorted input current. But the THD reduces at increasing load, matching the prediction in Section 5.4. The storage capacitor

voltage V_B throughout the load range at different line voltages is recorded in Figure 5.5. In theory, V_B equals (1.54/0.31)*28=139V according to (5.3). In practice, due to the inevitable wiring and leakage inductances, V_B increases as input voltage increases, as predicted in (5.4). However, the increment of V_B of the proposed single-switch S^2PFC converter (around 50-75V for 90-240Vrms input) is much smaller than that of the existing single-stage topologies (at least 200V difference). It can also be seen that the variation of V_B is small even for large changes of output power (or load current). Furthermore, it is shown that V_B can be loosely regulated at a voltage lower than the peak input voltage at high line (240Vrms in this case), so that a smaller voltage-rating capacitor can be used (e.g. 250V). By comparing with existing converter topologies, Figure 5.6 shows that the proposed S^2PFC converter has the lowest V_B at high line voltage and the least V_B variation for a given change of line voltage. Figure 5.7 shows that the measured efficiency of the S^2PFC converter at different input voltages is around 80% at output power above 20W. The line and load regulations have been tabulated in Table 5.2, showing less than 4% steady-state error, which is acceptable for general AC/DC applications (e.g. battery chargers). Depending on the regulation requirement, this can be improved by using remote sensing and increasing copper area for power traces.

5.7 Discussion

As compared to conventional S^2PFC converters, the proposed converter adds one transformer and diode. However, the output power is shared by the main and auxiliary transformers, so as the added diode and main flyback diode. Therefore the size, hence the cost, of additional components will more or less the same as conventional ones. In addition, the power switch handles only part of input power due to the direct power transfer process. Furthermore, due to the improved conversion efficiency, smaller heat sinks for cooling can be used. All these bring down the size and total cost.

From Table 5.1, it is observed that the total harmonic distortion increases

with the line voltage. This is the result of direct power transfer from line input to output through T1. When the line voltage increases, the output power shared by T1 is increased. This forces T2 to run into DCM more earlier. The power switch duty cycle therefore appears in valley-shape to keep the output power constant. From the experiment the THD is out of IEC 1000-3-2 class-D specification, which requires THD roughly below 30%. To reduce THD, T2 should be designed to run more deeper in CCM. This can be achieved by increasing magnetizing inductance and storage capacitor voltage.

5.8 Summary

This chapter made an attempt to control the intermediate storage capacitor voltage of a single-switch single-stage power-factor-corrected (S^2PFC) AC/DC converter. The method is to use a dual-output flyback converter, where one output is connected to the tightly regulated output load and the other output is connected to the intermediate storage capacitor. Analysis and experimental results showed that the storage capacitor voltage can be loosely regulated. Due to the presence of wiring inductance and leakage inductance in the transformer, however, the storage capacitor voltage cannot be tightly regulated. The proposed converter achieved high power factor as the input stage is a DCM flyback converter and provided that the main transformer is operated in CCM.

Chapter 6

Direct Control of Storage Capacitor Voltage

6.1 Introduction

In previous chapters, we have introduced some circuits to reduce the high voltage stress on the storage capacitor in S^2PFC converters. Chapter 4 introduced a S^2PFC converter using an auxiliary transformer to reduce a fraction of this voltage throughout the entire line and load ranges. In Chapter 5, a flyback transformer with dual-output is used to loosely regulate the storage capacitor voltage through the output voltage feedback. Nevertheless, all the circuits proposed in Chapter 4 to 5 so far are using single-switch. Although single-switch S^2PFC converters are simple and easy to control, they do have some weaknesses.

Firstly, standby power feature is hardly achieved where the input power from line to the converter has to be cut off. Due to the sharing of power switch, single-switch S^2PFC converters draw input power from line and deliver power to load from storage capacitor simultaneously. Secondly, the storage capacitor voltage still suffers from significant variation according to the change of line. Once the power switch is used to control the output voltage, there is no room for regulation of storage capacitor voltage against line voltage. The converter proposed in Chapter 5 provides additional control dimension for single-switch S^2PFC converters, but the leakage inductance is an inevitable obstacle at present

to achieve tight storage capacitor voltage regulation.

In this chapter, a family of S^2PFC converters with an additional bi-directional switch is introduced. This switch is placed in series with the storage capacitor to 1) control the storage capacitor voltage; 2) assist tight regulation of output voltage; 3) provide direct power transfer feature; 4) provide standby power feature. To show the capability of the converters to reduce current and voltage stresses inherently, specific control of the storage capacitor voltage is first ignored in the analysis; only the output voltage is controlled. But the practical consideration of the control of storage capacitor voltage and simulation verification will be given afterwards.

6.2 Proposed Concept and Implementation

The conceptual diagram of the proposed S^2PFC converter with bi-directional switch is shown in Figure 6.1. With both uni-directional switches S_{in} and S_{out} opened, a portion of the input power, rP_1, from the rectified line input $|v_{in}|$ is processed by the DC/DC converter and transferred to output load directly. The rest of it, $(1-r)P_1$, will be diverted to the storage capacitor C_B through S_{in} for second power process (P_2), when the input power P_1 is smaller than output power P_o. Power from C_B to output load is processed by the same DC/DC converter when S_{out} is closed to maintain output power/voltage constant. Therefore S_{in} and S_{out} form a bi-directional switch to control the direction of power flow to and from C_B.

With this bi-directional switch, additional control dimension and reduction of switch current stress are provided for the converter. First, the storage capacitor voltage is regulated by controlling the amount of energy in and out of it against change of input voltage. That is, the control of time ratio of S_{in} and S_{out}. Second, direct power transfer feature is provided by turning off the bi-directional switch. Some input power will be processed by the DC/DC converter and diverted to output directly, so less input power will be processed twice through the power switch of the DC/DC converter. Moreover, the bi-directional switch prevents the

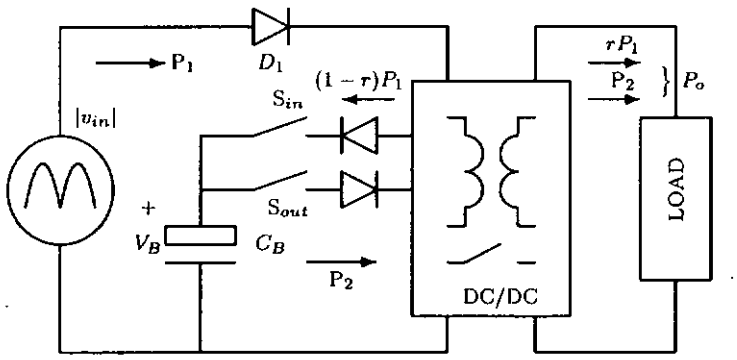


Figure 6.1: Conceptual diagram of the proposed S^2PFC converter with bi-directional switch.

simultaneous injection of currents from both input voltage and storage capacitor voltage sources, as it happens in single-switch S^2PFC converters. This also reduces the switch current stress, especially the peak current stress. Another advantage of using the control switch is to block the input power when standby mode is required by the electronic system which is connected to this power converter. Power is saved by disconnecting the line voltage source from the DC/DC converter. This feature is hardly achieved in all single-switch topologies.

The realisation of the proposed concept on a S^2PFC converter is shown in Figure 6.2. A power switch S2 and diode D_2 instead of two uni-directional switches are used to reduce the complexity of circuitry and control of the bi-directional switch. The DC/DC converter is a flyback type, which is composed of transformer T_1, power switch S1, output diode D_o and output capacitor C_o. A boost inductor L_1 working in DCM is added to achieve PFC function inherently and to deliver energy to the storage capacitor C_B. The converter supports standby mode operation by keeping S2 closed. As the storage capacitor voltage V_B is always higher than rectified line voltage $|v_{in}|$, the input current ceases to flow into the circuit due to the reverse bias of the input bridge-diode.

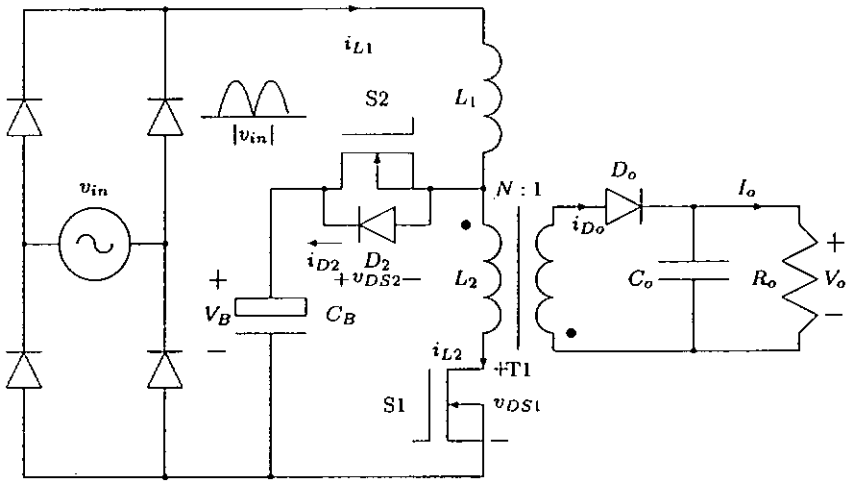


Figure 6.2: Realisation of the proposed S^{2}PFC converter using a boost-flyback topology.

6.3 Operating Principle and Control Strategy

6.3.1 Circuit Operation

To facilitate the steady-state analysis of the circuit in Figure 6.2, some assumptions are made (within each switching period). First, inductor L_1 works in DCM and transformer T2 operates in CCM. Second, capacitors C_B and C_o are large enough so that the low frequency ripples on V_B and V_o are negligible; V_B and V_o are essentially dc voltage sources. Third, the switching frequency $f_s(= 1/T_s)$ is much faster than the line frequency so that the rectified input voltage $|v_{in}|(= V_m|sin\omega t|$, where V_m is the peak input voltage and ω is the angular frequency of the input voltage) within a switching interval T_s is constant. Fourth, L_2 is the magnetizing inductance of T2. Finally, all circuit components have ideal characteristics except for the parasitic output capacitance of S2, C_{oss2}.

In the steady state, there are five stages of operation and their equivalent circuits are shown in Figure 6.3. The key switching waveforms are shown in Figure 6.4. The circuit operation is fully analyzed as follows:

Stage 1 $(t_0 - t_1)$ [Figure 6.3(a)]: Both the switches S1 and S2 are turned on.

The voltage applied across L_2 equals V_B. Since, at any instant, V_B is higher than $|v_{in}|$, the bridge diodes are reverse-biased and no current from the line input can flow into the circuit. As L_1 is operated in DCM and the energy in L_1 has already been discharged before the switches turn on, L_1 will not charge up. With the constant voltage V_B, L_2 is then charged up linearly at a rate given by

$$\frac{di_{L2}}{dt} = \frac{V_B}{L_2} \tag{6.1}$$

At the same time, a reverse voltage equals $(V_B/n+V_o)$ is applied across diode D_o. Therefore D_o is reverse-biased. During this time interval, the output capacitor C_o sustains the output voltage V_o. The stage ends when S2 is turned off.

Stage 2 $(t_1 - t_2)$ [Figure 6.3(b)]: At $t = t_1$, S2 is turned off and S1 is kept on. The parasitic output capacitance C_{oss2} of S2 is charged up and its voltage rises towards V_B+nV_o (assuming negligible forward bias voltage of D_o). Upon reaching V_B+nV_o, D_o is forward-biased and the voltage polarity across L_2 is reversed. The reflected voltage from output voltage V_o on L_2 is nV_o (non dotted-end of T2 is now positive) which adds up to $|v_{in}|$ to charge up L_1. i_{L1} rises linearly at a rate given by

$$\frac{di_{L1}}{dt} = \frac{|v_{in}| + nV_o}{L_1} \tag{6.2}$$

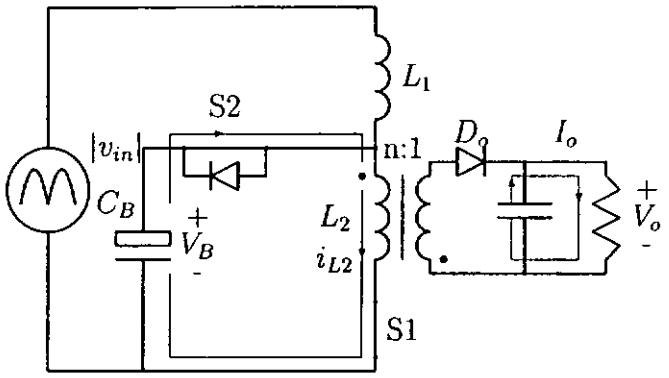
From (6.2), it can be seen that even when $|v_{in}| = 0$, input current can still flow into the circuit as L_1 ramps up according to the voltage nV_o applied across it. This will help obtain a better power factor, as being shown in [45], when the input current is not purely sinusoidal. The current in L_2 also ramps up with the same rate as that of L_1 because L_1 and L_2 are connected in series during this interval. In the meantime, as D_o conducts, some energy acquired in L_2 during Stage 1 is coupled to the load at a rate partly controlled by (6.2) and is given by

$$\frac{di_{Do}}{dt} = -\left[\frac{n^2V_o}{L_2} + \frac{n\left(|v_{in}| + nV_o\right)}{L_1}\right] \tag{6.3}$$

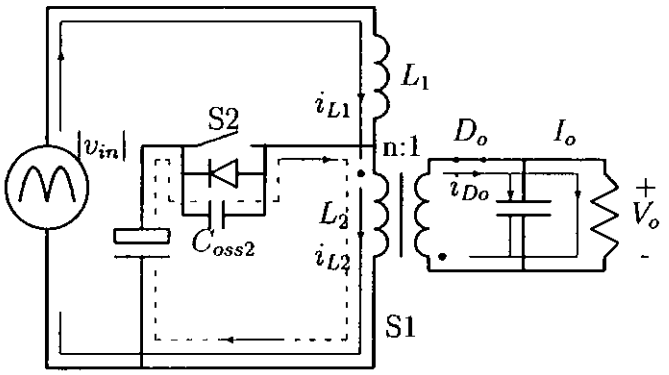
This interval ends when i_{Do} decreases to zero.

Stage 3 $(t_2 - t_3)$ [Figure 6.3(c)]: During this interval, S1 remains on. As i_{Do} has reached zero, a reverse voltage is applied across D_o with magnitude equals

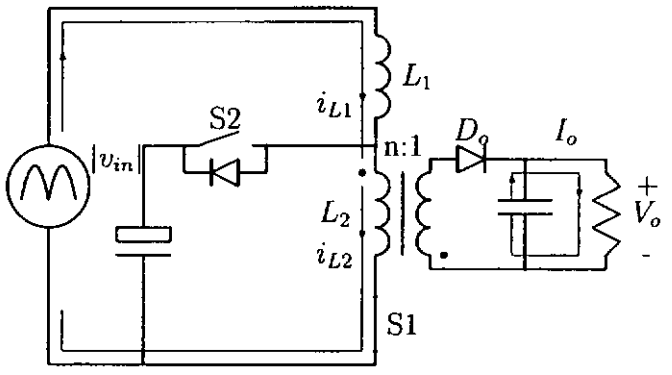
$$v_{Do} = \frac{L_2|v_{in}|}{n(L_1 + L_2)} + V_o \tag{6.4}$$



(a) Stage 1 ($t_0 - t_1$)



(b) Stage 2 ($t_1 - t_2$)



(c) Stage 3 ($t_2 - t_3$)

Figure 6.3: Five operation stages of the proposed converter during one switching period.

The voltage applied across L_1 and L_2 are $|v_{in}|L_1/(L_1+L_2)$ and $|v_{in}|L_2/(L_1+L_2)$ respectively and they continue to charge up at the same rate

$$\frac{di_{L1}}{dt} = \frac{di_{L2}}{dt} = \frac{|v_{in}|}{L_1+L_2} \tag{6.5}$$

During the period, only C_o provides power to the load. This stage ends when S1 is turned off. It should be noted that within this interval L_2 is charged up by $|v_{in}|$ in which the energy stored will be delivered to the load without re-process it. Namely, Stage 3 is the period for the converter to achieve direct power transfer function. Therefore the proposed converter has potentially higher efficiency than that of the cascaded design of AC-DC converters.

Stage 4 ($t_3 - t_4$) [Figure 6.3(d)]: At $t = t_3$, S1 is switched off. v_{DS1} rises towards nV_o shortly and D_o conducts. L_2 couples its stored energy to the output through T2 at the rate equals

$$\frac{di_{Do}}{dt} = \frac{-n^2V_o}{L_2} \tag{6.6}$$

At the same time, i_{L1} discharges C_{oss2} until it reaches zero, D_{S2} is then forward-biased. L_1 delivers its stored energy to C_B at the rate given by

$$\frac{di_{L1}}{dt} = \frac{-(V_B - |v_{in}|)}{L_1} \tag{6.7}$$

At the end of this interval, i_{L1} reaches zero and a reverse voltage $V_B - |v_{in}|$ is setting up on D_{S2}. It is noted that once there is input current flowing into the circuit, energy is stored in L_1. This stored energy is used to discharged C_{oss2} in order to achieve ZVS of S2 at turn-on period. As discussed in Stage 2 and from (6.2), energy is always stored in L_1 during period $t_1 - t_2$ even at the zero crossing region of input voltage. This implies ZVS turn-on of S2 is always available and is also independent of the line and load conditions.

Stage 5 ($t_4 - t_5$) [Figure 6.3(e)]: D_{S2} is reverse biased and stops conducting at $t = t_4$. The bridge diodes are also reverse-biased and input current i_{in} ceases flowing into the circuit. L_2 continues to deliver the rest of its energy to the output. At the end of this interval, S1 and S2 are turned on again to begin the next switching cycle.

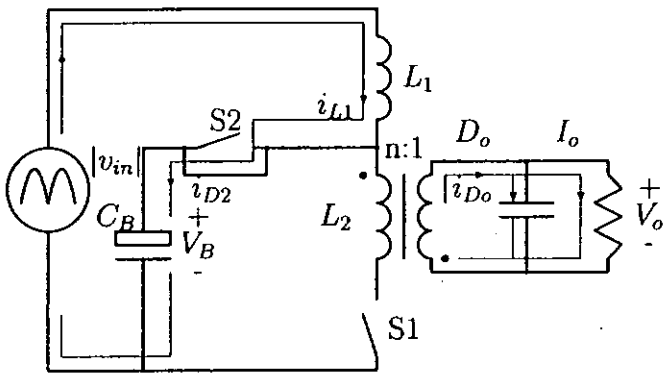
Realization of reduced repeated power processing by charging up L_1 and L_M in series not only improves conversion efficiency but also reduces switch current stress. As in the existing single-switch PFC converter topologies, [18]-[20] for examples, the peak inductor currents of L_1 and L_M happen at the end of each turn-on period of switch S1, as shown in Figure 6.5(a). The peak switch current is simply the sum of these peak inductor currents. However for the proposed S^2PFC converter, as shown in Figure 6.5(b), the peak inductor current of L_1 and L_M happen at separate turn-on periods of S1 (i.e. t_1 and t_3 respectively).

Consider the current through the power switches during the operation modes, it can be shown that at a time the current flowing through S1 comes from one source only, either $|v_{in}|$ or V_B. For the single-switch S^2PFC converters as in [18]-[20], however, the circuits were constructed so that when the switch is turned on, both the currents from V_B and $|v_{in}|$ are injected into the switch. For the two-switch S^2PFC converter in [19], the bottom switch also suffers the same high current stress as that of the single-switch S^2PFC because currents are injected from V_B and $|v_{in}|$ simultaneously. For proposed converter, S2 only turns on for part of the turn-on period of S1. Depending on the control factor K, smaller K will result in lower current stress of S2. With the decreasing current stress on the switches, the conduction loss and switching loss of the proposed converter will be decreased.

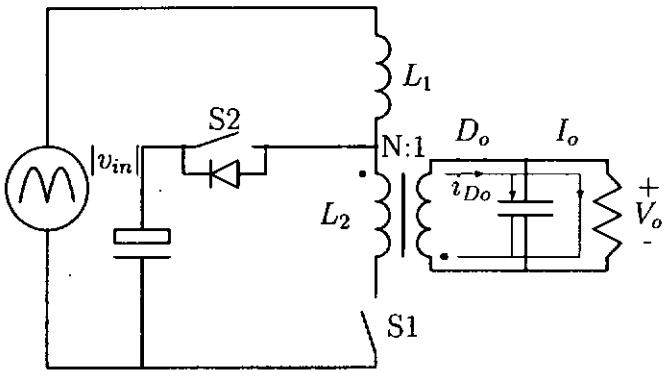
6.3.2 Control Strategy

The main objective of the control system is to find a simple and effective way to control the two switches S1 and S2 so that PFC is achieved and the output voltage V_o is regulated as line and load vary. Since L_1 is operated in DCM throughout the line cycle, PFC is achieved automatically if the duty cycles of S1 and S2 are roughly constant because L_1 functions as a boost inductor. Therefore, the two duty cycles of S1 and S2 will be dependent on the changes of output only.

From the circuit operation discussed previously, L_2 is powered by two sources, $|v_{in}|$ and V_B, and with S1 and S2 to control these two sources. The energy stored



(d) Stage 4 ($t_3 - t_4$)



(e) Stage 5 ($t_4 - t_5$)

Figure 6.3: Five operation stages of the proposed converter during one switching period.

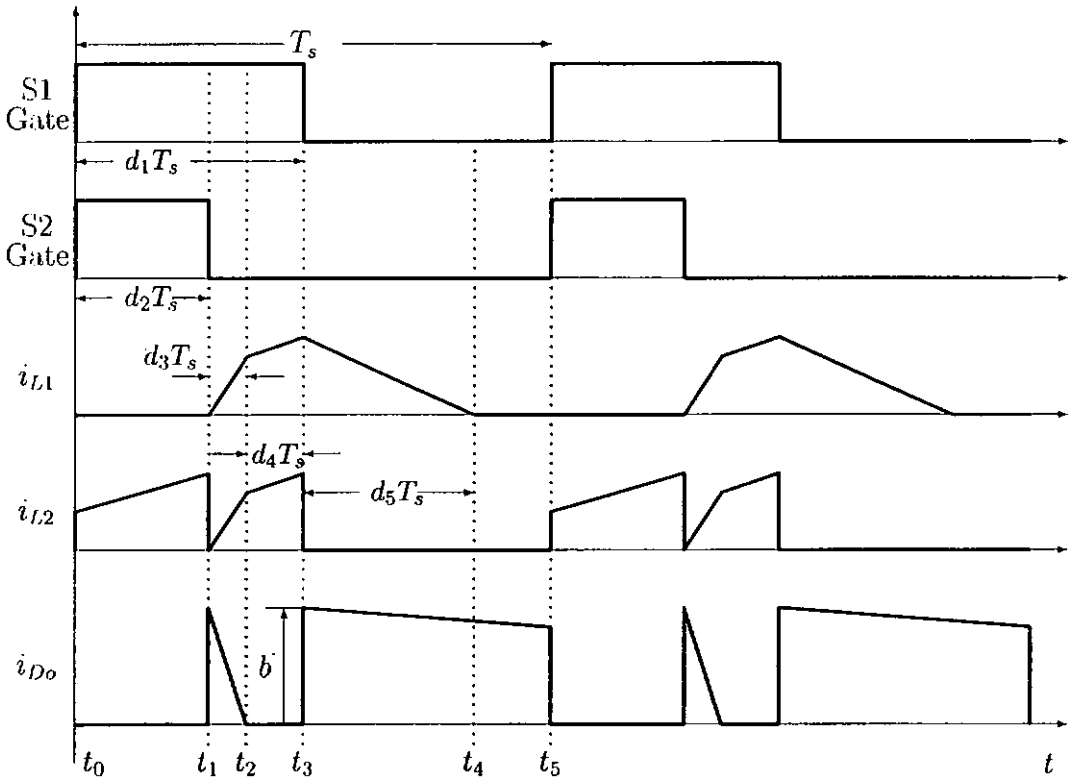


Figure 6.4: Key theoretical waveforms within several switching periods.

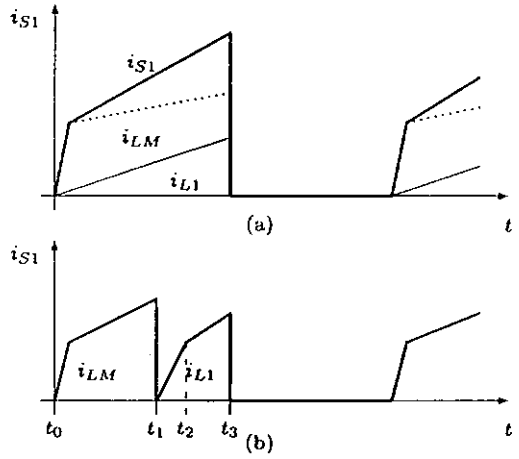


Figure 6.5: Comparison of switch current of the (a) existing single-switch PFC topologies and (b) proposed S^2PFC converter.

in L_2 will be diverted to power the load after the switches turn off. Although there is a short instant, as shown in Figure 6.4, that L_2 will couple some energy to the output when S2 is off and S1 remains on, L_2 is mainly working in CCM. With CCM operation of the flyback transformer T2, the duty cycles of S1 and S2 are almost constant. It is because the discharging slope of T2 secondary side, as indicated in (6.6), will be adjusted as V_o varies. To explain this further, we take an example when $|v_{in}|$ increases or the load resistance R_o increases. In both cases, V_o will be increased if the duty cycles of S1 and S2 do not change instantaneously. With V_o increased, the discharging rate of D_o will be increased as indicated in (6.6). Then when the next switching cycle S1 and S2 turn on again, the initial charging current reflected on L_2 will be lowered comparing to the previous switching cycle. Since the feedback control network is designed to have a cutoff frequency well below the switching frequency f_s (usually less than a quarter of f_s) for system stability reason, the duty cycles cannot response so fast that they will remain unchanged. So the instantaneous input power in T2 during this switching cycle will be smaller and so as the output power. V_o will then be fallen into the regulation range again.

Now, a control constant K is introduced such that

$$K = \frac{d_2}{d_1} = \frac{d_2}{d_2 + d_3 + d_4} \tag{6.8}$$

where the numerator and the denominator of the above equation are the duty cycles of S2 and S1 respectively. This control constant K links up the duty cycles and allows them to vary in a synchronized manner as the line and load vary. This makes a single voltage feedback control loop possible. Figure 6.6 shows the basic schematic of the proposed feedback control for the converter. The output voltage is sensed by the inverting input of the error amplifier E/A with compensation network, and an error control voltage v_c is generated. v_c is shared by two PWM comparators to produce desired duty cycles for S1 and S2. For the upper comparator, v_c is compared with a sawtooth-waveform at a fixed frequency f_s with a peak amplitude V_T so that the duty cycle of S1, d_1, can be expressed by

$$d_1 = \frac{v_c(t)}{V_T} \tag{6.9}$$

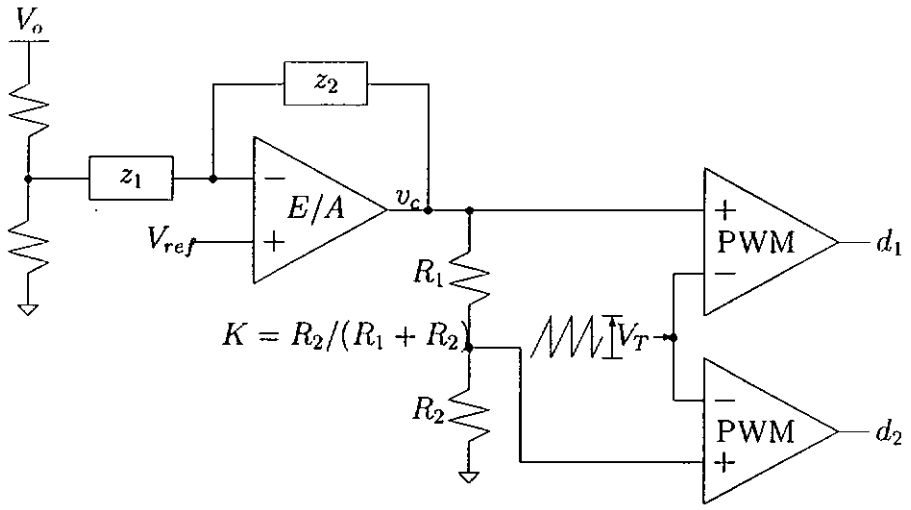


Figure 6.6: Configuration of the adopted PWM control.

For the lower comparator, v_c is reduced to a level set by the values of R_1 and R_2. The duty cycle of S2, d_2, is then given by

$$d_2 = \frac{R_2}{R_1 + R_2} \frac{v_c(t)}{V_T} \tag{6.10}$$

Figure 6.7 illustrates the generation of duty cycles for the switches. From (6.8), (6.9) and (6.10) we can relate the theoretical value of K to the practical circuit

$$K = \frac{R_2}{R_1 + R_2} \tag{6.11}$$

6.4 Steady State Analysis

In this section, steady state analysis will be carried out to derive the relationship between the ratio of storage capacitor voltage to peak input voltage, M_2, and the circuit parameters such as control parameter K, turns ratio n and inductance ratio L_1/L_2. With these circuit parameters, the equations related to input current harmonics will also be formed. For the purpose of this analysis and design, the duty ratio expression of S1 will be obtained first.

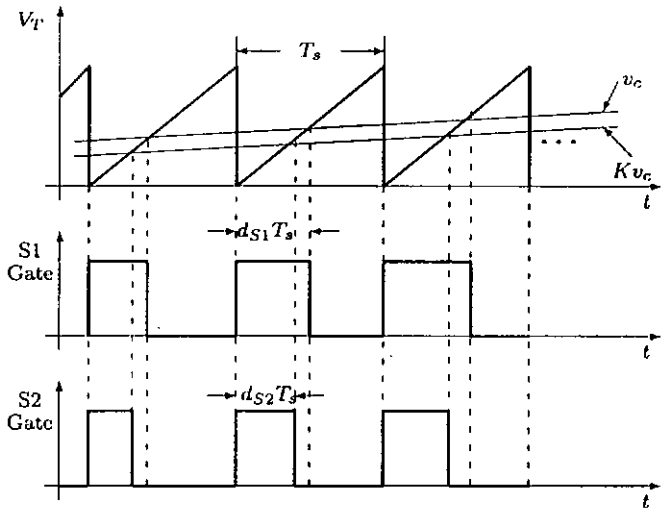


Figure 6.7: Illustration of generation of duty cycles for the switches.

6.4.1 Duty Ratio of Power Switches

Consider the voltage-second balance on L_2, the duty ratio d_4 can be expressed by

$$d_4 = \frac{\alpha + 1}{V_m|sin\omega t|}\left[nV_o d_3 - (KV_B + nV_o)d_1 + nV_o\right] \tag{6.12}$$

where

$$\alpha = \frac{L_1}{L_2} \tag{6.13}$$

From (6.8), d_4 can also be given by

$$d_4 = (1 - K)d_1 - d_3 \tag{6.14}$$

Equating (6.12) and (6.14), we obtain

$$d_3 = \frac{d_1[(1 - K)|sin\omega t| + (\alpha + 1)(nM_1 + KM_2)] - n(\alpha + 1)M_1}{|sin\omega t| + n(\alpha + 1)M_1} \tag{6.15}$$

where

$$M_1 = \frac{V_o}{V_m} \tag{6.16}$$

$$M_2 = \frac{V_B}{V_m} \tag{6.17}$$

For each switching period T_s, the average output current is found by adding up the average diode current i_{Do} at periods d_3T_s and $(1 - d_1)T_s$

$$I_o = \frac{V_o}{R_o} = \frac{n}{2}\left[\frac{nV_o}{L_2} + \frac{V_m|sin\omega t| + nV_o}{L_1}\right] d_3^2T_s + b(1-d_1) - \frac{n^2V_o}{2L_2}(1-d_1)^2T_s \tag{6.18}$$

Assume L_2 is large enough (because L_2 works in CCM) so that the peak current of D_o at t_3 (=b) can be approximately equal to that at t_1.

$$b = n\left[\frac{nV_o}{L_2} + \frac{V_m|sin\omega t| + nV_o}{L_1}\right] d_3 T_s \tag{6.19}$$

Substituting (6.15) and (6.19) into (6.18) and assuming $d_3 \ll 2(1-d_1)$, we have

$$d_1 = \frac{k_1 + 2k_2 - \sqrt{k_1^2 - 4(k_1+k_2)k_3}}{2(k_1+k_2)} \tag{6.20}$$

where

$$k_1 = (1-K)|sin\omega t| + (\alpha+1)KM_2 \tag{6.21}$$

$$k_2 = nM_1\left(1 + \frac{3\alpha}{2}\right) \tag{6.22}$$

$$k_3 = \frac{L_1}{nR_oT_s}M_1 \tag{6.23}$$

For the S^2PFC converter with CCM operation of the DC-DC regulator [22] - [23], which have a duty ratio depending on output voltage only, the duty ratio remains unchanged even the load becomes light. But for the proposed converter, it can be seen from (6.20) and (6.23) that duty ratio d_1 is a function of loading resistance R_o. In other words, the duty ratios of the switches carry the load information. When the load is reduced (i.e. R_o is increased), duty ratio d_1 (d_2 as well since $d_2 = Kd_1$) is also reduced. Therefore less energy will be stored in L_1 to feed C_B after both switches are turned off, reducing the storage capacitor voltage stress on light load. This will be verified by experiment in Chapter 8.6.

It is observed from the operation principle of the converter that, during stages 2 to 3 the current through L_2, which has the line ripple component, will be transferred to output. However, from (6.20) and (6.21) we can see that d_1 is also a function of line voltage and will respond to $|sin\omega t|$ to keep V_o free from line ripple component. In addition, the compensation network is designed to have cutoff frequency well above the line ripple frequency so that the output voltage will keep tightly regulated.

6.4.2 Storage Capacitor Voltage to Peak Input Voltage M_2

The energy stored in L_1 will be released to C_B during the off-state period of S1. The average charging current of C_B, which is the average discharging current of L_1, during this period (i.e. d_5T_s) is given by

$$i_{charge} = \frac{V_B - V_m|sin\omega t|}{2L_1} d_5^2 T_s \tag{6.24}$$

And d_5 can be found from the voltage-second balance of L_1, which is given by

$$d_5 = \frac{(V_m|sin\omega t| + nV_o)d_3 + V_m|sin\omega t|\frac{\alpha}{\alpha+1}d_4}{V_B - V_m|sin\omega t|} \tag{6.25}$$

When S1 and S2 are closed, the energy stored in C_B will be discharged to L_2. The average discharging current of C_B, which equals the average charging current of L_2, during this interval (i.e. d_2T_s) is then

$$i_{discharge} = \left[\frac{nV_o}{L_2} + \frac{V_m|sin\omega t| + nV_o}{L_1}\right] d_2 d_3 T_s - \frac{V_B}{2L_2} d_2^2 T_s \tag{6.26}$$

In steady state, the averaged capacitor current over a half line cycle should be zero, therefore

$$\frac{\omega}{\pi}\int_0^{\frac{\pi}{\omega}} i_{charge} dt - \frac{\omega}{\pi}\int_0^{\frac{\pi}{\omega}} i_{discharge} dt = 0 \tag{6.27}$$

Substituting (6.14), (6.15), (6.20), (6.24) and (6.26) into (6.27) and replacing ωt by θ, a transcendental expression of M_2 is found.

$$M_2 = \frac{V_B}{V_m} = \frac{F_1 - F_2}{F_3} \tag{6.28}$$

where

$$F_1 = 2K\int_0^{\pi} d_1\left[d_1(k_1 + n(\alpha+1)M_1) - n(\alpha+1)M_1\right] d\theta \tag{6.29}$$

$$F_2 = \frac{1}{(\alpha+1)^2}\int_0^{\pi} \frac{\{d_1[(1-K)|sin\theta| + kM_2 + nM_1] - nM_1\}^2}{M_2 - |sin\theta|} d\theta \tag{6.30}$$

$$F_3 = \alpha K^2 \int_0^{\pi} d_1^2 d\theta \tag{6.31}$$

Note that M_2 cannot be solved analytically. However, based on specified circuit parameters, (6.28) can be solved by numerical method.

6.4.3 Input Current Harmonics

The average instantaneous input current, which is also inductor L_1 current, is given by

$$i_{in,ave} = i_{L1,ave}$$

$$= \frac{V_m T_s}{2L_1}\left[d_4^2\frac{\alpha}{\alpha+1}|sin\omega t| + d_3(d_3+2d_4)(|sin\omega t| + nM_1) + d_5^2(M_2 - |sin\omega t|)\right] \tag{6.32}$$

The line input current i_{in} consists of mainly odd harmonics which can be calculated using Fourier analysis. Substitution of $\theta = \omega t$, the Fourier series of i_{in} is then expressed as

$$i_{in} = \sum_1^k b_k sink\theta \tag{6.33}$$

where

$$b_k = \frac{2}{\pi}\int_0^\pi i_{in,ave}(\theta)sink\theta d\theta, \qquad k = 1,3,5,...,(2N+1) \tag{6.34}$$

The value of N is chosen when b_k in the series is negligible. The total harmonic distortion (THD) and power factor (PF) are obtained using the following equations:

$$THD = \frac{\sqrt{\sum_3^k b_k^2}}{b_1} \tag{6.35}$$

$$PF = \frac{b_1}{\sqrt{\sum_1^k b_k^2}} \tag{6.36}$$

6.5 Design Considerations

The derived model equations will be used in this section for the design of an experimental 100kHz 60W/20Vdc converter prototype with line input voltage at 90 - $110V_{rms}$. The main design goal is to obtain a set of circuit parameter values so that low storage voltage stress, high percentage of direct power transfer, high power factor and low input current harmonics are achieved.

According to the storage capacitor voltage V_B, which is determined by (6.20)-(6.23) and (6.28), the design variables are inductance L_1, switching period T_s, loading resistance R_o, inductance ratio α, turns ratio n and control constant K.

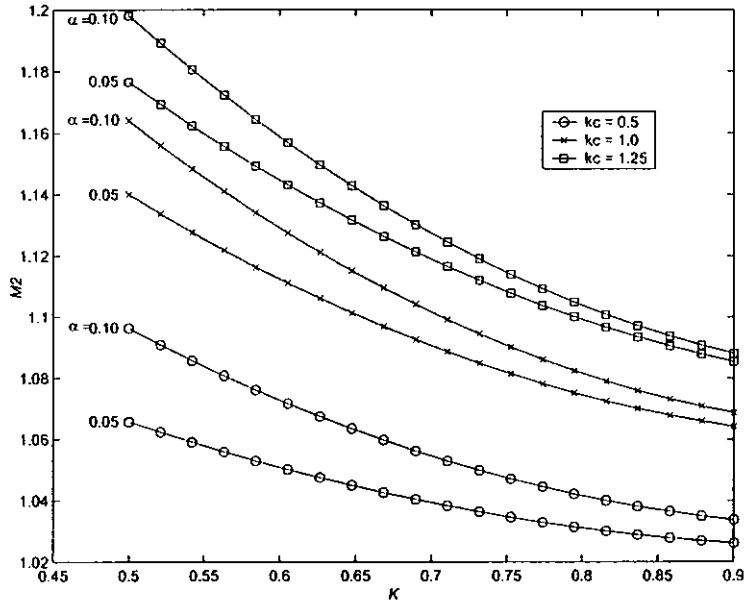


Figure 6.8: Calculated M_2 versus K for different values of k_c at V_m=127V and n=2.

To simplify the design, a coefficient k_c relating the circuit parameters is first defined

$$k_c = \frac{L_1}{R_o T_s} \tag{6.37}$$

The storage capacitor voltage stress V_B (indicated as M_2) is directly proportional to k_c as shown in Figure 6.8 at low line voltage $V_m = 90V_{rms}$ and n=2. However, lower value of k_c increases the selection range of K at the expense of increasing the current stress on the diodes and switches at the primary side (because L_1 gets smaller for lower k_c value). It follows from Figure 6.8 that $k_c = 1$ is set for full load condition.

Figure 6.9 shows the relationship between M_2 and K with $k_c = 1$ for different values of turns ratio n and inductance ratio α at $V_m = 90\sqrt{2} = 127$V. It can be seen that, for a given value of K, M_2 decreases with decreasing value of α or increasing value of n. When α is decreased, the portion of energy stored in L_1 to supply C_B will be decreased as L_1 is charged up in series with L_2 during period $d_4 T_s$. And if n is increased, the reflected output current to the primary side of T2 ($i_{L2} = i_{Do}/n$) during the turn-on instant of S1 and S2 will be reduced. The duty ratios of S1 and S2 will be increased and more charge will be taken away from C_B, resulting in a lower level of V_B. Moreover, for a given value of α, M_2

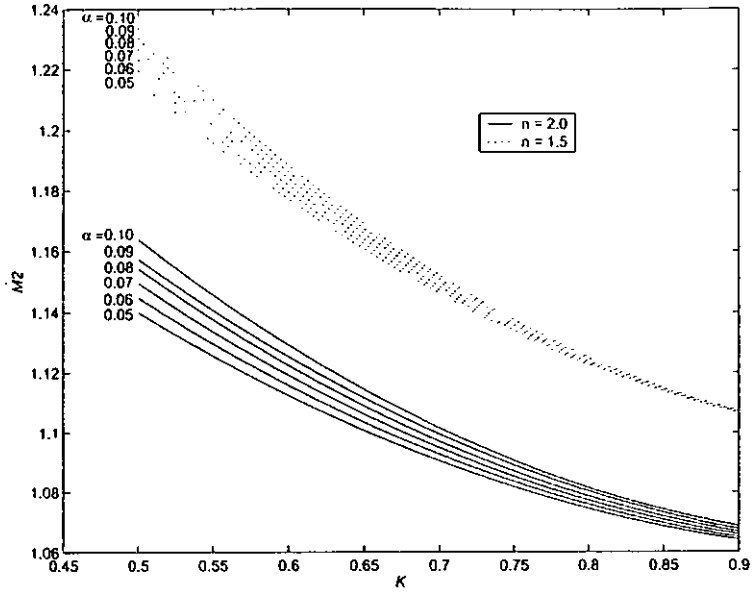


Figure 6.9: Calculated M_2 against K with $k_c = 1$ for different values of turns ratio n and inductance ratio α at V_m=127V.

K	n	α	M_2	THD	PF
0.5	1.5	0.08	1.2238	9.57	0.9954
0.5	1.5	0.10	1.2344	9.22	0.9958
0.9	1.5	0.08	1.1060	57.77	0.8659
0.9	1.5	0.10	1.1064	54.07	0.8796
0.5	2.0	0.08	1.1549	18.62	0.9831
0.5	2.0	0.10	1.1646	17.89	0.9844
0.9	2.0	0.08	1.0663	56.43	0.8709
0.9	2.0	0.10	1.0681	56.02	0.8724

Table 6.1: THD and PF versus K, n, α and M_2 at V_m=90V_{rms}.

decreases with increasing value of K. When K is increased, the ratio of the period for discharging C_B to the period for charging L_1 will be increased. Therefore the level of V_B will be lowered. It is also interesting to note from Figures 6.8 and 6.9 that at light load (i.e. R_o increases or k_c decreases) V_B decreases, which is opposite to that of the S^2PFC converter and will be proven by experiment in Chapter 8.6.

On the contrary, the line current quality of the proposed converter will be improved with increasing value of inductance ratio α and turns ratio n and decreasing value of K, as shown in Table 6.1. Therefore a compromise between

the line current quality and the storage capacitor voltage is made. Besides, K should be chosen as small as possible (i.e. increase the charging period of L_2 by $|v_{in}|$) to maximize the direct power transfer of input power to output load. In this design example, $K = 0.5$ is selected. Turns ratio $n = 2$ is then chosen according to Figure 6.9 because M_2 has to keep small at full load. Since L_1 is operated in DCM, $d_5 \leq (1 - d_1 + d_2)$ must be satisfied. Substituting (6.8), (6.14), (6.15) and (6.20) into the inequality, one can obtain an inequality relating the coefficient k_c

$$k_c \leq \frac{n}{M_1}(1 - k_4)[(k_1 + k_2)k_4 - k_2)] \tag{6.38}$$

where

$$k_4 = 1 - \frac{1}{M_2 + nM_1} \tag{6.39}$$

In order to maintain L_1 in DCM, two worst cases should be considered. Firstly, low-line and full-load condition is considered because d_1 and d_2 are at their maximum values. In this case,

$$M1 = \frac{V_o}{V_m} = \frac{20V}{90\sqrt{2}V} = 0.157$$

$$R_o = \frac{V_o^2}{P_{o,max}} = \frac{(20V)^2}{60W} = 6.67\Omega$$

where $P_{o,max}$ is the full-load output power. Secondly, L_1 is more susceptible to run in CCM at the peak input voltage. Therefore, the point at $\theta = \pi/2$ is used for the calculation of (6.38). On the other hand, for the CCM operation of L_2, diode current i_{Do} at t_5 must be greater than or equal zero.

$$b - \frac{n^2 V_o}{L_2} d_5 T_s \geq 0 \tag{6.40}$$

Putting (6.8), (6.14), (6.15) and (6.20) into (6.40), one gets

$$k_c \geq \frac{n}{M_1}(1 - k_5)[(k_1 + k_2)k_5 - k_2)] \tag{6.41}$$

where

$$k_5 = \frac{nM_1[(\alpha + 1)k_6 - \alpha nM_1]}{(k_6 - \alpha nM_1)[(1 - K)|sin\theta| + KM_2 + nM_1] + \alpha k_6(KM_2 + nM_1)} \tag{6.42}$$

$$k_6 = M_2 - |sin\theta| \tag{6.43}$$

1) First iteration: With the transformer turns ratio $n = 2$ and $K = 0.5$, it is first assumed that $\alpha = 0.05$ (A small value of α reduces the voltage stress). From

Figure 6.9, M_2 will be 1.14. Substituting (6.21), (6.22), (6.39) and (6.42) into (6.38) and (6.41), one obtains

$$-0.52 \leq k_c \leq 0.97$$

which indicates the assumption of $k_c = 1$ does not fall within range. This also implies that a CCM operation of L_1 would happen.

2) Second iteration: Now the value of α is increased from 0.05 to 0.1. From Figure 6.9, M_2 will be 1.16. Using (6.38) and (6.41) again it is found that

$$-0.09 \leq k_c \leq 1.07$$

which means L_1 will run in DCM and L_2 in CCM safely with the selected circuit parameters. Assuming f_s = 100kHz (or T_s = 10μs), the value of L_1 can be calculated using (6.37) when R_o is minimum (or output power is maximum).

$$L_1 = k_c R_o T_s = 66.7\mu\text{H}$$

Substituting the value of L_1 into (6.13), one obtains

$$L_2 = L_1/\alpha = 667\mu\text{H}$$

6.6 Experimental results

The hardware prototype of the proposed converter as shown in Figure 6.2 is implemented and tested. The circuit parameters and components used for the experiment are V_{in} = 90-110V_{rms}, L_1 = 64μH, L_2 = 640μH, n = 2, C_B = 220μF, C_o = 4700μF, S1/S2: MTW14N50E, D_o: MUR3040PT, V_o = 20V. The control circuit is simply composed of a voltage-mode controller (TL494), a comparator (LM311) and a logic gate, as shown in Figure 6.10. Figure 6.11 shows the key switching waveforms of the power circuit. The drain-to-source voltage of S1 and S2 when v_{in} = 127V_{dc} are shown in Figure 6.12. It can be seen that v_{DS2} is zero

before S2 is turned on. The filtered line current for different input line voltages and output currents are measured and shown in Figure 6.13 respectively. It can be seen that the input current is not zero at regions near the zero-crossing of the line input voltage. In Figure 6.14, the input current harmonics contents are plotted and shown fulfilling the IEC-1000-3-2 class D standard. Figure 6.15 shows that the power factor is above 0.96 at output power of 25W or higher. The load and line regulations have been tabulated in Table 6.2, showing below 8% steady-state error. The relatively larger error compared to that of Chapter 5 may due to the tolerance of components in the compensation network. To remedy the problem, components with narrower tolerance (i.e., 1% for resistor and 5% for capacitor) can be used. Moreover, the regulation can be further improved by using remote sensing and increasing copper area for power traces.

The measured storage capacitor voltage stresses from light load to full load are recorded in Figure 6.16. In both cases, the maximum storage capacitor voltage to peak input voltage ratio, M_2, is around 1.17, which is very close to the theoretical value. Moreover, it is also shown that the storage capacitor voltage decreases as the load decreases, alleviating the high voltage stress at light load in SSPFC and confirming the theoretical analysis in the previous section. To compare the reduction of the storage capacitor voltage under the same power factor around 0.97, the storage capacitor voltage against the output power of the SSPFC with both stages working in DCM or a DCM boost PFC circuit is also plotted in Figure 6.16. It can be seen that the proposed converter can achieve high power factor with lower storage capacitor voltage.

The conversion efficiency is also compared with the cascaded PFC AC-DC converter (using a boost converter followed by a flyback converter under same input and output conditions). The measurement is taken using the same hardware prototype of the converter for both cases. To measure the efficiency of the cascaded one, the individual efficiency for boost converter (measured by shorting primary of T2 and connecting the load to C_B) and flyback converter (measured by shorting S2 and connecting a DC supply to C_B) are first measured. Then the product of them is the overall conversion efficiency. The recorded result is shown

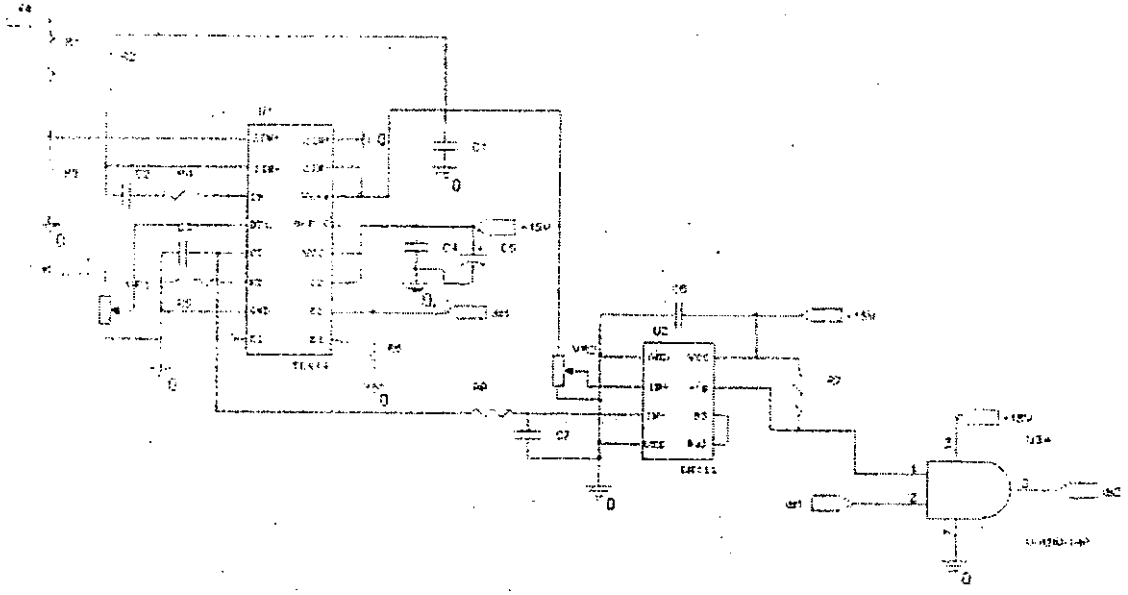


Figure 6.10: Control schematic of the proposed converter.

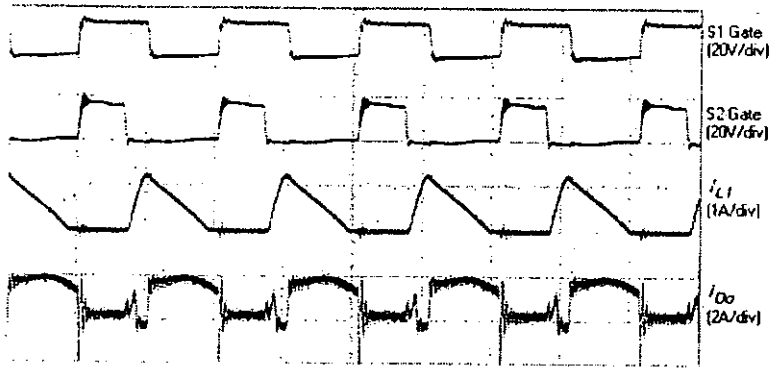


Figure 6.11: Experimental switching waveforms of the power circuit.

in Figure 6.17, showing the proposed converter has a higher conversion efficiency than that of the cascaded one.

6.7 Control of Storage Capacitor Voltage

Although the voltage stress on storage capacitor is significantly reduced using the proposed converter, the fluctuation of this voltage V_B according to line voltage $|v_{in}|$ is still considerable. In this section, a simple control method is proposed to control the storage capacitor voltage V_B of the converter in Figure 6.2 so that the voltage swing of storage capacitor due to line input voltage is further reduced.

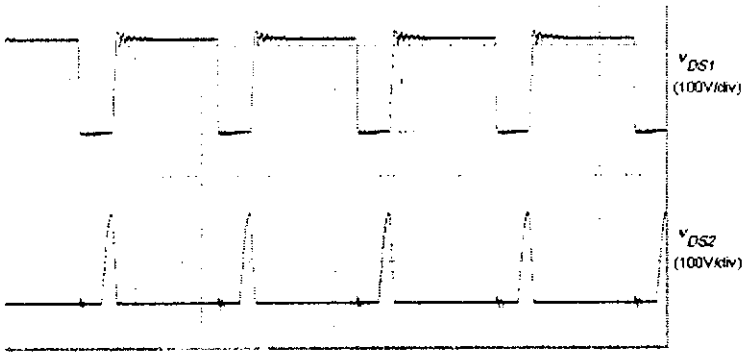
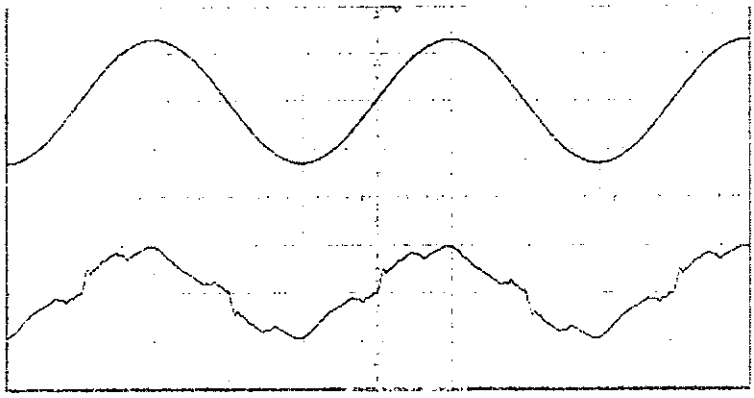
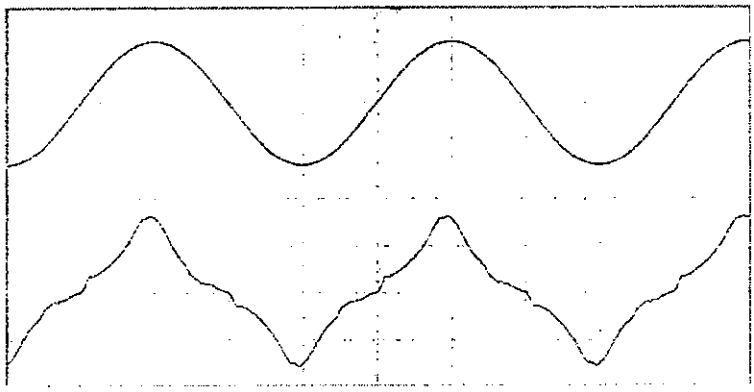


Figure 6.12: Drain-to-Source voltages of S1 and S2 at input voltage equals 127V$_{dc}$. (With RCD snubbers connected across drain and source of S1 and S2.)

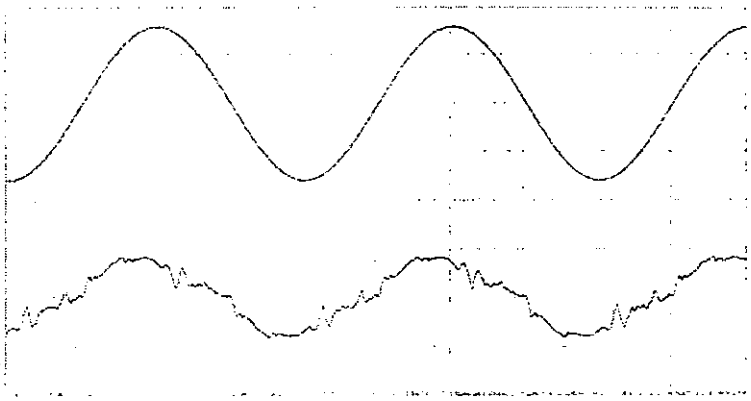


(a) Upper: V_{in} (100V/div); Lower: I_{in} (500mA/div)

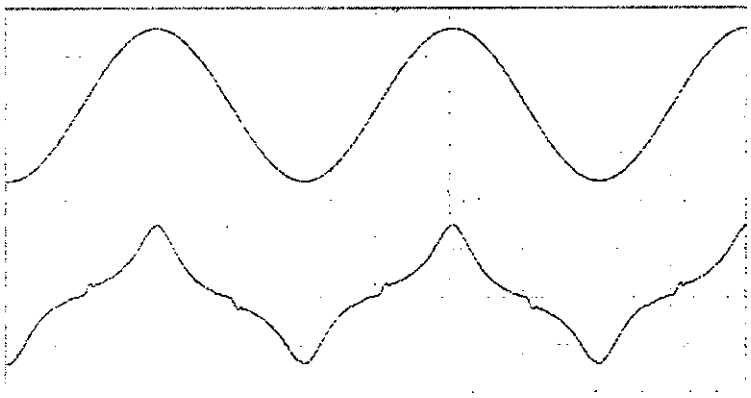


(b) Upper: V_{in} (100V/div); Lower: I_{in} (1A/div)

Figure 6.13: Measured filtered line-voltage and current at different line voltages and output currents. (a) V_{in}=90Vrms, I_o=1A; (b) V_{in}=90Vrms; I_o=3A; (c) V_{in}=110Vrms; I_o=1A; (d) V_{in}=110Vrms; I_o=3A.



(c) Upper: V_{in} (100V/div); Lower: I_{in} (500mA/div)



(d) Upper: V_{in} (100V/div); Lower: I_{in} (1A/div)

Figure 6.13: Measured filtered line-voltage and current at different line voltages and output currents. (a) V_{in}=90Vrms, I_o=1A; (b) V_{in}=90Vrms; I_o=3A; (c) V_{in}=110Vrms; I_o=1A; (d) V_{in}=110Vrms; I_o=3A.

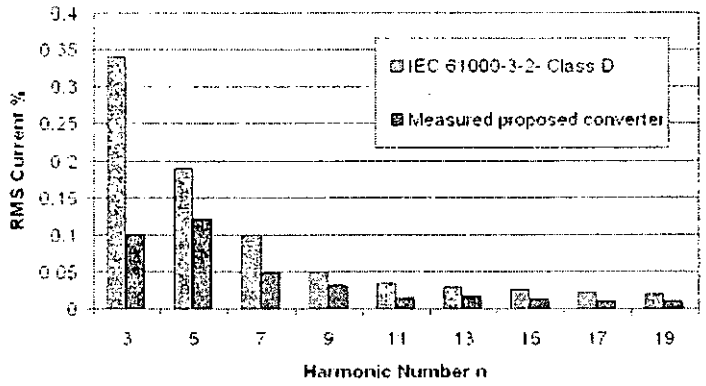


Figure 6.14: Measured harmonics currents at 110Vrms as compared to IEC-1000-3-2 Class D standard.

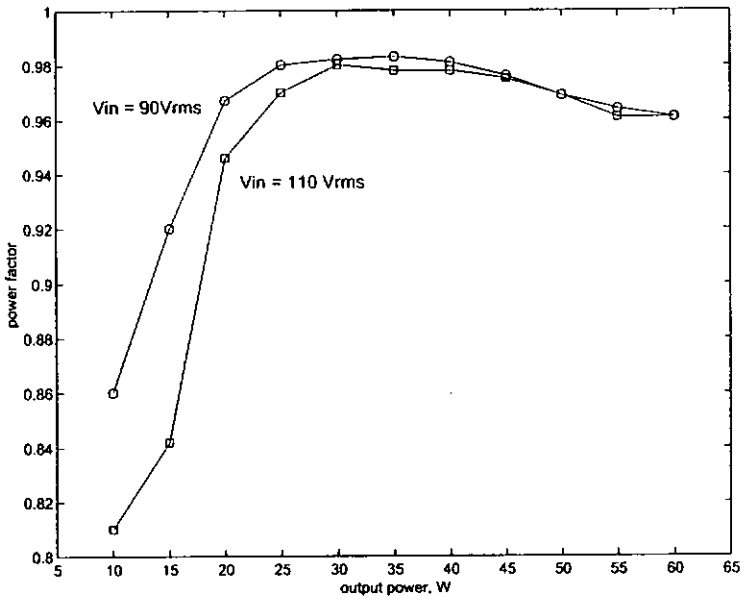


Figure 6.15: Measured power factor against different line and load conditions.

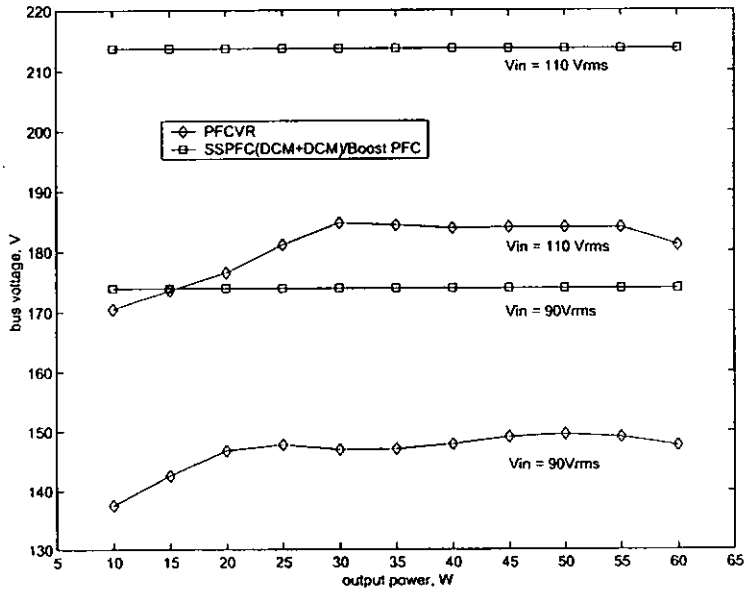


Figure 6.16: Comparison on storage capacitor voltage V_B between the proposed converter and S^2PFC/DCM Boost converter.

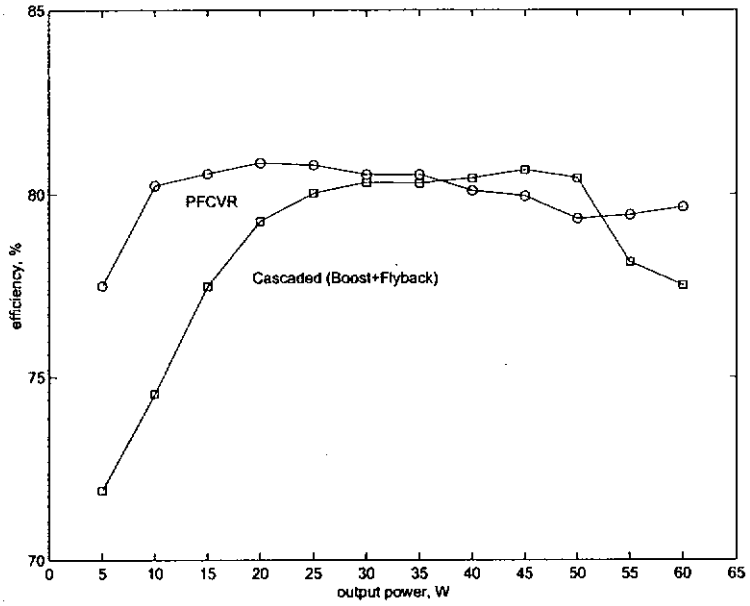


Figure 6.17: Comparison on efficiency between the proposed converter and the cascaded PFC AC/DC converter at V_{in}=110V_{rms}.

I_o(A)	V_o at V_{in}=90V	V_o at V_{in}=110V
0.5	20.76V	20.38V
1.0	20.75V	21.03V
1.5	20.74V	21.54V
2.0	20.74V	21.52V
2.5	20.73V	21.18V
3.0	20.71V	20.80V

Table 6.2: Line and load regulations of proposed converter.

6.7.1 Control Concept

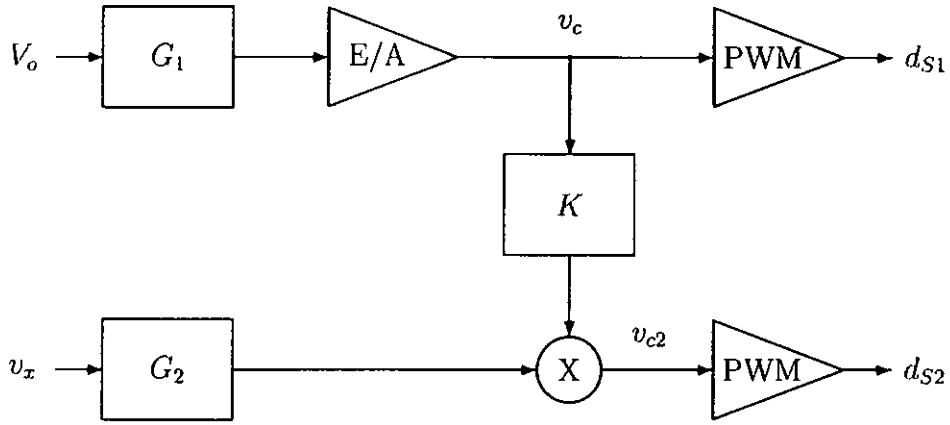
The idea is briefed as follows: when both S1 and S2 are turned on, output power is provided by the storage capacitor; when only the main switch is turned on, output power is provided by the line voltage; when all the switches turns off, energy is stored in the storage capacitor. Since these three power processes are done within a switching period, by controlling the on-time ratio of S2 to S1, K, according to line voltage, the current flowing in and out of the storage capacitor is controlled and hence its voltage can be regulated.

Referring back to Figure 6.8, we can identify the circuit parameters that affect the storage capacitor voltage V_B. It can be seen from this figure that V_B (indicated as M_2, for $M_2 = V_B/V_m$) changes due to the changes of inductance ratio α, coefficient k_c and control factor K. Since α and k_c (changes only slightly when load R_o is changed as shown in Figure 6.16) are fixed by design, the control factor K becomes the only parameter to vary V_B when the line voltage $|v_{in}|$ is changing.

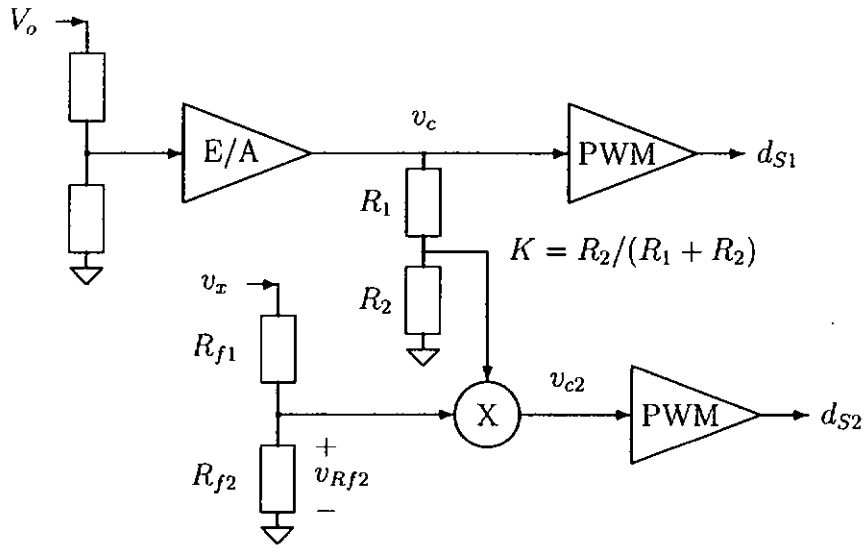
From Figure 6.8, V_B increases when K is reduced, and vice versa. Therefore, to minimize the fluctuation of V_B against change of $|v_{in}|$ (i.e. reduces M_2 when $|v_{in}|$ is increased), duty ratio of S2, d_{s2}, should be controlled in proportional to $|v_{in}|$. Since K is constant by nature, an external variable is needed to incorporate the information of $|v_{in}|$ to vary d_{s2}. A varying voltage v_x is then added and multiplied by K for producing a duty ratio (for S2) which is proportional to $|v_{in}|$ but at the same time fulfilling $d_{s2} < d_{s1}$, as shown in Figure 6.18(a). The control signal for S2, v_{c2}, is given by

$$v_{c2} = Kv_c \cdot G_2 v_x \tag{6.44}$$

Intuitively, this varying voltage v_x should be implemented by $|v_{in}|$ since it is the direct way to incorporate information of $|v_{in}|$ into the control signal v_{c2} of S2. However, if we allow certain fluctuation of V_B according to $|v_{in}|$, then V_B can also implement v_x because V_B also changes proportionally to $|v_{in}|$. Note that G_1 and G_2 are attenuation factors to produce desire range of voltages for compensation and for S2 control signal respectively.



(a) Using a varying voltage v_x as an additional variable to d_{S2} for control of V_B.



(b) Practical implementation of the adopted PWM control incorporating control of V_B.

Figure 6.18: Block diagrams of the adopted storage capacitor voltage control.

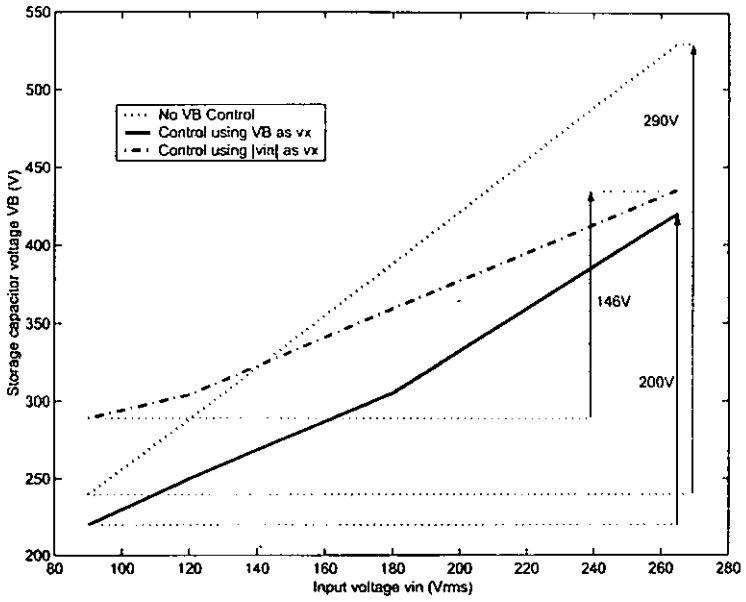


Figure 6.19: Comparison of V_B against $|v_{in}|$ with and without the proposed control.

6.7.2 Control Consideration and Implementation

In practical implementation, there are two main factors to minimize the fluctuation of V_B against $|v_{in}|$. First, the combination of circuit parameters, including α, k_c and n, should give the maximum deviation of M_2 against K, as shown in Figures 6.8 and 6.16. Second, the control signal v_{c2} according to (6.44) should be selected so that d_{s2} gives the maximum deviation with the given range of $|v_{in}|$. The whole range of d_{s2} (i.e. from 0 to d_{s1}) should be used to provide a widest control of V_B. However, if $d_{s2} = 0$ (i.e. no energy from C_B) then the output voltage V_o is out of regulation when $|v_{in}|$=0. If $d_{s2} = d_{s1}$ (i.e. no energy from $|v_{in}|$), then no current flows into the circuit. It follows that the duty ratio of S2 must be within the range given by

$$0 < d_{s2} = KG_2 v_x \frac{v_c}{V_T} < d_{s1} \tag{6.45}$$

where V_T is the peak voltage of the sawtooth waveform of the PWM comparator. As shown in Figure 6.18(b), the attenuation factors G_1 and G_2 and control factor K can be implemented by resistive divider network.

6.7.3 Simulation Results

To verify the proposed V_B control concept (Figure 6.18), a series of simulations using PSpice circuit simulator has been carried out for the proposed S^{2}PFC converter in Figure 6.2 with the following power stage parameters: V_o=20Vdc; P_o=60W; $L_1 = 150\mu$H; $\alpha = 0.2$ and $n = 1.5$. To show the effectiveness of the proposed approach, a comparison of V_B against $|v_{in}|$ with and without the proposed control is shown in Figure 6.19. Figure 6.19 also shows the proposed control using both V_B (with R_{f1}=200k and R_{f2}=1k) and $|v_{in}|$ (with R_{f1}=350k and R_{f2}=1k) as v_x. A small capacitor with value 0.82μF is inserted in parallel with R_{f2} to filter out the ripple voltage. It can be seen that, with the proposed V_B control, the fluctuation of V_B can be minimized to around 31% using V_B as v_x and 50% using $|v_{in}|$ as v_x comparing to the one without the dedicated V_B control. The maximum V_B can also be limited to below 450V for high line condition.

From the results shown above, the proposed control circuit inherits limitation. That is, once the minimum or maximum duty ratio is selected through tuning the values of R_{f1} and R_{f2}, the range of duty ratio d_{s2} according to v_x is confined by the following equation.

$$v_{Rf2} = v_x \frac{R_{f2}}{R_{f1} + R_{f2}} \tag{6.46}$$

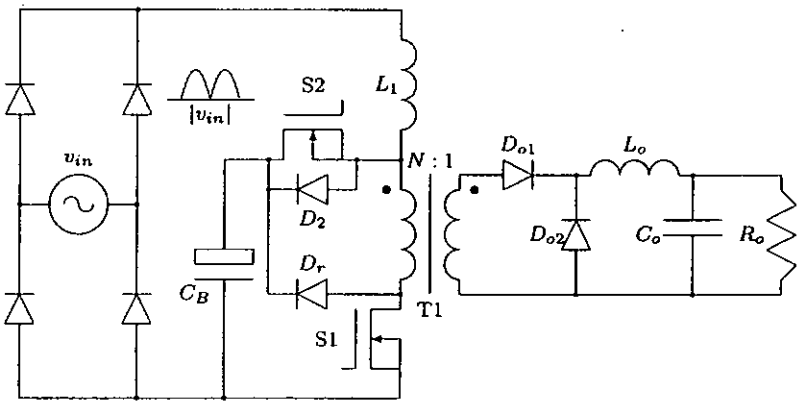
Therefore, to reduce the range of storage capacitor voltage fluctuation against line input voltage, $R_{f1}(R_{f2})$ should be decreased (increased). Table 6.3 confirms the effect of R_{f1} on V_B through another series of simulations ($R_{f2} = 1k\Omega$ and $v_x = V_B$ for all setup).

6.8 Topological Variations

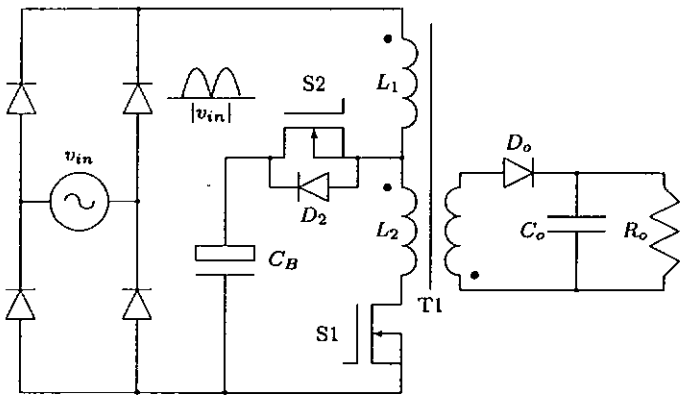
The proposed S^{2}PFC converter using reduced repeated power processing concept can be easily extended to other converters. Figure 6.20(a) shows the circuit of a boost-forward S^{2}PFC converter. It can be seen that when both switches S1 and S2 are turned on, input current from line flows through both L_1 and T1. Input power is diverted to output directly without being stored in the transformer

	$R_{f1} = 350k$	$R_{f1} = 250k$	$R_{f1} = 200k$
v_{in}(rms)	$V_B(V)$	$V_B(V)$	$V_B(V)$
90	262	245	218
120	308	274	250
180	382	339	305
265	478	435	422
ΔV_B	216	190	204

Table 6.3: Effect of R_{f1} on V_B against v_{in}.



(a) Boost-Forward S^{2}PFC converter with diode D_r reset.



(b) Coupled inductor-transformer boost-flyback S^{2}PFC converter.

Figure 6.20: Topological variations of the proposed S^{2}PFC converter.

because D_{o1} is conducted. When S2 turns off and S1 remains on, only C_B delivers power to output. When both switches are turned off, D_{o1} is reversed biased but D_{o2} is conducted. The energy stored in L_1 is transferred to C_B. Note that the addition of diode D_r in this circuit actually performs two functions. First, it is a transformer reset diode to reset the transformer T1 during the off time of switch S1. Second, it clamps the drain voltage of S1 to V_B. In this way, the voltage stress on S1 is reduced and limited to V_B.

To reduce the storage capacitor voltage further, the boost inductor L_1 can be coupled with transformer T1 as shown in Figure 6.20(b). When both switches are turned off, a portion of energy stored in L_1 will be coupled to output through secondary winding of T1 while the rest will be diverted to C_B. In this way, more input power is transferred to output directly after the first power process, improving the conversion efficiency as well. Moreover, since L_1 is coupled with T1, integrated magnetics which uses a single magnetic core is easy to implement. This also reduces the overall converter size.

6.9 Discussion

So far three methods to cope with the voltage and current stresses and conversion efficiency of S^2PFC converters have been introduced. The first method (named Method 1 here) in Chapter 4 added an auxiliary transformer and a few components to existing S^2PFC converter. The second method (named Method 2 here) in Chapter 5 uses output voltage feedback technique as in multiple-output converter to regulate the storage capacitor voltage. The third method (named Method 3 here) in Chapter 6 employed an auxiliary switch with zero-voltage-switching to a new topology. In this section, a brief comparison among these methods will be given.

The comparison of component count is based on the S^2PFC configuration as proposed in [22]. As shown in Table 6.4, Method 3 has the minimum additional component. It is because the auxiliary transistor switches between the input sources (The transformers and diodes added in Methods 2 and 3 assist parallelling

	Method 1(Ch. 4)	Method 2(Ch. 5)	Method 3(Ch. 6)
Transformer	1	1	0
Diode	1	2	0
Transistor	0	0	1
Controller	Conventional voltage-mode PWM	Conventional voltage-mode PWM	Modified voltage-mode PWM

Table 6.4: Comparison on additional component counts and the types of controller used for the proposed three methods (from Chapters 4 to 6).

input sources at the same time). As the auxiliary transistor enjoys zero-voltage-switching, the total size is much smaller than the auxiliary transformer and diode method (Methods 1 and 2). Moreover, it offers lower stand-by power as compared to the converters in Methods 1 and 2 because it can isolate the PFC stage from the DC/DC stage.

Conventional voltage-mode PWM controller can be used in Methods 1 and 2. A modified voltage-mode PWM controller is necessary to control the two switches in Method 3. However, as shown in Figure 6.10, only a few passive components together with a comparator is added to a standard PWM controller.

For storage capacitor voltage V_B reduction, Method 2 reduces V_B to a value below peak input voltage and offers the lowest change of storage capacitor voltage according to change of line voltage. It leads to the lowest and smallest storage capacitor used among the three methods.

All three methods can reduce the current stress on the main transistor and Method 3 results in lowest current stress. As part of the input power is directly coupled to output after the first power process, the transistor handles less input power and hence less input current. For Methods 2 and 3, the power switch handles currents from both input sources (i.e., AC line input and storage capacitor) simultaneously. The auxiliary switch in Method 3 reduces the drain peak turn-off current of main switch (MOSFET is used) by separating the current flowing into the switch from the two input sources.

6.10 Summary

A family of S^2PFC converters with a bi-directional switch to alleviate the intermediate storage voltage stress has been presented and analyzed in this chapter. Formation of the proposed converter using the reduced repeated power processing concept was discussed. By transferring part of the input power to the load directly after the first power process without being stored in the intermediate storage capacitor, the storage capacitor voltage stress is reduced. Even so, it has been experimentally verified that a high power factor is maintained even with lower intermediate storage capacitor voltage. Conversion efficiency is also improved. Furthermore, the storage capacitor voltage stress decreases as load decreases, alleviating the high voltage stress at light load problem in the existing S^2PFC. To reduce the large change of storage capacitor voltage against line input voltage, a simple PWM control strategy has also been proposed.

Chapter 7

Conclusions and Suggestions for Future Research

In this thesis, focus is put on the analysis and design of switching converters for power factor correction (PFC) applications. A number of converter circuits have been reported to solve various practical problems. In this concluding chapter, the major findings that have been obtained in the study are summarized. In addition, some suggestions for future work which may produce promising results are given.

7.1 Conclusions

This thesis proposed a low-loss passive snubber for a CCM boost converter. Experimental results of a 150Vdc/200W prototype confirmed that all the rectifiers were turned off softly and clamped to the output voltage. This concept solved the reverse-recovery related loss problem when the converter operates in CCM. Parasitic ringing was kept to minimum due to the voltage clamping of the rectifiers to the output voltage. Besides, the main switch also enjoyed low-voltage turn-on condition, providing the switching frequency is modulated inversely to the load current.

The main issues concerning single-stage PFC (S^2PFC) converters were investigated. High voltage stress under line and load variations, high current stress on the power switch(es), and low efficiency due to repeated power processing had

been identified. A S^2PFC converter with an auxiliary switch was proposed to solved the problems. Experimental results on a 15Vdc/60W prototype showed the voltage and current stresses were suppressed and the conversion efficiency was improved. It was also found that with CCM operation of the auxiliary transformer, the voltage stress was suppressed at decreasing load.

A S^2PFC converter with a dual-output flyback transformer was also proposed. Experimental results showed that the storage capacitor was loosely regulated by the output voltage. Analytical expression of the storage capacitor votlage relating circuit parameters was derived. It was found that in the presence of leakage and wiring inductances, the storage capacitor voltage changed slightly and proportionally to the input voltage.

A direct control method was applied to a S^2PFC converter with an ZVS bi-directional switch. By controlling the duty ratios of the main and auxiliary switch, the storage capacitor voltage change due to line voltage variation was reduced as much as 50% than that of without the delicated control.

7.2 Future Work

Though much work has been done during this studies, some problems remain unresolved and several new ideas come up from this work. This section introduces a few areas, following the work described in this thesis, which may produce promising results.

7.2.1 Topological Extension for Reducing the Rectifier Reverse-Recovery Current

Chapter 3 proposes a simple passive snubber for a CCM boost converter. This snubber can also apply on other non-isolated converters such as buck, buck-boost and Cuk. Some work needs to be done to incorporate the snubber to these converters. The snubber is also suitable for commonly used transformer-isolated converters such as flyback, forward, half-bridge and full-bridge. These

converters usually apply on high current applications so that the current stress due to the reverse-recovery current may be more severe than that of front-end PFC converters where voltage stress instead of current stress is of prime concern.

7.2.2 Frequency Modulation for Control of Storage Capacitor Voltage Against Line Voltage

Chapter 4 introduces an auxiliary transformer to reduce the voltage stress on the storage capacitor, especially on light load condition. However, the storage capacitor voltage still changes against line voltage variation. In order to reduce the size of storage capacitor, its voltage needs to be regulated. In the past, frequency modulation has been used to shape the input current or to suppress the storage capacitor voltage against load variation. For the proposed converter, only duty cycle is used to provide high power factor, reduced storage capacitor voltage against load variation and tight output regulation simultaneously. So the switching frequency may be used to regulate the capacitor voltage.

7.2.3 Investigation on Circuit Parameters for Control of Storage Capacitor Voltage

Chapter 5 reports using the tight output voltage feedback to control the storage capacitor voltage. However, the inevitable leakage inductance of the transformer hinders the tight regulation of storage capacitor voltage. An investigation on the circuit parameters which affect the variation of storage capacitor should be carried out. The best combination of parameters such as turns ratio and magnetizing inductance will be selected to minimize the influence of leakage inductance. Some other structures such as forward transformer may be considered to give better performance than the present dual-output flyback transformer. Besides, frequency modulation may be incorporated to assist tight regulation of storage capacitor. But the effect of frequency modulation on the regulation of output voltage and the distortion of input current should also be studied.

7.2.4 Optimization of Circuit and Control Parameters for Regulation and Conversion Efficiency

Chapter 6 introduces an active method to the control of storage capacitor voltage. Further improvement on the regulation of storage capacitor voltage and conversion efficiency are needed. Analysis of circuit parameters is needed to give the largest storage capacitor voltage to peak input voltage swing. A better control variable is also necessary to allow the full use of duty ratio range of the bi-directional switch. A detailed model including the leakage inductance and resistive component of each device should be derived to estimate the power dissipation and to find out where the losses go. Improvement on conversion efficiency can be achieved through a deliberate study on the model.

7.2.5 Soft-switching of Switching Power Devices

The S^2PFC converters proposed from Chapter 4 to 6 are of mostly hard-switching of power devices. Dissipative snubbers (e.g. RCD) are normally used to clamp the voltage stress on the power transistors and diodes. As a result, the conversion efficiency of these converters is limited. Boundary conduction mode (BCM) or critical conduction mode is by far the easiest way to achieve soft-switching as no addition of component is needed. BCM operation in the proposed converters may take place to improve the conversion efficiency.

Appendix A

Derivation of Rate of Change of Inductors and Diodes Currents in Chapter 3

At time t_0, the boost switch S1 is turned on. As mentioned, the voltage across L_1 and L_2 are expressed, respectively, as follows.

$$v_a + v_b = V_{in} \tag{A.1}$$

$$v_c + v_d = -(V_o - V_{in}) \tag{A.2}$$

Substituting (3.6) into (A.1) and (A.2), one obtains

$$v_b = \frac{v_a - v_c - V_o}{n-1} \tag{A.3}$$

Due to the magnetic coupling effect, the voltage v_b can also be written as

$$v_b = L_M \left(\frac{v_a}{nL_1 - L_M} + \frac{v_c}{L_2 - nL_M} \right) \tag{A.4}$$

Equating (A.3) and (A.4) one gets

$$v_c = \frac{L_2 - nL_M}{L_2 - L_M} \left[\frac{n(L_1 - L_M)}{nL_1 - L_M} v_a - V_o \right] \tag{A.5}$$

Substituting (3.3) and (3.4) into (A.1), we have another expression of v_c,

$$v_c = \frac{L_2 - nL_M}{L_M} \left[V_{in} - \frac{nL_1}{nL_1 - L_M} v_a \right] \tag{A.6}$$

Combining (3.3), (A.5)and (A.6) we finally obtain the rate of change of i_{L1}

$$\frac{di_{L1}}{dt} = \frac{(L_2 - L_M)V_{in} + L_M V_o}{L_1 L_2 - L_M^2} \tag{A.7}$$

Substitution of (3.1) and (3.2) into (A.7) will result in (3.8). The rest of all equations relating the rate of change of currents are derived using the same method above.

Bibliography

[1] B. Sharifipour, J. S. Huang, P. Liao, L. Huber, and M. M. Jovanovic, "Manufacturing and cost analysis of power-factor-correction circuits," in *IEEE Applied Power Electronics Conf.*, 1998, pp. 490-494.

[2] Electromagnetic compatibility (EMC) - Part 3-2: Limits-Limits for harmonic current emissions (equipment input current $\leq$ 16A per phase), IEC 61000-3-2 document Ed. 1.0: 1995.

[3] Electromagnetic compatibility (EMC) - Part 3-2: Limits-Limits for harmonic current emissions (equipment input current $\leq$ 16A per phase), IEC 61000-3-2 document Ed. 2.1: Oct. 2001.

[4] J. R. Genger, and C. Q. Lee, "Linear peak current mode control: a simple active power factor correction control technique for continuous conduction mode," in *IEEE Power Electronics Specialists Conf.*, 1996, pp. 196-202.

[5] S. B. Yaakov, and I. Zeltser, "The dynamics of a PWM boost converter with resistive input," in *IEEE Trans. Ind. Electron.*, vol. 46, no. 3, pp. 613-619, Jun. 1999.

[6] S. Buso, G. Spiazzi, and D. Tagliavia, "Simplified control technique for high-power-factor flyback Cuk and Sepic rectifiers operating in CCM," in *IEEE Trans. Ind. Appl.*, vol. 36, no. 5, pp. 1413-1418, Oct/Nov. 2000.

[7] M. H. L. Chow, K. W. Siu, C. K. Tse, and Y. S. Lee, "A novel method for elimination of line-current harmonics in single-stage PFC switching regulators," in *IEEE Trans. Power Electron.*, vol. 13, no. 1, pp. 75-83, Jan. 1998.

[8] G. Hua, C. S. Leu, Y. Jiang, and F. C. Lee, "Novel zero-voltage-transition PWM converters," in *IEEE Trans. Power Electron.*, vol. 9, no. 2, pp. 213-219, Mar. 1994.

[9] M. M. Jovanovic, and Y. Jang, "A new, soft-switched boost converter with isolated active snubber," in *IEEE Trans. Ind. Appl.*, vol. 35, no. 2, pp. 496-502, Mar/Apr. 1999.

[10] M. M. Jovanovic, and Y. Jang, "A novel active snubber for high-power boost converters," in *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 278-284, Mar. 2000.

[11] A. Elasser, and D. A. Torrey, "Soft switching active snubbers for DC/DC converters," in *IEEE Trans. Power Electron.*, vol. 11, no. 5, pp. 710-722 Sep. 1996.

[12] P. J. M. Menegaz, J. L. F. Vieira, and D. S. L. Simonetti, "A magnetically coupled regenerative turn-on and turn-off snubber configuration," in *IEEE Trans. Ind. Electron.*, vol. 47, no. 4, pp. 722-728, Aug. 2000.

[13] C. J. Tseng, and C. L. Chen, "A passive lossless snubber cell for nonisolated PWM DC/DC converters," in *IEEE Trans. Ind. Electron.*, vol. 45, no. 4, pp. 593-601, Aug. 1998.

[14] K. Fujiwara, and H. Nomura, "A novel lossless passive snubber for soft-switching boost-type converters," in *IEEE Trans. Power Electron.*, vol. 14, no. 6, pp. 1065-1069, Nov. 1999.

[15] J. K. Chung, and G. H. Cho, "Soft recovery PWM converter with energy recovery and folding snubber network suitable for high-power applications," in *IEE Electron. Letters*, vol. 37, no. 3, pp. 141-142, Feb. 2001.

[16] Q. Zhao, F. F. Tao, F. C. Lee, P. Xu, and J. Wei, "A simple and effective method to alleviate the rectifier reverse-recovery problem in continuous-current-mode boost converters," in *IEEE Trans. Power Electron.*, vol. 16, no. 5, pp. 649-658, Sep. 2001.

[17] M. H. Kheraluwala, R. L. Steigerwald, and R. Gurumoorthy, "A fast-response high power factor with a single power stage," in *IEEE Power Electronics Specialists Conf.*, 1991, pp. 769-779.

[18] I. Takahashi, and R. Y. Igarashi, "A switching power supply of 99% power factor by the dither rectifier," in *IEEE International Telecommunications Energy Conf.*, 1991, pp. 714-719.

[19] D. M. Divan, G. Venkataramanan, and C. Chen, " A unity power factor forward converter," in *IEEE Ind. Appl. Society Annual Meet.*, 1992, pp. 666-672.

[20] M. Madigan, R. Erickson, and E. Ismail, "Integrated high quality rectifier regulators," in *IEEE Power Electronics Specialists Conf.*, 1992, pp. 1043-1051.

[21] M. Brkovic, and S. Cuk, "Automatic current shaper with fast output regulation and soft-switching," in *IEEE Telecommunications Energy Conf.*, 1993. pp. 379 -386.

[22] R. Redl, L. Balogh, and N. O. Sokal, " A new family of single stage isolated power factor correctors with fast regulation of the output voltage," in *IEEE Power Electronics Specialists Conf.*, 1994, pp. 1137-1144.

[23] S. Luo, H. Wei, G. Zhu, and I. Batarseh, "Several schemes of alleviating bus voltage stress in single stage power factor correction converters," in *Proc. IEEE Power Electronics and Drive Systems Conf.*, 1999, pp. 921-926

[24] K. H. Liu, and Y. L. Lin, "Current waveform distortion in power correction circuits employing discontinuous-mode boost converters," *IEEE Power Electronics Specialists Conf.*, 1989, pp. 825-829.

[25] M. M. Jovanovic, D. M. C. Tsang, and F. C. Lee, "Reduction of voltage stress in integrated high-quality rectifier-regulators by variable-frequency control," in *Proc. IEEE Applied Power Electronics Conf.*, 1994, pp. 569-575.

[26] M. H. L. Chow, Y. S. Lee, and C. K. Tse, "Single-stage single-switch isolated PFC regulator with unity power factor, fast transient response, and low-voltage stress," in *IEEE Trans. Power Electron.*, vol. 15, no. 1, pp. 156-163, Jan. 2000.

[27] L. Huber, and M. M. Jovanovic, "Single-stage single-switch input-current-shaping technique with fast-output-voltage regulation," in *IEEE Trans. Power Electron.*, vol. 13, no. 3, pp. 476-486, May. 1998.

[28] J. Qian, Q. Zhao, and F. C. Lee, "Single-stage single-switch power factor correction AC/DC converters with dc-bus voltage feedback for universal line application, " in *IEEE Trans. Power Electron.*, vol. 13, no. 6, pp. 1079-1088, Nov. 1998.

[29] C. Qiao, and K. M. Smedley, "A topology survey of single-stage power factor corrector with a boost type input-current-shaper," in *IEEE Trans. Power Electron.*, vol. 16, no. 3, pp. 360-368, May 2001.

[30] Q. Zhao, and F. C. Lee, "Single-switch parallel power factor correction AC2DC converters with inherent load current feedback," in *IEEE Applied Power Electronics Conf.*, 2002, pp. 270-276.

[31] H. Wei, I. Batarseh, G. Zhu, and P. Kornetzky, "A single-switch AC-DC converter with power facter correction," in *IEEE Trans. Power Electron.*, vol. 15, no. 1, pp. 421-430, May. 2000.

[32] K. schenk, and S. Cuk, "A single-switch single-stage active power factor corrector with high quality input and output," in *Proc. IEEE Power Electronics Specialists Conf.*, 1997, pp. 22-27.

[33] Q. Zhao, F. C. Lee, and T. S. Tsai, "Voltage and current stress reduction in single-stage power factor correction ACDC converters with bulk capacitor voltage feedback, " in *IEEE Trans. Power Electron.*, vol. 17, no. 4, pp. 477-454, Jul. 2002.

[34] Y. Jiang, and F. C. Lee, "Single-stage single-phase parallel power factor correction scheme," in *IEEE Applied Power Electronics Conf.*, 1994, pp. 1145-1151.

[35] O. Garia, J. A. Cobos, P. Alou, R. Prieto, and J. Uceda, "A new approach for single stage ac/dc power factor correction converters with an improved energy processing", *IEEE Power Electronics Specialists Conf.*, 1998, pp. 1061-1067.

[36] J. Sebastian, P. J. Villegas, F. Nuno, and M. M. Hernando, "High-efficiency and wide-bandwidth performance obtainable from a two-input buck converter", *IEEE Trans. Power Electron.*, vol. 13, no. 4, pp. 706-717, Jul. 1998.

[37] O. Garcia, J. A. Cobos, P. Alou, R. Prieto, J. Uceda, and S. Ollero, "AC/DC converters with tight output voltage regulation and with a single control loop," in *IEEE Power Electronics Specialists Conf.*, 1999, pp. 1098-1104.

[38] T. F. Wu, Y. J. Wu, and Y. C. Liu, "Development of converters for improving efficiency and achieving both power factor correction and fast output regulation," in *IEEE Applied Power Electronics Conf.*, 1999, pp. 958-964.

[39] C. K. Tse, M. H. L. Chow, and M. K. H. Cheung, "Reduced redundant power processing (R^2P^2) PFC voltage regulators: circuit synthesis and control", *IEEE Power Electronics Specialists Conf.* (2000) 825-830.

[40] O. Garcia, J. A. Cobos, P. Alou, R. Prieto, and J. Uceda, "A simple single-switch single-stage AC/DC converter with fast output voltage regulation," in *IEEE Power Electronics Specialists Conf.*, 1999, pp. 111-116.

[41] J. Y. Lee, and M. J. Youn, "A single-stage power-factor-correction converter with simple link voltage suppressing circuit (LVSC)," in *IEEE Trans. Ind. Electron.*, vol. 48, pp. 572-584, Jun. 2001.

[42] D. D. C. Lu, D. K. W .Cheng, and Y. S. Lee, "A single-switch power-factor-corrected converter with reduced repeated power processing," Proceedings of *IEEE power electronics and drive systems conf.*, 2001, pp. 26-32.

[43] C. K. Tse, and M. H. L. Chow, "Theoretical Study of Switching Converters with Power Factor Correction and Voltage Regulation," *IEEE Trans. Power Electron.*, vol. 47, no. 7, pp. 1047-1055, Jul. 2000.

[44] O. Garcia, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, "Single phase power factor correction: a survey," in *IEEE Trans. Power Electron.*, vol. 18, no. 3, pp. 749-755, May 2003.

[45] Y .S. Lee, K. W. Siu, and B. T. Lin, "Novel single-stage isolated power-factor-corrected power supplies with regenerative clamping," in *IEEE Trans. Ind. Appl.*, vol. 34, pp. 1299-1308, Nov/Dec. 1998.

[46] A. Lazaro, A. Barrado, J. Pleite, R. Vazquez, and E. Olias, "New family of single-stage PFC converters with series inductance interval," in *IEEE Power Electronics Specialists Conf.*, 2002, pp. 1357-1362.