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Mixed-Signal Built-In Self-Test

by

Gorla, Naga Sujatha

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Department of Electronic and Information Engineering

The Hong Kong Polytechnic University

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Abstract

Due to the rapid advances in systems integration especially in the fields of multimedia, mobile communications and portable data systems, the growing need for mixed-signal integrated circuits (ICs) has accelerated efforts in the design and testing of analog circuits. Integrating both digital and analogue circuits on a single chip improves performance and reduces board size and cost. As a result, the circuits become more complex and hence raise the problem of design for testability. A traditional approach to testing a mixed signal IC is to partition the circuit into several sub-blocks, such that the inputs and the outputs from each sub-block can be directly controlled and observed. However the partition of a mixed-signal IC is a difficult proposition, since testability analysis is computationally very expensive and circuit partitioning requires the design and integration of test specific hardware.

Recently, a defect oriented technique known as Oscillation-based Test Methodology (OTM) has been widely studied as a core for a built-in self-test structure, to improve the design testability. The methodology is based on converting the whole circuit under test into an oscillator wherein the oscillation frequency is compared to the nominal oscillation frequency. Any deviation in the observed oscillation frequency or no oscillation indicates possible fault in the circuit under test. The OTM offers some unique advantages, such as the testing of a circuit without external stimuli and a reduction in test time due to the limited number of oscillation frequencies. Therefore, OTM can be easily implemented. However, one of the main disadvantages is that, it cannot precisely identify the fault location. Hence, in this research work, an attempt is made to improve the fault locating capability, by integrating OTM with the Power Supply Current (PSC) measurement technique.

In PSC technique, the current passing through the V_{DD} terminal is monitored during application of each input stimulus, wherein, every fault condition can be considered as a change in current through the V_{DD} terminal. A fault is considered as detectable when the corresponding current value exceeds a tolerance bound around the nominal value. The sensitivity of the PSC measurement is investigated by considering those faults, which are indistinguishable, by no-oscillation in OTM. In order to test the feasibility of this technique, the threshold detector, which is commonly used in telephone tone ringer applications, was chosen for this study. In the initial test phase, OTM is applied to the detector circuit and the results showed that 129 faults were detectable, but the location was unidentifiable. In the second phase PSC measurement technique is applied in addition to the OTM to improve the fault locating capability. The results showed that 3 faults were uniquely identified and the remaining faults were grouped into 78 equivalent fault sets. Finally, in order to further increase the efficiency of the fault diagnostic resolution, a Node Voltage Measurement (NVM) technique was combined along with the above mentioned OTM and PSC techniques.

In NVM measurement technique, voltage measurements were recorded at the output node of the individual op-amps and digital gates. Similar to PSC testing method, each measured node voltage has a tolerance band of ±5%. Since some faults within an equivalent fault set may cause different voltages to appear at different circuit nodes, these voltage amplitudes are then compared and used to further differentiate these faults within that particular equivalent fault set. Of the 126 faults unable to be located by the PSC technique, when tested by this method, the results showed that 44 faults were uniquely identified and the remaining were grouped into 122 equivalent fault sets. From the simulation experiment carried out, it is found that by coupling the OTM and PSC technique, only 8.24% of the fault location could be uniquely identified. Whereas,

by integrating NVM based on a pre-selected set of internal circuit nodes, the diagnostic resolution could be increased by 26.35%.

This thesis presents a detailed case study of the testing of a detector circuit using the OTM method and suggests solutions to enhance the fault diagnostic resolution. The difficulties and shortcomings of this testing approach are discussed in detail. In general, OTM is effective for its high fault coverage and is easy to implement. The major advantage over other testing approaches is that no test generation needs to be considered. The major weakness of OTM is the low identification capability of fault location. However, with careful selection of other parameters, such as power supply current measurement and node voltage measurements as carried out in this study, fault diagnostic resolution can be further improved

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Chapter 1

Introduction

1.1 Testing of mixed-signal ICs

Advances in semiconductor process and integrated circuit design technology have made testing an essential part of high quality manufacturing process, design and production efforts. Errors in manufacture can result in the production of defective units, which need to be discarded. Exhaustive test can be used to determine whether or not a device is functionally correctly. In this approach the outputs are verified for all different input values. This method is impractical for devices with a large number of inputs.

Effective test procedures are necessary components of any high quality manufacturing process. The primary objective of a test process is to determine if the unit, which is produced by the manufacturer, is defect–free and will function as desired. The secondary important objective is to generate new techniques that can be used to improve process yield and thereby reduce the cost. Though digital circuits occupy the larger parts of the whole system in the modern electronic industry, they cannot replace the role of analog parts completely. In modern electronic world ICs with digital, analog, and mixed-signal circuits on the same substrate are popular, because of their applications in wireless communication, networking, multimedia, process control, and real-time control systems. With the increasing commercial prominence of analog and mixed signal ICs, the testing of these ICs is received substantial attention from academic researchers, as well as from industry. As a result, analog and mixed-signal IC test is one of the hottest issues in test research and development.

1.2 Overview of mixed-signal testing

In a mixed-signal testing, the digital portion of a mixed-signal device is tested by the mature digital test methods (e.g. functional, structural, I_{ddq}) and DFT techniques. Furthermore, automatic test pattern generation (ATPG) techniques have reduced the test generation cost for digital circuits. Analog testing lacks such tools and techniques because of infinite number of values present in an analog signal. Therefore, analog testing is becoming a bottleneck in the testing of mixed-signal ICs in terms of cost and quality. In analog circuits, testing can be accomplished using specification-based (functional testing) and defect-based techniques (defect-oriented methodology).

1.2.1 Specification-based testing

The objective of functional testing is to validate the correct operation of a system with respect to its functional specifications. In analog functional testing analog circuits are tested for dc and ac specifications like input offset voltage, input bias current, common-mode voltage range, output voltage swing, output impedance and output current, total harmonic distortion, signal-to-noise ratio, slew rate and output power. The above specifications are tested by some ac and dc voltage measurements at different internal nodes using "bed of nails" concept. Specification-based tests offer the advantage of ensuring a circuit that passes the test process will meet a user's needs. Test generation is straightforward, since tests can be generated directly from the specifications. But all modern electronic systems are often multi-layered and/or coated, there by limiting the applicability of the "bed of nails" concept and also the verification of all specifications makes the functional testing costly and time consuming.

1.2.2 Defect-oriented testing

Application of a defect-oriented approach [1] in solving analog test problems has gained popularity in recent past [2 - 7]. It is proposed as one of the alternatives to analog functional testing. In this approach, a defect simulator translates the characteristics of actual defects occurring in the manufacturing process into a behavioral description of the circuit at the chosen level of abstraction. Two types of defects are considered during simulation: spot defects and variation in the process parameters. Stacking faults, oxide pinholes, and extra or missing pieces of a conductor or semiconductor layer are all considered to be spot defects. The above described defect simulation approach, which provides an objective basis for analog fault model development and test generation, is based on manufacturing process defects. The manufacturing process defects, catastrophic as well as non-catastrophic, form the core of the methodology. In this testing methodology realistic defects are sprinkled over the circuit to determine the realistic fault classes (determining whether the defects cause faults and if so extracting the circuit-level faulty behavior). Then fault simulation is performed for fault classes by inserting fault model into a circuit (e.g. catastrophic short in metal layers are modeled as a resistor with nominal value of 0.2 ohms, shorts in poly and diffusion layers are modeled with a resister of 20 and 60 ohms). The response of the analog simulator (e.g. SPICE) is called a fault signature or fault dictionary. A fault is considered detectable if the fault response differs from the fault-free (good) signature by a predetermined threshold. In general, faults in ICs can be categorized as catastrophic (HARD fault) and parametric (SOFT fault). Catastrophic faults are caused by stuck-shorts and stuck-open in a component or at the connection to a component. Parametric faults (out-of specification faults) could result from manufacturing process

fluctuations, design errors (due to simulation or layout problems) and aging or parasitic effects.

The implementation of the above methodology is separated into two phases. Phase-1 is related to defects and fault modeling, and phase-2 related to the analysis flow. The former is concerned with the collection of defect data for a given circuit under test (CUT), modeling of defects for a given fault simulator, and so on. The latter is concerned with establishing an analysis flow, determination of pass/fail criterion, etc.

The defect-oriented methodology is applied to the mixed-signal circuit of flash ADC [44] to calculate the fault coverage. It detected 93.3% of catastrophic and 93.1% of the non-catastrophic faults by voltage and current responses of analog simulator (SPICE). The methodology also proved to give useful DFT feedback. By taking specific DFT measures, the fault coverage could be increased to 99.1%. The test time needed to obtain this fault coverage is approximately 640us, which compares favorably with specification-oriented tests.

1.3 Basic concepts on mixed-signal testing

1.3.1 Fault modeling strategy

It has been implemented to develop analog fault models representing the effect of spot defects in CMOS circuits [8]. Fault models for analog functional blocks are performed by the following sequence of operations:

Step 1. Defect simulation

Step 2. Formation of the fault models

Step 3. Verification of the fault model

Defect simulation should be performed to find the circuit faults that are likely to occur in actual IC's. To do so defect simulator should insert defects into the circuit's element parameters and then determine if the resulting structure causes a change in the circuit's behavior.

Formation of the fault model should be a process of mapping circuit behaviors into a model, which could simulate such behaviors. Such mapping could be built by:

- Grouping results of defect simulation into sets having similar characteristics.
- Building a model of the analyzed functional block for "fault-free" operation.
- Introducing into this "fault-free" model modifications and extra elements that would be used to deform its behavior in the manner characteristic for each of the groups identified in above step.

The final step of the proposed methodology should be the fault model verification. In this the result of simulations are compared quantitatively (i.e., by measuring the difference between the obtained responses).

Based on the model analysis, many approaches are presented such as functional fault models, defect-based fault models, parametric fault models and mixed approaches [9]. Several fault location techniques reported in literature only address cases when just one component causes the fault. In practice, the multiple-fault case could occur, even though the probability is small, and some faults can mask the others. Recent techniques address this as a difficult case [10]. Although many other fault models have been proposed such as multiple-stuck faults, bridging faults, delay faults, etc, still the main faults are the single-stuck faults.

1.3.2 Fault coverage

Fault coverage is the percentage of detectable faults detected by the test set:

$$\text{Fault Coverage} = \frac{F_{detected}}{F_{total} - F_{undetectable}} \quad (1.1)$$

where $F_{detected}$ is the number of faults detected, F_{total} is the total number of faults considered, and $F_{undetectable}$ is the number of faults proven to be undetectable.

So it is important to decrease the undetectable faults. In fact, it is impossible to achieve 100% fault coverage in real circuits, but undetectable faults can be minimized to the greater extent. If fault coverage is obtained beyond 90%, then it is considered as a success. In reality, there are several ways of computing the fault coverage, and their results may differ greatly [34].

1.3.3 Diagnostic resolution

The degree of accuracy to which faults can be located is referred to as diagnostic resolution. The partition of all the possible faults into distinct sets of functionally equivalent faults defines the maximal fault resolution, which is intrinsic characteristic of the system. The fault resolution of a test sequence reflects its capability of distinguishing among faults, and it is bounded by the maximal fault resolution. This is illustrated in Figure 1.1. A,B,C,D,E, and F represent the sets of equivalent faults of a system. Consider a test sequence T that does not distinguish between (the faults in)A and (those in) B, or between E and F. The maximal fault resolution is the partition {A,B,C,D,E,F},while the resolution of T is $\{A \cup B, C, D, E \cup F\}$.

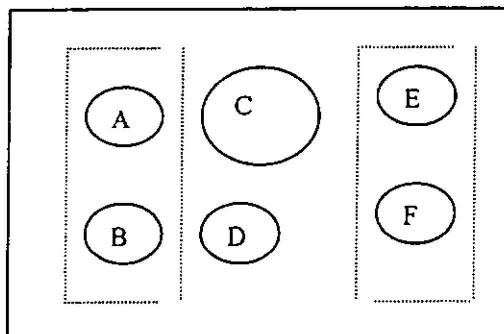

Figure 1.1 Fault resolution

1.4 Testing of analog and mixed-signal circuit using power supply current measurement

Quiescent power supply current (I_{ddq}) monitoring technique has been used for digital CMOS testing to detect the manufacturing defects. This idea was published [11,12] in early 1980s. In this technique I_{ddq} is defined as the current drawn by a CMOS IC during the logic quiescent period (when all logic states have settled and are in a steady state or quiescent mode). This current has a very low value, typically on the order of nano-amps for defect-free IC's, while raised to higher levels, on the order of milliamperes, by the presence of defects. But it is unsuitable for many analog circuits because of the large quiescent currents of such circuits. Similar methods using power supply current (I_{PS}) measurements have been proposed for analogue and mixed-signal ICs [37-42]. By taking the RMS value of the supply current variation [13], the quiescent component can be removed, potentially avoiding the masking of faults. In case of Fault dictionary based on I_{PS} measurement, the RMS value of I_{PS} for fault-free circuit is known as nominal value and a fault dictionary is formulated using the RMS value of I_{PS} for a variety of simulated extreme failures. A fault is considered as detectable when the corresponding RMS value of I_{PS} exceeds a tolerance bound around the nominal value (e.g.$\pm$10%, heuristic bound). When the RMS value of I_{PS} for the circuit under test is close to a value in the dictionary, within the heuristic bound, and its difference is more than $\pm$10% from all others, then the fault is considered as identified. Various number of circuits have been examined, and it has been found that very high levels of fault coverage can be achieved by applying a very small number of sinusoidal input stimuli with varying amplitudes, frequencies and DC offsets.

1.5 A DSP based approach for testing linear and non-linear analog circuits in time domain

Digital Signal Processing (DSP) test technique combine sampled-data method with mathematical analysis to make high accuracy analog measurements like voice frequency parameters such as gain, signal-to-distortion, harmonic distortion, intermodulation distortion and random noise [14]. An approach [15] based on signal processing and time domain analysis is proposed to test linear and non-linear analog circuits. In this process a step signal is applied as an input stimuli and the response is measured at the output. In practice, the measured output signal may be corrupted by superimposed signals such as DC offset and noise, which could influence the test decision. In order to overcome these problems, filtering and differentiation of the output signal are performed using a DSP unit. The differentiation technique increases sensitivity and reduces the number of samples necessary for testing. Different orders of the digital differentiators were examined to study their influence of sensitivity magnitude. The eighth order defferentiator gave the higher value for sensitivity but it required more hardware compared to the second and fourth order defferentiators. The filtering operation used to eliminate noise decreases the sensitivity of the derivative signal with respect to the different components.

Testing the analog portion is difficult because analog testing is still an art. It lacks the structure and the formalism of its digital counterpart. There are no well established mathematical models that can be used to automate analog test generation and measure analog test effectiveness. Concepts such as fault model and fault coverage are still being defined. Additionally, due to the integration of analog and digital circuits on a single device, access to the internal signals of the analog portion is limited. This

can greatly affect controllability and observability of the mixed-signal chip. The above problem of mixed-signal testing can be overcome by new design for testability (DFT) approaches.

1.6 Outline of the thesis

Chapter 1 presents an overview of the mixed signal testing that contains a detailed description of the specification-based testing and the defective oriented testing. This also includes the basic concept of mixed signal testing using different methods like power supply current method and the DSP method.

Chapter 2 discusses a variety of Design-for-Test (DFT) techniques that contains detailed description of generic and macro-based DFT techniques with special emphasis on the Built-In Self-Test approach. In this different design structures to improve the observability and controllability of their internal signals in analog and mixed signal circuits, the basic concept of the I_{ddq} current technique and brief description about on-chip and off-chip current measurement approaches are presented.

Chapter 3 presents a brief introduction of fault diagnosis based on Oscillation Test Methodology. In this the basic concept of OTM, different techniques to convert the CUT into an oscillator and the implementation of the OTM on single op-amp, are described.

Chapter 4 describes the fault diagnosis of a mixed-signal circuit based on the new proposed testing approach, which is a combination of OTM and power supply current measurement techniques. The feasibility of the proposed approach is conducted on a detector circuit which is used in telephone tone ringer chip. This chapter also contains the detailed description of the fault analysis from the simulation data obtained.

Chapter 5 covers the fault analysis of the detector circuits using I_{ddq} current measurement technique.

Chapter 6 discusses a proposed Node Voltage Measurement technique, which is used to further increase the fault locating capability of the proposed testing approach. It explains the basic concept of the NVM and provides detailed description of the fault analysis of the detector circuit using the NVM technique.

Chapter 7 concludes the summary of the work done and main achievements of this research work. Finally, future extension of the present work is also discussed.

Chapter 2

Design-for-testability

2.1 Overview of DFT

In many instances, traditional approaches to test generation and application may be too expensive. Alternatively, test generation may not provide an adequate coverage of expected physical defects. Design-for-test is one approach to reduce total test costs, test application time and/or improve defect coverage [45,46,47]. A design-for-test (DFT) technique modifies a circuit to improve its testability. The important attributes related to testability are controllability and observability. Controllability is a measure of the ease with which individual elements can be manipulated by stimuli applied to the system. Observability is a measure of the ease with which the behavior of individual elements can be seen from the test points or edge connections. In general, factors that must be considered when deciding upon the test method to be adopted in any design will include the following [16]:

- area overhead
- pin count overhead
- test length
- fault coverage
- automatic test equipment(ATE) requirements

2.2 Generic DFT techniques

In spite of the lack of general design techniques, and significant differences between various types of circuits, several generic test methods, such as partial scan, full scan, Built-In Self-Test (BIST) and boundary scan are developed. The main goal of these techniques are to increase the ability to control and observe the values of internal signals. Although they are mostly addressed in digital world, the principles may be suitable for analog part [17]. Analog circuits are typically characterized as being circuits where the signals are in the form of continuous variations in amplitude, phase, frequency, or waveform. They also present challenges in implementing DFT [18]. One of the more promising DFT techniques is the BIST approach [19,20,21,22,23] in which control, test stimulus generator and measurement circuitry are placed on the same chip and should be able to present a binary pass or fail result. Figure 2.1 shows the scheme, which may be used in any analog or mixed signal circuits.

Referring to Figure 2.1, the complete BIST scheme consists of five basic parts which are described below:

- The excitation part, which includes the test signal generator, an instrumentation amplifier and a frequency divider.
- The circuit under test (CUT) interface with analog multiplexers and buffers to connect the nodes of excitation, and the test points of the CUT to the proper inputs and outputs of the BIST structure.
- The comparison part, which compares responses to the nominal ones stored in the EPROM chip (called healthy signature dictionary).
- The timing circuitry.
- The fault-indicating part, which can locate the test points with faulty signatures.

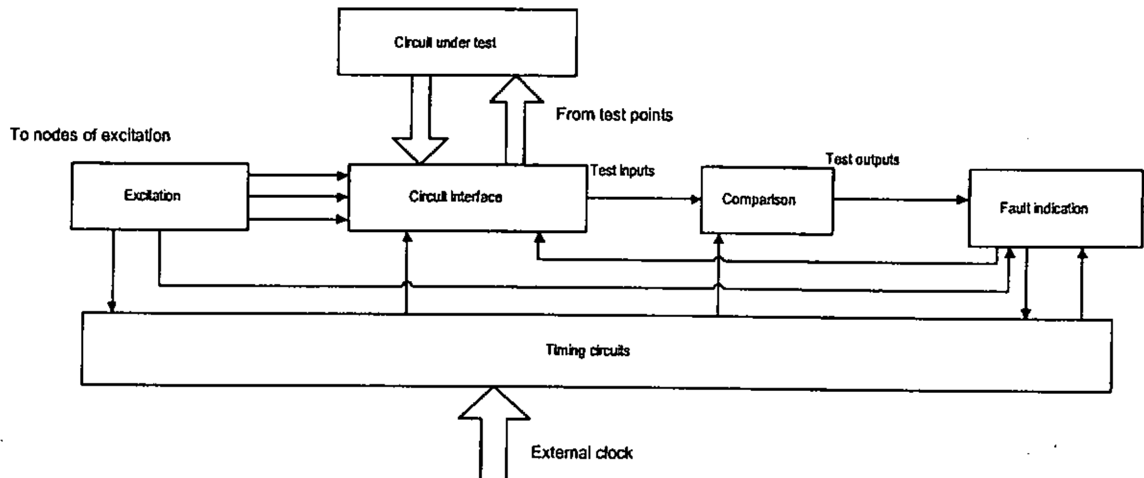

Figure 2.1 Block diagram of the analog BIST structure

A self-test of the CUT would be passed when the measurements agree with the corresponding prestored signatures, within certain tolerance bounds. To cope with the technology advances, automatic test equipment to test PCBs became so expensive in the late 1980s and it was almost impossible to continue producing PCBs profitably.

The use of the Boundary-Scan-Test (BST) methodology can drastically reduce these test costs. BST originates from the design-for-testability philosophy as applied in the IC technology. Today, in order to adapt the requirements in modern industry, a series of IEEE BST related standards [33] have been developed and maintained as mentioned below.

- IEEE Standard 1149.1 Standard Test Access Port and Boundary-Scan Architecture
- IEEE P1149.2 Extended Serial Test Bus (Draft Standard)
- IEEE P1149.4 Mixed Signal Test Bus (Draft Standard)
- IEEE P1149.5 Module Test and Maintenance Bus (Draft Standard)

The IEEE 1149.1 Boundary scan (also known as JTAG) standard, which defines digital testability structures for implementation on integrated circuits, has proven to be very successful. But this standard does not, however, address analog aspects of board test, such as measuring passive component values, detects opens and shorts between off-chip analog components and diagnostically testing differential signal paths.

In 1996, the P1149.4 working group, through various conference panel discussions, then proposed the P1149.4 standards for a mixed-signal test bus, which targets the above mentioned areas, and also provides access for external test of on-chip mixed-signal circuits.

2.2.1 Brief description of the P1149.4 mixed-signal test bus

The P1149.4 standard [1] is intended to be an extension of the IEEE 1149.1 standard. According to this P1149.4 standard, an IC will have the digital TAP controller pins defined in P1149.1, namely: TCK, TMS, TDI, TDO, and optionally TRST. It will also have at least two analogue bus (for parametric measurement) pins, AT1, AT2 and one IN or OUT pin.

The Salient features of the P1149.4 mixed-signal bus are:

- Continuous time access to selected nodes, by on-chip or off-chip test facilities
- Direct control and observation of voltages and currents through linear switches or buffers
- Measurement of continuous variables such as resistance, capacitance and delay
- The primary benefit is increased diagnosability, which can reduce IC and board design verification time and reduce board and system repair time.

- Because of all above advantages this will support for self-test.

Apart from the BST approach, there are several frequently used BIST structures, which use DFT techniques to increase the observability and controllability of an analog and mixed signal circuits. These techniques are described in the following paragraphs.

2.2.2 Analog BIST structure using scan-path technique

Figure 2.2 shows an analog built-in self-test (ABIST) structure using a scan-path technique [24,25]. It uses a sample and hold circuit to increase the number of accessible nodes while minimizing the output pin overhead. To do so, the sample and hold circuit simultaneously loads test point voltages into corresponding capacitors via a network of buffer amplifiers in a process termed parallel loading. Next, each test voltage is passed to a single output pin through a set of switched voltage followers (switch timing ensures that only one voltage is passed to the output at any one time). For example, the voltage at holding capacitor C_4 is passed to the output by closing the switch SP_4 and through voltage follower VF_4 and VF_{out}. According to the switching operation of the proposed ABIST structure, the data held at the first stage will be passed out last. As the result, the capacitance required in that stage must be large enough to hold the data before they are passed out. This structure provides more test points, while still keeping low pin overhead and it also provide an innovative feature that allows designers to use one channel of an oscilloscope to simultaneously monitor multiple output waveforms of analog circuits or systems.

Despite the advantages mentioned above, this structure has some disadvantages. For instance, if number of stages in unit-under-test (UUT) increases, the test circuit needs a larger capacitance value to hold the data before the data is passed to the output. Therefore a large chip area in the system is occupied because of a larger capacitance

area. There are also difficulties in generation of test vectors. Recently a number of oscillation-based testing methodologies [26,27,28] have been proposed to solve the above-cited difficulties. Detailed description of the OTMs will be given in Chapter 3.

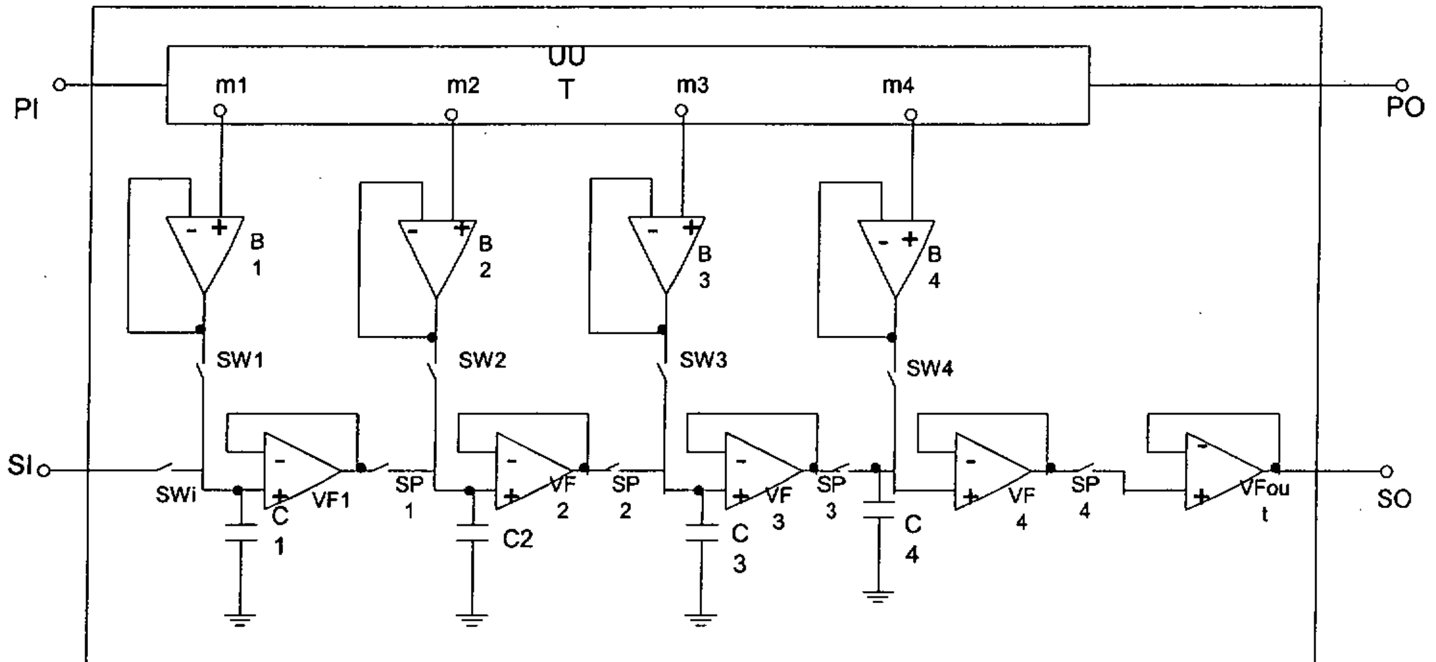

Figure 2.2 An analog BIST structure

2.2.3 Mixed-mode BIST structure

The mixed-mode BIST structure design [3] to enhance the observability is shown in the Figure 2.3. In this the isolation of CUT from the BIST structure is done by using unity-gain analog and digital buffers. Transmission gates T1-T6 are pulled on and off one by one to get analog and digital test point voltages to the output test point i.e. TEST OUT. A preferred clock circuit consists of two-phase static flip-flops (SFF), shown in Figure 2.4. Figure 2.5 shows the timing sequence needed at inputs TEST IN and TCLK to properly switch, one by one, switches T1-T6 on and of

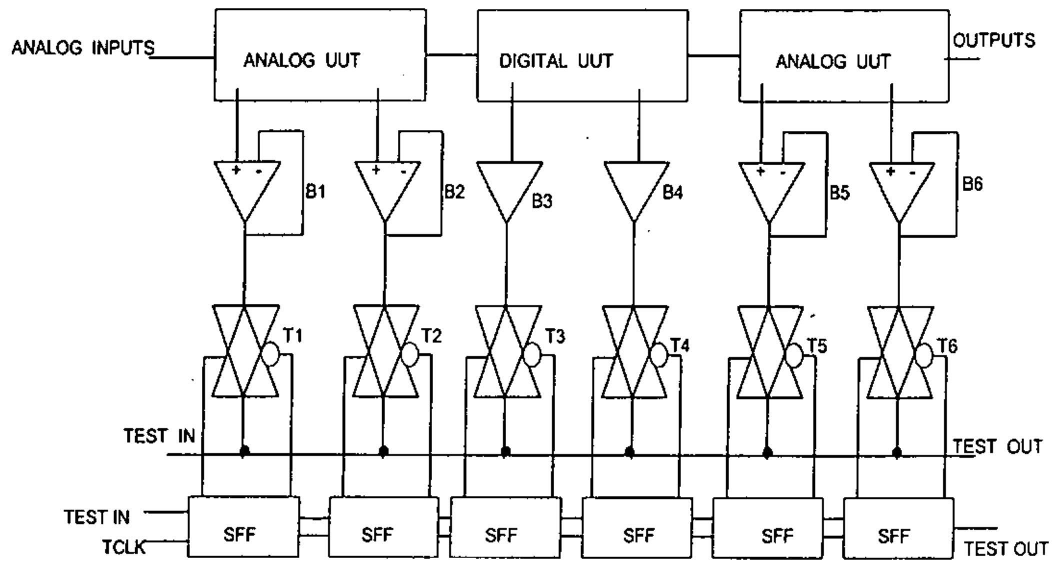

Figure 2.3 Mixed-mode BIST structure for enhanced observability

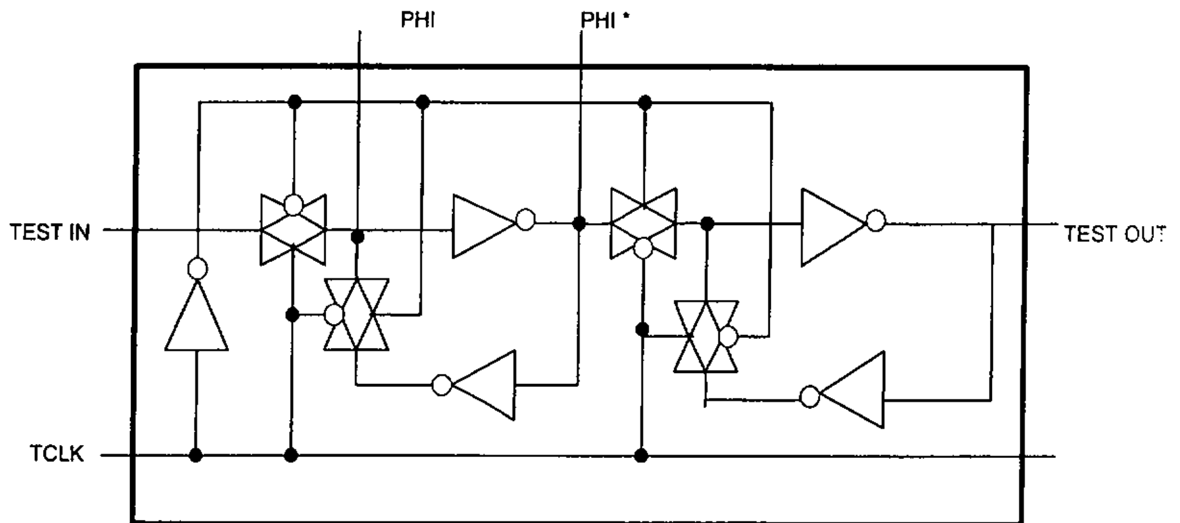

Figure 2.4 Two-phase static flip-flop.

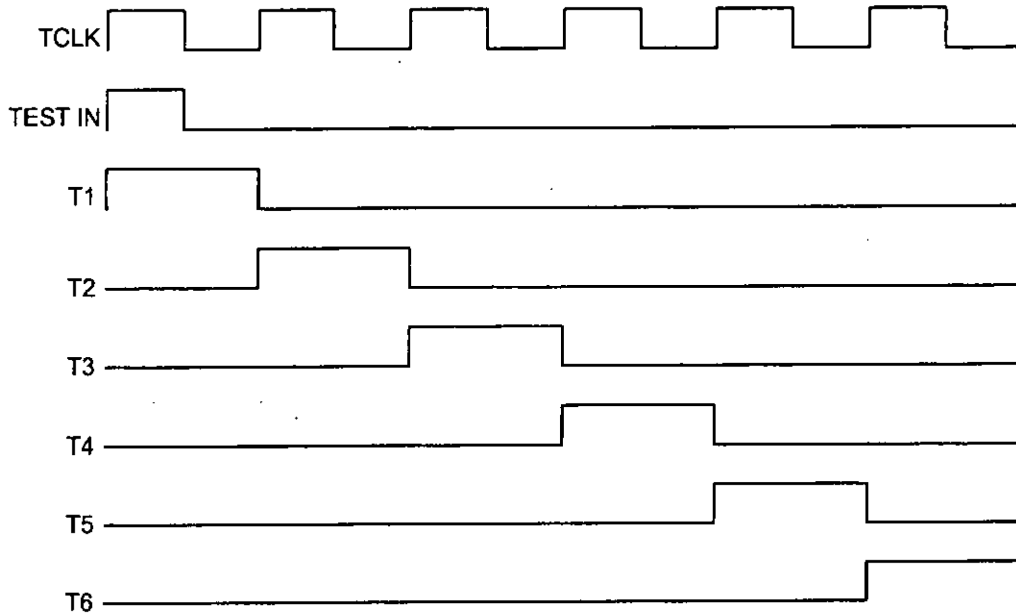

Figure 2.5 Mixed-mode BIST switch timing.

2.2.4 Control and observation structure-1 (COS1)

COS1 is shown in Figure 2.6 in which each stage contains three switches, one analog buffer, one observation, and one control point. These switches are controlled by the inputs D_i, A. Each stage performs one of several functions according to the instructions shown in Table 2.1. Stage-i performs the normal function when D_iA = 0x. If a specific stage receives D_iA = 11, it performs the sampling function. If it receives D_iA = 10, it performs the control function. Only one stage is active at a time, while other stages should receive D_iA = 0x,that is, in normal mode. The above instructions and their functions are shown in Table 2.1.

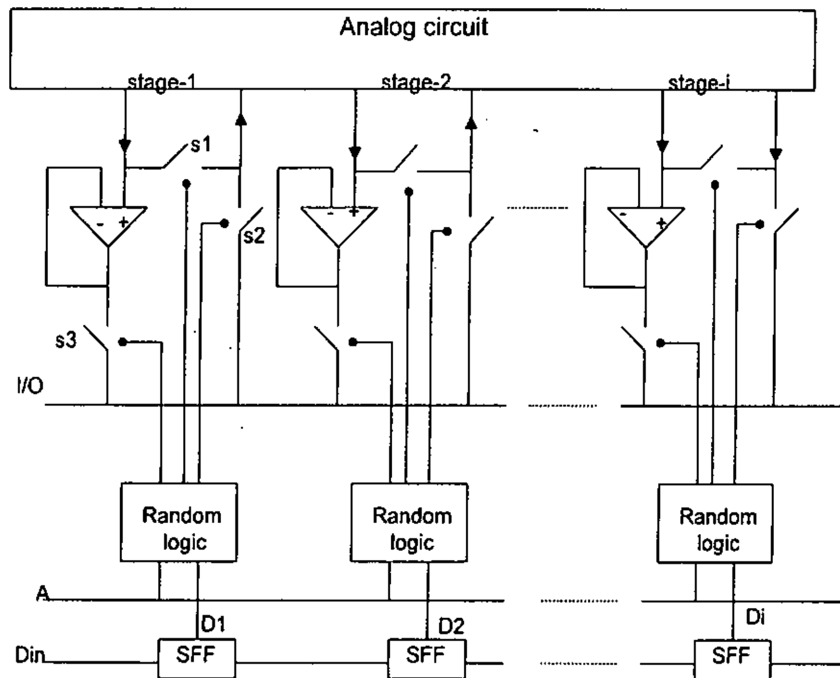

Figure 2.6 Analog control and observation structure COS1

Table 2.1 Functions and signal definitions of modified COS1

Instruction	D_i	A	S_1	S_2	S_3
Normal	**0**	**1**	**1**	**0**	**0**
	0	0	1	0	0
Sample	1	1	1	0	1
Control	1	0	0	1	0

In this COS1 structure , it contains only one bi-directional I/O pad and its function is controlled by the instructions or switch signals (such as A or S_1, S_2 and S_3). For example, we can apply a known dc voltage via this I/O pad if $D_iA = 10$. And we can measure a sampled dc voltage via the same I/O pad if $D_iA = 11$.The Boolean functions of S_1, S_2 and S_3 are $S_1 = A + \bar{D}_i$, $S_2 = \bar{A}D_i$ and $S_3 = AD_i$. The unity-gain buffers are provided in between COS and CUT to reduce the loading effects and to isolate the COS from the CUT. So, this structure is more practical. But it also has one disadvantage, i.e. it does not allow control of all test points simultaneously.

2.2.5 Control and observation structure-2 (COS2)

The second proposed structure, COS2, is shown in the Figure 2.7 that solves the above problem. By using this structure, we can control and sample all test points simultaneously. In COS2, each stage contains five switches, a capacitor (for analog memory) and one I/O-bus (for observation and control purpose). It also performs one of several functions according to the given instruction. Table 2.2 defines COS2's instruction and control signals.

Figure 2.8 shows the SFFs (scan flip-flop) and switch control circuit for COS2. The COS2 performs the normal operation when $D_1 = 0$ and ($AB = 00$ or $AB = 11$) for all stages. In sample mode, all test points are sampled simultaneously by changing the instruction from $ABD_i = 000$ to $ABD_i = 010$ and then all voltages from the test points will be sampled and held on the capacitors C1, C2...Ci simultaneously. Again by changing$ABD_i = 001$, we can read out the voltage levels one by one in the scan out instruction. To control all test points simultaneously, first we scan in the dc voltage of each test point one by one via the I/O terminal, using the scan in instruction. That is, we

set $ABD_i = 111$, insert a 1 into the scan chain, and shift it from one stage to the next. In each step of the shifting, we apply an appropriate voltage from the I/O terminal to the respective test point. Finally we apply $ABD_i = 100$ (control instruction) to control all stages simultaneously.

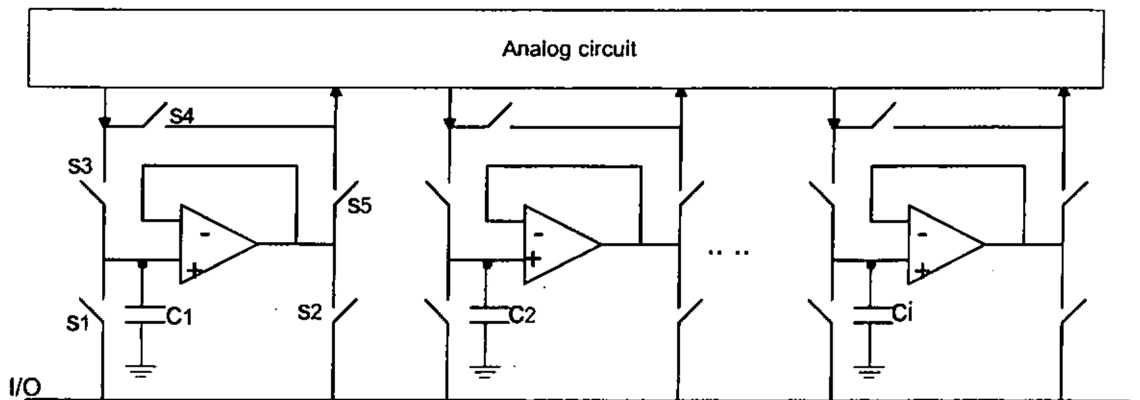

Figure 2.7 Analog control and observation structure COS2

Table 2.2 COS2 functions and signal definitions.

Instruction	D_iAB	S_1	S2	S3	S4	S5
Normal	000	0	0	0	1	0
	011	0	0	0	1	0
Sample	001	0	0	1	1	0
Scan out	100	0	1	0	1	0
Scan in	111	1	0	0	1	0
Control	010	0	0	0	0	1

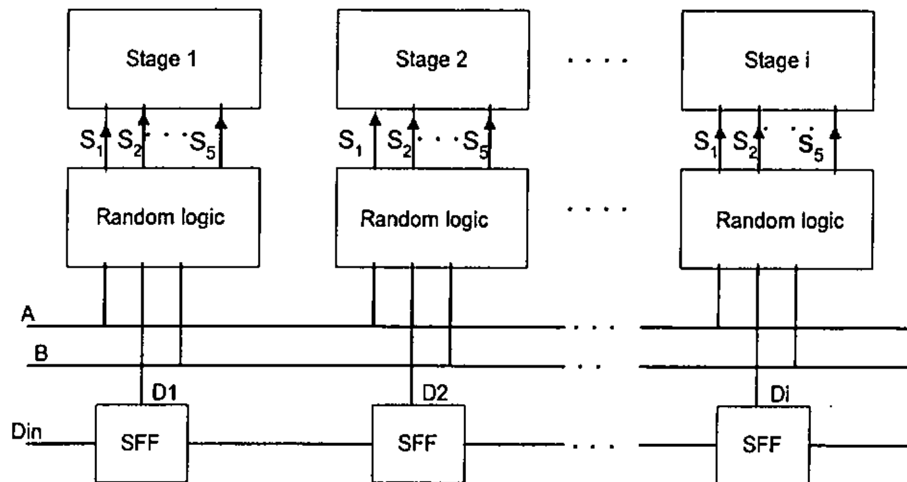

Figure 2.8 SFFs and switch control circuits for COS2

2.3 I_{ddq} testing

2.3.1 Basic concept of I_{ddq} testing

I_{ddq} current is defined as the current that flows in a CMOS integrated circuit when all logic states have settled and are in the quiescent state. For example, a CMOS gate consists of an NMOS pull down network and a complementary PMOS pull up network. In a fault-free situation for any given inputs, only one path conducts, connecting the output node to either the V_{dd} or the GND node. The gate output voltage is well defined at either logic level 1 or 0 and the circuit does not provide a conducting path from V_{dd} to GND. Thus in the fault-free situation, steady state current in the circuit is negligible. The circuit contains only junction leakage current. The magnitude of this leakage current is on the order of nA and for all practical purposes it can be neglected.

In the presence of various physical defects, the steady-state current in the CMOS circuit is raised to higher levels on the order of milli-amps. Thus, by monitoring the power supply current one may determine whether or not a circuit has a fault.

I_{ddq} testing is particularly effective in testing bridging faults, including gate oxide shorts, transistor stuck-on faults and parametric defects. One salient feature of I_{ddq} testing is that the size of the test vectors needed to achieve high fault coverage can be significantly small.

The external I_{ddq} testing is known as off-chip current testing, which can be monitored through the power supply pin of the integrated circuit package. Unfortunately, measurement of small current with very high accuracy and speed is not as simple as voltage measurement. The current measurement unit is required to be inserted in the current path; thus, it causes a voltage drop across it. Also, due to its nature, current measurement is relatively slow and susceptible to static noise in the power supply bus. The instrumentation limitations, such as speed and sensitivity, are serious concerns for external I_{ddq} testing. Since the major portion of I_{ddq} in CMOS integrated circuit is generated at the input/output pad circuits, I_{ddq} abnormalities can be masked by output currents. The large probe capacitances cause a delay in the test time, therefore a 10 to 100kHz testing frequency is used for external I_{ddq} testing. To overcome these limitations, the on-chip current testing has been adopted using a Built-In Current Sensing circuit (BICS).

2.3.2 Off-chip current sensing techniques

In off-chip current sensing techniques, the current sensor is connected externally to CUT to measure the I_{ddq} current. Commercially, some ac as well dc current probes are used externally to measure I_{ddq} current. The current probe can be

used in between the CUT and the power supply as shown in Figure 2.9 . The basic problem with the probing is the insertion inductance that causes voltage drop across it. To avoid that voltage drop, a FET bypass circuit is used in shunt with the sense resistor as shown in Figure 2.10. This bypass transistor is turned on only during the transient period. Thus, when the transient is settled down, the current is passed through the resistor. To filter the high impedance noise at high frequencies, a small capacitor C1 is connected between the sense circuit and CUT. The disadvantage with this method is that it causes a RC loading at the output resulting in more time to stabilize circuit. And this can be more suitable at about 10kHz test frequency.

At the present time an off-chip current sensor has to be tailored with the physical and electrical characteristics of the automatic test equipment. In [29] 1996, Bob Thomas and Rick Andlauer presented an ATE system to measure the I_{ddq} value. This research study was concluded as a reasonable, low cost solution for I_{ddq} testing that was easy to implement, has acceptable speed and offers protection to the DUT during I_{ddq} testing. It is easy to adaptable to ATE systems, which do not have specialized I_{ddq} measurement hardware and software.

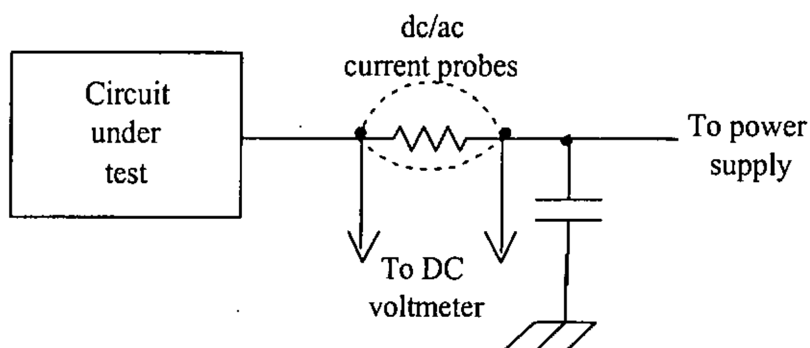

Figure 2.9 Schematics of current measurement technique with dc current probe

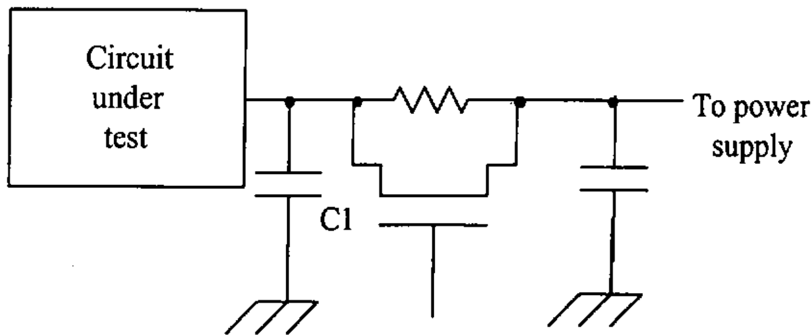

Figure 2.10 Current measurement techniques using external probe

2.3.3 On-chip current sensing circuit

An alternative to off-chip current monitoring, the I_{ddq} testing is done internally in a CUT by built-in current sensing circuits. The BICS is inserted in series with the power supply (V_{dd}) or the ground (GND) of the CUT to detect abnormal I_{ddq} current in integrated circuit. Figure 2.11 shows I_{ddq} testing with BICS inserted in the ground of the CUT. The BICS embedded in the integrated circuit checks the quiescent current is either above or below the threshold level. The existence of defects indicates the voltage drop in BICS.

Current testing using BICS has the following advantages when compared with external I_{ddq} testing.

- Low equipment cost.
- High testing rate.
- Improved delectability and observability of the CUT.
- A higher current sensing resolution.
- Avoidance of the influence of input or output current, which may dominate the total chips current.

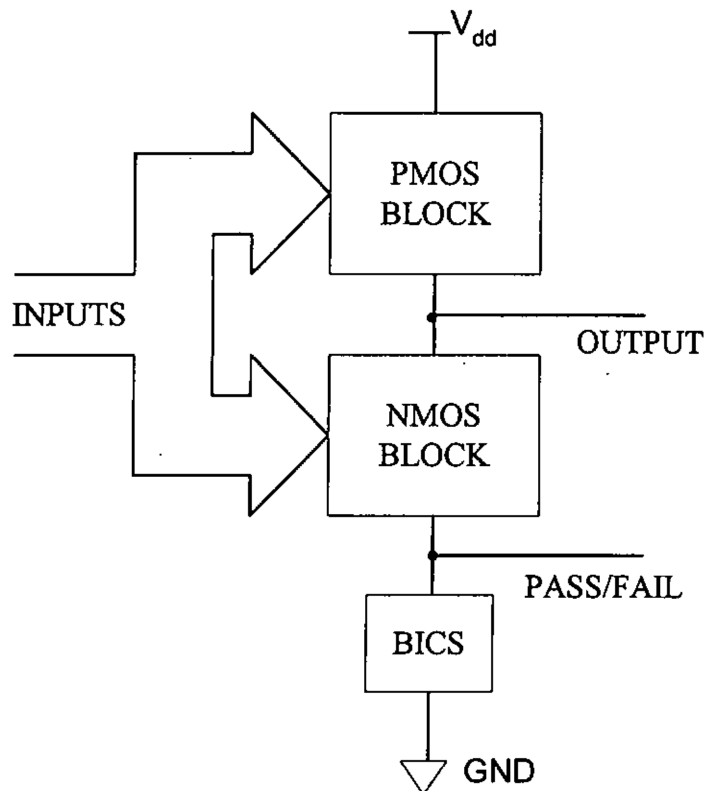

Figure 2.11 Block diagram of I_{ddq} testing

2.3.4 BICS circuits

Despite previous research studies [30-32] on BICS, there are still some drawbacks. For example, the BICS is inserted between the power signal (V_{dd} and GND) and the CUT, a large power level shift is possible, which causes a significant chip area overhead due to the size of BICS.

In 1998, Jeona Beom Kim *et al.* [53] proposed a BICS circuit. This circuit diagram of the BICS is shown in Figure 2.12. An essential element of this BICS is the current mirror circuit. The current mirror has a property that in a constant current stage, the reference current in one branch of the circuit is accurately reproduced or reflected in a second branch. The BICS consists of three NMOS transistors, two PMOS transistors, a constant reference current source and one inverter. The NMOS transistor Q_0 is

operated to switch either to isolate or to connect the BICS to the CUT. In CMOS integrated circuits, the peak I_{DD} current, called dynamic current or current spike, occurs when the inputs are switching, it is difficult to measure the momentary quiescent state current when inputs change. To overcome this difficulty, the TCLK pin that is joined to the gate of NMOS transistor Q_0 is added. The TCLK, control input pin , is connected to the clock of the test machine in the testing mode, and is connected to V_{dd} in the normal mode. When a peak I_{dd} current occurs in the input of BICS, NMOS current mirror pairs, Q_1 and Q_2, have no effect on the dynamic current, since the switch transistor Q_0 is turned on. Therefore, the dynamic current does not affect BICS output. The NMOS current mirror pairs, Q_1 and Q_2, replicate the defective current I_{DEF}. The reference current source. I_{REF}, has a constant current value which determines whether the CUT is defect-free or not. The PMOS current mirror pairs, Q_3 and Q_4 replicate this constant reference current I_{REF}. Drains of the PMOS replicating transistor Q_4 and the NMOS replicating transistor Q_2 are connected to the input of the inverter to generate the pass/fail signal. The constant reference current I_{REF} is the same as the quiescent state current when the CUT is defect-free. Therefore, by comparing I_{REF} with I_{DEF}, the BICS determines whether the CUT is defect-free or not.

Since the BICS is inserted in series with GND of the CUT, it causes a large capacitance between the CUT and the substrate. This capacitance must be charged in a finite time and thus causes an extra delay time to the CUT. These effects, the series voltage and its consequential capacitance delay time, cause the performance degradation and GND level shift. To reduce this undesirable effects the extra pin EXT is added to the BICS circuit. EXT is grounded in the normal mode, and is floating in the testing mode. This BICS has the normal mode and test mode.

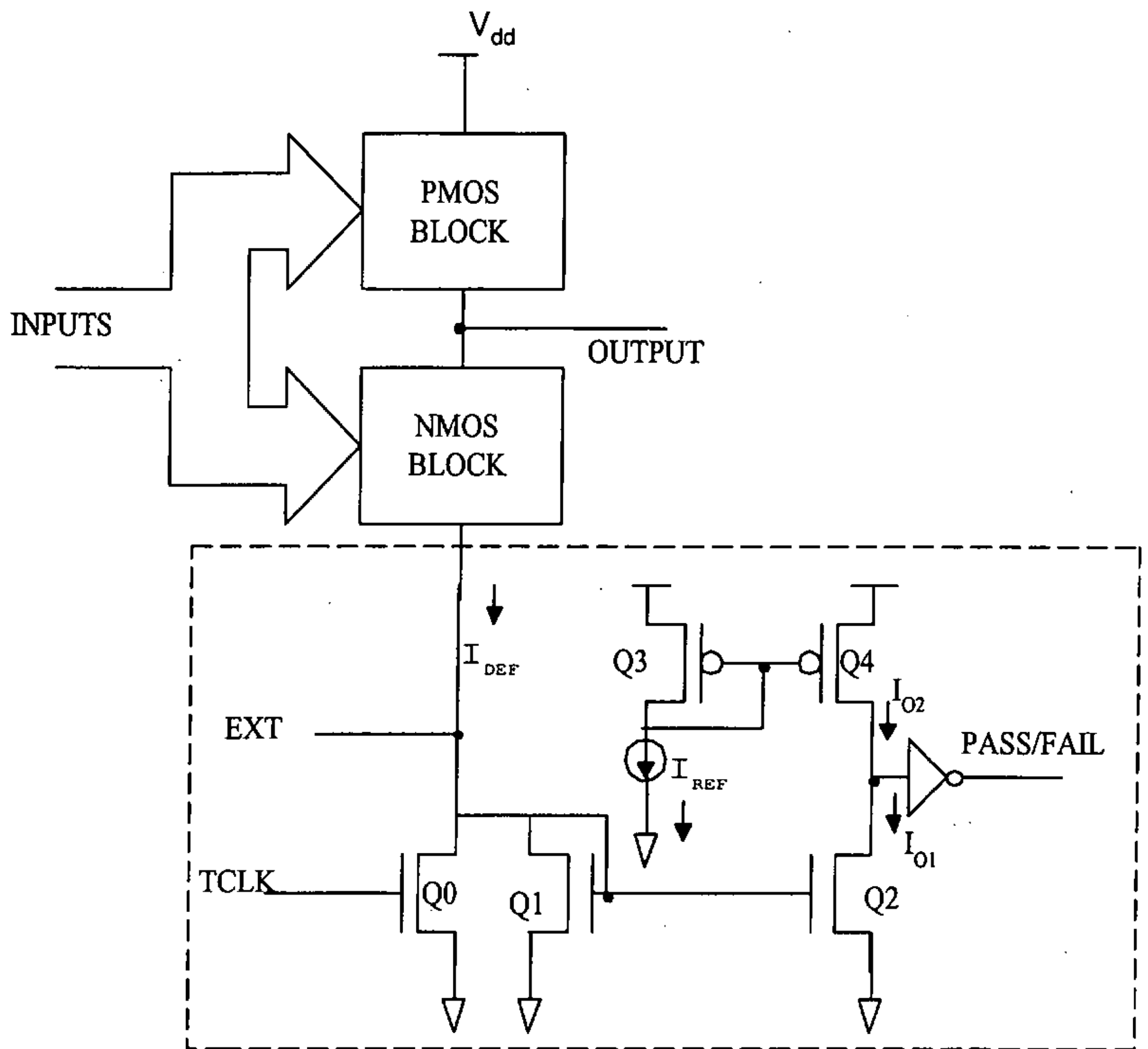

Figure 2.12 BICS circuit connected to the CMOS structure

In the normal mode, the EXT pin is connected to GND and the TCLK pin is connected to V_{dd}. During the normal mode, since the TCLK pin is connected to V_{dd}, the NMOS transistor Q_0 is turned on. Also, since The EXT pin is connected to GND, the NMOS transistors Q_1 and Q_2 are turned off. Therefore, the PASS/FAIL is set to 0, but this output is insignificant in the normal mode. Since the EXT pin is grounded bypassing the BICS, disturbance or level shift during normal operation of the circuit can be ignored.

For defect-free CMOS integrated circuits, there is no conducting path between power supply and ground if no inputs change. The current in CMOS integrated circuit

is not constant throughout the time. When an input or clock transition occurs, a peak I_{dd} current flows between the power supply and the ground. Since this current is envitable, the BICS must ignore this peak current during the Transition State. To prevent the BICS from detecting this peak current, NMOS transistor, Q_0 is used. The test timing diagram is shown in the Figure 2.13. During the input transition, the TCLK is set to 1. Thus the NMOS transistor Q_0 is turned on and the gate voltage of the NMOS transistors Q_1 and Q_2 is nearly 0. Therefore, the NMOS transistors Q_1 and Q_2 are turned off. Then the PASS/FAIL remains 0,which means it does not detect the peak current. When the input transition is settled to the quiescent state, the TCLK is set to 0. Thus the NMOS transistor Q_0 is turned off and the NMOS transistor Q_1 is fed with the defective current IDEF, if it exists. By the current mirror characteristic, the drain current of the NMOS transistor Q_2, I_{O1}, is proportional to I_{DEF}. In the PMOS type current mirror circuit, I_{O2}, taken at the drain of PMOS transistor Q_4, is proportional to I_{REF}. Therefore $I_{O1}= I_{DEF}$ and $I_{O2}=I_{REF}$ the circuit is defect-free, I_{DEF} is less than I_{REF}. Therefore, the BICS is sets the PASS/FAIL to 0.When the CUT is defective, I_{DEF} increases and is greater than I_{REF}. Therefore, the BICS sets the PASS/FAIL to 1.

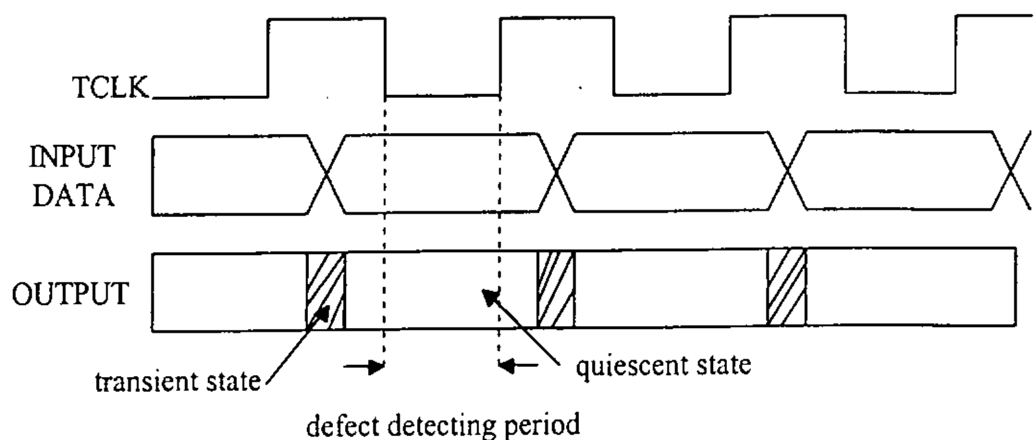

Figure 2.13 Timing diagram of the chip.

2.3.5 The advantages and disadvantages of on-chip testing

Advantages:

1. The major advantage of an on-chip current sensor is that I_{ddq} can be implemented as built-in self-test, because of on-chip current sensing, the large inductive circuit is avoided.
2. On-chip I_{ddq} testing can be performed at a much higher speed compared to the external current sensing.

Disadvantages:

1. The size of an on-chip current sensor is large and it causes significant area overhead.
2. An on-chip current sensor complicates the chip design because of its partition requirement.

Due to the above disadvantages, on-chip current sensors, at present, have only been used in the laboratories but not in production testing.

2.4 Macro-based DFT

Recent research efforts have concentrated on developing macro-specific DFT techniques. Macro-specific techniques reduce overhead costs by exploiting the unique characteristics of either the functionality or the structure of the target macro. A system-level DFT scheme can be formed by combining macro-level DFT schemes. Operational amplifiers, data converters and filters are the most popular macros in mixed-signal IC's. There are two types of macro-based DFT schemes:

- Code-based DFT
- Reconfiguration-based DFT

2.4.1 Code-based DFT

This approach is used for self-checking analog and digital circuits that provide on-line error detection [48,49]. The general structure of a self-checking circuit is shown in Figure 2.14. A digital logic circuit is modified such that its outputs are encoded. An on-line checker is used to verify that the outputs obey the code. A non-codeword at the output of the functional circuit indicates the fault in the circuit.

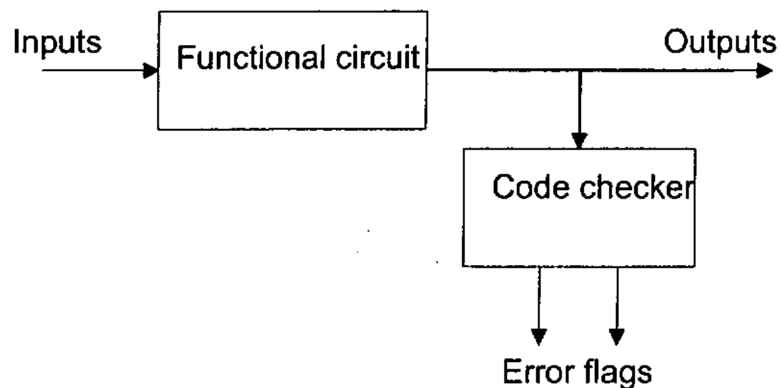

Figure 2.14 A self-checking circuit: general structure

Case study: Fully differential op-amp with two conjugate outputs that makes the path for signal propagation is used for demonstration. Fully differential analog code (FDAC) is used to encode the on-chip data. On-chip code checker, rather than off-chip instrumentation, can be used at the output of the amplifier to verify that the data code is not corrupted. A single fault inside the op-amp will effect only one of the two signal propagation paths. The common mode component of the output FDAC will be altered by the fault. A code checker at the output of the op-amp is triggered whenever the common mode component of the output FDAC greater or less than some threshold

value of a fault-free component. Then it detects the fault within the op-amp. With this technique the area overhead is limited by using simple codes.

2.4.2 Reconfiguration-based DFT

In this technique a system's testability can be improved by incorporating the ability to modify the circuit into more than one configuration during test. In the normal configuration, the circuit performs its normal function and in the different test configurations, the function is modified in order to increase the testability of the system. This is used to improve the testability of the analog and mixed-signal circuits. There are many testing methods that fallow the reconfiguration-based DFT technique, but two are mentioned below:

- current based test
- Oscillation based test.

In these two approaches the feedback structure around an in-circuit op amp during test is altered.

Current based test: A reconfiguration technique for current based test is suggested in [50]. The op-amp is tested for catastrophic faults by using this test method. In normal mode the op-amp is shown in Figure 2.15 (a) and in test mode the op-amp is configured as a source follower using additional switching circuitry is shown in Figure 2.15 (b), the output voltage at the op amp is essentially the offset voltage. The current from the power supply is determined by the offset voltage and the resistor R. It was determined that the offset voltage in majority of the faulty op amps was substantially higher than the offset voltage in a good op amp. Thus faulty op amps draw more current from the power supply.

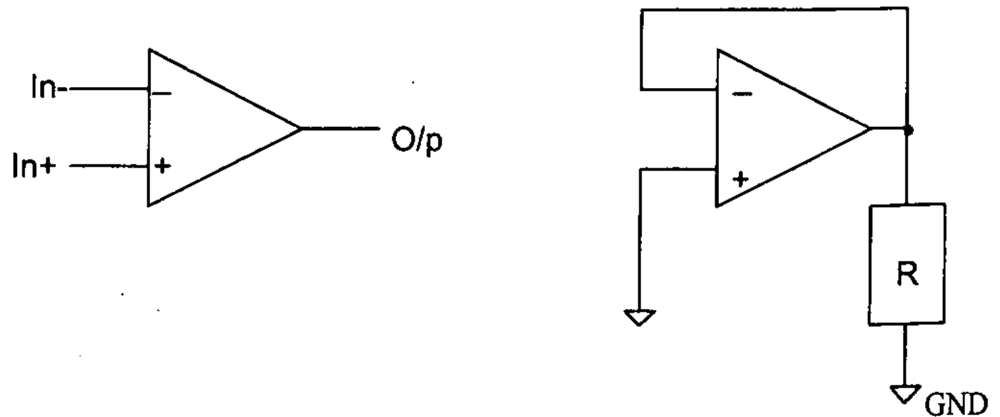

Figure 2.15 (a) op-amp in normal mode and 2.15 (b) Op amp configured as a source follower.

Oscillation based test: In this approach, feedback circuitry is added to an op amp in the test mode such that the resulting circuit is an oscillator. The oscillation frequency is determined by the circuit parameters such as the gain of the op amp, the unity gain frequency, and the values of the passive components. The core idea in the approach is that a fault in the op amp, or indeed in any component, will either prevent the circuit from oscillating or alter the oscillating frequency. The details about this method are mentioned in following chapter.

Chapter 3

Oscillation Test Methodology

3.1 Introduction

Due to the rapid developments in integrated circuit technology and market requirements, the trend of designing mixed-signal ASICs has been increased. The most important problem in designing mixed signal ASIC is the testing of analog portion of the circuit. Unlike the digital systems, the specifications of analog circuits are usually very broad which result in long testing time, poor fault coverage, and the requirement of dedicated test equipment.

Testing analog circuits can be accomplished using functional (and/or parametric) testing [1,2,3,4], power supply current (I_{ddq}) monitoring [7,8] and digital signal processing techniques. Various designs for testability techniques have been used in conjunction with the mentioned test methods to increase the controllability and observability and to simplify the test problem. The above mentioned methods depend on the selection of suitable test vectors to estimate their effectiveness. However, the generation of optimal test vectors assuring high fault coverage becomes critical as the complexity of the CUT increases. Built-In Self-Test (BIST) structures based on the existing test methods require the use of specialized input stimuli generation and output evaluation hardware, which introduce a significant area overhead and it is time consuming. The above-cited problems like large area overhead, long testing time, and difficulties in test vector generation are overcome by the newly developed oscillation test method (OTM).

3.2 Overview of the oscillation test methodology (OTM)

The oscillation test method for analog and mixed-signal circuits is based on transforming the CUT to an oscillator [51,26,27]. Using this method, the complex analog circuit is partitioned into functional building blocks such as: amplifier, operational amplifier, comparator, schmitt trigger, filter, phase lock loop (PLL), etc., or a combination of these blocks. During test mode, by adding some additional circuitry, each building block is converted to a circuit producing sustained oscillations. The oscillation frequency f_{osc} of each building block can be expressed either as a function of its components or as a function of its important parameters. The building blocks that generate inherently a frequency, such as oscillators, do not need to be rearranged, and their output frequency is directly evaluated. The simplified test structure of the oscillation-test strategy is shown in Figure 3.1. In test mode, the CUT is divided into building blocks that are converted to oscillators using additional circuitry. An analog multiplexer (AMUX) selects the output of selected building block, and its oscillation frequency is externally evaluated using test equipment. The functionality of the test structure is verified by activating the self-test (STest) signal before starting the test procedure. All these operations are managed using the control logic (CL). Existing faults in the circuit-under-test (CUT) related to components (or parameters) that are involved in the oscillator structure manifest themselves as a deviation of the oscillation frequency. Therefore, the deviation of the oscillation frequency from its nominal frequency or loss of oscillations indicates possible faults in the CUT. The oscillation test method reduces the test complexity, area overhead and testing time by avoiding the test vector generator and output evaluator in test circuitry.

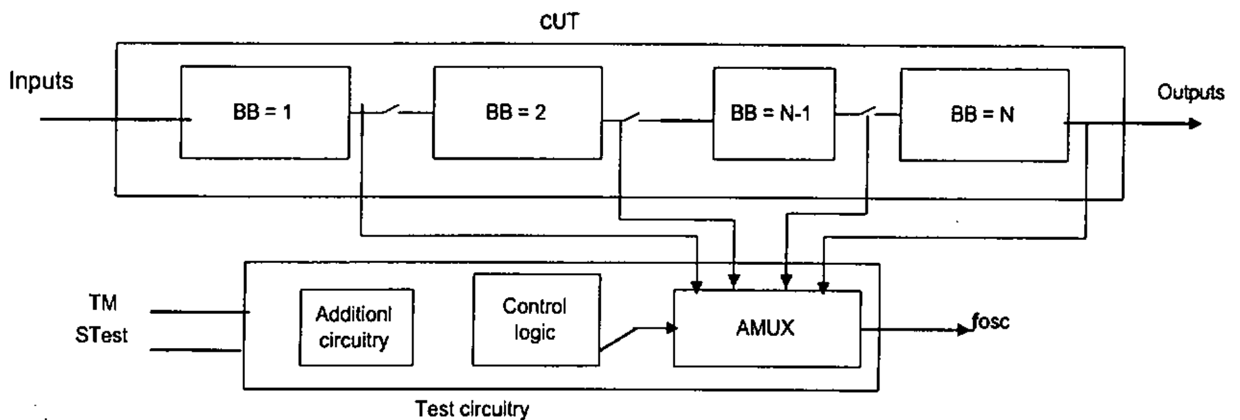

Figure 3.1 Simplified test structure of the oscillation-test strategy

Two frequently used DFT techniques to transform an analog and mixed-signal circuit to an oscillator in test mode. These techniques are described below:

(a) The technique employed to rearrange CUT to an oscillator is first to convert it to a bandpass system having a greater than unity gain within its passing band, and then establish a positive feedback by simply connecting the output to the input. As a result, the existing noise is bandpass filtered and amplified in the loop, and produces an oscillating signal. The oscillation frequency is determined by the bandwidth and the gain of the system. As the amplifier is a low-pass system, by cascading a simple high-pass RC filter, it becomes a bandpass system, which can be converted to an oscillator by feeding back its output to its input is shown Figure 3.2. The discrete bipolar amplifier consists of six transistors with 32 nodes represented on it. In order to determine the fault coverage, all open and short circuit faults are injected. The majority of injected faults resulted in the absence of oscillations and this was concluded that 100% of injected faults are detectable by the output frequency evaluation.

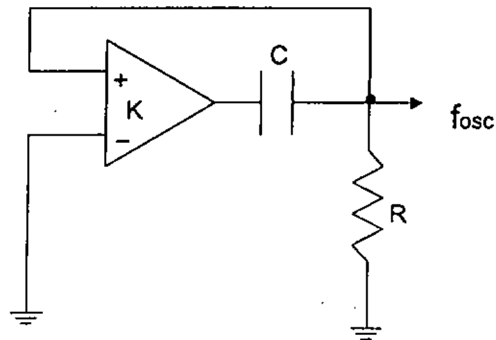

Figure 3.2 Single bipolar amplifier oscillator in test mode

(b) In the second technique [27] the CUT is converted into an oscillator by adding feedback block. A feed back amplifier with more than two poles can become unstable and break into oscillation if too much feedback is applied. Sinusoidal oscillators are analyzed as special case of feed back amplifier, which are intentionally rendered unstable. According to the Barkhausen Criterion the frequency at which a sinusoidal oscillator will operate is the frequency for which the total shift introduced, as a signal proceeds from the input terminals, through the amplifier and the feedback network, and back again to the input, is precisely zero.

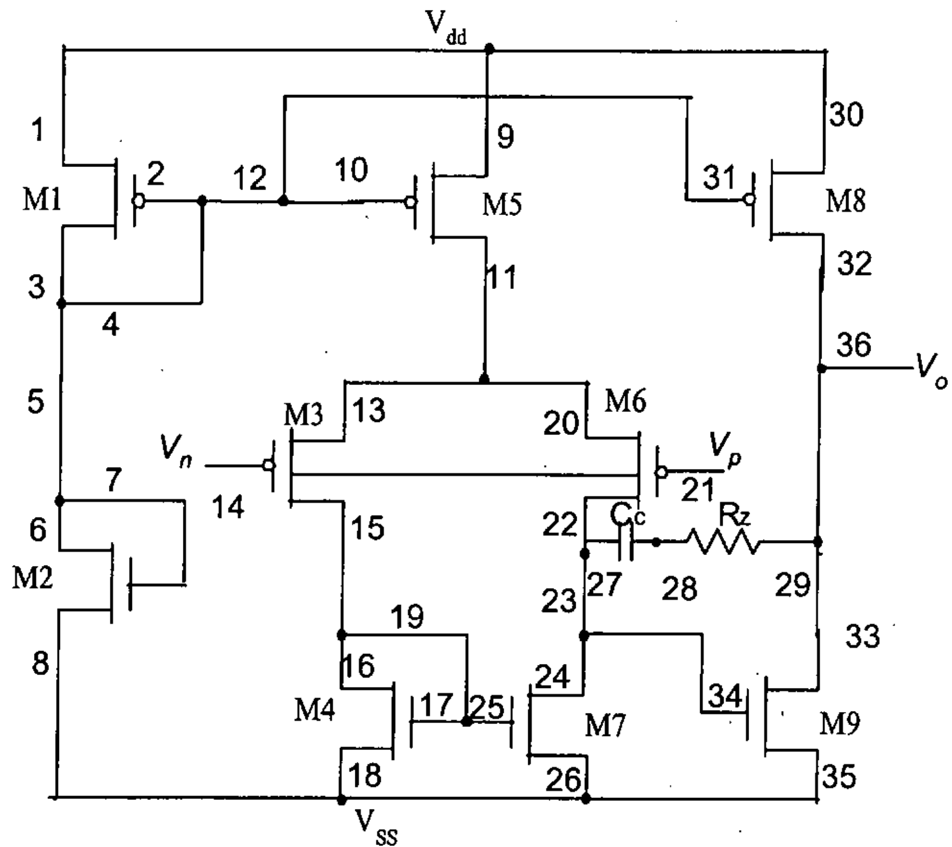

Figure 3.3 Compensated CMOS operational amplifier

Case study: The above technique is demonstrated on a single op-amp (OA)

Figure 3.3 shows the schematic representation of a two stage CMOS OA that is consider as the CUT. The op-amp is compensated and since it is designed for on-chip application, it is unbuffered. Capacitor C_c and R_z constitutes the compensation circuit.

The unity-gain bandwidth of the OA is calculated as follows:

$$w_T = 2\pi fT = a_v p_1 \tag{3.1}$$

As the OA is compensated, its transfer function can be approximated to a single-pole transfer function given by

$$a_v(s) = \frac{a_v}{1 - \frac{s}{p_1}} \tag{3.2}$$

where a_v is the DC open loop gain and P_1 represents its dominant pole.

In this case study both positive and negative feedback loops have been added to the op-amp to convert into a sinusoidal oscillator. The positive feedback loop consists of a RC delay and the negative feedback comprises a voltage divider that is shown in Figure 3.4. To facilitate the mathematical analysis, the combination of feedback loops is presented by a single negative feedback block in which the positive feedback appears as a term with a negative sign. The feedback block converts the OA under test to a second-order system, which has the potential of oscillation.

The new transfer function is derived as follows

$$A_v(s) = \frac{a_v(s)}{1 + a_v(s)f(s)} \tag{3.3}$$

For the condition of oscillator, the voltage at inverting input V- is slightly higher than the voltage at non-inverting input V+, we have

$$f(s) = (V-) - (V+) \tag{3.4}$$

Then

$$f(s) = G - \left(\frac{-s/p_2}{1 - s/p_2} \right) \tag{3.5}$$

In which $G = R_2 / (R_1+R_2)$ and $p_2 = -1/RC$. Substituting f(s) into $A_v(s)$. We obtain

$$A_v(s) = \frac{a_v p_1 (p_2 - s)}{s^2 + ((1-G)a_v p_1 - (p_1 + p_2))s + (Ga_v p_1 p_2 + p_1 p_2)} \tag{3.6}$$

The system poles are obtained by equating the denominator of the new transfer function to zero. In order to construct an oscillator from this new transfer function, its poles must be placed on the imaginary axis on the s domain by forcing the coefficient of the term s to zero, which is realized by proper selection of the value of G, which results in

$$((1-G)a_v p_1 - (p_1 + p_2)) = 0$$

$$G = 1 - \frac{p_1 + p_2}{a_v p_1}$$

The natural oscillation frequency for the new system is given by

$$w^2{}_{osc} = Ga_v p_1 p_2 + p_1 p_2 = a_v p_1 p_2 - p_2{}^2$$

The oscillation frequency depends strongly on important characteristics of the OA under test, which are determined by all components of the OA. Existing faults in the OA will deviate its characteristics from their nominal value, which can be monitored by observing the oscillation frequency. In order to evaluate the testability of the proposed techniques, the process of introducing shorts and opens at devices is used with five faults per transistor. Faults such as circuit node opens and shorts between different nodes of the CUT are also injected. Thirty-six different nodes are identified on

the OA schematic. Note that some nodes that seem schematically redundant such as 8,18, 26 and 35 are not physically redundant. The total number of 657 faults, consisting of 27 open faults and 630 short circuit faults (C_2^{36} = 36! / 2! (36-2)!) is used as the fault dictionary for the op-amp under test. In this particular case, the majority of injected faults resulted in a loss of oscillation and these faults cannot distinguish. From the results observed by the simulation, it concluded that the fault coverage is high, but the fault diagnostic resolution is poor because of large number of indistinguishable faults.

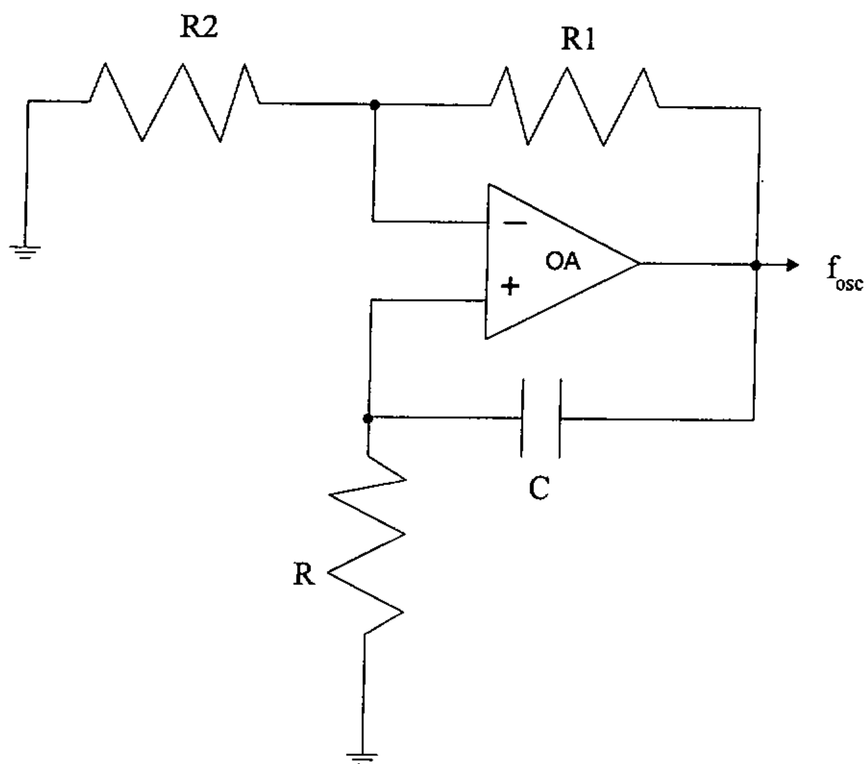

Figure 3.4 Single op-amp sinusoidal oscillator.

3.3 Conclusion

From the results of the case studied, it is concluded that the OTM offers a number of unique advantages which are mentioned below:

- There is no need of test vector in this test method, therefore test vector generation problem is eliminated
- The test time is very small because a limited number of oscillation frequencies is evaluated for each circuit under test.
- Due to its digital nature, the oscillation frequency can be easily interfaced to boundary scan.

Apart from above advantages, it can also offer high fault coverage and easy to implement. Because of the above characteristics, oscillation-test strategy is very attractive for wafer-probe testing as well as final production testing. The major weakness of these methods is the poor ability to perform fault location. Therefore despite the advantages mentioned above OTM remains practically difficult to use as an efficient fault diagnostic tool.

3.4 Objectives of the work

The objective of the research is the development of BIST structure for analog and mixed signal circuits based on a combination of the oscillation-based testing technique, power supply current measurement technique, and other techniques to be described in the following chapters. The OTM technique is used to obtain high fault coverage with the advantage of being easily implemented and less testing time, while the other techniques provide a comprehensive fault identification procedure to achieve effective fault location. In addition to the above techniques, a design and construction

of control and observation structure is added for node voltage measurement (NVM) at different nodes of the circuit under test mode. This NVM approach is used to further improve the fault diagnostic resolution of combined OTM and PSC measurement. One of the major objectives in this work is to enhance the fault isolation resolution to the component level. Current work is focused on the fault diagnosis of the threshold detector circuit of a telephone tone ringer IC. It is envisaged that the procedure formulated in this exploratory development phase will be beneficial and applicable to the test development of future mixed-signal IC designs.

Chapter 4

Fault diagnosis of threshold detector circuit using OTM and power supply current methodology

4.1 Introduction

Diagnostic resolution is the one of the most important parameters in calculating the efficiency of the testing techniques. With previous research studies, it was concluded that with OTM, the diagnostic resolution was poor. To increase the diagnostic resolution, i.e efficiency of the testing and fault coverage, we propose a new testing approach which is based on a combination of the oscillation-based testing technique and power supply current measurement technique for testing of the threshold detector block of Motorola's MC34017 Telephone Tone Ringer IC. The former technique is used to obtain high fault coverage with the advantage of being easily implemented, while the latter technique provides a fault identification procedure to achieve effective fault location.

One of the major objectives of above approach is to enhance the fault isolation resolution to the component level. Current work is focused on the fault diagnosis of the op-amps and the logic gates used in the detector block.. It is envisaged that the procedure formulated in this exploratory development phase will be beneficial and applicable to the test development of future mixed-signal IC designs.

4.2 The MC34017 tone ringer chip

The block diagram of the MC34017 Tone Ringer chip is shown in the Figure 4.1. The chip derives its power supply by rectifying the ac ringing signal. It uses this power to activate a tone generator and drive a piezo-ceramic transducer. The tone generation circuitry includes a relaxation oscillator and frequency divider, which produce high and low frequency tones as well as the tone warble frequency. According to the specification data, the relaxation oscillator frequency f_o can be set by resister R_2 and capacitor C_2 connected to pin RC. The oscillator will operate with f_o from 1.0kHz to 10kHz with the proper choice of external components.

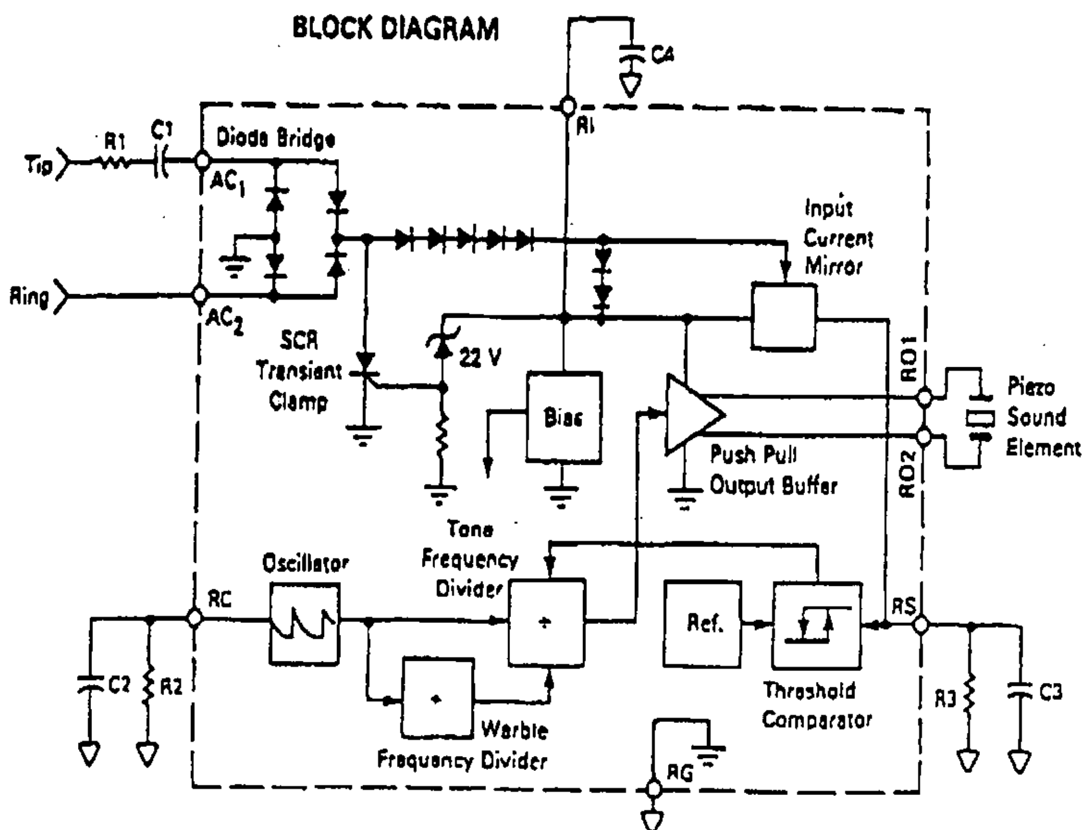

Figure 4.1 Block diagram of the MC34107 tone ringer chip.

Input signal detection circuitry activates the tone ringer output when the ac line voltage exceeds programmed threshold level. Resister R_3 determines the ringing signal amplitude at which an output signal at RO1 and RO2 will be generated. The ac ringing signal is rectified by the internal diode bridge. The rectified input signal produces a voltage across R3, which is referenced to RG. The voltage across resistor R3 is filtered by capacitor C3 at the input to the threshold circuit. When the voltage on capacitor C3 exceeds 1.27 volts, the threshold detector enables the tone ringer output.

4.3 The threshold detector block

The block diagram and the corresponding circuit schematic of the threshold detector section with nodes identified and labeled are shown in Figure 4.2 and Figure 4.3. The threshold detector forms part of a test development chip (currently under development) which is targeted for next generation telecommunication applications. The fabrication process used is based on BiCOMS technology. The threshold detector design is similar to the one used in the MC34017 Tone ringer chip. Basically, the detector consists of a threshold comparator and a reference generator. In order to make the comparator less sensitive to noise, hysteresis technique is employed. The amount of hysteresis is defined by the difference of the two reference levels. These reference levels are referred to as the REF_LOW (0.4-volt) and the REF_HIGH (1.27-volt). The two operational amplifier outputs are connected to a latch, which consists of a 2-input NOR gate, a 2-input NAND gate and a simple 1-bit memory gate. So that a chain of positive pulses will be generated to activate the tone ringer output whenever the DET input line voltage exceeds the programmed threshold level.

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Motivated by the fact that the threshold detector block comprises both analog circuits and digital logic gates, we have reconfigured and solved the diagnostic problem in a manner that makes it considerably easier to deal with the question of implementation. Under test mode, the threshold detector circuit is transformed into a ring oscillator by selecting the 'built-in' switch positions. The block diagram and the circuit schematic of the threshold detector under test mode, by assuming all switches are ideal, are shown in Figures 4.4 and 4.5 respectively. For clear understanding, the block diagram of the detector circuit with switches is shown in appendix-A.

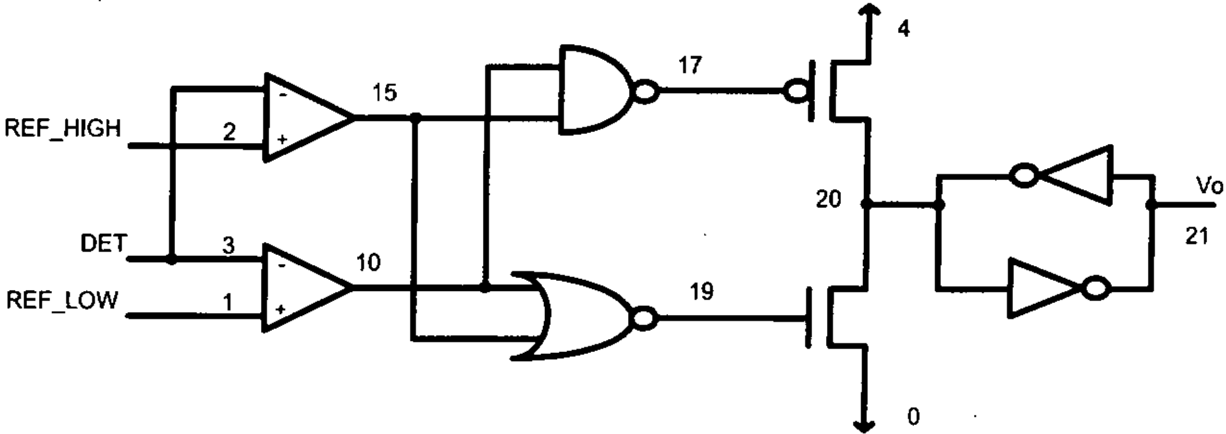


Figure 4.2 Block diagram of the threshold detector circuit

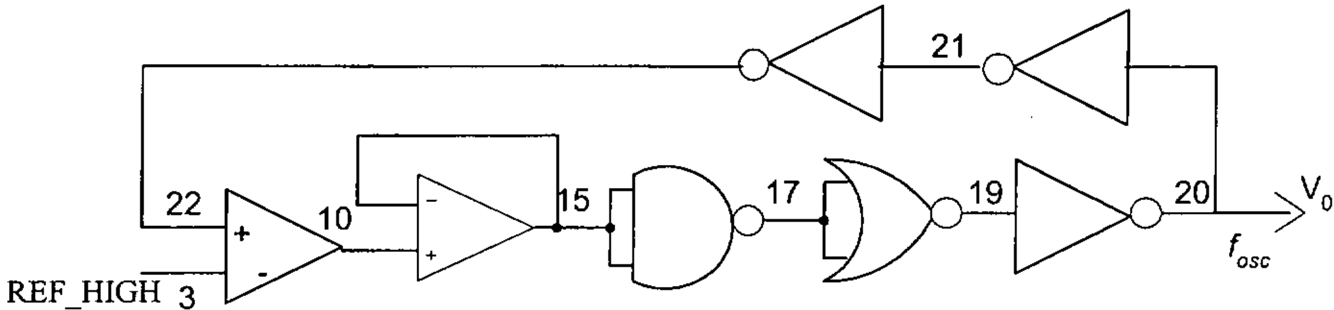


Figure 4.4 Block diagram of the threshold detector in test mode.

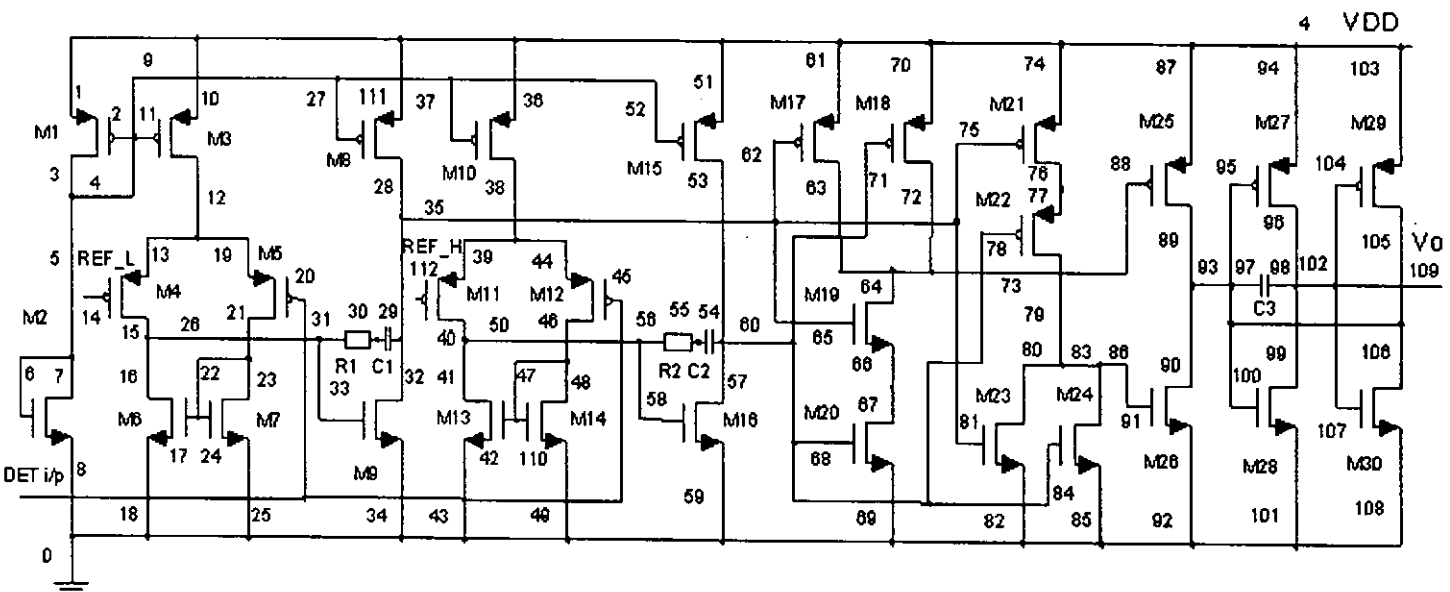


Figure 4.3 Circuit schematic of the threshold detector section.

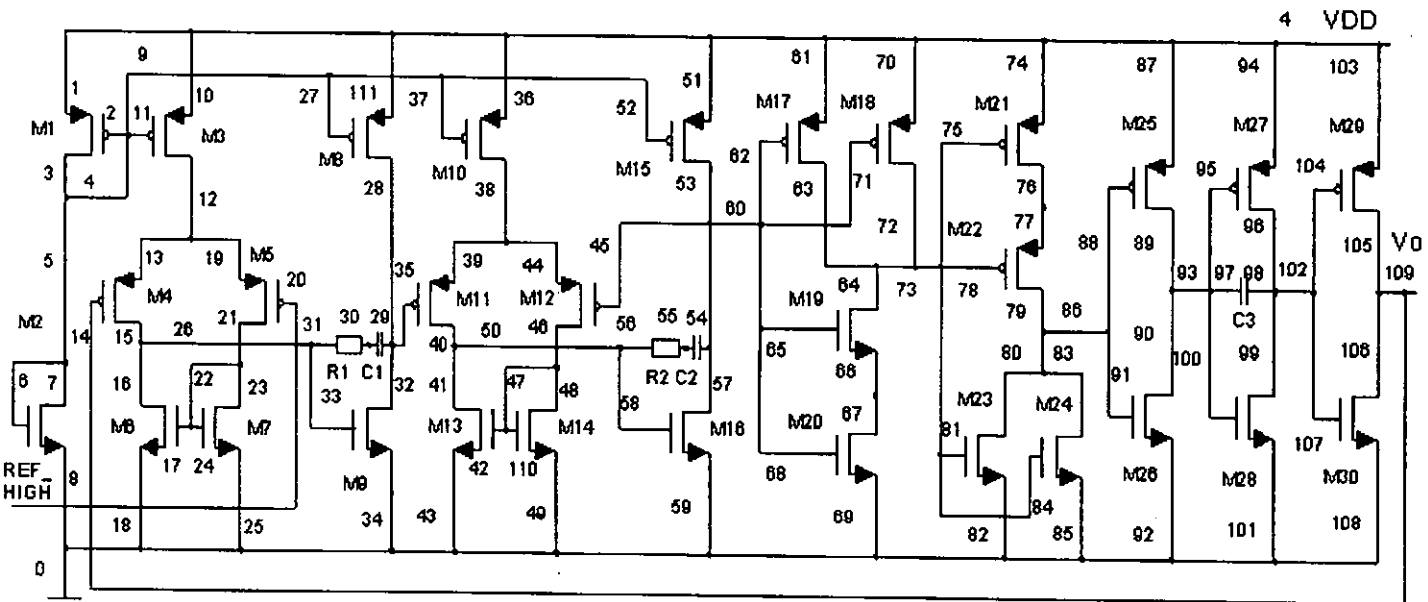


Figure 4.5 Circuit schematic of the threshold detector under test (oscillator) configuration.

4.4 Application of OTM to the test circuit

The oscillator shown in the Figure 4.4 is a ring oscillator implemented using op-amps and digital logic gates of the CUT (i.e. the detector circuit of the telephone tone ringer IC). The first op-amp is a non-inverting amplifier, the second is a voltage follower and logic gates are connected to form a string of inverters. These inverters, which are in odd number of stages, introduce a phase shift of 180° to the input. The oscillation frequency is equal to the inverse of the sum of the delays introduced by the two op-amps and the five inverters, therefore it can be estimated by

$$f_{osc} = 1 \Big/ \left[\sum_{i=1}^{2} PD_{OAi} + \sum_{j=1}^{5} PD_{INVj} \right] \tag{4.1}$$

where PD_{OAi} and PD_{INVj} represent the propagation delays of the op-amps and inverters respectively. As the op-amp operate as comparator in linear and non-linear region of the transfer function, the propagation delay must be determined using a large signal analysis. Each op-amp is equivalent to a two-stage comparator with capacitive load as shown in Figure 4.6. The total propagation delay of an op-amp equals the sum of the delays of each stage.

The delay for each stage is defined as the time it takes for its output voltage V_{DO} (which is shown in Figure 4.6) to make the transition from its quiescent state V_{QS} to the trip point V_{TRP} of the following stage. The trip voltage of a stage is approximated by the input voltage required for the current of its output switching transistor (in saturation) to equal the bias current of the transistor. The propagation delay of each stage can be characterised by

$$PD_{DN} = (V_{QS_N} - V_{TRP\,N+1})\frac{C_{TN}}{I_{SS\,N}} \tag{4.2}$$

where C_T represents the sum of charge, parasitic, and compensation capacitance seen at the output of the stage and I_{SS} is the current available to charge or discharge the capacitance C_T. More details about the estimation of the propagation delay and transistor-level analysis is found in [43]. It can be concluded that the propagation delay contributed by each op-amp depends on all its internal components and therefore the propagation delay has the potential of fault detection.

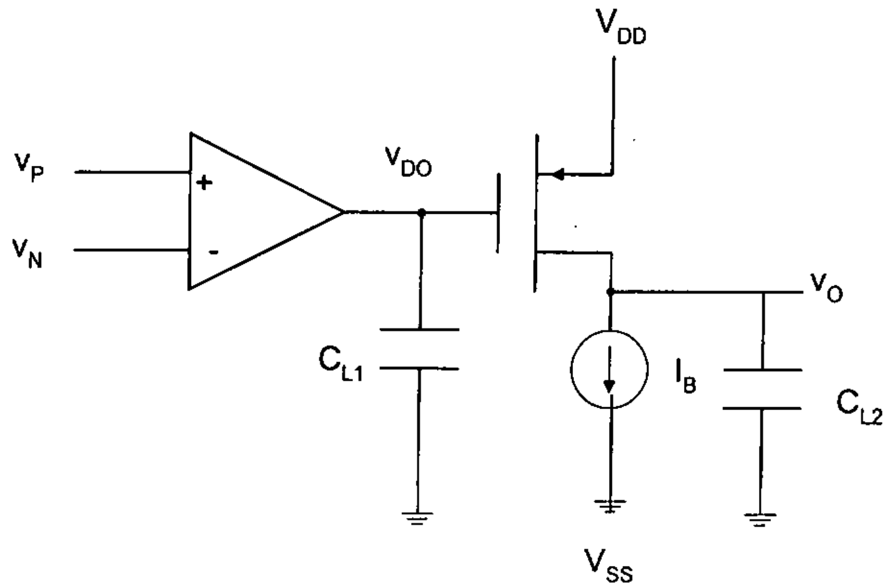


Figure 4.6 Equivalent circuit for two-stage compactor with load capacitance.

4.5 Simulation procedure for detector circuit in test mode

For integrated analog circuits, faults can be classified into either catastrophic or parametric [45,46]. Research results claim that 80-90% of observed analogue faults are

catastrophic faults, which consist of shorts or opens in diodes, transistors, resistors, and capacitors [27]. Moreover, the yield losses in CMOS process are primarily due to catastrophic faults [45]. Table 4.1 shows the probability of occurrence of faults of a MOS transistor [27,52] in a CMOS process.

Table 4.1 Occurrence Probability of CMOS Faults

Class	Device failures	Interconnect failures
Most likely	Gate-drain short Gate-source short	Short between diffusion lines
Less likely	Drain contact open Source contact open	Aluminum polysilicon Cross-over broken
Least likely	Gate-substrate short Gate contact open	Short between Aluminum lines

As reported in previous literature there have been two main approaches to produce a catastrophic fault list. The two approaches are:

- If the layout is available, the defect size and frequency distribution of the manufacturing process can be modeled using a Monte Carlo defect simulator that places missing or extra material in a given layer of a layout and extracts the impact on circuit topology [46].
- If the layout is not available, a fault list may be generated from a schematic. The faults under consideration consist of broken wires, gate-drain shorts, etc.[45].

In considering the schematic diagram of the detector circuit under test mode as shown in Figure 4.5, all possible open and short circuit faults excluding gate contact open faults are considered. There are thirty transistors in the circuit diagram and a total of 111 nodes are identified on the schematic diagram. In that some nodes are

schematically redundant such as 18, 25, 34, 43, 49, 59, 69, 82, 85, 92, 101, 108 are not physically redundant. The total number of 6186 faults, consisting of 81 open faults and 6105 short faults ($C_2^{111} = \frac{111!}{2!(111-2)!} = 6105$) is used as the fault dictionary for the circuit under test.

Although there are 6105 short faults in the dictionary, only 112 faults are considered as short circuit faults because of redundancy and less probability of short circuit between far-end branches in a component level. In these 112 short circuit faults, 41 are gate level faults and 71 are component level faults. The simulation work is carried out using SPICE in two separate phases.

In phase 1, the simulations have been done on detector circuit in test mode, which is shown in the Figure 4.4. For each injected short circuit and open circuit fault, the oscillation frequency or loss of oscillation is recorded and analysed.

In phase 2, PSC approach is applied to distinguish those faults, which caused no oscillation during the phase-1 test. The power supply currents corresponding to each one of these faults are recorded and analysed.

4.5.1 Fault modeling of threshold detector

The catastrophic faults considered in this study comprise all possible open faults at all circuit nodes excluding the transistor gate-terminal open faults. As for short circuit faults, our consideration is influenced by the fact that the circuit is a standard-cell-based design rather than a full-custom approach. Therefore, the total number of short circuit faults are grouped into two levels: level-1 faults comprise short circuit of the interconnections at the individual functional blocks (operational amplifiers) and

logic gates level; and level-2 faults comprise all short faults at individual components level, i.e. all inter- and intra-transistor faults within each operational amplifier and each logic gate. The faults are injected one at a time, multiple fault injection is not considered in this experiment. In SPICE simulation, all transistor open faults are modeled by a 20M-Ω resistor and short fault is modeled by a 10 Ω resistor as shown in the Figures 4.7(a) and 4.7(b).

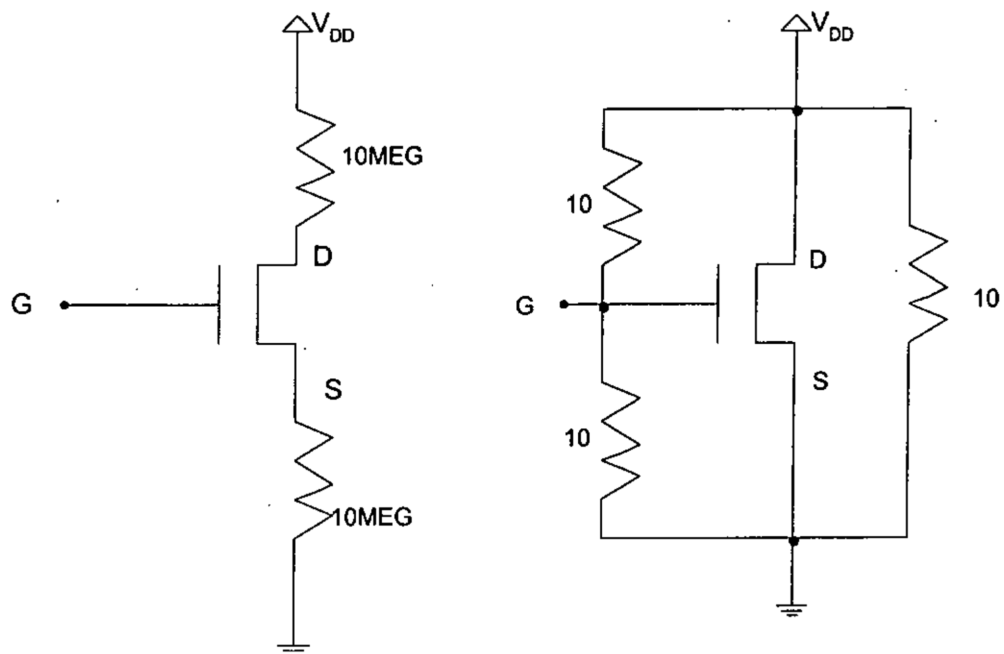


Figure 4.7(a) Modeling of Open Faults Figure 4.7(b) Modeling of Short Faults

4.5.2 Tolerance Limits of a Parameter

Tolerance limits of a parameter P_i are defined to be the maximum acceptable variations of that parameter in the CUT. For example, the oscillation frequency w_{osc} produced from the CUT is considered to be an indirect parameter. An indirect parameter is a parameter which is not of interest in the normal mode of the CUT and is evaluated only for test purposes. The tolerance limits of the indirect parameter W_{osc} is called the tolerance band of the oscillation frequency w_{osc}. The tolerance band of

oscillation frequency w_{osc} for the CUT is determined using a Monte Carlo analysis. In our analysis the tolerance band of the CMOS process used is ± 5%. This implies that if the values of parameters to be observed in the testing process appropriate to particular faults are within the tolerance band, these faults will be considered as tolerable and cannot be detected.

4.5.3 Equivalent fault set

An equivalent fault set is defined as a set of faults whose corresponding output parameter values such as current, frequency, voltage and their tolerance bands are overlapping each other. And these faults cannot be distinguishable within equivalent fault set. For example in the PSC measurement approach the faults S12, S214, S815, S1415, S812, S1214 injected in OA1 in Figure 4.5 results a current (Vdd) of 36.852uA, 40.697uA, 60.966uA, 60.926uA, 63.492uA, 64.195uA respectively and the tolerance band proposed for the current is ±5%. Table 4.2 shows the formation of equivalent fault sets.

From the table below the tolerance bands of faults S12, S214 are overlapping and the faults are grouped into two equivalent fault sets. In that, set 1 contains S12, S214 with a power supply current range of 35uA to 39uA and set 2 contains S214 with current range of >39uA to 43uA. In the same way the tolerance band of faults S815, S1415, S812, S1214 are overlapping and are grouped into three equivalent fault sets. In which set 1 contains S815, S1415, S812, S1214 with a current range of 58uA to 64uA, set 2 contains S1415, S812, S1214 with current range of >64uA to 66uA, and set 3 contains S812, S1214 with current range of >66uA to 67uA.

Table 4.2 Formation of equivalent fault sets

Fault	I(Vdd) in uA	Tolerance band -5%	+5%
S12	36.852	35	39
S214	40.697	39	43
S815	60.966	58	64
S1415	62.926	60	66
S812	63.492	60	67
S1214	64.195	61	67

35 to 39uA

>39 to 43uA

58 to 64uA

>64 to 66uA

>66 to 67uA

Note: the bracketed faults indicate the equivalent fault sets

4.6 Simulation results

Fault simulation of OTM-based testing of the detector circuit was done by injecting open and short circuit faults at different nodes on the circuit. Analysis of the simulation results revealed that majority of the injected faults resulted in no-oscillation. In case of open circuit fault simulation: a total of 81 open faults were injected into the detector circuit in test mode. In this, 43 were resulted in loss of oscillation and 32 were caused significant deviation of the oscillation frequency from its nominal frequency tolerance band. And these 32 faults were categorized into 5 unique faults, 26 sets of equivalent faults because of overlapping of tolerance band of their oscillation frequencies. Even though 6 faults resulted in oscillations, they were not detectable, because of the oscillation frequency was within the tolerance bound around the nominal value.

In case of short circuit fault simulation: a total of 112 short faults were injected in to the circuit. In this, 86 were resulted in loss of oscillation and 21 faults were caused significant deviation of oscillation frequency from its nominal frequency tolerance band. In these 21 faults, 7 faults were categorized into unique faults and 14 faults were grouped into 5 sets of equivalent fault sets. And 5 faults were undetectable because the oscillating frequency was within the bound around the nominal value.

The summary of the analysis of fault diagnosis by OTM is shown in Table 4.3

Table 4.3 Analysis of fault diagnosis by OTM

Fault Type	Total no. of faults injected	No. of faults detected (with oscillation)	No. of faults detected (without oscillation)	Fault coverage
Open faults	81	32 (5 unique faults and 26 sets of equivalent faults)	43	92.59%
Short faults	112	21 (7 unique faults and 5 sets of equivalent faults)	86	95.54%
Overall	193	53 (12 unique faults and 31 sets of equivalent faults)	129	94.30%

Table 4.3 shows that the fault coverage of OTM is very high. However, in view of fault location identification, the majority of faults that can be detected from the no oscillation cases cannot be distinguished hence resulting in poor diagnostic resolution.

In order to improve the fault diagnostic resolution, a power supply current measurement technique is proposed to supplement the fault location capability. In this PSC measurement technique, the current passing through the V_{DD} terminal is monitored during the application of the input stimulus, where in, every fault condition can be considered as a change in current through the V_{DD} terminal. A fault is considered as detectable when the corresponding current value exceeds a tolerance bound around the nominal value.

The sensitivity of the PSC measurement was investigated by considering those faults, which were indistinguishable, by no-oscillation in OTM. A total of 43 open circuit faults and 86 short circuit faults were resulted in no-oscillation and the power supply current was measured for these faults during the test mode. After analyzing the simulation results, measurements for most of the faults were closed to each other resulting in their tolerance bands overlapping each other. These faults were grouped into equivalent fault sets. In case of open circuit faults, after analyzing the simulation results, 43 indistinguishable faults were grouped into 20 equivalent fault sets. In case of short circuit faults, 86 indistinguishable faults were categorized into 3 unique faults and 58 equivalent fault sets. The details of the equivalent fault sets are shown in appendix-B. The results of analysis of applying the PSC approach and its comparison with OTM are given in Table 4.4.

Table 4.4 Analysis of fault diagnosis by OTM and PSC

Fault Type	Detected by OTM	Detected by PSC
Open faults detected (without oscillation)	43 (all are indistinguishable faults)	43 (forms 20 sets of equivalent faults)
Short faults detected (without oscillation)	86 (all are indistinguishable faults)	86 (3 unique faults and 58 sets of equivalent faults)
Overall	129 (all are indistinguishable faults)	129 (3 unique faults and 78 sets of equivalent faults)

4.7 Discussion

From the summary of the open and short circuit analysis of the detector circuit by OTM it was concluded that the fault coverage is high enough to detect the faulty circuit but it cannot be useful in identifying the location of the faults in the circuit. From the analysis of the open and short circuit faults of the detector circuit by integrating OTM and PSC, 3 faults were uniquely identified by PSC and the remaining were grouped into 78 equivalent fault sets. From these results it was concluded that there was an improvement in the fault locating capability comparing with the OTM. However, there are still 126 faults, comprise 78 equivalent fault sets, which cannot be distinguished. Thus, additional/supplementary testing approaches are needed to try to distinguish those equivalent faults within each of the 78 equivalent fault sets. The details about these testing approaches are described in the next chapter.

Chapter 5

Fault analysis of the detector circuit using I_{ddq} testing

5.1 Introduction

So far, the open and short circuit fault analysis of the detector circuit has been performed using OTM and power supply current measurement techniques under test mode. From the analysis, it has been concluded that this approach is efficient in terms of fault coverage. Despite its efficiency in terms of high fault coverage, there are still some undetected faults existing in digital circuitry. In an effort to improve the fault detectability of the detector circuit, I_{ddq} testing technique is supplemented to the OTM and power supply current measurement techniques. Especially under I_{ddq} testing, in addition to OTM and power supply current measurement techniques, some of the undetected faults in the digital portion of the detector circuit can be detected.

5.2 Fault analysis of the detector circuit by I_{ddq} testing

In this I_{ddq} testing, analysis of short and open circuit faults in the digital circuitry of the detector circuit are considered. Faults cannot be detected by the OTM and power supply current measurement techniques are fault simulated. The digital portion of the detector circuit with identified nodes is shown in Figure 5.1. In this simulation exercise, only one fault is injected at a time. Upon carrying out the analysis,

four short circuit faults and five open circuit faults in the NAND gate and the NOR gate are undetected by OTM and PSC. The I_{ddq} measurement is done on these faults using Spice with a zero voltage source at the ground path of the detector circuit in normal mode.

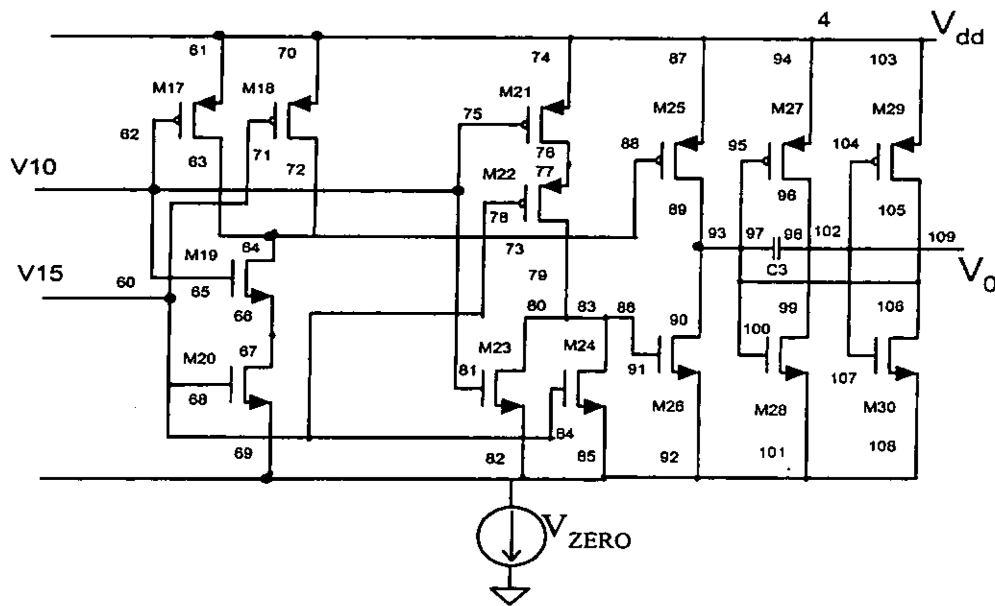


Figure 5.1 Digital portion of the detector circuit

5.2.1 Experimental setup

I_{ddq} test for the NAND gate:

In fault analysis of detector circuit only three faults, S_{6366}, S_{6669} and O_{64}, are found undetectable in NAND gate. The circuit of the NAND gate with two short circuit faults and one open circuit fault are shown in the Figure 5.2. The simulation results of a defect-free detector circuit in normal mode are shown in Figure 5.3.

Firstly, consider short circuit between nodes 63 and 66. When the input vector at gate terminal is AB=01, PMOS M17 and NMOS M20 are in saturation region and M18,

M19 are in cut-off region. Hence, under this short circuit fault for input AB=01, there is a low-impedance path from V_{dd} to GND. However, due to the presence of a low impedance path from V_{dd} to GND, there is a large steady state current in the order of 430 uA as shown in the Figure 5.4. An increased current spike of about 652.632uA at the state transition time is observed. By observing the I_{ddq} current with fault-free and faulty-one, faults can be detected. For short circuit between nodes 66 and 69, the input vector AB=10 is used. With this input the transistors M19, M18 are in saturation region. Hence, under this fault for inputAB=10, there is a low-impedance path from V_{dd} to GND. However, due to the presence of a low-impedance path from V_{dd} to GND, there is a large steady state current of 450.87uA, which is larger than the current in fault-free case as shown in Figure 5.5 and hence the fault can be detected.

I_{ddq} test is done with different input test vectors under the presence of open circuit fault at node 64 in NAND gate. From the simulation results, it is found that there is no change in the I_{ddq} current with fault-free and faulty case and it cannot be detected with I_{ddq} testing.

The brief summary of the I_{ddq} test on NAND gate is shown in the following Table 5.1.

Table 5.1 Summary of the I_{ddq} test on NAND gate.

Test vectors	Faults	Status
A=0, B=1	S_{6366}	Detectable
A=1, B=0	S_{6669}	Detectable
A=1,B=0;A=0, B=1; A=1,B=1	O_{64}	Undetectable

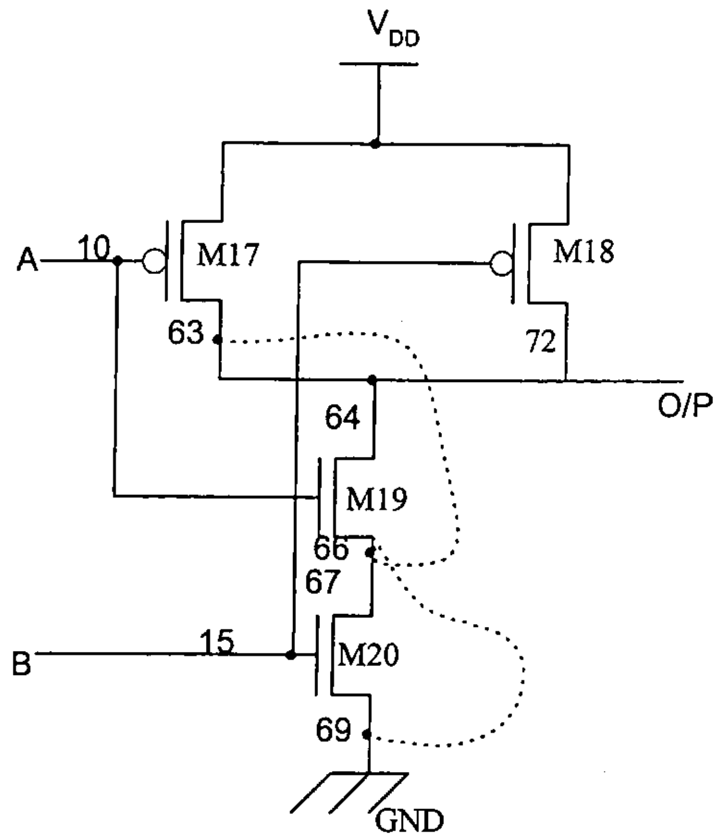


Figure 5.2 CMOS NAND gate to illustrate I_{ddq} testing

I_{ddq} test for the NOR gate:

In fault analysis of detector circuit only six faults, namely S_{7476}, S_{7679}, O_{80}, O_{82}, O_{83} and O_{85}, are found undetectable in the NOR gate. The circuit of the NOR gate with two short circuit faults and four open circuit nodes are shown in the Figure 5.6.

Consider short circuit between nodes 74 and 76. When the input vector at gate terminal is AB=10, the PMOS M22, NMOS M23 are in saturation region and M21, M24 are in cut-off region. Hence, under this short circuit fault for input AB=10, there is a low-impedance path from V_{dd} to GND. However, due to the presence of a low impedance path from V_{dd} to GND, there is a large steady state current of the order of 450.967 uA as shown in the Figure 5.7. So by observing the I_{ddq} current with fault-free

and faulty-one it can detect the fault. Whereas, for short circuit between nodes 76 and 79, the input vector AB=01 is used. With this input the transistors M21, M24 are in saturation region. Hence under this fault, for input AB=01 there is a low-impedance path from V_{dd} to GND. However, due to the presence of a low-impedance path from V_{dd} to GND, there is a large steady state current of 463.158uA current, which is larger than the current in fault-free case as shown in Figure 5.8 and hence the fault can be detected.

I_{ddq} test is carried out with different input test vectors under the presence of open circuit fault at nodes 80,82,83,85 in NOR gate. From the simulation results, it is found that there is no change in the I_{ddq} current with fault-free and faulty case and it cannot detect with I_{ddq} testing. The brief summary of the I_{ddq} test on the NOR gate is shown in Table 5.2 for easy reference.

Table 5.2 Summary of the I_{ddq} test on the NOR gate.

Test vectors	Faults	Status
A=1, B=0	S_{7476}	detectable
A=0, B=1	S_{7679}	detectable
A=1,B=0;A=0, B=1; A=1,B=1	O_{80},O_{82},O_{83}andO_{85}	undetectable

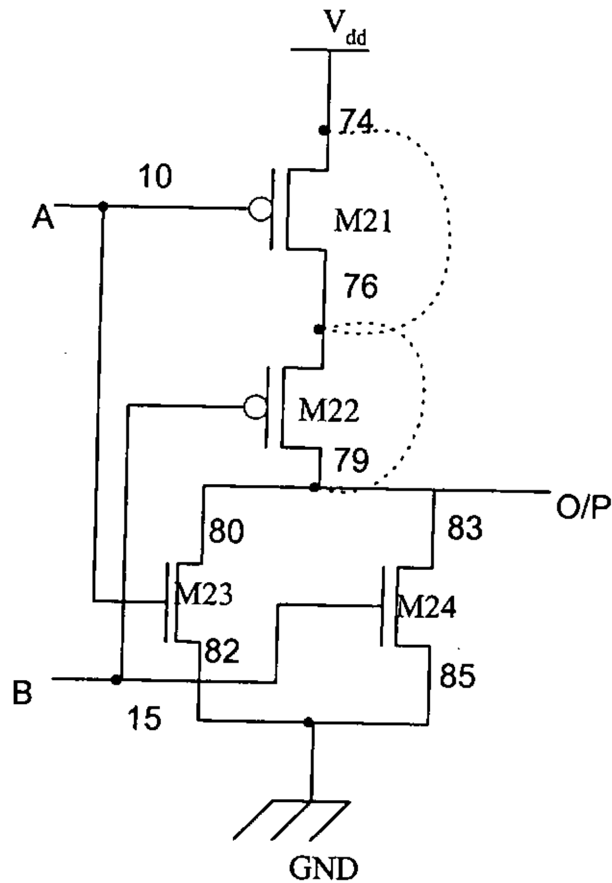


Figure 5.6 CMOS NOR gate to illustrate I_{ddq} testing

5.3 Conclusion

A brief review of the I_{ddq} testing was given. Both off-line and built-in current sensing techniques were described. Although many on-chip BICS's have been published literally, for reasons outlined above industries are still using off-chip current measurement methods to test the ASICs.

As described in the previous chapter, under test mode a total of 63 open and short circuit faults were injected into a digital portion of the circuit, in that 49 were detected by the OTM. The rest of the faults, which are undetected by the OTM, were considered using the I_{ddq} measurement. The digital portion of the detector circuit contains one NAND gate, one NOR gate, and three NOT gates. To improve the fault

coverage of the digital portion of the detector circuit, I_{ddq} test was conducted at normal mode. In this case study, simulation of faults is conducted using Spice by connecting a zero voltage source in series with the ground terminal. From the simulation results, four short circuit faults are detected by the I_{ddq} measurement. The fault coverage before the I_{ddq} measurement was 77.78%. By using I_{ddq} technique the fault coverage is increased to 84.13%.

Conclusively, from the above testing the I_{ddq} measurement helps in improving the fault coverage to a margin of 6.35%. However, this technique helps in improving the fault coverage but it cannot help to locate the faults in the circuit. So to further improve the fault resolution of the circuit, Node Voltage Measurement (NVM) technique is adapted. The detailed study of the NVM is described in the following chapter.

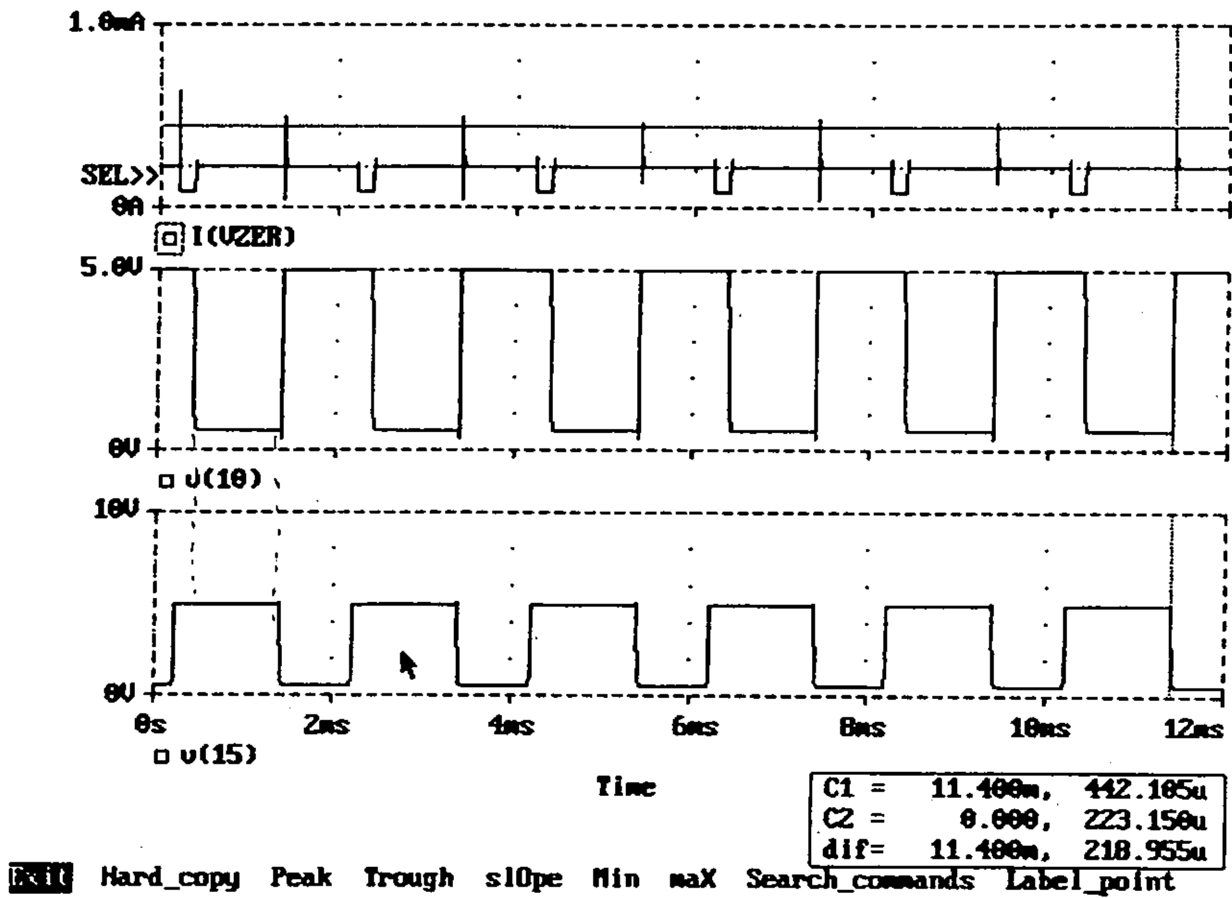


Figure 5.3 Simulation results of a defect-free detector circuit in normal mode

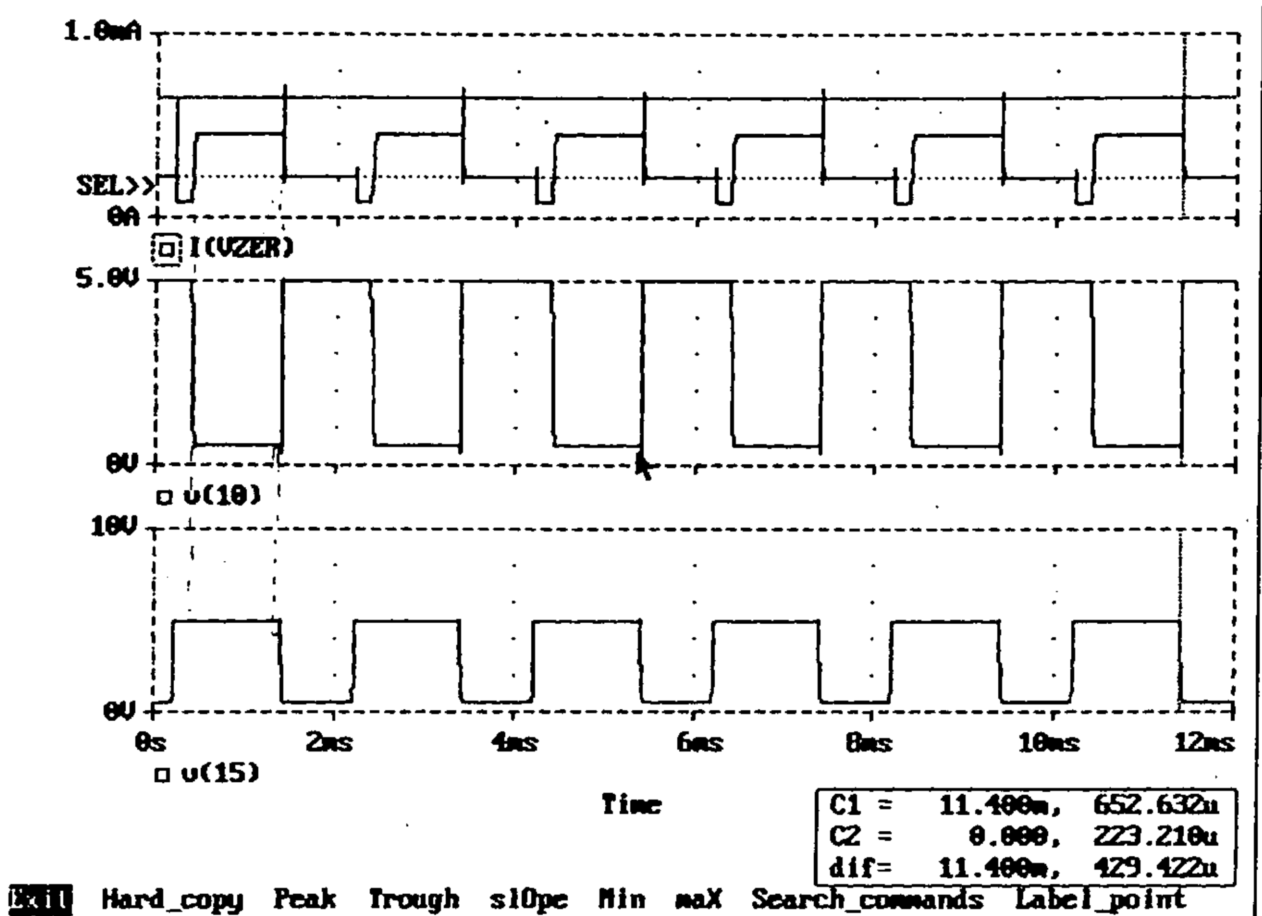


Figure 5.4 Simulation results of a defect detector circuit in normal mode with fault at S_{6366}

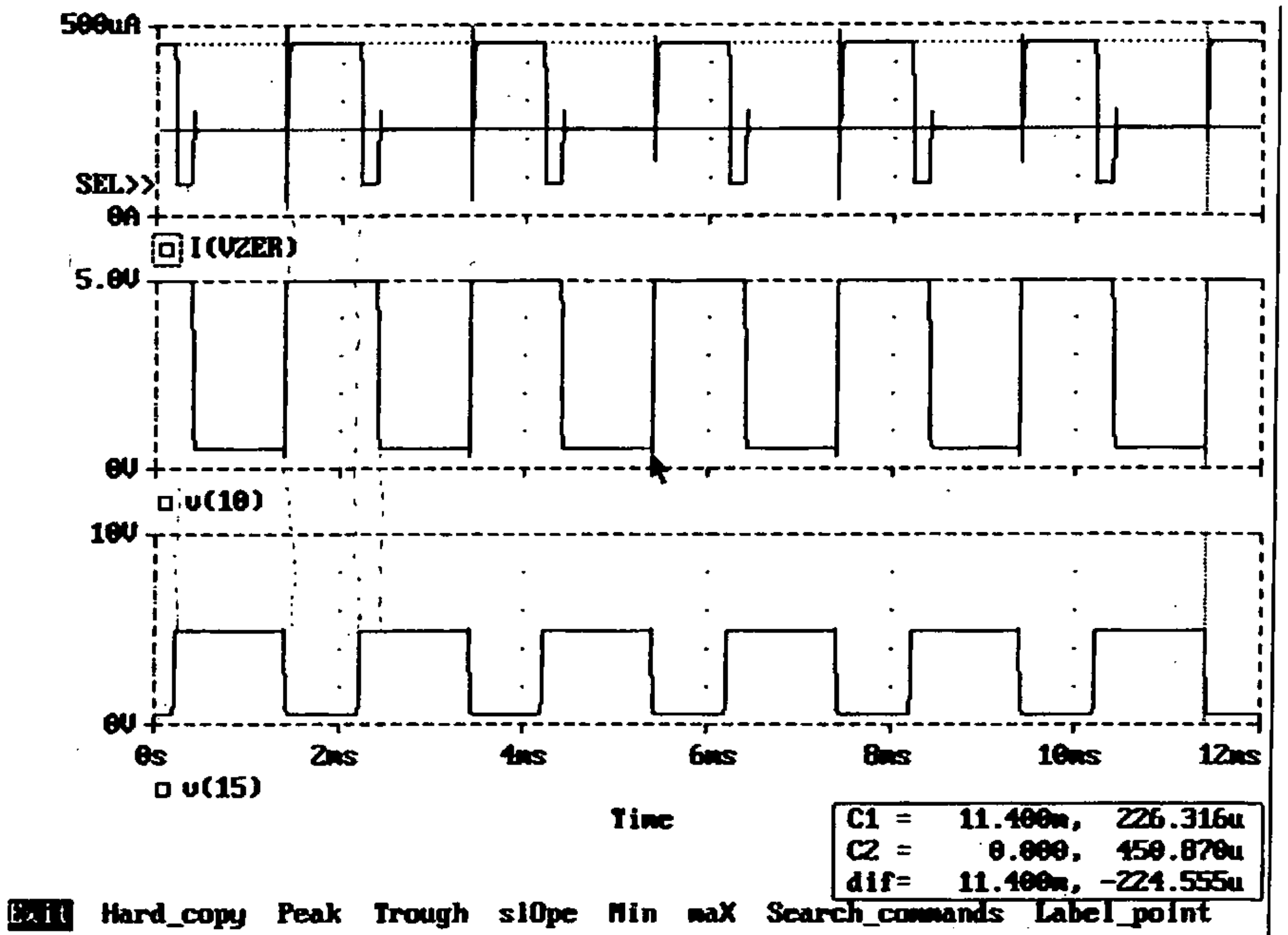


Figure 5.5 Simulation results of a defect detector circuit in normal mode with fault at S_{6669}

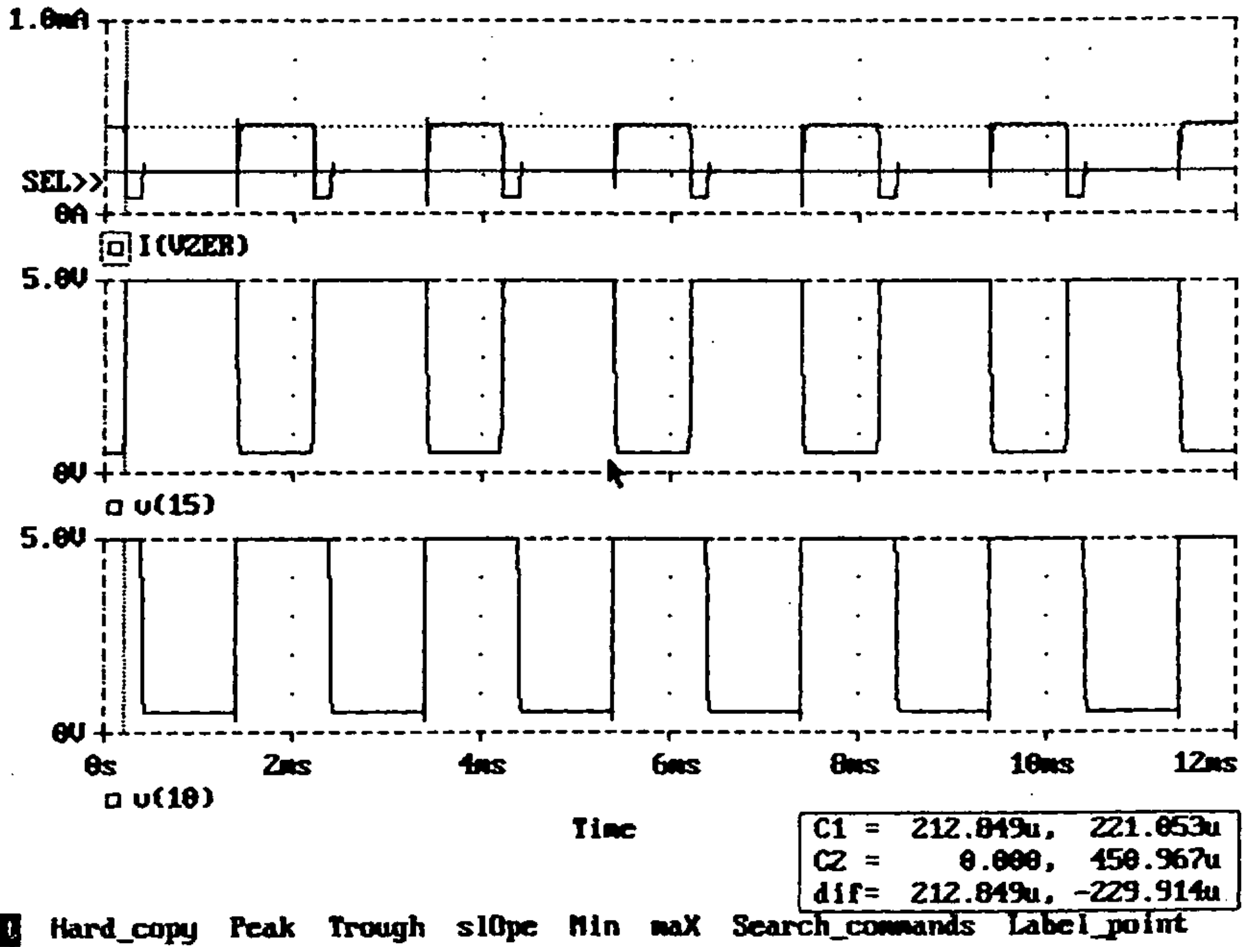


Figure 5.7 Simulation results of a defect detector circuit in normal mode with fault at S_{7476}

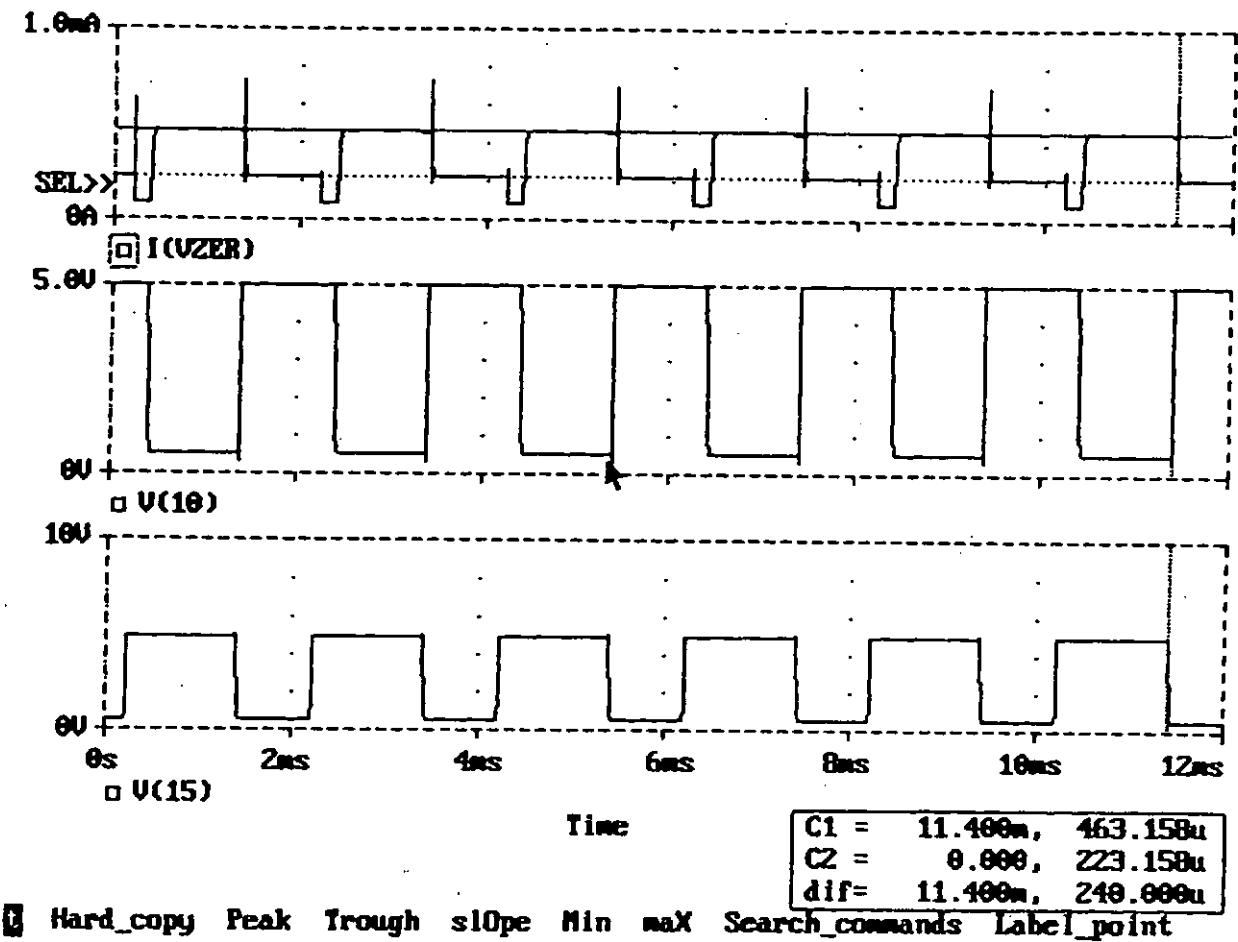


Figure 5.8 Simulation results of a defect detector circuit in normal mode with fault at S_{7679}

Chapter 6

Fault analysis of the detector circuit using NVM

6.1 Introduction

So far, we have developed and implemented an efficient testing approach based on a combination of OTM and PSC to detect and locate catastrophic faults (as described in Chapter 4) for the threshold detector, which are commonly used in the telephone tone ringer applications. Even though this approach has advantages like high fault coverage without use of any external stimuli and good diagnostic resolution, still there are 78 equivalent fault sets in which the faults cannot be differentiated and their locations cannot be identified.

To further differentiate those faults within the equivalent sets and identify the correct fault locations, Node Voltage Measurement (NVM) technique was developed to complement the above mentioned OTM and PSC techniques.

6.2 Concept of NVM

In NVM technique, voltage measurement was recorded at the output node of the individual op-amps and digital gates by simulating each fault in test mode. Similar to the PSC testing method, here ±5% tolerance was also considered for each measured node voltage. Since some faults within an equivalent fault set may cause different voltages to appear at different circuit nodes, these voltage amplitudes are then

compared and used to further differentiate these faults within that particular equivalent fault set.

6.3 Fault analysis of the detector circuit by NVM

The faults, which are undifferentiated by the combination of OTM and PSC, are considered for NVM. In this analysis each injected fault is simulated by the PSPICE and voltage at the gate level nodes such as 10,15,17,19,20,22 are measured.

For NVM testing two faults F_1 and F_2 are said to be equivalent if and only if the tolerance band of the voltage magnitude at particular gate output node under the presence of each fault are identical.

From the previous analysis by OTM and PSC, there are 58 equivalent sets of short circuit faults and 20 equivalent sets of open circuit faults are found and we cannot differentiate the faults within this equivalent fault set. The faults, which are undifferentiated within the equivalent fault set are considered for analysis by the NMV in test mode. After simulating each fault within the equivalent fault set, the magnitude of ±5% voltage value of each fault are compared with the remaining faults within that equivalent fault set. And these faults are further grouped into equivalent fault set if there is any overlapping in the voltage value, otherwise the fault is considered as a unique fault.

The results of the analysis of the NVM approach and the relationship between PSC and NVM approaches for those faults causing no oscillation are summarised in Tables 6.1(a) and 6.1(b).

It is worth mentioning that, in the analysis presented here, the degree of fault locating capability of different circuit nodes are varied. In order to achieve maximal

fault diagnostic resolution, all but with the exception of node 20 have to be accessed in the short faults simulation while all but node 17 have to be observed in the open faults simulation during the NVM test phase.

Though individual circuit nodes, such as nodes 10 and 15, provide higher fault diagnostic resolution than the others, more unique faults can be identified if output voltages at multiple nodes are analysed. For example, consider the equivalent short fault set No. 22 as shown in Table 6.1(a), three unique faults can be identified by observing the output voltages at node 19 while node 10 can identify another 2 faults. By observing both nodes, all 5 faults can be uniquely identified. Also, three unique faults of short fault set No. 37 can be identified by observing both nodes 10 and 19, while only 1 and 2 unique faults are identified when either node is observed.

Similarly, for the equivalent open fault set No. 18, observing both nodes 20 and 22 can identify 4 unique faults instead of 2. For equivalent open fault set No. 8, observing both nodes 19 and 21 can identify 3 unique faults instead of 1 (or 2). In addition, the fault diagnostic resolution of node 19 and 21 corresponds to open fault set No. 8 is 3(6,3,1)[1] and 4(4,3,1,1)[1] respectively. Some faults are grouped or differentiated in different subsets corresponding to different circuit nodes. Hence some groups of faults can be distinguished from other groups by observing multiple nodes. The combined analysis of multiple nodes can provide higher fault diagnostic resolution. Table 6.2 shows fault diagnostic resolution of PSC and NVM for faults causing no oscillation.

[1] See Note 4 below Table 6.1(b) for detailed explanation.

Table 6.1(a). Relationship between PSC and NVM for equivalent short fault sets

Short fault sets (PSC)		Number of subsets derived by NVM at different circuit nodes – as defined in Figure 2						
no.	elements	10	15	17	19	20	21	22
1	2	2(1,1)	2(1,1)	x	x	x	x	x
2	1	--	--	--	--	--	--	--
3	4	x	x	x	x	x	x	3(2,1,1)
4	3	x	x	x	x	x	x	3(1,1,1)
5	3	x	x	x	x	x	x	2(1,1)
6	5	x	3(1,2,2)	3(3,1,1)	3(3,1,1)	x	x	x
7	4	x	2(2,2)	3(1,1,2)	3(1,1,2)	x	x	x
8	5	x	3(1,2,2)	2(1,4)	2(1,4)	x	x	x
9	11	3(6,3,2)	5(2,2,5,1,1)	2(6,5)	3(5,5,1)	2(6,5)	2(6,5)	2(6,5)
10	9	3(4,3,2)	4(2,5,1,1)	2(4,5)	3(3,5,1)	2(4,5)	2(4,5)	2(4,5)
11	8	3(3,3,2)	4(1,5,1,1)	2(3,5)	3(2,5,1)	2(3,5)	2(3,5)	2(3,5)
12	7	3(2,3,2)	3(5,1,1)	2(2,5)	3(1,5,1)	2(2,5)	2(2,5)	2(2,5)
13	5	3(1,2,2)	2(4,1)	2(4,1)	2(4,1)	2(4,1)	2(4,1)	2(4,1)
14	5	3(2,1,2)	3(3,1,1)	2(3,2)	3(3,1,1)	2(3,2)	2(3,2)	2(3,2)
15	4	3(1,1,2)	3(2,1,1)	2(2,2)	3(2,1,1)	2(2,2)	2(2,2)	2(2,2)
16	2	x	2(1,1)	x	2(1,1)	x	x	x
17	2	x	2(1,1)	2(1,1)	2(1,1)	2(1,1)	2(1,1)	2(1,1)
18	2	x	x	2(1,1)	2(1,1)	2(1,1)	2(1,1)	2(1,1)
19	1	--	--	--	--	--	--	--
20	9	5(1,2,1,2,4)	5(1,2,1,2,4)	4(1,1,1,6)	2(3,6)	2(3,6)	2(3,6)	2(3,6)
21	8	4(2,1,2,4)	4(2,1,2,4)	3(1,1,6)	2(2,6)	2(2,6)	2(2,6)	2(2,6)
22	14	9(1,1,1,2,4,2,2,1,1)	7(1,1,2,4,2,2,3)	3(1,11,2)	5(2,9,1,1,1)	2(2,12)	2(1,13)	2(1,13)
23	13	8(1,2,4,2,2,1,1,1)	6(1,2,4,2,2,3)	2(11,2)	5(1,9,1,1,1)	2(1,12)	x	x
24	12	7(2,4,2,2,1,1,1)	5(2,4,2,2,3)	2(10,2)	5(1,8,1,1,1)	2(1,11)	x	x
25	11	6(4,2,2,1,1,1)	4(4,2,2,3)	2(9,2)	5(1,7,1,1,1)	2(1,10)	x	x
26	10	6(3,2,2,1,1,1)	4(3,2,2,3)	2(8,2)	5(1,6,1,1,1)	2(1,9)	x	x
27	7	5(2,2,1,1,1)	3(2,2,3)	2(5,2)	5(1,3,1,1,1)	2(1,6)	x	x
28	6	5(1,2,1,1,1)	3(1,2,3)	2(4,2)	4(1,3,1,1)	2(1,5)	x	x
29	3	3(1,1,1)	2(1,2)	x	2(1,2)	x	x	x
30	2	2(1,1)	x	x	x	x	x	x
31	3	2(2,1)	2(2,1)	2(2,1)	2(2,1)	2(2,1)	2(2,1)	2(2,1)
32	2	2(1,1)	2(1,1)	2(1,1)	2(1,1)	2(1,1)	2(1,1)	2(1,1)
33	1	--	--	--	--	--	--	--
34	4	3(1,2,1)	2(2,2)	x	x	2(1,3)	2(1,3)	4(1,1,1,1)
35	7	3(2,1,4)	3(2,1,4)	3(3,2,2)	2(3,4)	2(3,4)	2(3,4)	4(1,1,1,4)
36	6	3(1,1,4)	3(1,1,4)	3(2,2,2)	2(2,4)	2(2,4)	2(2,4)	3(1,1,4)
37	7	3(1,4,1)	3(1,4,1)	4(1,2,2,1)	2(1,5)	2(1,5)	2(1,5)	2(1,5)
38	7	4(4,1,1,1)	4(4,1,1,1)	4(2,2,1,2)	3(5,1,1)	3(5,1,1)	3(5,1,1)	3(5,1,1)
39	6	4(3,1,1,1)	4(3,1,1,1)	4(1,2,1,2)	3(4,1,1)	3(4,1,1)	3(4,1,1)	3(4,1,1)
40	6	4(2,1,2,1)	5(2,1,1,1,1)	4(2,1,2,1)	4(3,1,1,1)	4(3,1,1,1)	3(3,2,1)	3(3,2,1)
41	5	3(1,3,1)	4(1,2,1,1)	3(1,3,1)	4(1,1,2,1)	4(1,1,2,1)	3(1,3,1)	3(1,3,1)
42	4	2(3,1)	3(2,1,1)	2(3,1)	3(1,2,1)	3(1,2,1)	2(3,1)	2(3,1)
43	3	2(1,2)	3(1,1,1)	2(2,1)	2(2,1)	2(2,1)	2(1,2)	2(1,2)
44	2	x	2(1,1)	2(1,1)	2(1,1)	2(1,1)	x	x
45	1	--	--	--	--	--	--	--
46	2	x	x	2(1,1)	2(1,1)	2(1,1)	x	x
47	4	3(1,2,1)	3(2,1,1)	2(3,1)	2(3,1)	2(1,3)	2(1,3)	2(1,3)
48	3	2(2,1)	3(1,1,1)	2(1,2)	2(1,2)	x	x	x
49	2	2(1,1)	2(1,1)	x	x	x	x	x
50	1	--	--	--	--	--	--	--
51	1	--	--	--	--	--	--	--
52	2	2(1,1)	2(1,1)	x	x	x	x	x
53	1	--	--	--	--	--	--	--
54	2	2(1,1)	2(1,1)	2(1,1)	2(1,1)	2(1,1)	2(1,1)	2(1,1)
55	2	x	x	x	2(1,1)	x	x	x
56	1	--	--	--	--	--	--	--
57	1	--	--	--	--	--	--	--
58	1	--	--	--	--	--	--	--

Table 6.1(b). Relationship between PSC and NVM for equivalent open fault sets

Open fault sets (PSC)		Number of subsets derived by NVM at different circuit nodes – as defined in Figure 2						
no.	elements	10	15	17	19	20	21	22
1	3	2(2,2)	x	x	x	x	x	x
2	2	x	x	x	x	x	x	x
3	1	--	--	--	--	--	--	--
4	2	x	x	x	x	x	x	x
5	1	--	--	--	--	--	--	--
6	2	x	x	x	x	x	x	x
7	1	--	--	--	--	--	--	--
8	10	x	x	x	3(6,3,1)	2(6,4)	4(4,4,1,1)	3(2,6,2)
9	6	x	x	2(2,4)	2(2,4)	2(2,4)	2(2,4)	2(2,4)
10	6	x	x	2(4,2)	2(4,2)	2(4,2)	2(4,2)	x
11	4	x	3(2,1,1)	2(2,2)	2(2,2)	2(2,2)	2(2,2)	x
12	2	x	2(1,1)	x	x	x	x	x
13	1	--	--	--	--	--	--	--
14	6	x	x	x	x	x	x	x
15	6	3(4,1,1)	2(4,2)	2(4,2)	2(4,2)	2(4,2)	2(4,2)	2(4,2)
16	5	3(3,1,1)	2(3,2)	2(3,2)	2(3,2)	2(3,2)	2(3,2)	2(3,2)
17	2	2(1,1)	x	x	x	x	x	x
18	4	x	x	x	x	3(1,1,2)	2(2,2)	3(2,1,1)
19	4	x	x	x	x	x	x	x
20	2	x	x	x	x	x	x	x

Notes :

1. For circuit node number, refer Figure 4.4 - Block diagram of the threshold detector under test mode.
2. 'x' denotes the appropriate **equivalent fault set** that can not be differentiated by NVM.
3. '--' denotes the original **equivalent fault set** that consists of a set of faults that can not be further differentiated.
4. $w(s_1, s_2, \ldots, s_n)$ - denotes an **equivalent fault set** that can be differentiated by NVM into w subsets of equivalent faults, where $s_1, s_2, \ldots, s_n$ represent the number of equivalent faults in each subset.
5. Grey-shaded cell denotes highest fault diagnostic resolution achieved by NVM at a particular node for a particular equivalent fault set.

6.4 The 6 to 1 multiplexer

In order to observe the targeted internal nodes of the CUT and to minimise the number of additional accessible pins, a 6 to 1 multiplexer is proposed for this purpose. Although the observation provided at node 17 for the open faults, and node 20 for the short faults during the NVM test phase can be taken over by other nodes, the

observation provided at node 17 and node 20 have proved to be useful for short and open faults diagnosis respectively. Consequently, apart from node 20 (which is the output node and is already available) all the other six nodes should be made accessible in order to achieve maximal fault diagnostic resolution. Therefore, a 6 to 1 multiplexer is needed and the proposed block diagram of the threshold detector under test mode is shown in Figure 6.1.

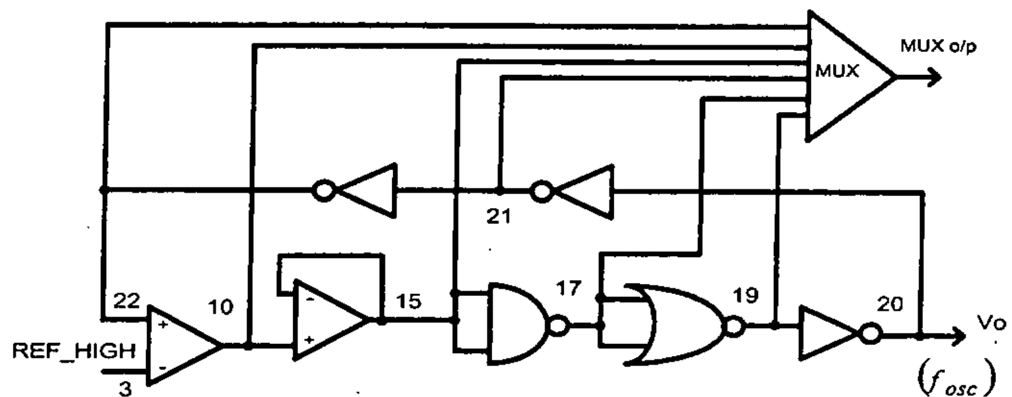


Figure 6.1 Block diagram of the threshold detector under test configuration with built-in 6-to-1 MUX

6.5 Conclusion

By adopting the NVM approach, the detectability of the number of unique faults of the combined OTM and PSC approach increases by 293.33%, the number of equivalent fault sets increases by 40.37% while the average number of equivalent faults per equivalent fault set decreases by 47.53%. The higher the number of unique faults identified, coupled with the higher the number of equivalent fault sets differentiated with respect to the same number of equivalent faults, and the lower the number of

equivalent faults per equivalent fault set, results in higher fault diagnostic resolution. Thus the NVM approach that can significantly improve the fault diagnostic resolution of OTM or combined OTM and PSC testing approaches is verified.

Table 6.2 Fault diagnostic resolution of PSC and NVM for faults causing no oscillation

Fault Type	Number of faults detected by PSC	Number of faults detected by NVM
Short faults (without oscillation)	86 (3 unique faults, and 58 sets of equivalent faults)	83 (33 unique faults, and 91 sets of equivalent faults)
Open faults (without oscillation)	43 (20 sets of equivalent faults)	43 (11 unique faults, and 31 sets of equivalent faults)

Chapter 7

Conclusions and future works

7.1 Conclusions

This thesis presents the fault diagnosis of a telephone tone ringer IC based on following techniques.

- Combination of the OTM and PSC measurement in test mode
- NVM technique
- I_{ddq} measurement in normal mode

The key points of above approach, which was based on combination of the oscillation-based testing technique (OTM) and power supply current measurement (PSC) technique, are to enable high fault coverage with the advantage of being easily implemented and to provide a fault identification procedure to achieve effective fault location.

The block diagram of the detector circuit of the telephone tone ringer circuit, which is shown in Figure 4.2, was used to investigate the feasibility of above techniques. We used similar fault models and assumptions as those stated in reference [27]. In our investigation, all transistor open circuit faults (except gate open faults) and short circuit faults were examined. Fault diagnosis of the detector circuit was carried out in three separate phases.

In phase-1 OTM was applied to the test circuit in which the detector circuit was converted into a ring oscillator and was shown in Figure 4.4. A total of 112 single short circuit faults and 81 single open circuit faults of the threshold detector circuit were

simulated under test mode. For each injected fault, the oscillation frequency or loss of oscillation was recorded and analysed. From the simulation results it was observed that most of the faults resulted no oscillations. Hence these faults couldn't be distinguished. In order to distinguish these faults the PSC measurement technique was integrated with OTM. In this PSC measurement technique the power supply currents corresponding to each one of these faults were recorded and analysed.

In phase-2 the circuit under test was configured back to normal mode and I_{ddq} measurement technique was applied to detect those faults which were undetected in the digital portion during the phase-1 test. In this test phase for each injected fault, the I_{ddq} value was measured and compared with the defect-free I_{ddq} value of the detector circuit to detect the fault.

In phase-3, NVM was applied to further differentiate all those faults, which are within the same equivalent fault set by the PSC technique. In this test phase all the output node voltages of individual op-amps and digital gates corresponding to each of these faults were measured and analysed.

7.1.1 Phase -1 conclusion

By applying OTM, the detector circuit was converted into ring oscillator (refer to Figure 4.4) by adding 19 extra NMOS transistors. In this analysis all switches were assumed as ideal. With reference to table 4.3, which presents the analysis of the fault diagnosis by OTM, 112 short circuit faults and 81 open circuit faults were injected in test mode. The oscillation frequency was measured at node no. 20 was shown in Figure 4.4. After analyzing the simulation results in test mode, 11 faults were resulted undetectable because of their oscillation frequencies fall within the 5% tolerance band

of nominal value. From the above analysis, it can be concluded that the overall fault coverage by OTM was about 94%.

By adapting the OTM, high fault coverage was achieved, on the whole the capability of identifying the fault location was poor due to the large number of no-oscillation results. To distinguish these no-oscillation faults, PSC measurement technique was integrated to the OTM. In this PSC measurement technique the current at V_{dd} terminal was recorded and analysed. With reference to the table 4.4, which presents the analysis of the fault diagnosis by OTM and PSC, 43 indistinguishable (no-oscillation) open circuit faults were distinguished by 20 sets of equivalent faults and 83 indistinguishable short circuit faults were distinguished by 78 sets of equivalent faults and three short circuit faults were uniquely distinguished by the PSC measurement under test mode.

7.1.2 Phase-2 conclusion

In this phase the detector circuit was switched back to normal mode and I_{ddq} test was conducted on faults which we cannot detect in digital portion of the detector circuit by OTM. With reference to table 5.1 and 5.2, which presents the results of the fault simulation by I_{ddq} test, only four short circuit faults were detected by I_{ddq} measurement out of 9 faults. The fault coverage of the digital portion before the I_{ddq} measurement was 77.7%, but after conducting the I_{ddq} testing technique the fault coverage was increased to 84.13%. Therefore, I_{ddq} measurement technique helps in improving the fault coverage to a margin of 6.35%.

7.1.3 Phase-3 conclusion

In this phase the faults, which are indistinguishable within the equivalent fault sets by PSC, were considered for fault analysis using NVM technique. With reference to table 6.2, which presents results of the fault simulation by NVM, 33 out of 83 short circuit faults were uniquely distinguished and the remaining were distinguished by 91 sets of equivalent faults. In case of open circuit faults, 11 out of 43 faults were uniquely distinguished and the remaining was distinguished by 31 sets of equivalent faults.

By adopting the NVM technique, the detectability of the number of unique faults of the combined OTM and PSC techniques increases by 293.33%, the equivalent fault sets increases by 40.37% while the average number of equivalent faults per equivalent fault set decreases by 47.53%. Thus the NVM technique that can significantly improve the fault diagnostic resolution of OTM or combined OTM and PSC testing techniques was verified.

To investigate the performance of the CUT with analog switches under OTM we conducted same open and short circuit fault simulations with analog switches. From the simulation results it was observed that the difference in the fault coverage with ideal switches and analog switches are very less and this can be negligible. Figure 7.1 shows a Venn diagram indicating the overall fault coverage and fault-locating capabilities corresponding to different phases of the proposed testing approach.

The major advantage of this approach, which is based on combination of OTM, PSC, I_{ddq} and NVM, are:

- the use of the oscillation-based testing technique to enable high fault coverage with the advantages of being easily implemented and less testing time;

- the adoption of power supply current measurements which do not consume any hardware overhead, provides a fault identification procedure to achieve certain fault locating capability;
- the integration of I_{ddq} testing approach that results in a improvement of fault coverage, but it needs extra hardware for measurement and;
- the incorporation of the node voltage measurements approach that results in a significant improvement of fault diagnostic resolution.

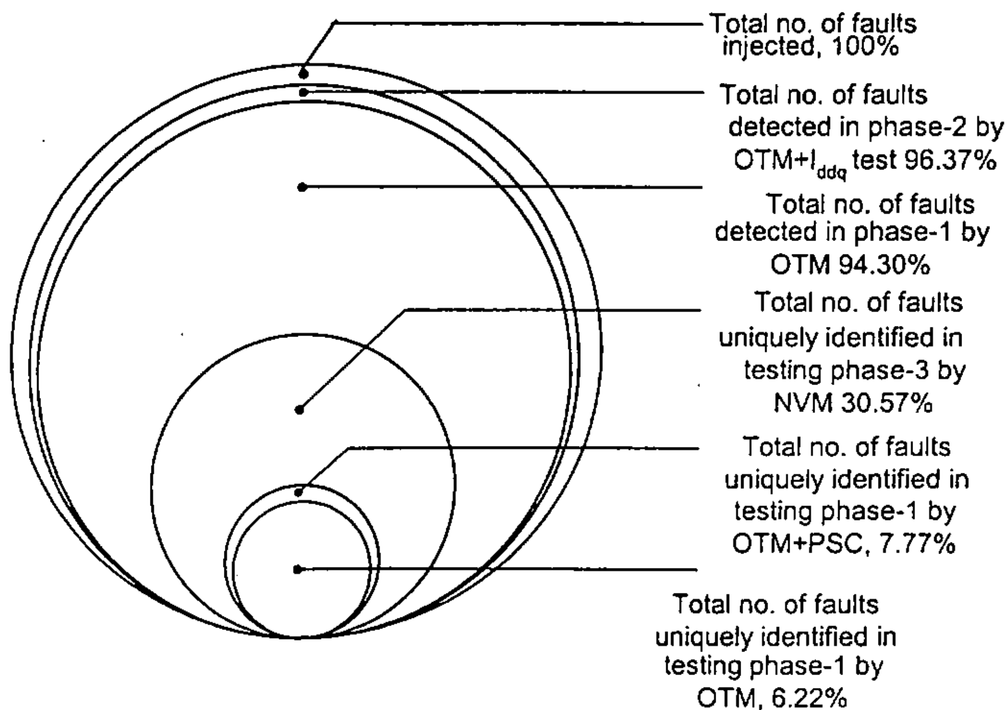


Figure 7.1 Venn diagram of fault coverage and unique fault identifications of the proposed testing approach

7.2 Future works

Since this new testing approach was performed in three separate phases and the fault diagnostic resolution was achieved incrementally, once a fault is located at any one phase, the successive phase(s), if there are any, need not be performed. Furthermore, only one observation is necessary in the OTM or PSC phase, and the voltages of internal circuit nodes during the NVM phase can be observed at the MUX output pin sequentially. Next these data are used to compare with the simulation results of a predefined fault list. Therefore a target fault or equivalent fault set can be identified easily and quickly. The proposed test procedure can be computerized to further increase efficiency, thus saving both time and effort. As far as the NVM phase is concerned, the major drawback is the need to compromise the fault diagnostic resolution and the additional hardware required.

We have proposed the future work as follows:

- Investigating other circuit parameters such as voltage wave form and phase shift to further enhance the fault identification effectiveness.
- Investigating the impact of performance of the NVM approach with the internal node access multiplexer built into the CUT.

List of Publications of the Author

[1] KO, K.Y., Gorla, N.S., Wong, M.W.T., and Lee, Y.S. "Improving Fault Diagnostic Resolution of OTM-Based Test Scheme for the Threshold Detector Circuit," *International Journal of Electronics,* U.K. Vol.88, No.2, pp.175-87, February 2001, U.K.

[2] Wong, M.W.T., Gorla, N.S., Ko, K.Y., and Lee, Y.S. "Mixed-Signal IC Testing Using Oscillation Test Methodology and Supply Current Measurement," *Proceedings, China Fifteenth National Conference on Circuits and Systems (NCCAS'99)*, Guangzhou, China, 24-26 November 1999, pp.214-217.

[3] Wong, M.W.T., Gorla, N.S., Ko, K.Y., Lin, K.L., and Lee, Y.S. "Testing of Catastrophic Faults for Mixed-Signal ICs ," *Proceedings, 8th International Symposium on Integrated Circuits, Devices and Systems (ISIC-99)*, Singapore, 8-10 September 1999, pp.68-72.

[4] Wong, M.W.T., Ko, K.Y., Gorla, N.S., and Lee, Y.S. "Effective Testing of the Threshold Detector of a Telephone Tone Ringer IC," *Proceedings, the 5th IEEE International Mixed Signal Testing Workshop (IMSTW'99)*, Vancouver, Canada, 15-18 June 1999, pp.171-175.

Bibliography

1. Shen, J. P., Maly, W. and Ferguson, F. J. "Inductive fault analysis of MOS. integrated circuits," *IEEE Design and Test of Computers*, Vol. 2, no. 6, pp.13-26 (1985)

2. Sachdev, M. "Catastrophic defect oriented testability analysis of a class AB amplifier," *Proc. of Defects and Fault Tolerance in VLSI Systems*, pp.319-326 (1993)

3. Soma, M. "Fault modeling and test generation for sample and hold circuits," *International Symposium on Circuits and Systems*, pp.2072-2075 (1991)

4. Soma, M. "An experimental approach to analog fault models," *Custom Integrated Circuit Conference*, pp. 13.6.1-13.6.4 (1991)

5. Meixner, A. and Maly, W. "Fault modeling for the testing of mixed integrated circuits," *Proc. of International Test Conference*, pp.564-572 (1991)

6. Sachdev, M. "Defect oriented analog testing: strengths and weaknesses," *Proc. of 20th European Solid State Circuits Conference*, pp.224-227 (1994)

7. Sachdev, M. "A defect oriented testability methodology for analog circuits," *Journal of Electronic Testing Theory and Applications*, vol. 6, no.3, pp.265-276 (1995)

8. Meixner, A. and Maly, W. "Fault modeling for the testing of mixed integrated circuits," *International Test Conference*, pp.564-571 (1991)

9. Nagi, N. and Abraham, J. A. "Hierarchical fault modeling for linear analog circuits," *Analog Integrated Circuits and Signal Processing*, vol. 10, pp.89-99 (1996)

10. Slamani, M. and Kaminska, B. "Multifrequency testability analysis for analog circuits," *Proc. IEEE VLSI Test Symposium*, pp.54-59 (1994)

11. Levi, M. "CMOS is most testable," *Proc. of International Test Conference*, Oct. 1981, pp.217-220 (1981)

12. Malaiya, Y. K. and Su, S.Y.H. "A new fault model and testing technique for CMOS devices." *Proc. of International Test Conference*, Sept. 1982, pp.25-34 (1982)

13. Zwolinski, M., Chalk, C., Wilkins, B. R. and Superjo, B. S. "Analog circuit test using RMS supply current monitoring," *IMSTW '96 Proceeding*.

14. Brgleg, F. "Digital signal processing considerations in filter-codec testing," *Proc. of the IEEE 1981 Test Conference, Computer Society of the IEEE Washington*, Dec., Oct. 1981, pp.193-200 (1981)

15. Slamani, M., Boukadoum, M. and Kaminska, B. "A DSP based approach for testing linear and non-linear analog circuits in time domain," *IMSTW '96 Proceeding*

16. Dislis, C., Dick, J. H., Dear, I. D. and amber, A. P. "Test economics and design for testability for electronic circuits and systems," Ellis Horwood, 1995

17. Wey, C. L. "Design of testability for analog fault diagnosis," *Int. Journal of Circuit Theory and Applications*, Vol. 15, pp.123-142 (1987)

18. Spalding, G. R. and Vanpeteghem, P. M. "Design for testability using Behavioral Models," *IEEE Trans. on Instrumentation Measurement*, Vol. 39, no. 6 (1990)

19. Hatzopoulos, A. A., Saskos, S. and Kontolean, J. M. "A complete scheme of built-in self-test (BIST) structure for fault diagnosis in analog circuits and systems," *IEEE Trans. Instrum. Meas.*, Vol. 42, pp.689-694 (1990)

20. Wey, C. L. "Built-In Self-Test (BIST) structure for analog circuit fault diagnosis," *IEEE Trans. Instrum. Meas.*, Vol. 39, no. 3, pp.517-521 (1990)

21. Wey, C. L. and Krishnan, S. "Built-In Self-Test (BIST) structure for analog circuit fault diagnosis with current test data," *IEEE Trans. Instrum. Meas.*, Vol. 31, no. 4, pp.535-539 (1992)

22. Wurtz, L. T. "Built-In Self-Test (BIST) structure for mixed-mode circuits," *IEEE Trans. Instrum. Meas.*, Vol. 42, no. 1, pp.25-29 (1993)

23. Toner, M. F. and Roberts, G. W. "A BIST scheme for a SNR, Gain tracking, and Frequency response test of a sigma-delta ADC," *IEEE Trans. on Circ. Syst.*, Vol. 42, no. 1, pp.1-15 (1995)

24. McCluskey, E. J. "Built-in self-test technique," *IEEE Design Test Comput.*, Vol. 2, pp.21-28, April (1985)

25. Wey, C. L., Jiang, B. L. and Wierzba, G. M. "Built-in self-test for analog circuits," *Proc. 31st Midwest Symp. Circuits Syst.*, St. Louis, Aug. 1988, pp.862-865 (1988)

26. Arabi, K. and Kaminska, B. "Oscillation-test strategy for analog and mixed-signal integrated circuits," *14th VLSI test symposium – 1996*, pp.476-482 (1996)

27. . Arabi, K and Kaminska, B. "Testing analog and mixed-signal integrated circuits using oscillation-test method," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 16, no. 7, July 1997, pp.745-753 (1997)

28. Dias, P. M., Franca, J. E. and Paulino, N. "Oscillation test methodology for a digitally-programmable switched-current biquad," *Proc. 2nd IMSTW*, May15-18, 1996 Canada, pp. 221-226 (1996)

29. Bob Thomas and Rick Andlauer, "Low cost test solution for I_{ddq}," *IEEE International Workshop on Iddq testing*, pp.50-53 (1996)

30. Maly, W. and Nigh, P., "Built-In current testing feasibility study" *Proceedings of the International Conference on Computer-Aided Design*," Santa Clara, USA, November 1988, pp.340-343 (1988)

31. Favalli, M.O. , Damiani , P.M. and Ricco, B. "Novel design for testability schemes for CMOS IC's ," *IEEE Journal of Solid-state Circuits*, Vol. 25, pp.1239-1246 (1990)

32. Maly, W. and Patyra, M. "Built-in current testing," *IEEE Journal of Solid-state Circuits*, Vol. 27, pp.425-428 (1992)

33. "IEEE standard test access port and boundary-scan architecture," *IEEE Standard 1149.1-1990 (includes IEEE std 1149.1a-1993)*, The IEEE, inc., 345 east 47th St., New York, NY, October 1993

34. Dunlop, A.E., Evans, W.J. and Rigge, L.A. "Managing complexity in IC design-past, present, and future," *Bell Labs Technical Journal*, Autumn 1997, pp.103-125 (1997)

35. Wong, M.W.T. "On the issues of oscillation test methodology," *Proceedings, the 16th IEEE Instrumentation and Measurement Technology Conference (IMTC/99)*, under the *SPECIAL SESSION ON INNOVATION and CHALLENGES in the Emerging Mixed-Signal Testing*, 1999 Venice, Italy.

36. Wong, M.W.T. and Ko, K.Y. "Enhancing mixed-signal ASICs reliability through the use of oscillation test methodology," *Proceedings, the 3rd International Conference On ASIC (ASICON '98)*, 21-23 October 1998, Beijing, China, pp.415-418 (1998)

37. Hatzopoulos, A.A. *et al.*, "Testing of analog and mixed-signal circuits by using supply current measurements," *IEE Proc.-Circuits Devices Syst.*, Vol.145, No.5, Oct 1998, pp.319-24 (1998)

38. Vinnakota, B."Monitoring power dissipation for fault detection," *Journal of Electronic Testing: Theory and Applications 11*, pp.173-181 (1997)

39. Bell, I.M. *et al.*,"Supply current testing of mixed analog and digital ICs," *Electron. Lett.*, 1991, 27, (17), pp.1581-1583 (1991)

40. Papakostas, D.K. and Hatzopoulos, A.A. " Supply current testing in linear bipolar ICs," *Electron. Lett.*, 1994, 30, (2), pp.128-130 (1994)

41. Miura, Y., Naito, S. and Kinoshita, K. " A case study of mixed-signal integrated circuit testing and application of current testing using the upper limit and the lower limit," *Proc. ISCAS'94*, London, UK, May 1994, pp.5.77-5.80 (1994)

42. Gielen, G. Wang, Z. and Sansen, W. "Fault detection and input stimulus determination for the testing of analog integrated circuits based on power supply monitoring," *Proc. ICCAD'94*, pp.495-498, (1994)

43. Allen, P. Holberg, D.R. "CMOS Analog Circuit Design," Holt, Rineheart and Winston (1987)

44. Kuijstermans, F.C.M., Sachdev, M. and Thijssen, A.P. "Defect-oriented test methodology for complex mixed-signal circuits," *European Design and Test Conference, 1995, Proceedings*, pp. 18-23 (1995)

45. Abramovici, M., Breuer, M. and Friedman, A. "Digital systems testing and testable design," Engle-wood Cliff, NJ, Computer Science Press (1990)

46. Wen Liu, R. "Testing and diagnosis of analog circuits and systems," Van Nostrand Reinhold (1991)

47. Ismail, M. and Fiez, T. "Analog VLSI: signal and information processing," McGraw-Hill (1994)

48. Sudhir Mallya, M. and Joseph Nevin, H. "Design procedures for a fully differential folded-cascade CMOS operational amplifier," *IEEE Journal of solid-state Circuits*, December (1989)

49. Vinnakota, B. and Harjani, R. "The design of analog self-checking circuits," *IEEE International Conference on VLSI Design*, January (1994)

50. Pang, C.Y., Cheng, K.T. and Gupta, S. "A comprehensive fault macromodel for op-amps," *IEEE International Conference on Computer Aiaded Design*, (1994)

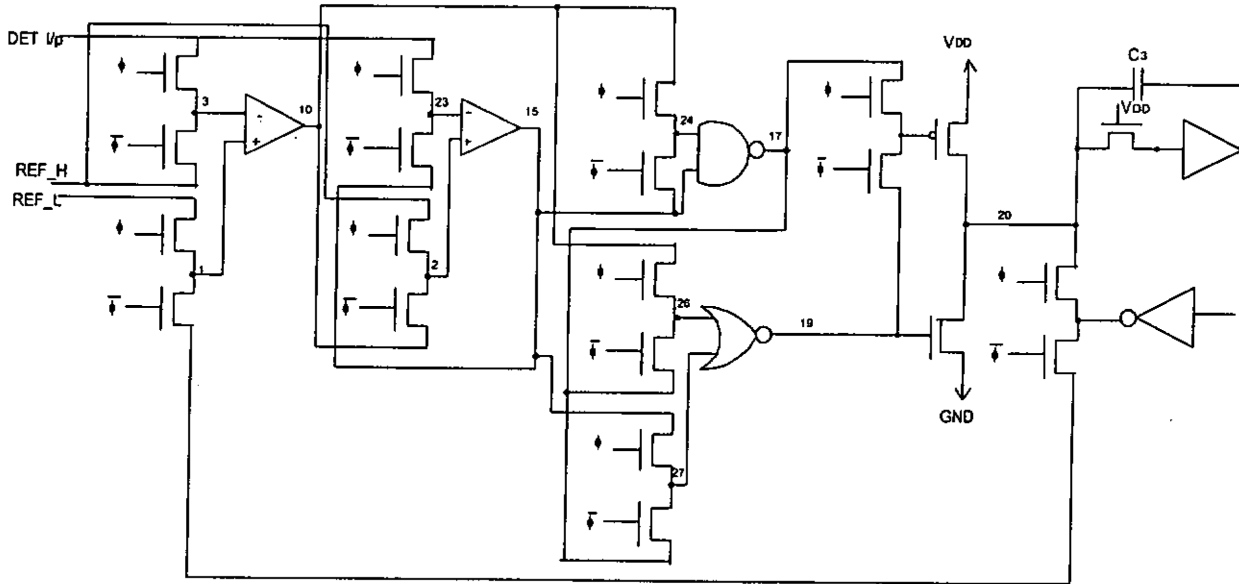
51. Arabi, K. and Kaminska, B. "Oscillation-based test strategy for analog and mixed-signal circuits," *U.S. Patent Application* , October (1995)

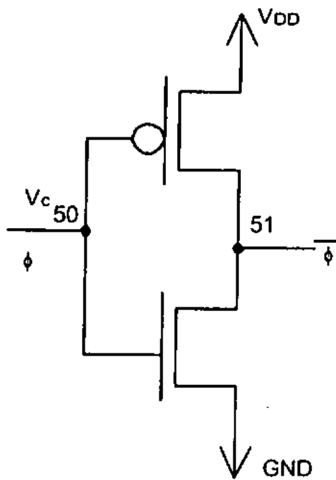
52. Milor, L. and Visvanathan, V. "Detection of catastrophic faults in analog integrated circuits," *IEEE Transation on Computer Aiaded Design*, Vol.8, no.2, February 1989, pp.114-130 (1989)

53. Jeong Beom Kim, Sung Je Hong and Jong Kim, "A CMOS built-in current sensing circuit," *International Journal of Electronics*, Vol. 85, No. 2, pp.181-205 (1998)

Appendix-A

Telephone Threshold Detector Circuit with Mode Selection Switches





Note:

1. Vc = ϕ = 5v $\Longrightarrow$ Normal mode
2. Vc = ϕ = 0v $\Longrightarrow$ Test mode

Appendix-B

The details of the Equivalent open fault sets in the PSC measurement by considering the no-oscillation open faults of OTM

Set no.	Tolerance band (uA) -5%	5%	Elements of fault set
1	14	15	o8, o5, o6
2	>15	16	o5, o8
3	>16	17	o6
4	32	35	o10, o12
5	>35	37	o12
6	48	53	o32, o34
7	>53	54	o34
8	56	62	o13,o15, o74, o76, o77, o79, o94, o96, o106, o108
9	>62	63	o64,o66, o67, o69, o106, o108
10	>63	70	o64,o66, o67, o69, o90, o92
11	>70	77	o51,o53, o90, o92
12	>77	78	o51,o53
13	>78	79	o53
14	182	201	o57,o59, o36, o38, o39, o40
15	>201	209	o111,o28, o36, o38, o39, o40
16	>209	210	o111,o28, o38, o39, o40
17	>210	227	o111,o28
18	347	384	o87,o89, o103, o105
19	644	711	o61,o63, o70, o72
20	8534	9432	o3, o1

The details of the Equivalent Short fault sets in the PSC measurement by considering the no-oscillation short faults of OTM

Set no.	Tolerance band (uA) -5%	5%	Elements of fault set
1	35	39	S12, S214
2	>39	43	S214
3	58	64	S815, S1415, S812, S1214
4	>64	66	S1415, S812, S1214
5	>66	67	S812, S1214
6	187	207	S6066, S7376, S7982, S4555, S4045
7	>207	210	S7376, S7982, S4555, S4045
8	>210	213	S7982, S4555, S4045, S3855, S3840
9	>213	227	S4555, S4045, S3855, S3840, S4043, S4345, S4355, S3540, S3843, S3538, S4245
10	>227	235	S3855, S3840, S4043, S4345, S4355, S3540, S3843, S3538, S4245
11	>235	236	S3840, S4043, S4345, S4355, S3540, S3843, S3538, S4245
12	>236	237	S4043, S4345, S4355, S3540, S3843, S3538, S4245
13	>237	238	S4355, S3540, S3843, S3538, S4245
14	>238	239	S3540, S3843, S3538, S4245, S4042
15	>239	240	S3843, S3538, S4245, S4042
16	>240	251	S4245, S4042
17	>251	264	S4042, S1217
18	>264	284	S1217, S6163
19	>284	299	S6163
20	301	332	S3842, S1220, S1520, S3555, S2030, S1530, S1528, S2028, S1517
21	>332	333	S1220, S1520, S3555, S2030, S1530, S1528, S2028, S1517
22	>333	348	S1520, S3555, S2030, S1530, S1528, S2028, S1517, S1728, S7682, S96101, S830, S1730, S1215, S828
23	>348	360	S3555, S2030, S1530, S1528, S2028, S1517, S1728, S7682, S96101, S830, S1730, S1215, S828
24	>360	364	S2030, S1530, S1528, S2028, S1517, S1728, S7682, S96101*, S830, S1730, S1215, S828
25	>364	365	S1530, S1528, S2028, S1517, S1728, S7682, S96101, S830, S1730, S1215, S828
26	>365	366	S1528, S2028, S1517, S1728, S7682, S96101, S830, S1730, S1215, S828
27	>366	380	S1728, S7682, S96101, S830, S1730, S1215, S828
28	>380	383	S7682, S96101, S830, S1730, S1215, S828
29	>383	384	S1730, S1215, S828
30	>384	385	S1215, S828
31	485	536	S6166, S114, S102105
32	>536	538	S114, S102105
33	>538	589	S102105
34	603	666	S9396, S1430, S1428, S105108
35	>666	694	S1430, S1428, S105108, S7476, S7679, S6669, S6366
36	>694	699	S1428, S105108, S7476, S7679, S6669, S6366
37	>699	706	S105108, S7476, S7679, S6669, S6366, S7379, S8689
38	>706	755	S7476, S7679, S6669, S6366, S7379, S8689, S3655
39	>755	756	S7679, S6669, S6366, S7379, S8689, S3655
40	>756	758	S6669, S6366, S7379, S8689, S3655, S6063
41	>758	779	S7379, S8689, S3655, S6063, S9496
43	>800	829	S3655, S6063, S9496
44	>829	836	S6063, S9496
45	>836	860	S9496
46	870	860	S6369, S8992
47	>961	860	S8992, S8789, S3640, S115
48	>1036	1060	S8789, S3640, S115
49	>1060	1093	S3640, S115
50	>1093	1096	S115
51	1209	1336	S7479
52	1613	1782	S128, S130
53	>1782	1856	S130
54	2089	2308	S212, S3755
55	>2380	2523	S3755, S3740
56	>2523	2774	S3740
57	8122	8977	S3645
58	10297	11381	S28