The Hong Kong Polytechnic University

Department of Electronic and Information Engineering

Design Optimization of Switching Voltage Regulators with Power Factor Correction

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CERTIFICATE OF ORIGINALITY

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_____ (Signed)

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Publications

Conference Papers

1. M. K. H. Cheung, M. H. L. Chow and C. K. Tse, "Design of a 1 kW PFC Power Supply Based on Reduced Redundant Power Processing Principle," *IEEE Power Electronics Specialists Conference,* Jeju, Korea, 3128-3134, June 2006.

2. M. K. H. Cheung, M. H. L. Chow and C. K. Tse, "Performance Considerations of PFC Switching Regulators Based on Non-Cascading Structures," *IEEE Power Electronics Specialists Conference,* Jeju, Korea, pp. 1236-1242, June 2006.

3. M. K. H. Cheung, M. H. L. Chow and C. K. Tse, "An Analog Implementation to Improve Load Transient Response of PFC Pre-regulators," *International Telecommunications Energy Conference, (INTELEC'07),* Rome, Italy, pp. 848-855, September 2007.

Journal Papers

1. M. K. H. Cheung, M. H. L. Chow and C. K. Tse, "Practical Design and Evaluation of a 1 kW PFC Power Supply Based on Reduced Redundant Power Processing Principle," *IEEE Transactions on Industrial Electronics,* vol. 55, no. 2, pp. 665-673, February 2008.

2. M. K. H. Cheung, M. H. L. Chow and C. K. Tse, "Design and Performance Considerations of PFC Switching Regulators Based on Noncascading Structures," to appear in *IEEE Transactions on Industrial Electronics.*

To my parents

Abstract

In general, a switching regulator with power-factor-correction (PFC) is composed of a PFC pre-regulator and a voltage regulator in order to satisfy both low input harmonic current distortion and fast voltage regulation simultaneously. The simplest approach to construct the switching regulator is to cascade the PFC pre-regulator with the voltage regulator. The input power of the switching regulator is processed by the PFC pre-regulator and the voltage regulator serially, so the efficiency of this switching regulator is inevitably deteriorated. Although the noncascading connection between the PFC pre-regulator and the voltage regulator is an effective method for constructing efficient switching regulators which can satisfy the relevant regulatory requirements for harmonic emissions, there is a lack of detailed discussion on the analyses of the achievable performances of different types of noncascading PFC switching regulators. This thesis presents the theoretical analysis with simulation results of the achievable performances of different types of noncascading PFC switching regulators and discusses the design aspects of implementing two types of noncascading PFC switching regulators at different output power levels. The particular design considerations such as the gained efficiency, the input current harmonics, and the size of the energy storage for load voltage regulation of each type of noncascading PFC switching regulators are discussed. This thesis also investigates the output load transient characteristics of PFC pre-regulators. The cause of sluggish load transient response of PFC pre-regulators is explained and an analog implementation to accelerate the load transient response without degrading the quality of the input current of PFC pre-regulators is proposed. Experiments are conducted to validate the analog implementation that provides sufficient improvement in the load transient response of PFC pre-regulators. An analytical approach to calculating the relationship between the inductor current, the output capacitance, and the output voltage ripple of continuous-conduction-mode (CCM) boost PFC pre-regulators is presented and some dynamic characteristics of output voltage are studied for different waveshapes of the input current.

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Preface

Harmonic current emission is one of the power quality issues arising from the public electricity networks. Huge non-resistive loads such as silicon-controlled rectifier (SCR) switched loads and switching regulators draw pulsating input current from the ac mains. Thus, harmonic currents at multiples of the ac mains frequency are inevitably generated. As a consequence, uncontrollable voltage variations of the ac mains, e.g., voltage sag, are resulted. This is because finite impedances of transmission lines of the public electricity networks with the harmonic current are creating a corresponding voltage distortion in the ac mains. Significantly, the third harmonic current generated by the non-resistive loads can cause overheating of the neutral conductor in a three-phase system, which is the most common system for transmitting electricity. Agencies such as the International Electrotechnical Commission (IEC) and the Institute of Electrical and Electronics Engineers Inc. (IEEE) have proposed their standards to promote the limits of harmonic current emission from consumers of the public electricity networks. Undoubtedly, efficient electricity usages have become one of the major concerns for the consumers due to increasing energy prices. In general, a switching regulator is composed of a power-factor-correction (PFC) pre-regulator and a voltage regulator to satisfy both low input harmonic current distortion and fast voltage regulation simultaneously. The input power of the switching regulator is processed by the voltage regulator to follow the PFC pre-regulator, so the efficiency of this switching regulator is inevitably deteriorated by this cascading connection. For satisfying the limits of the harmonic emissions and the need of the consumers, tremendous amount of research works have been devoted to the design of specific noncascading PFC switching regulators. However, there is a lack of detailed discussion on the analyses of achievable performance of noncascading PFC switching regulators and little investigation on the performances of PFC pre-regulators drawing imperfect sinusoidal input current.

The purpose of this study is to optimize the design of switching regulators with PFC. The study can be divided into two phases. The first phase studies the achievable performances of the noncascading PFC switching regulators. These achievable performances are efficiency, input current harmonic distortion, and size of the energy storage element for the voltage regulation. Noncascading PFC switching regulators can be classified into three categories and each category represents a

different possibility of the achievable performances of noncascading PFC switching regulators. The first category permits a tradeoff between the efficiency and the achievable power factor, the second permits a tradeoff between the efficiency and the size of the energy storage element for load voltage regulation, and the third allows a tradeoff among all the achievable performances. Analyses have been performed on noncascading PFC switching regulators of different categories. Examples of each categorized switching regulator are provided to illustrate their achievable performances. After that, an investigation is conducted in a single-phase noncascading PFC switching regulator that comprises a current-fed full-bridge converter and a buck-boost converter, both converters being operated in continuous-conduction-mode (CCM), for serving 1 kW output power. According to the pervious classification, this switching regulator belongs to the second category. The details of practical consideration in designing this noncascading PFC switching regulator are discussed. The achievable performances of the noncascading PFC switching regulator are verified with experimental results.

The second phase focuses on the subject of a crucial component, PFC pre-regulator, of PFC switching regulators. The investigation begins with discussing the sluggish load transient response of PFC pre-regulators and studies a simple and cost-effective analog implementation to accelerate the load transient response. The implementation involves inserting a notch filter between the voltage sensing network of the PFC pre-regulator and the voltage control loop of the PFC pre-regulator control circuitry. The improved load transient response of the implementation is observed experimentally. Afterwards, the investigation has gone one step further to analyze a CCM boost pre-regulator under average current-mode control. The analysis exposes the relationship between the reduced output ripple voltage and the dynamic characteristics of the output voltage of the CCM boost converter which is controlled by a standard average current-mode controller that maintains an imperfect sinusoidal input current, but still complies with the IEC 61000-3-2 Class D limit.

The main contributions of this thesis can be summarized as follows:

1. A thorough study into the achievable performances for different types of noncascading PFC switching regulators has been performed.

2. Based on the findings, the design and implementation of two types of noncascading PFC switching regulators have been presented from a circuit design perspective, along with experimental verification. Two prototypes under Category 2 and Category 3 have been constructed for different power level applications.

3. A simple and cost-effective circuit implementation that can be applied in accelerating the load transient response of PFC pre-regulators has been proposed and the effect of the implementation has been verified.

4. A detailed study regarding the input current and the output voltage characteristics of the CCM

boost pre-regulator has been conducted to formulate a systematic design procedure such that a waveshape manipulation of the input current can be traded off for improved dynamic response of the CCM boost pre-regulators.

This thesis is divided into seven chapters. In Chapter 1, the definitions of power factor (PF) and the total harmonic current distortion (THD) are explained. The latest international standards related to current harmonic control in the electricity networks in Europe and the United States are also reviewed. In addition, a brief review of the United States, joint saving energy programs, ENERGY STAR and 80 PLUS, is summarized. Chapter 2 gives a brief overview of different methods to achieve PFC. The essential components and their functions of a PFC switching regulator are described. A comprehensive literature review on various noncascading PFC switching regulators is provided. A useful tool, namely, power flow diagrams, which describes the noncascading PFC switching regulators is introduced. Chapter 3 investigates achievable performances of the noncascading PFC switching regulators in terms of efficiency, input current harmonic distortion, and size of energy storage element for load voltage regulation. The exploration begins with the power flow diagrams, based on which the noncascading PFC switching regulators can be classified into three categories, each offering a different possibility of the achievable performances. The achievable performances of each type of PFC switching regulators are investigated in detail. Chapter 4 discusses some practical issues associated with the design of a specific noncascading PFC switching regulator providing 1 kW output power. A current-fed full-bridge converter and a buck-boost converter are employed as a PFC pre-regulator and as a voltage regulator, respectively. Some practical problems related to implementation of these two converters are discussed. Chapter 5 examines the sluggish load transient response issue of PFC pre-regulators and provides a simple implementation to improve the load transient response. Chapter 6 studies the output voltage characteristics, steady state and transient state, of the CCM boost PFC pre-regulator drawing imperfect sinusoidal input current. This in turn allows the output regulation of the CCM boost PFC pre-regulator to be tightened while the input current waveform still satisfies the IEC 61000-3-2 Class D limit. Chapter 7, the final chapter, concludes the thesis by re-stating the theoretical and practical results that have been given to optimize the design of switching regulators with PFC. The various areas of future works are highlighted.

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Chapter 1

Introduction

1.1 Effects of Power Electronic Loads

The information system department informed a facility manager that an additional computer servers would be installed and would be powered by an existing panel board, therefore an analysis of the panel board and loading needs would be performed [1]. After the facility manager reviewed the annual testing and maintenance report. The reading of loads are 99 A, 130 A, and 77 A for the phase conductors and 130 A for the neutral conductor. The loads after the addition of the computer servers were estimated to be 132 A, 182 A, and 101 A for the phase conductors and 197 A for the neutral conductor. In practice, the three-phase power system operating in an unbalance manner is usually expected. The anticipated neutral currents are 46 A for the present load and 71 A for estimating the revised load, respectively. However, the surprisingly high neutral current was more than the anticipated neutral current in the unbalanced phase conductors. In fact the cause of this problem was the presence of harmonic currents, which are generated by nonlinear loads. The effects of excessive harmonic currents in the three-phase power system causes overloaded neutral cables [2], damaged distribution transformers [3], and voltage distortions [4].

History [5] has shown that problems associated with the harmonic currents have tormented power system engineers since 1893, the beginning of the electric power industry. In 1916, Steinmetz published a book [6] that devoted considerable attention to the harmonic currents in three-phase power system. Triplen harmonic currents (e.g. 3^{rd}, 9^{th}, 15^{th}, 21^{th}, etc) caused by saturated iron in transformers and machines have been covered in the discussion. In 1988, Gruzs [7] conducted a survey of neutral currents in three-phase computer systems over 195 sites across the United States. The results of the survey showed that 22.6% of the sites had neutral current in excess of 100% of the phase current. Two parallel conductors for doubling the neutral ampacity were suggested by Gruzs to prevent overheating in the neutral conductor. In 1994, a survey was conducted in six buildings

of Texas A&M University to show the effects of excessive harmonic currents flowing in the neutral conductor [8]. A mean ratio of the neutral current to the phase current of 133.1% had been found. This high value of the neutral current was primarily contributed by triplen harmonic currents. Such high neutral current indicated that the dominant load was single-phase power electronic load.

According to Clemmensen [9], the power quality problem in the United States causes about USD 13.3 billion in damage per year. A partial portion of the power quality problems is related to harmonic currents, therefore a several billions dollars should be saved if the nonlinear loads drew harmonic-free current. An estimation has been presented by Pileggi *et al.* [10] that in 1990, the cumulative present worth of the cost of harmonics was USD 2.00 per kVA at non ac mains frequency for feeders that did not need to install filters for reducing the harmonic current. However, when the filters must be installed by the electric providers to meet the IEEE std. 519-1992, the cost will jump one or two orders of magnitude. Based on the estimation, the harmonics currents generated by nonlinear loads in excess of 100 kVA (non ac mains frequency) can be cost-effectively filtered at the terminals of each nonlinear load. However, smaller nonlinear loads, less than 10 kVA (non ac mains frequency), cannot be economically filtered by individual filter units. A study showed that a boost type power-factor-correction (PFC) pre-regulator, built into the common electronic equipment switching regulator, was a cost-effective solution based on energy loss considerations alone [11]. A cost-benefit analysis compares the estimated cost of adding the PFC pre-regulator to the switching regulator to the potentially avoided cost of harmonic-related losses in the power system. The result showed that in a 60 kW office computer load, the PFC pre-regulator can save USD 2101 per year. PFC pre-regulators hold great promise for achieving cost saving and harmonic-free current in the switching regulators.

1.2 Harmonic Current Generation

Nowadays the most common sources of harmonic current are power electronic loads [12] such as personal computers, electrical appliances, electronic ballasts for compact fluorescent lamps, adjustable-speed motor drives over the entire range from watts to megawatts, battery chargers, and electronic control of a large variety of industrial loads. An example of a common circuit that produces harmonic current is a simple bridge rectifier with a capacitor input filter, which converts ac power from the ac mains to service a dc load, as shown in Fig. 1.1. The capacitor filters the ripple in the rectified voltage and provides a smooth dc voltage for the dc-dc converter. When the voltage supplied by the ac mains drops below the voltage of the capacitor, the energy stored in the capacitor supports the dc voltage to the dc-dc converter for a short duration. Unfortunately, this simple and inexpensive ac-dc power supply suffers from a high harmonic current distortion. Because the capacitor is large and maintains

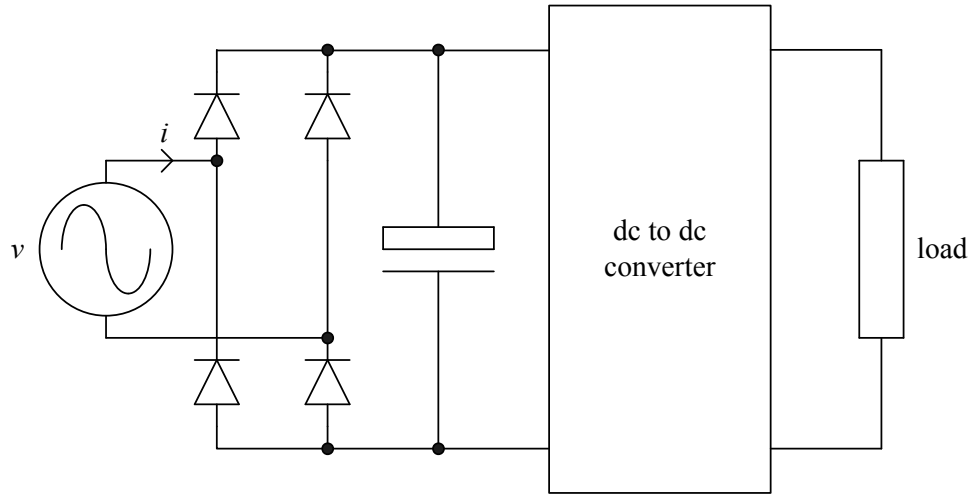


Figure 1.1: A simple bridge rectifier with capacitor input-filtered ac-dc power supply.

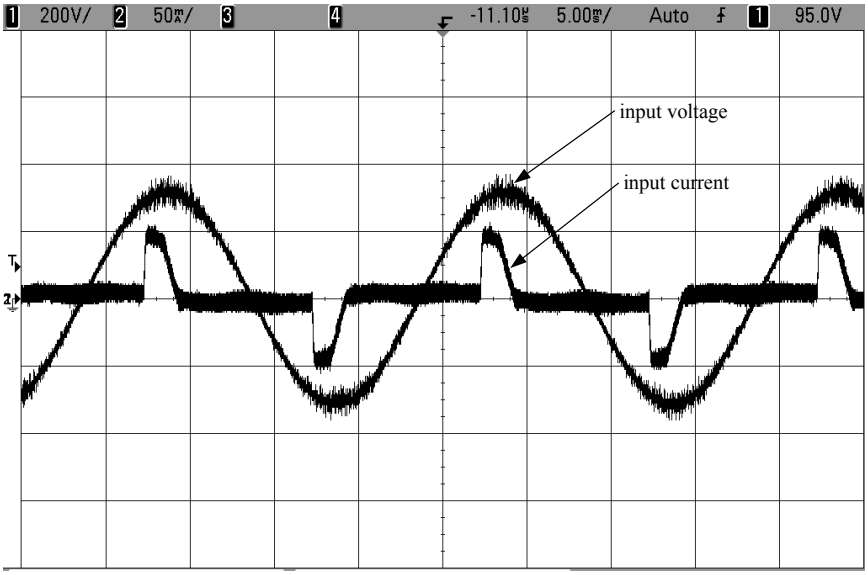


Figure 1.2: Measured input voltage and input current of the capacitor input-filtered ac-dc power supply.

a nearly constant voltage, the bridge rectifier turns on only for a short time when the input voltage is close to its peak resulting in peaky input pulse of the short duration as shown in Fig. 1.2. The harmonic currents contained in the input current are displayed in the harmonic spectrum as shown in Fig. 1.3.

Evaluation of the distortion of a periodic current waveform is by measuring the total harmonic distortion (THD) of the current. The THD is defined as the ratio of the root-means-square (rms) value of the current waveform not including the fundamental, to the rms fundamental magnitude. This can

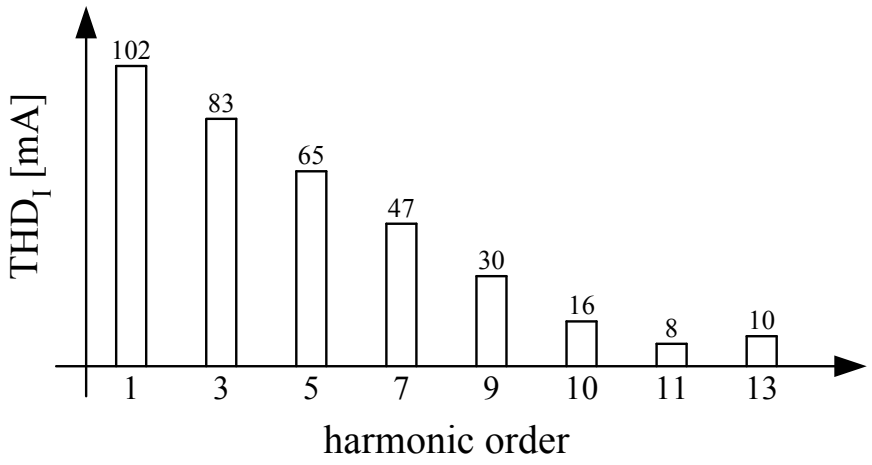


Figure 1.3: Measured total current harmonic distortion of the capacitor input-filtered ac-dc power supply.

be written as

$$\text{THD} = \frac{\sqrt{\sum_{\text{n}=2}^{\infty} I_{\text{n}}^2}}{I_1}. \tag{1.1}$$

The highly distorted current waveform as shown in Fig. 1.2 contains significant harmonic components, therefore the input current THD of the example circuit could easily exceed 100%. Referring to (1.1) and the measured harmonic current shown in Fig. 1.3, the THD of the example circuit is 119%.

1.2.1 Definition of Power Factor

The term power factor (PF) is borrowed from elementary ac circuit theory. The PF shows how effectively energy is transmitted between a power source to loads. Consider a load drawing a current i_{l} from the ac mains with voltage v_{l}. Both i_{l} and v_{l} are sinusoidal waveforms with period T_{l}. In this case, the PF is defined by

$$\begin{aligned} \text{Power Factor} &= \frac{P_{\text{ave}}}{V_{\text{lrms}} I_{\text{lrms}}} \\ P_{\text{ave}} &= \frac{1}{T_{\text{l}}} \int_0^{T_{\text{l}}} v_{\text{l}} i_{\text{l}} dt \\ V_{\text{lrms}} &= \sqrt{\frac{1}{T_{\text{l}}} \int_0^{T_{\text{l}}} v_{\text{l}}^2 dt} \\ I_{\text{lrms}} &= \sqrt{\frac{1}{T_{\text{l}}} \int_0^{T_{\text{l}}} i_{\text{l}}^2 dt} \end{aligned} \tag{1.2}$$

where P_{ave} is the average power drawn form the load, V_{lrms} and I_{lrms} represent the rms line voltage and line current, respectively, and $\int_0^{T_{\text{l}}}$ is the integral over any continuous interval of time length

T_1. Based on (1.2), a phase shift between the fundamental frequency of i_1 and v_1 occurs or a non-sinusoidal current is drawn by the load, or both. Therefore, the PF can be lower than unity. To fully describe the PF, (1.2) can be rewritten as

$$\text{Power Factor} = \text{PF}_{\text{disp}}\text{PF}_{\text{dist}} \tag{1.3}$$

where PF_{disp} and PF_{dist} are the displacement factor and the distortion factor, respectively. The displacement factor is defined as

$$\text{PF}_{\text{disp}} = \frac{P_{\text{ave}}}{V_{\text{Frms}} I_{\text{Frms}}} = \cos\theta \tag{1.4}$$

where V_{Frms} and I_{Frms} are the rms value of the fundamental voltage and the rms value of the fundamental current, respectively, and θ is the phase angle between these two fundamental components. The distortion factor relates to the frequency-domain problem. A periodic distorted current signal, i_{lD}, is represented by Fourier series with a fundamental angular frequency of ω as shown below

$$i_{\text{lD}} = I_{\text{lD}} + \sum_{\text{n}=1}^{\infty} a_{\text{n}} \cos \text{n}\omega t + b_{\text{n}} \sin \text{n}\omega t \tag{1.5}$$

where a_{n}, b_{n}, and I_{lD} are

$$a_{\text{n}} = \frac{1}{\pi}\int_0^{2\pi} i_{\text{lD}} \cos \text{n}\omega t dt \tag{1.6}$$

$$b_{\text{n}} = \frac{1}{\pi}\int_0^{2\pi} i_{\text{lD}} \sin \text{n}\omega t dt \tag{1.7}$$

$$I_{\text{lD}} = \frac{1}{2\pi}\int_0^{2\pi} i_{\text{lD}} dt \tag{1.8}$$

If the distorted current is an even function or an odd function, a_{n} must be zero. Therefore, the series becomes

$$i_{\text{lD}} = I_{\text{lD}} + I_1 \sin\omega t + I_2 \sin 2\omega t + \ldots \tag{1.9}$$

where I_{lD} is the dc current and I_1 is the fundamental component of i_{lD}. Because only fundamental current can contribute to average power, the distortion factor is defined as

$$\text{PF}_{\text{dist}} = \frac{I_1}{i_{\text{lD}}} \tag{1.10}$$

If the distorted current contains no dc component, then the distortion factor can be rewritten as

$$\frac{I_1}{i_{\text{lD}}} = \frac{1}{\sqrt{1 + \text{THD}^2}} \tag{1.11}$$

Fragmenting PF into two different factors is useful. If the load is reactive and nonlinear the input current can be both phase shifted and distorted. These two problems require entirely different solutions. For example, if a power system is heavily loaded with inductive (reactive) load, it will be compensated by installing suitable parallel capacitors to improve the phase shift between the system voltage and the current. However, a nonlinear load requires a different solution as will become clear in the next chapter.

1.3 Limits of Harmonic Current Emission

Harmonic pollution must be kept below certain limits. Most countries have their own regulatory standards or recommendations to control the levels of harmonic currents injected into the power system according to their local conditions. In this globalized economic era, the need for equipment manufactured in one country to comply with standards in another country has prompted efforts in formulating international standards for harmonic current emissions. A number of countries have collectively started applying similar harmonic current limits through the adoption of international standard or recommendation such as IEC 61000-3-2 [13] and IEEE std. 519-1992 [14].

1.3.1 European Standard

The International Electrotechnical Commission (IEC) adopted a philosophy of requiring manufacturers to limit their products consumption of current harmonics. IEC 61000-3-2 is described by the IEC as one that "specifies limits for harmonic current emissions applicable to electrical and electronic equipment having an input current up to and including 16 A per phase and intended to be connected to public low-voltage distribution systems." The tests according to this standard are type tests and test conditions for particular equipment are stated in the standard. For systems with nominal voltage less than 220 $\mathrm{V_{rms}}$ (line to neutral), the limits have not yet been considered. The effect of this standard started on 1^{st} January 2001 in the European Union, therefore the limit of harmonic current emissions is an enforcement.

1.3.1.1 Classification of Equipment

In IEC 61000-3-2, for the purpose of harmonic current limitation, equipment can be grouped into four classes as shown below:

Class A: Balanced three-phase equipment; household appliances, excluding equipment identified by Class D; tools excluding portable tools; dimmers for incandescent lamps; audio equipment; everything else that is not classified as Class B, Class C, or Class D.

Class B: Portable tools; arc welding equipment which is not professional equipment.

Class C: Lighting equipment.

Class D: Equipment must have power level 75 W up to and not exceeding 600 W. Personal computers, personal computer monitors, and television receivers are classified into this class.

1.3.1.2 Harmonic Current Limits

The original version of IEC 61000-3-2 was published in 1995 and the major modification of the standard has been performed in October 2001. The major change in the modified standard is how to classify Class D equipment. In the original version, Class D was applied to equipment with a special waveform that fitted a template defined by the IEC, however, in the modified version, this input current waveform template has been removed. IEC 61000-3-2 stated that the harmonics of the input current generated by the classified equipment shall not exceed certain harmonic current levels. The maximum permissible harmonic current levels are summarized in Table 1.1. For Class A equipment, the harmonics of the input current shall not exceed the absolute values given by the IEC. In Class B equipment, the maximum permissible harmonic current values are equal to the values of Class A multiplied by a factor of 1.5. The harmonic current limits of Class C equipment shall not exceed the relative limits given in the fourth column in Table 1.1. The maximum permissible harmonic currents of Class C are expressed as a percentage of the fundamental input current. For Class D equipment, the harmonic currents shall not exceed the values that can be derived from the fifth column in Table 1.1. Only odd harmonic currents are considered in Class D and the maximum permissible harmonic currents are defined as milliampere per watt. Furthermore the maximum harmonic currents of Class D equipment shall not exceed the absolute values shown in the last column in Table 1.1.

Table 1.1: Harmonic limits for different classes of equipment.

	Maximum permissible harmonic currents				
Harmonic order (n)	Class A (A)	Class B (A)	Class C (% of fundamental)	Class D (mA/W)	Class D (A)
3	2.30	3.45	$30\times\lambda^*$	3.4	2.30
5	1.14	1.71	10	1.9	1.14
7	0.77	1.155	7	1.0	0.77
9	0.40	0.60	5	0.5	0.40
11	0.33	0.495	3	0.35	0.33
13	0.21	0.315	3	3.85/13	0.21
$15\leq$ n ≤ 39	2.25/n	3.375/n	3	3.85/n	2.25/n
2	1.08	1.62	2	-	
4	0.43	0.645	-	-	
6	0.30	0.45	-	-	
$8 \leq$ n ≤ 40	1.84/n	2.76/n	-	-	
λ^* is the circuit power factor.					

1.3.2 The United States Standard

The Institute of Electrical and Electronics Engineers Inc. (IEEE) proposed a recommendation, which states that "IEEE std. 519-1992 IEEE recommended practices and requirements for harmonic control in electrical power system [14]." The recommendation sets the limits to both the voltage and current harmonics. It is an update of a previous IEEE std. 519-1981. In reality, the recommendation aims to balance between economic factors and the effectiveness of the harmonic control. The recommendation attempts to reduce the harmonic effects at any point in the entire power system by establishing limits on certain harmonic indices at the point of common coupling (PCC), which is a point of metering. In other words, the responsibility to reduce the current harmonics lies equally with the electricity providers and the consumers. However, the harmonic currents of the power system seen from the PCC often are not known accurately. Good engineering judgments are required on a case-by-case basis, and this recommendation in no way overrides such judgments.

1.3.2.1 Current Distortion Limits for Consumer

The philosophy of the recommended practice is to limit the harmonic injection from individual consumers so that they will not cause unacceptable voltage distortion levels under normal system operation. The recommendation restricts harmonic current emissions of the consumers to a relative value derived from the short circuit current, I_{sc}, at the PCC and the size of the consumer's non-linear load. Based on these limits, as the size of the user load decreases with respect to the size of the power sys-

Table 1.2: Current distortion limits for general distribution system (120 V through 69 kV)

Maximum harmonic current distortion in % of I_{L}						
	Individual odd harmonic order (n)					
$I_{\mathrm{sc}}/I_{\mathrm{L}}^{*}$	< 11	$11 \leq \mathrm{n} < 17$	$17 \leq \mathrm{n} < 23$	$23 \leq \mathrm{n} < 35$	$35 \leq \mathrm{n}$	TDD
< 20	4.0	2.0	1.5	0.6	0.3	5.0
$20 < 50$	7.0	3.5	2.5	1.0	0.5	8.0
$50 < 100$	10.0	4.5	4.0	1.5	0.7	12.0
$100 < 1000$	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0

Even harmonics are limited load current (15 to 30 min. demand).
Current distortion that result in a dc offset are not allowed.
*All power generating equipment is limited to these values regardless of actual $I_{\mathrm{sc}}/I_{\mathrm{L}}$.
I_{sc} = maximum short-circuit current at PCC.
I_{L} = maximum demand load current at PCC.

tem, the percentage of harmonic current that the consumer is allowed to inject into the power system increases. The limits are recommended to be used as system design values for the worst case for normal operation. Normal operation is the operating condition lasting longer than an hour. For shorter periods, such as start-up or unusual conditions, the limits may be exceeded by 50%. Table 1.2 lists the harmonic current limits based on the size of the load with respect to the size of the power system to which the load is connected. The recommended current distortion limits are concerned with an index, total demand distortion (TDD), which is the rms of harmonic current distortion in percentage of maximum demand load current (15 or 30 min demand).

1.3.3 Comparison of Two Standards

As the IEC and the IEEE are two principally different approaches, for harmonic current limit, a comparison of these two standards is summarized here. For IEC 61000-3-2,

- The IEC standards set limits to the amount of emission of individual equipment.
- The responsibility lies with the manufacturers of polluting equipment.
- IEC documents mainly aims at small customers that do not have the means to choose between mitigation options.

For IEEE std. 519-1992,

- IEEE harmonic standard limits the emission per consumer.
- The responsibility lies with the consumer who may decide to install filters instead of buying better equipment.
- IEEE standard aims at regulating the connection of large industrial consumers.

1.4 Efficient Electrical Usage Programs

On 12^{th} October 2007, the Norwegian Nobel Committee decided that the Nobel Peace Prize for 2007 is to be shared by two parties equally, the Intergovernmental Panel on Climate Change (IPCC) and Albert Arnold (Al) Gore Jr., for their efforts to build up and disseminate greater knowledge about human-made climate change, and to lay the foundations for the measures that are needed to counteract such change [15]. Greenhouse gas is one of the elements that leads the global climate change. Efficient electrical usage is a very effect strategy for reducing greenhouse gas emissions, and for saving money for electric bills [16]. ENERGY STAR is a joint program of the United States,

Environment Protection Agency (EPA) and the United States, Department of Energy helping people to save money and protect the environment through the use of energy efficient products and practices. 80 PLUS [17] is an innovative, electric-utility-funded incentive program to integrate more energy-efficient power supplies into desktop computers and servers.

1.4.1 ENERGY STAR

Since 1992, the United States EPA introduced ENERGY STAR as a voluntary labeling program designed to identify and promote energy-efficient products to reduce greenhouse gas emissions. Based on achievements from ENERGY STAR [16], USD 16 billion electric bills in the U.S. have been saved in 2007 due to the use of ENERGY STAR labeled products. The first labeled products were computers and monitors. In 1995 the labeled products have been expended to office equipment and residential heating and cooling equipment. Nowadays, the ENERGY STAR label is on major appliances, office equipment, lighting, home electronics, and more. The label has also extended to cover new homes and commercial and industrial buildings.

1.4.1.1 Program Requirements for Single Voltage External Power Supplies

To join the ENERGY STAR label program, single voltage external power supplies must be qualified for a specification [18]. The goal of the specification is to recongnize power supplies with an efficient ac-dc or ac-ac conversion process. EPA has prepared detailed definitions of the power supplies and other related terms as relevant to ENERGY STAR such as active mode and no-load mode. To be eligible for ENERGY STAR qualification, the power supplies must meet or exceed a minimum aver-

Table 1.3: Energy-efficiency criteria for active mode

Output Power (P_{no})	Minimum average efficiency in active mode (expressed as a decimal)*
0 to $\leq$ 1 W	$\geq 0.49 \times P_{\mathrm{no}}$
$>$ 1 to $\leq$ 49 W	$\geq [0.09 \times L_{\mathrm{n}}(P_{\mathrm{no}})]$+0.49
$>$ 49 W	$\geq$ 0.84
P_{no} stands for output power. L_{n} refers to the natural logarithm. * The algebraic order of operations requires that the natural logarithm calculation be performed first and than multiplied by 0.09, with the resulting output added to 0.49. An efficiency of 0.84 in decimal form corresponds to the more familiar value of 84 % when expressed as a percentage.	

Table 1.4: Energy consumption criteria for no load mode

Output Power (P_{no})	Maximum power in no-load
0 to $<$ 10 W	$\leq$ 0.5 W
$\geq$ 10 to $\leq$ 250 W	$\leq$ 0.75 W

age efficiency for active mode, which varies based on the power supplies' nameplate output power. Table 1.3 outlines the equations for determining minimum average efficiency. For the no-load mode maximum power consumption levels are provided in Table 1.4. To continually recognize the most efficient single voltage external power supply on the market and reflect forthcoming improvements in technology, EPA plans to implement more energy-efficiency criteria for active mode and less energy consumption criteria for no-load mode.

1.4.2 80 PLUS

On 20^{th} July 2007, ENERGY STAR specification for power supplies servicing desktop computers and servers adopted 80 PLUS certificate. The specification of the power supplies to satisfy 80 PLUS certificate are summarized below:

Internal form factor: Qualified computer units have an internal power supply form factor and provide multiple dc voltage outputs such as 12 V, 5 V, 3.3 V, etc.

Energy efficiency: Power supplies have a minimum efficiency of 80 % when tested at each of the following load conditions: 20 %, 50 %, and 100 % of rated power supply output.

Power factor: Power supplies maintain a true power factor of 0.9 or greater at 100 % of rated power supply output.

1.5 Terminology

Some conventions and terms which will be used throughout this thesis should be noted.

- A pre-regulator refers to power-factor-corrected pre-regulator. The function of the pre-regulator is to shape the current to achieve power factor correction.
- A noncascading switching regulator refers to a system constituted by two converters for providing power factor correction and voltage regulation. The constituent converters are connected in different noncascading forms.

- A cascading switching regulator or a classical switching regulator refers to a system constituted by two converters for providing power factor correction and voltage regulation. The constituent converters are connected in serial form.
- For brevity, PFC is used to denote power factor correction, PF is used to denote power factor, and CCM and DCM are used to denote continuous-conduction-mode and discontinuous-conduction-mode, respectively.

1.6 Summary

In the first part of this chapter, the effects of power electronic loads on the power system are described. The most common ac-dc power supply that produces harmonic current is depicted and total harmonic current in this power supply is shown. The definition of total harmonic distortion in terms of the distorted periodic current waveform and its relation to the power factor are given. The updated standards of the harmonic current emissions in the European Union and the recommended practices and requirements for harmonic control in the United States are also reviewed. In addition, ENERGY STAR labeling program and 80 PLUS electric-utility-funded incentive program for promoting efficient electrical usage are introduced in this chapter. Some conventions and terms used in this thesis are defined.

Chapter 2

Overview of PFC Methods

For reducing the harmonic current injected into power systems, a power factor corrected circuit in any off-line power supply system is necessarily required. There are two approaches, namely, filtering techniques and input current controlling techniques, for achieving PFC in an off-line power supply system. A comprehensive overview of both PFC techniques in an off-line power supply system has been given by Redl [19]. The filtering techniques can be divided into passive filter circuits [20] and active filter circuits [21], [22]. The input current controlling techniques are achieved by a dc-dc converter with an appropriate control circuitry [23]. Theoretical aspects for switching regulators to achieve PFC and voltage regulation have been investigated by Tse [24]. A comprehensive review of improved PF converters including control approaches has been given by Singh *et al.* [25], [26]. Some helpful hints to select a PFC solution for low and medium power single-phase switching regulators have been suggested by Fernández *et al.* [27]. A survey has been performed by García *et al.* [28] to study a great number of the PFC circuits drawn with imperfect sinusoidal input current for satisfying an efficient power conversion. In this chapter, an overview of theoretical aspects, circuit topologies, control strategies, essential components of switching regulators and noncascading switching regulators are given.

2.1 Passive and Active Filters

A simple way to reduce the line current harmonics of a conventional diode bridge rectifier is to place an inductor in series with its output as shown in Fig. 2.1. The inductor L and the capacitor C are used to filter the line current harmonics. This simple passive filtering technique is easy to implement and it is typically more reliable and robust than active filtering techniques especially in high-power applications (over 1 MW output power level). But this standard filter can only provide 0.75 PF in resistive loading condition [29]. For further improvement of the PF and the line current total harmonic

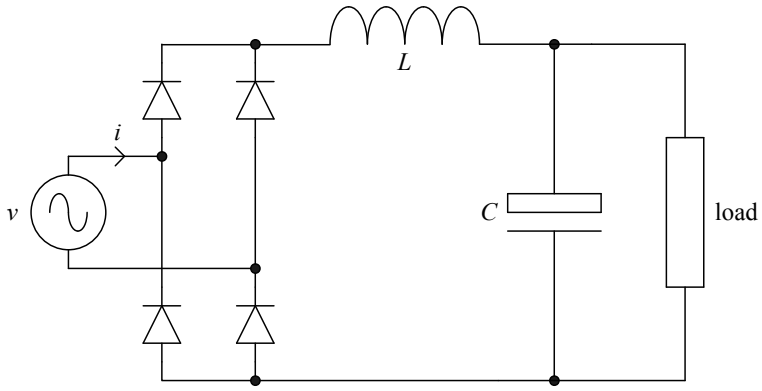


Figure 2.1: Conventional diode bridge rectifier with L-C filter.

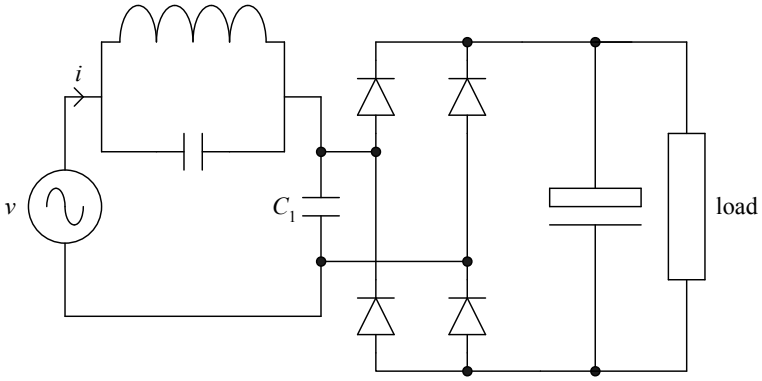


Figure 2.2: Single-phase diode bridge rectifier with improved L-C filter.

distortion, an improved passive filter has been proposed by Ji and Wang [30], as shown in Fig. 2.2. The proposed method is to place a resonant tank composed of a capacitor and an inductor between the ac mains and a bridge rectifier. This resonant tank presents infinite impedance to the third harmonic input current, therefore the third harmonic current is removed from the ac mains. A compensating capacitor C_1 is added in parallel with the bridge rectifier. It can compensate the reactive power, absorb the distortion power and improve the conversion efficiency. Experimental results showed that the maximum PF of this improved passive filter was 0.985 under 5 kW rated output power. However, heavy, bulky, and fixed compensation are the main disadvantages of these two passive filters.

An active filtering has become a common technology for harmonic current elimination and reactive power compensation in single-phase and three-phase (with or without neutral conductor) power systems with nonlinear loads. An active filter is applied to a group of power electronic circuits incorporating semi-conductor devices and passive energy storage elements. Many connected configurations, such as active series filter [31], [32], active shunt filter [33], [34], and combination of shunt and series filter [35] have been developed. Fig. 2.3 shows the block diagrams of the different config-

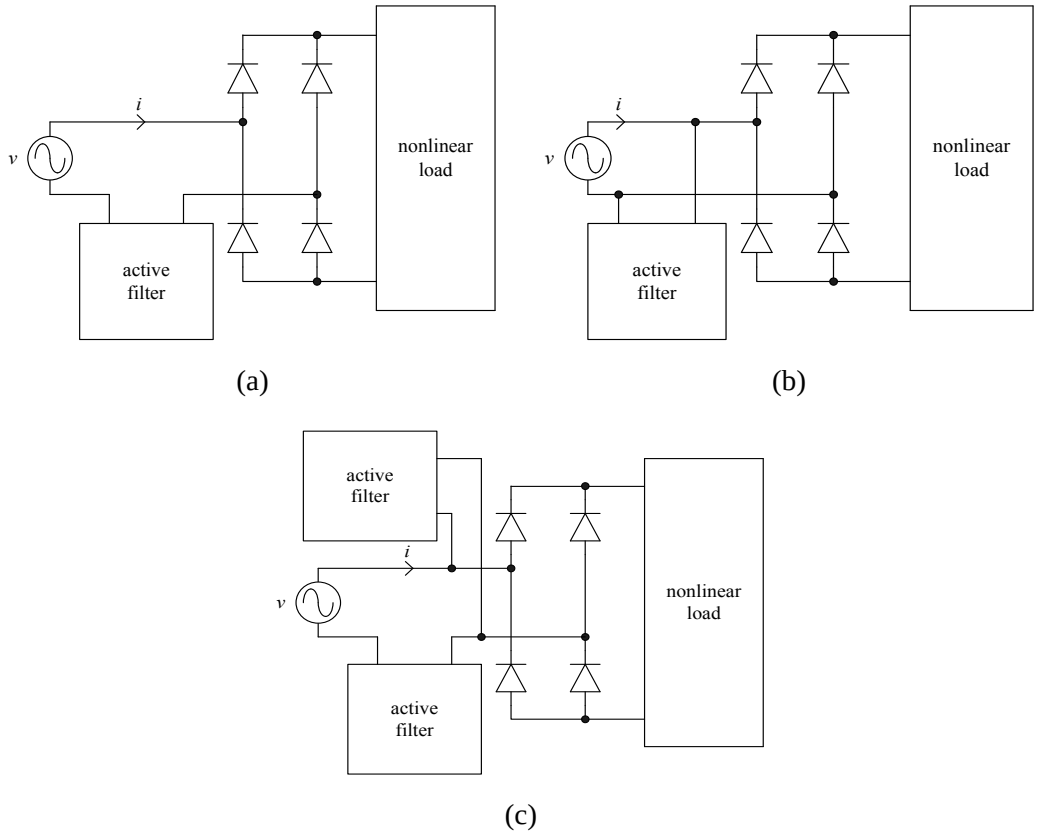


Figure 2.3: The block diagrams represent the active filter connection: (a) active series filter, (b) active shunt filter, and (c) combination of shunt and series filter.

urations of the active filter connections. The active series filter produces a voltage waveform which is added or subtracted to compensate the voltage distortion generated by nonlinear loads in order to maintain the ac mains voltage as a pure sinusoidal voltage. This active series filter is less commonly used in industry, because components of the active series filter have to handle high load current due to their serial connection. The active shunt filter is widely used in the industry. The purpose is to eliminate the nonlinear load current harmonics fed to the ac mains. It can also contribute to reactive power compensation and current balancing in the three-phase system. The power handling of the active shunt filter is relatively small compared to the active series filter, as the active shunt filter only compensates small amount of fundamental current to the ac mains. The combination of shunt and series filter can improve the voltage and current distortion of the ac mains, however the demand for this combined filter is limited due to their complexity and higher cost.

Obviously, the mentioned active filters provide a four-quadrant operation. It means that the filters are simultaneity required to inject or drain current at the positive and negative line cycle to achieve sinusoidal line current. Therefore the filters should have a minimum of four power switches

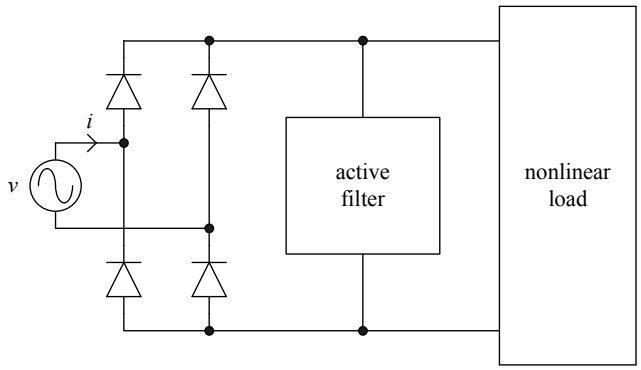


Figure 2.4: Active shunt filter connected in dc side for low-power applications.

and a complex control circuitry, and are only cost effective for high-power applications. However, in low-power application, an economical solution based on the well-known active shunt filter has been proposed [36]. Fig. 2.4 depicts the active shunt filter connection for low-power applications. The proposed active shunt filter is placed after a bridge rectifier, so the filter is designed for injecting or draining current at the rectified sinusoidal voltage to reduce the number of power switches and reduce the complexity of control circuitry.

2.2 Switching Regulator with PFC

Input current controlling techniques use a high switching frequency converter that shapes the averaged input current to an almost sinusoidal input current with a small amount of harmonic content. However, this high switching frequency converter cannot allow a tight regulated dc voltage at the same time that a high PF is achieved due to the energy imbalance between the instantaneous ac input power and the dc output power [19], [24]. Recently, ac-dc converters with PFC are being included in the text books [37], [38] and are reported in the power electronic industry [39]. The most common approach for ac-dc conversion with PFC and voltage regulation is shown in Fig. 2.5. Two converters compose the power chain. The front converter, known as pre-regulator, achieves a high PF and the followed converter, known as voltage regulator, obtains a fast output voltage regulation and they operate independently. The advantage of this straight-forward construction is that it is possible to match any set of particular specifications.

2.2.1 Energy Balance Consideration

An energy storage element is a necessary component in any PFC switching regulator. It provides energy balance between the pre-regulator and the voltage regulator. Assume that the input voltage of

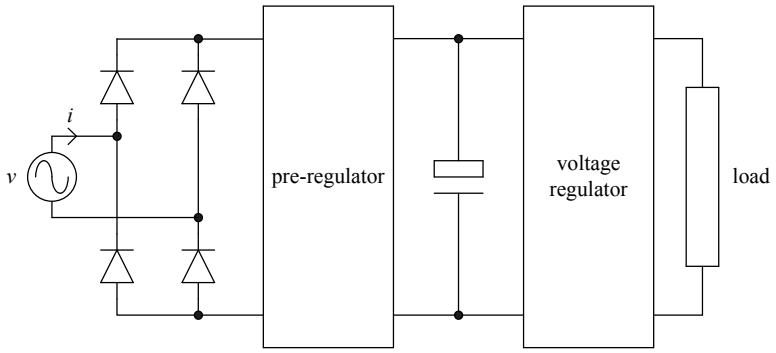
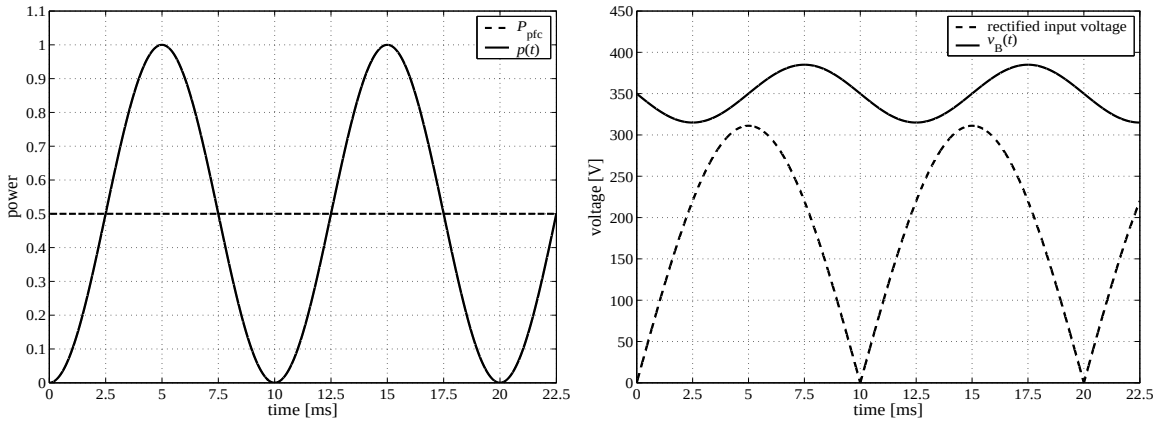


Figure 2.5: The most common approach for ac-dc power conversion with PFC and voltage regulation.



(a) (b)

Figure 2.6: (a) Waveforms of ideal pre-regulator input power and output power. (b) Waveforms of energy storage capacitor voltage, $v_{\rm B}(t)$ and rectified input voltage.

the pre-regulator is a rectified sinusoid, the PF is unity, and the output power of the voltage regulator is constant. Thus, the instantaneous input power of the pre-regulator is $p(t) = \hat{v}_{\rm in}\hat{i}_{\rm pfc}\sin^2 2\pi f_{\rm m}t$, where $\hat{v}_{\rm in}\sin 2\pi f_{\rm m}t$ and $\hat{i}_{\rm pfc}\sin 2\pi f_{\rm m}t$ are the input voltage and the input current of the pre-regulator, respectively, and $f_{\rm m}$ is the ac mains frequency. In the steady state, the output power, $P_{\rm pfc}$, of the pre-regulator is a constant and $\hat{v}_{\rm in}\hat{i}_{\rm pfc} = 2P_{\rm pfc}$. The power difference between the pre-regulator input terminal and output terminal is

$$p_{\rm B}(t) = 2P_{\rm pfc}\sin^2 2\pi f_{\rm m}t - P_{\rm pfc} = -P_{\rm pfc}\cos 4\pi f_{\rm m}t. \tag{2.1}$$

Fig. 2.6 (a) illustrates the waveforms of the instantaneous input power and the output power of ideal pre-regulator for 50 Hz ac mains frequency. The frequency of $p_{\rm B}(t)$ is twice of the ac mains frequency. An energy storage element absorbs energy in one-quarter of the ac mains period and releases the same amount of energy in the next quarter cycle. The energy stored in the energy storage element can be

calculated as

$$E(t) = \int p_{\mathrm{B}}(t)dt = -\frac{P_{\mathrm{pfc}}}{4\pi f_{\mathrm{m}}} \sin 4\pi f_{\mathrm{m}} t + \text{constant}. \tag{2.2}$$

From (2.2), "constant" is an arbitrary constant energy in the power balance condition between the input power and the output power of the pre-regulator. This constant energy maintains a constant voltage in a capacitive energy storage or a constant current in an inductive energy storage. If a capacitor serves as the energy storage element, the capacitor voltage, $v_{\mathrm{B}}(t)$, must fluctuate in order to provide the energy buffering action, that is $v_{\mathrm{B}}(t) = V_{\mathrm{B}} \pm \Delta v_{\mathrm{B}}$ where V_{B} is a static value and Δv_{B} is a ripple voltage varied at $2f_{\mathrm{m}}$. This voltage waveform of the capacitive energy storage is sketched in Fig. 2.6 (b) for 50 Hz ac mains frequency. The minimum and maximum values of $v_{\mathrm{B}}(t)$ occur when $\sin 4\pi f_{\mathrm{m}} t$ is equal to 1 and -1, respectively. The fluctuated energy (peak-to-peak) of the capacitor is given by

$$|\Delta E_{\mathrm{pp}}| = \frac{2P_{\mathrm{pfc}}}{4\pi f_{\mathrm{m}}}. \tag{2.3}$$

The energy stored in the capacitor is $\frac{1}{2}C_{\mathrm{B}}[(v_{\mathrm{Bmax}})^2 - (v_{\mathrm{Bmin}})^2]$ or $V_{\mathrm{B}}C_{\mathrm{B}}\Delta v_{\mathrm{B}}$, therefore the ripple voltage of the capacitor is

$$|\Delta v_{\mathrm{B}}| = \frac{P_{\mathrm{pfc}}}{2\pi f_{\mathrm{m}} C_{\mathrm{B}} V_{\mathrm{B}}}. \tag{2.4}$$

In this thesis, a capacitor serves as an energy storage element in a switching regulator and the capacitor voltage is defined as

$$v_{\mathrm{B}}(t) = V_{\mathrm{B}} - \frac{P_{\mathrm{pfc}}}{2\pi f_{\mathrm{m}} C_{\mathrm{B}} V_{\mathrm{B}}} \sin 4\pi f_{\mathrm{m}} t. \tag{2.5}$$

2.2.2 Pre-regulators

Pre-regulators are classified on the basis of topology and the type of converter used. The topology-based classification is categorized mainly as buck, boost, and buck-boost types. Some variant topologies such as Ćuk, Sepic, Sheppard-Taylor, and Zeta as pre-regulators are also included into the classification. The PFC performance of these topologies is affected by their operating modes, which is CCM or DCM, and control methods. The advantages of the buck-type pre-regulator are the limitation of the inrush current at start-up, ease of implementation of a short-circuit protection, and an inherent step-down voltage conversion. However the pulsed input current and inevitable line current distortion due to the notches around zero crossing of the line voltage cannot be overcome by the choice of operating mode and the control methods. The analyses of the buck-type pre-regulator are performed by Endo *et al.* [40]. The findings showed that the PF of the pre-regulator is over 0.9 in DCM by constant duty cycle operation. When the pre-regulator operated at CCM in the same constant duty cycle operation, the PF decreases to about 0.7. However, the PF of the CCM buck-type pre-regulator can be improved to over 0.9 by a sensing input current control method as shown in Fig. 2.7. A modified buck-type pre-regulator has been proposed by [41], as shown in Fig. 2.8. The proposed pre-regulator

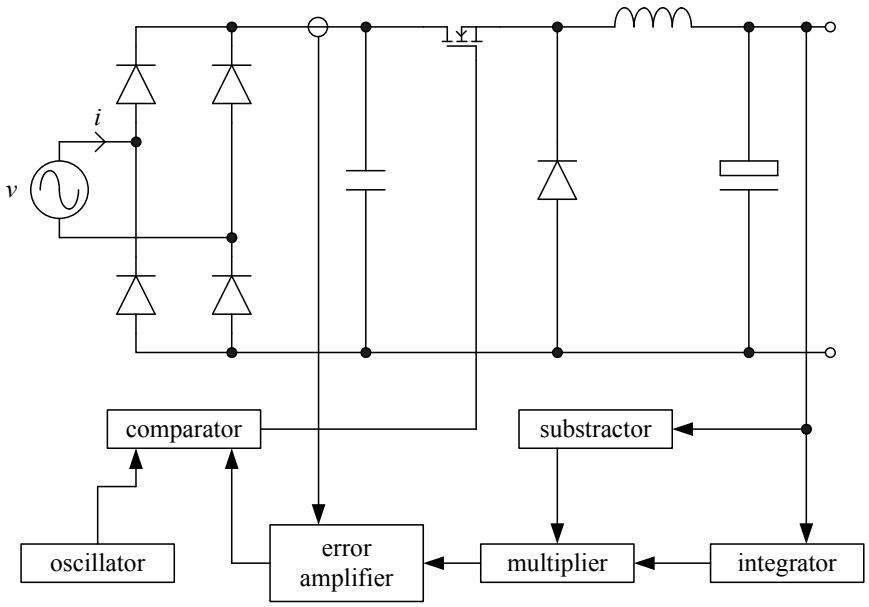


Figure 2.7: Input current sensing control method for buck-type pre-regulator.

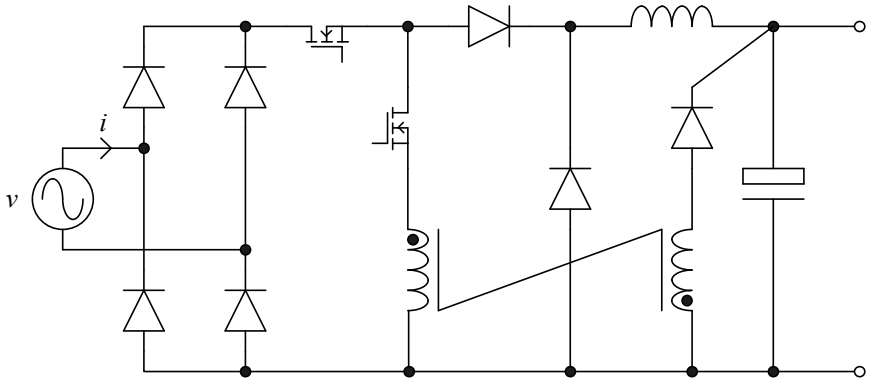


Figure 2.8: Integrated buck-flyback pre-regulator.

integrates a buck and a flyback stages to improve the input current notches around zero crossing of the line voltage. The flyback stage only operates when the input voltage is lower than the output voltage, therefore the input current notches can be filled by the flyback stage input current to improve the PF.

The most popular topology for PFC applications is the boost-type converter [42], as shown in Fig. 2.9 (a). In general, the boost-type pre-regulator offers a lowest current stress of the active switch comparing with any other topologies and uses a ground-reference switch. The main drawback of the boost-type pre-regulator is that the output voltage is always higher than the peak input voltage. Figs. 2.9 (b)-(d) depict the various configurations of such converter to provide PFC. A hybrid power module which replaces two grounded line rectifier diodes by two power switches was proposed by Martinez and Enjeti [43]. An interleaved boost-type pre-regulator has been discussed in [44]. The

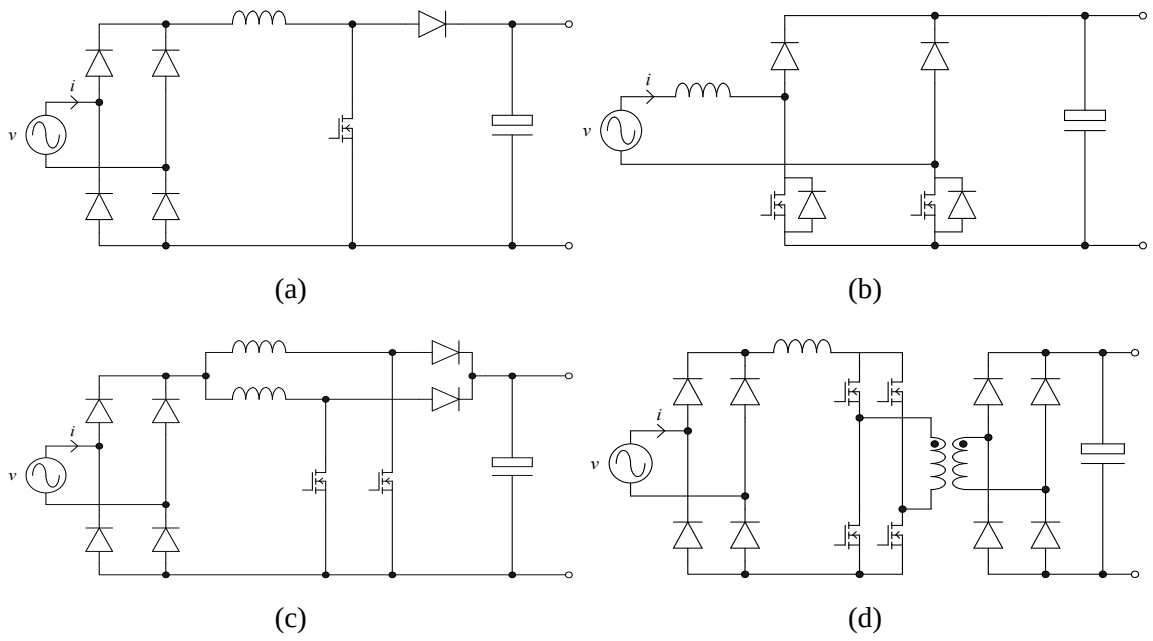


Figure 2.9: (a) Conventional boost-type pre-regulator. (b) Symmetrical two-devices boost-type pre-regulator. (c) Interleaved two-cell boost-type pre-regulator. (d) Isolated current-fed boost-type pre-regulator.

merit of this pre-regulator is that it increases the power density without reducing the efficiency, but an unequal current sharing in the pre-regulator inductors is generated. It can be solved by adding an extra sensing circuitry. An isolated current-fed boost pre-regulator is presented in [45]. Galvanic isolation and step-down voltage capability can be achieved by the high frequency transformer. However, the leakage inductance of the transformer that rings with the parasitic capacitance of the power switches will cause voltage spikes on the power switches resulting in high switching losses. To reduce the voltage spikes and increase the power conversion efficiency, a current-fed boost pre-regulator with zero current switching (ZCS) is proposed by Chen *et al.* [46]. In practice, cusp distortion in the boost-type CCM pre-regulator occurs just after the line voltage at zero crossing [47], as shown in Fig. 2.10. The cusp distortion generates current harmonic distortion of high order. The smaller inductance of the input inductor can improve the cusp distortion but it gives higher ripple current. Because the cusp distortion is a result of the topology of the pre-regulator, the input current distortion of the CCM boost-type pre-regulator cannot be eliminated by control methods. A detailed analysis of the effect of cusp distortion on the performance of the CCM boost-type pre-regulator in terms of PF and harmonic distortions was performed by Chow and Tse [48]. Specifically, the inductor current of the CCM boost-type pre-regulator is charged up during on-time by the input voltage. Since only the rectified voltage is connected to the input inductor when the power switch is turned on, the energizing rate of the inductor current is proportional to the rectified voltage. At the zero crossing voltage level,

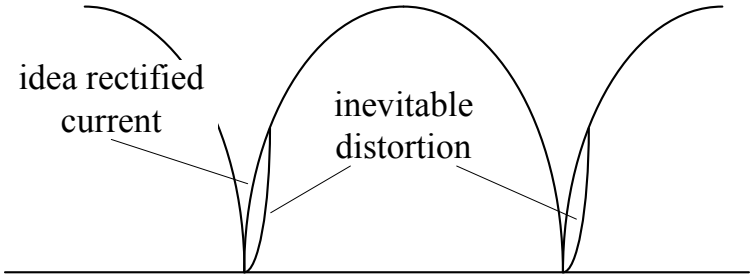


Figure 2.10: Cusp distortion in boost-type pre-regulator.

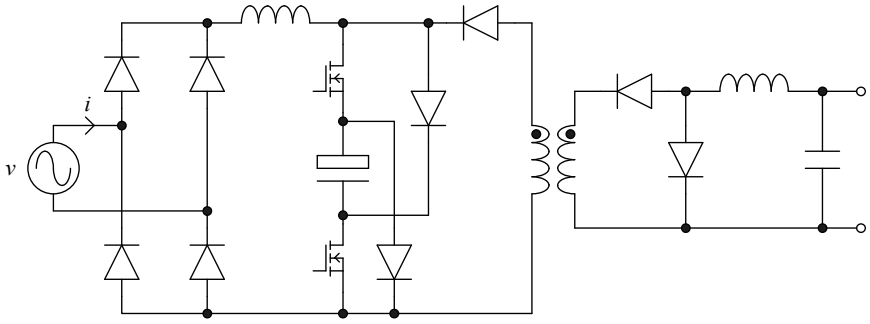


Figure 2.11: Sheppard-Taylor topology switching regulator with PFC and voltage regulation.

the rectified voltage is zero, giving zero current gradient. Therefore, it is impossible for the inductor current to catch up with the rectified input voltage. A solution to solve the cusp distortion by using Sheppard-Taylor topology was reported by Tse *et al.* [49], as shown in Fig. 2.11.

Since 1982 the CCM flyback converter has been used for PFC [50]. As usual, a common problem with the flyback pre-regulator is the leakage inductance of the high frequency transformer, which causes high turn-off voltage spikes. The problem is particularly serious for the high line voltage. Fig. 2.12 shows an active flyback pre-regulator which is presented by Watson *et al.* [51] to recycle the energy stored in the transformer leakage inductance, thereby reducing the voltage stress of the power switch.

For low-power applications, a converter operating in DCM is very commonly used in PFC. A simple DCM flyback converter operating without the current control loop presenting an resistive input characteristic has been discussed in detail [52] including design of the output voltage feedback loop. Simonetti *et al.* [53] has provided the theoretical analysis and shown the experimental results to illustrate the performance of Sepic and Ćuk converters working as pre-regulators in DCM. It should be noted that converters operating in DCM can automatically produce fairly good PF, but with a substantial amount of harmonic distortion on the line current for some topologies. A comparison of converter topologies operated in DCM for PFC has been reported in [54], [55]. Table 2.1 summarizes the averaged current drawn by the different converter topologies. DCM buck-boost-type pre-regulators give

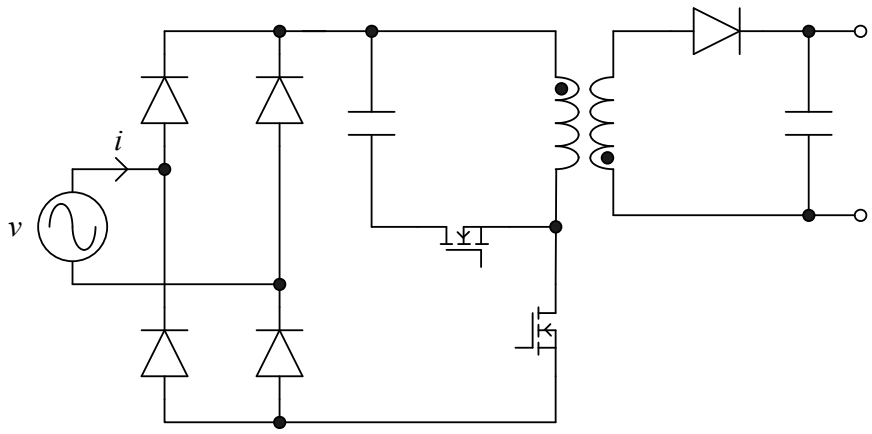


Figure 2.12: Active clamp flyback pre-regulator.

a perfect linear relationship between their input current and voltage, which can provide an excellent PFC property. The input characteristic of DCM boost-type pre-regulators is nearly linear when the output voltage, V_o, is substantially larger than the peak line voltage, $\hat{v}_{\rm in}$. Current waveform distortion of the DCM boost-type pre-regulator has been analyzed by Liu and Lin [56]. The input current of DCM Ćuk, Sepic, and Zeta pre-regulator contains a dc current, therefore their input current waveforms are inevitably subject to distortion. The input characteristic of DCM buck-type pre-regulators is linear only if the output voltage is equal to zero.

Pre-regulators operating in discontinuous capacitor voltage mode (DCVM) has been discussed in [57]. Applying the duality principle to generate DCVM pre-regulator has been presented by Tse and Chow [58]. Fig. 2.13 shows two simplified switching regulators using a boost pre-regulator cascading with a buck voltage regulator in DCM and DVCM, respectively. Briefly, in DVCM, the voltage across a certain capacitor becomes zero for a portion of a switching period. Based on the duality principle, DCVM pre-regulators are expected to have the same PFC property as their DCM

Table 2.1: Theoretical averaged input current of converters operating in DCM

Type of converter	Averaged input current
Buck	$\frac{D^2T_s}{2L}v_{\rm in}(t) - \frac{D^2T_s}{2L}V_o$
Boost	$\frac{D^2T_s}{2L}\frac{v_{\rm in}V_o}{V_o - v_{\rm in}(t)}$
Buck-boost	$\frac{D^2T_s}{2L}v_{\rm in}(t)$
Ćuk, Sepic, Zeta	$\frac{D^2T_s}{2L} + I_oD$
D = duty cycle, T_s = switching period, L = inductance of input inductor, $v_{\rm in}(t)$ = the line voltage, V_o = output voltage, and I_o = output current	

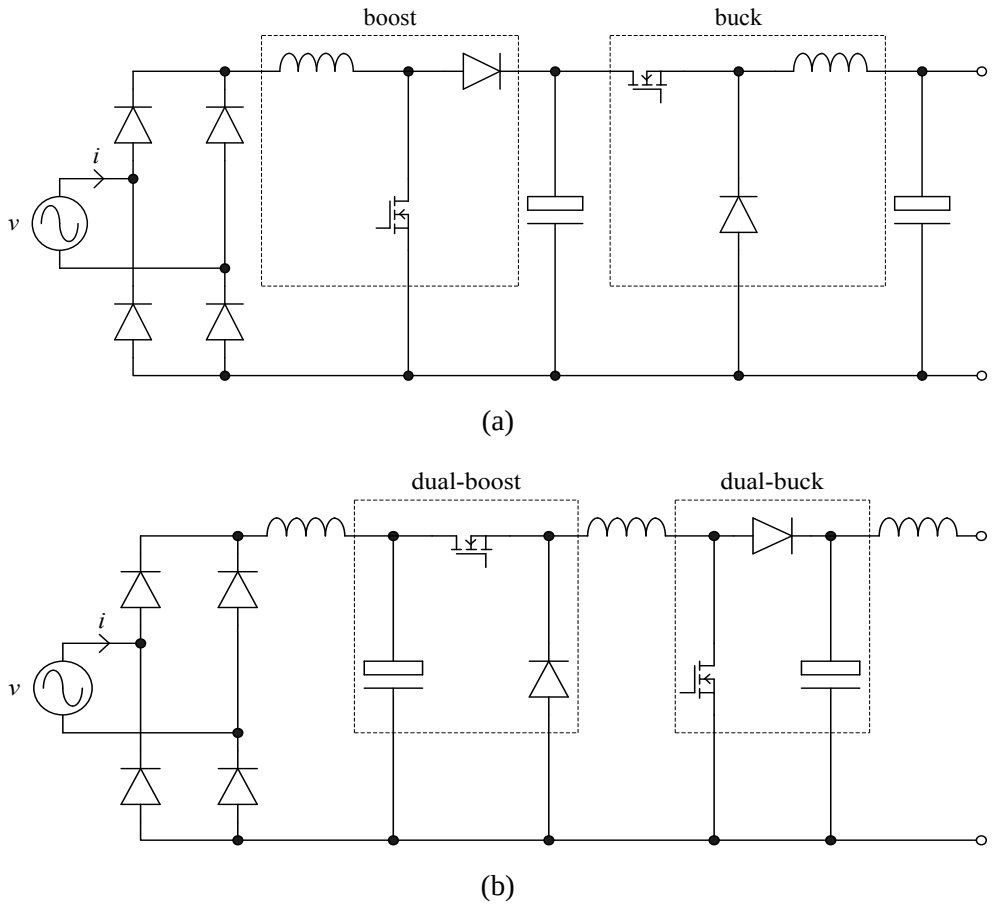


Figure 2.13: (a) Basic boost pre-regulator cascading with buck voltage regulator operated input inductor in discontinuous mode. (b) Dual circuit with input capacitor in discontinuous mode.

pre-regulators.

2.2.3 Control of Pre-regulator

Control methods are especially important in CCM operated pre-regulators. PFC operation of the CCM pre-regulators can be achieved by instantaneous monitoring and controlling the input current of the CCM pre-regulators using special control methods such as average current-mode control, peak current-mode control, hysteretic control and borderline control. However, Sivakumar *et al.* [59] proposed a method which can actively control the input current without current sensing. Fig. 2.14 shows the input current of a boost pre-regulator under various control schemes.

Average current-mode control tracks the inductor current with a high degree of accuracy [60], therefore the low harmonic current is achieved. Fig. 2.15 depicts the block diagram of the traditional average current-mode controller for pre-regulators. As the name implies, the inductor current of the

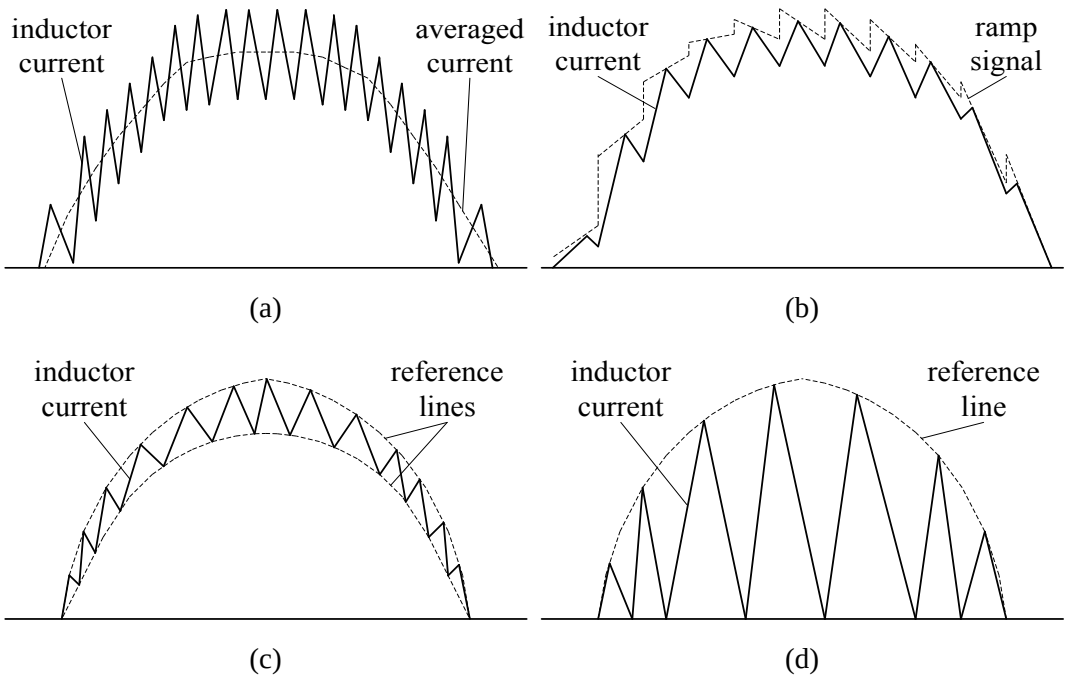


Figure 2.14: The input current of the boost pre-regulator under the different control (cusp distortion is omitted for brevity). (a) Average current-mode control. (b) Peak current-mode control. (c) Hysteretic control. (d) Borderline control.

per-regulators will be averaged over a few switching cycles by an integrator. Then, this averaged current is controlled usually with a high-loop-gain feedback loop. Since the inductor current is averaged, the switching noise affecting the current control loop can be effectively eliminated by the averaging operation. Referring to Fig. 2.15, the rectified input voltage, the inductor current, and the output voltage of the pre-regulator are sensed by the average current-mode controller to generate an appropriate duty signal for PFC. Rajagopalan *et al.* [61] created a general technique for derivation of average current-mode control laws for single-phase pre-regulators without input voltage sensing. An average current-mode controller without the input voltage sensing path has been reported by Luo *et al.* [62].

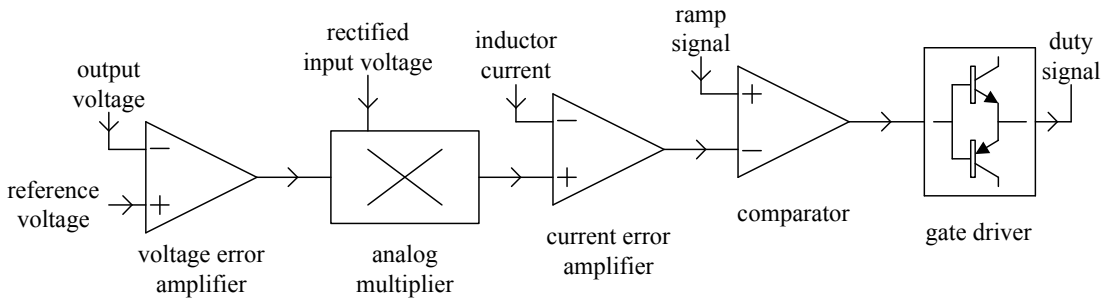


Figure 2.15: Block diagram of traditional average current-mode controller for pre-regulator.

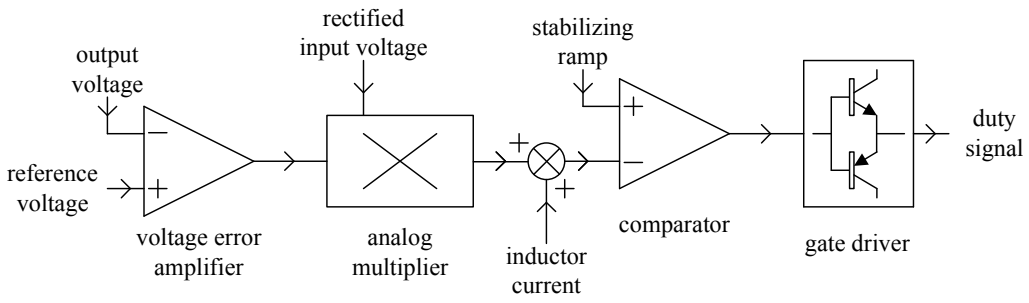


Figure 2.16: Conceptual diagram of peak current-mode control for pre-regulator.

Peak current-mode control can be implemented in a boost pre-regulator [63] and a flyback pre-regulator [64]. Fig. 2.16 shows the block diagram of a PFC controller applying peak current-mode control. A reference template that is controlled by the input and output voltage determines the peak value of the inductor current. Similar to applying peak current-mode control in a dc-dc converter, the ramp compensation is needed to avoid sub-harmonic oscillation, if the duty ratio is over 50% when the pre-regulator operates in CCM.

Hysteretic control applied to a boost pre-regulator has been discussed by Zhou *et al.* [65]. Two reference templates, which are an upper reference and a lower reference, determine the inductor current of the pre-regulator. The inductor will be energized until the inductor current reaches the upper reference. It will be de-energized until the inductor current reaches the lower reference. Variable switching frequency operation over the ac mains period is the main drawback of the hysteretic control. A modified hysteretic control for boost pre-regulators is proposed by Kazerani *et al.* [66] to solve the variable switching frequency problem. Fig. 2.17 shows the modified hysteretic controller with the inductor current waveform.

Borderline control is a simple version of hysteretic control. Design consideration for boost pre-regulators using borderline control has been discussed by Lai and Chen [67]. The difference between borderline control and hysteretic control is the level of the lower reference. The lower reference of the borderline control is at ground level. Thus, the inductor of the pre-regulator in the borderline control is operated in critical mode.

Using one-cycle control to achieve PFC in boost converters has been proposed by Brown and Soldano [68], as shown in Fig. 2.18. The one-cycle control technique was developed as a general PWM control method [69]. This control method uses the nonlinear nature of switching converters, e.g., pre-regulator, to achieve instantaneous control of the average value of the switched voltage or current. One-cycle control technique contends reductions in complexity comparing with average current-mode control, because it eliminates an analog multiplier and the current compensation network. Table 2.2 lists the PFC controllers available on the market, which are grouped according to the

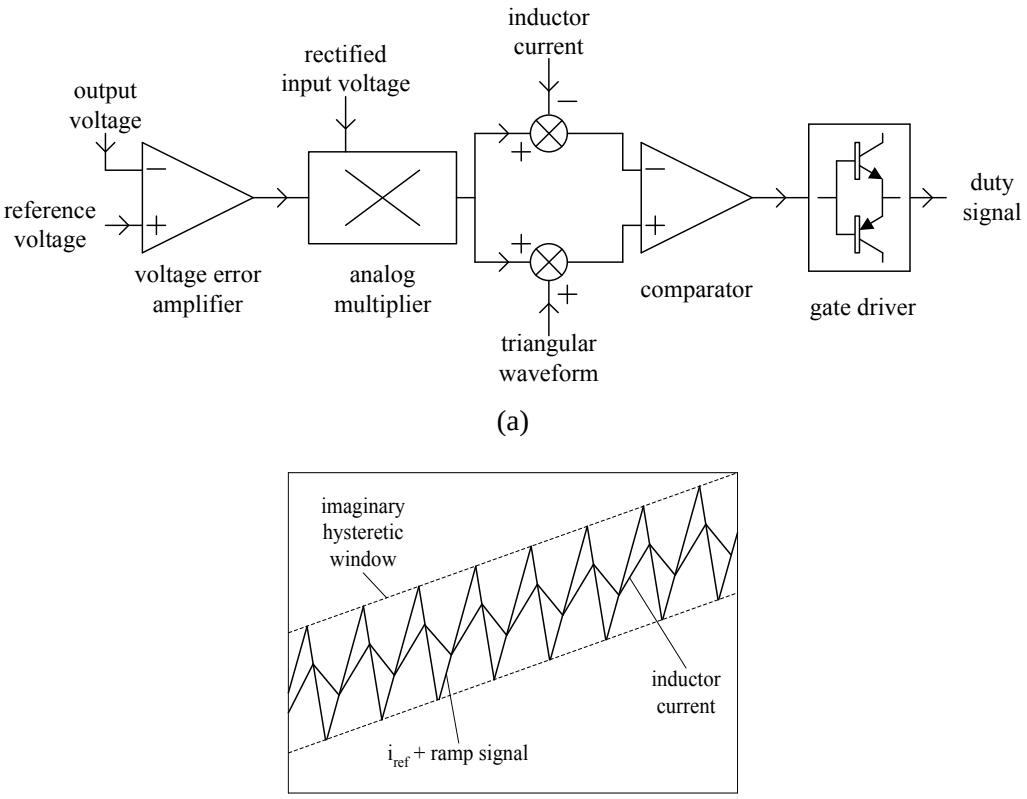


Figure 2.17: (a) Modified hysteretic controller block diagram. (b) Inductor current.

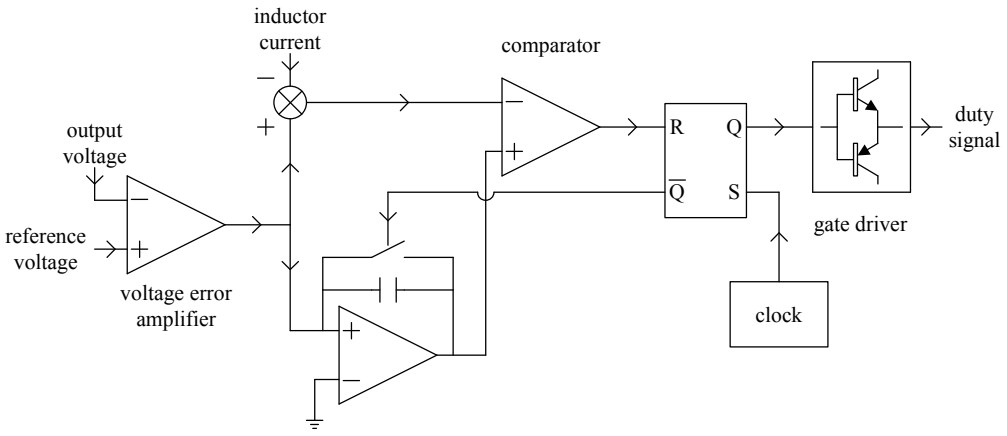


Figure 2.18: One-cycle controller for pre-regulator.

aforementioned control methods.

Table 2.2: PFC controllers

Control methodology	Part No. & Manufacturer
Average current-mode control	L4981 (ST) LT1248 (Linear technology) ML4821 (Fairchild) NCP1653 (ONsemi) UC3853 (TI) UCC3818 (TI)
Average current-mode control for interleaving CCM	UCC28070 (TI)
Average current-mode control with zero voltage transition	UC3855 (TI)
Average current-mode control without feedforward path	ICE1PCS01 (Infineon)
Peak current-mode control	ML4812 (Fairchild) NCP1653 (ONsemi) TDA4863 (Infineon) UC3852 (TI)
Borderline control	FAN7528 (Fairchild) L6561 (ST) MC33368 (ONsemi) MC34262 (ONsemi) UCC38050 (TI)
One-cycle control	IR1150 (IR)

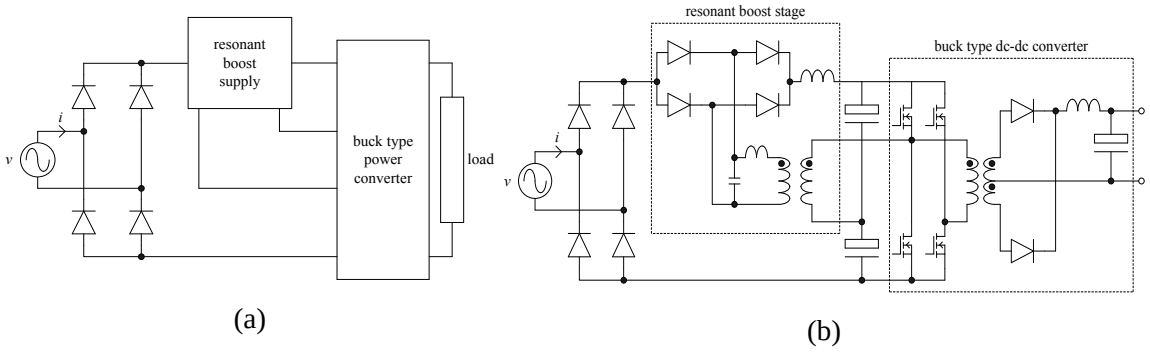


Figure 2.19: (a) Block diagram of noncascading switching regulator by splitting input power. (b) Circuit diagram.

2.3 Noncascading Switching Regulators

As discussed, PFC and voltage regulation are achieved by a pre-regulator and a voltage regulator, respectively, with an energy storage element. There have been numerous attempts [70], [71] in combin-

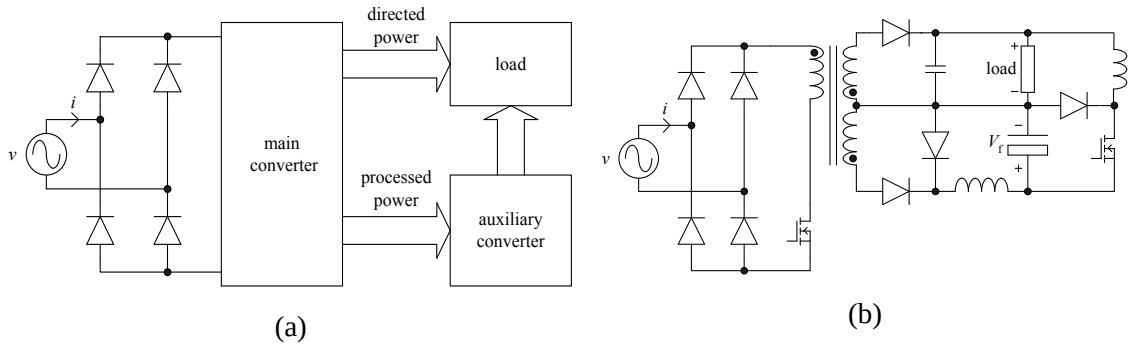


Figure 2.20: (a) Block diagram of noncascading switching regulator topologies proposed by García. (b) An implementation circuit diagram.

ing the pre-regulator with the voltage regulator to from a so-called “single-stage” high-power-factor voltage regulator. In general, the pre-regulator is a typical DCM operated switching converter [72], [73] and is followed by a dc-dc converter. Since the input power is still processed serially, efficiency is inevitably sacrificed.

Recently, for improving the overall efficiency of switching regulators, many researchers have rearranged the connection between the pre-regulator and the voltage regulator. For providing a clearer description, the switching regulators with rearranged connection is named noncascading switching regulators. In 1991, Kheraluwala *et al.* [74] proposed a noncascading switching regulator, as shown in Fig. 2.19. The proposed noncascading switching regulator is comprised of a resonant boost supply and a buck-type supply. Because a portion of the input power is only processed by the buck-type supply, the overall efficiency can be improved. In addition, the resonant boosting supply is controlled by frequency modulation and the buck-type stage is PWM controlled. Since both input current and output voltage can be controlled independently, PFC and voltage regulation can be maintained. A similar approach to constructing a noncascading switching regulator has been presented by Qian and Lee [75]. The difference between them is that the resonant boosting supply is replaced by a charge pump circuit for PFC.

Noncascading switching regulators providing imperfect PFC and tight voltage regulation have been proposed in [76]. The connection diagram between the pre-regulator and the voltage regulator is shown in Fig. 2.20 (a). The main converter contains one input power path and two output power paths. The auxiliary converter only contains one input power path and one output power path. Fig. 2.20 (b) shows a merged isolated converter as the main converter and a buck converter as the auxiliary converter. The basic purpose is to split the input power into two parts by using a merged isolated converter and to give one of the split power directly to the load. Thus, the directed power is only processed by one converter stage to improve the efficiency. Based on the circuit diagram, the merged

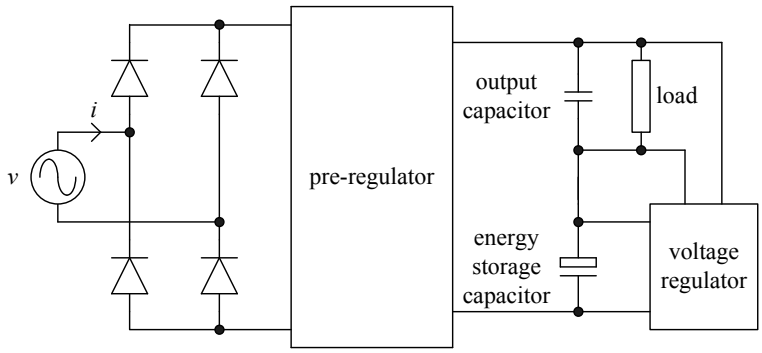


Figure 2.21: Power flow diagram for unity PF noncascading switching regulators.

isolated converter is operated in the flyback mode only when the voltage of the energy storage, $V_{\rm f}$, is larger than the input voltage, otherwise the merged converter is operated in the flyback mode and the forward mode simultaneously. The flyback mode transferred power is the directed power. Therefore, the circuit parameters such as the magnetizing inductor and the turns ratio of the transformer, the inductor of the forward output, and $V_{\rm f}$ have a strong influence in the splitting of the input power. García *et al.* [76] reported that two independent controls can achieve less harmonic input current and more efficient power conversion, since $V_{\rm f}$ is fully controlled.

Unity PF noncascading switching regulators are proposed in [77], [78], [79]. The power flow arrangement between the pre-regulator and the voltage regulator for these noncascading switching regulators can be represented by Fig. 2.21. Two power paths, representing a portion of power directly that goes to the load and another that reaches the load through the voltage regulator, are split after the pre-regulator. In this case, unity PF can be achieved. The rectifier-less noncascading switching regulator is presented by Rodríguez *et al.* [77], as shown in Fig. 2.22. The pre-regulator is an integrated flyback rectifier and the voltage regulator is a buck-boost converter. Both power stages are operated in DCM and controlled by a common duty signal. The amount of power processed by only one power stage is determined by the ratio of the output voltage and the energy storage voltage. Sebastián *et al.* [78] used a series-switching regulator as a voltage regulator to construct a unity PF noncascading switching regulator, as shown in Fig. 2.23. The function of the series-switching regulator is to compensate the difference between the output voltage of the noncascading switching regulator and the output voltage of the pre-regulator, therefore a considerable fraction of the output power (typically 85 %-90 %) of the pre-regulator comes up to the load without being processed by the series-switching regulator. The experimental results showed that the overall efficiency of this noncascading switching regulator is over 97 % at full load condition. Using single power switch to control unity PF noncascading switching regulator has been proposed by Mishra *et al.* [79]. The schematic diagram of the proposed noncascading switching regulator is shown in Fig. 2.24. A flyback converter and a merged isolated converter are used to construct the proposed noncascading switching regulator. Both con-

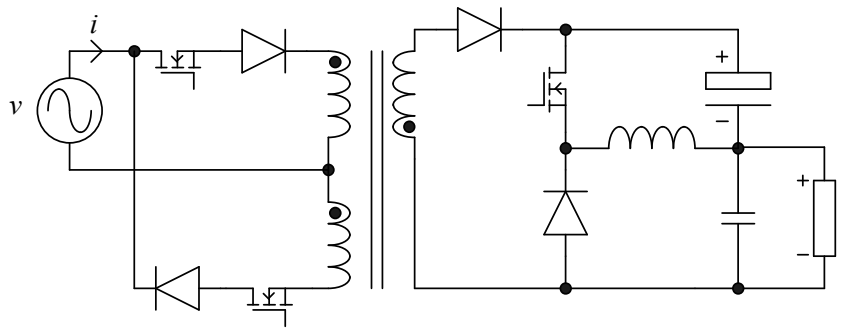


Figure 2.22: Rectifier-less noncascading switching regulator.

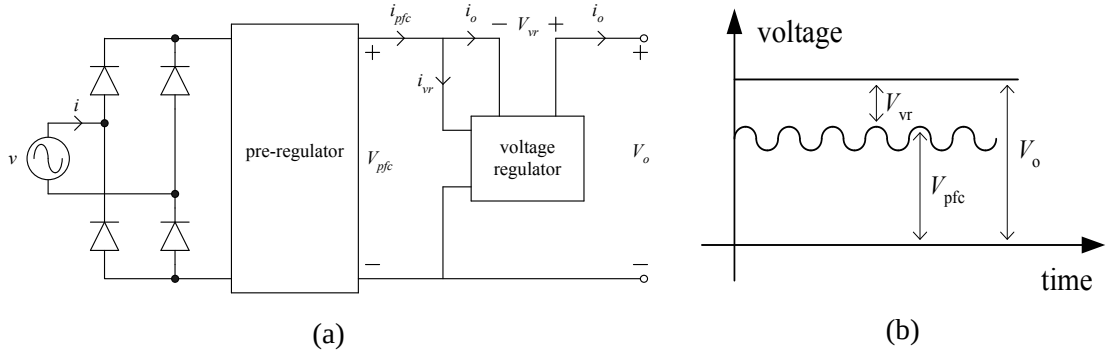


Figure 2.23: (a) Using series-switching regulator to construct noncascading switching regulator. (b) Output voltages relationship between different regulators.

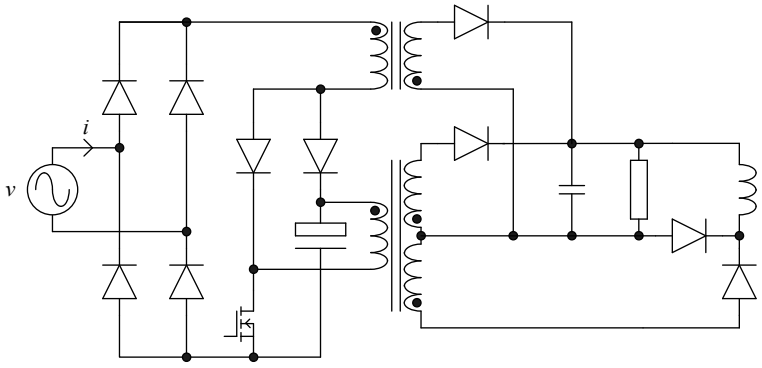


Figure 2.24: Two isolated converters construct a unity PF noncascading switching regulator.

verters are operated in DCM for PFC. The flyback converter directly transfers the ac mains power to the load. The merged isolated converter can be operated in the flyback mode and the forward mode depending on the rectified input voltage level, its transformer turns ratio, and the output voltage of the proposed switching regulator.

The parallel PFC scheme [80], [81], [82] also can produce noncascading switching regulators.

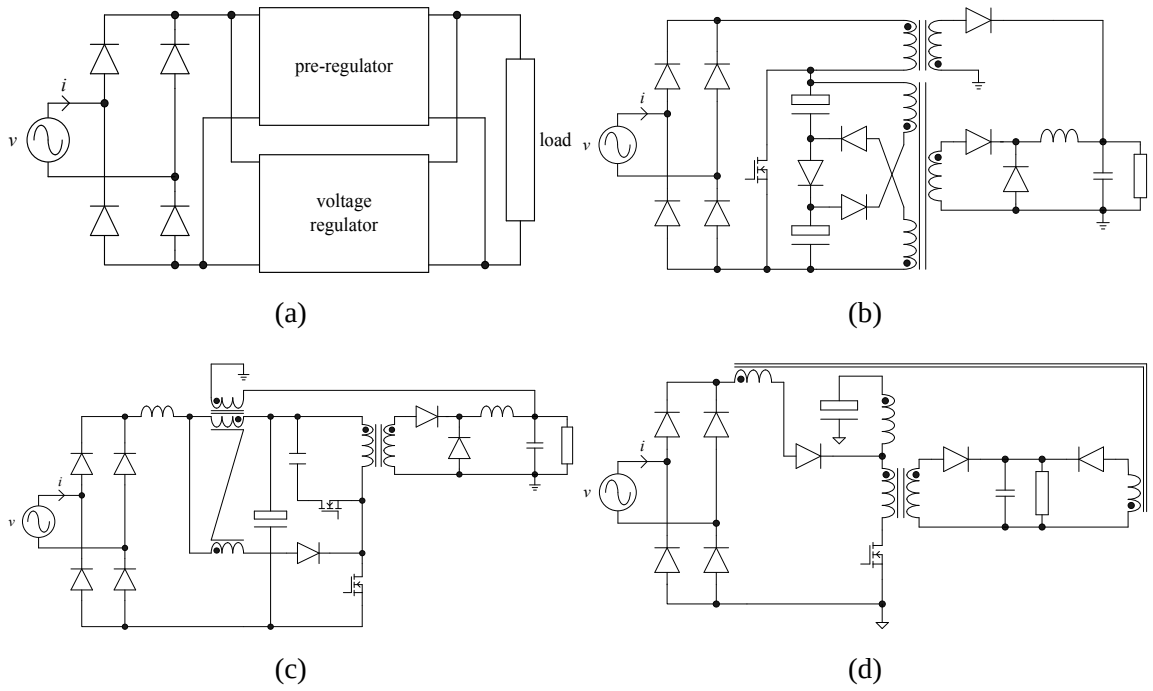


Figure 2.25: (a) Block diagram for noncascading switching regulators using parallel scheme. (b) Qiu's circuit. (c) Lee's circuit. (d) Do's circuit.

Fig. 2.25 (a) shows the connection diagram of this parallel scheme. As the name implies, the pre-regulator and the voltage regulator are parallel-connected. Therefore, the input power source is drawn by the pre-regulator and the voltage regulator simultaneously. Additionally, the output load is also parallel-connected with the pre-regulator and the voltage regulator. Based on the parallel scheme, the input power is split into two power paths. Part of the input power is controlled by the pre-regulator for PFC, and then reaches the output load. Another is processed by the voltage regulator to reach the load for voltage regulation. Figs. 2.25 (c)-(d) show the various noncascading switching regulators using the parallel PFC scheme proposed recently.

2.3.1 Power Flow Diagrams

The efficiency problem of the switching regulators can be effectively solved by noncascading connection between the pre-regulator and the voltage regulator due to the concept of partial power processing. The concept has been verified [83], [84] to be effective in increasing the overall efficiency of the switching regulators with tight voltage regulation and fulfilling the harmonic current emission standards.

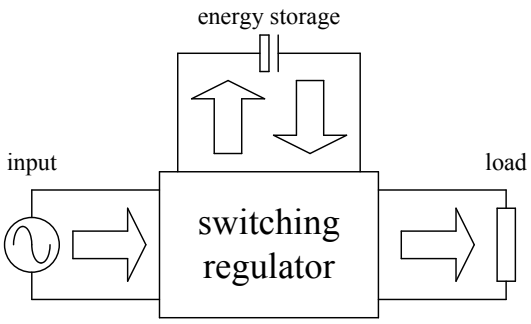


Figure 2.26: Three-port model of a switching regulator.

A general procedure for synthesizing minimal practical noncascading switching regulators based on the use of basic converters has been developed by Tse and Chow [85], [86]. A switching regulator as a three-port network terminating in an input voltage, an energy storage element, and an output load, is shown in Fig. 2.26. Suppose that the input port and the load port allow energy to be transferred in only one direction, while the energy storage element allows a bi-directional energy flow, as indicated by the arrows in Fig. 2.26. If each constituent converter has one input power port and one output power port, the minimum number of converters needed to construct the switching regulator which fully connects all power input and output ports is equal to 2. Two basic rules govern the connection. Firstly, in order for the switching regulator to perform the necessary power buffering function, it must allow power conversion from the input port to the energy storage and from the energy storage to the load. Secondly, to ensure the minimal number of power flow paths, no converter should convert power from a port back to itself, such as input port-to-input port, energy storage-to-energy storage, and output port-to-output port conversions should be avoided. According to the rules, only three power flow graphs can be used to connect the ports, as shown in Fig. 2.27. Power flow diagrams describe the way in which power is transferred among the three ports. Each power flow diagram contains two power flow graphs. The branches in a power flow graph denote the paths through which power is being transferred, and the arrows on the branches indicate the direction of power flow. Obviously, there are only four possible constructions, each comprising two power flow graphs, as shown in Fig. 2.28. Two converters are placed in the appropriate branches of the power flow paths in

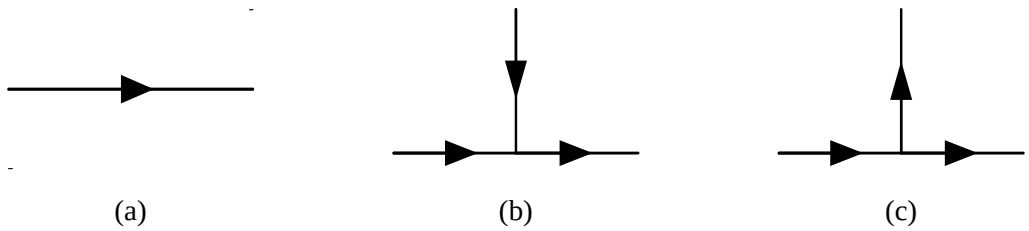


Figure 2.27: Power flow graphs. (a) Type I, (b) Type II, and (c) Type III.

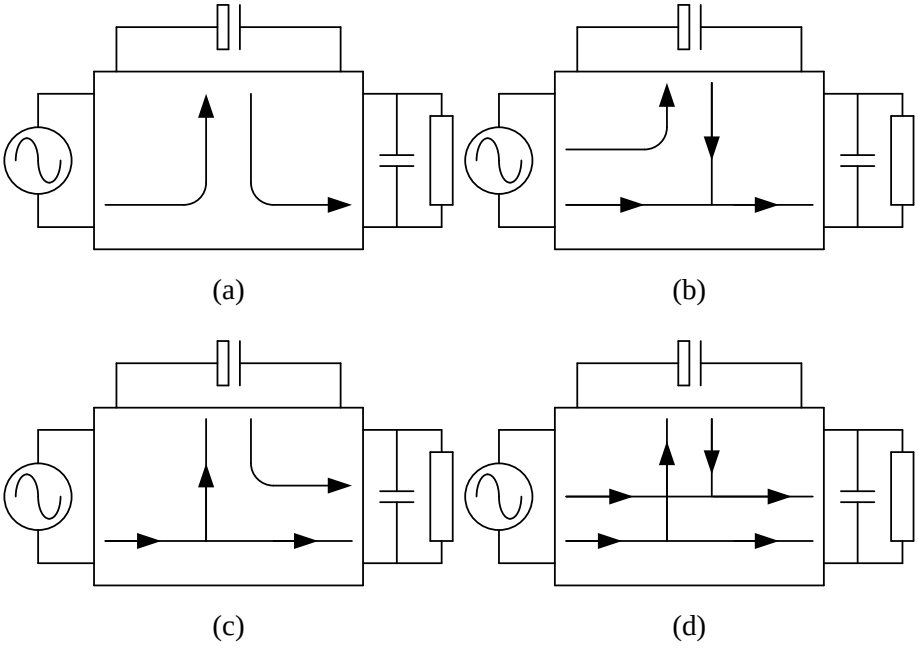


Figure 2.28: Power flow diagrams for switching regulator. (a) Type I-I, (b) Type I-II, (c) Type I-III, and (d) Type II-III.

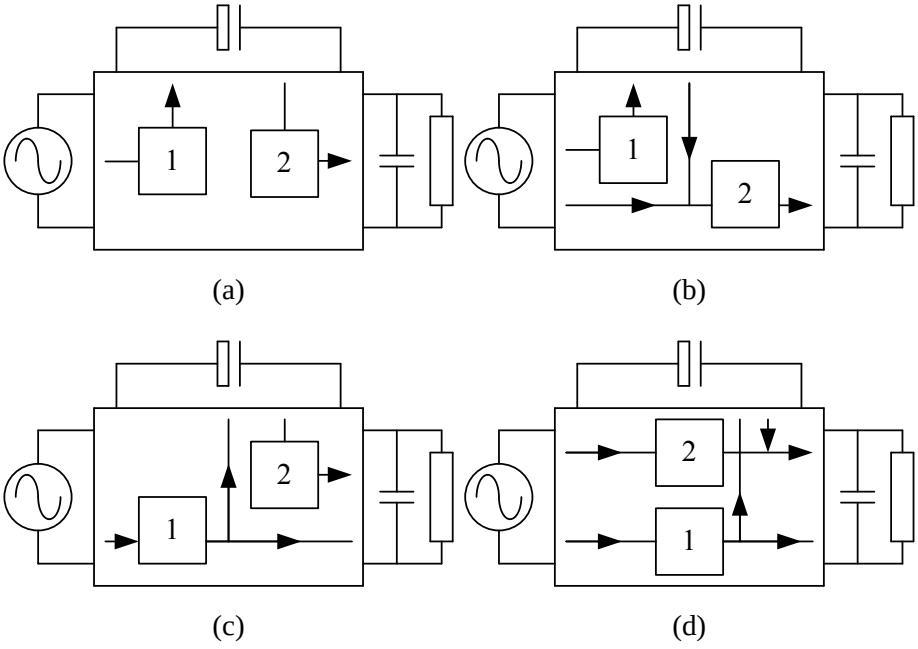


Figure 2.29: Configurations of switching regulator in terms of power flow diagrams for switching regulator. (a) Cascaded configuration, (b) Imperfect PF noncascading configuration, (c) Unity PF noncascading configuration, and (d) Parallel noncascading configuration.

order to take full control of power flow between the ports. After a set of procedures, sixteen possible configurations are generated. Some configurations are shown in Fig. 2.29 and solid squares boxes denote simple converters. The sixteen configurations and their calculated overall efficiencies are shown in Appendix A. The last logical step is to place converters appropriately in the square boxes in these sixteen configurations. Using the power flow diagram transferring into a practical noncascading switching regulator in circuit level has been reported at [87].

2.4 Summary

This chapter gives a brief overview of PFC methods. In general, PFC can be accomplished by two techniques, i.e., filtering techniques and input current controlling techniques. The filtering techniques are achieved by passive filters and active filters. The input current controlling techniques use a high switching frequency converter which draws a sinusoidal input current from the ac mains. The topologies, the operating modes, CCM or DCM, and the control methods of the high switching frequency converter affect the PFC performance. The advantages and disadvantages of various converter topologies are discussed. Based on the energy balance consideration, the essential components to construct a switching regulator with PFC and tight voltage regulation are shown. The concept of using noncascading switching regulators to increase the overall efficiency is explained with various noncascading example circuits. Furthermore, a set of procedures for generating noncascading switching regulators has been highlighted. Evidently, PFC and voltage regulation of a noncascading switching regulator is influenced by its connection between the pre-regulator and the voltage regulator, as shown in the example circuits. The next chapter will provide a detailed performance analysis on different types of noncascading switching regulators.

Chapter 3

Designs and Performances of Noncascading Switching Regulators

Methods of using noncascading structures to construct efficient switching regulators for achieving tight output regulation and PFC have been developed in the literature [86], [87], [88], which can be used to synthesize noncascading switching regulators. Unfortunately, industry has been slow to appreciate and exploit the considerable advantages of the noncascading switching regulators. This is mainly due to the lack of understanding among power supply engineers of noncascading switching regulators performances, which are efficiency, input current harmonic distortion, and load voltage regulation, and their relationship, as well as the lack of a systematic categorization of noncascading switching regulators. This chapter provides clear guidelines for assisting engineers to choose which noncascading structures are suitable for their design. This can also be attributed to the fact that much of the work on the subject has been reported from the efficiency's viewpoint, rather than from performance considerations.

Hence, the major objective of this chapter is to systematically investigate the performances of switching regulators based on noncascading structures in terms of efficiency, input current harmonic distortion, and load voltage regulation. The exploration begins with simplified power flow diagrams, which represent the noncascading switching regulators and describe the essential features of the noncascading switching regulators to achieve PFC and tight voltage regulation. Based on these diagrams, the noncascading switching regulators can be classified into three categories, each offering a different possibility of the achievable performances. The first category permits a tradeoff between the efficiency and the input current harmonic distortion, the second permits a tradeoff between the efficiency and the size of the storage element for the load voltage regulation, and the third allows a tradeoff among all the performances. With detailed analyses through analytical approaches, simulation results illustrate the performances of these three categories of noncascading switching regulators. An

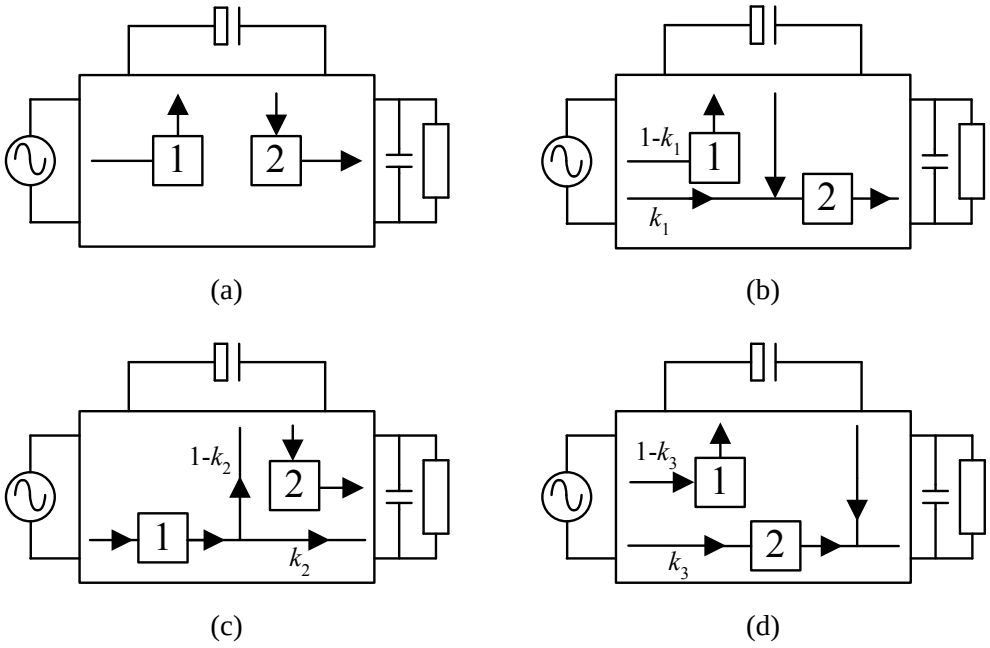


Figure 3.1: Power flow diagrams for describing switching regulators. (a) Classical (cascade), (b) Category 1, (c) Category 2, and (d) Category 3.

experimental prototype of the third category has been built to validate the analyses. This information allows power supply engineers to skip through laborious preliminary derivations when performing their design in noncascading switching regulators.

3.1 Classification of Noncascading Switching Regulators

The power flow diagrams describing several switching regulators are shown in Fig. 3.1. The branches in the power flow diagrams denote the paths through which power is being transferred, and the arrows on the branches indicate the direction of the power flow. Square boxes 1 and 2 represent a pre-regulator and a voltage regulator, respectively. Suppose that the regulators allow power to be transferred in only one direction and an energy storage allows a bi-directional power flow.

Fig. 3.1 (a) presents the power flow diagram of classical switching regulators which adopt a cascade structure. The total input power is transferred from the input power source to a storage element through a pre-regulator and then to a load through a voltage regulator. In this case, the input power and the output power are fully controlled by the pre-regulator and the voltage regulator, respectively, thus achieving the PFC and the load voltage regulation. The efficiency of such classical switching regulators is degraded as a result of the serial power processing. The overall efficiency of

this kind of switching regulators is

$$\eta_{\text{classical}} = \eta_{\text{pr}}\eta_{\text{vr}} \tag{3.1}$$

where η_{pr} and η_{vr} are the efficiencies of the pre-regulator and the voltage regulator, respectively.

Fig. 3.1 (b) presents Category 1 switching regulators [74], [89], [90], [91], and [92]. In this category, the output power is completely controlled by a voltage regulator. Thus, the load voltage regulation can be independently controlled. On the other hand, the input power is split into two parts, one going into a pre-regulator and the other going to the voltage regulator, and both to a load eventually. The overall efficiency of the switching regulators in this category is

$$\eta_{\text{Category1}} = \eta_{\text{pr}}\eta_{\text{vr}} + \eta_{\text{vr}}k_1(1 - \eta_{\text{pr}}) \tag{3.2}$$

where the *split factor* k_1 is the ratio at which the input power is split between the pre-regulator and the voltage regulator. For brevity and easy understanding, a subscript of the *split factor* denotes Category. k_1 indicates that a portion of the input power is directly processed by the voltage regulator and the remainder is transferred to the voltage regulator through the pre-regulator. Clearly, *tradeoff is mainly possible between the efficiency improvement and the attainable PF.*

The noncascading switching regulators proposed in some earlier publications [93], [94], [95], [96], [97], [98], and [99] belong to Category 2 and the power flow diagram is given in Fig. 3.1 (c). All of the input power in this category of switching regulators goes to a pre-regulator. Thus, the input current can be independently shaped by the pre-regulator. The efficiency of this category switching regulators is

$$\eta_{\text{Category2}} = \eta_{\text{pr}}\eta_{\text{vr}} + \eta_{\text{pr}}k_2(1 - \eta_{\text{vr}}) \tag{3.3}$$

where the *split factor* k_2 is the ratio at which the output power of the pre-regulator is split between a storage and the direct path to a load. A part of the pre-regulator output power is indicated by k_2 that goes to the load directly and the remaining output power delivers to the storage (then a voltage regulator). Clearly, *the size of energy storage and the output capacitor for load voltage regulation of the switching regulator can be traded off for some efficiency improvement.*

Fig. 3.1 (d) represents Category 3 switching regulators [100], [101], [102], and [103]. The efficiency of this category switching regulators is

$$\eta_{\text{Category3}} = (1 - k_3)\eta_{\text{pr}} + k_3\eta_{\text{vr}} \tag{3.4}$$

where the *split power* k_3 is the ratio at which the input power is split between a pre-regulator and a voltage regulator. k_3 signifies that how much input power is processed by the voltage regulator. Clearly, *both the PF and the load voltage regulation of the switching regulators cannot be independently controlled.* Thus, k_3 represents the tradeoffs between the efficiency, the PF, and the load voltage regulation. While this arrangement provides some flexibility for engineers to optimize the performances, the analysis could be rather complicated.

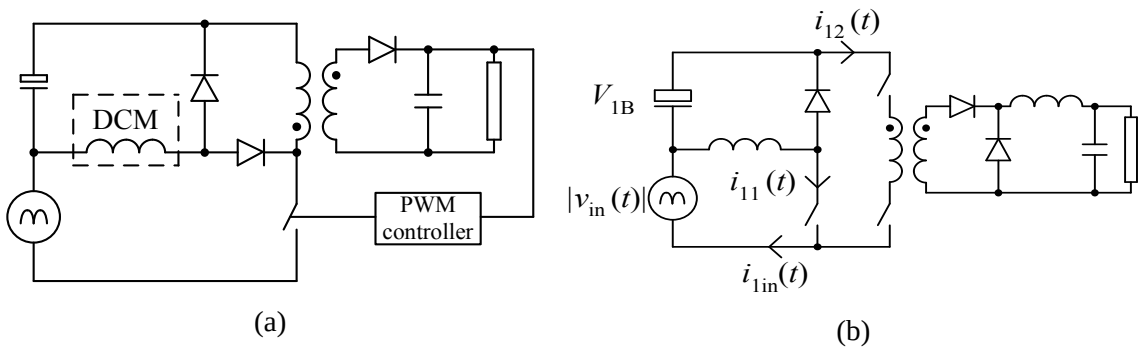


Figure 3.2: Category 1 switching regulators: (a) a single switch noncascading switching regulator proposed by Lin *et al.*; and a separately controlled noncascading switching regulator proposed by Chow *et al.*, core reset arrangement omitted for brevity.

3.2 Performance Analysis

In the following analysis we assume that each noncascading switching regulator is composed of a pre-regulator and a voltage regulator which are clearly separated. These regulators have independent controllers to drive their duty cycles. The controllers are crucial to achieving the low current harmonic and the load voltage regulation simultaneously in the noncascading switching regulators under study. Also, the input voltage of the switching regulators is a rectified sinusoid, and the PF of its pre-regulator is maintained at unity. The voltage of the energy storage in the noncascading switching regulators under study is defined as (2.5).

3.2.1 Category 1 Switching Regulator

Fig. 3.2 shows two noncascading switching regulators of Category 1, which were proposed earlier in [90], [91]. Fig. 3.2 (a) shows a single switch switching regulator, which is an integration of a buck-boost converter with a flyback converter using a single switch [90]. The buck-boost converter operates in discontinuous-conduction-mode (DCM) for achieving PFC, and the pulse-width-modulation (PWM) controller regulates the output voltage only. Another noncascading switching regulator shown in Fig. 3.2 (b) is a separately controlled noncascading switching regulator [91]. It employs a buck-boost converter and a two-switch forward converter as its pre-regulator and its voltage regulator, respectively. To simplify the performance analysis of Category 1 switching regulators, the separately controlled noncascading switching regulator [91] shown in Fig. 3.2 (b) is chosen as an example in the following discussion.

Before embarking on a discussion of this noncascading switching regulator performances, the split factor, k_1, in terms of circuit parameters has to be clarified. Assume that the energy storage

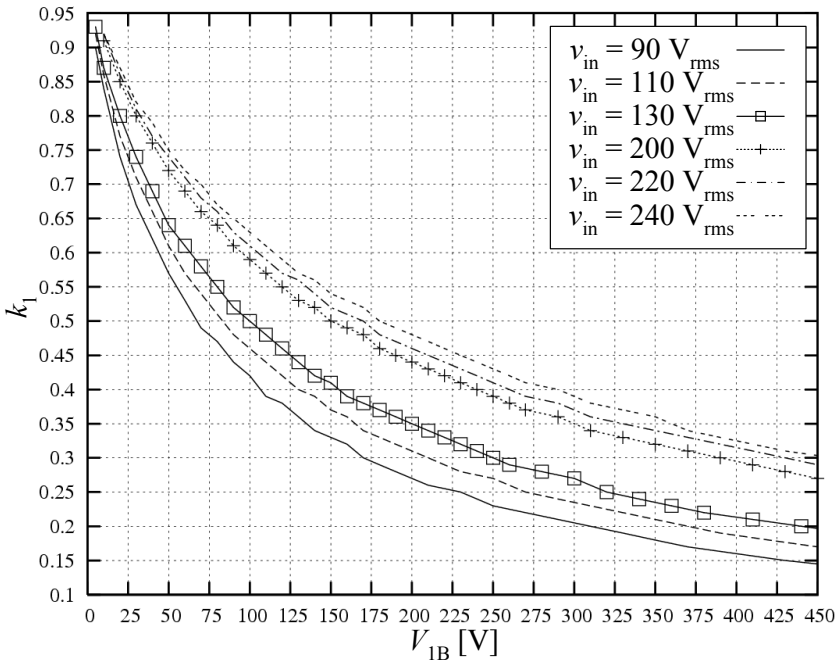


Figure 3.3: Numerical results of k_1 at different values of $V_{1\mathrm{B}}$ and v_{in}.

capacitor is large enough, thus the capacitor voltage, $v_{1\mathrm{B}}(t)$, of the Catergory 1 switching regulator under study is essentially constant and is equal to the capacitor static voltage, $V_{1\mathrm{B}}$. In the steady state, the two-switch forward converter draws a time-varying output power. The time-varying output power is given by

$$P_{1\mathrm{out}} = i_{12}(t)(V_{1\mathrm{B}} + \hat{v}_{\mathrm{in}}|\sin 2\pi f_{\mathrm{m}} t|) \tag{3.5}$$

where $i_{12}(t)$ is the input current of the forward converter, f_{m} is the ac mains frequency, and $\hat{v}_{\mathrm{in}}|\sin 2\pi f_{\mathrm{m}} t|$ is the rectified input voltage. The power processed by the buck-boost converter and flowing in the forward converter can be evaluated as

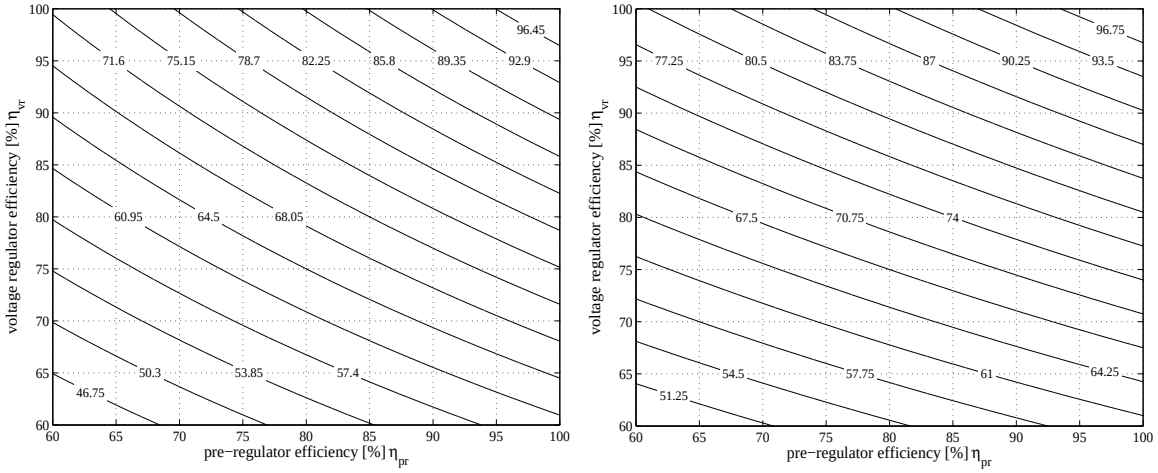
$$P_{1\mathrm{pfc}} = i_{12}(t)V_{1\mathrm{B}}. \tag{3.6}$$

Using the afore-described definition of the split factor for Category 1, the split factor of this noncascading switching regulator with circuit parameters is expressed as

$$k_1(t) = \frac{P_{1\mathrm{out}} - P_{1\mathrm{pfc}}}{P_{1\mathrm{out}}} = \frac{\hat{v}_{\mathrm{in}}|\sin 2\pi f_{\mathrm{m}} t|}{V_{1\mathrm{B}} + \hat{v}_{\mathrm{in}}|\sin 2\pi f_{\mathrm{m}} t|}. \tag{3.7}$$

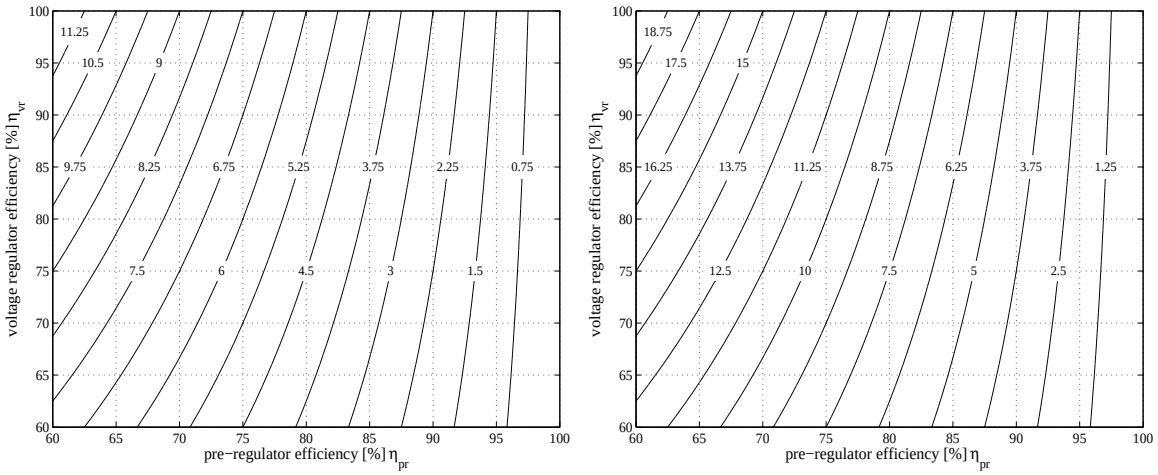
To calculate the overall efficiency, $k_1(t)$ is averaged over the rectified ac mains period and can be defined as

$$k_1 = \frac{1}{\pi}\int_0^{\pi} \frac{\hat{v}_{\mathrm{in}}|\sin 2\pi f_{\mathrm{m}} t|}{V_{1\mathrm{B}} + \hat{v}_{\mathrm{in}}|\sin 2\pi f_{\mathrm{m}} t|} d(2\pi f_{\mathrm{m}} t) \tag{3.8}$$



(a) (b)

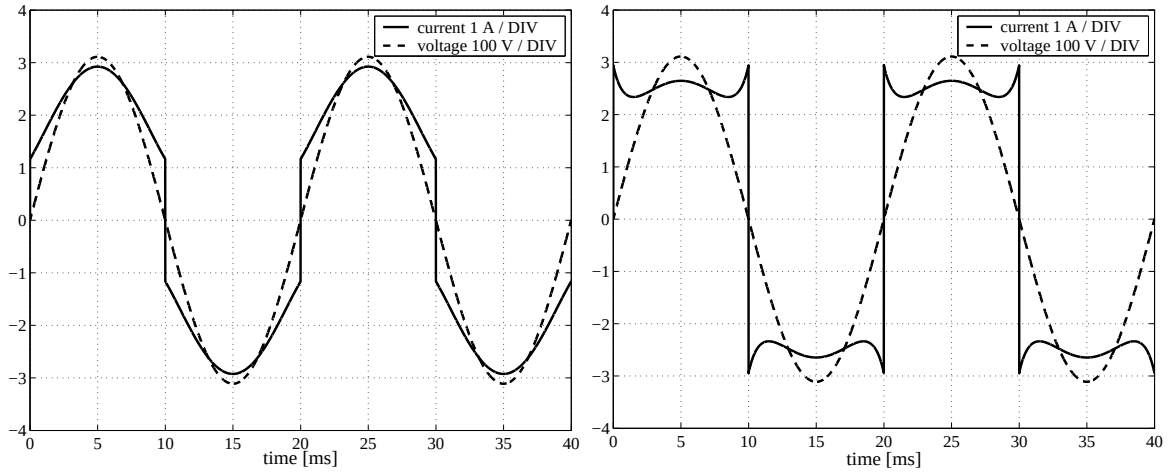
Figure 3.4: Overall efficiency of the Category 1 switching regulator under study at different values of k_1: (a) $k_1 = 0.3$ and (b) $k_1 = 0.5$.



(a) (b)

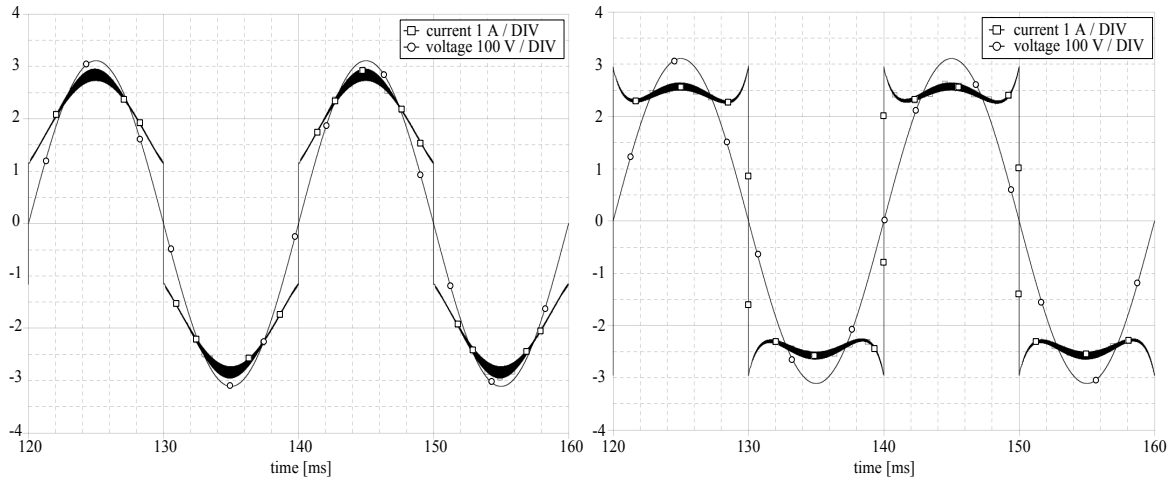
Figure 3.5: Increase in the overall efficiency of the Category 1 switching regulator under study over the classical switching regulator at different values of k_1: (a) $k_1 = 0.3$ and (b) $k_1 = 0.5$.

which can be solved numerically for given values of $V_{1\mathrm{B}}$ and $\hat{v}_{\mathrm{in}}$. Fig. 3.3 shows the numerical results of k_1 at different values of $V_{1\mathrm{B}}$ and v_{in}. Using (3.2) and (3.8), the overall efficiency of the noncascading switching regulator as a function of individual efficiencies of the pre-regulator and the voltage regulator are shown in Fig. 3.4. The efficiency of the pre-regulator becomes a minor factor in affecting the overall efficiency when k_1 increases, because less portion of the total output power is processed by the pre-regulator. A comparison is made to show that the overall efficiency of the non-



(a) (b)

Figure 3.6: Calculated input current waveforms with the input voltage of the Category 1 switching regulator under study at different values of k_1: (a) $k_1 = 0.3$ and (b) $k_1 = 0.5$.



(a) (b)

Figure 3.7: Simulated filtered input current waveforms of the Category 1 switching regulator under study at different values of k_1; (a) $k_1 = 0.3$ and (b) $k_1 = 0.5$.

cascading switching regulator is higher than that of the classical switching regulator. Fig. 3.5 shows the quantitative results to illustrate the overall efficiency of the noncascading switching regulator over that of the classical switching regulator.

Now, in order to satisfy the input current harmonic limits of some international standards [13],[14], the harmonic current contents of the rectified input current of the noncascading switching regulator

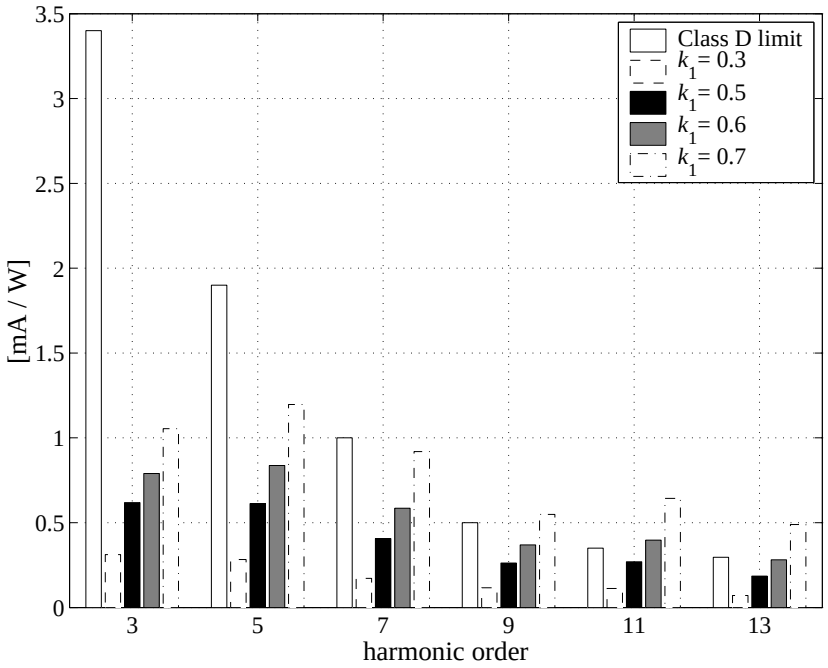


Figure 3.8: Harmonic components comparison between IEC 61000-3-2 Class D limit and the Category 1 switching regulator under study at different values of k_1.

should be predicted. The rectified input current can be defined by

$$i_{1\text{in}}(t) = i_{12}(t) + \hat{i}_{11}|\sin 2\pi f_{\text{m}} t|. \tag{3.9}$$

Because the input current of the buck-boost converter is defined to synchronize with the input voltage waveform, i.e., the input current is rectified sinusoid, the harmonic current is only generated by $i_{12}(t)$. For a given output power and input voltage, increasing $V_{1\text{B}}$ can reduce the value of $i_{12}(t)$ to diminish the harmonic current. However, k_1 decreases due to the increased amount of input power processed by the pre-regulator and the voltage regulator serially. Putting (3.5) into (3.9), we get

$$i_{1\text{in}}(t) = \frac{P_{1\text{out}}}{V_{1\text{B}} + \hat{v}_{\text{in}}|\sin 2\pi f_{\text{m}} t|} + \hat{i}_{11}|\sin 2\pi f_{\text{m}} t|, \tag{3.10}$$

and $\hat{i}_{11}$ can be approximated as

$$\hat{i}_{11} = \frac{2(1-k_1)P_{1\text{out}}}{\hat{v}_{\text{in}}}. \tag{3.11}$$

Based on (3.8), (3.10) and (3.11), the calculated input current waveforms with the input voltage of the noncascading switching regulator at different values of k_1 are shown in Fig. 3.6. To verify (3.10) and (3.11), some input current waveforms of the noncascading switching regulator from PSpice simulation are shown in Fig. 3.7. It reveals that the calculated results in Fig. 3.6 are close to those in Figs. 3.7. Since the input current of the buck-boost converter is assumed to be a rectified sinusoid,

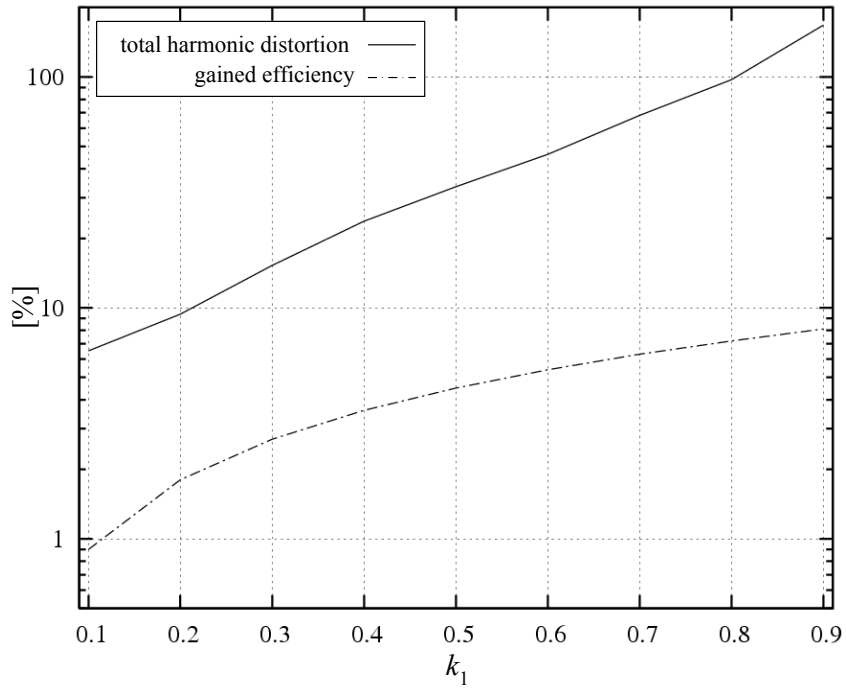


Figure 3.9: Input current total harmonic distortion (solid line). Increase in the overall efficiency of the Category 1 switching regulator over that of the classical switching regulator (dash line). The circuit parameters are: $P_{1\text{out}} = 500$ W, $\eta_{\text{pr}} = \eta_{\text{vr}} = 0.9$, and the input voltage $= 220\ \text{V}_{\text{rms}}$.

these two calculated input current waveforms shown in Fig. 3.6 depict the ideal PFC performance of the noncascading switching regulator. The parameters of the noncascading switching regulator are defined as follows: the input voltage is 220 V_{rms} and the output power is 500 W. Fig. 3.8 shows the normalized harmonic current contents of the noncascading switching regulator in the ideal PFC performance to compare IEC 61000-3-2 Class D limit. For k_1 below 0.5, the harmonic current contents of this noncascading switching regulator are within the Class D limit. However, in practice, the efficiencies of the buck-boost converter and the two-switch forward converter should be taken into account, modifying (3.10) as

$$i_{1\text{in}}(t) = \frac{P_{1\text{out}}}{\eta_{\text{vr}}(V_{1\text{B}} + \hat{v}_{\text{in}}|\sin 2\pi f_{\text{m}} t|)} + \frac{\hat{i}_{11}|\sin 2\pi f_{\text{m}} t|}{\eta_{\text{pr}}\eta_{\text{vr}}} \tag{3.12}$$

where η_{pr} and η_{vr} are the efficiency of the buck-boost converter and the efficiency of the two-switch forward converter, respectively. Based on (3.12), (3.8), and (3.2), Fig. 3.9 shows two important design curves versus k_1: one curve reveals the total input current harmonics to describe PFC performance and the other depicts increase in overall efficiency of the Category 1 switching regulator under study over the classical switching regulator. Clearly, the split factor k_1 controls the input current harmonic distortion and the increased overall efficiency.

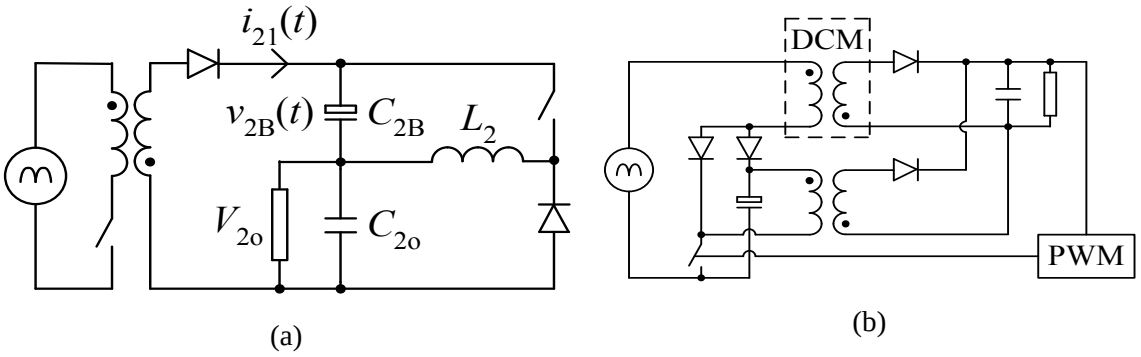


Figure 3.10: Category 2 switching regulators: (a) a simple example proposed by García *et al.*, and (b) another one from Luo *et al.*.

3.2.2 Category 2 Switching Regulator

Fig. 3.10 shows two simplified circuits representing Category 2 switching regulators. In a likewise fashion, a Category 2 switching regulator proposed by [95] is chosen for the analysis, because it was constructed by clearly separated pre-regulator and voltage regulator. It is to reveal the relationship between its split factor and the required value of its capacitive components, $C_{2\mathrm{B}}$ and $C_{2\mathrm{o}}$, especially in the load transient condition. From Fig. 3.10 (a), a flyback converter and a buck-boost converter are employed as a pre-regulator and a voltage regulator, respectively. The voltage regulator keeps drawing the power from the energy storage element to maintain the direct power path between the output port of the pre-regulator and the load. $i_{21}(t)$ is the pre-regulator output current and supports a portion of the load current. The pre-regulator output current flows through the serially connected $C_{2\mathrm{B}}$ and $C_{2\mathrm{o}}$. $C_{2\mathrm{o}}$ is in parallel with the output load. $V_{2\mathrm{o}}$ is the output voltage of the Category 2 switching regulator under study. If the voltage of $C_{2\mathrm{o}}$ is tightly governed by the voltage regulator, the voltage across $C_{2\mathrm{o}}$ can be considered practically as a voltage source and only $C_{2\mathrm{B}}$ serves as an energy storage element. The function of the voltage regulator provides a current to compensate the variation of $i_{21}(t)$ for achieving the dc load current. To illustrate the role of $i_{21}(t)$ and the output current of the voltage regulator play in supporting the output load, the current waveforms from PSpice simulation are depicted in Fig. 3.11.

From Fig. 3.11, the split factor of this noncascading switching regulator must be limited within 0.5 to keep $V_{2\mathrm{o}}$ free from low frequency (100 Hz or 120 Hz) ripple voltage. This can be explained by power balance between the output power of the pre-regulator and the output power of the voltage regulator. If the PF and the efficiency of the noncascading switching regulator are unity, the peak output power of the pre-regulator is twice of the output power of the noncascading switching regulator. To minimize reductant power processing [84], the voltage regulator only allows one direction of power flow (positive output power only), thus the power directly flowing into the output load must be

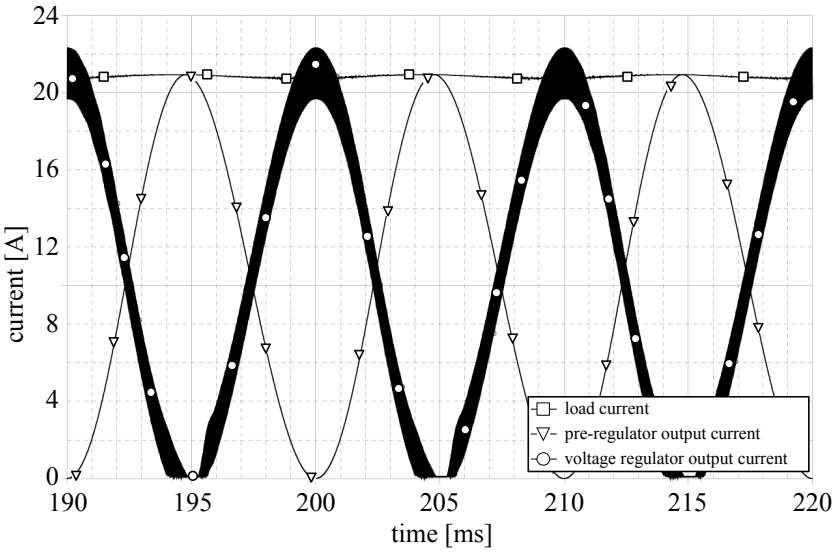


Figure 3.11: Simulated current waveforms of the Category 2 switching regulator under study for $k_2 = 0.5$.

lower than half of the pre-regulator output power, i.e. the maximum split factor is 0.5, to maintain a low-frequency ripple voltage free output.

The derivation of the split factor in terms of circuit parameters has been reported in [95]. As a prelude to the investigation of the performances of this noncascading switching regulator, a summary is shown to clarify the split factor. The part of the pre-regulator output power directly transferred to the load is given by

$$P_{2\mathrm{di}} = i_{21}(t)V_{2\mathrm{o}}. \tag{3.13}$$

If $C_{2\mathrm{B}}$ is large enough, only small amount of the low-frequency ripple voltage is appearing on $C_{2\mathrm{B}}$. The voltage of $C_{2\mathrm{B}}$ can be considered as the static voltage, $V_{2\mathrm{B}}$, so the total output power of the pre-regulator is

$$P_{2\mathrm{pfc}} = i_{21}(t)(V_{2\mathrm{o}} + V_{2\mathrm{B}}). \tag{3.14}$$

Even though the ripple voltage appearing on $C_{2\mathrm{B}}$ may cause a slight error in calculating $P_{2\mathrm{pfc}}$, the split factor k_2 can be defined by

$$k_2 = \frac{P_{2\mathrm{di}}}{P_{2\mathrm{pfc}}} = \frac{V_{2\mathrm{o}}}{V_{2\mathrm{o}} + V_{2\mathrm{B}}}. \tag{3.15}$$

By observing (3.2) and (3.3), the overall efficiency calculation in Category 2 switching regulators is in symmetry of that in Category 1 switching regulators. Figs. 3.4 can be reused to describe the overall efficiency in Category 2 switching regulators. In the overall efficiency calculation, the role of the pre-regulator efficiency in Category 2 switching regulators is similar to the role of the voltage regulator efficiency in Category 1 switching regulators. For example, the pre-regulator efficiency in Category

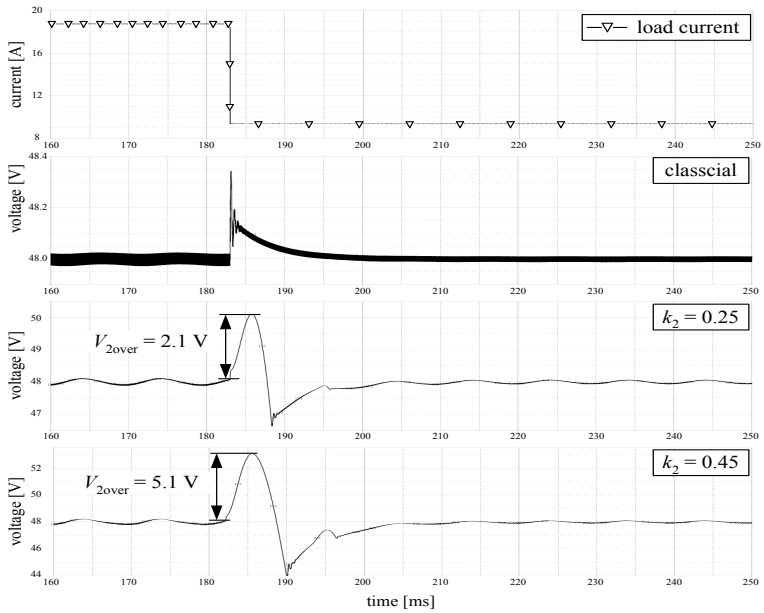
2 switching regulators dominates in controlling the overall efficiency. From (3.15), increasing k_2 indicates less portion of the output power processed by the voltage regulator. Hence, designing an efficient pre-regulator together with increasing k_2 can further improve the overall efficiency.

Obviously, k_2 and $V_{2\mathrm{o}}$ determine the static voltage of $C_{2\mathrm{B}}$. According to (2.4), if the ripple voltage on $C_{2\mathrm{B}}$ is designed at the allowable maximum value, i.e. $2V_{2\mathrm{B}}$, the minimum value of $C_{2\mathrm{B}}$ is obtained and calculated by

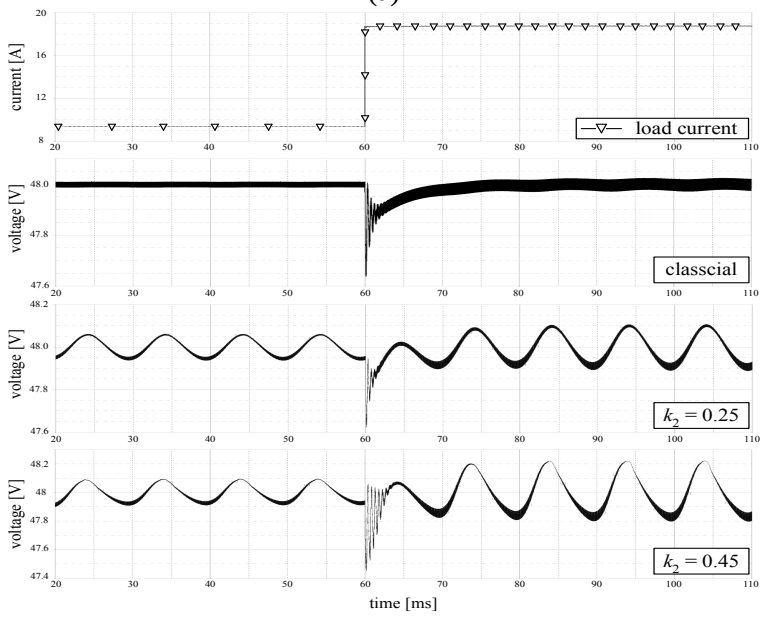
$$C_{2\mathrm{B}_{\min}} = \frac{P_{2\mathrm{out}}}{2\pi f_{\mathrm{m}}} \frac{1}{2(V_{2\mathrm{B}})^2} \tag{3.16}$$

where $P_{2\mathrm{out}}$ is the output power of the noncascading switching regulator and f_{m} is the ac mains frequency. $C_{2\mathrm{B}_{\min}}$ only provides power balance between the pre-regulator output power and the voltage regulator output power in the steady state output load. When the load is changed from a light output power to a full output power, the energy stored in $C_{2\mathrm{B}}$ must be capable of supporting all the transient output power. This design criterion is similar to the design of the classical switching regulator. However, care should be taken that the static voltage of $C_{2\mathrm{B}}$ is usually lower than that of the classical switching regulator especially in the high k_2.

As mentioned before, the pre-regulator output current of the noncascading switching regulator directly flows into the output load. The voltage loop of the pre-regulator governs the output current which is designed at one-fifth of the ac mains frequency bandwidth [52], [104] to maintain the sinusoidal input current of the pre-regulator. As a result, the load voltage regulation of the noncascading switching regulator is affected by the sluggish voltage control loop of the pre-regulator especially under a negative stepped load condition. In Fig. 3.12, the simulated output voltage waveforms from PSpice simulation are shown to illustrate the load transient performance. The simulated waveforms depict the output voltage of this noncascading switching regulator at different values of k_2 to compare with the output voltage of the classical switching regulator. For providing a fair comparison, both switching regulators are employed same set of control circuitries and voltage regulator. The circuit parameters of this voltage regulator are: $L_2 = 100$ μH, $C_{2\mathrm{B}} = 4700$ μF, $C_{2\mathrm{o}} = 2720$ μF, switching frequency = 50 kHz, and output voltage = 48 V. $V_{2\mathrm{B}}$ is equal to 125 V in the case of the classical switching regulator and $V_{2\mathrm{B}}$ in the case of the noncascading switching regulator is changed appropriately for different values of k_2. The low-frequency ripple voltage appearing on the noncascading switching regulator output in the simulated waveforms is due to use of the voltage mode control in the voltage regulator. This ripple voltage can be eliminated by peak current-mode control, as shown next chapter. According to the simulation results shown in Fig. 3.12 (a), a voltage overshoot of the noncascading switching regulator is much more profound when the negative stepped load occurs. It is clearly shown that the voltage overshoot becomes more serious when k_2 increases. The major cause of the voltage overshoot is that the excessive pre-regulator output current cannot be absorbed by the voltage regulator during the negative stepped load change, so this current charges $C_{2\mathrm{o}}$. From Fig. 3.12 (b),



(a)



(b)

Figure 3.12: Simulation voltage waveforms for the stepped load: the classical switching regulator (second trace) and the Category 2 switching regulator under study: (a) load change from 900 W to 450 W, (b) load change from 450 W to 900 W.

the output voltage regulation of the noncascading switching regulator provides similar performance to that of the classical switching regulator at a positive stepped load. The output voltage undershoots are around 0.6 V. Because the positive stepped transient response is completely dependent on the energy

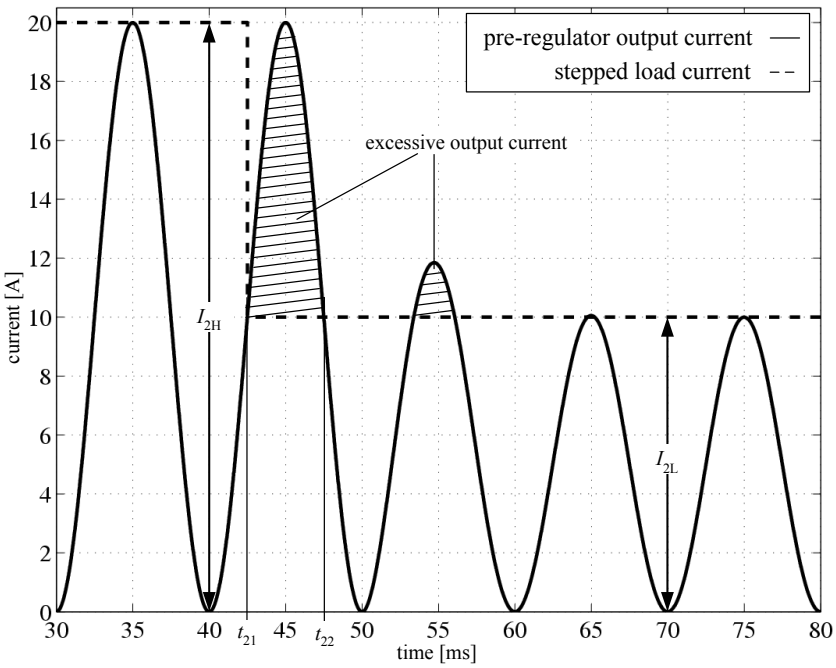


Figure 3.13: Current waveforms to illustrate the maximum overshoot voltage of the Category 2 switching regulator under study at full load to an half load stepped load change condition.

storage capacitor and the control circuity of the voltage regulator. $i_{21}(t)$ and the stepped load current sketched in Fig. 3.13 can be used to explain the overshoot voltage. From Fig. 3.13, the noncascading switching regulator is changed from full load to half load and k_2 is defined at the maximum value, i.e. 0.5. The maximum voltage overshoot occurs in this half load change when the negative stepped load starts at t_{21}. Since the pre-regulator controller cannot respond to this negative stepped load current immediately, in the worst case, $i_{21}(t)$ remains in the form of $k_2 I_{2\mathrm{H}}(1 - \cos 4\pi f_{\mathrm{m}} t)$ until t_{22} such that the maximum overshoot output voltage is generated, where $I_{2\mathrm{H}}$ is the output current of the noncascading switching regulator at the full load condition. Therefore the current charging $C_{2\mathrm{o}}$ can be expressed as

$$\begin{aligned} I_{2\mathrm{e}}(t) &= k_2 I_{2\mathrm{H}}(1 - \cos 4\pi f_{\mathrm{m}} t) - I_{2\mathrm{L}} \\ &\quad \text{for} \quad 0 < k_2 \leq 0.5 \end{aligned} \tag{3.17}$$

where $I_{2\mathrm{L}}$ is the half load output current. The overshoot voltage can be calculated as

$$V_{2\mathrm{over}} = \frac{1}{C_{2\mathrm{o}}} \int_{t_{21}}^{t_{22}} I_{2\mathrm{e}}(t)\, dt. \tag{3.18}$$

Thus, we may conclude that maximizing k_2 for gaining a higher overall efficiency results in a negative impact in terms of maximum overshoot voltage during a negative stepped load, i.e. full load to light

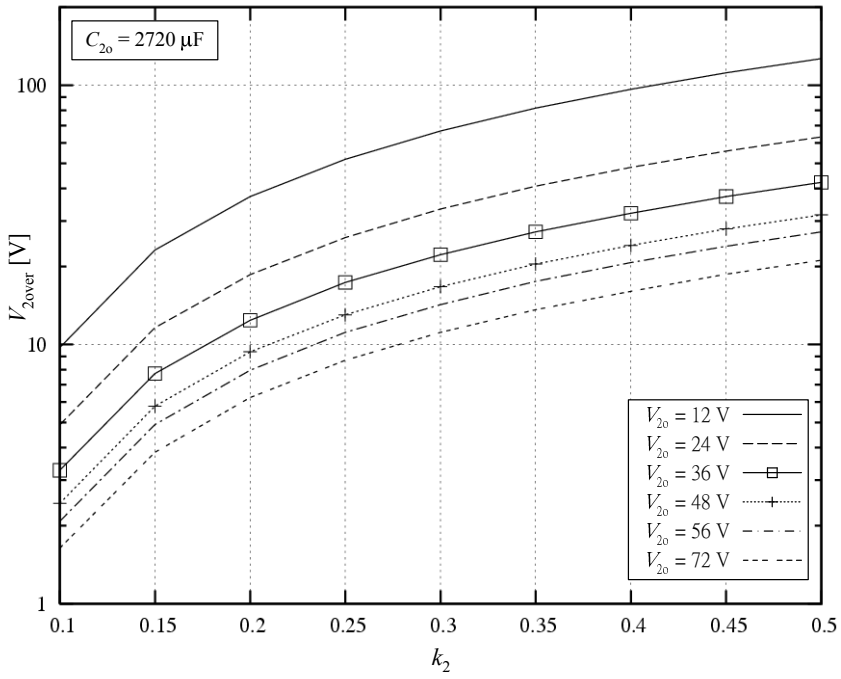


Figure 3.14: k_2 versus $V_{2\text{over}}$ at different values of output voltage for the load change from 1 kW to 100 W and $C_{2\text{o}} = 2720$ μF using $V_{2\text{o}}$ as parameters.

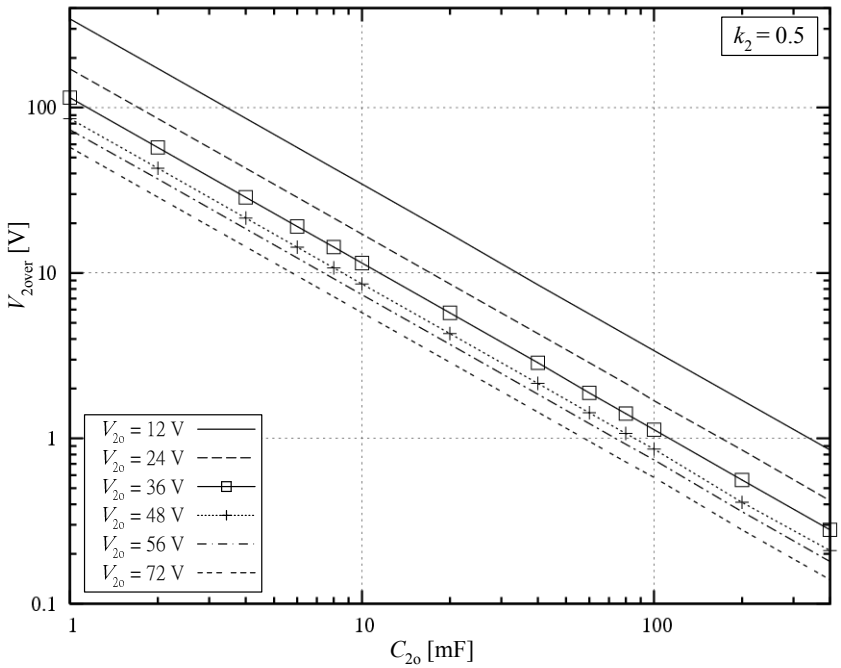


Figure 3.15: $V_{2\text{over}}$ versus $C_{2\text{o}}$ at different value of output voltage for the load change from 1 kW to 100 W and $k_2 = 0.5$.

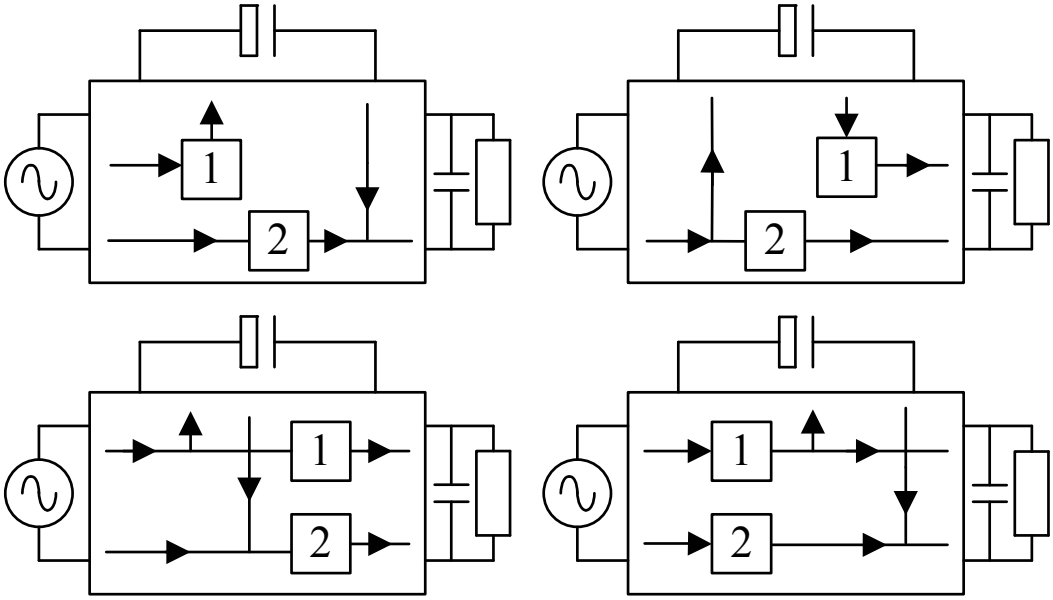


Figure 3.16: Some power flow diagrams are classified into Category 3.

load, unless the output capacitor is substantially increased. Fig. 3.14 depicts the simulated overshoot voltage level versus k_2 at different values of output voltage for the load change from 1 kW to 100 W. The overshoot voltage level versus C_{2o}, for $k_2 = 0.5$ and the load change from 1 kW to 100 W is shown in Fig. 3.15. For a given output power, the voltage overshoot of the low output voltage, i.e $V_{2o} = 12$ V, is the largest, because the pre-regulator output current level at this low output voltage is higher than any other output voltages. Notwithstanding the above, the requirement of the energy storage in the Category 2 switching regulator under study is same as the energy storage in the classical switching regulator, but care should be taken that the static voltage of the energy storage element of the noncascading switching regulator is relatively lower than that of the classical switching regulator. In the negative stepped load, the output voltage overshoot of the noncascading switching regulator is higher than that of the classical switching regulator because part of the load current is controlled by the pre-regulator of the noncascading switching regulator. In order to reduce the output voltage overshoot in the noncascading switching regulator, increasing the value of the output capacitor, C_{2o}, is essential.

3.2.3 Category 3 Switching Regulator

Much has been said about the performance of Category 1 switching regulators and Category 2 switching regulators which provide either perfect load voltage regulation or perfect PF. In Category 3 switching regulators, both performances are imperfect. The noncascading switching regulators proposed

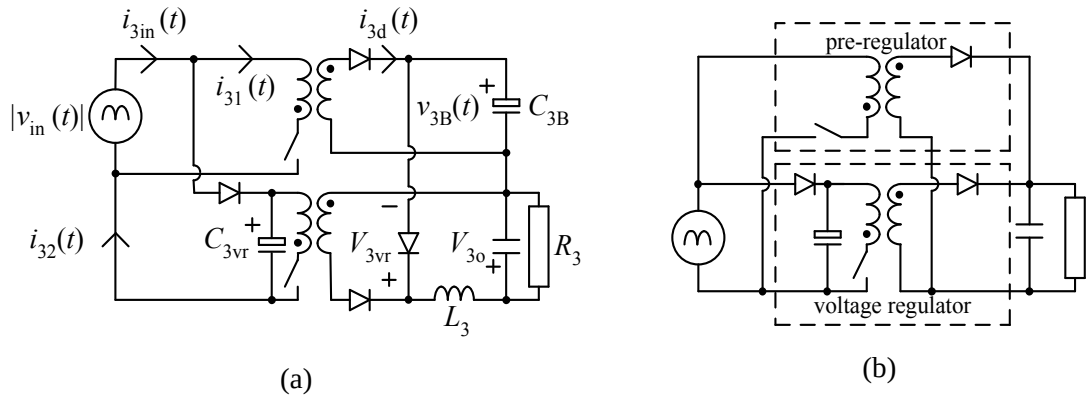


Figure 3.17: Simplified circuits of Category 3 switching regulators: (a) the Category 3 switching regulator under study proposed by Tse *et al.* circuit (Core reset arrangement is omitted for brevity) and (b) proposed by Srinivasan *et al.*

earlier by [100], [101], [102], [103] belong to Category 3. In fact, Category 3 switching regulators can be represented by several power flow diagrams [84], as shown in Fig. 3.16. Two simplified circuits of Category 3 switching regulators are shown in Fig. 3.17. The following discussion investigates the Category 3 switching regulator shown in Fig. 3.17 (a).

The Category 3 switching regulator under study employs a flyback converter as a pre-regulator and a single-switch two-input forward converter [105] as a voltage regulator. The output voltage, V_{3o}, of the noncascading switching regulator is supported by two voltage sources, $v_{3B}(t)$ and V_{3vr}. $v_{3B}(t)$ and V_{3vr} are the output voltage of the pre-regulator and the step-down input voltage of the voltage regulator, respectively. To achieve the load voltage regulation, these voltage sources must fulfill the condition that $v_{3B}(t) < V_{3o} < V_{3vr}$. According to [105], the output power of the noncascading switching regulator supporting by the pre-regulator can be expressed as

$$P_{3pfc}(t) = v_{3B}(t)\frac{V_{3o}}{R_3} \tag{3.19}$$

where $v_{3B}(t)$ is equal to $V_{3B} - \hat{v}_3 \sin 4\pi f_m t$. V_{3B} and $\hat{v}_3$ are the static voltage of C_{3B} and the peak ripple voltage of C_{3B}, respectively. The remaining output power is transferred from the voltage regulator and is given by

$$P_{3vr}(t) = (V_{3o} - v_{3B}(t))\frac{V_{3o}}{R_3} \tag{3.20}$$

where R_3 is the output load of the noncascading switching regulator. From (3.4), the split factor is given by

$$k_3(t) = \frac{P_{3vr}(t)}{P_{3pfc}(t) + P_{3vr}(t)} = \frac{V_{3o} - v_{3B}(t)}{V_{3o}}. \tag{3.21}$$

To calculate the overall efficiency, $k_3(t)$ is averaged over the ac mains period and can be defined as

$$\begin{aligned} k_3 &= \frac{1}{2\pi}\int_0^{2\pi} \frac{V_{3\mathrm{o}} - (V_{3\mathrm{B}} - \hat{v}_3 \sin 4\pi f_{\mathrm{m}} t)}{V_{3\mathrm{o}}} d(2\pi f_{\mathrm{m}} t) \\ &= \frac{V_{3\mathrm{o}} - V_{3\mathrm{B}}}{V_{3\mathrm{o}}}. \end{aligned} \tag{3.22}$$

Based on (3.4) and (3.22), Fig. 3.18 shows the noncascading switching regulator overall efficiency as a function of individual efficiencies of the pre-regulator and the voltage regulator. In Category 3, the input power is processed by either the pre-regulator or the voltage regulator only. For achieving higher overall efficiency in Category 3 switching regulators, the more efficient converter should process the large portion of the input power. In the Category 3 switching regulator under study, the pre-regulator efficiency is a dominant factor to control the overall efficiency when k_3 is close to 0. On the other hand, the voltage regulator efficiency determines the overall efficiency when k_3 approaches 1. The overall efficiency of the noncascading switching regulator over that of the classical switching regulator is quantified in Fig. 3.19. It shows that using Category 3 switching regulators can provide more efficient power conversion than Category 1 and Category 2, because no input power is processed by the pre-regulator and the voltage regulator serially in Category 3 switching regulators. However, only increasing k_3 cannot increase in the overall efficiency in Category 3 switching regulator over that in the classical switching regulator. For example, referring to Fig. 3.19, if the efficiencies of the pre-regulator and the voltage regulator are both at 70 %, the increased efficiencies at $k_3 = 0.3$ and $k_3 = 0.5$ are both 21 %.

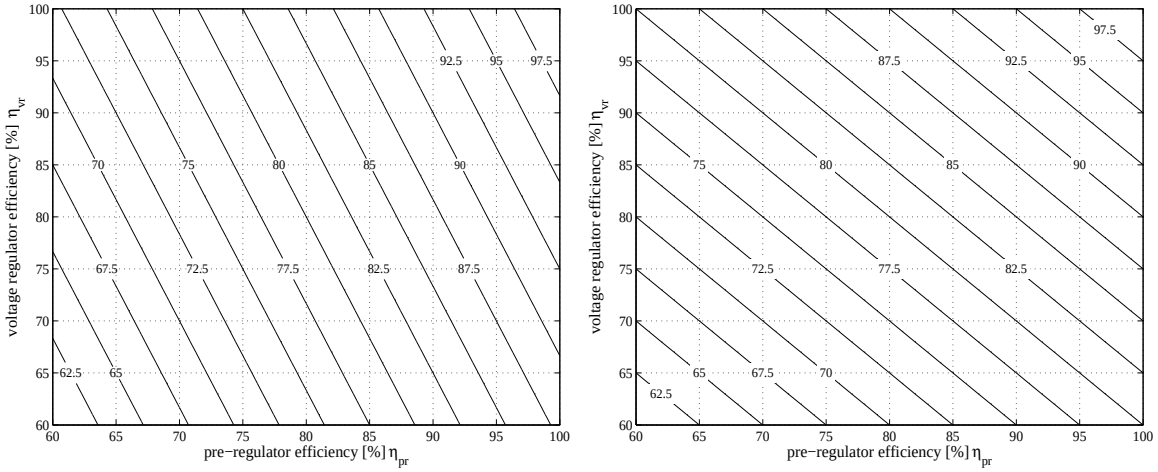
To satisfy the international standards [13], [14], a prediction of the input current harmonic in the noncascading switching regulator should be performed. From Fig. 3.17 (a), the rectified input current is

$$i_{3\mathrm{in}}(t) = \hat{i}_{31} |\sin 2\pi f_{\mathrm{m}} t| + i_{32}(t) \tag{3.23}$$

where $\hat{i}_{31}|\sin 2\pi f_{\mathrm{m}} t|$ is the pre-regulator input current and $\hat{i}_{31}$ can be calculated as

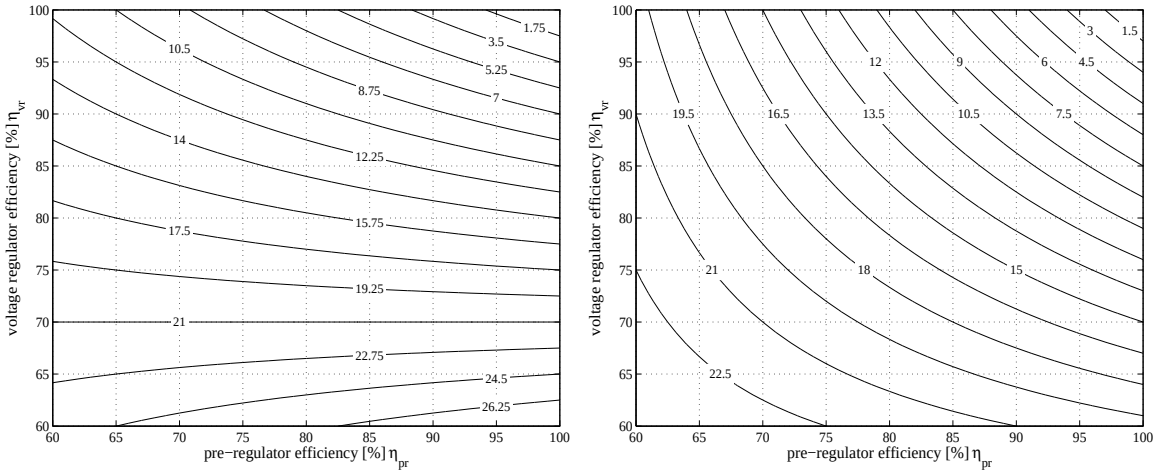
$$\hat{i}_{31} = \frac{2(1-k_3)P_{3\mathrm{out}}}{\hat{v}_{\mathrm{in}}\eta_{\mathrm{pr}}} \tag{3.24}$$

where $\hat{v}_{\mathrm{in}}$ and η_{pr} are the peak input voltage of the noncascading switching regulator and the efficiency of the pre-regulator, respectively. $i_{32}(t)$ is the only source that introduces the harmonic current in $i_{3\mathrm{in}}(t)$. For a given output power, $i_{32}(t)$ is controlled by the rectified capacitor, $C_{3\mathrm{vr}}$, and k_3. PSpice simulation provides a simple way to calculate the input current harmonic contents. Fig. 3.20 depicts the simulated input current waveforms with the input voltage of the noncascading switching regulator at different values of k_3 and $C_{3\mathrm{vr}}$. Fig. 3.21 shows the simulated results about k_3 versus the total harmonic distortion of $i_{3\mathrm{in}}(t)$ at $P_{3\mathrm{out}} = 200$ W. The total harmonic distortion of $i_{3\mathrm{in}}(t)$ is proportional to k_3 and $C_{3\mathrm{vr}}$. In this case, the maximum allowable k_3 within IEC 61000-3-2 Class D limit is equal to 0.5 when $C_{3\mathrm{vr}}$ is equal to 22 μF. Decreasing k_3 and $C_{3\mathrm{vr}}$ can reduce the harmonic



(a) (b)

Figure 3.18: Overall efficiency of the Category 3 switching regulator under study at different values of k_3: (a) $k_3 = 0.3$ and (b) $k_3 = 0.5$.



(a) (b)

Figure 3.19: Increase in the overall efficiency in the Category 3 switching regulator under study over the classical switching regulator at different values of k_3: (a) $k_3 = 0.3$ and (b) $k_3 = 0.5$.

current contents of $i_{3\mathrm{in}}(t)$. However, using small value of $C_{3\mathrm{vr}}$ leads that the voltage regulator of the noncascading switching regulator suffers large input voltage variation. Since a buck-type converter is employed as the voltage regulator, $V_{3\mathrm{vr}}$ should be higher than the output voltage to maintain the load voltage regulation. In short, the value of $C_{3\mathrm{vr}}$ is determined by some parameters such as the transformer turns ratio, the output voltage, and input current harmonic contents. A design example of the noncascading switching regulator is shown in Section 3.4.

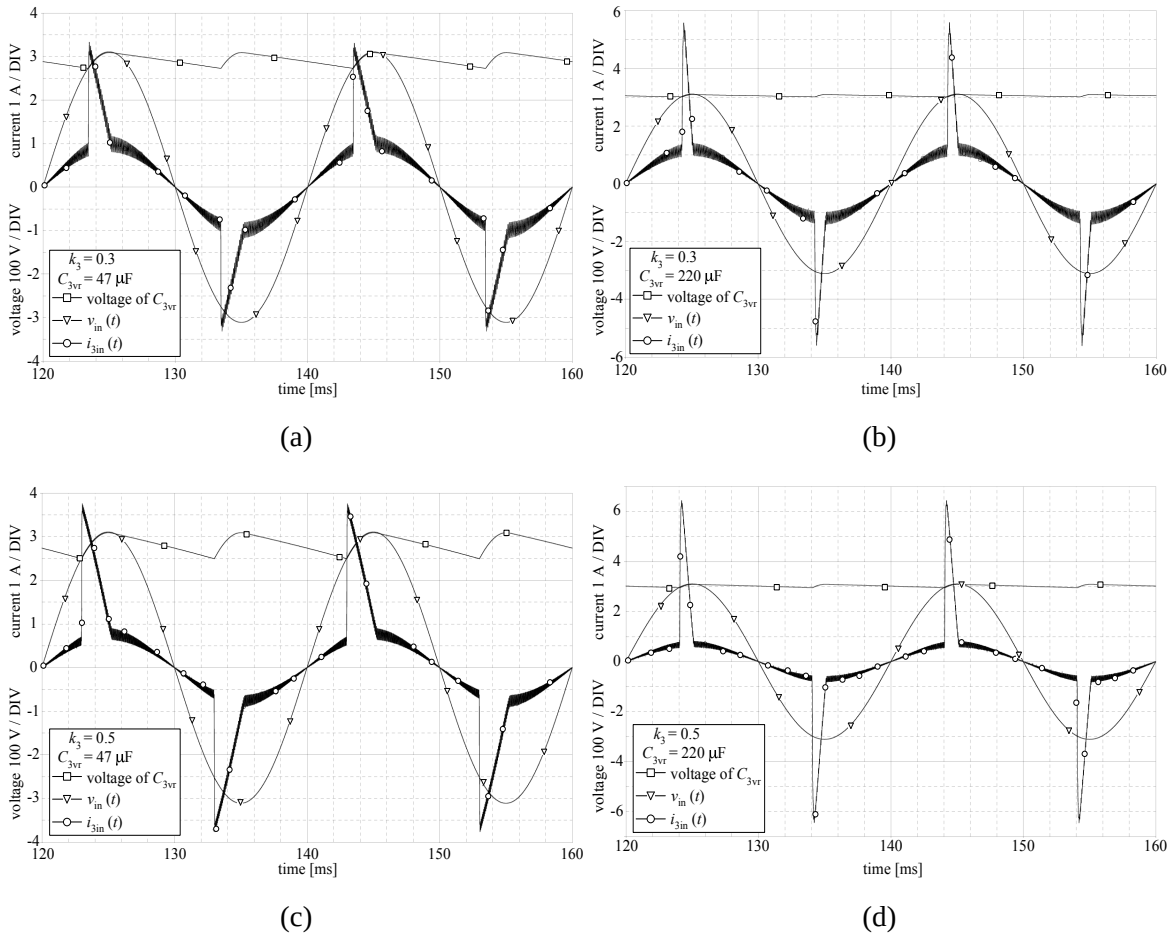


Figure 3.20: Simulated input current waveforms with input voltage of the Category 3 switching regulator under study at different values of k_3 and $C_{3\mathrm{vr}}$.

Since the range of k_3 is restricted by the harmonic current contents of $i_{3\mathrm{in}}(t)$, the variation of k_3 falls in a range between 0 to 0.5 only. From (3.22), $V_{3\mathrm{o}}$ and k_3 control the static voltage of $C_{3\mathrm{B}}$. The maximum ripple voltage of $C_{3\mathrm{B}}$ only exists for $k_3 = 0.5$, i.e. $2V_{3\mathrm{B}}$. Otherwise, the ripple voltage of $C_{3\mathrm{B}}$ must be lower than $2(V_{3\mathrm{o}} - V_{3\mathrm{B}})$. From (2.4), the minimum value of $C_{3\mathrm{B}}$ is given by

$$C_{3\mathrm{B}_{\min}} = \frac{P_{3\mathrm{out}}}{2\pi f_{\mathrm{m}}} \frac{1 - k_3}{2(V_{3\mathrm{o}} - V_{3\mathrm{B}})\eta_{\mathrm{pr}}} \tag{3.25}$$

where $P_{3\mathrm{out}}$ is the output power of the noncascading switching regulator and f_{m} is the ac main frequency.

As discussed before, $v_{3\mathrm{B}}(t)$ must be smaller than $V_{3\mathrm{o}}$ to fulfill the voltage regulation. $C_{3\mathrm{B}_{\min}}$ only provides the voltage regulation in the steady state. In the load transient condition, Fig. 3.22 shows the simulated voltage waveforms, $V_{3\mathrm{o}}$ and $v_{3\mathrm{B}}(t)$, at $k_3 = 0.1$. For k_3 close to 0, when the minimum capacitance of $C_{3\mathrm{B}}$ is employed, $v_{3\mathrm{B}}(t)$ may overtake the output voltage at a negative stepped load.

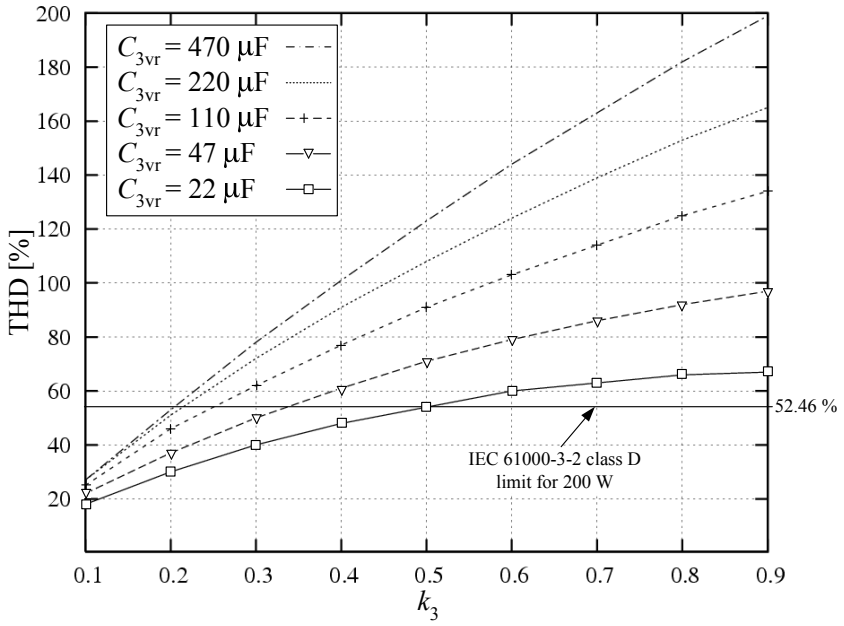


Figure 3.21: Relation between the split factor and the total harmonic distortion of $i_{3\mathrm{in}}$ using the rectified capacitor values as a parameter. $v_{\mathrm{in}}(t) = 220\sqrt{2}\sin 2\pi 50t$.

However increasing $C_{3\mathrm{B}}$ can enhance the output voltage overshoot of the noncascading switching regulator. This output voltage regulation performance of the noncascading switching regulator in the load transient condition resembles to that of the previous Category 2 switching regulator under study. Since $v_{3\mathrm{B}}(t)$ is controlled by the sluggish voltage control loop of the pre-regulator, the voltage overshoot calculation at $C_{3\mathrm{B}}$ is similar to the computation of the output voltage overshoot in the case of Category 2. Fig. 3.23 shows the pre-regulator output current and the load current of the noncascading switching regulator at the negative stepped load for $k_3 = 0.1$. For example, the output power is changed from 200 W to 20 W and $V_{3\mathrm{o}}$ is equal to 48 V. Therefore, the load current is altered from 4.16 A to 0.416 A. The diode current of the pre-regulator can be approximated as

$$\begin{aligned} i_{3\mathrm{d}}(t) &\approx \frac{\hat{v_{\mathrm{in}}}\hat{i_{31}}}{2V_{3\mathrm{B}}\eta_{\mathrm{pr}}}(1-\cos 4\pi f_{\mathrm{m}}t) \\ &\approx \frac{(1-k_3)P_{3\mathrm{out}}}{V_{3\mathrm{B}}\eta_{\mathrm{pr}}}(1-\cos 4\pi f_{\mathrm{m}}t) \end{aligned} \tag{3.26}$$

where $\hat{v_{\mathrm{in}}}\hat{i_{31}}/2$ is the averaged output power of the pre-regulator. For the worst case, i.e. the maximum voltage overshoot, the negative stepped load takes place at t_{31} as depicted in Fig. 3.23. The diode current of the pre-regulator is in the form of $I_{3\mathrm{H}}(1-\cos 4\pi f_{\mathrm{m}}t)$ until t_{32}. Thus, the extra current

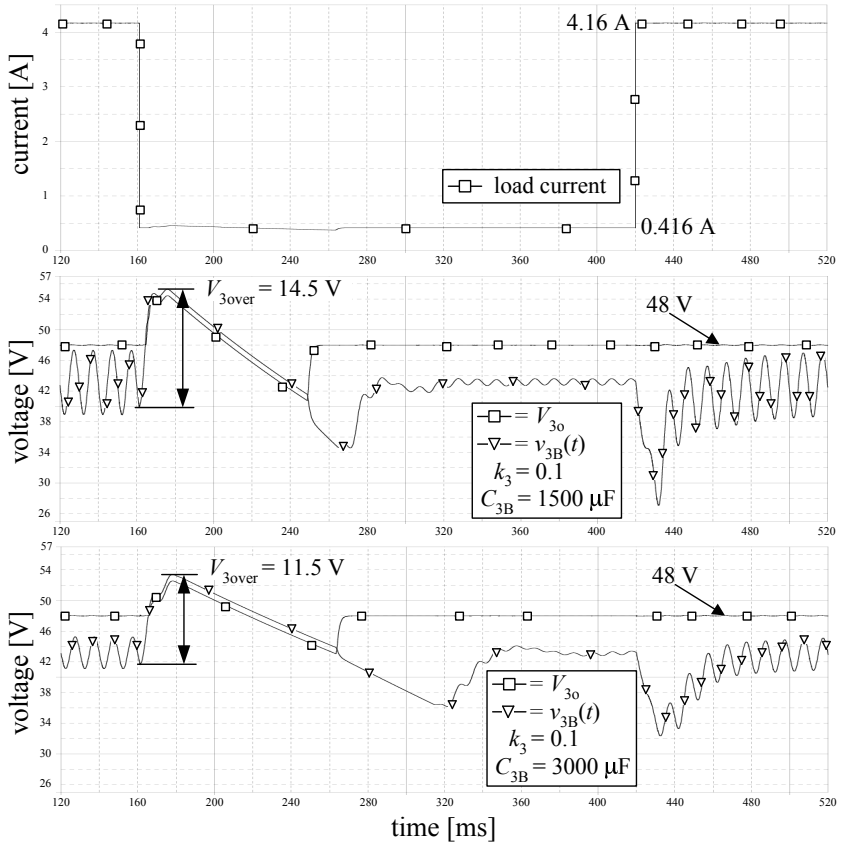


Figure 3.22: Simulation results for stepped load (200 W to 20 W and vice versa) for the Category 3 switching regulator under study.

generates the first overshoot voltage of C_{3B} is

$$I_{3e}(t) = I_{3H}(1 - \cos 4\pi f_m t) - I_{3L} \tag{3.27}$$

$$V_{3over} = \frac{1}{C_{3B}} \int_{t_{31}}^{t_{32}} I_{3e}(t)dt \tag{3.28}$$

where I_{3H} is the initial load current at the negative stepped load, I_{3L} is the final load current, and V_{3over} is the first overshoot voltage of C_{3B} generated by $I_{3e}(t)$. Based on (3.27) and (3.28), Fig. 3.24 shows V_{3over} versus C_{3B} at different values of output voltage for the load change from 200 W to 20 W at $k_3 = 0.1$. When designing the value of C_{3B}, the major consideration is to maintain the load voltage regulation in the load transient condition of the noncascading switching regulator especially k_3 close to 0.

Clearly, the split factor k_3 affects the input current harmonic contents and controls the size of the energy storage element to maintain the load regulation. In addition, k_3 defines the portion of input power processed by the pre-regulator and the voltage regulator in Category 3 switching regulators.

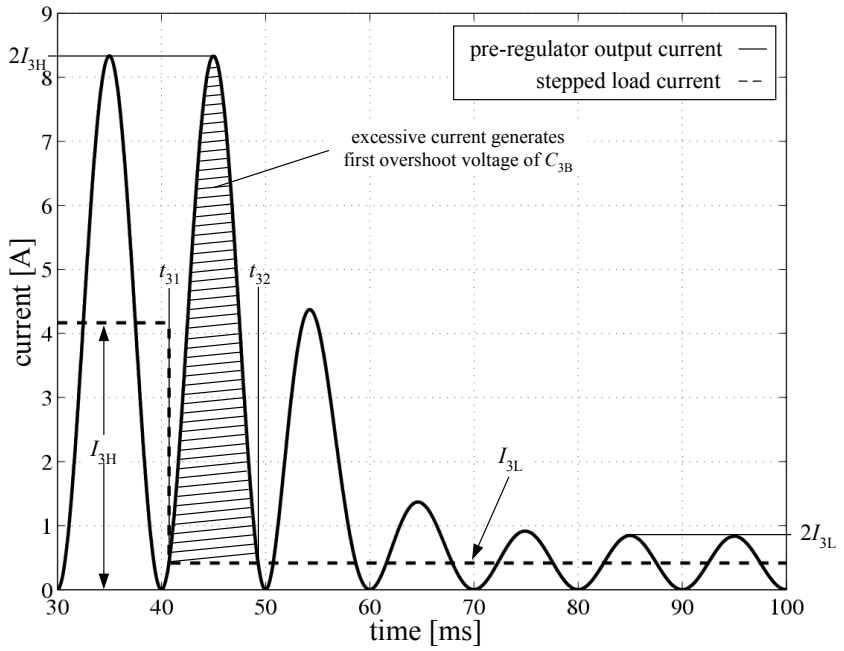


Figure 3.23: Current waveforms to illustrate the maximum overshoot voltage of the Category 3 switching regulator under study at full load to 10 % load.

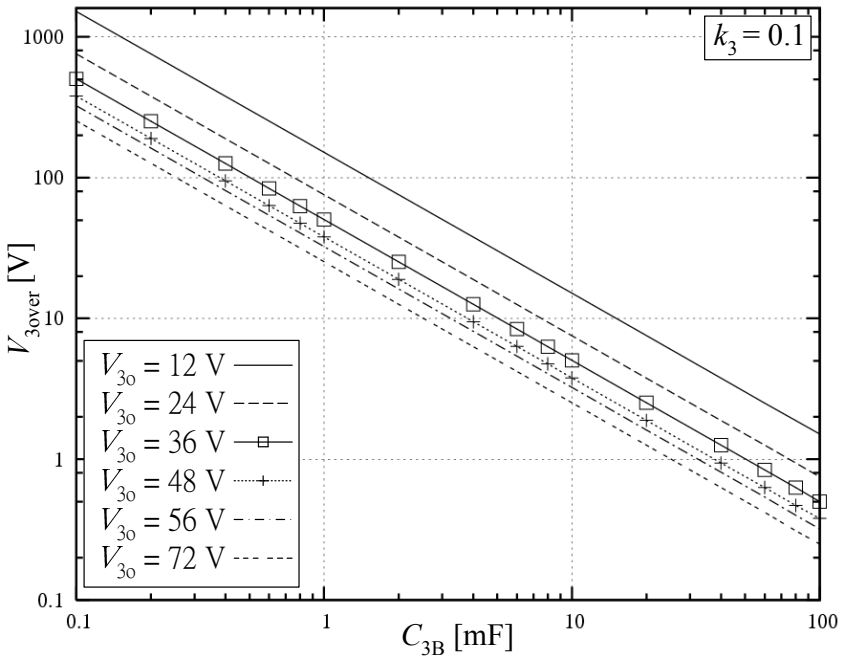


Figure 3.24: $V_{3\text{over}}$ versus $C_{3\text{B}}$ at different values of output voltage for the load change from 200 W to 20 W at $k_3 = 0.1$.

Table 3.1: Performance comparison between classical switching regulators and noncascading switching regulators.

	Classical	Category 1	Category 2	Category 3
overall efficiency	low	improved by increasing k_1 and dominant in $\eta_{\rm vr}$	improved by increasing k_2 and dominant in $\eta_{\rm pr}$	dependent on k_3, $\eta_{\rm pr}$ and $\eta_{\rm vr}$
PF	perfect	degraded by increasing k_1	perfect	degraded by increasing k_3
load voltage regulation	independent	independent	rely on energy storage	rely on energy storage
power processed by pre-regulator	$P_{\rm in}$	$(1-k_1)P_{\rm in}$	$P_{\rm in}$	$(1-k_3)P_{\rm in}$
power processed by voltage regulator	$P_{\rm out}$	$P_{\rm out}$	$k_2P_{\rm out}$ (steady state) $P_{\rm out}$ (transient)	$k_3P_{\rm out}$ (steady state) $P_{\rm out}$ (transient)
static voltage of energy storage	independent	controlled by k_1 and $\lvert v_{\rm in}(t)\rvert$	controlled by k_2 and $V_{2\rm o}$	controlled by k_3 and $V_{3\rm o}$

Increase in the overall efficiency in Category 3 switching regulator over that of the classical switching regulator is independent on the values of k_3 which relates the efficiencies of the pre-regulator and the voltage regulator.

3.3 Comparison of Three Categories

In this section, a comparison is made between classical switching regulators and the different categories of switching regulators in terms of overall efficiency, PF, power handling of the constituent converters, role of the energy storage element, etc. Table 3.1 summarizes the performances of each categories switching regulators.

1. The highest overall efficiency is Category 3 switching regulators, because the pre-regulator and the voltage regulator are parallel connected. This arrangement prevents the input power processed by the pre-regulator and the voltage regulator serially. The overall efficiency of Category 1 is governed by k_1 and the efficiency of the voltage regulator in Category 1 switching regulators. The overall efficiency of Category 2 is dominated by k_2 and the efficiency of the pre-regulator in Category 2 switching regulators.

2. Using Category 2 switching regulators and classical switching regulators, we can achieve perfect PF because the input current is fully controlled by their pre-regulators. In Category 1 and Category 3 cases, only part of the input current is governed by their pre-regulators and the PF is deteriorated by their split factors.

3. The load voltage regulation of Category 2 and Category 3 switching regulators cannot be fully regulated by their voltage regulators. In the transient state, the output capacitor is a crucial component in Category 2 and the value of the storage element is a crucial component in Category 3.

4. Pre-regulators designed for serving classical switching regulators and Category 2 switching regulators are required to handle the total input power of their switching regulators. For Category 1 and Category 3, part of the input power is directly processed by their voltage regulators, so the power handled by pre-regulator in Category 1 and Category 3 is less than the total input power and depends on the split factors.

5. The power handled by the voltage regulator is equal to the total output power for classical switching regulators and Category 1 switching regulators. In the steady state, the voltage regulator designed for Category 2 switching regulators and Category 3 switching regulators only process part of the total output power depending on their split factors, but in the load transient period, the voltage regulator in Category 2 and Category 3 are required to handle total transient power.

3.4 Experimental Results

A laboratory prototype based on the Category 3 switching regulator shown in Fig. 3.17 (a) has been constructed to meet the following major design specification: the input voltage is 220 $\mathrm{V_{rms}}$, the ac mains frequency is 50 Hz, the output voltage is 48 V, the maximin output power is 200 W, and $C_{3\mathrm{vr}}$ is fixed at 47 μF. Fig. 3.25 shows the schematic diagram of the prototype with control circuitries. An average current-mode controller is employed to provide PFC function of the flyback converter and a peak current-mode controller is used to control the single-switch two-input forward converter for voltage regulation. Figs. 3.26 and 3.27 show the input current and the input voltage at full load condition at the different values of the split factor. It reveals that the current waveform in Fig. 3.26 is close to the simulated current waveform in Fig. 3.20 (a). Fig. 3.28 depicts the measured PF and the split factor. Based on these measured results, the PFC performance of the prototype is undoubtedly deteriorated by increasing the split factor. A comparison is made between the harmonic components of the experimental prototype input current and IEC 61000-3-2 Class D Limit for 200 W output power

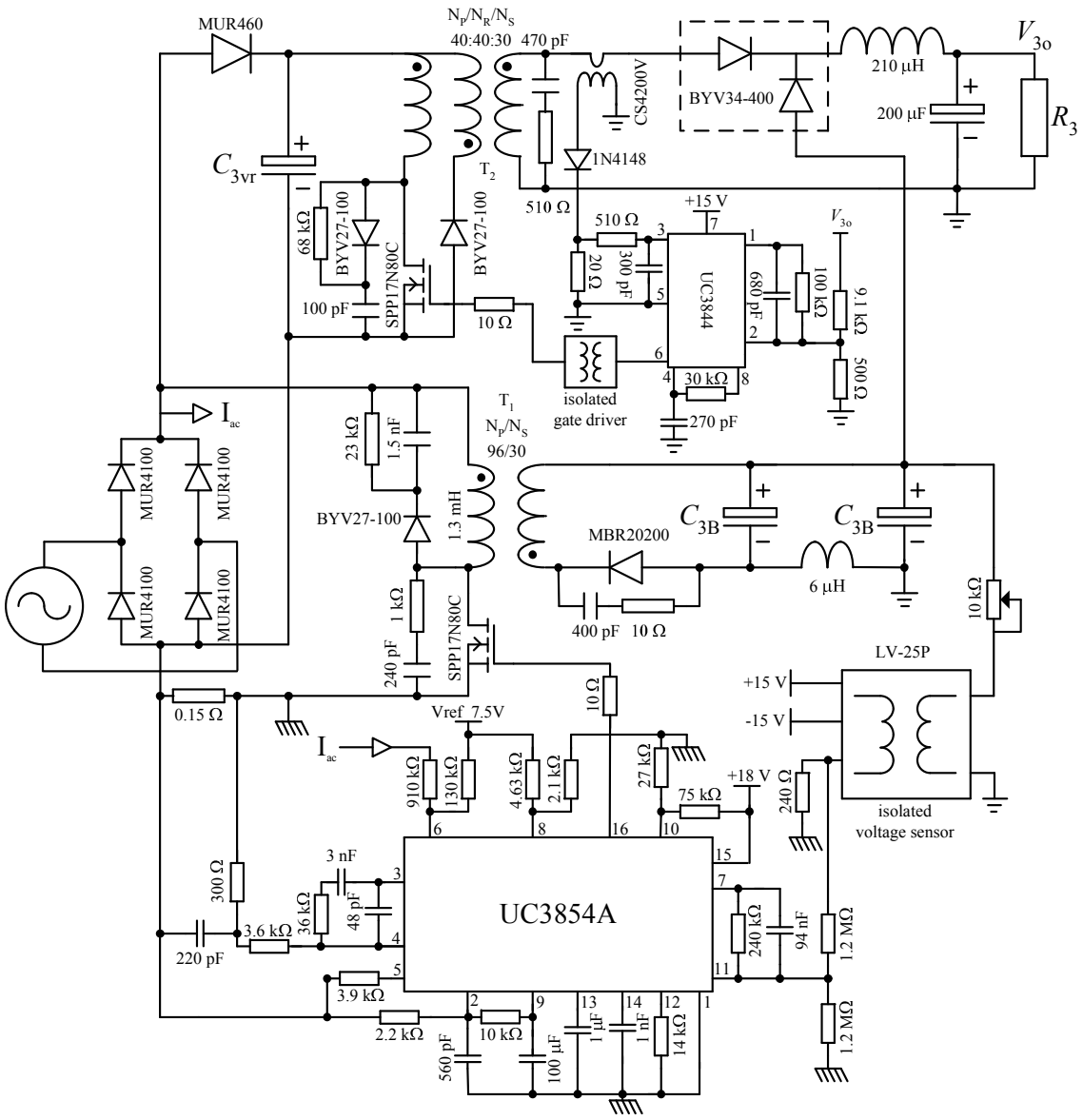


Figure 3.25: Full schematic diagram of the experimental prototype based on the Category 3 switching regulator shown in Fig. 3.17 (a).

at different split factors, as shown in Fig. 3.29. The measured results show that the prototype fails the Class D Limit when the split factor k_3 is equal to 0.4 at 9^{th} harmonic order.

Fig. 3.30 shows the measured overall efficiency curve with a split factor of 0.3. The prototype is tested over a power range from 20 W to 200 W. The overall efficiency at full load condition is around 86 %. In this split factor, the output power handling of the prototype pre-regulator is 140 W. The output power handling of the voltage regulator is 60 W in the steady state, but the prototype voltage

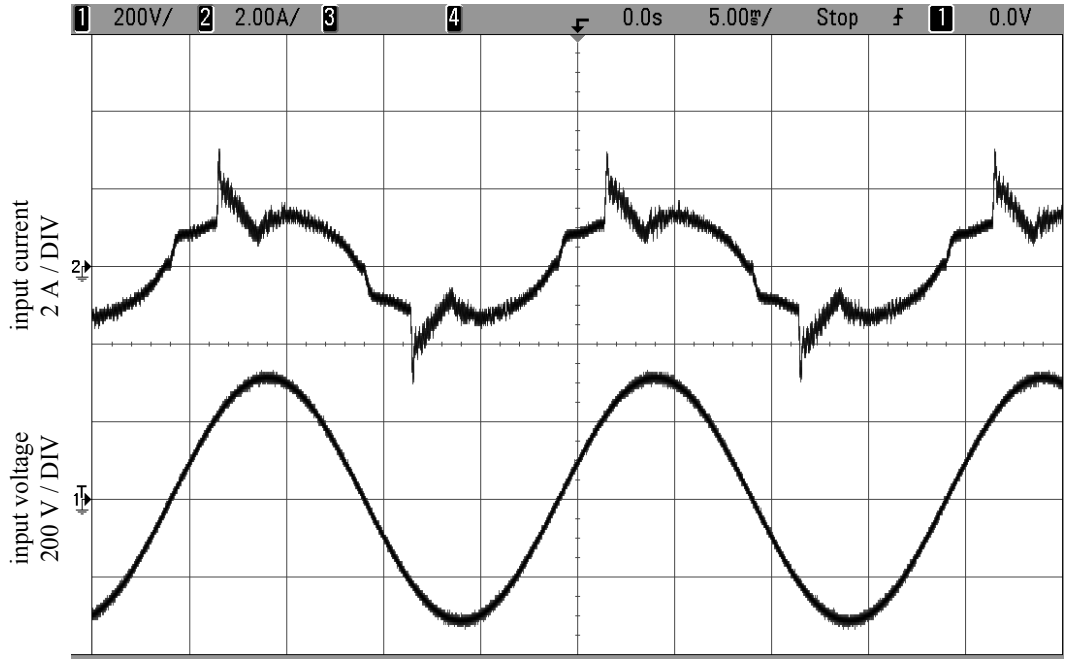


Figure 3.26: Measured input current (upper trace) with input voltage (lower trace) of the experimental prototype at $k_3 = 0.3$

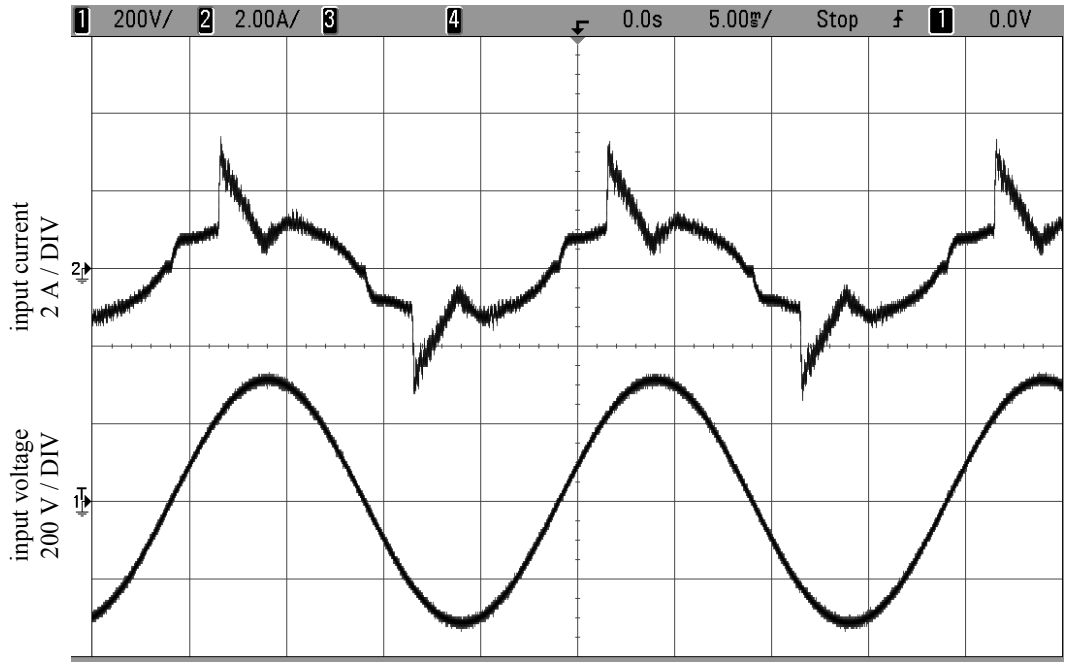


Figure 3.27: Measured input current (upper trace) with input voltage (lower trace) of the experimental prototype at $k_3 = 0.4$

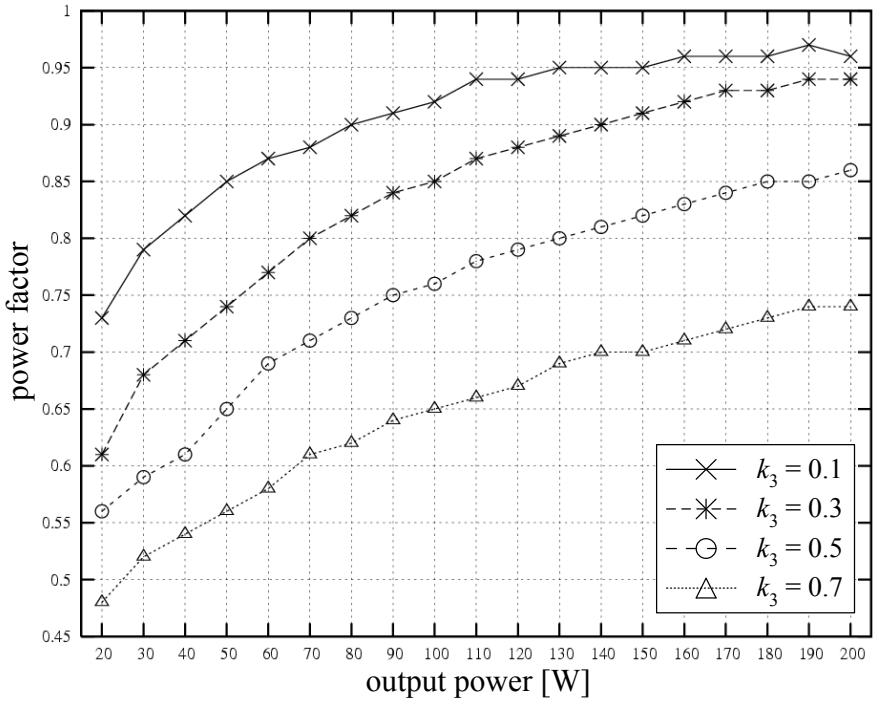


Figure 3.28: PF versus output power from 20 W to 200 W at the different values of the split factor.

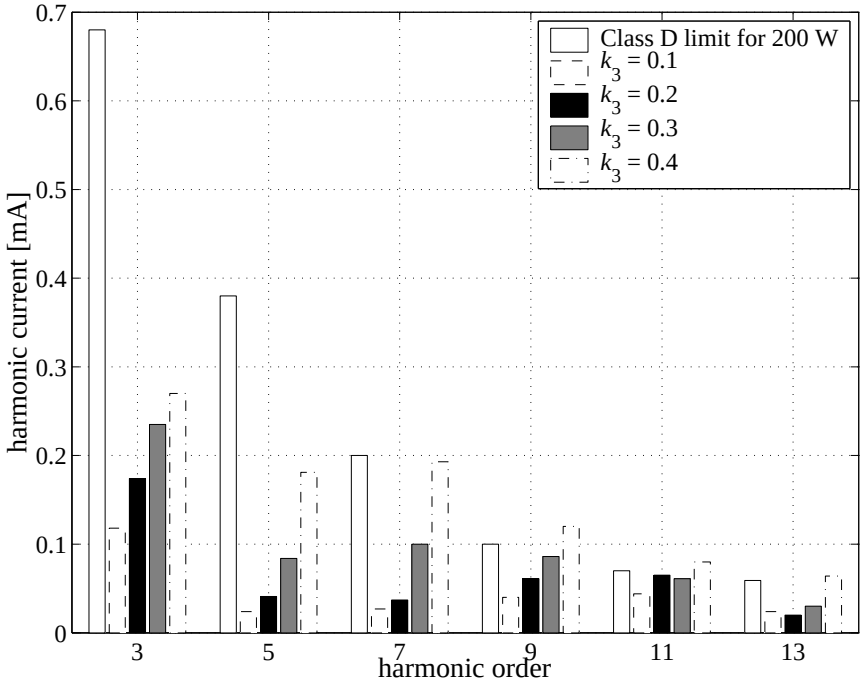


Figure 3.29: Measured harmonic input current components of the experimental prototype comparing with IEC 61000-3-2 Class D limit for 200 W output power.

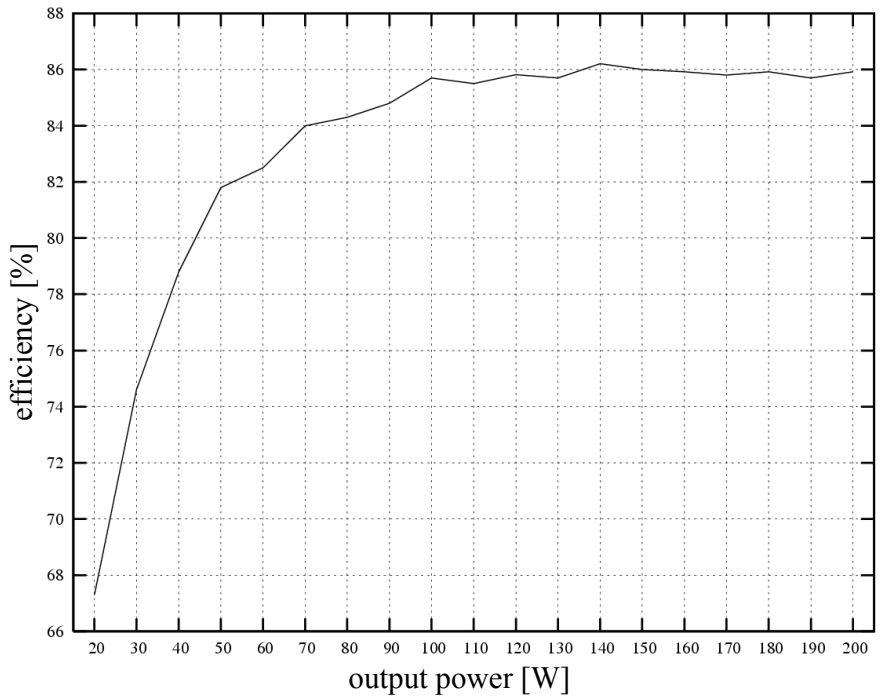


Figure 3.30: Efficiency versus output power from 20 W to 200 W with a split factor of 0.3.

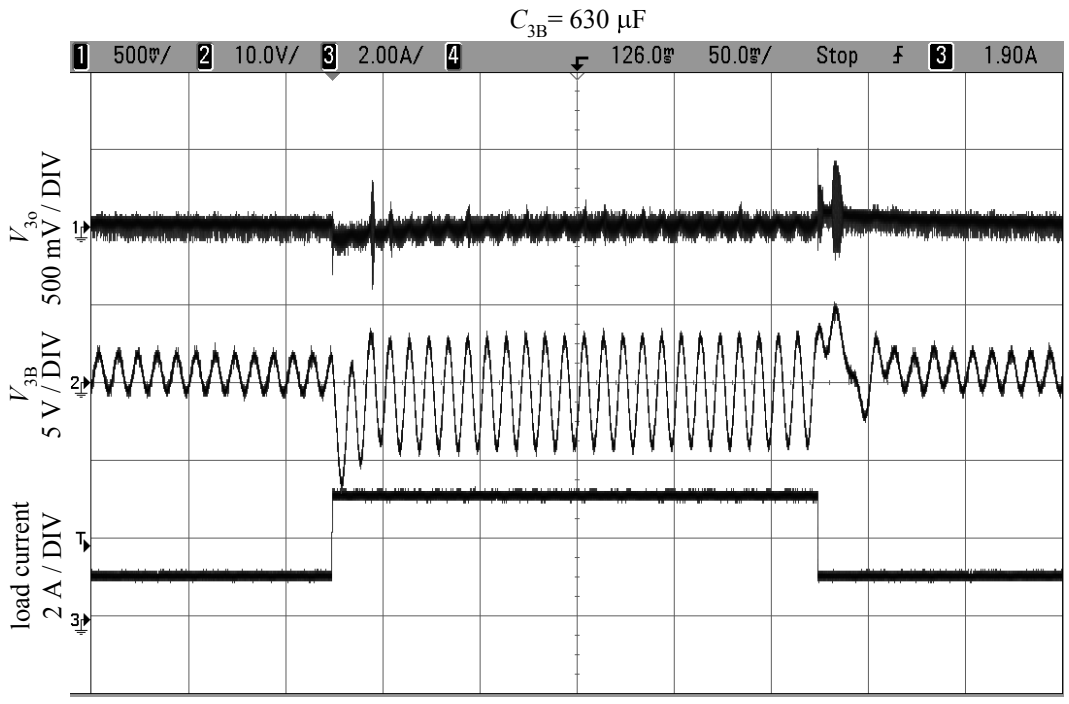


Figure 3.31: Measured output voltage (upper trace), voltage of energy storage element (middle trace), and load current (lower trace) at $C_{3B} = 630$ μF with a split factor of 0.3. Time scale = 50 ms / DIV.

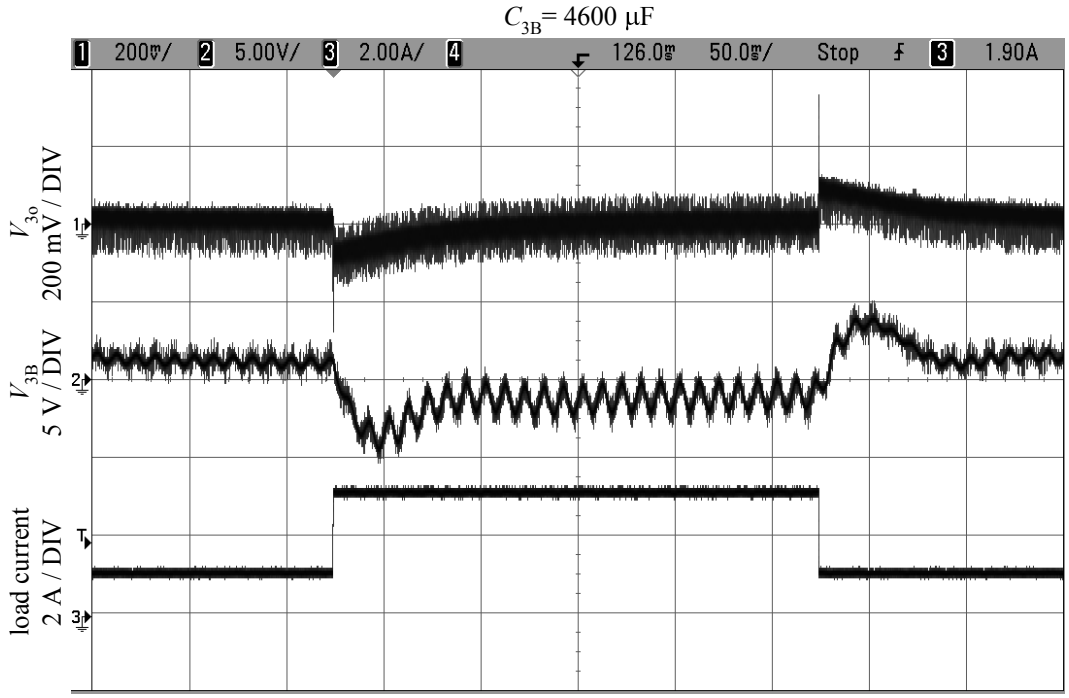


Figure 3.32: Measured output voltage (upper trace), voltage of energy storage element (middle trace), and load current (lower trace) at $C_{3B} = 4600$ μF with a split factor of 0.3. Time scale = 50 ms / DIV.

regulator needs to handle all the transient output power in the positive stepped load. To provide similar overall efficiency performance as the classical switching regulator, the pre-regulator and the voltage regulator efficiencies are required to be higher than 93.7 %. Furthermore, both constituent regulators of the classical switching regulator are required to handle at least the total output power. Figs. 3.31 and 3.32 show the performance of the load voltage regulation of the prototype for the output power changing from 50 W to 150 W and vice versa. These figures show the output voltage (upper trace), the voltage of the energy storage element (middle trace), and the load current (lower trace) at the different values of C_{3B} with a split factor of 0.3. The load voltage regulation is deteriorated by the reduced values of the energy storage element.

3.5 Summary

In view of the number of noncascading switching regulators reported recently, this chapter has presented a systematic study of the noncascading switching regulators characteristics with an aim to understanding the various attainable performances. Many switching regulators are constructed from a noncascading structure, i.e., the pre-regulator and the post voltage regulator are not connected in cascade. Efficiency is generally improved, but often at a price. The chapter has shown the relation-

ship between the type of structure and the possible tradeoff it offering to engineers. Specifically, the analysis has considered efficiency, PF and the size of the energy storage element for load voltage regulation. Describing how different structures affect the optimization of the different performance areas. Hence, according to the analyses, a summary has made to explain the performances of each category of switching regulators. Some simulation and experimental results have illustrated the basic phenomena.

Chapter 4

Practical Design and Evaluation of 1 kW Noncascading Switching Regulator

The theoretical analysis of the achievable performances in the noncascading switching regulators has already been performed as given in the previous chapter. The noncascading switching regulators can achieve a higher overall efficiency as a result of the use of a noncascading structure that involves less repeated processing of the input power, but the achievable performances of the noncascading switching regulators may be degraded.

Despite its simplicity, the conventional design of ac-dc switching regulators based on cascading a pre-regulator and a voltage regulator incurs an efficiency penalty due to redundant power processing, as illustrated in the power flow diagram shown in Fig. 4.1. To improve the overall efficiency, many noncascading structures have been proposed for constructing the ac-dc switching regulator with PFC and tight voltage regulation. These noncascading switching regulators allow part of the input power to be processed by only one power stage, thereby reducing the amount of power redundantly processed by the two constituent power converters. As discussed, there are three categorized noncascading structures to reducing the redundant power processing. One of the categorized noncascading structures can create a unity PF noncascading switching regulators [95], [98], [106], [107], and [108]. Fig. 4.2 shows the power flow diagram of the unity PF noncascading switching regulator.

This chapter investigates the unity PF noncascading switching regulator, which is classified as Category 2, for serving 1 kW output power. The noncascading switching regulator employs a current-fed full-bridge converter as the pre-regulator, and a buck-boost converter as the voltage regulator. Both regulators are operated in CCM. The advantage of CCM is that the current stress of the devices of the regulators is relatively low, and hence is more suitable for high-power applications. The objective in this chapter, however, is to provide a detailed consideration of several practical issues related to the

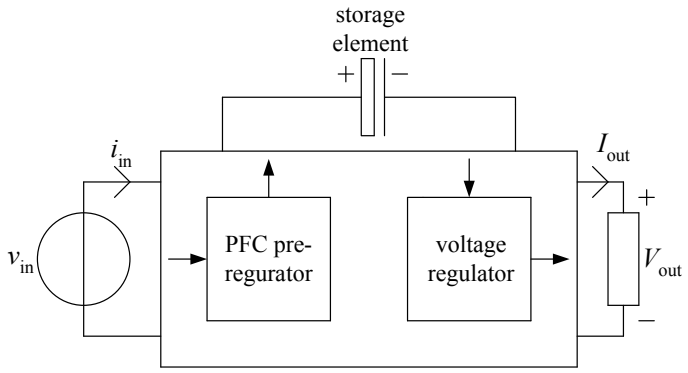


Figure 4.1: Power flow diagram for the classical switching regulator. All power is processed by the two stages serially.

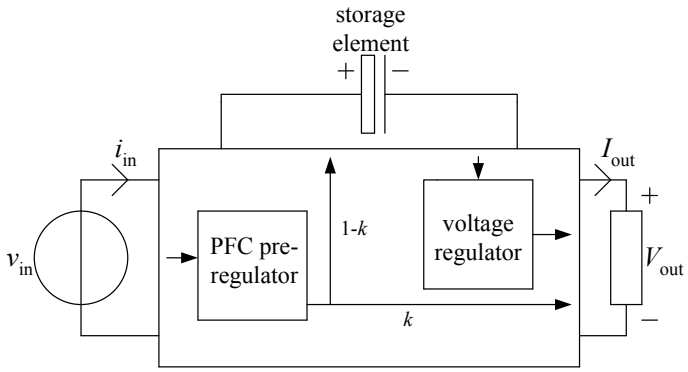


Figure 4.2: Power flow diagram for the noncascading switching regulator under study, where k is the fraction of power that goes to the output directly after being processed by the pre-regulator.

design of this Category noncascading switching regulator. Specifically, the relationships between the gained efficiency, the load transient response and the capacitive components requirements of this noncascading switching regulator will be examined in order to confirm the theoretical analysis. Beside, care over implementing in these two converters will also be reported.

4.1 Summary of Theoretical Analysis in the Noncascading Switching Regulator

The schematic of the Category 2 noncascading switching regulator under study is shown in Fig. 4.3. It consists of a current-fed full-bridge converter and a buck-boost converter connected in the Category 2 noncascading structure fashion. To maintain power balance, a low-frequency storage element is required to buffer the difference between the instantaneous input power and output power. Capacitor $C_{\rm B}$ and $C_{\rm o}$ are connected serially. The series combination forms the loading for the current-fed full-

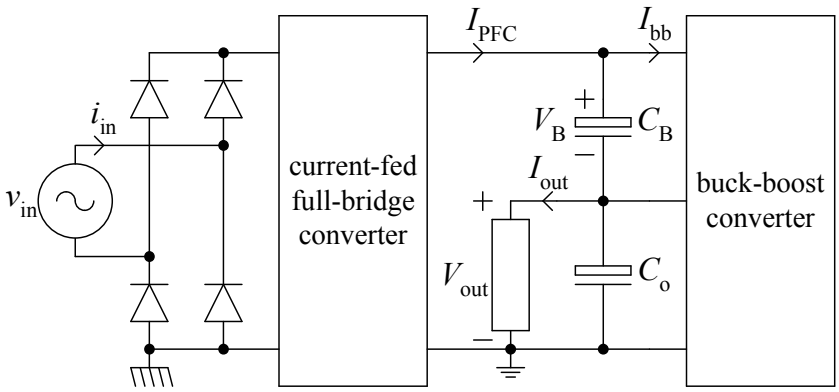


Figure 4.3: Schematic diagram of the noncascading switching regulator.

bridge converter. Thus, a portion of the output energy from the converter is transferred directly to the output since $C_{\rm o}$ is in parallel with the load. Due to the tight voltage regulation of the buck-boost converter, the voltage of $C_{\rm o}$ is free of low-frequency ripple. Therefore, as far as the current-fed full-bridge converter is concerned, the voltage of $C_{\rm o}$ can be considered practically as a voltage source and only $C_{\rm B}$ serves as an energy storage element. Furthermore, the dc output voltage of the current-fed full-bridge converter must be larger or minimum equal to $V_{\rm out}$ in order to meet the load voltage regulation requirement.

4.1.1 Split Factor Versus Efficiency Gain

One crucial parameter in the design of the Category 2 noncascading switching regulator is the fraction of input power which is processed only once, i.e., by only one converter [84], [87]. The theoretical efficiency of the Category 2 noncascading switching regulator is described in the following equation:

$$\begin{aligned} \eta_{\rm Category2} &= (1-k)\eta_{\rm pfc}\eta_{\rm vr} + k\eta_{\rm pfc} \\ &= \eta_{\rm pfc}\eta_{\rm vr} + \eta_{\rm pfc}k(1-\eta_{\rm vr}) \end{aligned} \tag{4.1}$$

where $\eta_{\rm pfc}$ and $\eta_{\rm vr}$ are the efficiencies of the pre-regulator and the voltage regulator, respectively, and k is the split factor which is defined as the ratio at which the amount of the input power is split at the output of the pre-regulator to the output load. The efficiency gain of the Category 2 noncascading switching regulator is $k\eta_{\rm pfc}(1-\eta_{\rm vr})$. Obviously, the overall efficiency depends on the pre-regulator efficiency since the total input power from the ac mains must be processed by the pre-regulator before it is transferred to the load or the voltage regulator.

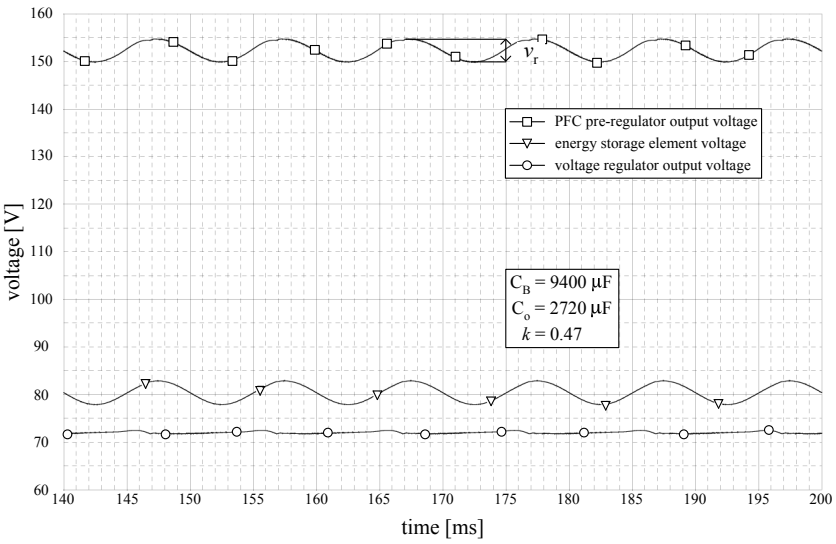


Figure 4.4: Simulated voltage waveforms of the noncascading switching regulator under study for $k = 0.47$.

4.1.2 Split Factor Versus Transient Response

In this Category 2 noncascading switching regulator under study, k affects the efficiency gain and the load transient response. The total current harmonic distortion is independent of this factor due to the input current being fully processed by the pre-regulator. Referring to Figs. 4.3 and 4.4, the output power of the pre-regulator can be written as

$$P_{\rm PFC} = I_{\rm PFC}(\frac{v_r}{2}\sin 2\omega t + V_{\rm B} + V_{\rm out}) \tag{4.2}$$

and

$$P_{\rm direct} = I_{\rm PFC}V_{\rm out}. \tag{4.3}$$

From (4.2) and (4.3), the directed power can be calculated as

$$P_{\rm direct} = \frac{V_{\rm out}}{\frac{v_r}{2}\sin 2\omega t + V_{\rm B} + V_{\rm out}}P_{\rm PFC} \tag{4.4}$$

where $P_{\rm PFC}$ and $I_{\rm PFC}$ are the output power and the output current of the current-fed full-bridge converter, and $P_{\rm direct}$ denotes the amount of output power of the converter directly transferred to the load. Also, $\frac{v_r}{2}\sin 2\omega t$ and $V_{\rm B}$ represent the low-frequency ripple voltage and the static voltage of $C_{\rm B}$, respectively, and ω is the angular frequency of the ac mains. Therefore, the low-frequency ripple voltage affects k according to

$$k(t) = \frac{V_{\rm out}}{\frac{v_r}{2}\sin 2\omega t + V_{\rm B} + V_{\rm out}} \quad \text{for} \quad 0 < k(t) < 0.5. \tag{4.5}$$

Moreover, for calculating the overall efficiency, $k(t)$ can be averaged over the ac mains period and represented by

$$k = \frac{V_{\rm out}}{V_{\rm B} + V_{\rm out}} \tag{4.6}$$

which is consistent with the results reported in Garcia *et al.* [95], [106].

Furthermore, according to (4.5), the input voltage of the buck-boost converter is determined by $V_{\rm out}$ and $k(t)$. Now, if the effect of the controller on the load transient response is ignored, the transient response time is purely controlled by the input voltage of the voltage regulator at the positive stepped load. From Fig. 4.3, volt-second balance equation of the buck-boost converter inductor, L_2, can be written as

$$\frac{\Delta I_{\rm bb}}{\Delta t} = \frac{\frac{v_{\rm r}}{2}\sin 2\omega t + V_{\rm B}}{L_2}, \tag{4.7}$$

where $\Delta I_{\rm bb}$ is the change in input current of the buck-boost converter at the load transient at the positive stepped load, Δt is the transient response time, and L_2 is the inductance of the converter. Assume that the duty cycle is unity in the transient period. Since the current-fed full-bridge converter is controlled by a low bandwidth (one-fifth of the ac mains frequency) voltage control loop to maintain PFC [104], only the buck-boost converter would provide transient power to the load. Suppose the load changes from 10% to 90% of the full load condition during transient. Then, we have

$$\Delta I_{bb} = \frac{(0.9P_{\rm out} - 0.1P_{\rm out})}{\eta_{\rm vr}(\frac{v_{\rm r}}{2}\sin 2\omega t + V_{\rm B})} \tag{4.8}$$

where $P_{\rm out}$ is the full output power drawn from the load. Therefore, putting (4.8) in (4.7), the transient response time is expressed as

$$\Delta t = \frac{(0.9 - 0.1)P_{\rm out}L_2}{\eta_{\rm vr}(\frac{v_{\rm r}}{2}\sin 2\omega t + V_{\rm B})^2}, \tag{4.9}$$

$$= \frac{(0.9 - 0.1)P_{\rm out}L_2k^2(t)}{\eta_{\rm vr}(V_{\rm out} - V_{\rm out}k(t))^2}. \tag{4.10}$$

Referring to (4.5), the low-frequency ripple voltage is one of the parameters that affect the load transient response. Fig. 4.5 shows the simulation results based on (4.5) and (4.10) to illustrate the relation between the transient time and the split factor for different values of output voltage. For brevity, the transient response time can be normalized as

$$f_1 = \frac{k^2(t)}{(V_{\rm out} - V_{\rm out}k(t))^2} \tag{4.11}$$

where f_1 is in proportion to the transient response time. In Fig. 4.5, k is fixed at 0.35, and $v_{\rm r}$ is equal to $V_{\rm B}$ (maximum allowable ripple voltage). The transient response time of the voltage regulator increases as $k(t)$ and $V_{\rm out}$ increase. Evidently, the split factor $k(t)$ not only controls the efficiency gain of the noncascading switching regulator, but also affects the load transient response of the voltage regulator.

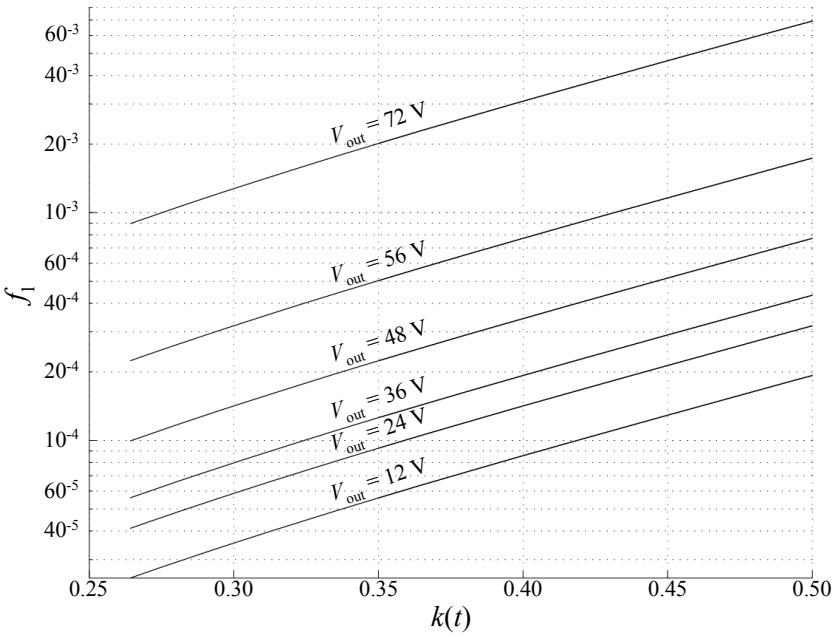


Figure 4.5: The normalized transient response, f_1, versus the split factor k for different values of output voltage for $k = 0.35$.

4.1.3 Split Factor Versus Size of the Storage Element

The storage element plays an important role in any switching regulators. Suppose the current-fed full-bridge converter delivers a constant output power, $P_{\rm PFC}$. Then, the power drawn from the ac mains with unity PF is

$$P_{\rm mains} = \frac{P_{\rm PFC}(1 - \sin 2\omega t)}{\eta_{\rm pfc}}. \tag{4.12}$$

The minimum stored energy necessary for achieving unity PF is equal to the difference between the energy consumed by the constant power load and the energy delivered by the ac mains during one-quarter of its period $\frac{\pi}{2\omega}$ starting with zero energy. The energy consumed by the load during $0 < t < \frac{\pi}{2\omega}$ is

$$E_{\rm dc} = \frac{P_{\rm PFC}}{\eta_{\rm pfc}} \frac{\pi}{2\omega}. \tag{4.13}$$

The energy delivered by the ac mains during $0<t<\frac{\pi}{2\omega}$ is

$$\begin{aligned} E_{\rm ac} &= \int_0^{\frac{\pi}{2\omega}} \frac{P_{\rm PFC}}{\eta_{\rm pfc}}(1 - \sin 2\omega t)dt \\ &= \frac{P_{\rm PFC}}{\eta_{\rm pfc}} \left(\frac{\pi}{2\omega} - \frac{1}{\omega} \right). \end{aligned} \tag{4.14}$$

The minimum stored energy of the storage element is the difference between the two energies, i.e.,

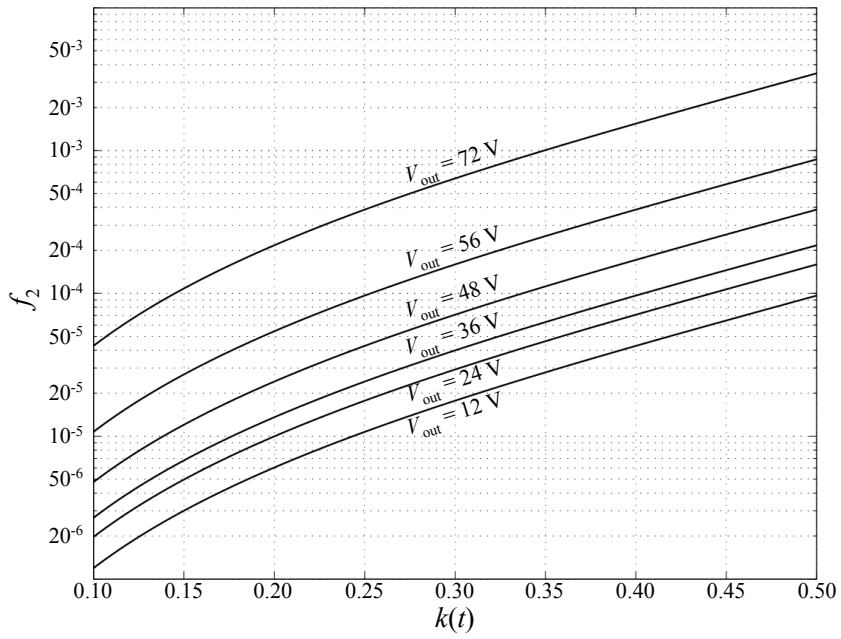


Figure 4.6: The minimum capacitance of the storage element in the different k at the different values of the output voltage. $f_2 = 1/(2V_{\rm B}^2)$.

$$\begin{aligned} E_{\rm C_{B_{min}}} &= E_{\rm dc} - E_{\rm ac} \\ &= \frac{P_{\rm PFC}}{\eta_{\rm pfc}\omega}. \end{aligned} \tag{4.15}$$

In the Category 2 noncascading switching regulator under study, the storage element is a capacitor $C_{\rm B}$. Referring to Fig. 4.4, the energy stored in the capacitor is

$$\begin{aligned} E_{\rm C_B} &= \frac{1}{2}C_{\rm B}((V_{\rm B} + \frac{v_{\rm r}}{2})^2 - (V_{\rm B} - \frac{v_{\rm r}}{2})^2) \\ &= C_{\rm B}V_{\rm B}v_{\rm r}. \end{aligned} \tag{4.16}$$

Using (4.15) and (4.16), the voltage ripple of $C_{\rm B}$

$$v_{\rm r} = \frac{P_{\rm PFC}}{\eta_{\rm pfc}\omega C_{\rm B}V_{\rm B}}. \tag{4.17}$$

Basically, the calculation of the voltage ripple in this noncascading switching regulator energy storage element is similar to the classical switching regulator. Thus, the voltage ripple amplitude can be reduced by using a large capacitor under a high static stress. In the case of this noncascading switching regulator, for maintaining the unity PF operation and output voltage regulation, the size of storage capacitance required is minimal if the capacitor voltage is allowed to vary at twice the value of the static voltage during each half of the ac mains period, i.e., $v_{\rm r} = 2V_{\rm B}$. The minimum size of storage capacitance required is

$$C_{\rm B_{min}} = \frac{P_{\rm PFC}}{\eta_{\rm pfc}\omega 2{V_{\rm B}}^2}. \tag{4.18}$$

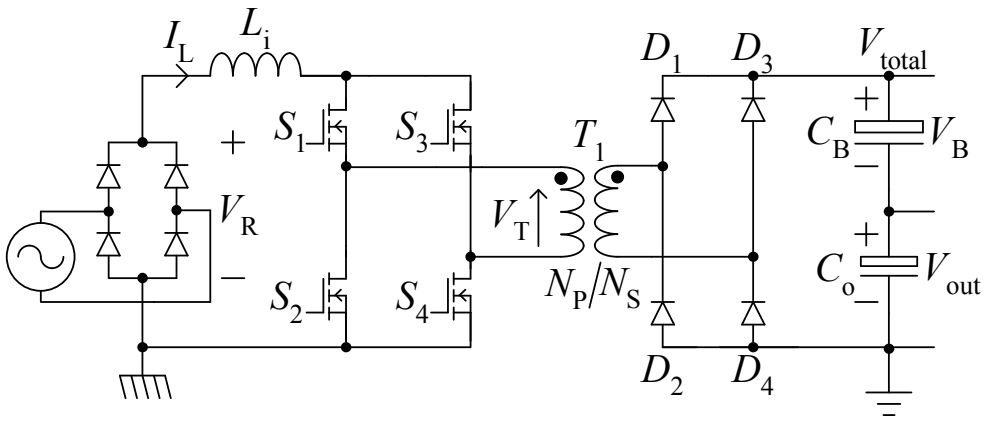


Figure 4.7: Simplified circuit of the current-fed full-bridge converter.

According to (4.18), the relation between the minimum capacitance and k at different values of output voltage are shown in Fig. 4.6. The minimum capacitance requirement is also in proportion to k and $V_{\rm out}$, since $V_{\rm B}$ is restricted by these two factors. In the results of Fig. 4.6, $v_{\rm r}$ is defined by twice of $V_{\rm B}$ to get the minimum capacitance, however, in practice, the ripple voltage should keep as small as possible to provide a stable input voltage source for the voltage regulator operation. In general, the capacitance of the noncascading switching regulator requires a larger value than that of the classical switching regulator because the allowable voltage ripple and the static voltage of $C_{\rm B}$ are limited by $V_{\rm out}$ and k. The relationship between the output voltage overshoot at negative step load and the values of the output capacitor ,$C_{\rm o}$, in this noncascading switching regulator have already been derived in Section 3.2.2.

4.2 Circuit Overview

Pre-regulator Stage

In this study, the current-fed full-bridge converter [94], [109], [110], [111] as the pre-regulator is employed. The input current of this converter can be fully controlled for achieving PFC. The pre-regulator of this noncascading switching regulator can be a simple boost converter. However, the current-fed full-bridge converter provides additional advantages over the boost converter such as the size and cost of the input boost inductor can be reduced due to its frequency-doubling effect. Also, the transformer provides galvanic isolation and steps down the output voltage. However, the leakage inductance of the transformer generates high voltage spikes on the power switches, when the switches are turned off. A simple method to suppress the voltage spikes is to use a passive or active snubber circuit at the expense of some power loss.

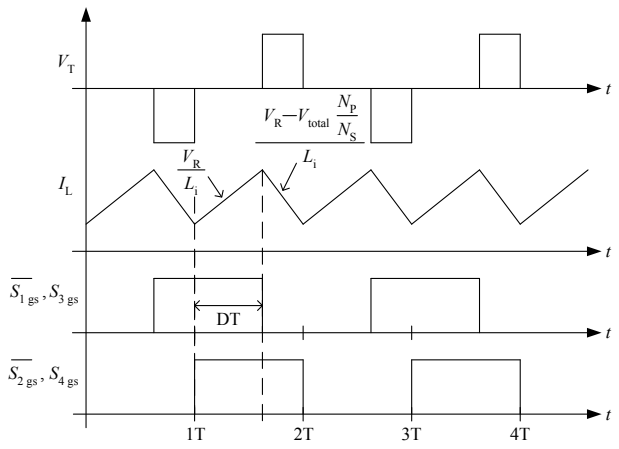


Figure 4.8: Gate timing diagram with corresponding waveforms.

The simplified circuit of the current-fed full-bridge converter is shown in Fig. 4.7. The set of waveforms that relate the ideal gate timing with the corresponding inductor current and transformer voltage is shown in Fig. 4.8. It is easy to see that the operation of this converter resembles that of a typical boost converter. The conversion ratio is controlled by the phase difference between S_1 and S_2. It can be easily derived by applying the principle of volt-second balance to the inductor current waveform, i.e.,

$$\frac{V_{\rm R}}{L_{\rm i}} DT = -\left(\frac{V_{\rm R} - V_{\rm total}\frac{N_{\rm p}}{N_{\rm s}}}{L_{\rm i}}\right)(1-D)T. \tag{4.19}$$

Thus, the conversion ratio is

$$\frac{V_{\rm total}}{V_{\rm R}} = \frac{N_{\rm s}}{N_{\rm p}}\frac{1}{(1-D)}, \tag{4.20}$$

which is similar to that of a typical boost converter conversion ratio with an additional factor of $\frac{N_{\rm s}}{N_{\rm p}}$ due to the transformer turns ratio.

Voltage Regulator Stage

Based on the description in Section 4.1, the voltage regulator processes only part of the total output power in the steady-state loading condition. However, during load transient, the buck-boost converter is required to deliver the total transient output power due to the slow voltage control loop of the pre-regulator. Fig. 4.9 shows the relation between the power, $P_{\rm direct}$, drawn from the ac mains through the pre-regulator to the load and the power, $P_{\rm vr}$, drawn from $C_{\rm B}$ through the voltage regulator to the load. The power handled by the voltage regulator is dependent of k and the load transient power level. While the semiconductor devices of the voltage regulator are selected to operate for the maximum output power, the thermal design of the voltage regulator would only need to process part of the total output power only, i.e., depending on the split factor. The buck-boost converter, the Ćuk converter

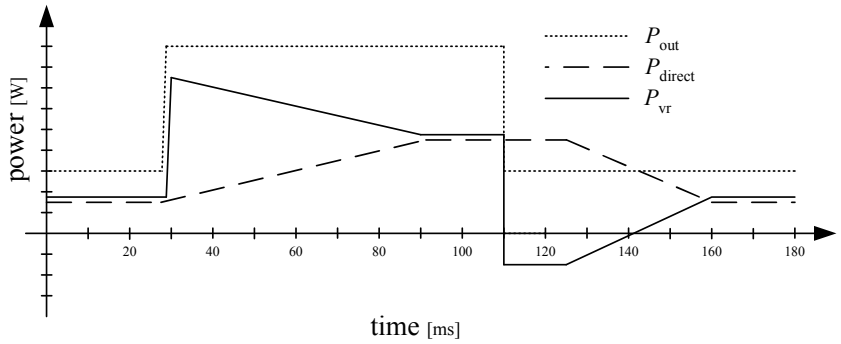


Figure 4.9: Simplified power sharing waveforms of the noncascading switching regulator at load transient period for $k \approx 0.5$.

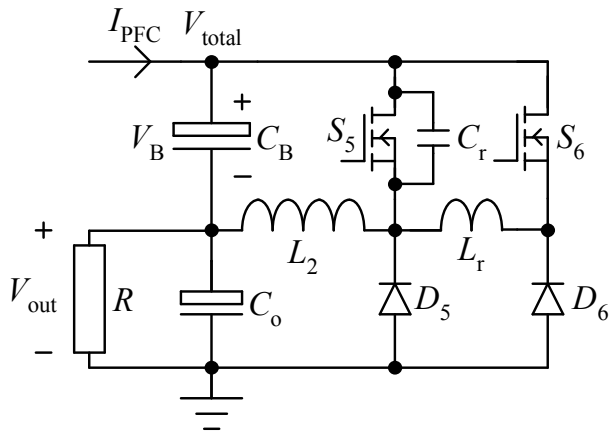


Figure 4.10: Simplified schematic circuit of the buck-boost converter using ZVT technique.

and any isolated converters [87], [95] are suitable candidates for the voltage regulator because, in this noncascading structure, the negative input terminal must be connected to the positive output terminal according to Fig. 4.3. The buck-boost converter is chosen here because of the simple control circuit design.

The buck-boost converter is required to handle power according to the split factor k and the transient load power level. During load transient, as mentioned earlier, the converter has to provide the total transient output power for a short duration. Our design employs the zero-voltage-transition (ZVT) technique [112], in which the voltage stress of switching devices are clamped at a level equal to $V_{\rm B}$+$V_{\rm out}$. The simplified voltage regulator is shown in Fig. 4.10. The basic components of the buck-boost converter include S_5, D_5, and L_2. ZVT is achieved by an auxiliary switch, S_6, a power diode, D_6, and a resonant network, which consists of $L_{\rm r}$ and $C_{\rm r}$. This technique can provide zero-voltage switching in S_5, and also reduce power loss in D_5 due to a longer reverse recovery time.

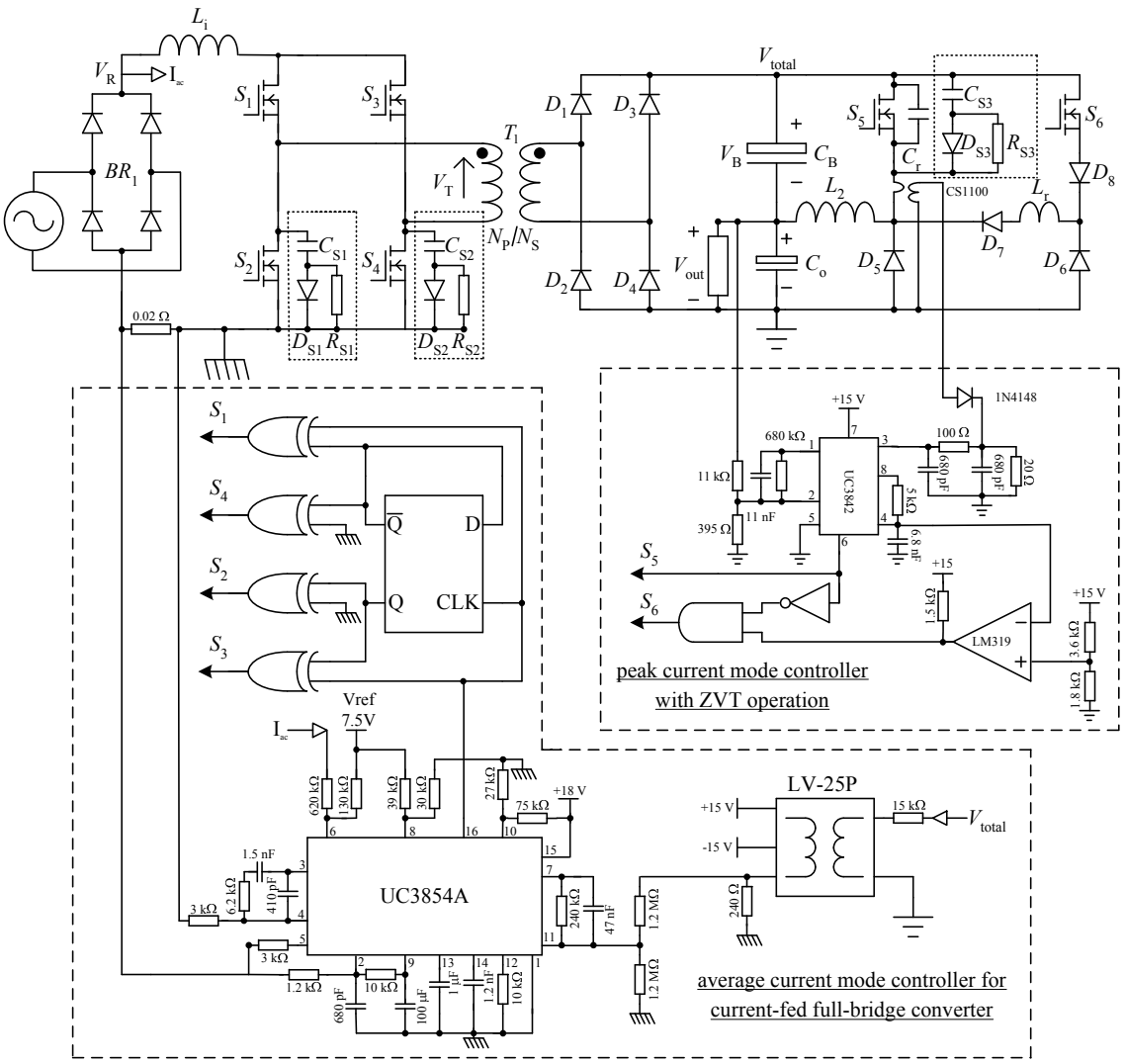


Figure 4.11: Schematic diagram of the experimental noncascading switching regulator prototype.

4.3 Noncsacading Switching Regulator Implementation

A laboratory prototype has been constructed to meet the following major design specifications: the input voltage is 220 V_{ac}, the ac mains frequency is 50 Hz, the voltage of the energy storage element is 83 V_{dc}, the output voltage is 72 V_{dc}, the output power is 1 kW. The switching frequency for both regulators is 50 kHz, but two converters are operated asynchronously. The lists of components of the pre-regulator and the voltage regulator are shown in Tables 4.1 and 4.2, respectively. Fig. 4.11 shows the implemented schematic diagram of the Category 2 noncascading switching regulator with the control circuitries. Two passive snubber circuits are added in the primary side to suppress the primary switches voltage stress. In the voltage regulator, for preventing the parasitic ringing between L_r and the output capacitor of S_6, two diodes, D_7 and D_8, are added. A turn-off snubber circuit is

Table 4.1: List of components for the current-fed full-bridge converter

Designator	Part No./Value
L_{i}	500 μH
BR_1	20ETF10 $\times$ 4
S_1, S_2, S_3, S_4	IXFK 27N80
D_1, D_2, D_3, D_4	DESP 30-03A
T_1 core	ETD 54 Philips 3C90
T_1 magnetizing inductance	18 mH
T_1 primary leakage inductance	9.4 μH
T_1 primary winding	58 T
T_1 secondary winding	21 T
C_{S1}, C_{S2}	4.7 nF, 2 kV
R_{S1}, R_{S2}	100 Ω, 25 W
D_{S1}, D_{S2}	MUR4100

Table 4.2: List of components for the buck-boost converter

Designator	Part No./Value
S_5	IXFK73N30
S_6	IXFK48N50
D_5	APT30D30
D_6, D_7, D_8	BYV29-400
L_2	100 μH
L_{r}	10 μH
C_{B}	2700 μF $\times$ 5, 160 V
C_{o}	680 μF $\times$ 4, 100 V
C_{r}	2.2 nF, 630 V
C_{S3}	2 nF, 1 kV
R_{S3}	360 Ω, 2 W
D_{S3}	MUR460

also attached in the secondary side power switch, S_5, to clamp the voltage stress.

Average current-mode control based on the PFC controller UC3854A is employed to control the current-fed full-bridge converter. There are four active switches, which have to be controlled for realizing the PFC function. Thus, additional logic circuits are required to generate the required gating pulses according to Fig. 4.8. For simplify the circuit design peak current-mode control based on

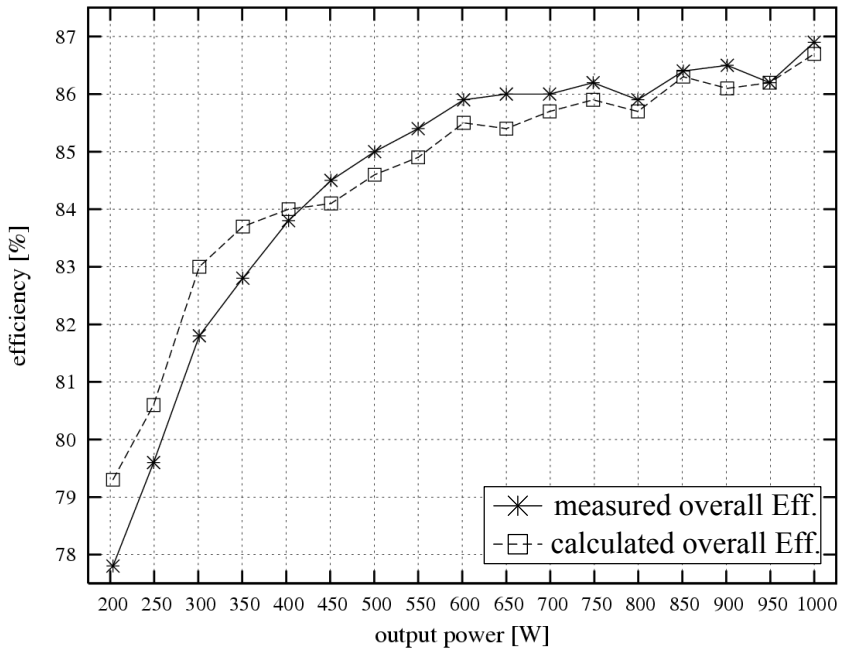


Figure 4.12: Efficiency versus output power from 200 W to 1 kW for $k = 0.46$, confirming the efficiency formulae (equations (4.1) and (4.6)). Calculated values are based on efficiency formula and measured values of $\eta_{\rm pfc}$ and $\eta_{\rm vr}$. Measured values are from direct measurement of the overall efficiency.

UC3842 is employed in the buck-boost converter for providing the voltage regulation. As mentioned before at Section 3.2.2, the split factor k must lower than 0.5 to maintain low-frequency ripple voltage free at the output load. Therefore, 0.46 is an appropriate value of k to achieve higher overall efficiency in this noncascading switching regulator. The gate signal of the auxiliary switch for ZVT operation is attained by a voltage comparator with a simple logic circuit.

4.4 Experimental Results

In this section, the advantages of the noncascading switching regulator are demonstrated experimentally. Fig. 4.12 shows two overall efficiency curves for confirming the efficiency formulae (4.1) and (4.6). The measured overall efficiency of the noncascading switching regulator under study is 87 % at 1 kW output power. The main power loss is in the snubber circuits of the pre-regulator. Fig. 4.13 shows the efficiency comparison of the noncascading connection with the classical two-stage cascade structure. The circuit is tested over a power range from 170 W to 1 kW, as the buck-boost converter is designed to provide 1 kW output power for a short duration. The efficiency gain of the noncascading structure is around 6 % at 1 kW, compared with the classical (cascade) connection.

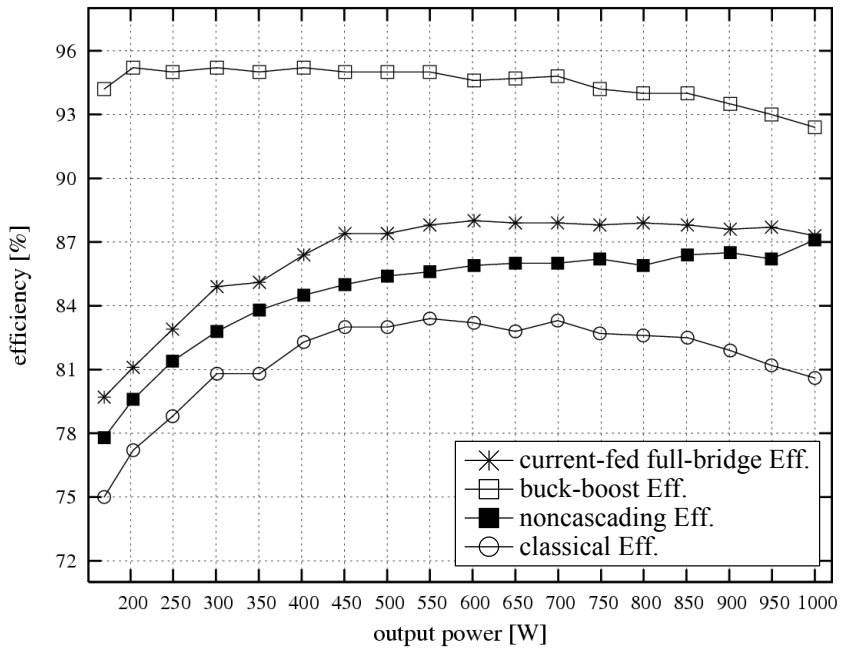


Figure 4.13: Efficiency comparison showing improved overall efficiency of the noncascading structure, for $k = 0.46$, over the classical connection. The top two curves are the efficiencies of the individual converters. The lower two curves are the overall efficiencies of the noncascading switching regulator and classical switching regulator.

Figs. 4.14 and 4.15 show the waveforms of the current-fed full-bridge converter at 1 kW output power. The upper trace is the current of inductor, $L_{\rm i}$. The middle trace and the lower trace are $V_{\rm ds}$ of S_2 and $V_{\rm ds}$ of S_4, respectively. The voltage spikes on the switches are around 750 V at full load condition. The spikes are generated by a resonant network, which is composed of the leakage inductance of the power transformer and the output capacitors of the switches.

Fig. 4.16 shows the voltage waveforms of the major devices of the voltage regulator. The upper trace and the middle trace show that S_5 is operated in zero voltage switching. The lower trace is the voltage waveform of the power diode, D_5. Fig. 4.17 shows the different output voltage waveforms of the pre-regulator and the voltage regulator. It depicts that the peak current-mode controller with appropriate split factor can effectively to keep the tight output load voltage.

Fig. 4.18 depicts the performance of the noncascading switching regulator for a step load change from 500 W to 1 kW. The undershoot and overshoot output voltage at transient load is a negligible level when the input power of the pre-regulator is close to the zero level. Fig. 4.19 shows the noncascading switching regulator waveforms under a negative load step from 1 kW to 500 W at the maximum input power condition. The output voltage is inevitably overshoot, because the output power of the pre-regulator is controlled by the sluggish voltage control loop as mentioned in Chapter 3.

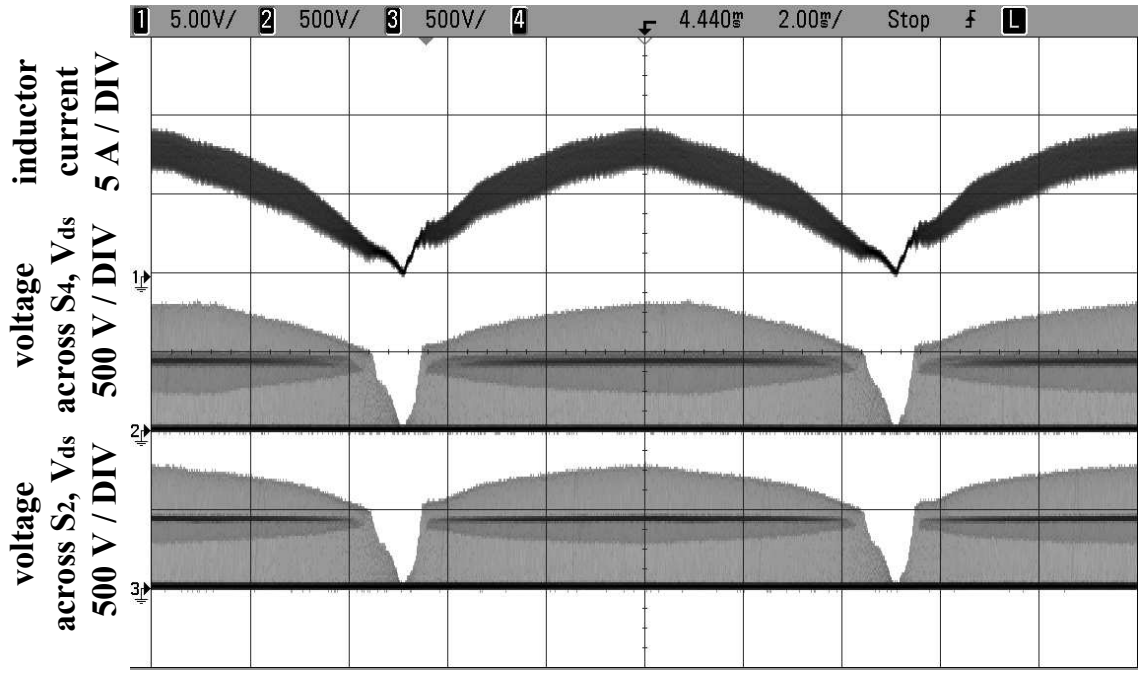


Figure 4.14: Measured waveforms of the pre-regulator: input inductor current (upper trace), $V_{\rm ds}$ of S_4 (middle trace), and $V_{\rm ds}$ of S_2 (lower trace). Time scale is 2 ms / DIV.

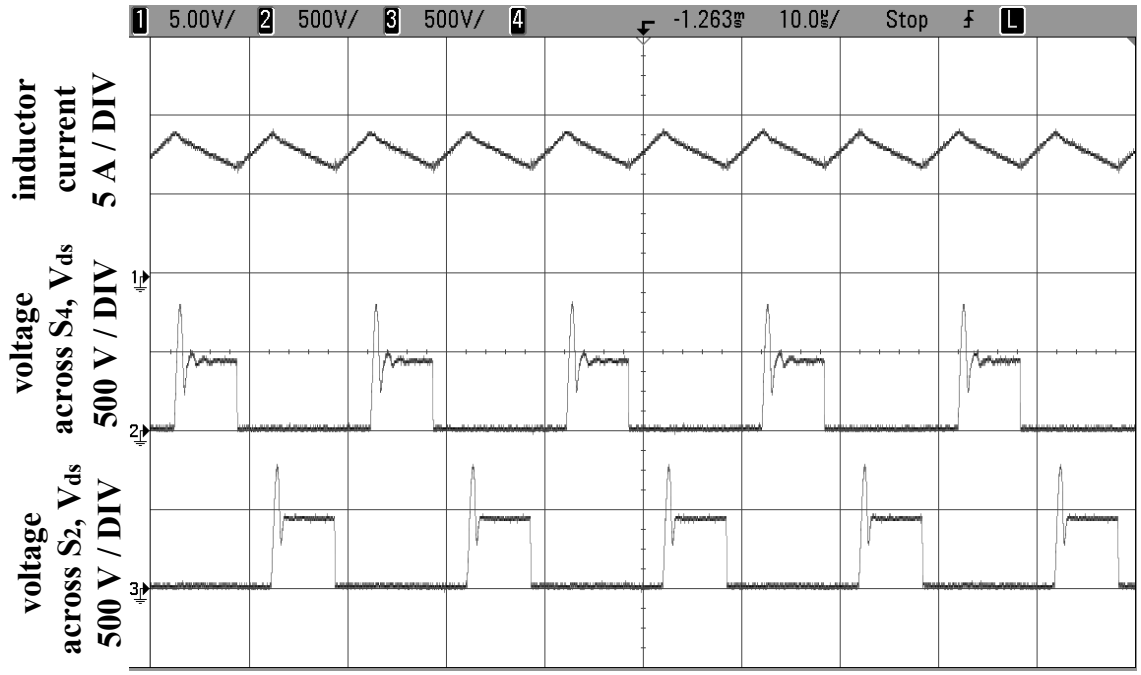


Figure 4.15: Measured waveforms of the pre-regulator: input inductor current (upper trace), $V_{\rm ds}$ of S_4 (middle trace), and $V_{\rm ds}$ of S_2 (lower trace). Time scale is 10 μs / DIV.

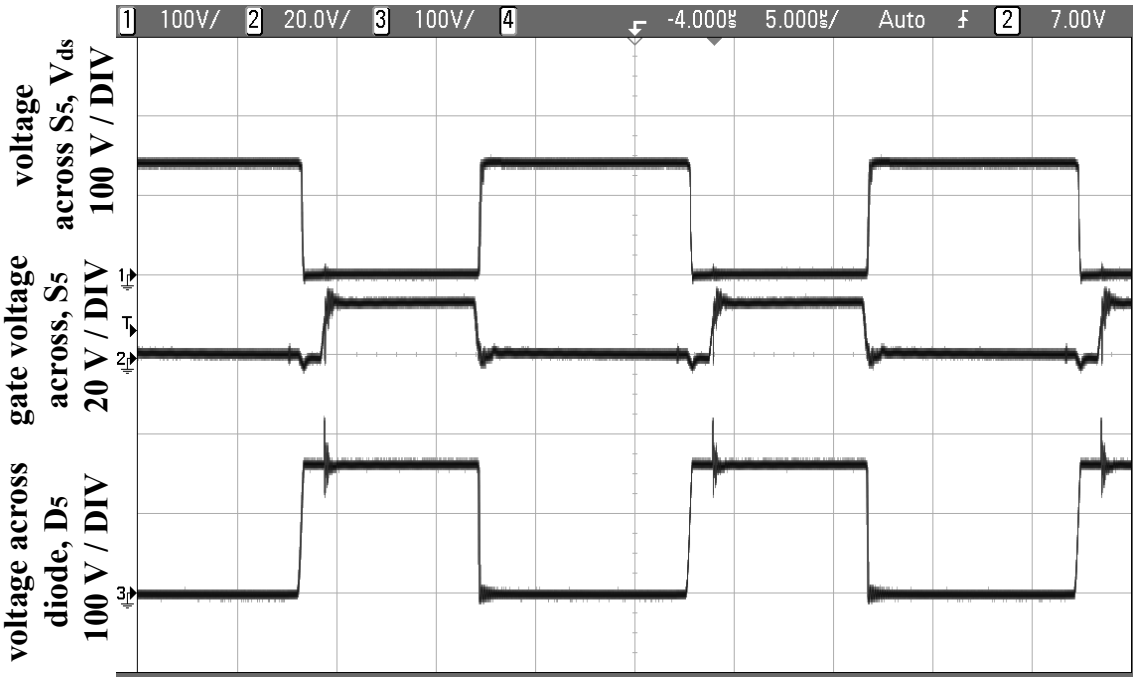


Figure 4.16: Measured waveforms of the voltage regulator with ZVT operation: $V_{\rm ds}$ of S_5 (upper trace), $V_{\rm gs}$ of S_5 (middle trace) and the voltage across D_5. Time scale is 5 μs / DIV.

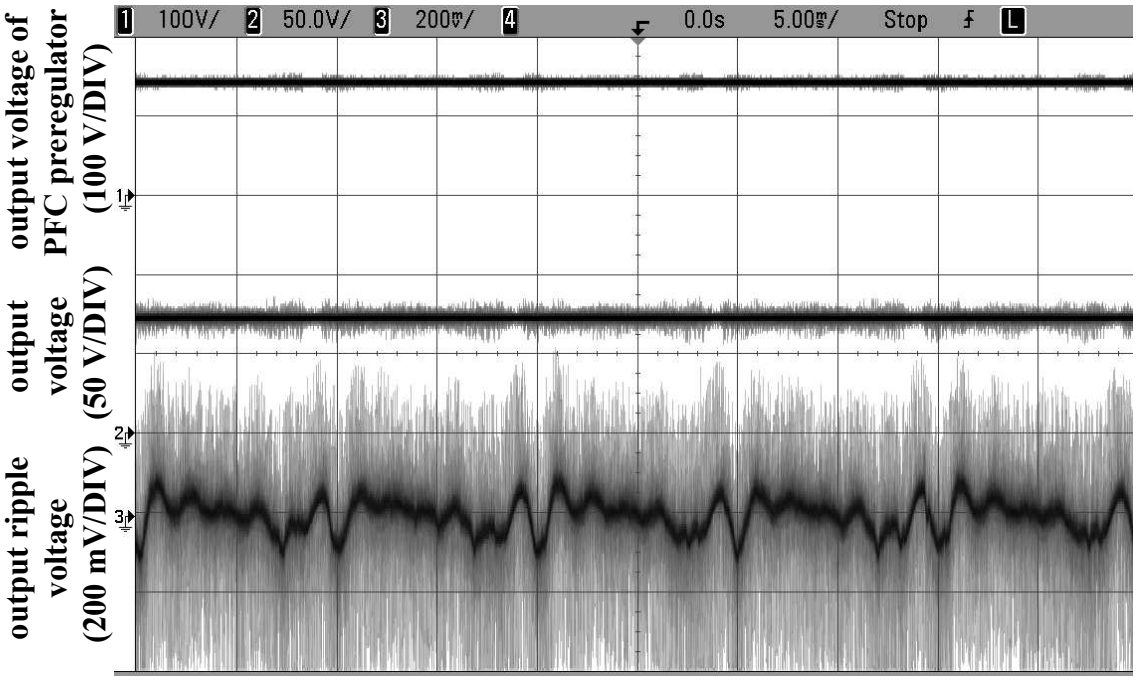


Figure 4.17: Measured waveforms of the output voltage of pre-regulator (upper trace), output voltage (middle trace) and ripple voltage (lower trace). Time scale is 5 ms / DIV.

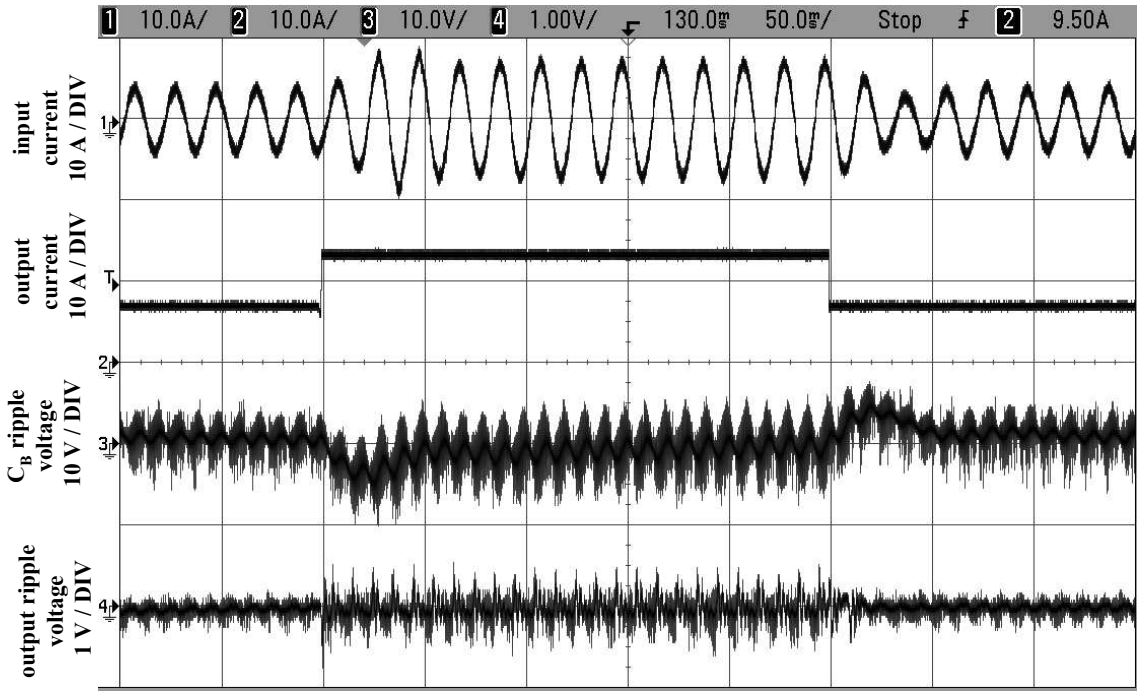


Figure 4.18: Measured waveforms of the filtered input current of pre-regulator (upper trace), load current (middle trace), C_{B} ripple voltage (third trace), and output ripple voltage (lower trace). Time scale is 50 ms / DIV.

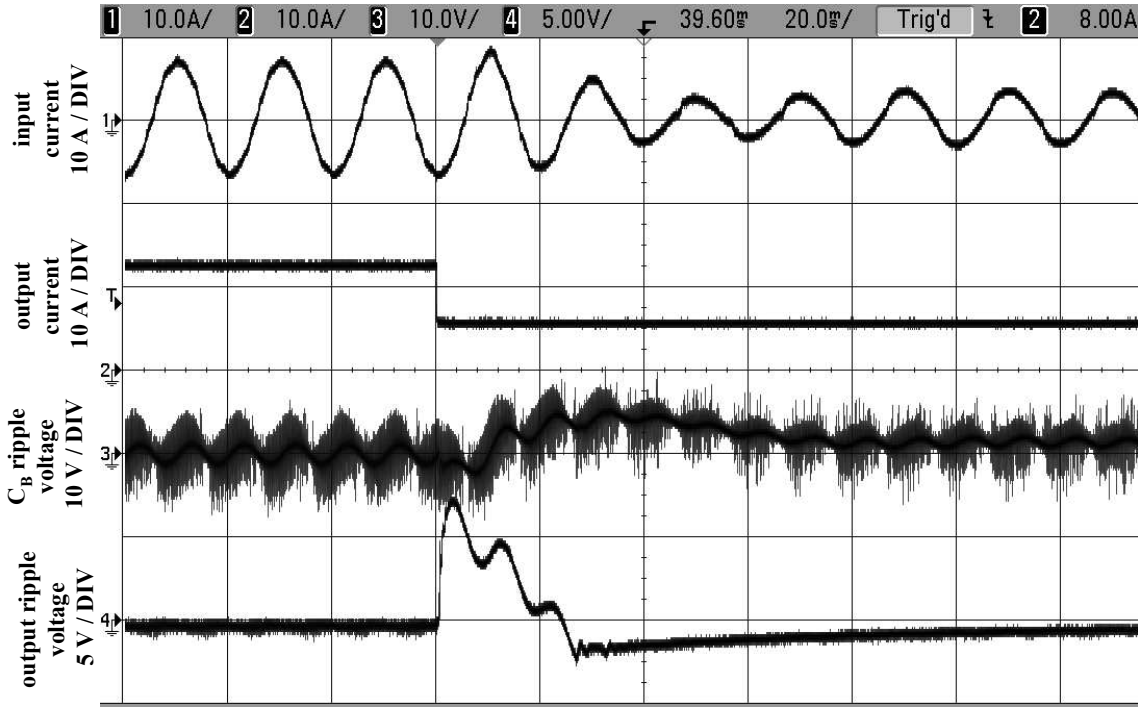


Figure 4.19: Measured waveforms under a negative load step at the maximum input power are shown. Filtered input current of pre-regulator (upper trace), load current (middle trace), C_{B} ripple voltage (third trace), and output ripple voltage (lower trace). Time scale is 20 ms / DIV.

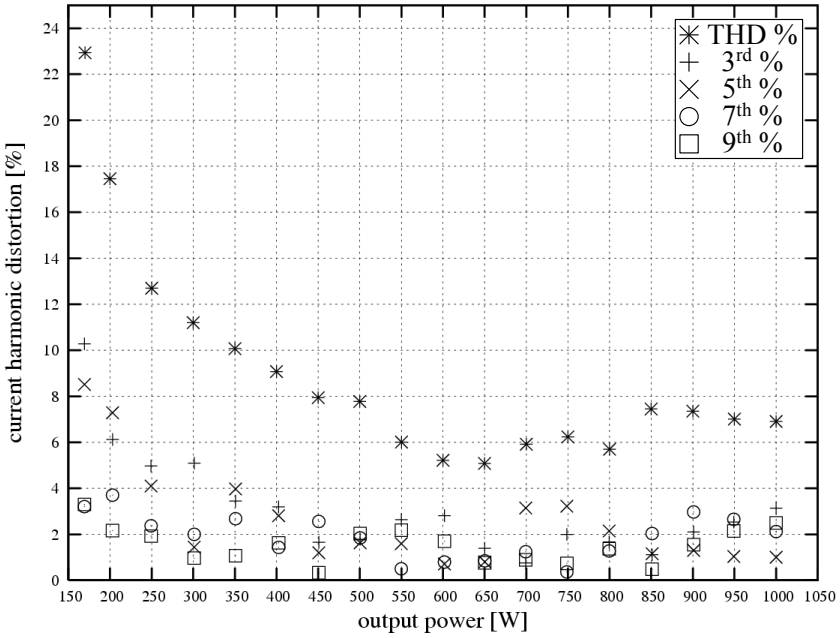


Figure 4.20: Measured harmonic distortion versus output power.

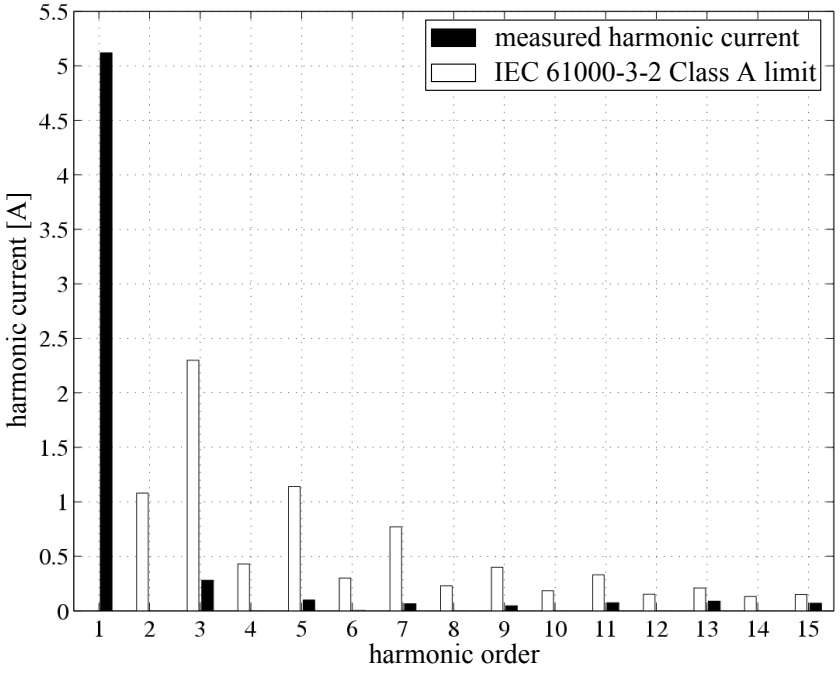


Figure 4.21: Harmonic current comparison between the measured input current at 1 kW output and IEC 61000-3-2 harmonic current limits for Class A equipment.

Finally, to verify the PFC function, the harmonic distortions are measured for different output power levels, as shown in Fig. 4.20. A comparison is made between the maximum permissible harmonic current limits for Class A equipment of IEC 61000-3-2:2005 [13] and the noncascading

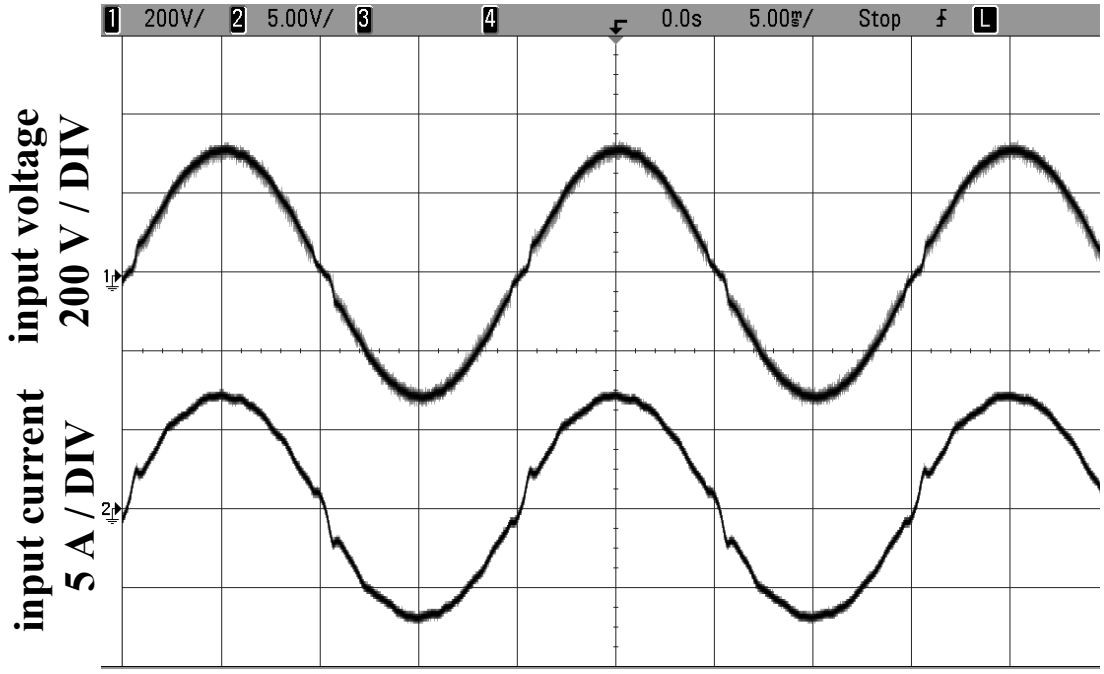


Figure 4.22: Measured waveforms of the input voltage (upper trace) and the filtered input current (lower trace) at full load condition. Time scale is 5 ms / DIV.

switching regulator input current at 1 kW power output, as shown in Fig. 4.21. The input voltage (upper trace) and the filtered input current (lower trace) at full load condition are shown in Fig. 4.22.

Obviously, the overall efficiency of the noncascading switching regulator is generally improved, but often at a price. The split factor k is one crucial parameter in the design. It affects the overall efficiency, the transient response and the size of the energy storage. Therefore, care should be taken to select k to optimize the performance of this noncascading switching regulator according to the specific application concerned.

4.5 Disadvantages and Possible Solutions

For providing galvanic isolation and steps down voltage functions, a current-fed full-bridge converter is employed, however one of the major disadvantages of this converter is high switching loss occurred in the power switches. Because, in this noncascading switching regulator, all the input power must be processed by the current-fed full-bridge converter, reducing the switching loss is necessary to further improve the overall efficiency of the noncascading switching regulator. ZVT used in current-fed full-bridge pulse-width-modulation converter for single-stage PFC is reported by Cho *et al.* [113]. Zero voltage switching in the current-fed full-bridge converter can only improve the converter efficiency,

but it cannot solve the high voltage spikes on the switches of the converter. A study to use zero current switching in a current-fed full-bridge pre-regulator is presented by Chen *et al.* [46]. The problem of the high voltage spikes is solved, but engineers should consider that the solution leads the converter operating in variable switching frequency.

In this particular noncascading switching regulator, the overshoot output voltage at the load transient period is uncontrolled by the voltage regulator and the value of the overshoot output voltage relies on the output capacitor. There are three possible approaches to reduce the value of the overshoot output voltage at the negative stepped load. The simplest approach is to increase the output capacitor of the voltage regulator. However this approach culminates in reducing the overshoot voltage only. The other approach is to employ a bidirectional voltage regulator in the noncascading switching regulator, therefore the excessive output power can be drained by the voltage regulator and transferred back to the energy storage. But this solution demands a high complexity in the voltage regulator and the control circuitry. The third approach of eliminating the overshoot output voltage at the negative load change condition which is the topic of discussion in the next chapter.

4.6 Summary

In this chapter, the practical design constraints of switching regulators that use a noncascading structure have been studied. The results complement the pervious chapter on the theoretical analysis in the achievable performances of different noncascading switching regulators, and provide further information about the design of such switching regulators. In particular, a 1 kW isolated switching regulator using the Category 2 noncascading connection of a current-fed full-bridge converter and a buck-boost converter has been thoroughly investigated. According to the idea of noncascading structure, the overall efficiency of the Category 2 noncascading switching regulator can be improved because part of the output power of the pre-regulator is transferred directly from the input to the regulated output and achieves unity PF. The chapter presents some design criteria for this Category 2 noncascading switching regulator, which include the relationships between the split factor, the load transient response and the energy storage requirement. The overall efficiency can be improved by increasing the split factor, but the load transient response time and the energy storage requirement will be deteriorated. Furthermore, to maintain the output voltage of the noncascading switching regulator without low frequency ripple voltage, substantial energy storage is required. Some practical problems related to the implementation of the current-fed full-bridge converter and the buck-boost converter are discussed. A 1 kW experimental prototype has been built with zero-voltage-switching incorporated in the voltage regulator stage. The measured results are presented to validate the analytical predictions.

Chapter 5

Improvement of Load Transient Response of Pre-regulators

As discussed in Section 2.2.2, a common method to achieve PFC is to use a CCM boost converter with average current-mode control [47] for medium to high-power applications. Alternatively, a DCM flyback converter with voltage mode control [52] is also commonly used for low power applications. In any pre-regulator, including CCM pre-regulator and DCM pre-regulator, the output voltage inevitably contains the second-harmonic (100 Hz or 120 Hz) ripple voltage. This can be easily explained by Tellegen's theorem [114], which concludes that the sum of powers of all branches of the pre-regulator is zero. A power flow diagram of the pre-regulator is depicted in Fig. 5.1. The power balance of the pre-regulator can be expressed as

$$\begin{aligned} v_{\rm in} i_{\rm in} \sin^2 \omega t &= \frac{P_{\rm in}(1-\cos 2\omega t)}{2} \\ &= \frac{V_{\rm out}^2}{R_{\rm load}} \end{aligned} \tag{5.1}$$

where $P_{\rm in}$, $V_{\rm out}$, and $R_{\rm load}$ are the peak input power, the output voltage, and the load, respectively, of the pre-regulator, and ω is the angular frequency of the input voltage. Since the output power is composed of a dc component and an ac component at twice of the ac mains frequency, the second-harmonic ripple voltage appears at the output capacitor. This ripple voltage cannot be compensated by the voltage control loop without causing the input current distortion. Therefore, the bandwidth of the pre-regulator voltage control loop is placed around one-fifth [104] of the ac mains frequency, the main drawback is that the pre-regulator provides sluggish load transient response, and the output capacitor will require to store substantial energy to support the transient load. A study is conducted by Lamar *et al.* [115] about limitations of flyback pre-regulator as one-converter switching regulator for providing fast voltage regulation. The finding is that directly increasing the voltage error amplifier bandwidth of the pre-regulator controller causes difficulty in complying with IEC 61000-3-2 standards [13].

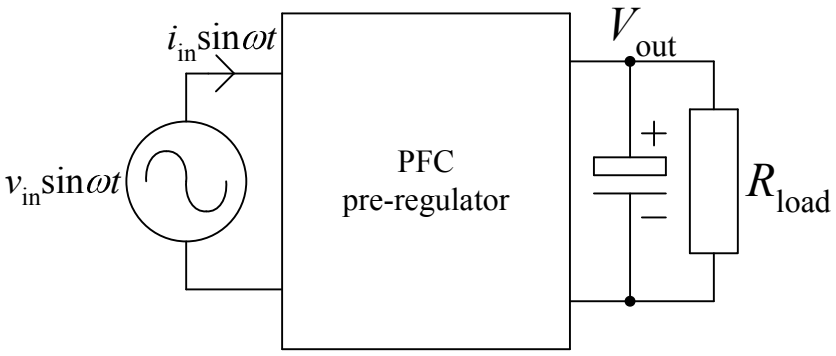


Figure 5.1: Pre-regulator power flow diagram.

Therefore Lamar *et al.* provides a set of relationships between the volume of the output capacitor, the output voltage ripple, and the output voltage dynamic response in different bandwidth designs.

This chapter presents an analog implementation to improve the load transient response of pre-regulators. By means of a notch filter inserted between the output-voltage sensing network of the pre-regulator and the voltage control loop of the pre-regulator control circuitry, the bandwidth of the voltage control loop is greatly expanded without introducing extra input current harmonics into the pre-regulators. This approach uses operational amplifiers with R-C networks to realize the notch filter, therefore it can be implemented into the existing pre-regulators with minor modification. The notch filter can be applied in both CCM pre-regulators and DCM pre-regulators. Furthermore the size of the output capacitor of the pre-regulators can be reduced due to the expanded bandwidth of the voltage control loop.

5.1 Improvement in Load Transient Response

To respond quickly to load disturbances without distorting the input current during steady-state operation, several techniques have been proposed in the literature [116] and [117]. Some proposed solutions aim to eliminate the ripple voltage from the output voltage feedback signal by a ripple compensation techniques [118], [119], [120]. The bandwidth of the voltage control loop can be greatly expanded, however, the technique is accomplished by a complicated controller to synchronize the phase of the ripple voltage and to detect the ripple voltage level. Sliding mode control [121] and boundary control [122] were proposed which allow faster load transient response, but these methods require the pre-regulator to operate with variable switching frequency. The use of an extra voltage control loop for decreasing the output impedance of the pre-regulator was reported [123]. The method improves the load transient response without the need for a wide bandwidth voltage control loop, but the load transient response improvement is less effective as compared to the aforementioned meth-

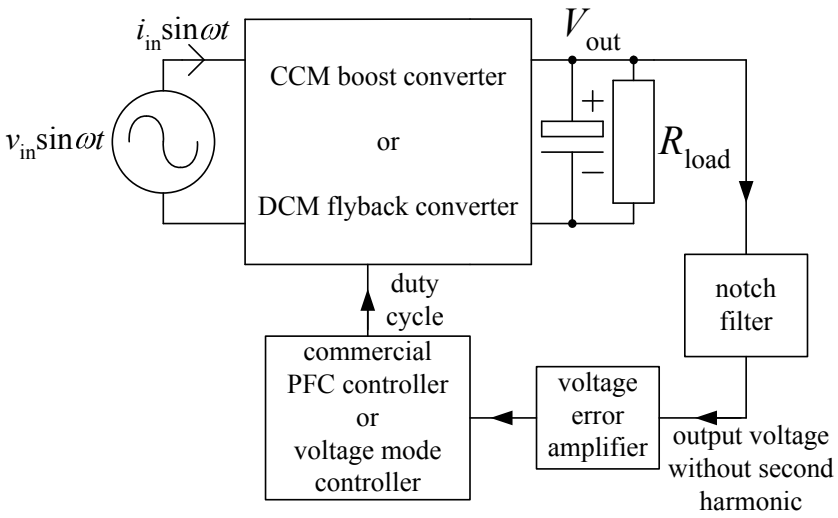


Figure 5.2: Simplified connection diagram of the pre-regulator with the notch filter.

ods. A load-current-injection technique for boost pre-regulator with average current-mode control to ameliorate the output voltage response is proposed in [124]. The load current becomes one of feedback signal, which bypasses the sluggish voltage control loop, to generate the reference current of the average current-mode controller. The notch filter method has also been widely discussed in [125] and [126]. Unfortunately, the filters proposed in these works were implemented by a micro-controller [125] and a digital signal processor [126]. The major drawback is that the existing pre-regulator requires a complete redesign in their control circuitry to enjoy the advantages of the notch filter.

5.2 Notch Filter

Fig. 5.2 depicts the simplified connection diagram of the pre-regulator with an analog notch filter. The notch frequency of the filter is fixed as twice the ac mains frequency in order to attenuate the second-harmonic ripple voltage of the voltage error amplifier input. As a result, the bandwidth of the voltage control loop can be expanded to accelerate the load transient response. On the other hand, the filter reveals that the expanded voltage control loop cannot improve the load transient response at twice the input voltage frequency.

The general transfer function of the notch filter [127] is represented by

$$H_N(s) = \frac{s^2 + \omega_o^2}{s^2 + s\frac{\omega_o}{Q} + \omega_o^2}, \tag{5.2}$$

where ω_o is the angular notch frequency and Q controls the filter bandwidth of the notch frequency. An analog notch filter based upon a modified twin tee network is depicted in Fig. 5.3. The operational amplifiers, OP1 and OP2, are connected as voltage followers to reduce the loading effect. From

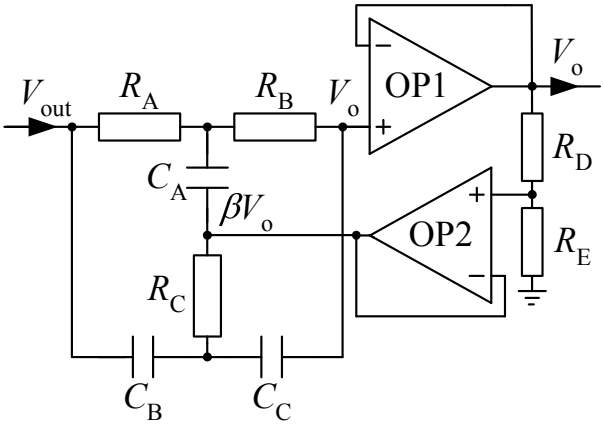


Figure 5.3: Adjustable Q notch filter implemented by analog circuit.

Fig. 5.3, assuming that

$$\begin{aligned} R &= R_{\rm A} = R_{\rm B} = 2R_{\rm C}, \\ C &= \frac{C_{\rm A}}{2} = C_{\rm B} = C_{\rm C}, \\ \beta &= \frac{R_{\rm E}}{R_{\rm D} + R_{\rm E}}, \end{aligned}$$

the transfer function of the twin tee network can be derived as

$$\frac{V_{\rm o}}{V_{\rm out}} = \frac{s^2 + (\frac{1}{RC})^2}{s^2 + s\frac{1}{RC}(1-\beta)4 + (\frac{1}{RC})^2}, \tag{5.3}$$

where $V_{\rm out}$ is the output voltage of the pre-regulator and $V_{\rm o}$ is the filtered voltage to the voltage error amplifier. We compare (5.3) with the general notch filter transfer function (5.2). Equating like terms give

$$\omega_{\rm o} = \frac{1}{RC} \tag{5.4}$$

and

$$Q = \frac{R_{\rm D} + R_{\rm E}}{4R_{\rm D}}. \tag{5.5}$$

The notch frequency can be evaluated as

$$f_{\rm o} = \frac{1}{2\pi RC} \tag{5.6}$$

and then the filter bandwidth is expressed as

$$BW = \frac{f_{\rm o}}{Q}. \tag{5.7}$$

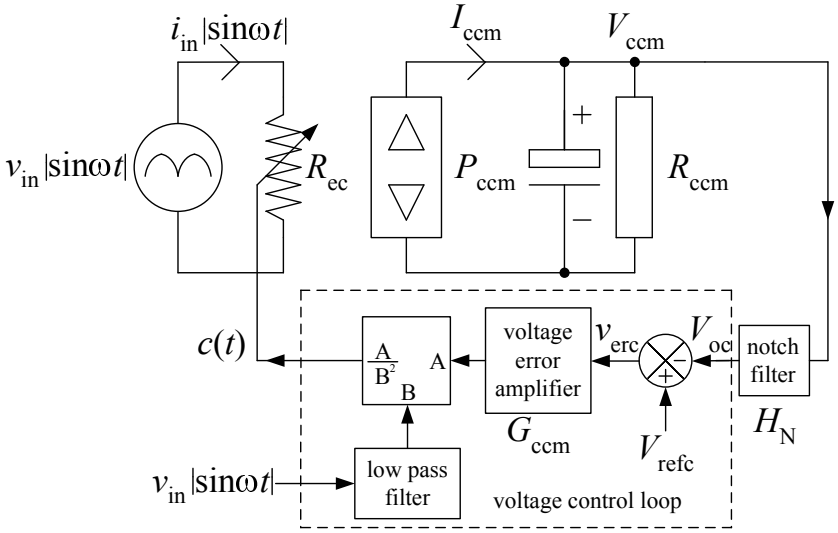


Figure 5.4: Large signal model with the loss-free resistor representing the CCM boost pre-regulator under average current-mode control.

5.3 Pre-regulator Modeling and Analysis

An average current-mode controller consists of two interconnected control loops [47], which are the inner current control loop and the outer voltage control loop. In this discussion, our consideration aims of the voltage control loop and assumes that the input current loop provides the "ideally shaped" sinusoidal current.

Based on our assumption, Fig. 5.4 depicts a large-signal model [38] for the CCM boost pre-regulator. The input port characteristic of the pre-regulator is simulated by the loss-free resistor, $R_{\rm ec}$, to maintain the sinusoidal current. This resistor is made by a wide-bandwidth current control loop. The value of $R_{\rm ec}$ can be found by

$$\frac{v_{\rm in}|\sin\omega t|}{i_{\rm in}|\sin\omega t|} = R_{\rm ec}c(t) \tag{5.8}$$

where $v_{\rm in}|\sin\omega t|$ and $i_{\rm in}|\sin\omega t|$ are the rectified input voltage and input current, respectively, and $c(t)$ is a signal to control the resistance $R_{\rm ec}$ depending on the voltage error amplifier output and the root mean square value of the input voltage. The function of the voltage control loop is to keep the output voltage, $V_{\rm ccm}$, regulated by changing $R_{\rm ec}$. The output power source, $P_{\rm ccm}$, can be written as

$$P_{\rm ccm} = \frac{(v_{\rm in}|\sin\omega t|)^2}{R_{\rm ec}c(t)}. \tag{5.9}$$

Thus, the output current, $I_{\rm ccm}$, is given by

$$I_{\rm ccm} = \frac{(v_{\rm in}|\sin\omega t|)^2}{V_{\rm ccm}R_{\rm ec}c(t)}, \tag{5.10}$$

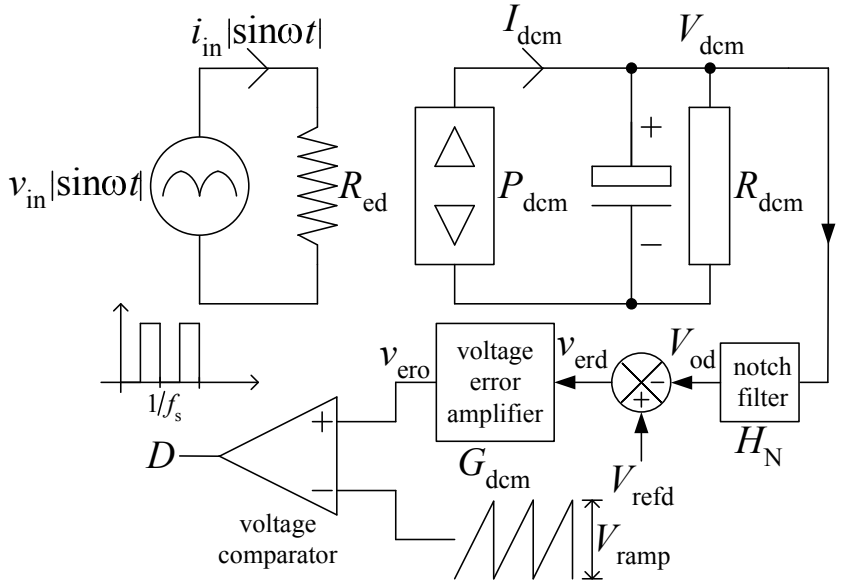


Figure 5.5: Large signal model of DCM flyback pre-regulator under voltage-mode control.

where $V_{\rm ccm}$ is the dc value of the output voltage. Also, $c(t)$ of the CCM boost pre-regulator can be expressed as

$$c(t) = \frac{G_{\rm ccm} v_{\rm erc}}{v_{\rm in,rms}^2}, \tag{5.11}$$

where $v_{\rm erc}$, $v_{\rm in,rms}$, and $G_{\rm ccm}$ are the error voltage, the root mean square value of the input voltage, and the gain of voltage error amplifier, respectively.

A large-signal model that represents a DCM flyback pre-regulator under voltage-mode control by using a loss-free resistor is shown in Fig. 5.5 [52]. The input port of the DCM flyback pre-regulator behaves inherently as a pure resistor. The equivalent resistance of the input port is given by

$$R_{\rm ed} = \frac{2Lf_{\rm s}}{D^2}, \tag{5.12}$$

where L, $f_{\rm s}$, and D are the inductance of the input inductor, the switching frequency, and the duty cycle, respectively, of the pre-regulator. Therefore, the resistance can be controlled by varying of the duty cycle. The output power source can be evaluated by

$$P_{\rm dcm} = \frac{(v_{\rm in}|\sin\omega t|)^2}{R_{\rm ed}}, \tag{5.13}$$

and the output current is given by

$$I_{\rm dcm} = \frac{(v_{\rm in}|\sin\omega t|)^2}{2Lf_{\rm s}V_{\rm dcm}} D^2, \tag{5.14}$$

where $v_{\rm in}|\sin\omega t|$ and $V_{\rm dcm}$ are the rectified input voltage and the dc value of the output voltage, respectively. The duty cycle of the DCM flyback pre-regulator can be expressed as

$$D = v_{\rm erd} \frac{G_{\rm dcm}}{V_{\rm ramp}}, \tag{5.15}$$

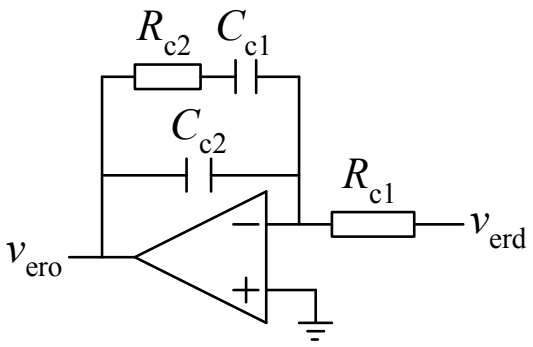


Figure 5.6: Simple compensation network is employed for the expanded voltage control loop.

where $v_{\rm erd}$, $G_{\rm dcm}$, and $V_{\rm ramp}$ are the error voltage, the gain of the voltage error amplifier, and the peak-to-peak voltage of the ramp signal, respectively, of the DCM flyback pre-regulator.

A small signal model applicable for frequencies below the line frequency and useful for designing the standard voltage control loop can be found in [128], [129]. However this model is invalid for frequencies above the ac mains frequency. The bandwidth of the expanded voltage control loop is higher than the ac mains frequency. So the traditional compensator design technique based on the small signal model is inappropriate to the expanded voltage control loop. Our approach of designing the expanded voltage control loop is based on computer simulations and experimental measurements. A simple PI control is employed for the expanded voltage control loop, as shown in Fig. 5.6. The transfer function of the expanded voltage control loop is given by

$$\frac{v_{\rm ero}}{v_{\rm erd}} = \frac{sR_{\rm c2}C_{\rm c1}+1}{s^2R_{\rm c1}R_{\rm c2}C_{\rm c1}C_{\rm c2}+sR_{\rm c1}(C_{\rm c1}+C_{\rm c2})}. \tag{5.16}$$

The improved load transient response is proven by experimental verification as documented in next Section.

5.4 Experimental Results

In this section, a DCM flyback pre-regulator is used as an example to demonstrate the advantage of the expanded voltage control loop with the analog notch filter. The major specifications of the pre-regulator are follows: the input voltage is 110 $\rm V_{rms}$, the ac mains frequency is 60 Hz, the maximum output power is 100 W, the output voltage is 48 V, and the switching frequency is 100 kHz. The simplified schematic of the experimental prototype is shown in Fig. 5.7. Two voltage-model control circuitries are built. One circuitry uses a quad-operational-amplifier IC, LM324, to construct the voltage error amplifier with the notch filter. The notch frequency is designed at 120 Hz and the Q factor of the filter is 10. Fig. 5.8 shows the magnitude and the phase characteristics of the expanded voltage control loop with the notch filter. In this control loop, the zero is placed around 54.4 Hz and

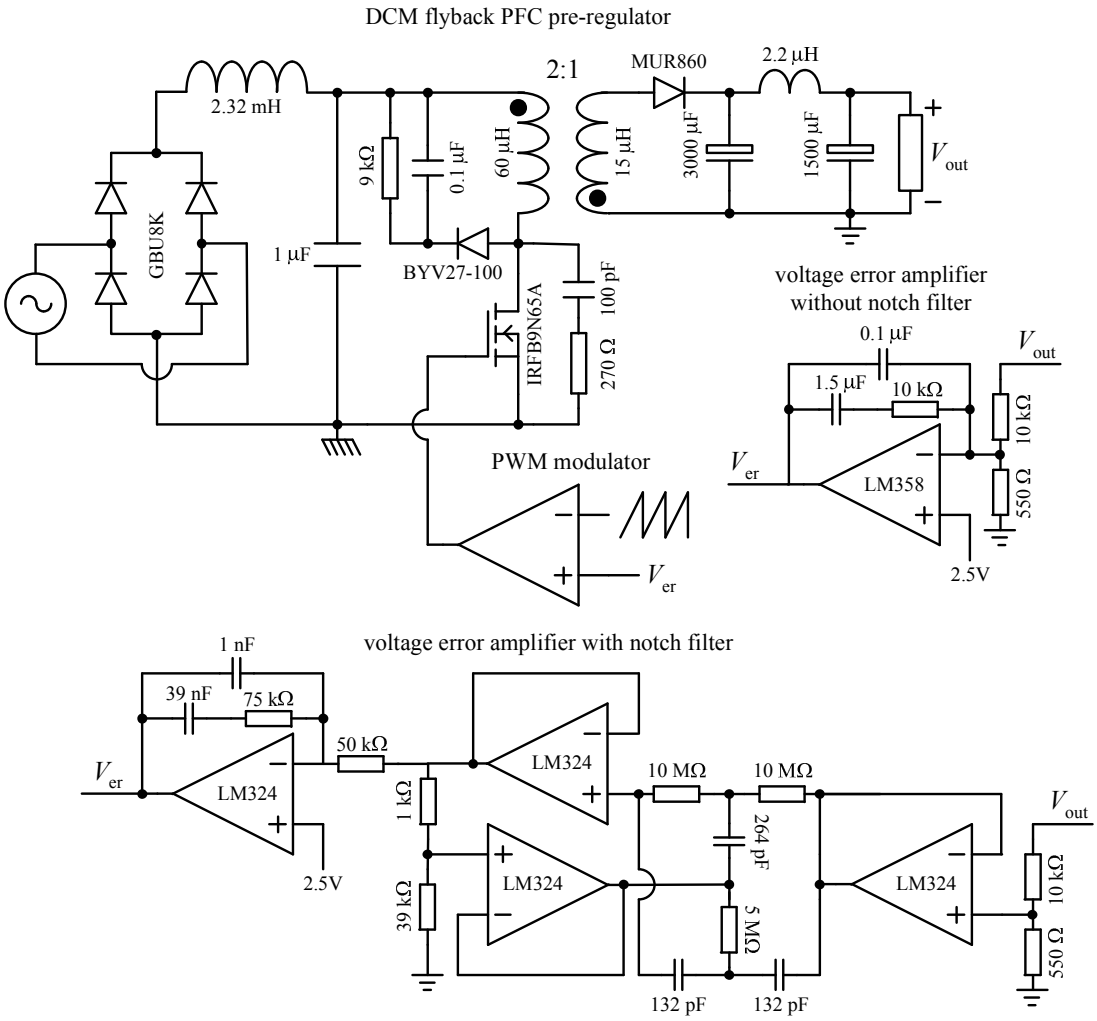


Figure 5.7: Simplified schematic of the experimental prototype.

the pole is placed around 2.12 kHz. Another circuitry uses a dual-operational-amplifier IC, LM358, to construct the voltage error amplifier without the notch filter. As aforementioned, the wide bandwidth of the voltage control loop causes the input current harmonic distortion, for providing a comparison, the PF and tuned the compensation networks of these two voltage error amplifiers to provide similar PF at different power levels at steady state output power condition have been measured, as shown in Table 5.1. Therefore, there is no significant difference of the performance of the two control circuitries from the ac mains viewpoint. Fig. 5.9 exhibits a comparison of the output voltage regulation of the DCM flyback pre-regulator between using the expanded bandwidth voltage control loop with the notch filter and using the standard voltage control loop without the notch filter. The load regulation of the pre-regulator with the expanded bandwidth voltage control loop is 0.38%, but the load regulation of the pre-regulator with the standard voltage control loop is 0.81%

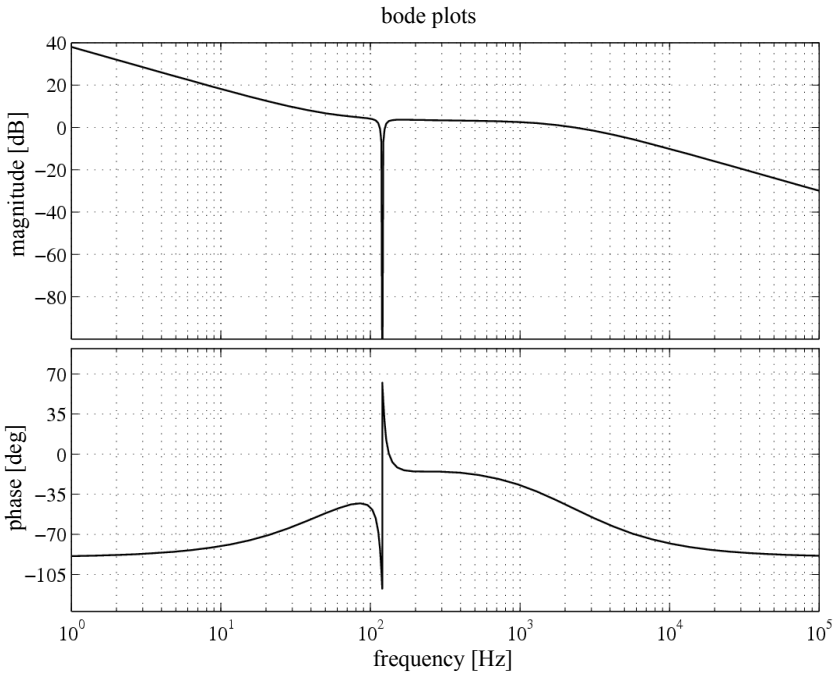


Figure 5.8: Magnitude and phase characteristics of the expanded voltage control loop with the notch filter.

Figs. 5.10 (a) and (b) show the measured waveforms for a load stepping from 50 W to 100 W of the DCM pre-regulator with the expanded bandwidth voltage control loop with the notch filter and the standard voltage control loop without the notch filter, respectively. In Fig. 5.10 (a), the overshot output voltage is 5.5 $V_{\rm pp}$ and the settling time is around 100 ms. Figs. 5.11 (a) and (b) show the

Table 5.1: Measured PF and input current total harmonic distortion (THD%)

$P_{\rm out}$ (W)	P.F. with N.F. (THD%)	P.F. without N.F. (THD%)
10	0.824 (10.50%)	0.814 (10.61%)
20	0.938 (6.57%)	0.931 (6.33%)
30	0.968 (5.14%)	0.963 (4.58%)
40	0.981 (3.97%)	0.977 (4.22%)
50	0.987 (3.47%)	0.984 (3.96%)
60	0.989 (3.17%)	0.988 (4.07%)
70	0.991 (3.52%)	0.990 (4.27%)
80	0.992 (4.48%)	0.991 (4.28%)
90	0.992 (4.82%)	0.992 (4.72%)
100	0.993 (4.77%)	0.993 (4.57%)

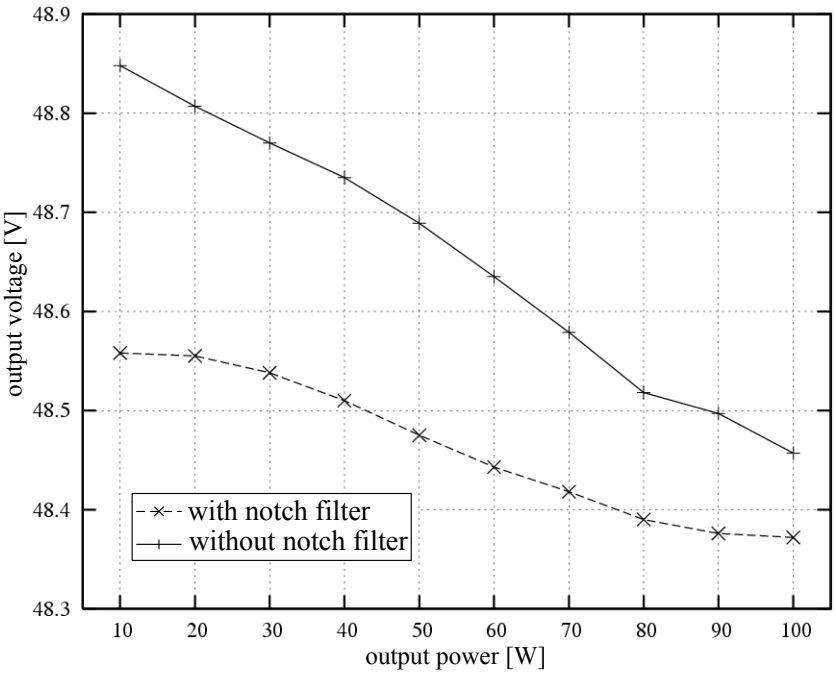
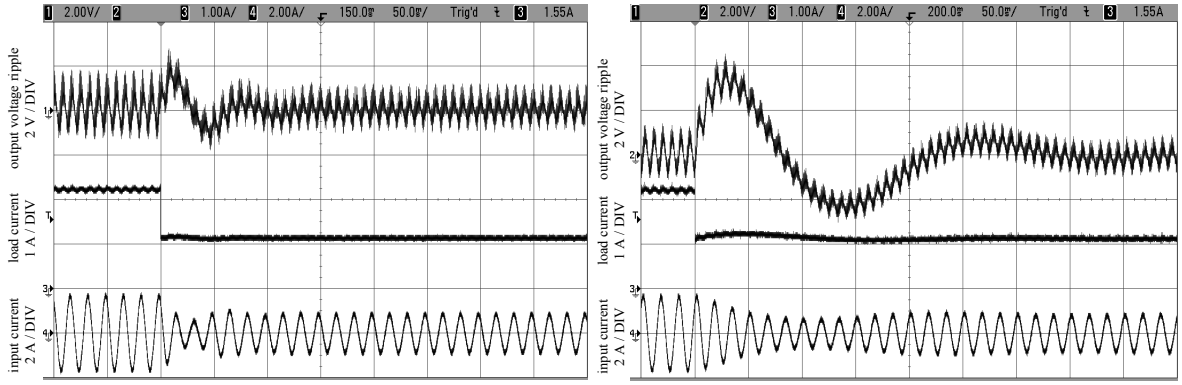


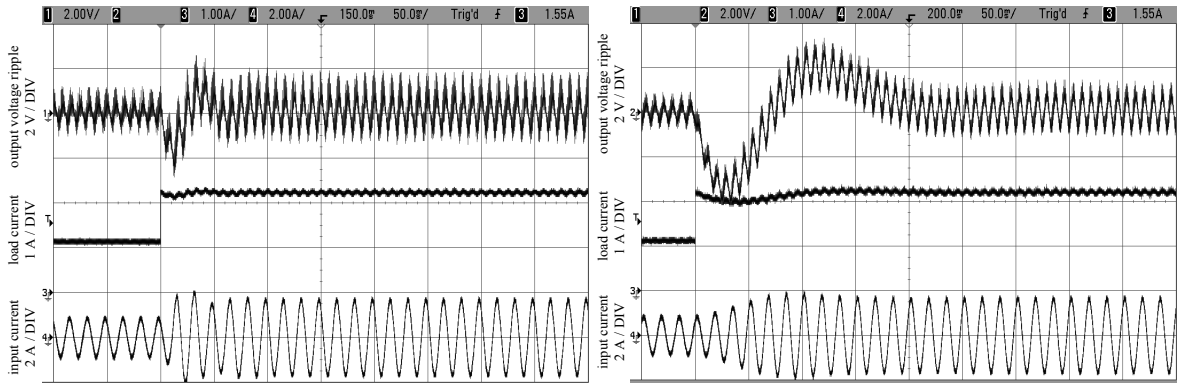
Figure 5.9: Measured load regulation comparison between the expanded bandwidth voltage control loop with the notch filter and the standard voltage control loop without the notch filter.



(a) (b)

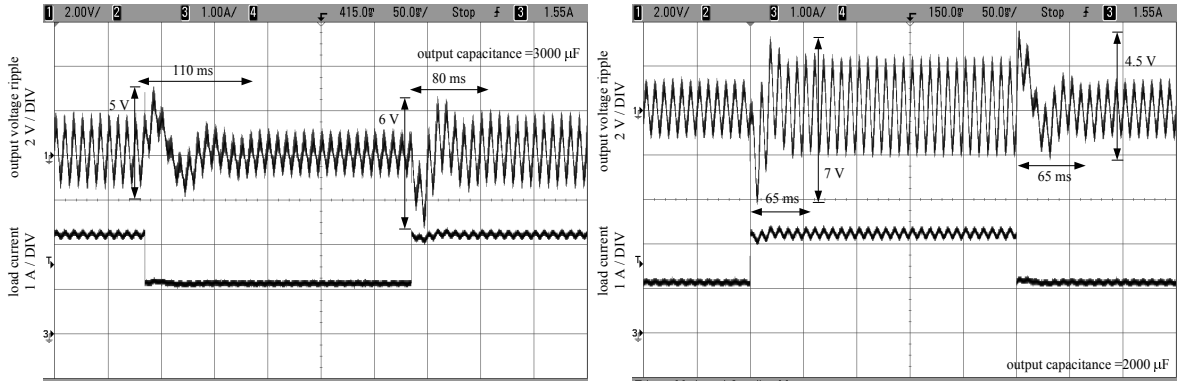
Figure 5.10: Transient response for the change of load from 100 W to 50 W: (a) the expanded bandwidth voltage control loop with the notch filter and (b) the standard voltage control loop without the notch filter. Upper trace is the output voltage ripple, middle trace is the load current, and lower trace is the input current. The output capacitance is 4500 μF. Time scale is 50 ms / DIV.

measured waveforms at the load change from 100 W to 50 W of the DCM pre-regulator with the expanded bandwidth voltage control loop and the standard voltage loop, respectively. In Fig. 5.11 (a), the dropped output voltage is 5 $V_{\rm pp}$ and the settling time is around 130 ms. The load transient

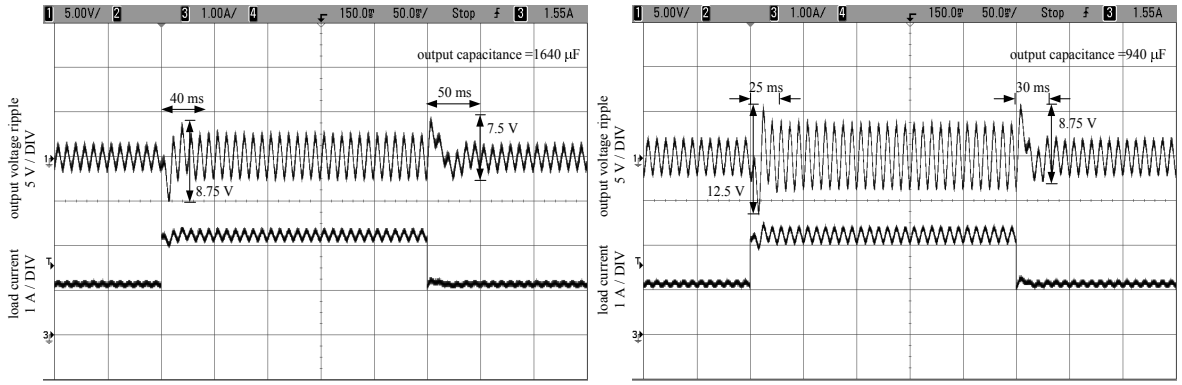


(a) (b)

Figure 5.11: Transient response for the change of load from 50 W to 100 W: (a) the expanded bandwidth voltage control loop with the notch filter and (b) the standard voltage control loop without the notch filter. Upper trace is the output voltage ripple, middle trace is the load current, and lower trace is the input current. The output capacitor value is 4500 μF. Time scale is 50 ms / DIV.

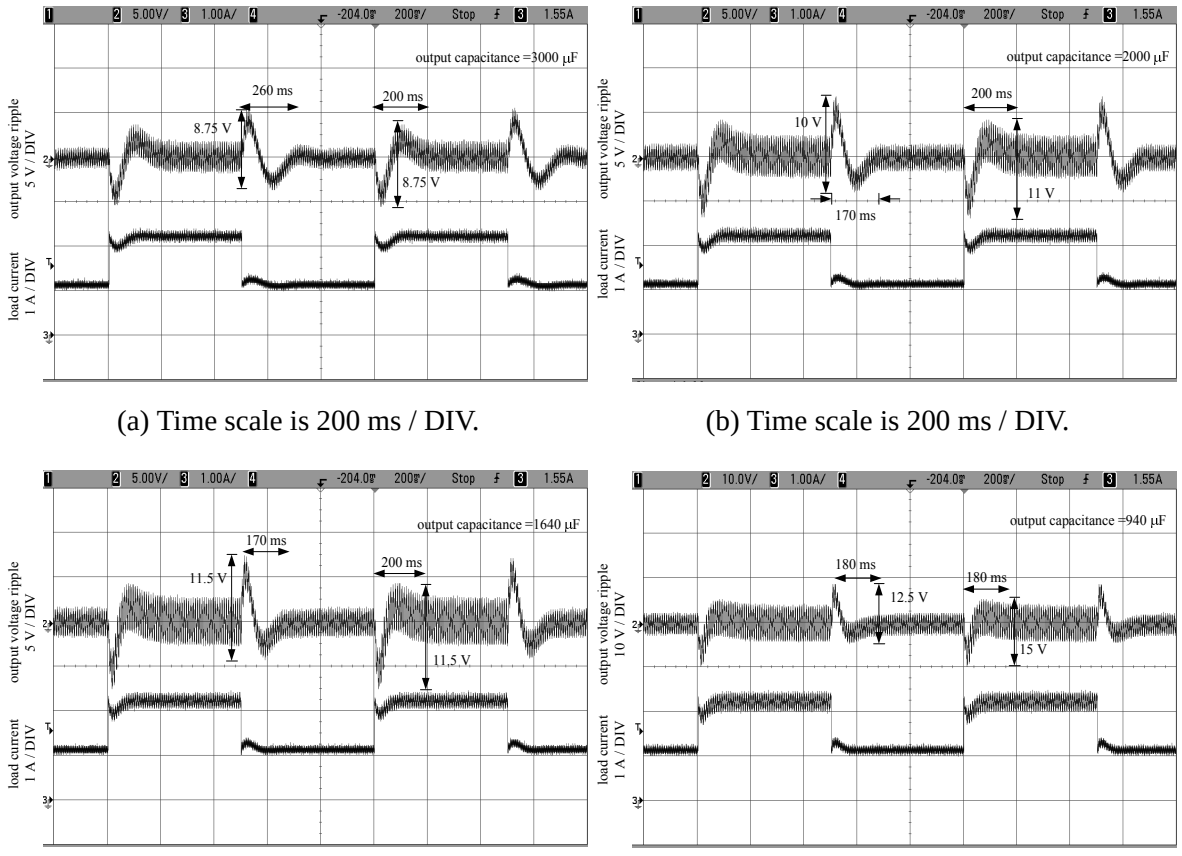


(a) Time scale is 50 ms / DIV. (b) Time scale is 50 ms / DIV.



(c) Time scale is 50 ms / DIV. (d) Time scale is 50 ms / DIV.

Figure 5.12: Experimental waveforms of the DCM pre-regulator with notch filter for step load change from 50 W to 100 W with different output capacitor values.



(a) Time scale is 200 ms / DIV.

(b) Time scale is 200 ms / DIV.

(c) Time scale is 200 ms / DIV.

(d) Time scale is 200 ms / DIV.

Figure 5.13: Experimental waveforms of the DCM pre-regulator without notch filter for step load change from 50 W to 100 W with different output capacitor values.

response of the control loop with the notch filter is much better than the standard control loop.

Figs. 5.12 and 5.13 show the comparative experimental response of the output voltage to a load step from 50 W to 100 W with both the expanded bandwidth voltage control loop with the notch filter (Figs. 5.12 (a) to (d)) and the standard voltage control loop (Figs. 5.13 (a) to (d)) at different output capacitor values. The value of the output capacitor has negligible influence on the transient voltage drop of the DCM pre-regulator with the expanded voltage control loop. A tabulation of the data showing the properties of the DCM pre-regulator with the expanded voltage control loop and with the standard voltage control loop at different values of the output capacitor are given in Appendix B. The measured results show that the load transient response of the expanded voltage control loop is relatively faster than the standard one.

The traditional small signal model cannot elaborate on the accurate behavior of the DCM flyback pre-regulator after the ac mains frequency. Hence, the experimental measurement is a direct method to observe the behavior of the DCM flyback pre-regulator with the expanded voltage control loop.

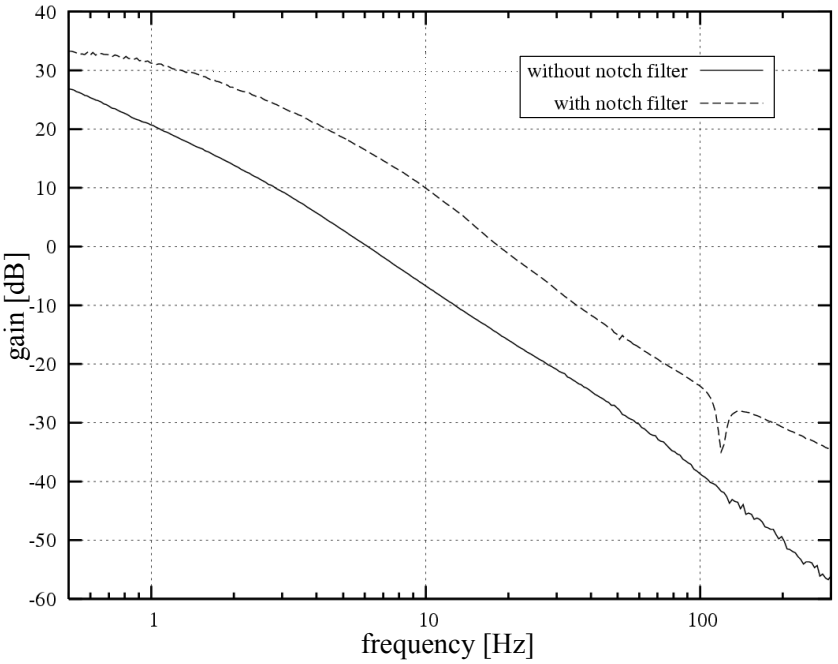


Figure 5.14: Comparison of the gain of the DCM flyback pre-regulator between using the expanded voltage control loop with the notch filter (dash line) and using the standard voltage control loop. The output capacitor value is 4500 μF.

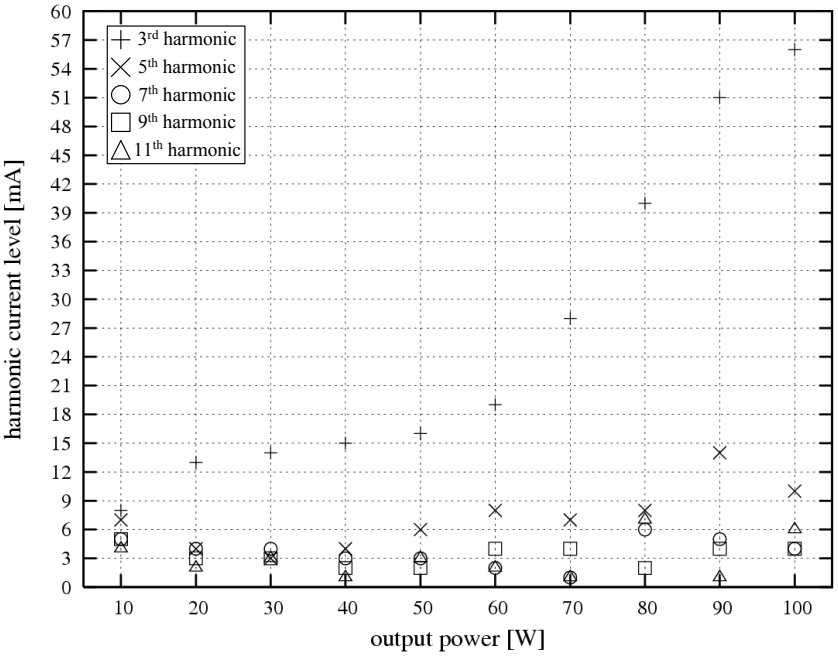


Figure 5.15: Measured harmonic current level of the DCM flyback pre-regulator with the expanded bandwidth voltage control loop with the notch filter. The output capacitor value is 4500 μF.

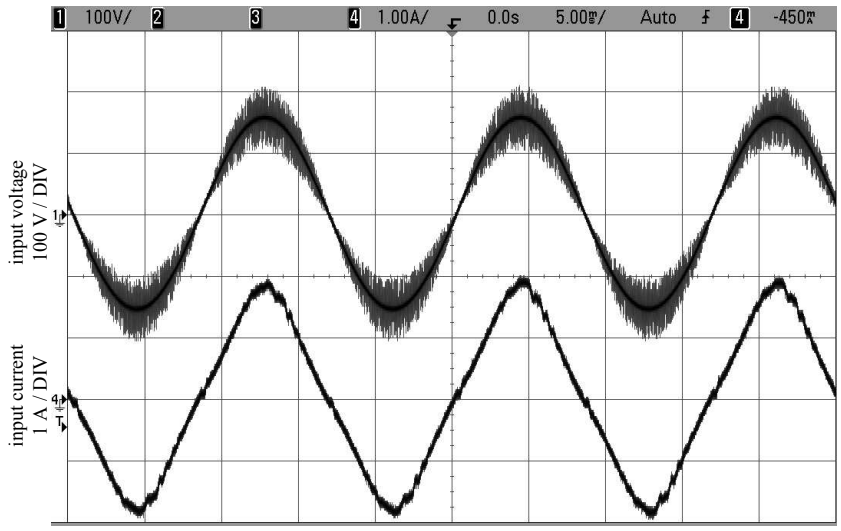


Figure 5.16: Measured waveforms of the input voltage (upper trace) and the filtered input current (lower trace) at 100 W output power of the DCM flyback pre-regulator with the expanded voltage control loop.

The bode plots of the loop gain function with notch filter and without notch filter are measured as shown in Fig. 5.14. The measurements have been carried out by means of a real time frequency response analyzer NF FAR5097 and represented with GNUPLOT software. The measured gain of the closed-loop DCM flyback pre-regulator with both the expanded voltage control loop and the standard voltage control loop is shown in Fig. 5.14. The measurement conditions are that the output power is 100 W and the input voltage is 155 $V_{\rm dc}$. According to the observation from Fig. 5.14, the gain bandwidth of the DCM flyback pre-regulator is much better with the expanded voltage control loop than with the standard one. Note that the expanded voltage control loop with the notch filter can attenuate the gain at 120 Hz (the second harmonic of the ac mains frequency).

Finally, in order to verify the PFC function of the DCM flyback pre-regulator with the expanded bandwidth voltage control loop, the current harmonic distortions are measured for different output power level, as shown in Fig. 5.15. The input voltage and the filtered input current at 100 W output power are shown in Fig. 5.16.

5.5 Summary

This chapter describes a simple analog circuit implementation to accelerate the load transient response of pre-regulators. The analog notch filter is inserted between the output voltage of the pre-regulator and the voltage error amplifier of the pre-regulator control circuitry. This implementation can be ap-

plied in existing pre-regulators with minor modification. The notch filter setup in terms of the circuit value is reported. Furthermore a set of measurements on the DCM flyback pre-regulator with different values of the output capacitor using the expanded voltage control loop has been performed. Based on the measurement, the input current harmonic is deteriorated when output capacitor is too small. However, quick response to load disturbances without distorting the input current during steady-state can be achieved. Experimental results show the benefits of this cost-effective solution in improving the load transient response of the pre-regulator.

Chapter 6

Performance Tradeoffs of Boost Pre-regulators

In the previous chapter, a method to accelerate the output load transient response of the pre-regulator without affecting the input current quality has been discussed. In this chapter, the investigation will go one step further to analyze a CCM boost pre-regulator under average current-mode control. The objective is to analyze the relationship between the reduced output ripple voltage and the dynamic characteristics of the output voltage of the CCM boost converter which is controlled by a standard average current-mode controller that maintains an imperfect sinusoidal input current, but complies with the IEC 61000-3-2 Class D limit. The output ripple of the CCM boost pre-regulator can be reduced if the input current is allowed to take an imperfect sinusoidal waveform. This in turn allows the output regulation of the CCM boost pre-regulator to be tightened while the input current waveform still satisfies the IEC 61000-3-2 harmonic current emission standard. Furthermore, the overall efficiency can be further improved for switching regulators that adopt a noncascading configuration when their CCM boost pre-regulators are drawing imperfect sinusoidal input current.

Boost-type pre-regulators have become the most widely used power converters to achieve PFC [25], [26], [47], [130]. To maintain a very low harmonic current distortion, the input current of the pre-regulator is controlled to be sinusoidal and in phase with the input voltage. As mentioned in Chapter 5, the output voltage of the pre-regulator inevitably contains second-harmonic (100 Hz or 120 Hz) ripple voltage [24], [27], and the dynamic response of the pre-regulator becomes sluggish due to the placement of a very low frequency pole in the output voltage control loop [52], [115]. However, most international standards of harmonic current emissions limits, such as IEC 61000-3-2 [13], do allow a small amount of input current harmonics, and it is therefore unnecessary to achieve perfect sinusoidal input current. It has been shown [131], [132], [133] that pre-regulators drawing imperfect sinusoidal input current can effectively reduce the second-harmonic output ripple voltage

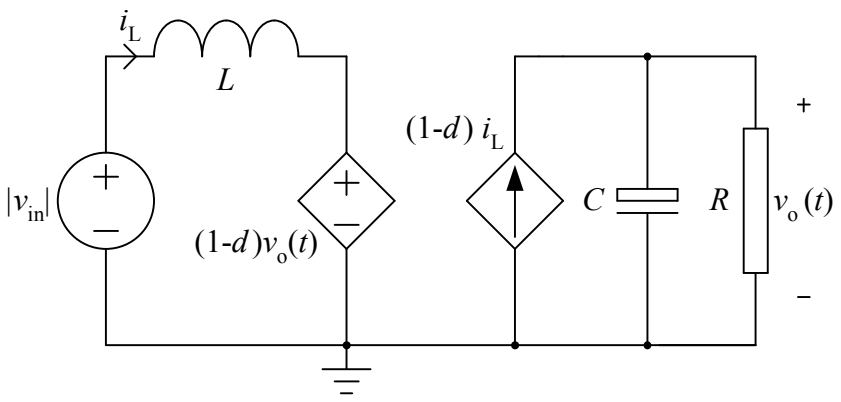


Figure 6.1: State-space model for CCM boost converter.

without increasing their output capacitor. This reduced output ripple voltage arrangement can lead to more stable operation of CCM boost pre-regulators [134] and provide possibility of expanding the gain of the output voltage control loop for enhancing the static output voltage regulation. In this chapter, a detailed study regarding the relationship between the reduced output ripple voltage and the dynamic characteristics of the CCM boost pre-regulator drawing imperfect sinusoidal input current is conducted to formulate a systematic design procedure such that the waveshape manipulation of the input current can be used to tradeoff dynamic response of the CCM boost pre-regulators. Furthermore, manipulating the waveshape of the input current can further enhance the power conversion efficiency in some specific designs of noncascading switching regulators [95], [135], [136].

6.1 Analysis of Boost Pre-regulator

The CCM boost converter is the most popular topology for pre-regulators [25]. Non-pulsating input current and low current stress in semi-conductor devices are the advantages of using the CCM boost converter as a pre-regulator. For brevity and without confusion, the *boost pre-regulator* is used to refer the CCM boost pre-regulator. Fig. 6.1 shows a standard state-space model for the CCM boost converter [137]. The state equations of the CCM boost converter are given by

$$\frac{dv_{\rm o}}{dt} = \frac{1}{C}\left[i_{\rm L}(1-d) - \frac{v_{\rm o}}{R}\right] \tag{6.1}$$

$$\frac{di_{\rm L}}{dt} = \frac{1}{L}\left[|v_{\rm in}| - v_{\rm o}(1-d)\right] \tag{6.2}$$

where d is the duty cycle, $v_{\rm o}$ is the output voltage, $i_{\rm L}$ is the inductor current, C is the output capacitance, and L is the inductance. Singular perturbation theory [138] provides a method to reduce the order of the state-space model by using time-scale separation. If the CCM boost converter is operated as a pre-regulator under average current-mode control, the dynamics of the inductor current is

controlled by the current control loop and is much faster than the dynamics of the output capacitor. Therefore, time-scale separation can be applied to simplify the design of the voltage control loop. Details of the time-scale separation as applied to the boost pre-regulator can be found in [119], [139]. The dynamics of the output voltage of the boost pre-regulator is described by (6.1) only, and the conversion ratio of the boost pre-regulator is given by

$$1 - d = \frac{|v_{\rm in}|}{v_{\rm o}}. \tag{6.3}$$

Substituting (6.3) into (6.1), the output voltage of the boost pre-regulator is calculated as

$$\frac{dv_{\rm o}}{dt} = \frac{|v_{\rm in}|i_{\rm L}}{v_{\rm o}C} - \frac{v_{\rm o}}{RC}. \tag{6.4}$$

This equation illuminates the dynamics of the inductor current on the output ripple voltage and facilitates study of the dynamics of the output voltage of the boost pre-regulator. The time-scale separation can also be applied to buck-boost PFC pre-regulator, and the dynamics of the output voltage is expressed as

$$\frac{dv_{\rm o}}{dt} = -\left(\frac{|v_{\rm in}|i_{\rm L}}{v_{\rm o}C} + \frac{v_{\rm o}}{RC}\right). \tag{6.5}$$

6.1.1 Derivation of Output Ripple Voltage of Boost Pre-regulator

The single-phase power conversion application is considered in here. The input voltage $v_{\rm in}$ and the input current $i_{\rm in}$ of the boost pre-regulator are taken as ideal sinusoids. Therefore, the inductor current is a rectified sinusoid, i.e.,

$$\begin{aligned} v_{\rm in} &= V\sin\omega t \\ i_{\rm in} &= I_1\sin\omega t \\ i_{\rm L} &= I_1|\sin\omega t| \end{aligned}$$

where V is the peak input voltage, I_1 is the peak value of the fundamental input current, and ω is the angular frequency of the ac mains. Therefore, (6.4) can be expressed as

$$2v_{\rm o}\frac{dv_{\rm o}}{dt} = \frac{VI_1}{C}(1-\cos 2\omega t) - \frac{2v_{\rm o}^2}{RC}. \tag{6.6}$$

Variable x is denoted the nonlinear term $v_{\rm o}^2$, and (6.6) is reformatted as

$$\frac{dx}{dt} + \frac{2x}{RC} = \frac{VI_1}{C}(1-\cos 2\omega t). \tag{6.7}$$

The general solution of $x(t)$ is

$$\begin{aligned} x(t) &= e^{\frac{-2t}{RC}}\Big[\int e^{\frac{2t}{RC}}\frac{VI_1}{C}(1-\cos 2\omega t)dt\Big] \\ &= \frac{VI_1}{C}Ae^{\frac{-2t}{RC}} + \frac{VI_1R}{2}\Big(1 - \frac{\cos 2\omega t + \omega RC\sin 2\omega t}{1+(\omega RC)^2}\Big) \end{aligned}$$

where A is a constant depending on the initial condition. The general solution of $v_{\rm o}(t)$ is given by

$$v_{\rm o}(t) = \sqrt{\frac{VI_1}{C}Ae^{\frac{-2t}{RC}} + \frac{VI_1R}{2}\Big(1 - \frac{\cos 2\omega t + \omega RC\sin 2\omega t}{1+(\omega RC)^2}\Big)}. \tag{6.8}$$

For $v_{\rm o}(0) = 0$, A is given by

$$A = -\frac{RC}{2}\Big(1 - \frac{1}{1+(\omega RC)^2}\Big). \tag{6.9}$$

The first term of (6.8) will vanish when $t \gg RC/2$, hence $v_{\rm o}(t)$ can be further simplified as

$$v_{\rm o}(t) \cong \sqrt{\frac{VI_1R}{2}\left(1 - \frac{\sin(2\omega t+\phi)}{\sqrt{1+(\omega RC)^2}}\right)} \tag{6.10}$$

where ϕ is equal to $\arctan\frac{1}{\omega RC}$ and represents the time delay generated by the output capacitor C and the loading resistor R.

As mentioned earlier, international standards for harmonic current emissions, such as IEC 61000-3-2 [13], allow a certain amount of harmonic current to be drawn to the input of the switching regulator. Possible tradeoff between the input current waveform and the size of pre-regulators has been studied in [131], [132], [133]. In this chapter, an analytical solution for the output voltage ripple of the boost pre-regulator drawing imperfect sinusoidal input current is provided to predict the relationship between the imperfect sinusoidal input current and the output ripple voltage level. Since odd harmonic current can effectively reduce the output ripple voltage [133], the imperfect sinusoidal current is represented in the following form:

$$i_{\rm L_{HD}} = \Big|I_1\Big(\sin\omega t + \sum_{\rm n=1}^{\infty}\beta_{\rm 2n+1}\sin(2{\rm n}+1)\omega t\Big)\Big| \tag{6.11}$$

where $\beta_{\rm 2n+1}$ is the peak amplitude ratio of the odd harmonic current to the fundamental current; and $2{\rm n}+1$ denotes the harmonic order. To simplify the calculation, only third, fifth and seventh harmonic current components of the output voltage ripple are considered. Combining (6.11) with (6.7), the output voltage of the boost pre-regulator drawing imperfect sinusoidal input current is gotten as

$$\begin{aligned}\frac{dx_{\rm HD}}{dt} + \frac{2x_{\rm HD}}{RC} \;=\; & \frac{VI_1}{C}(1 - \cos 2\omega t + \beta_3\cos 2\omega t \\ & -\beta_3\cos 4\omega t + \beta_5\cos 4\omega t \\ & -\beta_5\cos 6\omega t + \beta_7\cos 6\omega t \\ & -\beta_7\cos 8\omega t)\end{aligned} \tag{6.12}$$

$$
\begin{aligned}
x_{\mathrm{HD}}(t) &= e^{\frac{-2t}{RC}}\left[\int e^{\frac{2t}{RC}}\frac{VI_1}{C}\Big(1-(1-\beta_3)\cos 2\omega t\right. \\
&\quad -(\beta_3-\beta_5)\cos 4\omega t-(\beta_5-\beta_7)\cos 6\omega t \\
&\quad \left.-\beta_7\cos 8\omega t\Big)dt\right] \\
v_{\mathrm{o_{HD}}}(t) &= \left[\frac{VI_1R}{2}\Big(1-(1-\beta_3)\frac{\cos 2\omega t+\omega RC\sin 2\omega t}{1+(\omega RC)^2}\right. \\
&\quad -(\beta_3-\beta_5)\frac{\cos 4\omega t+\omega RC\sin 4\omega t}{1+(2\omega RC)^2} \\
&\quad -(\beta_5-\beta_7)\frac{\cos 6\omega t+\omega RC\sin 6\omega t}{1+(3\omega RC)^2} \\
&\quad \left.-\beta_7\frac{\cos 8\omega t+\omega RC\sin 8\omega t}{1+(4\omega RC)^2}\Big)\right. \\
&\quad \left.+\frac{VI_1}{C}A_{\mathrm{HD}}e^{\frac{-2t}{RC}}\right]^{\frac{1}{2}}
\end{aligned}
\tag{6.13}
$$

where $v_{\mathrm{o_{HD}}}(t)$ is the output voltage of the boost pre-regulator drawing imperfect sinusoidal input current and A_{HD} is a constant in the general solution of $v_{\mathrm{o_{HD}}}(t)$. For $v_{\mathrm{o_{HD}}}(0)=0$, A_{HD} is given by

$$
\begin{aligned}
A_{\mathrm{HD}} &= -\frac{RC}{2}\left(1-\frac{1-\beta_3}{1+(\omega RC)^2}-\frac{\beta_3-\beta_5}{1+(2\omega RC)^2}\right. \\
&\quad \left.-\frac{\beta_5-\beta_7}{1+(3\omega RC)^2}-\frac{\beta_7}{1+(4\omega RC)^2}\right).
\end{aligned}
\tag{6.14}
$$

The output voltage of the boost pre-regulator drawing imperfect sinusoidal input current in the steady state is

$$
\begin{aligned}
v_{\mathrm{o_{HD}}}(t) &\cong \left[\frac{VI_1R}{2}\Big(1-(1-\beta_3)\frac{\sin(2\omega t+\phi_1)}{\sqrt{1+(\omega RC)^2}}\right. \\
&\quad -(\beta_3-\beta_5)\frac{\sin(4\omega t+\phi_2)}{\sqrt{1+(2\omega RC)^2}} \\
&\quad -(\beta_5-\beta_7)\frac{\sin(6\omega t+\phi_3)}{\sqrt{1+(3\omega RC)^2}} \\
&\quad \left.-\beta_7\frac{\sin(8\omega t+\phi_4)}{\sqrt{1+(4\omega RC)^2}}\Big)\right]^{\frac{1}{2}}
\end{aligned}
\tag{6.15}
$$

where ϕ_1, ϕ_2, ϕ_3, and ϕ_4 are equal to $\arctan\frac{1}{\omega RC}$, $\arctan\frac{1}{2\omega RC}$, $\arctan\frac{1}{3\omega RC}$, and $\arctan\frac{1}{4\omega RC}$, respectively. A detailed comparison of the output voltage ripple of the boost pre-regulator drawing sinusoidal input current and that drawing imperfect sinusoidal input current will be shown in Section 6.2.

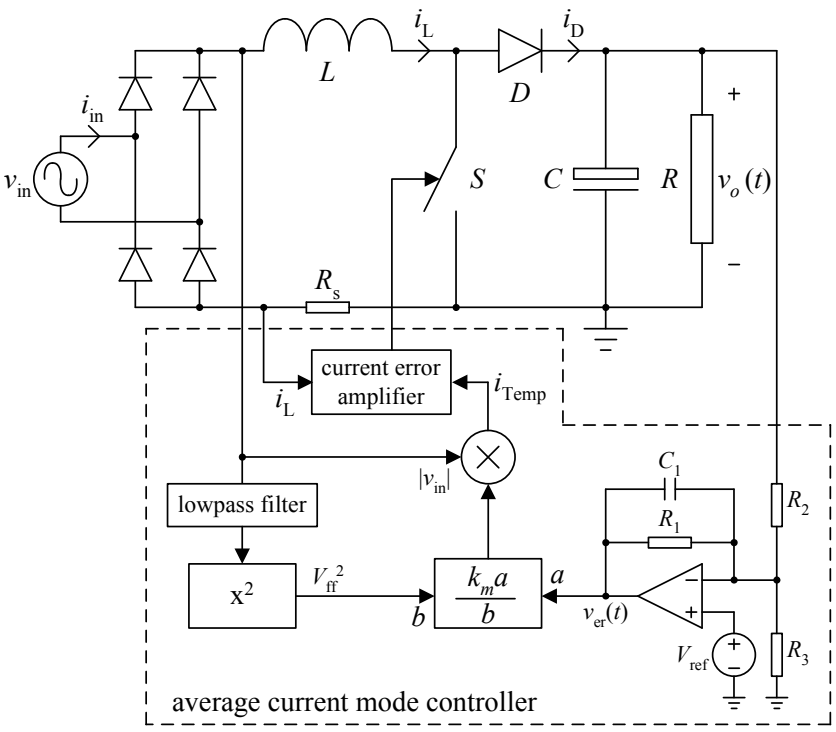


Figure 6.2: CCM boost pre-regulator under average current-mode control.

6.1.2 Derivation of Output Voltage Dynamics of Boost Pre-regulator

In this subsection, the output voltage dynamics for the boost pre-regulator under average current-mode control is studied. Fig. 6.2 shows the boost pre-regulator with average current-mode control [47]. The inductor current $i_{\rm L}$ is programmed by the current template signal $i_{\rm Temp}$ to follow the rectified input voltage. Here, $i_{\rm Temp}$ is generated by an analog multiplier which multiplies the rectified input voltage by the voltage error amplifier output $v_{\rm er}(t)$. Thus, $v_{\rm er}(t)$ effectively adjusts the inductor current to control the amplitude of $i_{\rm Temp}$. Assume that $i_{\rm L}$ is driven to follow $i_{\rm Temp}$ by the current error amplifier. From Fig. 6.2, $i_{\rm L}$ is generated by the multiplier with three inputs, i.e.,

$$i_{\rm L} = \frac{k_{\rm m} v_{\rm er}(t)|v_{\rm in}|}{V_{\rm ff}^2} = \frac{k_{\rm m} v_{\rm er}(t) V |\sin \omega t|}{(V/\sqrt{2})^2} \tag{6.16}$$

where $V_{\rm ff}$ is generated by a low-pass filter and represents the root-means-square value of the ac mains voltage; $V_{\rm ff}^2$ is a feedforward signal for compensating the disturbances in the ac mains input voltage; $|v_{\rm in}|$ provides the waveshape such that $i_{\rm L}$ synchronizes with the rectified input voltage; and $k_{\rm m}$ represents the gain of the analog multiplier. In some commercially available PFC average current-mode control ICs, such as UC3854 and ML4824, $k_{\rm m}$ is pre-determined by the boost pre-regulator design and is chosen as $V/2$ in this chapter. Therefore, $i_{\rm L}$ corresponds to

$$i_{\rm L} = v_{\rm er}(t)|\sin \omega t| \tag{6.17}$$

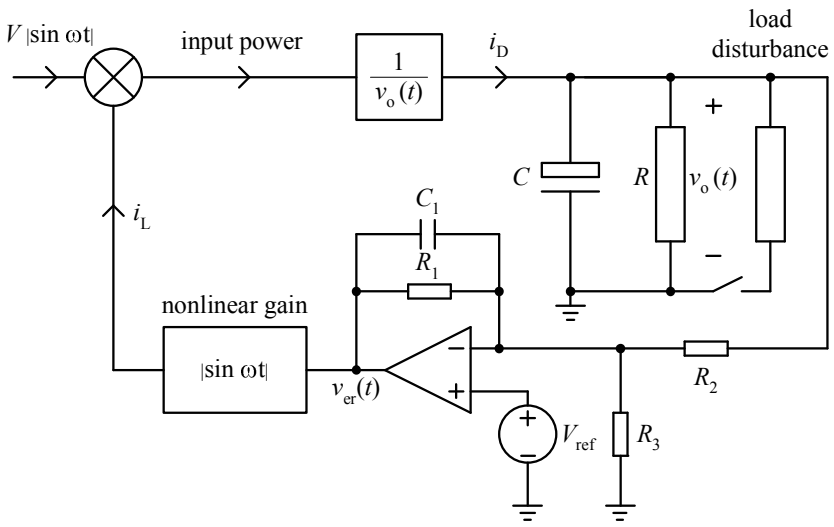


Figure 6.3: Simplified block diagram for evaluating the load transient response of the average current-mode controlled boost pre-regulator.

where $v_{\rm er}(t)$ is continually adjusted by a voltage error amplifier to maintain the desired output voltage. Obviously, to maintain $i_{\rm L}$ as a rectified sinusoid, a low-pass type feedback circuit is used to generate a nearly fixed $v_{\rm er}(t)$. Referring to Fig. 6.2, the control equation for $v_{\rm er}(t)$ is given by

$$\tau\frac{dv_{\rm er}(t)}{dt}+v_{\rm er}(t)=-G(v_{\rm o}-V_{\rm ref})+\left(\frac{R_1}{R_3}+1\right)V_{\rm ref} \tag{6.18}$$

where $V_{\rm ref}$ is the reference voltage from the average current-mode controller, $\tau = R_1C_1$ is the time constant of the feedback circuit, and $G = R_1/R_2$ is the dc gain of the feedback circuit. By substituting (6.17) into (6.4), the closed-loop output voltage dynamics of the boost pre-regulator drawing a sinusoidal input current can be expressed as

$$2v_{\rm o}\frac{dv_{\rm o}}{dt}+\frac{2v_{\rm o}^2}{RC}=\frac{Vv_{\rm er}(t)}{C}(1-\cos 2\omega t). \tag{6.19}$$

Now, (6.18) and (6.19) fully describe the closed-loop output voltage dynamics of the boost pre-regulator drawing a sinusoidal input current under average current-mode control and the corresponding block diagram is shown in Fig. 6.3. For the case of imperfect sinusoidal input current, the function $|\sin\omega t|$ in the nonlinear gain block can be replaced by $|(\sin\omega t+\sum_{\rm n=1}^{\infty}\beta_{\rm 2n+1}\sin(2{\rm n}+1)\omega{\rm t})|$. Since the system is nonlinear and subject to large variation in the input voltage, the usual averaging and linearization analysis [128] is not capable of capturing the dynamical behavior accurately. A numerical approach is employed to solve (6.18) and (6.19) for identifying the output voltage dynamics of the boost pre-regulator, as will be elaborated in the next section.

Table 6.1: Component values and circuit parameters used in simulations and calculations

Circuit components	Values
Input voltage	220 $\mathrm{V_{rms}}$
The ac mains frequency	50 Hz
Max. output power	200 W
Inductance L	1 mH
Load resistance R	722 Ω for 200 W
Load resistance R	1444 Ω for 100 W
Output voltage $v_{\mathrm{o}}(t)$	≈ 380 V
Switching frequency	100 kHz
V_{ref}	3 V
R_1	160 kΩ
C_1	100 nF

6.2 Model Verification

Since the foregoing derivations are based on a set of nonlinear differential equations which are derived from the standard state-space boost converter model, they fall short of predicting the details of the boost pre-regulator, especially for frequency range close to the switching frequency. In this section, the foregoing derivations is verified by PSPICE which simulates some crucial waveforms of an exact CCM boost converter controlled by the average current-mode controller UC3854. The complete PSPICE netlist is shown in Table C.1. Since the simulation model is the exact physical circuit model, the simulation results would represent valid verification of the behavior of the actual circuit. Furthermore, the salient characteristics of the boost pre-regulator drawing imperfect sinusoidal input current can be identified from the analytical model. The circuit parameters used in our analysis and simulations are shown in Table 6.1.

In order to visualize the reduced output voltage ripple of the boost pre-regulator drawing imperfect sinusoidal input current, the calculated output voltage based on (6.10) and (6.15) are shown in Fig. 6.4. In calculating the output voltage of the boost pre-regulator drawing imperfect sinusoidal input current, assume that the harmonic current components are at the maximum allowable levels as defined by the harmonic current emissions class, i.e. the IEC 61000-3-2 Class D limit. The maximum permissible harmonic currents in the root-means-square value of the standard are defined by milliampere per watt. For example, the maximum permissible third harmonic current can be expressed as

$$\frac{I_3}{\sqrt{2}} = \frac{VI_1}{2} 3.4 \times 10^{-3}\ \mathrm{A} \tag{6.20}$$

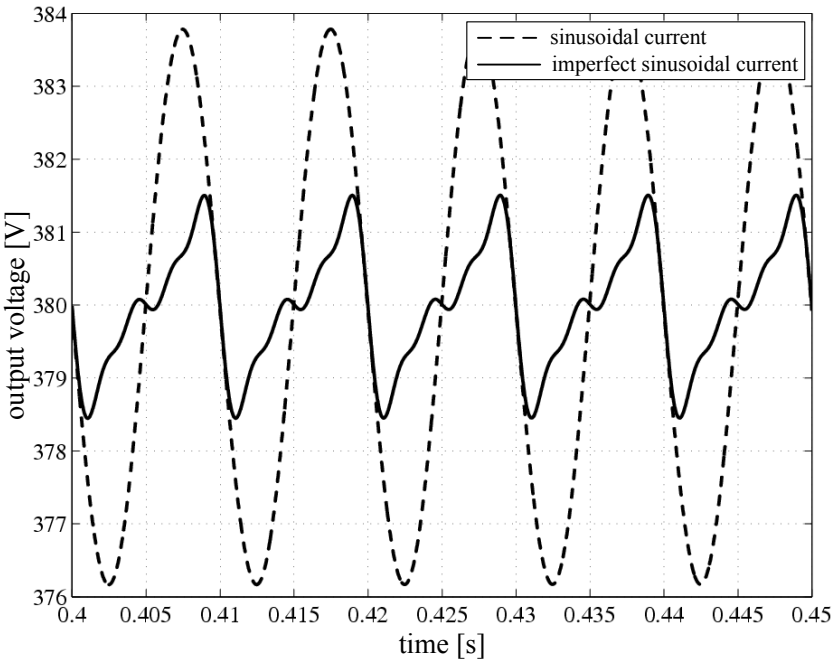


Figure 6.4: Output voltage ripple comparison between sinusoidal input current and imperfect sinusoidal input current of the boost pre-regulator.

where I_1 and I_3 are the peak value of fundamental input current and the peak value of third harmonic current, respectively, and $(VI_1)/2$ is the output power of the boost pre-regulator. Therefore, the ratios between the peak harmonic currents and the peak fundamental current are defined as

$$\begin{aligned} \beta_3 &= \frac{I_3}{I_1} = \frac{V}{\sqrt{2}} 3.4 \times 10^{-3} \\ \beta_5 &= \frac{I_5}{I_1} = \frac{V}{\sqrt{2}} 1.9 \times 10^{-3} \\ \beta_7 &= \frac{I_7}{I_1} = \frac{V}{\sqrt{2}} 1.0 \times 10^{-3}. \end{aligned} \tag{6.21}$$

Fig. 6.5 shows the calculated inductor current waveform based on (6.21) for 220 $\mathrm{V_{rms}}$ input voltage at 200 W output power. The simulated output voltage waveforms are obtained to verify the calculated output voltage waveforms, as shown in Fig. 6.6. It reveals that the calculated results shown in Fig. 6.4 are close to the simulated results shown in Fig. 6.6. The calculated results shown in Fig. 6.5 are also close to the simulated inductor current waveforms under average current-mode control shown in Fig. 6.7. For the same values of output capacitor, output voltage, and output power, the boost pre-regulator drawing imperfect sinusoidal input current gives smaller output voltage ripple compared to the boost pre-regulator drawing perfectly sinusoidal input current. According to the calculated results, the output voltage ripple is reduced by 59.8 % as a result of drawing imperfect sinusoidal input current from the ac mains. Fig. 6.8 shows the relation between the reduced voltage ripple and the level of the

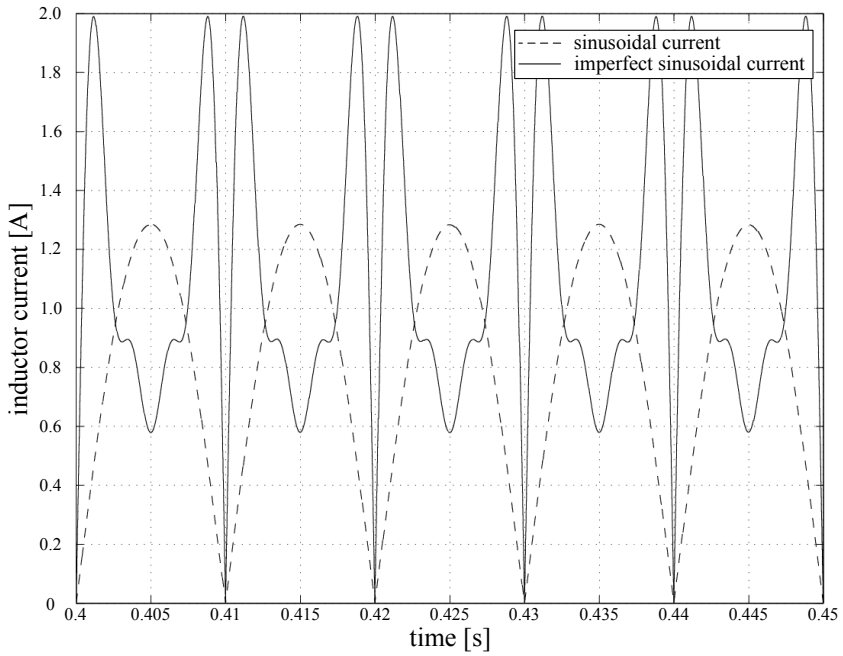


Figure 6.5: Calculated inductor current for 220 V_{rms} input voltage at 200 W output power: rectified sinusoidal inductor current (dash line) and imperfect rectified sinusoidal inductor current (solid line) based on Eqn. 6.21.

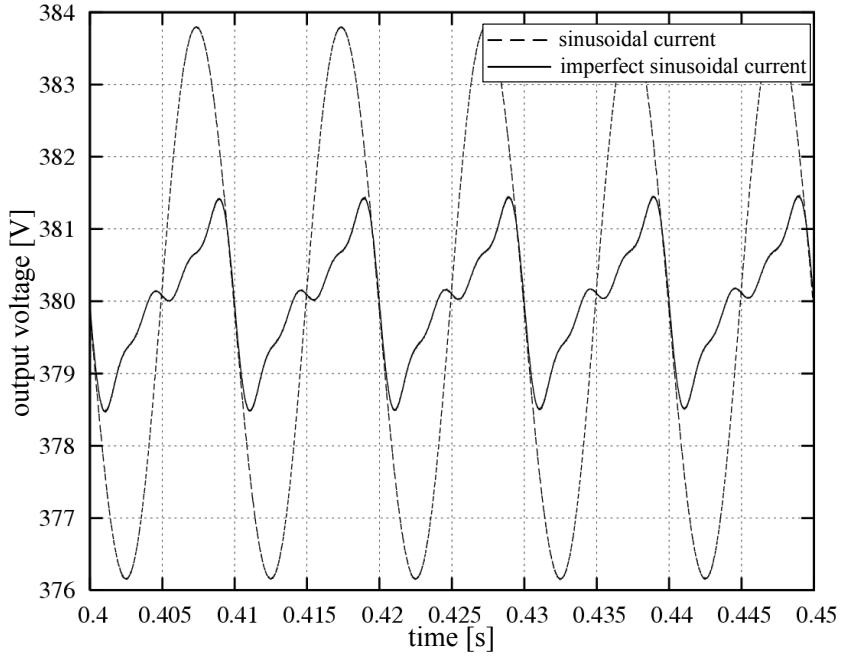


Figure 6.6: Simulated output voltage waveforms of sinusoidal input current and imperfect sinusoidal input current of the boost pre-regulator.

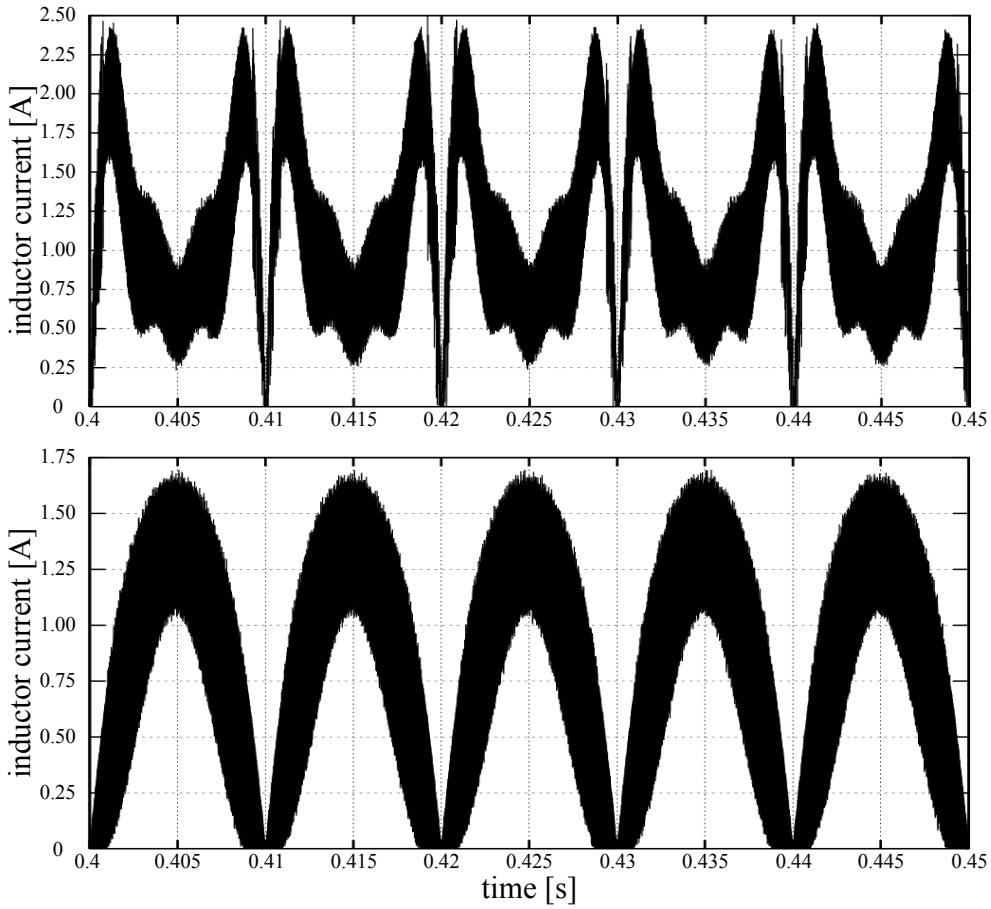


Figure 6.7: Simulated imperfect sinusoidal inductor current waveform (upper trace) and simulated sinusoidal inductor current waveform (lower trace) of the CCM boost converter under average current-mode control.

input current harmonic content based on the IEC 61000-3-2 Class D limit. At the maximum allowed harmonic current contents, i.e., total of 19 harmonic components, the output voltage ripple of the boost pre-regulator drawing imperfect sinusoidal input current reduced by 61.3 %. Fig. 6.9 shows the relation between the reduced output capacitance and the level of the input current harmonic content based on the same standard. Assuming that the output ripple voltage is defined at 1 % of the output voltage, i.e., the peak-to-peak value of the output ripple voltage is 3.8 V, from (6.10), the output capacitance of the boost pre-regulator drawing sinusoidal input current is required to be 440 μF at 200 W output power. However, the output capacitance of the boost pre-regulator drawing imperfect sinusoidal input current is greatly reduced. Based on (6.15) and (6.21), when the boost pre-regulator drawing input current contains third, fifth, and seventh harmonic components, the output capacitance can be reduced to 176 μF under the same condition. Fig. 6.10 shows the relationship between the peak-to-peak value of the output ripple voltage and the output capacitance for various input current

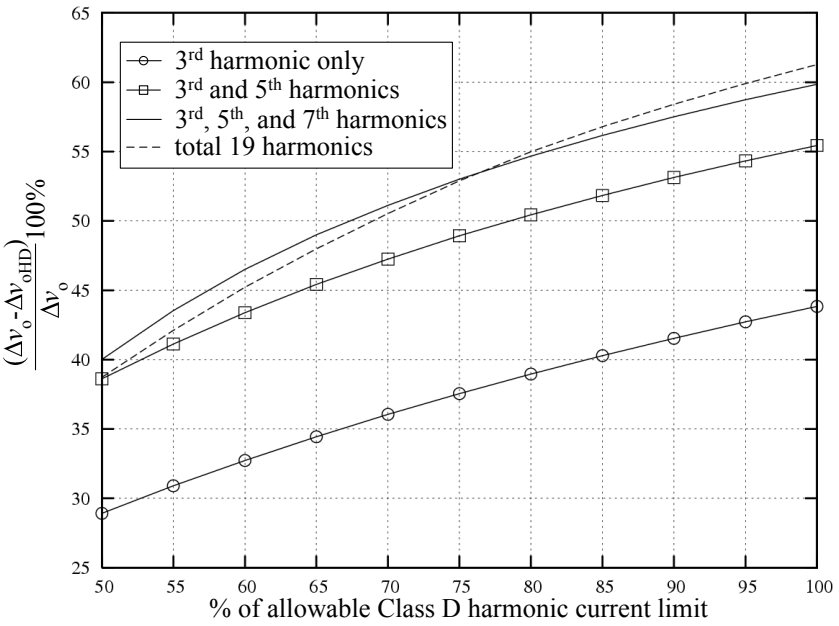


Figure 6.8: Relation between the reduced voltage ripple and the input current harmonic content at 200 W output power. $\Delta v_{\rm o}$ is the peak-to-peak output ripple voltage for sinusoidal input current and $\Delta v_{\rm oHD}$ is the peak-to-peak output ripple voltage for imperfect sinusoidal input current.

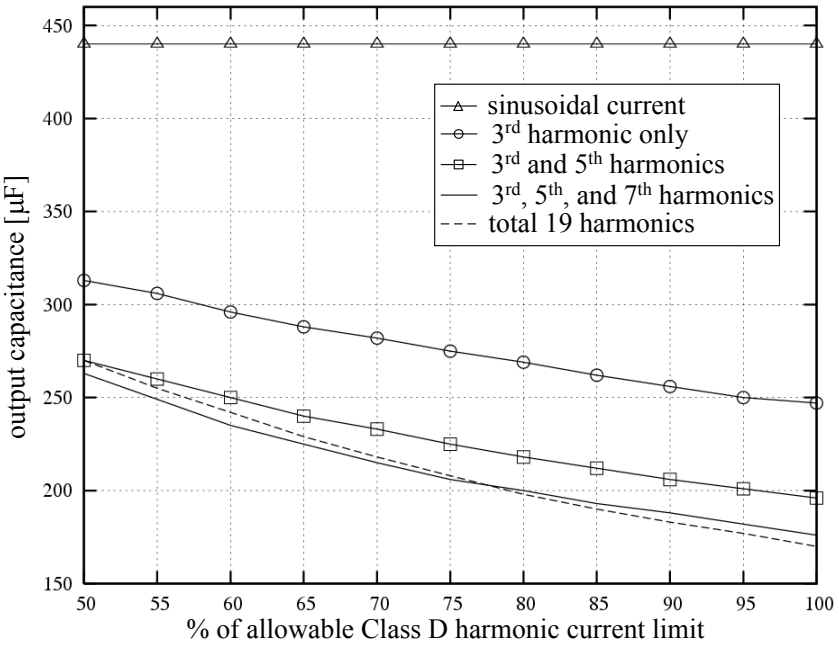


Figure 6.9: Relationship between the output capacitance and the different harmonic contents of input current at 200 W output power. The peak-to-peak value of output voltage ripple is 3.8 V.

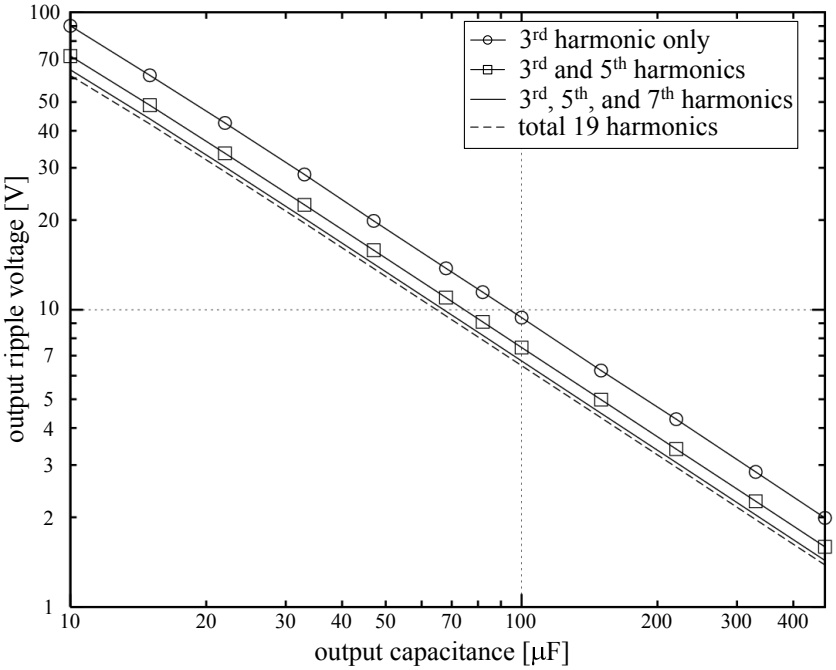


Figure 6.10: Relation between the peak-to-peak values of output ripple voltage and the output capacitance at different waveshapes of imperfect input current based on maximum harmonic current limit of the IEC 61000-3-2 Class D limit at 200 W output power.

waveshapes that correspond to the maximum harmonic current limit of the IEC 61000-3-2 Class D limit.

As studied in Section 6.1.2, two nonlinear differential equations have been derived to describe the output voltage dynamics of the boost pre-regulator. To clarify (6.18) and (6.19), a comparison is made between the calculated output voltage by a numerical approach[1] and the output voltage from PSPICE simulation under a load transient condition, as shown in Fig. 6.11. It reveals that the calculated results closely match the simulated results. Of course, the output voltage dynamics of the boost pre-regulator is influenced by two time constants, τ and RC, as well as the dc gain G of the feedback circuit. To help visualize how the output voltage dynamics is affected by these parameters, we will henceforth focus on the variation of these parameters. Our calculation is based on (6.18) and (6.19) to generate the output voltage waveforms under load transient condition. However, as mentioned before, τ of the feedback circuit should be five times longer than the ac mains cycle in order to maintain a low input-current distortion [27], [47], [52], [115],[130]. In particular, our focus is on the qualitative change of the output voltage dynamics when G or C are varied. To observe the trend, C is fixed while G is varied. Similar trend is observed when G is fixed while C is varied. A summary of the observed

[1] A MATLAB program for calculating $v_{\rm o}$ and $v_{\rm er}(t)$ of the boost pre-regulator under average current-mode control is shown in Table C.2 in the Appendix C.

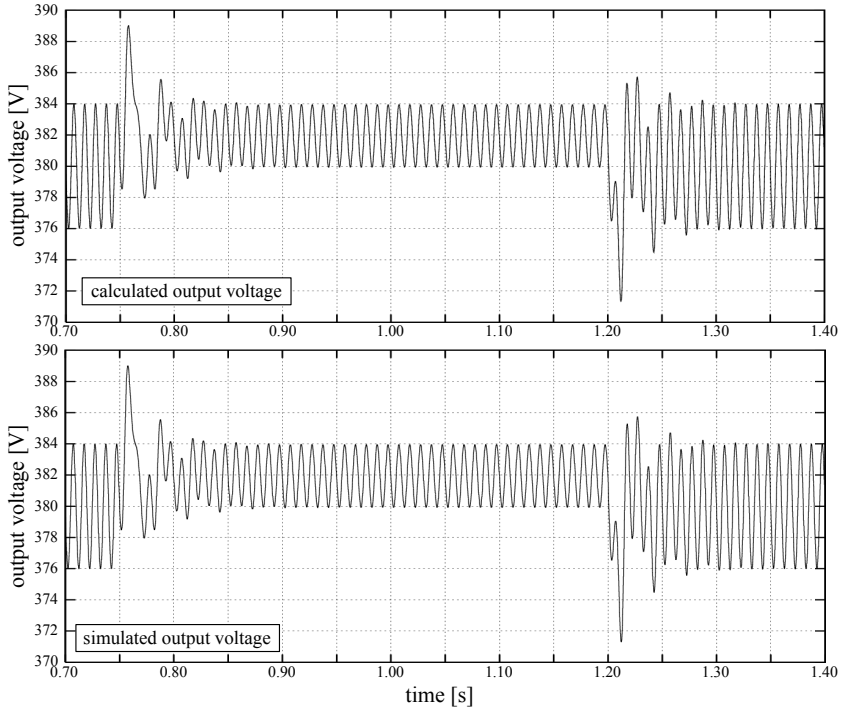


Figure 6.11: Calculated and simulated output voltage waveforms for sinusoidal input current for load stepping between 200 W and 100 W for verification of (6.18) and (6.19).

behavior is as follows.

1. Due to the action of the low-pass feedback circuit, increasing G improves the static output voltage regulation. Fig. 6.12 shows the calculated output voltage waveforms for different values of G.

2. When C is large, the voltage overshoot level becomes less severe. Fig. 6.13 shows the calculated output voltage waveforms for different values of C.

However, the caution is that increasing G causes an extra input current harmonics [27] as well as instability problem in the boost pre-regulator [134]. Some calculated voltage waveforms are shown in Fig. 6.14 when the output power is changed from 100 W to 200 W in the boost pre-regulator under average current-mode control and drawing imperfect sinusoidal input current. This imperfect sinusoidal input current is constructed from mixing fundamental current with third, fifth and seventh harmonic components and the amplitudes of the harmonic current are determined from (6.21). Interestingly, in Fig. 6.14, the boost pre-regulator drawing imperfect sinusoidal input current allows higher G values than the boost pre-regulator drawing sinusoidal input current. Since the output voltage ripple for the case of imperfect sinusoidal input current is relatively smaller than for the case of sinusoidal input current, the smaller voltage ripple appearing on the feedback path leads to more stable opera-

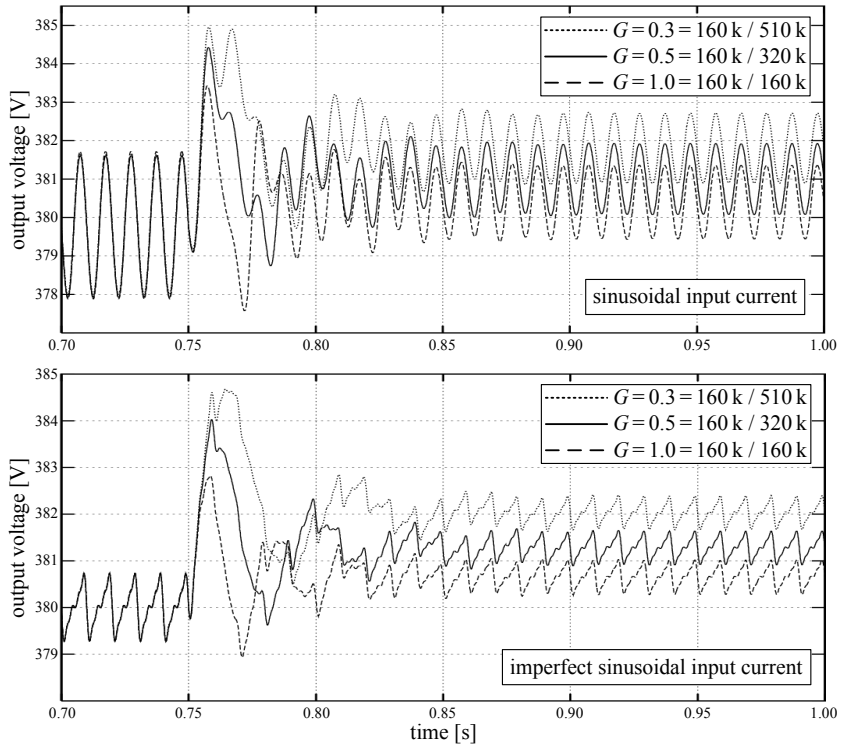


Figure 6.12: Calculated output voltage waveforms to illustrate the effect of G. $C = 470$ μF and output power stepping between 200 W and 100 W.

tion [134]. In addition, with smaller voltage ripple, the range of G in the boost pre-regulator can be expanded for enhancing the static output voltage regulation. Our analysis has shown that the boost pre-regulator drawing imperfect sinusoidal input current has better static output voltage regulation and smaller output ripple voltage than the boost pre-regulator drawing sinusoidal input current. Several design curves can be plotted to provide a quick guideline for designing the imperfect sinusoidal input-current boost pre-regulator. Since there are no common definitions for the settling time, the output voltage overshoot, and the output voltage undershoot at load transient condition, the following definitions to facilitate further discussion in the subsequent parts of the chapter will be adopted. The output voltage waveform of the boost pre-regulator at load transient condition shown in Fig. 6.15 assists to illustrate the definitions.

- $T_{\rm so}$ and $T_{\rm su}$ denote the settling time under a positive stepped load and a negative stepped load, respectively. The settling time includes the propagation delay plus the time required for the output to slew to the final state. The final state is the first peak (positive or negative) output voltage in the steady state.

- Voltage overshoot, $V_{\rm os}$, is defined as the difference between the last negative peak output voltage before the load transient and the highest positive peak output voltage after the load transient.

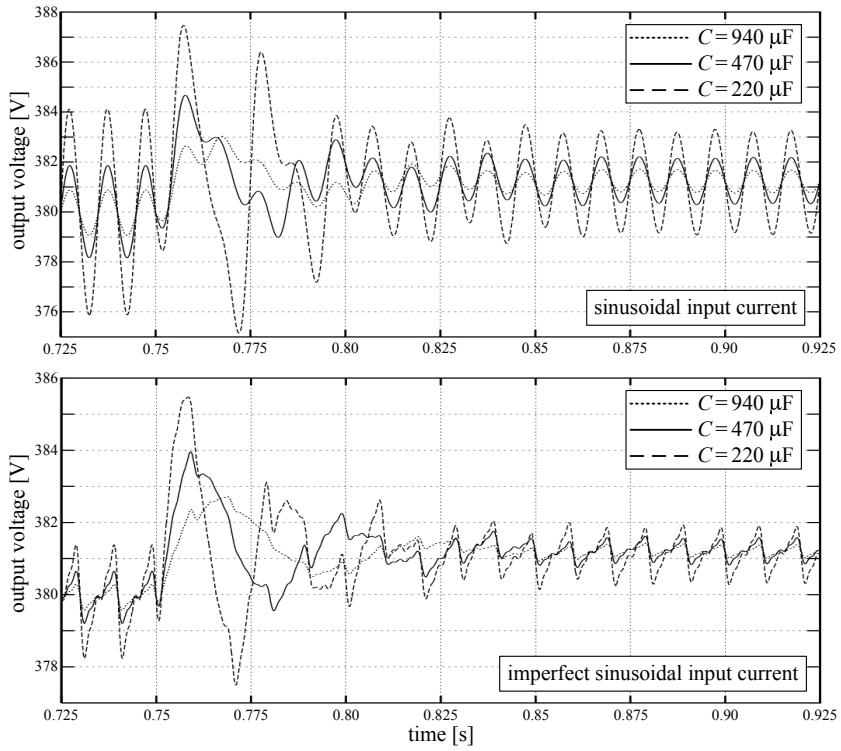


Figure 6.13: Calculated output voltage waveforms to show the effect of C. G is equal to 0.5 = 160 kΩ/320 kΩ and output power steps from 200 W to 100 W.

- Voltage undershoot, $V_{\rm us}$, is defined as the difference between the last positive peak output voltage before the load transient and the lowest negative peak output voltage after the load transient.

Since the primary concerned is the stability of the boost pre-regulator drawing imperfect sinusoidal input current in conjunction with the gain of the feedback circuit G and the boost pre-regulator output capacitance C, our attention is drawn to the effects of varying G and C on the stability boundary of the boost pre-regulator. Fig. 6.16 (a) shows a set of numerical results based on (6.18) and (6.19), which define stability boundaries for different values of G and C for the boost pre-regulator drawing imperfect sinusoidal input current. Since increasing G generates an extra input current harmonic distortion, the boundary of G is further restricted for the case of imperfect sinusoidal input current. In order to give a better view of the output voltage dynamics of the boost pre-regulator drawing imperfect sinusoidal input current, a large number of calculated results based on (6.18) and (6.19) under load transient condition have been collected. Here, a few representative parameters of output voltage transients in Figs. 6.16 (b) to (d), which serve to exemplify the salient findings concerning the output voltage dynamics of the boost pre-regulator drawing imperfect sinusoidal input current, are showed. Fig. 6.16 (b) depicts the settling times for different values of G and C. For a given

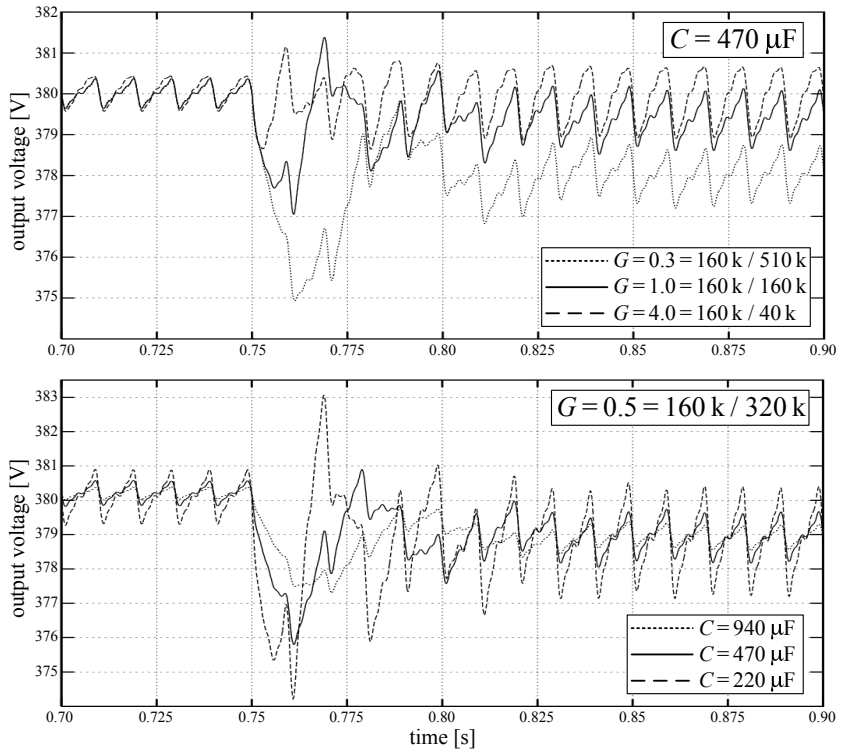


Figure 6.14: Calculated output voltage waveforms for imperfect sinusoidal input current to show the effect of G (upper figure) and the effect of C (lower figure). Output power is stepped from 100 W to 200 W.

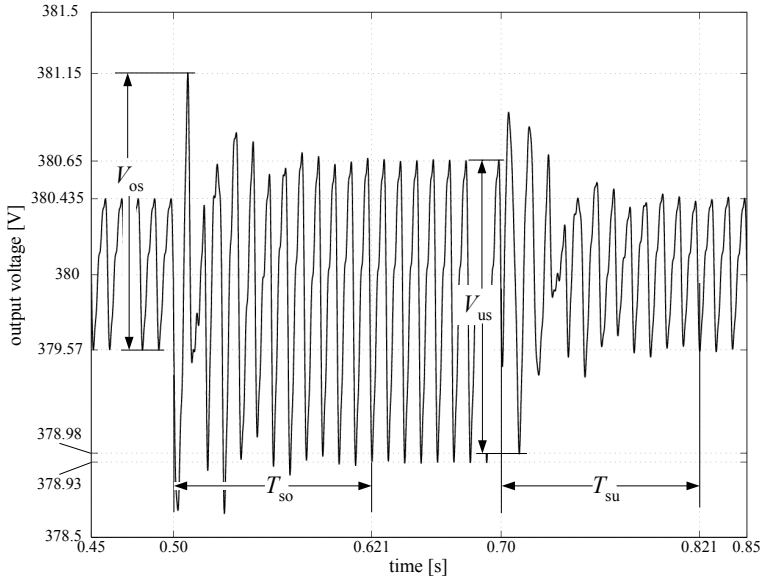


Figure 6.15: Definitions of settling time, output voltage overshoot, and output voltage undershoot at load transient situation in the boost pre-regulator.

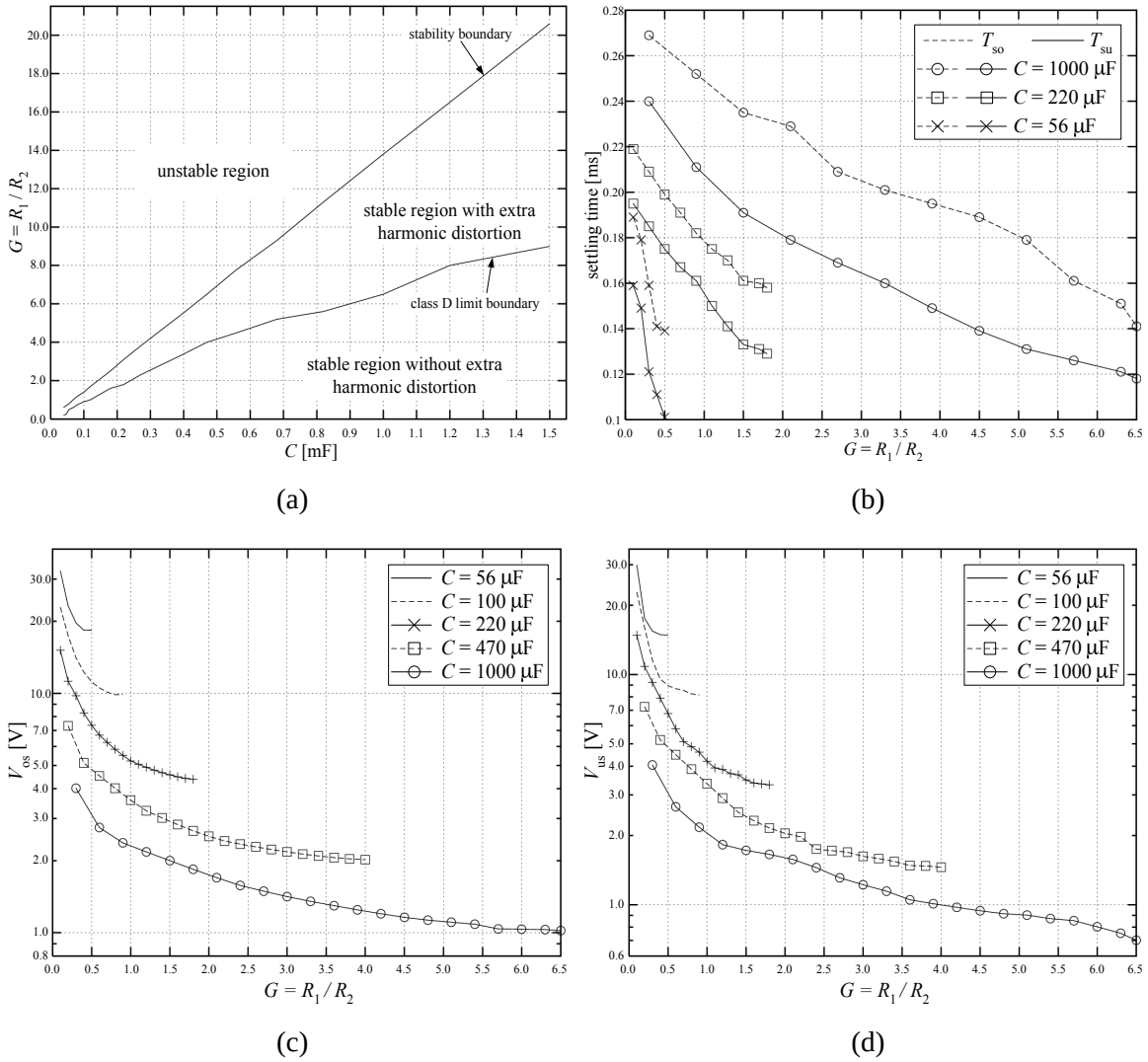


Figure 6.16: (a) Calculated stability boundary of the boost pre-regulator drawing imperfect sinusoidal input current at different values of G and C at 200 W ($R = 722\ \Omega$) output power. (b) Settling times of the boost pre-regulator drawing imperfect sinusoidal input current for load stepping between 200 W and 100 W. (c)–(d) Voltage overshoot and voltage undershoot for different values of G and C for load stepping between 200 W and 100 W (722 Ω and 1444 Ω).

G, the settling times for small values of C are shorter than the settling times for large values of C. However, increasing C with high G, the settling times can be greatly reduced. Figs. 6.16 (c) and (d) show the output voltage overshoot levels and the output voltage undershoot levels, respectively, under load transient condition. It can be observed that increasing C is more effective than increasing G in reducing the output voltage overshoot and undershoot.

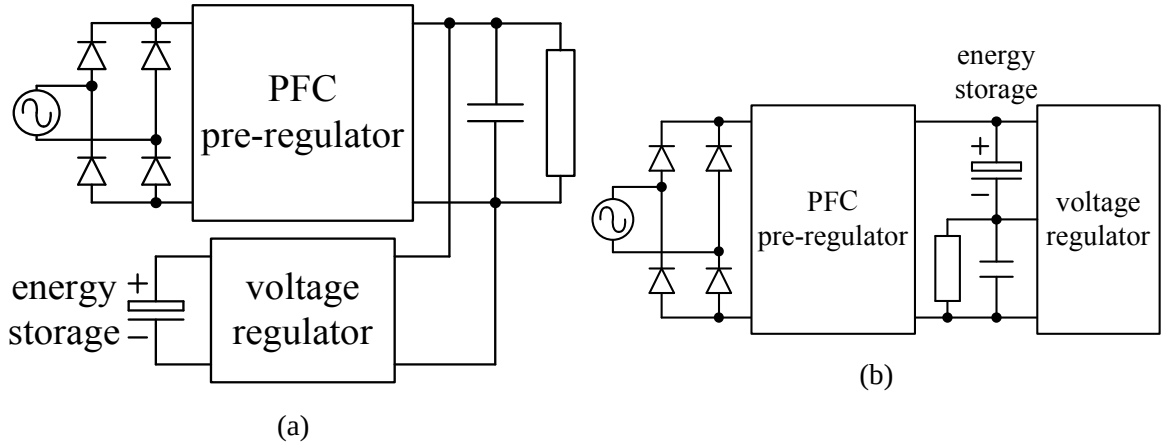


Figure 6.17: Block diagram of switching regulator with tight voltage regulation and fast load transient response. (a) proposed by Gegner *et al.* and (b) proposed by Garcíc *et al.*.

6.3 Design Examples

In the following, the design performance tradeoffs of switching regulators in terms of meeting the IEC 61000-3-2 Class D limit, achieving a higher efficiency, and maintaining a tightly regulated output voltage will be illustrated.

Example 1

A noncascading switching regulator which is composed of a pre-regulator and a parallel-connected voltage regulator, as shown in Fig. 6.17 (a), is considered. The voltage regulator absorbs the excessive power of the pre-regulator. The excessive power is stored in an energy storage element through the voltage regulator. This stored energy is released through the voltage regulator again to the output load for keeping a constant output power. Therefore, the voltage regulator is a bi-directional converter and processes the excessive power twice in the rectified ac mains period. The operational details and the output load voltage performances of this switching regulator can be found in [135], [136]. The switching regulator achieves low-frequency ripple-free output voltage with fast load transient response. Fig. 6.18 illustrates the excessive power processed by the voltage regulator when the pre-regulator is drawing sinusoidal input current. The excessive power in one rectified ac mains period can be calculated as

$$\begin{aligned} P_{\rm e} &= \frac{1}{t_{\rm p}} \int_{0.25t_{\rm p}}^{0.75t_{\rm p}} [P_{\rm o}(1-\cos 2\omega t) - P_{\rm o}]dt \\ &= 0.318P_{\rm o} \end{aligned} \tag{6.22}$$

where $P_{\rm o}(1-\cos 2\omega t)$ and $P_{\rm o}$ are the input power of the pre-regulator and the output load power,

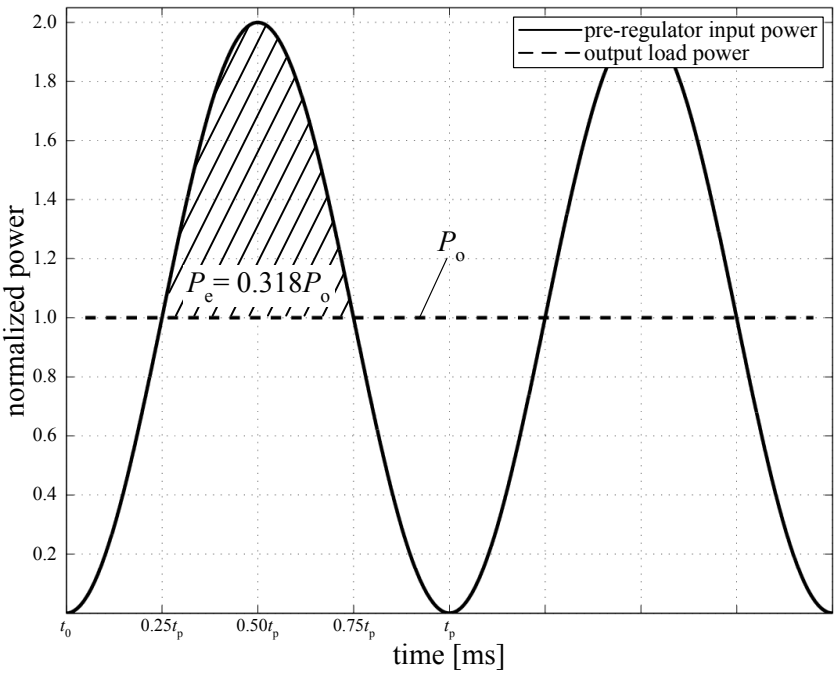


Figure 6.18: Power waveforms in pre-regulator drawing sinusoidal input current to illustrate the efficiency improvement of the noncascading switching regulator proposed by Gegner *et al.*.

respectively, and $t_{\rm p}$ is the period of the rectified ac mains. From (6.22), 31.8 % of the total input power is processed by the voltage regulator twice in one rectified ac mains period. Therefore, the total processed input power of this switching regulator drawing sinusoidal input current is 1.636 times [28] in one rectified ac mains period instead of twice in the conventional cascade configuration [130]. This parallel-connected configuration generally enhances the power conversion efficiency. Moreover, the efficiency by drawing imperfect sinusoidal input current can be further improved. Fig. 6.19 illustrates the relation between the excessive output power and the output load power. Intuitively, the excessive power in the case of the imperfect sinusoidal input current is much smaller than that of the sinusoidal input current. Thus, less input power is processed by the voltage regulator to improve the power conversion efficiency. The imperfect sinusoidal input current parameters are based on (6.11) and (6.21). The excessive output power for the pre-regulator drawing imperfect sinusoidal input current in one rectified ac mains period can be expressed as

$$\begin{aligned} P_{\rm eHD} &= \frac{1}{t_{\rm p}}[\int_{t_1}^{t_2}(P_{\rm inHD}-P_{\rm o})dt+\int_{t_3}^{t_4}(P_{\rm inHD}-P_{\rm o})dt] \\ P_{\rm inHD} &= P_{\rm o}[1-(1-\beta_3)\cos 2\omega t-(\beta_3-\beta_5)\cos 4\omega t \\ &\quad -(\beta_5-\beta_7)\cos 6\omega t-\beta_7\cos 8\omega t] \end{aligned} \tag{6.23}$$

where $P_{\rm inHD}$ is the input power of the pre-regulator drawing imperfect sinusoidal input current. t_2-t_1 and t_4-t_3 are the time intervals where $P_{\rm inHD}$ is higher than $P_{\rm o}$. Referring to Fig. 6.19, t_1, t_2, t_3, and

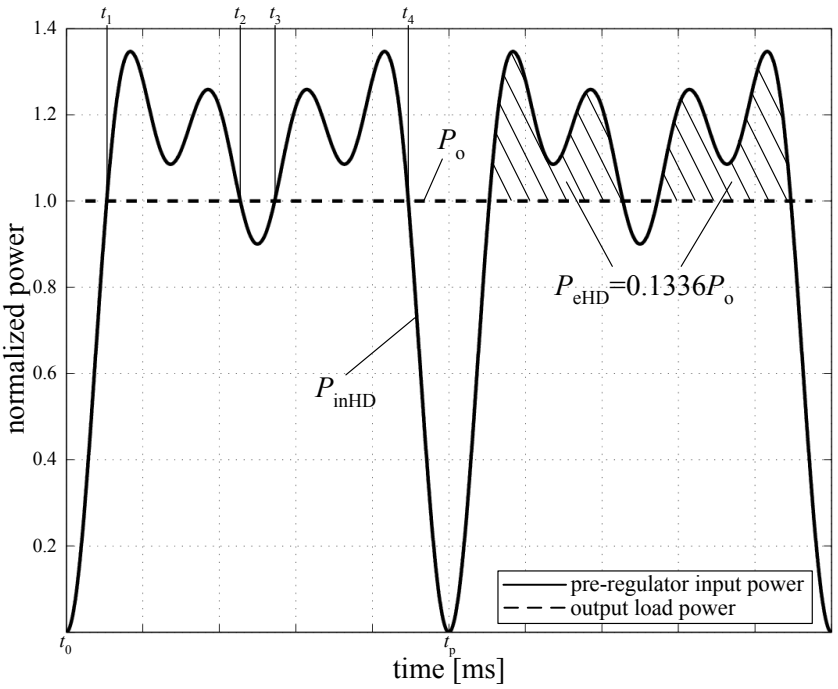


Figure 6.19: Power waveforms in pre-regulator drawing imperfect sinusoidal input current to illustrate the efficiency improvement of the noncascading switching regulator proposed by Gegner *et al.*

t_4 can be solved by

$$\begin{aligned} 1 &= 1-(1-\beta_3)\cos 2\omega t-(\beta_3-\beta_5)\cos 4\omega t \\ &\quad -(\beta_5-\beta_7)\cos 6\omega t-\beta_7\cos 8\omega t \end{aligned} \tag{6.24}$$

From (6.21) and $V = 220\sqrt{2}$ V, $t_{\rm n}$ in terms of $t_{\rm p}$ can be defined as

$$\begin{aligned} t_1 &= 0.105886t_{\rm p} \\ t_2 &= 0.455159t_{\rm p} \\ t_3 &= 0.544841t_{\rm p} \\ t_4 &= 0.894114t_{\rm p}. \end{aligned}$$

Therefore, from (6.23), $P_{\rm eHD}$ in terms of $P_{\rm o}$ is equal to

$$P_{\rm eHD} = 0.1336P_{\rm o}. \tag{6.25}$$

From (6.25), only 13.36 % of the total input power is processed twice by the voltage regulator in one rectified ac mains period. The total processed input power of this switching regulator drawing imperfect sinusoidal input current in its constituent regulators is reduced from 1.636 times to 1.2672 times. Fig. 6.20 shows the relation between the excessive input power and the various input current

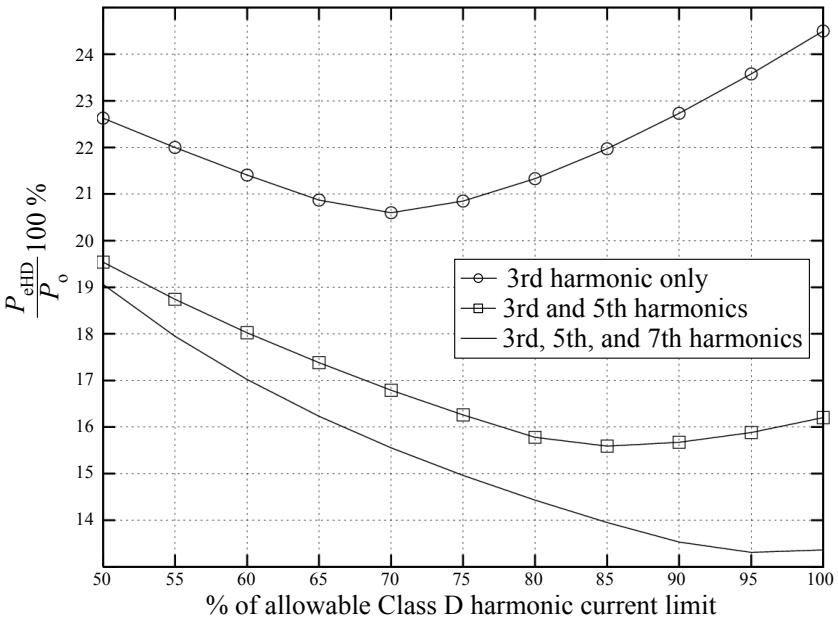


Figure 6.20: Relation between the excessive input power and the different harmonic contents of input current for the noncascading switching regulator proposed by Gegner *et al.*.

waveshapes that correspond to the maximum harmonic current limit of the IEC 61000-3-2 Class D limit.

Fig. 6.17 (b) shows a noncascading switching regulator connection diagram that has been proposed by García *et al.* [95]. Since a portion of the input power (direct power) of the switching regulator is processed by only its pre-regulator and given to the load directly, more efficient power conversion is expected. The design details and the output load voltage performances of this switching regulator can be found in Chapter 4. Fig. 6.21 illustrates the amount of input power that is processed by only the pre-regulator and transferred to the load when the pre-regulator is drawing different waveshapes of input current. To maintain a tight voltage regulation and maximize the direct power transfer to the load, the peak of the direct power should be equal to the output load power. Therefore the maximum direct power when the pre-regulator is drawing sinusoidal input current can be calculated as

$$\begin{aligned} P_{\rm d} &= \frac{1}{t_{\rm p}}\int_0^{t_{\rm p}} \frac{P_{\rm o}}{P_{\rm inp}}(1-\cos 2\omega t)dt \\ &= 0.5P_{\rm o} \end{aligned} \tag{6.26}$$

where $P_{\rm o}(1-\cos 2\omega t)$ and $P_{\rm o}$ are the input power of the pre-regulator and the output load power, respectively, $P_{\rm inp}$ is the peak value of the input power, and $t_{\rm p}$ is the period of the rectified ac mains. From (6.26), only 50 % of the total input power is processed by only the pre-regulator and directly transferred to the load. However, the value of the direct power can be increased when the pre-regulator

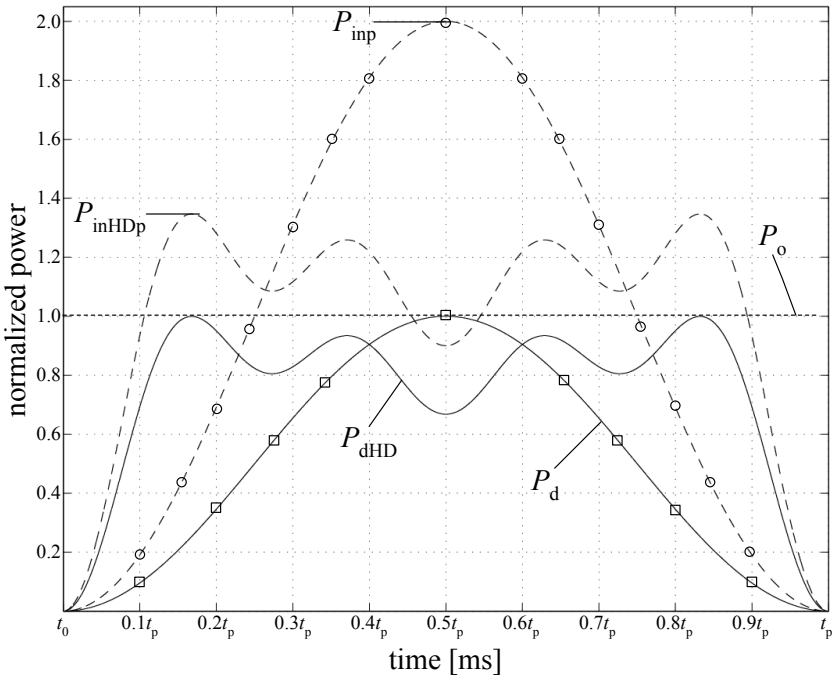


Figure 6.21: Power waveforms to illustrate the relation between the direct power and the different waveshapes of the input current for the noncascading switching regulator proposed by García *et al.*.

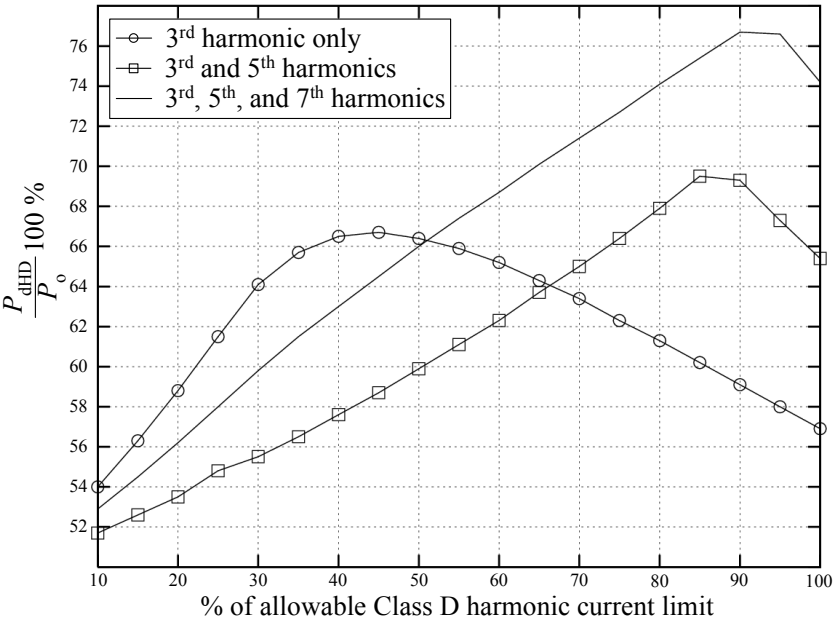


Figure 6.22: Relation between the values of the maximum allowable direct power and the different waveshapes of imperfect input current based on maximum harmonic limit of the IEC 61000-3-2 Class D limit at 220 V_{rms} input voltage for the noncascading switching regulator proposed by García *et al.*.

is drawing imperfect sinusoidal input current. The maximum direct power in the case of the imperfect sinusoidal input current is much larger than that of the sinusoidal input current, as shown in Fig. 6.21. The direct power for the pre-regulator drawing imperfect sinusoidal input current in one rectified ac mains period can be expressed as

$$\begin{aligned} P_{\mathrm{dHD}} &= \frac{1}{t_{\mathrm{p}}}\int_0^{t_{\mathrm{p}}} \frac{P_{\mathrm{o}}}{P_{\mathrm{inHDp}}}[1-(1-\beta_3)\cos 2\omega t \\ &\quad -(\beta_3-\beta_5)\cos 4\omega t-(\beta_5-\beta_7)\cos 6\omega t \\ &\quad -\beta_7\cos 8\omega t]dt \qquad (6.27) \\ &= 0.742P_{\mathrm{o}} \end{aligned}$$

where P_{inHDp} is the peak input power of the pre-regulator drawing imperfect sinusoidal input current and the values of β_{n} are based on (6.21) at input voltage equal to 220 $\mathrm{V_{rms}}$. Based on the result from (6.27), 74.2 % of the total input power is processed by only the pre-regulator and directly transferred to the load. Fig. 6.22 shows the relation between the direct power and the various input current waveshapes that correspond to the maximum harmonic current limit of the IEC 61000-3-2 Class D limit. In short, drawing imperfect sinusoidal input current of these switching regulators allow further improvement of the power conversion efficiency. Furthermore, the power handling of their voltage regulators also greatly reduced.

Example 2

In some applications, the output load remains more or less constant and a very fast output voltage response is unnecessary [140], [141]. For these applications, the pre-regulator alone is an adequate solution [27], [115]. This design example uses the one-converter configuration drawing imperfect sinusoidal input current to achieve moderately fast output voltage response with maximized power conversion efficiency. As the input power is only processed by one switching converter, the power conversion efficiency can be maximized. In addition, the output ripple voltage can be reduced by drawing imperfect sinusoidal input current. To improve output voltage response without adding extra harmonic distortion during steady-state operation, several techniques have been proposed in the literature, e.g., adaptive output ripple voltage estimator [119], load-current injection method [124], and regulation band circuit [116], [129]. The regulation band circuit is easier to implement than the adaptive estimator and the load-current injection method is used in commercial PFC controllers. In particular, the regulation band circuit can be constructed by discrete analog circuits. Fig. 6.23 shows a block diagram of the one-converter switching regulator with modified PFC controller for achieving moderately fast output voltage response. The operation of the regulation band circuit is simple. If the output voltage remains within a defined regulation band, the voltage control loop gain of the switching regulator is held constant. When the output voltage goes out of the regulation band during

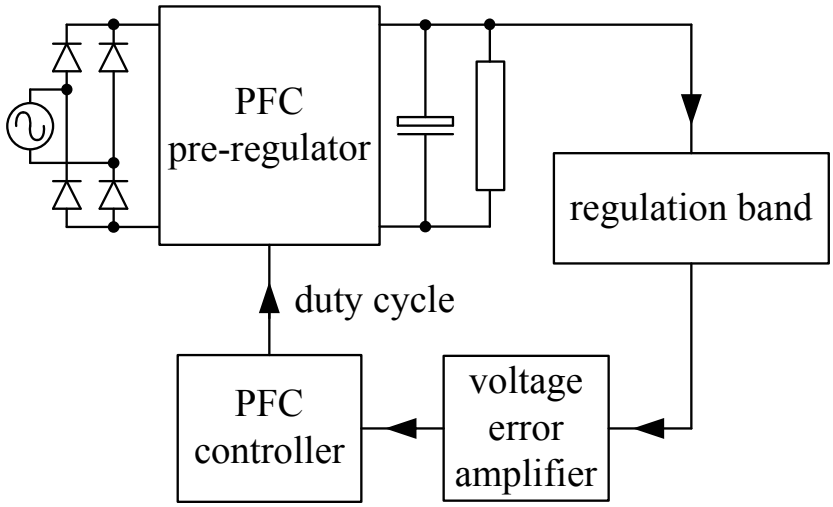


Figure 6.23: Block diagram of one-converter switching regulator with modified PFC controller for achieving moderately fast output voltage response.

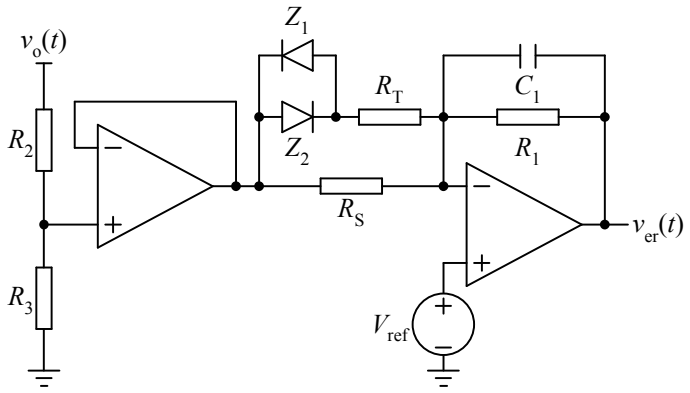


Figure 6.24: Practical regulator band circuit with voltage feedback loop.

the load transient, the voltage control loop gain is increased to rapidly return the output voltage to the regulation band. The output voltage with the regulation band circuit provides fair voltage regulation. A practical regulator band circuit is shown in Fig. 6.24. $\frac{R_1(R_T+R_S)}{R_T R_S}$ and $\frac{R_1}{R_S}$ are the voltage control loop gain of the transient state and the voltage control loop gain in the steady state, respectively. Also, Z_1 and Z_2 are zener diodes which define the regulation band. When the output voltage is out of the regulation band, either Z_1 or Z_2 will conduct. Therefore, the gain of the voltage loop changes from $\frac{R_1}{R_S}$ to $\frac{R_1(R_T+R_S)}{R_T R_S}$. To help design the regulation band circuit, Fig. 6.16 (a) can be used to define the voltage control loop gain of the transient state and Figs. 6.16 (c) and (d) can be used to identify the regulation band.

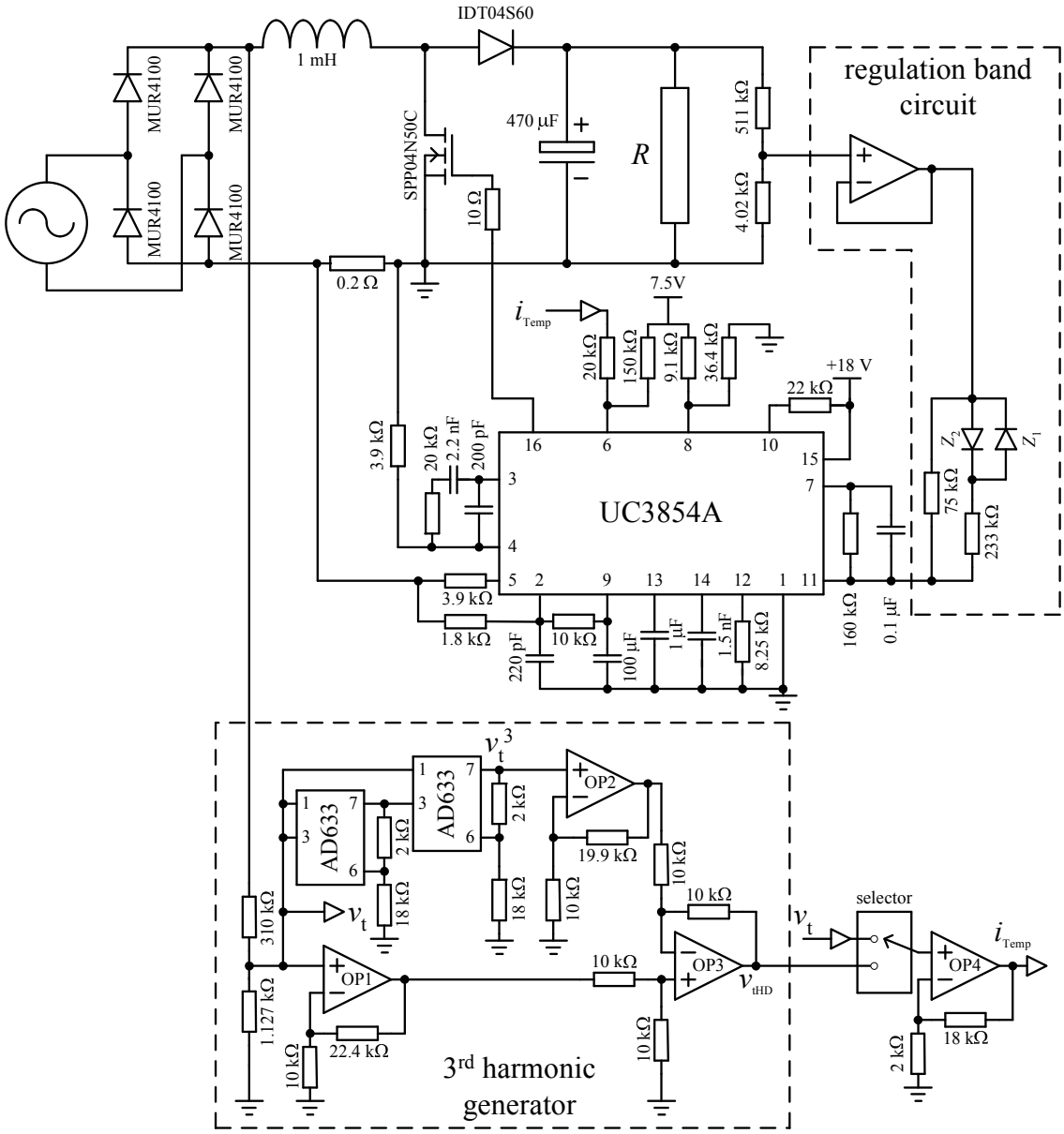


Figure 6.25: Full schematic diagram of the experimental prototype based on one-converter configuration with a third harmonic injection circuit and a regulation band circuit.

6.4 Experimental Results

To verify the validity of the effect of drawing imperfect sinusoidal input current for reducing the output ripple voltage, an experimental prototype based on the one-converter switching regulator drawing imperfect sinusoidal input current with regulation band control has been constructed. In addition, the design of the regulation band circuit parameters are determined by the salient findings that are shown in Fig. 6.16. The major design specifications of the prototype are: the input voltage is 220 V_{rms}, the

ac mains frequency is 50 Hz, the output voltage is 380 V, the maximum output power is 200 W, and the input current is imperfect sinusoidal satisfying the IEC 61000-3-2 Class D limit. Fig. 6.25 shows the schematic diagram of the prototype with a third harmonic generator [133] and the regulation band circuit. The average current-mode controller UC3854 is employed to provide PFC function. The voltage template for shaping the inductor current is created by the third harmonic generator. The third harmonic generator is constructed from two analog multipliers and a few operational amplifiers. The input current of the prototype can be expressed as

$$i_{\mathrm{L_{HD}}} = \left| I_1(\sin \omega t + 0.748 \sin 3\omega t) \right| \tag{6.28}$$

where I_1 is controlled by the the output voltage of the voltage error amplifier. Therefore the voltage template for the imperfect sinusoidal input current is

$$v_{\mathrm{tHD}} = \left| (3.244 \sin \omega t - 2.992 \sin^3 \omega t) \right|. \tag{6.29}$$

The operational amplifiers provide appropriate voltage gains and subtraction function to formulate (6.29). The voltage gains of OP1 and OP2 are set as 3.244 and 2.99, respectively. OP3 provides a subtraction function. OP4 gives a voltage gain of 10 to satisfy the signal requirement of UC3854. The effect of the output ripple voltage on the input current with third harmonic current is examined. Fig. 6.26 shows the experimental waveforms at full load condition when i_{Temp} synchronizes with the rectified input voltage. The output ripple voltage (peak-to-peak) is around 7.5 V. Fig. 6.27 shows the experimental waveforms at full load condition when i_{Temp} is generated by the third harmonic generator. The output ripple voltage (peak-to-peak) is around 4.6 V. It can be seen that the output ripple voltage of the prototype drawing the input current with third harmonic component is reduced by 39 %. The regulation band circuit inserted in the voltage loop is tested. Fig. 6.16 (a) is used to design the voltage control loop gain. The value of the voltage loop gain is defined as 2.8 at the transient state. Experiments for the output voltage dynamic are also carried out for the prototype. The dynamic response is tested by a load stepping between 100 W to 200 W, as shown in Fig. 6.28. From Fig. 6.28 (b), we observe that the settling times, the voltage overshoot, and the voltage undershoot are reduced by the regulation band circuit. A XiTRON 2551 single-phase general purpose power analyzer is used to measure the total harmonic distortions. Fig. 6.29 shows the measured harmonic contents for different waveshapes of i_{Temp} at full load condition. A comparison is made between the harmonic components of the input current in the experimental prototype and the IEC 61000-3-2 Class D limit for 200 W output power for different waveshapes of i_{Temp}. Based on the measured results, all the measured harmonic current levels of the experimental prototype comply with the IEC 61000-3-2 Class D limit. Fig. 6.30 shows the measured PF for different waveshapes of i_{Temp}. Fig. 6.31 shows the measured overall efficiency. The prototype is tested over a power range from 20 W to 200 W. The overall efficiency at full load condition is around 96.73%.

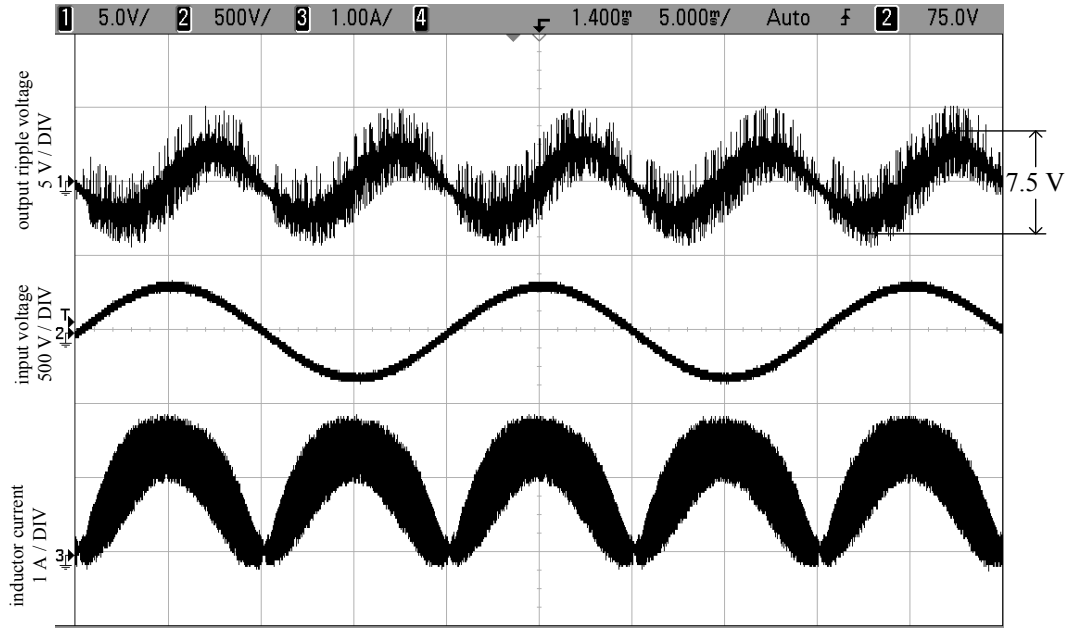


Figure 6.26: Measured waveforms at full load condition using the rectified input voltage as an inductor current reference: output ripple voltage (upper trace), input voltage (middle trace), and inductor current (lower trace). Time scale is 5 ms / DIV.

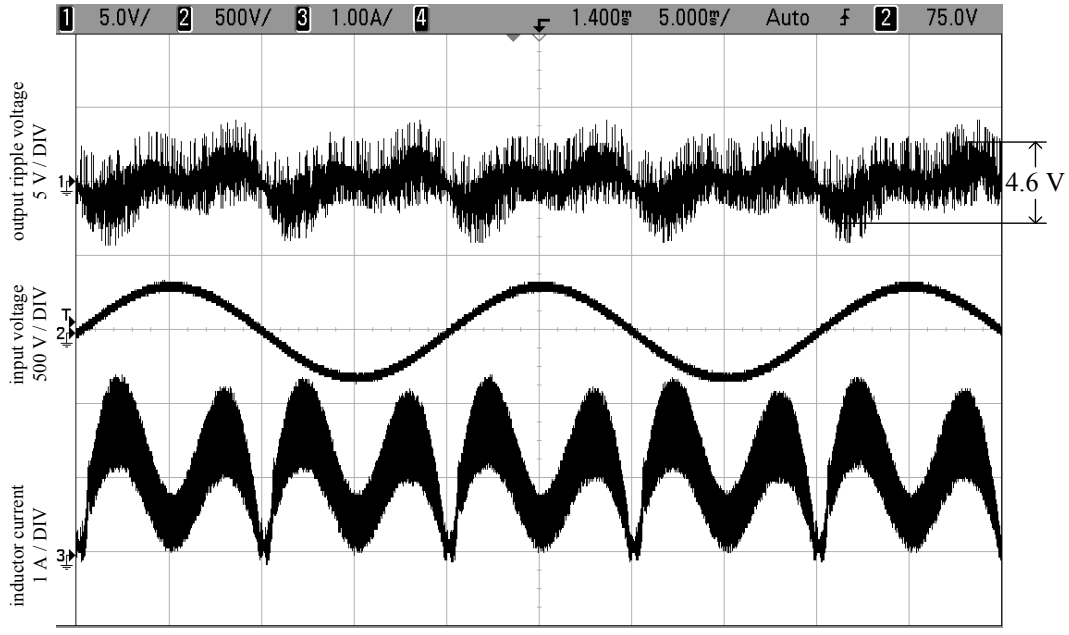
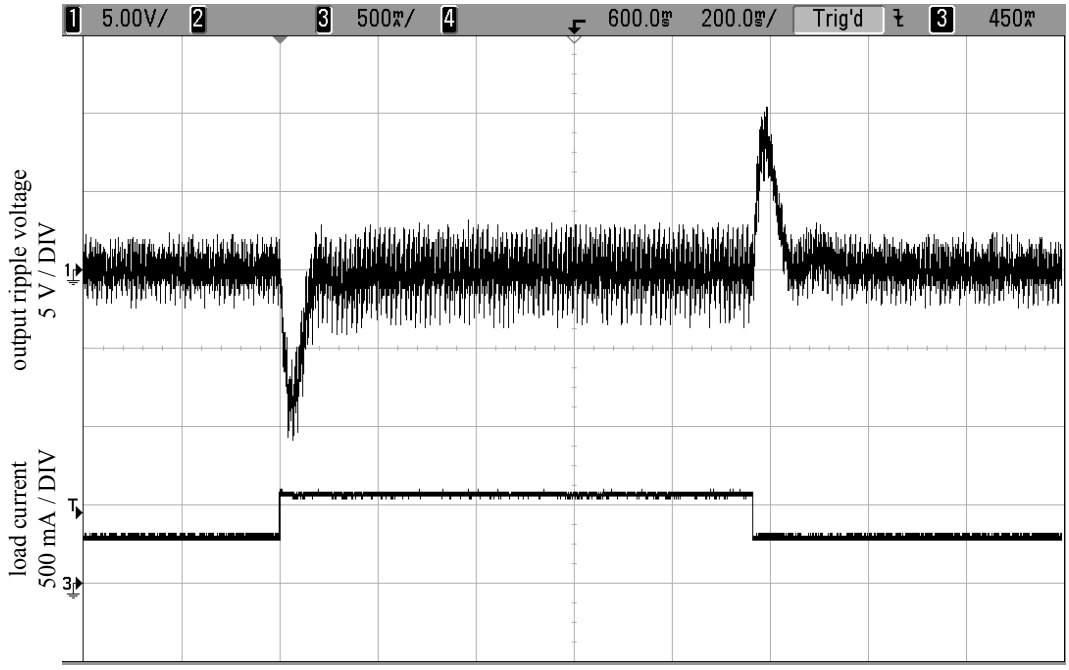
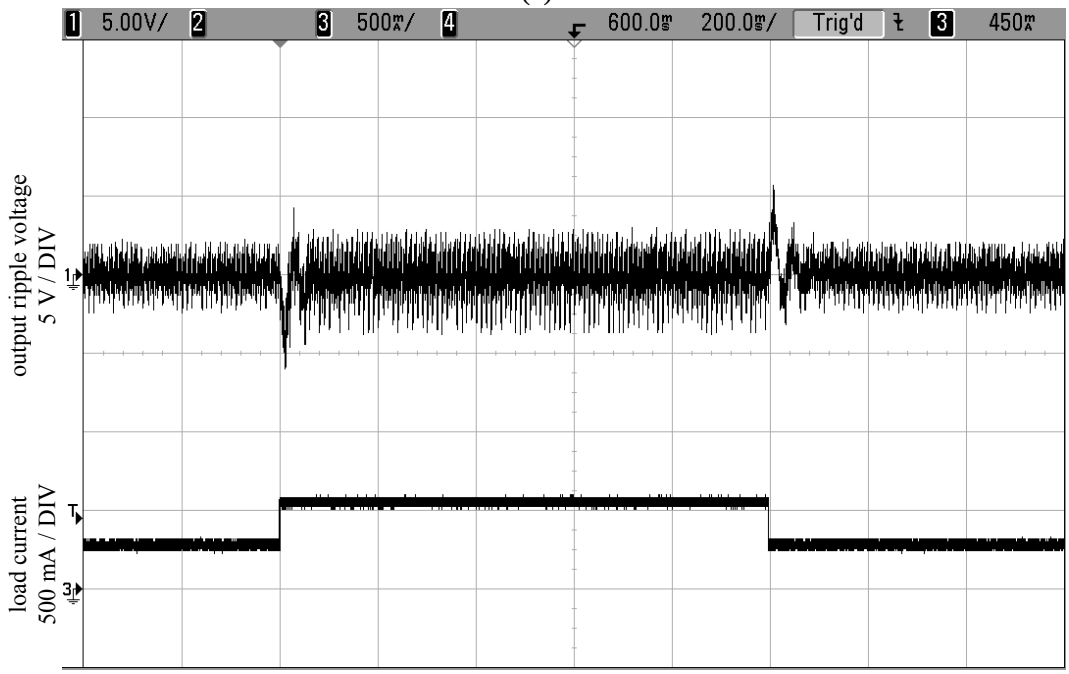


Figure 6.27: Measured waveforms at full load condition with the third harmonic i_{Temp} as an inductor current reference: output ripple voltage (upper trace), input voltage (middle trace), and inductor current (lower trace). Time scale is 5 ms / DIV.



(a)



(b)

Figure 6.28: Measured output ripple voltage (upper trace) and measured load current (lower trace): (a) without regulation band circuit and (b) with regulation band circuit. Time scale is 200 ms / DIV.

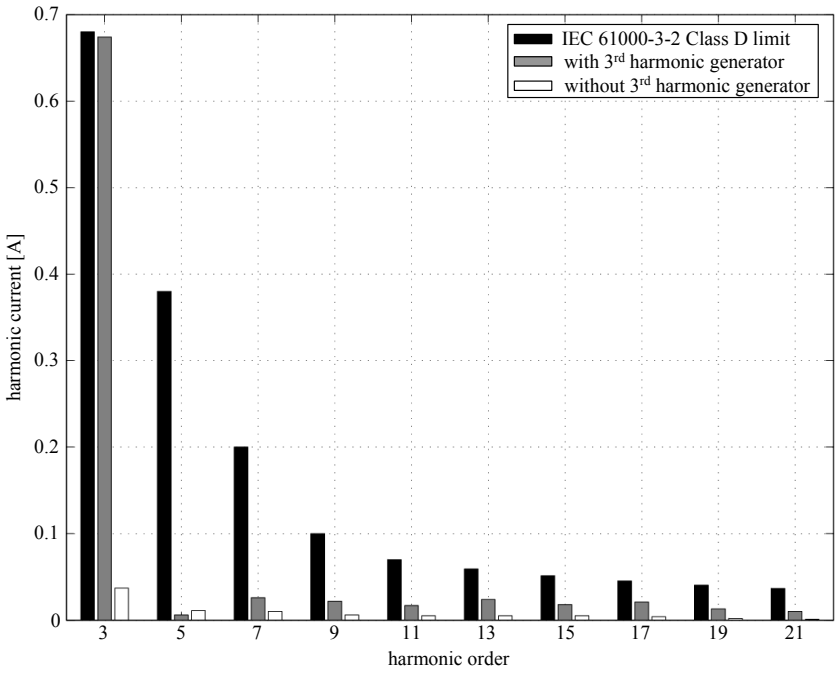


Figure 6.29: Measured harmonic current level of the experimental prototype for different waveshapes of i_{Temp}.

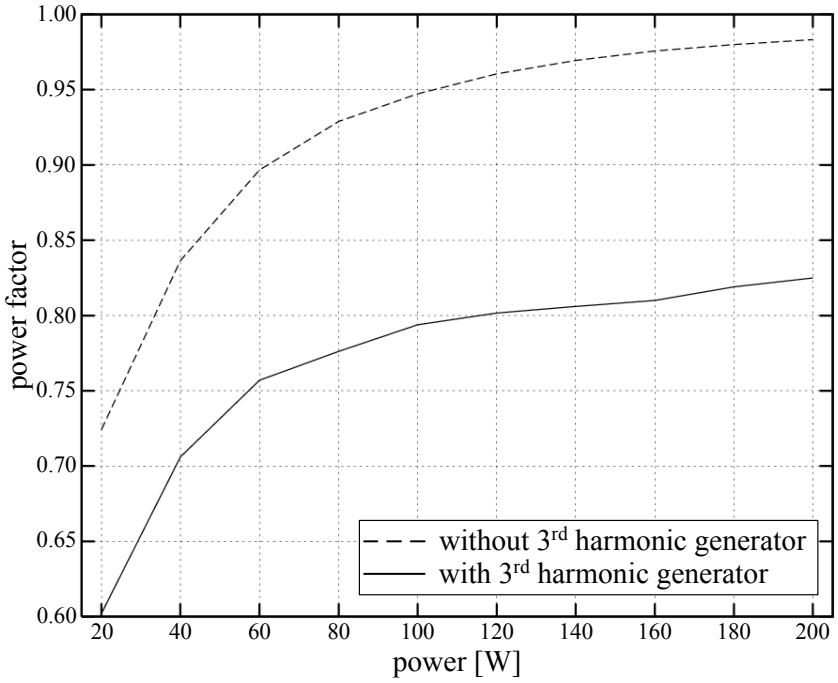


Figure 6.30: PF versus output power from 20 W to 200 W for different waveshapes of i_{Temp}.

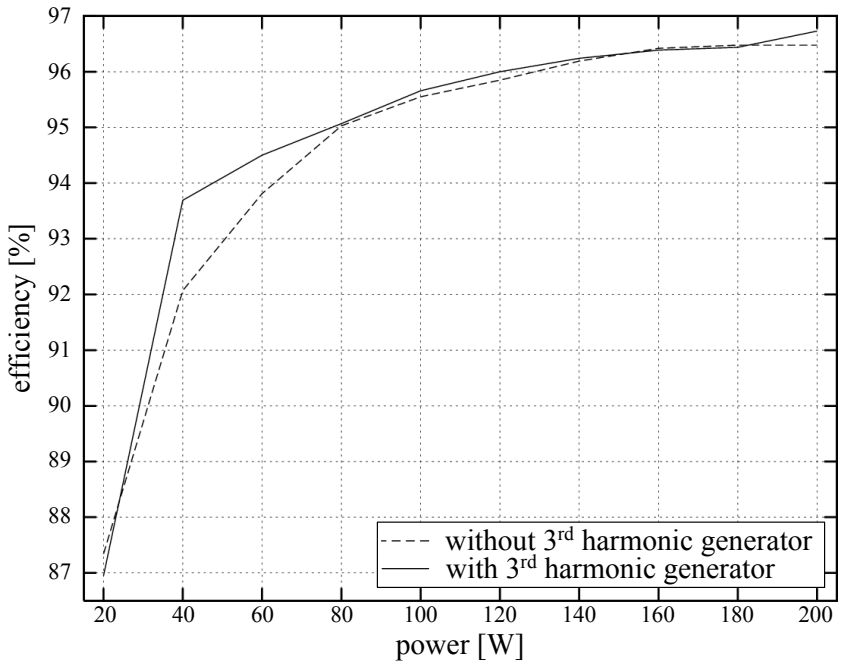


Figure 6.31: Efficiency versus output power from 20 W to 200 W of the experimental prototype with different waveshapes of i_{Temp}.

6.5 Summary

This chapter provides a detailed analysis of the output voltage ripple and the dynamic characteristics of a CCM boost pre-regulator that draws imperfect sinusoidal input current. Achieving very high power quality comes with deterioration of other performances, such as efficiency and output load voltage transient response. This chapter shows that allowing an imperfect waveshape of the input current can reduce the output load ripple voltage and improve the output load transient response of the boost pre-regulator. Using two noncascading switching regulators, it has been shown that the power conversion efficiency can be further improved by letting the boost pre-regulator draw imperfect sinusoidal input current. Experimental results show that the output ripple voltage of the prototype can be reduced by drawing imperfect sinusoidal input current and the regulation band circuit design based on the salient findings is used to accelerate the output voltage dynamics of the prototype.

Chapter 7

Conclusion and Future Research

History has shown that the harmonic current emission in three-phase power systems causes overloaded neutral cables [2], damaged distribution transformers [3], and voltage distortions [4]. Nowadays the most common sources of harmonics current are power electronic loads [12] such as personal computers, electrical appliances, electronic ballasts for compact fluorescent lamps, adjustable-speed motor drives over the entire range from watts to megawatts, battery chargers, and electronic control of a large variety of industrial loads. Therefore regulatory agencies such as the IEC and the IEEE propose their requirements [13], [14] to limit the harmonics in the line current drawn by various power electronic loads. On the other hand, efficient electricity usages have become one of the major concerns for the consumers due to energy prices. Furthermore, the United States government encouraged programs such as ENERGY STAR and 80 PULS which are designed to identify and promote energy-efficient products helping people save money and protect the environment.

To accomplish PFC for reducing harmonic current emission, there are two general methods, namely the filtering techniques and the input current controlling techniques. In terms of size, cost effectiveness, and harmonic current emission, the input current controlling techniques are more favorable at operating power levels below several kilo watts. In general, a switching regulator is composed of a pre-regulator and a voltage regulator to satisfy both low input harmonic current distortion and fast voltage regulation simultaneously. The simplest approach to construct the switching regulator is to form a chain connection between the pre-regulator and the voltage regulator. The input power of the switching regulator is processed by the pre-regulator and the voltage regulator serially, so the efficiency of this switching regulator is inevitably deteriorated. In order to satisfy the limits of the harmonic emissions and the need of the consumers, tremendous amount of research works have been concentrated to design specific noncascading switching regulators. Obviously, these noncascading switching regulators allow part of the input power to be processed by only one power stage, thereby reducing the amount of power redundantly processed by the two constituent power converters and

hence improving the overall efficiency [83], [84].

7.1 Contributions of The Thesis

The contributions of this thesis are mainly in Chapter 3 to Chapter 6. Chapter 3 and Chapter 4 give a detailed exposition on the various performance analysis, design curves, and practical information that are relevant to design of noncascading switching regulators for increasing power conversion efficiency. Chapter 5 and Chapter 6 mainly discuss the various design aspects of pre-regulators, which include the output voltage dynamics improvement and understanding the relation between the reduced output ripple voltage and the dynamic characteristics of the boost pre-regulator drawing imperfect sinusoidal input current.

Due to the potential in enhancing the overall efficiency, the noncascading switching regulators are studied in detail. Each noncascading switching regulator has its particular design considerations such as the gained efficiency, the input current harmonic, and the size of the energy storage for load voltage regulation, depending on the particular noncascading structure used. Basically, the noncascading switching regulators can be classified into three categories and each category represents a different possibility of achievable performances. The first category permits a tradeoff between the efficiency and the PFC; the second permits a tradeoff between the efficiency and the size of the energy storage element for load voltage regulation; and the third allows a tradeoff among all the achievable performances. This thesis examines achievable performances of each category of noncascading switching regulators in terms of the split factors. The split factor, k_1, directly controls the gained efficiency and the input current harmonic distortion in the Category 1 noncascading switching regulator. In other words, increasing k_1 achieves improvement in the gained efficiency but causes a deterioration in harmonic distortion of the input current. The split factor, k_2, of the Category 2 noncascading switching regulators steers the gain of efficiency and determines the static voltage of the storage element. Although the higher overall efficiency is attributed to increasing k_2, it also demands a higher values in the capacitive components to maintain the load voltage regulation. In the last category, the split factor, k_3 , influences the input current harmonic contents, controls the portion of input power processed by the pre-regulator and the voltage regulator, and the size of the energy storage element for maintaining the load voltage regulation. Increase in the overall efficiency in Category 3 switching regulators over that of the classical switching regulator is independent on the values of k_3 which affects the efficiencies of the pre-regulator and the voltage regulator. Many switching regulators are constructed by noncascading structures. Efficiency is generally improved, but often at a price. Chapter 3 has shown the relationship between the type of structure and the corresponding possible performance tradeoff.

Because only Category 2 noncascading switching regulators can provide unity PF, an evaluation of the Category 2 noncascading switching regulator is included in this thesis. This noncascading switching regulator has been discussed in the literature [95], [106]. However, the discussions are mainly focused on the efficiency view point in low power applications. Some practical design aspects for high-power applications for this noncascading switching regulator were not well recognized in the past. Specifically, the relationships between the gained efficiency, the load transient response, and the energy storage requirement has been examined in order to confirm the theoretical analysis given in Chapter 3. The noncascading switching regulator employs a current-fed full-bridge converter as the pre-regulator, and a buck-boost converter as the voltage regulator. Both regulators are operated in CCM. The advantage of CCM is that the current stress of the devices of the regulators is relatively low, and hence is more suitable for high-power applications. A 1 kW laboratory prototype has been constructed to study the performances of this Category 2 noncascading switching regulator. In particular this thesis discusses two concerns in the design of the noncascading switching regulators under load transient condition. One is the power handling of the voltage regulator. In the steady state the voltage regulator only processes part of the output power based on the split factor. However, in the positive load step change, the voltage regulator is required to support the total transient output power in a short period. Moreover, the inevitable overshoot voltage at negative load step change will be generated when the input power of the pre-regulator is close to the peak level.

Chapter 5 conducts an analog implementation to accelerate the load transient response of pre-regulators. This simple implementation involves inserting an analog notch filter between the output-voltage sensing network of the pre-regulator and the voltage control loop of the pre-regulator control circuitry. The bandwidth of the voltage control loop is greatly expanded without introducing extra input current harmonics into the pre-regulators. This approach uses operational amplifiers with R-C networks to realize the notch filter. Therefore it can be implemented into the existing pre-regulators with minor modification. The notch frequency of the filter is fixed as twice the ac mains frequency in order to attenuate the second-harmonic ripple voltage of the voltage error amplifier input. Furthermore a set of measurements on the DCM flyback pre-regulator with different values of the output capacitor using the expanded voltage control loop has been performed. Based on the measurement, the input current harmonic is deteriorated when the output capacitor is too small. However, quick response to load disturbances without distorting the input current during steady-state can be achieved. Experimental results show the benefits of this cost-effective solution in improving the load transient response of the pre-regulator.

In Chapter 6, a detailed study regarding the relationship between the reduced output ripple voltage and the different waveshapes of the input current of the CCM boost pre-regulator in steady state is conducted. The dynamic characteristics of the output voltage of the CCM boost pre-regulator that is controlled by a standard average current-mode controller are investigated. The analysis shows that

there are possible tradeoffs between the imperfect sinusoidal input current and the output voltage dynamics while the CCM boost pre-regulator satisfies the harmonic current emissions standards. Furthermore, manipulating the waveshape of the input current can further enhance the power conversion efficiency in Category 2 noncascading switching regulators. Using two noncascading switching regulators, it has been shown that the power conversion efficiency can be further improved by letting the CCM boost pre-regulator to draw imperfect sinusoidal input current. Experimental results show that the CCM boost pre-regulator drawing imperfect sinusoidal input current can reduce the output ripple voltage and can also increase the gain of voltage control loop to improve the output voltage dynamics.

7.2 Suggestions for Future Research

It has been shown in Chapter 3 and Chapter 4 that the theoretical overall efficiency of noncascading switching regulators is higher than that of cascading switching regulators. These results are based on using the same pre-regulator and voltage regulator to perform the comparison. To provide a complete comparison in terms of the overall efficiency, component-stress originated efficiency comparison should be performed. Petersen *et al.* [142] have proposed their method to focus on the comparison in the component stresses between the cascading switching regulator and some noncascading switching regulators. It is possible to extend this research further to calculate the power losses in semi-conductor devices of the cascading switching regulator and the noncascading switching regulators. Based on the study of component stresses in each noncascading switching regulator, power loss calculations of the cascading and noncascading switching regulators can be approximated. Therefore, the complete overall efficiency for different categories of noncascading switching regulators can be provided.

Although the pre-regulator becomes a necessary component in cascading switching regulators and noncascading switching regulators, it is still worthwhile to investigate a new model to simulate the pre-regulator responds under certain specified conditions. The new model should take into consideration the rectified input voltage parameters. In the past research works [128], [129], the rectified input voltage is averaged to a dc level. Therefore, the resulting model cannot accurately represent the pre-regulator behavior over a quarter of the frequency of the rectified input voltage. This disadvantage causes the difficulty in designing the voltage control loop of the pre-regulator. This problem becomes more serious in the re-design of the expanded voltage control loop for improving the load transient response.

Appendix A

Sixteen Configurations

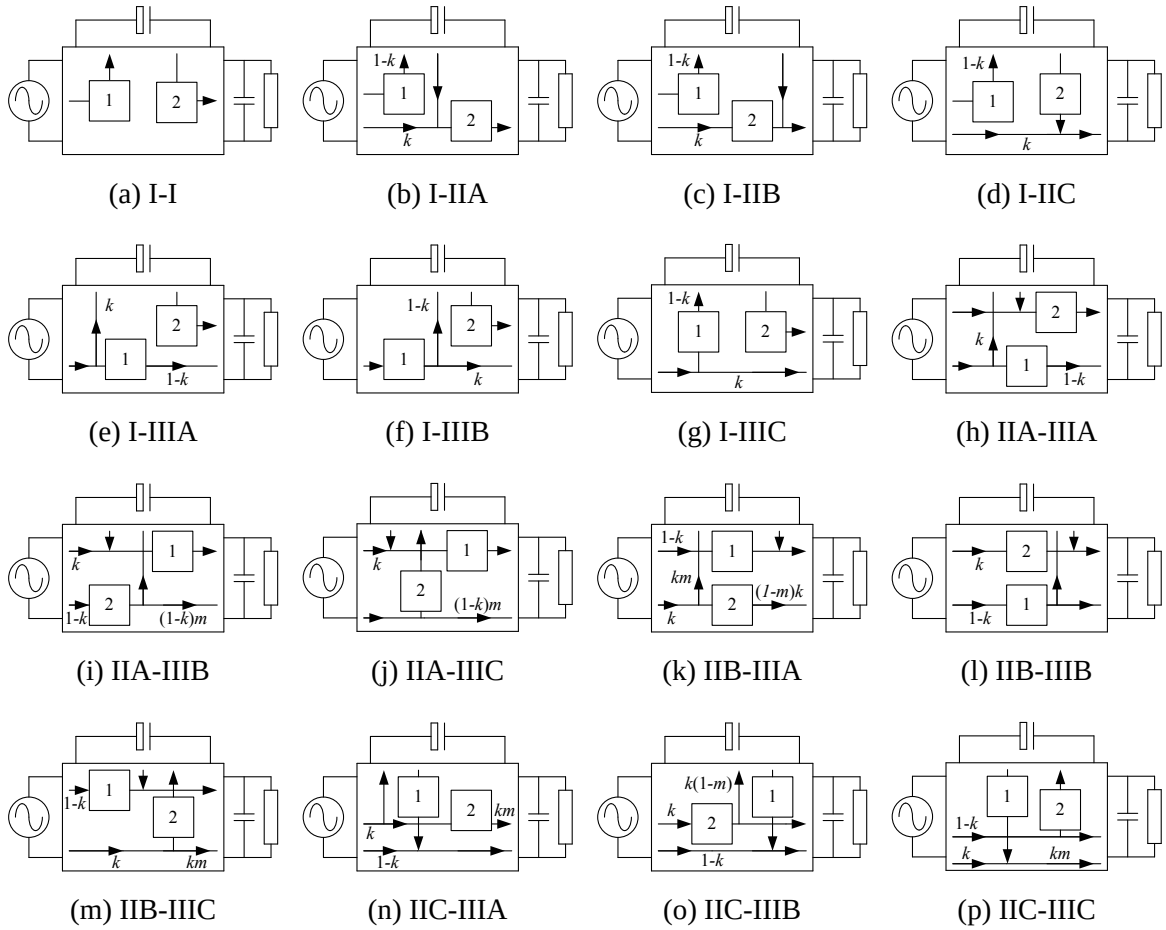


Figure A.1: Sixteen configurations of switching regulator in terms of power flow diagram. Solid square boxes denote simple converters.

Table A.1: Theoretical efficiencies of sixteen configurations.

Config.	Overall efficiency	
I-I	$\eta_1\eta_2$	
I-IIA	$\eta_1\eta_2 + k\eta_2(1-\eta_1)$	where $k\eta_2(1-\eta_1) > 0$
I-IIB	$(1-k)\eta_1 + k\eta_2$	where $(1-k)\eta_1 + k\eta_2 > \eta_1\eta_2$
I-IIC	$\eta_1\eta_2 + k(1-\eta_1\eta_2)$	where $k(1-\eta_1\eta_2) > 0$
I-IIIA	$(1-k)\eta_1 + k\eta_2$	same as I-IIB
I-IIIB	$\eta_1\eta_2 + k\eta_1(1-\eta_2)$	where $k\eta_1(1-\eta_2) > 0$
I-IIIC	$\eta_1\eta_2 + k(1-\eta_1\eta_2)$	same as I-IIC
IIA-IIIA	$(1-k)\eta_1 + k\eta_2$	same as I-IIB
IIA-IIIB	$\eta_1\eta_2 + m(1-k)\eta_2(1-\eta_1)$ $+k\eta_1(1-\eta_2)$	where $m(1-k)\eta_2(1-\eta_1)$ $+k\eta_1(1-\eta_2) > 0$
IIA-IIIC	$\eta_1\eta_2 + m(1-k)(1-\eta_1\eta_2)$ $+k\eta_1(1-\eta_2)$	where $m(1-k)(1-\eta_1\eta_2)$ $+k\eta_1(1-\eta_2) > 0$
IIB-IIIA	$\eta_1\eta_2 + \eta_1\eta_2[\frac{k_m}{\eta_1}(\frac{1}{\eta_2}-1)$ $+(\frac{(1-k)\eta_1+k\eta_2}{\eta_1\eta_2}-1)]$	where $(1-k)\eta_1$ $+k\eta_2 > \eta_1\eta_2 > 0$
IIB-IIIB	$(1-k)\eta_1 + k\eta_2$	same as I-IIB
IIB-IIIC	$\eta_1\eta_2 + \eta_1\eta_2[\frac{k_m}{\eta_1}(\frac{1}{\eta_2}-1)$ $+(\frac{(1-k)\eta_1+k\eta_2}{\eta_1\eta_2}-1)]$	same as IIB-IIIA
IIC-IIIA	$\eta_1\eta_2 + \eta_1\eta_2[\frac{(1-k)\eta^{'}+k\eta_1\eta_2}{(\eta_1\eta_2)\eta^{'}}-1]$	where $\eta^{'} = \frac{\eta_1\eta_2}{(1-m)\eta_1+m\eta_2}$ and $(1-k)\eta^{'} + k\eta_1\eta_2 > \eta_1\eta_2\eta^{'}$
IIC-IIIB	$\eta_1\eta_2 + \eta_1\eta_2[k+$ $(\frac{(1-k)\eta_2+k\eta^{''}}{\eta_2\eta^{''}}-1)]$	where $\eta^{''} = \eta_1\eta_2$ and $(1-k)\eta_2 + k\eta^{''} > \eta_2\eta^{''}$
IIC-IIIC	$\eta_1\eta_2 + (1-km)(1-\eta_1\eta_2)$	where $(1-km)(1-\eta_1\eta_2) > 0$
η_1 = efficiency of the square-box-1 converter η_2 = efficiency of the square-box-2 converter k and m are the ratio of the power splitting in two different power paths. the value of k and m must between 0 to 1 (i.e. $0 \leq k \leq 1$ and $0 \leq m \leq 1$)		

Appendix B

Supplementary Measured Results

Table B.1: Load transient properties of the DCM PFC pre-regulator with the expanded voltage control loop at different values of output capacitor.

Output capacitance	Load change from 50 W to 100 W	Load change from 100 W to 50 W	P.F. and THD% at 100 W output power
4500 μF	ΔT_{st}=100 ms, $\Delta V_{\mathrm{o\ pp}}$=5.5 V	ΔT_{st}=130 ms, $\Delta V_{\mathrm{o\ pp}}$=5.0 V	0.993, 4.77%
3000 μF	ΔT_{st}=80 ms, $\Delta V_{\mathrm{o\ pp}}$=6.0 V	ΔT_{st}=110 ms, $\Delta V_{\mathrm{o\ pp}}$=5.0 V	0.990, 6.99%
2400 μF	ΔT_{st}=70 ms, $\Delta V_{\mathrm{o\ pp}}$=6.0 V	ΔT_{st}=90 ms, $\Delta V_{\mathrm{o\ pp}}$=6.0 V	0.989, 7.34%
2000 μF	ΔT_{st}=65 ms, $\Delta V_{\mathrm{o\ pp}}$=7.0 V	ΔT_{st}=65 ms, $\Delta V_{\mathrm{o\ pp}}$=4.5 V	0.988, 7.77%
1640 μF	ΔT_{st}=40 ms, $\Delta V_{\mathrm{o\ pp}}$=8.75 V	ΔT_{st}=50 ms, $\Delta V_{\mathrm{o\ pp}}$=7.5 V	0.988, 7.89%
1360 μF	ΔT_{st}=40 ms, $\Delta V_{\mathrm{o\ pp}}$=8.75 V	ΔT_{st}=40 ms, $\Delta V_{\mathrm{o\ pp}}$=7.5 V	0.987, 8.31%
940 μF	ΔT_{st}=25 ms, $\Delta V_{\mathrm{o\ pp}}$=12.5 V	ΔT_{st}=30 ms, $\Delta V_{\mathrm{o\ pp}}$=8.75 V	0.986, 8.71%
660 μF	ΔT_{st}=25 ms, $\Delta V_{\mathrm{o\ pp}}$=15.75 V	ΔT_{st}=25 ms, $\Delta V_{\mathrm{o\ pp}}$=11.25 V	0.982, 10.23%
440 μF	ΔT_{st}=20 ms, $\Delta V_{\mathrm{o\ pp}}$=17.5 V	ΔT_{st}=25 ms, $\Delta V_{\mathrm{o\ pp}}$=12.25 V	0.973, 13.75%

Table B.2: Load transient properties of the DCM PFC pre-regulator with the standard voltage control loop at different values of output capacitor.

Output capacitance	Load change from 50 W to 100 W	Load change from 100 W to 50 W	P.F. and THD% at 100 W output power
4500 μF	$\Delta T_{\rm st}$=300 ms, $\Delta V_{\rm o\ pp}$=7.0 V	$\Delta T_{\rm st}$=4500 ms, $\Delta V_{\rm o\ pp}$=7.5 V	0.993, 4.57%
3000 μF	$\Delta T_{\rm st}$=200 ms, $\Delta V_{\rm o\ pp}$=8.75 V	$\Delta T_{\rm st}$=260 ms, $\Delta V_{\rm o\ pp}$=8.75 V	0.992, 5.00%
2400 μF	$\Delta T_{\rm st}$=200 ms, $\Delta V_{\rm o\ pp}$=10.0 V	$\Delta T_{\rm st}$=220 ms, $\Delta V_{\rm o\ pp}$=10.0 V	0.992, 5.02%
2000 μF	$\Delta T_{\rm st}$=200 ms, $\Delta V_{\rm o\ pp}$=11.0 V	$\Delta T_{\rm st}$=170 ms, $\Delta V_{\rm o\ pp}$=10.0 V	0.992, 5.10%
1640 μF	$\Delta T_{\rm st}$=200 ms, $\Delta V_{\rm o\ pp}$=11.5 V	$\Delta T_{\rm st}$=170 ms, $\Delta V_{\rm o\ pp}$=11.5 V	0.991, 5.45%
1360 μF	$\Delta T_{\rm st}$=180 ms, $\Delta V_{\rm o\ pp}$=11.87 V	$\Delta T_{\rm st}$=200 ms, $\Delta V_{\rm o\ pp}$=11.25 V	0.990, 5.88%
940 μF	$\Delta T_{\rm st}$=180 ms, $\Delta V_{\rm o\ pp}$=15.0 V	$\Delta T_{\rm st}$=180 ms, $\Delta V_{\rm o\ pp}$=12.5 V	0.991, 5.63%
660 μF	$\Delta T_{\rm st}$=160 ms, $\Delta V_{\rm o\ pp}$=15.0 V	$\Delta T_{\rm st}$=160 ms, $\Delta V_{\rm o\ pp}$=15.0 V	0.992, 5.20%
440 μF	$\Delta T_{\rm st}$=160 ms, $\Delta V_{\rm o\ pp}$=20 V	$\Delta T_{\rm st}$=160 ms, $\Delta V_{\rm o\ pp}$=17.5 V	0.991, 5.56%

Appendix C

Pspice Netlist and MATLAB Code

Table C.1: Complete PSPICE netlist of an exact CCM boost converter with average current-mode control

```
     **Remark: input voltage source**
01   Vs ns 0 DC 0 sin (0 311.1269837 50)
02   Rvs ns 0 1Meg
03   Bin nsp nsn v=abs(v(ns))
     **Remark: imperfect sinusoidal voltage template**
04   Vs1 ns1 0 DC 0 sin (0 311.1269837 50)
05   Vs3 ns3 ns1 0 DC 0 sin (0 232.7229838 150)
06   Vs5 ns5 ns3 0 DC 0 sin (0 130.0510792 250)
07   Vs7 ns7 ns5 0 DC 0 sin (0 68.44793642 350)
08   Rvsh ns7 0 1Meg
09   Bhd nsp1 nsn v=abs(v(ns7))
     **Remark: CCM boost converter**
10   Cin nsp nsn 0.1u
11   L nsp nl 1m ic=0
12   S nl 0 nd sw1
13   D nl nv1 Dout
14   C nv1 0 220u ic=380
15   Rs nsn 0 0.25
     **Remark: voltage error loop**
16   R2 nv1 nean 510k
17   R3 nean 0 4.08k
```

```
C1 nean nea 100n
R1 nean nea 160k
Vref neap 0 3.0V
Bea nea 0 v=1e6*(v(neap)-v(nean))
**Remark: multiplier for sinusoidal current**
Bmul 0 nmul i=2*v(npwl)*(v(nsp)-v(nsn))*v(nea)/(620000*15.6025)
**Remark: current error loop**
Rca1 nsn nmul 3.9k
Rca2 0 ncan 3.9k
Rcaf ncan nca3 40k
Cca1 nca3 nca 680p
Ccaf ncan nca 68p
Bca nca 0 v=1e6*(v(nmul)-v(ncan))
**Remark: multiplier for imperfect sinusoidal current**
Bmul 0 nmul i=2*v(npwl)*(v(nsp1)-v(nsn))*v(nea)/(620000*15.6025)
**Remark: ramp signal**
Vramp nramp 0 DC 0 pulse(1.1 5.4 0 9.805u 0.1u 0.1u 10.005u)
**Remark: duty signal**
Bd nd 0 v=10*u(1.0e6*(v(nca)-v(nramp)))
**Remark: soft start**
vpwl npwl 0 dc 1 pwl 0 0.5 2.5e-3 0.5 2.5e-3 0.5 10e-3 1
**Remark: loading**
Ro1 nv1 0 1444
Ro2 nv1 nr2 1444
S2 nr2 0 np 0 sw2
Vpulse np 0 PULSE(0 10 0 1us 1us 0.75s 1.2s)
.model dout D Cjo=23pF vj=1.8v
.model sw1 sw vt=6V vh=2V Ron=0.1
.model sw2 sw vt=6V vh=2V Ron=0.001
.tran 2u 450ms 400ms 1u uic
.option method=gear
.end
.control
shell time/t
run shell time/t
plot i(L1) xcompress 50
plot v(nv1) xcompress 50
.endc
```

Table C.2: Complete MATLAB program for calculating the output voltage dynamics of the pre-regulator based on (6.18) and (6.19).

```
01  function yp=Ve(t, y)
    %Remark: Input peak voltage
02  V=220*sqrt(2);
    %Remark: Loading resistor
03  R=1444;
    %Remark: Output capacitor
04  C=220e-6;
05  R1=160e3;
06  R2=510e3;
07  R3=4.08e3;
08  C1=0.10e-6;
    %Remark: Angular frequency
09  w=2*pi*50;
    %Remark: Output voltage
10  vo=y(1);
    %Remark: Output of voltage error amplifier
11  ver=y(2);
    %Remark: Switching for loading network
12  if t>0
13  u=1; end
14  if t>0.75
15  u=0; end
16  if t>1.2
17  u=1; end
    %Remark: vo calculation for sinusoidal input curren
18  yp1=V*ver*(1-cos(2*w*t))/(2*vo*C)-vo/(R*C)-u*vo/(R*C);t
    %Remark: vo calculation for imperfect sinusoidal input current
19  yp1=[ver*(sin(w*t)+V*3.4e-3*sin(3*w*t)/sqrt(2)+V*1.9e-3*sin(5*w*t)/sqrt(2)
    +V*1e-3*sin(7*w*t)/sqrt(2))]*V*sin(w*t)/(vo*C)-vo/(R*C)-u*vo/(R*C);
    %Remark: ver calculation
20  yp2=Vref*(R1*R2+R2*R3+R1*R3)/(R1*R2*R3*C1)-vo/(R2*C1)-ver/(R1*C1);
    %Remark: Numerical ODE solver
21  options=odeset('RelTol', 2e-9, 'AbsTol', [1e-10 1e-10]);
22  [t, y]=ode45(@Ve, [0 1.5], [380;1.27], options);
23  plot(t, y);
```

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