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INVESTIGATION OF METAL-INDUCED CRYSTALLIZATION OF SILICON THIN FILMS AND SILICON BASED NANOSTRUCTURES

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Investigation of Metal-induced Crystallization of Silicon Thin Films and Silicon Based Nanostructures

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A thesis submitted in partial fulfillment of the requirements for the degree of Master of Philosophy

August 2011

THE HONG KONG POLYTECHNIC UNIVERSITY
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To my beloved parents …

I. Abstract

The main focus of this thesis is on low temperature processing of polycrystalline Silicon (Si) thin films and Si nanorods. It has also been extended to induce the growth of more complicated nanostructures, such as superlattice and nanodots. The fabrication techniques for all of them, however, are based on catalytic metal assisted growth. As you read through this thesis, you will find that we start off with preparation of two dimensional (2-D) structure, then 1-D structure like nanorods, and finally nanodots, which are of 0-D geometry.

Owing to the world energy crisis and the hazard of global warming due to carbon emission, it is meaningful and highly desirable to develop renewable energy technologies. Si based photovoltaic, by far, has been considered as one of the most promising candidates for replacing the conventional energy sources, like fuel and oil. Nevertheless, solar photovoltaic devices based on bulk crystalline Si (c-Si) is too expensive for large scale solar energy harvesting. An alternative is to use polycrystalline Si (poly-Si) thin films. The present most mature chemical vapor deposition (CVD) technique of fabricating Si thin film solar cells involves annealing the films at high temperature of above 900 ^{o}C. For this reason, there is less degree of freedom on choosing cheap substrate, such as soda-lime glass. With currently fast growth of thin film technology, we aim to fabricate poly-Si thin film with large grain on inexpensive and transparent soda-lime glass substrate at low temperature, say 450 ^{o}C.

Herein, we have adopted metal induced or metal mediate Si crystallization method to fabricate poly-Si on glass substrate. It is compatible to use Aluminum (Al) because of its low cost and being a standard electronic material, which can act as p-type dopant. The Al

catalytic layer is deposited at room temperature under high vacuum by electron beam (ebeam) evaporation. Without breaking the vacuum, the Si was subsequently deposited at

450 ^{o}C. During this process, it is very likely and highly reproducible to obtain poly-Si with grain size of more than 5 μm. Post annealing at the same temperature was used to improve the crystallinity of Si. The physical mechanism has been investigated and studied based on various characterization techniques, such as X-ray diffraction, micro-Raman spectroscopy, Field Emission Scanning Electron Microscopy and Transmission Electron Microscopy. The as-prepared poly-Si thin film can be used as a seed layer for the homo-epitaxial growth of a thick poly-Si absorbing layer. As a consequence, the IV characteristics of a solar cell with a lateral structure of glass/ITO/poly-Si (p^+ type)/poly-Si (p type)/a-Si (n-type)/Al are also presented.

It has been well known that Si, as an indirect bandgap semiconductor material, exhibiting relatively low absorption capability in the solar spectrum. In order to enhance the light absorption it is vitally important to introduce micro- or nano- scale structures on Si thin films. In this respect, Si nanorods fabricated by vapor-liquid-solid (VLS) method on (111) oriented Si wafer has been studied in this project. The initial growth involves deposition of a very thin Au layer coating on Si wafer. Upon thermally treated at 500 ^{o}C, this thin Au layer turns into numerous nano-sized droplets uniformly distributed on the Si wafer surfaces. During the subsequent deposition of Si, the substrate temperature is raised to 600 ^{o}C. The continue supply of Si atoms leads to the nucleation and crystallization of Si at the site of the Au droplet. The cap which is made of Si-Au eutectic guides the growth direction of Si nanorods (SiNRs). From the experiment, we found all the SiNRs are well aligned vertically.

Apart from the poly-Si thin films fabrication and Si nanorods growth, long range order Si twinning superlattice based on the interdiffusion of Al-Si has been demonstrated. This

promising discovery differs from the conventional epitaxial growth of superlattice structure with two well lattice-matched materials or the molecular beam epitaxial growth of twinning superlattice by inserting boron (B) layer in between. It opens up a new method in dealing with single crystalline phase superlattice of a single material on amorphous substrate, such as glass.

The final part of this thesis is devoted to studies of the most popular 2-D graphene. A complex nonlithographic patterning technique will be demonstrated. Large area and uniform crystalline Si nanodots (c-SiNDs) fabricated on CVD-made single layer graphene is expected to be useful for future nanoelectronic applications.

II. List of Publications

Journal Papers

- Kai Wang and Kin Hung Wong, ***Low temperature processing of a large grain polycrystalline silicon thin film on soda-lime glass***, IOP Semi. Sci. & Tech. 26, 095031 (2011).
- K. Wang, G. Tai, K. H. Wong, S. P. Lau and W. Guo, ***Ni induced few-layer graphene growth at low temperature by pulsed laser deposition***, AIP Advances **1**, 022141 (2011).
- Guo'an Tai, Kai Wang, Jun Yin, Zhenhua Sun, Sheung Mei Ng, Jianxin Zhou, Chi Wah Leung, Kin Hung Wong, Shu Ping Lau and Wanlin Guo, ***Nonlithographic fabrication of Ni-induced crystalline silicon nanodots on graphene for nanoelectronic application***, J. Phys. Chem. C, 116, 532 (2011).
- J.Z. Xin, K.C. Hui, K. Wang, H.L.W. Chan, D.H.C. Ong and C.W. Leung, ***Thermal Tuning of Surface Plasmon Resonance: Ag Gratings on Barium Strontium Titanate Thin Films***, Appl. Phys. A 107, 101 (2012).

Conference Papers

- Kai Wang and Kin Hung Wong, ***Growth of large grain polycrystalline silicon thin film on soda-lime glass at low temperature for solar cell applications***, MRS proceedings, 1321, mrss11-1321-a06-12 (2011).
- Kai Wang and Kin Hung Wong, ***Raman spectroscopic study of metal induced graphene fabricated by pulsed laser deposition***, International Conference on Materials for Advanced technology (ICMAT) E-PO3-27 (2011).
- K. Wang and K. H. Wong, ***Vapor-liquid-solid growth of silicon nanowires fabrication by electron beam evaporation*, **ICMAT 11-A-3391, (2011).
- Guoan Tai, Kai Wang, Shu Ping Lau and Wanlin Guo, ***Temperature and pH effect on deoxygenation of exfoliated graphite oxide in aqueous solution***, International Conference on Materials for Advanced technology (ICMAT) E-PO3-23 (2011).
- G. Tai, K. Wang, S. P. Lau and W. Guo, ***ZnO nanowire arrays: controllable preparation and effect of annealing temperature on optical properties***, ICMAT 11-A-2830, (2011).
- Jianzhou Xin, K. C. Hui, Kai Wang, H. L. W. Chan, H. C. Ong and Chi Wah Leung, ***Surface plasmon resonance of Ag gratings on barium strontium titanate thin films***, International Conference on Materials for Advanced technology (ICMAT) S-PO2-28 (2011).

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IV. Table of Contents

I. Abstract ii

II. List of Publications v

III. Acknowledgements vi

IV. Table of Contents viii

Chapter 1 Introduction and Literature Reviews .... - 1 -
1.1 Overview of Current Photovoltaics .... - 1 -
1.2 Silicon Technology .... - 3 -
1.2.1 The History of Silicon .... - 3 -
1.2.2 Current Issues in Si Based Photovoltaics .... - 5 -
1.2.3 Amorphous Silicon .... - 6 -
1.2.4 Microcrystalline Silicon .... - 7 -
1.2.5 Polycrystalline Silicon .... - 8 -
1.3 Realization of Metal-induced Crystallization Method .... - 9 -
1.4 The Development of Si Nanowires .... - 12 -
1.4.1 Chemical Vapor Deposition .... - 14 -
1.4.2 Annealing in Reactive Atmosphere .... - 15 -
1.4.3 Evaporation of SiO2 .... - 15 -
1.4.4 Molecular Beam Epitaxial (MBE) Growth .... - 16 -
1.4.5 Laser Ablation .... - 17 -
1.4.6 Solution Based Technique .... - 17 -
References .... - 18 -

Chapter 2 Fabrication and Characterization Methods of Poly-Si Thin Films and Si Nanowires .... - 23 -
2.1 Vacuum system - Electron Beam Evaporation System .... - 23 -
2.2 Vacuum System - Pulsed Laser Deposition System .... - 25 -
2.3 Raman Spectroscopy .... - 27 -
2.4 X-ray Diffraction .... - 29 -
2.5 Transmission Electron Microscopy .... - 30 -
2.6 Atomic Force Microscopy .... - 32 -
2.7 Hall Measurement .... - 33 -
References .... - 36 -

Chapter 3 Metal Induced Crystallization of Silicon .... - 38-

3.1 Introduction ....- 38-
3.2 Experimental procedures ....- 39-
3.3 Results and discussion ....- 41-
3.4 Summary ....- 58-
References ....- 58-

Chapter 4 Si Nanowires and Nanorods Growth by Electron Beam Evaporation ....- 59-
4.1 Introduction ....- 59-
4.2 Experimental procedures ....- 61-
4.3 Results and discussion ....- 63-
4.4 Summary ....- 72-
References ....- 73-

Chapter 5 Silicon Twinning Superlattice and c-Silicon Nanodots for Future Nanoelectronic Applications ....- 75-
5.1 Silicon Twinning Superlattice ....- 75-
5.1.1 Introduction ....- 75-
5.1.2 Experimental procedures ....- 78-
5.1.3 Results and Discussion ....- 78-
5.1.4 Summary ....- 83-
5.2 Crystalline Silicon Nanodots ....- 83-
5.2.1 Introduction ....- 83-
5.2.2 Experimental Procedures ....- 84-
5.2.3 Results and Discussion ....- 86-
5.2.4 Summary ....- 91-
References ....- 95-

Chapter 6 Conclusions and Perspectives ....- 97-

Chapter 1 Introduction and Literature Reviews

1.1 Overview of Current Photovoltaics

By definition, solar photovoltaic (PV) is a method of direct converting solar radiation into electrical power. It is considered that the sun can provide energy to earth for many billion years. By comparison natural energy resources, such as oil, coal and natural gas are finite and will be exhausted in a few terms of years. Thus solar PV has been considered as one of the most promising ways for future electrical energy supply. A way of extracting solar energy relies on device, called solar cell or PVs or PV cell. Both solar cell and light emitting diode (LED) are solid state devices with opposite functions in electricity production and injection. Solar cell is the one that absorbs solar radiation and generates electricity.

According to the materials used for solar cell constructions, they are often classified into two groups; one representing a relatively young and new rising group is the organic solar cells, while the other is inorganic solar cells, which by far more reliable and has been used for some time already. For the former one, numerous recent studies have indicated that, in terms of efficiency, stability and longevity, the organic based photonic devices still have a long way to go.[1-4] On the contrary; inorganic solar cells, in particular for those based on Si, have been in commercial uses for over thirty years. Up to date, numerous researches are still engaging in maximizing the efficiencies of the inorganic solar cells. Meanwhile, some governments have launched unprecedented plans to offer subsidies for

utility-scale photovoltaic projects. For instance, China produced solar modules with an output of 13 GW in 2010, which represents about half of the global PV production.

Despite the stability issue, the reduction of the cost for solar cell production is also important and keeps accelerating the development of photovoltaic technology in the recent decade. Indeed, the percentage of photovoltaic applications in daily life still accounts for small at present by comparing with the ones of the conventional energy sources. For promotion of wide applications of photovoltaic devices in the near future, one of the key issues is how to balance the production cost and the output value. Moreover, the lifetime and performance of the solar cells should long last and reliable. Even at present, the mainstream of photovoltaic technology is still based on the somewhat expensive crystalline silicon (c-Si) and polycrystalline silicon (poly-Si) bulk wafers. This is a robust and proven technology.[5-8] Regarding cost issue, the processing of bulk Si consumes a lot of energy and causes serious environmental pollutions. These directly contradict the spirit of renewable energy and are not environmentally friendly. With current fast development of nanotechnology and thin film fabrication techniques, Si thin films solar cells have gained particular attention and being developed on various substrates. Large scale and inexpensive production of poly-Si thin film solar cells are expected.[6]

1.2 Silicon Technology

1.2.1 The History of Silicon

c-Si is the most common tetravalent metalloid. The tetravalence describes the state of an atom with four electrons available for covalent chemical bonding in its valence.[9-11] As we can see from figure 1.1(a), each Si atom is bonded with four identical Si atoms. By kept adding Si atoms but following the same atomically structural configuration, figure 1.1(b), (c) and (d) show the exactly same c-Si structure. The spatial variations are due to different viewing angles in atomic lattice space. According to the electronic configuration of the electron shells, Si is placed at the fourth group in the periodic table. The Metalloid means the general physical and chemical properties of c-Si are neither the ones of metals nor nonmetals. Such element is classified as semiconductor. Sometimes, semimetal and near metal are used synonymously.

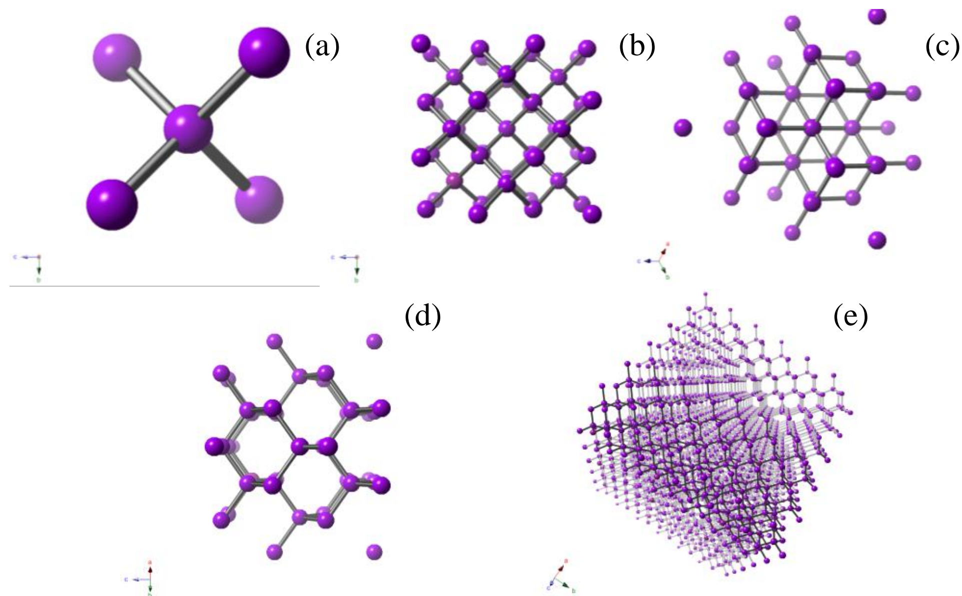

Figure 1.1 The virtualization of Si-Si bonding structures (a) One Si atom forms tetravalent bonds with other four Si atoms. Viewing from (b) Si (100) crystalline plane, (c) Si (111) crystalline plane, (d) Si (002) crystalline place. (e) Si molecules. Pictures made by *crytal maker software*.

Indeed, Si is the eighth most common element in the universe by mass, but it rarely exists in the form of a pure element in nature. It is widely distributed in dusts, sands, planetoids and plants in various kinds of forms such as silicon dioxide (silica) or silicates. In Earth's crust, Si is the second most abundant element after oxygen, making up 27.7% of the crust by mass. Because c-Si is vastly used for electronic and photonic devices and plays an important role in semiconductor industries, the requirements of obtaining high quality c-Si are crucially important in achievement of high performances of devices.

In general, the first step towards Si wafer manufacture is the preparation of raw silicon materials.[12, 13] As it is shown in figure 1.2(a), the raw Si material possess a gray color and metallic luster. By taking this raw Si material and placing it inside a crucible, it requires very high temperature (~1600 ^{o}C) to reach the melting point of Si (figure 1.2(b)). A pure Si seed crystal is placed into the molten Si bath as it is shown in figure 1.2(c). This crystal will be pulled out slowly as it rotates. Such single c-Si ingot making method is well known as the Czochralski (CZ) technique. In figure 1.2(d), some pure Si cylinders with different sizes were achieved and they are called ingots. For integrated circuits (ICs) usage and other electronic applications, the Si ingots are sliced into very thin wafers (figure 1.2(e)). This is usually done with a diamond saw. After this, the Si wafers experience some necessary etching, thickness sorting, flatness checking and polishing processes in order to ensure the quality. Si wafer has been commercialized for decades.

Nowadays, it is easily to see every corner of research labs leaves its shadow. Global photonic and electronic companies consume unprecedented amount of Si wafers annually.

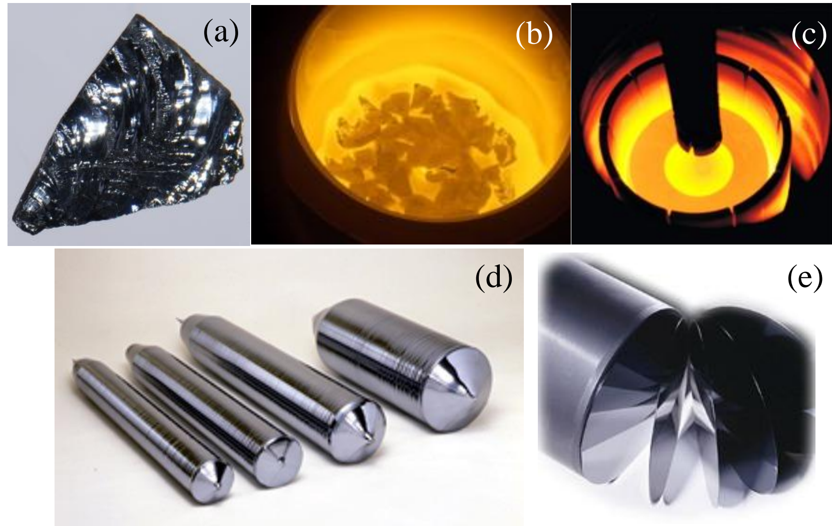

Figure 1.2 (a) Raw Si material. (b) molten Si in a crucible. (c) Si ingot growth via a Si seed crystal. (d) Si ingots with different sizes. (d) After polishing, the ingot is sliced into wafers.
Pictures come from http://www.surfacenet.de/html/czochralski__cz__puller.html.

1.2.2 Current Issues in Si Based Photovoltaics

Evidently, photovoltaic industry is booming with growth rate of more than 30% per year over the last decade. This explosive growth is driven by market development programs and rapidly increasing fossil fuel prices.[14] Si, by far, is still dominating the photovoltaic market although significant progresses have been made by cadmium telluride (CdTe) and copper indium diselenide (CIS). The main challenge on Si based photovoltaics is the reduction of the cost/W for the photovoltaic modules.[15,16] The first generation of Si bulk wafer based photovoltaics has already reached its mature stage. Further reduction of the cost/W is unlikely. By contrast, Si thin films based photovoltaics have drawn particular attention due to the ability to fabricate the solar cell on inexpensive foreign substrates and

to greatly reduce semiconductor material consumption. Thus, the following part of this section will give a brief review on amorphous, microcrystalline and polycrystalline Si materials for Si thin film solar cells. Table 1.1 also lists some important properties for Si films with different forms according to their grain sizes.[9]

1.2.3 Amorphous Silicon

By comparing with the diamond crystalline structure of Si, the amorphous silicon (a-Si) is a non-crystalline allotropic form of Si. It can be deposited onto various substrates ranging from glass to ceramic at room temperature. It offers some unique capabilities for diverse applications in electronics and optoelectronics. Although the accumulation of Si atoms is random, and owing to the presence of the Si dangling bonds, hydrogenated a-Si (a-Si: H) is quite often utilized to alleviate the degradation problem. The a-Si: H deposited by plasma-enhanced chemical vapor deposition (PECVD) at about 200 ^{o}C has been established in the 1970s.[17] It has been reported that this technology possessed tremendous desirable properties for cost efficient Si PVs, including a high optical absorption coefficient which gives rise of building up very thin absorber layer (thickness of 300nm or less).[18-20] It also led to the deposition of Si onto rigid and even flexible substrates at affordable low temperature, and monolithic series interconnection of the individual cells.

	nc-Si	μc-Si	poly-Si
Average grain size	1nm – 50nm	0.01μm – 1μm	0.5μm – 1mm
Growth temp. (^{o}C)	150<T_g<300°C	250<T_g<500°C	T_g>500°C
Electron mobility (cm^2/Vs)	1-10	10-50	50-500
Hole mobility (cm^2/Vs)	0.01-0.1	0.1-10	10-200
Minority carrier diffusion length	<0.1μm	<1μm	1-20μm
Applications	NMOS, solar cells	CMOS, TFTs, solar cells	PMOS, CMOS, TFTs, Sensors, solar cells

Table 1.1 Classification of Si films according to grain size.[9]

The only reason why a-Si: H has not been able to conquer a significant share of the global photovoltaic market is the low stable average efficiency. One factor behind this is the Staebler Wronski Effect (SWE), which refers to light induced degradation in the a-Si: H. The defect density of a-Si: H increases with light exposure.[20] As a result, it causes an increase in the recombination of charge carriers and consequently leads to the reduction in the sunlight to electricity conversion efficiency. However, research is still continuing in finding ways to solve this problem and the scope of using a-Si: H for large scale energy generation remains.

1.2.4 Microcrystalline Silicon

Microcrystalline Si (μc-Si) sometimes is known as nanocrystalline Si (nc-Si), is a form of porous Si. It consists of both crystalline and amorphous phases. The nc-Si contains many small grains which are embedded in the amorphous phase. This is in direct contrast with poly-Si, which contains c-Si gains in the micro-meter range. Those c-Si grains are well defined by grain boundaries. Because the major difference is solely from the size of the c-

Si grains, it is more appropriate to use nc-Si rather than μc-Si. Apparently, the term, nc-Si, refers to a range of Si materials around the transition regions from amorphous to microcrystalline phase within the Si thin film. The amount of crystalline volume can be estimated from Raman spectroscopy. Because a particular attraction for a-Si is low temperature process, this saves time and money in the factory. In the early 1990s, researchers at the University of Neuchatel successfully fabricated hydrogenated μc-Si (μc-Si:H) by very high frequency PECVD technique.[21] Importantly, they found the solar cell performance was stable even under light soaking conditions. This gave hope to further investigation in this material. By the end of the 1990s, researchers have demonstrated that low temperature fabrication of μc-Si:H solar cell on glass could reach a stable efficiency of up to 8.5%. However, owing to the low deposition rate (<40 nm/min) of the μc-Si:H and technical challenges with the development of industrial-scale very high frequency PECVD, thin film solar cells based on single junction μc-Si seems to be difficult at present.[22-24]

1.2.5 Polycrystalline Silicon

Apart from single c-Si, poly-Si, perhaps, is the most reliable c-Si material in the Si family. Poly-Si differs from single c-Si is solely because it is made of numerous Si crystals with certain gain sizes. Usually, the poly-Si grains are randomly oriented. The grain boundary between each pair of adjacent c-Si grains makes the charge carriers in poly-Si less mobile. However, by comparing with a-Si, it shows much greater stability under electric field and

light induced stress. In the thin film technology, it is difficult to directly fabricate single c-Si on an arbitrary substrate unless both crystallization temperature of Si (~1300 ^{o}C) and suitable single crystal substrate are brought into fabrication. Thus, one feasible way of using c-Si in thin film technology on cheap substrate such as ordinary transparent glass is to fabricate poly-Si.[25, 26]

1.3 Realization of Metal-induced Crystallization Method

The formation of high quality poly-Si thin films on foreign substrates is one of the most challenging tasks in processing Si thin film solar cells, thin film field effect transistors (FETs), image sensors and liquid crystal displays. In recent years, many methods have been developed. Some typical and applicable methods include solid phase crystallization (SPC), excimer laser annealing (ELA) and metal-induced crystallization (MIC).[27-40] The SPC makes deposited a-Si directly transfer into poly-Si upon high temperature annealing. Crytalline phase nucleates and grows until the entire film is transferred into poly-Si. However, the annealing temperature can be as high as 1000 ^{o}C and the annealing time can be as long as 60 hours. Although industrial scale can be obtained, such high temperature exceeds thermal affordability of some substrates such as glass. In addition, long time annealing raises the fabrication cost. Although ELA yields high quality poly-Si thin films, this technique involves very expensive external facility, and high cost is needed for equipment maintenance. Moreover, the uniformity over large area of the thin film is not satisfactory. It has demonstrated that conventionally pulsed excimer laser produces poly-Si with maximum grain size of 1μm. Such small grain, as a consequence,

will definitely influence charge transportations within poly-Si thin films. As we can see from figure 1.3, both (a) and (b) show the energy band diagrams of p- and n- type Si respectively. Figure 1.3 (c) shows the simulated picture for the formation of Si-Si bond at the Si grain boundary.[41]

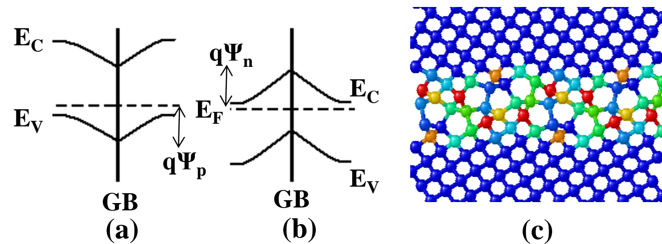

Figure 1.3 Band diagram at a grain boundary in (a) p-type and (b) n type Si. The Fermi level is pinned around midgap. (c) Simulated Si-Si bond formation at the grain boundary.
Simulated picture comes from http://www.csm.ornl.gov/SC98/mat2.html.

The symmetric depletion regions formed at the grain boundaries hinder current transportation by majority charge carriers. This is the reason why the charge carrier mobility in poly-Si with very small grains is lower than in the single c-Si. Furthermore, the interfacial charges attract minority charge carriers so that increasing the recombination of electron and hole pair. This leads to the reduction of the open circuit voltage. Although poly-Si can be made by both SPC and ELA methods, no significant breakthrough has been achieved for poly-Si thin films with uniform and several μm in grain size.

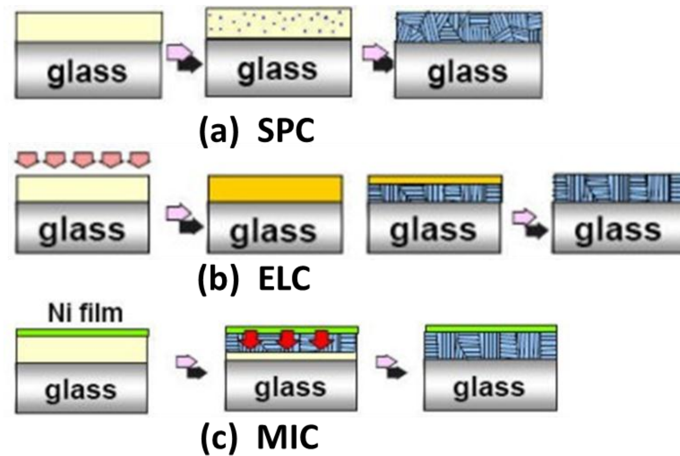

Figure 1.4. Schematic diagrams for (a) Solid phase crystallization method. (b) Excimer laser crystallization. (c) Metal-induced crystallization.
Picture is available from http://www.neopoly.net/polytech.htm

Recently, MIC has gained particular attention due to its potential usage in obtaining large poly-Si thin films at reduced temperature.[42, 43] The processing time can be made as short as a few hours and the grain size can reach several μm. All these desirable outcomes make it as a promising technique for poly-Si thin film solar cell production. In this method, catalytic metals, such as Au, Al, Sb, In, and Ag play an important role.[44-47] These metals form metal-Si eutectics according to conditions illustrated by their binary phase diagrams. However, other metals, like Pd, Pt, Ti and Ni usually form silicides with Si.[48-51] For MIC of Si, Al is the most favorite catalytic metal due to its low cost. It is a standard electronic material with an advantage to acts as an acceptor. Researchers even directly used the Al layer as a top or bottom electrodes after the MIC fabrication process.[52] One challenging issue is to fabricate high quality poly-Si thin films without metal contaminations. Otherwise, poly-Si will lose its semiconductor properties and is not applicable for solar cell applications. Although many studies have indicated that poly-Si

thin film can be achieved by this method, a thoroughly study and characterization of the quality of the poly-Si thin films produced by MIC are still necessary. Moreover, during the poly-Si formation process, a significant reaction between Si and metal takes place. Even up to now, the physical mechanism is still not very clear.

1.4 The Development of Si Nanowires

Although single c-Si, poly-Si and a-Si thin film have gained dramatic attractions because of their low cost, abundance, non-toxicity and mature processing techniques, their capabilities of light absorption decrease significantly with the reduction of film thicknesses. Owing to the indirect bandgaps of single c-Si and poly-Si thin films, light absorption needs to be substantially enhanced for effective sun light-charge conversion.[53-56] This is the reason why bulk c-Si can reach higher efficiency. However, unwanted defects can be introduced if the thin film thickness is within a range of several micrometers, especially for the poly-Si, charge scattering at the grain boundaries gives rise to the decrease in the charge mobility and the charge diffusion length. As a result, improving light absorption is crucial for Si thin film solar cells. In recent years, among some well developed methods, such as zig-zag microstructures and anti-reflective layer, Si nanostructures, such as nanowires, nanorods and nanowhiskers, have been demonstrated by both experiments and theories for excellent light trapping and efficient charge transportations properties.[53] When incident light experiences multi-reflection within Si nanowire arrays, this tends to increase the light optical path without varying

film thickness. As such nanostructures approach 1-D, The charge carriers generated by light absorption can pass through each individual nanowire without concerning too much about charge collision. In other words, charge carrier ballistic transportation can be realized.

To the best of our knowledge, the first paper about Si wires growth should go back to 1957.[57] The authors reported on the successful synthesis of Si whiskers with (111) crystalline orientation. Up to date, the term, whisker, is most commonly used for filamentary growth of crystalline nanowire. In additional to whisker and nanowire, nanorod is sometimes used and it can be distinguished from nanowire based on the different aspect ratio. In the 1960s, seven years after the first report about nanowires, Wagner and Ellis published their highly impacted research work on Si nanowires growth by vapor-liquid-solid (VLS) method.[58] This method has been extensively studied and developed for more than half century. Even though the fabrication method has been modified these days in order to meet some purposes in nanostructure modification, the foundations are still established on the most famous VLS method.[59-68] Before we describe various types of synthesis techniques based on VLS method, let's briefly review the definition of VLS method. Accordingly, VLS refers to double stage transitions, which is from vapor to liquid and then to solid phase. This is how Si is transferred from original source to form nanowires. However, the catalytic metal plays an important role including eutectic formation and determination of the growth direction throughout the entire nanowire formation. In the VLS process, the metal is always in the liquid phase unless

the growth stops and the growth temperature is reduced below the eutectic temperature of metal-Si. The catalytic metal is in a droplet form and the radius of the droplet (*R*) is slightly larger than the one of Si naowire (*r*). This can be understood referring to the equilibrium equation for the relationship between R and r during VLS growth[69]

$$R = \sqrt{\frac{1}{\left(1-\left(\frac{\sigma_{1s}}{\sigma_1}\right)^2\right)}} \qquad \text{Equation 1.1}$$

in which, σ_{1s} and σ_1 are the surface tension of the liquid catalyst and the interface tension of the liquid/solid interface respectively. One remarkable thing for the VLS method is that the diameter of the Si nanowires can be as small as a few nanometers or as large as hundreds of nanometers.

In the followings, we summarize some well developed Si nanowires fabrication techniques based on the VLS method.

1.4.1 Chemical Vapor Deposition

In Chemical vapor deposition (CVD), a volatile gaseous Si precursor, such as silane (SiH_4) or silicon tetrachloride ($SiCl_4$) serves as the Si source.[70-73] It is transported onto the surface of substrate at which the precursor reacts and cracks into its constituents. CVD allows epitaxial growth of Si nanowires with growth velocity varying from about 10^{-2} to

10^3 nm per min. The growth rate depends on the Si source being used and the temperature of substrate. CVD also offers broad ways of controllable growth of Si nanowires in length and diameter. The property of Si nanowires can be modified such as doping with different materials in order to meet certain requirements. One disadvantage of CVD for Si nanowires growth is unidirectional growth for diameters which are smaller than 50 nm. But this problem can be solved when a template such as anodic aluminum oxide (AAO) is used.

1.4.2 Annealing in Reactive Atmosphere

This idea has already been seen in 1960s for Si nanowhisker growth.[74, 75] A Si substrate which is contaminated with metal impurity is exposed to reactive gases like hydrogen, iodine, or bromine. The substrate is heated up to 900 ^{o}C for Si nanowhisker growth. At such temperature, the gases can react with solid Si, locally generating Si compounds like SiH_4, SiI_2, or SiB_2. Similar to CVD, the catalytic metal assists the growth of Si nanowhisker or nanowires. For some reasons, this method can be considered as the predecessor of nanowires growth by CVD method.

1.4.3 Evaporation of SiO2

This is a cost-efficient way of producing Si nanowires on large-scale. The basic requirements are inert gas supply, small amount of SiO granulate and a tube furnace. The

key for the Si nanowires growth is the temperature gradient from about 1350 °C to 900 °C along the tube furnace. SiO is evaporated from the hot end of the tube and flows with inert gaseous stream to the relatively cooler end of the tube, where the SiO undergoes a disproportionate reaction into Si and SiO_2. This gives a final production of Si nanowires.[76-78]

1.4.4 Molecular Beam Epitaxial (MBE) Growth

MBE is originally used for epitaxial layer by layer growth in ultra-high vacuum. The film thickness can be well controlled and seen from integrated high reflective energy electron diffraction (RHEED).[79,80] For Si nanowires growth, a solid high purity Si source is heated until Si evaporates. The vaporized Si directionally aims at the heating substrate, at which the Si atoms are adsorbed and crystallized. Different from CVD, there are no precursors pass by the Si substrate and form metal-Si alloy. Therefore, this method can not be treated as the conventional VLS method. In MBE, two fluxes govern the nanowires growth. First, the direct flux of Si from Si source; and, the second one is the diffusing Si adatoms from the substrate surface. The produced Si nanowirs are usually grown on (111) oriented c-Si surface. Furthermore, MBE offers excellent controllability in terms of the incoming flux, such that doped nanowires and heterostructure can be achieved by changing the evaporation source in-situ.

1.4.5 Laser Ablation

The Si nanowires produced by laser ablation differs from the one made by MBE. One can produces large quantities of Si nanowires with large aspect ratio. During the fabrication process, high energy laser bombards the surface of the Si containing metal target.[81] The target is placed in a tube furnace and purged with an inert gas. The laser ablated Si material is cooled by collision with inert gas molecules, and the atoms condensed into liquid droplet with the same composition as the target. The Si nanowires start to grow once the supersaturation status reaches. There are two major advantages associated with this technique. First, there is no substrate requirement, and the composition of the resulting Si nanowires can be varied by changing the composition ratio of Si-catalytic metal.

1.4.6 Solution Based Technique

The solution based techniques are applied for high-yield Si nanowires production. One method uses highly pressurized supercritical organic fluids enriched with liquid Si precursor, such as diphenylsilane and metal catalytic particles. At reaction temperature above the eutectic temperature of Si-metal, the Si precursor decomposes and forms an alloy with metal. Analogous with VLS method, the Si nanowires start to grow once the supersaturation status of the Si-metal eutectic is satisfied. Crystalline Si nanowires with diameter as low as 5 nm but several micrometer in length has been achieved by this method.[82, 83]

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Chapter 2 Fabrication and Characterization Methods of Poly-Si Thin Films and Si Nanowires

2.1 Vacuum system – Electron Beam Evaporation System

Modern thin film fabrication techniques are broadly classified as both chemical vapor deposition (CVD) and physical vapor deposition (PVD).[1-6] Electron beam (Ebeam) evaporation system is a form of PVD. A schematic Ebeam system is displayed in figure 2.1(a). The thin film processing is carried out inside a stainless steal chamber under high vacuum (~10^{-6} Torr). The major component of the system is an electron gun (e-gun) pocket which usually locates at the bottom of the chamber (figure 2.1(b)). A substrate holder is designed vertically facing the e-gun. Therefore, it gives a result of bottom to up approach for the thin film deposition. Electron beams can be generated by thermionic emission, field electron emission or the anodic arc method. In our system, when the accelerating voltage is set to be 8 kV to 10 kV, the Ebeams are produced based on thermionic emission by a charged tungsten (W) filament. The W filament here performs as a cathode while the crucible of the e-gun pocket is anode. A magnetic field is also used to bend the electron beams trajectories. The details of the e-gun design can be seen from figure 2.1(c). Figure 2.1(d) and (e) show the photographic images of various Ebeam liners used for the deposition of different materials. Different materials require suitable liners in order to avoid contaminations and chemical interactions. For both Si and Al, glassy coated graphite liner will do. The liner sits in the copper made crucible. Water

cooling is throughout the e-gun pocket. Such fascinating design can greatly reduce the film contamination problem by comparing with filament heating thermal evaporation technique. During the film deposition, the bombardment of the focusing high energy electron beams on materials leads to the phase change from solid to liquid, and then vapor phase.

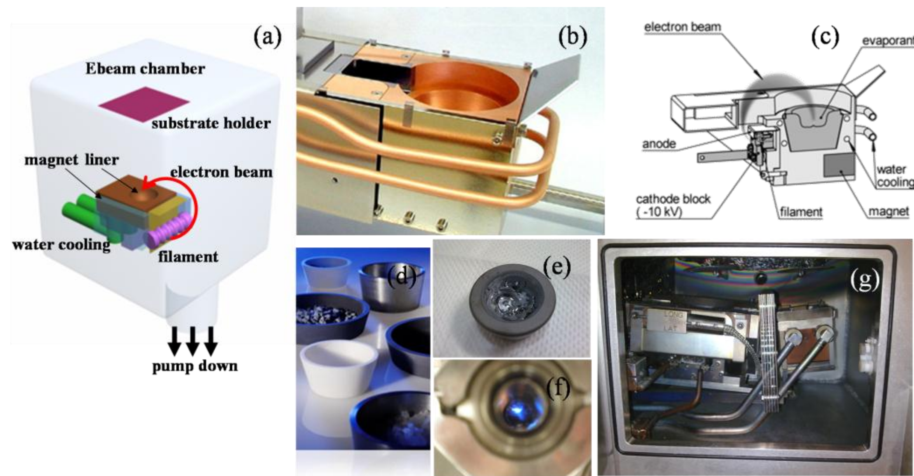

Figure 2.1 (a) 3-D drawing of Ebeam evaporation system. (b) e-gun crucible. (c) Details of e-gun configuration. (d) Different types of liners are Ebeam system. (e) Si target placed inside glassy coated graphite liner. (f) Electron beams viewed from viewing port. (g) E-gun chamber which contains a large and a small e-guns.

Figure 2.1(f) shows the photographic image, from which we can see the electron beams focused onto Si. Approximately 85% of the kinetic energy of the electron beams will be converted into thermal energy during the bombardment. Some of the incident electron energy is lost in the excitation of X-ray and secondary emission. As the materials reach the vapor phase, they vaporized and condensed onto substrate to form thin films. For

most of the Ebeam evaporation systems, the substrate holder is always equipped with a heater and substrate rotator. This can further improve the functionalities of the Ebeam evaporation system. Figure 5 (g) shows the e-gun chamber in our lab. Both the large and small e-guns are well shielded. Based on the Ebeam system design, it performs very well in dealing with semiconductor and metal materials. For micro- and nano- electronic devices fabrications, Ebeam system is excellent in making conductive electrodes.

2.2 Vacuum System – Pulsed Laser Deposition System

Pulsed laser deposition (PLD) is another form of PVD. The system design is somewhat different from other PVD systems because an external laser source is required.[7-10] The useful range of laser wavelengths for thin films growth by PLD lie between 200nm and 400nm since most materials exhibit strong absorption in this spectral region. Within this range, there are few commercially available laser sources capable of easily delivering the high energy densities (>1 J/cm^2), in relatively large areas (10 mm^2 or larger), which are required for PLD works. A homogenous uniform laser output is also important for high quality thin films fabrications. Most of PLD work done these days uses excimer lasers, in which the lasing medium is a mixture of some reactive gases such as krypton (Kr), fluorine (F) and neon (Ne). More details about how lasing occurs can be found from reference 7. An experimental setup for a typical PLD system is shown in figure 2.2(a). The vacuum chamber can be placed direct facing the output laser pulse or be set at certain angles. For the latter case, a UV reflecting mirror is necessary. Inside the PLD chamber, a

target and a substrate holder are align on the same line but are separated by a distance of 3 cm to 4 cm. Such distance range has been well experimentally confirmed for efficient laser ablation. When the incident focusing laser beam bombards the rotating target, the rise of the localized temperature causes vaporization of the material. It is in a feature of plasma plume with high energetic ions, electrons, atoms and molecules, clusters, particulates and molten globules. For an ideal PLD based thin films fabrication, we hope that the clusters, particulates and molten globules can be avoided. The film growths depend on several parameters, such as laser fluence, laser repetition rate, substrate temperature, and vacuum level.

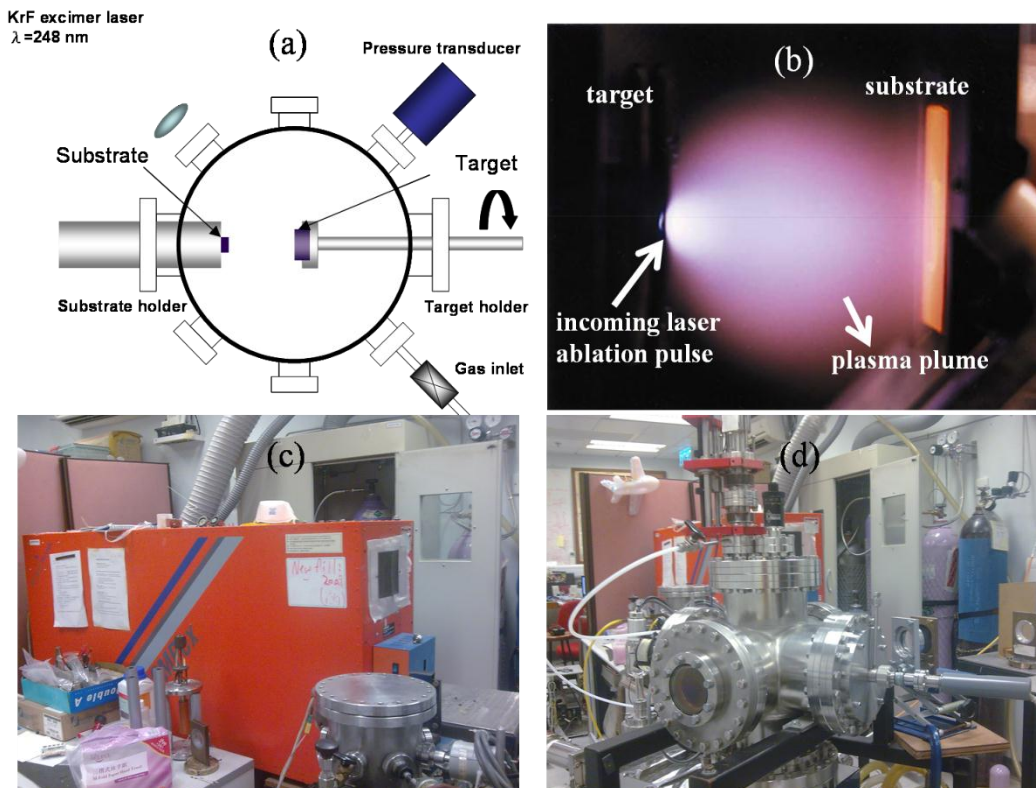

Figure 2.2 (a) A schematic illustration of PLD system. (b) Plasma generation during laser ablation process. (b) The Excimer laser with wavelength of 248 nm. (d) PLD system in our lab.

2.3 Raman Spectroscopy

Raman spectroscopy plays an important role in modern spectroscopy and it has become a standard tool for solid state physics, chemistry and materials science.[11] It is the inelastic scattering of light quanta or photons by some excitation of a material.[12] Conventionally, the excitation sources are coherent lasers ranging from near infrared (near-IR) to ultra-violet (UV). The term Raman scattering is now widely accepted to denote light scattering from acoustic and optical phonons respectively. Briefly speaking, in Raman spectroscopy, a sample is illuminated with a laser beam. Both elastic and inelastic scattered lights are collected with a lens and then send through a monochromator. Due to elastic Rayleigh scattering, the wavelengths close to the laser line are filtered out. The rest of the inelastic light is dispersed onto a detector.

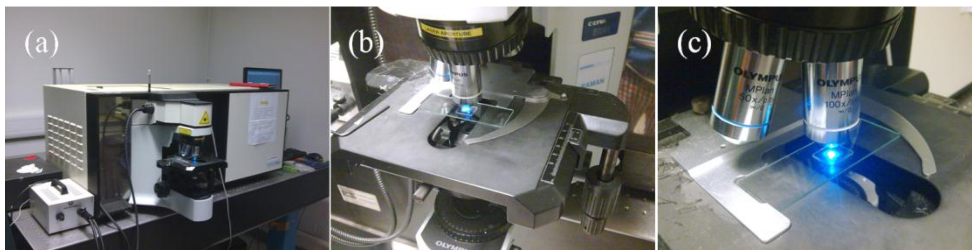

Figure 2.3 (a) The feature of Raman spectrometer. (b) and (c) are the sample is examined by Raman spectroscopic technique.

Physically, the incident light is an electromagnetic (EM) wave which is oscillatory. Owing to materials, themselves, contain vibrational modes. The interaction between incident light and matter thus gives the polarization

$$P = \varepsilon_0 \chi E \qquad \text{Equation 2.1}$$

where, ε_0 is permittivity in free space, χ is the dielectric susceptibility of the material and E is the electric field of the incident light with angular frequency ω_i and wave vector k_i. More complicated expression for the time dependent polarization (p) can be derived by introducing electric field of incident light and the expression for second-rank tensor χ. Here, we extract only the term represents the first-order Raman scattering which is as

$$p = \frac{1}{2}\varepsilon_o \left(\frac{\partial\chi(k_i\omega_i)}{\partial u}\right)_{u=0} u(q,\omega_{ph})E(k_i,\omega_i) \times \{\cos[(k_i+q)\cdot r-(\omega_i+\omega_{ph})t]+\cos[(k_i-q)\cdot r-(\omega_i-\omega_{ph})\cdot t]\}$$ Equation 2.2

This part of the induced polarization contains cosine terms oscillating at sum and difference of frequencies which refer to anti-Stokes and Stokes Raman shifts. Furthermore, there is a transfer of momentum between the incident photons (momentum $\hbar k_i$) and the phonon mode (crystal momentum $\hbar q$) so that the scattered photons have energy and momentum given by the following expressions

$$\omega_S = \omega_i \pm \omega_{ph}$$ Equation 2.3

$$k_S = k_i \pm q$$ Equation 2.4

The above two equations are as required for the conservation of energy and momentum. For a particular material, the phonon dispersion relationship can be investigated by observing the values of ω_{ph} and q in a Raman spectroscopic experiment. Typically, the photon momenta are small on the scale of the Brillouin zone and so q is small. Thus at least at pure bulk semiconductor, only phonons near the Brillouin zone centre are probed.

2.4 X-ray Diffraction

X-ray diffraction (XRD) is a well known characterization technique mainly for determining crystalline orientations of materials.[13, 14] The types of materials cover from inorganic to organic materials and from metals to semiconductors. The basic principal of XRD technique is established on Bragg's law, in which the diffracted angles and the crystalline lattice planes of the materials should obey the following relationship

$$2 \cdot d_{hkl} \cdot \sin\theta_{hkl} = \lambda \qquad \text{Equation 2.5}$$

For thin films samples, XRD is a very useful characterization technique to precisely determine the lattice constants. The measurements are derived from $2\theta - \theta$ scans. The resultant XRD spectra, diffracted angles $2\theta - \theta$ versus diffraction intensities, provide information about lattice constants, lattice mismatch between heterostructure films, and film with substrate. This is indicative of the presence of strain and stress. Moreover, rocking curve measurement is a way of looking at the crystalline quality of the films. It can be done by doing a θ scan at a fixed 2θ angle. The measured full width at half maximum (FWHM) of the XRD bands are inversely proportional to the dislocation density of in the films. Furthermore, XRD technique also frequently appears at measuring superlattice structure. Glancing angle incidence can be applied when the film thicknesses are superior thin.

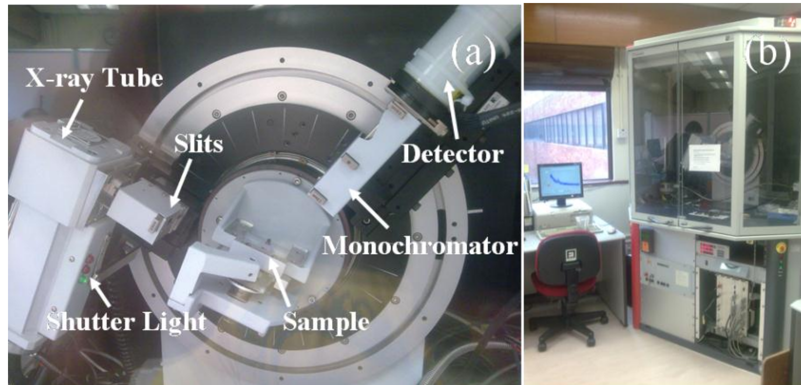

Figure 2.4 (a) XRD configuration. (b) A view of entire XRD system.

2.5 Transmission Electron Microscopy

Transmission electron microscopy (TEM) is a powerful tool for characterizing nanometric scale-structured materials.[15] Modern TEM is now able to perform characterizations down to the atomic scale.[16-18] The main reason for the use of the electron microscopy resides in its superior resolution. The very small wavelength of the electrons, depending on the acceleration voltage (100 to 1500 kV), varies in the range of 4 to 0.3 pm. It is many orders of magnitude smaller than the visible light wavelength (350 nm to 700 nm). Thus, many good reasons of using TEM in studying materials, for example, TEM produces wide range of signals which give many details on the examined samples. Among these, information can be obtained on the surface and lateral morphological features, crystal lattice parameter, the crystal structure, presence of ordering or different phases, and defect distribution; more importantly, electron diffraction pattern gives contributions on the crystallinity and the impurity phase analysis.

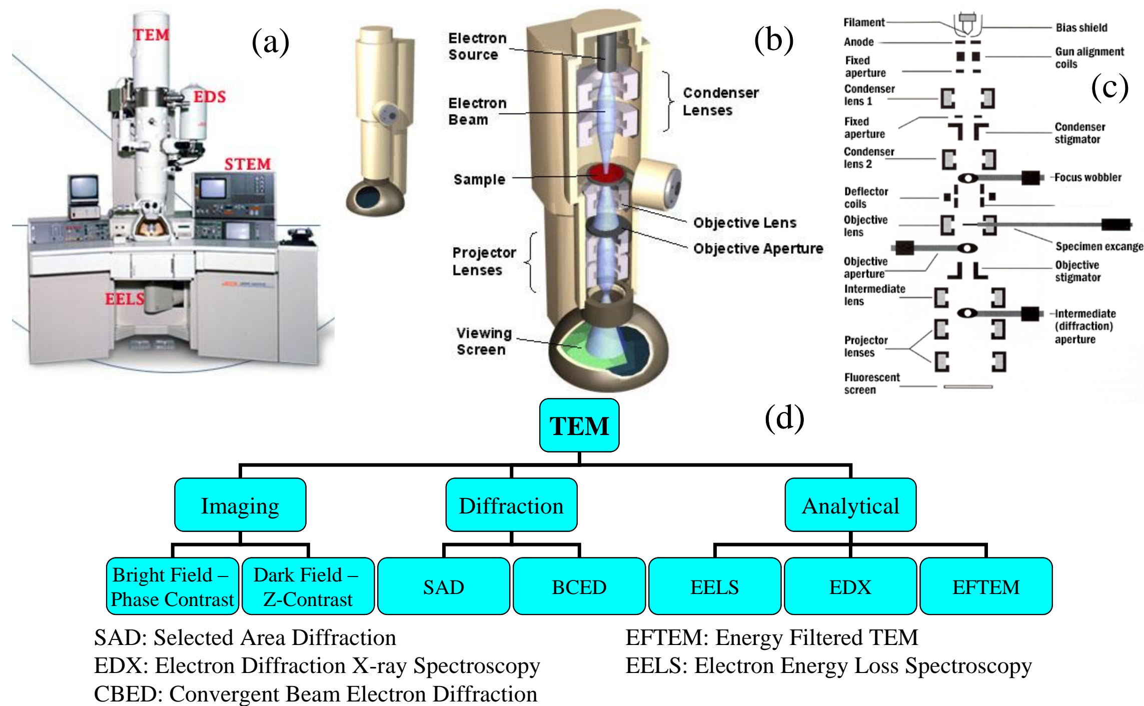

Figure 2.5 (a) An external illustrations of TEM components. (b) Internal configuration of the TEM imaging system. (c) Schematic sketch of the details for the TEM imaging system. (d) TEM functions. Pictures are from http://barrett-group.mcgill.ca/teaching/nanotechnology/nano02.htm (b), http://www.globalsino.com/micro/1/micro9997.html (c).

Figure 2.5(a) reveals the external feature of a typical TEM device. It includes four functions such as TEM imaging system, energy dispersive X-ray spectroscopy (EDS), scanning transmission electron microscopy (STEM) and electron energy loss spectroscopy (EELS). Figure 2.5(b) shows the internal configuration of the TEM imaging system. In general, the produced electron beams are focused via a series of aligned condenser lenses and then pass through a specimen. The imaging information regarding the specimen will be magnified and recorded after the through-out electron beams projected onto the viewing screen. However, the real design of TEM is much more complicated and the details of the internal configuration of the TEM imaging system is

shown in figure 2.5(c) and references. Figure 2.5(d) lists some important characterization methods, from which, bright field electron microscopy, selected electron diffraction (SED) and electron diffraction X-ray spectroscopy (EDX) will be applied in this thesis study.

2.6 Atomic Force Microscopy

The major utilization of atomic force microscopy is to examine samples' morphologies in 2D spaces. However 3D image can be done by the computer programmable treatment. Almost any types of surface, including polymers, ceramics, composites, glass and biological samples, are suitable.[19-21] The basis of AFM can be illustrated in figure 2.6 (a). After appropriate alignment of the AFM device, a laser beam, usually red Helium-Neon laser, is reflected from the back of the AFM cantilever. AFM tips and cantilevers are commonly microfabricated from Si or Si nitride Si_3N_4. A typical tip radius is from a few to tens of nanometers. When the tip is brought into proximity of a sample surface, the force between the tip and the sample surface leads to a deflection of the laser beam. The force obeys Hook's law

$$F = kx \qquad \text{Equation 2.6}$$

The measuring force is varied according to different purposes. Normally for the morphological determination, two modes, both contact and tapering modes, are frequently used. During the surface scan, the deflective laser spot recorded by an array of photodiodes. The resulting map of the area in x and y directions represents the topography of the sample.

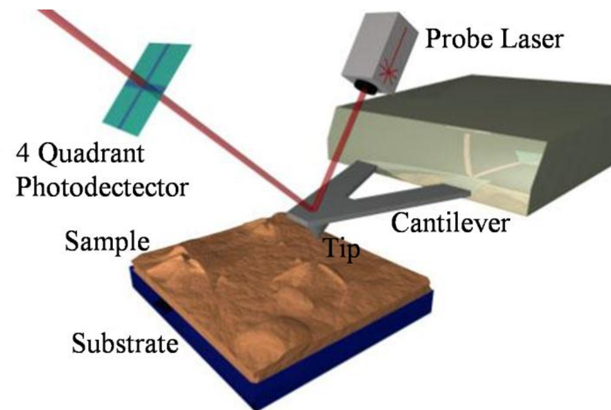

Figure 2.6 The schematic illustration for the principal of AFM.

2.7 Hall Measurement

Hall measurement method is used to quantify the current-carrying capability of materials and carry out meaningful comparisons between different samples. It is different from two terminal I-V measurement; Hall measurement can provide information about the type, number and properties of the charge carriers that constitute the current. The heart of Hall measurement is the Lorentz force law (figure 2.7(a)), which can be expressed by

$$\tilde{F}_{Lorentz} = q \cdot \left[\tilde{E} + (\tilde{v} \times \tilde{B})\right] \qquad \text{Equation 2.7}$$

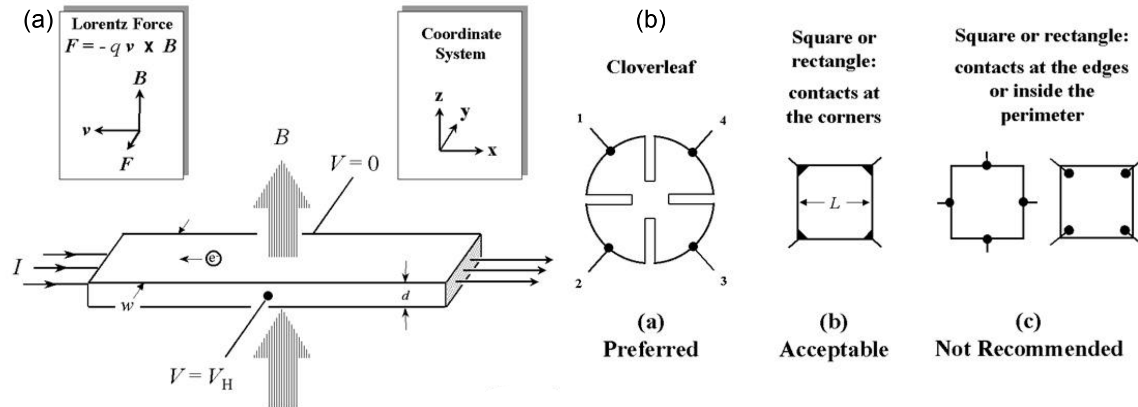

Figure 2.7 (a) Illustration of the Lorentz force law in a bar of conducting material. (b) Different geometries for sample measurements.
Images come from http://www.nist.gov/pml/semiconductor/hall_fig1.cfm,
and http://www.nist.gov/pml/semiconductor/hall_fig4.cfm.

When an electron moves along a direction perpendicular to an applied magnetic filed, it experiences a force acting normal to both moving and magnetic field direction. Herein, it is worthwhile to explain Hall measurement in details. Van der Pauw technique is a reliable and convenient way used in semiconductor industries. Examples of Van der Pauw configurations are shown in figure 2.7(b). Each configure contains four ohmic contacts which are numerically labeled counterclockwise. In the following equations, I_{12} means that positive dc current I injected into contact 1 and taken out from contact 2, likewise for I_{23}, I_{34}, I_{41}, I_{21}, I_{14}, I_{43} and I_{32}. V_{12} means dc voltage measured between contacts 1 and 2, that is $V_1 - V_2$ without applied magnetic field (B=0), likewise for V_{23}, V_{34}, V_{41}, V_{21}, V_{14}, V_{43} and V_{32}. Owing to four probes test, eight measurements of voltage yield eight values of resistance and all of them must be positive

$$R_{21,34} = \frac{V_{34}}{I_{21}}, \; R_{12,43} = \frac{V_{43}}{I_{12}}, \; R_{32,41} = \frac{V_{41}}{I_{32}}, \; R_{23,14} = \frac{V_{14}}{I_{23}},$$

$$R_{43,12}=\frac{V_{12}}{I_{43}},\ R_{34,21}=\frac{V_{21}}{I_{34}},\ R_{14,23}=\frac{V_{23}}{I_{14}},\ R_{41,32}=\frac{V_{32}}{I_{41}}. \qquad \text{Equation 2.8}$$

The sheet resistance R_s can be determined from the two characteristic resistances

$$R_A=\frac{(R_{21,34}+R_{12,43}+R_{43,12}+R_{34,21})}{4},$$

$$\text{and, } R_B=\frac{(R_{32,41}+R_{23,14}+R_{14,23}+R_{41,32})}{4}. \qquad \text{Equation 2.9}$$

Thus, the sheet resistance R_s can be calculated through Van der Pauw equation

$$e^{\frac{-\pi\cdot R_A}{R_S}}+e^{\frac{-\pi\cdot R_B}{R_S}}=1 \qquad \text{Equation 2.10}$$

The bulk electrical resistivity R_B can be calculated using

$$R_B=R_S\cdot d \qquad \text{Equation 2.11}$$

For metals and heavily doped semiconductors, the majority charge carrier is unique (either electrons or holes). The Hall voltage V_H is given by

$$V_H=\frac{-I\cdot B}{n\cdot e\cdot d} \qquad \text{Equation 2.12}$$

where B is the magnetic flux density, d is the depth of the plate which is as shown in figure 2.7(a), e is the electron charge (1.602×10^{19} C), and n is the charge carrier density.

Since sheet resistance involves both sheet density and mobility, one can determine the Hall mobility from the equation

$$\mu=\frac{|V_H|}{R_S\cdot I\cdot B}=\frac{1}{e\cdot n\cdot R_S} \qquad \text{Equation 2.13}$$

The Hall coefficient is defined as

$$R_H=\frac{E_y}{j_z B}=\frac{V_H\cdot d}{I\cdot B} \qquad \text{Equation 2.14}$$

where j_z is the current density of the carriers along z direction.

If intrinsic and lightly doped semiconductors are measured, the mobilities and weight densities of both of the carrier types must be taken into calculation. The Hall coefficient is thus defined as

$$R_H = \frac{\mu_h^2 \cdot p - \mu_e^2 \cdot n}{e \cdot (\mu_h \cdot p + \mu_e \cdot n)^2} \qquad \text{Equation 2.15}$$

where μ_h and μ_e are the hole and electron mobilities and p, n are the respective carrier densities.

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Chapter 3 Metal Induced Crystallization of Silicon

3.1 Introduction

In this chapter, we demonstrate that high quality poly-Si thin film can be fabricated in-situ on soda-lime glass at 450 ^{o}C by Al-induced crystallization method (AIC) using Ebeam evaporation system. The catalytic Al is found to diffuse to the top of the crystallized Si layer and can be easily etched away by a mixture of acids. This low temperature Si crystallization process is well explained by thermodynamic consideration. Subsequent annealing at the same temperature (450 ^{o}C) for six hours improves the crystallinity of the film and enlarges the average grain size to over 5μm. There are no observable impurity phases. X-ray diffraction (XRD) shows that (111) is the dominating crystalline orientation. Defect-free and excellent crystalline-structure has been revealed by Transmission Electron Microscopy (TEM). The electrical measurements such as resistivity, carrier concentration and charge mobility were carried out. Because of the participation of Al, I will show that the as-prepared poly-Si thin films exhibit heavily doped p-type (p^{+}-type) electrical property. For the 0.5 μm thick poly-Si thin film, I used it as a seed layer and epitaxial grow another p-type absorber Si layer with thickness of 0.9μm at 500 ^{o}C. The TEM confirmed good homo-epitaxial growth. Without breaking the high vacuum, an n-type a-Si layer with thickness of 0.7μm was coated onto the absorber layer to form a p-n junction. The corresponding I-V characteristic suggests that our low temperature processing technique is applicable for production of poly-Si thin film solar cell on low cost substrates.

3.2 Experimental procedures

Prior to film fabrication, the inexpensive soda-lime glass substrates as shown in figure 3.1(a) were cleaned with acetone, ethanol and de-ionized water. Al pellets (99.999% in purity, Kurt J. Lesker) and intrinsic Czochralski-Si flakes (99.999% in purity, Kurt J. Lesker) were used as the evaporation sources for Ebeam evaporator (NEE-4000 E-beam evaporation system, Nano-Master). Al layers varied from 50 nm to 200 nm in thickness were deposited onto glass substrates. The corresponding picture is shown in figure 3.1(b). Si thin films were subsequently coated onto the Al thin film at 400 ^{o}C, 450 ^{o}C, and 500 ^{o}C respectively (figure 3.1(c)). The deposition rate was 10 nm/min. Whereas the deposition at room temperature always leads to formation of amorphous Si, various degrees of Si crystallization occurs at growth temperature above 400 ^{o}C. The entire fabrication process, together with subsequent annealing for some samples (figure 3.1(d)), was carried out in high vacuum (around 2.5×10^{-6} Torr).

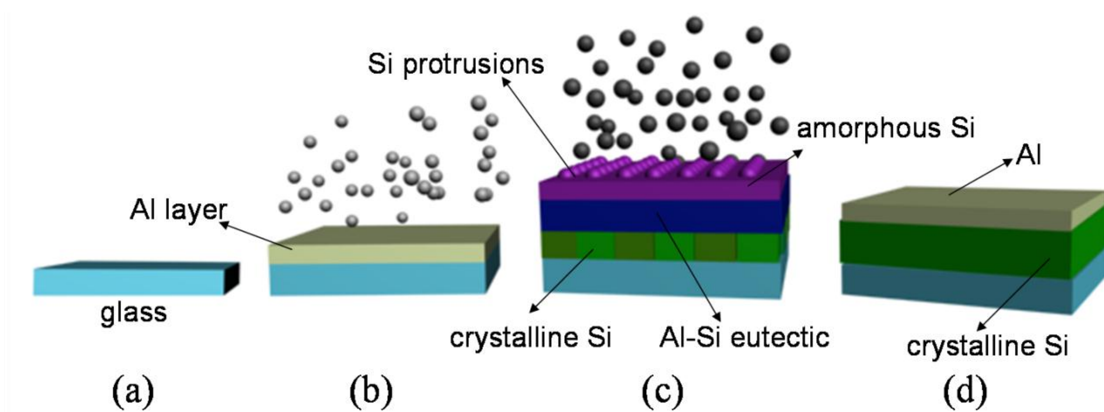


Figure 3.1 Schematic diagrams of AIC fabrication process. (a) As-prepared soda-lime glass substrate. (b) The deposition of Al layer at room temperature. (c) The deposition of Si at 450 ^{o}C. (d) The final stage of AIC process.

The effects of different thickness ratios of Al to Si have been studied. Raman spectroscopy (Horiba-HR800, λ=488 nm) and Hall characterization of the as-grown films were carried out after the Al top layers were etched away by a mixture of 70 ml H_3PO_4 (to dissolve the Al_2O_3), 5 ml HNO_3 (for Al oxidation), 10 ml CH_3COOH (for wetting and buffering) and 15 ml DI-H_2O (dilution). The crystalline quality of these films was evaluated by X-ray diffraction (Burker D8-Discover, CuKα, λ=1.541 Å) and Raman spectroscopy. The surface and cross-sectional morphologies were studied by Field-Emission Scanning Electron Microscopy (FESEM-JEOL JSM-6335F). Energy Dispersion X-ray Spectroscopy (EDS) was used to investigate the Al and Si distributions after post-annealing. Transmission Electron Microscopy (TEM-JEOL JEM2010) was utilized to characterize the cross-section of the sample. The Hall measurement (Ecopia, HMS-5000) was adopted to investigate the electronic properties, such as bulk resistivity, carrier concentration and charge mobility. Afterwards, one poly-Si thin film sample was picked up and used as the seed layer. A relatively thick p-type Si layer of about 900nm in thickness was deposited at 500 ^{o}C. Then an n-type a-Si layer with 700 nm in thickness was subsequently coated at room temperature. The corresponding epitaxial film quality and current-voltage (I-V) characteristic were examined.

3.3 Results and discussion

Figure 3.2 shows the XRD spectra for samples with the structure of glass/Al (50 nm)/Si (200 nm). Si was coated onto the Al layers at different temperatures. No post annealing was carried out. Apart from the Si (111) peak, no other XRD peaks of Si are observed. This is because the (111) crystalline plane corresponds to the lowest free energy and is most favorable to growth.[1] It is clearly seen from Figure 3.2 that the Si thin film fabricated at 450 ^{o}C gives the sharpest and strongest diffraction peak of Si (111) at 28.4^{o}. This suggests the presence of the largest crystalline grain size and the strongest chemical interdiffusion in the Si-Al binary system. The diffraction peak at 38.5^{o} is due to Al (111) crystalline planes. By comparison, poly-Si films deposited at 500 ^{o}C actually showed a poor crystalline quality. This agrees with the fact that soda-lime glass has a strain point temperature of 450 ^{o}C.[2] Films deposited at above the strain point temperature will inevitably exhibit worsened crystalline quality. Therefore, I chose 450 ^{o}C as the fabrication temperature for crystallized Si thin films based on AIC method for the rest of our investigations

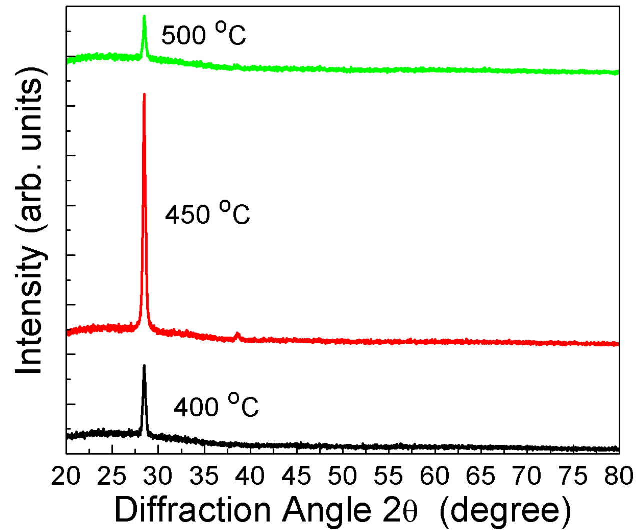


Figure 3.2 XRD profiles for glass/Al (50 nm)/Si (200 nm) structure prepared at 500 °C, 450 °C and 400 °C.

Al template layers with different thicknesses have been used to investigate the AIC process. The Si layer thickness in this study is fixed to about 500 nm. As revealed by XRD, all samples, irrespective to different Al layer thicknesses, show good Si crystallinity even without further thermal treatment (Spectra are similar to those in Figure 3.2 and are not shown here). However, the XRD characterization cannot yield information about a-Si. The relative amount of a-Si embedded in the poly-Si thin film has not been determined at this stage. The same set of samples was examined by Raman spectroscopy. In figure 3.3, the Raman peak at 520 cm^{-1} represents Si-Si Transverse Optical (TO) and Longitudinal Optical (LO) phonon band (crystalline phase). A broad Raman shift at approximately 480 cm^{-1} corresponds to a-Si. For all these three samples, both crystalline and amorphous phase Si co-exist. Although we have demonstrated that poly-Si can be produced in-situ at 450 °C, the presence of the a-Si suggests that

subsequent annealing is necessary in order to improve the crystallinity for realistic applications.

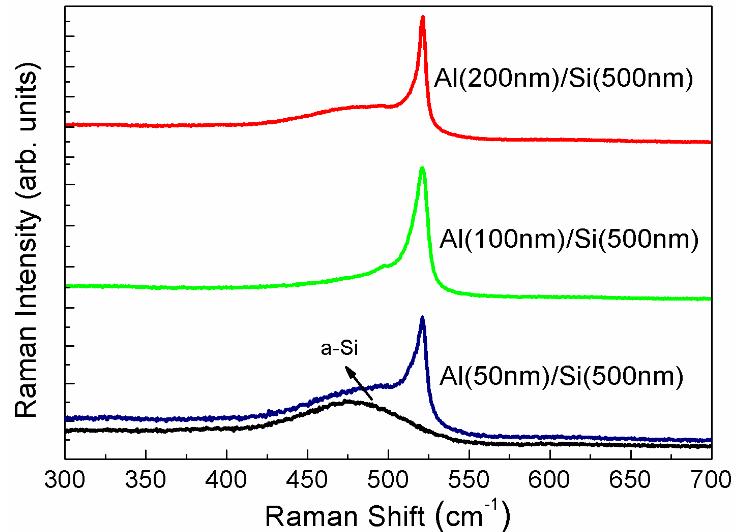
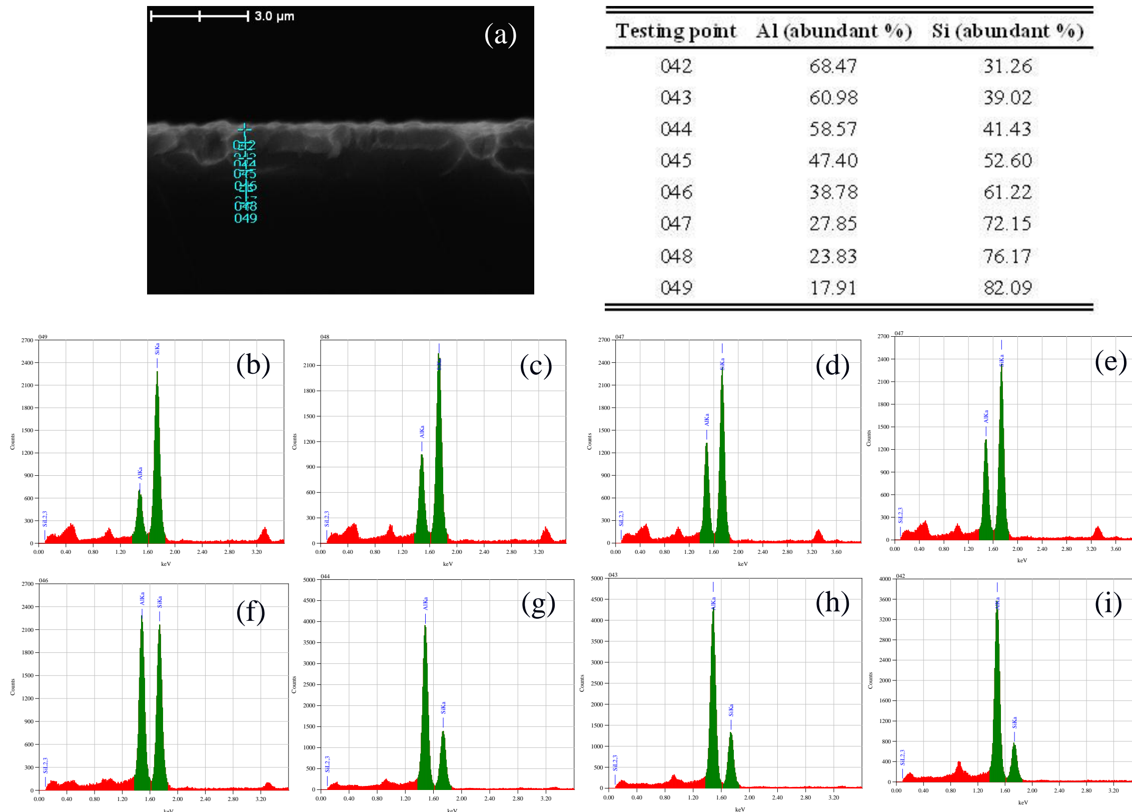


Figure 3.3 Raman spectra for the samples with different thickness ratios of Al to Si.

In order to determine the elements distributions after the deposition of Si at 450 °C by electron beam evaporation, a SEM cross section view for the sample with 500 nm thick of Si is shown in figure 3.4(a). Along the lateral direction, as indicated by blue crosses, eight different locations from the top of the sample down to its bottom were randomly picked up and examined by EDS. From figure 3.4(b) to (i), the relative amounts of Al and Si are plotted. The inset table recorded the corresponding weight percentage for both Al and Si at those eight points in sequence. Evidently, the abundant percentage of Al is maximum at the place near the sample surface. Below this points, the abundant percentage of Al with respect to Si start to decrease and they have equivalent amount at the middle point of the sample. At the lowest place, which is the nearest point to the glass substrate, the Si dominates. Remember that in the experiment, I initially deposited Al at

room temperature and Si was deposited subsequently at 450 °C. From the observation of this experiment, it verifies that the interdiffusion of Al and Si occurs during the deposition of Si at 450 °C.



Testing point	Al (abundant %)	Si (abundant %)
042	68.47	31.26
043	60.98	39.02
044	58.57	41.43
045	47.40	52.60
046	38.78	61.22
047	27.85	72.15
048	23.83	76.17
049	17.91	82.09

Figure 3.4 EDS investigation of the sample with 500 nm Si. (a) The cross sectional view of the sample, blue marks is the positions which was examined by EDS. The inset table shows the abundant percentages for both Al and Si at different position along the cross section of the sample. From (b) to (i), they are the corresponding EDS spectra.

In order to study the interdiffusion process of the Al-Si binary system, a sample, which has the structure glass/Al (500 nm)/a-Si (500 nm), was fabricated at room temperature. It was subsequently heat treated in high vacuum at 450 °C for 6 hours. As we can see from figure 3.5(a), the Al layer displays a well defined columnar structure, while the

amorphous Si forms a continuum film. A metastable silicide layer appears at the interface of Al and a-Si. The top surface constitutes a number of silicon protrusions. This is because the surface tension of Al film tends to minimize the gross surface area as much as possible when Si is coated. The surface energy of Al in this case can be approximated by

$$\sigma_{surface} \approx \frac{n' \times N^*}{n \times N_\circ} \times \Delta H_S \qquad \text{Equation 3.1}$$

in which, n' is the number of free bonds of atoms on the crystal surface, n is the number of the nearest-neighbor atoms in the crystal, N^* is the number of atoms on the crystal surface, N_o is Avogadro's constant (6.022×10^{23} mol^{-1}) and ΔHs is the latent heat (per 1 mole) of Al. In the case of (111) surface of face-centre cubic (fcc) structure of Al, $\Delta Hs \approx$ 8.600 kJ·mol^{-1}, n′ = 3, n = 12, and Al lattice constant (a_{Al}) = 4.050 Å. N^* can be approximated as

$$N^* = \frac{4}{\sqrt{3} \times a_{Al}^2} = 1.408 \times 10^{19} \qquad \text{Equation 3.2}$$

Referring to equation 3.1, the surface energy of Al, $\sigma_{surface}$, is approximately equal to 0.050 J/m^2. There is a distinct mixture phase which is sandwiched between the Al and Si films.

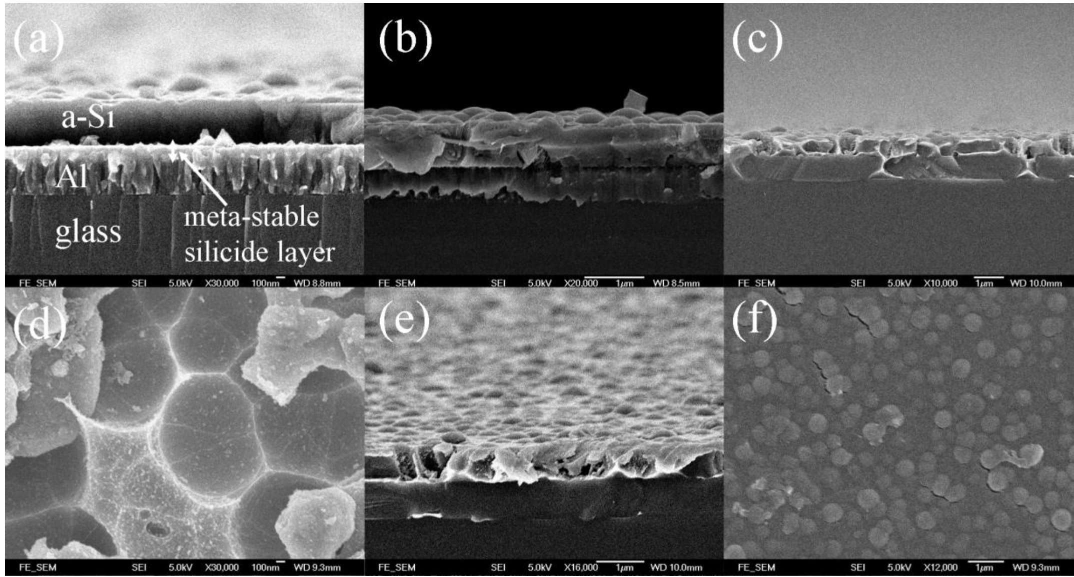


Figure 3.5 FE-SEM images for (a) glass/Al(500 nm)/a-Si(500 nm), (b) after half an hour annealing, (c) crossing sectional observation of Si grains formation after 3 hours annealing, (d) top view of of Si grains formation after 3 hours annealing, (e) crossing sectional view after 6 hours thermal treatment, (f) top surface observation after 6 hours thermal treatment.

During the initial half an hour annealing in high vacuum, the interdiffusion occurs at the interface (figure. 3.5(b)).[3] Since the annealing temperature is below the eutectic temperature of Al-Si, it leads to the formation of solid solution. Al-Si solid solution experiences a transition from order to disorder at this temperature, which leads to the change of entropy of the overall system. From thermodynamic consideration, the interdiffusion phenomenon depends on the gradient of chemical potential ($\partial\mu/\partial z$).[4, 5] For Si, it can be mathematically expressed as follow

$$\frac{\partial \mu_{Si}}{\partial z} = \left(\frac{\partial \mu_{Si}}{\partial x_{Si}}\right) \times \left(\frac{\partial x_{Si}}{\partial z}\right) = \left(\frac{R \times T}{x_{Si}}\right) \times \left[1 - \frac{(2 \times \Omega \times x_{Si}) \times (1 - x_{Si})}{R \times T}\right] \times \left(\frac{\partial x_{Si}}{\partial z}\right) \quad \text{Equation 3.3}$$

in which, x_{Si}, R, T and Ω are Si weight percentage ($0 \leq x_{Si} \geq 100$ %) in Al-Si solid solution, molar gas constant (8.314 $J \cdot mol^{-1} \cdot K^{-1}$), temperature and Al-Si interaction parameter respectively. For the Al-Si binary system, the interaction parameter, Ω, is approximately

equal to -13.640 kJ·mol^{-1}.[6] The diffusion flux (J) of Si can be calculated by taking the product of the concentration c_{Si} (mol/m^3) and the diffusion rate v_{Si} (m/s).

$$J_{Si} = c_{Si} \times v_{Si} = -m_{Si} \times R \times T \times \left[1 - \frac{(2 \times \Omega \times x_{Si}) \times (1 - x_{Si})}{(R \times T)}\right] \times \left(\frac{\partial c_{Si}}{\partial z}\right) \qquad \text{Equation 3.4}$$

The common term inside [ ] for equations 3.3 and 3.4 is known as the thermodynamic factor of diffusion coefficient. Si atoms that migrate into the Al rich region form solid solution with Al. In our case, as the annealing process goes on at 450 ^{o}C, the interdiffusion between Al and Si gradually increases the weight percentage of Si. Thus the term inside [] becomes significant. For the sample glass/Al(500 nm)/a-Si(500 nm) with 1 cm×1 cm surface area (the density of Si is about 2.329 g·cm^{-3}), the gradient of concentration of Si ($\partial c_{Si}/\partial z$) can be estimated to be approximately 4.996×10^{22} cm^{-3}. M_{Si} is mobility of Si atoms. In addition to the diffusion flux of Si, the coefficient of interdiffusion ($D_{Al\text{-}Si}$) of Al-Si can be written as

$$D_{Al-Si} = (D_{Si} \times x_{Al} + D_{Al} \times x_{Si}) \times \left[1 - \frac{(2 \times \Omega \times x_{Si}) \times (1 - x_{Si})}{(R \times T)}\right] \qquad \text{Equation 3.5}$$

In equation 3.5, D_{Si} and D_{Al} are defined as the diffusion coefficients for Si and Al respectively. The term $\Omega \cdot x_{Si} \cdot (1 - x_{Si})$ is called enthalpy of mixing. The negative sign which is added in the front of that term means Al atoms and Si atoms are attractive and Si is easy to merge with Al. During this process, the a-Si with covalent bonds is screened by

the free electrons in Al which leads to the reduction of binding energy.[7] The excess energy is further utilized for prompting the dissolution of Si atoms. The Si atoms experience interface migration and precipitation. Once the supersaturated condition is reached, the nucleation occurs at the surface of a substrate. The Al is simultaneously pushed away and diffuses out. The process ultimately leads to the formation of Si grains. The grain boundaries define the trajectories where the Al can diffuse out and finally reach the top surface. In figure 3.5 (e) and (d), it is clear to see that some residual Al left at the grain boundaries after annealing for 3 hours. The mechanism includes both surface diffusion and grain boundary diffusion at this circumstance, and the apparent diffusion coefficient (D) which includes both the diffusion coefficients for the gain surface (D_{surf}) and the gain boundary (D_{gb}) can be expressed as

$$D = f_{lat} \times D_{lat} + f_{gb} \times D_{gb} = \left(\frac{r}{r+\delta}\right) \times D_{lat} + \left(\frac{\sigma}{r+\sigma}\right) \times D_{gb} \qquad \text{Equation 3.6}$$

where, f_{lat} is fraction of cross-sectional area of Si gain, f_{gb} is fraction of cross-sectional area of Si grain boundary, D_{lat} is diffusion coefficient in the Si grain, D_{gb} is diffusion coefficient at the grain boundary, r is Si grain radius and σ is Si grain boundary width. Therefore, the apparent diffusion coefficient depends on the dimension of Si grain. Indeed, it is essential to get rid of all the Al otherwise charges are more preferentially conducted in metal rather than in Si. For this reason prolonged annealing, such as for another 3 hours, is required for up migration of all Al. As we can see from figure 3.5 (e) and (f), the top surface is covered with Al protrusions after 6 hours thermal treatment and

it is quite similar with previous amorphous Si surface. Prolonged annealing at 450 ^{o}C leads to the formation of large poly-Si grains and the size of the grain is much larger than the film thickness. In our experiment, we found the average gain size of poly-Si is more than 5 μm, which is useful for device fabrications.

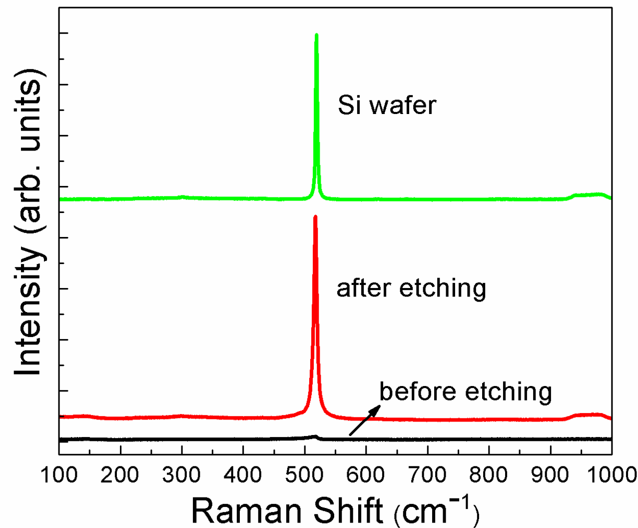


Figure 3.6 Raman spectroscopy of poly-Si before and after chemical etching

From the Raman spectra shown in figure 3.6, owing to the whole top surface is covered by diffused Al, there is no decernable crystalline Si peak at 520 cm^{-1}. After chemically removing the top Al, however, a sharp peak at exactly 520 cm^{-1} appears. The amorphous component, as revealed in figure 3.3, is no longer observed. The FWHM of the crystalline Si peak is comparable with that of Si wafer and there is no noticeable shift of the Raman peak position.

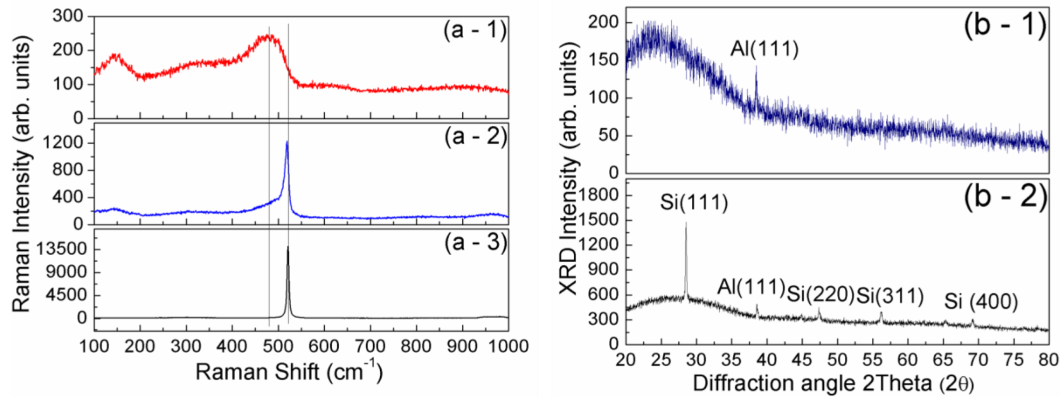


Figure 3.7 Micro-Raman spectroscopic and XRD spectroscopic characterizations of poly-Si. (a) Micro-Raman spectroscopic studies for (a-1) a-Si, (a-2) AIC fabrication without post annealing, and (2-3) AIC fabrication with 6 hours annealing. (b) XRD studies for (b-1) sample fabricated at room temperature, (b – 2) sample fabricated by AIC with 6 hours post annealing at 450 ^{o}C.

We also use non-destructive Raman spectroscopy to evaluate the Si thin films prepared under different conditions. Figure 3.7 shows the micro-Raman spectra for samples fabricated at room temperature and at 450 ^{o}C with and without post annealing. In figure 3.7(a-1), of which the sample was fabricated at room temperature, a dominating band centered at around 480 cm^{-1} with a full width at half maximum (FWHM) of 113.88 cm^{-1} is the a-Si phase. It is ascribed to the transverse optical (TO) mode. Another distinct peak for the a-Si at 150 cm^{-1} is associated with transverse acoustic (TA) vibrational mode. There is no discernable Si crystalline phase. Figure 3.7(a-2) shows the Raman spectrum for sample fabricated at 450 ^{o}C without post-thermal treatment. A sharp but asymmetric Raman peak occurs at 518 cm^{-1}. It represents the zone-center longitudinal optical (LO) and transverse optical (TO) phonon mode in c-Si. The Al gives rise to p-type Si formation. The Raman shift is smaller than the one of undoped single c-Si. The FWHM of this band is 10.44 cm^{-1}. Owing to the coexistence of amorphous phase, the calculated crystalline volume based on the intensity ratio of the peaks at 480 cm^{-1} and 518 cm^{-1} is

approximately equal to 0.58. For the sample that has been post annealed at 450 ^{o}C for 6 hours we found that the Si was fully crystallized. As shown in figure 3.7(a-3), there is no observable amorphous phase. The FWHM is decreased to 5.00 cm^{-1} and the dominating Raman shift is exactly at 520 cm^{-1} of an undoped single c-Si. Figure 3.7(b) shows the XRD spectra for samples fabricated at room temperature and at 450 ^{o}C with 6 hours post annealing. In figure 3.7(b-1), the glass substrate results in a broad diffracted band extends from 20° to 35°. The X-ray diffraction at 2θ = 38.47 originates from Al (111) crystalline planes. There is no trace of c-Si peak. By contrast, figure 3.7(b-2) reveals out-of-plane crystalline orientations for the Si fabricated by AIC method. The dominating crystalline orientation is (111).

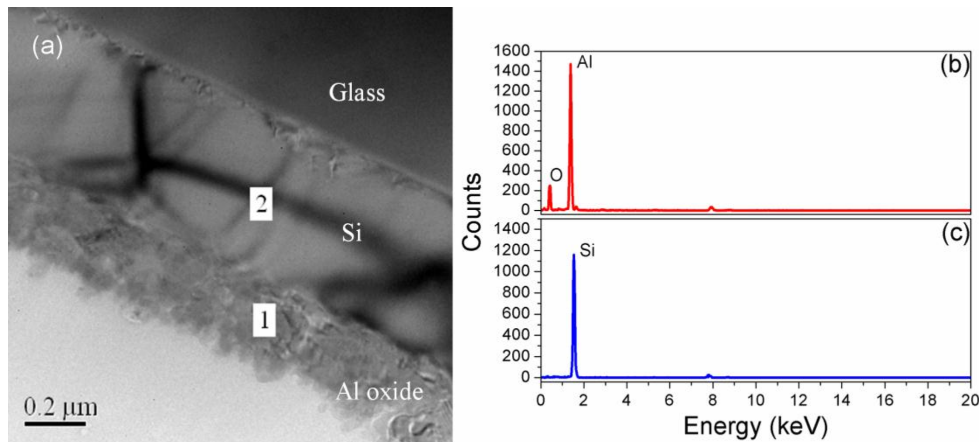


Figure 3.8 (a) Cross-sectional BF-TEM image of poly-Si film on glass, (b) EDS at location 1, (c) EDS at location 2.

We used EDS to investigate the spatial distributions of Al and Si in the films. Figure 3.8 (a) shows the results of a sample of glass/Al (200nm)/Si (500nm). The sample has been thermally treated at high vacuum at 450 ^{o}C for 6 hours after Si deposited onto Al at the same temperature. The picture in figure 3.8(a) was obtained by TEM and the points 1 and

2 were randomly chosen from the crossing section of the sample. Only Al is found around location 1 (figure 3.8(b)). The appearance of oxygen (O) is due to oxidation during the sample preparation process. By comparison, only Si is detected at location 2 (figure 3.8(c)).

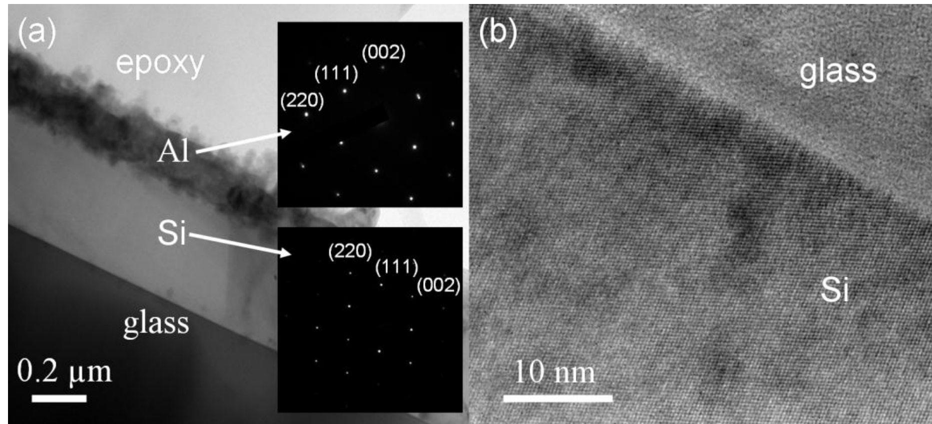


Figure 3.9 TEM images of AIC fabricated poly-Si thin film. (a) Crossing sectional view of glass/poly-Si (500 nm)/ Al (200 nm), the insets show the selected area diffraction patterns for both poly-Si and Al layers. (b) High resolution-TEM image for as-grown poly-Si thin film.

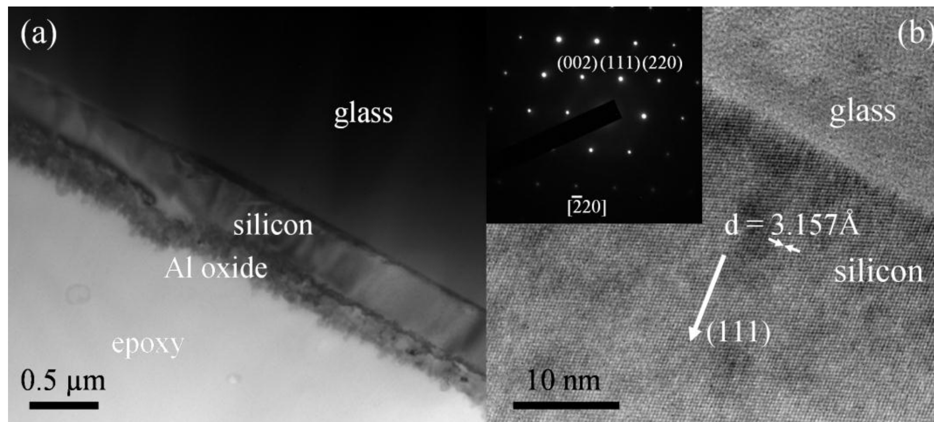


Figure 3.10 (a) Low magnification cross-sectional BF-TEM image of poly-Si, (b) cross-sectional HR-TEM image of the interface between poly-Si layer and glass substrate, the inset shows electron diffraction pattern for the crystalline Si thin film.

Apart from EDS, further evaluation of the poly-Si thin film crystalline quality can be seen from the selected area electron diffraction (SAED) pattern for both poly-Si and Al layer respectively. The TEM image of the layer cross section was captured and displayed in figure 3.9(a). SADP for each layer was taken and displayed in the insets. The white arrows connect the layers with their corresponding SADP. For the catalytic Al layer, three diffraction spots, (220), (002) and (111), have been indexed. Similar calculation was made for the poly-Si layer. Three representative diffraction spots for face central cubic (f.c.c) structure of poly-Si are labeled. Figure 3.9(b) displays the high resolution-TEM (HR-TEM) image. The lattice arrangement of Si has been clearly revealed. There is no impurity phase at the poly-Si and soda-lime glass interface. Figure 3.10(a) shows the sample with even lower magnification of the cross section. Judging from figure 3.10(a), no distinct grain boundaries are observed. The AIC Si grains with more than 5 μm in size are in close contact with the glass substrate. It also exhibits excellent crystallinity without any defects and dislocations. Figure 3.10(b) displays the corresponding HR-TEM image of the AIC poly-Si film. There is no a-Si phase in between the amorphous glass and poly-Si thin film. It is evident that all a-Si is crystallized. The regular arrangement of Si lattice planes is clearly observed. The arrow with (111) indicates the direction of Si crystalline planes which are nearly perpendicular to the interface of glass and silicon. Crystalline quality of this Si layer was remarkably good as revealed by the lattice planes in HR image and electron beam diffraction pattern in figure 3.10(b) and the inset respectively. The diffraction spots were indexed with the corresponding diffraction planes. The zone axis in this case is $[\bar{2}20]$ which is normal to all the indexed diffraction spots. For the fcc

lattice, such as Si with diamond structure, the miller indices (h, k and l) are all even or all odd. The connection of (111) diffraction spots in reciprocal space is parallel with the (111) lattice plane in the real space in figure 3.10(b). The distance of each pair of adjacent lattice planes along (111) direction is approximately equal to 3.157 Å. Therefore, the lattice constant of Si can be calculation as $a_{Si} = d\times\sqrt{(h^2+k^2+l^2)} = 3.157Å\times\sqrt{3} \approx 5.468$ Å. The result is close to bulk single crystal Si and agrees well with previous report.[8]

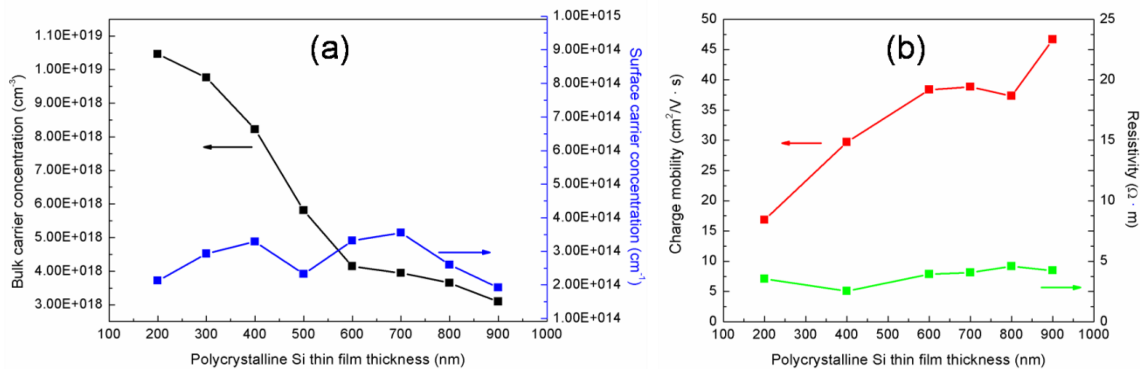


Figure 3.11 Hall measurements for (a) bulk carrier concentration and surface carrier concentration as a function of poly-Si thin film thickness, (b) charge mobility and resistivity as a function of poly-Si thin film thickness.

Figure 3.11 shows the results of Hall measurement for the poly-Si thin films with different thicknesses. After AIC process, the thicknesses of the poly-Si thin films ranging from 200 to 900 nm but the thickness of Al was always maintained at 200 nm. Both the bulk carrier concentrations and the surface carrier concentrations are revealed in figure 3.11(a). The bulk carrier concentration decreases with the increase in the poly-Si thin film thickness. This is primarily due to the presence of the same amount of Al was used

in the AIC process but the thickness of Si was varied. The sign for all the measured samples showed that the majority charge carriers within those materials are positive and

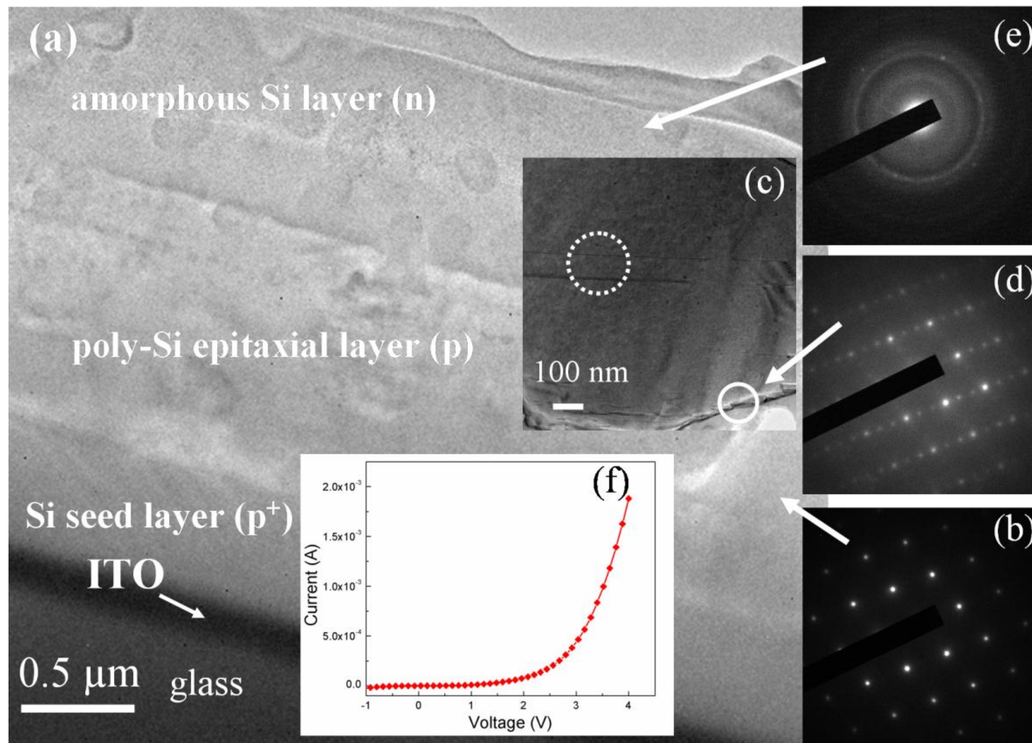


Figure 3.12 TEM image of a prototype poly-Si thin film solar cell. (a) Crossing sectional view of the solar cell. (b) SADP for the epitaxial layer. (c) LM-TEM image captured from poly-Si grain boundaries. (d) SADP taken from poly-Si grain boundaries. (e) SADP for the n-type a-Si layer. (f) IV-characteristic curve.

the samples possess the heavily doped p type semiconductor characteristic.[9, 10] However, the surface carrier concentrations for all the samples are almost equal. In addition, their charge mobilities and resistivities were also measured and the results are shown in figure 3.11(b). The charge mobility increases from 16.5 $cm^2/V\cdot s$ to 46.5 $cm^2/V\cdot s$ when the thickness of the poly-Si thin film is increased from 200 nm to 900 nm. Similar with surface carrier concentration, the resistivity has no remarkable variation along with different sample thicknesses.

Owing to the use of catalytic Al during the poly-Si seed layer growth, this gives rise to the heavily doped p-type (p^+-type) Si formation. Hall measurement of this 0.5 μm poly-Si layer revealed a resistivity (ρ), hole concentration (n_h) and mobility (μ_h) to be 3.28×10^{-2} $\Omega\cdot$cm, 5.81 $\times10^{18}$ cm^{-3} and 34.11 $cm^2\cdot V^{-1}\cdot s^{-1}$ respectively. In order to demonstrate the feasibility of our poly-Si thin film fabrication technique for future solar cell application, a p-n junction structure partially based on poly-Si thin film was fabricated on an ITO coated soda-lime glass substrate. The TEM image of the films cross section is shown in figure 3.12(a). The Si seed layer growth is based on the AIC technique. The fabrication temperature for such seed layer was 450 ^oC and the post-annealing was carried out at the same temperature. Then, a p-type poly-Si absorber layer was epitaxial grown on the p^+-type poly-Si seed layer at 500 ^oC via Ebeam evaporation. Excellent crystalline quality of the poly-Si epitaxial layer was confirmed by SADP (figure 3.12(b)). Figure 3.12(c) shows the low magnification-TEM (LM-TEM) image taken around the grain boundaries (solid white circle). The corresponding SADP is displayed in figure 3,12(d). Occasionally, we observed the appearance of dislocations which has been highlighted by white dotted circle. Subsequently, an n-type a-Si layer was coated onto the p-type expitaxial layer at room temperature by Ebeam evaporation in order to form a p-n junction. Figure 3.12(e) displays the SADP of this n-type layer. In figure 3.12(f), good rectifying profile has been clearly shown here. Figure 3.13 also displays such poly-Si thin film solar cell design in a low magnification manner via SEM. The corresponding photo-response for this prototype poly-Si thin film solar cell is indicated in figure 3.14.

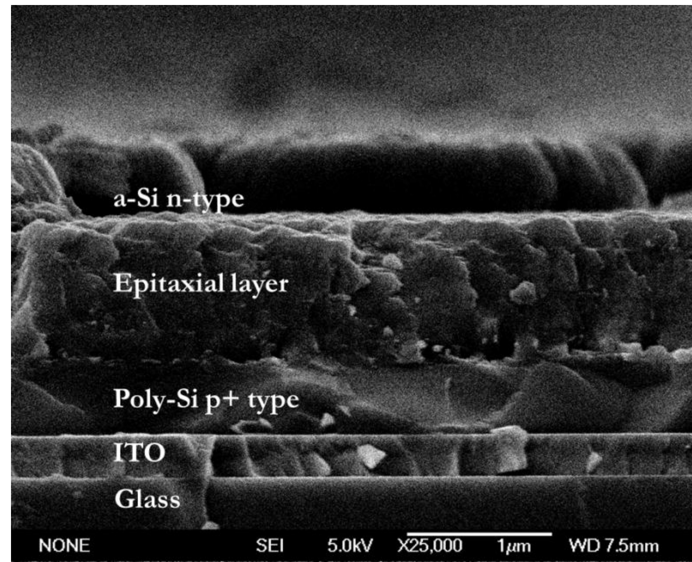


Figure 3.13 SEM image for the crossing sectional view of the poly-Si thin film solar cell.

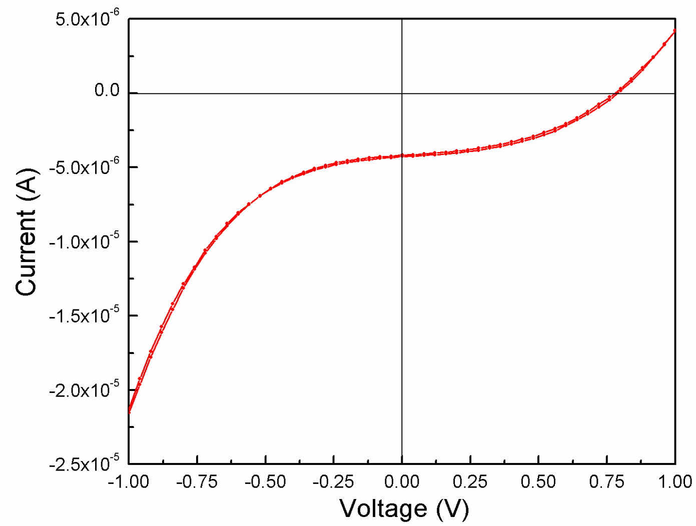


Figure 3.14 Photo-response for the sample which is illuminated with white light.

3.4 Summary

In this chapter, the AIC technique has been demonstrated for the poly-Si growth on soda-lime glass at reduced temperature. Both spectroscopic and microscopic characterizations verified the high quality of the poly-Si thin films. The low temperature epitaxial growth and the resultant IV characteristic indicate this novel processing technique is promising in the poly-Si thin films based solar cell applications.

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Chapter 4 Si Nanowires and Nanorods Growth by Electron Beam Evaporation

4.1 Introduction

One dimensional (1-D) Si nanostructure such as rods, wires, belts and tubes have gained particular attention because the popular role of Si in semiconductor industry and the fact that these nanostructures can be utilized as interconnects and functional units in electronic, optoelectronic and storage devices.[1-3] Vapor-liquid-solid (VLS) method is one of the well known techniques to make Si nanorods (SiNRs) and Si nanowires (SiNWs).[4] The concept of VLS was introduced by Wagner and Ellis in 1964 in order to explain the unidirectional whisker growth involving impurities.[5] From observation of the Si whiskers shown in that article, it reveals three key facts: I. Si whiskers do not contain an axial screw dislocation; II. Catalytic impurity is essential for whisker growth; and III. A small globule of the catalytic metal or metal eutectic is present at the top of the whisker during the growth. Up to date, many researchers have used this VLS technique to grow of SiNRs.[6,7] The present study is devoted to both experimentally and theoretically investigation of the growth mechanism of SiNRs made by VLS method and Ebeam evaporation. The SiNRs fabrication procedure is similar to those grown by conventional chemical vapor deposition (CVD) method, except with the absence of the chemical reactive precursors such as $SiCl_4$ and H_2. For the CVD fabricated SiNRs or SiNWs, the

thermal requirement for the reduction of those chemical precursors is crucially important in producing Si atoms.[8] The physical deposition of Si by Ebeam evaporation, however, helps to reduce the growth temperature of SiNRs to below of 500°C. Under the present scheme of stylizing VLS method and Ebeam evaporation, the initial stage of fabricating SiNRs relies on depositing a very thin catalytic metal layer, such as Au. The corresponding schematic diagrams are shown in figure 4.1(a) and (b). Upon annealing at temperature above the eutectic temperature of Au-Si binary system, Au-Si eutectic is formed (figure 4.1(c)). Due to the high surface tension and the high surface tension and the hydrophobic Si surface, the molten eutectic tends to agglomerate into droplets, whose size depends on the initial Au layer thickness. In cases where the growth temperature is below the eutectic temperature of Au-Si, it leads to the solid solution formation, in which the interdiffusion between Au and Si occurs according to their concentration gradients. This mechanism is the so-called metal mediate or metal-induced crystallization in the early report.[9] It is sometimes being referred as vapor-solid-solid (VSS) growth mode. In general, VSS is used for large-scale c-Si film fabrication, where VLS is used for growing SiNRs or SiNWs. In the VLS growth mode, a continue supply of Si vapor condensation, drives the Au-Si eutectic phase or liquid solution to Si saturation or supersaturation status. The diffusion of Si in the liquid solution leads to the incorporation of Si atoms in the c-Si lattice of the c-Si substrate underneath. Nucleation of Si at bottom reduces the amount of Si in the Au-Si eutectic. It therefore requires adsorption of more Si atoms from the top in order to maintain a Si saturation status in the Au-Si liquid solution. This is achieved by

the catalytic Au cap, which not only collects the Ebeam evaporation produced Si atoms but plays an important role in guiding the SiNRs growing direction. The details of this VLS and Ebeam evaporation based SiNR growth mechanism is explained satisfactorily by the linearized stability theory. The unusual phonon confinement by the SiNRs has also been revealed in studies using non-destructive mirco-Raman spectroscopy.

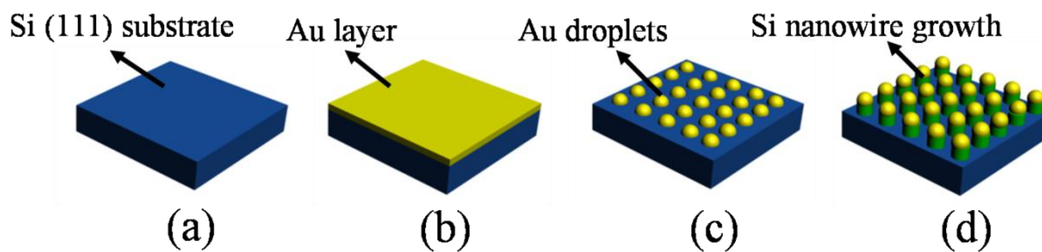

Figure 4.1 The schematic diagram of the VLS method. (a) Si (111) substrate preparation. (b) Very thin Au layer coating. (c) Au droplets formation via thermal annealing. (d) Si nanorods growth by EBE system.

4.2 Experimental procedures

In the experiment, both PLD and Ebeam evaporation systems were responsible for Au coating and SiNRs growth respectively. For the former one, we used excimer laser (KrF, Lambda Physik) with wavelength of 248 nm as the ablation source. Inside a cylindrical stainless steel PLD chamber, high purity (99.999%, Kurt Lesker) Au was used as the laser ablation target. One side polished single c-Si wafer with (111) crystalline orientation was used as substrate. The Si wafer was initially cut into small pieces with 1×1 cm^2 in area. They were then washed subsequently in acetone, ethanol and de-ionized

water under the ultrasonic vibration for a few minutes. In order to efficiently remove organic contaminants and metal flakes, the Si substrates were subject to the standard RCA cleaning processes. The native Si dioxide (SiO_2) can be completely removed by diluted HF (5 %) at room temperature. After the Si substrate was placed on the substrate holder which is directly facing the Au target, the separation between these two was set to be 40 mm. The evacuated PLD chamber was kept at a base pressure of 2.0×10^{-6} Torr. Deposition was carried out at room temperature. With the laser running at 4 Hz and 240 mJ pulsed laser energy throughout the experiment, different deposition time intervals produced different thicknesses of Au layers. Immediately after this Au coating, the samples were immediately transferred into the EBE system without further delay. Under a similar base pressure as the PLD system, the substrate temperature was rapidly increased to 500 ^{o}C in order to induce the formation of the gold droplets. After annealing for 30 min, the electron beam was utilized to melt and evaporate intrinsic Si flakes placed inside a glassy coated graphitic linear. The deposition rate was well controlled by a thickness controller at 1 nm/s. After the SiNRs reach desirable lateral heights, the temperature was naturally reduced down to the room temperature in high vacuum. The distributions and the size effect of the Au droplets have been studied via atomic force microscopy (AFM) and transmission electron microscopy (TEM, JEOL-JEM-2010). Field emission scanning electron microscopy (FESEM, JEOL-JSM-6335F) was used to characterize the feature of the as-grown SiNRs and SiNWs. Micro-Raman spectroscopy (Horiba-HR800) equipped with an excitation laser of λ = 488nm was used to study the inelastic scattering for those as-fabricated SiNRs.

4.3 Results and discussion

Figure 4.2 shows the AFM images of Au layers deposited at 8 different laser ablation time intervals by PLD system and have been annealed at 500 ^{o}C for 30min. The AFM image of the (111) crystalline oriented Si without Au coating which is shown in figure 2 (a) revealing absence of any metal impurities. Au deposition with very short laser ablation times, for instance, the ones of 5s and 10s are depicted in figure 4.2 (b) and (c). Some small and randomly distributed Au dots can be observed. Distinctly, from figure 4.2 (d) to (f), which correspond to the laser ablation time of 15s, 20s and 25s respectively, it is seen that a longer laser ablation time leads to bigger and less dense assembly of Au dots. For 30s laser ablation time of Au shown in figure 4.2 (g), the number of the Au dots is likely to increase again. Further increase in the deposition time of the Au to 50s, lead to closely packed Au dots over large area. The corresponding AFM image is displayed in figure 4.2 (h). Obviously if the thickness of the initially PLD coated Au layer exceeds a critical thickness, it can no longer congregated into uniformly distributed Au droplets upon annealing.

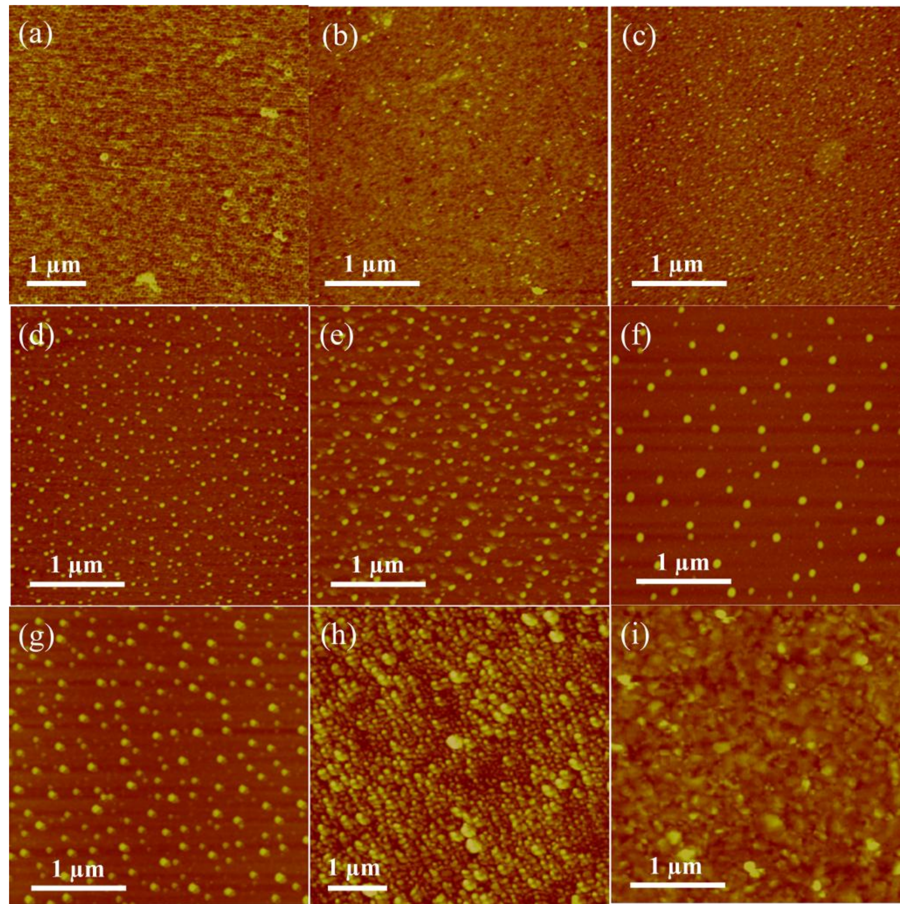

Figure 4.2 AFM images for (a) oxide-free (111) Si substrate. (b) 5s Au coating with annealing. (c) 10s Au coating with annealing. (d) 15s Au coating with annealing. (e) 20s Au coating with annealing. (f) 25s Au coating with annealing. (g) 30s Au coating with annealing. (h) 50s Au coating with annealing. (i) 70s Au coating with annealing.

Indeed, all the AFM images shown in figure 4.2 do not give clear 3 dimensional (3-D) features of the Au dot and its relationship with c-Si substrate. Based on the sample coated with Au via 30s laser ablation time, TEM examination suggests that these Au dots have hemi-spherical shape. A typical TEM image is shown in figure 4.3 (a); and, figure 4.3 (b) gives a magnified image. For each large Au dot, it is surrounded by a few small Au dots.

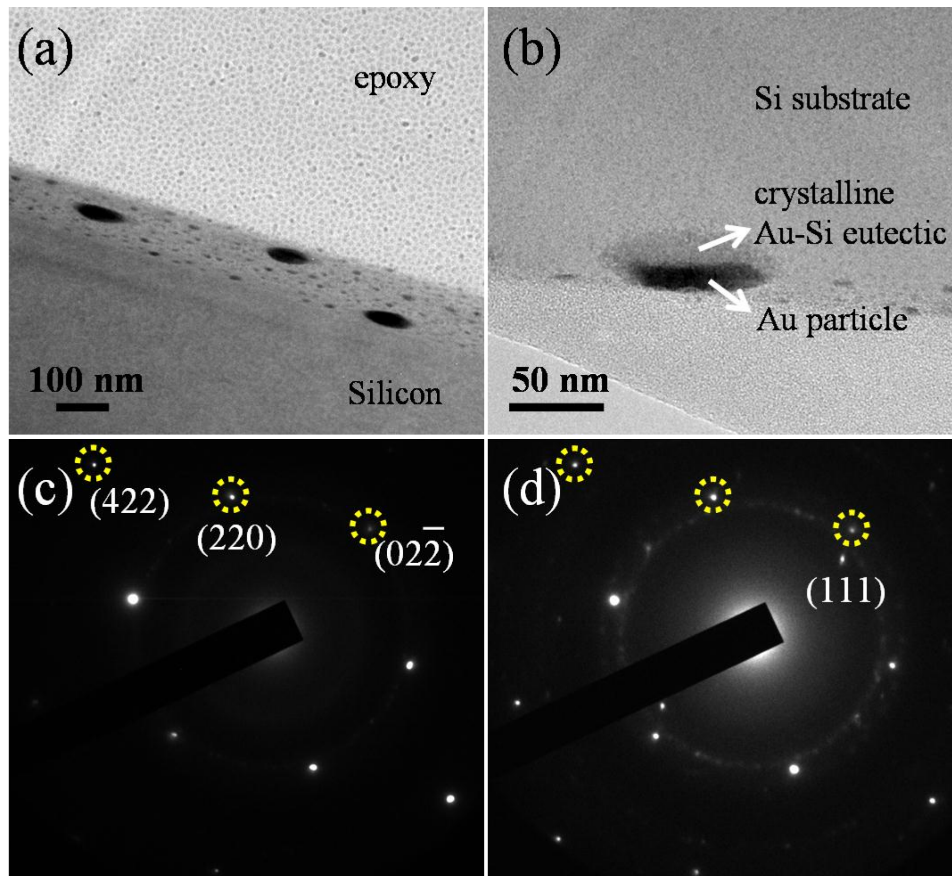

Figure 4.3 (a) TEM image for Au droplets formation on Si substrate. (b) Au-Si eutectic formation upon annealing. (c) SAED pattern for (111) crystalline oriented Si. (d) SAED pattern for Au-Si eutectic.

This is consistent with the observation of the AFM image in figure 4.2(g). It is expected that Annealing at 500 ^{o}C which is above the eutectic temperature of Au-Si alloy, the Au precipitated on the surface of Si substrate which gives rise to formation molten Au-Si eutectic layer. The formation of this intermediate layer or the Au-Si eutectic phase should lead to the decrease of the lattice mismatch of these two materials, to the appearance of stress at the interface and to the increase of the elastic energy of the interface. In addition, the selected area electron diffraction (SAED) pattern captured only for the (111) crystalline oriented Si substrate shown in figure 4.3(c) consists of no impurity phases.

Some relevant diffracted spots have been indexed for reference. By comparison, the SADP for the Au-Si eutectic is displayed in figure 4.3(d). Apart from those three diffracted spots for the c-Si, the (111) crystalline orientation of Au can also be observed. A dim diffracted ring which represents the polycrystalline characteristic of the Au can be found amid the Si and the (111) oriented Au diffracted spots.

As we can see from figure 4.4(a), the inset shows the initial stage of the SiNRs growth. During which, Si atoms are supplied in the vapor phase from top. The diameter of the SiNRs are defined and limited by the size of the Au-Si eutectic droplets. A corresponding schematic diagram is also shown in figure 4.5 (a). As the SiNRs keep growing, the number of Si atoms are adsorbed by the eutectic should be equal to the number of Si atoms extracted from the Au-Si eutectic. As a consequence, the Au-Si eutectic phase is always in the saturation status. The number of the adsorbed (N_{ads}) and the one of the extracted (N_{ext}) Si atoms can thus be expressed as[10]

$$N_{ads} = 2 \cdot \pi \cdot R \cdot (R + \sqrt{R^2 - r^2}) \cdot n = N_{ext} = \frac{10^6 \cdot \pi \cdot r^2 \cdot S \cdot \rho \cdot N_{arv}}{M}$$ Equation 4.1

where, R, r, n, S, ρ, N_{arv}, and M are the curvature of the radius of the Au-Si eutectic droplet, the curvature of the radius of the SiNR (figure 4.5(b)), the number of Si atoms from the Si vapor impinging on a unit plane surface in a unit time, the surface area of Si nucleation site, the Avogadoro constant and the molar mass of Si respectively. The extracted Si atoms are, therefore, the constituent of the SiNRs. In figure 4.4(b) and its inset, it is clear to see that EBE technique can yield large area and homogeneous SiNRs

and their average aspect ratio is 3:1. In Some case, when the initial formation of the volume of the Au-Si eutectic droplets are small and their distribution is very close, it gives a consequence of a number of SiNRs grow laterally but jammed together (figure 4.4(c)). However, there is a critical diameter at which the SiNRs or SiNWs growth completely stops. This is primarily due to the reason that as the diameters of the SiNRs becomes smaller, the vapor pressure and the solubility of Si tend to increase. Referring to the Gibbs-Thomson effect, the relationship between the supersaturation and the SiNR radius can be written as[11]

$$\Delta\mu = \Delta\mu_0 - \frac{2 \cdot \Omega \cdot \alpha}{r} \qquad \text{Equation 4.2}$$

where $\Delta\mu$ is the effective difference between the chemical potentials of Si in the vapor phase and in the SiNR, $\Delta\mu_0$ is the same difference at a plane boundary, α is the specific free energy of the SiNR surface and Ω is the atomic volume of Si. Indeed, it is also likely to fabricate SiNWs when using sufficient longer deposition time of Si but the same deposition rate. It tends to increase the aspect ratio of as-prepared SiNRs. The corresponding SEM image is shown in figure 4.4(d). As indicated by the red dotted circles, the side faces of SiNRs tend to grow by a two-dimensional mechanism for the SiNWs. In many cases, such side faces are stepped although they grow much slower than the Si nucleation at the tip of the SiNRs. Similar phenomenon can be found from CVD technique.[12, 13]

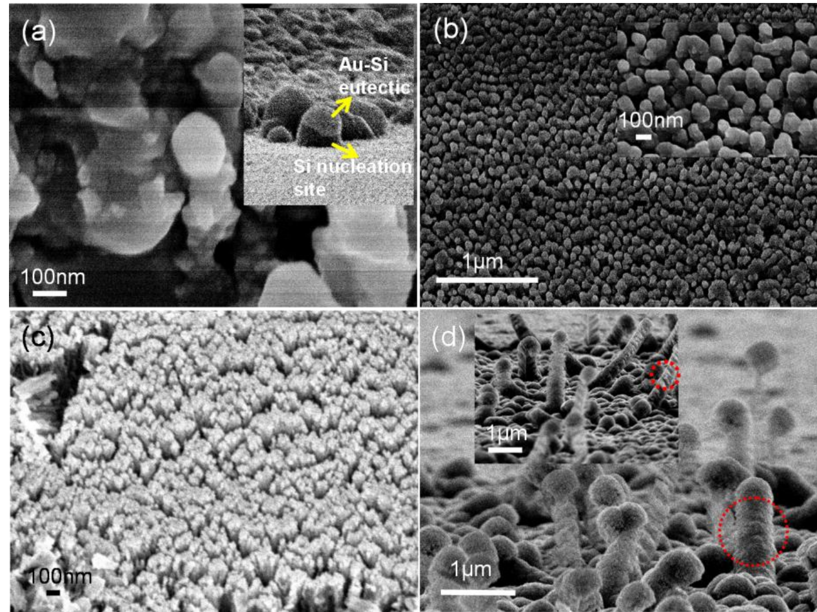

Figure 4.4 SEM images for (a) SiNRs growth, and the inset shows the formation of the Au-Si eutectic at the most top. (b) Large area SiNRs, the inset shows the corresponding magnified image. (c) Highly densely assembled SiNRs. (d) SiNRs with large aspect ratio, 10:1, and the inset shows the corresponding magnified image.

A useful model to investigate the critical size of the nuclei of SiNRs based on the VLS method is linearized stability theory.[14] This theoretical model is based on two assumptions. Firstly, the eutectic Au and Si is perfect spherical; and, the Si nuclei are mutually non-interactive. From the point view of thermodynamics, the phase transformation from vapor to solid via liquid phase is ascribed to the difference of Gibbs free energies. As we can see from the geometrical sketch in figure 4.5(c), the Gibbs free energy difference of such SiNR can be written as[15]

$$\Delta G = (\sigma_{liq-SiNR} - \sigma_{liq-vap}) \times A_1 + \sigma_{SiNR-vap} \times A_2 + \Delta g_{vap} \times V \qquad \text{Equation 4.3}$$

where $\sigma_{liq\text{-}SiNR}$, $\sigma_{liq\text{-}vap}$, and $\sigma_{SiNR\text{-}vap}$ are the interface densities of the Au-Si liquid solution with the SiNR, the Au-Si liquid solution with the Si vapor, and the SiNR with the Si

vapor respectively. A_1 and A_2 are the corresponding interface areas for the eutectic phase and SiNR respectively. Both of them can be assumed to have cylindrical shapes with different radius. Mathematically, A_1 and A_2 can be expressed as: $A_1 = 2 \cdot \pi \cdot R \cdot h$ and $A_2 = 2 \cdot \pi \cdot r \cdot H$ respectively. Δg_{vap} is the Gibbs free energy difference per unit volume from vapor to solid. It is given in terms of pressure (P), temperature (T), gas constant (R) and the molar volume (M_v) of the SiNR respectively. V is the volume of SiNR. The detailed mathematical derivation can be found at Wang, etc. al..[10] Based on the geometry described in figure 4.5 (b) and (c), the Gibb free energy of the SiNR can be written as

$$\Delta G = \pi \cdot R \cdot (\sigma_{SiNW-vap} - \sigma_{liq-vap}) \cdot \left(R - \sqrt{R^2 - r^2 + \frac{r^2 \cdot (R \cdot \cos\theta - r)^2}{R^2 + r^2 - 2 \cdot R \cdot r \cdot \cos\theta}} \right) +$$

$$2 \cdot \pi \cdot \sigma_{SiNW-vap} \cdot r^2 \cdot \left(1 - \frac{R \cdot \cos\theta - r}{\sqrt{R^2 + r^2 - 2 \cdot R \cdot r \cdot \cos\theta}} \right) + \frac{1}{6} \cdot \pi \cdot \left(\frac{R \cdot T}{M_V} \ln\left(\frac{C}{C^{eq}} \right) \right) \times$$

$$\left(\left(R - \sqrt{R^2 - r^2 + \frac{r^2 \cdot (R \cdot \cos\theta - r)^2}{R^2 + r^2 - 2 \cdot R \cdot r \cdot \cos\theta}} \right)^3 + 3 \cdot r^2 \cdot \left(R - \sqrt{R^2 - r^2 + \frac{r^2 \cdot (R \cdot \cos\theta - r)^2}{R^2 + r^2 - 2 \cdot R \cdot r \cdot \cos\theta}} \right) \times \right.$$

$$\left(1 - \frac{(R \cdot \cos\theta - r^2)}{R^2 + r^2 - 2 \cdot R \cdot r \cdot \cos\theta} \right) - r^3 \cdot \left(1 - \frac{R \cdot \cos\theta - r}{\sqrt{R^2 + r^2 - 2 \cdot R \cdot r \cdot \cos\theta}} \right)^3 -$$

$$\left. 3 \cdot r^3 \cdot \left(1 - \frac{R \cdot \cos\theta - r}{\sqrt{R^2 + r^2 - 2 \cdot R \cdot r \cdot \cos\theta}} \right) \times \left(1 - \frac{(R \cdot \cos\theta - r)^2}{R^2 + r^2 - 2 \cdot R \cdot r \cdot \cos\theta} \right) \right)$$

Equation 4.4

where, C and C^{eq} are the Si concentrations on the solid and liquid lines of the Au-Si binary phase diagram. In this equation and referring to figure 4.5 (d) and (e), the angle θ is the contact angle between the SiNR and Au-Si eutectic. The Gibbs free energy of SiNR

growth depends on the size of the liquid solution of Au-Si. The critical size of the nuclei of SiNRs is the minimum size of the SiNRs growth. Theoretically, the critical size of the nuclei of SiNRs can be attained when $\partial \Delta G(r)/\partial r = 0$.

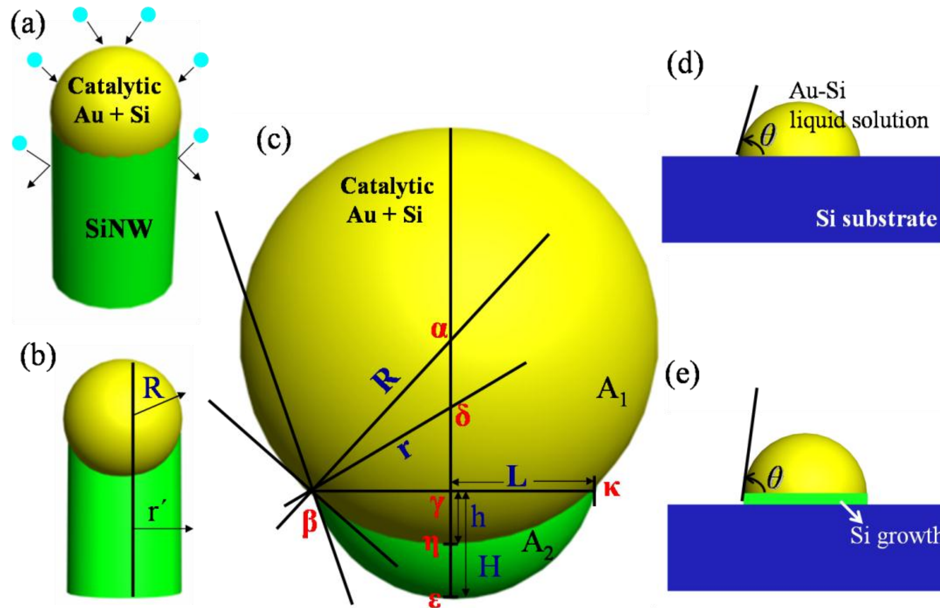

Figure 4.5 Schematic diagrams show the VLS mechanism and the SiNRs nucleation and kinetic growth processes. (a) The metal catalytic Au forms liquid solution with the Si and the solid SiNR, capturing and rejecting Si atoms from Si vapor phase. (b) The dimension description of the SiNR. (c) The thermodynamic nucleation for SiNR. (d) and (e) the contact angle varies during the SiNR growth.

By comparing with bulk single c-Si, SiNRs exhibit unusual phonon confinement.[16] The influences of lattice structures of SiNRs can be well revealed by micro-Raman spectroscopy. Figure 4.6(a) shows the Raman profile of bulk c-Si with a full width at half maximum (FWHM) of 3 cm^{-1} at 520 cm^{-1}. Such band is ascribed to the Brillouin zone centre longitudinal optical (LO) and transverse optical (TO) phonon mode in single c-Si. This assigned band shows significant red-shift when SiNRs are considered. As revealed in figure 4.6(b) and (c), the Raman profiles represent the different thicknesses of the Au

layer but the same lateral heights of the as-prepared SiNRs. The aspect ratios are 3:1 in this case. Both bands shift towards smaller wavenumber with respect to the one of bulk c-Si. But, there is no observation of any variation in the shape of the Raman profiles. Moreover, the Raman line-shape broadening is another characteristic for SiNRs. Besides, the Raman spectrum of SiNRs with aspect ratio of 10:1 (figure 4.6(d)) shows red-shift as well but the profile is asymmetric. Previous researches have mentioned that factors such as excited laser power, different laser wavelength and sample measurement temperature can give rise to such red-shift, line broadening and asymmetric characteristics.[17-19] In our experiment, all the samples were measured in ambient by the same laser excitation source and under the same integration time. Therefore, the red-shift and the symmetric line broadening are primarily due to the laser heating, and indeed, the SiNRs are very sensitive to such inhomogeneous local heating effect. By comparing with bulk c-Si and owing to the size effect, the SiNRs have much lower thermal conductivity. This phenomenon is not only restricted to SiNRs, but is a general feature of other nanocrystalline and nanotructural Si materials. Due to relative large aspect ratio for the longer SiNRs, local heating by laser can create much more free charge carriers. These charge carriers can interfere with the Si phonon line and gives a result of an asymmetric Fano line shape.[20-22] Therefore, for SiNRs with large aspect ratio, the corresponding Raman spectrum in figure 4.6(d) shows both red-shift and asymmetric characteristics.

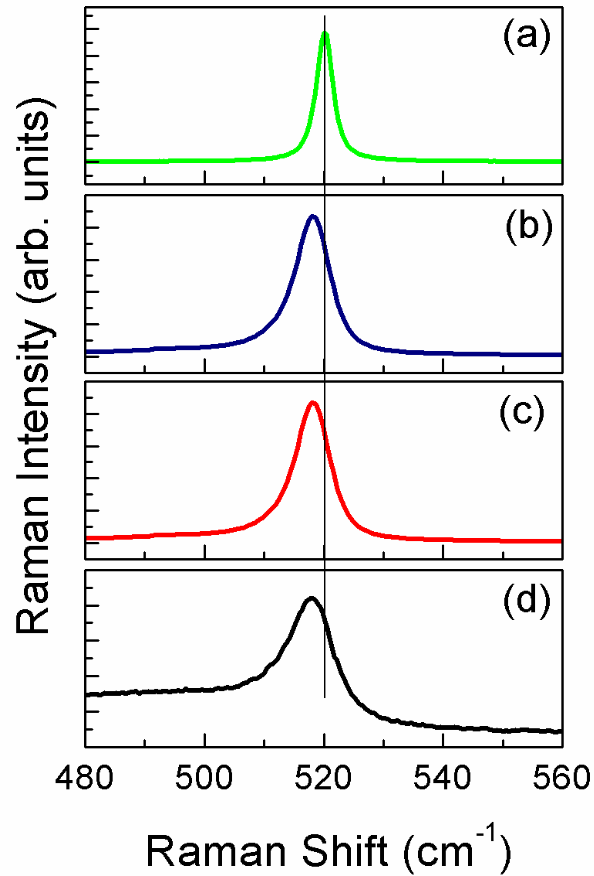

Figure 4.6 Raman spectra for (a) Bulk c-Si wafer. (b) and (c) SiNRs with same aspect ratio of 3:1 but are different in the time of Au coating, 10s and 20s respectively. (d) SiNRs with aspect ratio of 10:1.

4.4 Summary

In this chapter, the VLS method has been adopted for SiNWs and SiNRs growths on the (111) oriented c-Si wafers via Ebeam evaporation system. The formation of Au droplets on the oxide-free Si surface has been studied. The initial stage of the Au-induced Au-Si eutectic formation and the growth of SiNWs and SiNRs have been observed and studied based on the thermodynamic consideration.

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Chapter 5 Silicon Twinning Superlattice and c-Silicon Nanodots for Future Nanoelectronic Applications

5.1 Silicon Twinning Superlattice

5.1.1 Introduction

With currently fast growth of interest in nanotechnology research, one of the most attractive representatives is superlattice structure. The conventional way of fabricating high quality superlattice structure requires that both materials are well lattice-match, to ensure the periodic heteroepitaxy. Failure to meet this condition results in large number of defects and dangling bonds in the vicinity of the interface. The large amount of accumulated defects tends to degrade the charge transport across the interface. This is primarily due to charge scattering. In the recent years, researchers have gradually turned their attention to "heterojunction" which consists of a same material but with different crystalline phases (poly-type), such as wurtzite/zinc-blende or lonsdaleite/diamond heterostructure (SiC and ZnS being typical examples).[1-3] The primary desirable properties like defect-free, highly coherent, and lattice-matched, are retained due to involvement of only one chemical constituent. Superlattice formed by one of the most important representative semiconductor material, Si, has believed possessing some advantages such as absence of alloy scattering and interface broadening by interdiffusion. Almost two decades ago, Z. Ikonic et. al. have postulated the stacking fault induced Si twinning superlattice.[4] In their theoretical studies, the main focus was about the

electronic properties of the proposed Si twinning superlatice.[5,6] But, the idea also brings us to the field of planar defects in crystal growth. It is also known as stacking faults that we shall briefly discuss here. Stacking faults are the most common types of defects in diamond (e.g. Si) and zincblend crystalline type structures (e.g. GaAs), as well as in many face-centered-cubic (f.c.c.) metals. They are created when changes of the atomic plane stacking sequence in the crystalline (111) direction which corresponds to the lowest formation energy. The most common stacking fault is known as the twinning stacking fault. It comprises a sequent layers which are arranged periodically in space without breaking bonds at the interface of two adjacent layers. When the twinning stacking fault yields multiple layers with a few nanometers thick for each layer, it refers to twinning superlattice structures. The concept of obtaining twinning superlattice structure can be understood by cutting a perfect crystal, such as $AA'BB'CC'A|A'CC'BB'AA'$, into two and rotating half of the crystal by 180° about the bond axis. In order to ensure the absence of breaking bonds at the cutting edge, those dangling bonds should be reconnected. Therefore, at all the interfaces of twinning superlattices, the bond lengths and angles are preserved and no dangling bonds are generated.

Even up to date, the fabrication of Si twinning superlattice still relies on introducing an extra layer, such as Boron (B).[7-9] This B layer is able to reconstruct the Si (111) crystalline phase upon high temperature annealing (between 900 ^oC and 1250 ^oC). B appears as a monolayer at the boundaries of each pair of adjacent Si layers. Indeed, the exact physical mechanism involved has not been precisely understood. However owing to

the large difference in lattice constants between B and Si, the epitaxial growth of Si can yield large amount of planar dislocations. Indeed, it is so difficult to find a suitable lattice-matched material with Si except Ge nowadays. In contrast to previous reports, we would like to demonstrate here a novel approach for producing coherent periodic Si structure with the same crystalline structure but difference in the lattice spatial arrangement. This twinning Si superlattice structure can be distinguished from poly-type Si in the sense that only single crystalline phase is involved. In our scheme, we used Al-mediate or Al-induced method to fabricate not only the c-Si at reduced temperature (~ 450 ^{o}C) but also to generate coherent Si twinning superlattice in a long range order fashion. By comparing with B induced twinning superlattice, the physical mechanism is likely due to interdiffusion between Al and Si. The deposition temperature of Si at 450 ^{o}C was too low for the Si adatom to crystallize at the surface. However, with the assistance of the catalytic Al, both Si and Al can easily form a miscible solid solution at that temperature. Indeed the poly-Si film fabricated by this Al induced crystallization (AIC) method was successfully demonstrated in earlier chapters. Unlike those B induced Si twinning superlattice, at which a monolayer of B appears between layers, there is no residual metal Al observed at the twinning interface. However, some Al atoms doped in the Si lattice gives rise to p-type Si.[10] This has been verified from our previous experience in the poly-Si thin film fabrication. We suggest this twinning supperlattice fabrication method is the third way of achieving coherent twinning superlattice with single crystalline phase and absence of impurity at the twinning junction.

5.1.2 Experimental procedures

The experiment was conducted in high vacuum Ebeam evaporation system. Prior to the fabrication, the glass substrate undergoes necessary cleaning process. Oxygen plasma was used to ensure the dust-free of the glass substrate surface. The Al was initially deposited onto glass with a deposition rate of 6 nm/min at room temperature. The thickness of the as-prepared films can be well controlled by a build-in thickness controller. The thickness of Al layer is usually within the range of 15nm to 20 nm. Afterwards, the substrate temperature was quickly increased up to 450 ^{o}C. The deposition of Si proceeded under this temperature. The thickness of Si was varied from 5nm to 10nm. The interdiffusion of Al and Si occurs at this temperature. This gives a rise to Si crystallization. For each deposition of Si with a desirable thickness, the sample experienced post-annealing for 15min prior to the next Si deposition. Al always diffused to the top surface of the sample and therefore was used as the metal-induced catalytic layer for the subsequent deposition of Si. After the fabrication, the sample was naturally cooled down to room temperature. TEM was used to characterize the sample structure. Non-destructive micro-Raman spectroscopy was carried out in ambient.

5.1.3 Results and Discussion

Figure 5.1 (a) shows the TEM image of Al induced crystallization of Si. The resultant Si film shows crystalline structure which is in close contact with the amorphous glass

substrate. The physical mechanism based on thermodynamics has been studied in the chapter two. Here, we notice that the dislocation which is indicated by dotted red circle in figure 5(a) sometimes appears during the crystal growth. The inset shows the high resolution TEM image of the AIC process generated dislocation. However, the dislocation in this case only occurs accidently. In other words, we can not predict when and where the dislocation comes up. In the AIC process, the interdiffusion occurs between Al and Si is primarily dominated by interstitial solid solution diffusion. Al, which captures less energy to escape from the crystalline lattice of the as grown Si within a single grain can easily produce a point defect. This is commonly happened in the conventional AIC process for producing poly-Si thin films. In the Si twinning superlattice scheme, the Al generated defect or dislocation actually plays an important role.[11] The low magnification cross section TEM image of the poly-Si twinning superlattice is shown in figure 5(b).

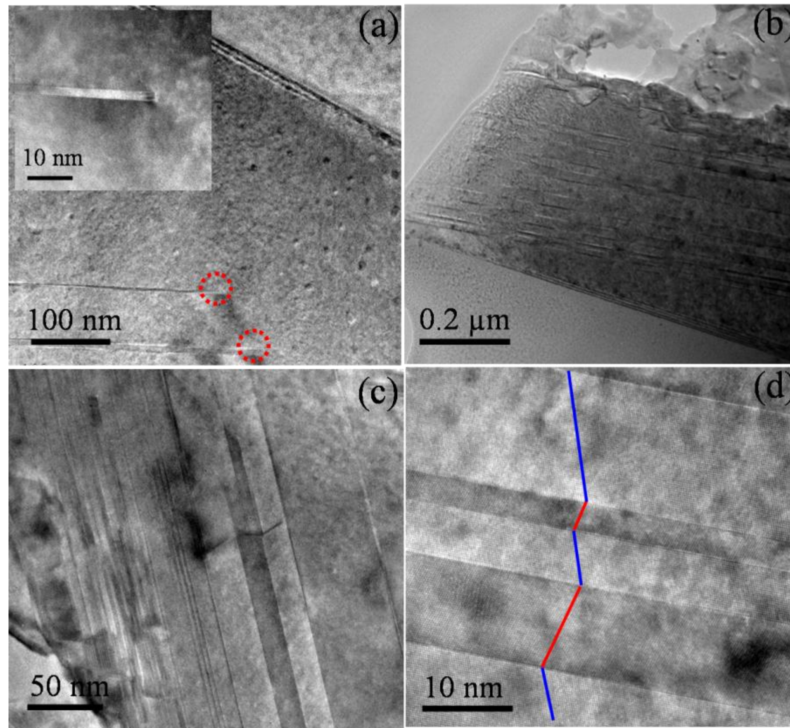

Figure 5.1(a) The TEM image of AIC Si thin film with appearance of dislocation (red dotted circle), the inset shows the HRTEM image of the dislocation during crystal growth. (b) Low magnification TEM image of Si twinning superlattice. (c) Si twinning superlattice growth within a single Si grain. (d) HRTEM image of Si twinning superlattice.

Evidently, the growth of the poly-Si superlattice is not along with the normal direction to the glass substrate. It displays the long range order periodicity, and the out-diffused Al forms on the top of the sample. In the AIC process, the interdiffusion between Al and Si initially precedes at the metastable phase which is at the interface of Al and Si. The interdiffusion mechanism is ascribed to the difference in the gradient of concentrations and the chemical potentials. Upon 450 ^{o}C thermal treatment, the Si tends to diffused downward to glass substrate and form nucleation site. This leads to the further grow of Si

grain. However, the majority of catalytic Al can be found at the Si grain boundaries until it absolutely diffuses above poly-Si. Therefore, the Si grain boundary has to accommodate a misfit through a grain boundary dislocation, which is generated by Al diffuses via Si grain boundary. Figurer 1(c) shows the poly-Si periodic superlattice at the grain boundary (red dotted circle). At location close to the grain boundary, it suggests that the Si twinning superlattice can not grow through the grain boundary but is confined within a single Si grain. Furthermore, the band width of the single twin seems to be narrow at the position close to the Si grain boundary. By observing the high resolution TEM image in figure 1(d), the Si twinning superlattice follows the zig-zag path.

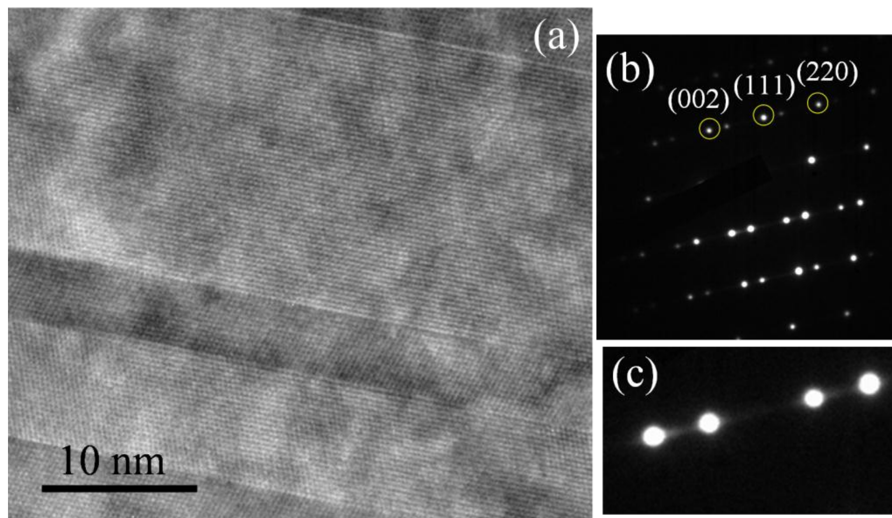

Figure 5.2 (a) High resolution TEM image for Si twinning superlattice with sharp boundaries at the twinning sites. (b) The SAEP pattern captured from Si twinning superlattice. (c) A magnified view of the SAED pattern.

As we can see from figure 5.2(a), the Si twinning superlattice shows distinct and sharp boundaries at the twinning sites. Apart from Si crystalline lattice planes, there has no impurity phase. This can be also revealed from selected area electron diffraction (SADP)

which is as shown in figure 5.2(b). It exhibits a multiple of six bright spots in a six-fold symmetry corresponding to the Si (111) single crystal direction. In addition, the magnified image of the extended diffracted spots which is as shown in figure 5.2(c) evidently indicates the long periodic superlattice structure.

Figure 5.3 shows the corresponding Raman spectra for the Si twinning superlattice (figure 5.3(a)) and single crystalline Si (figure 5.3(b)). By comparison, it clearly manifests two distinct features. The sharpness of the line appears at 520 cm^{-1} means a high degree of crystal perfection. Since the as-fabricated Si twining superlattice is included within Al-induced poly-Si grain and the actual Si crystalline structure is distorted, the expected Raman spectrum for Si twinning superlattice shows asymmetric broadening characteristic.[12] In addition, owing to the absence of heterojunction induced strain effect for Si twinning superlattice, a slight shift of the Raman spectrum of the Si twinning superlattice toward smaller wavenumber reflects the present of Al doping.

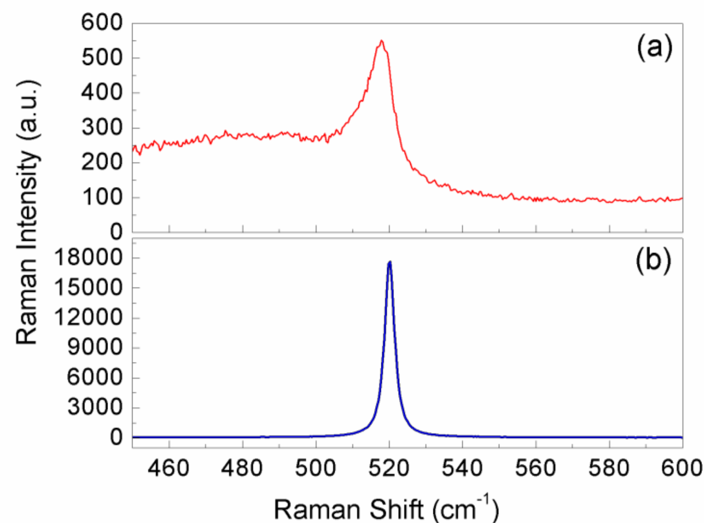

Figure 5.3 Raman spectra for (a) Si twinning superlattice and (b) single c-Si.

5.1.4 Summary

Ebeam evaporation method fabricated coherent poly-Si twinning superlattice on glass substrate has been successful demonstrated. The catalytic Al has the functions of producing c-Si at reduced temperature and generates the stacking fault at the as-grown Si grain boundary. This Si twinning superlattice can be classified as the third type twinning superlattice together with the poly-type superlattice and B induced twinning superlattice.

5.2 Crystalline Silicon Nanodots

5.2.1 Introduction

With current explosive growth of interest in graphene, we aimed at introducing semiconductor nanostructure such as c-Si nanodots (c-SiNDs) with graphene. Graphene is a two dimensional (2D) sp^2-bonded carbon atoms arranged in honeycomb lattice.[13-15] Its high intrinsic carrier mobility (~200,000 $cm^2V^{-1}s^{-1}$) and near ballistic transport at room temperature make it a promising candidate for future nanoelectronic applications, such as p-n junction diodes, high-speed field effect transistors (FET) and low-noise electronic and optical sensors.[16-19] Owing to the low density of states near the Dirac point and extremely large surface-to-volume ratio, single-layer graphene is very sensitive to modification by nanostructures.[20,21] Previous researches have shown that graphene modified by semiconductor nanodots (SNDs) can provide close-to-ideal transport pathway for charge carriers.[22] Some recent studies report on introducing random SNDs

on reduced graphene oxides (RGOs).[23,24] However, the electrical characteristics of RGOs are undesirable because of the low charge carriers mobilities (<1 $cm^2V^{-1}s^{-1}$) and the hopping transport phenomenon between each adjacent RGO layers.[25] Therefore, SNDs directly grown on high quality single-layer graphene is necessary. Indeed, fabricating large-scale, high quality and uniform SNDs on graphene is a very important step towards making semiconductor and graphene based micro- and nanoelectronic devices. In this project, we chose Si as the material for SNDs because it is still the standard semiconductor material for electronics nowadays.

5.2.2 Experimental Procedures

We used ultrathin anodic porous alumina (UAPA) template and a nonlithographic approach to fabricate uniform c-SiNDs on pristine single-layer graphene. In our experiment, the UAPA template with lateral thicknesses ranging from 80 nm to over 1μm is a structurally controllable template for cost-efficiency and large-scale nanofabrication.[26] As shown from the schematic diagram in Figure 5.4(a), a commercial high purity Al foil was dealt with a two-step electrochemical anodization. The schematic picture of the as-prepared UAPA is displayed in Figure 5.4(b) and (c). The transferring process of the UAPA involves PMMA coating, residual polycrystalline Al (poly-Al) etching and pore widening. Prior to UAPA transfer and SNDs growth, a single-layer graphene made by CVD technique was initially transferred onto SiO_2/Si substrate (Figure 5.4(d) and (e)). Then, the UAPA layer coated with PMMA, which is shown in Figure 5.4(c), was transferred on the top of this single-layer graphene/SiO_2 (0.3 μm)/Si (500 μm)

(Figure 5.4(f)). The PMMA was easily dissolved in acetone (Figure 5.4(g)). Technically speaking, to fabricate large-scale c-SiNDs at low temperature (<500 ^{o}C) is highly desirable. At much higher temperature, for example close to the crystallization temperature of Si (> 1000 ^{o}C), will destroy the UAPA pattern. Here, we used Ni-induced crystallization method to fabricate c-SiNDs at 400 ^{o}C. The catalytic Ni tends to form solid solution with Si at this temperature. The interdiffusion between Si and Ni leads to the nucleation and crystallization of Si inside each UAPA pore. Owing to the gradient concentration difference in Si and Ni, the final step of the Ni-induced crystallization is a completely interchange between Ni and Si (Figure 5.4(h)). Finally, uniform c-SiNDs on single-layer graphene can be obtained after removing the UAPA template. The corresponding schematic picture is shown in Figure 5.4(i).

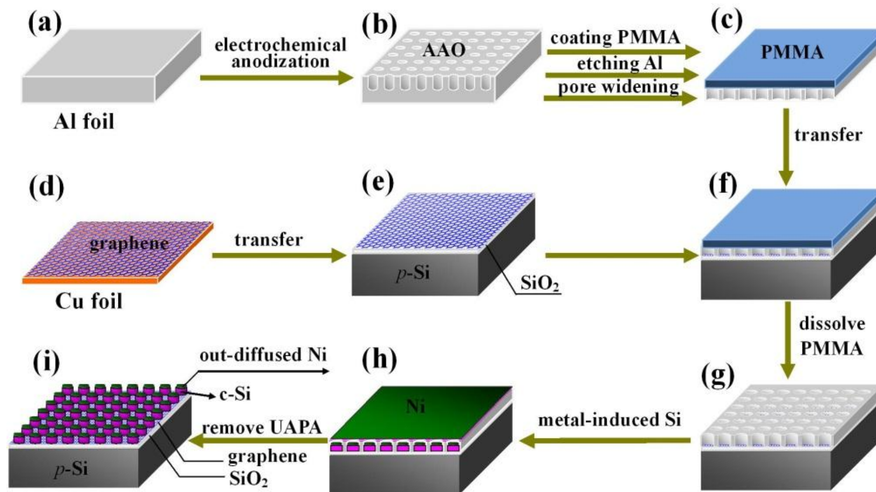

Figure 5.4 Schematic diagram of fabrication process for Ni induced Si nanodots arrays on graphene: (a) Al foil preparation. (b) Ultrathin anodic porous alumina (UAPA) fabricated by a two-step electrochemical anodization. (c) Transferring process includes PMMA coating residual Al removing and pore widening. (d) Single-layer graphene prepared by CVD technique. (e) Transferring graphene onto SiO_2/Si substrate. (f) Transferring UAPA onto the graphene/SiO_2/Si. (g) Dissolving PMMA. (h) Ni-induced Si crystallization at 400 ^{o}C. (i) Ni-induced c-Si nanodots formation.

5.2.3 Results and Discussion

Figure 5.5(a) shows a TEM image of the pristine single-layer graphene. The red dotted circle indicates the presence of graphene ripples which is a typical characteristic of a single-layer graphene.[27] The selected area diffraction pattern (SADP) shown in the inset displays the hexagonal symmetry of the diffracted spots. Two of them have been clearly indexed with (110) and (101). The zone axis being [001] is perpendicular to all the electron diffracted spots. The inset of Figure 5.5(b) illustrates the photographic image of the UAPA template transferred on top of 1 cm^2 single-layer graphene/SiO_2/Si. Figure 5.5(b) shows a FESEM image of the UAPA template. Excellent self-ordering of the hexagonally close-packed alumina cells in each cell is observed. High magnification FESEM image in Figure 5.5(c) shows that the UAPA possesses a close-packed hexagonal array. For each cell, the cell size and the pore diameter are 105 nm and 60 nm, respectively. The cross-sectional FESEM image revealed in Figure 5.5(d) shows the straight parallel through-hole UAPA arrays with the lateral height of 160 nm. The interactive force between the UAPA and the single-layer graphene is guaranteed by van der Waals force.

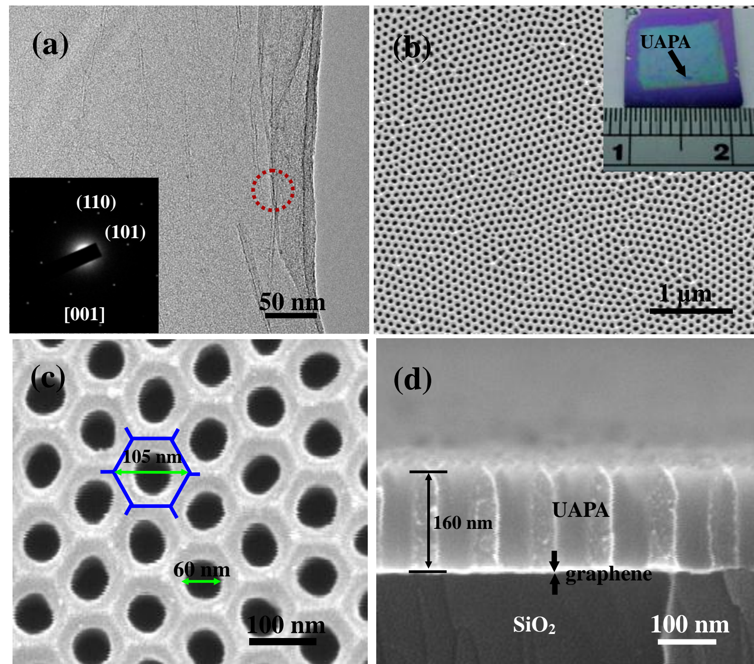

Figure 5.5 (a) TEM image of single-layer graphene, inset shows corresponding electron diffraction pattern. (b) Top-view of SEM image of the UAPA template, inset shows a photographic image of the UAPA template on graphene/SiO_2/Si. (c) High resolution FESEM image of the UAPA. (d) Cross sectional SEM image of the template.

After partially removing the UAPA template, a number of Ni-induced c-SiNDs on single-layer graphene is exposed. In addition to this, the residual template together with out-diffused Ni layer can be also observed. These are clearly revealed in figure 5.6(a). Further evaluation of the area coverage of Ni-induced c-SiNDs can be seen from figure 5.6(b). According to the inset of figure 5.6(b), the average nanodot density based on the SEM images was calculated to be around 1.2×10^{10} /cm^2. The diameter of the nanodots is 60 nm, and the spacing between the each pair of nanodots is 105 nm. The result is consistent with the previous observed inter-pore distance. The same sample was examined by AFM and the corresponding AFM image with 2 μm × 2 μm in area is shown in figure 5.6(c). Four c-Si nanodots in the AFM image were randomly chosen for

depth profile measurement. Figure 5.6(d) indicates the lateral height of the as-prepared

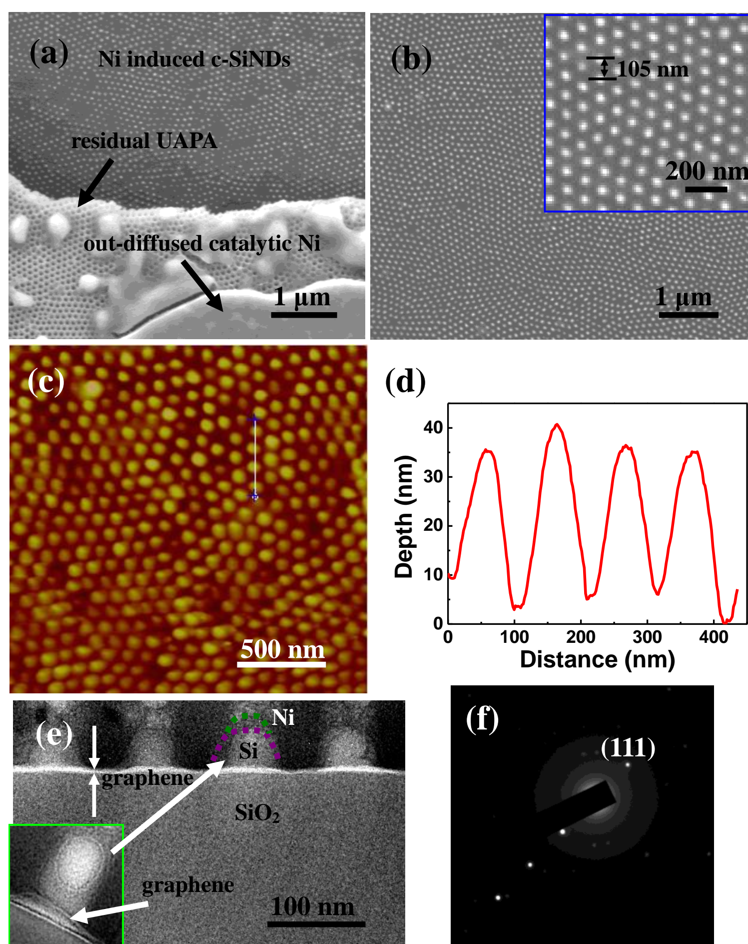

Figure 5.6 (a) Top-view FESEM image of Ni-induced c-SiNDs on single-layer graphene with remaining UAPA template. (b) The well-ordered nanodots arrays on graphene after completing lift-off. (c) AFM image of the nanodots on single-layer graphene. (d) The corresponding depth profile of the nanodots on graphene. (e) Cross-sectional TEM image of the nanodots on graphene/SiO_2/Si. (f) The corresponding electron diffraction pattern of the nanodot.

Ni-induced c-SiNDs is 35 ± 5 nm. Furthermore, as we can see from the TEM image in figure 5.6(e), four c-SiNDs are well aligned in a horizontal plane. The lateral height for each c-SiND is 35 nm which is consistent with the result of AFM depth profile measurement. The SAED (figure 5.6(f)) captured for an individual NIC SiND indicates single crystalline quality.

Raman spectroscopy plays an important role in studying and characterizing graphitic materials, especially when considering heterostructure. Graphene, in this regard, can be identified in terms of number and orientation of layers by means of inelastic light scattering. Furthermore, it also performs as a probe for heterojunction induced strain effect. A common feature of pristine graphene is shown in Figure 5.7(a). The graphitic (G) band which appears at 1591 cm^{-1} is due to C-C sp^2 bond. The G band corresponds to the E_{2g} phonon at the Brillouin zone centre.[28] It represents the crystallinity of graphene. The band located at 2706 cm^{-1} is caused by double resonance process activated second-order Raman scattering near the boundary of the Brillouin zone of graphene.[29] It is usually denoted as G´ or 2D band. Moreover, it is recognized as a fingerprint for single-, bi- and few layer graphene. In single-layer graphene, 2D band shows a highly symmetric single peak. But for bi-layer graphene, it tends to split into four components which correlated with four virtual transitions. In spite of this, the intensity ratio of I_{2D}/I_G is an alternative indicator to judge the number of graphene layers involved. For our CVD growth pristine single-layer graphene, the intensity ratio of I_{2D}/I_G is close to 0.5. This implies our graphene is single-layer.[30] Owing to the excellent crystalline quality, our graphene shows the absence of defective (D) band at 1364 cm^{-1}. Such band is due to the breathing modes of sp^2 atoms and requires a defect for its activation.[28] By comparing with the pure graphene sample, the Ni-induced c-SiNDs coated graphene exhibits an increased intensity ratio of I_{2D}/I_G up to 1.7 and a noticeable D band. According to Figure 5.7(b), the

2D bands of the pristine graphene and the one with nanodots are well fitted by highly symmetric Lorentzian curves. Besides, there is no splitting of the 2D band, indicating that the only double resonance (DR) process for such decorated single-layer graphene.[31] Therefore, although the intensity ratio of I_{2D}/I_G is changed after the fabrication of nanodots, our experimental result reveals that it has no effect on the number of graphene layers. Moreover, the rise of D band is observed at 1364 cm^{-1}. We attribute the D band to ion implantation during PLD fabrication process because it is known that laser ablation is a process of producing high energetic species such as ions, atoms and molecules. In figure 5.7(b), a significant blue-shift of the 2D band by 14 cm^{-1} can be observed. We considered two primary reasons; one is thermal effect and the other is Ni-induced c-SiNDs. Nevertheless, we have found that the samples with the structure of single-layer graphene/SiO_2/Si, annealed at 400 ^{o}C in high vacuum (2×10^{-6} Torr) for 1 h yield the same Raman result as the one of pristine graphene without thermal treatment. Therefore, we believe that the nanodots cause the blue-shift of the 2D band. In figure 5.7(c), the blue-shift of the G band by 10 cm^{-1} can also be observed for the sample with nanodots. Both blue-shifts are likely due to significant compressive strain in the graphene surface.[32] The strain comes from the lattice mismatch between graphene and the as-deposited c-SiNDs. Based on the Raman spectrum, the strain ε can be deduced mathematically according to $\varepsilon = (\Delta\omega/\ \omega)/\gamma$, where $\Delta\omega$ is the change in Raman shift from the unstrained value ω, and γ is the Grüneisen parameter. The γ value is around 1.8 for the G mode. Thus, the calculated ε for G band is 0.3%.

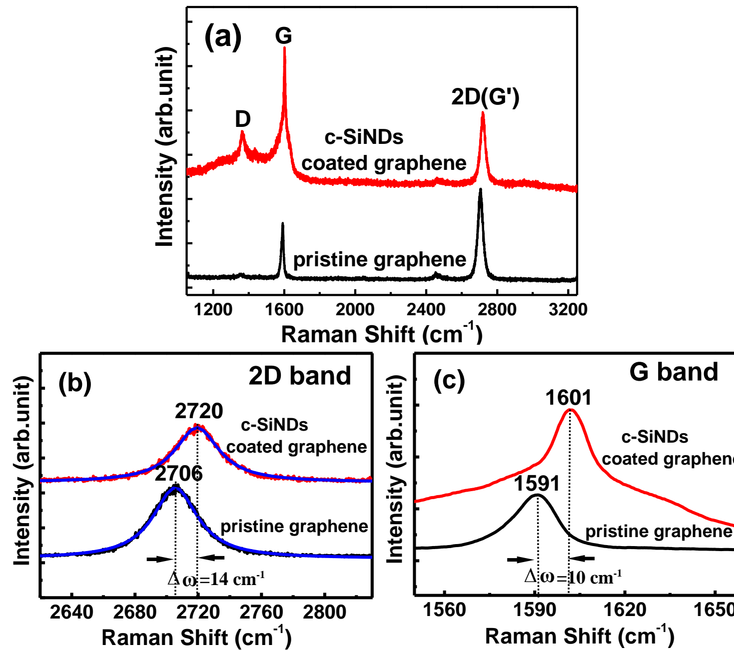

Figure 5.7. (a) Raman spectra of single-layer graphene with (red) and without (black) the nanodots. (b) The Raman spectra of the 2-D bands with lorentzian fitting. (c) The Raman spectra of the G bands.

Figure 5.8(a) shows the I_{ds}-V_g transfer characteristic of the pristine graphene field effect transistor (FET) device. The V_{ds} was set to be 0.5 V. The I_{ds}-V_g curve is constituted of both hole branch (negative) and electron branch (positive). The curve exhibits a symmetric ambipolar transfer characteristic. In this case, the gate voltage (V_g) at the lowest point of the I_{ds}-V_g curve is known as the Dirac point or neutrality point (V_{dirac}). A slight mis-match of the hysteresis can be observed when the forward and the reverse V_g bias voltages are applied. This mis-match is primarily due to charge trapping effect in graphene.[33,34] During the CVD growth, the morphology or the grain size of graphene replicates the one of Cu foil. Charge accumulation at the grain boundaries can lead to

charge scattering. Thus, charge trapping effect mainly comes from two reasons, one is material itself (single or polycrystalline materials) and the other is due to fabrication technique. In our experiment, we found the charge trapping effect can be greatly reduced when the Ni-induced c-SiNDs was introduced into graphene based FET device. The I_{ds}-V_g transfer characteristic curve of the graphene with nanodots FET device is shown in Figure 5.8(b). This gives a result of asymmetric ambipolar transfer characteristic. Furthermore, the entire curve shifts towards positive. As a consequence, the corresponding V_{dirac} is 18 V. This is in direct contrast with the one of the pristine graphene fabricated FET device. Similar phenomenon was discovered when potassium (K) doped into graphene.[35] Moreover, the major part of this I_{ds}-V_g curve is attributed to the hole branch, which indicates the injected charge carrier from nanodots to graphene is hole. In other words, the graphene was doped by positive charge. Based on this I_{ds}-V_g curve, the excess hole concentration can be calculated as

$$n_{\text{ex-h}} = \frac{\varepsilon_0 \varepsilon_r}{e d_{\text{ox}}} \Delta V_{\text{dirac}} \quad (1)$$

where, ε_0 is the permittivity of vacuum, ε_r is the relative permittivity of SiO_2 (3.9), e is the electronic charge (1.602×10^{-19} coulombs) and d_{ox} is the thickness of SiO_2 (300 nm). Thus, the calculated excess hole concentration, $n_{ex\text{-}h}$, is 1.280×10^{12} cm^{-2}. Besides, field effect mobilities ($\mu_{e,h}$) can be calculated as[36]

$$\mu_{\text{e,h}} = \frac{\text{L}}{\text{W}C_{\text{ox}}V_{\text{ds}}} \frac{\Delta I_{\text{ds}}}{\Delta V_{\text{g}}} \quad (2)$$

where L and W are the length and the width of the FET channel, respectively. C_{ox} is the gate oxide capacitance and can be expressed as $\varepsilon_{ox}\varepsilon_o/d_{ox}$. $\triangle I_{ds}/\triangle V_g$ is the transconductance in the linear regime of the I_{ds}-V_g curve. For the pristine graphene-based FET device and referring to the corresponding I_{ds}-V_g curve in Figure 5.8(a), the electron and hole mobilities are 65 $cm^2V^{-1}s^{-1}$ and 62 $cm^2V^{-1}s^{-1}$, respectively. The relatively low charge mobilities in our experiment are ascribed to long channel length (100 μm) which definitely increases the diffusion length for charge carriers.[37] We adopted such channel length because it is adequate for our measurement. Some calculations were carried out for the sample with Ni-induced c-SiNDs, the electron and hole mobilities are 25 $cm^2V^{-1}s^{-1}$ and 43 $cm^2V^{-1}s^{-1}$, respectively. By comparison, the decrease in charge carriers mobilities are due to the introduction of some scattering centres within graphene. In addition, for the sample with nanodots, the difference between hole and electron mobilities is relatively large. This also verifies the majority charge carrier in our graphene is hole. Therefore, the Fermi energy level of the graphene has been reduced. Regarding the on/off current ratios for both samples in Figure 5a,b, the on/off ratio is increased from 1.2 to 2.3 at V_g = -50 V when nanodots are taken into account. Figure 5.8(c) and (d), which corresponds to both samples in Figure 5.8(a) and (b) respectively, show the I_{ds}-V_{ds} output characteristics at five different V_g (-50 V, -25 V, 0.0 V, 25 V and 50 V). In contrast, the sample with nanodots has more degree of freedom on tuning I_{ds}-V_{ds} output characteristic.

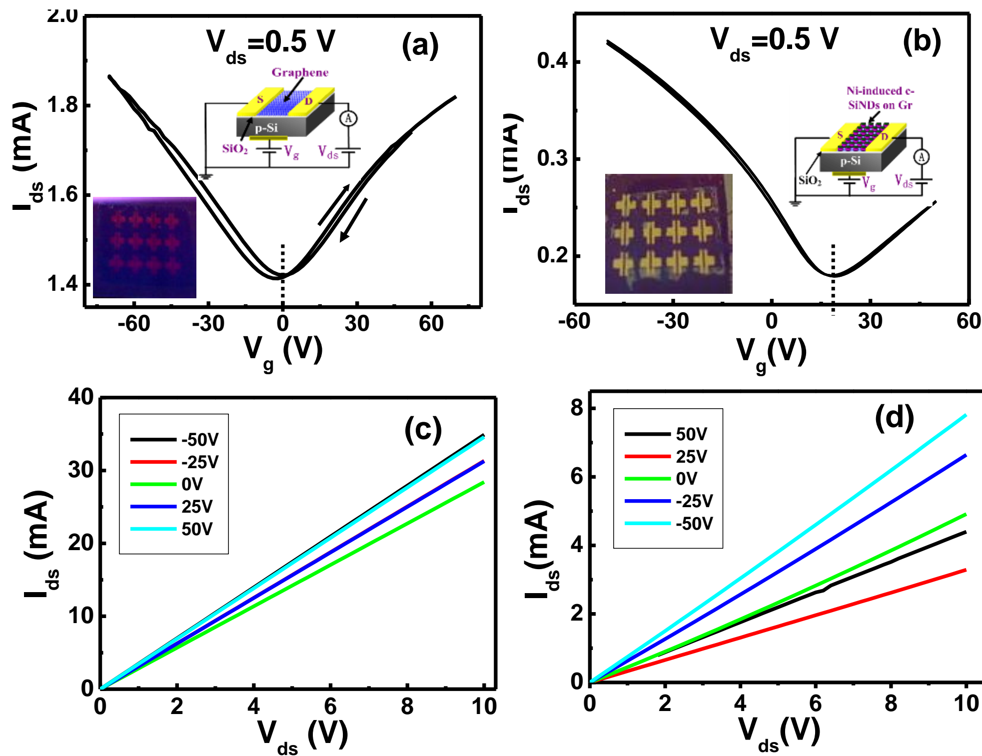

Figure 5.8 (a) I_{ds}-V_g transfer characteristics of a pistine single-layer graphene based FET device at V_{ds}=0.5 V. The dotted lines indicates the Dirac point (the minimum conductance point). The V_g sweeping direction is indicated by the arrows. Inset shows an optical microscope image and schematic picture of the FET device layout. (b) I_{ds}-V_g transfer characteristics of Ni-induced c-SiNDs fabricated on graphene. Inset shows an optical microscope image and schematic picture of the FET device layout. (c) The corresponding I_{ds}-V_{ds} output charateristics of single-layer graphene based FET tested at 5 different gate voltages (V_g=-50 V, -25 V, 0.0 V, 25 V and 50 V). (d) The corresponding I_{ds}-V_{ds} output characteristics of Ni-induced c-SiNDs and graphene based FET tested at 5 different gate voltages (V_g=-50 V, -25 V, 0.0 V, 25 V and 50 V).

5.2.4 Summary

Large scale and uniform c-Si nanodots pattern on pristine single-layer graphene has been fabricated via UAPA and Ni-induced crystallization methods. The c-Si nanodots decorated single layer graphene shows significant variations. The appearance of D band is due to ion implantation during PLD process, while the shift of 2D and G bands is because the consequence of c-Si nanodots generated strain effect.

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Chapter 6 Conclusions and Perspectives

In this thesis, we report studies of the fabrication processes of poly-Si thin films, Si nanowires, poly-Si twinning superlattice and c-Si nanodots. All of these processes rely on the metal-induced crystallization (MIC) method. Different metals, such as Al, Ni and Au, have different eutectic temperatures at which they react with Si. Thus in experiments, we have the freedom of choosing various catalytic metals so as to grow the Si based structures at the desired temperature. The following paragraphs will be a summary for all the works that we have done in this project.

In chapter 3, I have demonstrated the fabrication of poly-Si thin film on soda-lime glass at 450 ^{o}C by E-beam evaporation via AIC technique. The entire deposition and, for some cases, post annealing were done in-situ within a single vacuum cycle. No native Al oxide layer was needed for AIC poly-Si film growth. The as-deposited Si tends to crystallize with and without post annealing. Only (111) preferred orientation thin film is obtained. From the Raman spectroscopy, prominent single crystalline phase was detected when the silicon thin films were deposited at 450°C. This is due to the formation of solid solution of Al and Si. The interdiffusion process occurs when the thermal requirement is satisfied. We have obtained poly-Si thin films with grain size more than 5 μm by subsequent annealing at 450 ^{o}C. The low temperature AIC can be explained with the aids of FESEM and EDS characterizations. BF-, HR- TEM images and DP verify the large crystalline size and excellent quality of the thin films. Judging from the results of Hall measurement,

it indicates that our AIC fabrication technique based on E-beam evaporation has excellent capability in producing high quality poly-Si thin films on Soda-lime glass at low temperature. I also used the 500 nm poly-Si coated on ITO/glass substrate as an epitaxial seed layer. From the structural quality of the as-fabricated solar cell and its corresponding IV-characteristics, our low temperature poly-Si thin film fabrication technique can be used for cost-reduction and large-scale solar cell production. In fact, photonic industries are usually concerned about the samples' surface roughness. Although the poly-Si thin film has desirable crystalline and electrical properties, the final stage which involves the complete interchange of Al and Si always leaves the Al-Si eutectic phase at the interface. The conventional chemical wet-etching can not yield a good and smooth poly-Si surface. In consequence, it will lead to current leakage, charge random scattering at the interface and defect generation. Future work includes finding an appropriate way to smooth out the poly-Si thin film surface. Chemical mechanical polishing and electrochemical polishing are supposed to be suitable candidates here.

In chapter 4, the SiNWs and SiNRs with different size and aspect ratios can be fabricated by EBE system at reduced temperature of 500 ^{o}C via VLS method. By comparing with CVD technique, the Si atoms in the vapor phase can be directly produced from the evaporation source by EBE and impinge onto Au-Si liquid solution. We have emphasized that thermodynamics plays a key role in understanding the kinetic mechanism of this VLS method. Furthermore, the red-shift, the line-width broadening and the band shape of

the Raman spectra of the SiNRs with different aspect ratios have been studies. Raman spectra thus show confinement signatures for the SiNRs. For solar cell applications, the aim of introducing Si nanorods is for light trapping and charge mobility improvement. Therefore, the growth of Si nanorods on the Si thin film is proposed to have some improvement in the efficiency for solar cell applications. However, such work can only be done on high quality Si thin film with very smooth surface, similar to the Si nanorods that I have achieved on Si wafer. Therefore, the growth of Si nanorods on Si thin film in future has close connection with previous work done in this project.

In chapter 5, we have showed the fabrication of Si twinning superlattice on glass substrate with single crystalline phase. It opens a new fabrication method when comparing with the epitaxial growth of heterojunction superlattice, poly-type superlattice and B-induced twinning superlattice. However, the formation of such impressive nanostructure has not been fully understood yet because it involves many physical mechanisms, such as Al-Si interdiffusion, Si crystallization, defect production and twinning formation. Therefore, more efforts are needed for the fundamental investigation in this field.

Lastly, the large scale and uniform 0-D Si nanodots were fabricated on single layer graphene was firstly demonstrated. This approach tends to connect the very classical and

standard electronic material Si with one of the most prevailing 2-D graphene. In additional to the demonstration of such nonlithographic technique which can be done in most laboratories, future work may involve producing nanoelectronic and nanophotonic devices.