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**Design of an Intelligent Switch for Fully
Integrated Power Nets**

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M.Phil.

The Hong Kong Polytechnic University

2007

The Hong Kong Polytechnic University

Department of Electronic and Information Engineering

Design of an Intelligent Switch for Fully Integrated Power Nets

Wong Siu Hong

A thesis submitted in partial fulfillment of the requirements for

the degree of Master of Philosophy

February 2007



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Abstract

of the thesis entitled ‘Design of Intelligent Switch for 42V DC Power Net’

Submitted by Wong Siu Hong

for the degree of Master of Philosophy

at The Hong Kong Polytechnic University at 12-02-2007

This thesis focuses on the structural design of a proposed intelligent switch system and demonstrates how the electrical power system of a vehicle can be simplified with advanced power management features by using the proposed intelligent switch system. The design concept of the proposed scheme is basically a DC power bus with a number of power switches controlled remotely by means of DC powerline communication. With the proposed system, users are able to manage and install any appliance into a vehicle without installing new wires. However, even though the AC powerline communication technology is mature and has been widely used in many applications, there is no DC powerline communication system in the market due to the technology limitations. The major difficulties of realizing DC powerline communication are due the low impedance and low frequency cut-off characteristics of the DC powerline, which introduces serious signal attenuation and distortion to the carrier signal. These problems lead to poor signal to noise ratio. In order to mitigate these effects, a high efficiency carrier transceiver which consists of a carrier transmitter and a carrier receiver is required for the intelligent switch system.

The proposed transmitter is basically an H-bridge switching circuit with a

capacitor and a 1:100 transformer connected in series. The H-bridge is designed to operate in switching mode to minimize power losses while the switching frequency of the switches is set slightly lower than the resonance frequency of the series capacitor and transformer. The capacitor and the transformer behave like a LC circuit and will resonance at the switching frequency and transmit a sine-wave like carrier to the powerline at high power efficiency. Data symbols '0' and '1' are modulated into continuous frequency changes. Since it is almost impossible to have an ambient noise varying at the same pattern as the modulated symbols and existing at the same time, the problem of noise jamming is minimized. Also since the transformer boosted up the current acquired from the power bus one hundred times, the signal to noise ratio can be maintained at an acceptable level. The design of the receiver is based on the simple ratio detector which has been widely used in commercial radio. The ratio detector converts frequency change into voltage variation, which will then be digitalized by an analog to digital converter (A/D converter) and decoded by a microcontroller. Since the transceiver circuitry is very simple and no special component is needed, the objective of developing a simple and low cost in-vehicle intelligent switch system is achieved.

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Chapter 1

Introduction

1.1 Motivation

In a rapidly growing society, efficient transportation is one of the major forces pushing the growth behind and is also an undividable part of our daily life. In order to adapt the ever changing needs of consumers while keeping good sale in the competitory automobile market, vehicle manufacturers make use of a lot of electronic equipment such as multimedia entertainment system and GPS (Global Positioning System) in their product to make driving and traveling more safe and comfortable. However, the additional electronic equipments increase both the material and assembling cost of vehicles production which eventually reflect in the selling price. In order to fight against competitors, vehicle manufacturers tend to simplify the infrastructure of their products to reduce production cost. Since modern vehicles are made of metal, which dominate over 80% of the total weight of a vehicle and are mostly distributed in the vehicle body and cable harness of electrical power system. The production cost and weight of a vehicle can be reduced effectively by reducing the use of metal, which also results in an efficient use of fuel. Since the cables of the in-vehicle electrical power system are made of copper which is expensive and heavy, in order to reduce the

material cost and weight of vehicles, the amount of copper wires must be minimized.

In modern vehicles, electronics are usually powered by a high capacity lead acid battery via a star-like cable harness. Though it is simple and direct, to fulfill the ever increasing demand of in-vehicle automation such as multimedia control, device failure acknowledgement and high level power monitoring, a conventional star-like power system with mechanical switches became inadequate since most of these operations require bi-directional data communication. The star-like configuration leads to high cabling complexity and also high material cost which results in high selling price of automobiles. In order to simplify the wiring system, several in-vehicle power control networks in bus topology have been proposed, such as CAN bus and LIN bus. They help in simplifying the wiring system by transforming the conventional star-like wiring system into a bus configuration. Both the CAN bus and LIN bus require a dedicated communication bus along with a power cable harness, which is a piece of wire installed around a car as a main trunk with many branches connected to the CAN/LIN controllers. With the additional communication bus, the structure of the power cable harness becomes flexible and the cabling material can also be reduced. As long as electrical power is deliverable, the power cable harness can be in a bus structure with tree type branches or a star structure with bus type branches and so on. However, though these bus type power control network help greatly in simplifying the in-vehicle electrical power system and cost cutting, it is not an optimized design. Since all electronic devices need power, power cable reaches everywhere electronic device is installed, the cost of the electrical power system can be further reduced by integrating the communication media into power bus.

1.2 Background

Nowadays, driven by the ever increasing demand of the consumer market of automobile, vehicles are not produced only for the purpose of transportation. Modern vehicles should provide a safe, comfort and enjoyable environment to the travelers. As electronics penetrate deeply to the design of automobiles, the controllability of the appliance in a vehicle has become a key issue that differentiating the value among vehicles. In the old days, before the hyper fast development of the semiconductor industries, the infrastructure of the electrical system of a vehicle is simple and the services provided by the system are limited to lighting, engine starting and other simple signal indications. However, along with the increasing of signal processing power with decreasing manufacturing cost, the incorporation of electronics in a modern vehicle has been vastly increased and so has the complexity and weight of the cable harness. The weight of the cable harness typically dominates 7 – 10% of the total weight of a modern vehicle which is leading to fuel wastage. Also since the cables are made of copper which dominates a large percentage of the manufacturing cost of a vehicle, to maintain competitive in the vehicle market, the structure of the electrical system in vehicles has to be simplified. In order to provide more automatic functions by stuffing electronic content into a vehicle, the vehicle manufacturers and researchers have been working on simplifying the electrical infrastructure by applying a communication network to vehicles that aims at reducing the weight and material costs of the cable harness, such networks are known as ‘automotive network’. These networks help in reducing the amount of cable used in the cable harness by sending control signal over a dedicated communication medium to control the appliances.

Other than using automotive network, simplification of the electrical power system can also be achieved by increasing the source voltage of the system. Because of the source voltage is increased, the entire electrical system is able to deliver more power through the cable harness at lower current. 42V DC has been globally agreed to be the highest DC voltage that can be safely used in a closed area and has become the standard power supply voltage of the new generation vehicles.

Although there have been a number of proposed approaches that aims at simplifying the electrical infrastructure and reducing the manufacturing costs of vehicles, however, not much research work had been report on optimizing the electrical system of a vehicle by integrating the communication medium into the power cable harness to facilitate high level in-vehicle power control and management.

1.3 Objective

Combining the mediums of data communication and power transmission is the fundamental concept of power communication technology. The idea of powerline communication has been proposed over 40 years. Such technology has been widely used in AC power systems in many aspects, such as the applications of home automation. However, despite of the popularity of AC powerline communication system, there are very few research focus on facilitating communication over DC powerline. The objective of this research is to develop an intelligent switch system which is able to control and monitor the appliances inside a vehicle by using the power cables as a communication medium. In the research, the characteristics of the in-vehicle DC power system will be studied; circuits of signal transceiver will be

designed; special communication schemes for facilitating communication over DC power net will be proposed and an intelligent switch system for 42VDC power net will be practically developed.

1.4 Outline of the Thesis

The thesis is consisted of six chapters, in chapter one, the structure of contemporary in-vehicle electrical power system is reviewed. In chapter 2, the design of in-vehicle power bus and the corresponding characteristic is introduced. In chapter 3, a novel design of high efficiency carrier transceiver for transmitting carrier signal over the power bus is proposed. The results obtained from both computer simulation and practical experiments show superior performance from the proposed transceiver circuit and proved that stable DC powerline communication is achievable. In chapter 4, an implementation of communication protocol with error handling is discussed. In chapter 5, the idea of multiple node intelligent switch system is presented. In this chapter, the performance of the whole proposed intelligent switch system with multiple nodes is presented. In the last chapter, suggestions of further improvement and application are presented.

Chapter 2

Basics of in-vehicle automation system

2.1 Introduction

As mentioned in Chapter 1, the focus of this thesis is on in-vehicle automation of motor vehicles. A lot of studies have stated that the amount of electronic contents in motor vehicles will be boosted by vehicle manufacturers who are trying to differentiate their products from others by means of electronic contents and the relative functionality, such as multimedia entertainment. Since all kinds of electronics in a vehicle are powered by a battery source through a cable network, in cases the demand of in-vehicle automation increases, the cable network becomes more complex and bulky. In order to simplify the cable system, numerous power system designs have been proposed. This chapter presents a brief introduction to the basics of in-vehicle automation and the popular cable network topologies. The corresponding operation principles and analytical models of automation systems are also reviewed.

2.2 14V DC electric power system

In general, the simplest in-vehicle electrical power system consists of a 12V battery power source, alternator, copper wires/cables, a number of consumers (appliances) and switches for turning the appliances on and off. In such design, the consumers are powered by the battery through dedicated cables and mechanical switches installed on the control panel of a vehicle which is basically a star-like power network with a battery placed at the centre as shown in Figure 2.1. Since it is relatively direct, effective and reliable, the star-like design has never been changed in the past decades.

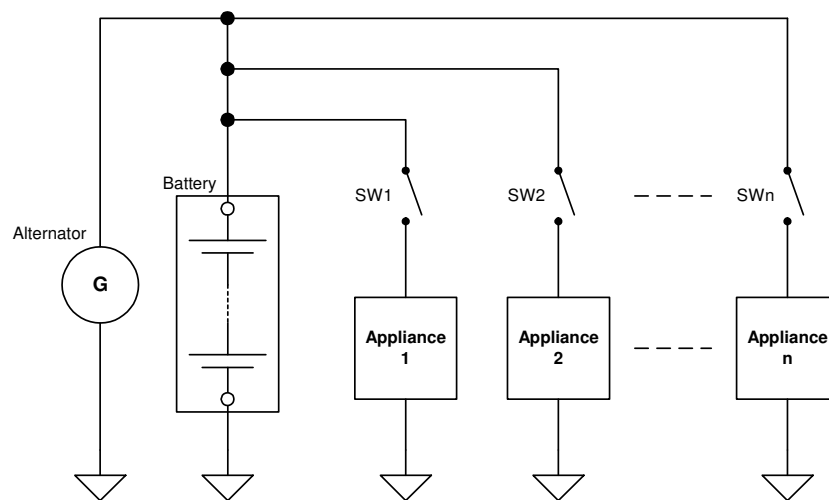


Figure 2.1 Electrical power system of conventional motor vehicle

In the conventional electrical power system design, since the battery charging current generated by the alternator could be very high and could cause high voltage drop between the alternator and battery, those consumers that are sensitive to voltage fluctuation should be connected close to the battery. However, if all the consumers are

connected close to the battery, due to the high voltage drop over the cable, the charging voltage will be lower. In order to balance the two situations, the configuration of cable connections and the use of appropriate cable thickness are decisive to the performance of the power system.

2.3 Dual battery system

In the conventional design, the battery has to be dimensioned both for engine starting and powering up the electrical system. During the engine starting sequence, the battery is subjected to high output current that the surge loading current can be as high as 500A, the associated voltage drop may affect the operation of certain consumers such as those with microcontrollers. In order to fulfill the needs of both engine starting and stable electrical power supply, an extra battery dedicated for engine starting is added, which becomes a dual battery system. The basic circuit of the dual battery system is presented in Figure 2.2.

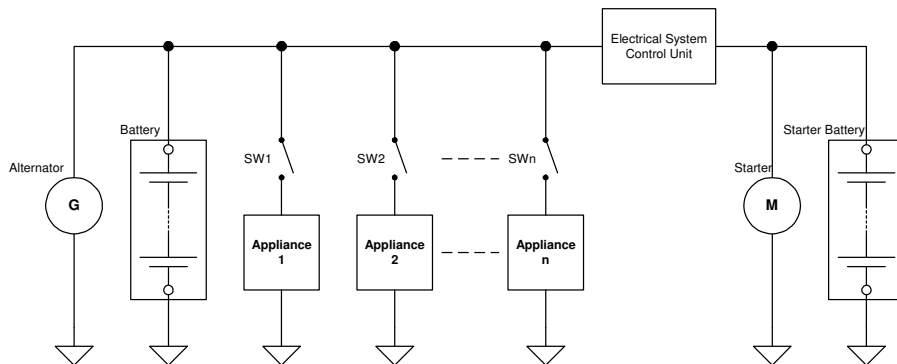


Figure 2.2 Basic circuit of a dual battery power system

The dual battery electrical system consists of two sections separated by an electrical system control unit, while one is for engine starting and the other is for general electrical supply. The purpose of using the control unit is to prevent the consumers that are sensitive to voltage changes suffer from the voltage drop generated by the starter motor having an effect on. The control unit functions like a switch which prevents the motor starting battery being discharged by consumers and connects the two sections for temporarily power backup when the general power-supply battery has run out of charge. It maintains the fully charged starter battery available to power the whole system.

2.4 42V electrical system

The employing of more electrical equipment in automobiles provides greater safety, economy and comfort, for example, a heated windshield for greater safety and an interior air warmer for greater comfort in winter. However, with those consumers installed, the peak electrical power demand would be so large that beyond the capacity of a 14V electrical system. The practical limit for common vehicle electrical systems is about 200 amperes, beyond which the wire diameter becomes too large and bulky to handle. For a 14V system, 200 amperes implies almost 3kW power consumption, it is obvious that a higher source voltage is needed to fulfill the future demand over 3kW. Without exceeding the limit of 200 amperes, 42V is used. 42V has been internationally agreed as the maximum voltage that can be safely used in a conventional vehicle system without additional protection and also a 42V system is able to deliver up to 9kW without exceeding the 200 amperes current limit of the wires. The general structure of a 42V DC power system is shown in Figure 2.3.

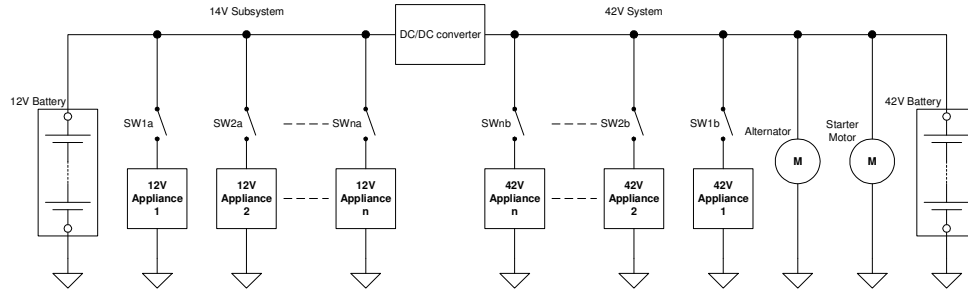


Figure 2.3 General structure of a 42V DC power system

2.5 Basics of Powerline communications

Today's vehicles are equipped with increasing number of electronic systems that are aimed at providing more safe and comfort traveling, for instance, Antilock Braking System (ABS) and Traction Control System (TCS). Along with the needs of data and information exchange among different systems, the quantities and speeds of data exchange are also continuously increasing. In order to guarantee perfect driving stability, it is vital to interconnect the core controllers of different electrical systems individually by means of networks for secure data exchanges. Conventionally, data exchanges are implemented by point-to-point connection through dedicated data lines. However, as the number of electronics increase, the point-to-point network design reaches its limit since the complexity of the wiring harness and size of the connectors become very difficult to manage. In fact the number of dedicated wires for data exchange can be greatly reduced by employing powerline communication technology to an in-vehicle power system. It helps in simplifying the structure of a power system by integrating a communication medium into the power cables. The powerline communication technology can be mainly divided into two categories: AC powerline communication

system and DC powerline communication system. The operation principle of the two systems will be introduced in the following sections.

The basic idea of powerline communication is using the powerline for transmitting both electrical energy and data, which has already been proposed over 20 years. A basic powerline communication system is typically composed of a power source, a signal transmitter and a signal receiver, as shown in Figure 2.4. In the figure, R_1 , R_2 and R_n represent the DC resistance of the powerline while L_1 , L_2 and L_n represent the parasitic inductance. u_d is the original data stream to be transmitted to the received side. Assuming R_{load} is the only resistive load connected to the powerline, to transmit u_d to the receiver, the transmitter modulates u_d by a high frequency carrier signal u_c , forming a modulated signal u_m . The modulation method can be of any type such as amplitude modulation, frequency modulation, spread spectrum modulation and the like. The function of the power amplifier A_1 is to amplify u_m to provide sufficient power for signal transmission, ensuring an acceptable signal-to-noise ratio. The structure of the receiver is very similar to the transmitter just with reversed operations. The carrier signal is decoupled from the powerline by carrier signal coupler 2, reconditioned by amplifier 2 and finally demodulated into original signal u_d by the demodulator.

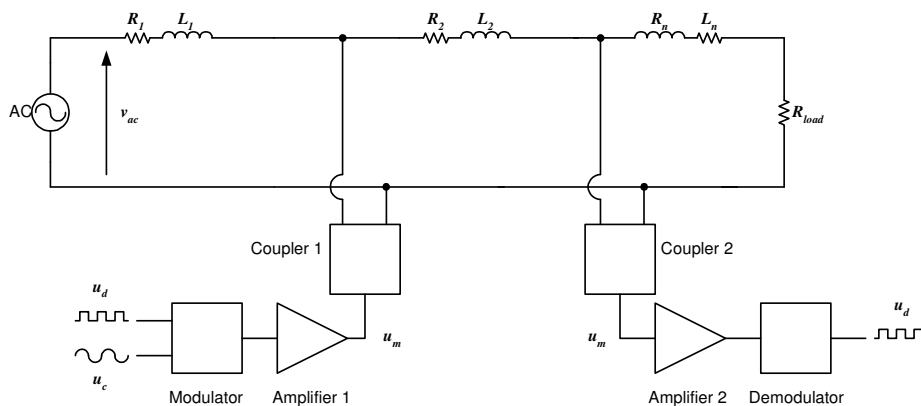


Figure 2.4 A simple powerline communication system

AC powerline line communication system

Powerline communication (PLC) is a technology that uses the pre-existing power cables for data transmission and has become a new trend for in-home intelligent control. Powerline communication technologies are widely used in applications which high speed data communication is not required and the system structure is not intended to be changed in a short time. The technologies of powerline communication can be classified into two categories; AC powerline communication and DC powerline communication. For AC power systems, the major applications recently are home automation and in-home networking over AC powerline. A number of researches about the applications of powerline communication have been done and proven that it is an effective and economical technology for home automation in recent years. Currently, AC PLC technology provides data transmission rate up to 14Mbps that is fast enough for establishing digital audio network and is expected to step forward to provide further higher data rate for audio visual applications. Due to the advantages of easy installation and low RF noise, AC powerline communication has been widely used in medium to high speed data communication applications such as local area network

connection and home automation systems.

DC powerline communication system

Generally, DC powerline communications is developed on the basis of AC powerline communication technology which has been proposed several tenth years ago. The fundamental structure of a DC powerline communication system is very similar to that of the AC system but with a DC power source instead of an AC source. For safety consideration, the peak voltage of DC power systems is usually lower than that of AC power systems. The internationally agreed maximum DC voltage that can be safely used in consumer electrical systems is 42VDC [2]; in other words, with the same power loading condition, a DC power system will have lower load impedance but higher peak current flowing through the power cables than those of an AC power system. It is not an issue for a simple electrical system that consists of power source and loads only. However, the powerline impedance is one of the critical issues that influence the performance of a PLC system especially for DC PLC systems. In order to achieve reliable data communication over the low impedance DC powerline, a high efficiency carrier transceiver for DC powerline communication has been proposed. A brief discussion about the implementation of the transceiver will be given in the later section.

Since the powerline is responsible to deliver both electrical power and signals for data communication, and the frequency characteristics of the powerline are usually unpredictable and vary according to the loading condition, impedance matching by using resistive terminator is not suitable. Hence limiting the transmission rate of the

PLC network is a useful method. In order to increase the transmission rate, numerous researches on signal modulation, data compression and security coding have been done. The communication technologies that are commonly used in PLC include spread spectrum modulation, ultra-wide-band modulation, multiple channel transmission and so on.

2.6 Summary

In this chapter, the basics of the automation systems of modern vehicles are introduced. The electrical structure of the conventional 14V power system, dual battery power system and the latest 42V DC power system are briefly introduced. A brief discuss of the operation ideas of recent in-vehicle networks are given. Moreover, a design of DC powerline communication system is proposed. The design procedure of such DC powerline communication system will be discussed in the later part of this thesis.

Chapter 3

High Efficiency Carrier transceiver for DC powerline

3.1 Introduction

Automobile manufacturers increasingly differentiate their products by providing more sophisticated and inventive features such as safety, stability, control, comfort, convenience, and entertainment. However, the employment of these applications requires high volume data exchange and a highly reliable data communication network to enable effective and efficient control over electronic devices. On the other hand, since the conventional electrical infrastructure leads to weighty and bulky cable harness that result in poor acceleration performance and limiting the top speed of a vehicle, in other words, part of the fuel is consumed inefficiently for moving the weighty cable harness. Moreover, since both the power cables and control wires are placed roundly inside the vehicle body, the vehicle has to be sizably disassembled prior to installing new devices and hence limiting the expandability of the electrical system. In order to simplify and standardize the electrical system of vehicles, a number of communication standards and protocols have been proposed. Most of the in-vehicle

communication systems are modified on the basis on the existing commercial communication technologies to meet the requirements for in-vehicle automations such as high stability and error correction capability. Generally, almost all automotive networks for automobiles are digital networks due to its high stability in terms of noise immunity and error correction capability. The design of automotive networks can be classified into to two major categories: high speed automotive network and low speed automotive network. High speed automotive networks are deigned to have wide bandwidth and specialized in multimedia applications such as digital audio visual signal transmissions. The high speed automotive networks are usually used in large scale automobiles, for instance, the interconnection between the audio/video signal source and entertainment terminals of a shuttle bus. The examples of high speed automotive systems that are commonly used on in-vehicle automations are:

- Media Oriented System Transport(MOST):
- IDB 1394:
- Universal Serial Bus (USB):

Media Oriented System Transport (MOST) is a fibre-optics point-to-point network. It can be configured in different topologies such as ring, star, bus and so on. By means of maximum data rate, MOST is a relatively low cost but high performance communication technology for high-speed communication applications such as audio, video and wide-band data transmission.

IDB1394 is a data bus system based on the IEEE1394 (Firewire) standard with considerations for automotive applications. It is a high speed communication standard that has been commonly used in high volume audio-visual signal transmission in automotive environments.

USB has been recognized as the most popular bus system that supports plug-n-play connectivity for consumer electronic. The latest version (2.0) of USB supports up to 120Mbit/Sec. Because the cost per bit of USB is relatively low and its popularity in consumer electronics and portable devices market, making car makers consider the incorporation of USB system in light vehicles.

Due to the deep penetration of electronics of modern vehicles, the weight, material cost, installation overheads and expandability of the electric power system have become the most concerned topics of automobile industries. By comparing to the multimedia system, the cable harness of an in-vehicle devices controlling/monitoring system includes much more wires and has a more complicate wiring structure. To simplify the electrical infrastructure, it is essential to reduce the number of wires of the device controlling system. Unlike multimedia applications, the data exchange rate for device controlling and monitoring purposes is low since the transmitted packets usually consist of simple address field, short length data and checksum for error handling. In order to achieve intelligent control, several low speed automation network designs have been proposed. The low speed automation networks are usually used in applications where the system cost is a concern and high speed communication is not required.

Typical examples of low speed automation network are:

- Controller Area Network (CAN):
- Local Interconnect Network (LIN):

CAN is an asynchronous multi-transmitter network specially designed for data exchange among electronic control modules in vehicles [11]. Conventionally, the maximum data rate is 1Mbit/Sec; however, some of the CAN modules are designed to have a physical layer capable to run slightly over 1Mbit/Sec for medium speed applications such as voice transmission. Being a serial communication system for networking intelligent devices as well as sensors and actuators, CAN has been recognized as the most widely used network system in light vehicles.

Like the CAN system, Local Interconnect Network (LIN) is also a serial asynchronous multi-transmitter data exchange system designed for vehicles but focused at low cost applications [11]. To reduce cost, LIN is designed to be a single wire system with data exchange speed up to 20Kbit/Sec instead of twisted pair wires operating at 1Mbit/Sec that CAN does. LIN is originated at networking sensors and actuators in short distance where the high bandwidth and versatility of CAN is not required.

An optimum in-vehicle network helps in reducing the number of wires and simplifies the assembly process with enhanced features, results in vehicles with attractive features selling at low price. It is also the major force that pushes the development, standardization and introduction of new in-vehicle networking

technologies such as the CAN (Controller Area Network) bus and LIN (Local Interconnect Network). Since the major objective of an in-vehicle network is to simplify the electrical infrastructure, most standardized in-vehicle networks are serial communication systems. Both the CAN and LIN bus are serial communication system with balanced interface running on twisted wires pair where the CAN bus has been widely used in automobile industries due to its robustness and error-correction capability. Despite there have been a number of in-vehicle communication standards available in industry and proven that they are applicable to in-vehicle intelligent control effectively, dedicated communication medium is necessary for data communication. For instance, the CAN runs on twisted pairs and the MOST runs on fibre-optics that an extra communication medium has to be installed along with power cables. However, by making use of the powerline communication technologies, a simpler in-vehicle automation system with additional intelligent features can be built. In order to achieve intelligent control over the power bus of vehicles, a design of intelligent switch system for 42V DC power net is proposed. In this chapter, a brief discussion about the design and implementation procedures of the proposed intelligent switch system is given.

3.2 Proposed DC power bus communication system

The basic idea of a DC powerline communication system is to establish data communication over DC powerline without installing additional wires. The simplified circuit of a DC powerline communication network is shown in Figure 3.1.

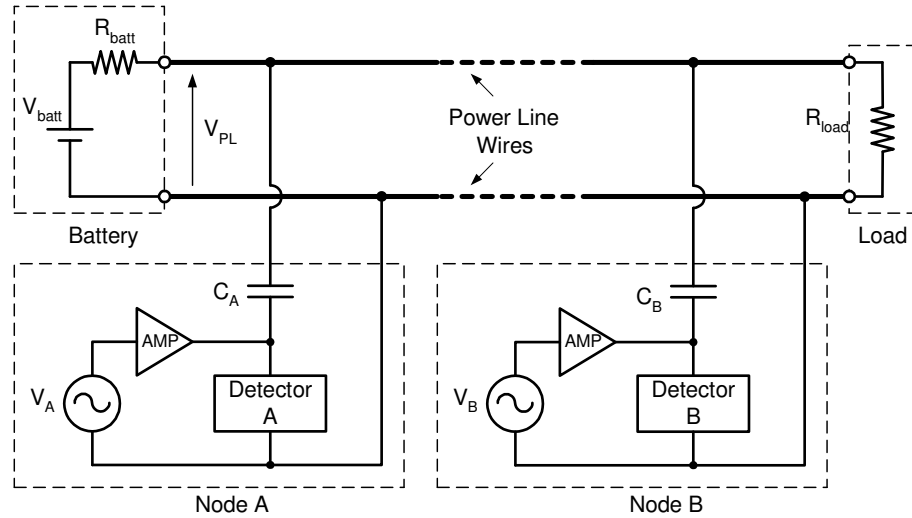


Figure 3.1 General configuration of a battery power bus communication system with two communication nodes

Figure 3.1 demonstrates a simplified conventional circuitry of injecting a sine-wave carrier signal to a DC power line with isolation. Node A and Node B are both powerline communication transceivers that consist of a power amplifier for carrier transmission and a detector for carrier detection. In the figure, v_{batt} is the battery voltage, R_{batt} is the internal resistance of the battery, v_{pl} is the power line voltage, v_{load} is the voltage of R_{load} and v_A and v_B are the sine-wave signal to be injected into the power line and is amplified by a power amplifier. The output stage of the transceivers consist of an amplifier and a signal decoupling circuit. DC powerline communication is a communication technology that makes use of the internal resistance of the power source and the parasitic components of the power cables and loads. The internal resistance of the power source is a designating factor to the communication performance since the power source is usually the component connected to the powerline with the lowest impedance, most of the transmitted signal power would be dissipated at the power source. When Node A is about to transmit a

signal to Node B through the DC powerline, the signal to be transmitted would be first amplified by the amplifier. The amplifier is usually a power amplifier to deliver adequate signal power due to the low impedance characteristic of the DC powerline. The transmitted signal travels through the cables of the DC powerline and gets attenuated along the cables, a large percentage of the signal power is dissipated at the battery and parasitic components of the powerline. Travelling through the powerline, the transmitted signal is attenuated and is sometimes distorted depending on the loading conditions of the power system. Upon reception, the detector reconstructs the distorted signal and filters out the noise. The signal transmitted by the Node A through the DC powerline is then regenerated. Figure 3.2 shows the simplified circuit of using an amplifier to transmit carrier signal to a DC power bus.

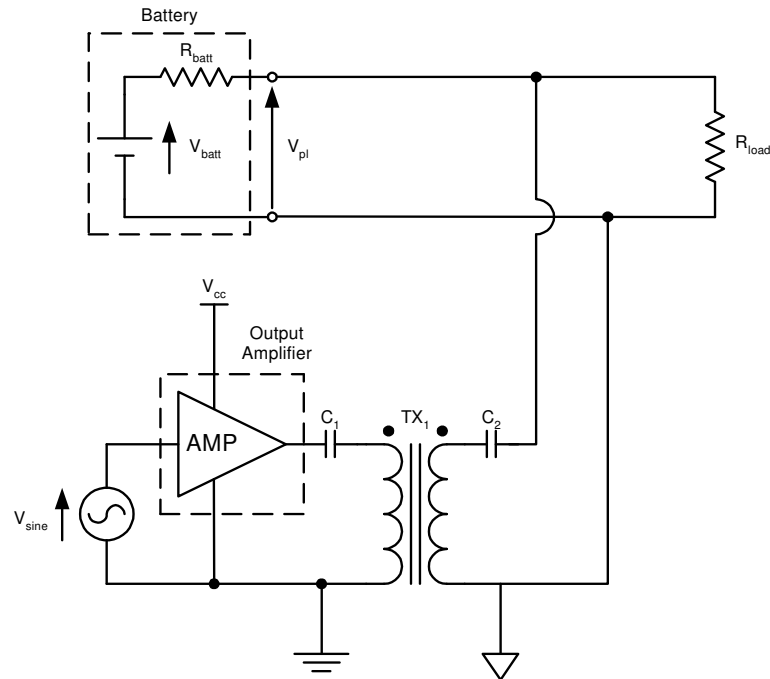


Figure 3.2 The circuitry of transmitting carrier signal to a power bus by using an amplifier

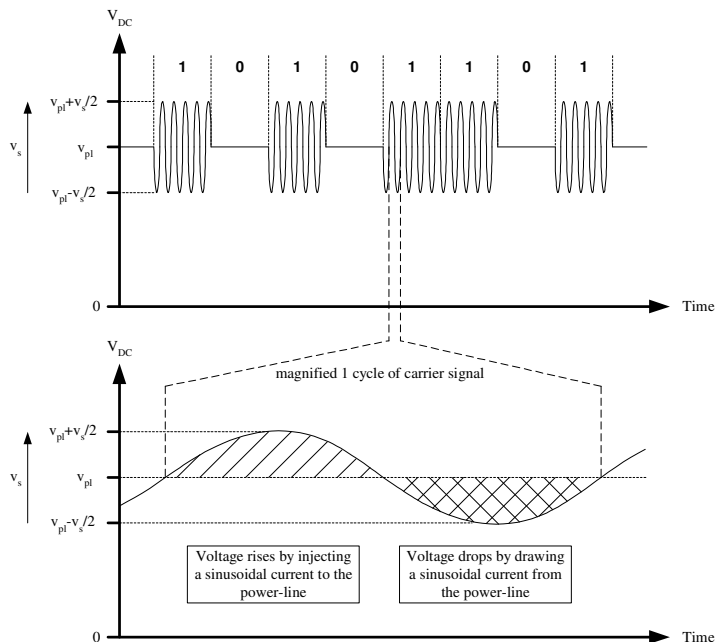


Figure 3.3 Waveforms of the DC power bus voltage with ripple carrier

In Figure 3.3, since the voltage of the power bus is clamped by the low impedance battery, in order to generate carrier signal in the form of voltage ripple, the power amplifier has to deliver high current to the powerline to drive up the line voltage and also sinks large current from the battery powerline to drive the line voltage down. It leads to high power loss and thermal stress at the power amplifier of the modulator. The power efficiency of the conventional design is always depends on the impedance of the DC powerline: the power loss at the power amplifier increases as the powerline impedance decreases. However, as mentioned in the previous chapters, the peak voltage of DC power systems is usually low for safety reasons even for high power applications, meaning that the powerline impedance is always low.

It can be seen that the major problems of the conventional design of powerline transmitter are:

- ◆ Low power efficiency
- ◆ High thermal stress at the output stage

In order to realize high efficiency signal transmission over DC powerline, a design of high efficiency carrier transmitter with a specially designed receiver is proposed. The circuits of the proposed design have been practically built and simulated by using PSpice.

3.3 Operation principles of the proposed Carrier Transmitter

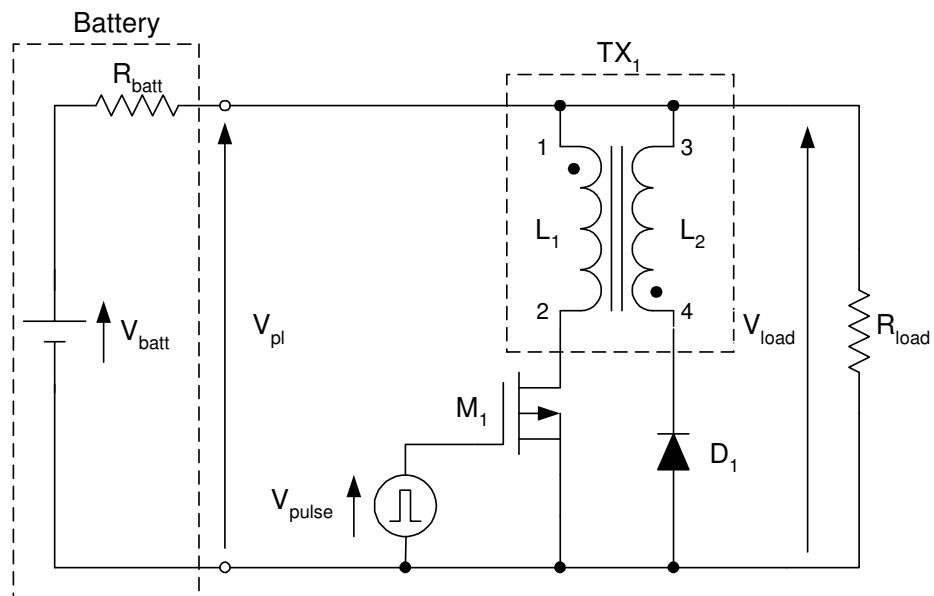


Figure 3.4 Proposed ripple carrier transmitter for battery power line communication

The basic circuit of the proposed carrier transmitter is shown in Figure 3.4. It behaves like a switching amplifier which obtains power directly from the DC powerline. The transmitter is basically a fly-back converter operating in switching mode with input and output connected together. In the figure, M_1 is a N-channel MOSFET, D1 is a Diode and R_{load} is a purely resistive and is also the only load connected to the power line. V_{batt} is the voltage of the battery to power up the whole system. To simulate a real battery, the battery has an internal resistance is denoted by R_{batt} . V_{pl} is the voltage of the powerline; V_{load} is the voltage across the load R_{load} . V_{pulse} is a pulsating voltage source that outputs a series of square pulse driving the MOSFET M_1 . L_1 and L_2 are two inter-coupled inductors having identical inductances, forming the 1:1 transformer of the fly-back circuit. The carrier frequency being transmitted to the battery power line is equal to the switching frequency of switch M_1 . In order to assure the symmetry of the carrier signal, the switching duty cycle of M_1 is fixed at 50%. Inductor L_1 and L_2 are reversely coupled on the same core and have the same inductance. They act as two current sources that L_1 draws current from the power line while M_1 is 'ON' and L_2 injects current to the power line while M_1 is 'OFF'. By making use of the internal resistance of the battery, the power line voltage can be "pulled down" by drawing a shunt current from the power line or "pushed up" by injecting a shunt current to the power line. Since L_1 and L_2 are reversely coupled on the same core, energy obtained from the power line when M_1 is turned on will be released back to the power line when M_1 is turned off; power loss at the transmitter is then minimized. Unlike the conventional design, this design has the carrier signal generated by the proposed transmitter as a series of triangular waves with sharp edges instead of sinusoidal waves, where the frequency of the carrier signal changes according to the encoded data stream. By making use of the low impedance and low

frequency cut-off characteristics of the DC powerline, the harmonic components of the triangular carrier signal will be filtered and the fundamental frequency will be detected by the receiver. It should be noted that the terminal 1 of L_1 and terminal 3 of L_2 are connected together to the battery. This arrangement can effectively clamp the voltage of L_2 to the power line voltage even when the loading resistance is large. The operation of the carrier transmitter can be simply divided into two stages:

Stage 1:

When switch M_1 is turned on, the transmitter has a simplified equivalent circuit as shown in Figure 3.5(a). L_1 draws current from the power line and pulls down the voltage of the power line to $v_{pl(ON)}$. Current flows through L_1 and stores energy in TX_1 . The voltage waveform of the power line is as shown in Figure 3.5(b).

Stage 2:

When switch M_1 is turned off, the transmitter has a simplified equivalent circuit as shown in Figure 3.5(c). The energy stored in TX_1 is released to the power line through L_2 and is used to push up the voltage of the power line to $v_{pl(OFF)}$. The voltage waveform of the power line is as shown in Figure 3.5(d). One carrier transmission cycle is completed and M_1 will turn on again to start the next switching cycle.

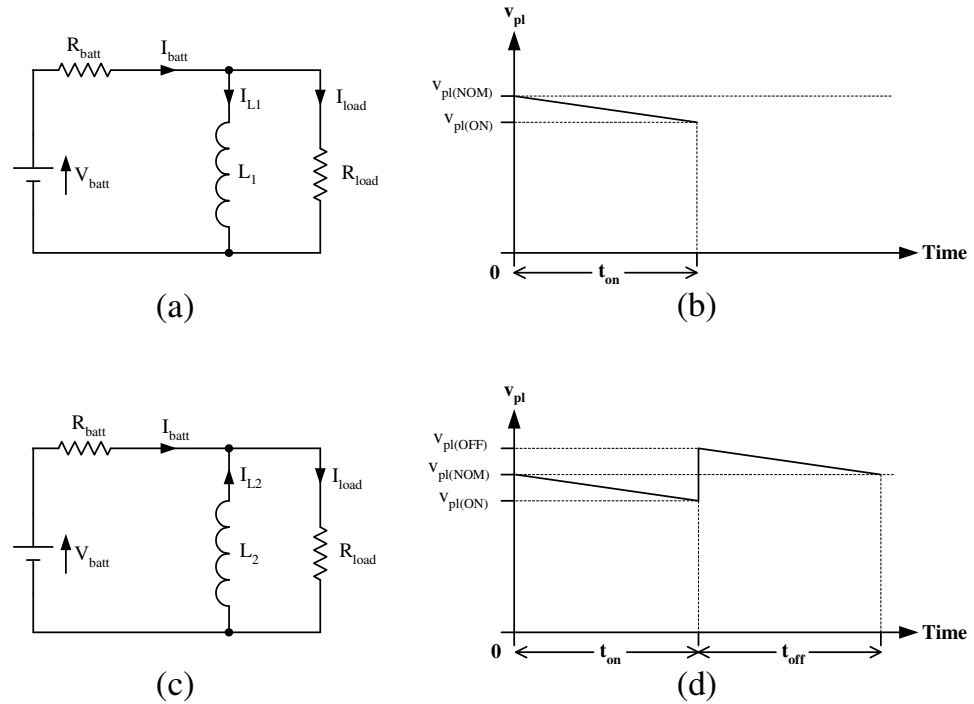


Figure 3.5 Simplified equivalent circuit of the proposed ripple-carrier transmitter and the corresponding power line voltage waveforms when the switch M1 is (a),(b) ON; (c),(d) OFF

From Figure 3.5, the carrier signal is a continuous saw-tooth wave with sharp edges at the transition that switch M1 changes from “ON” to “OFF”. The duration between two consecutive edges equals to the switching period of switch M1, in another words, that is the period of the carrier signal. The carrier signal can be demodulated by a simple diode-capacitor detector. For signal receiving, a design of signal receiver for receiving the signals generated by the proposed transmitter from DC powerline is introduced. The design and implementation procedures of the proposed receiver will be discussed in latter sections in detail.

3.4 Mathematical expressions

Let L be the inductance of L_1 and L_2 , D be the switching duty cycle and T be the switching period of switch M_1 . When M_1 is turned on, the following equations can be obtained.

The power line voltage when the switch M_1 is turned on, $v_{pl(ON)}$ is given by

$$v_{pl(ON)} = v_{L_1} \quad (1a)$$

$$i_{L_1} = \frac{v_{L_1}}{L} DT \quad (1b)$$

$$i_{batt} = i_{load} + i_{L_1} \quad (1c)$$

$$v_{pl(ON)} = v_{batt} - R_{batt} \times i_{batt} \quad (1d)$$

Substituting (1a)-(1c) into (1d), we have

$$v_{pl(ON)} = v_{batt} - v_{pl(ON)} \left(\frac{R_{batt}}{R_{load}} + \frac{R_{batt}}{L} DT \right) \quad (1e)$$

The power line voltage when the switch M_1 is turned on is given by

$$v_{pl(ON)} = \left(\frac{1}{1 + \frac{R_{batt}}{R_{load}} + \frac{R_{batt}}{L} DT} \right) v_{batt} \quad (1f)$$

When M_1 is turned off, the following equations can be obtained.

Let the power line voltage when the switch M_1 is turned on be $v_{pl(OFF)}$

$$v_{L_2} = v_{pl(OFF)} \quad (2a)$$

$$i_{L_2} = \frac{v_{L_2}}{L} (1-D)T \quad (2b)$$

$$i_{batt} = i_{load} - i_{L_1} \quad (2c)$$

$$v_{pl(OFF)} = v_{batt} - R_{batt} \times i_{batt} \quad (2d)$$

Substituting (2a)-(2c) into (2d), we have

$$v_{pl(OFF)} = v_{batt} - v_{pl(OFF)} \left[\frac{R_{batt}}{R_{load}} - \frac{R_{batt}}{L} (1-D)T \right] \quad (2e)$$

The power line voltage when the switch M_1 is turned off is given by

$$v_{pl(OFF)} = \left[\frac{1}{1 + \frac{R_{batt}}{R_{load}} - \frac{R_{batt}}{L} (1-D)T} \right] v_{batt} \quad (2f)$$

Therefore the peak-to-peak voltage of the ripple carrier signal is given by

$$v_{carrier} = v_{pl(OFF)} - v_{pl(ON)} \quad (3a)$$

Substituting (1f) and (2f) into (3a) and making $D = 0.5$,

we have

$$v_{carrier} = \left(\frac{1}{1 + \frac{R_{batt}}{R_{load}} - \frac{R_{batt}}{2L/T}} - \frac{1}{1 + \frac{R_{batt}}{R_{load}} + \frac{R_{batt}}{2L/T}} \right) v_{batt} \quad (3b)$$

According to (3a), since R_{batt} is fixed and D is equal to 0.5, the amplitude of the ripple carrier signal is then depended on the loading resistance and value of L_1 and L_2 . The amplitude of the carrier signal is proportional to the loading resistance and is inversely proportional to the inductance of L_1 and L_2 at a fixed switching frequency. To verify the design, simulation and experimental results have been obtained and will be discussed in the following sections.

3.5 Simplex DC powerline communication system

In section 3.3, the basic operation principle of the proposed carrier transmitter had been discussed. To facilitate ‘real’ data communication over DC powerline, other than the carrier signal transmitter, the system should be consists of a DC powerline, at least one signal transmitter and one signal receiver, that is a simplex communication system. The simplified system design of a simplex DC powerline communication using the proposed powerline transmitter is shown in Figure 3.6.

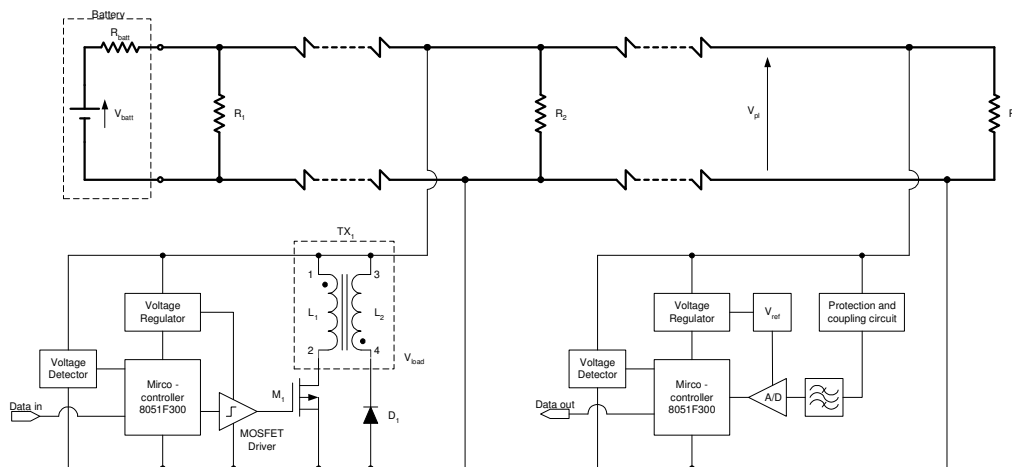


Figure 3.6 Block diagram of the proposed DC powerline communication system with simplex communication

The function of the circuit shown in Figure 3.6 is to transmit a data stream from the sender side to the receiver side, which is a very simple communication system that data only flow in one direction, from sender to receiver. Upon the data stream is input to the sender, it is coded, frequency modulated and finally transmitted to the power net by using the proposed carrier transmitter. Traveling through the power net, the carrier

signal is decoupled through a decoupling circuit at the receiver and demodulated into the original data stream. A simplex data transmission is then completed. The data rate of the system is set at 1Kbps using FSK (Frequency Shift Keying) modulation. The using of FSK in the system is due to its simple modulation and demodulation processes. Assuming the sender and receiver are very close to each other that the resistance and parasitic components of the power cables are too small that can be neglected. R1, R2 and R3 are three purely resistive loads connected to the power net.

To facilitate communication over DC powerline, internal resistance of the DC power source (in this case, the battery) must exist since the battery is normally the component that carries the lowest impedance connected to the powerline, most of the signal power delivered by the transmitter would be dissipated by the battery rather than distributed to the receivers on the powerline. This problem is significant in communications over DC system with heavy loading as the internal resistance is usually low in high capacity batteries. To solve the problem, an additional inductor may be added between the battery and the powerline to increase the impedance of the battery source; as a result, decreasing the signal power dissipates at the battery. The inductance of the additional inductor is not necessarily large, an air inductor with a few μH inductance is enough to increase the impedance of the power source.

3.6 Transmitting carrier signal to the DC power bus

The proposed carrier transmitter is used in the circuit of the sender. The operations of the circuit are control by a program stored in the flash memory of the

microcontroller (Silicon Labs 8051F300). The sender behaves like a FSK (Frequency Shift Keying) modulator that the two logic symbols ‘0’ and ‘1’ of the input signal are represented by two different frequencies; in the design, they are represented by 90KHz and 140KHz respectively. Since the system is designed for controlling and monitoring devices on the power line that is originated at low speed data exchange, the data rate was set to 1Kbit per second that a low cost medium speed microcontroller 8051F300 is capable to handle the task. The logic flow of transmitting a data stream is shown in Figure 3.7.

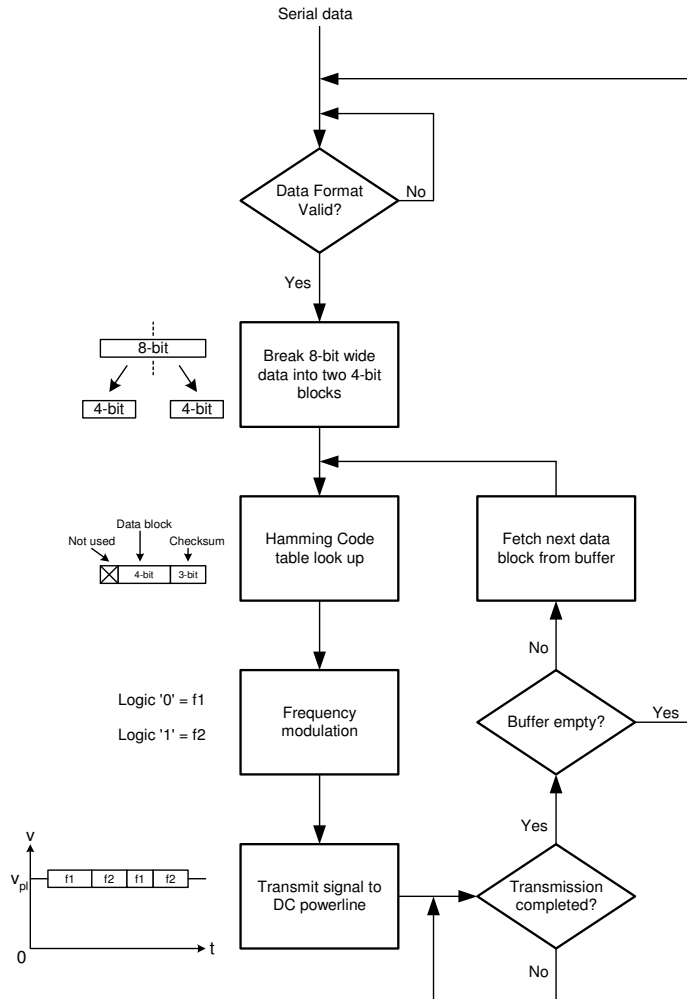


Figure 3.7 Operation flow chart of the sender

Since the characteristics of the DC power net are always unpredictable and could be harsh, in cases of signal distortion and collision happened on the power net, retransmission might not be the feasible approach for error handling. It is because the retransmission approach reduces the average data rate in noisy environments which should be avoided particularly in the low bandwidth DC power net communication system. In order to avoid the occasion of retransmission, for those minor errors such as bit loss, an error correction code is used. The advantage of incorporating error correction code into the raw data is that the error correcting process is performed at the receiver side which doesn't affect the average communication speed of the system. The microcontroller accepts external serial data through the build-in RS-232 port and encodes the data stream by error-correcting code. With the limitations of the operating speed and computing power of the microcontroller, the primitive (7,4) hamming code was chosen due to its simple coding process. It supports 1-bit error correction and 2-bit error detection that is adequate for evaluating the performance of the system. After the raw data is encoded, the microcontroller would generate a sequence of square pulse according to the encoded data stream to the transmitter introduced in the preceding sections, the raw data is then modulated and transmitted to the DC powerline.

3.7 Receiving carrier signal from the DC powerline

The design of the receiver side is very similar to the transmitter side that both of them are mainly consisted of a microcontroller, voltage regulator, voltage monitoring circuit and a signal coupling circuit. The only difference among the two circuits is that the DC powerline transmitter of the transmitter side is replaced by a high speed analog

to digital converter (ADC) circuit. The ADC of the receiver side is used to convert the AC signals that decouple through the coupling circuit into a series of digital samples for frequency detection. To reduce the number of components of the receiver circuit, most of the operations of the receiver rely on the program stored in the microcontroller that only a few external components are used. The coupling circuit is only responsible for signal coupling and primary filtering; the tasks of signal demodulation and decoding are carried out by the program stored in the microcontroller. The controller demodulates the analog signal into digital format and then performs hamming error detection, a 1-bit error will be recovered where 2-bit or more errors will be detected with an error signal raised.

As discussed in the previous sections, in a battery powered electrical system, the battery itself is always the component carrying the lowest impedance that clamps the voltage of the powerline at a very stable DC level. To facilitate data communication over powerline, the carrier signal power should be sufficiently large to maintain an acceptable signal to noise ratio. The loads (electric consumers) in DC power systems are usually paralleled with filtering capacitors. Other than the battery, these filtering capacitors also absorb the power of the carrier signal significantly. It effects in signal distortion and finally data receiving errors. To reduce the power loss of the carrier signal at the capacitors, one possible approach is to reduce the capacitance of the filtering capacitors of the loads. However, reduction of the capacitance would result in unstable operation of the electrical devices especially for those noise sensitive and with high power consumption such as the circuits with signal processors. To balance the needs of communication over powerline and stable operation of the electrical devices, a carrier signal receiver circuit making use of the signal power dissipated on the

filtering capacitors is proposed. From the point of view of power quality of a DC power system, the carrier signal is in fact some kind of noise that has to be eliminated, which is usually performed by large capacitors paralleled to the loads. As the power of the carrier signal is dissipated at the filtering capacitors while the information carried by the carrier is frequency modulated in the form of current ripples, it is possible to be picked up by coupling the AC current from the capacitors. The circuit of the signal coupling circuit is shown in Figure 3.8.

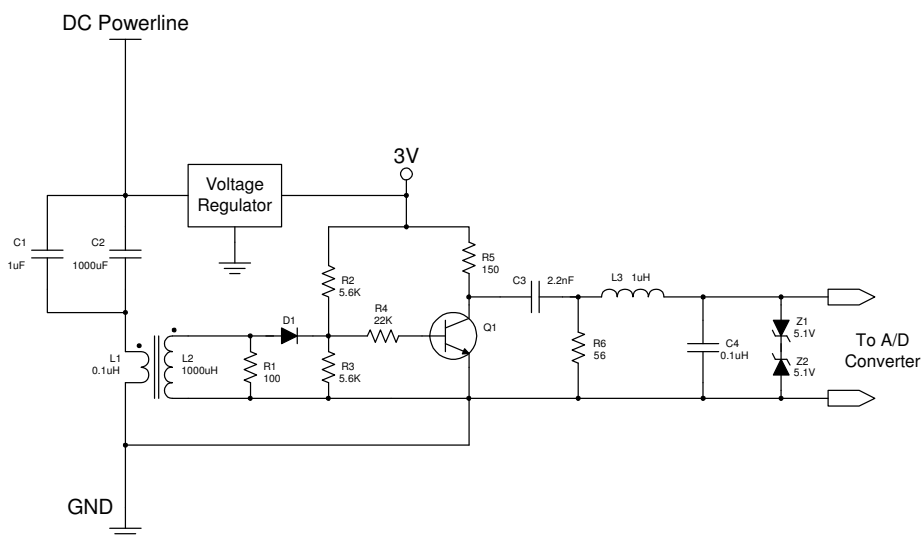


Figure 3.8 Capacitor current coupling circuit for carrier signal receiving

Figure 3.8 shows the carrier signal coupling circuit of the receiver. It is consisted of a capacitor current coupler followed by a single transistor voltage limiter. C_1 and C_2 are the filtering capacitors paralleled to the load attached to the intelligent switch that C_1 is a low ESR ceramic capacitor where C_2 is a dielectric capacitor with large capacitance; L_1 and L_2 are two inductors which are inter-coupled together to form a 1:100 current transformer. To reduce the input impedance of the coupling circuit, L_1 is designed to have one turn only. The current transformer couples the current flows

through L_1 that equals the current of the filtering capacitors to L_2 . The operation of the carrier signal coupling circuit is based on picking up the AC current of the filtering capacitors as the power of the carrier signal is dissipated on the filtering capacitors. The AC current of the filtering capacitors is coupled from the primary side (L_1) to secondary side (L_2) of the current transformer and is stepped down by a ratio of 1:100. Due to L_2 is terminated by 100 ohms resistor, the stepped down current is converted into voltage form and the negative voltage is blocked by the diode D_1 . Since the signal is usually jammed by noise and unwanted frequencies, it is amplified by a single transistor amplifier formed by R_2 , R_3 , R_4 , R_5 and Q_1 and band-filtered by a band-pass filter formed by C_3 , R_4 , L_3 and C_4 . The filter signal would then be fed into the A/D converter attached to the microcontroller for frequency detection. Other than coupling the carrier signal from the filtering capacitors, the other major functions of the circuit is to provide primitive band-limiting and power gain to the coupled signal. As parametric resistance, inductance and loading capacitance exist in the power net and are unpredictable; the transmitted carrier signal would be distorted and attenuated along the power cables in an unknown pattern. That makes the received signal always highly distorted with very small amplitude. However, since the power net has low-pass characteristics where the carrier signal is designed to be a saw-tooth waveform with sharp edges, the fundamental frequency is still able to be recognized as long as the peak voltages between two consecutive waveforms are still detectable after amplification.

The task of frequency detection is done by the microcontroller and is implemented by a stored program. The operation of frequency detection is simple. As the carrier signal is coupled into the receiver circuit, it is sampled by the A/D converter

and stored in the microcontroller one by one. Since the time between the peak voltages of two consecutive carrier waves is the fundamental period of the carrier signal, to determine symbolized frequencies, the microcontroller is programmed to continuously detect the peak voltage of the received signal and record the corresponding time between voltage peaks. The microcontroller behaves like a slope detector that it subtracts the current sample to the previous one divided by the sampling time until the calculated slope equals zero. When the subtracted result is a positive value, the voltage of the carrier is still going up and not yet reaching the peak. When the result is a negative value, meaning that the previous sample is the closest sample to the peak voltage, the value of the sample would then be stored and wait until the next peak voltage is detected, then the time (number of clock pulse) between the two detecting of peak voltages is the period of the carrier signal. The operation flow chart of the receiver is shown in Figure 3.9.

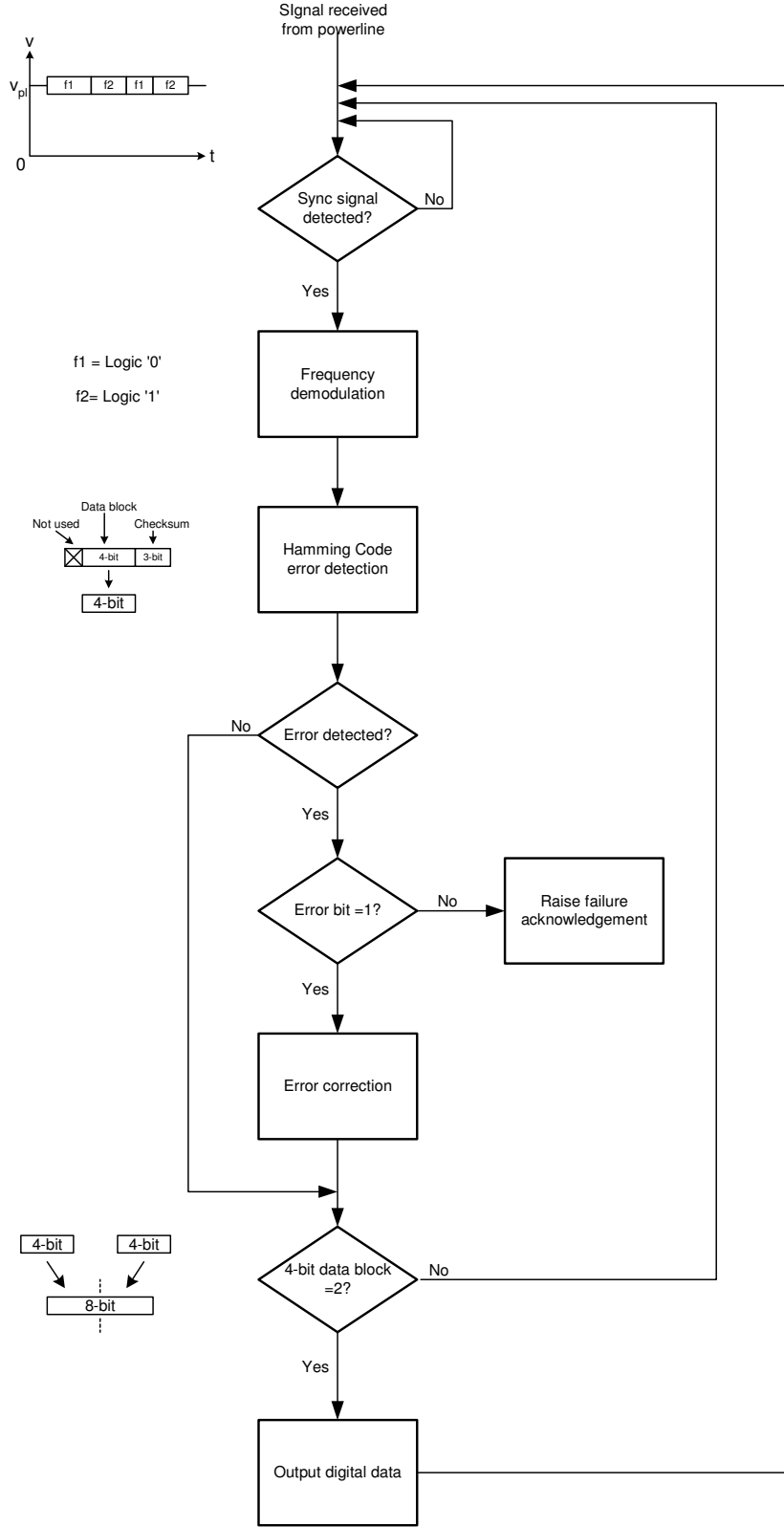


Figure 3.9 Operation flow chart of the receiver

In order to verify the ideas of the proposed signal transmitter and receivers for 42V DC power net, a simulation has been carried out by using Pspice. The corresponding parameters are listed in Table 3.1.

Parameters	Value	Units
Nominal DC power net voltage	42	VDC
Modulating frequency for Logic '0'	200	KHz
Modulating frequency for Logic '1'	270	KHz
Internal resistance of the battery	10	mohm
Loading resistance	10	ohm
Loading capacitance	1000	uF
Data length	5	bits
Data pattern	10010 _b	/

Table 3.1 Major parameters of the simulation

The simulation circuit is shown in Figure 3.10 (Appendix Figure A.1). It is a simplex DC powerline communication system with one signal transmitter and one receiver only. The system is powered by a 42V battery which is consisted of a 42V voltage source V_3 with 10mohms internal resistance denoted by R_1 . Since parasitic resistance and inductance exist in cables practically and the signal transmitter and receiver are always placed apart along the power cable, L_3 , L_4 , R_2 and R_6 are added to simulate the basic characteristic components of the power cables. Since in practical power systems, the loading condition could be very complicate and unpredictable, to make the simulation simpler, it is assumed that resistor R_1 is the only load connected to the power net with the filtering capacitor C_1 connected in parallel. The operation

principles and design considerations of a 42V DC power net communication system with multiple loads would be discussed in the latter chapters.

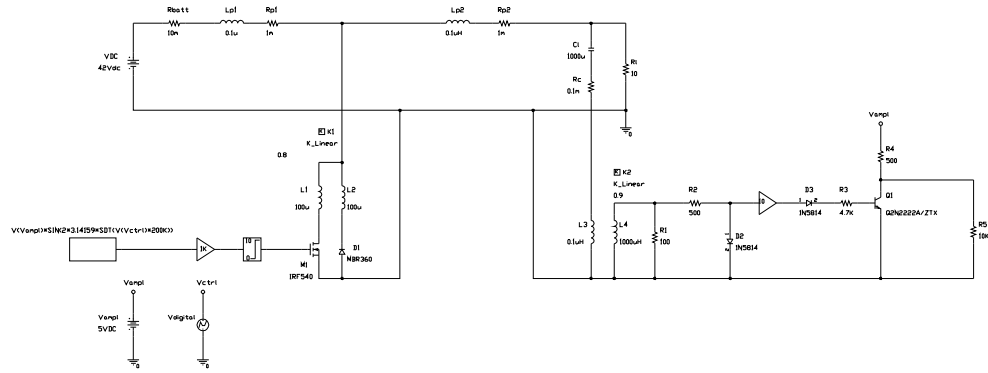


Figure 3.10 Simulation circuit of a simplex 42V DC power net communication system

3.8 Simulation Results

The simulation results are obtained by using Pspice, which has accurate models of both passive and active components such as diodes and MOSFETs. The simulation describes how a digital signal stream is frequency modulated and transmitted over the DC power net by using the proposed carrier transmitter and receiver under steady state. The operations of carrier signal detecting, demodulating and error handling are not included in the simulation as these operations are performed by the program stored in the microcontroller. Figure 3.11 shows the waveform of the original data stream which is 10010_b and the corresponding waveform of the frequency modulated signal on the power net. In the simulation, the original data stream is implemented by using a programmable pulse source that logic '0' and logic '1' are represented by 1V and 1.35V

respectively. Since the transmitter circuit activates only when data transmission is needed, in the simulation, the transmitter is shut down when the input signal is at zero volt. Figure 3.12 shows the ripple voltage of the power net at the transition of changing modulation frequency. The transition time of changing from logic '1' to logic '0' is 10ns. Figure 3.13 shows the current waveform of the filtering capacitor of the load comparing to the original modulating digital signal. Figure 3.14 shows the capacitor current at the transition of the modulation frequency changes. The voltage regenerated by the current sensor circuit according to the current of the filtering capacitor is shown in Figure 3.15. Figure 3.16 depicts the final output voltage of the whole receiver circuit. The output of the receiver circuit is a series of square pulse where the time interval equals the modulating frequency of the carrier signal; it is not yet demodulated since the tasks of signal demodulating and decoding are carried out by the microcontroller. From Figure 3.11 to Figure 3.16, the driving signal of the MOSFET M_1 is compared to the output signal of the receiver circuit. It is observed that the original data stream is successfully modulated, transmitted through the 42V DC power net by using the proposed transmitter and recovered by using the proposed receiver.

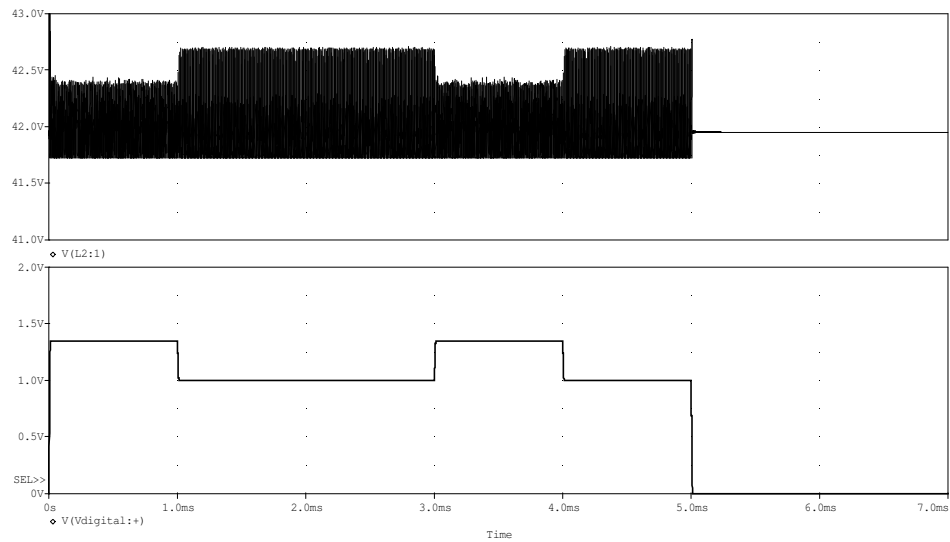


Figure 3.11 Simulation result of the proposed carrier transmitter and receiver design. Upper trace: voltage of the DC power net; lower trace: modulating digital signal (10010b)

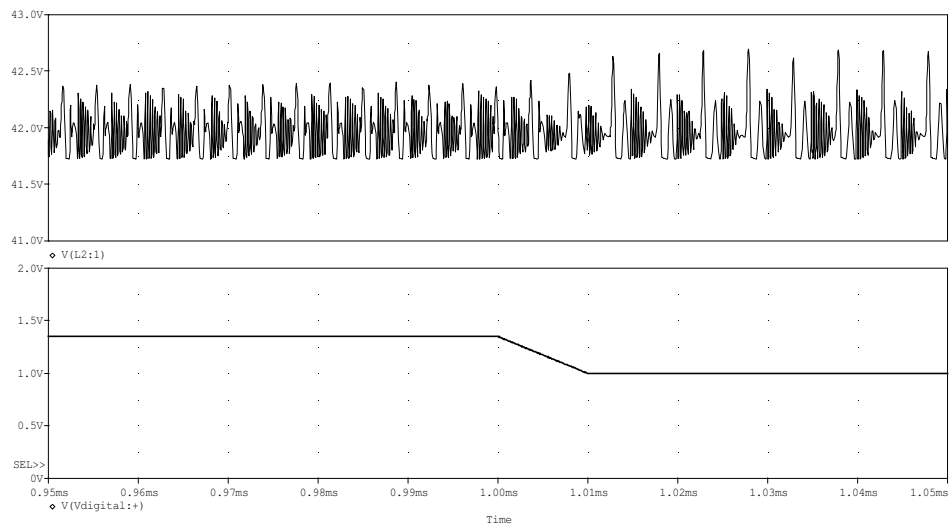


Figure 3.12 Simulation result of the proposed carrier transmitter and receiver design at the transition of changing modulation frequency. Upper trace: voltage of the DC power net; lower trace: modulating digital signal (logic '1' to logic '0')

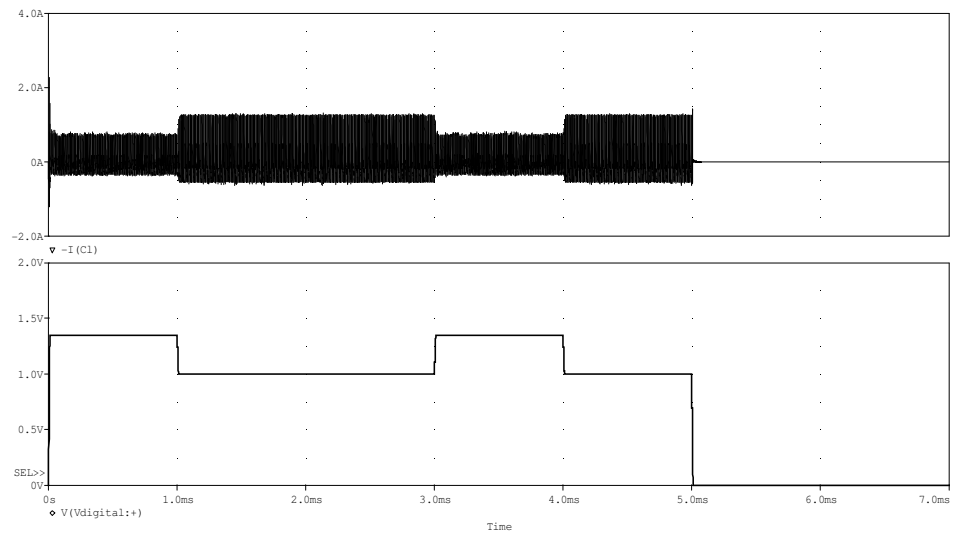


Figure 3.13 Current waveform of the filtering capacitor of the load. Upper trace: current of the filtering capacitor; lower trace: modulating digital signal (10010b)

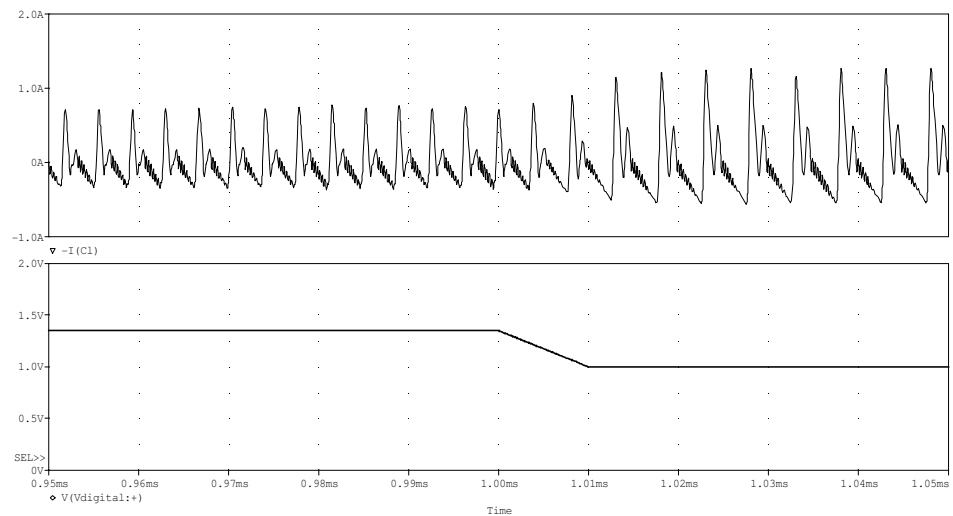


Figure 3.14 Current waveform of the filtering capacitor of the load at the moment of changing modulation frequency. Upper trace: current of the filtering capacitor; lower trace: modulating digital signal (10010b)

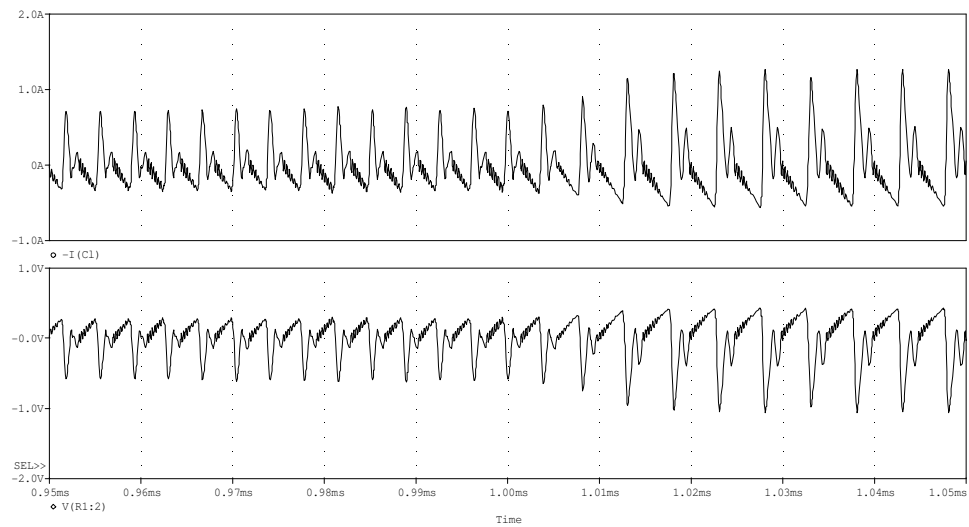


Figure 3.15 Waveforms of the current of the filtering capacitor and the output voltage of the current sensor. Upper trace: current of the filtering capacitor; lower trace: Output voltage of the current sensor

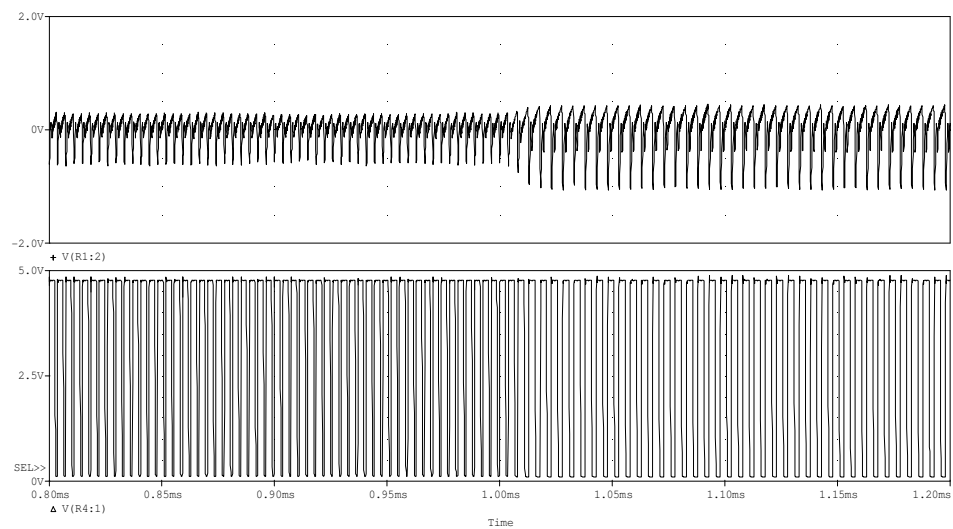


Figure 3.16 Waveforms of the current of the filtering capacitor and the output voltage of the receiver circuit. Upper trace: current of the filtering capacitor; lower trace: Output voltage of the receiver circuit

In the simulation, the signal modulator is consisted of analog behavior model, the gain stages and limiters are implemented by ideal components. Since these components do not exist practically, to further verify the performance of the proposed DC power net communication system, an experimental setup has been built with the parameters listed in Table 3.1. The configuration of the experimental setup is similar to the circuit shown in Figure 3.10 while the transmitter is driven by a microcontroller and the output of the receiver circuit is connected to another microcontroller for signal detection. In order to have a simple operation environment, a 42V DC power net communication system with only one 10ohms resistive load is developed. The Experimental results are shown in Figure 3.17 and Figure 3.18. In Figure 3.17, the signal transmitted to the 42V DC power net is generated by a microcontroller with the proposed signal transmitter. The original data is modulated by the transmitter and transmitted to the power net in the form of voltage ripple, it can be seen that the original data (10010110b) is successfully regenerated by the receiver. The receiver output the demodulated signal after the whole packet is received with some delay. Figure 3.18 shows the ripple current of the power net when a logic 0 is transmitting (200KHz), the current ripple is a series of saw tooth wave where the fundamental frequency equals the frequency of the pulse signal generated by the microcontroller. In the Figures, we find that the experimental results show good agreement to the initial prediction.

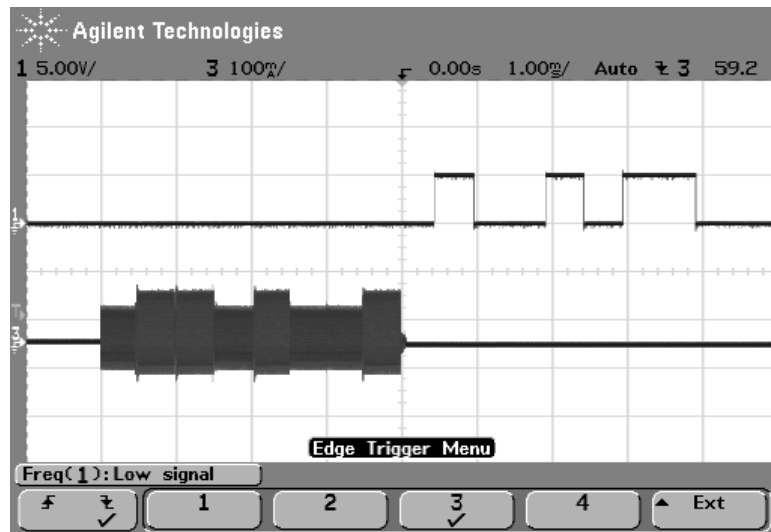


Figure 3.17 Practical waveforms of the 42V power net communication system. Upper trace: digital output of the receiver; lower trace: ripple voltage on the DC power net which is the original digital data (10010110b)

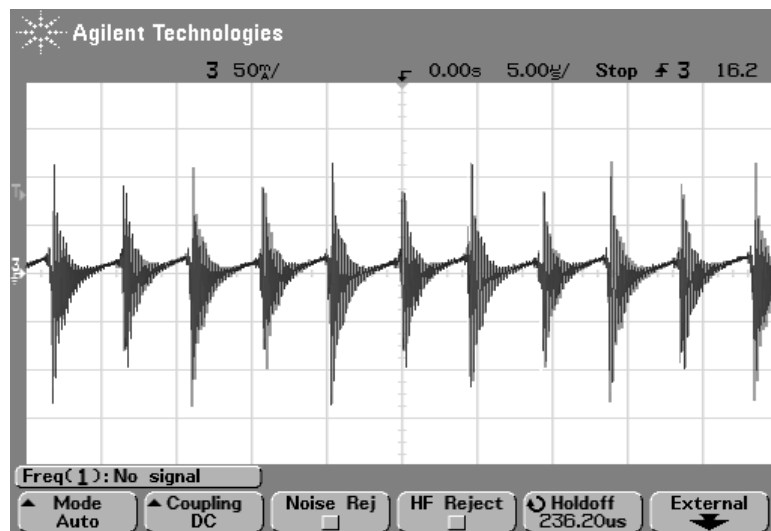


Figure 3.18 Ripple current of the 42V DC power net at the carrier frequency equals 200KHz

3.9 Conclusion

A design of power line communication system for 42V DC power net is presented in this chapter. The system is basically a combination of communication system and power delivery system where the communication media is integrated into the power cables. In order to simplify the cabling structure and to minimize the amount of cables of the system, the structure of the system is designed to be a bus network that the main power cable is pre-installed around the vehicle. The simulation results show that data communication over low impedance DC power net is achievable with the proposed carrier signal transmitter and receiver. The main circuit of the transmitter is basically a fly-back converter with the input and output terminal connected together and operates in switching mode to achieve high efficiency signal transmission. Being controlled by a microcontroller, the carrier transmitter is able to frequency modulates and transmits a 1Kbps data stream to the power net. Because the carrier signal travels through the power net in the form of ripple current that is filtered by the filtering capacitors of the loads, to facilitate signal receiving, the receiver is designed to be a current coupler that obtains the carrier signal from the current of the filtering capacitors. The receiver behaves like a simple current to voltage converter which converts the coupled current signal into square pulses, where the period of the pulse sequence carries the fundamental frequencies of the modulation frequencies. Signal demodulating and decoding processes are carried out by the microcontroller with hard-coded program. Practical implementation of the proposed DC power net communication is discussed. The simplicity of the proposed DC power net communication system makes it not only suitable for vehicles, but also any DC power system that wiring complexity is a concern.

Chapter 4

Electrical characteristics of the proposed intelligent system

4.1 Introduction

Electronics is playing an important role in modern vehicles. The number of electronic devices in a vehicle is expected to increase rapidly in the future. The conventional method of controlling electronic devices in a vehicle is to install wires between the control panel and every single node along with wires delivering power. However, it implies high wiring complexity and high production cost. In order to simplify the wiring system in a vehicle, several in-vehicle networking standards had been proposed, such as “CAN BUS” and “LIN BUS”. Both “CAN BUS” and “LIN BUS” require a dedicated line for communication. However, the network can be further simplified by combining the communication bus and the battery powerline. In this chapter, we proposed a design of intelligent switch system for in-vehicle control application that based on battery powerline communication. A prototype of the proposed intelligent switch system has been developed to verify the design.

The proposed intelligent switch system is designed for in-vehicle applications and consists of a host controller and a number of intelligent switches. All the nodes (including the host controller and all the intelligent switches) are able to transmit signal to and receive data signal from the 42V power net. The reason of choosing 42VDC as the bus voltage is higher bus voltage helps in reducing the diameter of the power cables while 42VDC is the internationally agreed maximum DC voltage that can be used safely in an enclosed area [11]. The 42V power net design has been recognized as the standard electrical infrastructure for the next generation vehicles. Adapted to the 42V system, the proposed intelligent switch system is able to control and monitor any device connected to the power net with an intelligent switch attached. The major features of the intelligent switch system are:

1. Integrate all components necessary for powerline communication, power switching and monitoring.
2. DC Powerline communication
3. Automatic over-current cut off
4. Automatic failure reporting
5. Replace mechanical switches and relays directly
6. Small package size
7. Easy installation

4.2 Operation principles of the proposed intelligent switch system

The simplified circuit of the intelligent switch system is shown in Figure 4.1. The proposed intelligent switch system reduces the use of copper wires by replacing the mechanical switches in a vehicle with electronic switching circuits that communicate with a unique host controller through the battery powerline. The basic idea of the intelligent switch system is to transmit high frequency carrier signal over the power cables to facilitate remote power management [5]. In Figure 4.1, it can be seen that the system is a bus network that consisting of a single intelligent host controller, a number of intelligent switches, loads (appliances), power source (battery) and cables that delivers both signal and power. The reason of using bus configuration is the intelligent switch is designed to be accessible wherever electrical power is reachable, where bus configuration is the simplest way that allows the power cable to go around the vehicle body with minimum amount of cable. When a new device with an intelligent switch (intelligent device) is about to be added to the system, There is no more to do except connecting the intelligent device to the power bus since the power cable is pre-installed surrounding the vehicle. The host controller is the centre of the whole intelligent switch system, it is attached to a user interface which interacts with the users that delivers information about the system to users and receives command from users. Upon receiving a command from the user through the user interface, the host controller transmits a signal to the corresponding intelligent device through the power net with an unique address tag attached. The transmitted signal is broadcasted and distributed to the whole power bus that received by all the intelligent devices. The intelligent devices identify the address tag enclosed in the signal, only the one matched to the address

would respond to the command. On the other hand, when a device is detected to be failed, the corresponding intelligent switch would send a ‘device failure’ acknowledge signal to the host controller and inform the user that there is a failed device. The host controller and intelligent switches communicate with each other over the power bus to facilitate power controlling and monitoring among appliances.

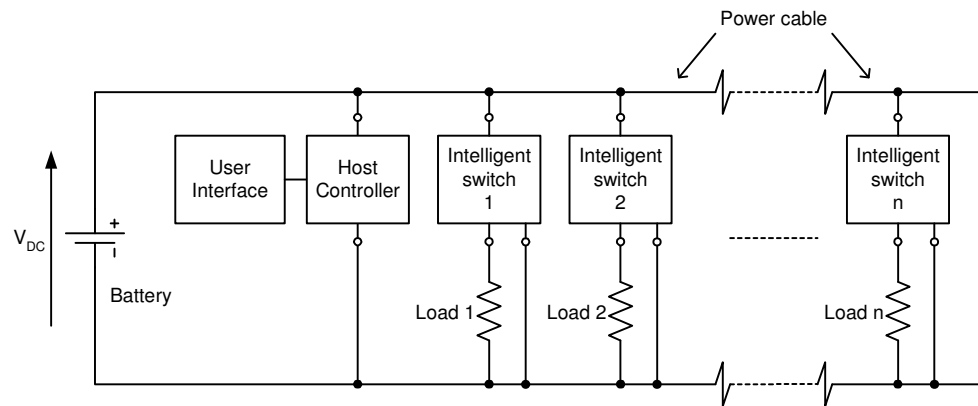


Figure 4.1 Simplified circuit of the intelligent switch system

Other than simply controlling the ON/OFF and monitoring the status of electronic devices, advanced device management can also be achieved with the proposed intelligent switch system. A typical example of the intelligent features is the intelligent switches are able to monitor the operation conditions such as average operation current and store in the internal memories. In case the attached load draws large current from the power bus abnormally (say several time of the previous average current), the corresponding intelligent switch will first disconnect the load from the power bus and report to the user about the failure. All the intelligent switches are designed to have three terminals only; namely, they are ‘Power’, ‘Ground’ and ‘Switch’ as shown in Figure 4.1. Since the communication media is integrated into the power bus, the wiring

complexity and the amount of cable used in a vehicle is reduced [9]. The using of bus topology minimizes multi-path echo and ensures predictable propagation delay for communication [4], it results in low signal collision probability and also helps in reducing the amount of cable used.

4.3 Modeling and analysis of a 42V DC power net

In practice, since parasitic resistance and inductance do exist in the power cables while the appliances on the power bus are usually paralleled with capacitors, making the power bus behaves like a multi pole low-pass filter [1] with very low cut-off frequency and introducing attenuation to the carrier signal. The filter characteristic of the power net varies according to the number of loads connected and the distance between them, are not alterable. This makes the distortion and attenuation of the carrier signal uncontrollable. Before the intelligent switch system is implemented, it is necessary to study the structure and characteristics of the battery driven DC power net. Figure 4.2 shows the circuit of a practical power net with a number of intelligent switches connected. In the figure, V_{DC} is the battery voltage; R_{batt} is the internal resistance of the battery; R_{P1} , R_{P2} , R_{P3} and R_{Pn} are the segment resistance of the power cables; L_{P1} , L_{P2} , L_{P3} and L_{Pn} are the parasitic inductance of the power cable; R_{L1} , R_{L2} and R_{L3} are the loads that connected to the intelligent switch units; C_1 , C_2 and C_3 are the filter capacitors paralleled to the loads; R_{C1} , R_{C2} and R_{Cn} are the equivalent series resistance (ESR) of the filter capacitors.

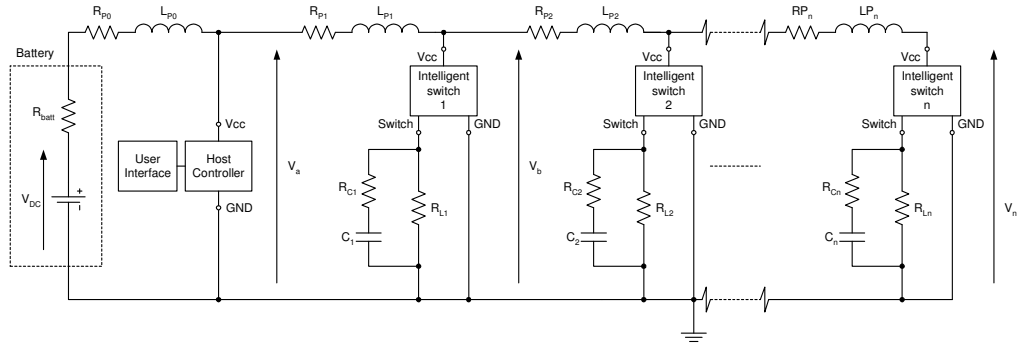


Figure 4.2 Simplified circuit of the proposed intelligent switch system with parasitic components of the power bus

Looking at the circuit of the intelligent switch system shown in Figure 4.2, assuming a command is input through the user interface to the host controller to control the intelligent switch 2. To complete the job, the host controller will simply transmit a series of signal to intelligent switch 2 over power net with the corresponding address enclosed, then the intelligent switch 2 response to the command received. However, when there is more than one intelligent switches connected to the power net and are turned on, the situation is no longer simple. For example, again the host controller is transmitting signal to intelligent switch 2 but the intelligent switch 1 has already been turned on, the carrier signal that transmits from the host controller has to pass through a low-pass T-filter to the intelligent switch 2. Such filter is composed of the resistance and inductance of the power cable, loading resistor and filter capacitor. In this example, they are R_{P1} , R_{P2} , L_{P1} , L_{P2} , R_{C1} , R_{L1} and C_1 . The filter introduces attenuation and distortion to the transmitted signal that are depend on the length of the power cables and the characteristics of the filtering capacitor, such as the ESR (equivalent series resistant). R_{P1} and R_{P2} are the DC resistance of the power cables that are linearly related to the length of power cables, the longer the cable, the higher the resistance. It can be seen that the resistance and inductance of the cables are the

dominating factors that affect the filter characteristic of the power net. Since the current flows through the power net could be very large and is limited by the resistance of the cables, to minimize the power dissipated on the cables, thick wires are used. RayChem CMC-055-1 is the cable that commonly used as main power cable in modern vehicles. It is one kind of multi-core nickel plated copper wire sized at AWG1 (0.38 inch dia.) with double layers insulation. Take the CMC-055-1 as an example, the maximum resistance under normal temperature (20 degree) is 149mohm/km, then the straight line inductance L_{p1} and R_{p1} in terms of length can be found:

$$L_{p1} = 0.0002 \times \text{length}(mm) \left[\ln \left(\frac{2 \times \text{length}(mm)}{\text{radius}(mm)} \right) - 0.75 \right] \mu H$$

$$R_{p1} = \text{length}(mm) \times 1000 \times 5m\Omega$$

For easier understanding, let the battery contributes no loading effect to the system, the transfer function of the segment between the host controller and intelligent switch 1 can be easily defined:

$$V_b = \left[\frac{R_{L1} \times \left(R_{C1} + \frac{1}{2\pi f C_1} \right)}{R_{L1} \times \left(R_{C1} + \frac{1}{2\pi f C_1} \right) + (R_{p1} + 2\pi f L_{p1}) \times \left(R_{L1} + R_{C1} + \frac{1}{2\pi f C_1} \right)} \right] \times V_a \quad (1a)$$

Therefore:

$$V_n = \left[\frac{R_{L1} \times \left(R_{C1} + \frac{1}{2\pi f C_1} \right)}{R_{L1} \times \left(R_{C1} + \frac{1}{2\pi f C_1} \right) + (R_{p1} + 2\pi f L_{p1}) \times \left(R_{L1} + R_{C1} + \frac{1}{2\pi f C_1} \right)} \right] \times \left[\frac{R_{L2} \times \left(R_{C2} + \frac{1}{2\pi f C_2} \right)}{R_{L2} \times \left(R_{C2} + \frac{1}{2\pi f C_2} \right) + (R_{p2} + 2\pi f L_{p2}) \times \left(R_{L2} + R_{C2} + \frac{1}{2\pi f C_2} \right)} \right] \times \dots$$

$$\times \left[\frac{R_{Ln} \times \left(R_{Cn} + \frac{1}{2\pi f C_n} \right)}{R_{Ln} \times \left(R_{Cn} + \frac{1}{2\pi f C_n} \right) + (R_{pn} + 2\pi f L_{pn}) \times \left(R_{Ln} + R_{Cn} + \frac{1}{2\pi f C_n} \right)} \right] \times V_a \quad (1b)$$

i.e. the signal attenuation between the host controller and the last intelligent switch is:

$$\begin{aligned}
 \text{Attenuation}(dB) = 20 \log_{10} & \left[\frac{R_{L1} \times \left(R_{C1} + \frac{1}{2\pi f C_1} \right)}{R_{L1} \times \left(R_{C1} + \frac{1}{2\pi f C_1} \right) + (R_{P1} + 2\pi f L_{P1}) \times \left(R_{L1} + R_{C1} + \frac{1}{2\pi f C_1} \right)} \times \frac{R_{L2} \times \left(R_{C2} + \frac{1}{2\pi f C_2} \right)}{R_{L2} \times \left(R_{C2} + \frac{1}{2\pi f C_2} \right) + (R_{P2} + 2\pi f L_{P2}) \times \left(R_{L2} + R_{C2} + \frac{1}{2\pi f C_2} \right)} \times \dots \right. \\
 & \left. \times \frac{R_{Ln} \times \left(R_{Cn} + \frac{1}{2\pi f C_n} \right)}{R_{Ln} \times \left(R_{Cn} + \frac{1}{2\pi f C_n} \right) + (R_{Pn} + 2\pi f L_{Pn}) \times \left(R_{Ln} + R_{Cn} + \frac{1}{2\pi f C_n} \right)} \right] \quad (1c)
 \end{aligned}$$

In equation 1a to 1c, it can be seen that the attenuation of the carrier signal over the power bus is determined by several factors, which includes the parasitic inductance and resistance of the power cable, loading capacitance and the corresponding ESR, loading resistance and finally the number of loads. Since these factors contribute different level of attenuation to the carrier signal, to facilitate signal transmission over the power bus, it is necessary to identify the factor which causes signal attenuation the most. Assuming the loading resistance is 100ohm and the carrier frequency is 100KHz, the relationship among the carrier signal attenuation, cable length (in other words, parasitic inductance and resistance of the power cable.) and the loading capacitance of one segment of the power bus is as shown in Figure 4.3.

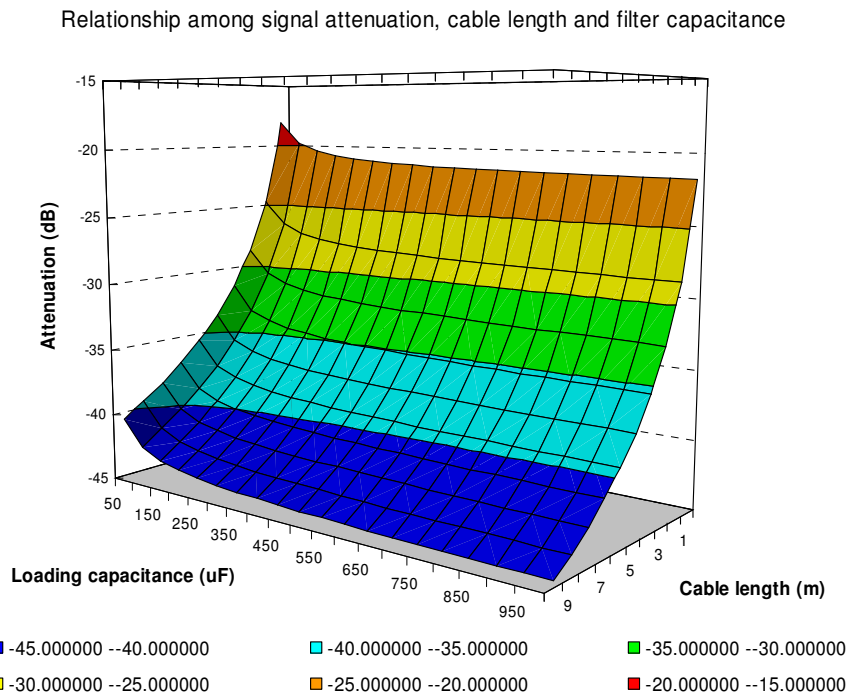


Figure 4.3 Relationship among the signal attenuation, cable length and loading capacitance of the 42V DC power net. X axis: Loading capacitance (uF); Y axis: Length of the cable (meter); Z axis: Attenuation (dB)

In Figure 4.3, it can be seen that the signal attenuation causes by the increasing of the cable length is far more serious than that causes by the increasing of loading capacitance. The signal attenuates more than 2 dB as the cable length increases by 1 meter. Figure 4.4 shows the relationship among the signal attenuation, loading resistance and capacitance. It is obvious that the loading resistance is nearly irrelevant to the attenuation of the 100KHz carrier signal.

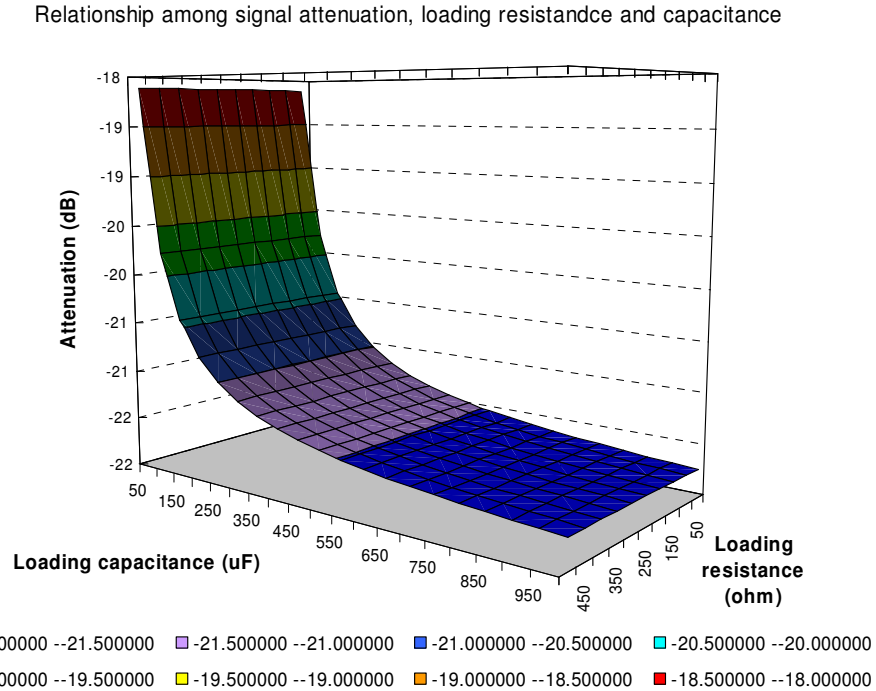


Figure 4.4 Relationship among the signal attenuation, loading resistance and loading capacitance of the 42V DC power net. X axis: Loading capacitance (uF); Y axis: Loading resistance (ohm); Z axis: Attenuation (dB)

Assuming the cable length of each segment is 1m while the loading capacitance equal to 1000uF with 10mohm ESR and 100ohm loading resistance, the relationship between the carrier signal attenuation and the number of cable segment (number of loads) is as shown in Figure 4.5. It can be seen that the carrier signal attenuates rapidly as the number of cable segment increases. When the number of cable segment equals 7, the signal attenuation is 100dB, that means when the signal source and the receiving end is 7meters apart with a 100uF capacitor connected to the power bus every meter, the received signal will be 1/100000 of the transmitted signal.

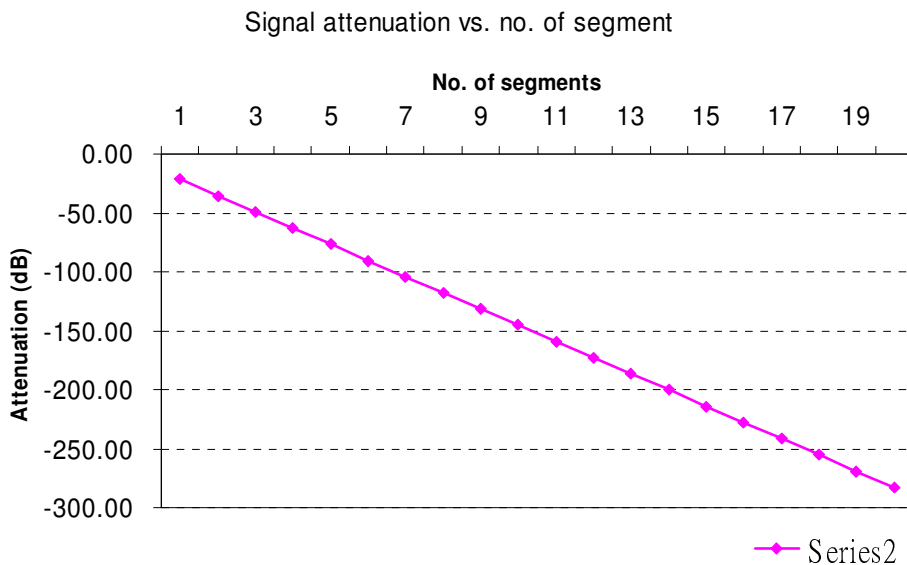


Figure 4.5 Relationship between the signal attenuation and the number of distanced load. (Condition: $R_{P1}=R_{P2}=\dots R_{Pn}=5\text{mohm}$; $L_{P1}=L_{P2}=\dots L_{Pn}=0.9\mu\text{H}$; $R_{C1}=R_{C2}=\dots R_{Cn}=5\text{mohm}$; $C_1=C_2=\dots C_n=1000\mu\text{F}$; $R_{L1}=R_{L2}=\dots R_{Ln}=100\text{ohm}$; segmented cable length = 1m)

4.4 Conclusion

In this chapter, the electrical characteristics of a 42V DC power net are discussed. Pspice simulation has been carried out to investigate the electrical characteristics of the power net. An electrical model of the power net is built to study the relationship between the loading condition of the power net and the performance of the proposed DC power net communication system. The simulation results show that the DC power net behaves like a low-pass filter that introduces attenuation and distortion to the high frequency carrier signal. Since the power net is designed for in-vehicle applications, the noise on the DC bus is sweeping according to the speed of a vehicle; to facilitate data communication over the power net, special error coding and modulation schemes are required.

Chapter 5

A design of carrier transmitter for 42V

DC power net

5.1 Introduction

In modern vehicles, most of the equipments are driven by electrical power and controlled electrically. As the number of electronics increases, the material cost, installation cost and weight of the cable harness increase. All these overheads would reflect on the selling price of automobiles and finally reduce the competitive power in the market. Since most of the cables and wire are made of copper which is some kind of expensive metal, reduction of copper wires has become a popular topic of automobile industries. Reducing the amount of copper wires benefits in many aspects, for instant, reducing the weight of vehicles that helps in fuel saving. In automobile industry, car manufacturers define the electrical infrastructure for their own vehicles and do not act in accord with each other due to the difference in technology level and corporation preference. Despite different manufacturers have their own design preference for the electrical system, the electrical infrastructures of modern vehicles are generally either in star or tree topology. In such designs, all the devices are

connected directly to the battery and alternator with dedicated wires, thus a star or tree type electrical system is formed. The major advantages of using the star/tree type structure are simple installation, easy maintenance and high reliability. Currently, the star or tree electrical infrastructures are still popular designs in modern vehicles. The inherence of the star/tree electrical system in modern vehicles is in fact a historical factor that is not adaptable to the rapidly growing demand of in-vehicle services. As the total power consumption increases as the number of electronic device and provided services increases, thick power cables have to be used to handle the high current flow. In order to deliver sufficient power to the devices while keeping the weight of the cable harness light, several designs of in-vehicle electrical infrastructure have been proposed, where the 42VDC bus is one of the most popular designs in the industry [2]. It is introduced with the concept of bus network into the power system where all the devices are connected to the unique 'power bus' that installed around the vehicle instead of directly connected to the battery by dedicated cables. The reason of using 42VDC as the bus voltage is 42VDC has been globally agreed as the highest DC voltage that can be used safely in a closed area [11]. Also since the source voltage is raised from conventional 14V to 42V, the maximum deliverable power is increased with no thicker cables, this enables the system to feature new functions that require high power consumption, such as wind shield heating.

The major purposes of incorporating electronics into vehicles are to control and monitor the mechanical components. Other than the power cables, the wires for controlling and monitoring purposes are the major components of the cable harness. As the demand of in-vehicle services increases, the number of wires and the wiring complexity also increases. In most cases, the control signal is very simple, low speed

and represented by means of analog voltage changes, to reduce the number of wires of the cable harness, several dedicated low speed communication system for automobiles have been proposed, such as CAN and LIN bus. However, these communication systems can be further simplified by integrating the communication media into the power cables. Due to the power cables are used only for DC power transporting, it is possible to perform signal transmission by making use of the available bandwidth of the power cables, which is known as DC powerline communication technology. The DC powerline communication technology is developed on the basis of the AC powerline communication technology which has been proposed several tenths of years. At the moment, the maximum speed of an AC communication system has reached 14Mbps which is capable to handle digital video transmission. On the other side, though the technology of AC powerline communication is claimed to be mature, the technology of DC powerline communication is still staying at the stage of lower than 1Mbps data rate due to the natural characteristics of DC systems.

Structurally, the AC communication system and DC powerline communication are very similar. However, due to the very different electrical characteristics among the two systems, the design considerations are greatly deviated from each other. In AC power system, most of the power consumers are inductive while in DC power systems, most of the consumers are capacitive. In addition, the peak voltages in AC power systems are usually much higher than that of a DC power system. These factors indicate that the powerline impedance of DC power systems is usually far lower than AC power systems. Since the line impedance is determined by the type and loading conditions of the loads, it is not possible to perform impedance matching by resistor termination. Due to the low impedance of the DC powerline, data exchange over DC

powerline requires high signal power and cooled transmitter stages that is not easy to achieve in limited small space. It is the major reason of the slow evolution of DC powerline communication technologies. If we look into an in-vehicle control system, there may be a number of consumers in different types connected to the DC powerline that results in the line impedance as low as several milliohms, the attempt of data communication over powerline is even more difficult. As the powerline impedance and signal transmission power are the obstacles of performing data communication over DC powerline, to tackle the problem, a design of intelligent switch system for 42VDC power net is proposed. The operation principles, design procedures and implementation processes will be discussed in this chapter briefly.

5.2 Basics of DC powerline communication technology

The basic requirement of a battery powerline communication system is the use of conductors which deliver power as a communication medium. In order to facilitate signal transmission over a battery powerline, the transmitting signal is modulated with a high frequency carrier and amplified by an amplifier to provide adequate signal power, is then coupled to the powerline through a coupling capacitor. The transmitted signal superimposes with the powerline voltage and travels through the powerline in the form of voltage ripple. Similar to the common communications systems, a DC powerline communication system is consisted of at least one sender and one receiver that are connected by a communication medium. The major characteristic that DC powerline communication system differ from the generic system is that the communication medium is not only used to transport signal but also electric power that

powers up the entire system including both the sender and receiver circuits. Since this project is focused on in-vehicle power management while the electrical system of modern vehicles are powered by lead acid batteries, a DC powerline communication system can be simply regarded as a battery connected in parallel to a common communication system as shown in Figure 5.1.

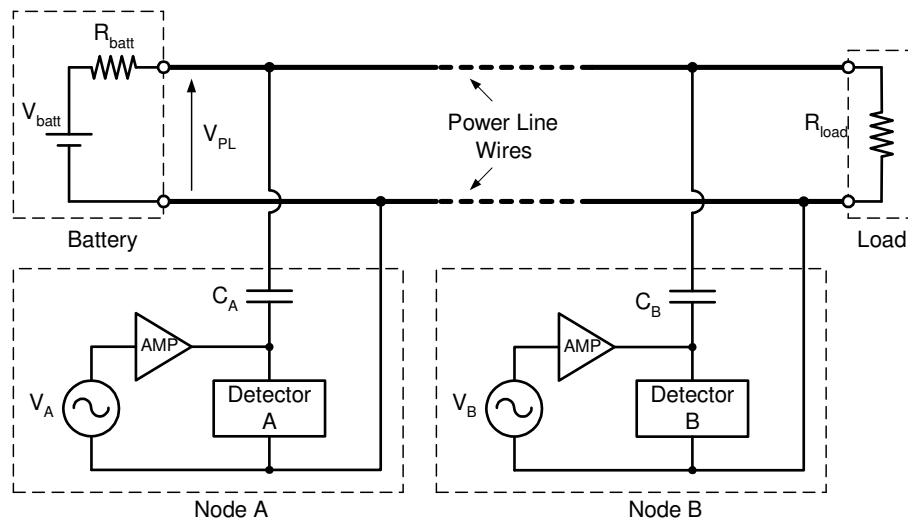


Figure 5.1 General configuration of a battery powerline communication system with two communication nodes

The circuit shown in Figure 5.1 is a simple battery driven DC powerline communication with two nodes. In the Figure, V_{pl} is the voltage of the powerline while V_{batt} and R_{batt} are the voltage and internal resistance of the battery respectively. The value of the internal resistance is important as it is a major factor that determines the signal amplitude. Node A and node B are two communication nodes having identical structures where both of them are able to transmit signal to and receive signal from the powerline. Due to the low pass characteristics of the DC powerline, Node A and node B are required to use the same frequency band for communication. In other words, the

two nodes are not intended to transmit signal at the same time, otherwise, collision occurs. The signals to be transmitted to the powerline are generated by the AC signal sources V_A and V_B , they are amplified by amplifiers which provide current gain and coupled to the powerline through C_A and C_B . To facilitate data communication over power lines, there have been a number of modulation methods available, some of them are being used popularly in commercial products for AC power systems, for instant, multicarrier transmission, dual channel transmission, spread spectrum carrier transmission (SSC transmission), ultra wideband transmission (UWB transmission) and so on. Multi-carrier transmission is a technique developed on the basis of frequency division multiplexing that transmits data by dividing the data stream into several interleaved bit stream and using these to modulate several carriers. By using multiple carriers, the available bandwidth of the powerline can have better utilization and higher data rate. The idea of dual carrier transmission is very similar to that of multi-carrier transmission which uses only two individual carriers for signal modulation and transmission. This approach achieves high noise immunity by modulating the original data by two carriers in different frequencies, in case one of the carriers is lost or destructed, it is still possible to regenerate the original data by using the other carrier. Comparing to multi-carrier transmission, as the number of carrier is reduced to two, the hardware design is simpler and the required bandwidth is much narrower. Spread spectrum transmission has been commonly used in powerline communication systems due to its high resistance to interference. It is a communication scheme which is proposed on 1940 and originally designed for military purposes. It generally makes use of a sequential noise-like signal structure to spread the normally narrowband information signal over a relatively wideband of frequencies. The receiver retrieves the original signal by correlating the received noise-like

frequencies. The basic idea of Ultra wideband transmission is very similar to which of spread spectrum, but modulating the original signal into even wider frequency band. The advantages of using wide transmission bandwidth are high data rate and high communication security, enabling the powerline communication system to handle bandwidth demanded applications such as audio-visual signal transmission.

However, in modern vehicles, the quantity of wires used in audio-visual and entertainment applications are far less than those used in control and monitoring purposes while most of them do not require high speed communication or high volume data exchange. This indicates that a low speed and cost effective in-vehicle control network is more necessary than a high speed one. Although a high-speed in-vehicle network is capable to handle both control and multimedia applications, it may be too expensive to install communication nodes to every single device in a vehicle even for those very simple devices such as the head lamps. In order to achieve low cost and simple in-vehicle controlling and monitoring, a design of intelligent switch system using DC powerline communication technology and simple frequency modulation with a special encoding scheme is proposed.

5.3 System Configuration of the intelligent switch system

The proposed intelligent switch system is designed for controlling the ON/OFF of the devices in a vehicle with advanced monitory and supervisory functions such as failure detection. The configuration of the intelligent switch system is generally a bus network which data are modulated by high frequency carrier and being transmitted to

the receiver(s) through the main trunk. The main trunk of the network is in fact a piece of power cable that delivers power from the battery to the load while the chassis of the vehicle is used as the electrical return path. As all the devices including the host controller are able to transmit signal to and receive signal from the power bus, the intelligent switch system can be treated as a battery driven power system with a number of signal source connected. As the communication medium is integrated into the power cable and is terminated by a battery, most of the power of the transmitted signal is dissipated at the battery. On the other hand, since resistance exists in the battery, by making use of the internal resistance together with a power efficient signal transmitter and special modulation scheme, data communication over DC power bus is achieved.

To minimize the number of wires used in the electrical power system, the structure of the proposed intelligent switch system is basically a bus network (DC power bus) that the main trunk is installed around the body of a vehicle. The main trunk is the medium that transports both electrical power and data. All the devices in the network are attached to an intelligent switch. The intelligent switches are used to manage the ON/OFF and monitor the operation of the attaching device. The intelligent switches are supervised by a unique host controller over the DC power bus by means of powerline communication. The host controller supervises the activities of all the intelligent switches according to the command applied by the user. It is also the only unit equipped with a user interface that enables the user to interactive with. In order the facilitate communications over DC power net, both the circuits of the host controller and intelligent switch are designed to have a signal transmitter for transmitting signal to the power net and a signal receiver for receiving the signals transmitted by the

senders from the power net. In this chapter, a design of intelligent switch system for 42V DC power net with novel designs of signal transmitter and receiver is proposed. To verify the ideas, computer aided simulations by using PSpice have been carried out. A prototype of the proposed system is built to verify the theoretical predictions.

5.4 Signal transmitter for 42V DC power bus

The basic principle of performing communication over power cables is to transmit AC signal to the powerline in the form of voltage ripples. However, due to the low impedance characteristic of battery driven DC power systems, transmitting voltage ripple requires high instantaneous power and high power output stages. The conventional linear amplifier circuits are not suitable in this application since they subjected to high thermal stress and heat dissipation. Also since the amplitude of the carrier signal arrived at the receiver circuits varies corresponding to several factors such as the number of activated loads on the power bus, type of the loads, length of the power cable between the sender and receiver and so on, the modulation method used in the proposed communication system is based on conventional frequency due to its insensitivity to the fluctuations of carrier amplitude. In order to generate carrier signal over the low impedance power bus, a special circuit of carrier signal transmitter is proposed, the analog part of the transmitter is shown in Figure 5.2. In the figure, it can be seen that the transmitter circuit is driven by a pulse source where the frequency of the pulse series is identical to the carrier frequency to be transmitted to the power net. The pulse series is generated by a microcontroller with pre-installed program. The design procedure and the flow of the program will be discussed in the later part of this chapter.

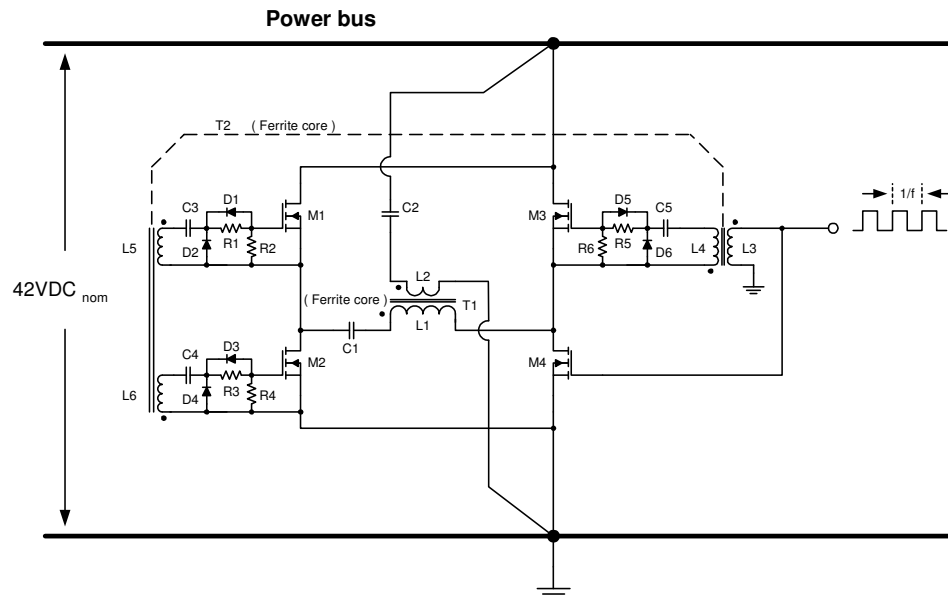


Figure 5.2 Practical transmitter circuit of the proposed intelligent switch system

5.5 Circuit description

The objective of designing the transmitter circuit shown in Figure 5.2 is to transmit approximated sine-wave carrier signal to the DC power net effectively. Since the circuit is operated in switching mode, the approximated sine-wave is generated by making use of the resonant characteristic of the circuit. The circuit is very similar to the generic full-bridge converter with the voltage input and output connected together. In Figure 5.2, M_1 , M_2 , M_3 and M_4 are four N-channel MOSFETs operating in switching mode where M_1 , M_4 and M_2 , M_3 are complimentary pairs. They are driven by the same pulse source signal where the period equals the fundamental frequency of the carrier signal to be transmitted through the gate driving transformer T_2 , in other words, the gate driving signal of the MOSFETs is in fact the input modulating signal to

the transmitter. T_2 is consists of four inter-coupled windings L_3 , L_4 , L_5 and L_6 having identical inductance. L_1 and L_2 are inter-coupled together at a large turn ratio to step up the output current and reduce the output impedance of the transmitter. The resonance frequency of L_1 and C_1 are designed to be slightly higher than the fundamental frequency of the driving pulses of the MOSFETs, so that the output frequency of the transmitter can be varied linearly according to the period of the input pulse and coupled to the power bus through L_2 in the form of current ripple. Figure 5.3 shows the frequency response of the LC resonance circuit formed by L_1 and C_1 . In the figure, f_c is the centre frequency of the resonance circuit, f_1 is the minimum frequency that would be used in the MOSFET driving signal and Δf is the range of the deviation of the input frequency, so $f_1 + \Delta f$ is the maximum input frequency. The centre frequency of the LC circuit is set higher than the maximum input frequency and only the frequency range with linear gain would be used.

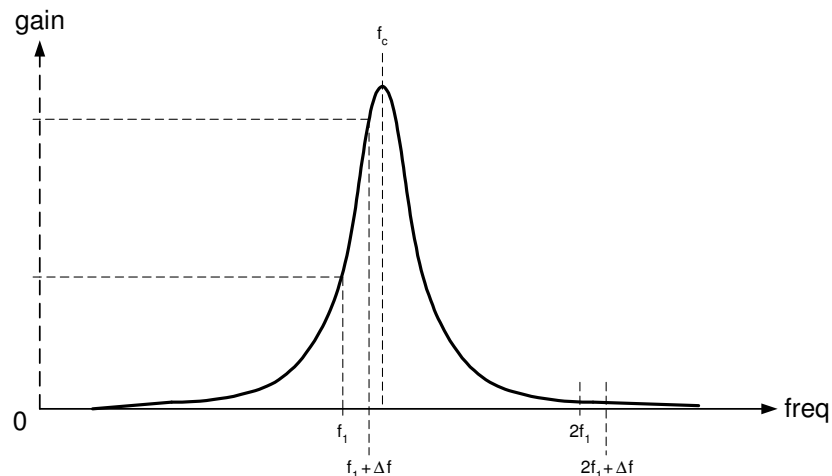
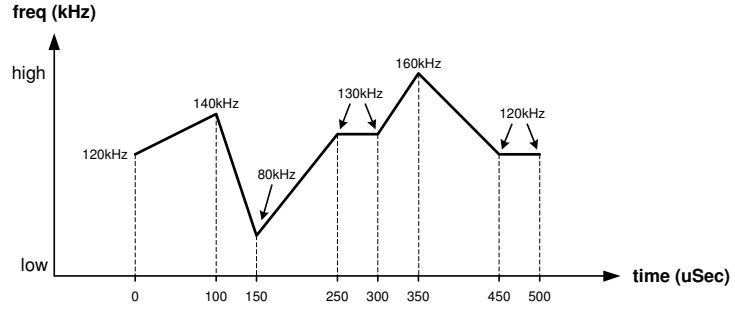


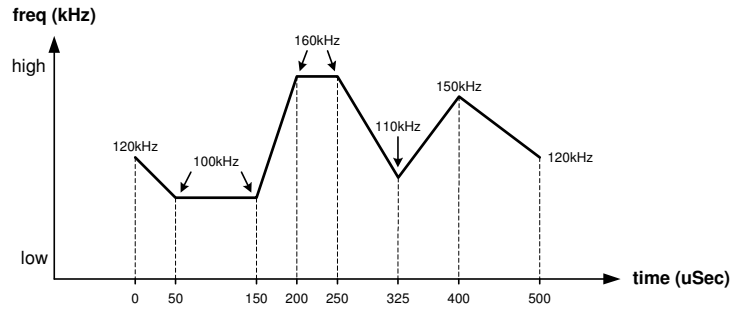
Figure 5.3 Frequency response of the transmitter circuit

In this transmitter design, frequency modulation is use due to the advantages of simple implementation and low response on changes of carrier amplitude. However,

since the frequency of the noise generated by the alternator sweeps across a wide frequency band which changes according to the running speed of the engine, simple frequency modulation might suffer from serious signal distortion and high error rate which is not suitable for in-vehicle power net communication. To decrease the transmission error rate, one simple approach is increase the ‘uniqueness’ of the modulated signal pattern. Unlike the generic data communication using frequency modulation that the logic states are represented by two different frequencies, in this design, the input data is ‘encoded’ into special pattern of frequency changes rather than fixed frequencies. Since the raw data are modulated into frequency changes in special patterns, the probably of noise jamming is reduced. With this special modulation scheme, in case the modulated signal is destructed by noise at a particular frequency, error correction is still performable. The frequency patterns representing logic ‘0’ and logic ‘1’ are presented in Figure 5.4. In the figure, it can be seen that the frequency patterns of the two logic states are very different to each other. The start and stop frequency of both the frequency patterns are set at 120KHz to avoid sudden frequency change. The length of them is defined to be 1ms, so excluding the time taken for hand shaking and processing, the maximum data rate could be 1Kbit per second. Figure 5.5 shows how a 8bit data stream is represented by the frequency patterns.



Frequency pattern of logic '0'



Frequency pattern of logic '1'

Figure 5.4 Frequency patterns of logic 0 and 1; upper: logic 0; lower: logic 1

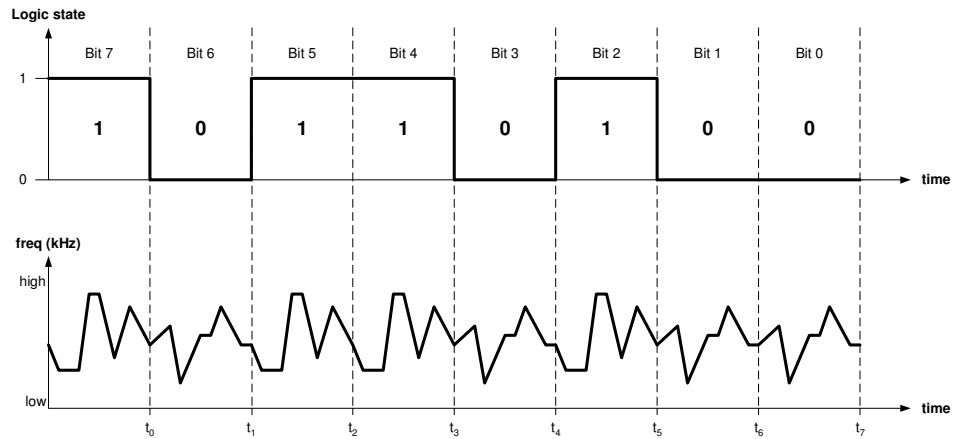


Figure 5.5 Waveforms of the input data stream and the corresponding frequency patterns

Converting logic signal into the frequency patterns shown in Figure 5.4 is a direct mapping process that a microcontroller would do the job well. The conversion process is implemented by the program stored in the integrated memory of a microcontroller (8051F300). Figure 5.6 illustrates the program flow of the frequency mapping process. Since the conversion process is performed by means of software, the number of external components and size of the circuit are minimized. The microcontroller monitors the input port continuously until the first valid data bit is detected. In order to make the program runs fluently, the size of the input frame is defined at 1 byte which equals the data bus width of the microcontroller. The content stored in the memory rotates once upon a new data bit is received until the entire memory cell is filled full. Since all the intelligent devices are designed to share the same frequency band for signal transmission, signal retransmission due to receiving error may occupy the transmission medium in noise environments and results in a drop of average data rate. In order to reduce the number of retransmission over the power bus, error correction code is employed in the design. When one raw data byte is received, it would be broken into two 4-bits data block for hamming code encoding, generating two 8-bits hamming coded data blocks with one dummy bit in each block. The coded data block would then be represented by two different patterns of frequency changes bit by bit. As shown in Figure 5.6, the logic '0' and logic '1' are represented by two different patterns of continuous frequency change. The patterns are preset in the program stored in the microcontroller. The frequency patterns of logic '0' and '1' are presented in Figure 5.4. In order to avoid sudden changes of carrier frequencies, the start and stop frequency of both logic '0' and logic '1' are set at the same frequency, 120kHz. The patterns are designed to be very different to each other to distinguish logic '0' and '1'. Since the frequency patterns are very special that the chance of having unrecoverable

receiving errors due to noise jamming is greatly reduced. Figure 5.5 describes how a data stream is represented by a series of frequency changes. Since the logic states are frequency modulated and represented in a special manner, in order to receive the modulated signals from the power bus and regenerate the original data according to the received signals, a design of receiver circuit is introduced in the latter section.

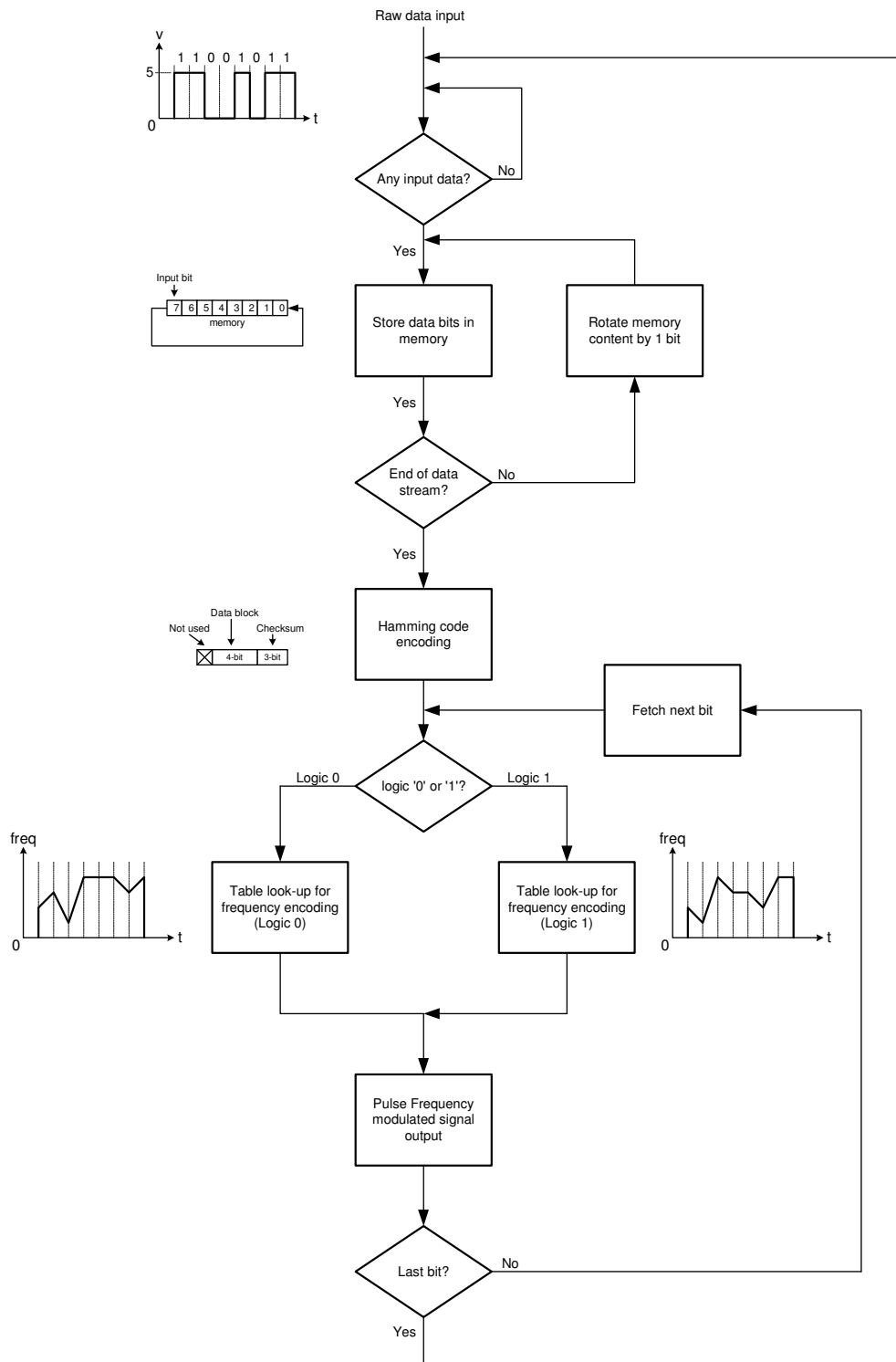


Figure 5.6 Flow chart of the frequency pattern conversion process

5.6 Signal receiver for 42V DC power bus

In this section, a design of signal receiver for receiving the signal generated by the transmitter circuit discussed in the previous section is introduced. Since the DC power bus behaves like an attenuator with uncertain noise, the signal receiver should be able to recognize the weakened and distorted carrier signal from the power bus. The proposed receiver circuit is basically a frequency to voltage converter followed by a microcontroller with several external auxiliary components such as low noise amplifiers. The frequency to voltage converter is used to convert the frequency patterns in the carrier signal into voltage variations for the convenience of signal detection by the microcontroller. The task of frequency to voltage conversion is accomplished by a balance demodulator, in this design, a Foster-Seely discriminator is adopted. The Foster-Seely discriminator is a widely used FM detector in commercial FM radio circuits which converts a range of input frequency into voltage linearly. The Foster-Seely discriminator uses a double tuned transformer to convert the frequency variations of the input signal into amplitude variations. The amplitude varying signal is then rectified and filtered to provide a DC output voltage. Such voltage varies in both frequency and amplitude as the input frequency changes. The typical circuit of a Foster-Seely discriminator is presented in Figure 5.7.

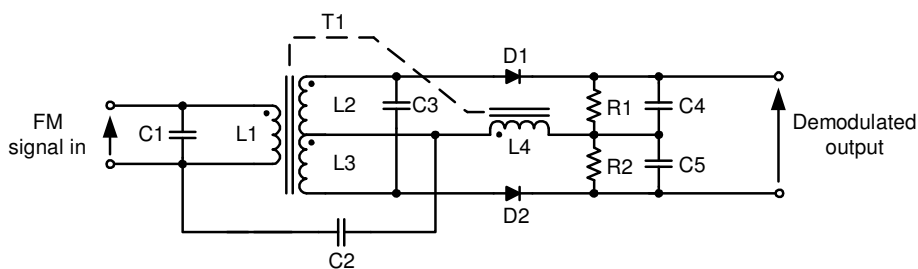


Figure 5.7 Circuit of a Foster-Seely discriminator

The operation of the Foster-Seely discriminator is based on the resonance characteristics of two tank circuits. In Figure 5.7, the primary tank circuit is consisted of C_1 and L_1 while the secondary tanks circuit is consists of C_2 , L_2 and L_3 . Both the tank circuits are turned to the centre frequency of the input FM signal. Choke L_3 is the DC return path for the rectifiers D_1 and D_2 and is inter-coupled to the core of L_1 , L_2 and L_3 . R_1 and R_2 are the loading resistors. C_4 and C_5 are the filter capacitors used to remove the high frequency components of the output voltage. The frequency response of the Foster-Seely discriminator is shown in Figure 5.8. The output voltage of the discriminator is zero when the input frequency is equal to the centre frequency of the carrier signal. When the input frequency rises above the center frequency, the output increases in positively. When the input frequency drops below the center frequency, the output decreases negatively.

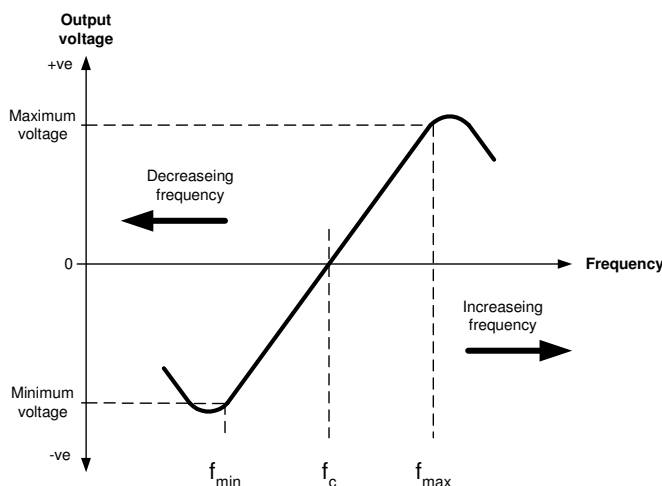


Figure 5.8 Frequency response of a Foster-Seely discriminator

In Figure 5.8, f_c is the centre frequency of the input signal while f_{\min} and f_{\max} are the minimum and maximum frequencies that the discriminator responds linearly to the

input frequency respectively. In the frequency range f_{\min} to f_{\max} , the output voltage of a Foster-Seely discriminator changes linearly as the input frequency varies between f_{\min} and f_{\max} . When the input frequency is above f_c , the output voltage of the discriminator is positive, vice versa. The Foster-Seely discriminator is sensitive to both frequency and amplitude variations, the amplitude variation of the input signal would be detected as noise and causes demodulation errors. To remove the amplitude variations, a limiter circuit is added. The limiter is consisted of a NPN transistor and RC circuits, it removes the amplitude variations by clipping the input signal into a constant amplitude square waves. Since the Foster-Seely discriminator is designed to respond according to a limited frequency range near to the centre frequency, no output variation would be contributed by the harmonics of the square wave.

As mentioned in the previous sections, being limited by the low frequency cut-off characteristic of the DC power bus, the original data are frequency modulated in special format and is transmitted in the form of current ripples by the transmitter. To facilitate signal receiving, the carrier signal is obtained from the current variation of the filtering capacitors. Since the receiver is connected in parallel to the loads on power bus, the impedance of the receiver circuits has to be as low as possible in order to ensure the signal current is large enough to be picked up. Signal receiving is facilitated by a cascaded 1:100 current transformer to the filtering capacitor where the primary winding of the current transformer has one turn only, the signal current is then stepped down by 100 times. The secondary side of the current transformer is connected to the limiter circuit of the Foster-Seely discriminator through resistors as the current transformer is an AC current source while the limiter is a current driven transistor circuit. The negative current output from the transformer is not useful to demodulation

and is therefore suppressed by a diode since only the period of the modulated signal is useful for regenerating the original data. The analog part of the proposed receiver is shown in Figure 5.9.

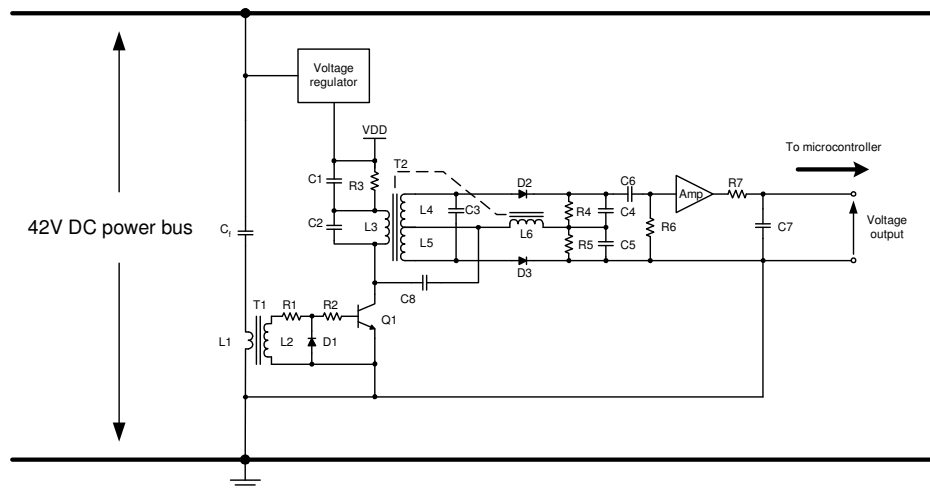


Figure 5.9 Analog part of the proposed receiver circuit

In order to avoid loading effect, the output of the Foster-Seely discriminator is amplified by an amplifier with high input impedance before being fed to the microcontroller. Since the output of the circuit which shown in Figure 5.9 is a series of voltage variation, it is digitized by the internal A/D converter and stored in the internal memory of the microcontroller for further operations such as error detection. The major tasks carried out by the microcontroller are listed as below:

- ◆ Communication protocol handling
- ◆ Error code decoding
- ◆ Error handling
- ◆ Data regeneration

In order to reduce the quantity of the component of the receiver circuit, these tasks are performed by the program stored in the flash memory of the microcontroller. The flow chart of the data receiving process is shown in Figure 5.10. Upon the frequency pattern corresponded to the first bit is stored in the memory buffer in digital format, the microcontroller would recognize whether it is a logic '1' or logic '0' according to the likeness between the received frequency pattern and the preset patterns of the two logic states. In this stage, the received pattern would be recognized as either logic '1' or logic '0' and would not be discarded no matter how the received pattern is distorted. The recognizing process must be finished before the next bit is received or otherwise data loss may occur. The recognized bit would then be stored in a memory cell which rotates one bit until all the bits of that memory cell are filled full. Having received 7 bits and stored in the memory, error detection would be performed. As described in the previous section, the original data is encoded by using (7,4)hamming code, thus only four of the received data bits carry original information where the rest are hamming code checksum. Due the data bus width of the selected microcontroller (8051F300) is eight bit, a dummy bit is inserted as the MSB and would not be processed. Since the error detection/correction process has to be finished before the arrival of the first bit of next data block, the error detection is achieved by means of table lookup instead of immediate calculation, which is realized by comparing the received data byte (includes one dummy bit) to the entries of a pre-calculated checksum table until a matching is found. A matching indicates that the received data is correct, or otherwise, one or more error bits present. Once an error is found, the error byte would be correlated to an error detection matrix for error correction, a one bit error would be corrected. For those more than one bit errors, the entire data byte would be discarded and a negative acknowledge would be sent for requesting retransmission.

Upon an error-free data byte is obtained, one cycle of regenerating the original data transmitted by the transmitter is finished. The regenerated data would be used as the command of device controlling or status of intelligent switches. For the intelligent switches, the regenerated data are in fact the commands submitted by the user and transmitted by the host controller for turning the appliances ON or OFF and selecting the operation mode. For the host controller, the regenerated data are the signal acknowledgements, monitoring results and urgent requests submitted by the intelligent switches.

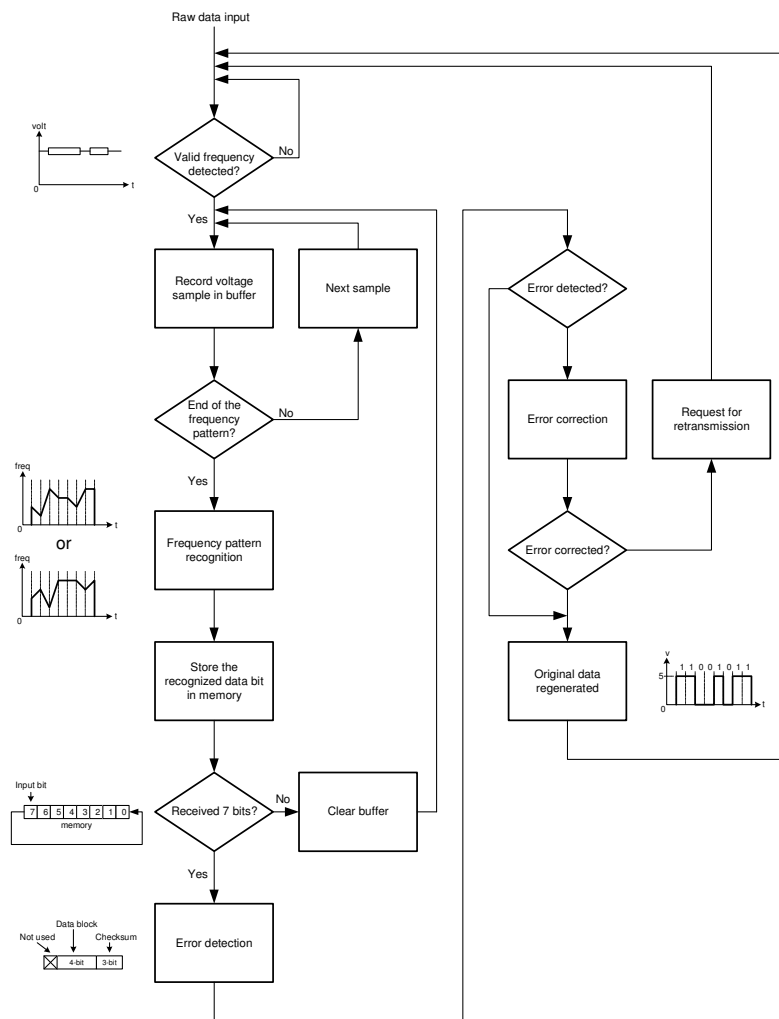


Figure 5.10 Flow chart of the data regeneration process at the receiver side

5.7 Power switching part of the intelligent switches

The power switching part of the intelligent switches is very simple, it is basically composed of a N-channel MOSFET, a High-side MOSFET driver and a current sensing circuit. The simplified circuit of the power switching part of the intelligent switches is shown in Figure 5.11.

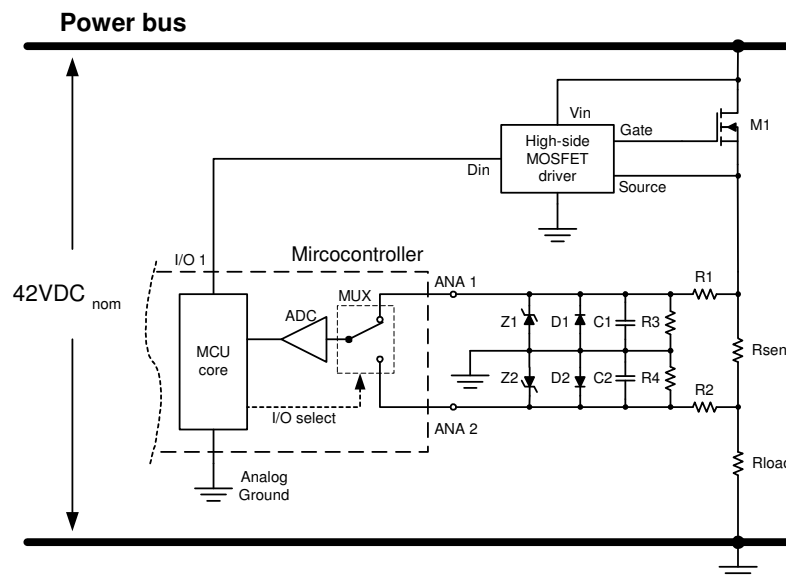


Figure 5.11 Power switching circuit of the intelligent switch

The reason of using high-side power switching instead of the simple low-side switching approach is because the appliances in modern vehicles are grounded through the chassis, which is in fact the electrical return path of the electrical power system. Though the circuit of low-side power switching is simple, it requires all the appliances to be isolated from the chassis which is nearly impossible in most cases. In order to

monitor the operation of the attached appliance, a current sensing resistor is connected between the MOSFET and the appliance. The voltage across the resistor is continuously detected by the A/D converter of a microcontroller (8051F300). The voltage across the resistor is obtained by subtracting the voltage across the load by the voltage of node X. Since there is only one A/D converter in the microcontroller, the A/D converter is multiplexed to detect the two voltages.

As both the voltage and current values of the appliance are obtained, gathered with the control commands received from the power net, the operation of the appliances can be classified into ten statuses as listed in Table 5.1 according to the symptoms detected. The intelligent switches are programmed to inspect the operation status of the attached appliance every one second and send the corresponding status code to the host controller upon request or when any failure is detected. When a failure is detected, the intelligent switch would automatically disconnect the appliance by turning off the MOSFET to avoid further damages. In the cases that the over current device is not able to be disconnected by turning off the MOSFET, the fuse is the last barrier for over current protection.

Status code dec (bin)	Operation status	Driving status of the MOSFET	Detected loading voltage value	Detected loading current value	Actions
1 (0001 _b)	Normal operation (ON)	ON	Average voltage +/- 10%	Average current +/- 10%	None
2 (0010 _b)	Normal operation (OFF)	OFF	0 Volt	0 Ampere	None
3 (0011 _b)	Load disconnected	ON	V _{in} +/- 10%	0	Turn off the MOSFET and report the error to host controller
5 (0100 _b)	Over current	ON	N/A	Average current + 30%	
6 (0101 _b)	Over voltage	ON	Average voltage + 30%	N/A	
7 (0110 _b)	Under current	ON	N/A	Average current - 30%	
8 (0111 _b)	Under voltage	ON	Average voltage - 30%	N/A	
9 (1000 _b)	MOSFET failure (shortened)	OFF	V _{in} +/- 10%	> 0 Ampere	
10 (1001 _b)	MOSFET failure (opened)	ON	0 Volt	0 Ampere	

Table 5.1 Errors detectable by the intelligent switches and the corresponding status code

5.8 Design of the Host controller

The host controller is composed of a signal transmitter for signal transmission and modulation; a signal receiver for signal reception and demodulation; a microcontroller for data exchange management and an interactive user interface that enables the users to control and monitor the operations of the whole intelligent switch system. The operation flow chart of the program executed by the host controller is shown in Figure 5.12.

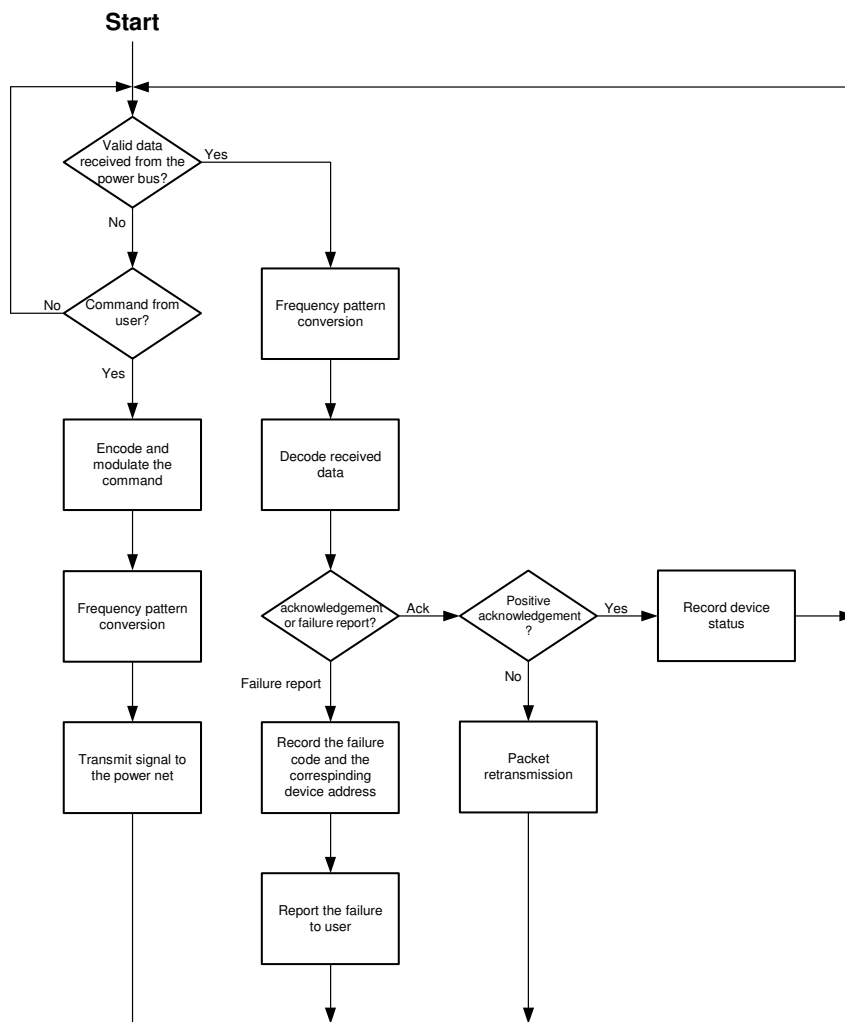


Figure 5.12 Operation flow chart of the program of the host controller

5.9 Simulations

In order to verify the designs of both the carrier transmitter and receiver circuits, simulations have been done by using PSpice. The circuit used in the simulations is presented in Figure 5.13. The circuit is basically composed of three parts, which are the DC power bus, carrier transmitter and carrier circuits discussed in the previous section. The aim of the simulations is to modulate and transmit two consecutive data bits (a logic '0' followed by a logic '1') to the receiver side through the DC power side. The frequency patterns that used to represent the logic states are identical to those shown in Figure 5.4. To simulate a practical DC power system, the power bus is terminated by a 4700uF capacitor (Cload) and a resistor (Rload). The MOSFETs M_1 , M_2 , M_3 and M_4 are driven by a frequency generator where the switching frequency is controlled by two programmable voltage sources V_{logic0} and V_{logic1} . The frequency generator is implemented by an analog behavior model (ABM) of Pspice. The nominal frequency of the generator is set at 120KHz where the output frequency equals to 120KHz multiplied by the voltage of V_{ctrl} . C3 is the additional capacitor that used to sense the ripple current transmitted by the transmitter. It is connected in series to the primary side of the current transformer consists of L_4 and L_5 for coupling ripple current from the DC power bus. In order to find out how the changes of the source voltage and loading resistance influence the performance of the communication system, several simulations using different source voltage and loading resistance have been done. The major parameters of the simulations are listed in Table 5.2 and the simulation results are shown in Figure 5.14 to Figure 5.19.

	Minimum	Maximum
Power net voltage	36VDC	48VDC
Carrier frequency	80KHz	120KHz
Loading resistance	0.5ohm	100ohm

Table 5.2 Major parameters used in the simulations

In Figure 5.14 to Figure 5.16, the trace at the top is the output voltage of the receiver circuit; the second trace is the current flows through the additional capacitor C_3 for signal pickup; the third trace is line voltage of the DC power bus while the last one is the original control voltage of the frequency generator of the transmitter circuit. In order to make the simulations simpler, only two data bits is transmitted; frequency patterns of logic '0' and logic '1' are transmitted at the time of 1.0ms to 2.0ms and 2.0ms to 3.0ms respectively. In the figures, the shape of the output voltage waveform under different loading condition are very similar to each other, it implies that the performance of the receiver circuit is independent of the loading resistance.

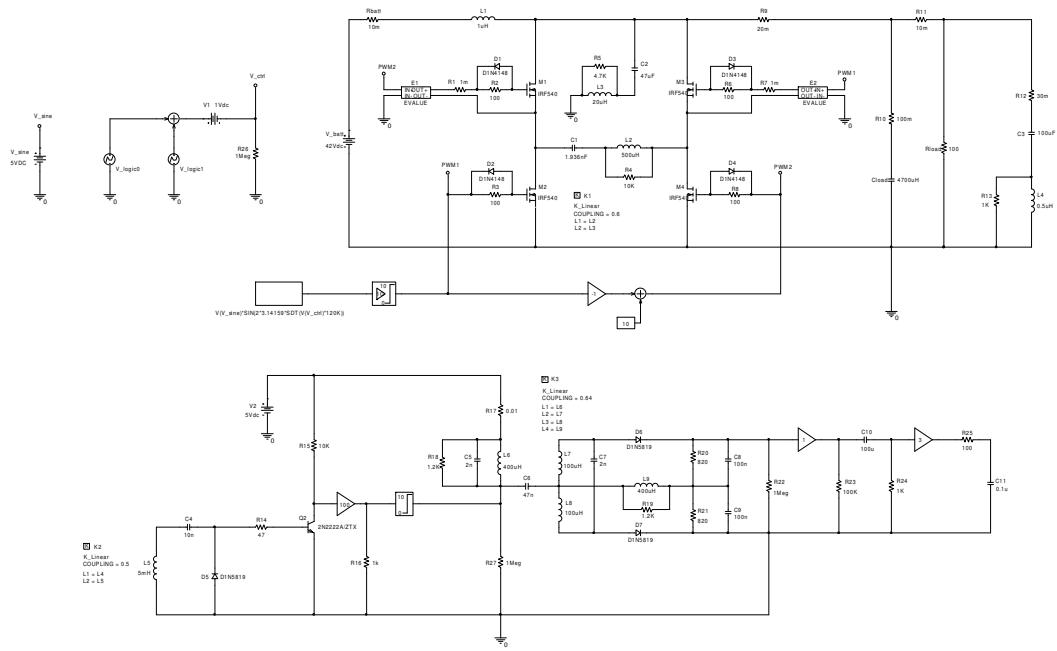


Figure 5.13 Transmitter and receiver circuits used in the Pspice simulations

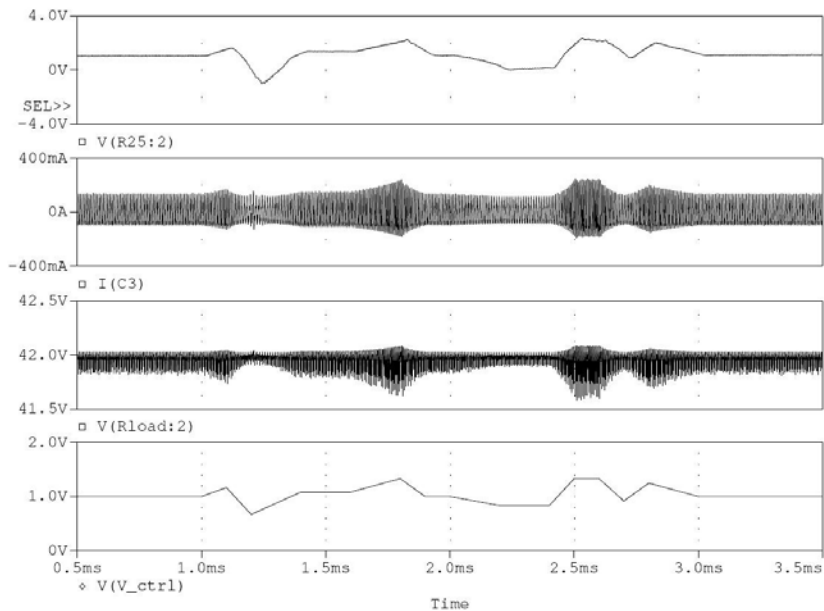


Figure 5.14 Pspice simulation results of the proposed DC power net communication system at 42VDC supply voltage and 100ohm loading resistance. Top trace: Output voltage of the receiver; Second trace: Current of capacitor C₃; Third trace: Voltage of the DC power bus; Forth trace: Modulation signal of the transmitter.

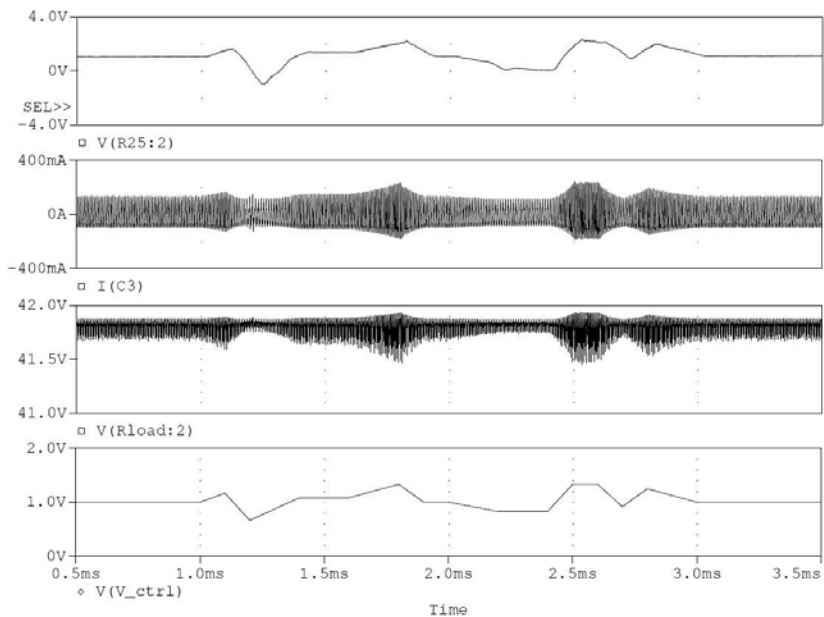


Figure 5.15 Pspice simulation results of the proposed DC power net communication system at 42VDC supply voltage and 10ohm loading resistance. Top trace: Output voltage of the receiver; Second trace: Current of capacitor C₃; Third trace: Voltage of the DC power bus; Forth trace: Modulation signal of the transmitter.

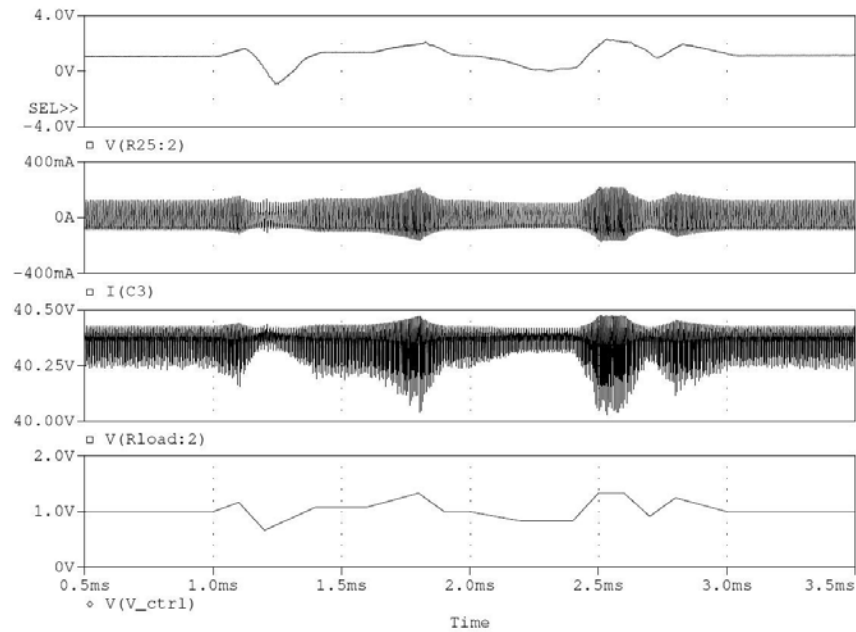


Figure 5.16 Pspice simulation results of the proposed DC power net communication system at 42VDC supply voltage and 1ohm loading resistance. Top trace: Output voltage of the receiver; Second trace: Current of capacitor C_3 ; Third trace: Voltage of the DC power bus; Forth trace: Modulation signal of the transmitter.

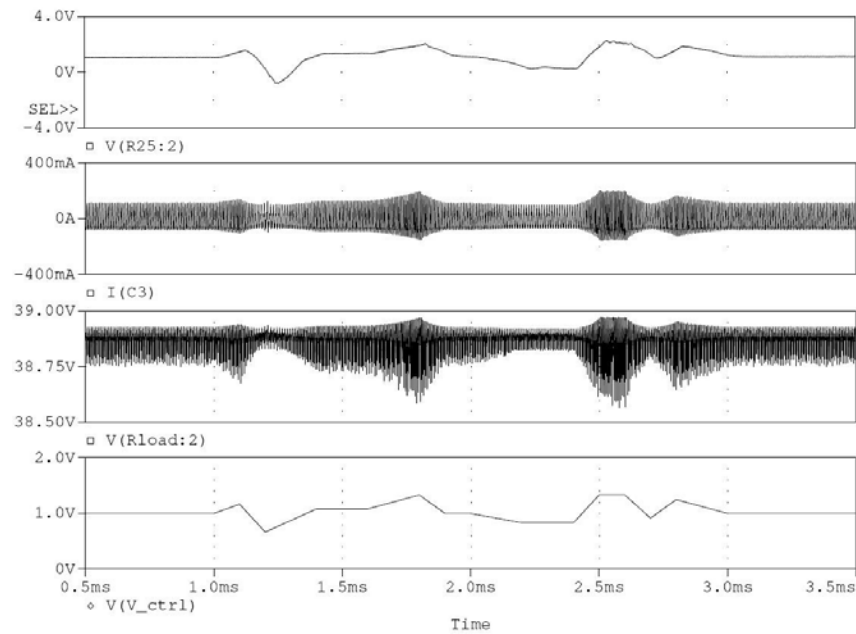


Figure 5.17 Pspice simulation results of the proposed DC power net communication system at 42VDC supply voltage and 500mohm loading resistance. Top trace: Output voltage of the receiver; Second trace: Current of capacitor C_3 ; Third trace: Voltage of the DC power bus; Forth trace: Modulation signal of the transmitter.

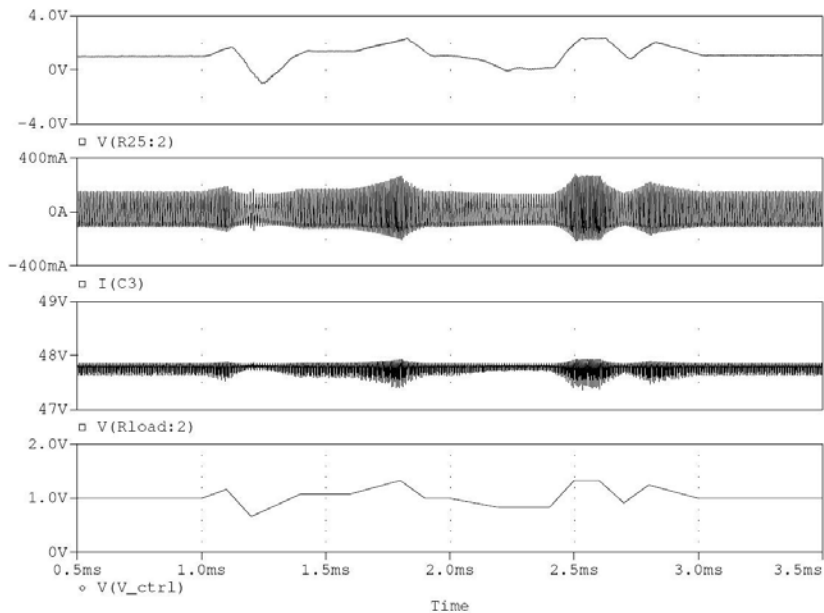


Figure 5.18 Pspice simulation results of the proposed DC power net communication system at 48VDC supply voltage and 1ohm loading resistance. Top trace: Output voltage of the receiver; Second trace: Current of capacitor C₃; Third trace: Voltage of the DC power bus; Forth trace: Modulation signal of the transmitter.

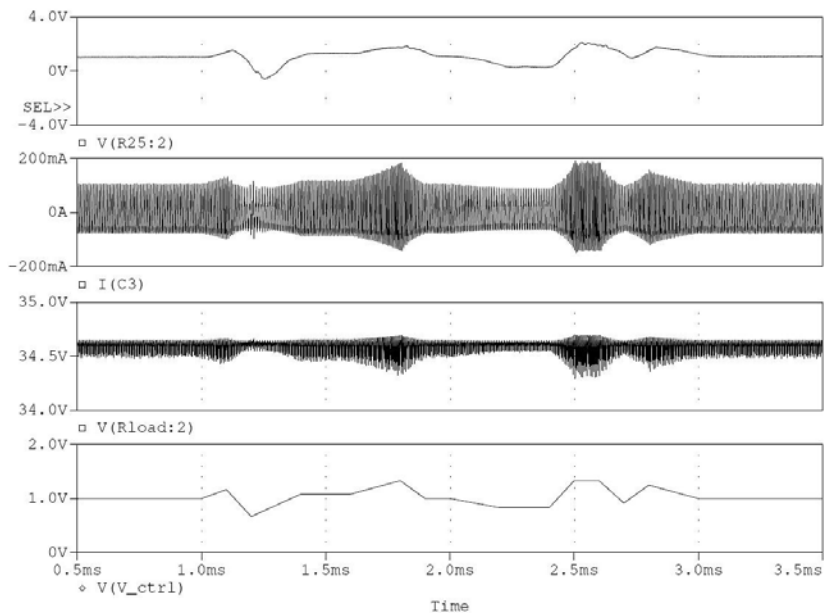


Figure 5.19 Pspice simulation results of the proposed DC power net communication system at 36VDC supply voltage and 1ohm loading resistance. Top trace: Output voltage of the receiver; Second trace: Current of capacitor C₃; Third trace: Voltage of the DC power bus; Forth trace: Modulation signal of the transmitter.

5.10 Experimental results

An intelligent switch system for 42V DC power net with one host controller and one intelligent switch is built. The circuits used are shown in Figure 5.20 and Figure 5.21 and have the parameters as listed in Table 5.2. The operations of the host controller and intelligent switch are following the flow charts shown in Figure 5.12 and Figure 5.10 respectively. In the system, a DC power supply (Sorensen DLM80-50E) is used as the power source to the power net, a 10ohm resistor paralleled and a 6800uf capacitor as connected to the power net as a load. They are connected by a pair of copper wires at 2.5 meters long while the intelligent switch is connected 0.5meter close to the power supply and the intelligent switch is connected in parallel to the 10ohm load. In order to evaluate the performance of the system, different loading current have been applied to the system. Figure 5.22 and Figure 5.23 shows the demodulated waveforms of logic '0' and logic '1' obtained at the output of the receiver circuit respectively. Figure 5.24 shows the ripple voltage on the 42V DC power net and the corresponding driving signal of the MOSFETs generated by the microcontroller. In the figure it can be seen that the square pulses generated by the microcontroller is converted into approximated sinusoidal signal by using the proposed transmitter circuit (Figure 5.2). Figure 5.2.5 compares the waveforms of the ripple voltage of the power net and the current signal picked up at the receiver circuit. In the figure, it can be seen that the received signal picked up at the receiver is a sinusoidal signal that the harmonics and noise are filtered by the DC power net. Figure 5.26 shows the response of the intelligent switch system at the transition of the carrier frequency increases from 80KHz to 120KHz.

In order to examine the performance of the prototype of the intelligent switch system, the relationship between the number of error packet and the loading resistance of the power net is investigate by a test practically. The test is facilitated by transmitting one hundred data packet through the power net and record the number of error packet under different loading resistance. The testing conditions are as listed in Table 5.3.

	Minimum
Power net voltage (VDC)	42
Loading resistance (ohm)	0.5 - 100
Cable length (meter)	5
Packet length (bit)	8
No. of packet transmitted	100

Table 5.3 Testing condition of the prototype of the intelligent switch system

Figure 5.27 shows the results of the testing. The error packets are those not correctable by the error correction system of the receiver. In the Figure, it can be seen that the number is error is kept at zero when the loading resistance is between 50 to 100 ohm. When the loading resistance is 20 to 40ohm, only one error packet is received out of the one hundred received packets, which is acceptable and can be solved by packet retransmission. The number of error packet starts to increase to two when the loading resistance is at 10 ohms and further increases to four when the loading resistance equals 0.5ohm. At a whole, the maximum error rate is 4% (4 errors out of 100), which the errors can be corrected by data retransmission.

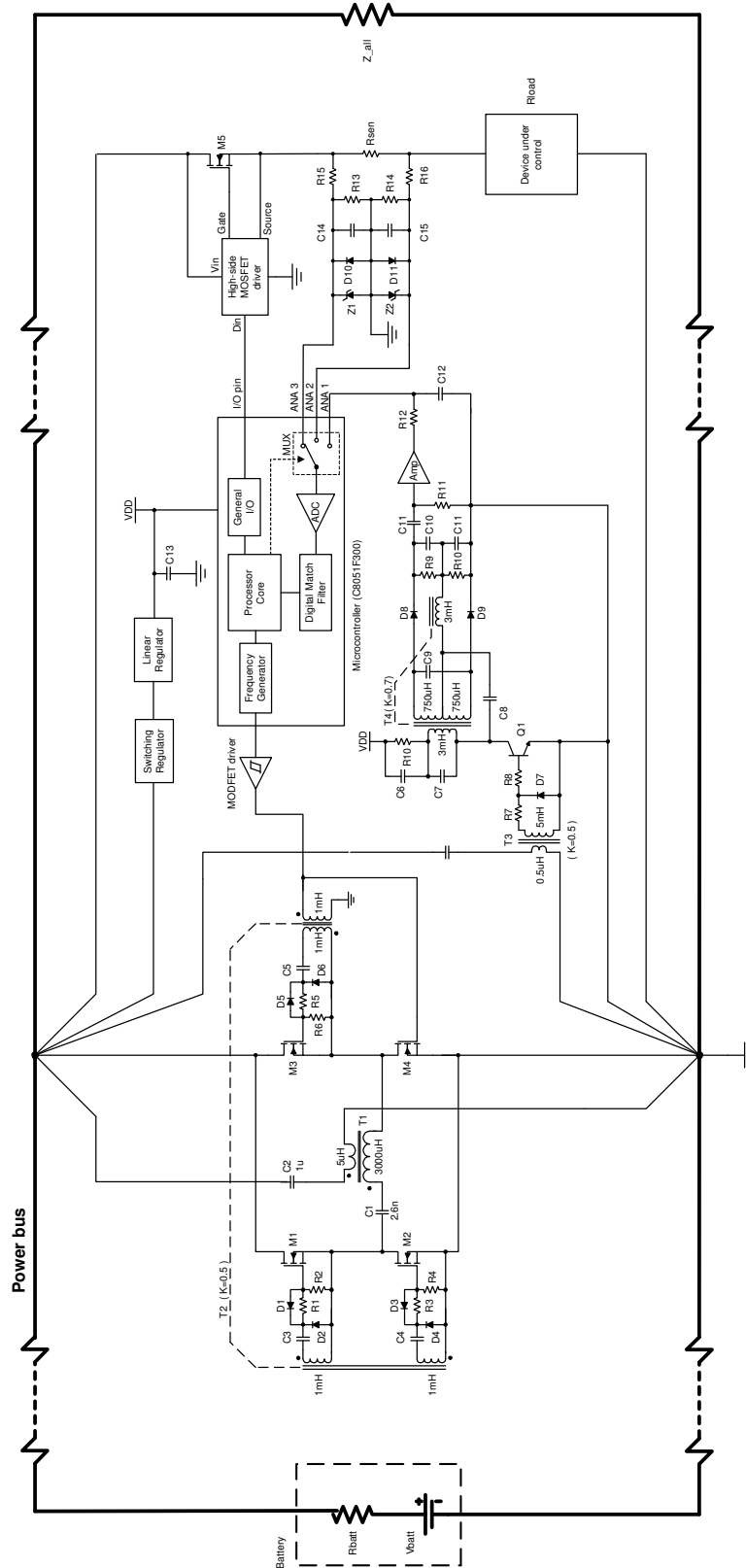


Figure 5.20 Practical circuit of the intelligent switch

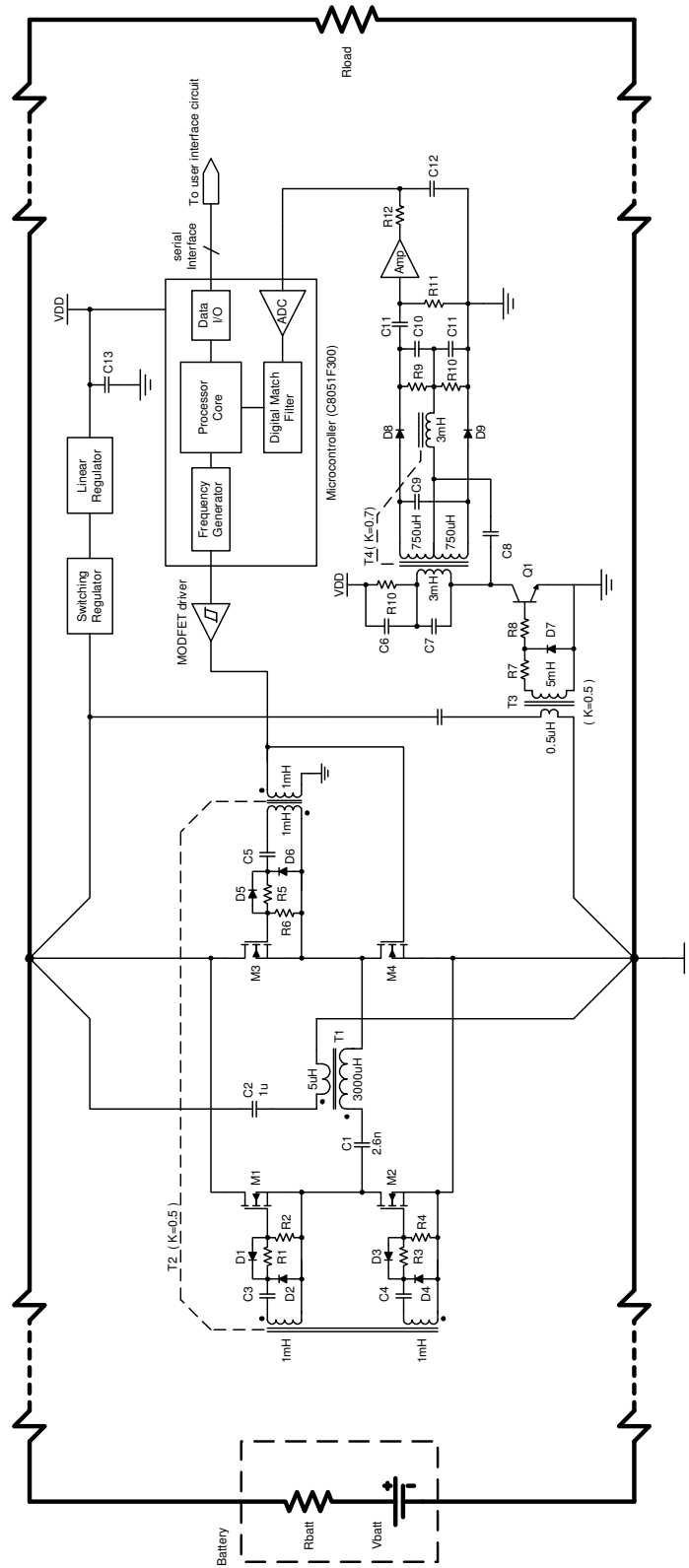


Figure 5.21 Practical circuit of the host controller

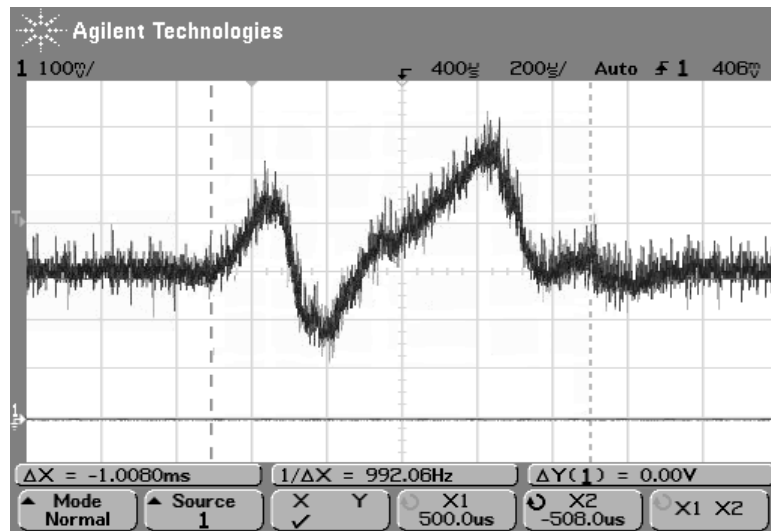


Figure 5.22 Output voltage of the receiver (Logic 0)

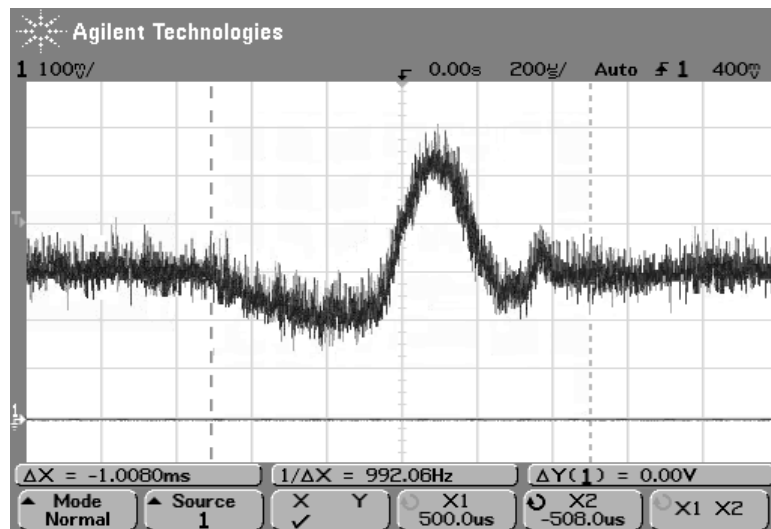


Figure 5.23 Output voltage of the receiver (Logic 1)

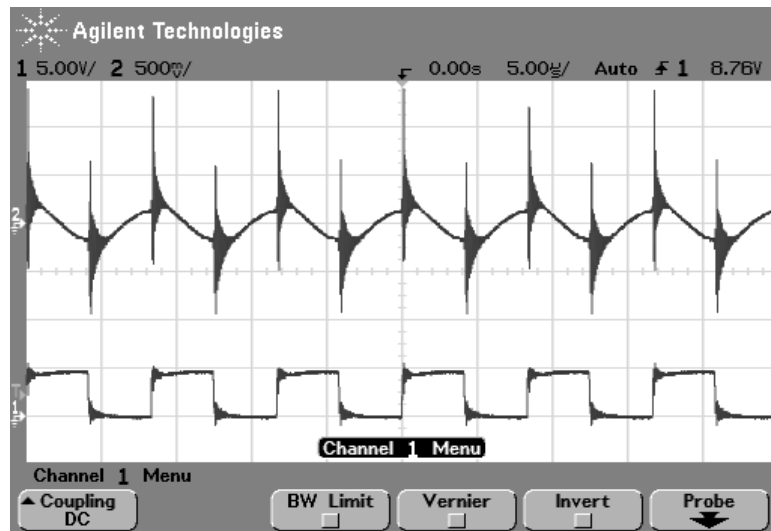


Figure 5.24 Experimental waveforms of the proposed intelligent switch system. Upper trace: Voltage ripple (carrier signal) on the power net, transmitted by the transmitter at 120KHz; Lower trace: MOSFET driving signal generated by the microcontroller.

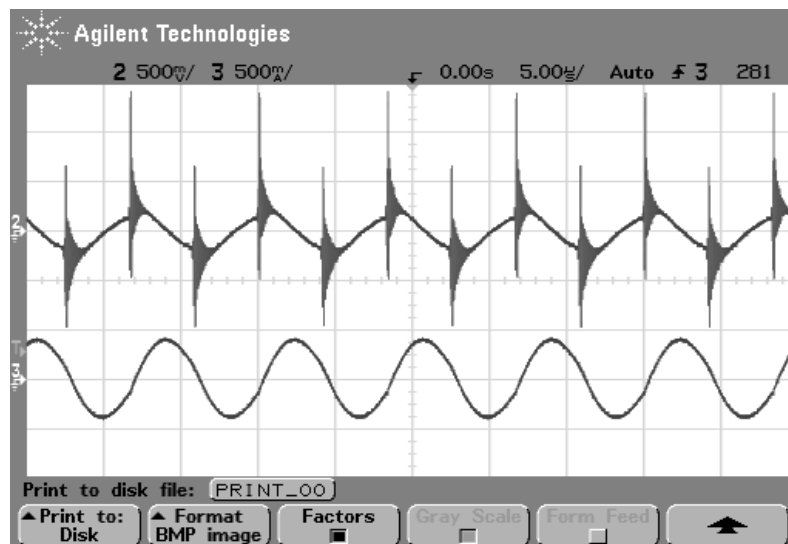


Figure 5.25 Experimental waveforms of the proposed intelligent switch system. Upper trace: Voltage ripple (carrier signal) on the power net, transmitted by the transmitter at 120KHz; Lower trace: Current ripple (carrier signal) picked up by the receiver circuit from the power net.

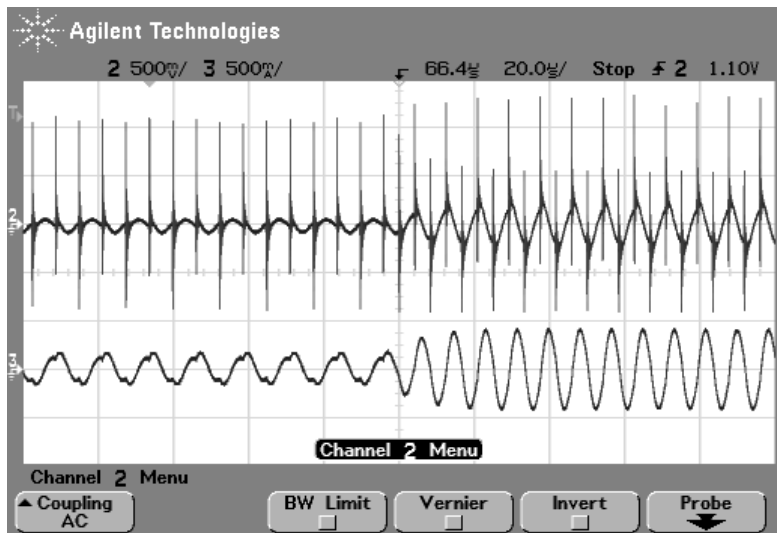


Figure 5.26 Experimental waveforms of the proposed intelligent switch system at the transition of the carrier frequency increases from 80KHz to 130KHz. Upper trace: Voltage ripple (carrier signal) on the power net, transmitted by the transmitter at 120KHz; Lower trace: Current ripple (carrier signal) on the power net.

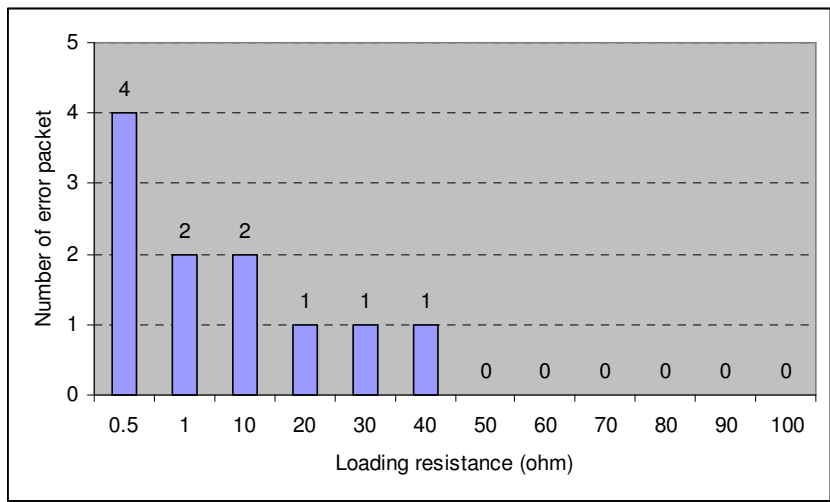


Figure 5.27 Relationship between the loading resistance of the power net and the number of error packet out of 100 received packet.

5.11 Conclusion

In this chapter, a design of intelligent switch system for 42V DC power net is discussed. By using the proposed transmitter and receiver circuits, data communication over the low impedance 42V DC power net is achieved. The output stage of the transmitter is operating in switch mode therefore the power dissipation of the entire transmitter is minimized. The original data are modulated into two kinds of frequency patterns; therefore, the noise rejection ability is improved. Pspice simulations and practical experiments have been carried out to verify the design of the intelligent switch system. The results show good performance of the proposed intelligent switch system on 42V DC power net.

Chapter 6

Conclusions and Suggestions for Future

Research

6.1 Introduction

This thesis presents a research on the implementation of an intelligent switch system for 42V DC power net in the new generation vehicles. The intelligent switch system allows the users to control the appliances in a vehicle remotely over DC power net. Conventionally, the electrical power system in vehicles is generally a star like network due to its simple design. However as the demand of in-vehicle automation increases, the power system in star structure suffers from weighty, costly and bulky to vehicle manufacturing. In order to simplify the power system for the new generation vehicles, a design of intelligent switch system with 42V DC power bus is proposed. For the design of the power system topology, the focus is put on the reduction of the power cable. For the circuit design of the intelligent devices, the focus is put on the integration of communication medium and the power cables. In this conclusion chapter, important results that have been obtained in the research are summarized, along with some suggestions for future work on in-vehicle control systems.

6.2 Contributions of the Thesis

In this section, the major contributions of this thesis are summarized into three topics.

1. Signal transmitter and receiver for DC power net

The feasibility of performing data communication over DC power net has been investigated. Due to the low and unpredictable impedance of the DC power net, a high power efficiency signal transmitter is needed especially in the noisy electrical environment of a vehicle. A signal transmitter that operates in switching mode is proposed to facilitate carrier signal transmission to the DC power net. The transmitter is consisted of a H-bridge circuit and a microcontroller. The H-bridge circuit is operating in switching mode where the switching frequency is controlled by the microcontroller according to the input data. In order to receive the carrier signal generated by the transmitter circuit, a receiver circuit which consists of a frequency-to-voltage convert and a microcontroller is proposed. Simulation and experimental results show the outstanding performance of both the transmitter and receiver circuits for data communication over 42V DC power net. The practical implementation of the power net communication system is discussed. Due to the simple circuitry of the proposed transmitter and receiver, it is shown that they can be integrated into a monolithic module, thus making the power net communication system to be simple installing and cost effective.

2. Modeling of a DC power net

Since the performance of the proposed intelligent switch system is closely related to the electrical characteristics of the DC power net, an electrical model of DC power net is introduced. An extensive analysis has revealed that the attenuation of the carrier signal is closely related to the length of the power cable. Pspice simulations have been carried out to verify the analytical results.

3. Special frequency modulation scheme for DC power net communication

By modulating the original data into two kind of predefined frequency patterns, the transmission error rate of the proposed intelligent switch system is greatly reduced. As a carrier signal travels through the DC power bus to the receiver, it is attenuated and distorted by the low-pass characteristic of the power net which leads to poor signal-to-noise ration and results in receiving errors. The special frequency modulation scheme helps in increasing the uniqueness of the transmitted signal in a noisy and low impedance power net. Since the frequency patterns received by the receiver are processed by a microcontroller with its stored program in the integrated memory, the component used in the receiver is minimized. This modulation scheme is applicable to the proposed intelligent switch system but also any DC power system that data exchange is need. Simulation and experimental results confirm the theoretical predictions.

6.3 Suggestions for Future Research

In order to further improve the performance of the intelligent switch system, further research can be carried out in the following directions:

1. Increase the data rate of the DC power net communication system

Since the proposed intelligent switch system manages all the operations of the in-vehicle electrical system, as the number of intelligent switches increase, it is advantageous to have a faster response with higher transmission data rate. In order to introduce an intelligent switch system with higher communication data rate, a microcontroller with higher operation speed is needed. Theoretically the communication data rate is possible to be increased by simply increasing the carrier frequency. However, as the number of the intelligent switches increases, the impedance of the entire system will be further decreased, in order to adapt the proposed intelligent switch to the applications that high communication speed is required, it is necessary to investigate the characteristics of the complete system.

2. Error correction coding for the original data stream

In the design of the proposed intelligent switch system, the original data stream is encoded by using hamming code which is able to recover one bit error. For those extremely noisy environments, hamming code may not be adequate. In order to ensure an acceptable average data rate, error codes with higher security can be used.

Appendix

In this appendix, Figure A.1 shows the complete simulation circuit shown in Figure 3.10. Figure A.2 shows the complete circuit shown in Figure 5.13.

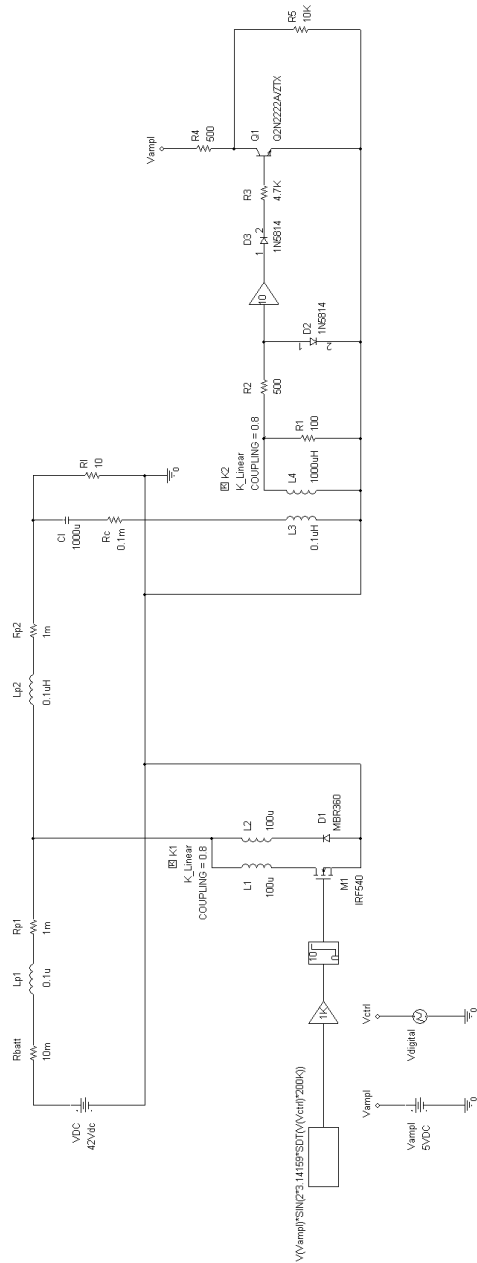


Figure A.1 Complete simulation circuit of Figure 3.10

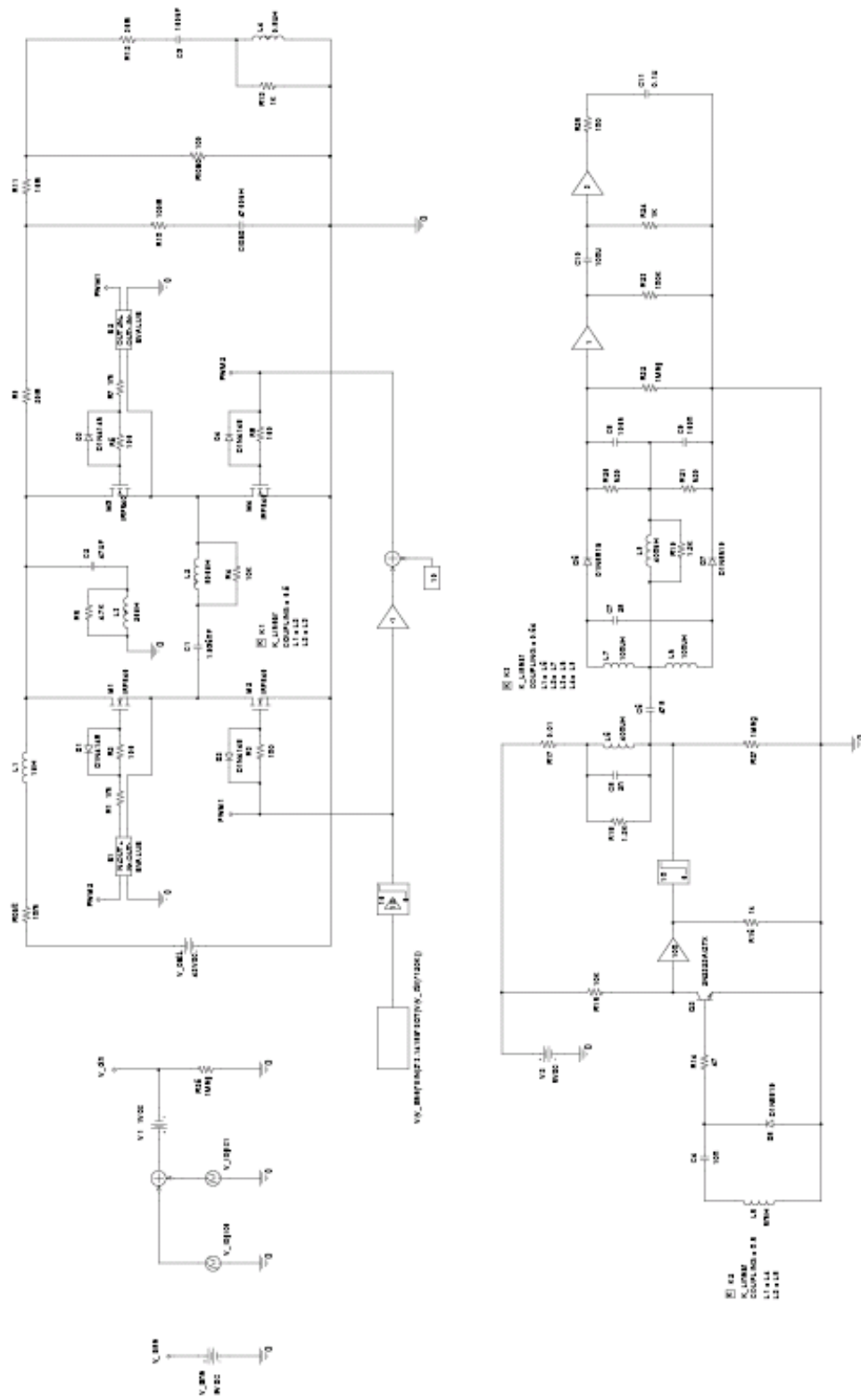


Figure A.2 Complete simulation circuit of Figure 5.13

Publications

Conference papers

- [1] Siu-Hong Wong, David Ki-Wai Cheng, Yin-Shu Lee and Martin H.L. Chow, “Design of Intelligent Switch System for In-vehicle Control Application”, Proceedings, IEEE Power Electronics Specialists Conference 2005 (PESC), pp. 1865-8, June 12-26, 2005, Recife, Brazil.

- [2] Siu-Hong Wong, David Ki-Wai Cheng, Yin-Shu Lee and Martin H.L. Chow, “Design of Intelligent Switch System for Modern Vehicles”, Proceedings, International Conference on Instrumentation, Control and Information Technology. (Sponsored by the Society of Instrument and Control Engineers (SICE) and technically cosponsored by IEE/IES, IEEE/RAS, IEEE/CSS, IEEE/SMC, The Instrumentation, System and Automation Society (ISA)), pp. 1430-3, 8-10 August 2005, Okayama, Japan.

- [3] K.Y. Kan, S.H.Wong, D.K.W. Cheng and Y.S.Lee, “Intelligent Switch in 42V DC Power Net”, Proceedings, IEEE Power Electronics Specialists Conference 2004 (PESC), pp. 1149-54, June 20-25, 2004, Aachen, Germany.

References

- [1] Kwasniok, P.J.; Bui, M.D.; Kozlowski, A.J.; Stanislaw, S.S., “Technique for measurement of powerline impedances in the frequency range from 500 kHz to 500 MHz” *Electromagnetic Compatibility, IEEE Transactions on* Volume 35, Issue 1, Feb. 1993 Page(s):87 – 90
- [2] T. Teratani, K. Kuramochi, H. Nakao, T. Tachibana, K. Yagi and S.Abou, “Development of Toyota Mild Hybrid System (THS-M) with 42V PowerNet”, *Electric Machines and Drives Conference, 2003. IEMDC'03. IEEE International*, Volume: 1, 1-4 June 2003, Page: 3-10.
- [3] Rice, B.F., “A multiple-sequence spread spectrum system for powerline communications” *Spread Spectrum Techniques and Applications Proceedings, 1996., IEEE 4th International Symposium on* Volume 2, 22-25 Sept. 1996 Page(s):809 - 815 vol.2
- [4] Gershon, R.; Propp, D.; Propp, M., “A token passing network for powerline communications” *Consumer Electronics, IEEE Transactions on* Volume 37, Issue 2, May 1991 Page(s):129 – 134
- [5] Beikirch, H.; Voss, M., “Powerline communications interface in CSMA/CA-networks” *Emerging Technologies and Factory Automation, 2003. Proceedings. ETFA '03. IEEE Conference* Volume 2, 16-19 Sept. 2003 Page(s):117 - 120 vol.2
- [6] Yi-Fu Chen; Tzi-Dar Chiueh, “A 100-kbps power-line modem for household applications” *VLSI Technology, Systems, and Applications, 1999. International Symposium on* 8-10 June 1999 Page(s):179 – 182
- [7] Lee, Y.-S.; Cheng, D.K.W.; Wong, S.C., “A new approach to the modeling of converters for SPICE simulation,” *Power Electronics, IEEE Transactions on* , Volume: 7 , Issue: 4 , Oct. 1992
- [8] Zimmermann, M.; Dostert, K., “A multipath model for the powerline channel,” *Communications, IEEE Transactions on* , Volume: 50 , Issue: 4 , April 2002
- [9] Zimmermann, M.; Dostert, K., “Analysis and modeling of impulsive noise in broad-band powerline communications,” *Electromagnetic Compatibility, IEEE Transactions on* , Volume: 44 , Issue: 1 , Feb. 2002

- [10] Olsen, R.G., "Technical considerations for wideband powerline communication-a summary," Power Engineering Society Summer Meeting, 2002 IEEE , Volume: 3 , 21-25 July 2002
- [11] Hans-Dieter Hartmann, Sican GmbH, Hannover, "Standardisation of the 42V PowerNet-History, Current Status, Future Action", HDT conference "42V-PowerNet: The first Solutions", Villach, Austria, Sept.28-29,1999, Page:1-4.