The Hong Kong Polytechnic University

Department of Electronic and Information Engineering

# Design of a 1kVA Intelligent Voltage Sag Compensator for Semiconductor Industry

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A thesis submitted in partial fulfillment of the requirements for the degree of Master of Philosophy

March, 2012

# CERTIFICATE OF ORIGINALITY

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# Abstract

Nowadays, in order to achieve high automatic production processing and decrease the human working hours, more and more voltage sensitive equipment are in widespread use in the industry. The power quality problem of voltage sag has become a major apprehension in semiconductor industry. The voltage sensitive equipment in semiconductor processing includes an adjustable speed motor, microcontroller, AC controller relay and PLC etc. This equipment could be easily interrupted by voltage sags in the AC mains. The voltage sag possibly stops the working process and causes damage in the equipment. As a result, the whole manufacturing semiconductor process could be delayed while for waiting repair. Furthermore, voltage sag is an unpredictable event; it causes semiconductor production to be continuously behind in the market needs. Therefore semiconductor industry directly relates to the voltage sag problem.

This thesis explains the issue of power quality problem arising from voltage sags, which affects the semiconductor industry. The characteristics of the voltage sag are investigated and the existing solutions to solve the voltage sag problem are evaluated. A new topology of parallel type AC voltage sag compensator is introduced. The compensation method of the AC voltage sag compensator is discussed in detail with program a flow chart and circuit block diagram. The function of this compensator is to tolerate transient open-circuit faults in the AC mains during voltage sag compensation period. A practical 120Vac 50Hz/60Hz 1kVA intelligent voltage sag compensator is constructed for evaluating the compensation method. Experimental results show the compensator can support sensitive equipment under different types of voltage sags.

# Acknowledgements

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**Publications**

1. Hon-Chee So, Yim-Shu Lee, and Martin H. L. Chow, "Design of a 1-kVA parallel-type AC voltage sag compensator," *Power Electronics, IET*, vol.5, no.5, pp.591-599, May 2012
2. Yim-Shu Lee, Hon-Chee So, and Martin H. L. Chow, "Design of Voltage Sag Compensators," *IEEE 6th International Power Electronics and Motion Control Conference 2009*. pp.2587 – 2590, May 2009

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# Chapter 1: Background

## 1.1 The power quality problem: voltage sag

Nowadays power quality problem [1-3] is a major concern in the industry. With the deregulation of the electricity market, has resulted in an increased number of generators connected to the power grid, the situation has become even worse. Sensitive loads such as programmable logic controllers, AC contactors, and computer numerical control units can easily malfunction under transient power interruptions. Previous research [4-9] has discovered that poor power quality increased the cost of production in the industry. According to a report from Electric Power Research Institute (EPRI) in 1991, the economic losses are due to poor power quality that amounted to $400 billion dollars per year in the United States [4].

Voltage sags are major sources of power quality problem which are generated by short interruptions at power networks. A Canadian National Power Quality Survey [10] defines a “single voltage sag incident” as “the occurrence of one or more voltage sags on one or more phases within one second”. An example of voltage sag waveform is shown in Fig. 1.1. AC mains are temporary reduced of its nominal voltage for 6 cycles, before it returns to its nominal voltage. It is estimated that over 90% of the AC mains power interruptions are due to voltage sag incidents.

Voltage sags are unpredictable incidents and are randomly caused by different sources. These sources could be classified into three types. The first type is induced by the AC power transmission network such as accidental short circuit or open circuit in the power line or socket. The second type is coming from environmental factors [11] such as lightning strikes or faulty solar-panel inverters. The third type is caused by loading changes [12-14] such as the starting of a large

motor or air conditioner. In all these cases, the resultant voltage sag influences the normal operation of sensitive equipment. As a result, the automatic production processing is required to work against all such interferences in industry [13].

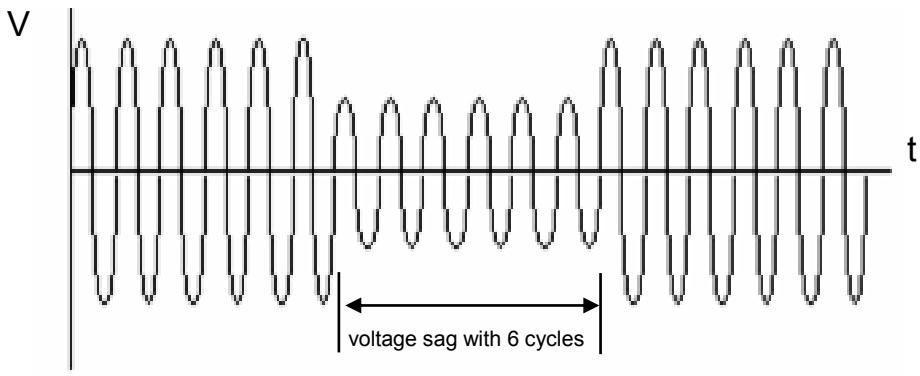



Fig. 1.1 Example of typical voltage sag in power network with 6 cycles at 50% sag depth

Electronic devices in the industry such as: programmable logic controllers (PLCs), sensors, robots, computer numerical control (CNC) machines, adjustable-speed drives, AC relays, and contactors are highly sensitive to voltage sags [15]. In practice, voltage sags have different sag durations and voltage shapes which are factors affecting the operations of equipment. In order to minimize the effect of voltage sags, the semiconductor industry introduces some regulations on the production processing to minimize using the sensitive devices in critical applications. However, the application of the sensitive devices is still essential in semiconductor industry equipment. Semiconductor manufacturers are looking for solutions to solve the voltage sag effect on the equipment in order to reduce economic loss.

## 1.2 Semiconductor industry and the organization of SEMI

The term “semiconductor industry” is often used to mean a group of semiconductor device manufacturers. Eminent examples of such manufacturers include Intel Corporation and Texas Instruments in United States of America (USA), Samsung Electronics in South Korea, Toshiba Semiconductors and Sony

in Japan, ST Microelectronics in Italy and France, for example. These international manufacturers mainly focus on the fabrication of semiconductor devices such as diodes, transistors, thyristors, linear integrated circuits, digital integrated circuits, application specific integrated circuits (ASICs) and CPUs.

An organization known as Semiconductor Equipment and Materials International (SEMI) was established in 1970. SEMI is a trade association representing more than 2300 member companies that includes develop and manufactured materials, devices and equipment, providing services and new technology to support the manufacturing of semiconductors, photovoltaic cells, and flat panel displays (FPDs). It has been stated from SEMI organization that "The member companies are the engine of the future, enabling smarter, faster and more economical products that improve our lives". SEMI generates a series of standard specification to the semiconductor industry. The aims of these standards are to ensure an open market in the new industry and to lower the semiconductor manufacturing cost. In the 1990s, the importance and size of SEMIs have enabled it to become a global semiconductor equipment manufacturer representative. The advanced critical technologies support a 100 billion global market.

## 1.3 SEMI F47

As stated previously, SEMI announces standards to decrease the production cost of semiconductor industry. So as to tackle voltage sag problems in the semiconductor industry, the SEMI was defined in 1996, a voltage sag immunity standard, entitle SEMI F47-0200 [16] and SEMI F42-0200 [17], for semiconductor processing equipment manufacturers. Equipment compliant to this standard must meet the specified immunity characteristics against voltage sags without the use of lead acidic batteries. The standard was redefined in 2006, as SEMI F47-0706 [18] and expected new semiconductor processing equipment design to be compliant. SEMI F47-0706 requirement will be extended to other application areas. IEEE standard of IEEE 1346 [20], European standard of EN50160 [20], and IEC [21] have similar guidelines for different equipment on voltage sag immunity.

## 1.4 Objective of the thesis

Fig. 1.2 highlights a key part of this thesis that will be considered. In real life, AC mains might contain voltage sag from different causes which will be explained in this thesis. In order to guarantee the equipment to operate under nominal voltage without disturbance from unpredicted voltage sag, devices called voltage sag compensators or protectors are designed and implemented between the power source and equipment. In Fig. 1.2, although two cycles of voltage sag appear at the output voltage of AC power source (V1), the compensator could regenerate nominal voltage (V2) to the equipment.

*Chapter 1: Background*

Plenty of papers and research discuss voltage sags problems. Modeling and simulation of voltage sag immune devices are also crucial topics for research study based on the theoretical assumption, however, only few papers or research focuses on design and construction of a practical voltage sag compensator. This thesis is to fill this by a well-organized compendium of useful information for engineers to develop a practical voltage sag compensator for satisfying industry needs. A series type voltage sag compensator will be discussed, which has already been developed and exists in market today.

The objective of this research project is to analyze the characteristics of voltage sags, based on previous research and design, and to develop a new parallel type of practical AC voltage sag compensator for the semiconductor industry. A topology of parallel type voltage sag compensator will be discussed, which was not discussed in previous research. It could be a new topology for solving voltage sag problems in the semiconductor industry. In fact, a similar approach already exists in uninterruptible power supply (UPS) systems, but using lead acid batteries is not suitable for the semiconductor industry. In this design, the voltage sag compensator mainly focuses on the requirements of semiconductor industry standard SEMI-F47. A 1kVA voltage sag compensator prototype is constructed to meet the semiconductor industry needs. This prototype circuit is based on some fundamental power electronics circuits like: voltage double circuit, boost converter, inverter and microcomputer unit. Hardware design will also be outlined in this research step by step. The software program is developed originally based on these hardware circuits. This prototype demonstrates that the topology of parallel type voltage sag compensator can solve voltage sag problems.

This research provides a novel solution for immunity of voltage sag problems. Intelligent control interfaces are integrated into the voltage sag compensator, which allow users to apply the compensator to different devices. The high reliability protection mechanism is also developed in the project. Based on this topology of voltage sag compensator, the power rating can be increased by additional hardware components. Software control can also be upgraded by programming the microcomputer controller.

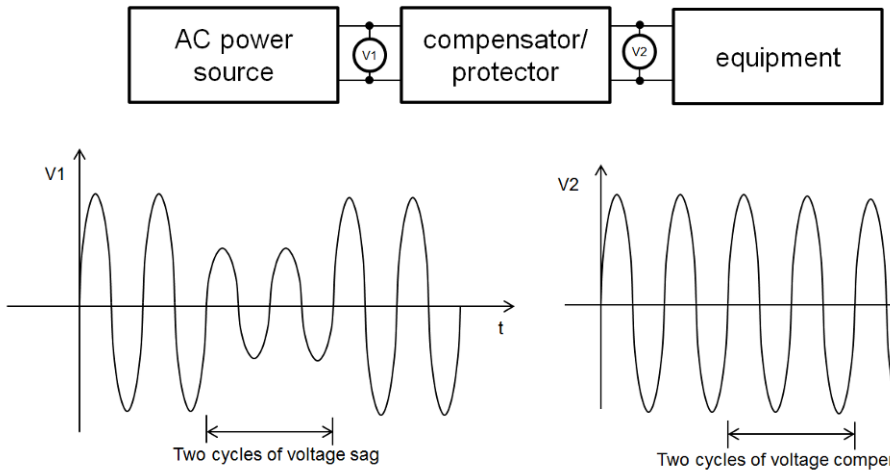



Fig. 1.2 Application of voltage sag compensator/protector

## 1.5 Outline of the thesis

This thesis is composed of this introductory chapter and six other chapters and appendixes. Chapter 2 provides an outline about the characteristics and classifications of the voltage sag from previous researchers. Several voltage sag mitigation devices are reviewed for different applications. The existing industrial standards on voltage sag are also summarized. Some suggestions are also given in to minimize the effects of voltage sag. Chapter 3 investigates the basic operation theory of the voltage sag compensator as well as the topology of series and parallel type compensators. Chapter 4 describes the hardware design of the voltage sag compensator. Chapter 5 explains the advantages using software control for the voltage sag compensator. Chapter 6 illustrates the experimental results of a 120Vac 1kVA voltage sag compensator to achieve semiconductor industry requirements. Finally, Chapter 7 presents a conclusion of this thesis and suggests future improvements.

## 1.6 Summary

A short introduction on voltage sag problem is offered. The SEMI group of companies and the standard of SEMI-F47 are briefly introduced. The objective and outline of this thesis are described in this chapter. Various research results and some existing standards on voltage sag problems will be further reviewed in the next chapter.

# Chapter 2: Previous research and existing standards on voltage sag

## 2.1 Introduction

This chapter begins with a review of previous research related to the effects of voltage sags. The characteristics of voltage sags are examined, while solutions and previous literature on voltage sags immunity will be discussed. The standard of SEMI F47 published by semiconductor industry is also studied in this chapter. To help minimize the influence of the voltage sag incidents, the sensitivity of different devices on voltage sag is considered. Some practical solutions are suggested to achieve voltage-sag immunity. The purpose of these reviews is to provide an understanding of the previous research in this area, as well as identifying areas with potential for extended research.

## 2.2 Voltage sags in industry

According to the research findings from “Canadian National Power Quality Survey: Frequency of Industrial and Commercial Voltage Sags” [10], the probability of appearance of voltage sags in industrial sites is higher than that in commercial sites. The results were collected from monitoring 22 utilities in Canada and 550 sites in industrial and commercial electrical users for 3 year period.

Fig. 2.1 illustrates the datum related to the frequency of occurrence of voltage sags at the 120/208V utility secondary voltage level at commercial customer sites. Fig. 2.2 shows the corresponding data at the utility primary voltage level, also at commercial customer sites. The result indicated that voltage sags occurrence at the secondary voltage level is more frequent than that of occurrence at the primary level.

Fig. 2.3 exemplifies the frequency of occurrence of voltage sags at utility primary voltage level at industrial customer sites. The average number of voltage sag incidents at industrial sites is higher than that of commercial sites. Some industrial sites experience significantly high frequency of voltage sags, around 50-60 sags per phase per month, at the primary voltage level. Fig. 2.4 shows the frequency of occurrence of voltage sags at the secondary voltage level at the industrial customer sites. The frequency of voltage sags in this group is the highest comparing with other groups. It is because the loading in the industry facilities consists of high power consumption devices and large motors. Furthermore, the industrial processes involve heavy load switching. System faults at the industrial sites could easily affect the power stability of the network.

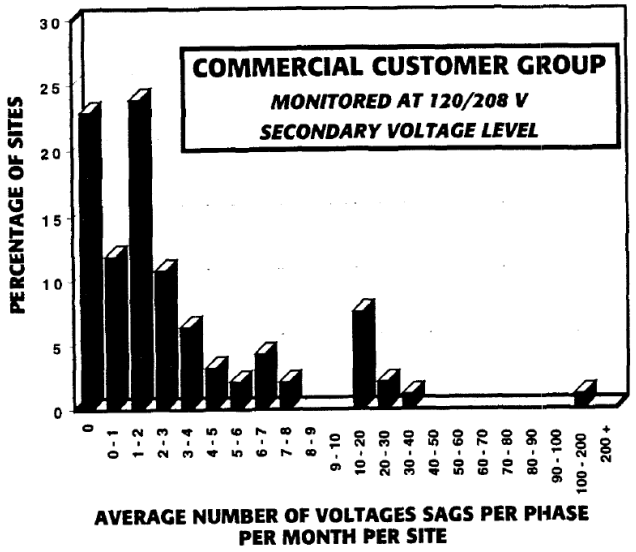



Fig. 2.1 Percentage of sites versus the average number of voltage sags per phase per month per site (commercial customer group - monitored at 120/208V secondary voltage level) [10]

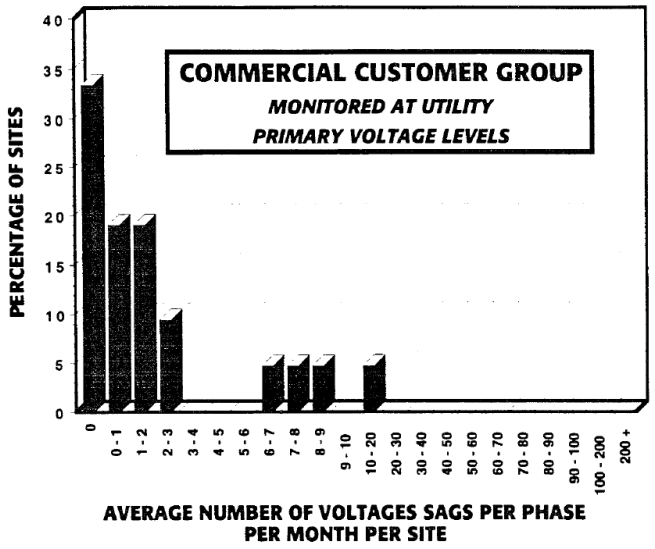



Fig. 2.2 Percentage of sites versus the average number of voltage sags per phase per month per site (commercial customer group – monitored at utility primary voltage levels) [10]

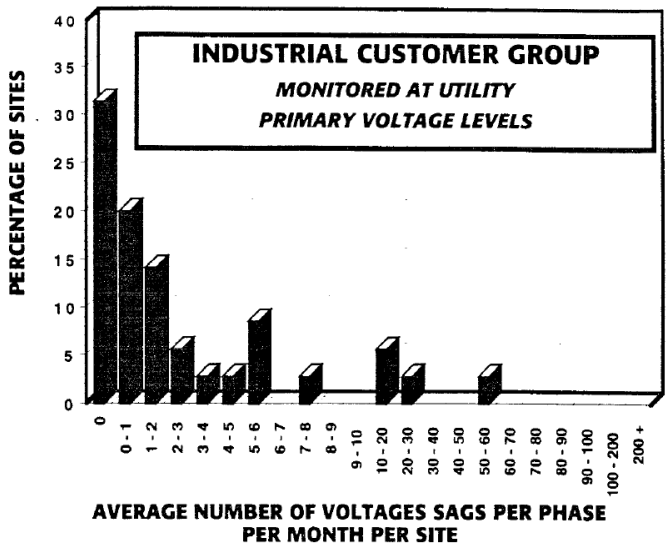



Fig. 2.3 Percentage of sites versus the average number of voltage sags per phase per month per site (industrial customer group - monitored at utility primary voltage levels) [10]

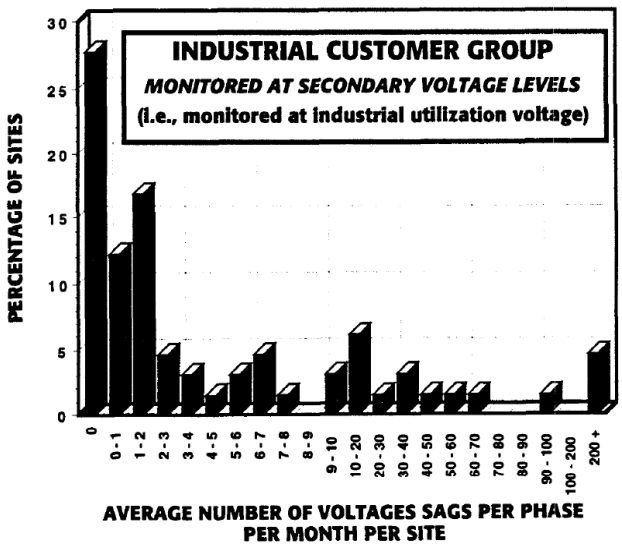



Fig. 2.4 Percentage of sites versus the average number of voltage sags per phase per month per site(industrial customer group - monitored at secondary voltage levels) [10]

Voltage sag is a major concern in industrial systems. McGranaghan [12] commented that "Voltage sags are the most important power quality problem facing many industrial customers." In industrial systems, the most sensitive equipment include motor contactors, electromechanical relays, high-intensity discharge (HID) lamps, adjustable speed motor drives (ASD), and programmable logic controllers (PLC). These devices may malfunction, shutdown, get damaged or reset during voltage sag incidents.

Voltage sags lead to huge economic loss in industrial plants. After a voltage sag incident, the equipment in production lines may have to be stopped for maintenance if the equipment becomes damaged. Assembling the semi-product may need to be discarded due to degradation of product's quality. Furthermore, the delay in delivery of the products may also result in customer's dissatisfaction. Therefore the semiconductor industry is extremely concerned with voltage sags.

The causes of voltage sags can be basically separated into two categories: external and internal causes. Both are unpredictable and unavoidable. The external causes include power system problems in the power distribution plant and the

wiring structure of transmission line and environmental problems arising from lightning, animal's activities and constructions. The internal causes include heavy load starting at normal operation, short circuit faults in the AC mains or abnormal use of electricity in the factory. However, although the causes of voltage sags can be classified, there is no cure-all solution to stop these voltage sag events up to now.

A typical example of voltage sag due to heavy load starting is examined in Fig. 2.5. The figure shows that the root mean square (RMS) voltage during motor starting, the RMS voltage temporarily drop to 80% and take ~3.8s to recover. The sensitive equipment can easily be influenced at this duration. This type of incident frequently appears in industrial plants.

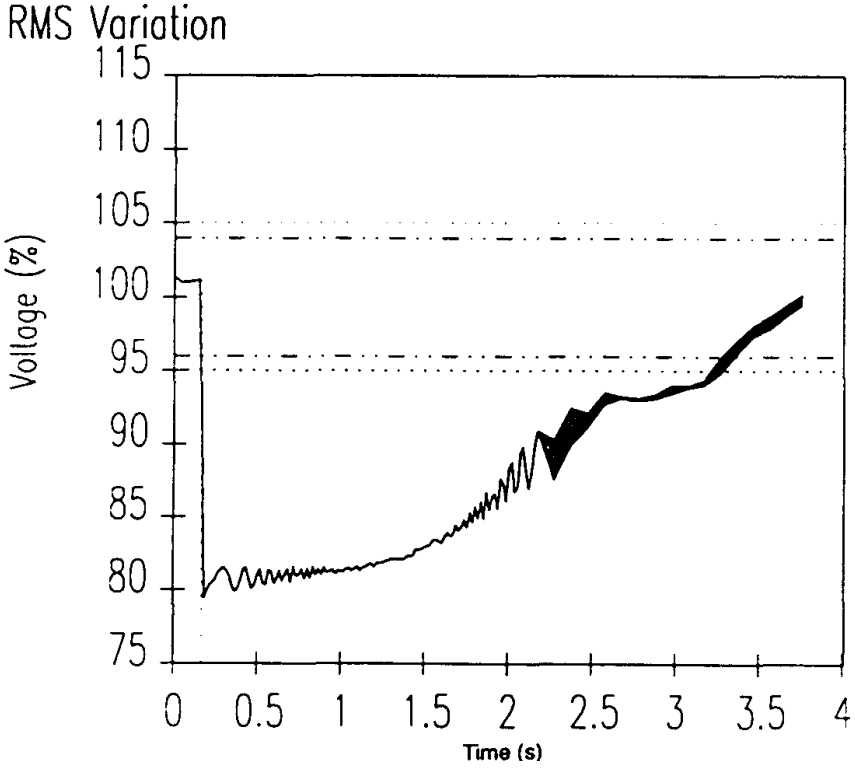



Fig. 2.5 Temporary voltage sag caused by motor starting [3]

## 2.3 The characteristics of voltage sags

Engineers and researchers discuss the term "voltage sag" based on voltage RMS value and its duration, but neglected some important characteristics of voltage sags. Although this point of view is generally correct for some basic electronic devices, such as personal computers and consumer products, in which rectifiers are used at the primary stage to convert the AC voltage to the DC voltage, only the energy level of the AC voltage is the main concern [24-32]. For some sensitive equipment, the phase shift of voltage sags and the waveform distortion of voltage sags can be critical factors which affect the normal operation of equipment. In order to minimize the effects on sensitive equipment, the characteristics of voltage sags should also be analyzed and clarified for the design of voltage sag compensators. This section will study the factors of voltage sags affecting the sensitive equipment.

### 2.3.1 Sag magnitude and duration

Fig. 2.6 points out some examples of voltage-sag sensitivity curves from McGranaghan's research [12]. The area below the sensitivity curve is the problematic operating region. The Computer Business Equipment Manufacturers Association (CBEMA) curve in ***Appendix A*** shows the limit line of the standard. It defines the power quality requirement for a group of sensitive equipment, like motor contactors and electromechanical relays, high-intensity discharge (HID) lamps, adjustable speed motor drives (ASD), and programmable logic controllers (PLC). The area under the upper bound but above the lower bound is the allowable operating area. The lower bound is specifically for protection against voltage sags.

From the results in Fig. 2.6, if the voltage sag period is one cycle (or more) with 0% of nominal voltage, the operation of contactors will have problems. The operation of contactors will not be affected by any voltage sag if the voltage does not fall below 50% of nominal voltage.

ASD can survive a 2~3 cycles of voltage sag, no matter how serious the voltage sag is. However, the ASD requires ~90% of nominal voltage to maintain a normal operation under steady-state condition.

It is established that without the help of a voltage compensation device, the ASD will be unable to meet the CBEMA requirement. For example, at the point marked with an "x" in Fig. 2.6, when the voltage sag is at 70% of the nominal voltage and lasting for 6 cycles, the ASD will be stopped.

Equally, the contactor fails to meet the CBEMA requirement in the small triangular area formed by the CBEMA curve and the knee of the contactor characteristic.

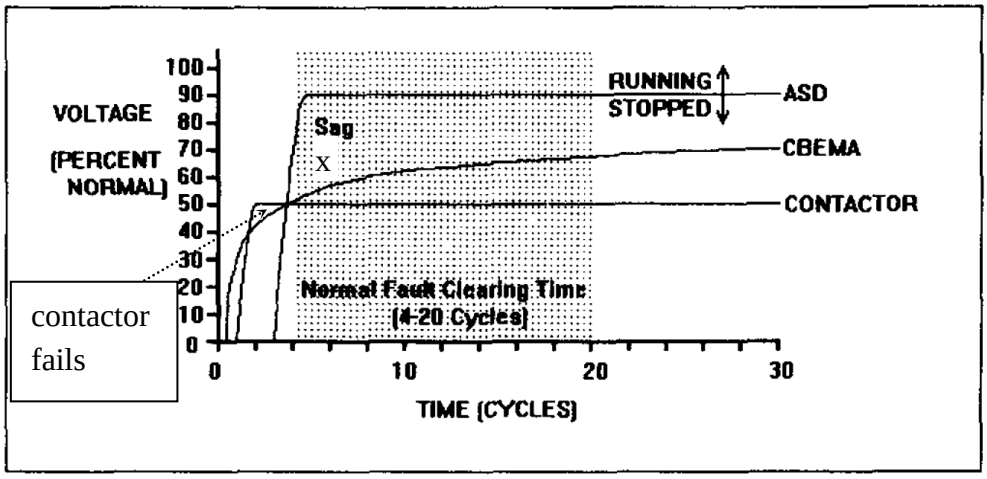



Fig. 2.6 The range of equipment sensitivity to voltage sags [12]

### 2.3.2 Phase shift on voltage sag

The importance of phase shift on voltage sag is discussed in [22]. The term "post-sag phase shift" is defined as the phase shift of the voltage after the sag duration, comparing with the original phase, as indicated in Fig. 2.7. The term "during-sag phase shift" is defined as the phase shift during the voltage sag. According to research findings in [22, 24, 25] post-sag phase shift is just around 1-2% of phase shift, which has only a small influence on sensitive equipment. Nevertheless, the effect of during-sag phase shift can significantly disturb the system operation.

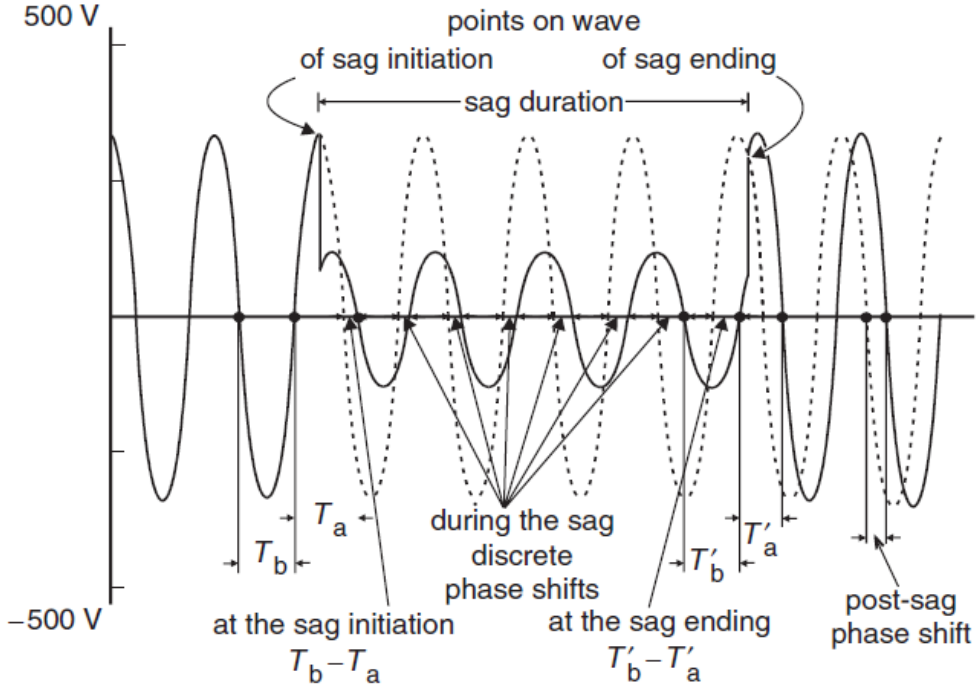



Fig. 2.7 Simulated voltage sag showing discrete values of the during sag phase shift and post-sag phase shift [22]

Research results [25] on the influence of during-sag phase shift for sensitive AC coil contactors are shown in Fig. 2.8 and Fig. 2.9. These results are recorded for $0^o$ sag-initiation and $90^o$ sag-initiation respectively.

It should be interesting to note that in Fig. 2.8 (for $0^o$ sag-initiation) the

worse-case voltage sag depth is not 0% (0V), but is about 30%. It is found that if the sag initiates at $0^o$, the acceptable margin for the contactor is quite large. The contactor can accept up to 30ms sag time and 50% sag depth. With $0^o$ sag-initiation, the during-sag phase shift has only a small influence on the contactor.

By contrast, when the sag initiates at $90^o$, as shown in Fig. 2.9, the contactors are highly sensitive. There is only about a 4ms margin for the contactor without the risk malfunction.

Fig. 2.8 and Fig. 2.9 indicate that in order to ensure the contactor can operate without tripping, the response time of the voltage sag compensator or corrector must be less than 4ms.

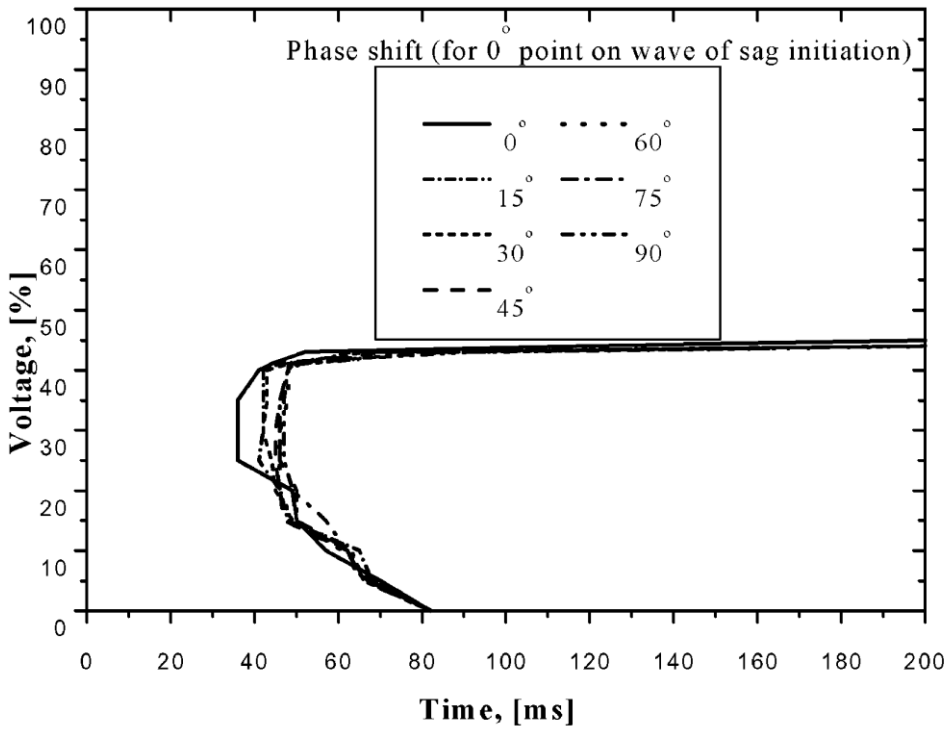



Fig. 2.8 Influence of during-sag phase shift for sensitive contactors ($0^o$ sag-initiation) [25]

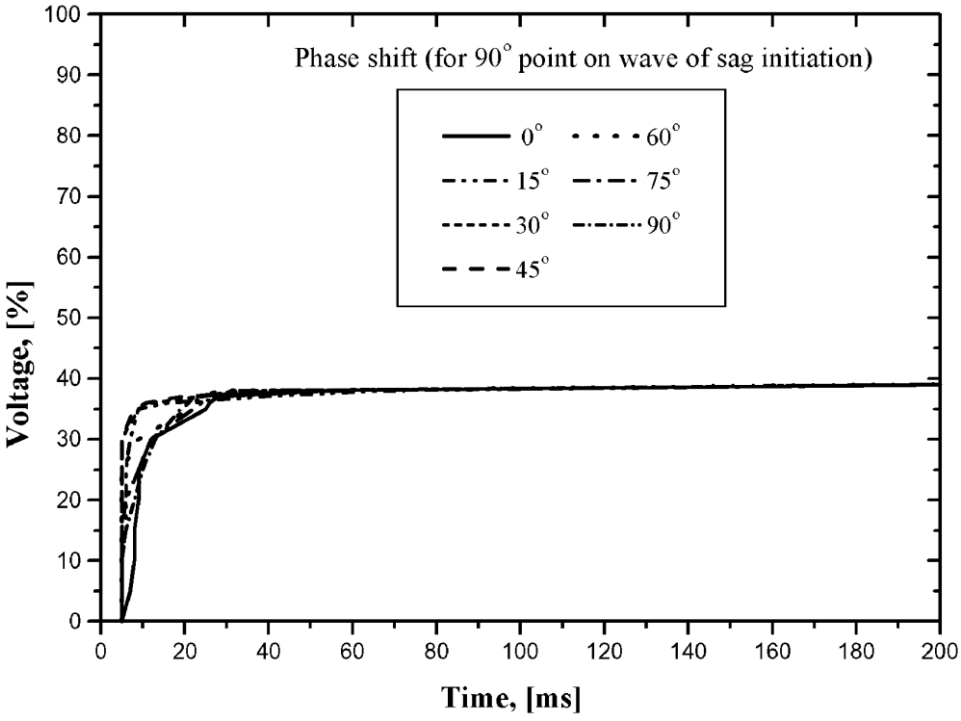



Fig. 2.9 Influence of during-sag phase shift for sensitive contactors (90 $^{o}$ sag-initiation ) [25]

### 2.3.3 Sag-initiation point

Since voltage sags are unpredictable events, they can occur at any phase angle (in addition to the $0^{o}$ and $90^{o}$ examples shown in Fig. 2.8 and Fig. 2.9). A detailed plot of the contactor sensitivity for different sag-initiation points (assuming no during-sag phase shift) is shown in Fig. 2.10. Even without any during-sag phase shift in the waveform, the contactors have vastly different responses to different sag-initiation points. From Fig. 2.10, the worst case for 0% sag is around 4ms at $90^{o}$. The worst case for 30V sag is around 5ms to 6ms at $60^{o}$ sag-initiation.

Fig. 2.10 shows a voltage compensator (or corrector) whose response time is less than 4ms; then the contactor will be able to operate safely.

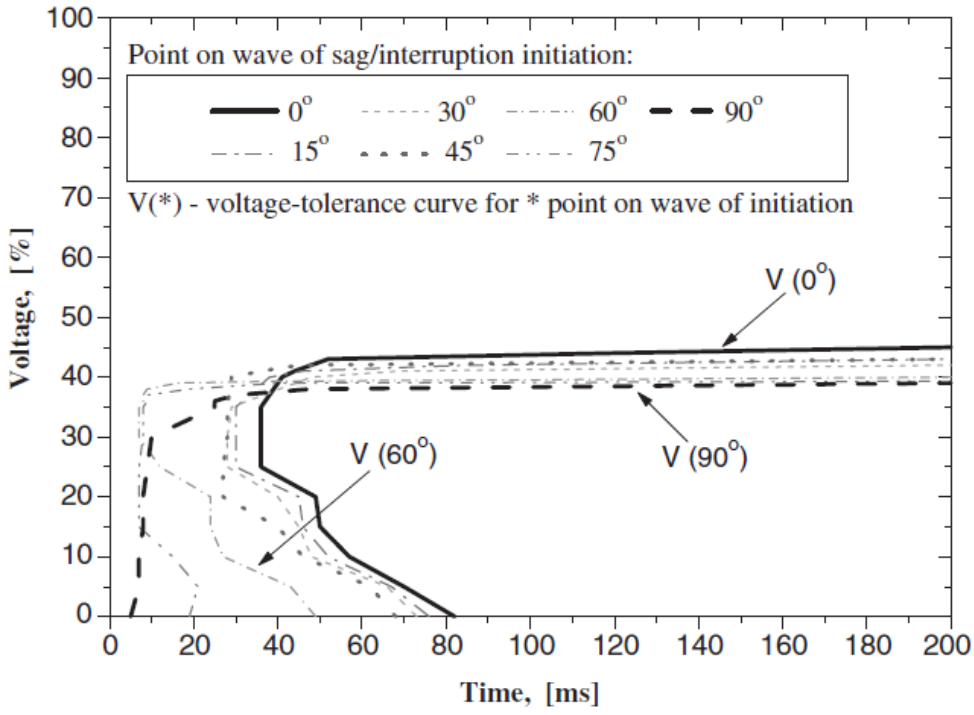



Fig. 2.10 Influence of sag-initiation point on contactor sensitivity (assuming no phase shift) [25]

## 2.4 Practical solutions on immunity of voltage sags

As discussed in the previous section, different equipment could have different responses to the same voltage sag. The magnitude, duration, phase shift, and the point on wave of the voltage sag also are factors affecting the equipment response. There were different approaches [33-40] to solve the voltage sag problem. In this section, the existing practical solutions on the voltage sag immunity in the industry will be evaluated.

### 2.4.1 Switching mode power supply

There are AC or DC devices in industrial plants. If the devices are designed to operate with regulated DC, a switching mode power supply (SMPS) with wide universal input range (85Vac~277Vac) could be the solution for the voltage sag. While a short duration of the voltage sag in AC input induces a spiky current in the SMPS, the output regulated DC voltage can be maintained [41]. The basic structure of a universal input SMPS is shown in Fig. 2.11. The input AC is first pre-rectified to a pulsating DC and then boosted up by the power factor correction (PFC) circuit to around 380V~400V. To maintain a longer operating time for critical load, the output filtering capacitors of the PFC circuit are designed to act as energy storage.

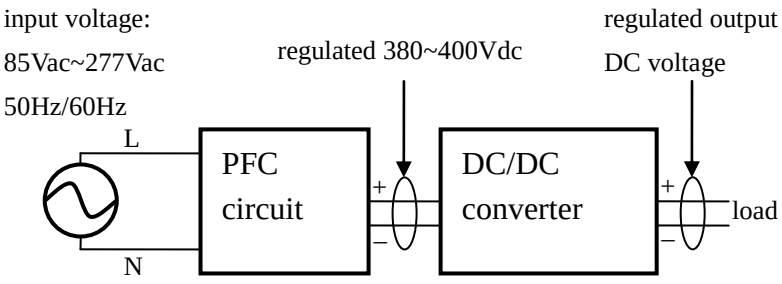



Fig. 2.11 Basic structure of SMPS with universal input

### 2.4.2 Uninterruptible power supplies

Nowadays, the measures of using SMPS to store the energy in DC format are practical solutions for many DC input equipment, which are already applied in many industrial plants. However, despite its simplicity and ease of installation, it cannot solve the voltage sag problems in applications where AC power supplies are required.

Uninterruptible power supply (UPS) is commonly used to solve voltage sag problems for AC loads like computers. There are two basic structures of UPS. Fig. 2.12 is an offline/standby UPS block diagram. Under nominal AC voltage, the AC mains directly supply power to output load through a high power switch. The battery is being charged at the same time. During a voltage sag period, the output voltage will be supplied by an inverter using battery as the energy source, as shown in Fig. 2.13.

Fig. 2.14 shows an online UPS, which is also called a double conversion UPS. The online UPS continuously converts the AC mains to DC and then connects DC to the AC output. It is a perfect device to support the output voltage of equipment without voltage sag.

However, UPS is not a suitable solution for many applications because of the following reasons:

1) UPS requires a battery. The acid, lead, and other particles from a battery are harmful to the operating environment. The maintenance of the battery being used and the disposal of the expired batteries could also induce many problems.
2) The output of a low-cost UPS is often a modified sine-wave voltage, as shown in Fig. 2.15. The modified sine-wave voltage waveform is undesirable for sensitive equipment operate only with sine-wave AC voltage.
3) Normally the low-cost UPS would not allow inductive loads.
4) The delay in offline UPS’s response (delay in detecting a voltage sag plus delay in transferring the load to the output of the UPS) of the low-cost UPS is long. This may cause sensitive loads such as programmable logic controllers, AC contactors, and computer numerical control units in the load to malfunction.

5) There is continuous power wastage in an online UPS. The efficiency of a high cost online UPS is around 92% [42].

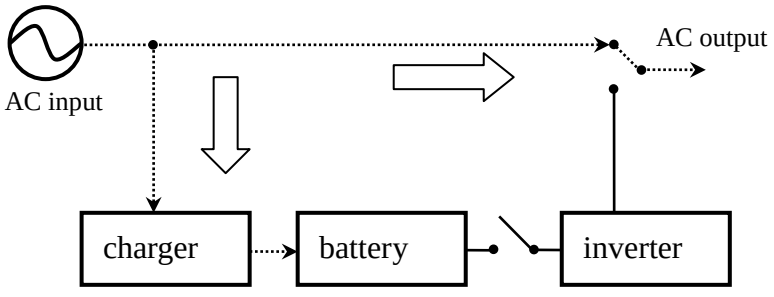



Fig. 2.12 Block diagram of offline/standby UPS running under normal AC power input

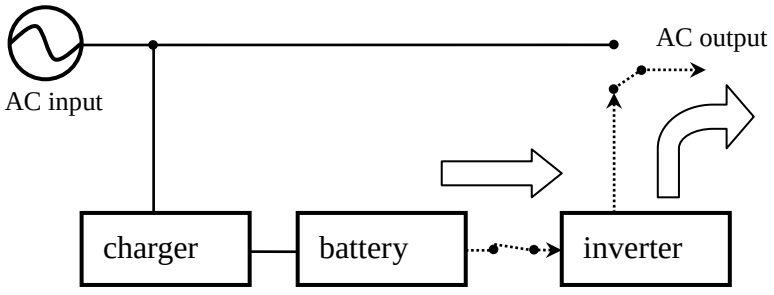



Fig. 2.13 Block diagram of offline/standby UPS running during voltage sag period

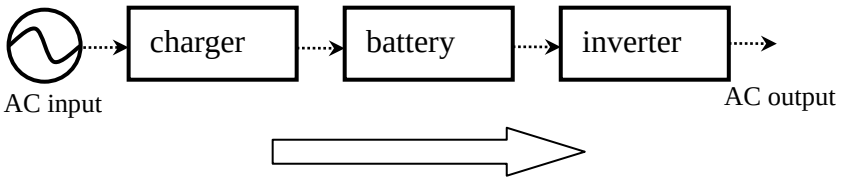



Fig. 2.14 Block diagram of online UPS (double conversion)

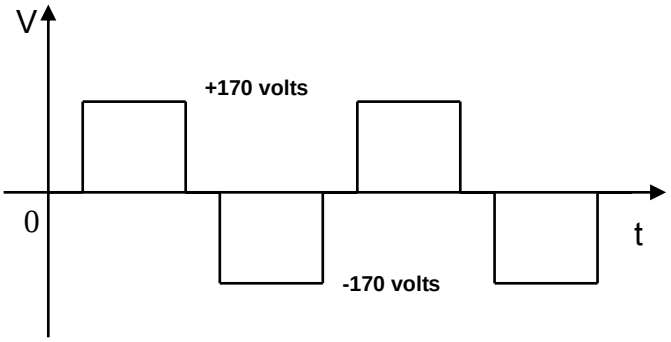



Fig. 2.15 Voltage waveform of modified sine-wave

### 2.4.3 Ferro-resonant transformer

Ferro-resonant transformer, also called constant voltage transformer (CVT), is a special type of laminated low frequency isolation transformer, which can maintain a regulated AC output voltage, provided that the AC input voltage has a limited variation. Fig. 2.16 shows the basic structure of ferro-resonant transformer [43].

Ferro-resonant transformer consists of a primary winding, two secondary windings, and a resonant capacitor. When the primary line voltage increases, the secondary voltage increases according to its winding turn ratio. If the voltage increases over the preset value, the effect of resonance at the secondary winding and the capacitor will increase the secondary flux density. It causes saturation of that a portion of the transformer core. This magnetic design provides a path for the

primary flux to return to the primary winding and without coupling to the secondary. In contrast, the secondary flux can couple to the secondary winding. As a result, the resonant LC circuit can provide energy backup for the output voltage for a short duration, if there is voltage sag in primary line AC input.

This transformer based solution is easy to implement into the system by connecting between AC mains and the equipment. There are no maintenance problems on replacing the batteries regulatory. The transformer also provides isolation between input and output terminals which advance for safety and special separation purposes. The cost of this transformer is lower than UPS from the point of view of maintenances and setup charges.

Despite its simplicity, the transformer is quite sensitive to temperature change. The temperature coefficient affects the output voltage level accuracy and reliability. The phase of the output voltage is following the input source, so the transformer cannot immunize the sag from phase shift. If the magnetic field emission from the transformer would interfere with the operation of the equipment; some shielding measure may be required for sensitive components. AC to AC conversion is a low efficient process which is wasting power during operating. Furthermore, the power rating and the size of the transformer are custom designed for the specified loading for different immunity requirements. Hence, flexibility and compatibility of the transformer are low. The load regulation is not good, as it is the inherent internal regulation of the transformer. Referring to Table 1, the voltage tolerance of +3 to -6% may not be suitable for some equipment. The high inrush current in some equipment (e.g. motor driver) can easily cause the input voltage to collapse.

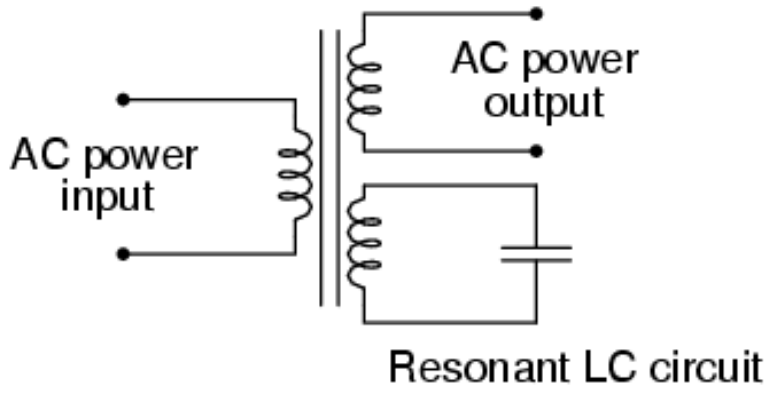



Fig. 2.16 Basic structure of ferro-resonant transformer [43]

Table 1 Allowable voltage sag versus transformer loading for ferro-resonant transformers [43]

| Amount of Load | Minimum Input Voltage[a] |
|---|---|
| 1/4 of rating | 36 V (30% of 120 V) |
| 1/2 of rating | 55 V (46% of 120 V) |
| Full loaded | 85 V (71% of 120 V) |
| 150% of rating (overloaded)[b] | Voltage collapses, even at full input |

[a]If the input voltage is above the minimum input voltage, the output voltage will remain in the range of +3 to -6% of normal value. These transformers are also available with 480-V input.

[b]Inrush current greater than 150% rating will cause the voltage to collapse. Inductive loads such as contactors require special consideration to ensure that the transformer has adequate capacity to handle current inrush requirements.

### 2.4.4 Coil hold-in device

Another one of the solutions of mitigating voltage sag problems is using the coil hold-in device, which already exists on the market. The coil hold-in device [44] is individually connected between the AC mains and contactors. The key function of the device is to keep the relay or contactor operation without chatter

during the input voltage drop. Coil hold-in device is a battery-less device designed to immunize the voltage sags, which has the benefit of reducing maintenance costs. However, the voltage cannot drop to around 25% of nominal voltage, otherwise the device still drop out. The sag protection range is shown in Fig. 2.17. Coil hold-in device is a low cost solution to solve the voltage sag problems at relays or contactors. It should be noted that the coil hold-in device only works well with AC contactors or relays to immunize the voltage sags.

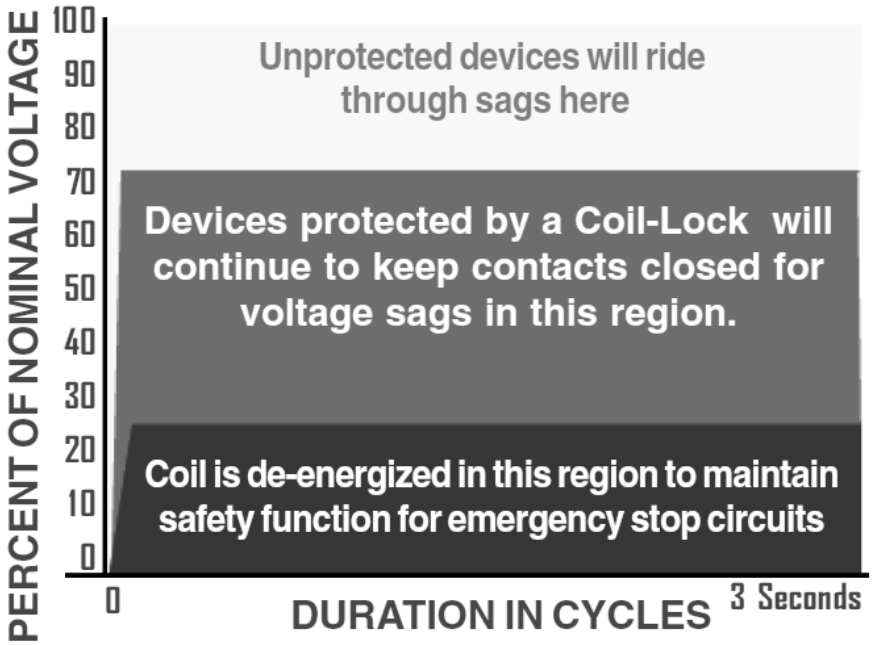



Fig. 2.17 Typical unprotected versus PQSI coil-lock protected devices voltage sag protection performance [44]

### 2.4.5 Dynamic voltage restorer

Dynamic voltage restorer (DVR) [45-46], as shown in Fig. 2.18, consists of energy storage, a controller, a detection circuit and a transformer. This device injects a controllable dynamic voltage to the AC mains for voltage compensation. The dynamic voltage is determined by the voltage difference between the input and the output voltage of the device. The dynamic voltage is injected to AC mains by using transformer coupling. The advantages and disadvantages of DVC are listed below.

The advantages of DVR:

1) If Vdc is provided by battery, then battery maintenance will be an issue. If Vdc is provided by capacitors, then the time for voltage support is limited.
2) The topology is able to support voltage sag drop to 0% of nominal voltage.
3) The response time to compensate voltage sag is swift.
4) The required sag ride-through time can be extended by an energy storage bank capacitance.
5) Power rating of protected equipment depends on the energy storage bank capacitance, power rating of the series transformer and the inverter rating in DVR.

The disadvantages of DVR:

1) Detection method of the voltage sag may be based on the RMS value of the input voltage.
2) Some phase shift type voltage sag still create problems on many sensitive loads.
3) DVR cannot operate when there is a temporarily open circuit at the input terminal.
4) The series transformer provides power loss during operating without the voltage sag.
5) DVR may not provide smooth sine wave at the output during the voltage sag.

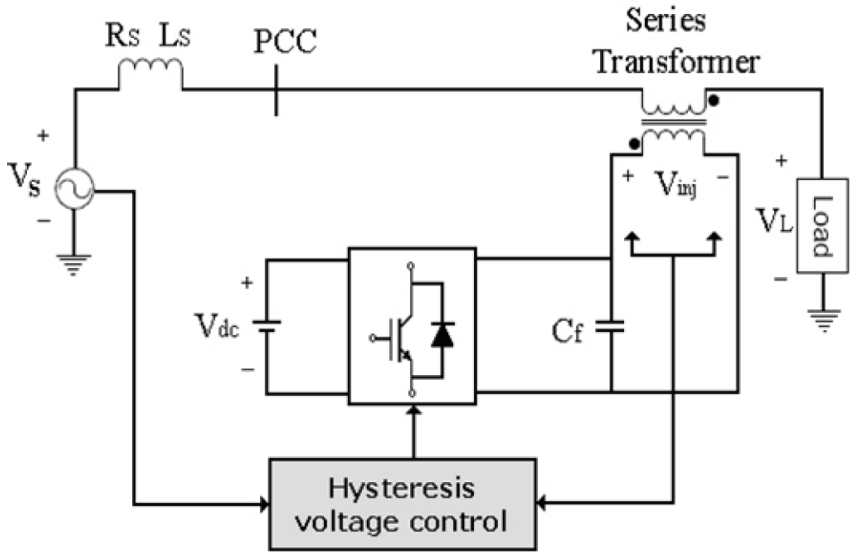



Fig. 2.18 Block diagram of dynamic voltage restorer

## 2.4.6 Dynamic sag corrector

Fig. 2.19 demonstrates the block diagram of dynamic sag corrector (DSC) [47-48]; DSC reported by [48] is also called voltage sag compensator in this thesis. It is a device that compensates the voltage sag by directly injecting voltage to the original input voltage. It stores energy and regenerates AC voltage to output when the voltage sag occurs at the AC mains. It consists of a capacitor bank, two fast response switches and an AC regenerator. The topology shown is a series type voltage sag compensator, and a detailed operating principle of this compensator will be discussed in chapter 4.

The advantages of DSC:

1) There are not any maintenance problems on batteries replacement.
2) The topology is able to support voltage sag drop to 0% of nominal voltage.
3) The response time to compensate voltage sag is swift.
4) The required sag ride-through time can be extended by increasing energy storage bank capacitance.

5) Power rating of protected equipment depends on energy storage bank's capacitance, power rating of capacitance, current rating of static switch, and inverter rating in DSC.

The disadvantages of DSC:

1) The DSC cannot operate when there is a temporarily open circuit at the input terminal.
2) There is power loss in the static switch all the time.
3) The model of DSC with pure sine-wave output cannot support voltage sag down to 0%. Only the model of DSC with modified sine-wave output can support voltage sag down to 0%.

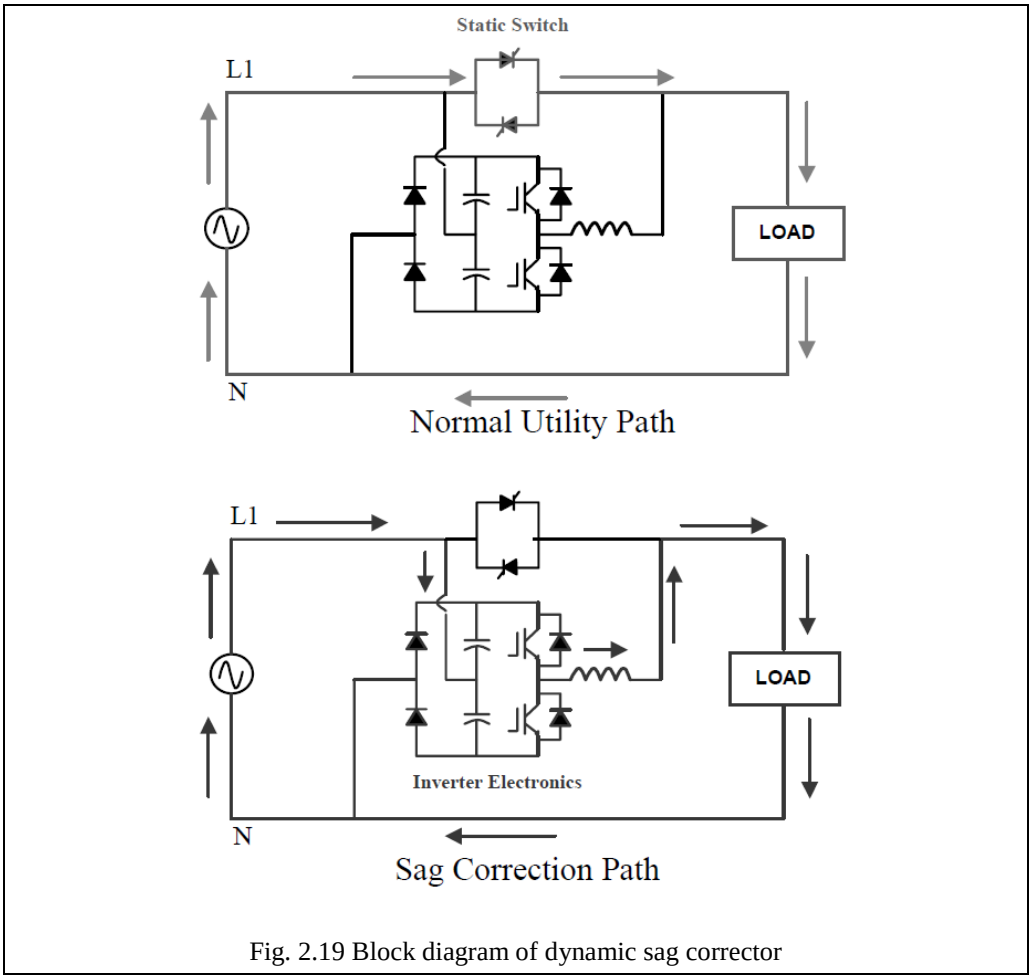



Fig. 2.19 Block diagram of dynamic sag corrector

## 2.5 The requirements of standard SEMI F47

SEMI F47 [16, 18] is a popular standard for the semiconductor industry. The new design of equipment should satisfy the requirement of SEMI F47, which provides an appropriate platform for immunity the voltage sag. This standard is to define the voltage sag immunity required for semiconductor processing, metrology, and automated test equipment, while striking a balance between the voltage sag immunity and the increased equipment cost.

The specification is focusing on susceptibility of the voltage sags on the semiconductor processing equipment, their subsystems, and components. They are listed as follows:

(a) The primary focus of SEMI F47 is on semiconductor processing equipment:

1) Etch equipment(Dry & Wet)
2) Film deposition equipment (CVD & PVD)
3) Thermal equipment
4) Surface prep and clean equipment
5) Photolithography equipment (Scanner, Stepper & Tracks)
6) Ion implant equipment
7) Metrology equipment
8) Automated test equipment
9) Chemical mechanical polishing / Planarization

(b) The secondary focus of SEMI F47 is subsystems or components:

1) Power supplies
2) Radio frequency generators and matching networks
3) Ultrasonic generators
4) Computers and communication systems
5) Robots and factory interfaces
6) AC contactor coil and AC relay coils
7) Chillers and cryo pumps

Table 2, shows the specification of SEMI F47-0706 Standard. In the first column of the table, the sag depth is the percentage of the voltage remaining in the AC mains. For example, a sag depth of 80% for 120Vac means that the voltage is reduced to 96Vac. If the percentage of sag depth is low, the load will be seriously affected. The second to fourth columns show the period of time or cycles of the voltage sag. The longer the time of the voltage sag; the greater is the probability of a fault occurring. This standard is constructed by statistics on the voltage sags affecting the sensitive loading. Equipment meeting this standard should be able to ride through most of the voltage sags for practical applications. However, special cases like total power down are not included in this standard; these cases cannot be dealt with easily at a low cost.

SEMI F47-0706 requirements can also be plotted as shown in Fig. 2.20. The vertical axis is the percentage of equipment nominal voltage; the horizontal axis is the duration of the voltage sag in seconds.

Table 2 Specification of SEMI F47-0706 standard

| **sag depth*** | **duration at 50Hz** | **duration at 60Hz** | **time** |
|---|---|---|---|
| 50% | 10 cycles | 12 cycles | 0.2 second |
| 70% | 25 cycles | 30 cycles | 0.5 second |
| 80% | 50 cycles | 60 cycles | 1 second |

*Sag depth is expressed in percent of remaining nominal voltage. For example, a sag depth of 80% for 120V AC means that the voltage is reduced to 96V.

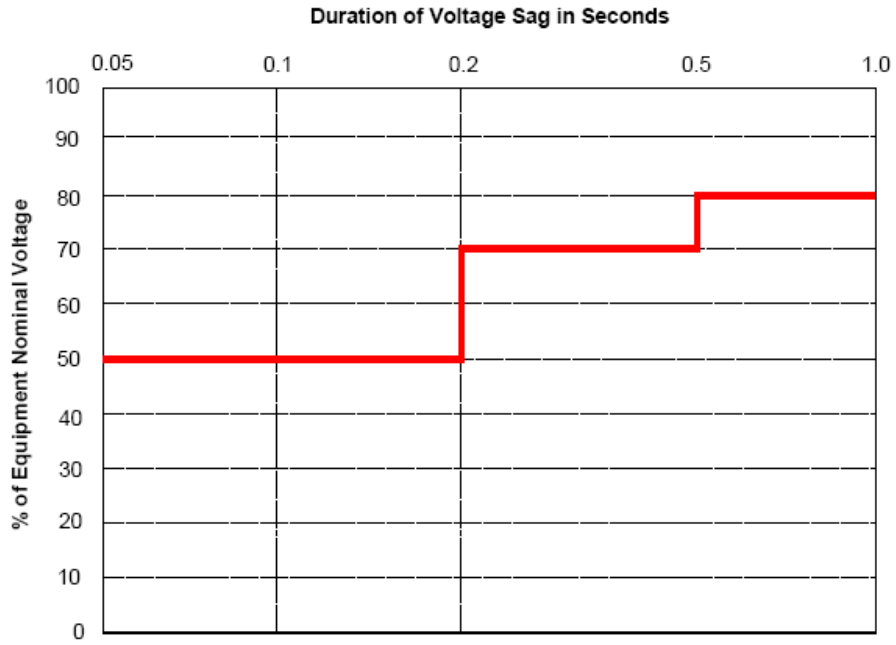



Fig. 2.20 SEMI F47 standard requirement

In the specification, it is important to note that the equipment could not immune to "ALL Real-World Voltage Sags". Although an additional cost is spent on the equipment to meet the requirement of SEMI F47, there is still no guarantee preventing faults during the voltage sag. So as to earn the benefits from this specification, the end customers and suppliers of semiconductor equipment should have clear understanding of their equipment and applications.

Hence, the specification also mentions the "preferred voltage sag immunity solutions" for semiconductor processing equipment and materials. Use of on-board battery backup system of UPS is discouraged because maintenance-free solution is preferred. Another suggestion is, "do not add voltage sag correction to an entire semiconductor processing equipment, but applying voltage sag correction to subsystems or components of processing equipment are acceptable".

Moreover, engineers should pay particular attention to the transient currents during and after sags. During sag, current flow at the input wire is higher than nominal rating, because the load draws the same power at a low input voltage comparing with normal input line. Immediately after voltage sag, the input

capacitors need to be recharged back to their nominal level, resulting in an inrush current for the AC mains. Engineers should be conscious of these sudden current changes to avoid incorrect triggering of protection devices.

## 2.6 Suggestions to minimize the economic loss in industry

As mentioned before, the voltage sag is a crucial concern for semiconductor manufacturers because the resulting economic loss could be colossal. Though the voltage sags are unpredictable, this section will put forth suggestions to industrial plants in order to minimize the loss by voltage sags.

1) The wiring structure should be reasonably arranged to ensure high power quality. Professional wiring structure may reduce the effects of voltage sags due to internal faults. Additionally, clean power can benefit the operation of all equipment [52].
2) Moreover, manufacturers should ensure that all power transmission lines have sufficient current rating and voltage rating. Independent fuses or circuit breakers may be used to isolate the load from the AC mains if the load fails or is short circuited.
3) The power line should be separated into different sectors for different loading groups. For example, one sector for a group of heavy loads (e.g. motor driver), and another for sensitive devices or sensitive controller units. Under this arrangement, the interference among different sectors could be minimized.
4) By using Universal wide range AC-to-DC regulators and equipment with DC input, the influence of voltage sag in the AC mains can be minimized. There are many types of SMPS DC supplies that meet SEMI F47 standard. So, it is a wise choice to select equipment using DC input to resist voltage sag if it is available.
5) System upgrading and replacement of old equipment are possible ways to minimize voltage sag problems, but these methods are costly. Hence, industrial plants should use equipment with SEMI F47 certification for new installation and for replacement of old equipment. Otherwise, they may have to pay more in the future for loses due to voltage sags.
6) Frequent maintenance and periodic checking of the equipment could help reduce the possibility of faults or short circuits, which may cause voltage sags.
7) Voltage sag problems could be alleviated by using protection devices like UPS, CVT, coil hold-in devices, voltage sag compensators and voltage sag restorers

for critical loads[49].

8) Setup power quality workshops and seminars for engineers to learn and discuss the causes and possible solutions of voltage sag problems[50].
9) Install voltage sag recorder in the plant to monitor the voltage sag events and investigate the source of voltage sags professionally [51].

As discussed before, the equipment cannot be designed to be immune from all real-world voltage sags because of the unpredictability. But, users can minimize the loss resulting from voltage sag events, based on their characteristics and methods to reduce their effects. In this respect, the industry may need to pay more attention to upgrade their system in order to improve productivity.

## 2.7 Summary

This chapter investigated the seriousness of the voltage sag in terms of numerical survey results. The data indicated that the probability of voltage sag event is higher in an industrial plant, when compared with a commercial area. The main reason is most likely due to the high power rating of industrial equipment and heavy load switching in industry. The characteristics of the voltage sag are discussed. The effects of sag magnitude, sag duration, during-sag phase shift and sag-initiation point on sensitive devices were briefly outlined.

In order to solve the voltage sag problems, some additional devices are used in the industry. These devices include SMPS, UPS, CVT, coil hold-in devices, DVR, DSC, etc. Each device has its advantages and disadvantages on immunity of the voltage sag. The selection of a suitable device is an important step to protect the equipment under voltage sag. Standard SEMI F47 provides a guideline to the semiconductor industry on semiconductor processing machines. Finally, some solutions were given to industrial plants for minimizing the economic loss in the voltage sag incidents. The next chapter will discuss the operation of voltage sag compensator.

# Chapter 3: Operation theory of voltage sag compensator

## 3.1 Introduction

As discussed previously, the semiconductor industry requires equipment to meet SEMI F47. Existing products on the market may not completely fulfill their needs. UPS could only be operated with battery and has slow response time for voltage sag immunization. The existing voltage sag compensator on the market cannot operate under open circuit or very light load condition. Thus, a new design of voltage sag compensator is required to help ride through voltage sag incidents with less limitation.

In this chapter, firstly, the operation of voltage sag compensator will be described. Secondly, the topologies of series type voltage sag compensator and parallel type voltage compensator are discussed in detail. Finally, the advantages and disadvantages of both types of compensators are analyzed.

## 3.2 Analysis of voltage sag compensator

The voltage sag compensator is an electronic device which is connected between the AC mains and the loading to immunize voltage sag. The input and output of voltage sag compensators are AC voltages with specific amplitude and frequency. The voltage level of the compensator should be the same as that of the existing power network i.e. 110Vac/120Vac for US and Japan, and 220/230Vac for Europe and China. The output frequency of the compensator is depending on the power station requirements i.e. 50Hz or 60Hz.

When the voltage sag compensator is operating under nominal condition, the compensator will store up energy from the AC mains to a set of capacitors as backup. At that moment, there is no interruption to the output load. At the same

time, the compensator is continuously detecting the waveform of the AC mains. Once a voltage sag is detected in the AC mains, the energy stored in the capacitors will be used to regenerate sinusoidal output voltage to drive the output load. If detection response time and switching transfer time is fast enough, the AC supply at the output load will be reasonably clean and stable to let the load to ride through the voltage sag event.

The voltage sag compensator is similar to a sine-wave AC backup power system. The inverter in the sag compensator is activated to provide back-up AC voltage during voltage sag events. Depending on how the inverter is connected between the AC mains and the load, sag compensators can be classified into two types. The inverter is connected in series with the AC mains which is known as the series compensator. The inverter is worked in such a way that when a voltage sag occurs, the inverter will independently supply AC power to the load, which is known as parallel compensator.

## 3.3 Topology of series type voltage sag compensator

A block diagram of a series type voltage sag compensator [53-54] is shown in Fig. 3.1. The series type voltage sag compensator is discussed in previous research [45-48]. Some existing products, DVR and DSC are developed and applied on market. The main idea of this compensator is that the microcomputer controller monitors the AC mains voltage and controls the operations of the inverter to supply output voltage. Referring to Fig. 3.1, when nominal AC mains are supplied to the compensator, capacitors, C1 and C2, will be charged up by a rectifier. The energy is stored in DC status for backup. Simultaneously, AC mains are connected to output load through a switch, SW. Fig. 3.2 shows the current flow direction with a dotted line in the series sag compensator during normal operation. When a voltage sag incident in the AC mains is detected by the microcomputer controller, the inverter starts to generate a backup AC voltage. At the same time, the load is transferred through SW to the output terminal of the inverter. The current flow during the voltage sag incident is shown in Fig. 3.3. Here the inverter is connected in series with the AC mains to provide power to the

load. At the end of the voltage sag incident, the microcomputer controller switches the load back to the AC mains. C1 and C2 are recharged to store up the energy required for the next cycle of voltage compensation. The DC voltage regulator may be used to regulate the high-tension DC voltages supplied to the inverter.

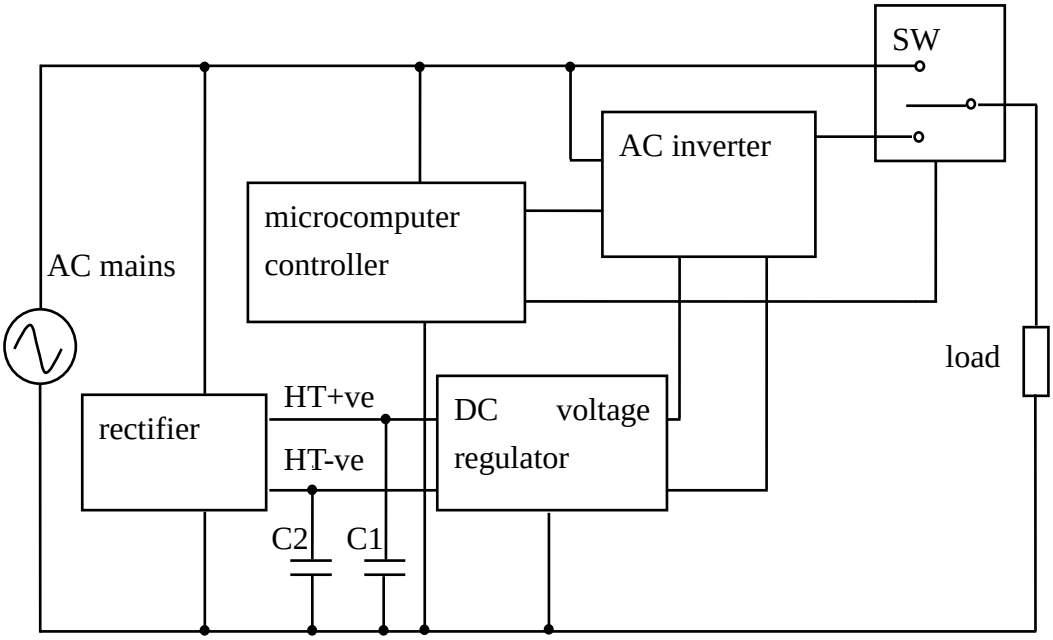



Fig. 3.1 Block diagram of series type voltage sag compensator [53] [54]

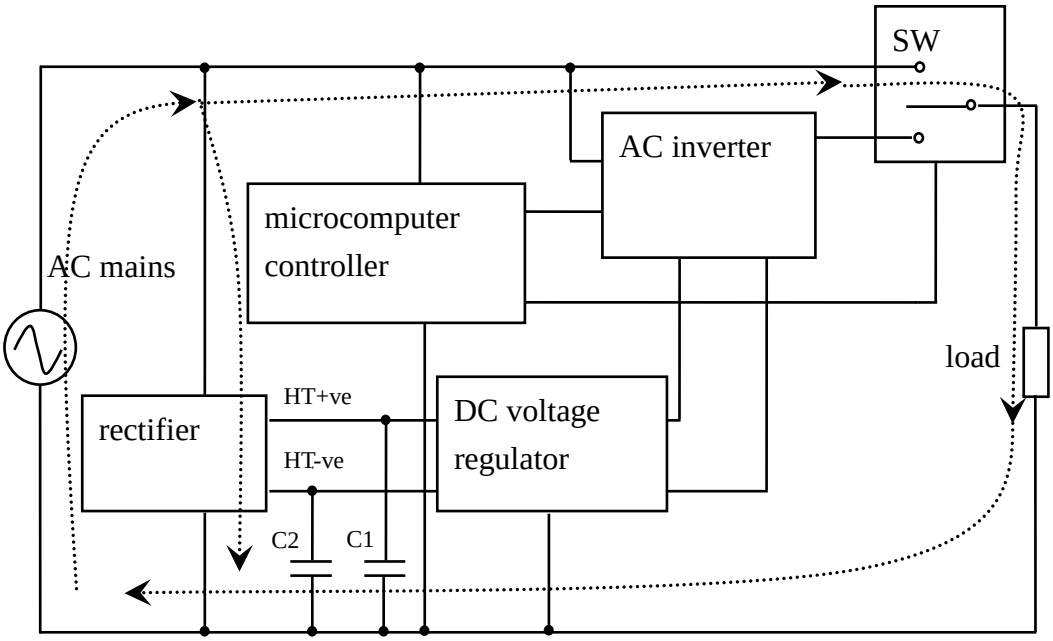



Fig. 3.2 AC current direction of series type voltage sag compensator (during nominal input)

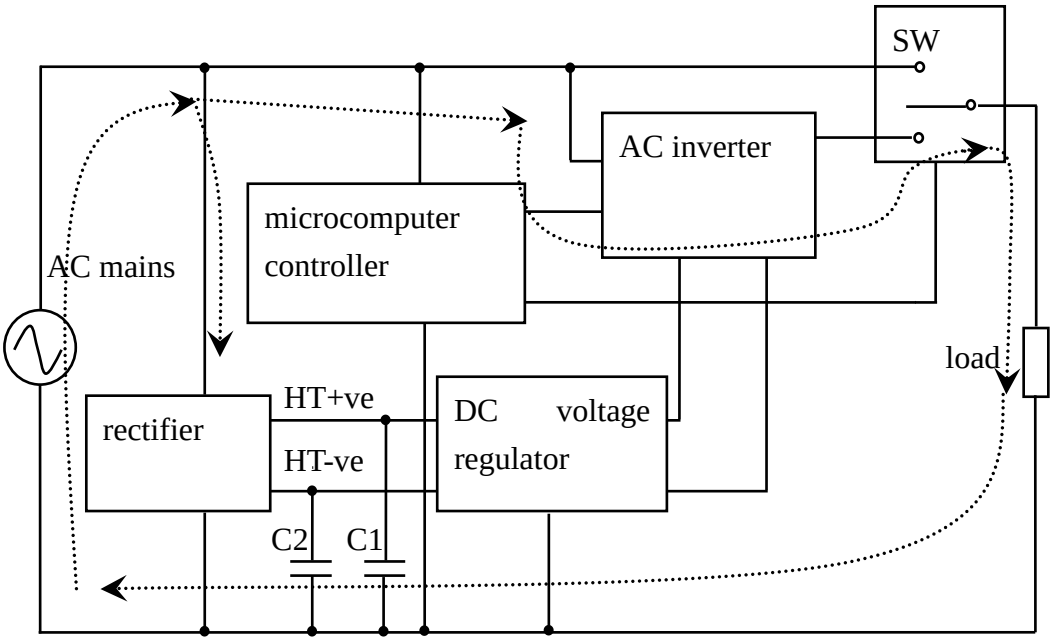



Fig. 3.3 AC current direction of series type voltage sag compensator (during voltage sag)

## 3.4 Topology of parallel type voltage sag compensator

The topology of new parallel type compensator is based on UPS's topology. Referring to section 2.4.2, the offline UPS can supply voltage to load when there is voltage sag. But, batteries and slow voltage sag response time in UPS are two main disadvantages, when it is applied in semiconductor industry for voltage sag compensation. So, the topology of new parallel type compensator is designed, which is based on UPS's topology replacing the batteries by a large capacitor bank for backup purpose. Furthermore, the response time of compensator should be improved to meet semiconductor industry's requirements.

A block diagram of a parallel type compensator [53-54] is displayed in Fig. 3.4. Fig. 3.5 shows the current flow direction with dotted line during normal operation. The operation of the parallel type voltage sag compensator is similar to that of the series type compensator shown in

Fig. 3.1, except that during the voltage compensation period the load is now disconnected from the AC mains and connected to the output of the inverter through the transfer switch, SW, as shown in Fig. 3.6.

Fig. 3.6 indicates the AC inverter alone provides all the power required by the load over the entire compensation period during the voltage sag incident. This arrangement enables the parallel type voltage sag compensator to deliver a smooth sine-wave output voltage over the entire compensation period, which is unaffected by the transients in the AC mains during the voltage sag incident.

The parallel type voltage sag compensator also has the advantage of being able to tolerate open-circuit faults in the AC mains during the voltage sag incident. If there is a transient bad contact in the AC mains circuit, the series type compensator will fail to provide continuous power to the load.

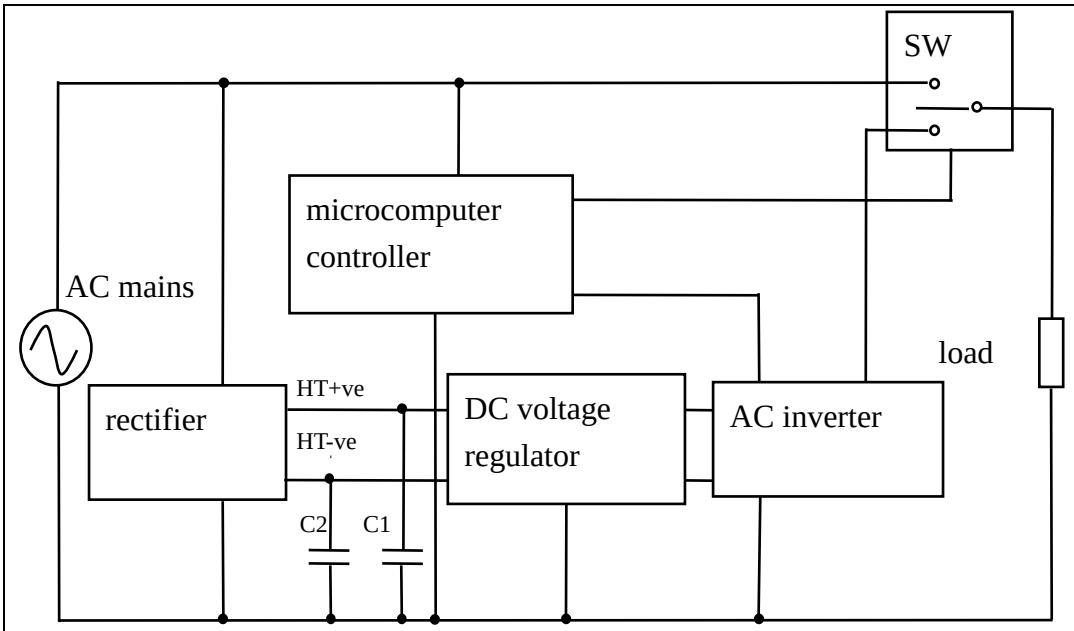



Fig. 3.4 Block diagram of parallel type voltage sag compensator [53] [54]

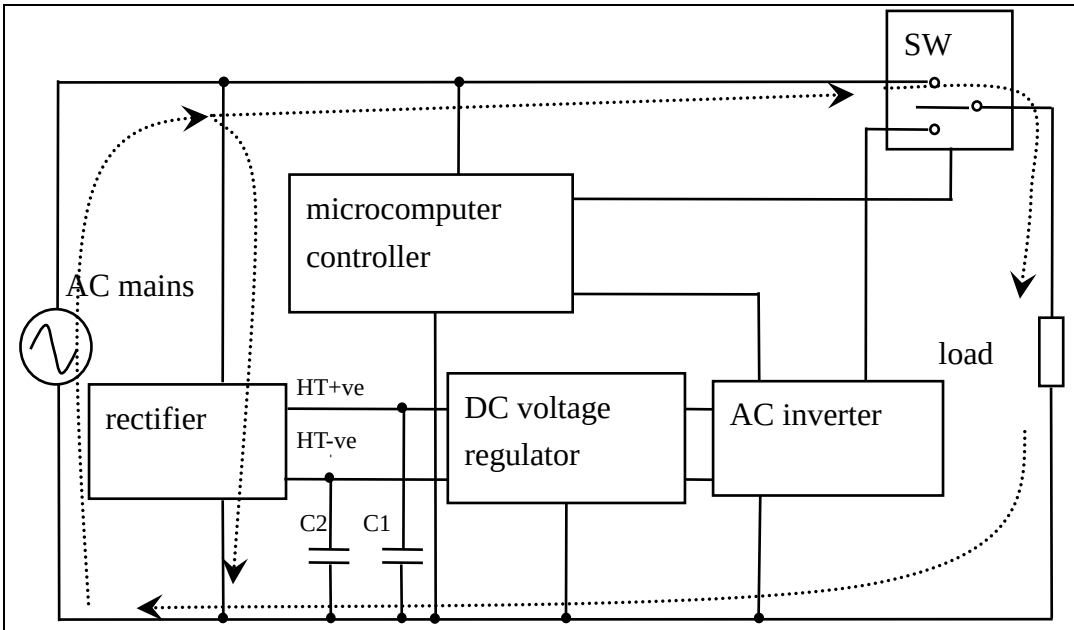



Fig. 3.5 AC current direction of parallel type voltage sag compensator (during nominal input)

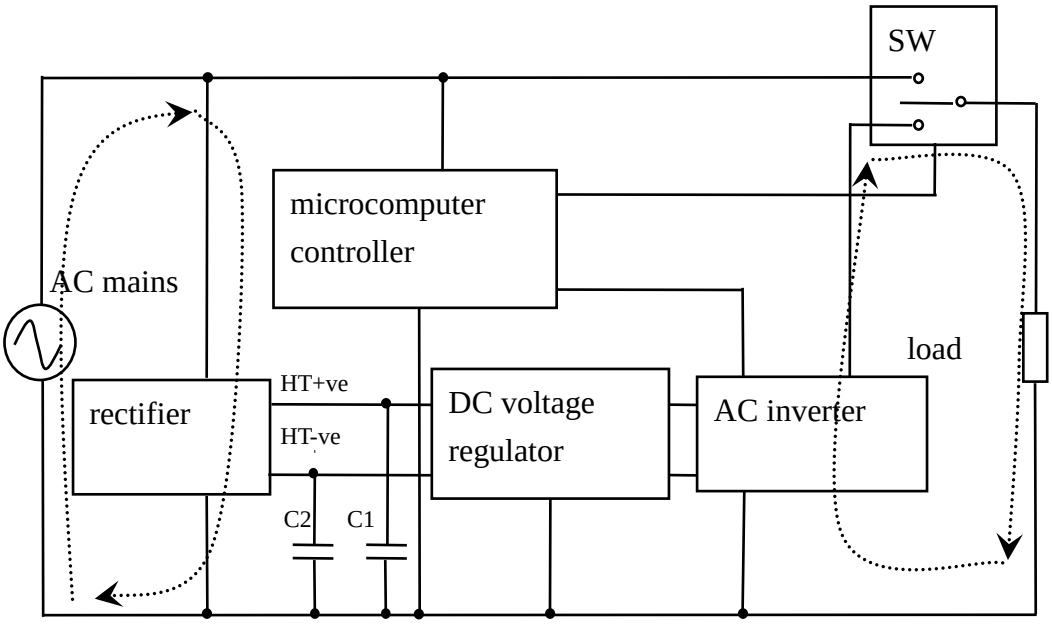



Fig. 3.6 AC current direction of parallel type voltage sag compensator (during voltage sag)

## 3.5 Comparison between series type and parallel type compensators

Referring to the topologies of series type and parallel type discussed in section 3.3 and section 3.4, during voltage sag compensation, the AC inverter in a series type compensator assists the AC mains by superimposing the compensation voltage on the AC mains to provide power to the load. The AC inverter in a parallel type compensator has to provide all the power to the load during the voltage sag incident. Thus, sometimes, the AC inverter in the series type compensator will be required to provide less output power comparing with the AC inverter in a parallel type compensator under the AC mains voltage without completely down to zero during the voltage sag incident. However, when the AC mains voltage drops completely to zero, the power required from the AC inverter in either a series type compensator or a parallel type compensator will be equal. Therefore, as far as the worst-case design is concerned, the maximum required power ratings of the AC inverter in either the series type compensator or the parallel type compensator should be the same.

In addition, the compensated voltage level of series type compensator is according to the input sag voltage level, but compensated voltage level is directly generated from inverter in parallel type compensator. Then, the parallel type compensator has less consideration on the original sag voltage level for compensation. Also, some voltage sags, due to phase angle shifting, may make the design on series type compensator more complicated.

It is interesting to note that a functional test can be carried out on an output open-circuited (or very lightly loaded) parallel type compensator by turning the AC mains switch of the compensator to the off position for a short period (for example: one second) and see if the AC output can be maintained during the AC mains switch turn-off period. If the AC output voltage of the compensation can maintain during the turn-off period, the compensator will be functionally normal. The same test cannot be applied to a series type compensator because as soon as

the AC mains switch is turned off (open-circuited), the output voltage of the series type compensator will be interrupted, because current flow of voltage compensation will be blocked when there is open circuit at input. There will be no output voltage at the load. In order to test the operation of a series type compensator, a programmable AC source is required.

## 3.6 Benefits of using new parallel type voltage sag compensator

UPS is widely used in different applications to solve power quality problems. It has a longer compensation time (e.g. >2hours) in comparison with compensation time 0.2~2sec. in parallel type compensator depending on the output load. But, batteries in UPS limit the application to solve voltage sag problems in the semiconductor industry, as high frequency periodic maintenance is required for battery reliability. The parallel type compensator using capacitors as backup storage benefits it to apply in semiconductor industry which can meet the SEMI F47 requirement. The fast response time of the parallel type compensator is also suitable for highly sensitive AC equipment.

Both series type and new parallel type compensators have similar component count. They require the same energy storage for voltage sag and dropped completely to zero for the same load. However, the parallel type compensator can ride through voltage sag in a temporary open circuit without any problems, but the series type compensator will malfunction in this case.

Furthermore, design methodology of the parallel type voltage sag compensator may be easier than that of series type, because the parallel type compensator has less related to the original sag voltage level for compensation. The compensation voltage is independent to input AC mains. In contrast with parallel type compensator, series type compensator always concentrates on the input voltage sag to provide the superimposing voltage compensation. Moreover, due to phase angle shifting, voltage sag, may make trouble to series type compensator.

Dynamic voltage restorer (DVR) [45][46], discussed in section 2.4.5, is a series type compensator, By considering the voltage waveform of DVR as shown in Fig. 3.7, it is observed that the output voltage waveform(Vload) contains many distortions. Because, the compensated voltage is injected into output through an isolated transformer. Impedance and coupling efficiency of the transformer are affecting the output voltage level. The overshoot voltage may also damage the equipment. By contrast, the parallel type compensator can provide relatively smooth waveform to load, because the inverter output is directly connect to load without an isolated transformer.

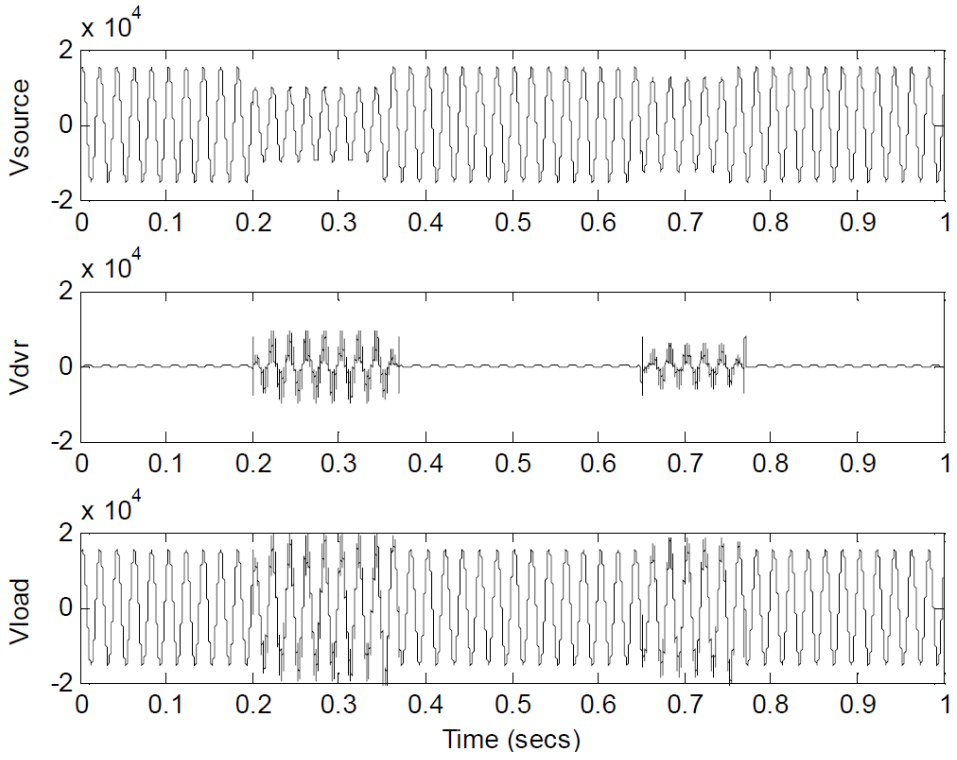



Fig. 3.7 Single phase voltage sag compensation in DVR[46]

Dynamic sag corrector (DSC) [47-48], discussed in section 2.4.6, is another series type compensator, which has a similar circuitry to parallel type compensator. The main difference is that the power switch in series type compensator blocks the original current path, and an inverter superimposes

voltage with the input and outputs to regenerate voltage to load. This arrangement may minimize the time delay on switch transfer, but the compensator cannot be used in open-circuit type voltage sag.

The advantages of parallel type voltage sag compensator:

1) There are not any maintenance problems on battery reliability. The rechargeable capacitor bank is used as energy backup.
2) The topology is able to support voltage sag drop to 0% of nominal voltage.
3) The response time for voltage sag compensation is faster than UPS, which can satisfy semiconductor industry's requirement.
4) The required sag ride-through time can be extended by increasing storage bank capacitance.
5) Power rating of voltage sag compensator can easily be expanded by increasing the energy storage capacitance and the rating of inverter.
6) During sag compensation, output voltage is independent of input AC voltage level and phase angle shifting. This property benefits compensator to ride through different type of voltage sag. Also, compensation voltage with smooth sine wave can be easily supplied by a high quality inverter at the output during the voltage sag incident.
7) The topology allows temporary open circuit at input during compensation.

Disadvantages of parallel type voltage sag compensator:

1) The compensation time is limited to around 2~3 seconds which is relatively short comparing with UPS.
2) The response time for the voltage sag is dominated by switch transferring delay, because, it is required to ensure that the output load is disconnected to input and connected to inverter output before inverter is activated during compensation.

## 3.7 Critical requirements for the compensator design

The power quality requirement of the semiconductor industry is harsher than that of common industry plants. SEMI F47 standard published by the semiconductor industry is, in general, more stringent than the CBEMA standard on the voltage sag immunity. Referring to SEMI F47 standard, mentioned in Section 2.5 in Fig. 2.20, the semiconductor devices should be able to ride through voltage sag of 0% with 0.05 second, but CBEMA standard in ***Appendix A*** only require the device ride through voltage sag of 0% with 0.02 second.

In order to increase the usability of the voltage sag compensator in different countries, the compensator is required to operate under frequency of 50Hz or 60Hz. The voltage sag detector in the compensator should be designed to be capable of detecting not only the RMS value but also the waveform of the AC mains. The detection and control algorithm should enable the compensator to synchronize its operation to either 50Hz or 60Hz AC mains frequency intelligently. The AC mains frequency has +/- 1% variation. The synchronization mechanism should be able to avoid error triggering due to such frequency variations.

The compensator output waveform should be good sinusoidal wave for serving some sensitive equipment that only accept sine-wave AC input voltage for normal operation. Different users should require different voltage sag triggering levels to start the voltage compensation process. Therefore the triggering level should be selectable by the user. It is important for the end user to appropriately preset the voltage sag protection level for any specific applications.

Reliability and safety are important requirement in the design of the voltage sag compensator. The additional voltage sag compensator should not add more trouble to the system under protection.

In addition the voltage sag compensator should be deigned to be easy for functional testing without expensive equipment such as programmable AC voltage source.

## 3.8 Summary

In this chapter, the operation of voltage sag compensator is introduced. The topologies of series type and parallel type voltage sag compensators are analyzed. The main disadvantage of the series type compensator is that it cannot operate when the input connection is opened during the voltage sag period. The required energy-storage capacitance for both compensators is the same for equal output power rating when the voltage sag depth is down to 0V. Finally, the critical requirements of the new design of compensator are described. The next chapter will discuss the design of a 1kVA parallel type voltage sag compensator.

# Chapter 4: Hardware design for voltage sag compensator

## 4.1 Introduction

In this chapter, the hardware design of a 1kVA parallel type voltage sag compensator, based on Fig. 4.1, will be discussed. Although, the voltage sag compensator was discussed based on simulations in many publications, few researchers apply them to hardware circuit. In order to fill this gap, this research includes description of the hardware circuit construction. The compensator is compatible for the AC mains 50Hz/60Hz 120Vac. The hardware part design of the voltage sag compensator is separated into four sections. The first part is the design of the rectifier for energy backup with a set of capacitor banks. The second part is the design of the DC regulator block, which provides power to the AC inverter. The third part is the design of the AC inverter block. The fourth part is the design of the power supply for the microcomputer controller and protection circuitry for the compensator. A summary will be at the end.

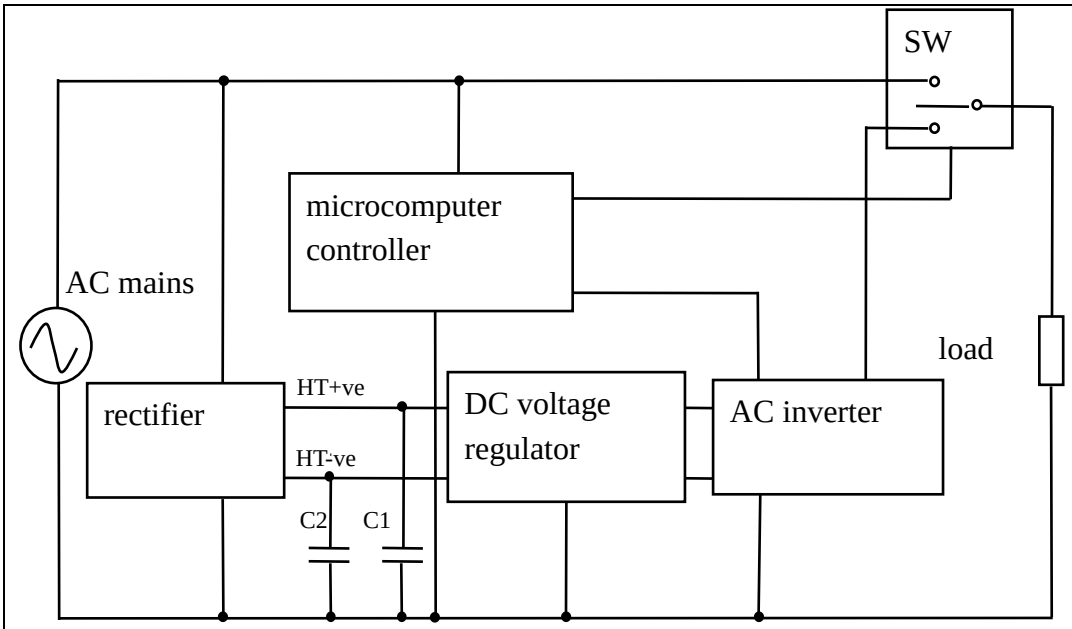



Fig. 4.1 Block diagram of parallel type voltage sag compensator (Fig. 3.4 repeated here for convenience of reader)

## 4.2 Hardware design

The hardware of the voltage sag compensator, as shown in Fig. 4.1, has a structure similar to that of a UPS system, but now a backup capacitor bank is used instead of a battery. The capacitor bank is self-recharged by the compensator itself. The AC inverter operates only during the sag period. The power supply for each circuit is specially arranged to allow the system working under transient condition. The transfer switch between the AC mains input and the AC inverter is an advanced design to provide fast response to the voltage sag.

### 4.2.1 Design of the rectifier block

Referring to Fig. 4.1, when there is no voltage sag in the AC mains, the AC mains will directly supply power to the load through the high power switch, SW. At the same time, in order to provide the positive and the negative power supply voltages to the AC inverter, a voltage doubler circuit is used to charge both the

high side capacitor C1 and the low side capacitor C2 of the capacitor bank. The selection of capacitance for the capacitor bank will be discussed in the next section.

The voltage doubler circuit to be used can be seen in Fig. 4.2. As the input voltage is 120Vac, the DC capacitors C1 and C2 are charged up to 170Vdc. Hence, the AC voltage is rectified to provide the -170Vdc and +170Vdc output voltage. In order to avoid high inrush current during large capacitor charging up, some additional negative temperature coefficient (NTC) thermistors are required to limit input current for protection. The selection of fuse is critical in the design of the compensator. It should be noted that even during the compensation period, the rectifier can continue to provide energy to the AC inverter.

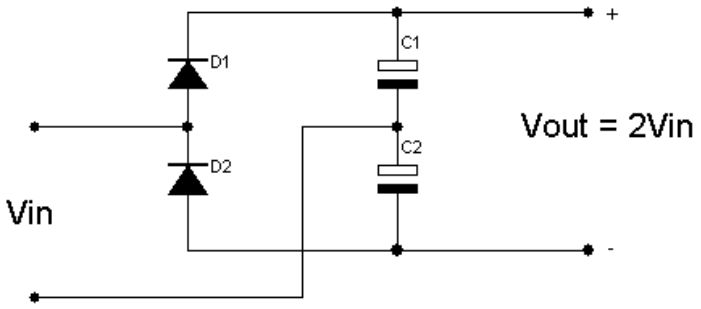



Fig. 4.2 Basic structure of voltage doubler circuit

### 4.2.2 Selection of energy-storage capacitors and design of the DC voltage regulator block

The selection of energy-storage capacitors C1 and C2 is necessary to make the energy storing in the capacitor banks supporting for the AC inverter provided the output power during the voltage sag period, as specified in SEMI F47 standard. In addition, the output voltage of the AC inverter must be reasonably regulated against the drop of the capacitor voltage during the voltage sag incident. This is achieved by two DC to DC boost regulators, which are used to regulate the high-tension DC supply voltages to the AC inverter.

An output voltage envelope during with or without a boost regulator is evaluated in a test as shown in Fig. 4.3. To simulate the output voltage envelope without a boost regulator, at the beginning, input capacitor, $C_{in}$ = 13200uF is full

charged up to ~170V, which simulate the DC level rectified from AC mains. The load(56ohm) is directly connected to the output port and parallel with $C_{out}$ = 2200uF. At t = 0, switch is opened, the output voltage envelope can be recorded as shown in

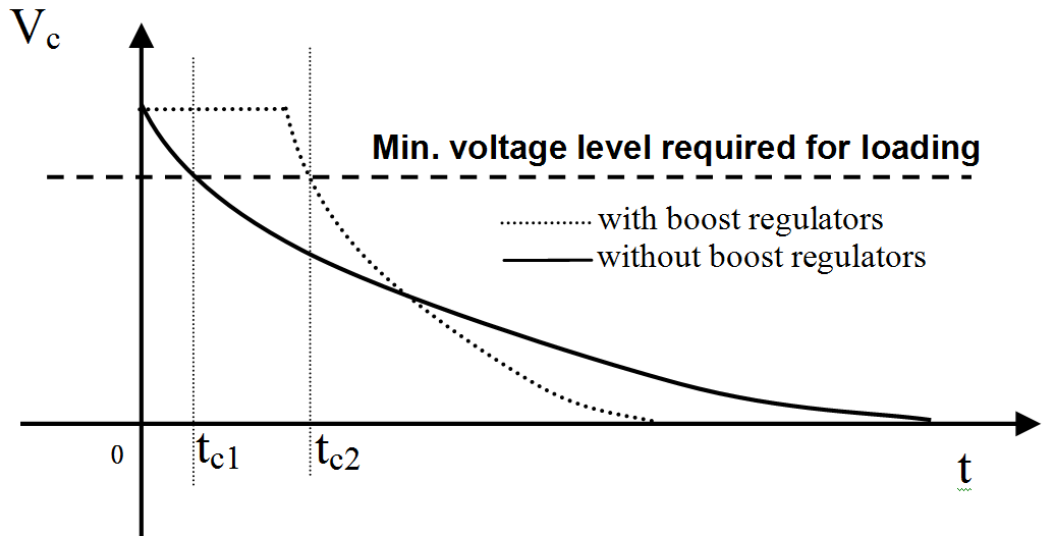



Fig. 4.4 with a solid line. When input supply is disconnected, the output voltage will drop rapidly with the exponential discharge curve.

Similarly, to evaluate the output voltage envelope with boost regulator, $C_{in}$ is full charged up to ~170V. The load is connected to the boost regulator output and parallel with $C_{out}$. At t = 0, switch is opened, the output voltage envelope can be recorded as shown in

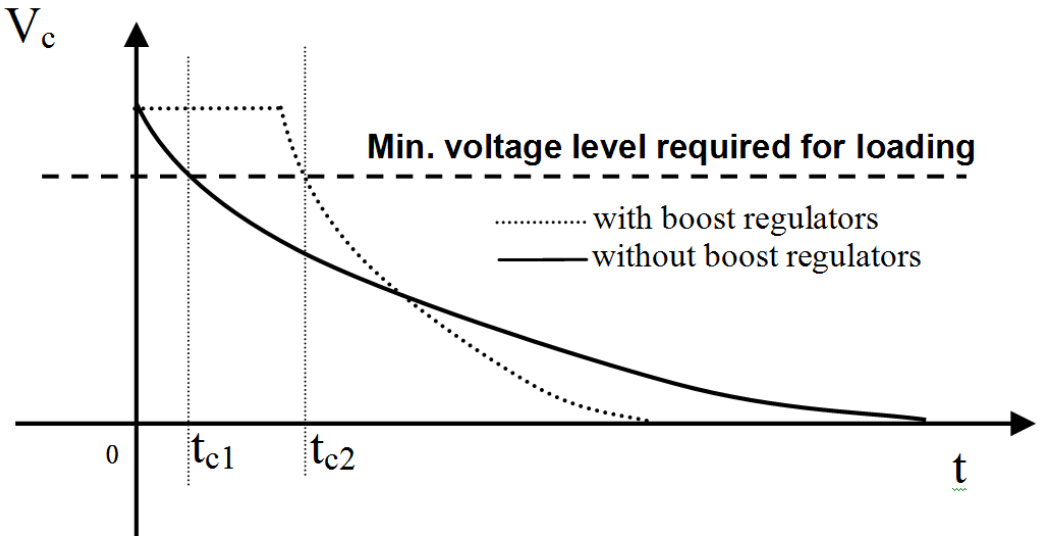



Fig. 4.4 with a dotted line. When input supply is disconnected, the output voltage will be regulated at 170Vdc for a short period, because this boost regulator is designed to operate with minimum input voltage = 50V and output voltage = 170V. Actually, the hold time is depending on the capacitance and the property of the boost regulator.

Referring to the test results in

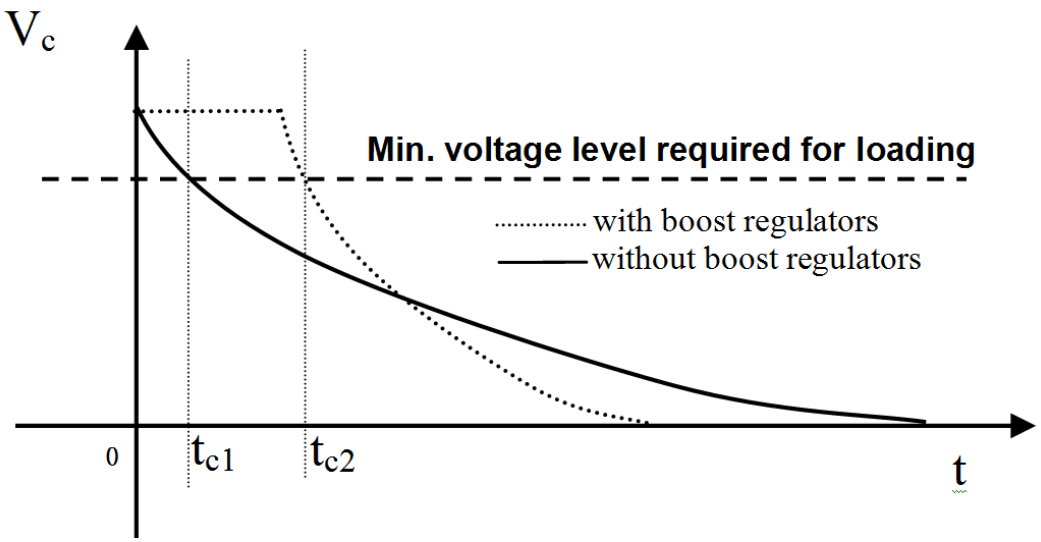



Fig. 4.4, without these DC to DC boost regulators, the high-tension DC voltage available to the AC inverter will drop exponentially when the AC mains

fails (fall to zero). This will result in a similar exponential falling in the envelope of the AC output voltage of the AC inverter. Assume that a minimum level voltage requirement for the load is the dotted line as shown in

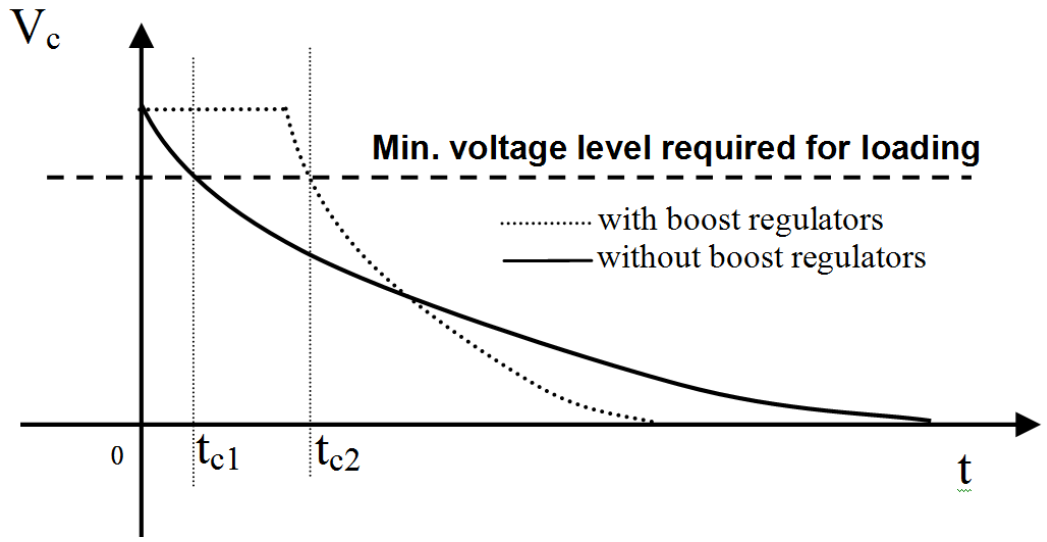



Fig. 4.4. The compensation time $t_{c1}$ without boost regulator will be very short. On the contrary, using an additional DC to DC boost regulators, output voltage can be supplied to the AC inverter with regulation until the input voltage in the energy-storage capacitors falling to a low level(<50V). As a result, the compensation time can be extended to $t_{c2}$ using equal capacitance. The boost regulators guarantee that the energy-storage capacitors C1 and C2 in Fig. 4.2 is much more efficiently used, so as to minimize the capacitance required for a given compensation time $t_{c2}$.

On the other hand, the waveform of the resulting high-tension DC voltage, which is indicative of the envelope of the AC output voltage of the AC inverter, is shown in

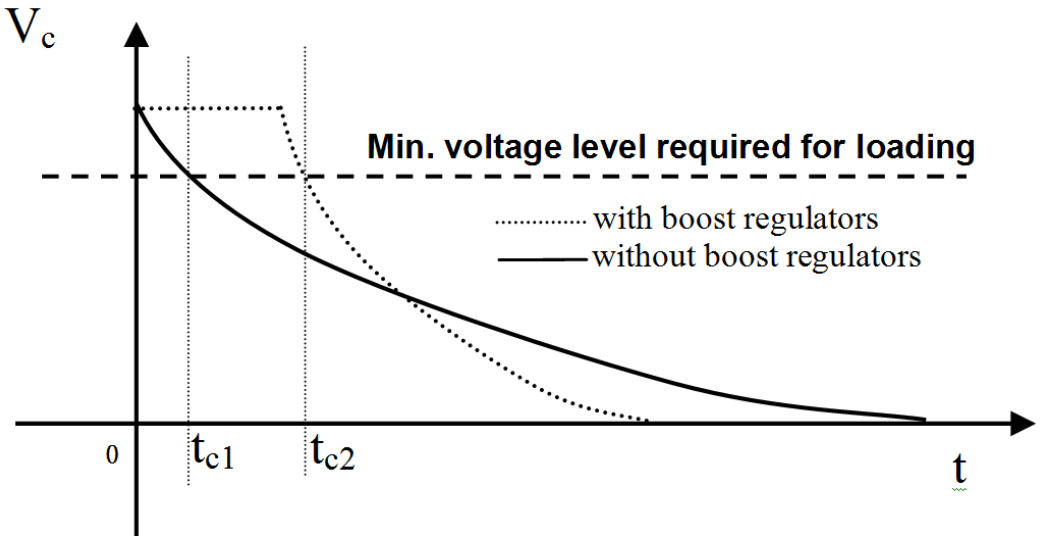



Fig. 4.4. If the AC mains voltage is recovered within the regulation time at point A than the output voltages of the boost regulators are still working under regulation, then the output voltage of the voltage sag compensator can be smoothly maintained over the entire voltage sag incident.

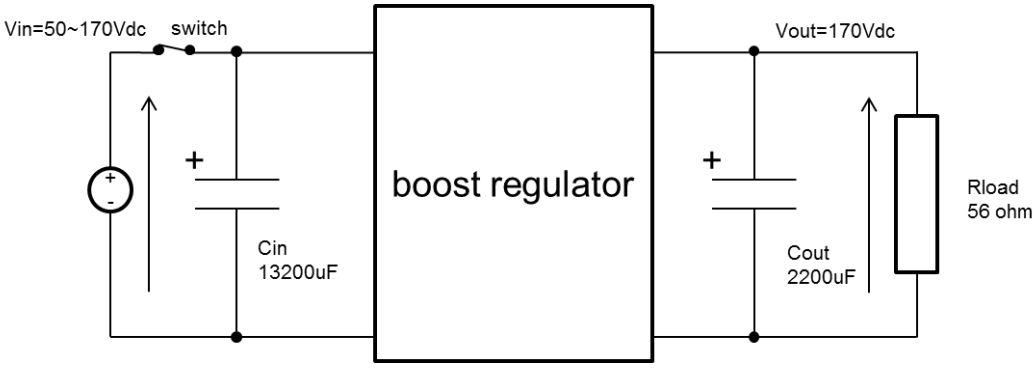



Fig. 4.3 Evaluation test setting on with or without boost regulator.

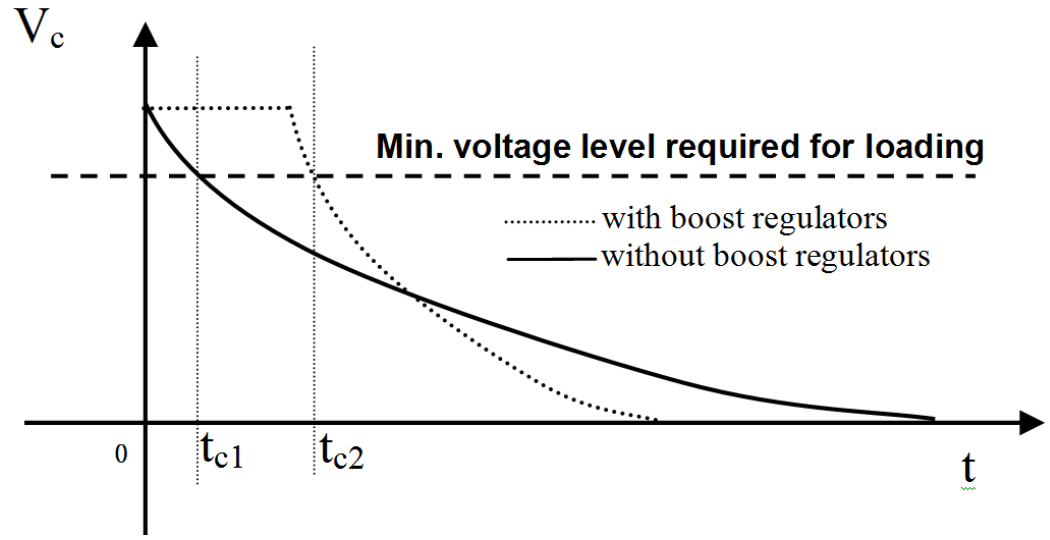



Fig. 4.4 The waveform of the high-tension DC voltage available to the inverter when the AC mains voltage fails (drops to zero) [53]

Assuming that the minimum acceptable DC input voltage of the boost regulators is $V_{cmin}$, the minimum capacitance of C1 and C2 is set to enable the compensator to ride through a complete loss of the AC mains voltage for a sag period of $T_{sag}$ can be found as follows:

Energy available from boost regulators = Energy dissipated in the load

$$2[\frac{1}{2}CV_{c\max}{}^2 - \frac{1}{2}CV_{c\min}{}^2] = PT_{sag}$$

Where $C$ = C1= C2 ,

$V_{c\max} = 1.414V_{ac}$,

$P$ = Power dissipation in the load, and

$T_{sag}$ = Duration of voltage sag.

The required capacitance is found to be $$C = \frac{PT_{sag}}{2V_{ac}{}^2 - V_{c\min}{}^2}$$

Two boost regulators are used in the DC voltage regulator to regulate the outputs at +170Vdc (high-side) and -170V (low-side). During the normal operation, when the AC inverter is disabled and there is no power consumption in the AC inverter, the boost converters are almost in a dormant state. However, during the voltage sag period, these boost converters will draw power from the AC mains to maintain the +170Vdc and -170Vdc outputs until the AC mains falls to a very low level. A boost converter circuit is illustrated in Fig. 4.5. The gate driver signal shown in Fig. 4.7 drives the MOSFET Q1 and Q2 to boost up the output voltage.

The block diagram in Fig. 4.6 shows the structure of a boost regulator. Power management PWM controller IC UC3846 designed by Texas Instruments is used in this regulator. The boost regulator is working in continuous conduction mode (CCM) with current mode control. A slope compensation resistor (R11) is added in Fig. 4.6 , which sums up oscillating signal directly with current sensing signal, that could stabilize the converter working with >50% duty cycle under current mode control.

Each side of the boost regulator circuit design specification is defined as follows:

Maximum power output $P_o$ = 500W (each boost converter)
Minimum input voltage, $V_{in}$ = 50Vdc
Maximum input voltage, $V_{in}$=170Vdc
Nominal output voltage, $V_{out}$ = 170Vdc
Nominal output load current, $I_o$ = 3A
Switching frequency, $f_s$ = 80kHz
Duration of voltage sag $T_{sag}$ = 0.3seconds
Efficiency under full load condition = 80~99% depending on input voltage

Key components value and part no. in Fig. 4.5 are selected as follows:

Inductor, L = 100uH
Diode, D = MUR1560 x 2
N-channel power MOSFET 1, Q1 = IXFX32N50Q x 2
N-channel power MOSFET 2, Q2 = IXFX32N50Q x 2
Input capacitor, $C_{in}$ = 13200uF / 200V
Output capacitor, $C_{out}$ = 2200uF / 200V

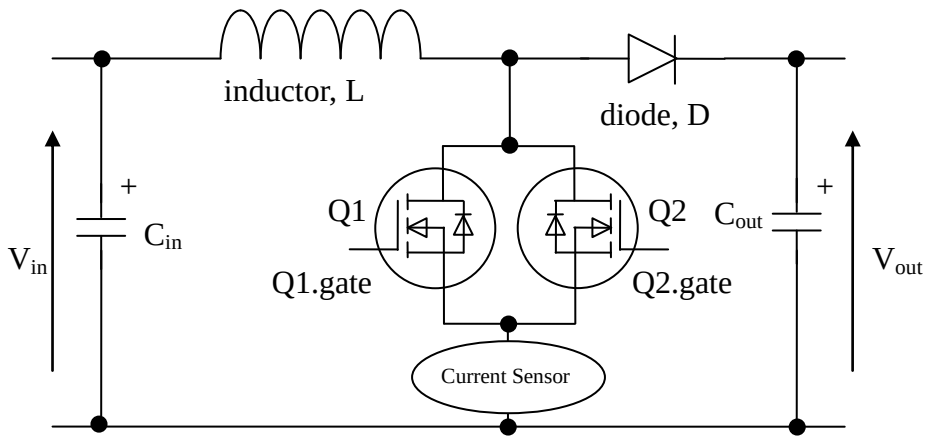



Fig. 4.5 The simplified boost converter circuit at high-side and low-side

In this boost converter, controller supply voltage, Vcc, of both high-side and low-side controllers are supplied from AC mains by step-down transformers, but the power MOSFETs are directly connected to high-side and low-side circuits. In order to a provide maximum duty cycle with isolation control signal for a boost converter, there is a special arrangement with a driving signal on that switches by using an isolation pulse transformer. It solves the isolation problem and advances the boost converter working in duty cycle >50%. The driving signal on Q1.gate and Q2.gate are shown as Fig. 4.7. The equivalent "ON" duty cycle of Q1 and Q2 are > 50% as Fig. 4.8. Under this conversion on the driving signal, the power switch can operate at >50% with isolation to controller. This allows the remaining charges in $C_{in}$ to boost up to $C_{out}$, which supplies nominal voltage level to inverter during compensation.

Fig. 4.8 shows the typical voltage and current waveform of a continuous conduction mode (CCM) operation of a boost converter, with the inductor average current, $I_{L(avg)}$ would never drop to zero current in the conversion. In CCM, there are two stages of power transfer process during "ON" and "OFF" state.

During "ON" state, the power switch is on, and current from input source flows across inductor, L. The charging equation can be expressed as follows:

$$\frac{dI_{L,on}}{dt} = \frac{V_{in}}{L}$$
$$\Delta I_{L,on} = \frac{1}{L}\int_{o}^{DT} V_{in}\,dt$$
$$\Delta I_{L,on} = \frac{DT}{L}V_{in}$$

Where Vin= input voltage level, Vout= output voltage level

D = ON duty cycle, T = switching period

During "OFF" state, the power switch is off, inductor L will be discharged. The output voltage, Vout is equal to the sum of the input voltage and the voltage in L. The equation can be expressed as follows:

$$V_{in} - V_{out} = L\frac{dI_L}{dt}$$
$$\Delta I_{L,off} = \int_{DT}^{T} \frac{V_{in}V_{out}}{L}\,dt$$
$$\Delta I_{L,off} = \frac{(V_{in} - V_{out})(1-D)T}{L}$$

As input energy and output energy should be converted, thus input voltage and output voltage relationship can be found:

$$\Delta I_{L,on} + \Delta I_{L,off} = 0$$
$$\frac{DT}{L}V_{in} + \frac{(V_{in} - V_{out})(1-D)T}{L} = 0$$
$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D}$$

The maximum duty cycle of CCM boost converter:

$$D_{\max} = \frac{V_{out} - V_{in,\min}}{V_{out}}$$

The minimum duty cycle of CCM boost converter:

$$D_{\min} = \frac{V_{out} - V_{in,\max}}{V_{out}}$$

The minimum required inductance $L_{(\min)}$ for CCM boost converter:

$$L_{(\min)} = \frac{V_{in,\min} D_{\max}}{f_s \Delta I_L}$$

Where $I_p = I_{L(avg)} + \frac{\Delta I_L}{2}$, $I_{L(avg)} = \frac{I_o}{1 - D_{\max}}$, $f_s = \frac{1}{T}$

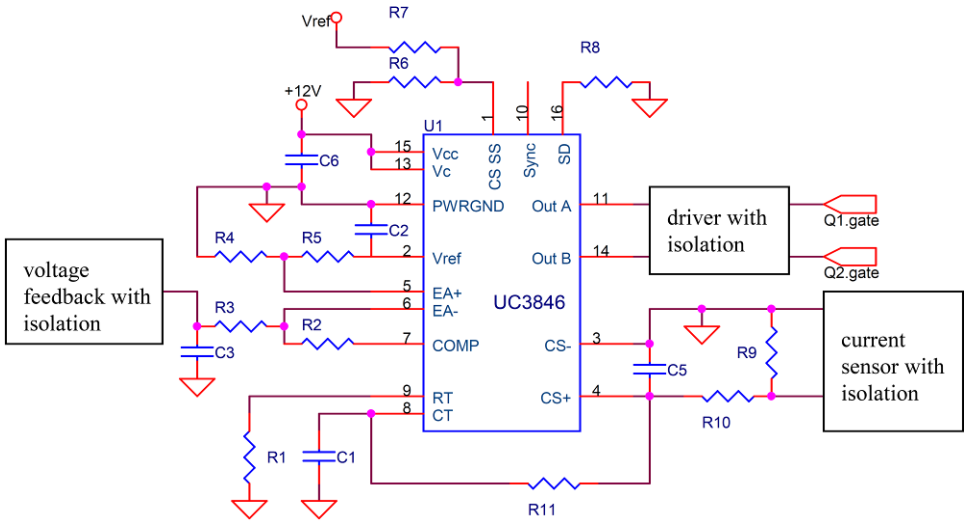



Fig. 4.6 The simplified UC3846 control circuitry using current mode control with slope compensation.

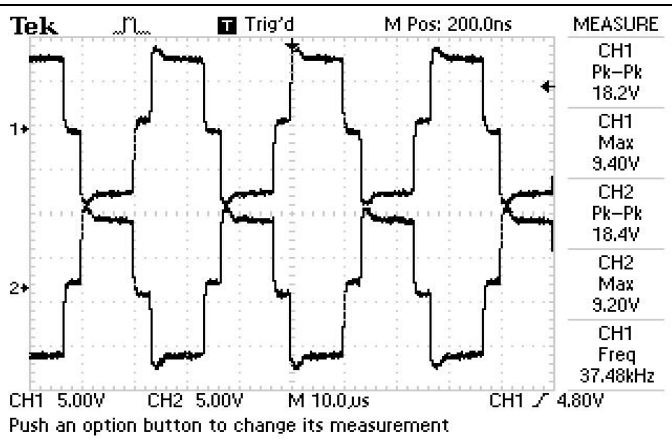



Fig. 4.7 Driving signal waveform on MOSFET Q1.gate and Q2.gate at $D_{max}$

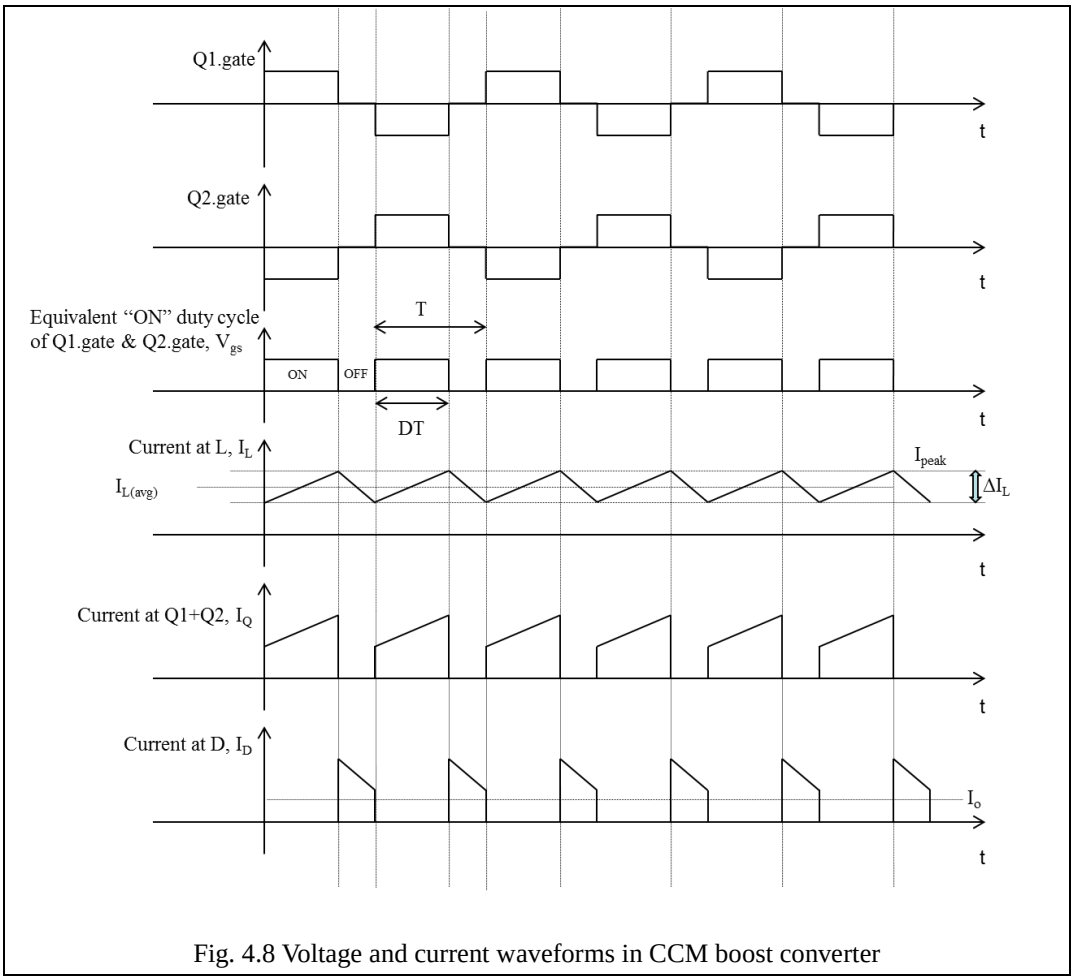



Fig. 4.8 Voltage and current waveforms in CCM boost converter

### 4.2.3 Design of the AC inverter block

Fig. 4.9 highlights a simplified circuit of the AC inverter in Fig. 4.1. The AC inverter is designed to have a fast response time and to provide sinusoidal output voltage. The design of the AC inverter involves the synthesis of the MOSFET gate control signal and the signal is generated by microcomputer controller shown in Fig. 4.1, which will be discussed in Chapter 5. The DC input voltages of the AC Inverter are +170Vdc and -170Vdc (referring to the neutral at 0Vdc). The hardware part of the AC inverter consists of high-power switching MOSFETs and a filtering LC circuit for the 50/60Hz output. The AC inverter is activated only during the voltage compensation period. During normal operation the AC inverter is in standby mode. So, it can be expected that the average power dissipation of the AC inverter is very low. As a result, a relatively small heat sink can be used. However, during the voltage compensation period, the power loss in the AC Inverter is temporarily increased. In order to prevent overheating, a protection scheme is required. This inverter can be rapidly activated at any time slot of sinusoid waveform according to PWM control signal which is different from existing low-cost inverters on the market using isolated transformer scheme. This property allows the compensator compensate voltage sag at any unpredictable time instance.

Design specification of the inverter is defined as follows:

Output power rating = 1.2kVA(1.2 times of nominal rated power 1kVA)
High side input voltage = 170Vdc
Low side input voltage = 170Vdc
Inverter output voltage in rms = 120Vac
Inverter output current in rms = 10A
Output frequency = 50Hz or 60Hz (depending on PWM driving signal)
Output waveform shape = trend to smooth sinusoid
Output waveform start angle = 0 degree ~ 360 degree of phase angle (depending on PWM driving signal)

Key components used in the inverter are shown as follows:
Input capacitor a, $C_a$ = 2200uF/200V
Input capacitor b, $C_b$ = 2200uF/200V
N-channel power MOSFET a, $Q_a$ = IXFX32N50Q x 2
N-channel power MOSFET b, $Q_b$ = IXFX32N50Q x 2
Filtering inductor, $L_{filter}$ = 400uH
Filtering capacitor, $C_{filter}$ = 20uF/250Vac

The designed inverter is evaluated with input voltage of +170Vdc and -170Vdc. Output load are combinations of resistive loads, capacitive loads, inductor loads and AC relays, AC contactors. Experimental results show that all loads operate well with inverter as similar as using AC mains. A waveform trend to sinusoid wave with 120Vac can be measured at the output of inverter.

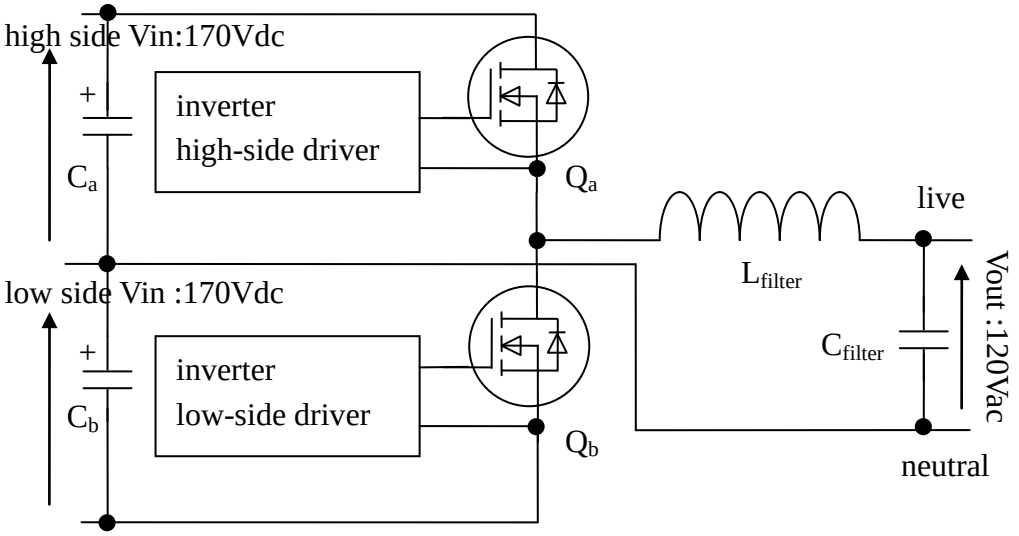



Fig. 4.9 A simplified AC inverter circuit

### 4.2.4 Power supply arrangements for microcomputer controller block

In the design of a voltage sag compensator, one of the major problems is the transient nature of the voltage sag incident, during which many parts of the circuit are actually working in a transient state.

Referring to Fig. 4.1, during the voltage sag incident the AC mains will no longer be a reliable source to supply power to the microcomputer controller. In the design of the power supplies for the control circuits, a super capacitor is used to store up the required back-up energy for the control circuits. In addition, it is arranged that the AC power for the microcomputer controller is derived from the output of the sag compensator. Since the output of the voltage compensator should be well maintained to ride through the voltage sag incident, the power supplies for the microcomputer controller should have no interruption under the voltage sag are within the design limits. The DC power supply to the microcomputer controller can also be maintained constant until the very last minute when practically all the energy stored in the energy-storage capacitor bank has been used. This mechanism can fully protect the proper operation of the compensator under transient conditions.

### 4.2.5 Design to reduce delay in voltage sag compensation and to minimize chattering of AC contactors in the load

Naturally, there are delays in the voltage sag compensation process. The delays include in detecting the occurrence of the voltage sag incident and in transferring the load from the AC mains to the AC inverter. These delays cause problems in sensitive loads such as programmable logic controllers, AC contactors, and computer numerical control units. A possible way to reduce the transfer delay is to use semiconductor devices to implement the function of the transfer switch. However, the use of semiconductor switches will result in considerable voltage drop and power dissipation. The relatively poor reliability of semiconductor switches under transient conditions is also a concern. On the other hand, if a relay switch is used to implement the function of the transfer switch SW, the transfer delay could be intolerably long due to inappropriate design.

In our design the delay problem is alleviated by a combined use of relay switch and software control of the semiconductor switches in the AC inverter. The

relay switch provides low power dissipation and robustness against transients, and the semiconductor switches gives fast speed of transfer.

The delay in transferring the load from the AC inverter back to the AC mains is relatively not critical, because this transfer can be adjusted to take place around the zero-crossing region of the AC mains. A slight delay in the zero-crossing region would not do much harm to the operation of the load.

A very important task of the voltage sag compensator is to ensure that the operation of AC contactors in the loading circuit will be least affected by the transfer operation between the AC mains and the AC inverter. In order to achieve this objective, a study was conducted in detail in the operation of the AC contactor and developed a z-parameter model of the AC contactor to help analyze the behavior of the contactor under transient conditions. The following is a summary of these findings and the works:

(1) In an AC contactor, in order to ensure that the energizing solenoid will not drop out during the zero-crossing region of the AC driving current, the solenoid is split into two halves. Half of it has an effective one-turn short-circuited secondary winding. The total energizing force of the solenoid is the sum of the energizing force from the energizing coil and that from the one-turn short-circuited secondary winding. Since the induced current in the one-turn short-circuited secondary winding is inductively phase-shifted, the sum of these two energizing forces (added together in terms of absolute values) will not drop to zero over the entire cycle of the AC mains. This arrangement enables the solenoid to be energized over the entire cycle of the AC mains without dropping. However, the complex structure of the AC contactor makes the analysis of its behavior difficult.

(2) As point (1) mentioned, a study developing a z-parameter model of the AC contactor in a PSpice program [55] is performed. This z-parameter model makes use of the gyrator concept to derive an equivalent circuit of the energizing solenoid, including the one-turn short-circuited secondary winding, of the contactor. The equivalent circuit can then be mixed with the voltage sag compensator circuit to simulate the behavior of the AC contactor under transient conditions. The model has been extensively used to help optimize the design of the compensator.

In the voltage sag compensator, the microcomputer controller compares the AC mains voltage with a sine-wave look-up table to detect the occurrence of the voltage sag incident. The detection time can be kept reasonably short, which helps reduce the total delay time in the voltage sag compensation process.

In the design, tailor-made software is developed to minimize the chattering of AC contactors during transfer periods.

## 4.3 Protections and user interfaces

The protection of voltage sag compensator can be achieved by hardware configurations. Input and output fuses can prevent damage of the compensator when the output of the compensator is short circuited. A current sensing and limiting circuit in the inverter can avoid excessive compensator output current. Dip switches can be used to provide a user-friendly interface to select suitable compensation time and voltage sag triggering level for different applications.

## 4.4 Design specification of a 1kVA voltage sag compensator

Based on the considerations given above, the design specification of a 1kVA voltage sag compensator is summarized in Table 3. [57]

Table 3 List of design specification of a 1kVA voltage sag compensator

| **INPUT SUPPLY** | |
|---|---|
| Nominal input voltages | 110~120Vac,single phase |
| Maximum input voltages | 125Vac,single phase |
| Input frequency | 50Hz/60Hz auto-sensing ± 1% |
| Full load current(120Vac) | 8.33A |
| Connection configuration | hardwire terminal blocks |
| Initial time | 10 seconds |
| **SYSTEM CONDITION** | |
| Support voltage | 90% of nominal(10% sag) to 0% of nominal(100% sag) |

| | |
|---|---|
| Adjustable transfer voltage | user adjustable from 50%-90% |
| Inrush capability | 8 times nominal current (to withstand variable/ inductive load inrush current) |
| Operating conditions | 0~45°C/32~113°F |
| **INVERTER OUTPUT** | |
| Maximum output current | 8.33A |
| Maximum output power | 1kVA |
| Output voltages | 120Vac -15%/+15% |
| Power factor range | cosΦ from 1 to 0 |
| Output frequency | 50Hz/60Hz (depends on input frequency) ± 1% |
| Ride-through cycle | 80 cycles |
| Maximum response time for compensation | 2 milliseconds |
| Maximum recharge time after sag | 3 seconds |
| Efficiency | ~99% (test under full load normal operation) |
| **PROTECTIONS** | |
| Short circuit protection | required |
| Undervoltage protection | required |
| Low voltage level disable | required |
| **INDICATORS** | |
| Input power indicator | green neon light |
| Inverter running indicator | amber neon light |
| Output power indicator | red neon light |
| **MECHANICAL** | |
| Standard package | 19” rack |
| Weight | 13kg / 29lbs |

## 4.5 Summary

This chapter described the hardware design considerations for voltage sag compensators. It covered the areas of AC-DC voltage doubler, the energy storage charge bank, the boost DC regulator, the AC inverter, the power supply for control circuits, the transfer switch, and the protection and the user interface. The design specification of a 1kVA compensator was summarized. The software design considerations of the voltage sag compensator will be discussed in the next chapter.

# Chapter 5: Software design considerations for the voltage sag compensator

## 5.1 Introduction

The hardware parts have been discussed in chapter 4. This chapter will focus on the software design of the voltage sag compensator. Firstly, the program flow chart and the selection of microcontroller unit will be discussed. Secondly, each critical function in the system will be described. The schemes on safety and the protection will also be touched. Finally, there will be a summary.

## 5.2 Why software control is required for compensator?

There is a lot of inexpensive MCU ICs on the market which contain pulse width modulation (PWM) generators, A/D converters, and timers. Such MCUs can be programmed to function as the microcomputer controller of the voltage sag compensator.

Software control is used in the compensator. Compared with the hardware approach, software control has the following advantages:

1) The detection of the input voltage, the AC mains frequency and the phase of the input voltage can be easily and accurately implemented using an A/D converter and a sine-wave reference look-up table in the MCU. Implementation of such functions using hardware can be complicated and costly.

2) The control functions in the MCU are less likely affected by noise or unstable power supply.

3) The MCU approach using software control has less component count, simplified the circuit, high reliability, and is cost competitive.

For the reasons given above, Atmega8 was chosen to function as the microcomputer controller of the voltage sag compensator.

## 5.3 Structure of microcomputer controller

A high performance MCU IC Atmega8 was selected for this thesis. It is a low power 8-bit microcontroller, manufactured by Atmel Corporation [56]. ***Appendix B*** shows the block diagram of Atmage8. The main features:

1) 8K bytes of in-system self-programmable flash
2) 1K bytes of internal SRAM
3) Clock rate: 0 - 16 MHz
4) Three timers - Two 8-bit timers and one 16-bit timer.
5) Four channels of 8-bit input/output.
6) Support six channels of analog-to-digital converting pins
7) Three-channel PWM generator.

The MCU in the microcomputer controller works as an automatic frequency detector for 50Hz or 60Hz at start-up. It detects the zero-crossings of the AC mains voltage to identify the frequency of AC mains. If the detected frequency is out of the preset range, the compensator will not operate. This arrangement prevents the compensator from being trapped by an unstable power system.

The MCU has an internal analog-to-digital converter in the Fig. 5.1, which provides a means of accurate voltage comparison. The voltage level of the AC mains is continuously measured during operation. If a voltage sag incident is detected in the AC mains, a control signal will be sent to the inverter to start generating an AC voltage to do the compensation.

Referring to Fig. 5.1, accurate timing control signals can be generated by the crystal oscillator of the MCU. Timing control of the transfer switch and the inverter is a key part of the operation. The transfer switch should be switched as fast as possible and the inverter should be turned on/off at the correct time. Otherwise, transient short circuits may occur between the inverter and the AC mains. Highly accurate PWM driving signals for the inverter are also generated by the MCU.

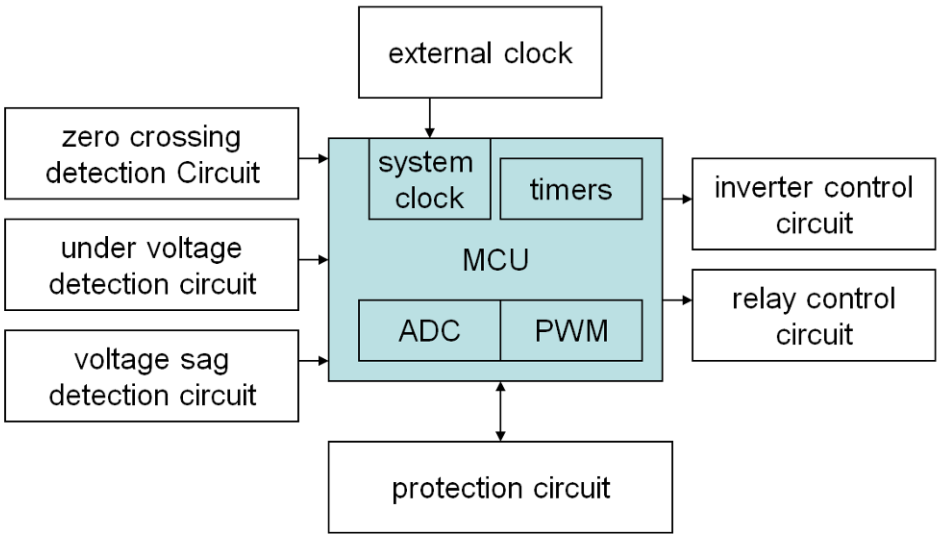



Fig. 5.1 The block diagram of microcontroller controller and external control unit in compensator

## 5.4 Program flow chart

Fig. 5.2 shows the program flow chart for the voltage sag compensator. The program flow is revealed as following:

**Step 1:**

When the MCU in the microcomputer controller, shown in Fig. 4.1, is powered up at the beginning, it will initialize all variables for the whole system. At the same time, the hardware circuits step down the input AC mains voltage to the MCU. The analog voltage is converted to digital signal by the ADC inside the MCU. The MCU performs calculations and comparisons with internal database reference to determine whether the AC voltage is normal or not. The program will loop here until nominal input AC voltage is detected.

**Step 2:**

When nominal input AC mains voltage is confirmed, the internal timer of the MCU will be triggered by the zero crossing signal of the AC mains voltage. The

timer will start to count the time period between two zero crossing signals to measure the frequency of the AC mains. If the frequency does not fall within the range of 50Hz or 60Hz, the frequency detection process will repeat until the range of 50Hz or 60Hz is detected.

**Step 3:**

Once the auto-frequency detection is finished, another internal timer will start the voltage measurement based on the detected frequency. This timer provides interruptions for the voltage detections and the comparisons at different time slots. The content of timer's interrupt routine is to (a) enable ADC to get the digital format of the existing AC mains voltage at the input, (b) compare the existing AC mains voltage with an internal reference in database to detect voltage sag, (c) detect the zero crossing signal and update the timer register for frequency synchronization.

**Step 4:**

If a voltage sag is detected in an interrupt routine, the MCU will provide a control signal to the relay to enable it to break the load from the AC mains input. At the same time the MCU generates a PWM signal in phase with the AC mains to drive the AC inverter control circuit. The PWM signal is initialized by input zero-crossing signal from the AC mains, at the same time the MCU will generate the pulse width according to sinusoid lookup table, which has been embedded in its memory. The AC inverter then regenerates a sinusoidal AC output voltage for the load.

**Step 5:**

The AC inverter regenerates the AC voltage until the end of the compensation period. The length of the compensation period is preset by the user. At the end of the compensation period, the MCU will provide a control signal to the relay to enable it to switch the load back to the AC mains.

**Step 6:**

After a complete voltage sag event, the program will reset all variables. It will then loop back to the detection of under-voltage again and restart the voltage sag checking, as mentioned in Step 2.

It is important to note that there is the MCU under-voltage lockout in the

program flow chart shown in Fig. 5.2. This under-voltage lockout serves to stop the MCU program when the DC supply voltage of the MCU is below the minimum of 2.7V. The lockout function prevents the MCU from working erroneously and sending hazardous control signals under abnormal conditions.

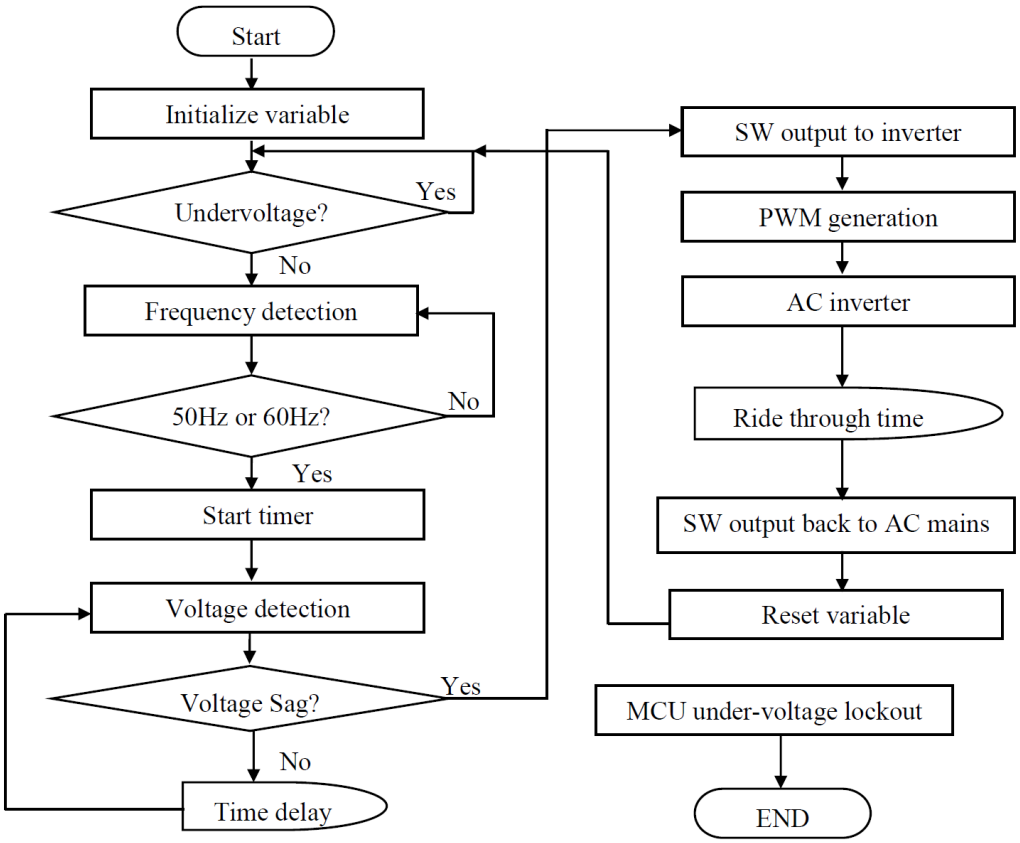



Fig. 5.2 Program flow chart for voltage sag compensator [53]

## 5.5 Software design

In the voltage sag compensator, Atmega8 is used as the MCU in the microcomputer controller. The internal timers, PWM generator, analog-to-digital converter and, real time calculations in the MCU, work together to perform the functions of the controller. This section will analyze these functions one by one.

### 5.5.1 Frequency detection

The compensator is designed to operate at 50Hz or 60Hz AC mains frequency. The auto-sensing of the frequency detection routine is run at the beginning of the program to identify the input frequency. As the input voltage waveform of the AC mains is in sinusoidal shape, the AC waveform is clipped to square shape by a simple hardware circuit as shown in Fig. 5.3. The zero-crossing time is detected from the negative edges of the square pulse providing interruption for a routine. In the routine, the zero crossing point is monitored via an internal analog-to-digital converter. The build-in clock counters measure the frequency of 50Hz or 60Hz with repeated checking. Once the frequency is identified, all related variables will be correspondingly preset to that frequency. The timers will also be set and started for voltage sag checking accordingly.

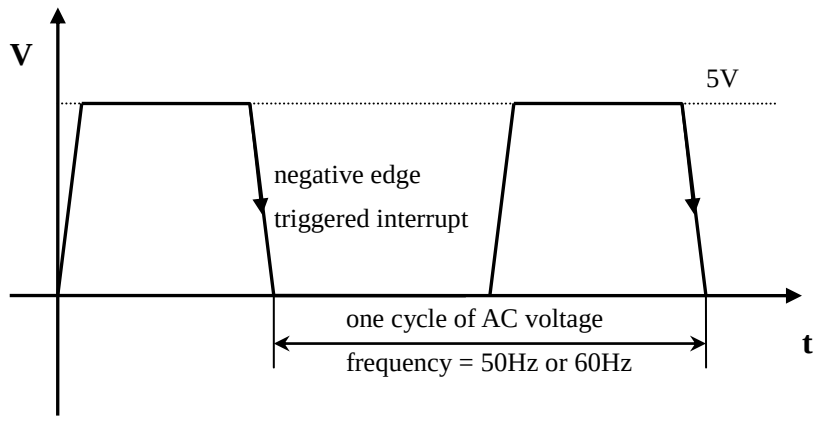



Fig. 5.3 The square shape waveform for zero crossing detection

### 5.5.2 Frequency synchronization

Although the frequency of the AC mains is detected at the beginning of the program, there can be up to 1% variations in the real environment. By simple calculation, if there is 1% of frequency variation for 1 hour at 50Hz, the worst case voltage waveform will shift 0.36 seconds comparing with ideal 50Hz AC mains. If there is no synchronization, the time shift will easily cause false voltage sag detection. In order to avoid this problem, the frequency synchronization is required in each cycle of the sinusoidal waveform. The timer will be updated at $0^{o}$

by detecting the zero-crossing of the AC mains. This synchronization ensures that the AC waveform is compared with a corrected reference. In order to minimize the noise for zero crossing detection, 0.01uF of capacitor is added between input pin of MCU and GND. The iterative method is used to check the voltage level of that signal to ensure the actual signal.

### 5.5.3 Voltage detection

The main purpose of the voltage detection is to identify whether the voltage sag exists in input AC mains or not. The high potential AC mains input is converted to a lower voltage by a low frequency transformer. The voltage is then rectified (using a bridge rectifier) as shown in Fig. 5.4 in solid line.

As previously stated, the timer interrupt routine runs the function of the voltage sag detection in each time slot. The MCU extracts the voltage level from the analog-to-digital conversion. The dotted line in Fig. 5.4 shows the protection area in the MCU's database. If the detected voltage is smaller than the protection level, the MCU will judge that there should be the voltage sag at the input AC mains. In order to prevent error triggered by noise, the detection process will rapidly repeat again to ensure that there is a real sag. If a voltage sag is confirmed, the compensator will generate AC from the inverter to output.

The MCU does the comparison for each voltage sample with lookup table in internal database which is stored in the ROM of the MCU. If the voltage samples are below the preset value, the program will start the compensation for output. The solid line is set to the peak level at 2.5V for 120Vac level. The peak voltage of level of should be set to 2.08V (100Vac) for factory preset value. It means that if voltage sag drops below to 83.33%, the compensator will be triggered to provide compensation.

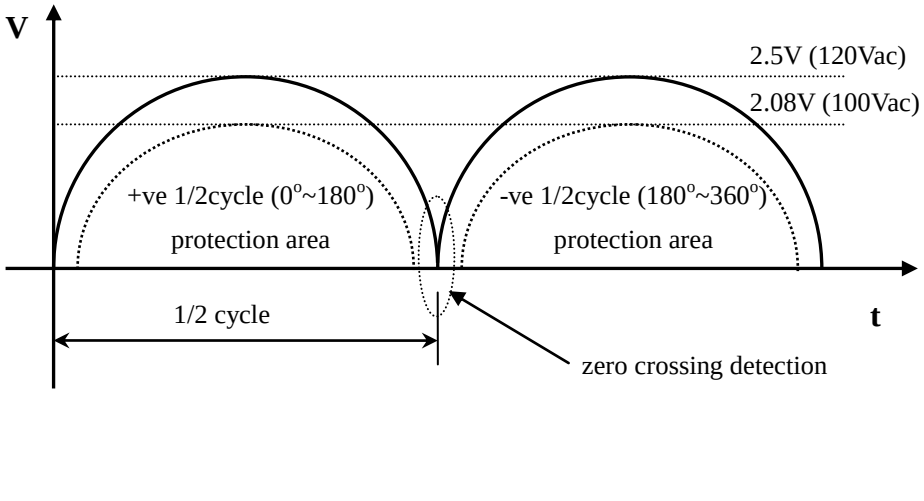



Fig. 5.4 Voltage waveform for voltage detection

## 5.5.4 PWM generation

The AC inverter requires a PWM gate driving signal to regenerate a smooth sinusoidal AC waveform. The built-in PWM generator in the MCU, with an accurate clock, synthesizes the driving signal in a simple way. In the implementation, the width of PWM signal is programmed to follow a sinusoidal look up table which is stored in the internal memory of the MCU. The PWM signal is also synchronized to the AC mains in frequency and phase. An example of the waveform is shown in Fig. 5.5.

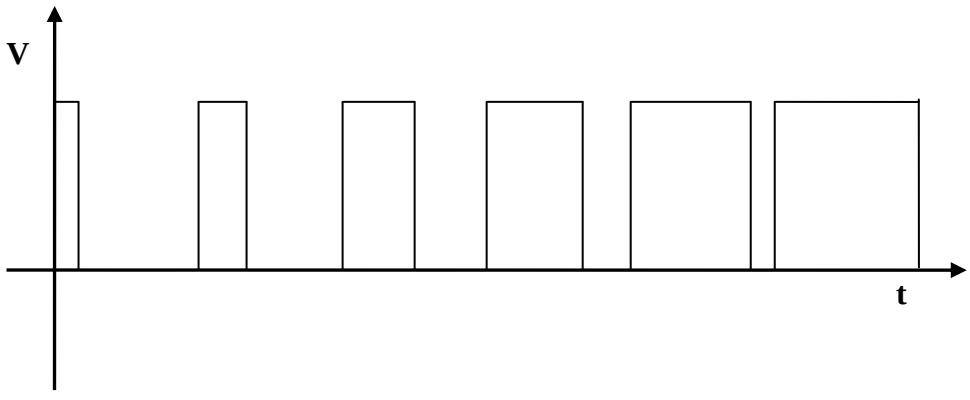



Fig. 5.5 A PWM control waveform to inverter control circuit

A predicted sample of the PWM signal with AC inverter output waveforms are demonstrated in Fig. 5.6. The AC inverter output is generated by the PWM on/off switching of the high-side and low-side MOSFETs in the inverter. An LC-filter smoothes the switching square pulses to sine wave. As voltage sags can randomly occur in any time slot, the starting point and ending point of the AC inverter output can also exist in any time slot.

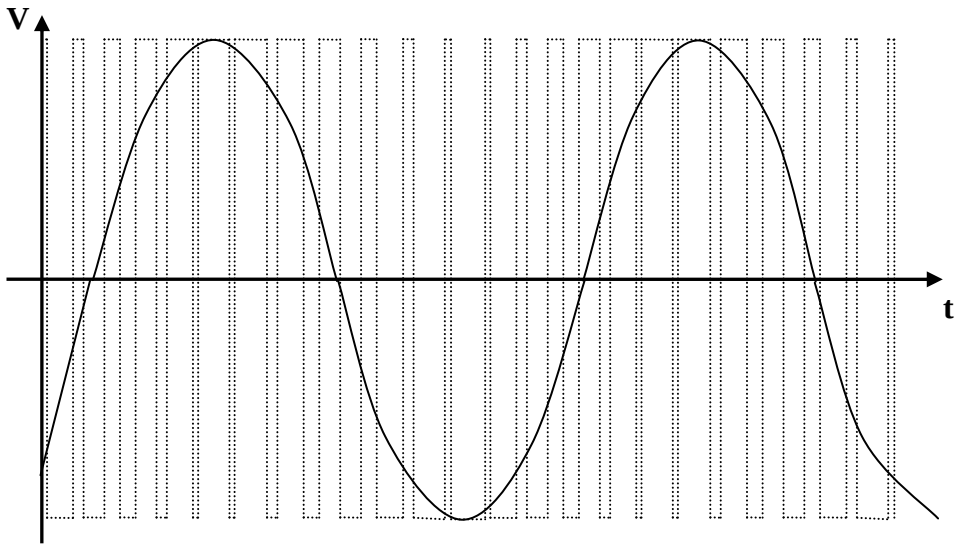



Fig. 5.6 The predicted AC voltage waveform at inverter output

### 5.5.5 Timing control

Timing control is critical for the voltage sag compensator. A crystal clock generator is used to give the accuracy of the internal timers. Switching between the AC mains input and the AC inverter output also requires accurate timing control.

### 5.5.6 User interface and control

This flexible software control allows end users to select the ride through time for the compensation and the sag threshold voltage. These are important options for the voltage sag compensation, because different loading, or equipment, can have different sensitivities to the voltage sag.

The sag compensation threshold voltage of the voltage sag compensator can be adjusted from 85Vac to 115Vac in steps of 5Vac, as shown in Table 4. The factory default setting is 100Vac (ON-OFF-OFF).

The sag compensation time of the voltage sag compensator can be adjusted from 0.25sec to 2.00sec in steps of 0.25sec, as shown in Table 5. The factory default setting is 2.00 sec (ON-ON-ON).

Table 4 Table of threshold voltage selector

| **Threshold voltage selector (SW1)** | | | |
|---|---|---|---|
| **$V_{TH}$** | **SW1_1** | **SW1_2** | **SW1_3** |
| 115Vac | ON | ON | ON |
| 110Vac | ON | ON | OFF |
| 105Vac | ON | OFF | ON |
| *100Vac | ON | OFF | OFF |
| 95Vac | OFF | ON | ON |
| 90Vac | OFF | ON | OFF |
| 85Vac | OFF | OFF | ON |
| 100Vac | OFF | OFF | OFF |

* Factory default setting

Table 5 Table of compensation time selector

| **Compensation time selector (SW2)** | | | |
|---|---|---|---|
| **$T_{COMP}$** | **SW2_1** | **SW2_2** | **SW2_3** |
| *2.00s | ON | ON | ON |
| 1.75s | ON | ON | OFF |
| 1.50s | ON | OFF | ON |
| 1.25s | ON | OFF | OFF |
| 1.00s | OFF | ON | ON |
| 0.75s | OFF | ON | OFF |
| 0.50s | OFF | OFF | ON |
| 0.25s | OFF | OFF | OFF |

* Factory default setting

### 5.5.7 Safety and protection scheme

As stated previously, the input frequency is detected at the beginning of the startup process. If the frequency is out of the range of 50Hz/60Hz +/-1%, the program will be looped in this statement until the input frequency is within a preset range. This subroutine prevents the system from operating in an incorrect environment.

The under-voltage protection program uses a similar algorithm. As the compensator is normally working at 120Vac input AC mains, the compensator will start to be ready for compensation only if the input voltage is over 95Vac. On the other hand, the number of voltage sag compensation events is counted by the program; the high frequency of voltage sag events exist in short period of time will latch the whole system. No compensation will start at the period time, although the voltage sag exists in the AC mains input. The compensator will recover after a time penalty. This protection scheme avoids the compensator working under noisily power network which is incapable to supply the output voltage to electronic devices.

Under abnormal operating conditions, the inverter in the sag compensator may be repetitively started to compensate the AC mains voltage. A typical example of an abnormal condition is when the AC mains voltage is consistently below the threshold compensation level. Under such condition, the sag compensator will initially compensate the AC mains voltage for 2 seconds and then reconnect the load to the AC mains for 3 seconds. If the AC mains voltage is then still below the threshold compensation level, the compensator will begin another cycle of "2-second compensation followed by 3-second back to the AC mains". However, if the repetitive rate of the compensation cycle is more than 4 times in every minute, the sag compensator may enter a protective mode operation. Under this mode of operation, the sag compensator will stop the compensation operation for 2 minutes, waiting the heat-generating components in the sag compensator to cool down. Within this 2-minute period, the load will be connected to the AC mains without compensation. At the end of the 2-minute period, the sag compensator will start another round of effort to compensate the AC mains voltage, as mentioned above.

The sag compensator can stay in the protective mode of operation indefinitely without damage. As a further protective measure, it is recommended that a circuit breaker be used with the compensator for protection against overloading. The current rating of the circuit breaker should be about 150% of the maximum current rating of the sag compensator.

## 5.6 Summary

This chapter describes the software design considerations of the voltage sag compensator. It covers the areas of program flow chart, algorithms of the input voltage and the mains frequency detection, PWM generation, timing control and protection. The additional user interface is also described. In comparison with prior approaches, this software design is more convenient for users to apply in semiconductor industry to meet SEMI F47 requirements. The construction details of the voltage sag compensator will be discussed in next chapter.

# Chapter 6: Construction of a 120Vac 1kVA voltage sag compensator

## 6.1 Introduction

In this chapter, the design procedure and a construction of a practical parallel type 120Vac 1kVA voltage sag compensator will be described. Some test results to verify the function of the parallel voltage sag compensator will be reported. A user guide for the compensator is prepared. Finally, a summary will be given at the end.

## 6.2 Design procedure of a prototype 120Vac 1kVA voltage sag compensator

Refer to the block diagram of the parallel type voltage sag compensator shown in Fig. 4.1.

**Step 1:** Design and construction of the rectifier block

A voltage doubler circuit was developed to charge up the capacitor bank. The power rating of a bridge rectifier should have enough capacitance for voltage compensation. The inrush current through the input fuse and the rectifier is quite high at start-up period. The inrush current problem could be solved by additional NTC thermistor.

As there are many inductor loads in semiconductor processing machine, some customers request the voltage compensator to meet the specification of compensation power factor 0.25 at full load, the compensator should be able to maintain the AC output voltage for a voltage sag incident of 1-sec duration. By considering of worst case condition, required capacitance can be calculated as

follows:

Assume the high-side and low–side of boost regulators can output 170V when input capacitor voltage drop to 70Vdc, and equivalent power output of 1kVA(power factor 0.25) is equal to 250VA. Referring to formula in section 4.2.2:

$$C = \frac{PT_{sag}}{2V_{ac}^{\ 2} - V_{c\min}^{\ 2}}$$

$P$ = 250VA, $T_{sag}$ = 1sec., $V_{ac}$=120V, $V_{c\min}$ = 70V

$C$ = 10460uF (minimum required capacitance in each regulator to meet the specification for 1kVA power output)

Slow blow input fuse with current rating of 20A (325/326 series Littel Fuse) and rectifier diode of GBPC3508W (35A,800V) are used in the compensator. During start-up, inrush current is high during charging the capacitors. In order to provide a reliable capacitor bank, a negative temperature coefficient (NTC) thermistor of MS35-3R030(30A, 3Ω) is added in series between fuse and rectifier diode. The inrush current of through fuse can be evaluated practically by using different values of resistors peak current, the experimental results are shown in Table 6. It is observed that NTC with 3Ω can limit the inrush current under 15A, which provides sufficient current margin for fuse and rectifier diode.

Table 6 Five samples of input inrush current using different resistors in series

| Test samples / Resistor value | **1** | **2** | **3** | **4** | **5** |
|---|---|---|---|---|---|
| 5Ω | 10.4A | 10.6A | 10.2A | 11.0A | 10.2A |
| 3Ω | 12.6A | 12.4A | 12.4A | 13.0A | 12.4A |
| 1Ω | 15.2A | 16.0A | 15.4A | 15.6A | 15.2A |
| 0Ω | 32.0A | 30.4A | 30.4A | 31.6A | 32.4A |

**Step 2:** Design and construction of the DC voltage regulator block

Two boost regulators are designed and constructed. One is for the high-side inverter MOSFET and the other one is for the low-side inverter MOSFET. Fig. 6.3 shows the prototype of the two boost regulators providing DC power to the AC Inverter which are discussed previously in section 4.2.2. Without these regulators, the output voltage of the AC inverter will be exponentially decaying during the compensation period, as shown in Fig. 6.1. This waveform is unsuitable for the sensitive load. Once the regulators are added, the output voltage of the AC inverter will be more stable (within the compensation period), as shown in Fig. 6.2. It can be observed that boost regulators can extend the compensation time at nominal voltage level with equal capacitance.

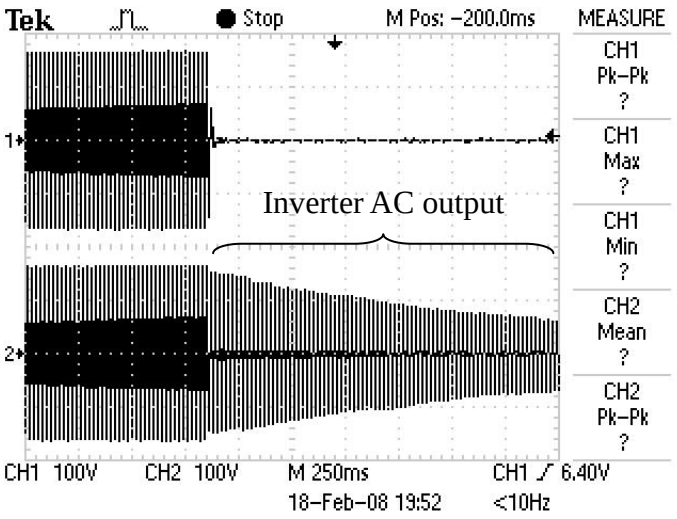



Fig. 6.1 Voltage sag compensator output waveform without boost regulator

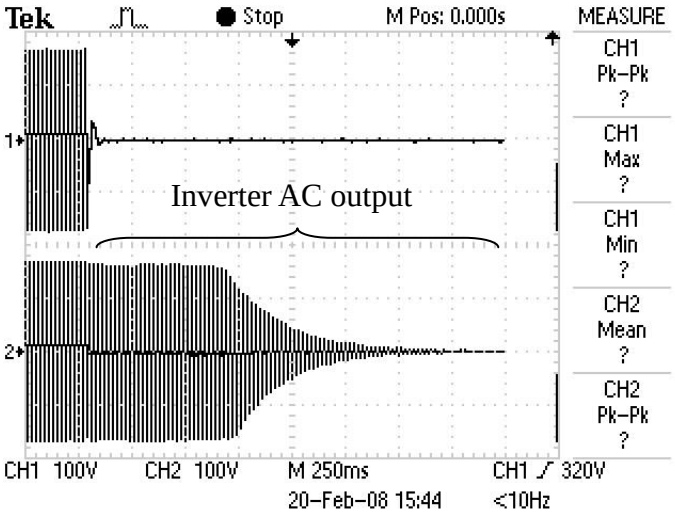



Fig. 6.2 Voltage sag compensator output waveform with boost regulator

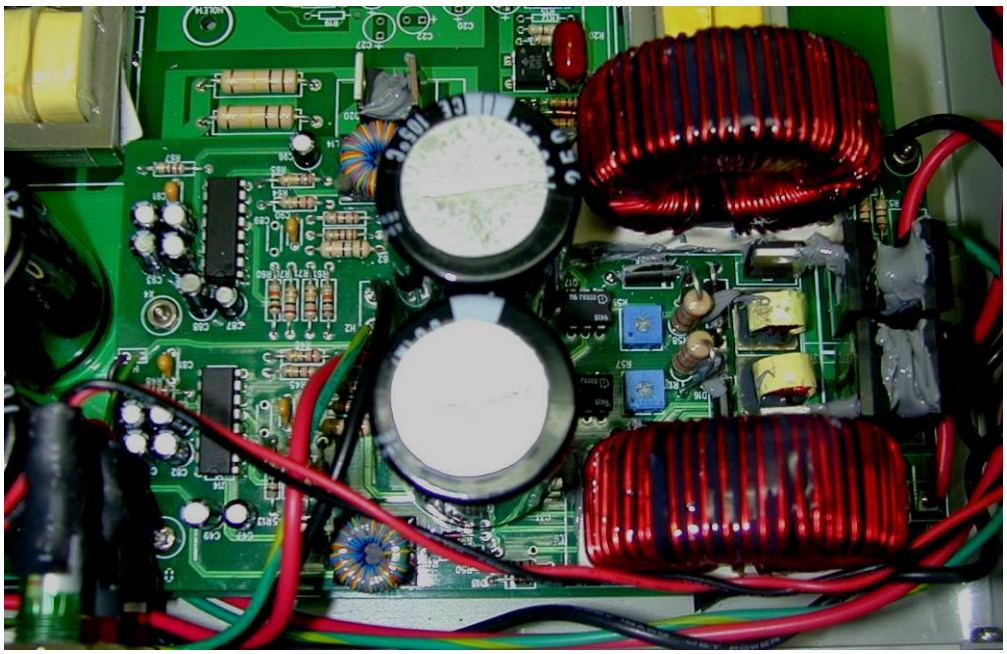


Fig. 6.3 Prototype of two boost regulators for inverter

**Step 3:** Design and construction of the zero crossing detection circuit, the voltage sensing circuit and the microcomputer controller block

The zero crossing detection circuit, the voltage sensing circuit, and the microcomputer controller hardware are designed and constructed. The MCU (Atmega8) in the microcomputer controller with an accurate crystal oscillator is programmed to detect the frequency, the phase and the amplitude of the AC mains voltage to provide the control signals.

**Step 4:** Design and construction of the AC inverter block

An inverter circuit is built, as discussed previously, in section 4.2.3 which generates AC output when driven by the PWM control signal from the MCU of the microcomputer controller. An AC inverter output waveform is recorded in practical experiments during a voltage sag event, as shown in Fig. 6.4. Channel 1 is showing input voltage waveform of AC mains and the channel 2 is showing output voltage waveform of AC inverter. When there is no voltage sag in AC mains, the output voltage is following the input voltage waveform. But, if there is voltage sag at input, the output voltage is regenerated by inverter from DC capacitor bank. The AC contactors and AC relays, the output loads, can operate without any malfunctions in the whole process, which can guarantee that the AC inverter is functioning properly. Voltage sags at different phase angles are randomly generated at input, which shows that the AC inverter is able to start the voltage compensation at any phase angle.

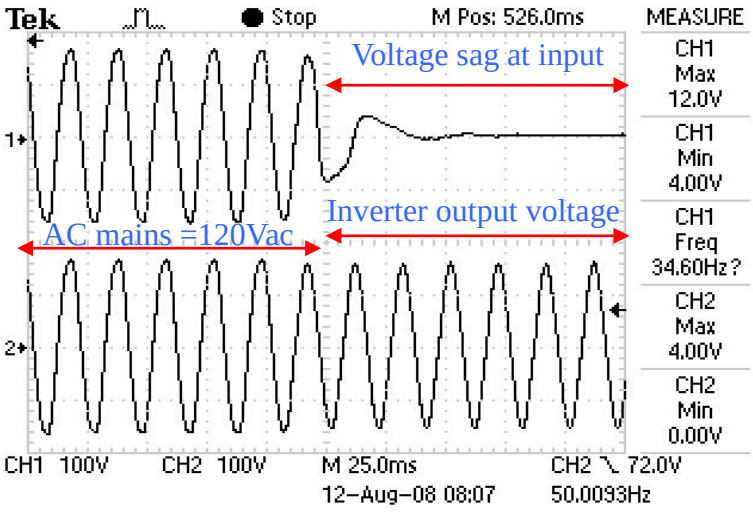



Fig. 6.4 Inverter output waveform at channel 2

**Step 5:** Integration of all the building blocks into a complete system

After independent testing in each hardware part, all blocks are integrated into a single PCB. The hardware and software are then evaluated together. The layout of the PCB is shown in ***Appendix C***. Fig. 6.5 shows a simplified schematic diagram of the parallel type voltage sag compensator.

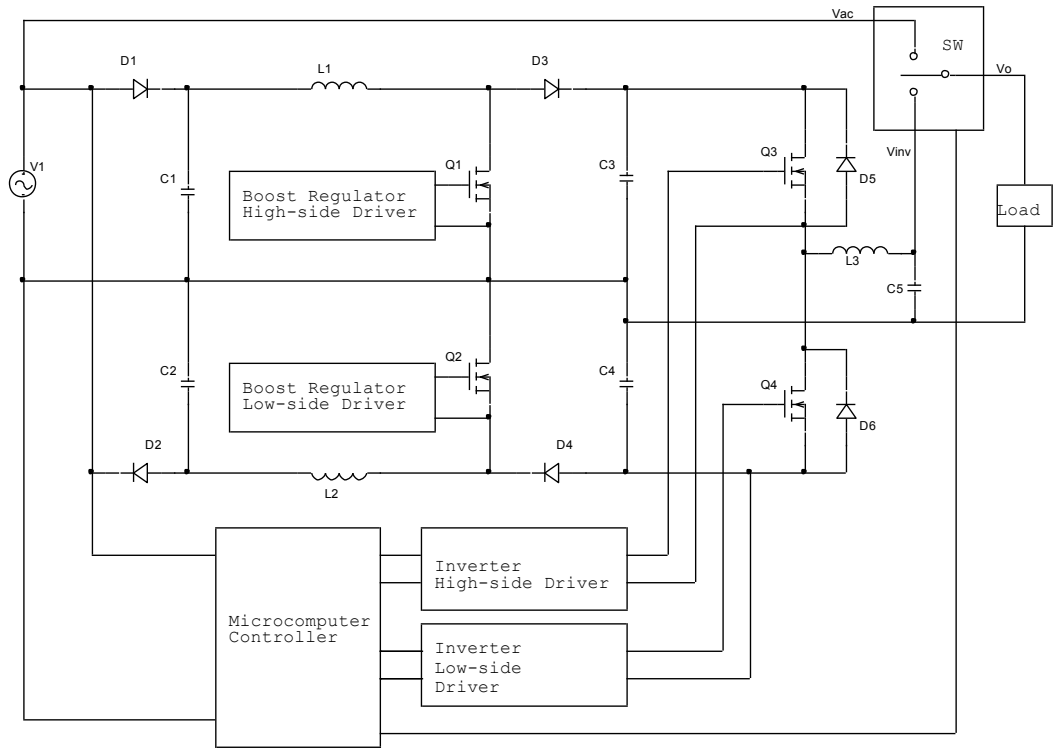



Fig. 6.5 Simplified schematic diagram of the parallel type sag compensator

The following is a brief overview of the operation of the parallel type sag compensator shown in Fig. 6.5.

The rectifier D1 in Fig. 6.5 charges up the capacitor bank, denoted as C1, providing a positive DC input voltage to the positive boost regulator, which is composed by L1, Q1, D3, and C3. The rectifier D2 charges up another capacitor bank, denoted as C2, providing a negative DC input voltage to the negative boost regulator which is composed by L2, Q2, D4, and C4. The capacitor banks C1 and C2 are the major energy storage elements. C3 and C4 are the output filtering capacitors of the boost regulators, having much smaller capacitance compared with C1 and C2. The boost regulators ensure that the high-tension DC voltages supplied to the AC inverter remain constant during the entire voltage sag procedure. Q3, Q4, D5, D6, L3, and C5 form a half-bridge Inverter.

In the microcomputer controller shown in Fig. 6.5, there is an analog-to-digital converter to sample the AC mains voltage regularly. The digital output of the analog-to-digital converter is compared with a sine-wave look-up

table in the microcomputer. When the comparison indicates that the AC mains voltage is below a preset percentage of the nominal input voltage, the microcomputer controller will send out a control signal to disconnect the load from the AC mains. At the same time, a PWM signal is generated to drive the switching transistors Q3 and Q4 of the inverter. The AC inverter is thus started to provide back-up power to the load. The phase of the AC inverter output is synchronized to that of the AC mains. The practical construction of a 120Vac 1kVA 50/60Hz voltage sag compensator is shown in Fig. 6.6.

Key components of 120Vac 1KVA voltage sag compensator are shown as follows:

D1,D2 = GBPC3508W(35A,800V)
C1 = 13200uF/200V
C2 = 13200uF/200V
L1 = 100uH
L2 = 100uH
Q1 = IXFX32N50(500V,32A) x 2
Q2 = IXFX32N50(500V,32A) x 2
D3 = MUR1560(15A,600V) x2
D4 = MUR1560(15A,600V) x2
C3 = 2200uF/200V
C4 = 2200uF/200V
Q3 = IXFX32N50(500V,32A) x 2
Q4 = IXFX32N50(500V,32A) x 2
D5 = MUR1560(15A,600V) x2
D6 = MUR1560(15A,600V) x2
L3 = 400uH
C5 = 20uF/250Vac
SW = K10P-11D15-110 (15A,120VAC) DC coil Relay

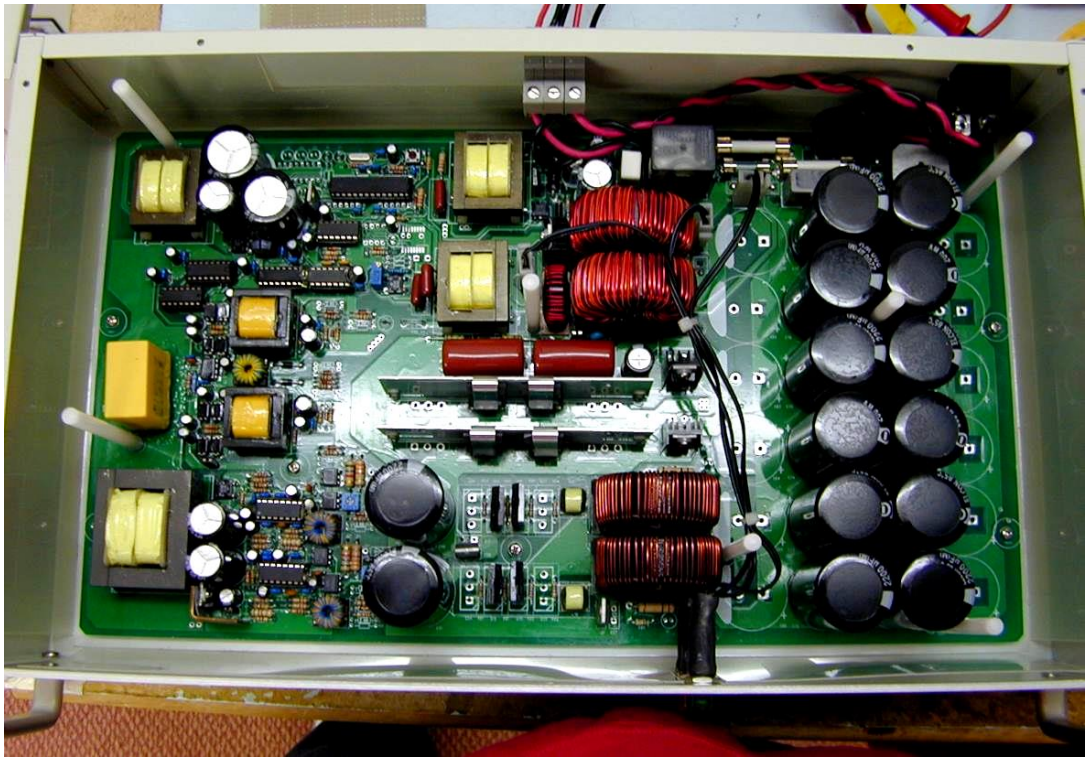


Fig. 6.6 Practical construction of a 120Vac 1kVA 50/60Hz voltage sag compensator

## 6.3 Test procedures and test results

Some tests are undergone to evaluate the usability of voltage sag compensator.

### 6.3.1 Test equipment and test procedures

The 1kVA 120Vac 50/60Hz voltage sag compensator is tested under different loading conditions to prove the functionality with different loads.

Test equipment:

| | | |
|---|---|---|
| A) | 1:100 voltage probe | 2 |
| B) | Digital signal oscilloscope (DSO) Tektronix TDS1002B | 1 |
| C) | Isolation transformer 50kVA | 1 |
| D) | Autotransformer 10kVA | 1 |
| E) | Resistive dummy loads with different values | |

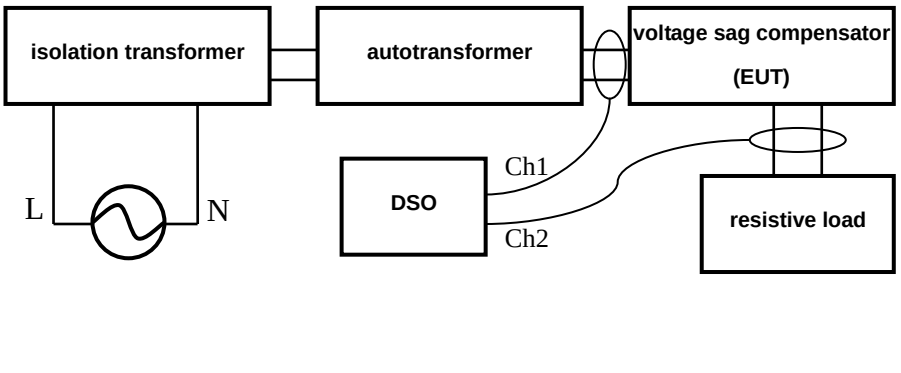



Fig. 6.7 Connections of test equipment

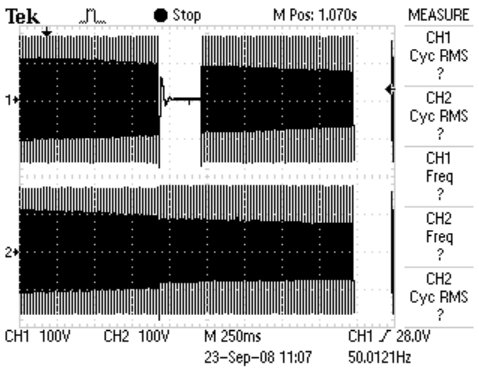
Fig. 6.7 shows the testing arrangement. For safety reasons, an isolation transformer is used to isolate the voltage sag compensator from the AC mains during testing.

### 6.3.2 Voltage waveforms of compensator under different loading conditions

Fig. 6.8 shows a sample of the input and the output voltage waveforms of the voltage sag compensator during a voltage sag event when the loading current is zero. Fig. 6.9 shows the expanded waveforms at the start of the voltage sag. Fig. 6.10 shows the expanded waveforms during compensation. Fig. 6.11 shows the waveforms at the end of compensation (for a loading current of 0A).

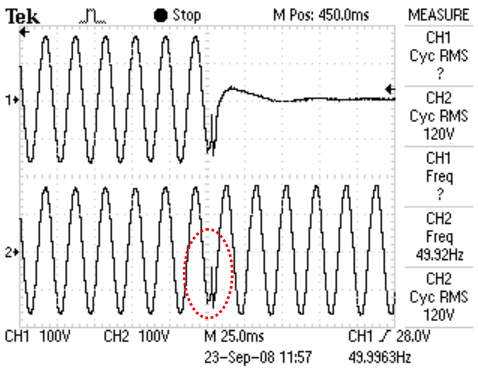
Similarly, Fig. 6.12 shows a sample of the input and the output voltage waveforms of the voltage sag compensator during a voltage sag event when the loading current is 7.08A. Fig. 6.13 shows the expanded waveforms at the start of the voltage sag. Fig. 6.14 shows the expanded waveforms during compensation. Fig. 6.15 shows the waveforms at the end of compensation (for current of 7.08A).

**Waveform of VSC under 0A loading current**



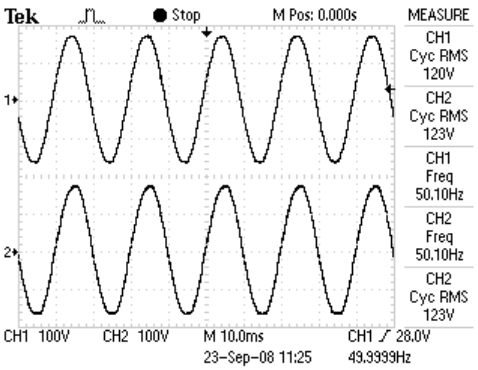

Ch1: Input of VSC Ch2: Output of VSC

Fig. 6.8 Input and output voltage waveforms (0A loading)



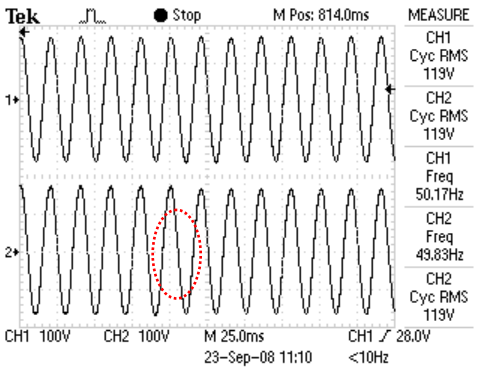

Ch1: Input of VSC Ch2: Output of VSC

Fig. 6.9 Expanded waveforms at the start of voltage sag(0A loading)



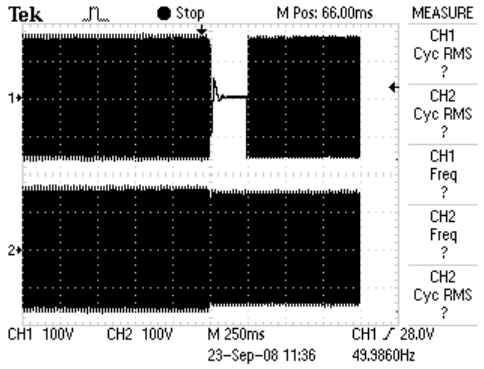
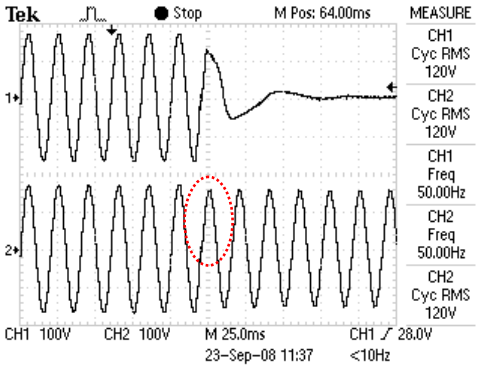
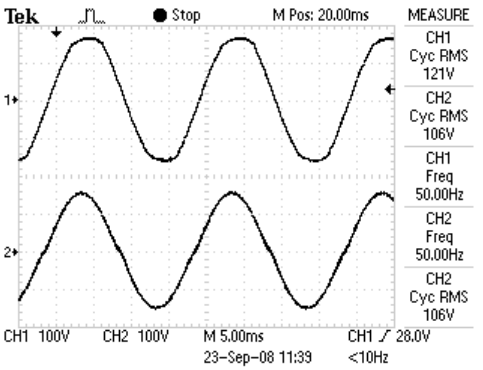
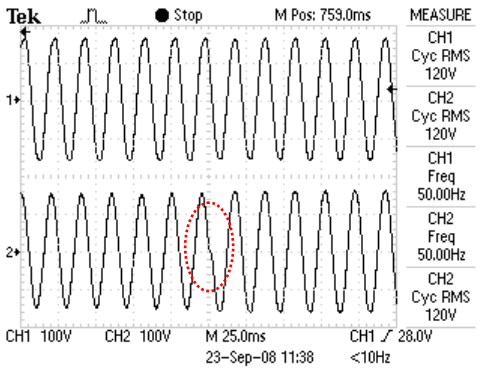

Ch1: Input of VSC Ch2: Output of VSC

Fig. 6.10 Expanded input and output voltage waveforms during compensation (0A loading)




Ch1: Input of VSC Ch2: Output of VSC

Fig. 6.11 Waveforms at the end of compensation (0A loading)

<table>
<tr><th colspan="2">Waveform of VSC under 7.08A loading current</th></tr>
<tr><td> 
</td><td> 
</td></tr>
<tr><td>Ch1: Input of VSC Ch2: Output of VSC</td><td>Ch1: Input of VSC Ch2: Output of VSC</td></tr>
<tr><td>Fig. 6.12 Input and output voltage waveforms (7.08A loading)</td><td>Fig. 6.13 Expanded waveforms at the start of voltage sag(7.08A loading)</td></tr>
<tr><td> 
</td><td> 
</td></tr>
<tr><td>Ch1: Input of VSC Ch2: Output of VSC</td><td>Ch1: Input of VSC Ch2: Output of VSC</td></tr>
<tr><td>Fig. 6.14 Expanded input and output voltage waveforms during compensation (7.08A loading)</td><td>Fig. 6.15 Waveforms at the end of compensation (7.08A loading)</td></tr>
</table>

### 6.3.3 Ride-through time

Fig. 6.16 shows the input and the output voltage waveforms of the voltage sag compensator when the input AC mains are turned off. The test loading current is 2.1A (loading power = 250VA). It is found that the ride through time is about 1.4 seconds. This test shows that the sag compensator can support a full load with load power factor 0.25 (i.e.250VA) for more than 1 second.

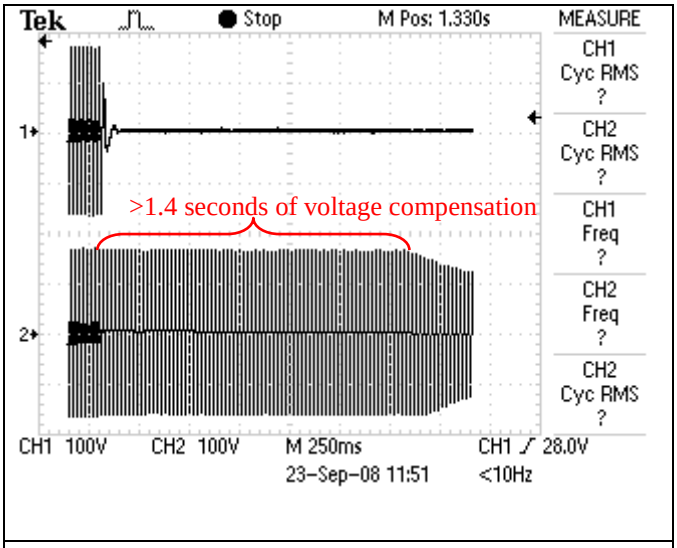



Fig. 6.16 Ride-through time under 2.1A loading

### 6.3.4 Performance of relays/contactors during voltage sag

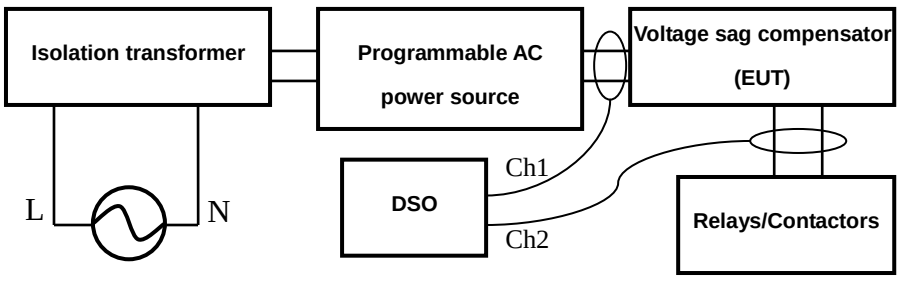



Fig. 6.17 Testing of relays/contactors

The relays/contactors tested include the following:

A) Contactor 1 – YS1N-12FA120 from Idec corporation Coil Rating: 120Vac 50/60Hz
B) Relay 1 – 8501KP12V20 from SQUARE D, Coil Rating: 120Vac 50/60Hz
C) Relay 2 – 8501KU12V20 from SQUARE D, Coil Rating: 120Vac 50/60Hz
D) Resistor 1 - 30 ohm / 1kWatt resistor

Test procedures:

The test equipment is connected as illustrated in Fig. 6.17. By using programmable AC power source with nominal voltage of 120Vac to simulate the voltage sag, the sags are with different voltage started at $0^o$, $45^o$ and $90^o$. The loading (Contactor 1, Relay 1 and Relay 2) connected at compensator's output are monitored by a simple chattering detection circuit at the same time.

Some samples of the input and the output voltage waveforms of the voltage sag compensator, which are used for testing, are shown in Fig. 6.18 through Fig. 6.23. Chattering does not occur in different loads. The results indicate that equipment working with the voltage sag compensator meets the SEMI-F47 requirements. The starting point of voltage sag ($0^o$, $45^o$ and $90^o$) does not affect the operation of the relays/contactors.

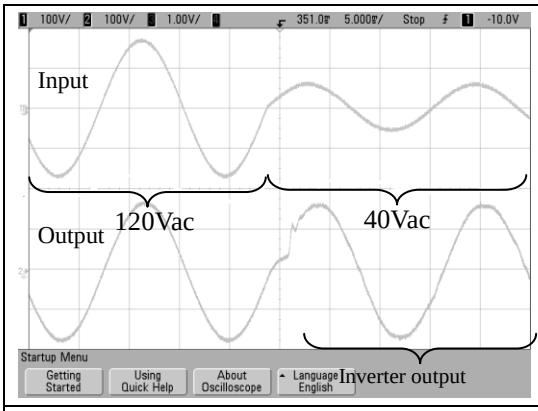



Fig. 6.18 Voltage sag down to 40Vac at $0^o$ 50Hz

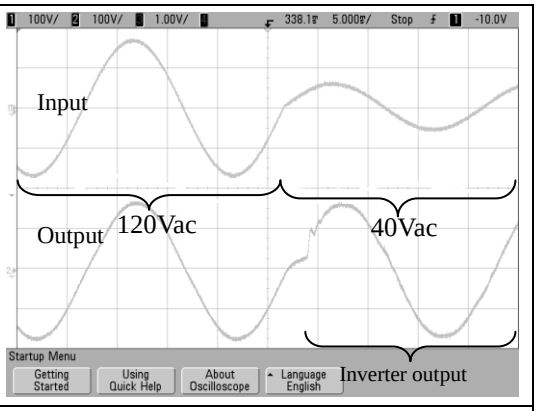



Fig. 6.19 Voltage sag down to 40Vac at $0^o$ 60Hz

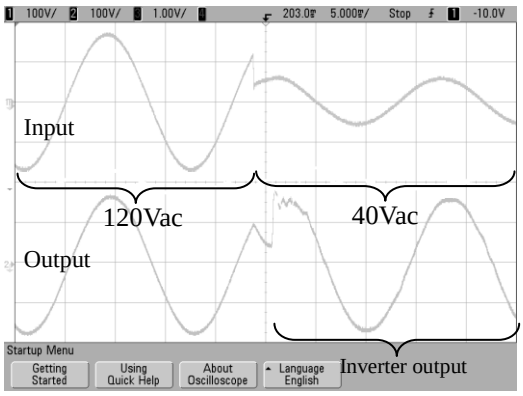



Fig. 6.20 Voltage sag down to 40Vac at 45° 50Hz

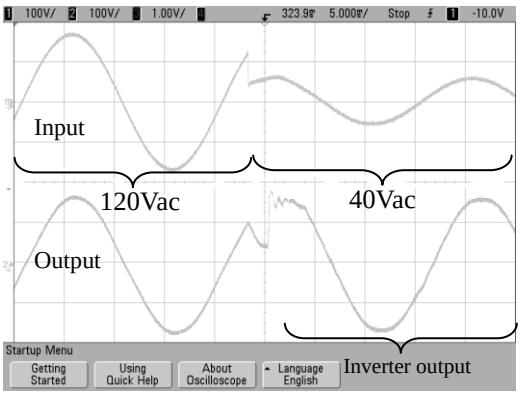



Fig. 6.21 Voltage sag down to 40Vac at 45° 60Hz

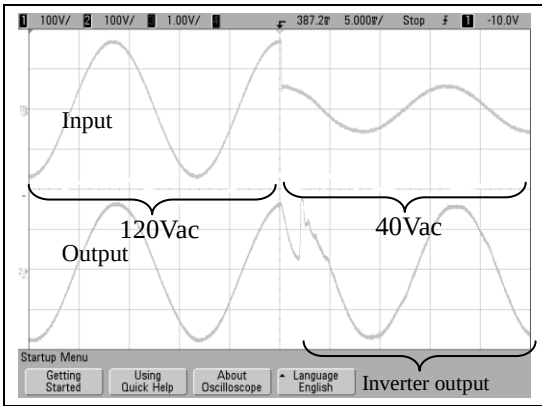



Fig. 6.22 Voltage sag down to 40Vac at 90° 50Hz

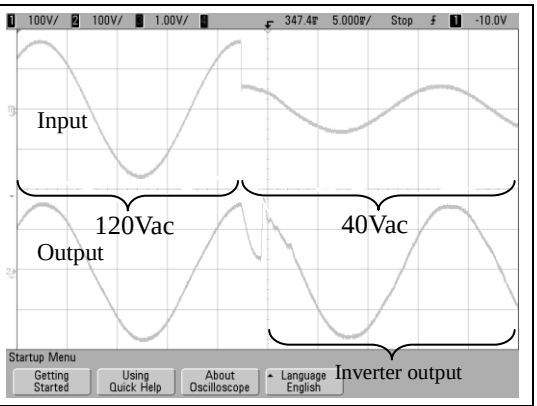



Fig. 6.23 Voltage sag down to 40Vac at 90° 60Hz

## 6.3.5 Discussions

Thorough testing of the 120Vac 1kVA voltage sag compensator indicates that the compensator can operate well under various input and loading conditions. The output waveform is a smooth sinusoidal wave. The ride through time for full load at power factor 0.25 is found to be about 1.4 second. The threshold voltage setting and the compensation time setting are working well for different sensitivity loads. The intelligent frequency auto-sensing and the under-voltage protection are useful features for end users. The relays/contactors are protected by the sag compensator. These results show that this compensator can meet the SEMI-F47 specification to solve the most of the voltage sag problems in semiconductor industry.

## 6.4 Reliability test

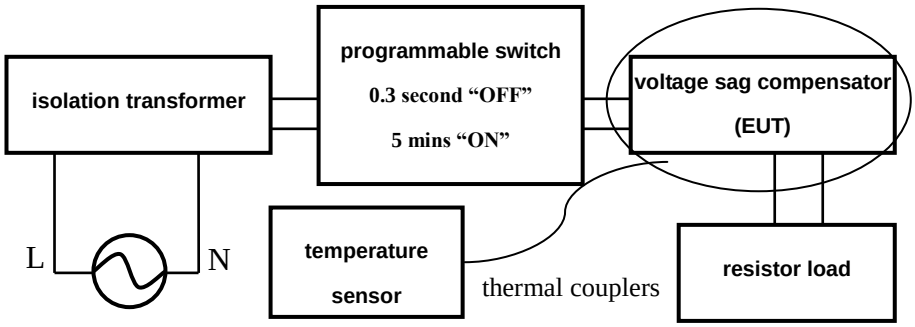



Fig. 6.24 On/Off reliability test arrangement.

The arrangement shown in Fig. 6.24 is set up to test the reliability of the voltage sag compensator. The programmable switch in Fig. 6.24 is programmed to a repetitive 5-minute ON 0.3-second OFF switching cycle. The output loading is 1kVA full load. The testing results are shown in Table 7, which indicate that the voltage sag compensator can operate in 40$^{o}$C~50$^{o}$C environmental temperatures without any error or malfunction.

Table 7 Temperature variations of components in on/off reliability test

| Time | NTC ($^oC$) | Relay ($^oC$) | MOSFET($^oC$) | Environmental in case ($^oC$) | Electronic incubator($^oC$) |
|---|---|---|---|---|---|
| 00:00 | 47 | 50 | 38 | 40 | 40 |
| 00:20 | 57 | 55 | 44 | 44 | 45 |
| 00:40 | 63 | 60 | 49 | 46 | 46 |
| 01:00 | 65 | 62 | 51 | 46 | 46 |
| 01:20 | 68 | 63 | 52 | 48 | 47 |
| 01:40 | 68 | 62 | 50 | 48 | 48 |
| 01:55 | 67 | 61 | 51 | 48 | 48 |
| 03:00 | 54 | 62 | 52 | 48 | 48 |
| 03:20 | 64 | 66 | 54 | 48 | 48 |
| 03:40 | 71 | 68 | 56 | 49 | 49 |
| 04:00 | 73 | 68 | 57 | 49 | 49 |
| 04:20 | 75 | 67 | 58 | 50 | 49 |
| 04:40 | 75 | 67 | 58 | 50 | 50 |

*NTC, Relay, MOSFET are key components dissipating power during compensator working.

## 6.5 Mechanical features

The mechanical design of the voltage sag compensator is based on the widely used 19 inch rack standard. The mechanical drawings are shown in ***Appendix D***.

The user interface dip switches are placed at the rear panel as shown in Fig. 6.25, which enables end users to select suitable threshold compensation voltage and compensation time. The terminal block with cover is placed at the centre of the panel.

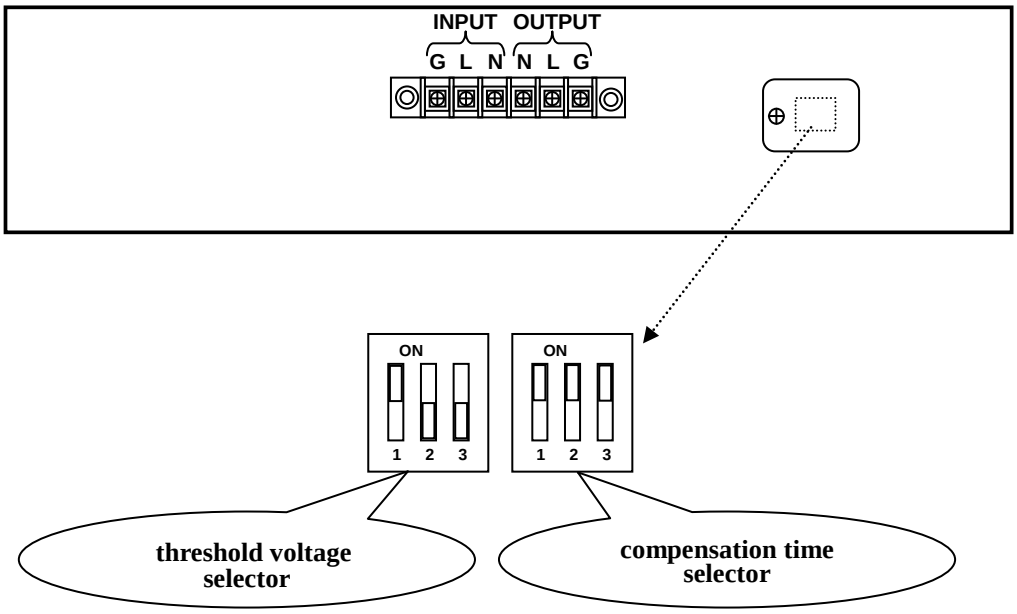



Fig. 6.25 Rear panel of voltage sag compensator

In the front panel, displayed in Fig. 6.26, there are three neon lamp indicators. These are indicating the mode of operation of the voltage sag compensator. The functions of the indicators are shown in Table 8. The advantage of using a neon lamp is that a neon lamp, powered by AC voltage, can directly show the real status of the AC input and output.

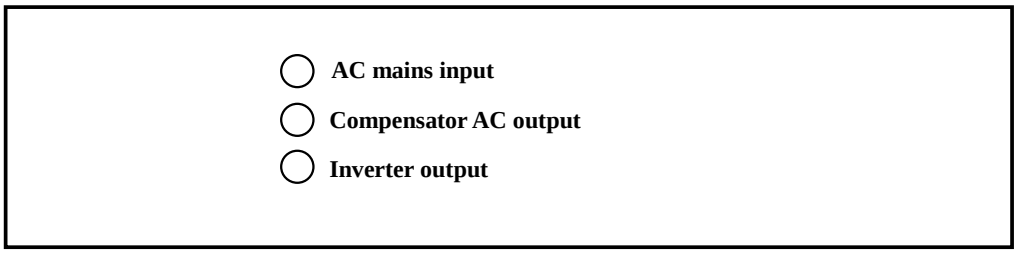



Fig. 6.26 Front panel of voltage sag compensator

Table 8 Neon lamp inductors of voltage sag compensator

| **Neon Lamp Label** | **Color** | **Description** |
|---|---|---|
| AC Mains Input | Green(at the top) | Power is on. |
| Compensator AC output | Amber(in the middle) | AC mains is available to the load. |
| Inverter output | Red(at the bottom) | 1. The AC Inverter is activated and is regenerating AC output to drive the load<br><br>2. The bulk capacitor bank is discharging. |

## 6.6 Performance comparisons

The following is a table that compares the performance of the voltage sag compensator constructed (DSC) with those of other designs from previous research [48]. A column of the parallel type voltage sag compensator is added into the Table 9. The table summarizes the percentage of total power quality events, which are classified as spikes and surges, depth of voltage sag and duration of voltage sag. (1) Spike suppressor can provide only a small range of protection to spikes and surges, it cannot protect the load under voltage sag. (2) Voltage regulator can protect DC load with sag to 80%, because there is capacitance storage at the input. Additionally, some universal input voltage regulators can work at low input voltage level. But, voltage regulator cannot apply in AC load. (3) Transformer-less DSC[47] and parallel type voltage sag compensator have similar abilities on voltage sag immunity. They could solve approximately 92% of total power quality events without using batteries as backup, which is suitable for the semiconductor industry's applications. The main advantage of a parallel type voltage sag compensator is that it is able to tolerate open-circuit faults in AC input during sag period. (4) UPS can solve most of the power quality problems. It provides decent emergency power to load and protect equipment, but the batteries in UPS limit the applications in the semiconductor industry.

The result points out that the parallel type voltage sag compensator constructed in this project has more advantages than those of other designs, provided that the voltage sag is not excessively long.

Table 9 Protection capability of different designs [48]

| Type of event | % of total power quality events | Spike suppressor | Voltage regulator | Transformer-less DSC[47] | UPS systems | **Parallel type voltage sag compensator** |
|---|---|---|---|---|---|---|
| Spikes & surges | 5% | Protected | Protected | Protected | Protected | **Protected** |
| Sag to 80% | 35% | No | Protected | Protected | Protected | **Protected** |
| Sag from 50-80% | 45% | No | No | Protected | Protected | **Protected** |
| Interruption 0-0.15 sec | 7% | No | No | Protected | Protected | **Protected** |
| Interruption 0.15-500 sec | 4% | No | No | No | Protected | **Partially protected (up to a few seconds)** |
| >500 sec outage | 4% | No | No | No | No | **No** |
| % of total power quality events solved | 100% | 5% | 40% | 92% | 96% | **~92%** |
| kVA range | -- | 1-1000KVA | 1-200kVA | 1-2000kVA | 0.2-1000kVA | **1kVA (extendable)** |
| Able to tolerate open-circuit faults in AC input during sag period | -- | No | Yes | No | Yes | **Yes** |
| Operate without battery | -- | Yes | Yes | Yes | No | **Yes** |

## 6.7 Summary

A 120Vac 50Hz/60Hz 1kVA voltage sag compensator has been constructed and thoroughly tested. The results have demonstrated that the compensator can meet the specification listed in chapter 4 and pass SEMI F47 requirement on voltage sag immunity for the semiconductor industry. The reliability ON/OFF test indicates that the compensator can operate under high temperatures.

# Chapter 7: Conclusions and future development

## 7.1 Contributions of thesis

This thesis examined the power quality problems caused by the AC mains voltage sags, which can cause huge economic loss in industrial plants. The characteristics of the voltage sags and the existing methods to minimize their adverse effects were reviewed. The details of SEMI F47 standard for voltage sag immunity were described.

A new parallel type AC voltage sag compensator is proposed. Both the hardware and software designs of the compensator were discussed. A practical and intelligent 120Vac 50Hz/60Hz 1kVA AC voltage sag compensator is constructed for industrial applications. The compensator was thoroughly tested and its performance fully evaluated. It has been proven that the new voltage sag compensator is as reliable and practical as a commercial product. Performance measurements indicate that the compensator meets the SEMI F47 requirements. It is expected that the compensator is capable of solving the majority of the problems caused by the voltage sags in the semiconductor industry. The component counts and the cost of parallel type AC voltage sag compensator are similar to existing products like: DSC, DVR. The price is depending on the power rating of compensator.

## 7.2 Suggestions for future development

The following are some suggestions for future development:

1) Based on the 1kVA 120Vac 50Hz/60Hz AC voltage sag compensator constructed in this project, it is suggested that a 2kVA version of the compensator be developed. The modification required is to use a larger energy-storage capacitor bank and higher current-rating power MOSFETs in the AC Inverter.

2) A 220/230Vac version of the voltage sag compensator should be developed to match the needs in areas with 220/230Vac mains.

3) A data recorder could be added to capture the data related to the voltage sag events. For example, the date and the time of occurrence, the sag depth and the duration, whether the compensation is successful or not, etc. Such datum should be useful for the analysis of the voltage sag events on site and for developing further strategies to deal with future voltage sag events.

4) The performance of series type and parallel type voltage sag compensator can be further compared by using different voltage sag with different voltage level, phase angle and sag period.

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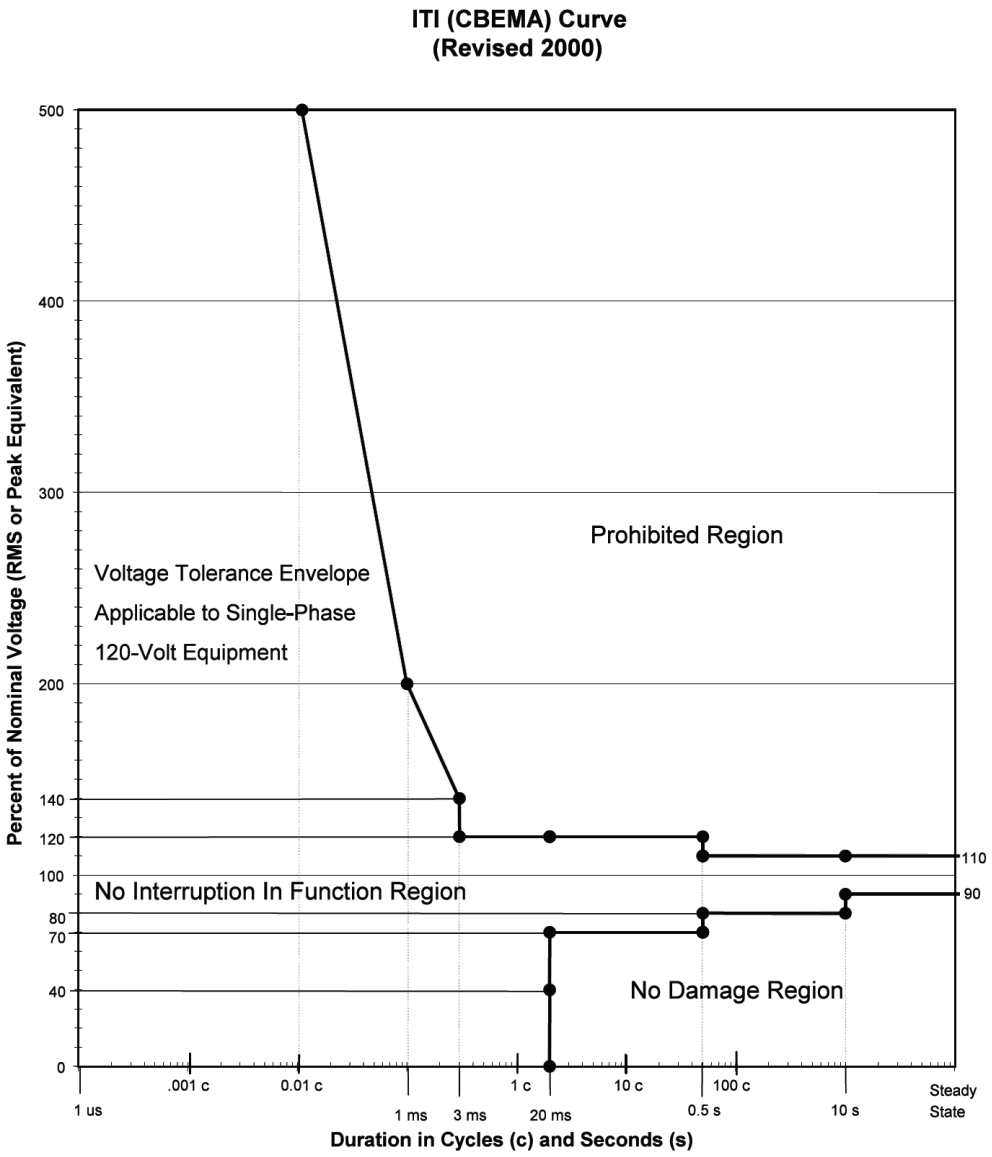
# Appendix A CBEMA curve

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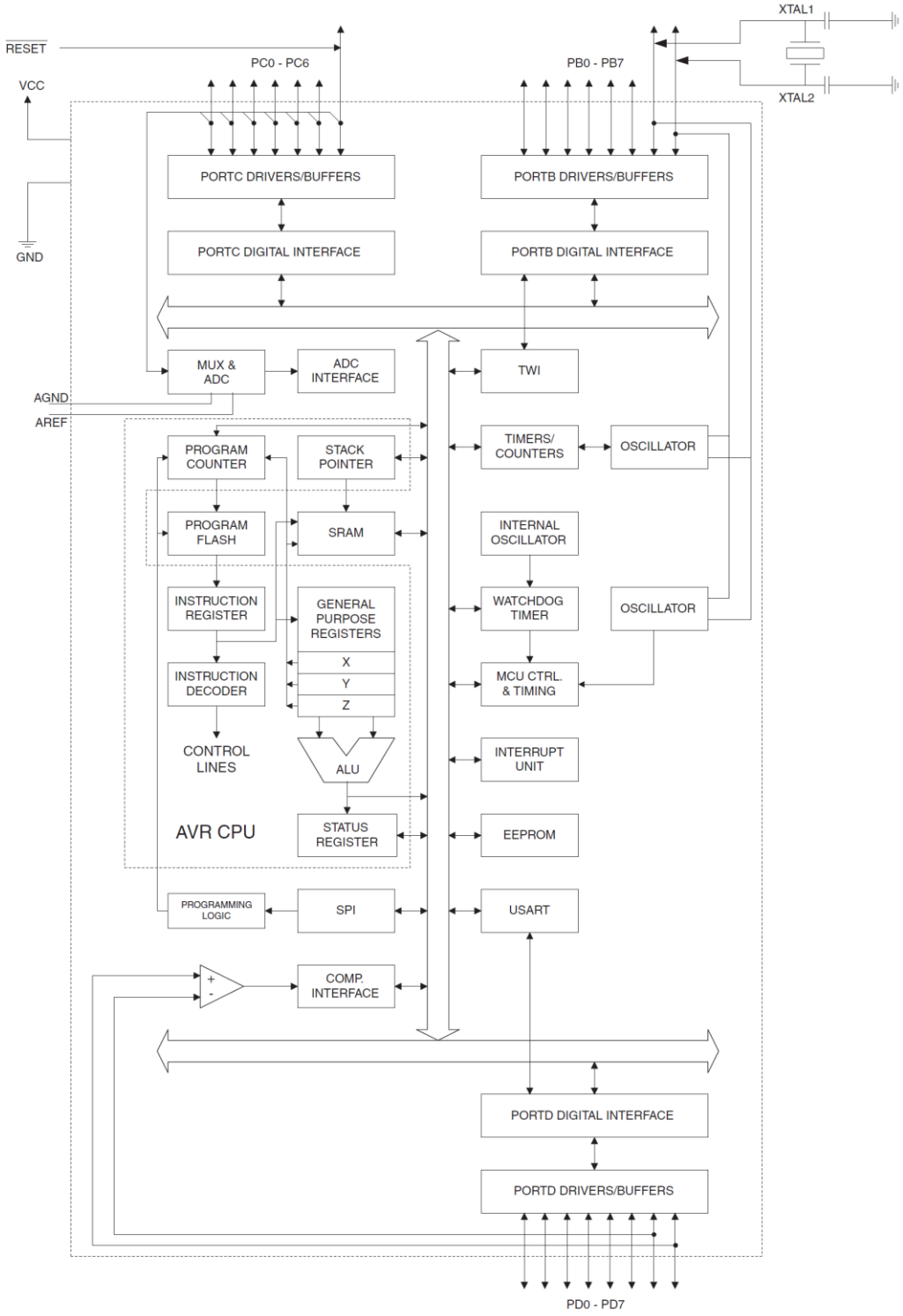
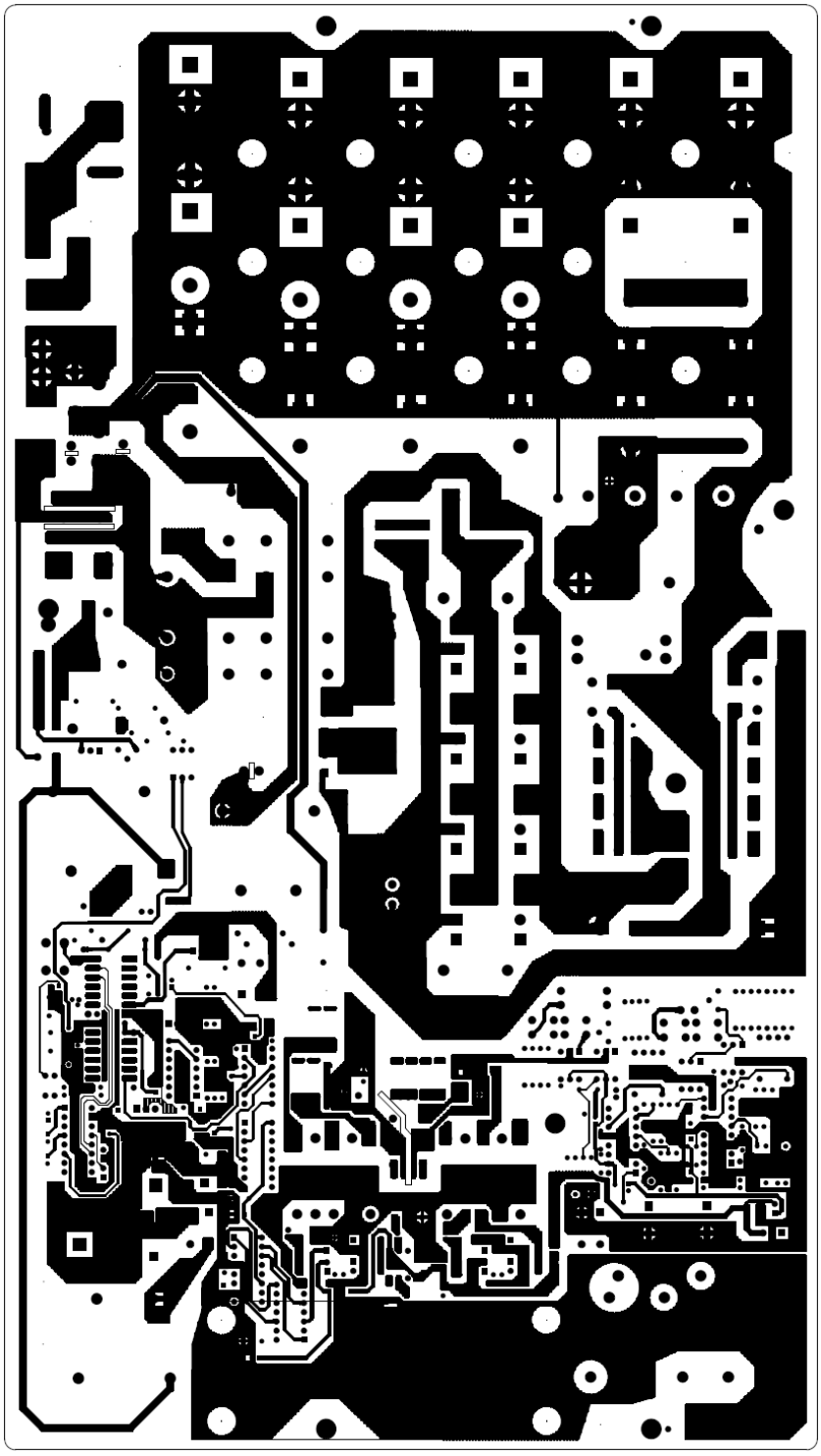
## Appendix B Block diagram of Atmage8

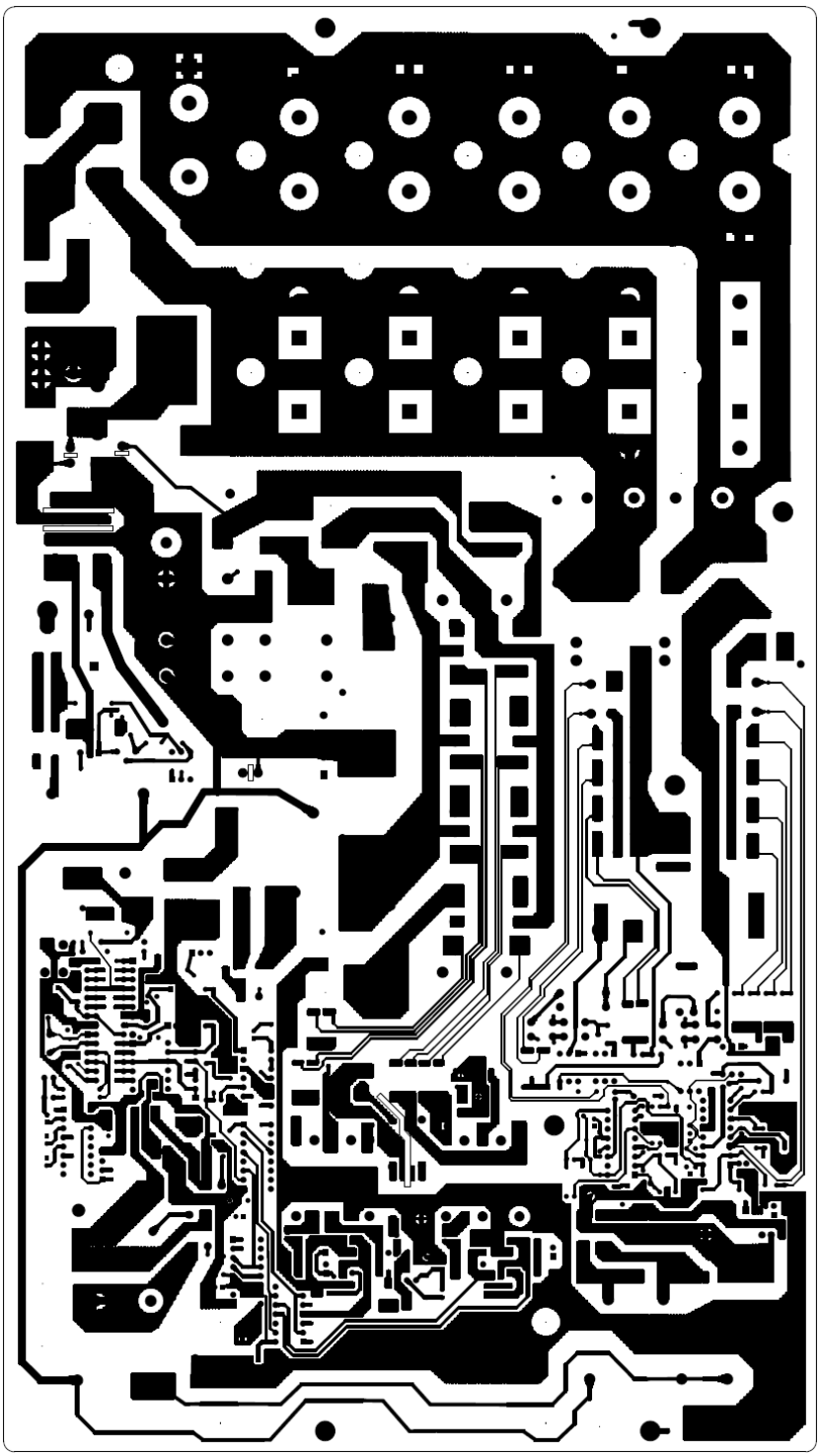


## Appendix C Diagram of PCB layout



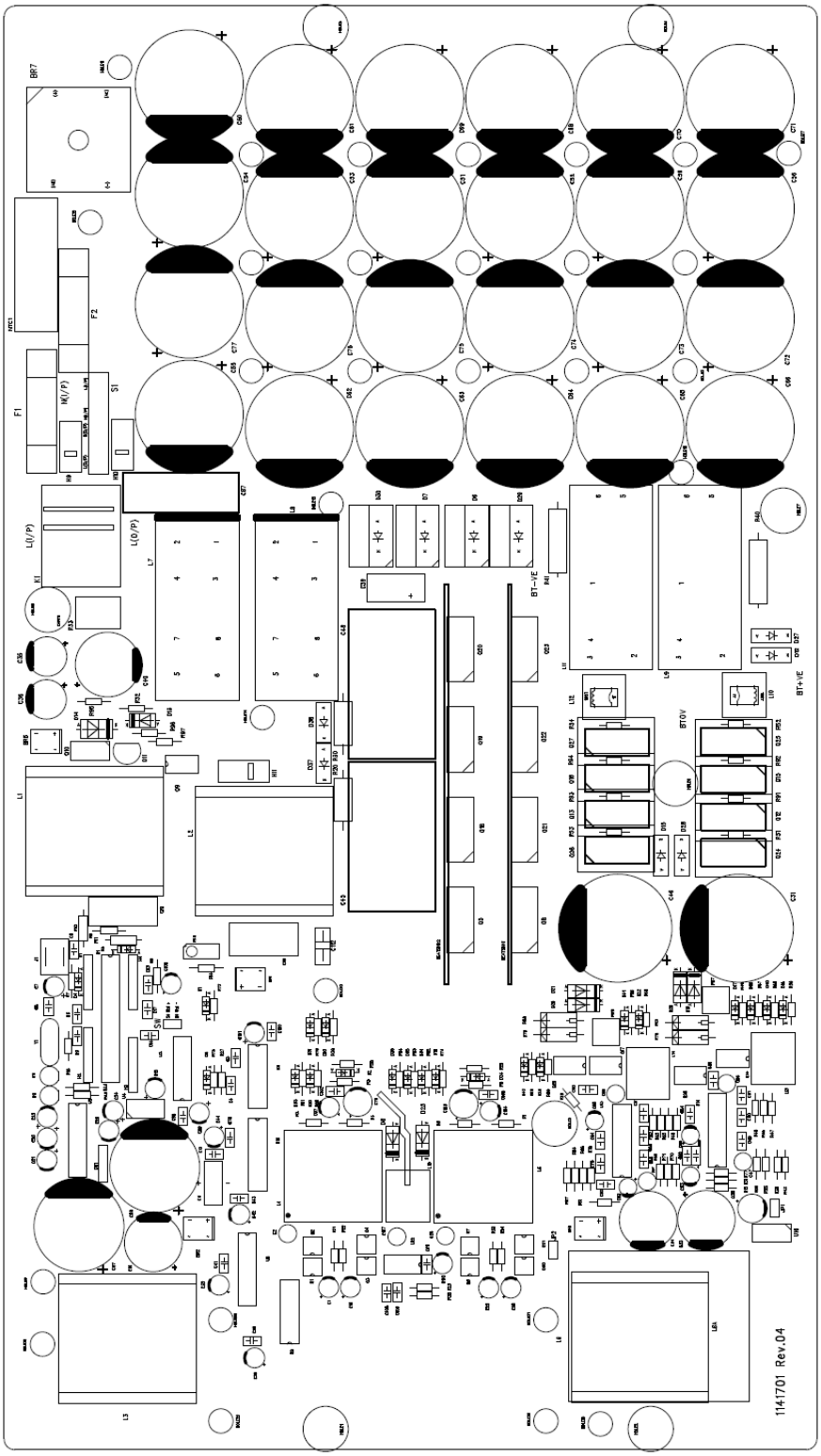
Top layer (non-scaled)

*Appendix C*



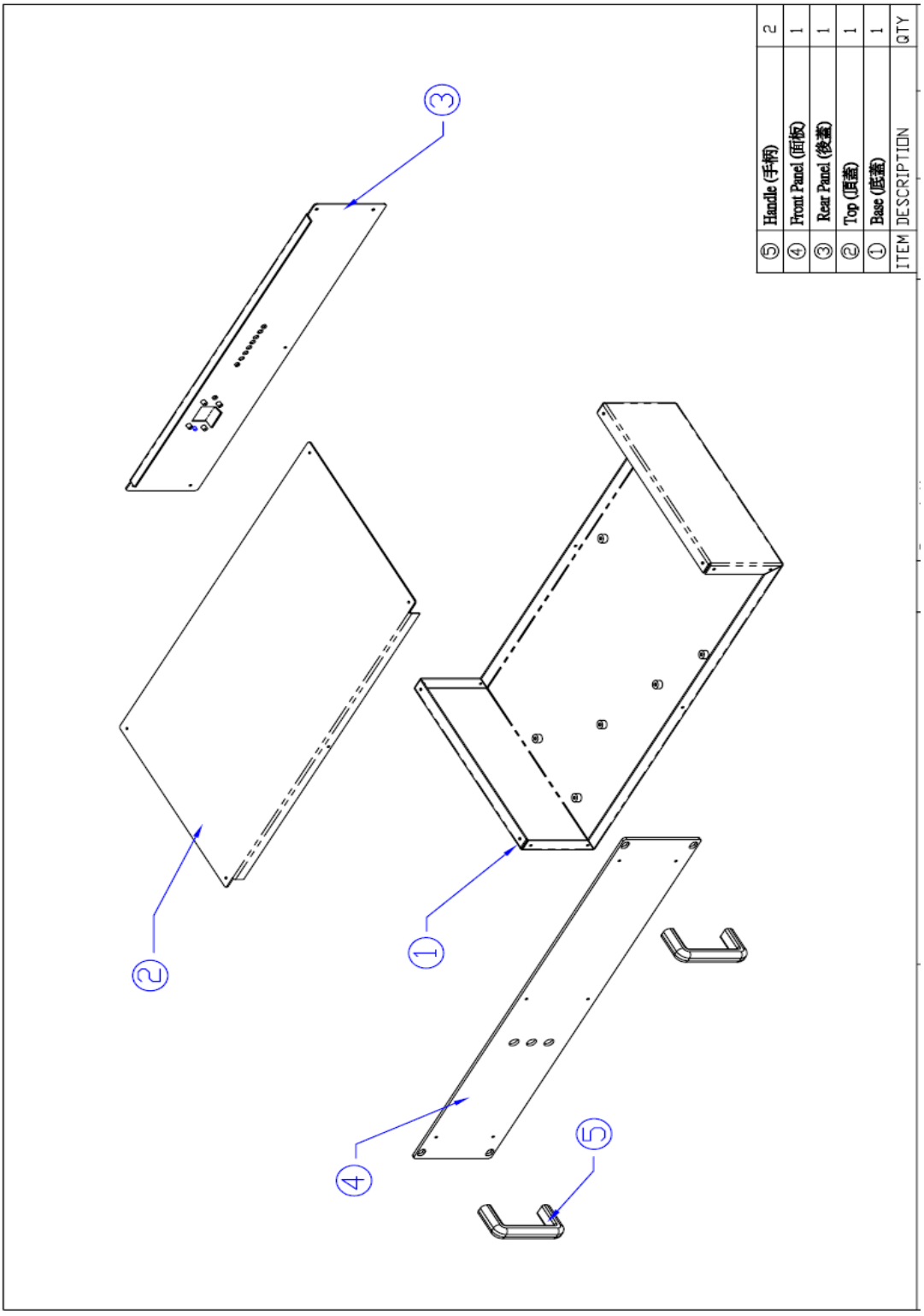
Bottom layer(non-scaled)

*Appendix C*

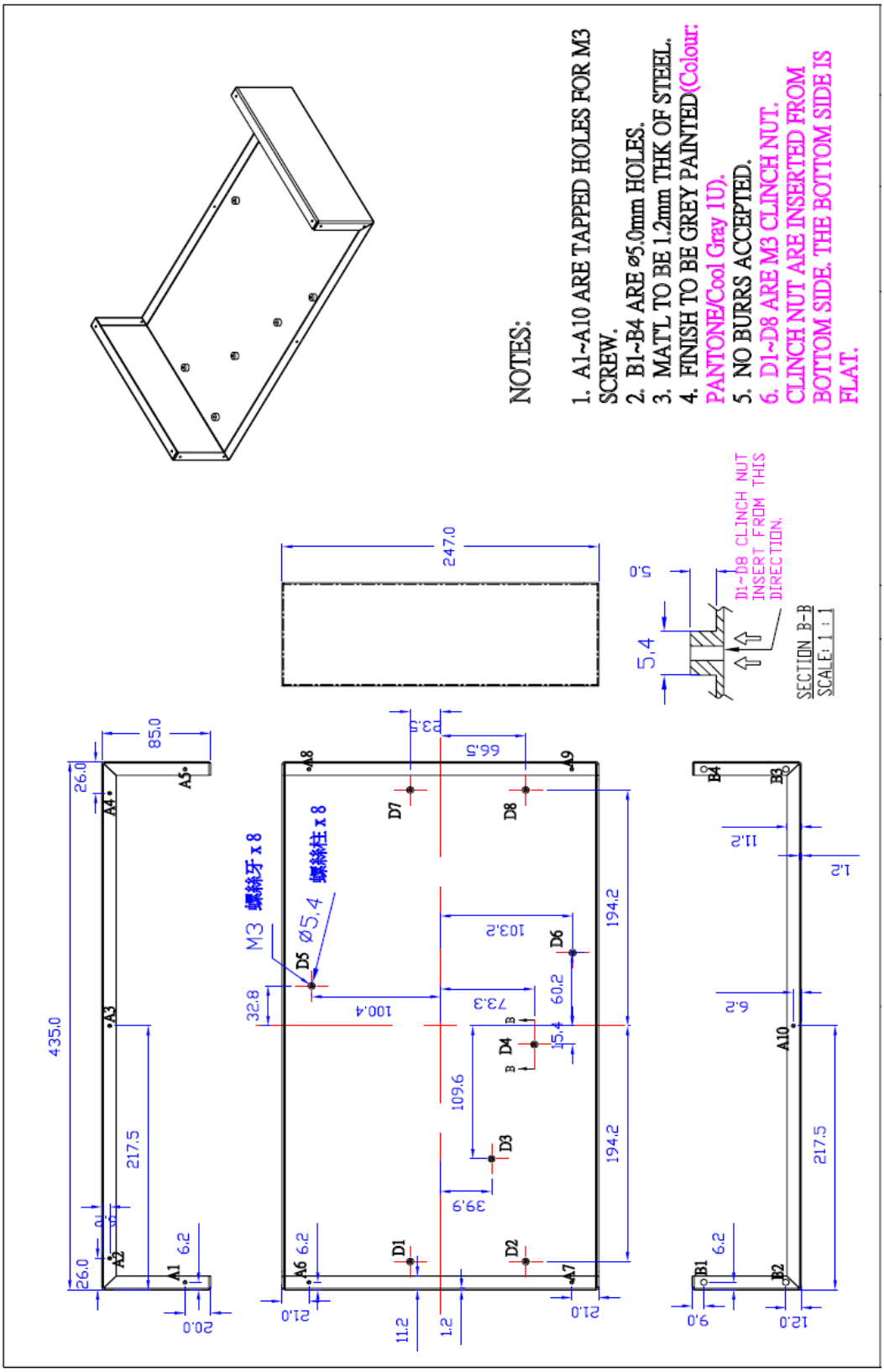



Top placement (non-scaled)

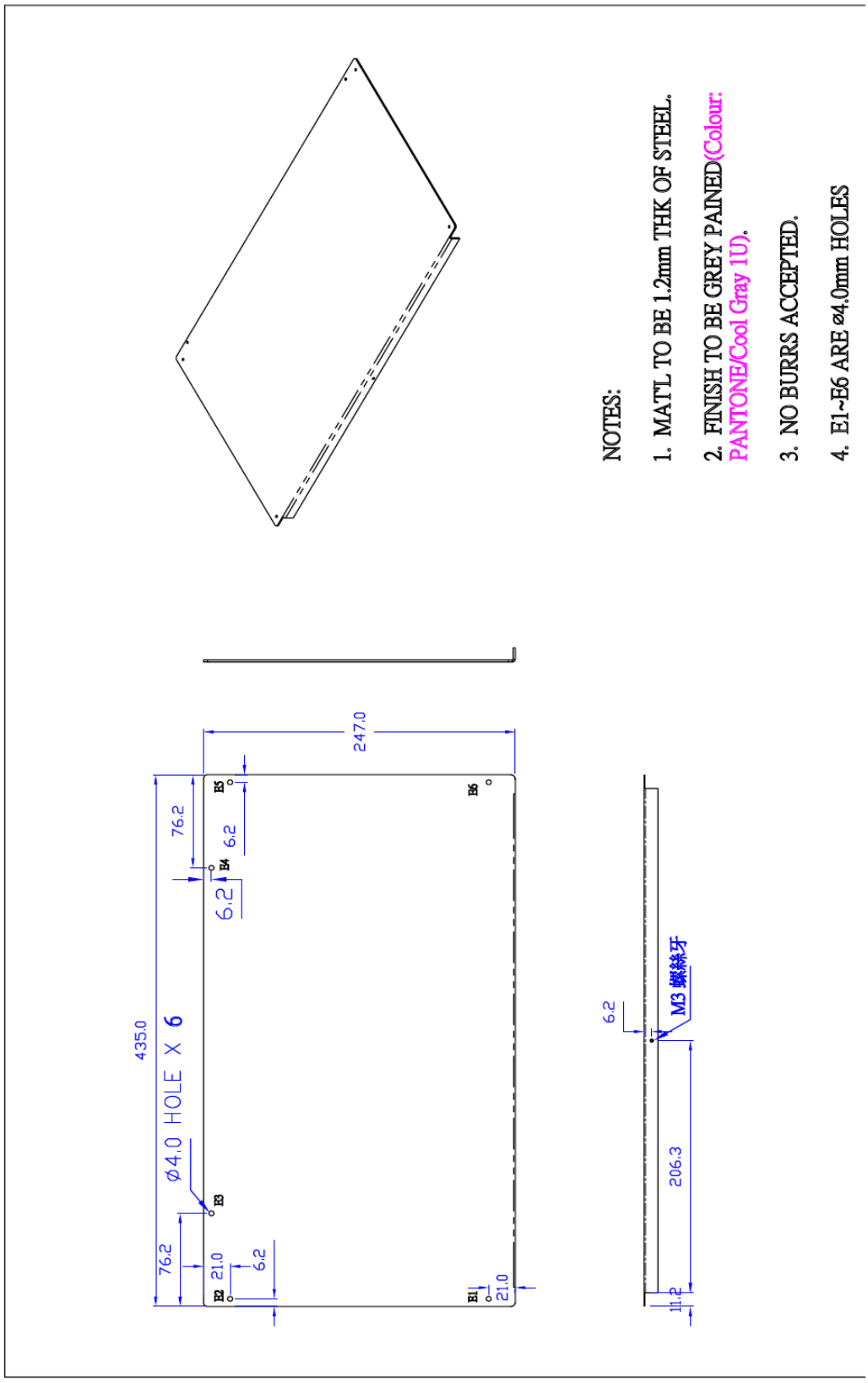
## Appendix D Mechanical drawing of 1kVA 19” rack



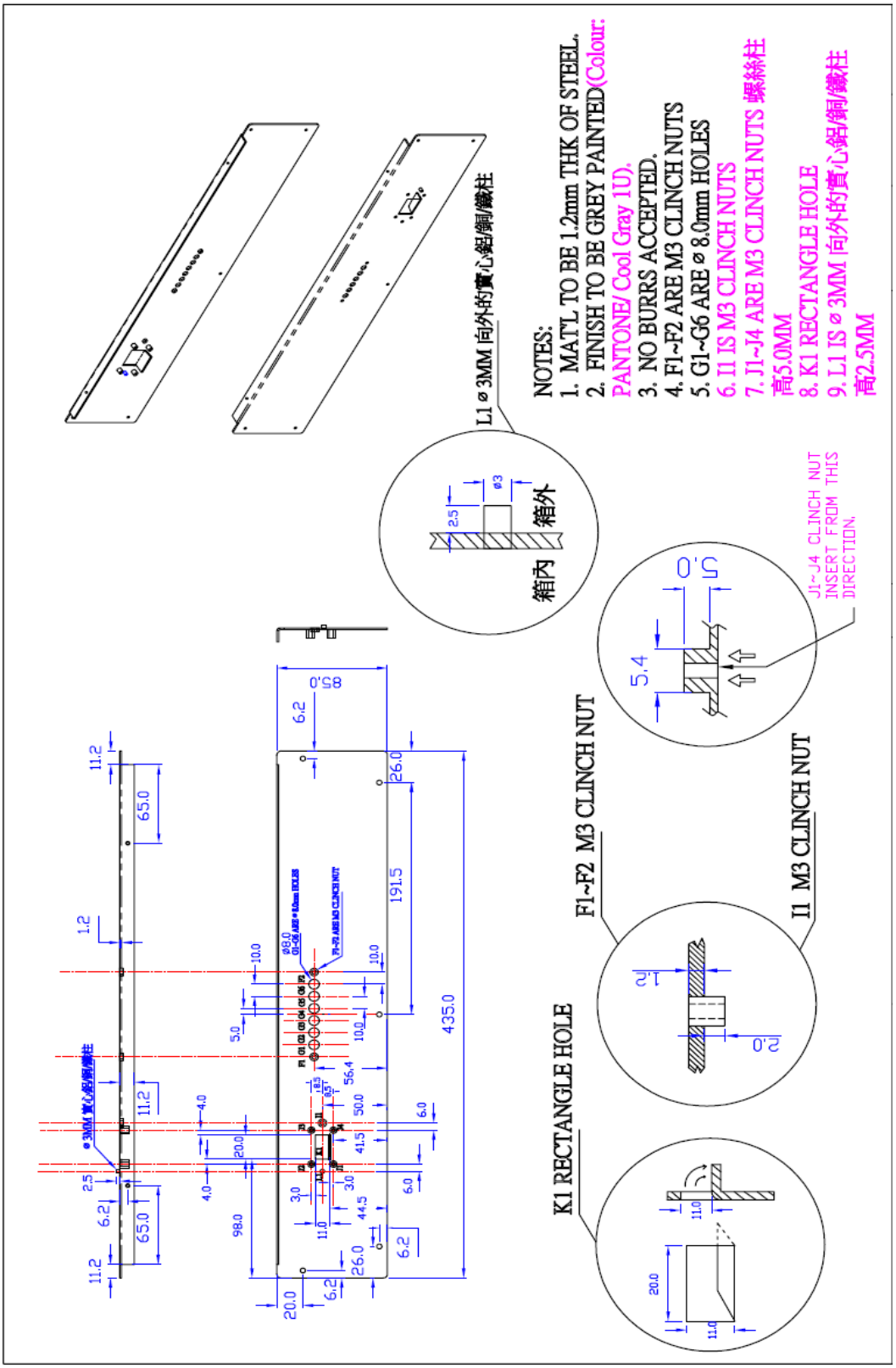
*Appendix D*


NOTES:
1. A1~A10 ARE TAPPED HOLES FOR M3 SCREW.
2. B1~B4 ARE ø5.0mm HOLES.
3. MATL TO BE 1.2mm THK OF STEEL.
4. FINISH TO BE GREY PAINTED(Colour: PANTONE/Cool Gray 1U).
5. NO BURRS ACCEPTED.
6. D1~D8 ARE M3 CLINCH NUT. CLINCH NUT ARE INSERTED FROM BOTTOM SIDE. THE BOTTOM SIDE IS FLAT.
247.0
D1~D8 CLINCH NUT INSERT FROM THIS DIRECTION.
5.0
5.4
SECTION B-B
SCALE: 1 : 1
M3 螺絲牙 x 8
Ø5.4 螺絲柱 x 8
435.0
85.0
26.0
217.5
194.2
103.2
73.3
100.4
66.5
109.6
39.9
60.2
32.8
15.4
6.2
20.0
21.0
11.2
1.2
12.0
9.0
11.2
1.2
6.2

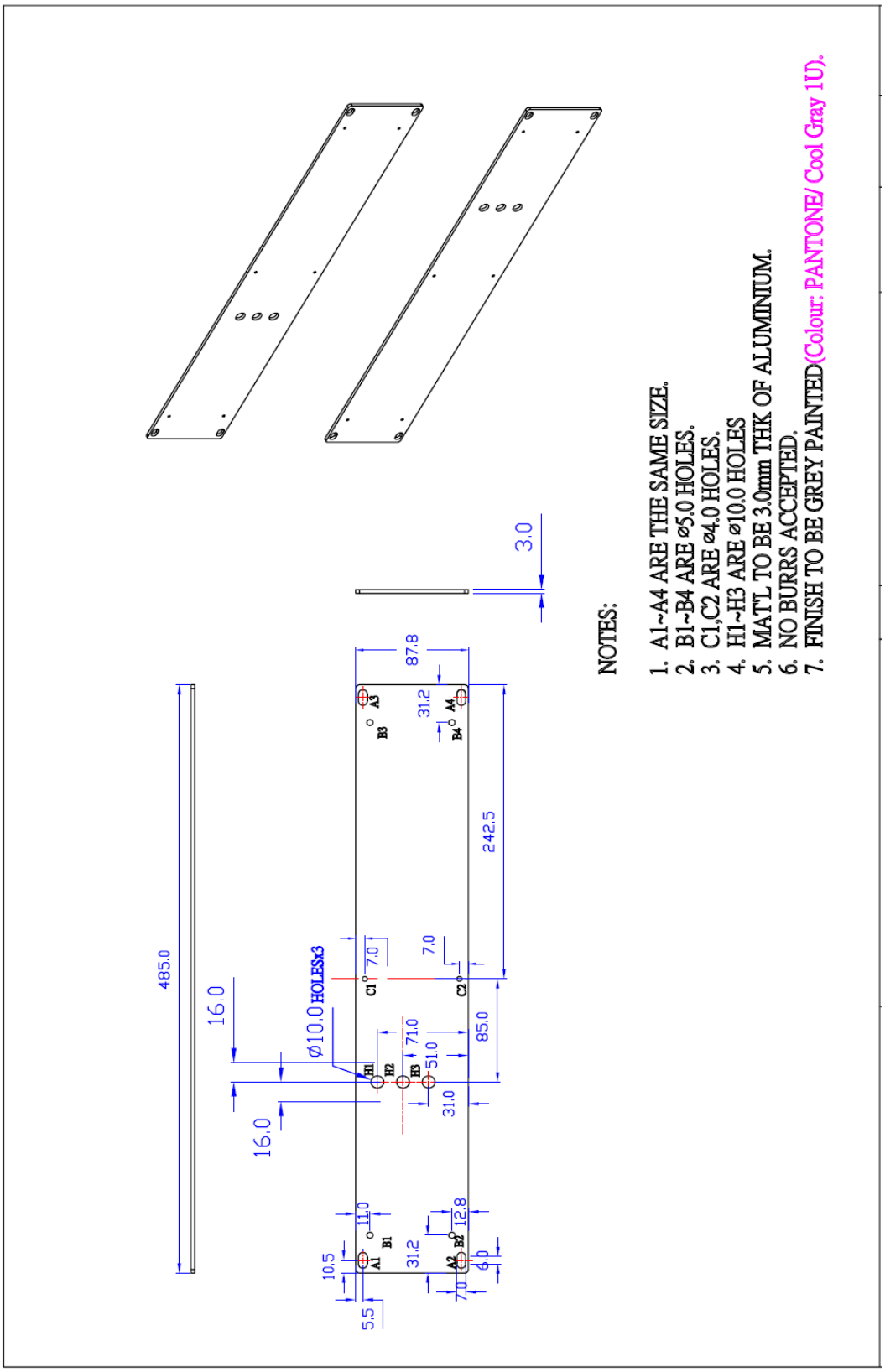
*Appendix D*


NOTES:
1. MATL TO BE 1.2mm THK OF STEEL.
2. FINISH TO BE GREY PAINED(Colour: PANTONE/Cool Gray 1U).
3. NO BURRS ACCEPTED.
4. E1~E6 ARE ø4.0mm HOLES
247.0
435.0
ø4.0 HOLE X 6
76.2
6.2
21.0
E1
E2
E3
E4
E5
E6
M3 攻絲牙
206.3
11.2

*Appendix D*


NOTES:
1. MATL TO BE 1.2mm THK OF STEEL.
2. FINISH TO BE GREY PAINTED(Colour: PANTONE/ Cool Gray 1U).
3. NO BURRS ACCEPTED.
4. F1~F2 ARE M3 CLINCH NUTS
5. G1~G6 ARE ⌀ 8.0mm HOLES
6. I1 IS M3 CLINCH NUTS
7. J1~J4 ARE M3 CLINCH NUTS 螺絲柱高5.0MM
8. K1 RECTANGLE HOLE
9. L1 IS ⌀ 3MM 向外的實心鋁/銅/鐵柱高2.5MM
L1 ⌀ 3MM 向外的實心鋁/銅/鐵柱
箱外
箱內
J1~J4 CLINCH NUT INSERT FROM THIS DIRECTION.
K1 RECTANGLE HOLE
F1~F2 M3 CLINCH NUT
I1 M3 CLINCH NUT
435.0
191.5
98.0
65.0

*Appendix D*


NOTES:
1. A1~A4 ARE THE SAME SIZE.
2. B1~B4 ARE ⌀5.0 HOLES.
3. C1,C2 ARE ⌀4.0 HOLES.
4. H1~H3 ARE ⌀10.0 HOLES
5. MATL TO BE 3.0mm THK OF ALUMINIUM.
6. NO BURRS ACCEPTED.
7. FINISH TO BE GREY PAINTED(Colour: PANTONE/ Cool Gray 1U).
3.0
87.8
31.2
242.5
485.0
16.0
Ø10.0 HOLESx3
7.0
71.0
51.0
85.0
31.0
16.0
11.0
12.8
31.2
10.5
5.5
6.0
A1
A2
A3
A4
B1
B2
B3
B4
C1
C2
H1
H2
H3

END