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THE DEPARTMENT OF APPLIED PHYSICS

NANOCRYSTALS EMBEDDED IN HfO_2-BASED DIELECTRICS AS CHARGE STORAGE NODES OF NANO-FLOATING GATE MEMORY

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CERTIFICATE OF ORIGINALITY

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Abstract

Nanocrystals (NC) embedded in dielectrics have attracted a great deal of attention recently because they can potentially be applied in nonvolatile, high-speed, high-density and low-power memory devices. Compared with conventional floating gate memories such as flash, a device composed of nanocrystals isolated by dielectrics benefits from a relatively low operating voltage, high endurance, fast write-erase speeds and better immunity to soft errors. The nanocrystal materials suitable for the nanocrystal floating gate memory application can be either metals or semiconductors. Recent studies have shown that high-*k* dielectrics, instead of SiO_2, for the tunneling layer in nanocrystal floating gate memory can improve the trade-off between data retention and program efficiency due to the unique band alignment of high-*k* dielectrics in the programming and retention modes. Being physically much thicker than SiO_2, high-*k* dielectrics such as HfO_2 with leakage current several orders of magnitude smaller than SiO_2 with the same equivalent oxide thickness (EOT), result in superior data retention property. The lower electron barrier heights of high-*k* dielectrics can also reduce the programming voltage and thus the operation power compared to the traditionally used SiO_2 gate dielectric. In this project, HfAlO has been selected as the high-*k* dielectric for the nanocrystal floating gate memory structure, since it has been shown to be a promising high-*k* material.

Two deposition techniques, namely pulsed-laser deposition (PLD) and nanocluster source, have been implemented to fabricate nanocrystals. Structural properties of the nanocrystal floating gate memory trilayer structures were characterized by transmission electron microscopy, and atomic force microscopy. Their memory and charge retention characteristics were characterized by capacitance-voltage (*C*-*V*), capacitance-time (*C*-*t*) and current-voltage (*I*-*V*) measurements.

The trilayer structure (HfAlO/Ge-NC/HfAlO) on Si was fabricated by PLD at a relatively low temperature. The effects of deposition temperature and growth rate in forming Ge nanocrystals were investigated and it revealed that relatively low substrate temperature and growth rate are favourable for the formation of smaller-size Ge nanocrystals. Effects of size/density of the Ge NC, the tunneling and control oxide layer thicknesses and the oxygen partial pressure during their growth on the charge storage and charge retention characteristics have also been studied. The island structure of the Ge NC suggests that the growth is based on the Volmer-Webber mode. The self-organized Ge nanocrystals so formed were uniform in size (5-20 nm diameter) and distribution with a density approaching 10^{12} -10^{13}cm^{-2}. Flat-band voltage shift (ΔV_{FB}) of about 3.6 V and good retention property have been achieved.

Another approach is to use a nanocluster source combined with PLD. The nanocluster source has been shown to be capable of generating nanoclusters of semiconductors and metals with the size of a few nanometers, which is the ideal size for nanocrystal floating gate memory application. The implementation of the nanocluster source in fabricating semiconductor nanoclusters is expected to provide a new approach for the fabrication of nanocrystal floating gate memory. By varying aggregation distance, sputtering gas pressure and ionization power, nanoclusters of Ge with different sizes can be formed. Memory effect of Ge nanocluster floating gate memory structure consisting of HfAlO high-*k* dielectric tunneling and control oxides has been investigated. The memory effect of the trilayer structure (HfAlO/Ge-NC/HfAlO) so formed with 10 nm Ge nanoclusters are manifested by the counter-clockwise hysteresis loop in the *C-V* curves and a maximum flat-band voltage shift of 5.0 V has been achieved.

The major advantages of metal nanocrystals include higher density of states around the Fermi level, stronger coupling with the conduction channel, a wide range of

available work functions, and smaller energy perturbation due to carrier confinement. For comparison purposes, metal nanocrystals have also been investigated by utilizing both of the physical deposition methods as mentioned above. Silver (Ag) nanocrystals with size of 10-40 nm have been embedded in HfAlO matrix in the trilayer capacitor structure and a flat-band voltage shift of 2.0 V has been achieved.

List of Publications

1. W. L. Liu, P. F. Lee, J. Y. Dai, J. Wang, H. L. W. Chan , C. L. Choy, Z. T. Song and S. L. Feng, "Self-organized Ge nanocrystals embedded in HfAlO fabricated by pulsed-laser deposition applied to floating gate memory" Appl. Phys. Lett. **86**, 013110 (2005).
2. Shiye Wang, Weili Liu, Qing Wan, J. Y. Dai, P. F. Lee, Luo Suhua, Qinwo Shen, Miao Zhang, Zhitang Song, and Chenglu Lin, "Investigation of Ge nanocrystals in a metal-insulator-semiconductor structure with a HfO_2/SiO_2 stack as the tunnel dielectric" Appl. Phys. Lett. **86**, 113105 (2005).
3. P. F. Lee, W. L. Liu, Z. T. Song, and J. Y. Dai "Ge nanocrystals embedded in Hf-aluminate high-*k* gate dielectric for floating gate memory application" Proc. SPIE **5650**, 141 (2005).
4. X. B. Lu, P. F. Lee, and J. Y. Dai, "Synthesis and memory effect study of Ge nanocrystals embedded in $LaAlO_3$ high-k dielectrics" Appl. Phys. Lett. **86**, 203111 (2005).
5. P. F. Lee, X. B. Lu, J. Y. Dai, H. L. W. Chan, Emil Jelenkovic, and K. Y. Tong, "Memory effect and retention property of Ge nanocrystal embedded Hf-aluminate high-*k* gate dielectric" Nanotech. **17**, 1202 (2006).
6. P. F. Lee, J. Y. Dai, and H. L. W. Chan, "Formation of Ge nanocrystals by utilizing nanocluster source" Material Science in Semiconductor Processing **9**, 817 (2006).
7. P. F. Lee, X. B. Lu, J. Y. Dai, and H. L. W. Chan, "Nanocluster beam deposition of Ge nanoclusters embedded in high-*k* dielectrics for non-volatile flash memory application" Thin Solid Film, submitted.
8. P. F. Lee, K.C. Chan, J. Y. Dai, and H. L. W. Chan, "Nanocluster beam deposited Ag nanocrystals embedded in high-*k* dielectrics for non-volatile memory application",

to be submitted.

9. X. F. Wang, Q. Li, R. F. Egerton, P. F. Lee, J. Y. Dai, Z. F. Hou and X. G. Gong, "Effect of Al addition on the microstructure and electronic structure of HfO_2 film" J. Appl. Phys. **101**, 013514 (2007).

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Chapter 1 Introduction

The first prototype floating gate nonvolatile memory (NVM) devices were introduced in the early 70's at Bells Telephone Laboratory by Kahng and Sze [1]. In this memory device, electrons were transferred from the floating gate layer to the Si substrate by tunneling through a 3 nm thin silicon dioxide (SiO_2) layer. This novel device at that time revolutionized the memory industries which still concentrated on magnetic-core memory. The invention of floating gate NVM raised researchers' attention to the massive market of portable electronic systems, thus, a new memory structure, the so-called flash memory, has widespreaded rapidly since commercialized from the early 90's. Figure 1 is a simple diagram showing a flash memory cell based on floating gate electron tunneling mechanism. A memory cell is an electronic device or system element that contains one bit of information. A standard commercial flash device is illustrated in Fig. 1. The basic device is a metal-oxide-semiconductor field effect transistor (MOSFET) with a modified gate stack structure that has a control gate and a floating gate embedded in a dielectric material such as silicon dioxide (SiO_2) [1-2].

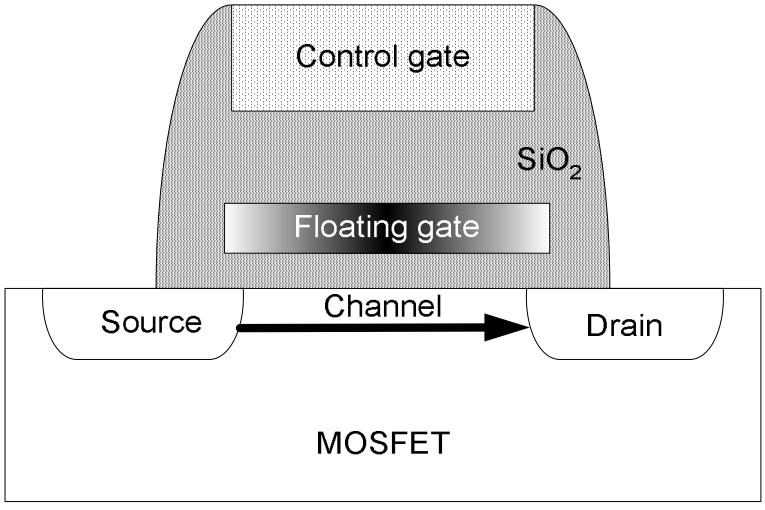


Figure 1 A schematic diagram of a standard commercial flash memory.[1-2]

However, to sustain the continuous scaling into nanometer scale, conventional flash devices may have to undergo revolutionary changes. The scale of stacked-gate structure is one of the major limitations in scaling down of the conventional flash memory [3]. The reason is that, on one hand the tunnel oxide layer must provide electronic charge transfer path between floating gate layer and channel; on the other hand, the tunnel oxide must also provide superior isolation under retention in order to maintain the charge storage over a period of up to a decade. Thus, the thickness of tunnel oxide is a trade-off between fast-write-erase speed and retention reliability. Usually, local defect and leakage path will be present in the tunnel oxide layer after the memory cell is being operated repeatly under high electric field stress (to boost the program/erase current), and consequently, charges stored in the whole continuous floating gate layer will lose in the leakage path. This mechanism is called stress-induced leakage current (SILC). Therefore, if the tunnel oxide is too thin, the retention characteristics will be degraded. In contrast, when the tunnel oxide becomes thicker for better isolation, the read-write speed will be reduced.

Following is a brief review of the flash memory industry development in recent years and some discussions of the scaling down issues regarding future memory applications.

1.1 Flash memory development

1.1.1 Conventional flash memory

Flash memories have been developed from single device component to megabit NVM arrays since Fujio Masuoka from Toshiba first introduced the concept of flash memory in 1984 [4]. Flash memory is a type of electrically erasable and programmable

read only memory (EEPROM) that allows blocks, which consist of a large number of memory cells, to be erased or written in a single action, i.e., in a flash (and hence its name). A flash memory is much faster than a conventional EEPROM, which allows erasure and writing only at the byte level. Flash memory cells provide reading and programming for a byte or a word at one time in random access manner and fast simultaneous block electrical erase (i.e. erased by the entire chip or large sections of the chip).

Many electronic portable devices such as mobile phones, digital camera, personal data assistants (PDA) and compact flash memory cards are fabricated based on flash memory cells due to the advantages of low-power and robust flash systems [2].

Recently, the system-on-chip (SOC) concept for ultra-large scale integration (ULSI) of microelectronic devices has received a great deal of attention. To increase system speed and capability, functional modules (e.g. digital logic, memory, analog components and signal processing) are integrated on a single chip based on this circuit-level integration concept. Embedded flash devices will bring to the SOC design the ability of in-system re-programmability and non-volatile data storage. This capability will lead to low-power and easily re-configurable systems with dense memory capability in future [2].

Integrating an effective flash technology compatible with the standard CMOS device process flow faces many challenges. Inter-related scaling requirement for voltage and gate oxide for embedded flash devices is one of the prominent problems. The aggressive scaling of gate dielectric to eliminate short-channel effect in logic devices is intrinsically incompatible with the requirement to preserve a minimum dielectric thickness in flash devices to maintain oxide reliability and data-retention [2].

In addition, the program and erase voltages of flash devices are typically above 10

volts. This is too large for the one-volt-operation of logic CMOS devices, and will cause the increase of irregular failure bits and stress-induced leakage current when a device is stressed under high bias conditions [2].

Consequently, research for embedded flash devices need to consider the following points [2]:

1) down scaling of device memory cell size,

2) low voltage operation.

To sustain the continuous scaling into nanometer regime, conventional flash memory devices may have to change with novel device concepts with new physical approaches.

1.1.2 Novel structures of flash memory

For conventional flash memory, programming uses channel hot electron (CHE) injection and the erase uses Fowler-Nordheim (F-N) tunneling, and the tunnel oxide under the floating gate cannot be scaled much below 100 Å. When the oxide gets too thin, it will develop leakage paths causing electrons stored in the floating gate to leak out, which reduces both the reliability and scalability of device. The commercial life of flash products, therefore, is predicted to be only about 5-8 years.

To circumvent limitations of conventional flash memories, new device concepts that can solve the leakage problem through oxide defects are being considered. Among the recent proposals are SONOS (Silicon/Oxide/Nitride/Oxide/Silicon) [5-7] (Fig 1.1.1), NROM (Nitride Read-Only Memory) [8-9] and nanocrystal floating gate memories.

Engineered tunnel barrier is another type of new-structure flash memory which includes crested barrier floating gate memory [10-11] and phase-state low-electron-number drive memory (PLEDM) (Fig.1.1.2) [12-13]. The crested barrier concept uses a stack of insulating materials to create a special shape of barrier enabling effective Fowler-Nordheim tunneling into and out of the storage node [10-11]. In the PLEDM memory cell, electrons are injected into the memory node through stacked multiple tunnel junctions with a double-gate structure. Engineered tunnel barriers serve to increase the read/write performance of memory cells while sustaining a long retention time typical for floating gate memories. The approach of floating gate memory with engineered tunnel barriers is currently in concept stage, since no memory operation has been experimentally demonstrated.

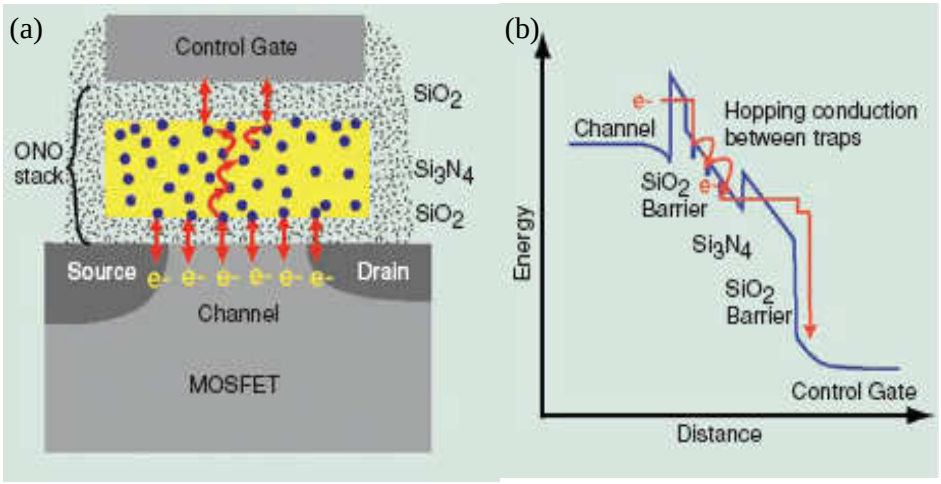


Figure 1.1.1 (a) Basic SONOS memory device structure. Arrows show paths of electron transport during memory operation. The electrons hop between trap sites (blue dots) within the Si_3N_4 layer. Fig. 1.1.1(b) Energy diagram illustrating the physical process of a typical SONOS program operation. [2]

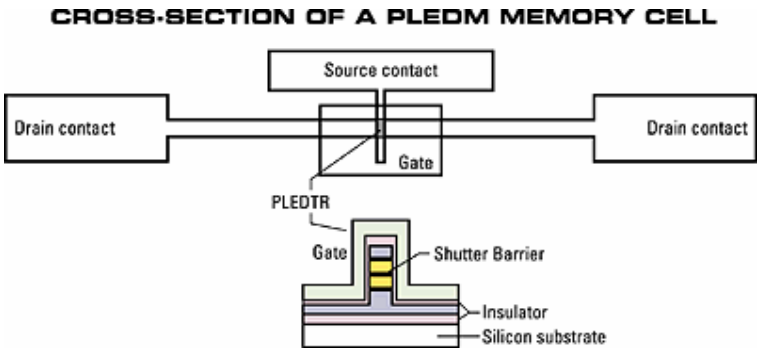


Figure 1.1.2 Cross-section of a PLEDM memory cell.[12-13]

1.1.3 Nano-floating gate flash memory

Nanocrystal floating (also called nano-floating) gate memory is a modified floating gate memory by replacing the continuous poly-Si layer with discontinuous nanocrystals (see Figs. 1.1.3 and 1.1.4). Nano-floating gate memory, composed of nanocrystals isolated by dielectric, increases the reliability and scalability because a single oxide defect does not lead to complete charge loss, and therefore is a promising device for application in future nonvolatile, high-speed, high-density and low power consuming memory.

Nano-floating gate memory, as a basic building block of semiconductor nonvolatile memories, can be used in many fields including PC, communications, consumable electronic products (such as PDA, MP3, mobile phone, and digital camera), and so on. According to the statistics and prediction, the flash memory market in 2004 was about $17.3 billion and has grown continuously because of the accretion of consumable electronic products. By 2007, flash memory is expected to be a $43 billion industry, according to Semico Research. Therefore, as a substitute of flash, nano-floating gate memory should have a greater market in the future.

IBM researchers first proposed a flash memory with a granular floating gate made out of silicon nanocrystals [14-15]. Fig. 1.1.3 is the schematic cross-section image of the prototype Si nanocrystals floating gate memory.

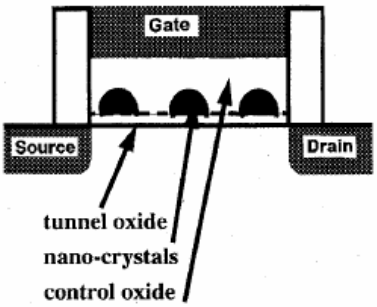


Figure 1.1.3 A schematic diagram of a nanocrystal floating gate memory cell.[14-15]

The memory node of nano-floating gate memory consists of multiple or single silicon nanocrystal dots [2]. The multiple floating dots are separated and independent, and electrons are injected to the dots via different paths. The endurance and retention problem can be much improved in multidot (nanocrystal) memory. Nano-floating gate memory with nanosized memory node is sometimes referred as single electron memory [16].

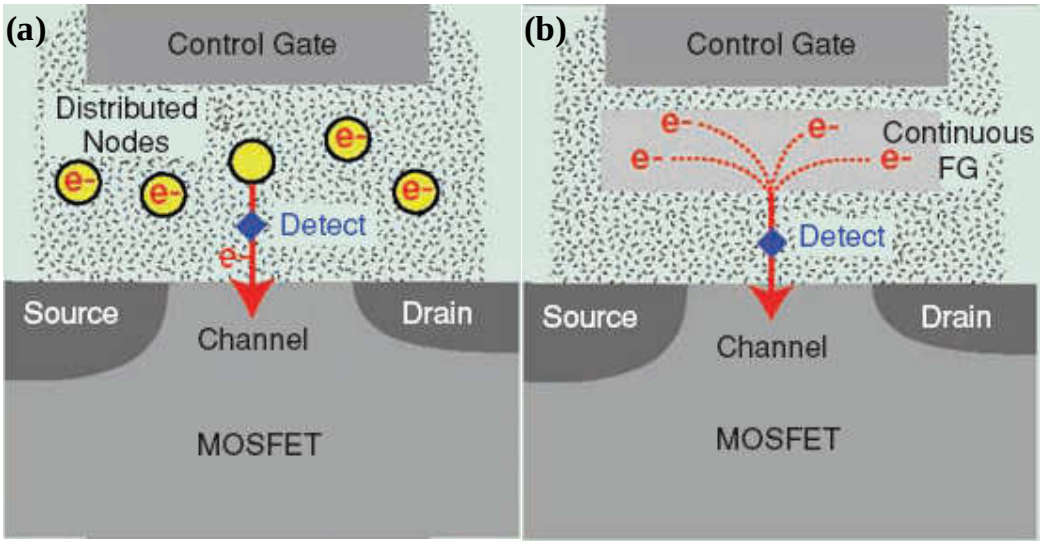


Figure 1.1.4 Charges stored in isolated storage nodes within the dielectric matrix (a), compared with a normal floating gate memory (b). [2]

These technologies replace the continuous floating gate structure with a great number of isolated nanocrystal charge-storage nodes in the dielectric. Continuous floating gate makes the conventional flash memory structure more easily to fail due to failure of charges isolation. Fatal path for discharging leads to the occurrence of long-term volatility even though there is only a small defect in the tunnel oxide layer. Unlike the continuous floating gate structure, due to the distributed nature of the charge storage node, stored charges in the nanocrystal layer cannot easily redistribute among themselves. Therefore, if the distributed storage node density is much higher than the defect density in the isolation dielectric, only a relatively small number of nodes will lose their stored charges through defects. That is to say, nano-floating gate memory is characterized by good immunity to SILC and local oxide defects [3,17]. This effectively prevents the leakage of all the stored charge out of the distributed nanocrystal floating gate layer (Fig. 1.1.4). Thus, aggressive scaling down of tunnel oxide can be achieved.

In 2003, Motorola announced a fully functional 4-megabit test memory chip, based on silicon nanocrystals and using standard deposition tools for 90 nm processes [18]. This is a key milestone in the development of nano-floating gate memory. Freescale semiconductor has had the technology ready for embedded use in system-on-chip (SOC) products such as highly integrated microcontrollers and digital signal processors [19]. International Technology Roadmap of Semiconductors (2005 edition) continues to suggest the incorporation of high-*k* dielectric with nanocrystal as nano-floating gate memory [20].

1.1.4 Motivation of this project

The nanocrystal floating gate memory has attracted a great deal of attention recently because it can potentially be applied in nonvolatile, high-speed, high-density and low-power memory [2-3, 14]. Compared to conventional floating gate memories such as flash, a device composed of nanocrystals isolated by dielectrics benefits from a relatively low operating voltage, high endurance, fast write-erase speeds and better immunity to soft errors [14].

For the first nano-floating gate memory, the materials of nanocrystals and dielectrics were Si and SiO_2, respectively [14-19, 21-42]. In the last two years, research has focused on high-*k* dielectric as the tunnel layer [43-61]. Results show that high-*k* dielectrics such as HfO_2 instead of SiO_2 for tunnel layer in nano-floating gate memory can improve the trade-off between data retention and program efficiency due to its unique band asymmetry in programming and retention mode [47]. Several high-*k* materials including Si_3N_4 [43-46], HfO_2 [47-52], Al_2O_3 [53-57] and ZrO_2 [57-58] have been studied, and HfO_2 is one of the most promising high-*k* materials because of its high dielectric constant and high energy band gap. Results also show that HfAlO combines the advantages of HfO_2 and Al_2O_3. [59-68]

In recent years, several new memory nodes such as Ge [55, 57, 59-61, 69-95], SiGe [51-52, 58, 96], Ni [48-50], Au, Ag, Pt, Co, Cu, TiN, and Sn [56, 97-114] have been investigated, and some of them were incorporated with high-*k* dielectrics [48-52, 55, 57-61]. The Ge nanocrystal is considered to be an ideal memory node due to its relatively small band gap compared to Si and compatibility with current complementary metal-oxide-semiconductor (CMOS) technology. However, it is still difficult to fabricate uniform and self-organized Ge nanocrystals. Most of the methods, including thermal annealing of Ge and dielectric mixture layer [55, 57], Ge ion implantation [69],

and oxidation of SiGe [70-71], require annealing at high temperatures. Baron *et al.* [90] has fabricated Ge nanodots on the SiO_2 matrix by low-pressure chemical vapor deposition. However, silicon nuclei are needed in this method.

Therefore, in this project, integration of nanocrystals including semiconductor Ge nanodots and metal Ag to high-*k* dielectric (HfAlO) as a new approach to fabricate nano-floating gate flash memory is studied. New approaches in fabricating Ge and Ag nanodots, i.e. by means of pulsed-laser deposition and nanocluster beam source, are tackled.

1.1.5 Key issues and problems that need to be addressed

Up to now, the key issues and problems for nano-floating gate memory are the followings:

(1) the formation of uniformly distributed nanocrystals whose size and density can be controlled;

(2) an appropriate tunnel layer that not only allows the charges tunnel through it and be stored into nanocrystals easily, but also can efficiently prevent the stored charges from leaking back into the channel layer;

(3) the optimization of device structure, and thus the performance of MOS.

In this project, the investigation will mainly focus on these key issues and to fabricate a nano-floating gate memory capacitor with high performance. Several novel ideas have been proposed in this program:

(1) fabricate well self-organized nanocrystals by pulsed-laser deposition (PLD) and nanocluster beam source;

(2) employ high-*k* dielectric as the tunnel layer and control layer to improve the trade-off between programming time and retention time.

1.2 High-*k* dielectric material considerations

1.2.1 Introduction on high-*k* dielectrics

Recently, a great deal of effort has been paid to develop an alternative high-permittivity (high-*k*) gate dielectric material in replacement of the currently used SiO_2 for further shrinking of the feature size to below sub 0.1 μm [115]. The driving force for high-*k* dielectrics is to solve the main problems related to high field stressing and the leaky scaled-down oxide barrier during the program and erase operations in a nonvolatile memory [2]. High-*k* dielectric materials would be able to improve the gate capacitance and thus, maintain an equivalent potential difference between the floating gate and the device body, with a thicker oxide layer (greater physical thickness) compared to SiO_2. Thus, the leakage current density can be suppressed and continuous scaling can be achieved.

Many materials are currently under investigation as a potential replacement for SiO_2 as the gate dielectric material to meet the next generation CMOS technology requirement. Among the reported materials, Si_3N_4, Ta_2O_5, TiO_2, Al_2O_3, $SrTiO_3$, HfO_2, ZrO_2 and pseudobinary systems (Zr-Si-O and Hf-Si-O, Hf-Al-O) have been thought of being possible candidates [43-68, 115-178]. Some key guidelines for selecting an alternative gate dielectric are (a) permittivity, band gap, and band alignment to Si, (b) thermodynamic stability, (c) film morphology, (d) interface quality, (e) process compatibility, and (f) reliability [115]. In this thesis, I would only address some of the above guidelines which are mainly related to retention properties for relevant memory application.

The above-mentioned dielectrics appear favorable in some of these areas, but very few materials are promising with respect to all of these guidelines. For example, except

Al_2O_3, all the other dielectric materials suffer from reaction with Si substrate to form SiO_2 and thus downgrade the high-*k* property and increase the equivalent oxide thickness (t_{eq}). This is a severe limitation as a gate dielectric. For Al_2O_3, however, a layer of SiO_2 can still be formed during Al_2O_3 deposition by most of the techniques. In addition, due to the relatively low dielectric constant (k = 9) of Al_2O_3 and easy path for boron diffusion, when polysilicon is used as the gate, it is only a short-term solution [121].

Silicon nitride (Si_3N_4), as a common high-*k* material in the current CMOS process flow, is a very promising candidate for alternative dielectric material to replace SiO_2 [43-45]. However, the thickness gain by Si_3N_4 (k = 7.5) is not much since its dielectric constant is rather close to that of SiO_2 (k = 3.9). This fact is encouraging extensive research for more high-*k* materials. So far, most of the high-*k* materials investigated are quite incompatible with standard CMOS processes. Moreover, a thicker high-*k* dielectric would only improve memory data retention at the expense of program speed [2].

Nano-floating gate memory devices using a crested tunnel barrier made of a stack of nitride–oxide–nitride (NON) layers have been demonstrated with enhanced performance in terms of programming/erasing speed and voltage, and retention time comparable to devices using a single tunnel SiO_2 barrier has been obtained [46].

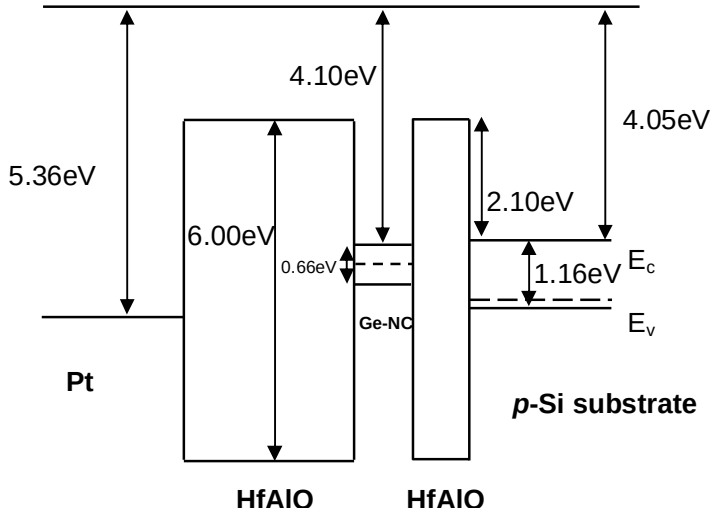


Figure 1.2.1 Energy band diagrams of the Ge nano-floating gate structure at flat-band condition [60].

Table 1.2.1 Band gaps of common materials at room temperature.[116]

Material	E_g	*k*
Si	1.1 eV	
Ge	0.6 eV	
SiO_2	9.0 eV	3.9
Al_2O_3	6.2; 8.8 eV	9-11
ZrO_2	5.8 eV	14-25
HfO_2	5.8 eV	15-26
$HfSiO_x$	6.5 eV	3.9-26, 11*
HfAlO	-	12-17**

* Typical values for Hf silicates corresponding to x=0.35.

** Experimental value.

Effort has also been paid to investigate the influence of embedding the nanocrystals within other high-*k* gate dielectric [46-61]. Table 1.2.1 compares the relevant properties for some high-*k* candidates and semiconductors. Figure 1.2.1 represents the band diagram of a nano-floating gate capacitor structure consisting of Ge nanocrystals embedded in HfAlO thin film matrix with Pt electrode. This approach exploits the smaller conduction band offset between high-*k* materials and Si channel, as well as the larger physical thickness, of high-*k* dielectric compared to SiO_2 tunnel barriers. Although no improvement in programming speed is expected when using high-*k* dielectric tunnel layer, lower programming voltages and better data retention can be achieved [21].

Among the various high-*k* dielectrics, HfO_2 and Hf-based dielectrics are promising candidates to replace SiO_2 to act as the thin film matrix in future memory application [47-52, 59-61]. Wang *et al.* [59] have synthesized Ge nanocrystals embedded in HfAlO high-*k* dielectric by co-sputtering of HfO_2, Al_2O_3, and Ge. A nonvolatile flash memory device using Ge nanocrystal floating gate embedded in HfAlO tunneling/control oxides has been fabricated by Chen *et al.* [60]. We have also shown that N_2 ambient annealed Ge nanocrystal embedded HfAlO and $LaAlO_3$ tunneling/control oxides floating gate memories are promising for future floating gate devices [179-183].

Lee *et al*. [47] have demonstrated the tunneling dielectric properties of Si nanocrystal memory devices both experimentally and theoretically. Figure 1.2.2 is the overall energy band diagram of the Si nanocrystal memory structure and the enlarged conduction band edge profiles of Si nanocrystals/tunneling dielectric/Si-substrate [47]. Kim *et al*. [58] has achieved a low write voltage and improved retention time by using ZrO_2 high-*k* dielectric as tunneling oxide.

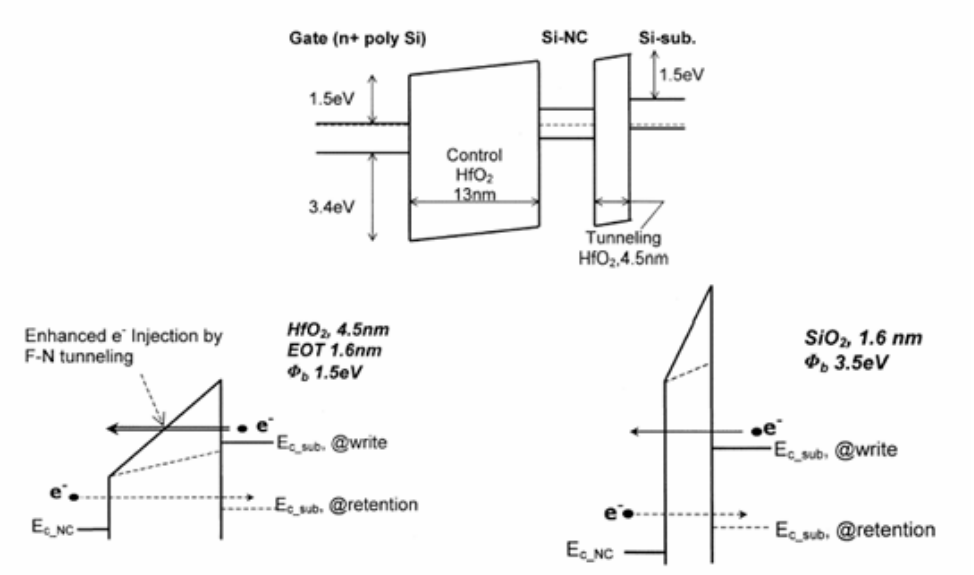


Figure 1.2.2 Energy band diagram of Si nanocrystal memory with HfO_2 at equilibrium, and enlarged conduction band-edge profile of Si nanocrystal/tunneling dielectric/Si substrate of (a) HfO_2, (b) SiO_2 , at writing mode. Dashed lines in (a) and (b) indicate conduction band edge profile at data retention. [47]

1.3 Nanocrystals implemented in this project

1.3.1 Ge nanocrystals

The conventional floating gate memory consists of a continuous layer of poly-Si floating gate layer between the control and tunnel oxide. Thus, the first trial material to fabricate the nano-floating gate memory was Si [14-18]. Motorola announced a fully functional 4-megabit test memory chip based on Si nanocrystals using standard deposition tools for 90 nm processes. Motorola planned to have the technology ready for system-on-chip products. Freescale Semiconductor successfully pioneered the use of nanocrystals in memory devices in March 2003, and discussed the demonstration of its 4-Mbit nanocrystal memory device in the December 2003 IEEE International Electron Devices Meeting (IEDM) in a paper entitled "A 6-V embedded 90-nm silicon nanocrystal nonvolatile memory" [18].

A non-volatile memory technology which is denser, faster and more cost-effective than conventional flash memory technology is closer to production, due to the continued efforts of Freescale Semiconductor to optimize the properties of Si nanocrystals. Freescale has manufactured the world's first 24-megabit (Mbit) memory array based on Si nanocrystals, which is a major step toward replacing conventional floating gate-based flash memories [19].

Nanocrystal storage is being forecast as the technology for the 45 nm technology node or beyond and as an extension to the floating gate or trapping site storage flash memories [184].

As Ge has smaller band gap and higher electron affinity when compared with Si, it is more favorable being the charge storage node in the nano-floating gate memory. A smaller band gap in Ge makes the minimum of the conduction band of Ge nanocrystals

lower than that of the conduction band in the Si channel of the MOS memory device (ΔE_c is approximately ~ 0.05eV for Ge/Si). This allows the same programming voltages but better retention characteristics for Ge nanocrystals since the back tunneling probability – from the nanocrystal to the channel – is considerably reduced. [21]

She *et al*. (Berkeley, USA) suggested that Ge nanocrystal memory devices could provides at least 10^6 times larger retention-time to write-time ratio than convectional floating gate memory devices and the optimum size of the nanocrystal is around 5 nm.[95] A Ge nanocrystal quasi-nonvolatile memory devices with SiO_2 was demonstrated by King *et al*. [70]. The significance of this device is that it can be programmed at low voltage and high speed. However, trap sites will be formed during the Ge implantation process and can degrade device performance. A Singapore-MIT Alliance research group reported the memory characteristics of Ge nanocrystals using a MOS structure in a trilayer configuration [78].

As mentioned in the previous section, nano-floating gate memory can have significantly improved programming efficiency and retention characteristics by using high-*k* dielectic. Wan *et al.* (from China Shanghai IMIT) reported the memory characteristics of Ge nanocrystals embedded in Al_2O_3 and indicated that annealing can effectively passivate the negatively charged tapping centers [55].

1.3.2 Metal nanocrystals

Metal nanocrystals have recently attracted much attention as charge storage elements in memory devices [48-50, 56, 97-114]. In principle, metal nanocrystals should present advantages over semiconductor nanocrystal floating gate memories. The higher electron affinity of several metals compared with Si allows engineering the potential well of the storage nodes in order to create an asymmetric barrier between Si channel and the storage nodes (Fig. 1.3.1). This form of barrier makes programming operation easier. At the same time, a higher energy barrier of metal nanocrystal also enhances retention characteristics. During erase operation, the Fermi level of the nanocrystal is brought above the Si conduction band edge, enabling high-erase current through the tunneling oxide. In addition, the high density of states around the Fermi level in a metal nanocrystal reduces the influence of traps at the nanocrystal/oxide interface [21].

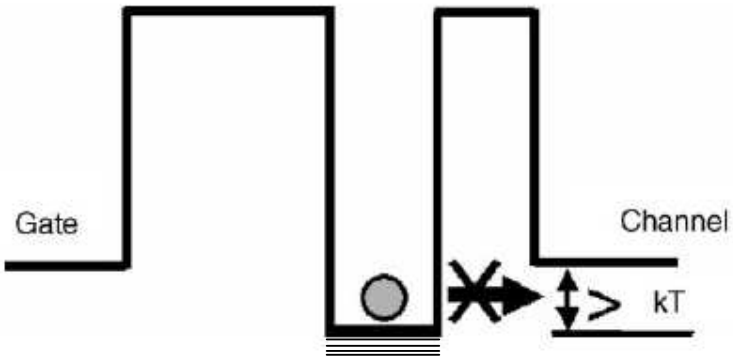


Figure 1.3.1 Energy barriers in the particular case of a metal nanocrystal with higher work function from silicon (channel area). [21]

Research on metal nanocrystals for floating gate memories is more limited and more recent than corresponding research efforts using semiconductor nanocrystals [21]. Z. T. Liu *et. al.* [97-99] has fabricated various types of metal nanocrystals (such as Au, Ag, Pt, W and Co) by the deposition of thin metallic films using evaporation of metal on top of a

tunnel thermal oxide by RTA at 800 °C. The size and density distribution of metal nanocrystals formed depend on the RTA conditions and the thickness of the deposited thin film as reported. The resulting floating gate memory devices prepared using this technique show clear memory windows. This technique could be further explored in future generations of metallic gate MOS devices since it allows more flexibility on nanoparticle energy barrier engineering. A Texas group [48-49] and a National Sun Yat-Sen University group [104-106] also performed a series of experiments regarding the promising nano-floating gate memory by utilizing metal nanocrystal. Metal nanocrystal deposition for floating gate device by utilizing a room temperature deposition technique has been also achieved [107]. In my project, Ag nanocrystals were selected for tackling the metal nanocrystal floating gate memory. Ag has a relatively high E_f of about 4.46 eV (Fig. 1.3.2) and rareness is less than that of gold and platinum, and thus greatly reduces cost.

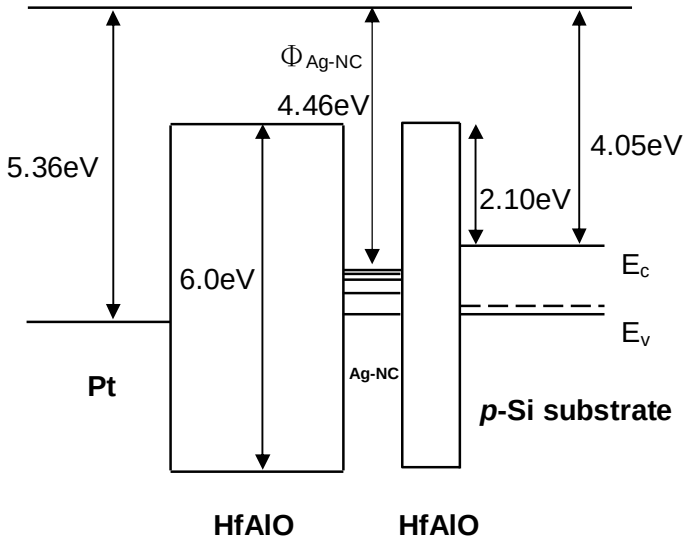


Figure 1.3.2 Energy band diagram of Ag trilayer nano-floating gate structure at flat band condition.

1.3.3 Size effect of nanoclusters

In nano-floating gate memory, when the memory node nanocrystals approach to a size of about 5 nm or below, some size effects need to be considered when analyzing their memory and retention properties. Usually, the size effects need to be considered are quantum confinement effect and Coulomb blockade effect.

- Quantum confinement effect

Quantum confinement effect of a nanodot is a phenomenon of the nonzero lowest energy and quantization of the allowed energy levels in low-dimensional structures. This phenomenon arises from the confinement of electrons within a limited space. It is illustrated as follows [185]:

A free electron moving in three dimensions has a kinetic energy corresponding to the space components of its impulse p_x, p_y, p_z:

$$E = \frac{1}{2m^*}\left(p_x^{\,2} + p_y^{\,2} + p_z^{\,2}\right),$$

or

$$E = \frac{\eta}{2m^*}\left(k_x^{\,2} + k_y^{\,2} + k_z^{\,2}\right),$$

where m^* is the effective mass of electron, which in solids is usually appreciably less than the electron rest mass m_0. k_x, k_y, k_z are the space components of the wave vector. Free motion of electrons in a low-dimensional structure is restricted, at least in one direction. In this direction, let it be the x direction, the forces which confine the electrons can conveniently be described by an infinitely deep potential well, as illustrated by Figure 1.3.3.

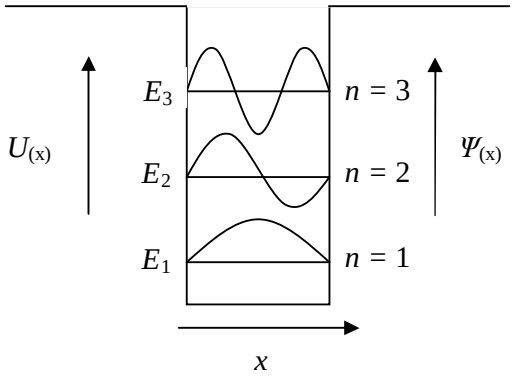


Figure 1.3.3 Potential well and wave functions of electrons confined in it.[185]

Noting that a is the width of the well in x-direction, the electrons have zero potential energy in the region $0<x<a$. Infinitely high impenetrable potential barriers prevent them from straying beyond this region. Thus, the electron wave function drops to zero at x=0 and a. Only a restricted set of wave functions meet these requirements. They can be only standing waves whose wavelength λ takes one of the discrete values given by:

$$\lambda_n = \frac{2a}{n}$$

(where n = 1, 2, ……). The allowed wave vectors of the waves are :

$$k_n = \frac{2\pi}{\lambda_n} = \frac{n\pi}{a} \quad .$$

The discrete wave vectors result in the set of discrete energy states of electrons defined by:

$$E_n = \frac{\eta^2 k_n^{\,2}}{2m} = \frac{\eta^2 \pi^2 n^2}{2ma^2} \quad .$$

The integer n is a quantum number that labels the state. It means that electrons confined to a region of space can occupy only discrete energy levels. The lowest state has the energy :

$$E_1 = \frac{\eta^2 \pi^2}{2ma^2} \quad .$$

The number of the directions remaining free of confinement is used for classification of elementary low-dimensional structures within three groups. These are quantum film, quantum wire and quantum dot shown schematically in Fig. 1.3.4.

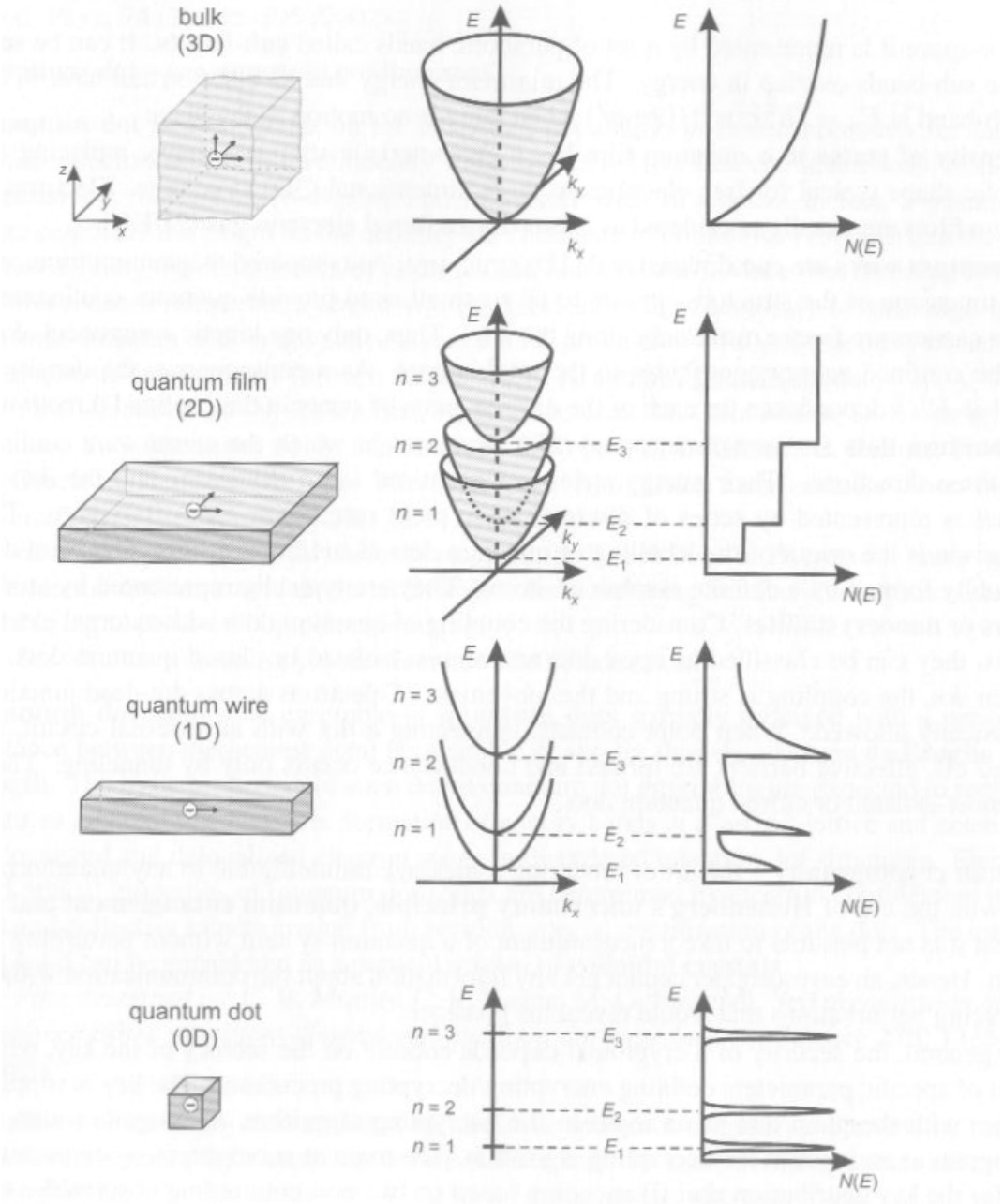


Figure 1.3.4 A schematic diagram of electron energy band structure and how the density of states changes as a function of dimensionality.[185]

A quantum films is two-dimensional (2D) structure in which quantum confinement acts only in one direction, which is in the *z* film thickness direction in Fig. 1.3.4. Charge carriers are free to move in the *xy* plane of the film, giving their total energy to be a sum of the quantum confinement induced and kinetic components:

$$E_n = \frac{\eta^2 \pi^2 n^2}{2ma^2} + \frac{\eta^2 k_x{}^2}{2m} + \frac{\eta^2 k_x{}^2}{2m} \quad .$$

In the *k*-space E_n is represented by a set of parabolic bands called sub-bands. It can be seen that the sub-bands overlap in energy. The minimum energy that an electron can have in the n^{th} sub-band is:

$E_n = \frac{\eta^2 \pi^2 n^2}{2ma^2}$, when there is no motion in the plane.

Density of states in a quantum film has a characteristic staircase shape, replacing the parabolic shape typical for free electrons in three-dimensional (3D) structures. Electrons in quantum films are usually considered as a two-dimensional electron gas (2DEG).

A quantum wire is one-dimensional (1D) structure. As compared to quantum films, one more dimension of the structure appears to be so small as to provide quantum confinement, and charge carriers are free to move only along the wire. Thus, only one kinetic component along with the confined energy contributes to the total energy. As a consequence, the density of states has $E^{1/2}$ dependence for each of the discrete pairs of states in the confined directions.

A quantum dot is zero-directional (0D) structure in which the carriers are confined in all three directions. Their energy states are quantized in all directions and the density of states is represented by series of discrete, sharp peaks resembling that of an atom. This comparison is the origin of the labeling of quantum dots as artificial atoms. Quantum dots are usually formed by a definite number of atoms. They are typically represented by atomic clusters or nanocrystals [185].

How are quantum confinement effects related to the memory effects of the nano-floating gate memory? According to Tsoukalas *et al.*, quantum confinement determines the conditions for charge retention in the Si-NCs since strongly confined NC electron states lie at higher energy than the conduction band edge in the Si substrate and should be able to prevent tunneling out [21].

She *et al*. reported that the size of Ge nanocrystal should not be scaled below 5 nm such that the quantum confinement effect would not become significant [95]. Large quantum confinement leads to the conduction band in the nanocrystal being much higher than that of the Si substrate, resulting in enhanced leakage from nanocrystal and shorter retention time. This is especially significant in the case of Ge nanocrystal embedded in HfAlO due to the smaller conduction band offset.

- Coulomb blockade effect

Coulomb blockade effect is an interdiction of an electron transfer into a region where it results in a change of the electrostatic energy greater than the thermal energy k_BT. Note that if the region is characterized by the capacitance C, its electrostatic energy is increased by $\frac{e^2}{2C}$ with the arrival of one electron. In macroscopic structures, this change in the energy is hardly noticeable; while in nanostructures, particularly in quantum dots, the condition $\frac{e^2}{2C} > k_BT$, is easily realized. The change in the electrostatic energy due to transfer of a single electron results in the gap of $\frac{e^2}{2C}$ in the energy spectrum at the Fermi level, and is referred as a Coulomb gap. Injection of an electron in a Coulomb blockade regime is inhibited until this energy gap is overcome through an applied bias. The phenomenon clearly manifests itself in single-electron tunneling [186].

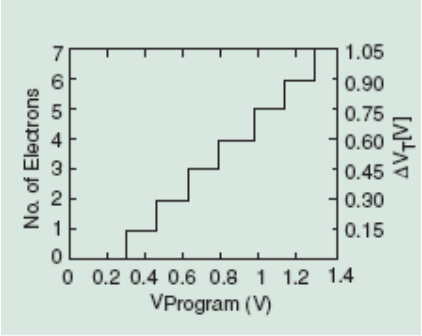


Figure 1.3.5 A simulated Coulomb staircase showing the change in the number of electrons in nanocrystals as a function of the program voltage (left axis). The corresponding threshold voltage memory shift is shown on the right axis. [2]

The Coulomb blockade effect can be described as “discrete changes in the charging energy of a small capacitor due to electrostatic interactions between single electrons.” [2]. The granular nature of electrons becomes significant because they are localized in a small region of space within the isolated nanocrystal.

In nanocrystal floating gate memory devices, electrons must overcome the Coulomb repulsion from the electrons already existing in the charge-storage node before entering a nanocrystal from the Si channel. Since nanocrystals are well distributed, the electric field from the existing electrons is not easily screened. The only way is to vary the control gate voltage to offset the Coulomb repulsion and allow another electron to tunnel into the nanocrystal. The amount of gate tuning ($dV_G = e/C$) corresponds to the capacitive charging energy given by :

$$E = \frac{e^2}{2C} \quad ,$$

where e is the fundamental charge unit and C is the capacitance of a nanocrystal in the order of 10^{-18} farads. Thus, the electrostatic energy variation of the nanocrystal is of the order of several hundreds of milli-electron volts (meV). This is larger than the thermal energy at room temperature, i.e. $k_BT \sim 26$ meV. As such, the microscopic charging effects in a nanocrystal floating gate memory are not easily buried by noisy thermal effects. This leads to immunity of the memory to soft errors due to noisy signal (Fig. 1.3.5) [2].

1.3.4 How to classicify nanocystal, nanodots and nanoclusters

Before I move on to discuss about the nano-floating memory in more detailed manner, some classification and definition about the nanodots need to be made such that no confusion occurs in understanding the content of this thesis. The classification and definition of the wordings are as follows:

Nanodots can be equivalently termed as quantum dots or nanoparticles. Nanodots may have a random arrangement of the constituent atoms or molecules (e.g., an amorphous or glassy material) or the individual atomic or molecular units may be ordered into regular, periodic crystalline structure.

Nanoclusters are particles that range in size from a few to a few hundreds of Angstrons. They are built by a number of atoms or molecules by means of physical or chemical bonding. A nanocluster may not have a particular geometric shape like a dot, so is more general in concept.

Nanocrystals are crystallized nanoparticles or nanodots which may be either a single crystal or polycrystalline.

In this thesis, I generally use nanocrystal floating gate memory for simplicity. In particular, in Chapter 4, where the memory nodes are not crystallized, nanocluster is used to represent the nanodot or nanocrystal.

1.4 Thesis organization

This thesis will be divided into six chapters:

Introduction of the floating gate memory development and motivation of novel memory structure and the thesis work is described in *Chapter 1*.

In *Chapter 2*, experimental techniques used in this work will be presented in detail. Some of the background knowledge will be discussed in this chapter too.

Chapter 3 is the first chapter to present the experimental results obtained in my project. This chapter mainly deals with the experimental results and discussion of Ge nanocrystals fabricated by using pulsed-laser deposition (PLD).

Novel fabrication system – nanoclusters beam source will be discussed in *Chapter 4*. Based on the successful formation of Ge nanoclusters, structural properties of the nanoclusters and parameters which govern the memory effects will be discussed systematically.

For analogous purpose, metal nanocrystals are also employed in the investigation. *Chapter 5* mainly presents the preliminary results of Ag nanocrystals floating gate capacitor.

Finally, in *Chapter 6*, conclusions and suggestions for future work will be given.

References

1. D. Kahng, and S. M. Sze, "A floating-gate and its application to memory device" The Bell System Technical Journal **46**, 1288 (1967).
2. A. Thean and J.-P. Leburton, "Flash memory: towards single-electronics" IEEE POTENTIALS **21**, 35 (2002).
3. J. D. Blauwe, "Nanocrystal nonvolatile memory devices" IEEE Trans. Nanotech. **1**, 72 (2002).
4. F. Masuoka, M. Asano, H. Iwahashi, and T. Komuro, "A new flash EEPROM cell using triple poly-Si technology" IEEE IEDM Tech. Dig., 464 (1984).
5. Y. Yang, A. Purwar, and M. H. White, "Reliability considerations in scaled SONOS novolatile memory devices" Solid-State Electronics **43**, 2025 (1999).
6. Y. Yang, and M. H. White, "Charge retention of scaled SONOS nonvolatile memory devices at elevated temperatures" Solid-State Electronics **44**, 949 (2000).
7. V. A. Gritsenko, K. A. Nasyrov, Yu. N. Novikov, A. L. Aseev, S. Y. Yoon, J.-W Lee, E.-H. Lee, and C. W. Kim, "A new low voltage fast SONOS memory with high-*k* dielectric" Solid-State Electronics **47**, 1651 (2003).
8. F. Libsch, A. Roy, and M. White, "A true 5-V EEPROM cell for high density NVSM," IEEE Trans. Electron Devices **ED-34**, 2371 (1987).
9. B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer, and D. Finzi, "NROM: A novel localized trapping, 2-bit nonvolatile memory cell," IEEE Electron Device Lett. **21**, 543 (2000).
10. K.K. Likharev, "Layered Tunnel Barriers for Nonvolatile Memory Devices," Appl. Phys. Lett. **73**, 2137–2139 (1998).
11. H. Mizuta, H.O. Müller, K. Tsukagoshi, D. Williams, Z. Durrani, A. Irvine, G.

Evans, S. Amakawa, K. Nakazoto, and Haroon Ahmed, "Nanoscale Coulomb Blockade memory and logic devices," Nanotechnology **12**, 155–159 (2001).

12. K. Nakazato, K. Itoh, H. Ahmed, H. Mizuta, T. Kisu, M. Kato, and T. Sakata, "Phase-state low electron-number drive random access memory (PLEDM)" IEEE International Solid-State Circuits Conference 2000 TA 7.4.
13. K. Nakazato, K. Itoh, H. Mizuta, and H. Ahmed, "Silicon stacked tunnel transistor for high-speed and high-density random access memory gain cells," Electronics Lett. **35**, 848–850 (1999).
14. S. Tiwari, F. Rana, Kevin Chan, H. Hanafi, W. Chan, and D. Buchanan "Volatile and non-volatile memories in silicon with nano-crystal storage" IEEE IEDM Tech. Dig., 521 (1995).
15. S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbe, and K. Chan, "A silicon nanocrystal based memory" Appl. Phys. Lett. **68**, 1377 (1996).
16. S. Tiwari, F. Rana, K.Chan, L. Shi, and H. Hanafi, "Single charge and confinement effects in nano-crystal memories" Appl. Phys. Lett. **69**, 1232 (1996).
17. C. Monzio Compagnoni, D. Ielmini, A. S. Spinelli, A. L. Lacaita, C. Gerardi, L. Perniola, B. De Salvo, and S. Lombardo, "Program/erase dynamics and channel conduction in nanocrystal memories" IEEE IDEM Tech. Dig., 549 (2003).
18. R. Muralidhar, R. F. Steimle, M. Sadd, R. Rao, C. T. Swift, E. J. Prinz, J. Yater, L. Grieve, K. Harber, B. Hradsky, S. Straub, B. Acred, W. Paulson, W. Chen, L. Parker, S. G. H. Anderson, M. Rossow, T. Merchant, M. Paransky, T. Huynh, D. Hadad, K.-M. Chang, and B. E. White Jr., "A 6V embedded 90nm silicon nanocrystal nonvolatile memory" IEEE IEDM Tech. Dig., 601 (2003).
19. Freescale semiconductor, "Freescale Manufactures World's First 24-Mbit Silicon Nanocrystal Memory" (http://www.freescale.com/) News Release, 28-Nov (2005).

20. International Technology Roadmap for Semiconductors (2005). [On-line] http://public.itrs.net/.

21. D. Tsoukalas, P. Dimitrakis, S. Kolliopoulou, and P. Normand, "Recent advances in nanoparticle memories" Mat. Sci. Eng. B **124-125**, 93 (2005).

22. B. De Salvo, G. Ghibaudo, G. Pananakakis, P. Masson, T. Baron, N. Buffet, A. Fernandes, and B. Guillaumot, "Experimental and theorretical investigation of nano-crystal and nitride-trap memory devices" IEEE Trans. Electron Devices **48**, 1789 (2001).

23. Y. Shi, K. Saito, H. Ishikuro, and T. Hiramoto, "Effects of traps on charge storage characteristics in metal-oxide-semiconductor memory structures based on silicon nanocrystals" J. Appl. Phys. **84**, 2358 (1998).

24. T. Baron, F. Martin, P. Mur, C. Wyon, and M. Dupuy, "Silicon quantum dot nucleation on Si_3N_4, SiO_2 and SiO_xN_y substrates for nanoelectronic devices," J. Cryst. Growth **290**, 1004 (2000).

25. T. Baron, F. Martin, P. Mur, C.Wyon, M. Dupuy, C. Busseret, A. Souifi, and G. Guillot, "Low pressure chemical vapor deposition growth of silicon quantum dots on insulator for nanoelectronics devices," Appl. Surf. Sci. **164**, 29 (2000).

26. C. Busseret, A. Souifi, T. Baron, G. Guillot, F. Martin, M. N. Semeria, J. Gautier, "Discharge mechanisms modeling in LPCVD silicon nanocrystals using *C-V* and capacitance transient techniques" Superlattices and Microstructures **28**, 493 (2000).

27. Y. Kim, K. H. Park, T. H. Chung, H. J. Bark, J.-Y. Yi, W. C. Choi, E. K. Kim, J. W. Lee, and J. Y. Lee, "Ultralarge capacitance-voltage hysteresis and charge retention characteristic in metal oxide semiconductor structure containing nanocrystals deposited by ion-beam-assisted electron beam deposition" Appl. Phys. Lett. **78**, 934 (2001).

28. S. Huang, S. Banerjee, R. T. Tung, and S. Oda, "Electron trapping, storing, and emission in nanocrystalline Si dots by capacitance-voltage and conductance-voltage measurements" J. Appl. Phys. **93**, 576 (2003).
29. G. Molas, B. De Salvo, D. Mariolle, G. Ghibaudo, A. Toffoli, N. Buffet, and S. Deleonibus, "Single electron charging and discharging phenomena at room temperature in a silicon nanocrystal memory" Soild-State Electronics **47**, 1645 (2003).
30. L. Tsybeskov, G. F. Grom, M. Jungo, L. Montes, P. M. Fauchet, J. P. McCaffrey, J.-M. Baribeau, G. I. Sproule, and D. J. Lockwood, "Nanocrystalline silicon superlattices: building blocks for quantum devices" Mat. Sci. Eng. **B69-70**, 303 (2000).
31. I. Crupi, D. Corso, S. Lombardo, C. Gerardi, G. ammendola, G. Nicotra, C. Spinella, E. Rimini, and M. Melanotte, "Memory effects in MOS devices based on Si quantum dots" Mat. Sci. Eng. **C 23**, 33 (2003).
32. D. Deleruyelle, J. Cluzel, B. De Salvo, D. Fraboulet, D. Mariolle, N. Buffet, and S. Deleonibus, "Electrical characterization of fast transient phenomena in a Si-rich based non-volatile random access memory" Solid-State Electronics **47**, 1641 (2003).
33. Y. H. Kwon, C. J. Park, W. C. Lee, D. J. Fu, Y. Shon, T. W. Kang, C. Y. Hong, H. Y. Cho, and Kang L. Wang, "Memory effects related to deep levels in metal-oxide-semiconductor structure with nanocrystalline Si" Appl. Phys. Lett. **80**, 2502 (2002).
34. C. Y. Ng, T. P. Chen, L. Ding, Y. Liu, M. S. Tse, S. Fung, and Z. L. Dong, "Static dielectric constant of isolated silicon nanocrystals embedded in a SiO_2 thin film" Appl. Phys. Lett. **88**, 063103 (2006).

35. S.-H. Choi and R. G. Elliman, "Reversible charging effects in SiO_2 films containing Si nanocrystals" Appl. Phys. Lett. **75**, 968 (1999).

36. L. Wu, M.Dai, X. Huang, W. Li, and K. Chen, "Size-dependent resonant tunneling and storing of electrons in a nanocrystalline silicon floating-gate double-barrier structure" J. Vac. Sci. Technol. B **22**, 678 (2004).

37. M. Saitoh, and T. Hiramoto, "Extension of Coulomb blockade region by quantum confinement in the ultrasmall silicon dot in a single-hole transistor at room temperature" Appl. Phys. Lett. **84**, 3172 (2004).

38. K. Han, I. Kim, H. Shin, "Programming characteristics of P-channel Si nano-crystal memory" IEEE Electron Device Lett. **21**, 313 (2000).

39. D. N. Kouvatsos, V. loannou-Sougleridis, and A. G. Nassiopoulou, "Charging effects in silicon nanocrystals within SiO_2 layers, fabricated by chemical vapor deposition, oxidation, and annealing" Appl. Phys. Lett. **82**, 397 (2003).

40. A. Thean and J.-P. Leburton, "Stark effect and single-electron charging in silicon nanocrystal quantum dots" J. Appl. Phys. **89**, 2808 (2001).

41. A. Thean and J. P. Leburton, "Three-demensional self-consistent simulation of silicon quantum-dot floating-gate flash memory device" IEEE Electron Device Lett. **20**, 286 (1999).

42. A. Thean and J. P. Leburton, "3-D Computer Simulation of Nanocrystal Flash Memory Devices" Proceedings of Non-Volatile Memory Technology Symposium 2000, 16 (2000).

43. N.-M. Park, S.-H. Choi, and S.-J. Park, "Electron charging and discharging in amorphous silicon quantum dots embedded in silicon nitride" Appl. Phys. Lett. **81**, 1092 (2002).

44. Zi. Pei, Alex Y. K. Su, H. L. Hwang, and H. L. Hsiao, "Room temperature

tunneling transport through Si nanodots in silicon rich silicon nitride" Appl. Phys. Lett. **86**, 063503 (2005).

45. T.-Y Kim, N.-M Park, K.-H. Kim, G. Y. Sung, Y.-W. Ok, T.-Y. Seong, and C.-J. Choi, "Quantum confinement effect of silicon nanocrystals *in situ* grown in silicon nitride films" Appl. Phys. Lett. **85**, 5355 (2004).
46. S. J. Baik, S. Choi, U. I. Chung, J. T. Moon, "High speed and nonvolatile Si nanocrystal memory for scaled flash technology using highly field-sensitive tunnel barrier" IEEE IEDM Tech. Dig.,267 (2003).
47. J. J. Lee, Xuguang Wang, Weiping Bai, Nan Lu, and Dim-Lee Kwong, "Theoretical and experimental investigation of Si nanocrystal memory device with HfO_2 high-*k* tunneling dielectric" IEEE Trans. Electron Devices **50**, 2067 (2003).
48. J. J. Lee and D.-L. Kwong, "Metal nanocrystal memory with high-*k* tunneling barrier for improved data retention" IEEE Trans. Electron Devices **52**, 507 (2005).
49. J. J. Lee, Y. Harada, J. W. Pyun, and D.-L. Kwong, "Nickel nanocrystal formation on HfO_2 dielectric for nonvolatile memory device applications" Appl. Phys. Lett. **86**, 103505 (2005).
50. Z. Tan, S. K. Samanta, W. J. Yoo, and S. Lee, "Self-assembly of Ni nanocrystals on HfO_2 and N-assisted Ni confinement for nonvolatile memory application" Appl. Phys. Lett. **86**, 013107 (2005).
51. D.-W. Kim, T. Kim, and S. K. Banerjee, "Memory Characterization of SiGe Quantum Dot Flash Memories With HfO_2 and SiO_2 Tunneling Dielectrics" IEEE Trans. Electron Devices **50**, 1823 (2001).
52. R. Gupta, W. J. Yoo, Y. Wang, Z. Tan, G. Samudra, S. Lee, Daniel S. H. Chan, K. P. Loh, L. K. Bera, N. Balasubramanian, and D.-L. Kwong, "Formation of SiGe nanocrystals in HfO_2 using in situ chemical vapor deposition for memory

applications" Appl. Phys. Lett. **84**, 4331 (2004).

53. T. Baron, A. Fernandes, J. F. Damlencourt, B. De Salvo, F. Martin, F. Mazen, and S. Haukka, "Growth of Si nanocrystals on alumina and integration in memory devices" Appl. Phys. Lett. **82**, 4151 (2003).
54. A. Fernandes, B. De Salvo, T. Baron, J. F. Damlencourt, A. M. Papon, D. Lafond, D. Mariolle, B. Guillaumot, P. Besson, P. Masson, G. Ghibaudo, G. Pananakakis, F. Martin, and S. Haukka, "Memory characteristics of Si quantum dot devices with SiO_2/ALD Al_2O_3 tunneling dielectrics" IEEE IEDM Tech. Dig., 155 (2001).
55. Q. Wan, C. L. Lin, W. L. Liu, and T. H. Wang, "Structural and electrical characteristics of Ge nanoclusters embedded in Al_2O_3 gate dielectric" Appl. Phys. Lett. **82**, 4708 (2003).
56. Q. Wang, Z. T. Song, W. L. Liu, C. L. Lin, and T. H. Wang, "Synthesis and electron storage characteristics of isolated silver nanodots on /embedded in Al_2O_3 gate dielectric" Appl. Surf. Sci. **230**, 8 (2004).
57. Q. Wan, N. L. Zhang, W. L. Liu, C. L. Lin, and T. H. Wang, "Memory and negative photoconductivity effects of Ge nanocrystals embedded in ZrO_2/Al_2O_3 gate dielectrics" Appl. Phys. Lett. **83**, 138 (2003).
58. D.-W. Kim, F. E. Prins, T. Kim, S. Hwang, C. H. Lee, D.-L. Kwong, and S. K. Banerjee, "Reduction of Charge-Transport Characteristics of SiGe Dot Floating Gate Memory Gate Memory Device With ZrO_2 Tunneling Oxide" IEEE Trans. Electron Devices **50**, 510 (2003).
59. Y. Q. Wang, J. H. Chen, W. J. Yoo, Y.-C. Yeo, S. J. Kim, D.-L. Kwong, A. Y. Du, and N. Balasubramanian, "Formation of Ge nanocrystals in HfAlO high-*k* dielectric and application in memory device" Appl. Phys. Lett. **84**, 5407 (2004).
60. J. H. Chen, Y. Q. Wang, W. J. Yoo, Y.-C. Yeo, G. Samudra, Daniel S. H. Chan, A. Y.

Du and D.-L. Kwong, "Nonvolatile Flash Memory Device Using Ge Nanocrystals Embedded in HfAlO High-*k* Tunneling and Control Oxides: Device Fabrication and Electrical Performance" IEEE Trans. Electron Devices **51**, 1840 (2004).

61. T. H. Ng, W. K. Chim, and W. K. Choi, "Conductance-voltage measurements on germanium nanocrystal memory structures and effect of gate electric field coupling" Appl. Phys. Lett. **88**, 113112 (2006).
62. H. Y. Yu, M. F. Li, B. J. Cho, C. C. Yeo, M. S. Joo, D,-L. Kwong, J. S. Pan, C. H. Ang, J. Z. Zheng, and S. Ramanathan, "Energy gap and band alignment for $(HfO_2)_x(Al_2O_3)_{1-x}$ on (100) Si" Appl. Phys. Lett. **81**, 376 (2002).
63. M. Kundu, N. Miyata, T. Nabatame, T. Horikawa, M. Ichikawa, and A. Toriumi, "Effect of Al_2O_3 capping layer on suppression of interfacial SiO_2 growth in HfO_2/ultrathin SiO_2/Si(001) structure" Appl. Phys. Lett. **82**, 3442 (2003).
64. D. C. Gilmer, R. Hegde, R. Cotton, R. Garcia, V. Dhandapani, D. Triyoso, D. Roan, A. Franke, R. Rai, L. Prabhu, C. Hobbs, J. M. Grant, L. La, S. Samavedam, B. Taylor, H. Tseng, and P. Tobin, "Compatibility of polycrystalline silicon gate deposition with HfO_2 and Al_2O_3/HfO_2 gate dielectrics" Appl. Phys. Lett. **81**, 1288 (2002).
65. R. S. Johnson, J. G. Hong, C. Hinkle, and G. Lucovsky, "Electron trapping in noncrystalline remote plasma deposited Hf-aluminate alloys for gate dielectric applications" J. Vac. Sci. Technol. B **20**, 1126 (2002).
66. P. F. Lee, J. Y. Dai, K. H. Wong, H. L. W. Chan, and C. L. Choy, "Study of interfacial reaction and its impact on electric properties of Hf-Al-O high-*k* gate dielectric thin films grown on Si" Appl. Phys. Lett. **82**, 2419 (2003).
67. P. F. Lee, J. Y. Dai, H. L. W. Chan and C. L. Choy, "Study of Hf-Al-O high-*k* gate dielectric thin films grown on Si" J. Integrated Ferroelectrics **59**, 1213 (2003).

68. J. Y. Dai, P. F. Lee, H. L. W. Chan, and C. L. Choy, "Epitaxial growth of yttrium-stabilized HfO_2 high-*k* gate dielectric thin films on Si" J. Appl. Phys. **94**, 912 (2003).

69. H. Hanafi, S. Tiwari, and I. Khan, "Fast and long retention-time nano-crystal memory" IEEE Trans. Electron Devices **43**, 1553 (1996).

70. Y.-C. King, T.-J. King, and Chenming Hu, "MOS memory using germanium nanocrystals formed by thermal oxidation of $Si_{1-x}Ge_x$" IEEE IEDM Tech. Dig., 115 (1998).

71. Y.-C. King, T.-J. King, and Chenming Hu, "Charg-trap memory device fabricated by oxidation of $Si_{1-x}Ge_x$" IEEE Trans. Electron Devices **48**, 696 (2001).

72. S. Duguay, J. J. Grob, A. Slaoui, Y. Le Gall, and M. Amann-Liess, "Structural and electrical properties of Ge nanocrystals embedded in SiO_2 by ion implantation and annealing" J. Appl. Phys. **97**, 104330 (2005).

73. C. J. Park, H. Y. Cho, S. Kim, Suk-Ho Choi, R. G. Elliman, J. H. Han, Chungwoo Kim, H. N. Hwang, and C. C. Hwang, "Annealing temperature dependence of capacitance-voltage characteristics in Ge-nanocrystal-based nonvolatile memory structures" J. Appl. Phys. **99**, 036101 (2006).

74. C. J. Park, K. H. Cho, W.-C. Yang, H. Y. Cho, Suk-Ho Choi, R. G. Elliman, J. H. Han, and Chungwoo Kim, "Large capacitance-voltage hysteresis loops in SiO_2 films containing Ge nanocrystals produced by ion implantation" Appl. Phys. Lett. **88**, 071916 (2006).

75. T. Kobayashi, T. Endoh, H. Fukuda, S. Nomura, A. Sakai, and Y. Ueda, "Ge nanocrystals in SiO_2 films" Appl. Phys. Lett. **71**, 1195 (1997).

76. C. L. Heng, L. W. Teo, Vincent Ho, M. S. Tay, Y. Lei, W. K. Choi, and W. K. Chim, "Effects of rapid thermal annealing time and ambient temperature on the charge

storage capability of SiO_2/pure Ge/rapid thermal oxide memory structure" Microelectronic Eng. **66**, 218 (2003).

77. C. L. Heng, and T. G. Finstad, "Electrical characteristics of a metal-insulator-semiconductor memory structure containing Ge nanocrystals" Physica E **26**, 386 (2005).
78. W. K. Choi, W. K. Chim, C. L. Heng, L. W. Teo, Vincent Ho, V. Ng, D. A. Antoniadis, and E. A. Fitzgerald, "Observation of memory effect in germanium nanocrystals embedded in an amorphous silicon oxide matrix of a metal-insulator-semiconductor structure" Appl. Phys. Lett. **80**, 2014 (2002).
79. E. W. H. Kan, W. K. Choi, C. C. Leoy, W. K. Chim, D. A. Antoniadis, and E. A. Fitzgerald, "Effect of annealing profile on defect annihilation, crystallinity and size distribution of germanium nanodots in silicon oxide matrix" Appl. Phys. Lett. **83**, 2058 (2003).
80. Vincent Ho, M. S. Tay, C. H. Moey, L. W. Teo, W. K. Choi, W. K. Chim, C. L. Heng, and Y. Lei, "Electrical characterization of a trilayer germanium nanocrystal memory device" Microelectronic Eng. **66**, 33 (2003).
81. B. H. Koh, E. W. H. Kan, W. K. Chim, W. K. Choi, D. A. Antoniadis, and E. A. Fitzgerald, "Traps in germanium nanocrystal memory and effect on charge retention: Modeling and experimental measurements" J. Appl. Phys. **97**, 124305 (2005).
82. K. Das, M. NandaGoswami, R. Mahapatra, G. S. Kar, A. Dhar, H. N. Acharya, S. Maikap, J.-H. Lee, and S. K. Ray, "Charge storage and photoluminescence characteristics of silicon oxide embedded Ge nanocrystal trilayer structures" Appl. Phys. Lett. **84**, 1386 (2004).
83. A. Kanjilal, J. Lundsgaard Hansen, P. Gaiduk, A. Nylandsted Larsen, N.

Cherkashin, A. Claverie, P. Normand, E. Kapelanakis, D. Skarlatos, and D. Tsoukalas, "Structural and electrical properties of silicon dioxide layers with embedded germanium nanocrystals grown by molecular beam epitaxy" Appl. Phys. Lett. **82**, 1212 (2003).

84. B. Gallas, and J. Rivory, "Investigation of a single Ge dots layer and its evolution upon oxidation by spectroscopic ellipsometry" Physica E **17**, 549 (2003).
85. P. I. Gaiduk, A. Nylandsted Larsen, J. Lundsgard Hansen, "MBE grown Ge dots on Si/SiGe ion implanted buffers" Physica E **17**, 510 (2003).
86. X. Y. Ma, Sh. H. Huang, Y. Chen, and F. Lu, "Investigation of the quantum confinement effects in Ge dots by electrical measurements" Appl. Surf. Sci. **225**, 281 (2004).
87. M. Kanoun, M. Lemiti, G. Bremond, A. Souifi, F. Bassani, and I. Berbezier, "Electrical study of MOS structure with Ge embedded in SiO_2 as floating gate for nonvolatile memory" Superlattices and Microstructures **36**, 143 (2004).
88. T. Sass, V. Zela, A. Gustafsson, I. Pietzonka, and W. Seifert, "Oxidation and reduction behavior of Ge/Si islands" Appl. Phys. Lett. **81**, 3455 (2002).
89. A. Hattab, F. Dufaye, F. Meyer, Vy Yam, Vinh Le Thanh, D. Bouchier, R. Meyer, O. Schneegans, and C. Clerc, "Effect of Ge-dots buried below the interface on the transport properties of Schottky diodes" Physica E **17**, 648 (2003).
90. T. Baron, B. Pelissier, L. Perniola, F. Mazen, J. M. Hartmann, and G. Rolland, "Chemical vapor deposition of Ge nanocrystals on SiO_2" Appl. Phys. Lett. **83**, 1444 (2003).
91. M. Kanoun, A. Souifi, T. Baron, and F. Mazen, "Electrical study of Ge-nanocrystal-based metal-oxide-semiconductor structures for *p*-type nonvolatile memory applications" Appl. Phys. Lett. **84**, 5079 (2004).

92. T. C. Chang, S. T. Yan, P. T. Liu, C. W. Chen, S. H. Lin, and S. M. Sze, "A novel approach of fabricating germanium nanocrystals for nonvolatile memory application" Electrochem. Solid-State Lett. **7**, G17 (2004).

93. Y. Kim, H. J. Cheong, K. H. Park, T. H. Chung, H. J. Bark, J.-Y. Yi, S. H. Bang, and J. H. Cho, "Charge retention characteristics in a metal-insulator -semiconductor capacitor containing Ge nanocrystals" Semicond. Sci. Technol. **17**, 1039 (2002).

94. J. K. Kim, H. J. Cheong, Y. Kim, J,-Y, Yi, H. J. Bark, S. H. Bang, and J. H. Cho, "Rapid-thermal-annealing effect on lateral charge loss in metal-oxide-semiconductor capacitors with Ge nanocrystals" Appl. Phys. Lett. **82**, 2527 (2003).

95. M. She, and T. -J King, "Impact of crystal size and tunnel dielectric on semiconductor nanocrystal memory performance" IEEE Tans. Electron Devices **50**, 1934 (2003).

96. Y. Zhu, D. Zhao, R. Li, and J. Liu, "Threshold voltage shift of heteronanocrystal floating gate flash memory" J. Appl. Phys. **97**, 034309 (2005).

97. Z. T. Liu, C. Lee, V. Narayanan, G. Pei, and Edwin C. Kan, "Metal nanocrystal memories – Part I: Device design and fabrication" IEEE Trans. Electron Devices **49**, 1606 (2002).

98. Z. T. Liu, C. H. Lee, V. Narayanan, G. Pei, and Edwin C. Kan, "Metal nanocrystal memories – Part II: Electrical characteristics" IEEE Trans. Electron Devices **49**, 1614 (2002).

99. Z. T. Liu, C. H. Lee, V. Narayanan, G. Pei, and Edwin C. Kan, "A novel quad source/drain metal nanocrystal memory device for multibit-per-cell storage" IEEE Electron Device Lett. **24**, 345 (2003).

100. S. Paul, C. Pearson, A. Molloy, M. A. Cousins, M. Green, S. Kolliopoulou, P. Dimitrakis, P. Normand, D. Tsoukalas, and M. C. Petty, "Langmuir-Blodgett Film Deposition of Metallic Nanoparticles and Their Application to Electronic Memory Structures" Nanoletters **3**, 533 (2003).

101. J.-Y. Tseng, C.-W. Cheng, S.-Y. Wang, T.-B. Wu, K.-Y. Hsieh, and R. Liu, "Memory characteristics of Pt nanocrystals self-assembled from reduction of an embedded PtO_x ultrathin film in metal-oxide-semiconductor structures" Appl. Phys. Lett. **85**, 2595 (2004).

102. C. H. Lee, J. Meteer, V. Narayanan, and Edwin C. Kan, "Self-assembly of metal nanocrystals on ultrathin oxide for nonvolatile memory applications" J. Electronic Mat. **34**, 1 (2005).

103. P. H. Yeh, H. H. Wu, C. H. Yu, L. J. Chen, P. T. Liu, C. H. Hsu, and T. C. Chang, "Fabrication of $NiSi_2$ nanocrystals embedded in SiO_2 with memory effect by oxidation of amorphous $Si/Ni/SiO_2$ structure" J. Vac. Sci Technol. A **23**, 851 (2005).

104. T. C. Chang, P. T. Liu, S. T. Yan, and S. M. Sze, "Electron charging and discharging effects of tungsten nanocrystals embedded in slicon dioxide for low-voltage nonvolatile memory technology" Electrochem. Solid-State Lett. **8**, G71 (2005).

105. T. C. Chang, S. T. Yan, P. T. Liu, C. W. Chen, H. H. Wu, and S. M. Sze, "Quasi-superlattice storage A concept of multilevel charge storage" J. Electrochem. Soc. **151**, G805 (2004).

106. T. C. Chang, S. T. Yan, P. T. Liu, C. W. Chen, H. H. Wu, and S. M. Sze, "Quasisuperlattice storage: A concept of multilevel charge storage" Appl. Phys. Lett. **85**, 248 (2004).

107. S. Kolliopoulou, P. Dimitrakis, P. Normand, H. L. Zhang, N. Cant, S. D. Evans, S. Paul, C. Pearson, A. Molloy, M. C. Petty, D. Tsoukalas, "Hybrid silicon – organic nanoparticle memory device" J. Appl. Phys. **94**, 5234 (2003).

108. S. Spiga, R. Mantovan, M. Fanciulli, N. Ferretti, F. Boscherini, F. d' Acapito, B. Schmidt, R. Grötzchel, and A. Mücklich, "Local structure of Sn implanted in thin SiO_2 films" Phys. Rev. B **68**, 205419 (2003).

109. J. H. Chen, W. J. Yoo, Daniel S. H. Chan, and L.-J. Tang, "Self-assembly of Al_2O_3 nanodots on SiO_2 using two-step controlled annealing technique for long retention nonvolatile memories" Appl. Phys. Lett. **86**, 073114 (2005).

110. S. Choi, S.-S. Kim, M. Chang, H. Hwang, S. Jeon, and C. Kim, "Highly thermally stable TiN nanocystals as charge trapping sites for nonvolatile memory device applications" Appl Phys. Lett. **86**, 123110 (2005).

111. U. Ganguly, Edwin C. Kan, and Y. Zhang, "Carbon nanotube-based nonvolatile memory with charge storage in metal nanocrystals" Appl. Phys. Lett. **87**, 043108 (2005).

112. B. Johannessen, P. Kluth, C. J. Glover, G. de M. Azevedo, D. J. Llewellyn, G. J. Foran, and M. C. Ridgway, "Structural characterization of Cu nanocrystals formed in SiO_2 by high-energy ion-beam synthesis" J. Appl. Phys. **98**, 024307 (2005).

113. A. Nakajima, T. Futatsugi, H. Nakao, T. Usuki, N. Horiguchi, and N. Yokoyama, "Microstructres and electrical properties of Sn nanocrystals in thin thermally grown SiO_2 formed via low energy ion implantation," J. Appl. Phys. **84**, 1316 (1998).

114. A. Nakajiama, T. Futatsugi, N. Horiguchi, and H. Nakao, "Single electron charging of Sn nanocrystals in thin SiO_2 film formed by low energy ion implantation," IEEE IEDM Tech. Dig., 159 (1997).

115. G. D. Wilk, R. M. Wallace, J. M. Anthony, "High-*k* gate dielectrics: Current status and materials properties considerations" J. Appl. Phys. **89**, 5243 (2001).

116. D. H. A. Blank, L. M. Doeswijk, K. Karakaya, G. Koster and G. Rijnders, "Pulsed laser deposition of dielecteics". In *High-k gate dielectrics*, edited by M. Houssa pp.89 (Institute of Physics, 2004).

117. S. Deleonibus, "Device architectures for the nano-CMOS era". In *High-k gate dielectrics*, edited by M. Houssa pp.524 (Institute of Physics, 2004).

118. C. Chaneliere, J. L. Autran, R. A. B. Devine, and Balland, "Tantalum pentoxide (Ta_2O_5) thin films for advanced dielectric applications" Mater. Sci. Eg. R **22** 269 (1998).

119. S. A. Campbell, D. C. Gilmer, X. Wang, M. T. Hisch, H. S. Kim, W. L. Gladfelter, and J. H. Yan, "MOSFET transistors fabricated with high permitivity TiO_2 dielectrics" IEEE Trans. Electron Devices **44**, 104 (1997).

120. K. Eisenbeiser, J. M. Finder, Z. Yu, J. Ramdani, J. A. Curless, J. A. Hallmark, R. Droopod, W.J. Ooms, L. Salem, S. Bradshaw, and C.D. Overgaard, "Field effect transistors with $SrTiO_3$ gate dielectric on Si" Appl. Phys. Lett. **76**, 1324 (2000).

121. D. G. Park, H. J. Cho, C. Lim, I. S. Yeo, J. S. Roh, C. T. Kim, and J. M. Hwang, "Characteristics of Al_2O_3 gate dielectric prepared by atomic layer deposition for giga scale CMOS DRAM devices" Tech. Dig. VLSL Symp. 2000, P.46.

122. M. Copel, M. A. Gribelyuk, and Gusev, "Structure and stability of ultrathin zirconium oxide layers on Si(001)" Appl. Phys. Lett. **76**, 436(2000).

123. R. C. Smith, N. Hoilien, C. J. Taylor, T. Z. Ma, S. A. Campbell, J. T. Roberts, M. Copel, D. A. Buchanan, M. Gribelyuk, and W. L. Gladfelter, "Low temperature chemical vapor deposition of ZrO_2 on Si(100) using anhydrous zirconium(IV) nitrate" J. Electrochem. Soc. **147**, 3472 (2000).

124. W. J. Qi, R. Nieh, B. H. Lee, K. Onishi, L. Kang, Y. Jeon, J. C. Lee, V. Kaushik, B. Y. Nguyen, L. Prabhu, K. Eisenbeiser, and J. Finder, "Performance of MOSFETs with ultra thin ZrO_2 and Zr silicate gate dielectrics" Tech. Dig. VLSI Symp. 2000, P.40.

125. C. H. Lee, H. F. Luan, W. P. Bai, S. J. Lee, T. S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kwong, "MOS characteristics of ultra thin rapid thermal CVD ZrO_2 and Zr silicate gate dielectrics**"** Tech. Dig. Int. Electron Devices Meet., 27 (2000).

126. Kazuhiko Yamamoto, Shigenori Hayashi, Masafumi Kubota, and Masaaki Niwa, "Effect of Hf metal predeposition on the properties of sputtered HfO_2/Hf stacked gate dielectrics" Appl. Phys. Lett. **81**, 2053 (2002).

127. K. P. Bastos, J. Morais, L. Miotti, R. P. Pezzi, G. V. Soares, I. J. R. Baumvol, R. I. Hegde, H. H. Tseng, and P. J. Tobin, "Oxygen reaction-diffusion in metalorganic chemical vapor deposition HfO_2 films annealed in O_2" Appl. Phys. Lett. **81**, 1669 (2002).

128. M.-H. Cho, Y. S. Roh, C. N. Whang, K. Jeong, S. W. Nahm, D.-H. Ko, J. H. Lee, N. I. Lee, and K. Fujihara, "Thermal stability and structural characteristics of HfO_2 films on Si (100) grown by atomic-layer deposition" Appl. Phys. Lett. **81**, 472 (2002).

129. P. D. Kirsch, C. S. Kang, J. Lozano, J. C. Lee, J. G. Ekerdt, "Electrical and spectroscopic comparison of HfO_2/Si interfaces on nitrided and un-nitrided Si(100)" J. Appl. Phys. **91**, 4353 (2002).

130. S. Sayan, E. Garfunkei, and S. Suzer, "Soft x-ray photoemission studies of the HfO_2/SiO_2/Si system" Appl. Phys. Lett. **80**, 2135 (2002).

131. V. Cosnier, M. Olivier, G. Théret, and B. André, "HfO_2-SiO_2 interface in PVD coatings" J. Vac. Si. Technol. A, **19**, 2267 (2001).

132. B. H. Lee, L. Kang, R. Nieh, W.-J. Qi, and J. C. Lee, "Thermal stability and electrical characteristics of ultrathin hafnium oxide gate dielectric reoxidized with rapid thermal annealing" Appl. Phys. Lett. **76**, 1926 (2000).

133. M. Gutowski, J. E. Jaffe, C.-L. Liu, M. Stoker, R. I. Hegde, R. S. Rai, and P. J. Tobin, "Thermodynamic stability of high-*k* dielectric metal oxides ZrO_2 and HfO_2 in contact with Si and SiO_2" Appl. Phys. Lett. **80**, 1897 (2002).

134. J. F. Conley, Jr., Y. Ono, R. Solanki, G. Stecker, and W. Zhuang, "Electrical properties of HfO_2 deposited via atomic layer deposition using $Hf(NO_3)_4$ and H_2O" Appl. Phys. Lett. **82**, 3508 (2003).

135. M. J. Cho, J. H. Park, H. B. Park, C. S. Hwang, J. H. Jeong, and K. S. Hyun, "Chemical interaction between atomic-layer-deposited HfO_2 thin films and the Si substrate" Appl. Phys. Lett. **81**, 334 (2002).

136. B. K. Park, J. H. Park, M. J. Cho, C. S. Hwang, K. Y. Oh, Y. K. Han, and D. Y. Yang, "Interfacial reaction between chemically vapor-deposited HfO_2 thin films and a HF-cleaned Si substrate during film growth and postannealing" Appl. Phys. Lett. **80**, 2368 (2002).

137. H. K. Kang, Y. H. Roh, G. H. Bae, D. G. Jung, and C.-W. Yang, "Characteristics of $HfO_2/HfSi_xO_y$ film as an alternative gate dielectric in metal-oxide-semiconductor devices" J. Vac. Sci. Technol. B **20**, 1360 (2002).

138. Y.-S. Lin, R. Puthenkovilakam, and J. P. Chang, "Dielectric property and thermal stability of HfO_2 on silicon" Appl. Phys. Lett. **81**, 2041 (2002).

139. C.-L. Liu, Z. X. Jiang, R. I. Hegde, D. D. Sieloff, R. S. Rai, D. C. Gilmer, C. C. Hobbs, P. J. Tobin, and Shifeng Lu, "Theoretical and experimental investigation of boron diffusion in polycrystalline HfO_2 films" Appl. Phys. Lett. **81**, 1441 (2002).

140. A. Y. Kang, P. M. Lenahan, J. F. Conley, Jr., R. Solanki, "Electron spin resonance

study of interface defects in atomic layer deposited hafnium oxide on Si" Appl. Phys. Lett. **81**, 1128 (2002).

141. H. Harris, K. Choi, N. Mehta, A. Chandolu, N. Biswas, G. Kipshidze, S. Ninkishin, S. Gangopadhyay, and H. Temkin, "HfO_2 gate dielectric with 0.5 nm equivalent oxide thickness" Appl. Phys. Lett. **81**, 1065 (2002).
142. V. V. Afanas'ev, A. Stesmans, F. Chen, X. Shi, and S. A. Campbell, "Internal photoemission of electrons and holes from (100)Si into HfO_2" Appl. Phys. Lett. **81**, 1053 (2002).
143. H. Ikeda, S. Goto, K.a Honda, M. Sakashita, A.Sakai, S. Zaima, and Y. Yasuda, "Structural and electrical characteristics of HfO_2 films fabricated by pulsed laser deposition" Jpn. J. Appl. Phys. **41**, 2476 (2002).
144. Z. Xu, M.Houssa, S. D. Gendt, and M. Heyns, "Polarity effect on the temperature dependence of leakage current through HfO_2/SiO_2 gate dielectric stacks" Appl. Phys. Lett. **80**, 1975 (2002).
145. R. R. Manory, T. Mori, I. Shimizu, S. Miyake, and G. Kimmel, "Growth and structure control of HfO_{2-x} films with cubic and tetragonal structures obtained by ion beam assisted deposition" J. Vac. Sci. Technol. A **20**, 549 (2002).
146. S. Sayan, S. Aravamudhan, B. W. Busch, W. H. Schulte, F. Cosandey, G. D. Wilk, T. Gustafsson, and E. Garfunkei, "Chemical vapor deposition of HfO_2 films on Si(100)" J. Vac. Sci. Technol. A **20**, 507 (2002).
147. Y. J. Cho, N. V. Nguyen, C. A. Richter, J. R. Ehrstein, B. H. Lee, and J. C. Lee, "Spectroscopic ellipsometry characterization of high-*k* dielectric HfO_2 thin films and the high-temperature annealing effects on their optical properties" Appl. Phys. Lett. **80**, 1249 (2002).
148. A. Callegari, E. Cartier, M. Gribelyuk, H. F. Okorn-Schmidt, and T. Zabel,

"Physical and electrical characterization of Hafnium oxide and Hafnium silicate sputtered films" J. Appl. Phys. **90**, 6466 (2001).

149. H. L. Lee, S. H. Jeon, and H. S. Hwang, "Electrical characteristics of a Dy-doped HfO_2 gate dielectric" Appl. Phys. Lett. **79**, 2615 (2001).
150. S. J. Wang, P. C. Lim, A. C. H. Huan, C. L. Liu, J. W. Chai, S. Y. Chow, J. S. Pan, Q. Li, and C. K. Ong, "Reaction of SiO_2 with hafnium oxide in low oxygen pressure" Appl. Phys. Lett. **82**, 2047 (2003).
151. V. V. Afanas'ev, A. Stesmans, and W. Tsai, "Determination of interface energy band diagram between (100)Si and mixed Al-Hf oxides using internal electron photoemission" Appl. Phys. Lett. **82**, 245 (2003).
152. H. Kim, P. C. Mclntyre, and K. C. Saraswat, "Effects of crystallization on the electrical properties of ultrathin HfO_2 dielectrics grown by atomic layer deposition" Appl. Phys. Lett. **82**, 106 (2003).
153. S. J. Wang and C. K. Ong, "Epitaxial Y-stabilized ZrO_2 films on silicon: Dynamic growth process and interface structure"Appl. Phys. Lett. **80**, 2541 (2002).
154. S. J. Wang, C. K. Ong, S. Y. Xu, P. Chen, W. C. Tjiu, J. W. Chai, A. C. H. Huan, W. J. Yoo, J. S. Lim, W. Feng, and W. K. Choi, "Crystalline zirconia oxide on silicon as alternative gate dielectrics"Appl. Phys. Lett. **78**, 1604 (2001).
155. S. Ramanathan, and P. C. Mclntyre, "Ultrathin zirconia/SiO_2 dielectric stacks grown by ultraviolet-ozone oxidation" Appl. Phys. Lett. **80**, 3793 (2002).
156. H. S. Chang, S. Jeon, and H. Hwang, and D. W. Moon, "Excellent thermal stability of $Al_2O_3/ZrO_2/Al_2O_3$ stack structure for metal-oxide-semiconductor gate dielectrics application" Appl. Phys. Lett. **80**, 3385 (2002).
157. C. Zhao, O. Richard, H. Bender, M. Caymax, S. De Gendt, and M. Heyns, E. Young, G. Roedden, O. Van Der Biest, and S. Haukka, "Miscibility of amorphous

ZrO_2--Al_2O_3 binary alloy" Appl. Phys. Lett. **80**, 2374 (2002).

158. A. Stesmans and V. V. Afanas'ev, "Si dangling-bond-type defects at the interface of (100)Si with ultrathin layers of SiO_x, Al_2O_3, and ZrO_2" Appl. Phys. Lett. **80**, 1957 (2002).
159. V. V. Afanas'ev and A. Stesmans, "Hole trapping in ultrathin Al_2O_3 and ZrO_2 insulators on silicon" Appl. Phys. Lett. **80**, 1261 (2002).
160. B.-O. Cho, J. J. Wang, L. Sha, and J. P. Chang, "Tuning the electrical properties of zirconium oxide thin films" Appl. Phys. Lett. **80**, 1052 (2002).
161. S. J. Wang, C. K. Ong, S. Y. Xu, P. Chen, W. C. Tjiu, A. C. H. Huan, W. J. Yoo, J. S. Lim, W. Feng, and W. K. Choi, "Electrical properties of crystalline YSZ films on silicon as alternative gate dielectrics" Semicond. Sci. Technol. **16**, L13 (2001).
162. M. Houssa, V. V. Afanas'ev, A. Stesmans, and M. M. Heyns, "Defect generation in $Si/SiO_2/ZrO_2/TiN$ structures: the possible role of hydrogen" Semicond. Sci. Technol. **16**, L93 (2001).
163. D. A. Muller, and G. D. Wilk, "Atomic scale measurements of the interfacial electronic structure and chemistry of zirconium silicate gate dielectrics" Appl. Phys. Lett. **79**, 4195 (2001).
164. J. P. Chang, and Y.-S. Lin, "Thermal stability of stacked high-*k* dielectrics on silicon" Appl. Phys. Lett. **79**, 3824 (2001).
165. J. P. Chang, and Y.-S. Lin, "Dielectric property and conduction mechanism of ultrathin zirconium oxide films" Appl. Phys. Lett. **79**, 3666 (2001).
166. S. J. Wang, C. K. Ong, L. P. You, and S. Y. Xu, "Epitaxial growth of yittria-stabilized zirconia oxide thin film on natively oxidized silicon wafer without an amorphous layer" Semicond. Sci. Technol. **15**, 836 (2000).
167. T. Yamaguchi, H. Satake, N. Fukushima, and A. Toriumi, "Study on Zr-silicate

interfacial layer of ZrO_2 metal-insulator-semiconductor structure" Appl. Phys. Lett. **80**, 1987 (2002).

168. G. D. Wilk and R. M. Wallace, "Stable zirconium silicate gate dielectrics deposited directly on silicon" Appl. Phys. Lett. **76**, 112 (2000).
169. M. Quevedo-Lopez, M. El-Bouanani, S. Addepalli, J. L. Duggan, B. E. Gnade, M. R. Visokay, M. Douglas, and L. Colombo, "Hafnium interdiffusion studies from hafnium silicate into silicon" Appl. Phys. Lett. **79**, 4192 (2001).
170. J.-H. Lee and M. Ichikawa, "Compositionally graded hafnium silicate studied by chemically selective scanning tunneling microscopy" J. Appl. Phys. **91**, 5661 (2002).
171. B. C. Hendrix, A. S. Borovik, C. Xu, J. F. Roeder, T. H. Baum, M. J. Beven, M. R. Visokay, J. J. Chambers, A. L. P. Rotandaro, H. Bu, and L. Colombo, "Composition control of $Hf_{1-x}Si_xO_2$ films deposited on Si by chemical-vapor deposition using amide precursors" Appl. Phys. Lett. **80**, 2362 (2002).
172. S. Gopalan, K. Onishi, R. Nieh, C. S. Kang, R. Choi, H.-J. Cho, S. Krishnan, and J. C. Lee, "Electrical and physical characteristics of ultrathin hafnium silicate films with polycrystalline silicon and TaN gates" Appl. Phys. Lett. **80**, 4416 (2002).
173. M. R. Visokay, J. J. Chambers, A. L. P. Rotondaro, A. Shanware, and L. Colombo, "Application of HfSiON as a gate dielectric material" Appl. Phys. Lett. **80**, 3183 (2002).
174. R. L. Opila, G. D. Wilk, M. A. Alam, R. B. van Dover, and B. W Busch, "Photoemission study of Zr- and Hf-silicates for use as high-kappa oxides: Role of second nearest neighbors and interface charge" Appl. Phys. Lett. **81**, 1788 (2002).
175. G. D. Wilk, R. M. Wallace, and J. M. Anthony, "Hafnium and zirconium silicates for advanced gate dielectrics" J. Appl. Phys. **87**, 484 (2000).

176. R. I. Hegde, C. C. Hobbs, L. R. Dip, J. Schaeffer, and P. J. Tobin, "Impact of metal-oxide gate dielectric on minority carrier lifetime in silicon" Appl. Phys. Lett. **80**, 3850 (2002).

177. D. A. Neumayer, and E. Cartier, "Materials characterization of ZrO_2-SiO_2 and HfO_2-SiO_2 binary oxides deposited by chemical solution deposition" J. Appl. Phys. **90**, 1801 (2001).

178. S.-Y. Lee, H. Kim, P. C. Mclntyre, K. C. Saraswat, J.-S. Byun, "Atomic layer deposition of ZrO_2 on W for metal-insulator-metal capacitor application" Appl. Phys. Lett. **82**, 2874 (2003).

179. W. L. Liu, P. F. Lee, J. Y. Dai, J. Wang, H. L. W. Chan , C. L. Choy, Z. T. Song and S. L. Feng, "Self-organized Ge nanocrystals embedded in HfAlO fabricated by pulsed-laser deposition applied to floating gate memory" Appl. Phys. Lett. **86**, 013110 (2005).

180. S. Y. Wang, W. L. Liu, Q. Wan, J. Y. Dai, P. F. Lee, L. Suhua, Q. W. Shen, M. Zhang, Z. T. Song, and C. L. Lin, "Investigation of Ge nanocrystals in a metal-insulator-semiconductor structure with a HfO_2/SiO_2 stack as the tunnel dielectric" Appl. Phys. Lett. **86**, 113105 (2005).

181. P. F. Lee, W. L. Liu, Z. T. Song, and J. Y. Dai "Ge nanocrystals embedded in Hf-aluminate high-*k* gate dielectric for floating gate memory application" Proc. SPIE **5650**, 141 (2005).

182. X. B. Lu, P. F. Lee, and J. Y. Dai, "Synthesis and memory effect study of Ge nanocrystals embedded in $LaAlO_3$ high-*k* dielectrics" Appl. Phys. Lett. **86**, 203111 (2005).

183. P. F. Lee, X. B. Lu, J. Y. Dai, H. L. W. Chan, Emil Jelenkovic, and K. Y. Tong, "Memory effect and retention property of Ge nanocrystal embedded Hf-aluminate

high-*k* gate dielectric" Nanotech. **17**, 1202 (2006).

184. Memory Strategies International, "NAND and NOR Nanocrystal Flash Memory - July 2006" (http://www.memorystrategies.com/report/focused/nanocrystal.htm)
185. V. E. Borisenko and S. Ossicini, *What is What in the Nanoworld*, pp.233 – 236 (Wiley-VCH, Weinheim, 2004).
186. V. E. Borisenko and S. Ossicini, *What is What in the Nanoworld*, pp.55 (Wiley-VCH, Weinheim, 2004).

Chapter 2 Experimental Techniques and Background Knowledge

Multiple techniques have been involved in fabricating and characterizing the nanocrystals/high-*k* dielectric embedded structure. In this chapter, the details of the nanocrystal fabrication and film coating techniques and structural and electrical characterizations will be introduced. Physics about the nano-floating gate memory and methodologies to analyze the electrical measurement results will also be presented.

2.1 Thin film fabrication techniques

In this project, pulsed-laser deposition (PLD) is the main technique to grow the high-*k* dielectric and nanocrystals in memory structure. PLD is a proven technique for depositing high quality thin oxide films on different substrates. The PLD system can be used to fabricate films by using a non-volatile target, a multi-component target and even a multi-target for multi-layer or alloy films. Films can be grown by PLD under conditions of ambient gas with a relatively low substrate temperature.

Figure 2.1.1 shows a schematic diagram of a PLD deposition system. During film deposition, a laser beam is focused onto the surface of a rotating target to ablate the target materials. By modifying different parameters, such as the substrate temperature, oxygen ambient, laser frequency and fluence, films with different structures can be deposited.

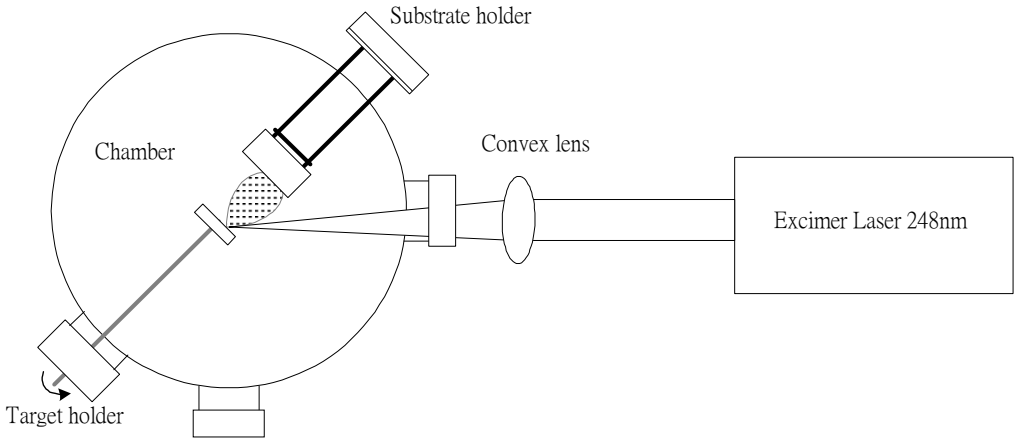


Figure 2.1.1 Schematic diagram of the PLD setup.

The term pulsed-laser deposition (or ablation) (PLD) is commonly employed to denote the process of vaporizing a solid phase material with a pulsed-laser. Smith and Turner (1965) [1] first introduced lasers to vaporize materials and obtain thin films as a deposit. At that time, it was found that the required thermal energy to evaporate the material arises when a focused laser beam irradiates the material. The driving force to utilize pulsed-laser for the deposition of a layer of film is the successful deposition of high temperature superconducting films with desired properties (Dijkkamp 1987) [2-4].

When the target material is irradiated by high fluence laser energy, a luminous plasma cloud which is normal to the target surface (a plume) containing particles such as ions, atoms, molecules, clusters and even particulates will be formed. These particles, with a translational energy of about 10-100 eV, will finally arrive at the substrate surface and, consequently, a layer of film will be deposited. The thermally evaporated target material consists of various compound substances enabling the deposition of stoichiometric thin films. Compared to other physical deposition techniques, one of the advantages for PLD is that the thin films deposited usually possess the same stoichiometry as the target materials [4].

Based on the microstructure, the films deposited by PLD can be categorized into three types: epitaxial, polycrystalline and amorphous. Epitaxy refers to the phenomenon of film growth where a fixed orientation relation between the structure of the film and the substrate exists. In particular, it commonly denotes a single crystalline layer grown on a single crystal surface. If the single crystalline film and the single crystalline substrate are of the same material, we call the growth homoepitaxy. If the film and the substrate are of different materials, we call the growth heteroepitaxy. A film with randomly oriented grains is known as polycrystalline. In an amorphous film, the atoms only have a short-range order but no long-range order. Therefore, no crystal structure and grains can be identified. The process of film growth is usually described by the following three different modes (Fig. 2.1.2) [5-9]:

1. Volmer-Weber, three-dimensional island growth. The deposited atoms are more strongly bonded to each other than they are to the substrate.

2. Frank-van der Merwe, two-dimensional full-monolayer growth. This is a layer-by-layer growth mode. The atoms of the deposited material are more strongly attracted to the substrate than they are to themselves.

3. Stranski-Krastinov, two-dimensional growth of full monolayers followed by the nucleation and growth of three-dimensional islands. This is also known as the layer-plus-island growth mode.

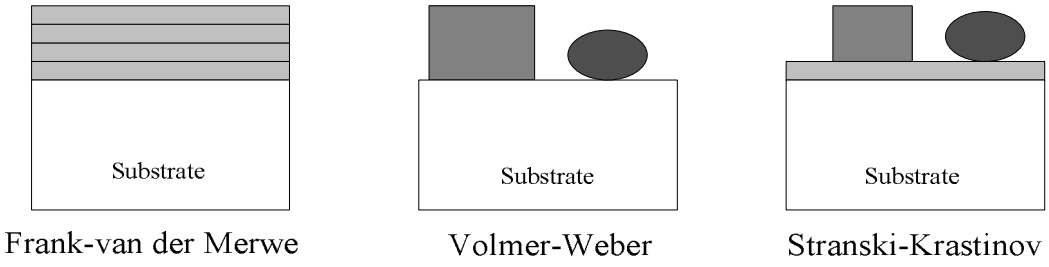


Figure 2.1.2 Three modes of film growth [6,8-9]. Layer-by-layer (Frank-Van der Merwe) growth consists of deposition of one monolayer at a time and results in a very smooth epitaxial film. Island (Volmer-Weber) growth results in the formation and growth of isolated islands. Mixed (Stranski-Krastanov) growth consists of island growth after the first monolayer forms successfully.

Parameters that alter the film properties

When films are deposited in vacuum, the effect of the target-to-substrate distance is mainly reflected in the angular spread of the ejected flux. In general, the particulate trajectories are more divergent when a defocused laser beam is used, as opposed to convergent jet for a tightly focused beam. However, when a PLD experiment is done in a poor vacuum, with an ambient gas, or at a substantially large target-to-substrate distance at which particulates can coalesce, the appearance of the particulates may be significantly different, depending on the position of the substrate [10].

The specific effects of target-to-substrate distance and ambient pressure are interrelated. Due to the increased numbers of collisions between the laser-produced plume and the background gas, the plume dimension decreases as the background gas pressure increases. Dyer *et al.* (1990) [11] have shown that E/P_0 is the scaling parameter for plume range, where E is the laser-pulse energy, and P_0 is the background gas pressure. The length of the plume is $L \propto \left(E / P_0 \right)^{1/3\gamma}$, where γ is the ratio of the specific heats of the elements in the plume. For an ambient pressure of 35 mTorr and a laser fluence of 4J/cm^2, the plume range L corresponds to approximately 5.5 cm [12]. When the

target-to-substrate distance is much smaller than L, there is no big difference in particulate size and density. As the target-to-substrate distance increases, the proportion of smaller particulates decreases, and a few larger particulates appear [13], indicating merging during flight. Once the substrate is located far beyond ~*L*, the adhesion to the substrate of the ejected matter, including the particulates and atomic species, is poor.

The use of an ambient gas is mainly to compensate for some loss of a constituent element such as oxygen or nitrogen in ceramics. It mainly affects the oxygen content of the deposited thin film. For example, the deposited oxide tends to be deficient in oxygen when the ablation experiment is done in vacuum. When a laser ablation deposition experiment is done in vacuum, there are virtually no collisions between the ejected species before they reach the substrate. Thus, the growth of the epitaxial thin film and the control of the crystal structure of the thin film can be done by varying the ambient gas with suitable values.

The surface mobility of the adatoms is greatly affected by substrate temperature. One of the possible effects is that metastable microstructures will be formed as there is insufficient thermal energy at very low temperature [14].

Investigation of the structural properties and stoichiometry of the layers, deposited at different conditions (substrate temperature, substrate-target distance and laser pulse energy) has shown that there is a critical substrate temperature, T_c, below which the structure of the films is not completely crystallized and the film composition deviates significantly from the stoichiometric one [15-16].

2.2 Nanocrystal growth

Controlling the location and the distribution of nanocrystal charge-storage nodes in the dielectric is crucial for nanocrystal memory. Ge nanocrystals can be synthesized by various methods, including Ge ion implantation [17-20], oxidation of SiGe [21-22], electron-beam evaporation [23-27], co-sputtering [28-35], molecular beam epitaxy [36-40], chemical vapor deposition [41-45], pulsed-laser deposition [46-48]. In this project, PLD is the main technique to grow Ge nanocrystals. By controlling the deposition time and temperature, isolated Ge nanocrystals can be formed by self-organized process.

Another approach to fabricate nanocrystals is through nanocluster beam source. Nanoclusters are particles with size in a range of a few to a few hundreds of Angstrons built by a number of atoms or molecules by means of physical or chemical bondings. The physical and chemical properties of the clusters are related to the number of atoms contained and the size of the clusters. Because of the size effect, the nanoclusters can be used to make nanodevices and are promising in a wide variety of applications in microelectronics. A large number of methods have been proposed for cluster production and assembly, and devices based on the nanomaterials have been demonstrated. There are many different kinds of means to fabricate nanoclusters, such as laser ablation of solid or liquid target, thermal evaporation, arc and ion sputtering etc. Among these methods, ion sputtering can be applied to almost any kind of materials from conductive to nonconductive (if RF-sputtering is used). By changing the sputtering parameters, nanoclusters with different size distributions and crystallinity (crystallized or amorphous) can be obtained. Compared to other methods, magnetron sputtering has higher rate in generating nanoclusters and thus possesses higher growth rate. In addition,

nanocluster source by magnetron sputtering method has been minimized and commercialized and can be attached to other film coating systems, either physical vapor deposition (PVD) or chemical vapor deposition (CVD).

2.3 Structural characterization

In this section, general description of characterization methods for both imaging (microscopy) and analysis (spectroscopy) is given. Some of the characterization techniques employed for the investigation of nanostructures will be discussed in the subsequent section of this chapter.

It is necessary to consider what information is required about a specimen and at what image resolution before employing a particular characterization technique. Based on our progress of research experiment, areas of concerns are as follow:

(1) Morphology and microstructure of the thin film and nanocrystals,

(2) Size, density and uniformity of nanocrystals.

The as-grown Ge nanocrystals and the cross-section of trilayer structures were investigated by high-resolution transmission electron microscopy (HRTEM) using JEOL 2010 electron microscope equipped with energy dispersive X-ray (EDX) analysis. Atomic force microscopy (AFM) and scanning electron microscope (SEM) were used to characterize the mean diameter and average density of nanocrystals.

2.4 Memory effect characterization

The memory effect of Ge-nanocrystal floating gate capacitors was characterized by capacitance-voltage (*C-V*), and capacitance-time (*C-t*) measurements using an Agilent HP4294A impedance analyzer. Leakage current density of the capacitors was characterized by means of Keithley 2410 source meter.

2.4.1 *C-V* characterization

The MOS capacitor is used to monitor the integrated circuit fabrication and to study the electrical properties of the MOS system. The MOS capacitor has the advantages of simplicity of fabrication and analysis by measuring its *C-V* characteristics. During the *C-V* measurement, the metal electrode should be made as small as possible to minimize leakage current which may greatly affect the accuracy. The following figure is a kind of real case that we come across mostly during the fabrication of the MOS capacitor. A thin layer of SiO_2 is usually present between the gate dielectric and the Si substrate.

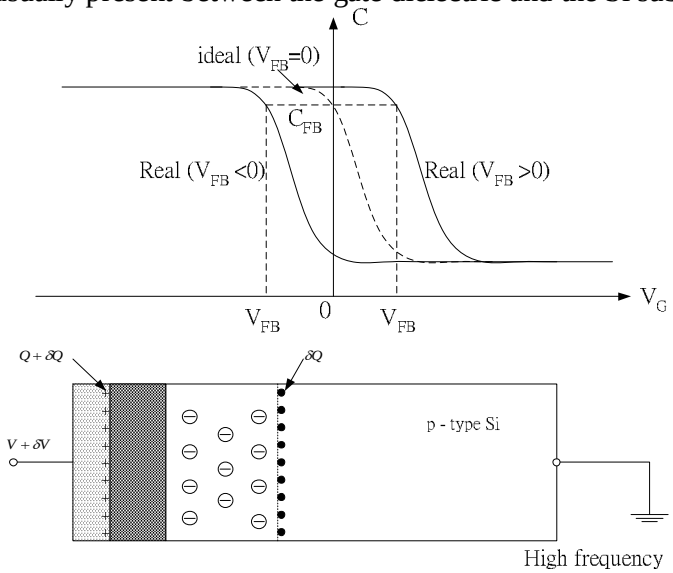


Figure 2.4.1 High frequency *C-V* curves and MOS block diagram.

C-V characteristics reveal the variation in the differential capacitance $C = \frac{dQ}{dV}$ of the MOS capacitor as a function of the gate bias voltage. In Fig. 2.4.1, the flat-band capacitance C_{FB} corresponds to the flat-band gate voltage, V_{FB} (In an ideal MOS system, V_{FB} is zero). C_{FB} is useful in determining the V_{FB} in a real MOS system. The *C-V* curve of a real MOS capacitor shifts in an amount of the "flat-band voltage" with reference to an ideal *C-V* curve. Once a *C-V* curve is obtained from the measurement, V_{FB} can be deduced from the measured C_{FB}. V_{FB} equals a group of values that may be found experimentally.

Figure 2.4.2 is a block diagram represents the memory effect during electron injection from the Si substrate. A counter-clockwise loop is formed after the bias voltage sweep. The resulting stored charge screens the gate charge and reduces the conduction in the inversion layer, i.e. it effectively shifts the threshold voltage of the device to be more positive, whose magnitude for a single electron per nanocrystal is approximately given by [49-50]:

$$\Delta V_T = \frac{q n_{well}}{\varepsilon_{ox}} \left(t_{cntl} + \frac{1}{2} \frac{\varepsilon_{ox}}{\varepsilon_{Si}} t_{well} \right)$$

Here, ΔV_T is the threshold voltage shift, t_{cntl} is the thickness of the control oxide under the gate, t_{well} is the linear dimension of the nanocrystal well, ε's are the permittivities, q is the magnitude of electronic charge, and n_{well} is the density of nanocrystals [49-50].

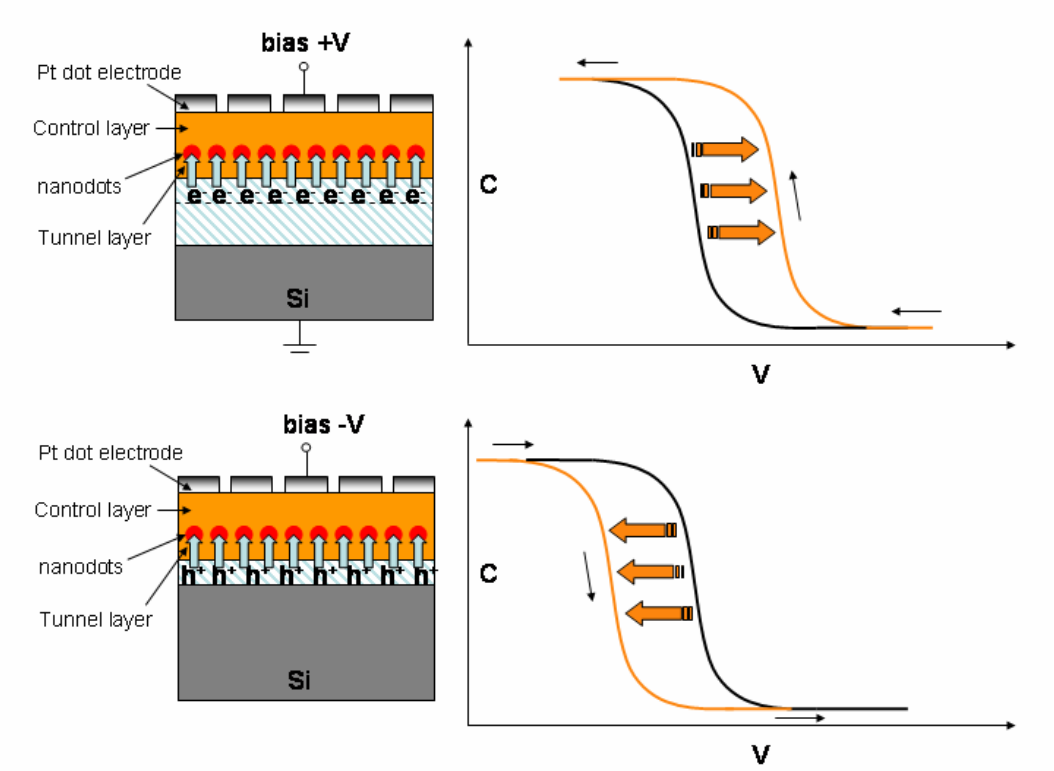


Figure 2.4.2 Diagram of a *C-V* curve of a nano-floating memory capacitor. Counter-clockwise loop represent an electron injection from the Si substrate.

2.4.2 *C-t* characterization

According to ITRS [51], the retention properties of a floating gate memory device can be characterized at 85°C by performing a flat-band voltage measurement against time. Another characterization method is employed in this project for elucidating the discharging mechanism of charges in nanocrystals, namely, the capacitance decay or capacitance transient measurement [52-54]. This is a time dependent characterization method and constant gate bias voltage is applied across the capacitors at the initial flat-band voltage (deduced from *C-V* measuremt). By the indication of capacitance decay as a function of discharging time, several conclusions can be drawn:

1. The way for charge carriers to escape is direct tunneling from the nanocrystals towards the substrate. This is due to low gate bias and the relatively low stored charge quantity as a result of low electric field in the oxide [52].
2. The general feature of the decay curves consists of two distinct decay regimes. The first is an initial fast decay and the other is the later slow decay. The Ge-rich regions give a lateral channel that allows charge transport along the nanocrystal layer. This contributes to the fast initial capacitance decay in the *C-t* measurement. On the other hand, some of the nanocrystals may be well localized by chance. In this case, the only possibility of charge loss is tunneling out via the tunneling barrier. Thus, the stored charges in the localized nanocrystals will exhibit long-term retention property. This effect results in the slow capacitance decay [53].
3. Huang *et al.* [54] suggested a model regarding the tunneling mode and retention characteristic. It is well known that the tunneling transparency depends on the electric field in the tunnel oxide [55]. When the gate voltage is held at the initial flat-band voltage after the nanocrystals are charged, the initial electric field across the tunnel oxide is due to the “fixed charge”. A built-in field will be formed and

hinder the discharging of other stored electrons. This build-in field may improve the retention properties significantly.

In this project, the memory data retention characteristics at room temperature for the trilayer memory capacitors were characterized by using capacitance-time (*C*-*t*) measurement. The memory capacitor specimens were first charged for 10-20 seconds at a bias voltage of 10-20 V. Then, a particular bias voltage was chosen (kept at initial flat-band voltage) for measuring the capacitance decay.

2.4.3 *I*-*V* characterization

Leakage current of a MOS capacitor is a critical electrical property which affects the retention property of a nano-floating gate memory capacitor. The leakage current is additional information for evaluating the MOS capacitor and memory property. The measurements of the current-voltage characteristics of the structures were performed with a Keithley 2410 source meter.

2.5 Background knowledge

Some background knowledge and information need to be clear before acquiring useful information from the experimental results obtained. In this section, some of the basic theories which are necessary in explaining the physics behind the experimental results achieved throughout this project will be briefly stated.

2.5.1 Flash memory

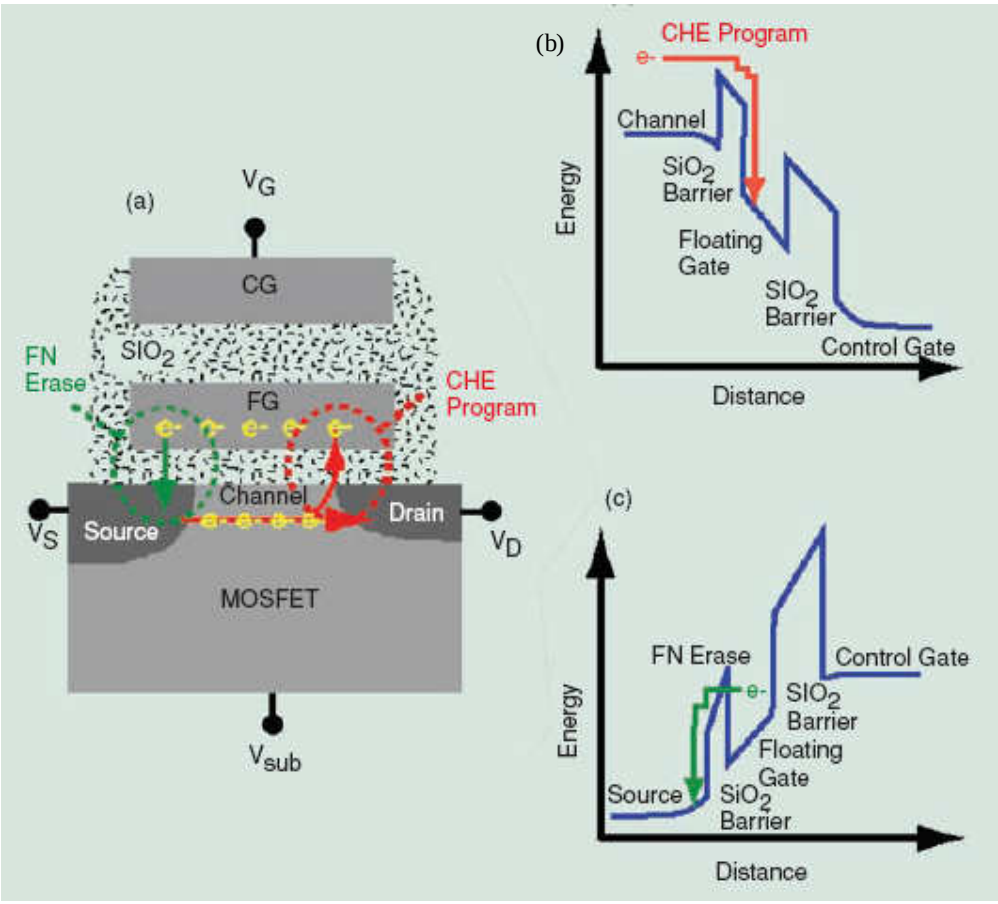


Figure 2.5.1 (a) Schematic of a basic ETOX (EPROM Tunnel Oxide) flash memory device showing the program and erase operations. (b) Electron flow during programming by CHE injection. (c) Electron flow during erasing by FN tunneling to the source. [57]

A standard commercial flash memory device is similar to the Intel EPROM tunnel oxide (ETOX) structure as shown in Fig. 2.5.1 (a) [57]. The floating gate (FG) is embedded in oxide matrix (can be SiO_2 or ONO) and situates between the control gate (CG) and the channel.The MOSFET modulates the electron current flow between the source and drain and forms the channel. Charges or data are stored in the electrcically isolated (disconnect from terminal voltage) floating gate and is being retained when the power supply is disconnected.

The flash memory device is programmed when electrons are stored in the floating gate by channel hot electron (CHE) injection or Fowler-Nordheim (F-N) tunneling [56-57]. These negatively charged electrons screen the channel from the control gate electric field. This action translates into a higher control gate voltage (V_G) and thus, a threshold voltage (V_T) increase for the operation of MOSFET. The net negative charges which remain in the floating gate shifts the V_T to a positive value. Memory is erased by removing the stored electrons mainly by F-N tunneling and restoring V_T to its original value.

The V_T shift between the programmed and erased states is denoted by a quantity known as the “memory window”. Figure 2.5.4 shows a typical current versus gate voltage characteristic of an erased floating gate memory device and its V_T shift when the device is programmed. The memory-state for the device can be determined by measuring the current in the MOSFET when a control gate bias is applied within the memory window [56-57].

2.5.2 Tunneling mechanisms in flash memory

(A) CHE programming

All floating gate memory device can be programmed by channel hot-carrier injection. The method of programming is by hot-electron injection for n-type memory device built on p-substrates and by hot-hole injection for p-type memory device built on n-substrates. Figure 2.5.1(b) illustrates the electron energy as a function of the vertical distance from the control gate to the channel near the drain region of the MOSFET. The SiO_2 dielectric is a barrier (~3.2 eV) for the low-energy electrons in the Si channel, the floating gate and the control gate.

The first SiO_2 barrier between the floating gate and the channel prevents electrons from leaking into the channel. A second barrier between the floating gate and the control gate prevents electrons from escaping to the control gate. Under typical programming conditions (usually 10 to 13 V), large positive drain and control gate biases are applied to produce a large electric field. This field sets the conditions for a current to flow from the source to the drain.

The memory cell is programmed by charging the floating gate via the injection of hot-electrons from the drains pinch-off region. The hot-electrons get their energy from the voltage applied to the drain of the memory cell. They are accelerated by the lateral electric field along the channel into even higher energy surrounding the drain depletion region. Once these electrons gain sufficient energy, they can overcome the energy barrier of 3.2 eV between the silicon substrate and the dielectric layer or gate oxide barrier and reach the floating gate.

This programming method is known as channel hot electron (CHE) injection: the hot electrons refer to the highly energetic electrons induced by the high electric field.

Upon overcoming the barrier, the electrons rapidly lose their kinetic energy through interactions with the atomic lattice vibration and other electrons, and finally are trapped in the floating gate [57].

(B) FN erase

Under erasure, a large negative control gate voltage is applied to turn the channel current off. Figure 2.5.1(c) shows the electron energy as a function of the vertical distance from the control gate to source of the MOSFET. The applied electric field between the control gate and the source increases the slope of the energy barrier, effectively thinning the barrier top.

At the same time, the high field gives kinetic energy to some of the floating gate electrons. It moves them energetically up towards the SiO_2 top where the electrons experience a reduced barrier to tunnel quantum-mechanically to the source. The term, tunnel, refers to the quantum process of a particle penetrating a potential barrier in a wave-like fashion, even when it does not have sufficient kinetic energy to overcome it classically [57].

This mechanism of high-field-assisted tunneling is known as Fowler-Nordheim (FN) tunneling (Fig. 2.5.1 (c)). Once the tunneling electrons penetrate the source, they rapidly thermalize through interactions with the source electrons and the crystal lattice [57].

Fowler-Nordheim (FN) tunneling describes charge carrier transport through insulators. The current density is

$J = CE^2 \exp\left(-\frac{E_0}{E}\right)$, where C and E_0 are constants in terms of effective mass and barrier height, E is the electric field in the insulator (Vm^{-1}) [58].

2.5.3 Background knowledge of nano-floating gate memory

Nanocrystals, as mentioned in Chaper 1, are extremely small nanoparticles or nanodots of atoms and usually range from 5 to 10 nm in diameter. They can be grown, deposited or implanted into the dielectric (Fig. 2.5.2 (a)). Nanocrystals can be deposited in a two-dimensional (2-D) layer at a fixed distance from the Si channel separated by a thin tunnel oxide (Fig. 2.5.2 (b)). By optimizing the growth condition of nanocrystal deposition to just one layer and controlling the thickness of the control gate dielectric oxide, charge leakage to the control gate from the storage nodes can be effectively prevented. [57].

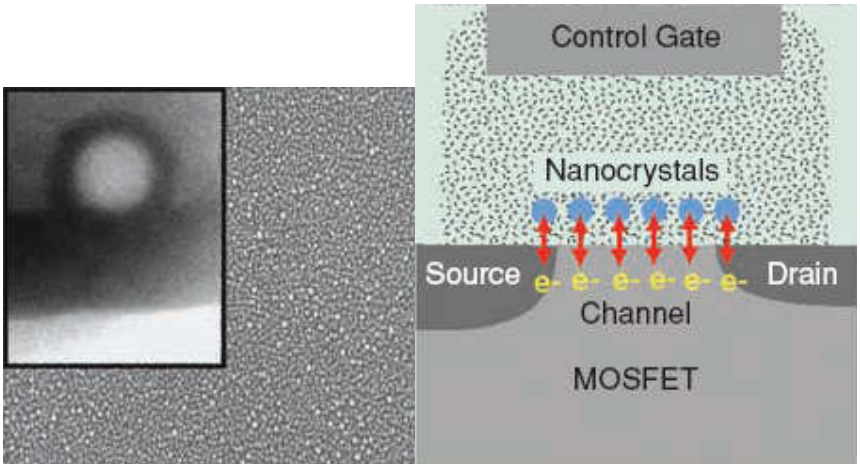


Figure 2.5.2 (a) A scanning electron micrograph of dense Si-nanocrystal coverage required for reliable flash memory operation. Inset: An energy-filtered transmission electron micrograph of a single nanocrystal, encapsulated in an oxide shell, on a tunnel barrier. (b) An illustration of a nanocrystal floating gate memory. [57]

Moreover, electron or hole energy states are energetically deeper in the nanocrystal wells. For example, the energy level of traps is typically 1-2 eV below the Si_3N_4 conduction band, while the electron ground state in nanocrystals could exceed 3 eV below the SiO_2 conduction band [57]. Hence, conduction between the well distributed

nanocrystals storage nodes can be totally prevented when the average separation of each nanocrystals is larger than 5nm. Besides that, the transport of charges is restricted to carrier exchange with the Si channel. The increased quantum confinement effects and the reduction in leakage imply that improved scalability of tunnel oxide can be achieved. Thus, lowering operating voltages and/or increase in operating speed can be achieved without sacrificing non-volatility. With a thinner tunnel oxide, direct quantum-mechanical tunneling can be exploited as a transport mechanism for programming and erasing the charges in the nodes.

The difference between direct quantum-mechanical tunneling, hot electron injection and FN tunneling is illustrated in Fig. 2.5.3. In direct tunneling, electrons tunnel through the full barrier thickness with a rate strongly dependent on the quantum penetration of the electron wave into the barrier. As for FN-tunneling, high-energy electrons tunnel through a narrower and lower barrier because of the high electric field. Hot-electron injection refers to highly energetic electrons induced by the high electric field overcoming the tunnel oxide barrier [57].

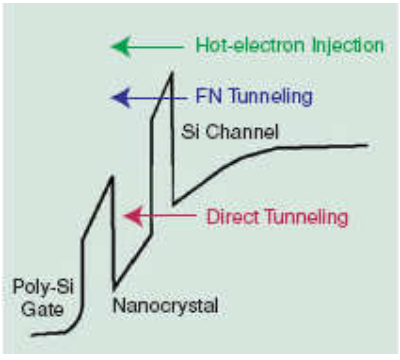


Figure 2.5.3 Energy band edge schematic illustrating direct quantum mechanical tunneling compared to other injection mechanism.[57]

Therefore, direct tunneling is typically a low-field process (3-4 V) compared to both channel hot-electron injection and FN-tunneling (10-12 V) [57]. The reduced program and erase voltages ease the stress on the tunnel oxide, thereby dramatically reducing dielectric leakage. Until now, nanocrystal floting gate memory devices can endure more than a million repeated program/erase cycles without suffering any apparent degradation of their memory window states [49-50]. Figure 2.5.4 illustrates the write, read and erase processes of a nano-floating gate memory cell.

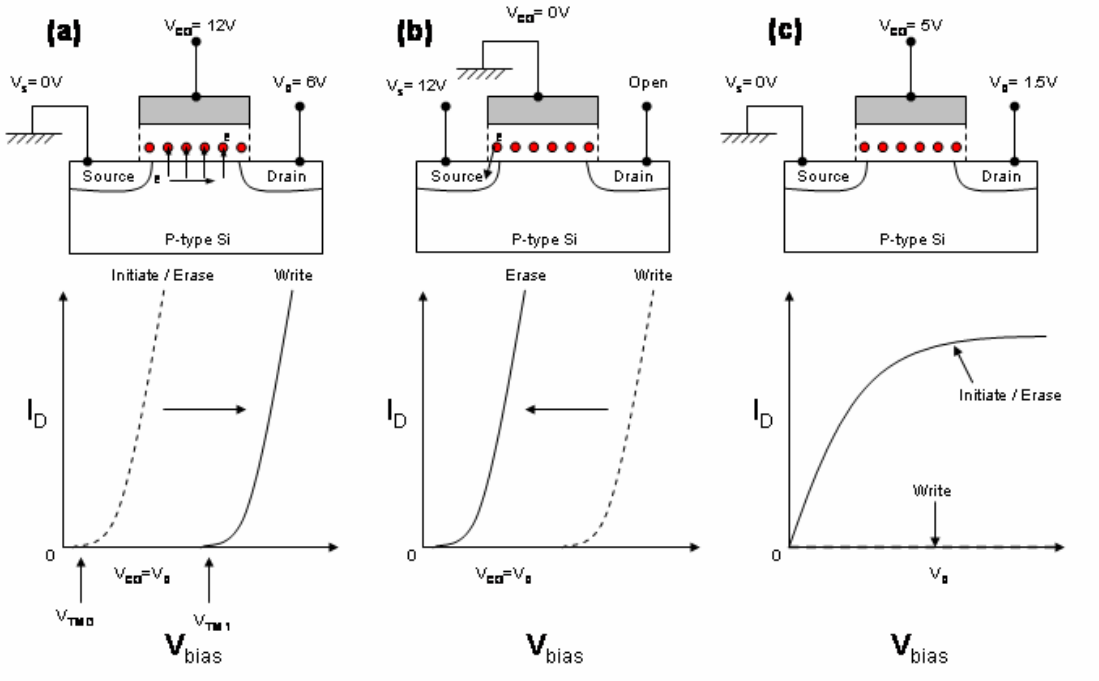


Figure 2.5.4 Schematic diagram describing the (a) write, (b) erase and (c) read processes of a nano-floating gate memory cell.

The most spectacular feature of nanocrystal memory is the demonstration of single electron/hole charging phenomena at room temperature [57]. This is a manifestation of the Coulomb blockade effect shown by Kim *et al.* [59] and Welser *et al.* [60].

The Coulomb blockade effect ensures discrete programming for every electron written into the floating gate charge-storage node for a given programming voltage, leading to accurate multi-charge-state self-convergent programming. Furthermore, the MOSFET channel is screened from the control gate by the high-density nanocrystals layer, and producing discrete V_T shifts. The self-convergent programming and accurate V_T shifts may be useful for realizing a quantum multi-bit memory [57].

For nanocrystal floating gate memory to be a reproducible technology suitable for mass production, a few technical issues remain to be solved. For example, a clear understanding of the mechanisms responsible for additional trapping due to local defects in nanocrystals and their influence on memory performance is essential. Moreover, achieving high-density nanocrystal coverage ($> 1 \times 10^{12}$ cm^{-2}) to enlarge the memory window, and controlling disturbances and static or thermal fluctuations occurring during the low-voltage write/read/erase operations are crucial. Finally, manufacturing issues, such as the control of wafer-level nanocrystal density distribution, will become prominent as this technology matures [57].

2.5.4 Simple model for storage charge density calculation

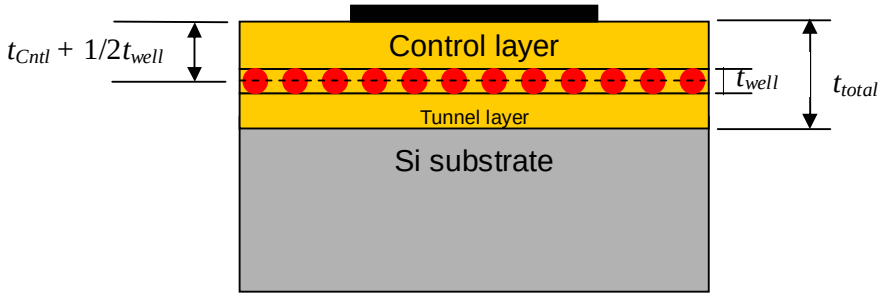


Figure 2.5.5 Schematic diagram of the trilayer nano-floating gate memory MOS capacitor.

In this project, the Tiwari's model was used to calculate storage charge density based on the flat-band voltage shift from the *C-V* loops measurement. Since there is no detailed explanation from the literatures, in this section, the detailed derivation of the model based on my understanding is introduced.

Tiwari *et al.* [49-50] suggested that the injection of an electron occurs from the inversion layer via direct tunneling when the control gate is forward biased with respect to the source and drain. The resulting stored charge screens the gate charge and reduces the conduction in the inversion layer, i.e. it effectively shifts the threshold voltage (ΔV_T) of the device to be more positive. It is assumed that a single electron is stored per nanocrystal, and the nano-floating gate layer is treated as a Si layer with thickness of t_{well} and dielectric constant as ε_{Si}. All the stored charges distribute in the middle of the floating gate layer.

Shi *et al.*[61] have proposed a model for the effect of traps on the long-term charge characteristic. A model of deep trapping centers including three-dimensional quantum confinement and Coulomb charge effect is developed to successfully explain the observed long-term charge retention behaviors. Applying a positive pulse voltage,

the V_{FB} shifts to the positive direction, reflecting that electrons are injected into the nanocrystals. The V_{FB} decays subsequently to its initial value with a logarithmic time dependence in the charge retention mode.

In writing mode, the charge transport mechanism changs from direct tunneling into Fowler-Nordheim (F-N) tunneling [62]. This gives rise to enhanced electron injection from the substrate into Si nanocrystals, resulting in more efficient programming. This event takes place in much lower programming voltage in HfO_2 than SiO_2 because the onset of the F-N tunneling depends on the electron barrier height [63], and for HfO_2 the value is 1.5 eV [64]which is much smaller than that in SiO_2 (3.5 eV).

A. Estimation of flat-band voltage shift from density of nanocrystal (*N*)

(1) One Si or Ge dot is stored with one electron

(2) Charge is stored in the middle layer of the dots

To compensate the charges stored in the nano-floating gate layer, a voltage ΔV_{FB} is applied across the capacitors. The series capacitance from top electrode to the middle of the floating gate, C_Δ is:

$$\frac{1}{C_\Delta} = \frac{1}{C_{Cntl}} + \frac{1}{C_{1/2\,well}} = \frac{t_{Cnt1}}{\varepsilon_{ox}} + \frac{1/2\, t_{well}}{\varepsilon_{well}}$$

For a unit area, the change of flat-band voltage due to the *Nq* stored charges is:

$\Delta V_{FB} = \frac{Nq}{C_\Delta}$, where *q* is the charge of one electron and *N* is the number of dots.

These two equations result in

$$\therefore \Delta V_{FB} = \Delta V_T = Nq\left(\frac{t_{Cnt1}}{\varepsilon_{ox}} + \frac{t_{well}}{2\varepsilon_{well}}\right) = \frac{qN}{\varepsilon_{ox}}\left(t_{Cnt1} + \frac{1}{2}\frac{\varepsilon_{ox}}{\varepsilon_{well}}t_{well}\right) \quad (1)$$

where ε_{well} is assumed to be equal to ε_{Si} (dielectric constant of Si nanodots). But, in fact it should be an average of ε_{Si} and ε_{ox} (SiO_2 or HfO_2, etc).

Equivalently, ΔV_{FB} can be set to be equal to ΔV_T as ΔV_{FB} is one of the components that contributes to ΔV_T.

B. Determination of stored charge density (*n*) from *C-V* hysterisis loop

Based on Kim's model [65], if we assume in the "well" layer, more area is the dielectric oxide, $\varepsilon_{well} = \varepsilon_{ox}$. Then, (1) changed to:

$$\Delta V_{FB} = \frac{qn}{\varepsilon_{ox}}\left(t_{Cntl} + \frac{1}{2}t_{well}\right) \quad (2)$$

From (2)

$$n = \frac{\varepsilon_{ox}\Delta V_{FB}}{q(t_{Cntl} + \frac{1}{2}t_{well})}, \text{ substitute } C_{ox} = \frac{\varepsilon_{ox}A}{t_{total}}$$

where C_{ox} is the accumulation capacitance, and A is unit area A=1, $\varepsilon_{well} = \varepsilon_{ox}$.

$$n = \frac{C_{ox}\Delta V_{FB}}{q(t_{Cntl} + \frac{1}{2}t_{well})/t_{total}}.$$

Define $t_{ratio} = \dfrac{t_{Cntl} + \frac{1}{2}D_{nc}}{t_{total}}$ where $D_{nc} = \dfrac{1}{2}t_{well}$ is the diameter of the nanocrystal, then

$$n = \frac{C_{ox}\Delta V_{FB}}{qt_{ratio}}. \text{ [65]}$$

From this equation, ΔV_{FB} and C_{ox} can be determined from *C-V* curve.

References

1. H. M. Smith and A. F. Turner, "Vacuum deposited thin films using a Ruby laser" Appl. Optics **4**, 147 (1965).
2. D. Dijkkamp, A. S. Gozdz, T. Venkatesan, and X. D. Wu, "Evidence for the Thermal Nature of Laser-Induced Polymer Ablation" Phy. Rev. Lett. **58**, 2142 (1987).
3. D. H. A. Blank, L. M. Doeswijk, K. Karakaya, G. Koster and G. Rijnders, "Pulsed laser deposition of dielecteics". In *High-k gate dielectrics*, edited by M. Houssa pp.89 (Institute of Physics, 2004).
4. K. S. Sree Harsha, *Principles of Physical Vapor Deposition of Thin Films*, 1st Ed. pp. 431 (Elsevier, Oxford, 2006).
5. J. S. Horwitz, and J. A. Aprague, "Film nucleation and film growth in pulsed laser deposition of ceramics". In *Pulsed Laser Deposition of Thin Films*, edited by Douglas B. Chrisey and Graham K. Hubler pp.231-235 (John Wiley & Sons, 1994).
6. G. K. Hubler, "Comparison of vacuum deposition techniques". In *Pulsed Laser Deposition of Thin Films*, edited by Douglas B. Chrisey and Graham K. Hubler pp.331 (John Wiley & Sons, 1994).
7. M. Ohring, *Materials Science of Thin Film -Deposition and structure*, 2nd Ed. (Academic Press, New York, 1991).
8. B. Lewis, and J. C. Anderson, *Nuclear and Growth of Thin Films*, (Academic Press, New York, 1978)
9. J. A. Venables, G. D. T. Spiller, and M. Hanbucken, "Nucleation and growth of thin-films" Rep. Prog. Phys. **47**, 399 (1984).

10. L.-C. Chen, "Particulates generated by pulsed laser deposition". In *Pulsed Laser Deposition of Thin Films*, edited by Douglas B. Chrisey and Graham K. Hubler pp.188 (John Wiley & Sons, 1994).
11. P. E. Dyer, R. D. Greenough, A. Issa, and P. H. Key, "TEA CO_2-laser ablation studies of Y-Ba-Cu-O" Appl. Surf. Sci. **43**, 387 (1989).
12. G. A. Smith, L. C. Chen, and M. C. Chuang, "Effects of processing parameters on KrF excimer laser ablation deposited ZrO_2 films" Mater. Res. Soc. Symp. Proc. **235**, 843 (1992).
13. Y. Nishikawa, K. Tanaka, and Y. Yoshida, "Morphology of particles generated from thin-film by excimer laser ablation" J. Jpn. I. Met. **55**, 581 (1991).
14. M. G. Norton, and C. B. Carter, "On the optimization of the laser ablation process for the deposition of $YBa_2Cu_3O_7$-Delta thin films" Physica C **172**, 47 (1990).
15. S. Metev, "Process characteristics and film properties in pulsed laser deposition". In *Pulsed Laser Deposition of Thin Films*, edited by Douglas B. Chrisey and Graham K. Hubler pp. 262-263 (John Wiley & Sons, 1994).
16. S. Metev, and M. Sendova, *Trends in Quantum Electronics*, 1033 (SPIE, Bellingham).
17. H. Hanafi, S. Tiwari, and I. Khan, "Fast and long retention-time nano-crystal memory" IEEE Trans. Electron Devices **43**, 1553 (1996).
18. S. Duguay, J. J. Grob, A. Slaoui, Y. Le Gall, and M. Amann-Liess, "Structural and electrical properties of Ge nanocrystals embedded in SiO_2 by ion implantation and annealing" J. Appl. Phys. **97**, 104330 (2005).
19. C. J. Park, H. Y. Cho, S. Kim, Suk-Ho Choi, R. G. Elliman, J. H. Han, Chungwoo Kim, H. N. Hwang, and C. C. Hwang, "Annealing temperature dependence of capacitance-voltage characteristics in Ge-nanocrystal-based nonvolatile memory

structures" J. Appl. Phys. **99**, 036101 (2006).

20. C. J. Park, K. H. Cho, W.-C. Yang, H. Y. Cho, Suk-Ho Choi, R. G. Elliman, J. H. Han, and Chungwoo Kim, "Large capacitance-voltage hysteresis loops in SiO_2 films containing Ge nanocrystals produced by ion implantation" Appl. Phys. Lett. **88**, 071916 (2006).
21. Y.-C. King, T.-J. King, and Chenming Hu, "MOS memory using germanium nanocrystals formed by thermal oxidation of $Si_{1-x}Ge_x$" IEEE IEDM Tech. Dig., 115 (1998).
22. Y.-C. King, T.-J. King, and Chenming Hu, "Charg-trap memory device fabricated by oxidation of $Si_{1-x}Ge_x$" IEEE Trans. Electron Devices **48**, 696 (2001).
23. T. Kobayashi, T. Endoh, H. Fukuda, S. Nomura, A. Sakai, and Y. Ueda, "Ge nanocrystals in SiO_2 films" Appl. Phys. Lett. **71**, 1195 (1997).
24. C. L. Heng, L. W. Teo, Vincent Ho, M. S. Tay, Y. Lei, W. K. Choi, and W. K. Chim, "Effects of rapid thermal annealing time and ambient temperature on the charge storage capability of SiO_2/pure Ge/rapid thermal oxide memory structure" Microelectronic Eng. **66**, 218 (2003).
25. C. L. Heng, and T. G. Finstad, "Electrical characteristics of a metal-insulator-semiconductor memory structure containing Ge nanocrystals" Physica E **26**, 386 (2005).
26. Q. Wan, C. L. Lin, W. L. Liu, and T. H. Wang, "Structural and electrical characteristics of Ge nanoclusters embedded in Al_2O_3 gate dielectric" Appl. Phys. Lett. **82**, 4708 (2003).
27. Q. Wan, N. L. Zhang, W. L. Liu, C. L. Lin, and T. H. Wang, "Memory and negative photoconductivity effects of Ge nanocrystals embedded in ZrO_2/Al_2O_3 gate dielectrics" Appl. Phys. Lett. **83**, 138 (2003).

28. W. K. Choi, W. K. Chim, C. L. Heng, L. W. Teo, Vincent Ho, V. Ng, D. A. Antoniadis, and E. A. Fitzgerald, "Observation of memory effect in germanium nanocrystals embedded in an amorphous silicon oxide matrix of a metal-insulator-semiconductor structure" Appl. Phys. Lett. **80**, 2014 (2002).
29. E. W. H. Kan, W. K. Choi, C. C. Leoy, W. K. Chim, D. A. Antoniadis, and E. A. Fitzgerald, "Effect of annealing profile on defect annihilation, crystallinity and size distribution of germanium nanodots in silicon oxide matrix" Appl. Phys. Lett. **83**, 2058 (2003).
30. V. Ho, M. S. Tay, C. H. Moey, L. W. Teo, W. K. Choi, W. K. Chim, C. L. Heng, and Y. Lei, "Electrical characterization of a trilayer germanium nanocrystal memory device" Microelectronic Eng. **66**, 33 (2003).
31. B. H. Koh, E. W. H. Kan, W. K. Chim, W. K. Choi, D. A. Antoniadis, and E. A. Fitzgerald, "Traps in germanium nanocrystal memory and effect on charge retention: Modeling and experimental measurements" J. Appl. Phys. **97**, 124305 (2005).
32. K. Das, M. NandaGoswami, R. Mahapatra, G. S. Kar, A. Dhar, H. N. Acharya, S. Maikap, J.-H. Lee, and S. K. Ray, "Charge storage and photoluminescence characteristics of silicon oxide embedded Ge nanocrystal trilayer structures" Appl. Phys. Lett. **84**, 1386 (2004).
33. Y. Q. Wang, J. H. Chen, W. J. Yoo, Y.-C. Yeo, S. J. Kim, D.-L. Kwong, A. Y. Du, and N. Balasubramanian, "Formation of Ge nanocrystals in HfAlO high-*k* dielectric and application in memory device" Appl. Phys. Lett. **84**, 5407 (2004).
34. J. H. Chen, Y. Q. Wang, W. J. Yoo, Y.-C. Yeo, G. Samudra, Daniel S. H. Chan, A. Y. Du and D.-L. Kwong, "Nonvolatile Flash Memory Device Using Ge Nanocrystals Embedded in HfAlO High-*k* Tunneling and Control Oxides: Device Fabrication

and Electrical Performance" IEEE Trans. Electron Devices **51**, 1840 (2004).

35. T. H. Ng, W. K. Chim, and W. K. Choi, "Conductance-voltage measurements on germanium nanocrystal memory structures and effect of gate electric field coupling" Appl. Phys. Lett. **88**, 113112 (2006).
36. A. Kanjilal, J. Lundsgaard Hansen, P. Gaiduk, A. Nylandsted Larsen, N. Cherkashin, A. Claverie, P. Normand, E. Kapelanakis, D. Skarlatos, and D. Tsoukalas, "Structural and electrical properties of silicon dioxide layers with embedded germanium nanocrystals grown by molecular beam epitaxy" Appl. Phys. Lett. **82**, 1212 (2003).
37. B. Gallas, and J. Rivory, "Investigation of a single Ge dots layer and its evolution upon oxidation by spectroscopic ellipsometry" Physica E **17**, 549 (2003).
38. P. I. Gaiduk, A. Nylandsted Larsen, J. Lundsgard Hansen, "MBE grown Ge dots on Si/SiGe ion implanted buffers" Physica E **17**, 510 (2003).
39. X. Y. Ma, Sh. H. Huang, Y. Chen, and F. Lu, "Investigation pf the quantum confinement effects in Ge dots by electrical measurements" Appl. Surf. Sci. **225**, 281 (2004).
40. M. Kanoun, M. Lemiti, G. Bremond, A. Souifi, F. Bassani, and I. Berbezier, "Electrical study of MOS structure with Ge embedded in SiO_2 as floating gate for nonvolatile memory" Superlattices and Microstructures **36**, 143 (2004).
41. T. Sass, V. Zela, A. Gustafsson, I. Pietzonka, and W. Seifert, "Oxidation and reduction behavior of Ge/Si islands" Appl. Phys. Lett. **81**, 3455 (2002).
42. A. Hattab, F. Dufaye, F. Meyer, Vy Yam, Vinh Le Thanh, D. Bouchier, R. Meyer, O. Schneegans, and C. Clerc, "Effect of Ge-dots buried below the interface on the transport properties of Schottky diodes" Physica E **17**, 648 (2003).
43. T. Baron, B. Pelissier, L. Perniola, F. Mazen, J. M. Hartmann, and G. Rolland,

"Chemical vapor deposition of Ge nanocrystals on SiO_2" Appl. Phys. Lett. **83**, 1444 (2003).

44. M. Kanoun, A. Souifi, T. Baron, and F. Mazen, "Electrical study of Ge-nanocrystal-based metal-oxide-semiconductor structures for *p*-type nonvolatile memory applications" Appl. Phys. Lett. **84**, 5079 (2004).
45. T. C. Chang, S. T. Yan, P. T. Liu, C. W. Chen, S. H. Lin, and S. M. Sze, "A novel approach of fabricating germanium nanocrystals for nonvolatile memory application" Electrochem. Solid-State Lett. **7**, G17 (2004).
46. Y. Kim, H. J. Cheong, K. H. Park, T. H. Chung, H. J. Bark, J.-Y. Yi, S. H. Bang, and J. H. Cho, "Charge retention characteristics in a metal-insulator -semiconductor capacitor containing Ge nanocrystals" Semicond. Sci. Technol. **17**, 1039 (2002).
47. J. K. Kim, H. J. Cheong, Y. Kim, J,-Y, Yi, H. J. Bark, S. H. Bang, and J. H. Cho, "Rapid-thermal-annealing effect on lateral charge loss in metal-oxide-semiconductor capacitors with Ge nanocrystals" Appl. Phys. Lett. **82**, 2527 (2003).
48. K. M. Hassan, A. K. Sharma, J. Narayan, J. F. Muth, C. W. Teng, and R. M. Kolbas, "Optical and structural studies of Ge nanocrystals embedded in AlN matrix fabricated by pulsed laser deposition" Appl. Phys. Lett. **75**, 1222 (1999).
49. S. Tiwari, F. Rana, K. Chan, H. Hanafi, Wei Chan, and Dong Buchanan "Volatile and non-volatile memories in silicon with nano-crystal storage" IEEE IEDM Tech. Dig., 521 (1995).
50. S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, Emmanuel F. Crabbe, and K. Chan, "A silicon nanocrystal based memory" Appl. Phys. Lett. **68**, 1377 (1996).
51. International Technology Roadmap for Semiconductors (2005). [On-line]

http://public.itrs.net/

52. C. Busseret, A. Souifi, T. Baron, G. Guillot, F. Martin, M. N. Semeria, J. Gautier, "Discharge mechanisms modeling in LPCVD silicon nanocrystals using *C-V* and capacitance transient techniques" Superlattices and Microstructures **28**, 493 (2000).
53. J. K. Kim, H. J. Cheong, Y. Kim, J,-Y, Yi, H. J. Bark, S. H. Bang, and J. H. Cho, "Rapid-thermal-annealing effect on lateral charge loss in metal-oxide-semiconductor capacitors with Ge nanocrystals" Appl. Phys. Lett. **82**, 2527 (2003).
54. S. Huang, S. Banerjee, Raymond T. Tung, and S. Oda, "Electron trapping, storing, and emission in nanocrystalline Si dots by capacitance-volatage and conductance-voltage measurements" J. Appl. Phys. **93**, 576 (2003).
55. S. Fleisher, P. T. Lai, and Y. C. Cheng, "Simplified close-form trap-assisted tunneling model applied to nitrided oxide dielectric capacitors" J. Appl. Phys. **72**, 5711 (1992).
56. B. G. Streetman, S. Banerjee, *Solid State Electronic Devices*, 5th Ed. pp. 470-474 (Prentice Hall, New Jersey, 2000).
57. A. Thean, and J.-P. Leburton, "Flash memory: towards single-electronics" IEEE POTENTIALS **21**, 35 (2002).
58. V. E. Borisenko and S. Ossicini, *What is What in the Nanoworld*, pp.107 (Wiley -VCH, Weinheim, 2004).
59. I. Kim, S. Han, H. Kim, J. Lee, B. Choi, S. Hwang, D. Ahn, and H. Shin, "Room temperature single electron effects in Si quantum dot memory with oxide-nitride tunneling dieelctrics" IEEE IEDM Tech. Dig., 111 (1998).
60. J. J. Welser, S. Tiwari, S. Rishton, K. Y. Lee, and Y. Lee, "Room temperature operation of a quantum-dot flash memory" IEEE Electron Device Lett. **18**. 278

(1997).

61. Y. Shi, K. Saito, H. Ishikuro, and T. Hiramoto, "Effects of traps on charge storage characteristics in metal-oxide-semiconductor memory structures based on silicon nanocrystals" J. Appl. Phys. **84**, 2358 (1998).
62. J. J. Lee, X. Wang, W. Bai, N. Lu, and D.-L. Kwong, "Theoretical and experimental investigation of Si nanocrystal memory device with HfO_2 high-*k* tunneling dielectric" IEEE Trans. Electron Devices **50**, 2067 (2003).
63. T. Hori, "Gate dielecrics and MOS ULSIs – Principles, technologies, and applications", in Electronics and Photonics, Berlin: Springer-Verlag **34**, 44 (1997).
64. J. Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices" J. Vac. Sci. Technol. B **18**, 1785 (2000).
65. D.-W. Kim, Freek E. Prins, T. Kim, S. Hwang, C. H. Lee, D.-L. Kwong, and Sanjay K. Banerjee, "Reduction of charge-transport characteristics of SiGe dot floating gate memory device with ZrO_2 tunneling oxide" IEEE Trans. Electron Devices **50**, 510 (2003).

Chapter 3 Ge Nanocrystals Grown by PLD

3.1 Introduction

Pulsed-laser deposition (PLD) has been extensively used to fabricate high quality thin films and micro- or nano-composite structures for various advanced applications [1-7]. As pulsed-laser deposition has its own advantages of high energetic laser pulse to form a jet of plasma, high quality thin film structure can be fabricated easily and efficiently. It has been shown that N_2 ambient annealed Ge nanocrystal embedded HfAlO and $LaAlO_3$ tunneling/control oxides floating gate memories are promising for the future floating gate memory devices [3-7].

The most remarkable difference between PLD and other vapor deposition methods is the high energy of the plasma generated by the laser ablation of the desired target material. When the pulsed-laser beam is focused on the Ge target, a dense layer of Ge vapor with high energy is generated on the target surface and then transferred to Ge plasma. As the plasma expands, the thermal energy will be transformed into the kinetic energy of the atoms and the plasma will "freeze". Therefore, during PLD the Ge plasma has a relatively high forward velocity, which leads to the uniform distribution of Ge nanocrystals.

In this chapter, the formation of Ge nanocrystals at relatively low substrate temperatures using PLD technique, and the memory effect of the memory structure will be discussed. Effects of size/density of the Ge nanocrystals, the tunneling and control oxide layer thicknesses and their growth oxygen partial pressures to the charge storage and charge retention characteristics are studied.

3.2 Experimental details

3.2.1 Pulsed-laser deposition conditions

Excimer laser (Lamda Physik 205) with 248 nm is utilized to act as the power source to irradiate on the target material forming a high energetic plume of atomic particles. The laser fluence and frequency used were 6 J/cm^2 and 2 Hz, respectively. Unless specified, all the thin films deposition and nanoparticles generation use the same fluence and frequency as mentioned above. Various tunnel and control layer thicknesses, Ge deposition duration, growth temperature and oxygen partial pressures have been studied.

Trial experiments have been performed to find out the optimized growth condition for Ge nanocrystals at the initial stage of the project. Two approaches have been used:

1. Ge multilayer deposition followed by subsequent annealing.

In this approach, just as many other research groups did, multiple Ge layers sandwiched with the HfAlO layers were deposited followed by high-temperature annealing. It is expected that high temperature annealing can form self-organized Ge nanocrystals by agglomeration in the HfAlO thin film matrix.

2. Deposition of a single layer Ge nanocrystal

This approach is a direct deposition of Ge nanocrystals in a shorter deposition duration, so that only a single layer of relatively small-size Ge clusters can be formed in each laser pulse.

It turned out that the first approach was not successful in forming Ge nanocrystals, and the results introduced in this chapter are from the second approach.

(A) Surface morphology study of as-grown Ge nanocrystals:

In order to study the as-grown Ge nanocrystals through surface imaging techniques, such as scanning electron microscopy (SEM) and atomic force microscopy (AFM), the Ge nanocrystals were deposited by PLD on the HfAlO/Si substrate without HfAlO capping layer. The conditions of the Ge deposition are as follow:

- Temperature = 300 – 600^{o}C.
- Vacuum = 1 x 10^{-4} Pa.
- Time of deposition = 30 seconds, 1 minute, 2 minutes, 3 minutes.
- The as-grown samples were characterized by SEM and AFM.

(B)Trilayer capacitor samples with Ge nanocrystals embedded:

The Ge nanocrystal floating gate memory structure (Fig. 3.2.1) was fabricated on p-type (100) Si substrates with sheet resistance of 4-6 Ω-cm. Hydrofluoric acid (HF) was used to remove the native oxide on the Si wafers leaving a hydrogen terminal surface. After placing the Si wafer into an ultrahigh vacuum chamber, a thin HfAlO tunneling layer was then deposited by PLD using a composite target containing HfO_2 and Al_2O_3 with the Hf:Al atomic ratio of 1:1. In fact, different ratios of Hf:Al have been tried, and it turned out that the 1:1 ratio was the best that resulted in the smallest memory window as a control sample. The thin HfAlO tunneling layer was deposited on a p-type Si substrate at substrate temperature of 550 ^{o}C. The Ge nanocrystals were then deposited on the surface of the HfAlO tunneling layer after the substrate temperature reached 600 ^{o}C under a vacuum of 1x10^{-6} Pa. Subsequently, a thicker HfAlO control layer was deposited at 550 ^{o}C with the same oxygen partial pressure. Different Ge nanocrystal deposition time (1 and 2 min) and HfAlO film growth oxygen partial pressures (5x10^{-3} and 0.2 Pa) were implemented in order to study their effects on the corresponding memory devices. A KrF

excimer laser (λ = 248 nm) with laser fluence of 6 Jcm^{-2} was used for the film deposition, and the laser frequency was set to 2 Hz.

In order to reduce the defects in the dielectric layers and study the structural stability under high temperature, the as-grown films were finally annealed at 800 ^{o}C for 45 min in N_2 ambient. Pt dot electrodes with a diameter of 0.2 mm were subsequently deposited by PLD [6].

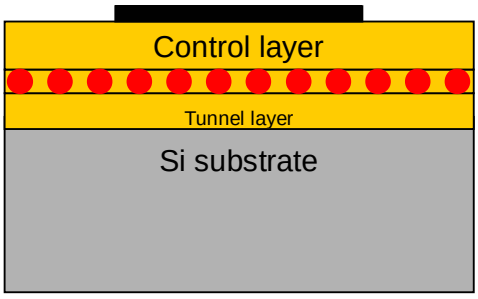


Figure 3.2.1 Schematic diagram of the trilayer nano-floating gate memory MOS capacitor.

3.3 Results

In this section, growth and characterization of the Ge nanocrystal embedded floating gate memory structures, especially the Ge nanocrystals characteristics and growth conditions, will be presented both in structural and electrical aspects. Details of the parameters governing the nano-floating gate memory effect will be discussed in more detail in Section 3.4.

3.3.1 Structural properties

(A) As- grown Ge nanocrystals

Figure 3.3.1 shows a typical SEM image of Ge nanocrystals grown at 600^{o}C. It can be seen that Ge nanocrystals are well self-organized and distributed uniformly. The density and mean size of the dots measured from the image are about $8\times10^{11}cm^{-2}$ and 25

nm, respectively. The island structure of the Ge suggests that the growth is based on the Volmer-Webber mode, where Ge atoms can easily combine with each other but not with HfAlO under the present experimental conditions. The relatively large size of these Ge nanocrystals may result in a relatively low charge storage density and also an increased surface roughness on the top dielectric that hinders the application of nanocrystal floating gate memory. Therefore, the deposition time of Ge was reduced accordingly in subsequent experiments.

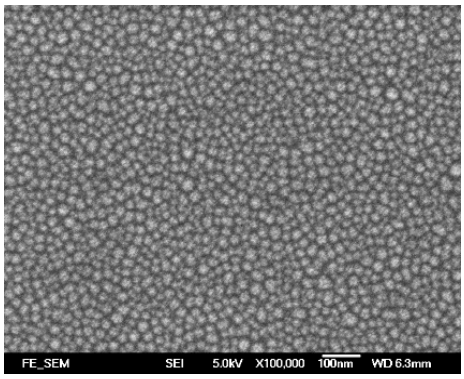


Figure 3.3.1 SEM picture of high density self-organized Ge nanocrystals deposited on HfAlO/Si substrate matrix by PLD for 1min at 600 ^{o}C.

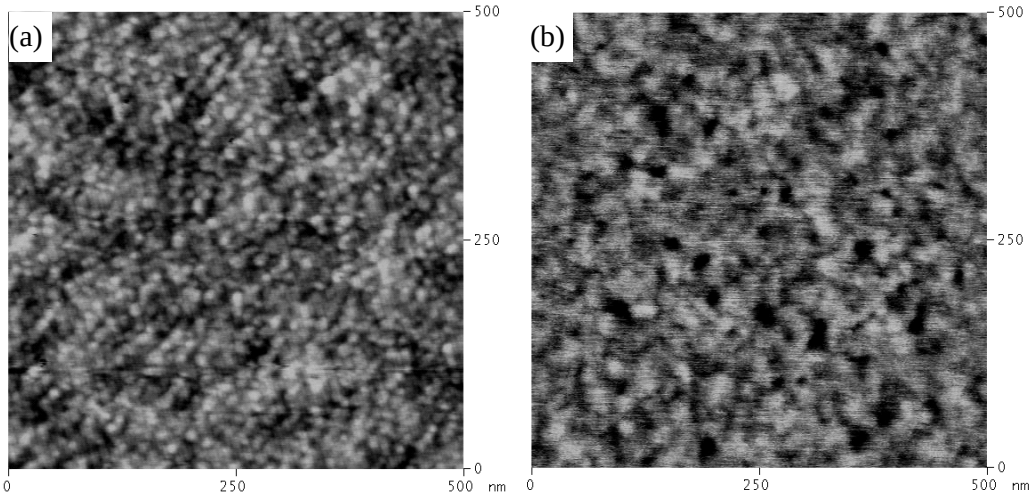


Figure 3.3.2 AFM images of Ge nanocrystals on HfAlO/Si matrix by PLD for 30 s at (a) 600 ^{o}C and (b) 700 ^{o}C.

The substrate temperature was found to be an important parameter for the growth of Ge nanocrystals. Figures 3.3.2 (a) and (b) show atomic force microscopy images of the Ge nanocrystals grown at the temperatures of 600°C and 700°C, respectively. It can be seen that the Ge nanocrystals are well self-organized and their diameter is about 10 nm. By contrast, the diameter of the Ge nanocrystals deposited at 700°C is larger and their height becomes smaller. This suggests that when the substrate temperature increases, the diffusion coefficient of Ge atoms also increases, and the Ge atoms are relatively easier to combine with the HfAlO atoms. Therefore, the substrate temperature of 600°C for the growth of Ge nanocrystals has been used to fabricate memory capacitors.

(B) Trilayer memory capacitor

Trial experiments have been done for optimizing the growth condition of the Ge nanocrystals embedded in the HfAlO thin film matrix. Figure 3.3.3 shows a cross-sectional HRTEM image of the first sample presenting Ge nanocrystals which are isolated from each other and in a hemispherical shape. However, due to the relatively long deposition time, the Ge nanocrystals are too large in size. The average diameter of the Ge nanocrystals is about 20-30 nm.

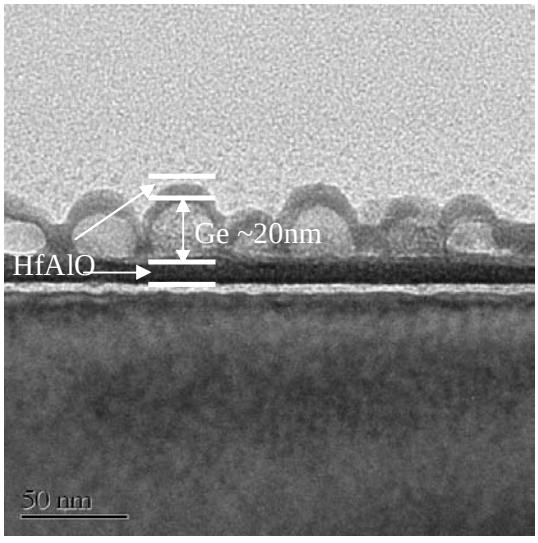


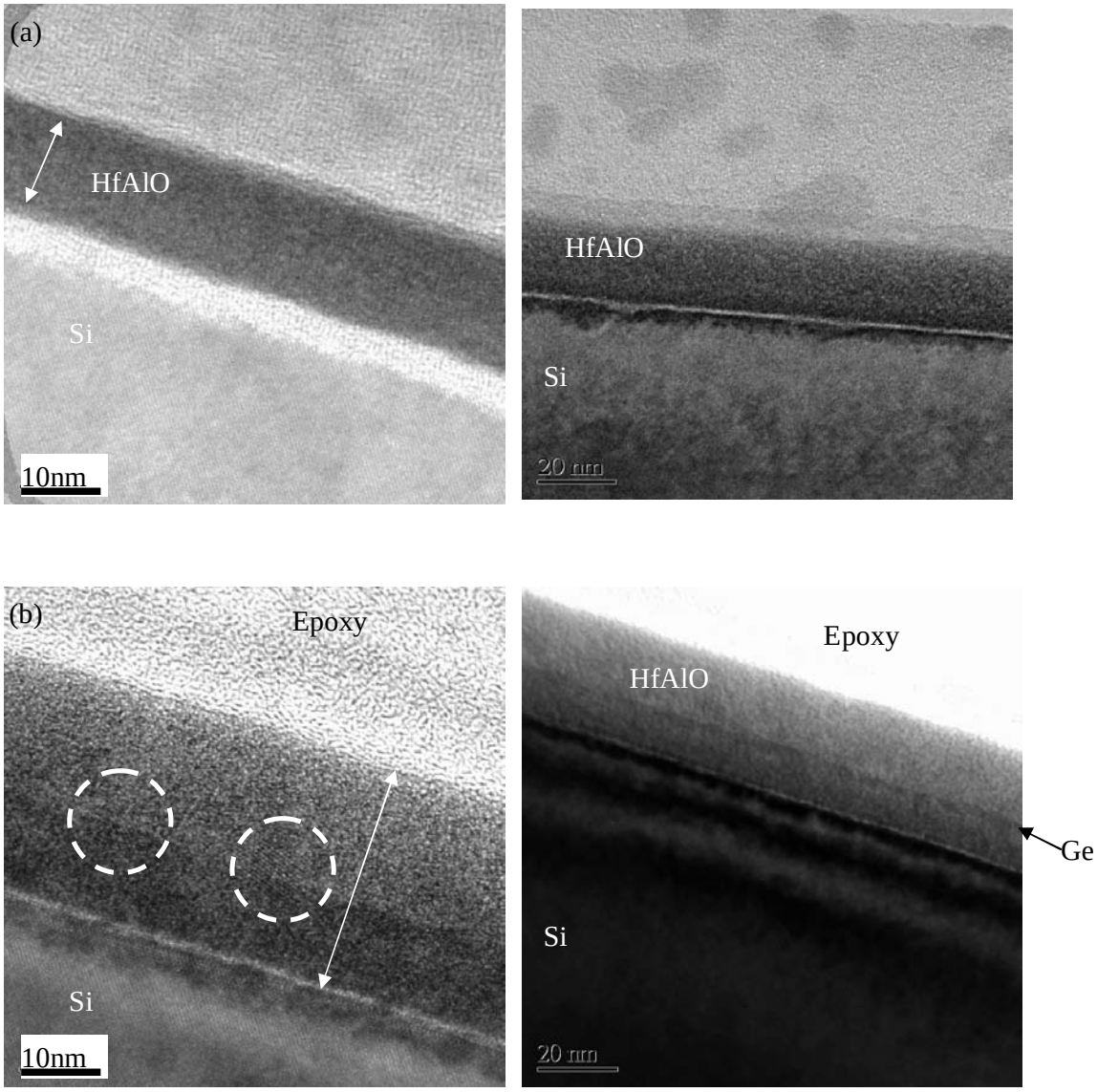
Figure 3.3.3 Cross-section TEM image of the as-grown sample.

After a series of experiment, a general trend in condition to grow good Ge nanocrystals has been figured out. Following is the TEM images (Fig. 3.3.4) of a series of Ge nanocrystals grown by using different growth conditions as shown in Table 3.1. It is apparent that as the deposition time increases from 30 s to 3-min, the Ge nanocrystals size increases from invisible to about 20 nm.

Table 3.1 Trilayer structure floating gate capacitors with various growth conditions.

No.	Tunnel layer/nm	Control layer/nm	O_2 pressure/Pa	Temperature/℃	Ge deposition Time
A1	2.5	7.5	x 10^{-3}	600	1-min@1Hz
A2	2.5	7.5	x 10^{-1}	600	1-min@1Hz
A3	2.5	7.5	x 10^{1}	600	1-min@1Hz
A4	5.0	15.0	x 10^{-3}	600	1-min@1Hz
A5	5.0	15.0	x 10^{-1}	600	1-min@1Hz
A6	5.0	15.0	x 10^{1}	600	1-min@1Hz
A7	5.0	15.0	x 10^{-3}	600	2-min@1Hz
A8	5.0	15.0	x 10^{-1}	600	2-min@1Hz
A9	5.0	15.0	x 10^{1}	600	2-min@1Hz

Higher magnification Lower magnification



Higher magnification Lower magnification

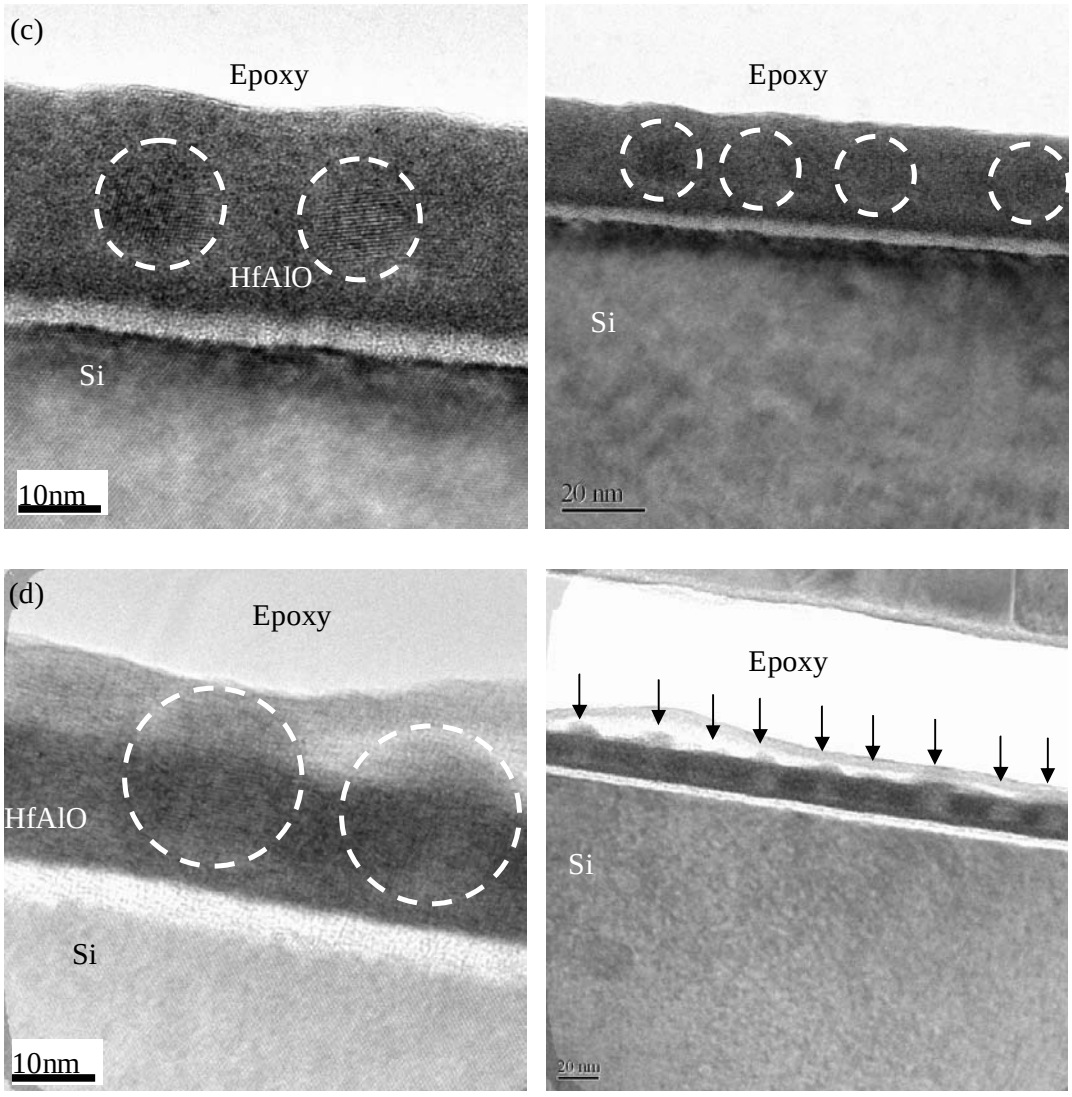
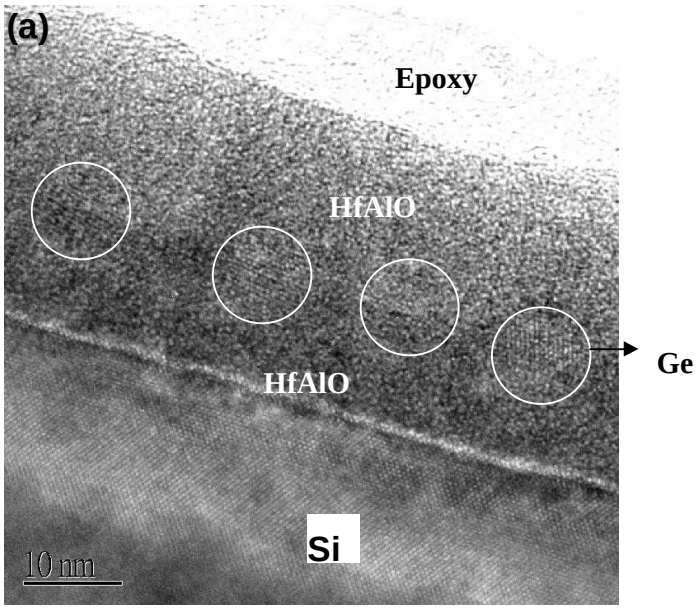


Figure 3.3.4 TEM images of the trilayer floating gate capacitors with different Ge deposition time: (a)30 s, (b)1-min, (c) 2-min , (d) 3-min. The dot-circle region and/or the arrow indicate that Ge nanocrystals are formed within the HfAlO matrix.

Experiments have been carried out for the detailed study of the growth mechanism of the Ge nanocrystals. The following paragraph describes a typical sample with a trilayer structure with the embedment of Ge nanocrystals within the HfAlO matrix. Both structural and electrical characteristics will be presented in the following paragraphs based on sample A9.

A 7 nm-thick tunneling HfAlO layer was first grown on a p-type (100) Si substrate at 550^{o}C. Subsequently, the Ge nanocrystals were deposited on the surface of the HfAlO at 600^{o}C. Different deposition time and substrate temperatures were implemented in order to study their effects on the formation of Ge nanocrystals. The memory structure used in this study is metal-oxide-semiconductor (MOS) capacitor with a dielectric stack made up of Ge nanocrystals sandwiched between the tunneling and control HfAlO layers. The control HfAlO layer, with a thickness of 10 nm, was deposited at 550 ^{o}C. The samples were finally annealed at 800^{o}C for 30 min in N_2 ambient, and Pt dot electrodes with a diameter of 0.2 mm were subsequently deposited by PLD.



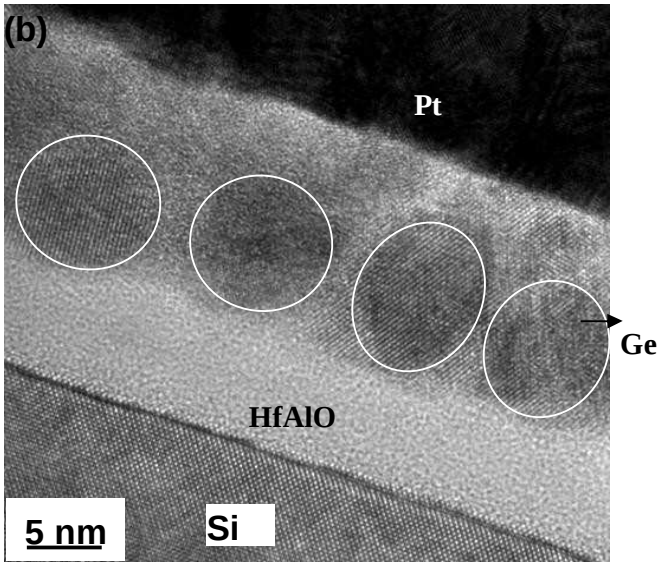


Figure 3.3.5 High-resolution TEM images of samples composed of HfAlO control gate, Ge nanocrystals, and HfAlO tunnel layer on Si substrate: (a) as-grown, and (b) annealed at 800 ^{o}C.

The structure of the memory capacitor was investigated by cross-sectional TEM. Figure 3.3.5 (a) shows the structure of the as-grown sample containing three obvious layers on silicon substrate, i.e., the HfAlO control layer, the Ge nanocrystals layer and the HfAlO tunnel layer. The interface between the HfAlO tunnel layer and the silicon substrate is almost free from any interfacial layer. The Ge nanocrystals indicated by white circles are uniformly distributed between the HfAlO control layer and the tunnel layer. The thicknesses of the tunneling layer and the control layer are about 7 nm and 10 nm, respectively.

It is apparent that the HfAlO layers have an amorphous structure and the Ge nanocrystals are single crystalline. The lattice fringes of the nanocrystals are identified as {111} planes of Ge (approximately 3.27 Å). Our experimental results showed that the growth rate can also affect the crystallinity of the Ge nanodots. It can also be seen from Fig. 3.3.5 (a) that the Ge nanocrystals are spherical in shape and their diameter is about 10 nm, which is consistent with the AFM result shown in Fig. 3.3.2 (a).

Figure 3.3.5 (b) is the high-resolution TEM image of the MOS structure annealed at 800°C. It can be clearly seen that even after annealing at 800°C, the interface between the HfAlO tunnel layer and the silicon substrate is still sharp and is probably free from SiO_2 interfacial layer. It can also be seen that after annealing at 800°C, the size of the Ge nanocrystals increases. Some crystal lattices in the control layer may be due to the diffusion of Ge. It is also worth noting that the existence of Ge and Ge diffusion may decrease the crystallization temperature of HfAlO and lead to localized crystallization. It is difficult to distinguish the crystal lattice spacing between HfO_2 and Ge.

3.3.2 Electrical properties

Pt electrode gate MOS capacitors were fabricated and characterized for all samples with the above conditions. The memory window was obtained from the flat-band voltage shift, ΔV_{FB}, of high-frequency *C-V* measurement after forward and reverse gate bias voltage sweeps. The *C-V* measurement of the as-grown and 800°C annealed MOS capacitors incorporating the Ge nanocrystals revealed that the as-grown sample exhibits abnormal *C-V* characteristics due to high leakage current (not shown), and the sample annealed at 800°C presents a significant hysteresis loop, indicating successful charge storage. Figure 3.3.6 (a) shows the high-frequency (1MHz) *C-V* curve of the sample annealed at 800°C. Clockwise hysteresis indicates electron or charge trapping in the capacitor [13-14]. The effect of the mobile ions on charge trapping can be ruled out, since no hysteresis was observed in the control sample without Ge nanocrystals under our experimental conditions and no obvious deformation can be observed in the *C-V* curves as shown in Fig. 3.3.6 (a). The flat-band voltage shift is about 0.6 V. Calculated by the formula in reference 17-19, the stored charge density is up to $1x10^{12}$ cm^{-2}.

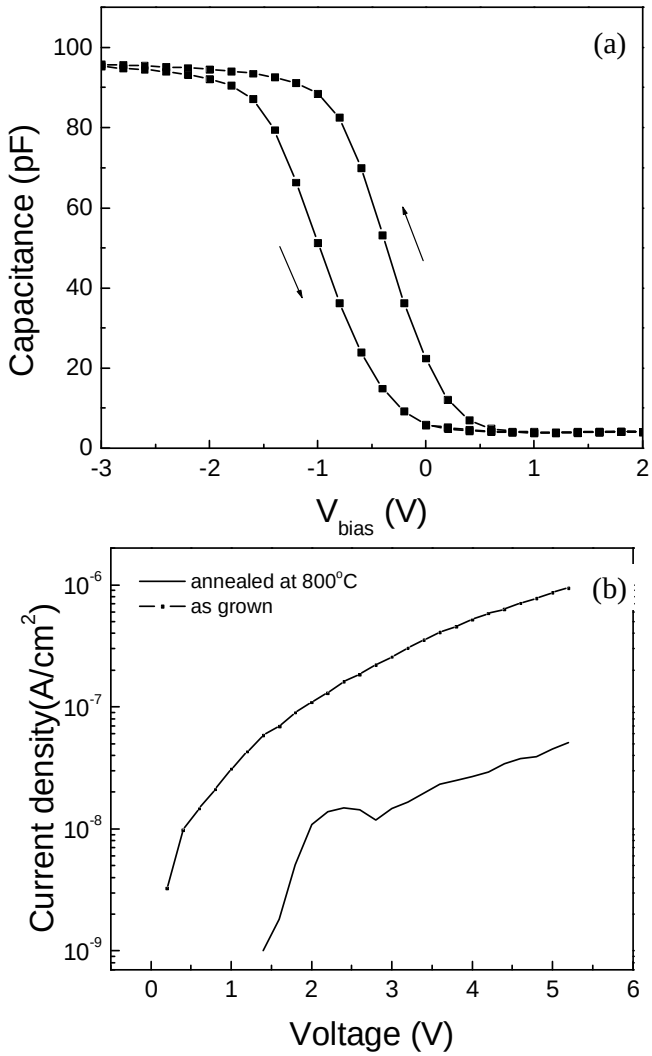


Figure 3.3.6 (a) High frequency (1MHz) *C-V* curves, and (b) *I-V* curves of as-grown and 800 °C annealed MOS capacitors.

The different *C-V* characteristics between the as-grown and the annealed samples can be understood by measuring their leakage currents. Figure 3.3.6 (b) shows the leakage currents of the two samples with and without annealing. It can be seen that the leakage current of the memory structure annealed at 800°C is very small and it is much smaller than that of the sample without annealing. The relatively large leakage current of the sample without annealing is due to the presence of a large amount of oxygen vacancies in the as-grown HfAlO films. Annealing at 800°C in a quartz tube reduced the oxygen vacancies and the leakage current.

3.4 Parameters governing the memory effect

(A) Ge nanocrystal size and the memory effect

Structural properties of the Ge nanocrystal floating gate memory capacitors were characterized by cross-sectional HRTEM. In Figs. 3.4.1 (a) and (b), a trilayer Ge nanocrystal memory capacitor structure, containing the HfAlO tunneling layer, the Ge nanocrystals and the HfAlO control layer, can be clearly seen. The crystalline Ge nanocrystals are formed in the amorphous HfAlO dielectric matrix for both 1-min and 2-min Ge deposition samples, and the HfAlO matrix contains 2.5 nm tunneling layer and 15 nm control layer. Since both capacitor structures have been post-annealed at 800 ^{o}C for 45 min in N_2 ambient, a slightly oxidized interfacial layer can be observed.

It is apparent that the Ge nanocrystals as shown in Fig.3.4.1 (b) with 2-min Ge deposition possess a relatively larger size, and the estimated average size of a spherical Ge nanocrystal is about 5 and 8 nm, for the 1-min and 2-min Ge deposition time, respectively. The number densities of the Ge nanocrystals corresponding to Figs. 3.4.1 (a) and (b) are estimated to be about $1x10^{12}$ cm^{-2} and $7x10^{11}cm^{-2}$, respectively.

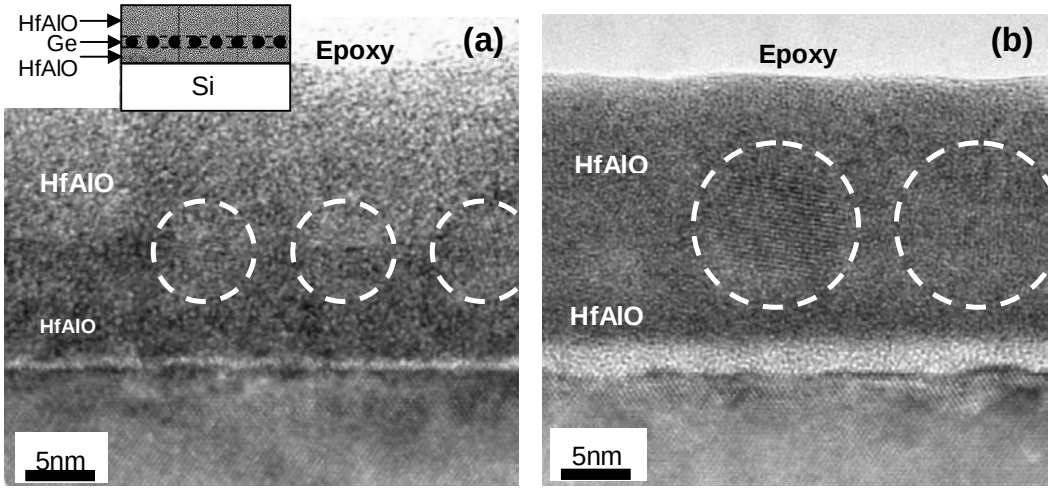


Figure 3.4.1 HRTEM images of the trilayer floating gate capacitors: (a) 1-min, and (b) 2-min Ge deposition . The region circled with dotted-line represents the Ge nanocrystals. The inset is a schematic diagram representing the trilayer structure.

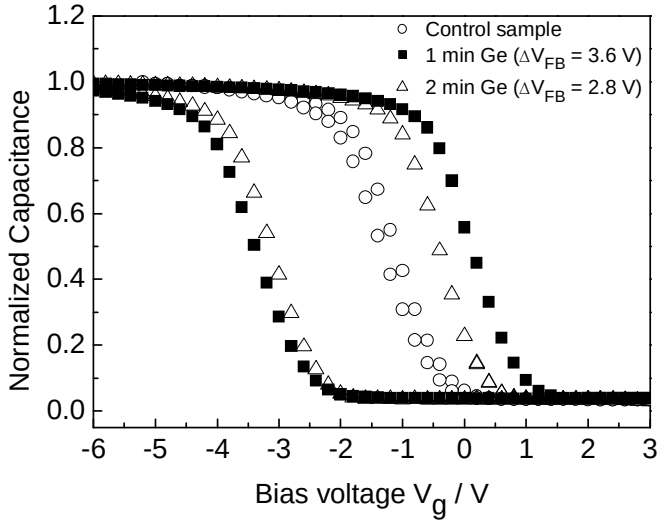


Figure 3.4.2 High frequency (1 MHz) *C-V* measurements of the trilayer floating gate capacitors with 1 and 2 min Ge deposition time and control sample without Ge nanocrystals. All samples have been annealed at 800 ^{o}C in N_2 ambient for 45 minutes. Large counter-clockwise hysteresis loop up to ΔV_{FB} = 3.6 V can be observed in the sample with Ge nanocrystals. All samples are normalized with accumulation capacitance of 0.15 nF.

High-frequency (1 MHz) *C-V* measurement of the MOS capacitors incorporating the Ge nanocrystals revealed significant hysteresis, indicating successful charge storage in the Ge nanocrystals. Figure 3.4.2 shows the high-frequency (1 MHz) *C-V* curves of three samples with and without Ge nanocrystals, where the control sample without Ge nanocrystals shows a typical *C-V* curve without obvious hysteresis loop; and by contrast, counter-clockwise hysteresis loops are present in the samples with Ge nanocrystals indicating charge trapping in the capacitors. It is worth noting that the effect of mobile ions on the charge trapping can be ruled out, since no significant hysteresis was observed in the control sample without Ge nanocrystals under the same experimental conditions. As shown in Fig. 3.4.2, the maximum flat-band voltage shift (ΔV_{FB}) for the 1-min deposited Ge nanocrystal sample is about 3.6 V, and the calculated storage charge density corresponding to the hysteresis loop is up to $1x10^{13}$ cm^{-2} based on the formula given by Tiwari [8] and Kim *et al.* [9].

The ΔV_{FB} corresponding to the longer Ge deposition time of 2 min is slightly smaller than that of the sample with 1-min Ge deposition (2.8 V and 3.6 V, respectively). We believe that this decrease in ΔV_{FB} for the sample with longer time of Ge deposition is because of the decrease in the nanocrystal density within the HfAlO matrix. In reference [10], a simulation model suggests that the threshold voltage shift ΔV_{th} decreases as the thickness of Ge nanocrystal layer increases. This equivalently explains our *C-V* characteristic curves as shown in Fig. 3.4.2, where a reduction of 0.8 V in ΔV_{FB} can be found when the Ge dot size varies from lower deposition time to higher deposition time. The 3-min sample shows abnormal *C-V* curve due to large leakage current. Too large Ge nanocrystals result in rough surface and large leakage and are not suitable for memory application.

The density of the Ge nanocrystals is a function of deposition time. The growth of Ge under our deposition condition follows the Volmer-Weber growth mechanism, i.e., island growth on the amorphous HfAlO film. The density of the nanocrystals increases at the earlier stage as the deposition time increases and reaches its maximum. When the time increases further, the islands tend to coalesce into larger islands and the density of the nanocrystals decreases. This trend has been illustrated by a series of experiments with different Ge deposition time from 1 to 2 and 3 min.

(B) Tunneling and control layers thickness effect

Figures 3.4.3 shows the high-frequency *C-V* curves of two different sets of Ge nanocrystal floating gate capacitors with different tunneling and control oxide layers thicknesses, while the Ge nanocrystal deposition time is 1 min. As shown in Fig. 3.4.3, the *C-V* characteristic curve of the capacitor with thinner tunneling and control layers

exhibits relatively smaller hysteresis compared to that of the thicker one. This thickness effect of the tunneling and control layers can be interpreted by the thickness dependence of the leakage current and thus the charge storage effect. The thicker tunneling and control layers result in a lower leakage current and thus a better charge storage effect. The inset in Fig. 3.4.3 illustrates the decrease of the leakage current as the thicknesses of the tunneling and control layers increase. In addition, 800 ^{o}C thermal annealing may result in Ge diffusion, and a thinner HfAlO tunneling layer increases the leakage of stored charges and thus degrades the memory effect. However, a thicker tunneling layer will reduce the writing and erasing speed. Therefore, the trade-off between programming efficiency and long retention time is still an important issue to be tackled.

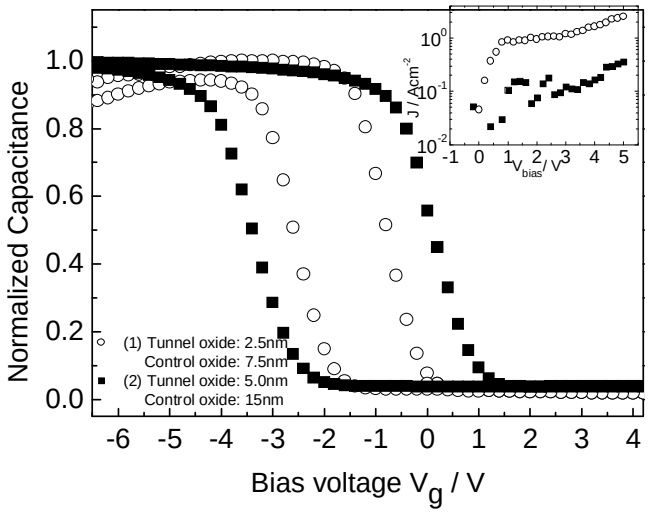


Figure 3.4.3 High frequency (1 MHz) *C-V* characteristics of the trilayer floating gate capacitors with the same growth condition of oxygen partial pressure of 0.2 Pa and substrate temperature of 550 ^{o}C, followed by a 800 ^{o}C annealing in N_2 ambient: (1) with total physical thickness of 10 nm (control layer ~ 7.5 nm, tunnel layer ~ 2.5 nm , and (2)with total physical thickness of 20 nm (control layer ~ 15 nm, tunnel layer ~ 5 nm). Inset is the *I-V* characteristic of the samples. The sample with thinner layers growth shows a higher leakage current density. All samples are normalized with accumulation capacitance of 0.15 nF.

(C) Film growth oxygen pressure dependence of the memory effect

The oxygen partial pressure during HfAlO film growth also plays an important role in threshold voltage shift. Figure 3.4.4 shows the *C-V* loops of two different samples deposited under different oxygen partial pressures of $5x10^{-3}$ and 0.2 Pa. All samples have been annealed in N_2 ambient for 45 mins. Two obvious trends can be noticed from Fig. 3.4.4. First, higher oxygen pressure during the HfAlO film growth results in larger hysteresis loop in the *C-V* curve and a lower oxygen pressure gives smaller hysteresis loop. This can be explained by two factors. One is that, at higher oxygen pressure, the HfAlO film possesses lower oxygen deficiency induced leakage current and thus a better charge storage retention property and larger flat-band voltage shift. The inset illustrates that the leakage current decreases as the oxygen pressure increases.

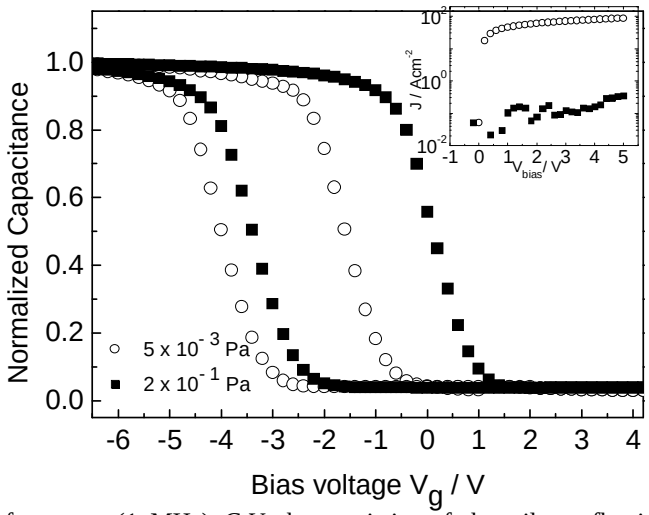


Figure 3.4.4 High frequency (1 MHz) *C-V* characteristics of the trilayer floating gate capacitors with HfAlO growth oxygen partial pressures of $5x10^{-3}$ and 0.2 Pa. All samples have been annealed in N_2 ambient for 45 min. Inset is the *I-V* characteristic of the samples. The sample with growth oxygen partial pressures of $5x10^{-3}$ Pa shows a higher leakage current density. All samples are normalized with accumulation capacitance of 0.15 nF.

The other reason to explain the oxygen pressure dependence of the memory effect is that, a higher oxygen pressure results in more GeO_x formation during the subsequent high temperature growth of the HfAlO control layer. It has been revealed that, GeO_x is highly volatile and can easily diffuse into the dielectric layer and form charge traps in the vicinity of the Ge nanocrystals and contribute to more charge storage and thus the flat-band voltage shift. According to Cho *et al.* [11], hysteresis loop of *C-V* curve is the result of a high interfacial charge trap density due to GeO_x formation. Another feature that can be noticed in Fig. 3.4.4 is the negative flat-band voltage (V_{FB}) shift for the lower oxygen partial pressure sample. This is due to the formation of positive fixed charges of oxygen vacancies resulted from the low oxygen pressure growth of the HfAlO layers.

(D) Charge retention characteristics

To evaluate the characteristics of stored charges in the Ge-nanocrystal floating gate memory capacitors, the stored charge lifetime must be known. *C-t* measurement results at room temperature shown in Fig. 3.4.5 reveal that the capacitance decreases as a function of time. After injecting electrons at 10 V for 20 s, gate voltage is changed to the flat-band voltage of -1 V and the charge retention time is expected to be long enough to withstand the loss of charge stored in the memory nodes. It can be seen that after 10^4 seconds of stress applied, the decay of capacitance for the floating gate memory capacitor with 1-min Ge deposition is about 8%, while for the 2-min Ge deposition sample it is 5%. It is also clearly shown that no significant initial charge decay can be observed.

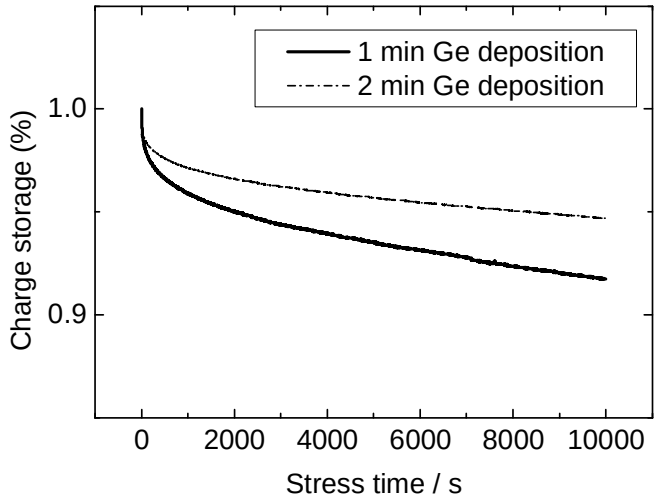


Figure 3.4.5 *C-t* characteristics of the trilayer floating gate capacitor after 800 ^{o}C annealing in N_2 ambient. The charging voltage is 10 V for 20 s and the measurement voltage of -1 V.

According to the work of Kim *et al*, the stored charges in the localized nanocrystals exhibit long-term retention property, since charge loss can only be through leaking from isolated nanocrystals to channel layer via the tunneling barrier [9]. As shown in Fig. 3.4.1, self-organized and isolated Ge nanocrystals have been formed and confined in the HfAlO matrix in our experimental condition, so good memory storage effect can be achieved. Shi *et al.* developed a model of deep trapping centers including three-dimensional quantum confinement and Coulomb blockade effect [12]. It states that a long retention time can be achieved by introducing a certain number of deep trapping centers in the nanocrystals and reducing the interface states between dielectric/Si interface. Based on this model, we believe that a relatively smaller density of interface states in the HfAlO/Si interface and high density of deep trapping centers in nanocrystals have been achieved.

It is worth noting that the charges in nanocrystals possessing larger size (longer deposition time) decay slower than that in the smaller ones, i.e., the retention characteristic of the 2-min sample is better than that of the 1-min sample (Fig. 3.4.5). Since the 1-min deposited Ge nanocrystals have a dimension of about 5 nm, the Coulomb blockade effect and the quantum confinement effects are significant for the "write/erase" process. The Coulomb blockade effect raises the electrostatic potential of the Ge nanocrystals, and the quantum confinement effect shifts the Ge nanocrystal conduction band energy upward and reduces the conduction band offset between the nanocrystals and HfAlO (the reported conduction band shift for 5-nm Ge nanocrystal is 0.15 eV) [13]. These two effects make the stored charges more easily to tunnel back to the Si channel area and degrade the retention property.

3.5 Summary

In conclusion, we have fabricated, at relatively low temperature by PLD method, a memory structure containing a HfAlO control gate, well self-organized Ge nanocrystals and a HfAlO tunnel layer. The substrate temperature and growth rate were found to be the key factors influencing the size and distribution of the Ge nanocrystals. The obvious memory effect of the trilayer structure was demonstrated by the presence of hysteresis in the *C-V* curves with a stored charge density of up to 10^{12} cm^{-2}. Memory effects of the capacitors have been characterized by using *C-V* and *C-t* measurements. Counter-clockwise hysteresis *C-V* loops have been obtained and a threshold voltage shift of up to 3.6 V has been achieved indicating stored electrons in the Ge nanocrystal floating gate and thus the memory effect. The effect of tunneling/control oxide layers thickness and the size/density of the Ge nanocrystals to the charge storage and thus the memory characteristics have been studied.

References

1. P. F. Lee, J.Y. Dai, K.H. Wong, H.L.W. Chan and C.L. Choy, "Study of interfacial reaction and its impact on electric properties of Hf-Al-O high-*k* gate dielectric thin films grown on Si"Appl. Phys Lett. **82**, 2419 (2003).
2. Shiye Wang, Weili Liu, Qing Wan, J. Y. Dai, P. F. Lee, Luo Suhua, Qinwo Shen, Miao Zhang, Zhitang Song, and Chenglu Lin, "Investigation of Ge nanocrystals in a metal-insulator-semiconductor structure with a HfO_2/SiO_2 stack as the tunnel dielectric" Appl. Phys. Lett. **86**, 113105 (2005).
3. W. L. Liu, P. F. Lee, J. Y. Dai, J. Wang, H. L. W. Chan , C. L. Choy, Z. T. Song and S. L. Feng, "Self-organized Ge nanocrystals embedded in HfAlO fabricated by pulsed-laser deposition applied to floating gate memory" Appl. Phys. Lett. **86**, 013110 (2005).
4. P. F. Lee, W. L. Liu, Z. T. Song, and J. Y. Dai "Ge nanocrystals embedded in Hf-aluminate high-*k* gate dielectric for floating gate memory application" Proc. SPIE **5650**, 141 (2005).
5. X. B. Lu, P. F. Lee, and J. Y. Dai, "Synthesis and memory effect study of Ge nanocrystals embedded in $LaAlO_3$ high-*k* dielectrics" Appl. Phys. Lett. **86**, 203111 (2005).
6. P. F. Lee, X. B. Lu, J. Y. Dai, H. L. W. Chan, Emil Jelenkovic, and K. Y. Tong, "Memory effect and retention property of Ge nanocrystal embedded Hf-aluminate high-*k* gate dielectric" Nanotech. **17**, 1202 (2006).
7. P. F. Lee, J. Y. Dai, and H. L. W. Chan, "Formation of Ge nanocrystals by utilizing nanocluster source" Material Science in Semiconductor Processing **9**, 817 (2006).
8. S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, Emmanuel F. Crabbe, and K. Chan, "A

silicon nanocrystal based memory" Appl. Phys. Lett. **68**, 1377 (1996).

9. J. K. Kim, H. J. Cheong, Y. Kim, J,-Y, Yi, H. J. Bark, S. H. Bang, and J. H. Cho, "Rapid-thermal-annealing effect on lateral charge loss in metal-oxide-semiconductor capacitors with Ge nanocrystals" Appl. Phys. Lett. **82**, 2527 (2003).
10. Y. Zhu, D. T. Zhao, R. G. Li and J. L. Liu, "Threshold voltage shift of heteronanocrystal floating gate flash memory" J. Appl. Phys. **97**, 034309 (2005).
11. M.-H. Cho, H. S. Chang, D. W. Moon, S. K. Kang, B. K. Min, D.-H. Ko, H. S. Kim, Paul C. Mclntyre, J. H. Lee, J. H. Ku and N. I. Lee, "Interfacial characteristics of HfO_2 films grown on strained $Si_{0.7}Ge_{0.3}$ by atomic-layer deposition" Appl. Phys. Lett. **84**, 1171 (2004).
12. M. She, and T. -J King, "Impact of crystal size and tunnel dielectric on semiconductor nanocrystal memory performance" IEEE Tans. Electron Devices **50**, 1934 (2003).
13. Y. Shi, K. Saito, H. Ishikuro, and T. Hiramoto, "Effects of traps on charge storage characteristics in metal-oxide-semiconductor memory structures based on silicon nanocrystals" J. Appl. Phys. **84**, 2358 (1998).

Chapter 4 Ge Nanoclusters Grown by the Nanocluster Beam Source

4.1 Introduction

In this project, besides the pulsed-laser deposition method, a novel approach to synthesize the nano-floating gate memory by means of Ge nanocluster beam source was carried out. The Ge nanoclusters are generated by magnetron sputtering of Ge target and aggregated under inert gas. Nanocluster beam source (Model NC200U Oxford Applied Research) is a novel method for fabricating various types of nanoclusters of metal and semiconductor materials. It can be combined with various vacuum systems to form nanoclusters of different sizes. Ar gas is usually used as both the sputtering gas for plasma generation and aggregation process. Helium gas can be mixed with Ar to reduce the size of nanoclusters. The advantages of utilizing nanocluster beam source in synthesis of nano-floating gate memory are:

1. Nanoclusters with finite size can be formed easily in a one-step process without subsequent annealing;
2. It can generate isolated nanoclusters with relatively uniform size distribution;
3. It enables in-situ growth of nanoclusters embedded in other kind of films, i.e., forming nanocomposite films.

In this section, the fabrication and characterization of Ge nanoclusters embedded in HfAlO high-*k* dielectric by utilizing the NC200U nanocluster source integrated into a PLD system are introduced. Structural properties of the HfAlO/Ge-NC/HfAlO trilayer memory capacitors are investigated by means of TEM, AFM and secondary ion mass

spectroscopy (SIMS). Memory effect of the nanoclusters are studied based on electrical characterization such as *C-V*, *I-V* and *C-t* measurements. Effects of size/density of the Ge nanoclusters, and their growth temperature on the charge storage and charge retention characteristics are tackled.

4.2 Experimental details

4.2.1 Nanoclusters deposition by the nanocluster beam source

The NC200U is a nanocluster source designed for working in an ultra high vacuum. A DC magnetron sputtering is used to generate the clusters. Inside the cooled aggregation tube, an inert gas, typically argon or its mixture with helium, cools and sweeps the atoms and clusters from the aggregation region towards an aperture. The cluster's size can be varied by adjusting several parameters such as the power supplied to the magnetron, the aperture size, the rate of inert gas flow, type of inert gas(es) being used, temperature of the aggregation region and distance between the magnetron and the aperture. The efficient use of electrons to promote ionization of the gas in the sputtering chamber is possible with the assistance of a magnetic field. Application of an axial magnetic field in a planar glow discharge system increases the path length of the electron of sputtering and leads to the formation of a circular "race-track" path. [1]

Various growth parameters governing the nanoclusters properties are:

(1) pressure,

(2) aggregation distance,

(3) substrate temperature, and

(4) growth duration.

Fine and uniform nanoclusters can be formed by optimizing the above growth parameters. Our goal is trying to find out how the above parameters affect the nanocluster properties and hence the memory properties of the nano-floating gate capacitors.

Our project included the following areas of study:

- Ge nanocluster formation by using the nanocluster beam source;
- Deposition of Ge nanoclusters on carbon film and HfAlO/Si sample;
- Characterization of trilayer capacitor sample by TEM, AFM, SIMS, *C-V*, *I-V* and *C-t* measurements.

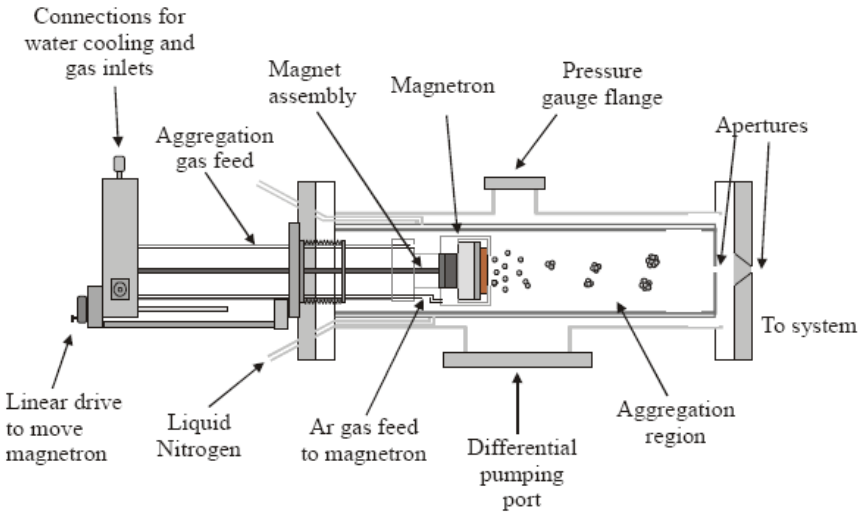


Figure 4.2.1 Schematic diagram of the nanocluster source (NC200U) system.

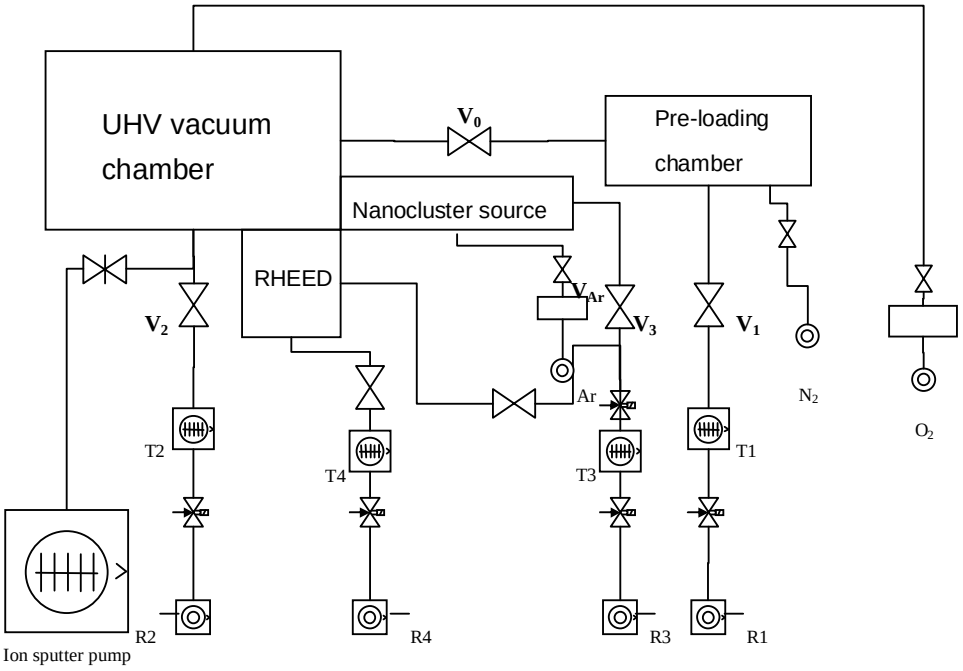


Figure 4.2.2 Vacuum system and gas circuit chart.

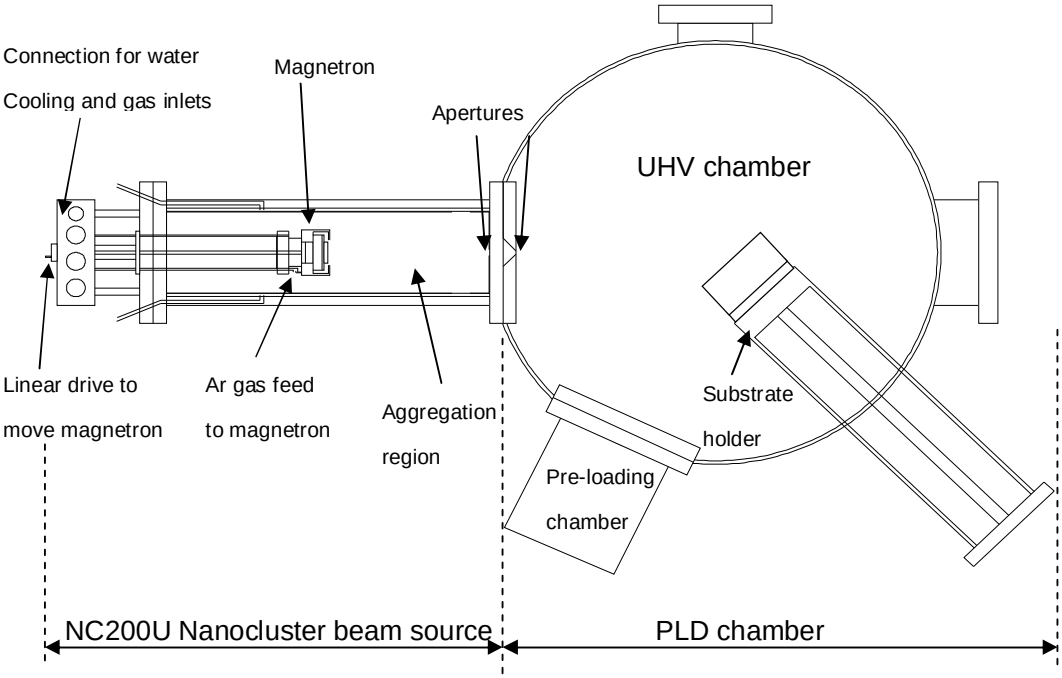


Figure 4.2.3 Schematic layout of the nanocluster beam source with laser molecular beam epitaxy vacuum chamber system.

Figure 4.2.1 is a schematic diagram of the commercialized NC200 nanocluster source (developed by Oxford Applied Research). We have attached this nanocluster source to a UHV chamber which is used for pulsed-laser deposition (Figs. 4.2.2 & 4.2.3). After deposition of the tunneling oxide by the pulsed-laser deposition, a layer of Ge nanoclusters can be in-situ deposited by the NC200 nanocluster source, and subsequently, a capping layer of dielectric can be deposited again by PLD.

The UHV chamber in fact can be used for the tunneling and control dielectric layers deposition such as physical vapor deposition or chemical vapor deposition. The middle floating gate layer containing nanoclusters of Ge can be deposited in between the two dielectric layers. The floating gate layer can be either a single or multi layers of Ge nanoclusters or even a mixture of Ge nanoclusters with the dielectric material by co-deposition of the Ge nanoclusters with the dielectric. The commercialized nanocluster source utilizing magnetron sputtering is also illustrated in Fig. 4.2.1, where a Ge target is used as an atom source, and the sputtered atoms are quenched by colliding with sputtering gas Ar and form nanoclusters. The nanoclusters are attracted out from the aperture due to the pressure gradient and form a nanoclusters beam. The size of the beam can be in the range of 5 cm in diameter. By rotating the wafer, size-uniform and size-controllable nanoclusters of Ge can be deposited in between the two dielectric layers. Several nanoclusters, including Si, Ge and SiGe or even metals can be synthesized and studied by this method.

The experiment of investigating the Ge nanocluster fabricated by using nanocluster source can be divided into two stages:

1. Uncapped Ge nanoclusters – a study of their size dependence on deposition conditions

For a simple and quick investigation of the Ge nanocluster size and distribution, TEM Cu-grid with carbon thin film was first used as the substrate for Ge nanocluster growth under different growth conditions using the NC200U nanocluster source. The samples were then subjected to plane-view TEM examination.

When the growth chamber reached a vacuum of ~1 x 10^{-5} Pa, sputtering gas was filled in the aggregation chamber under a differential pumping for reducing gas pressure in the deposition chamber. Three different parameters in the nanocluster growth have been studied in our experiment: power of the DC sputtering, sputtering gas flow rate and target-to-aperture distance (defined as aggregation length).

By applying sputtering voltage with suitable flow rate of sputtering gas (Ar), light violet color plasma can be observed through the small aperture. Sputtering power ranges from 30 to 100 W has been used. Other parameters such as Ar gas flow rate and aggregation distance have been chosen as 30 – 40 sccm and 60 – 100 mm, respectively.

2. Trilayer nano-floating gate memory structure with Ge nanoclusters embedded in thin film dielectric matrix

Pulsed-laser deposition was employed to fabricate the tunneling and control gate oxide layers. PLD is a good method to fabricate compounds because of its flexibility and ability to control the stoichiometry of compounds. The effect of growth conditions on the properties of high-*k* materials, including laser condition

(including energy density and frequency), substrate temperature, the distance between target and substrate, annealing condition, have been studied systematically in Chapter 3.

Ge nanoclusters were embedded in HfAlO matrix to fabricate trilayer MOS structures composed of a tunnel layer, a nanocluster layer and a control layer (Table 4.2.1). Thermal annealing in N_2 ambient is used to improve the dielectric films quality in reducing the leakage current. A trilayer structure as illustrated in previous Chapter (Fig. 3.2.2) was fabricated. Optimized MOS structure parameters including the thickness of tunneling and control gate layers, the size of and the density of Ge nanoclusters have been obtained.

Table 4.2.1 Growth parameters of the trilayer sample

Sample	Power /W	Distance /mm	Ar gas flow/sccm	Duration /min	Temperature /℃
050118NCGe (iii)	60	60	55	15	500
050119NCGe (iv)	60	100	55	15	600
050217NCGe	60	80	45	45	550
050223NCGe	60	100	45	45	550
050418NCGe (#18)	60	100	55	25	400
050419NCGe (#19)	60	100	55	60	400
050504NCGe	60	100	75	25	420
050511NCGe	60	100	60	30	420
050720NCGe	120	100	60	30	600
051117NCGe (#A14)	90	100	60	20	600

4.3 Results

4.3.1 Structural properties

(A) Ge nanoclusters on carbon film

Figure 4.3.1 shows high-resolution TEM images of crystallized Ge nanoclusters on carbon film. The size of the Ge nanoclusters grown at 600 ^{o}C, Ar gas flow rate of 40 sccm is in the range from 10-30 nm. Figures 4.3.1 (a) and (b)correspond the sputtering power of 100 and 40 W, respectively, with a fixed aggregation distance of 100 mm. It can be seen that the Ge nanoclusters are well self-organized and distributed uniformly. The mean size of the dots fabricated by higher sputtering power is 25 nm and the number density is calculated to be about 5×10^{10} cm^{-2}, while for a lower power the mean size of Ge dots is 10 nm and the density is 2×10^{10} cm^{-2}. From the inset of Fig. 4.3.1 (a), it can be clearly seen that the Ge nanocrystals are single crystalline. The observed lattice fringes are identified as {111} planes of Ge. It can also be seen from Fig. 4.3.1 (a) that the Ge nanocrystals are spherical in shape. By controlling the deposition time, substrate holder temperature and also the Ar gas flow rate, more uniform and self-organized Ge nanoclusters can be formed.

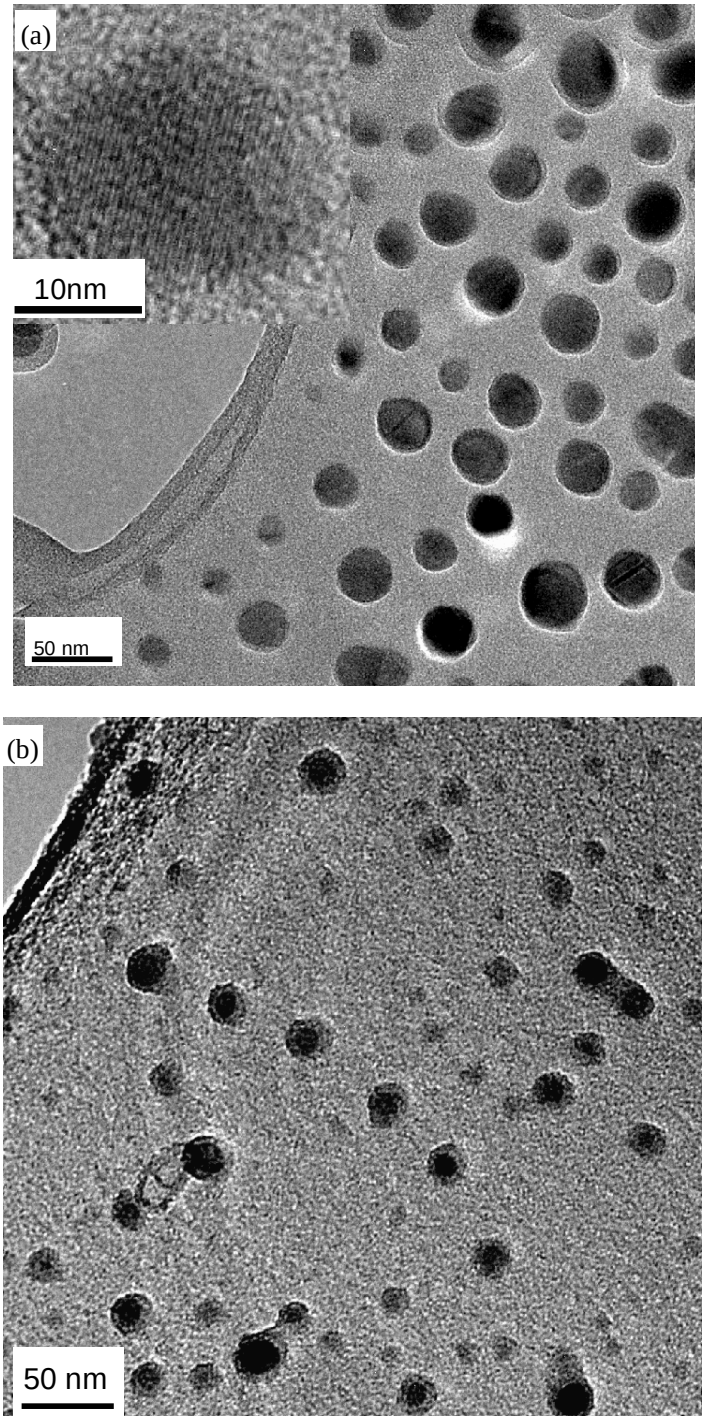


Figure 4.3.1 TEM images of Ge nanocrystals grown at 600 ^{o}C with a sputtering power of (a) 100 W and (b) 40 W. Aggregation distance is fixed at 100 mm and Ar gas flow rate at 40 sccm. Top-left inset is an image of Ge nanocrystal with a diameter of 20 nm. It shows that the as-grown Ge nanocrystals are crystalline under this condition. Bottom-left inset represents the HfAlO/Ge-NC/HfAlO/Si trilayer structure embedded with Ge-NC formed at 100 W sputtering power.

The most significant difference between nanocluster source and other vapor deposition methods is the high energy of the plasma generated by the DC magnetron sputtering of the desired target material. By controlling the pressure gradient between the UHV chamber and nanocluster source aggregation chamber, fine and dense Ge nanocrystals can be formed onto the surface of the desired substrate through a small aperture. Thus, Ge nanoclusters have a relatively high velocity towards the substrate, which leads to a uniform distribution of Ge nanocrystals by utilizing the nanocluster source. According to the observation by cross-sectional TEM as shown in the inset of Fig. 4.3.1, the height of these nanocrystals is about 30-40 nm for the 100-W sample, resulting in an increased surface roughness on the top dielectric that hinders the application in nanocrystal floating gate memory. Therefore, the sputtering power of Ge nanocluster source has been reduced accordingly in the latter runs in order to achieve the memory effect of the trilayer capacitor structure.

The Ar gas flow rate was found to be another important parameter for the growth of Ge nanocrystals. Figures 4.3.2 (a) and (b) show TEM images of the Ge nanocrystals grown at a temperature of 600 ^{o}C with Ar gas flow rates of 40 and 30 sccm, respectively. The sputtering power for the Ge dots is 40 W and aggregation distance is fixed at 100 mm. From Fig. 4.3.2 (a), it can be seen that the Ge nanocrystals are well self-organized and their diameter is about 10 nm. In contrast, the Ge nanocrystals deposited at 30 sccm, as shown in Fig. 4.3.2 (b), are less dense and smaller than thoes deposited at 40 sccm. This suggests that when the Ar flow rate decreases, less sputtering gas for initiating the plasma discharging results in lower sputtering rate, and relatively less Ge nanoclusters are formed.

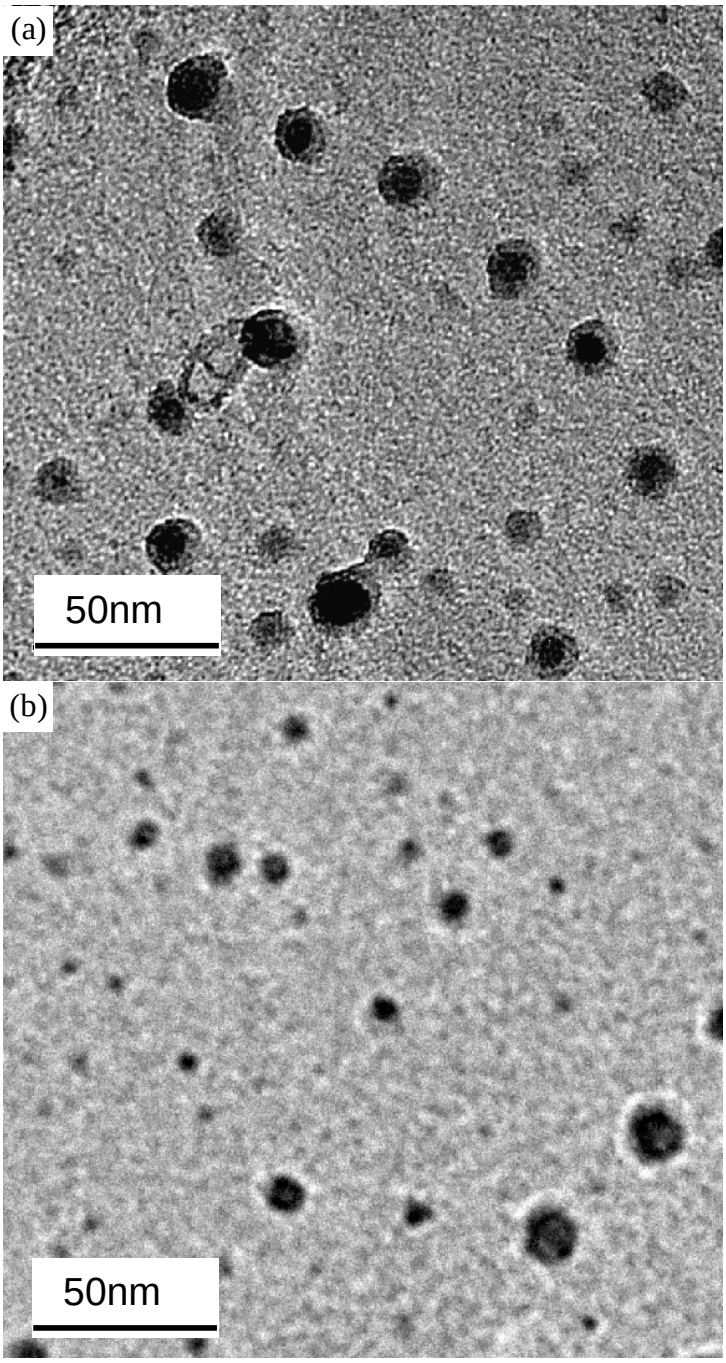


Figure 4.3.2 TEM images of Ge nanocrystals formed by nanocluster source. Both samples are grown at 600 ^{o}C with sputtering power of 40 W, and fixed magnetron-to-aperture distance of 100 mm. Only the sputtering gas flow rate is different: (a) 40 sccm and (b) 30 sccm.

The separation between the magnetron target and aperture (aggregation length) determines aggregation time and number of collisions among Ge atoms and Ar gas molecules in the aggregation region, and hence the nanocluster size. A pair of relatively lower power and lower substrate temperature samples with different aggregation distances have been investigated by TEM. Our experimental results showed that the as-grown substrate temperature affects the crystallinity of the Ge nanoclusters. When the as-grown substrate temperature is lower, i.e. 300 ^{o}C, the Ge nanocrystals are amorphous. Figure 4.3.3 (a) shows the structure of the as-grown samples containing uniform size amorphous Ge nanocluster distributed on the carbon film with a mean diameter of 10 nm. The Ge nanocrystals are isolated to each other with a larger separation as the sample is prepared at a much lower power (30 W). It is a good sample as a comparison for high-to-low power. From the TEM image, as shown in Fig. 4.3.3 (b), it can be seen that the Ge nanoclusters have very small mean diameter of less than 5 nm. It obviously points out that longer aggregation distance results in larger size of Ge nanoclusters. It can also be observed that the density of Ge nanoclusters formed under these lower power conditions is much less than that shown in Figs. 4.3.1 (a) and (b), which is around 1 $\times 10^{10}$ cm^{-2}.

To sum up, a relatively lower power, shorter aggregation length, shorter aggregation time and lower Ar flow rate of the nanocluster is necessary for the growth of Ge nanoclusters with mean diameter of 5 – 10 nm. The desired density of the nanocrystal can be achieved by controlling the time of growth.

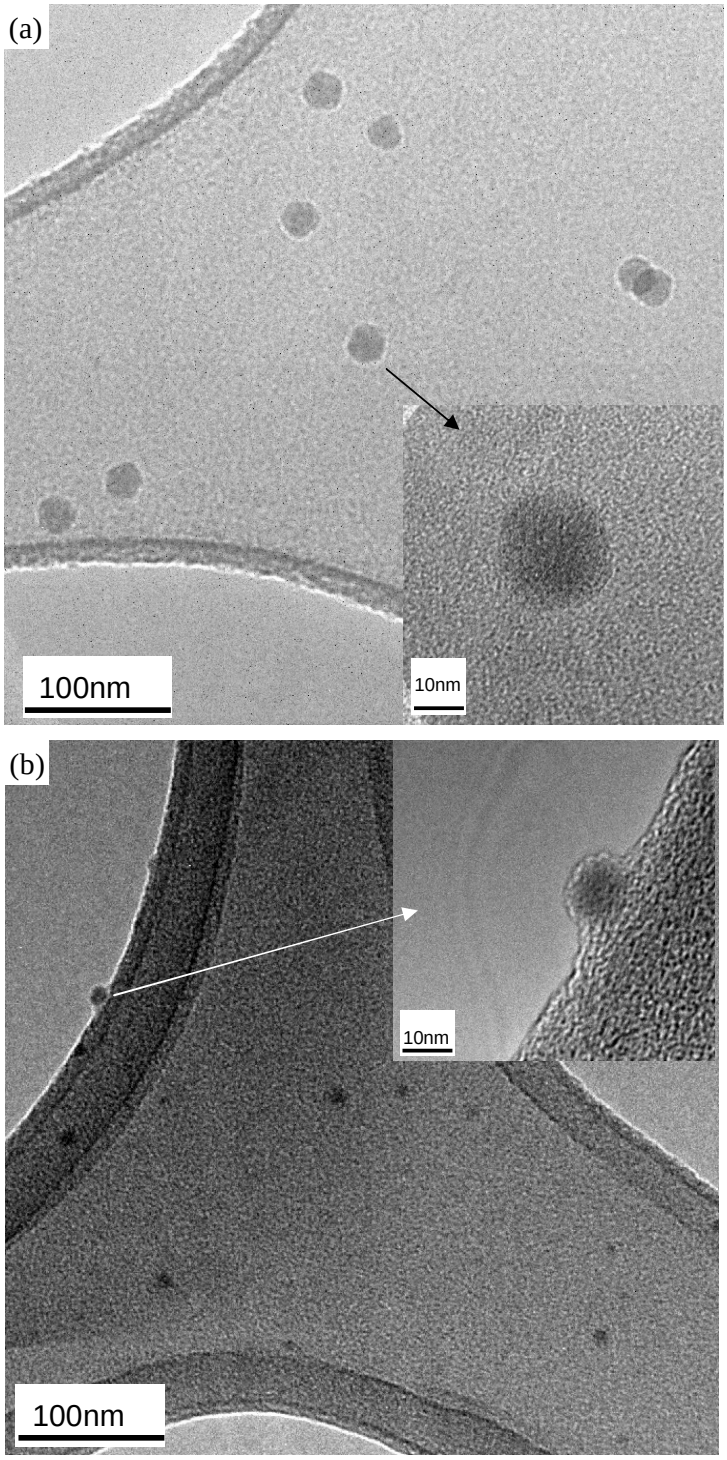


Figure 4.3.3 TEM images of low density and small mean diameter Ge nanocrystals formed by nanocluster source under the following condition: 300 °C, 30 W, 30 sccm. (a) 100 mm, and (b) 60 mm.

In order to investigate the Ge nanoclusters by means of AFM, deposition of one layer of Ge nanoclusters onto p-type Si substrate with a single thin amorphous HfAlO oxide layer on the surface was carried out. Figures 4.3.4 (a) shows an AFM image of the Ge nanocrystals grown at the temperature of 600^{o}C by nanocluster source. The average density of the as-grown Ge nanocluster on the thin layer of HfAlO is about 5x10^{12} cm^{-2}. The mean size of the Ge nanocluster is about 25-30 nm with an average separation of about 60-80 nm, average height is about 20 nm. It is also worth noting that no further high temperature thermal annealing is necessary to form the Ge nanoclusters.

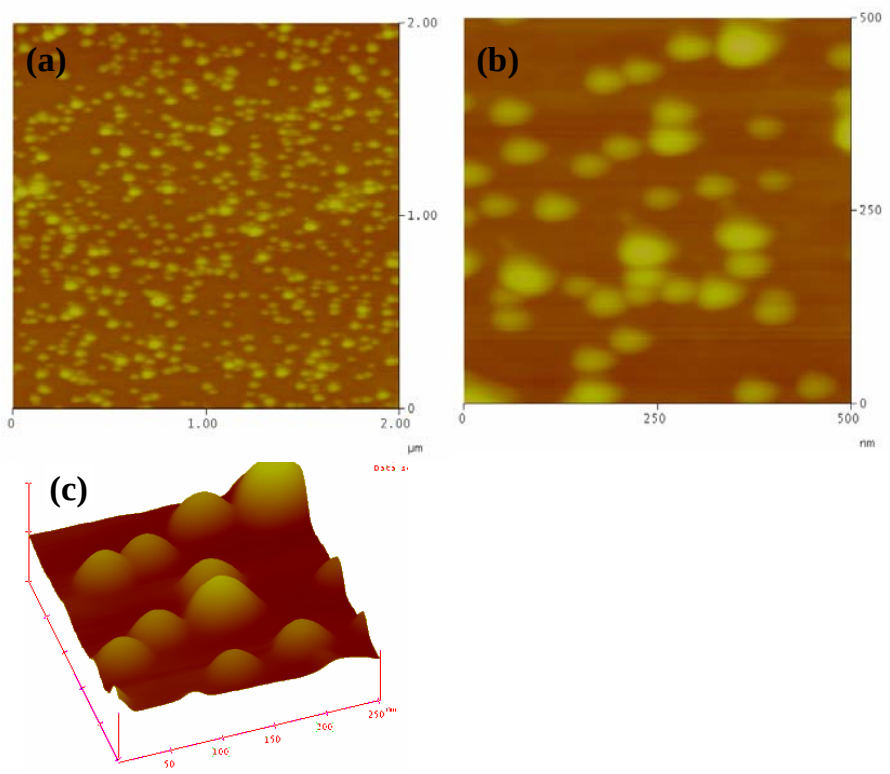


Figure 4.3.4 (a) AFM images of the Ge nanoclusters on HfAlO/Si substrate. (a) low magnification, (b) high-magnification, and (c) 3-D view.

(B) Trilayer structure

After optimizing the Ge nanoclusters growth conditions, trilayer structures with fine Ge nanoclusters are fabricated. All the as-grown and annealed samples have been examined by HRTEM, but no Ge crystal lattice fringes can be observed in the embedded layer. From the high-resolution TEM image, as shown in Fig. 4.3.5 (a), it can be seen that the HfAlO layers have an amorphous structure and the thicknesses of the tunnel and the control layers are about 5 and 15 nm, respectively. The absence of Ge crystal lattice is due to the fact that the Ge nanocluster is not crystallized. Secondary ion mass spectroscopy (SIMS) analysis as shown in Fig.4.3.5 (c) illustrates the existence of a Ge layer embedded in the HfAlO matrix. It should be noticed that, for sample with longer deposition time and sputtering power, dots can be found in the oxide film matrix (Fig. 4.3.5(b)).

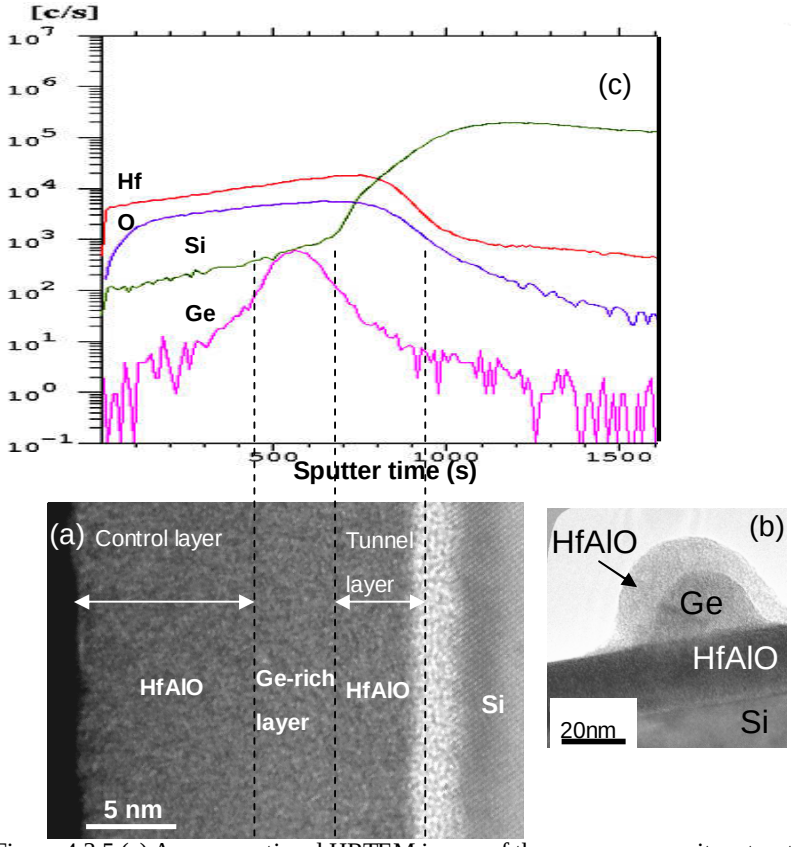


Figure 4.3.5 (a) A cross-sectional HRTEM image of the memory capacitor structure from the 15-min Ge nanocluster deposition sample, and (b) 30-min at 120W. (c) The depth profile SIMS result of the same sample in (a) showing content of Ge-rich layer inside the HfAlO oxide layer.

4.3.2 Memory characteristics

High-frequency (1 MHz) *C-V* measurement of the memory capacitors incorporating the Ge nanoclusters revealed significant counter-clockwise hysteresis loop, indicating successful charge storage in the Ge nanoclusters. Figure 4.3.6 shows the *C-V* curves of the two samples with and without Ge nanoclusters, where the control sample without Ge nanoclusters shows a typical *C-V* curve without obvious hysteresis loop; and by contrast, counter-clockwise hysteresis loops are present in the samples with the Ge nanoclusters indicating charge trapping in the capacitors. It is worth noting that the effect of mobile ions on the charge trapping can be ruled out, since no significant hysteresis was observed in the control sample under the same experimental conditions. Various positive and negative bias voltages have been applied to the MOS capacitors, and the result shows that the V_{FB} follows the bias voltage. It can be seen in Fig. 4.3.6, that the maximum flat-band voltage shift (ΔV_{FB}) for the 15 min-deposited Ge nanocluster sample is about 6.0 V under a -10 to 10 V DC sweep, and the calculated storage charge density corresponding to the hysteresis loop is up to $1\text{x}10^{13}$ cm^{-2} based on the simple formula $\Delta Q = C_a \Delta V$, where C_a is the accumulation capacitance. Since TEM examination couldn't find any Ge lattice fringes, we treat Ge as nanoclusters that are embedded in the HfAlO matrix and their size is neglected in the calculation. Ge-rich HfAlO has the memory characteristics somewhat between the SONOS and nanocrystal capacitors.

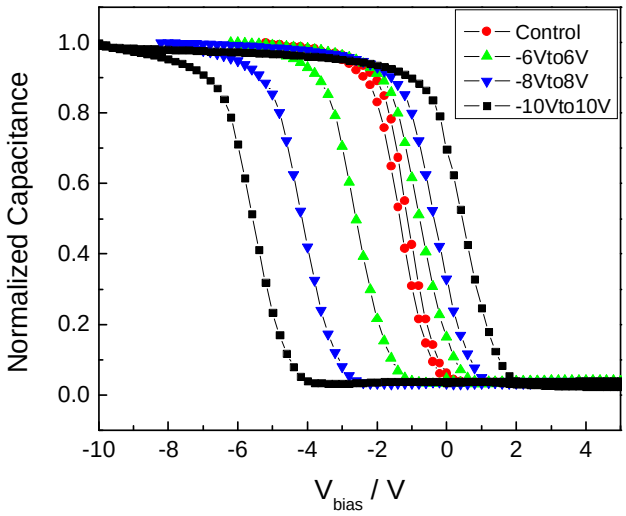


Figure 4.3.6 High frequency (1 MHz) *C-V* measurements of the trilayer floating gate capacitors with and without Ge deposition. Large counter-clockwise hysteresis loop up to ΔV_{FB} = 6.0 V can be observed in the sample of 15-min Ge nanocluster deposition. All samples are normalized with accumulation capacitance of 0.15 nF.

To compare the memory effects of different density/size of Ge nanoclusters, a group of *C-V* loops of the samples of 15, 25 and 60-min depositions are shown in Fig. 4.3.7. It can be seen that under the same sweep bias (-6 to 6 V), the ΔV_{FB} for the 15, 25 and 60-min samples are 2.3, 1.3 and 0.5 V, respectively, i.e., the longer the Ge deposition time, the smaller the ΔV_{FB}. We believe that the decrease in ΔV_{FB} for the sample with longer time of Ge deposition is because of the decrease in the nanocluster density caused by the Ge accumulation within the HfAlO matrix. The flat-band voltage shift ΔV_{FB} decreases as the thickness of Ge nanocrystal layer increases, which has been suggested based on a simulation model by Zhu *et al.*[2].

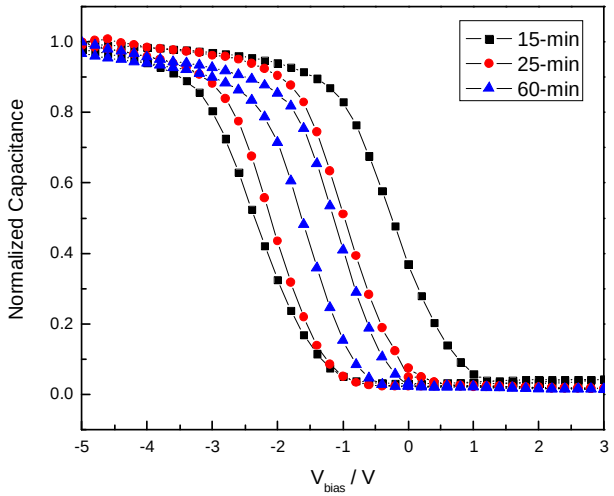


Figure 4.3.7 High frequency (1 MHz) *C-V* characteristics of the trilayer floating gate capacitors with: (1)15-min, (2)25-min, and (3)60-min Ge nanocluster deposition. All samples are normalized with accumulation capacitance of 0.15 nF.

To evaluate the characteristics of storage charges in the Ge-nanocrystal floating gate memory capacitors, the storage charge lifetime must be known. *C-t* measurement results at room temperature as shown in Fig. 4.3.8 reveal that the capacitance decreases as a function of time. After injecting electrons at 10 V for 20 s, gate voltage is changed to the flat-band voltage of -1 V, and the duration of retention is expected to be long enough to withstand the loss of charge stored in the memory nodes. It can be seen that after 10^4 seconds stress, the decay of capacitance for the floating gate memory capacitor with 60-min Ge deposition sample is 8%; while for the 25-min and 15-min Ge deposition samples, they are 14% and 35%, respectively.

It is worth noting that the Ge nanoclusters deposited for longer time decay less than that for shorter time deposition, i.e., the retention characteristic of the 60-min sample is better than that of the 15 and 25-min samples (Fig. 4.3.8). For smaller nanoclusters,

Coulomb blockade effect and quantum confinement effect are more significant for the "write/erase" process. The Coulomb blockade effect raises the electrostatic potential of the Ge nanocrystals, and the quantum confinement effect shifts the Ge nanocrystal conduction band energy upward and reduces the conduction band offset between the nanocrystals and HfAlO (the reported conduction band shift for 5-nm Ge nanocrystal is 0.15 eV)[3]. These two effects make the stored charges more easily tunnel back to the Si channel area and degrade the retention property.

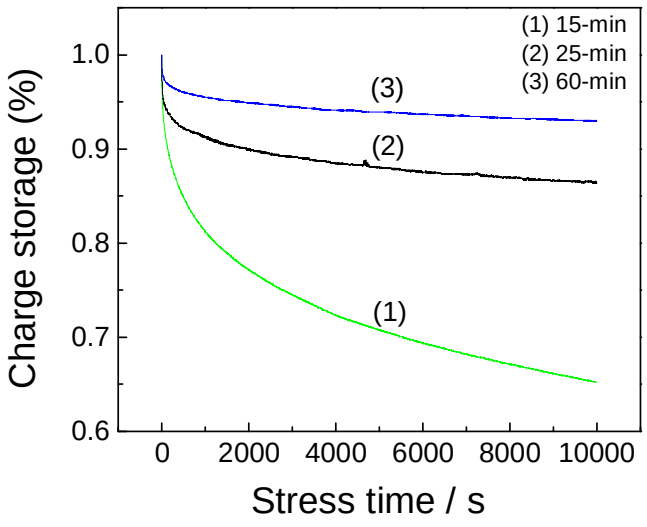


Figure 4.3.8 *C-t* characteristics of the trilayer floating gate capacitors with: (1) 15-min, (2) 25-min, and (3) 60-min Ge nanocluster deposition. The charging voltage is 10 V for 20 s and the measurement voltage is -1 V.

4.4 Summary

In conclusion, Ge nanoclusters fabricated by utilizing the NC200U nanocluster source have been investigated based on various growth conditions. Different diameters, as low as 5nm, of Ge nanoclusters with controllable densities have been acheived. Based on these preliminary results, prototype trilayer Ge-nanocrystal floating gate

capacitors with HfAlO high-*k* dielectric have been made by using PLD deposition and the NC200U nanocluster source. Memory effects have been characterized by using *C*-*V* measurements. A counter-clockwise hysteresis *C*-*V* loop has been obtained and a flat-band voltage shift of up to 6.0 V has been achieved indicating stored electrons in the Ge nano-floating gate and thus the memory effect.

References

1. K. S. Sree Harsha, *Principles of Physical Vapor Deposition of Thin Films*, 1st Ed. pp.594 (Elsevier, Oxford, 2006).
2. Y. Zhu, D. T. Zhao, R. G. Li and J. L. Liu, "Threshold voltage shift of heteronanocrystal floating gate flash memory" J. Appl. Phys. **97**, 034309 (2005).
3. M. She, and T. -J King, "Impact of crystal size and tunnel dielectric on semiconductor nanocrystal memory performance" IEEE Tans. Electron Devices **50**, 1934 (2003).

Chapter 5 Ag Nanoclusters Grown by the Nanocluster Beam Source

5.1 Introduction

Compared to semiconductor nanocrystal floating gate memory, metal nanocrystals have been less explored as charge storage elements in memory devices. However, metal nanocrystals should present, in principle, advantages and unique features over semiconductor nanocrystals memory. The major advantages of metal nanocrystals over their semiconductor counterparts include higher density of states around the Fermi level, a wide range of available work functions, and smaller energy perturbation due to carrier confinement [1]. The higher density of states makes metal nanocrystals more immune to Fermi-level fluctuation caused by contamination. The metal nanocrystals tend to have more uniform charging characteristics, resulting in more stable memory states. The wide range of available work functions provides one more degree of design freedom in engineering the trade-off between write/erase and charge retention, because the work function of nanocrystals affects both the depth of the potential well at the storage node and the density of states available for tunneling in the substrate.

By aligning the nanocrystal Fermi level within the Si bandgap under retention and above the conduction band edge under erase, a large erasing current/retention current ratio can be achieved even for very thin tunnel oxides. Therefore, the improvement of trade-off between the fast write/erase and the long retention time of flash memory can be achieved. Because writing is performed by electron tunneling from Si substrate into the nanocrystals (thus need to find available states to tunnel into) with writing current

level similar to erasing current, fast write/erase and long retention time can be achieved simultaneously in metal nanocrystal floating gate memories [1].

Metal nanocrystals also provide a great degree of scalability for the nanocrystal size. To enable single-electron or few-electron memories by the Coulomb blockade effect, smaller nanocrystals are preferred. However, for semiconductor nanocrystals, the band gap of nanocrystals is widened in comparison with that of the bulk materials due to the multidimensional carrier confinement that reduces the effective depth of the potential well and compromises the retention time. This effect is much smaller in a metal nanocrsytal because there are thousands of electrons in conduction band in a nanocrystal even in charge neutral state. As a result, the increase of Fermi level is minimal for metal nanocrystals. We can exploit the Coulomb blockade effect better with metal nanocrystals to achieve low-power memories without compromising the retention time from quantum mechanical confinement effects.[1] Wang *et al.* have proposed a fabrication method by using electron-beam evaporation method followed by annealing in N_2 ambient to synthesis high-density isolated silver (Ag) nanodots [2].

In this section, some unique features of metal nanocrystal memories in comparison with their semiconductor counterparts will be discussed. Preliminary results of Ag nano-floating gate capacitor will be presented.

5.2 Experiment

Previous chapters have discussed Ge nanoclusters fabrication method. Thus, no detail descriptions will be presented in this section, but only the growth condition of the investigated sample will be given. All the trilayer samples consist of embedment of Ag nanocrystals in the HfAlO thin film matrix (control layer – 15nm, tunnel layer – 5 nm). Growth conditions of Ag nanocrystals are as follow:

- Substrate temperature : 450^{o}C
- Ar gas flow rate : 15 sccm
- Aggregation pressure : 770 mTorr
- Sputtering power : 35 W
- Aggregation distance : 100 mm (unless specified otherwise)
- Sputtering time : 2-min (unless specified otherwise)

5.3 Results

Figure 5.3.1 shows the AFM images of the as-grown sample with 2-min Ag nanocluster beam source deposition. From these AFM images, it can be determined that the Ag nanocrystals density of 3 x 10^{11} cm^{-2} and the mean size of the Ag dots is 15 nm .

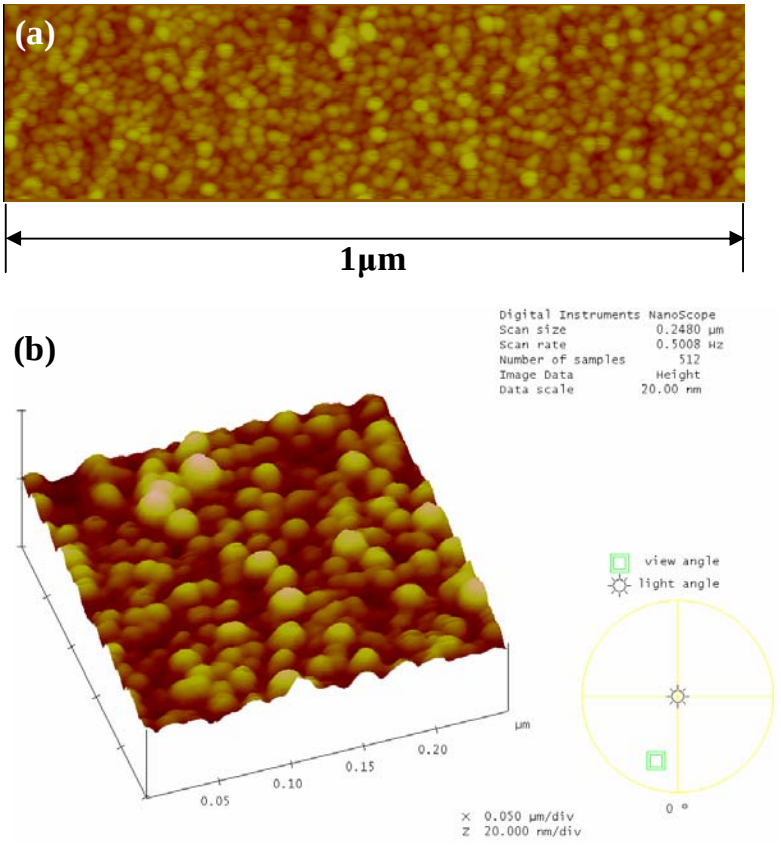


Figure 5.3.1 AFM images of the as-grown Ag nanocrystal on HfAlO; (a) surface image, and (b) 3-D view. From the AFM morphology images, the clear boundary indicates that the Ag nanocrystals are isolated from each other.

Two samples, including 2 and 5-min Ag nanocrystal (NC) depositions, have been examined by cross-sectional TEM. Figure 5.3.2 shows cross-sectional TEM images of the annealed trilayer structure of the 2 and 5-min samples containing three layers on p-type silicon substrate, i.e., the HfAlO control layer, the Ag NCs layer and the HfAlO tunneling layer. For the 2-min sample as shown in Fig. 5.3.2 (a), the Ag nanocrystals,

indicated by arrow, embedded in the HfAlO control and the tunneling layers are with a mean size of about 10 nm; while the thicknesses of the tunneling and control layers are about 5 and 15 nm, respectively. In contrast, the 5-min sample (Fig. 5.3.2 (b)) shows much higher density of Ag NCs. It is apparent that the HfAlO layers are in an amorphous structure, and Ag NCs also show crystallized lattice firings as shown in the enlarged images in the insets.

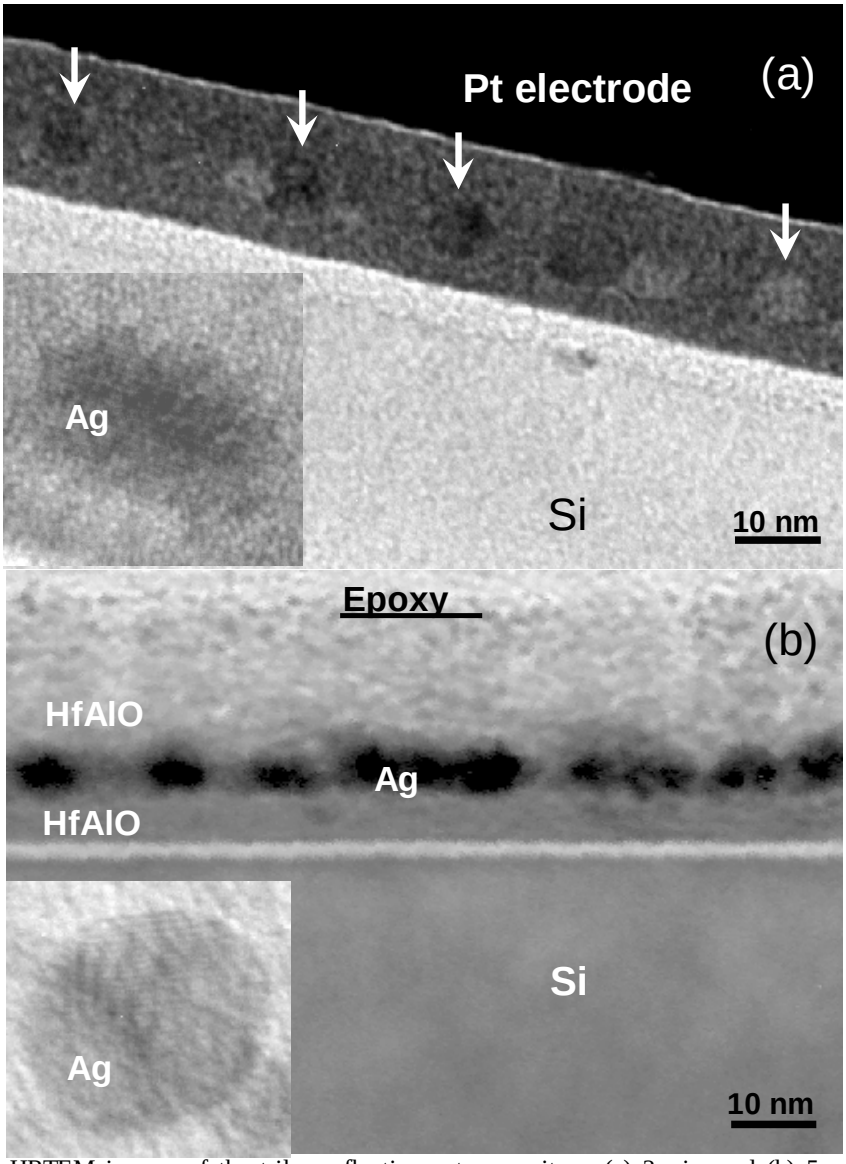


Figure 5.3.2 HRTEM images of the trilayer floating gate capacitors: (a) 2-min, and (b) 5-min Ag deposition.

High-frequency (1 MHz) *C-V* measurement of the Ag NC embedded capacitors revealed significant counter-clockwise hysteresis loop, indicating successful charge storage in the Ag NCs. Figure 5.3.3 shows the high-frequency *C-V* curves of the four samples with and without Ag NCs, where the control sample without Ag NCs shows a typical *C-V* curve without obvious hysteresis loop; and by contrast, counter-clockwise hysteresis loops present in the samples with the 1 and 2-min Ag nanocrystals indicating charge trapping in the capacitor. It can be seen that the maximum flat-band voltage shift (ΔV_{FB}) for the 2-min deposited Ag NCs sample is about 1.0 V under a - 4 to 4 V dc bias, and the calculated storage charge density corresponding to the hysteresis loop is up to $1x10^{11}$ cm^{-2} based on the formula given by Tiwari *et al.* [3] and Kim *et al.* [4]. The reason that the 2-min sample exhibits larger flat band voltage shift compared to the 1-min sample is that the 2-min sample has larger density of Ag NCs.

However, even though it is apparent that the 5-min sample possesses much larger density of Ag NCs compared to the 2-min sample, its flat band voltage shift is much smaller or even no loop can be observed. This is due to the fact that longer deposition time results in a more coalesced Ag NC layer. A relatively more continuous Ag NC layer results in easy lateral charge leakage, and therefore, if the tunneling layers is not thick enough or contains significant number of defects, the memory window (flat band voltage shift) will be inevitably narrow. In addition, we have observed that the control layer for the 5-min sample shows porous structure due to the existence of high-density Ag NCs leading to seed induced low density columnar growth.

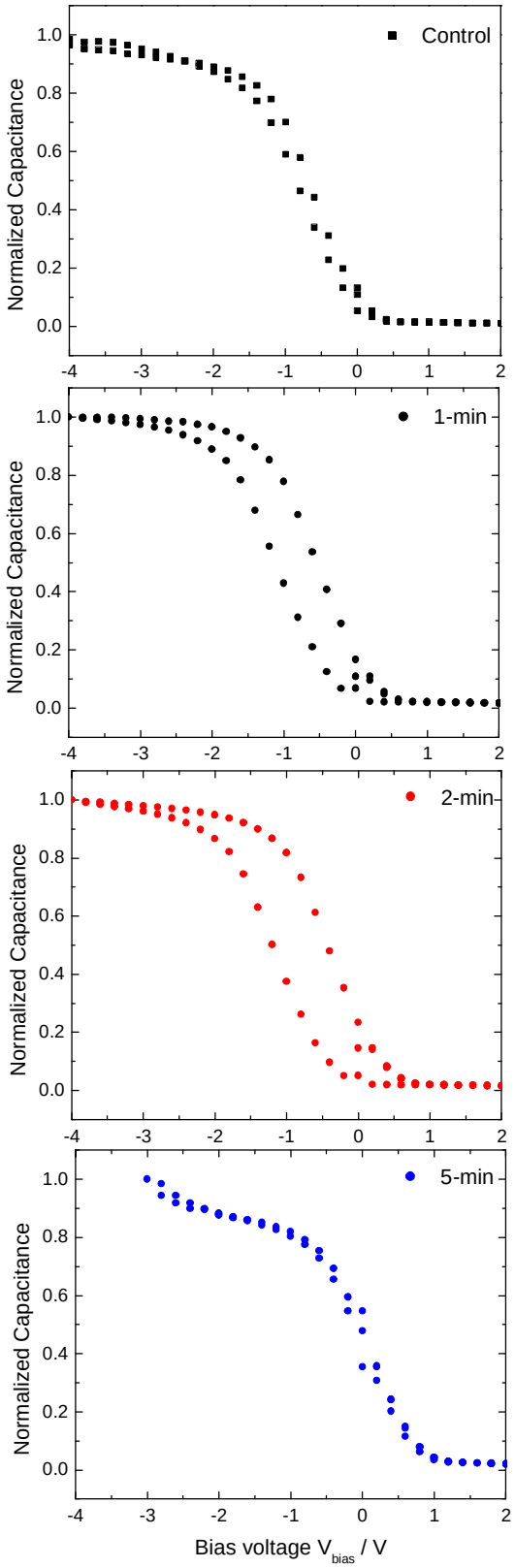


Figure 5.3.3 *C-V* measurement of the trilayer capacitor structure with different Ag nanocluster deposition time embedded in HfAlO matrix.

A unique feature for the Ag nanocrystal memory characteristic is that the flat-band voltage shift does not depend on the sweep voltage. For example, it is shown that the ΔV_{FB} under a -4 to 6 V bias is the same as that of the ΔV_{FB} under a -4 to 2 V bias (Fig. 5.3.4). This phenomenon is significantly different from semiconductor nanoclusters due to the unique electronic structure, i.e., there are plenty of states close to the Fermi energy and therefore smaller energy perturbation caused by the charge storage. By contrast, semiconductor nanocluster floating gate memory exhibits dependence of memory window on gate voltage, due to the fact that there are limited number of states in the conductive energy bands, and therefore, stored charges raise the energy level significantly and higher gate voltage is needed to make more charges tunnel from the channel area to the nanocluster [5-7].

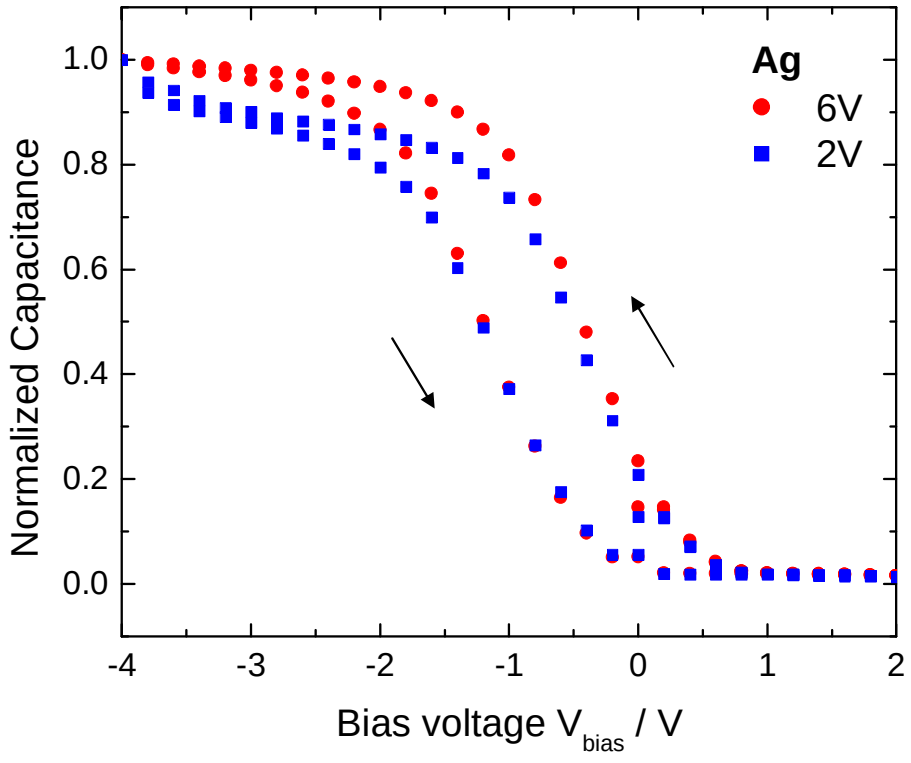


Figure 5.3.4 High frequency *C-V* measurement with (a) +6 V forward and -4 V reverse bias voltage and (b) +2 V forward and -4 V reverse bias voltage.

To evaluate the characteristics of stored charges in the Ag-nanoclusters floating gate memory capacitors, the stored charge lifetime must be known. *C-t* measurement results at room temperature as shown in Fig. 5.3.5 reveal that the capacitance decreases as a function of time. After injecting electrons at 10 V for 20 s, gate voltage is changed to the flat-band voltage of -1 V and the duration of retention is expected to be long enough to withstand the loss of charge stored in the memory nodes. It can be seen that after 10^4 seconds applied stress, the decay of capacitance, for the floating gate memory capacitor with 1 and 2-min Ag depositions, the capacitance decay is less than 10%. It is also clearly shown that no significant initial charge decay can be observed.

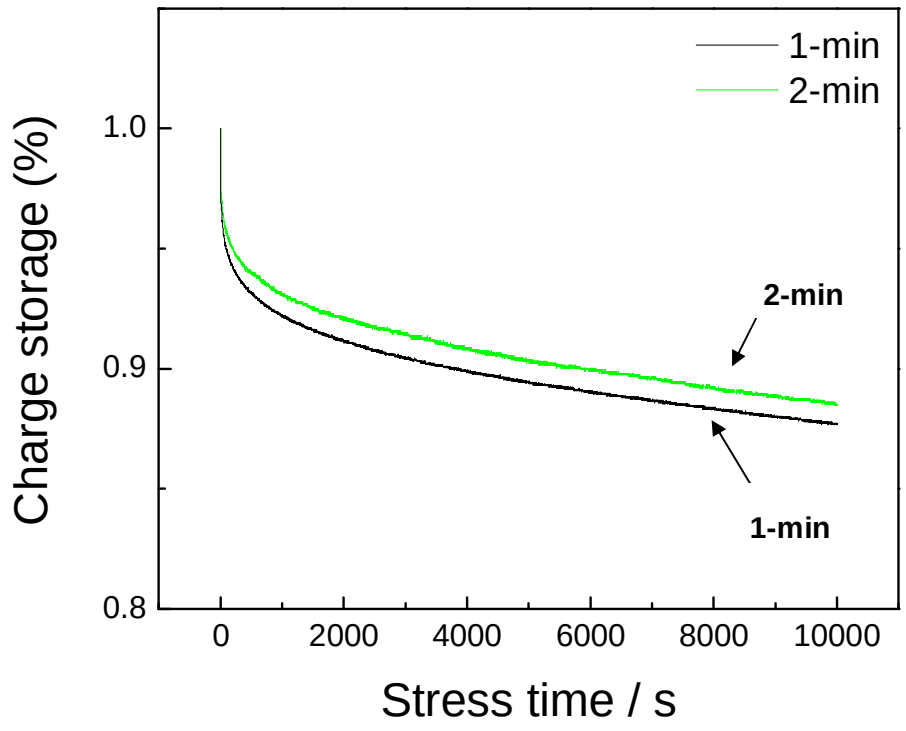


Figure 5.3.5 *C-t* characteristics of the trilayer floating gate capacitors with 1- and 2-min Ag nanocluster deposition. The charging voltage is 10 V for 20 s and the measurement voltage is -1 V.

5.4 Summary

In conclusion, trilayer Ag-nanocrystal floating gate capacitors with HfAlO high-*k* dielectric have been made by using PLD and nanocluster beam depositions. Unique memory effects with promising retention properties have been achieved. A counter-clockwise *C*-*V* hysteresis loop has been obtained and a threshold voltage shift of 1.0 V has been achieved indicating storage electrons in the Ag-nanocrystal floating gate and thus the memory effect.

References

1. Z. T. Liu, C. Lee, V. Narayanan, G. Pei, and Edwin C. Kan, "Metal nanocrystal memories – Part I: Device design and fabrication" IEEE Trans. Electron Devices **49**, 1606 (2002).
2. Q. Wang, Z. T. Song, W. L. Liu, C. L. Lin, and T. H. Wang, "Synthesis and electron storage characteristics of isolated silver nanodots on/embedded in Al_2O_3 gate dielectric" Appl. Surf. Sci. **230**, 8 (2004).
3. S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbe, and K.n Chan, "A silicon nanocrystal based memory" Appl. Phys. Lett. **68**, 1377 (1996).
4. J. K. Kim, H. J. Cheong, Y. Kim, J,-Y, Yi, H. J. Bark, S. H. Bang, and J. H. Cho, "Rapid-thermal-annealing effect on lateral charge loss in metal-oxide-semiconductor capacitors with Ge nanocrystals" Appl. Phys. Lett. **82**, 2527 (2003).
5. N.-M. Park, S.-H. Choi, and S.-J. Park, "Electron charging and discharging in amorphous silicon quantum dots embedded in silicon nitride", Appl. Phys. Lett. **81**, 1092 (2002).
6. D. N. Kouvatsos, V. loannou-Sougleridis, and A. G. Nassiopoulou, "Charging effects in silicon nanocrystals within SiO_2 layers, fabricated by chemical vapor deposition, oxidation, and annealing" Appl. Phys. Lett. **82**, 397 (2003).
7. T. H. Ng, W. K. Chim, and W. K. Choi, "Conductance-voltage measurements on germanium nanocrystal memory structures and effect of gate electric field coupling" Appl. Phys. Lett. **88**, 113112 (2006).

Chapter 6 Conclusion

In conclusion, HfAlO has been selected as the high-*k* dielectric for the nanocrystal floating gate memory structure throughout the project since it has been shown to be a promising high-*k* material. By utilizing the two different deposition techniques, pulsed-laser deposition (PLD) and the nanocluster beam source, Ge nanoclusters and Ag nanoclusters have been fabricated and promising memory characteristics have been achieved.

The trilayer nano-floating gate capacitor structure was fabricated by PLD at a relatively low temperature. Experimental results revealed that relatively low substrate temperature and growth rate are favourable for the formation of smaller-size Ge nanocrystals. The growth of Ge under our deposition follows the Volmer-Webber growth mechanism. Based on the memory effect characterization, the charge storage and charge retention characteristics have been investigated through the detailed study of the effects of different size/density of the Ge nanocrystals, various tunneling and control oxide layer thicknesses and their growth oxygen partial pressure. The self-organized Ge nanocrystals so formed were uniform in size and distribution with a controllable density. Flat-band voltage shift (ΔV_{FB}) and good retention property have been achieved.

By utilizing nanocluster beam source combined with PLD system, high quality nano-floating gate capacitors have been formed. Nanoclusters of Ge with different sizes have been formed by varying ionization power, aggregation distances and sputtering gas (Ar) pressure. Different average sizes, as low as 5 nm, of Ge nanocluster have been grown with uniform densities. Memory effect of Ge nanocluster floating gate memory structure consisting of HfAlO high-*k* dielectric tunneling and control oxides has been investigated and it revealed stored electrons in the Ge nano-floating gate and thus the

memory effect.

The nanocluster beam source has been shown to be capable in generating semiconductor and metal nanoclusters with the size of a few nanometers, which is the ideal size for nano-floating gate memory application. Silver (Ag) nanocrystals with size of 10-40 nm have been embedded in HfAlO matrix in the trilayer capacitor structure and shown a counter-clockwise hysteresis *C-V* loop indicating stored electrons in Ag-nanocrystal.

In summary, this project has proposed a nano-floating memory structure as one of the promising candidates with potential of achieving high-speed, high-density and low-power consuming memory devices. Fabrication processes of the trilayer nano-floating memory structure utilizing pulsed-laser deposition and nanocluster beam source have been developed. However, before reaching the final device fabrication stage, there is still a lot of rooms for investigating the process capability in conventional semiconductor industries. Revealing important physics, regarding quantum confinement and coulomb blockade effects in low-dimensional system, would highly improve the promise for achieving nanocrystal memory application. More work to the above aspects is expected in the near future in order to achieve further scaling of conventional flash memory devices.