LOW POWER ORGANIC FIELD EFFECT TRANSISTORS AND INVERTERS WITH HIGH DIELECTRIC CONSTANT (HIGH-K) AMORPHOUS METAL OXIDE

ZONGRONG WANG

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The Hong Kong Polytechnic University

Department of Mechanical Engineering

Low Power Organic Field Effect Transistors and Inverters with High Dielectric Constant (high-*k*) Amorphous Metal Oxide

Zongrong WANG

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CERTIFICATE OF ORIGINALITY

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(Signed)

Zongrong Wang (Name of Student)

Abstract

Organic field effect transistors (OFETs) are critical building blocks in many new generations of organic electronic devices, such as memories, bio-sensors, flexible organic light emitting diodes (OLEDs) displays. The main advantages of OFETs are lightweight, low processing temperature, compatibility with low cost flexible substrates and more. To make them suitable for portable and wearable electronics, the reduction of operating power in flexible of OFETs are becoming more important. For OFETs, low operating power means sufficient charges can be accumulated at the semiconductor/dielectric interface to generate a conductive channel at a low voltage at gate and it can be achieved by introducing high capacitance gate dielectric insulator into the device.

This thesis summarized the existing methods to achieve low operating power in OFETs, including high dielectric constant (high-*k*) inorganic dielectric and polymer dielectric, ultrathin dielectric with self-assemlely monolayers (SAMs). Although these areas have been rapidly developed since the last decade, a number of problems remain unresolved, such as high processing temperature for inorganic dielectric, instability of polymer under air and moisture, and surface specific properties in applying SAMs on the ultrathin oxide.

A new kind of metal oxide high-*k* dielectric with low processing temperature are proposed and developed by different methods have been detailed studied in this thesis.

We separately fabricated $Ba_{0.7}Sr_{0.3}TiO_3$ thin film by pulsed laser deposition (PLD) and $Ba_{0.62}Sr_{0.28}TiO_{3.03}$ thin film by UV-Ozone processing method. $Ba_{0.7}Sr_{0.3}TiO_3$ (BST-PLD) thin films of different thickness are deposited by the PLD at low temperature at 110^{o}C under vacuum environment. This is the lowest temperature of PLD applications for depositing $Ba_{0.7}Sr_{0.3}TiO_3$ thin film for OFET application that has ever been reported. OFETs devices based on BST-PLD thin films with different thicknesses are fabricated. It is found that the carrier mobility of pentacene OFET increases with the thickneses of the BST-PLD thin film. The highest mobility of 1.24cm^{2}V^{-1}s^{-1} can be obtained on 770nm thick BST-PLD film. Besides, we also investigated the flexibility of both the BST-PLD and the effect on the overall performance of OFETs. The details of the PLD processed BST is discussed in Chapter 3 of the thesis.

To further meet the needs of low cost and large area applications, sol-gel processed and solidified by UV-Ozone $Ba_{0.62}Sr_{0.28}TiO_{3.03}$ (BST-UVO) was developed. This thin film is deposited by spin coating with Ba-Sr-Ti sol solution and solidified by UV-Ozone at room temperature in ambient atmosphere. Pentacene OFETs on both Si and polyethylene naphthalate (PEN) substrates based on BST-UVO thin film are fabricated. The technical detials of this method and the performance of devices are discussed in the Chapter 4.

After succeeding in obtaining high quality solution-processed dielectric by the low temperature UV-Ozone processing, we take a step further to investigate the surface

properties of these high-*k* films under different storage conditions and their applications in both solution and vacuum processed transistors. The surface energy of BST-UVO thin film is found to be decrease with storage time in ambient air and decreases even faster when stored in evaporation chamber with diffusion pump. like 6,13-Bis (triisopropylsilylethynyl) pentacene (TIPS-pentacene) OFETs fabricated by DPC method, a new solution processing method, on the high surface energy fresh BST-UVO surface can achieve an averaged mobility of 0.11$cm^2V^{-1}s^{-1}$. The longer storage time in the evaporation chamber, the smaller surface energy would be obtained due to the surface contamination. By separately loading the BST-UVO thin films into the evaporation chamber for 5 hours and hours respectively, the work of adhesion between the BST and [2,3-b:2′,3′-f]thieno[3,2-b] thiophene (DNTT) are calculated to be 86.8 and 71.02 mJ/m^2, which gives different OFET device performance due to different growth mode of the semiconductor. The OFET devices based on 5h stored BST-UVO showed layer-island growth mode and higher average mobility of 1.51$cm^2V^{-1}s^{-1}$. The OFET devices based on 24h stored BST-UVO showed island growth mode and lower average mobility of that of 1.12$cm^2V^{-1}s^{-1}$. Two kinds of logic inverters consisting of two DNTT transistors are fabricated on PEN substrate. The saturated load one showed full-swing performance and shows a high gain as 25 and the depleted showed the gain of 12. The detailed surface energy calculation and the device performances are disussed in the Chpater 5.

Publications

Journal papers

1. Low cost universal high-*k* dielectric for solution processing and thermal evaporation organic transistors, Zongrong Wang, Xiaochen Ren, Congcheng Fan, Ya-Huei Chang, Hanying Li, Hongzheng Chen, Shien-Ping, Feng, Sanqiang Shi, and Paddy K. L. Chan, ***Advanced Materials Interfaces***, DOI: 10.1002/admi.201300119.

2. Zongrong Wang, Xiaochen Ren, Chi Wah Leung, Sanqiang Shi and Kwok Leung Chan, A UV-ozone treated amorphous barium–strontium titanate dielectric thin film for low driving voltage flexible organic transistors, ***Journal of Materials Chmistry C***, 2013, 1: 3825.

3. Zongrong Wang, Jianzhuo Xin, Xiaochen Ren, Xiaolei Wang, Chi Wah Leung, Sanqiang Shi, A. Ruotolo and Kwok Leung Chan, Low power flexible organic thin film transistors with amorphous $Ba_{0.7}Sr_{0.3}TiO_3$ gate dielectric grown by pulsed laser deposition at low temperature, ***Organic Electronics***, 2012, 13: 1223.

Conference presentations

1. Zongrong Wang, Xiaochen Ren, Congcheng Fan, Ya-Huei Chang, Hanying Li, Hongzheng Chen, Shien-Ping, Feng, Sanqiang Shi, and Paddy K. L. Chan, Low cost universal high-*k* dielectric for solution processing and thermal evaporation organic transistors, **MRS Fall, 2013, Boston**

2. Zongrong Wang, Xiaochen Ren, Chi Wah Leung, Sanqiang Shi and Kwok Leung Chan, Low temperature UV-Ozone treated amorphous barium strontium titanate dielectric thin film for the low driving voltage flexible organic transistors, **MRS Spring, 2013, San Francisco.**

3. Zongrong Wang, Jianzhuo Xin, Xiaochen Ren, Chi-Wah Leung, Sanqiang Shi and Paddy K. L. Chan, "High mobility low driving voltage organic transistor with high-*k* amorphous BST ($Ba_{0.7}Sr_{0.3}TiO_3$) gate dielectric on flexible substrate, **MRS Fall 2011, Boston.**

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Chapter 1. Introduction

The traditional silicon based transistors have been widely adopted as the key building blocks in the integrated circuit of computers, smart phones and displays industry for the past decades. Limited by the silicon wafer size, rigid nature of silicon and the high cost of silicon technology process, the industry calls for low cost candidate materials and techniques for low cost, flexilbe, portable and large area applications. Amorphous Si dominated the backplane market for liquid crystal display due to the well-developed techniques then. However, market turns the attention from the liquid crystal displays to the OLEDs for its instability[1]. The low processing temperature of organic material in OLEDs makes it possible to fabricate electronic devices on flexible substrates. Based on the strengths of OLEDs in the display application, new materials and new structures of new generation transistors (organic thin film transistors) for the OLED application draw intensive attention from both scientific and industry fields. Aside from OLED displays, sensors [2, 3] and radio frequency identification tags (RFIDs) [4] are the most promising applications based on organic thin film transistor too.

Many kinds of newly emerging organic electronic devices, like wearable temperature sensors for infants monitoring, flexible cell phones and other portable devices, the operating power must be low enough to be powered by batteries and then portable. As the switch unit in the integrated circuits, the operating voltage of transistor will mainly determine the operating power of the devices. The operating voltage of

transistors can be lowered by increasing the capacitance of the insulating layer. Higher capacitance can be realized for the commercial and widely used dielectric SiO_2 by decreasing the thickness. However, several serious problems may occur when the thickness is decreased to some extent, like large leakage current and significant manufacturing difficulties. Alternatively, three other different main solutions are proposed to get high capacitance. Firstly, ultra thin high-*k* inorganic with SAMs or multilayers are widely used. In this case, the capacitance of the dielectric increased by decreasing the thickness of the dielectric layer to a few nanometers without incurring leakage currents with SAMs blocking the leakage current. Yet, as the two ends of the monolayer moceculers, namely, terminal and functional groups of the SAMs may only work for particular gate electrodes, dielectrics and organic semiconductors. Different SAMs are required for various transistors and furthermore, it is also difficult to apply SAMs in OFETs with the top gate. Then, conventionally used SiO_2 in OFET requires to be replaced by high-*k* ones. Secondly, many kinds of inorganic high-*k* dielectric materials have been applied to replace SiO_2 and low operating voltage OFET are obtained. However, due to the high processing temperature, it is hard for them to be incorporated with flexible substrates as well as fragile substrate. Thirdly, high-*k* polymer dielectric are also pomising candidate. However, they are usually processed in inert atmosphere and some of them are really sensitive to moisture, which also limit their application in wearable sensor on human skin.

The main target of this theis is to propose brand new high-*k* dielectrics, processed at low temperature, versatile on all the structures and easy processing in air and so on. Before that, in chapter 2, we first introcued two main types of organic thin film transistors. The basic concepts and working mechanism of OFETs are introduced in detail. Many important factors of gate dielectric affecting the performance of the OFETs are summarized and discussed. At last, motivations for replacing SiO_2 with high-*k* dielectric materials were proposed and the current research are reviewed.

Chapter 3 demonstrated high-*k* BST dielectric derived by PLD at low temperature of 110^{o}C in vacuum. Pentacene OFETs on both silicon and PEN substrates are also fabricated with operating voltage less than 3V. From the high resolution transmission electron microscopy (TEM), the amorphous nature was confirmed. Atomic force microscope (AFM) mage of the pentacene deposited on top shows apparent layer-island growth mode. The highest mobility of OFET on silicon and PEN substrate are 1.24 and 1.01 $cm^2V^{-1}s^{-1}$, respectively. BST thin films with different thicknesses were investigated for the OFETs devices. Higher mobility was obtained for thicker BST thin film. Also the bending test of the flexible device shows decent flexibility. The mobility of OFETs on PEN substrate can maintain at around 0.5 $cm^2V^{-1}s^{-1}$ or higher even the bending radius is around 3mm for both upward and downward bending tests. These results show the high application potentials of the low temperature PLD growth high-*k* BST for the flexible circuits and portable electronics. To the best of our

knowledge, it is the first demonstration of amorphous BST thin film grown by PLD at low temperature for flexible OFET applications.

Chapter 4 demonstrates another newly-invented BST thin film derived by sol-gel and UV-Ozone method at low temperature of 85^{o}C in air atmosphere. The amorphous characteristic of BST was confirmed by high resolution TEM. The thickness was only around 28nm. Based on BST thin film, pentacene OFETs are fabricated on both silicon and PEN substrate. On top of the BST thin film, pentacene layer also shows layer-island morphology from AFM. For the OFET devices, they can be operated at voltage lower than 3V. OFET devices show mobility of 0.289cm^{2}V^{-1}s^{-1} and 0.252cm^{2}V^{-1}s^{-1} on silicon and PEN substrate. Also the inverter devices consisting of OFET and a resistor of 330 MΩ showed high gain of 20. Results showed that ultrathin BST thin film derived by UV-Ozone is promising in OFET and related electronic.

Chapter 5 demonstrates the universal application of UV-Ozone derived BST thin by fabricating OFETs with both solution processd and thermal evporated organic semiconductor on top of BST with different surface energy. By storing fresh deposited BST thin film after UV-Ozone in different atmospheres for different times, the surface energy drops slowly. For the BST thin films stored in evaporation chamber with diffusion pump, faster decrease in surface energy was observed. On fresh BST with high surface energy, TIPS-pentacene OFET devices are fabricated by droplet-pinned crystallization (DPC) method (one of the solution processing methods) and the averaged mobility is 0.11cm^{2}V^{-1}s^{-1}. The work of adhesion, caclulate from surface

energy of both BST and DNTT, between BST and DNTT are around 86.8 and 71.02 mJ/m^2 for BST stored in chamber for 5h and 24h, respectively. This results in different growth mode of the DNTT, which gives different OFET device performance. The OFET devices based on 5h stored BST show higher average mobility of $1.51 cm^2V^{-1}s^{-1}$. Two kinds of logic inverters are fabricated based on two p-channel DNTT inverters, including saturated load and depleted load inverters. The saturated load one showed full-swing performance and shows a high gain as 25.

Chapter 6 summarized the work and proposed three future working directions. For the solution processing OFET devices, only p-channel results are shown. In the future, n type solution processed semiconductors will be investigated to realize all solution processing and low operating power CMOS-like inverter device. Besides, based on the imporantce of presssure sensor based on OFET for the future real application and the normally high operating voltage for present research, other two future research directions will be in lowering the operating power of pressure sensor. Combining high-*k* BST and polydimethylsiloxane (PDMS) as bilayer is one way, and another is realizing percolation effect by introducing conductive phase into PDMS.

Chapter 2. Background of organic thin film transistor

2.1 Introduction of organic thin film transistors

There are mainly two different types in the family of organic thin film transistors depending on the different gate dielectric materials. One is OFETs type (see Figure 2.1) [5] and another is electrical double layer (EDL) type (see Figure 2.2) [6]. The former ones use normal solid dielectric materials and the devices work as capacitors, where the conducting channel between source and drain works as one electrode and gate electrode is another electrode. The gate electrode is used to control the charges in the channel by the electric field in the dielectric layer in between the channel and the gate

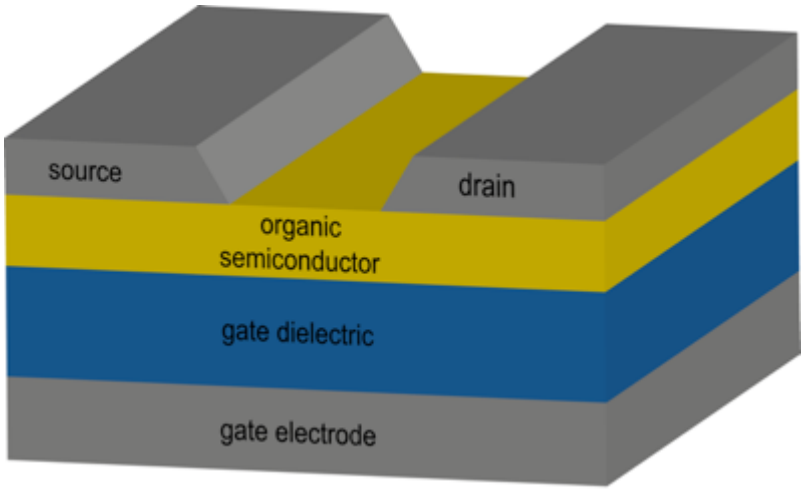

Figure 2.1 Representative structure of organic field effect transistor

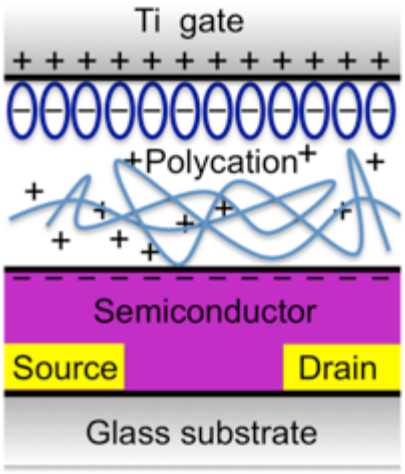

Figure 2.2 Schematic of electrical double layer transistor

electrode. For the EDL type, there is no solid dielectic layer, the interface layer between electrolytic solution and the semiconductor plays the role of dielectric. Then the capacitance of this interface layer could be very high (on the order of $\mu F/cm^2$), and the operationg voltage is ususally very small (lower than 1V). In this type of device, the active layer of organic seminconductor is directly in contact with the solvent of the electrolyte which may probably penetrate into the semiconductor layer, expecially the polymer semiconductor, [7] which will jeopardize the stability of the transistor device.

In the current thesis, I focus on the gate dielectric study of the OFET type. The application of OFETs devices in practical electronic circuits started in the late 1980s.[8, 9]. As the crucial part in almost all the circuit, it experienced rapid development in the research field. Almost every part and the corresponding technology of the OFETs

devices is hot topic, including the electrode materials, the organic semiconductor materials, gate dielectric materails and all the deposition technologies for all these parts. Here, both the dielectric and the semiconductor parts will be discussed in details.

A typical OFET device is composed of three parts, including gate dielectric layer, organic semiconductor layer and electrodes (gate, source and drain electrodes (S/D)). The characteristic defining of OFET is that the electric field created between gate and source electrodes in gate dielectric modulate the conductivity of channel between source and drain electrodes in organic semiconductor layer. There are four different arrangement of these three parts which result in four different structures of OFETs, as shown in Figure 2.3. For the configurations of Figure 2.3 (a) and (b), the gate dielectric layer is deposited on top of the gate electrode, which is called bottom gate (BG). While in configurations shown in Figure 2.3 (c) and (d), gate electrode is deposited on top the gate dielectric, which is defined as top gate(TG). For both of two configurations of BG and TG, there are two kinds of different contacts configurations depending on the order of the organic semiconductor and the S/D electrodes. If the the S/D electrods are on top of semiconductor, it will be top contact (TC). Otherwise, it will be bottom contact (BC). Ususlly, BC suffers from larger contact resistance. When considering getting started on silicon substrate as well as gate electrode, BGTC is the structure that will be used for all the OFETs in this thesis.

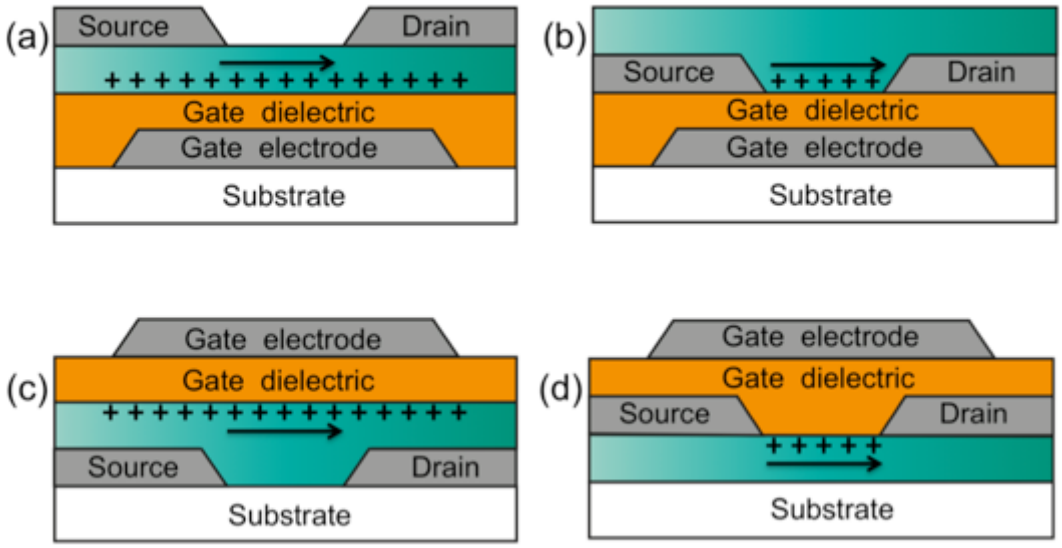

Figure 2.3 Four common organic-transistor geometries: (a) bottom gate, top contact (BGTC); (b) bottom gate, bottom contact (BGBC); (c) top gate, bottom contact (TGBC); and (d) top gate, top contact (TGTC).

With so many different structures, then the question is how does OFET work? Working as switches in the integrated circuit, same as inorganic transistors, OFETs have two states, known as the “on state” and ” off state”. “on state” means the resistance of the transistor device is smaller, and in this case device is called to be turned on. ”off states” means the resistance of the transistor device is much larger, and the device is called to be turned off then. Different from inorganic ones, the “on state”

of OFET is working as the accumlation of the majority carriers but the inorganic ones are working as the inversion of the minority carriers in the active semiconductor layer.

Figure 2.4 shows the schematic of working mechanism of a representative p type OFET device with BGTC architechture. Basically, the holes are injected into organic semiconductor from source electrode by applying negtive voltage on drain electrode relative to source and the holes will be accumulated by applying negtive voltage on gate electrode relative to source. Once the gate voltage is high enough, conducting channel will be formed and resistance between drain and source electrodes will be much smaller, which becomes “on state”. When the positive or no voltage is applied on the gate and drain electrodes, holes can not be injected and no conducting channel will be formed, which is then “off state”. From the viewpoint of band diagram, it is easier to understand the working mechanism. For instance, Shea and co-authors proposed

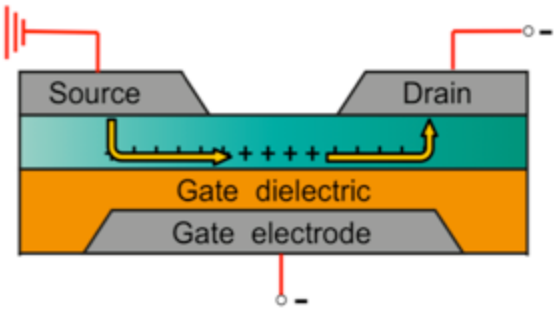

Figure 2.4 the working mechanism of a representative OFET device

band diagram of tetrabenzoporphyrin (29H, 31H-tetrabenzo [b, g, l, q] porphine (TBP, p type) OFET device with n++ Si as gate electrode and SiO_2 as gate dielectric, as shown in Figure 2.5 and Figure 2.6 [10]. From Figure 2.5, it can be noticed that holes will accumulate in the semiconductor TBP where is adjacent to interface between itself

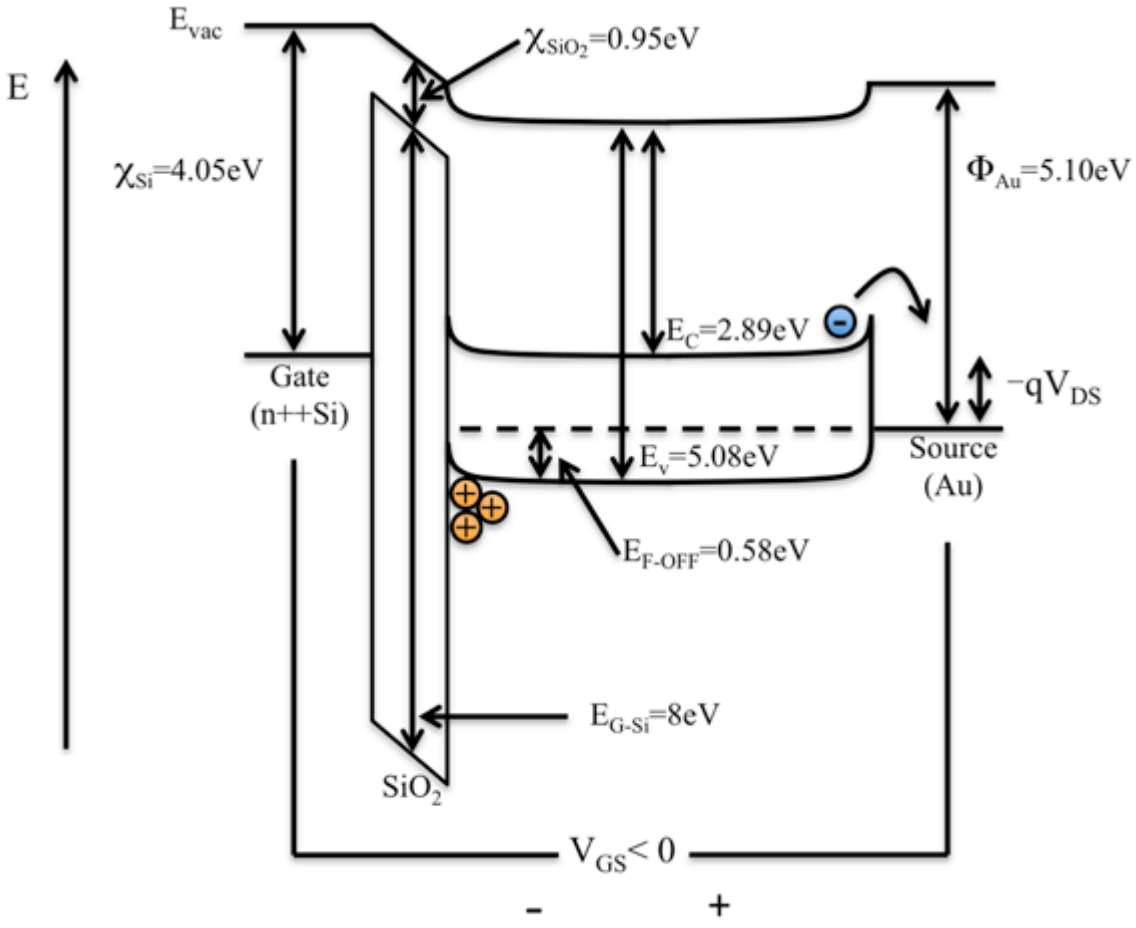

Figure 2.5 Proposed energy band diagrams in gate to source path for a TBP OFET with n++ Si as gate electrode and Au S/D electrodes.[10]

and SiO_2 gate dielectric when negtive voltage is applied on the gate electrode. Once negtive voltage is applied on drain electrode, then the holes which are injected into the organic semiconductor layer from source electrode are driven from source to drain to form a conducting channel, as shown in Figure 2.6. At this time, the device will be turned on. On the other hand, if the positive voltage is applied on, due to the energy barrier, no conducting channel can be formed, and the device will be turned off. One

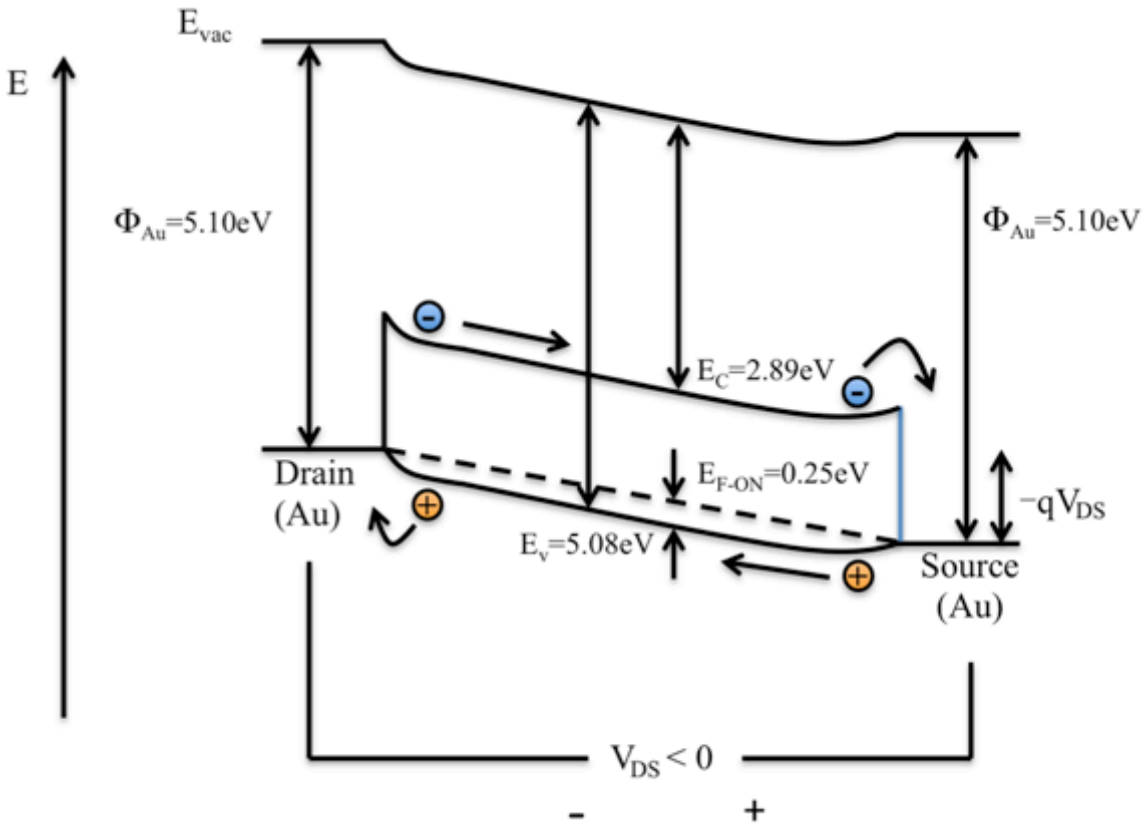

Figure 2.6 Proposed energy band diagrams in drain to source path for a TBP OFET with n++ Si as gate electrode and Au S/D electrodes.[10]

thing that we need to pay attention to their work is the authors determined Fermi level E_F by measuring the thermal activation energy of the drain current, namely E_A, for both OFF-state and the ON-state. The measured activation energy OFF-state corresponds to the energy of raising a charge carrier from bulk Fermi level to the valence bandedge. In this case, the activation energy of the OFF-state is almost equal to a bulk TBP Fermi level of about 0.58±0.1V. The exact values maybe different for various devices, but the basic working mechanism should be same like proposed in Figure 2.5 and Figure 2.6.

2.2 Basic characterizations and parameters of OFETs

2.2.1 Basic characterizations of OFET

Four different structures of OFET wree introduced in 2.2.1. However, no matter what architecture of OFET, the gate electrode is always isolated from the organic semiconductor by the gate dielectric materials, which will creat electric field in gate dielectric by applied voltage on gate electrode with reference with the source electrode. Then the voltage applied on gate electrodes control the conductance of channel region of organic semiconductor by this electric field, which result in the I_{DS} versus V_{DS} at different V_{GS} and I_{DS} versus V_{GS} at constant V_{DS}, namely output and transfer curves, respectively. Figure 2.7 (a) shows the schematic stucture of a representative pentacene OFET of BGTC structure with heavily doped Si and SiO_2 modified by octadecyltrichlorosilane (OTS) as gate electrode and gate dielectric, respectively. Pentacene is the active organic semiconductor. The channel is formed by thermal evaporating drain and source electrods through mechanical shadow mask, which are silver electrodes here. Channel width (W) and length (L) are with (W/L=20) indicated in the figure. Figure 2.7 (b) and (c) show the typical output (I_{DS} versus V_{DS} with different V_{GS}) and transfer curves (I_{DS} versus V_{GS} with constant V_{DS}) of the OFET as discussed previously. For the output curves, there are two regimes, linear regime where the V_{DS} is low and saturation regime where $V_{DS}>V_{GS}$. In two different regimes,

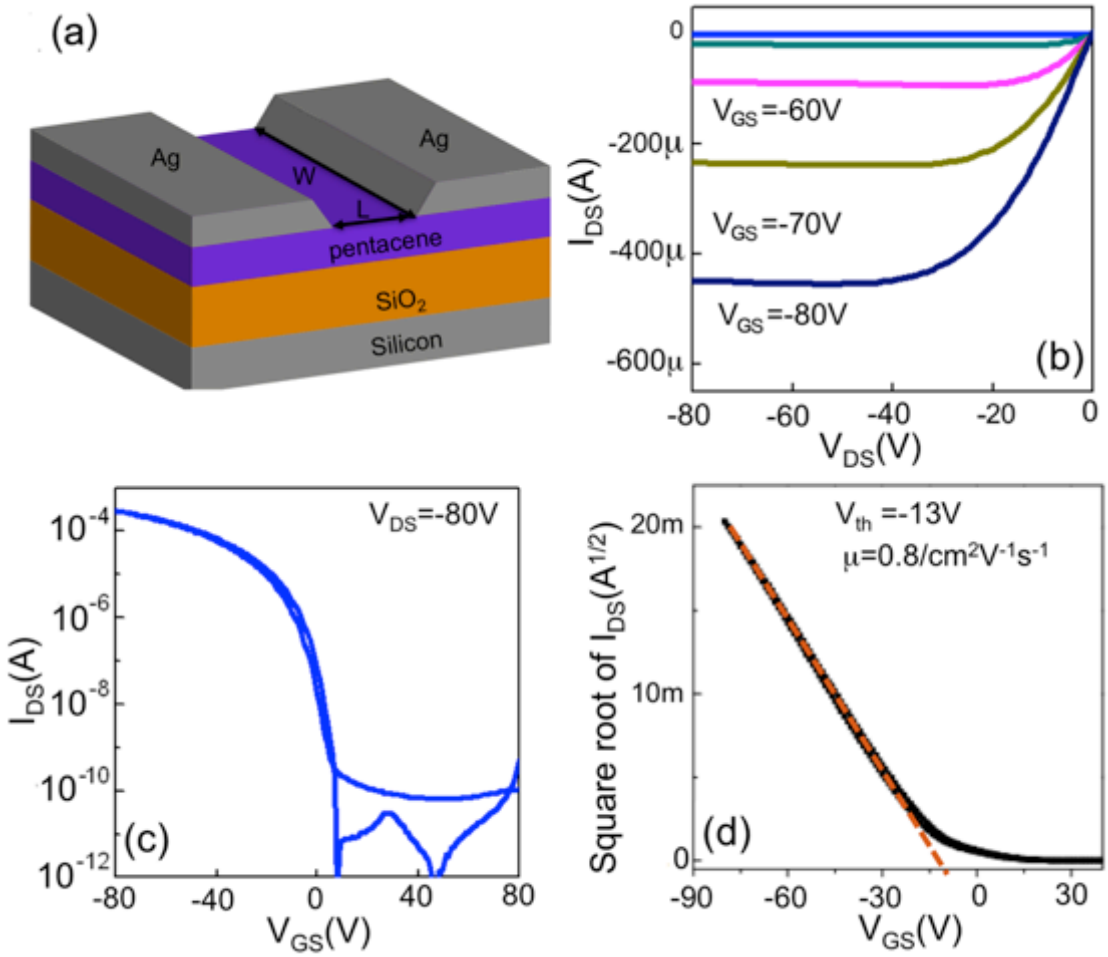

Figure 2.7 (a) The schematic structure of pentacene OFET with SiO_2 as gate dielectric material; (b) the corresponding output curve of the transistor; (c)The corresponding transfer curve of the transistor ; (d)Squrare root of (I_{DS}) (of the transfer curves shown in (c))versus V_{GS}.

different current versus voltage relationships can be described by Equation 2.1 and 2.2 [11].

In the linear regime,

$$(I_{DS})_{lin} = \frac{W}{L}\mu C_i \left(V_{GS} - V_{th} - \frac{V_{DS}}{2} \right) V_{DS} \qquad V_{DS} < V_{GS} \qquad \text{Equation 2.1}$$

For the saturation regime,

$$(I_{DS})_{sat} = \frac{W}{2L}\mu C_i \left(V_{GS} - V_{th} \right)^2 \qquad V_{DS} \geq V_{GS} - V_T \qquad \text{Equation 2.2}$$

In the two equations, $(I_{SD})_{lin}$ is the drain current in the linear regime, $(I_{SD})_{sat}$ is the drain current in the saturation regime, μ is the field effect carrier mobility of the semiconductor, W is the channel width, L is the channel length, V_{th} is the threshold voltage, V_D is the drain voltage, V_G is the gate voltage and C_i is the capacitance per unit area of the gate dielectric layer. The plot of Square root (I_{DS}) versus V_G shown in Figure 2.7 (d) is actually the relashioship based on Equation 2.3 below[12].

$$\sqrt{(I_{DS})_{sat}} = \sqrt{\frac{W}{2L}\mu C_i} \left(V_{GS} - V_{th} \right) \qquad \text{Equation 2.3}$$

2.2.2 Basic parameters of OFET

Field effect mobility (μ): μ is the one of the key parameters of interest—how quickly OFETs can switch. Different from the inorganic counterparts, OFETs working in the accumulation mode of majority charge carries. In this case, the mobility of majority carriers in organic semiconductor is of more interest. The charge carriers

transporting in organic compounds occurs within molecules (intramolecular), between molecules (intermolecualr), and between grains. These multiple 'barriers' strongly slow down the charge carriers. It has been shown that, larger grain size gives higher mobilty for less grain boundaries. [13] Besides, the mobility also depends on other parameters, like gate voltage, temperatureand so on. [14, 15] By plotting the I_{DS} versus V_{GS} in the linear regime according to Equation 2.1, the linear mobility of OFETs can be obtained from the slope. The saturation mobility of the transistor device can be derived from the slop of the straight line of $\sqrt{(I_{DS})_{sat}}$ again V_{GS}.

Threshold voltage (V_{th})*:* V_{th} is the voltage necessary to induce the charge required to completely populate the deep trap energy levels with charge carriers in an OFET. Threshold voltages are expressed by the equation $V_{th} = Q_{deep}/C_i$, where Q_{deep} is the charge necessary to completely occupy the deep trap energy levels and C_i is the capacitance of the gate dielectric.[16] V_{th} is the extrapolation of the line of $\sqrt{(I_{DS})_{sat}}$ again V_G to zero current for the saturation regiem. Basically, V_{th} determines the operating voltage of OFETs. If the V_{th} is small, then the device can be turned on with small voltage, then the operation voltage of OFET device will be low.

On/off ratio: It is actually on/off current ratio. This parameter indicates the extent to which OFET device can be turned off. It is particularly important in applications such as active matrix displays and logic circuits. The on/off ratio is extracted from transfer curve, as shown in Figure 2.7 of I_{DS} versus V_{GS}, which is the ratio of the maximum current to the minimum current.

Subthreshold slope (*SS*): SS indicates how efficiently the gate field modulates the "off" to "on" current and how abruptly the device turns "on". [17] It is calculated by Equation 2.4.

$$SS = \frac{dV_{GS}}{d\log I_{DS}} \qquad \text{Equation 2.4}$$

SS depends not only on the nature of the organic semiconductor but also on the chemical structure and dielectric properties of the insulator. The surface property of the gate dielectric also affects the SS value by the capacitance resulting from interface traps, shown as the Equation 2.5, which relates SS to the density of shallow trap level. [18]

$$SS = \frac{k_B T}{e\ln(10)}(1+\frac{C_{if}}{C_i}) \qquad \text{Equation 2.5}$$

where C_{if} is the capacitance resulting from the interface traps, k_B is the Boltzmann constant and e is the unit electric charge. The interface trap density is given by C_{if}/e. It is clear that the inferace traps will dominate the SS, which means less traps, smaller SS. And the transistor devices will be easily to be turned on.

2.3 Semiconductor mateirals

Many organic seminconductor materials have been used for OFET application, including p-type and n-type. Figure 2.8 shows some representative p type ones, including pentacene, ruberene for p type. Figure 2.9 lists some representative n type ones, including perfluorinated copper-phthalocyanine($F_{16}CuPc$) and so on. Typically, mainly two kinds of methods are widely used for deposition of different semiconductor materaials, physical methods for small moleculers and solution processing for polymer material.

The widely used physical methods include Organic molecular beam deposition, vacuum thermal evaporation, Organic Vapor Phase Deposition and so on. Great details have been reviewed by Shtein and coauthors. [19] The vaccum thermal evaporation method will be applied to deposit small moleculars in this thesis and will be disussed in detail. The schematic setup is shown in Figure 2.10. The small molecular materails are put in different kinds of boats, as shown in Figure 2.10 a, and the boat will be connected with two electrode on two ends. When the vaccum level reaches 10^{-6} to 10^{-7} Torr level, the boat will be heated up and so will be the materials by Joule effect. The materaisl will be deposited on to the substrate. And the thickness can be precisely controlled by the quartz crystals microbalance.

For the solution processed methods, including spin-coating, drop-casting, droplet-pinned crystallization and so on are widely reported. In this thesis, the

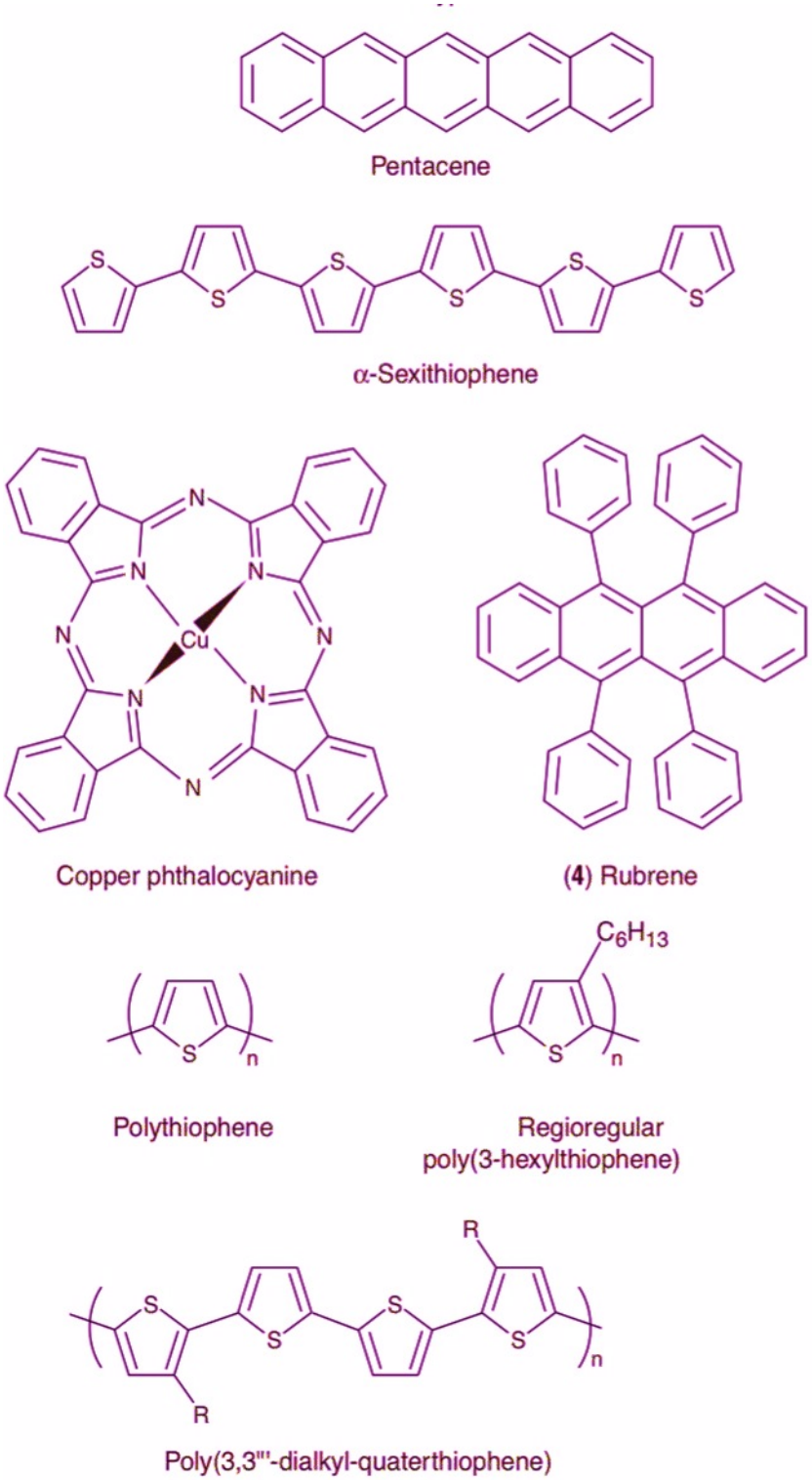

Figure 2.8 Widely reported p-type materials reviewed by Bao and co-authors [20]

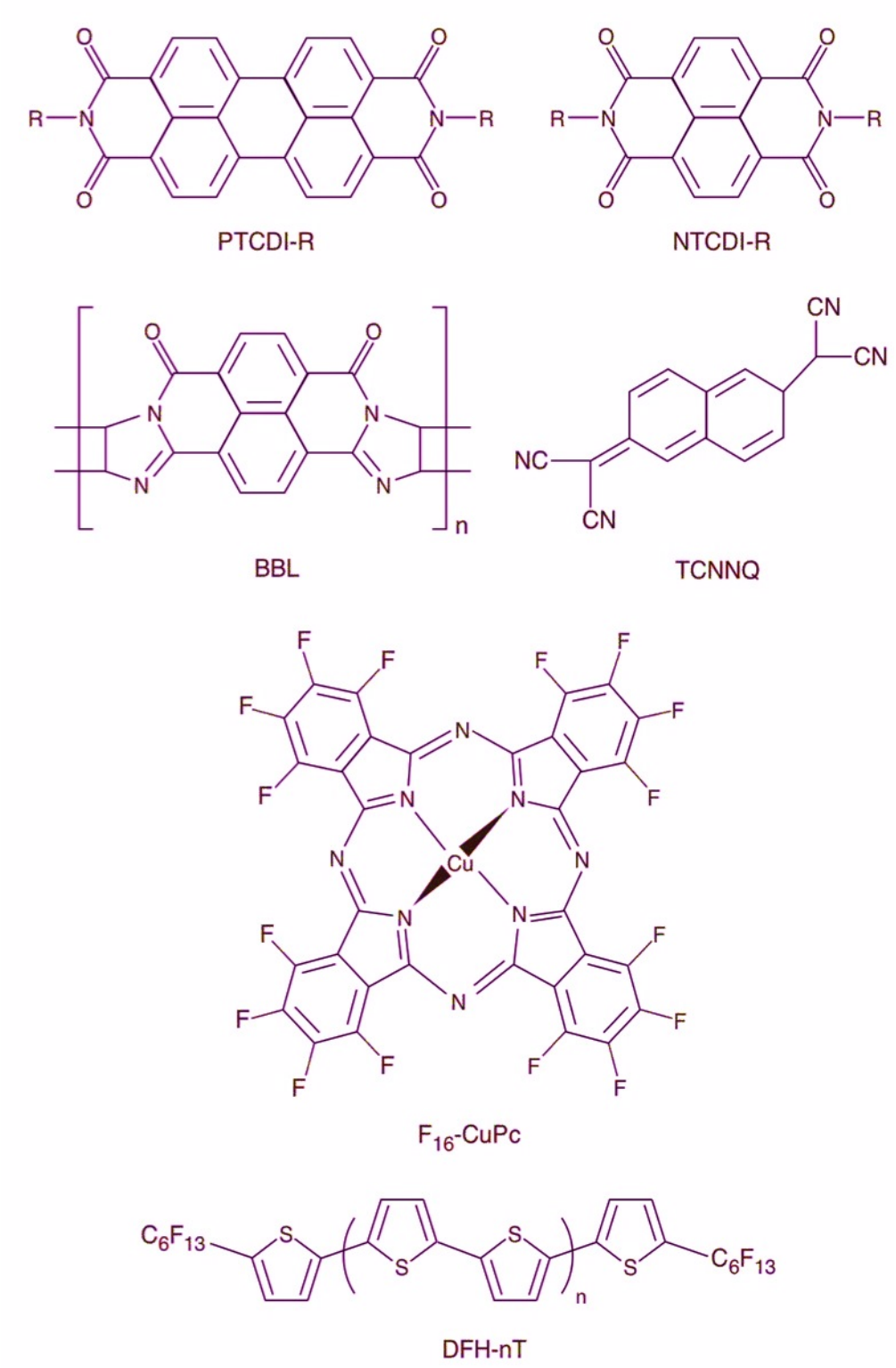

Figure 2.9 Widely reported n type materials reviewed by Bao and co-authors [20]

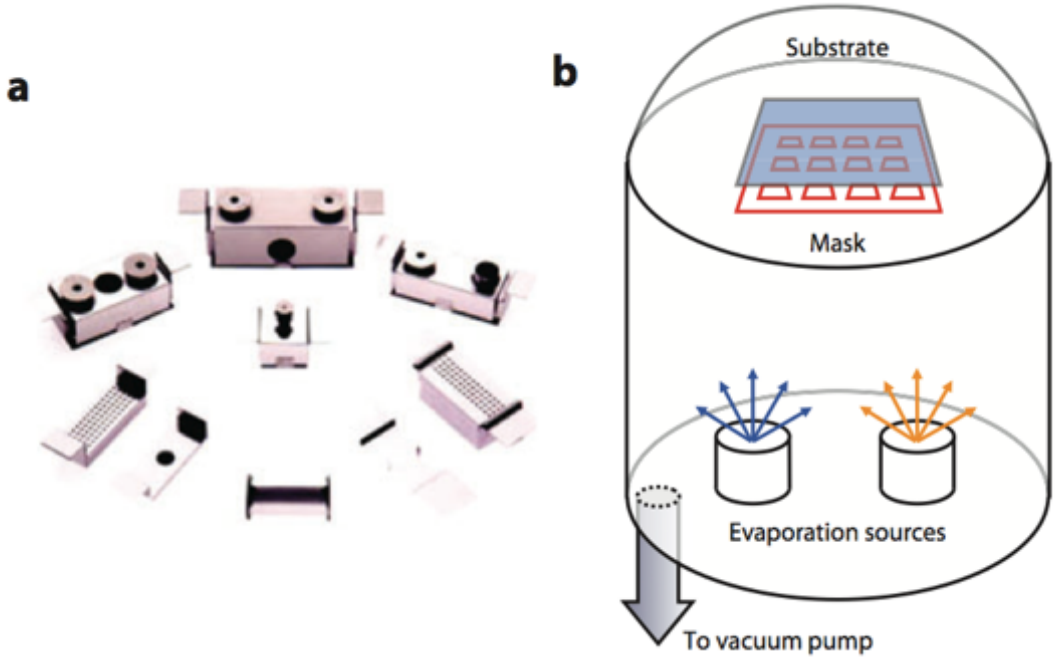

Figure 2.10 a. Different kinds fo boats to hold materials. b. Schematic of vacuum thermal evaporation.

DPC will be used to demonstrate the compatability of BST thin film with solution processing, then it will be introduced in detail. It was first proposed by Bao and coauthors, as shown in Figure 2.11. [21, 22] With a small pinner in the middle of the substrate, the solution drop is directly dropped on top of pinner and will the trapped around the pinner. During drying of the semiconductor solution, crystals nucleate near the contact line and grow along the receding direction (toward the center).

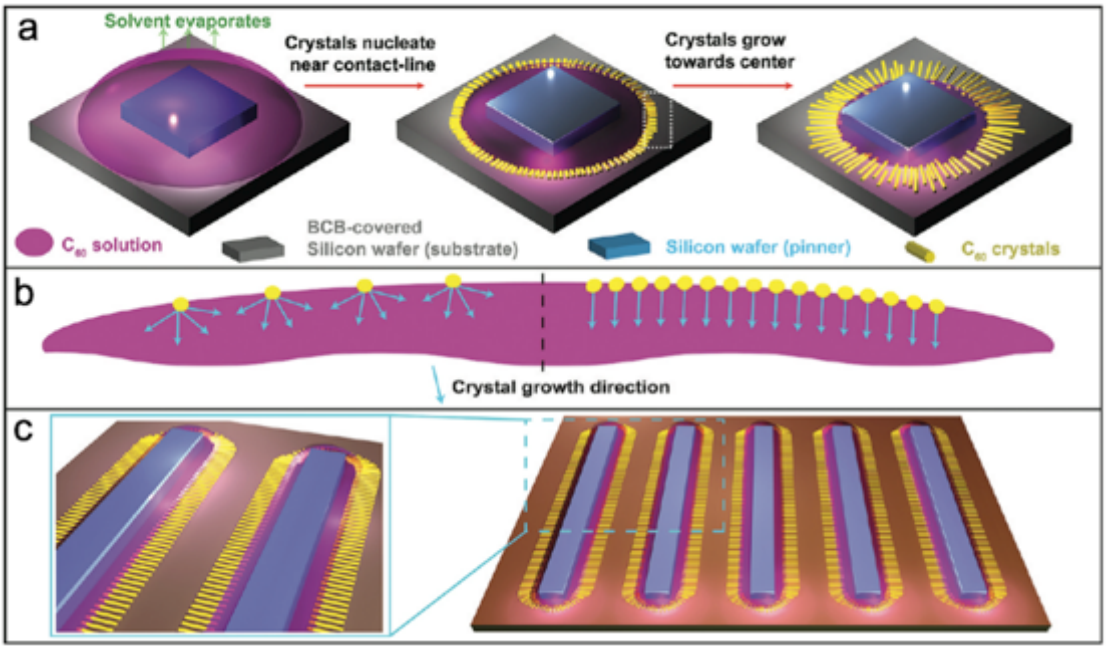

Figure 2.11 droplet-pinned crystallization method demostration with C_{60} solution with different shapes of pinner [22]

All the organic semiconductor materials that will be used in this thesis are shown in Figure 2.13. Pentacene is one typical material of acene, which is a class of small moleculers composed of linearly fused benzene rings, including anthracene, tetracene and so on. It is one of the most extensively studied organic semiconductor for OFETs application in the literature till now. [23-28] By tuning the surface property by SAMs, like OTS, the mobility can be as high as 3.0 $cm^2V^{-1}s^{-1}$, which is due to the almost perfect overlaping of frontier molecular orbitals within the molecules and herringbone packing of molecules. [29] However, pentacene is not stable in air due to the easy oxidization at the central benzene ring. [30]

Due to the high mobility, high stability in air and at high temperature, DNTT has attracted more attention recently [31-37]. Yamamoto and co-authors first reported DNTT showing the high mobility of 2.9$cm^2V^{-1}s^{-1}$ fabricated on SiO_2/Si substrate heated at 60°C and SiO_2 is modified by OTS.[32]Kuribara and co-authors reported mobility of 1.2$cm^2V^{-1}s^{-1}$ on AlO_x modified with n-tetradecylphosphonic acid (C_{14}-SAM). Ute Zschieschang etal.[36] have examined the stability of DNTT OFET after stored in air for 8 months and the mbility has just dropped around 50%, which has shown the great potentional in real application, as shown in Figure 2.12. Besides, in their later work [31], they report DNTT transistor connected with a blue OLED and showed the application potential of DNTT further.

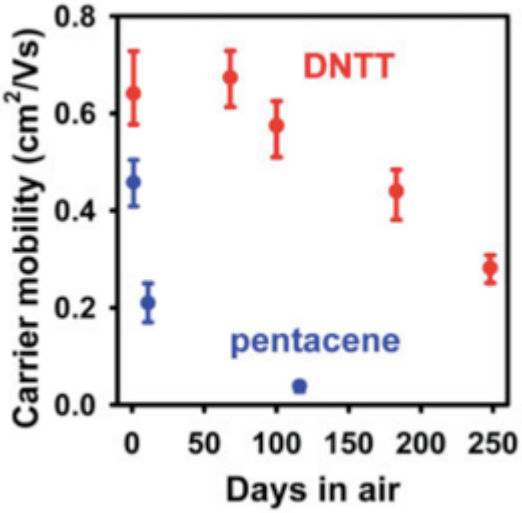

Figure 2.12 The comparasion of mobility change of OFET based on pentacene and DNTT

Pentacene and DNTT are choosen in this thesis for demonstration of the high-*k* dielectric applied for OFETs where the organic seminconductor on top is deposited by the thermal evaporation. To meets the needs in the market of low cost, the solution methods processed semiconductors, TIPS-pentacene and fulerene, are also discussed about. TIPS-pentacene is widly reported as solution processed small moleculerthe in organic semiconductor class. It has been shown that it will give dramatically varied performance for different growth methods. For drop casting, the mobility is 0.2 to 1.8 $cm^2\ V^{-1}s^{-1}$ (averaged 0.65 $cm^2\ V^{-1}s^{-1}$) . [38] For the dip-coated and spin-coated device, the mobilities range between

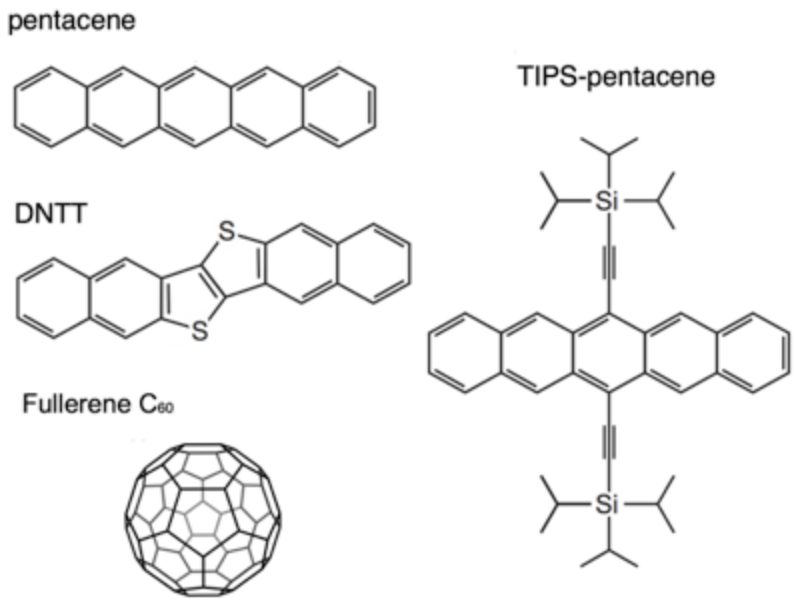

Figure 2.13 Pentacene and DNTT are for thermal evaporation OFETs. TIPS-pentacene and C_{60} are for solution processed OFETs.

0.01–0.6 $cm^2V^{-1}s^{-1}$ and 0.08–0.2 $cm^2V^{-1}s^{-1}$, respectively. [39] A lot higher mobility can be obtained by modifying the traditional drop-casting method by putting a small pinner on top of the surface where the TIPS-pentacene solution will be dropped on, ranging from 1.8 to 3.0$cm^2V^{-1}s^{-1}$. [21] The mobilities of the devices with strained film can further achieve 4.6$cm^2V^{-1}s^{-1}$[40] and 8.1$cm^2V^{-1}s^{-1}$ [41]. It has also been reported that, the angle between crystal growth direction and the carrier moving direction in the channel can give dramatically varied mobilities. [42] Usually, if the crystal alignment is parallel to the direction of the carries being transported in the channel, the highest mobility can be obtained. C_{60} has been reported that it can be deposited by different methods, like thermal evaporation and molecular beam deposition [43], which gives mobility on the order of $10^{-1}cm^2V^{-1}s^{-1}$. Recently, Li and coauthors reported one new method called DPC (one new developed solution processing method) with carbon tetrachloride(CCl_4) and m-xylene as co-solvents, which shows high mobility of 1.39-2.61 $cm^2V^{-1}s^{-1}$. [21]

In here, pentacene and DNTT are the organic semiconductors used in thermal evaporated OFETs, while TIPS-pentacene and C_{60} are employed for solution processed devices.

2.4 Gate dielectric and motivations for high-*k* ones

2.4.1 Interfaces properties of gate dielectric and effect on the figure-of-merits of OFETs

The gate dielectric is sanwiched between organic semiconductor and the gate electrode in OFETs. Then there are two important interfaces to be considered. The first one is the interface between gate dielectric and organic semiconductor. In most of the OFETs, the organic semiconductor layer is deposited on top of gate dielectric. In this case, the surface properties of the gate dielectric will determine the growth of the organic semiconductor on top, including (1) surface roughness, (2) surface charges and trap sites, (3)surface energy, (4)polarity.

(1) It has been reported that the surface roughness has strong effect on the mobility. Steudel and coauthers have reported that pentacene OFETs based on SiO_2 with roughness of 2.4Å, 11.5Å and 54Å show mobility of 0.49, 0.11 and 0.04$cm^2V^{-1}s^{-1}$, respectively. They attibuted this effect to the roughness (valleys), namely barrier, which hinder the transportation of charges. In other words, the hole trapped in the valleys in the direction perpendicular to the drain-source direction can not be moved out by the drain-source voltage. Besides, when the device is turned on, V_{GS} is also keeping the holes in the minima of the vallyes too. It shows that it is important to have smooth dielectric surface and the gate electrode below to gurantee the mobility.[44]

(2) Good control of surface charges or trap sites of the interface between gate dielectric and the semiconductor is equally important. Working as switch, consistence of V_{th} for switching on to off and off to on, which means no hysteresis in transfer curves in terms of electrical characterization. Then hysteresis is mainly due to the surface charges or trap sites that shift the V_{th}. Hystereses show different characterizations regarding different channels and traps type of the interface. Egginger and co-authors have publised a review discussing the hysteresis topic in detail. [45] To decrease or remove the surface traps, UV-Ozone has been proved to be a promising and simple solution. Guo and co-authors reported the decreased and higher mobility of pentaene OFET after UV-Ozone treatment. [46]

(3) Surface energy of gate dielectric is another very important factor to be considered. For the solution processing technologies, the surface energy determines whether the semiconductor can wet the surface of the gate dielectric and then get deposited and crystallized. For the wetting property of the solution on gate dielectric, wetting envelop is the mainly characterization that should be consided. For the physical deposition methods, surface energy of gate dielectric can also determins the crystalization mode of semiconductor by work of adhesion between the dielectric and the deposited semiconductor. For the solution processing methods, including spin-coating, drop-casting, spray coating and ink-jet printing, the wettability can be derived from work of adhesion between solution and the gate dielectric below is,

$$W_{sl}=\gamma_{lv}(\cos\theta + 1) \qquad \text{Equation 2.6}$$

The work of adhesion of the solution itself is,

$$W_{ll}=2\gamma_{lv} \qquad \text{Equation 2.7}$$

The difference between work of adhesion between solution and solid gate dielectric and solution itself can be obtained by doing subtraction between W_{sl} and W_{ll}.

$$W_{sl}-W_{ll}=\Delta W=\gamma_{lv}(\cos\theta-1) \qquad \text{Equation 2.8}$$

ΔW indicates the difference between the extent to which liquid adhere to the solid surface and the extent to which liquid adhere to itself. In other words, it shows the ability of a liquid drop to stick onto the solid surface during solution processing. [47]. From Equation 2.8, it can be seen that when $\theta=0$, $W_{sl}=W_{ll}$, which means the solution is equal to adhere to itself and the solid surface and the complete wetting will be observed. Besides, from the equation, it is clear that smaller contact angle gives better wettability.

Wetting envelop is plotting polar term of the surface tension versus the dispersion. The relationship of the polar term and dispersion term can be derived from different theory for different applications, like Wu (harmonic mean) method, Owens–Wendt–Kaelble method and so on. From the wetting envelop, it is easy to know whether the solution can completely wet the solid surface or not. If the surface energy components lie within the wetting envelope of contact angle of 0° should completely wet the

surface and form film by solution processing. When components lie below the contact angle of 40°, good wettability could still be expected.

Wöbkenberg and co-authors studied surface wettability of different semiconductor solutions on top of Al-AlO_x-n-octadecylphosphonic acid (ODPA), as shown in Figure 2.14. They studied the wetting property of different semicoductor solutions on top of Al-AlO_x-ODPA. F_{17}-DOPF, PCB-F_3 and PCB-F_6 show good wetting and film formation, whose surface energy lies blow plots for contact angle of 40^{o}C. But for those above, films can be hardly formed. They concluded that, for ODPA, semiconductor solutions whose dispersion term dominate are likely to wet well and form film well on the surface of ODPA.

For the physical depositon method, like thermal evaporation, vapor-jeting, instead of wetting envelope, work of adhesion between the semiconductor and the gate dielectric is the parameter determining the morphlogy and crystallization of the semiconductor. The work of adhesion between gate and semiconductor can be described by:

$$W_{gs}=\gamma_g+\gamma_s-\gamma_i \qquad \text{Equation 2.9}$$

where γ_g is the surface energy of the gate dielectric, γ_s is the surface energy of the semiconductor, and γ_i is the interfacial free energy.[48]

$$\gamma_s+\gamma_i \leq \gamma_g \qquad \text{Equation 2.10}$$

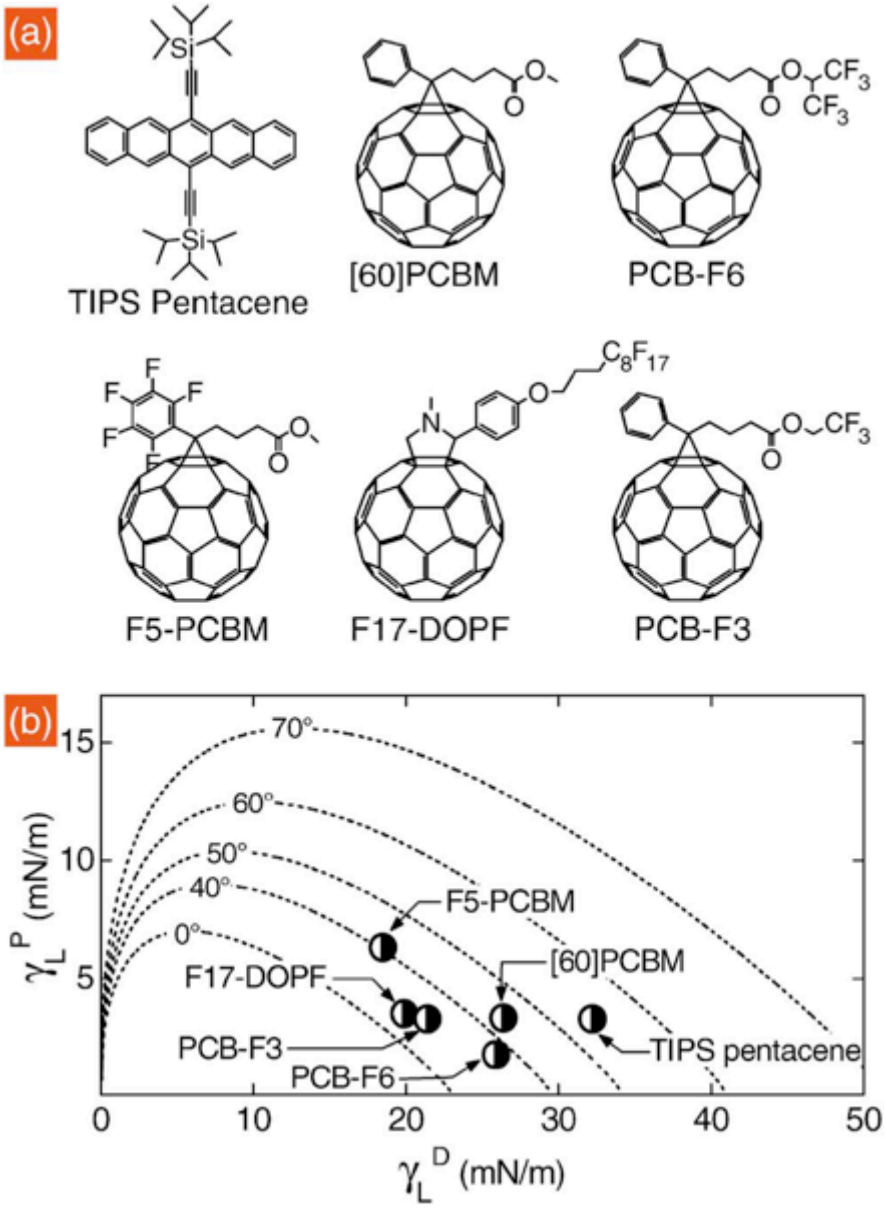

Figure 2.14 (a) Structures of different organic semiconductor studied. (b) Wetting envelopes for Al-AlO_x-ODPA surface with surface energy components of semiconductor solutions shown in plot as symbols[47]

$$\gamma_s+\gamma_i > \gamma_g \qquad \text{Equation 2.11}$$

If the surface energy of gate dielectric and semiconductor show the relationship of Equation 2.10, then the semiconductor on top will crystallize in Frank–van der Merwe mode (F-M mode), namely layer-by-layer growth mode. If Equation 2.11 is the case, then the semiconductor will form in Volmer–Weber growth mode (V-W mode), namely 3D island growth mode.

Add γ_s and two sides of the Equation 2.10 and 2.11 and transform them to work of adhesion form like shown in Equation 2.9. Then the relashionship between work of adhesion and two times of surface energy of semiconductor. If $W_{gs}>2\gamma_s$, the thin film will grow in F-M mode, If $W_{gs}<2\gamma_s$, the thin film will grow in V-W mode. When W_{gs} is close to $2\gamma_s$, there is another different growth mode, which is Stranski–Krastanov (S-K) growth mode, namely layer and island mode.

(4) The dielectric constant is the measurement of the polarizability of a material in response to electric field. [49] The polarizability resulting from the reorganization of charge, including interfacial or space charge, ionic, dipolar, and electronic four different motions, as shown in Figure 2.15. [50, 51] For different materials, different timescales of four different motions result in the frequency dependence of the corresponsing main contribution to the dielectric constant. In the case of electronic motion, the frequency is up to 10^{16} Hz. For materials in organic field effect transistor applications, ionic and electronic motion will mainly be the contribution to the

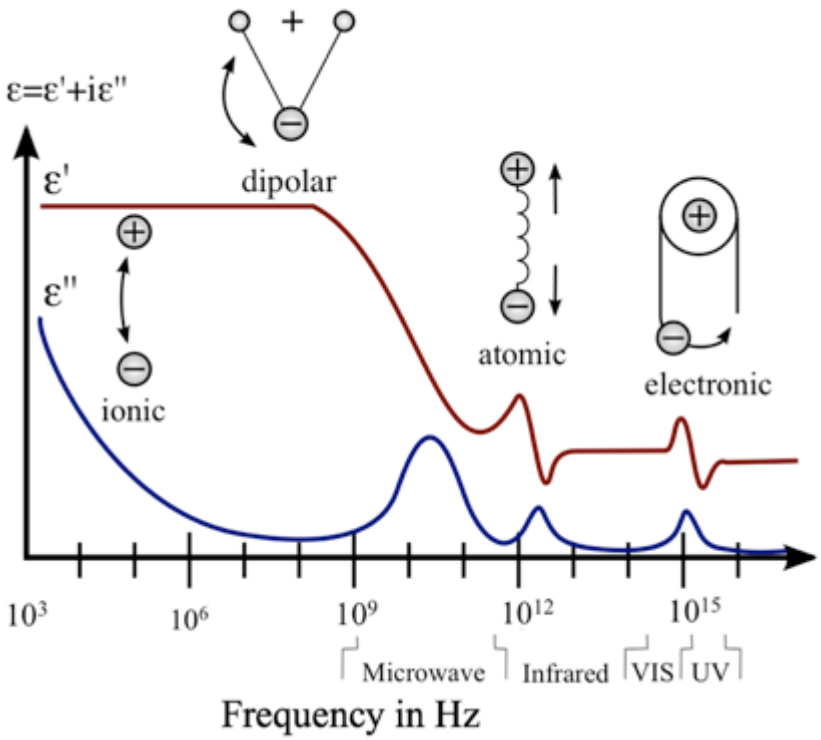

Figure 2.15 Depencence of dielectric constant on the frequency

dielectric constant. It has been reported that polarity of the dielectric surface will affect field effect mobility of the organic semiconductor on top by broadening the density of states. [11, 52] However, it was found out that this phenomenon is only obvious in organic materials, like polymer dielectric, due to their limited electronic band.

Another important interface will be the dielectric and gate electrode, where the issue of static charges or dynamic charges injection should be considered. These charges will adversely affect the V_{th}. Besides, the function of time. Furthermore, complete coverage of gate dielectric on top of the gate electrode is critical to prevent the leakage current.

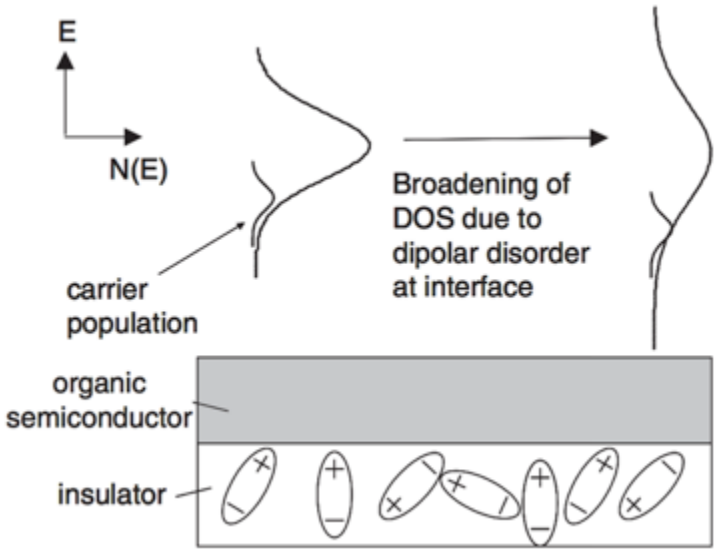

Figure 2.16 Mechanism of the broadening of density of states of organic semiconductor [52]

2.4.2 Motivations for high dielectric constant (high-*k*) materials to replace SiO_2

Considering all the important factors of gate dielectric, SiO_2 grown by thermal oxidization has been a well developed materials and widely used in both industry field and scientific research. However, with the new needs in the market and in new generation of products, SiO_2 is facing bottleneck. For example, Samsung has officially launched flexible OLED displays, which is called YOUM displays. The key point of YOUM panels is that they are bendable [53]. And OFETs are known to be responsible for the switch the OLED devices. Similar with displays based on OLEDs, wearable

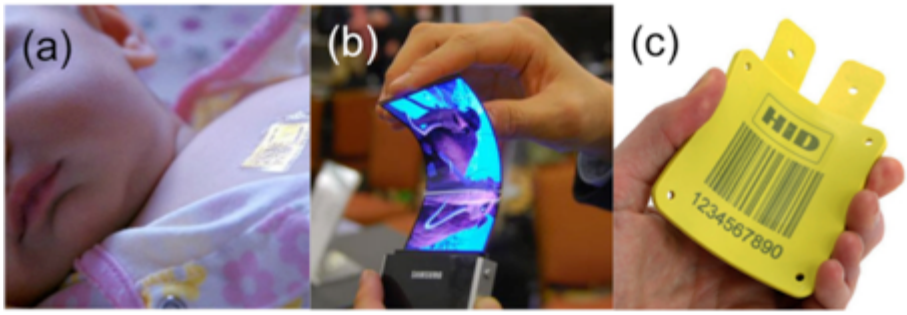

Figure 2.17 (a) mc10 sensor used to monitor the baby (b) Flexible LG smartphone (c) flexible RFID.

electronics, RFID and many other portable new generation electronic devices, as shwon in Figure 2.17. Another example is the wearable pressure sensor used for pulse monitoring reported by Bao and coauthors, as shown in Figure 2.18. However, the operatig power of the driving transistor is as high as 200V with low-*k* dielectric material PDMS, as shown in Figure 2.19, which is quite dangerous for the human body monitoring. [54] The applications mentioned above all require low small voltage so that they can be drived by battery and become portable and wearable.

According to Equations 2.1 and 2.2, a clear approach to substantially increasing the drain current while operating at lower biases is to increase the capacitance of the dielectric. As the *C'* is given Equation 2.12 as follows,

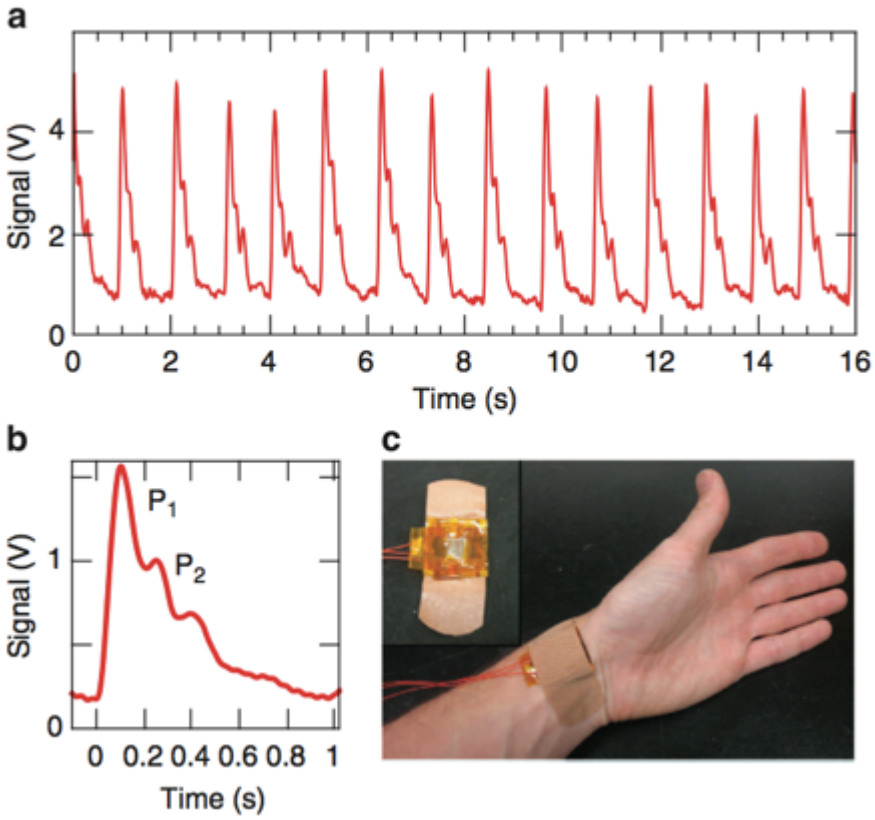

Figure 2.18 Pulse wave test of the radial artery with the pressure sensor based on organic field effect transistors.[54]

$$C' = \frac{\varepsilon\varepsilon_0}{t} \qquad \text{Equation 2.12}$$

where C' is capacitance per unit area, ε_0 is the permittivity of vacuum, ε and t are the dielectric constant and thickness of the gate dielectric material, respectively. Higher capacitance can be obtained either by decreasing the thickness of the traditionally used

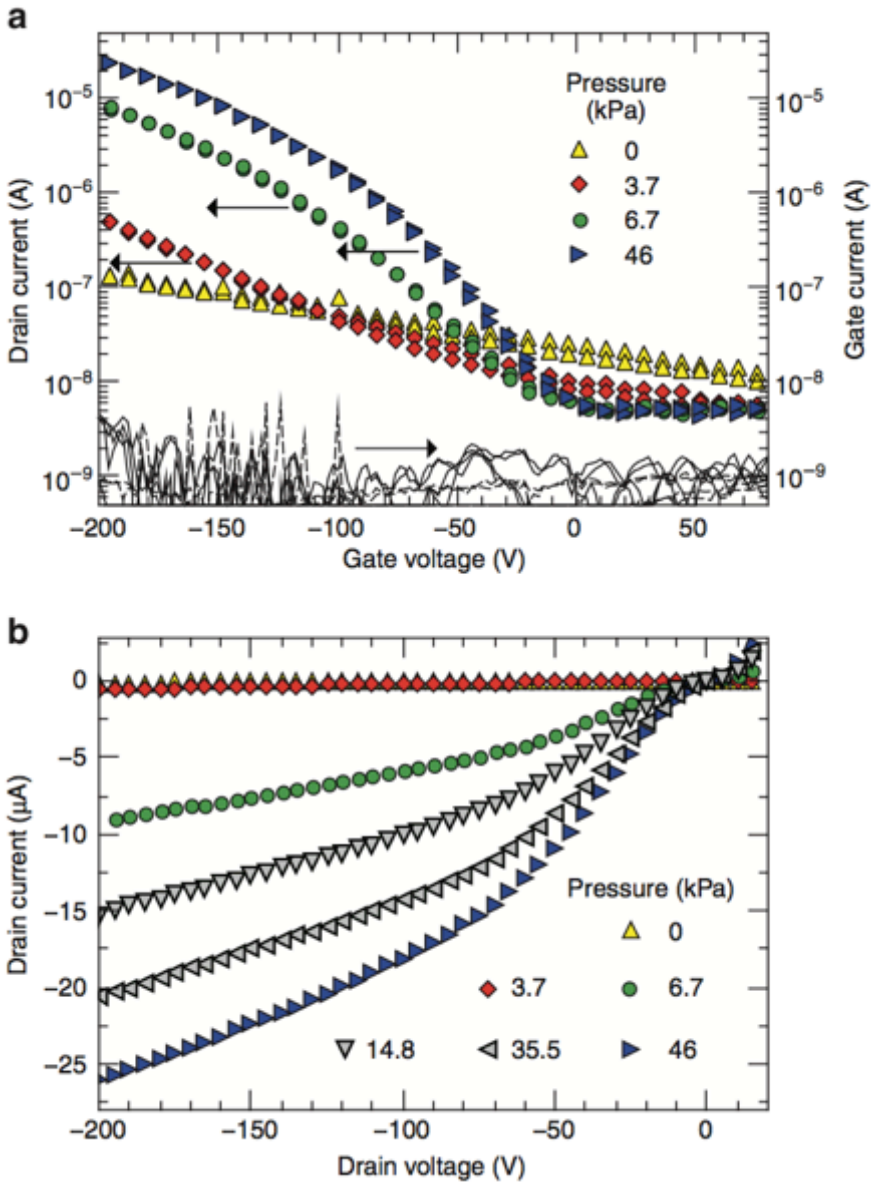

Figure 2.19 The electrical performance of pressure sensitive transistor[54]

low-*k* gate dielectric SiO_2 or replacing SiO_2 with high-*k* gate dielectric materials. In fact, the continuous drive to increase integrated circuit performance through shrinkage of the circuit elements requires the Si transistor dimensions to be scaled down according to the well-known Moore's law[55], which predicts that the number of transistor on an integrated circuit increases exponentially, doubling over a 2–3 year

period, as depicted in Figure 2.20. Thus the minimum feature size in a transistor decreases exponentially each year. For the most widely used gate dielectric materials SiO_2, the capacitance can be increased indeed by decreasing the thickness. However, the thickness of the SiO_2 layer presently used as the gate dielectric is now so thin (under 1.4 nm) that the gate leakage current due to direct tunneling of electrons

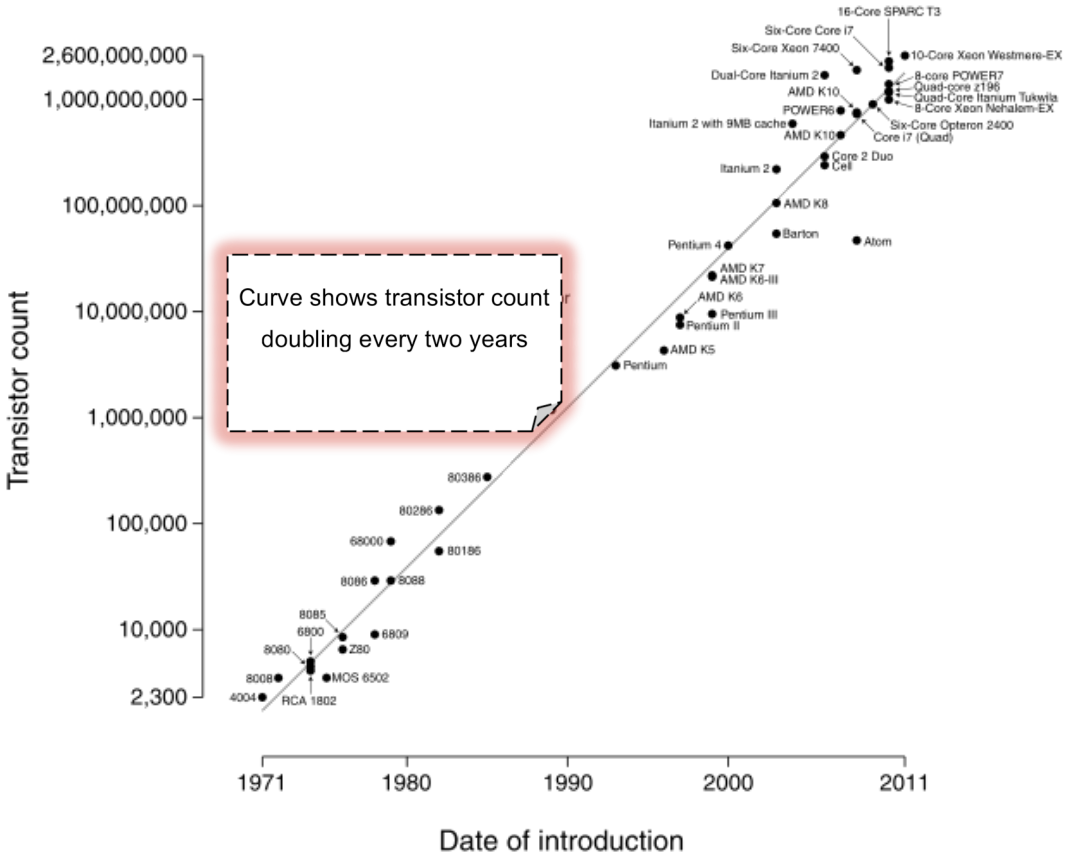

Figure 2.20 Microprocessor transistor counts 1971-2011

through the SiO_2 becomes too high, which exceeds $1Acm^{-2}$ at 1V, so that power dissipation increases to unacceptable values, like shown in Figure 2.21. In addition, it becomes increasingly difficult to make and measure accurately such thin films. Finally, the reliability of SiO_2 films against electrical breakdown declines in thin films. In thissense, SiO_2 has reached its scaling limit [11]. These reasons lead to a desire to replace SiO_2 with high-*k* materials instead of just decreasing the thickness of it.

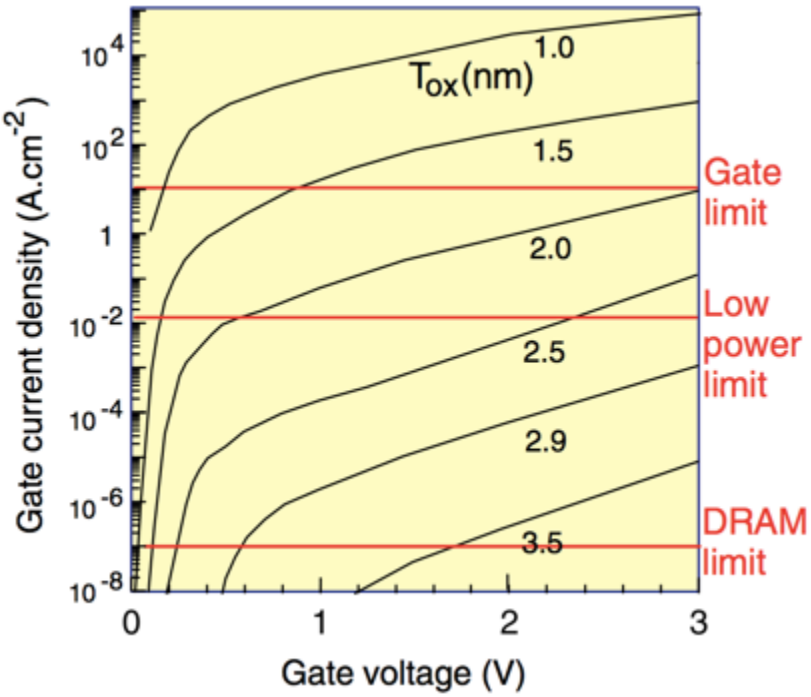

Figure 2.21 Leakage current versus voltage for various thickness of SiO_2 layers [56]

2.4.3 Previous research of high-*k* dielectric materials

Compared with widely used SiO_2, high-*k* dielectric materials, which can be not only physically thicker and at the same time gives higher capacitance, but also decrease the tunneling current. Different high-*k* dielectrics fabricated by different technologies have been reported, mainly including inorganic high-*k* materials, high-*k* polymers and ultrathin inorganic with SAMs.

OFETs with aluminum oxide (Al_2O_3)[57] $Ba_{0.6}Ti_{0.4}O_3$[58] and $Ba_{0.7}Ti_{0.3}O_3$ [58] by sol-gel method, Al_2O_3 by atomic layer deposition(ALD)[59], and hafnium oxide (HfO_2) grown by ALD, [60, 61] barium zirconate titanate (BZT) by magnetron sputtering method, have shown low operating voltages at around or even lower than 3V. [62] Yet, the high processing and annealing temperature for inorganic dielectric may limit their applications on flexible substrates with low glass transition temperatures.

Relatively high annealing temperatures of the commonly used high-*k* polymer materials, such as poly(vinylidenefluoride-co-trifluoroethylene) (P(VDF−TrFE)) (160^{o}C)-polyvinyl phenol (PVP) (175^{o}C), [63] PVPy (100^{o}C)[64] and PVP mixed with poly (melamine-co-formaldehyde) methylated (200^{o}C)[65] would limit their applications on paper-based or low glass transition temperature flexible substrates. [63, 65] 62] Furthermore, as the areal capacitance and surface morphology of the polymers dielectric are usually sensitive to moisture content, [64] this limits their applications in biological systems such as human skin. [66]

Ultrathin metal oxide dielectric thin film combined with SAMs is an effective solution for reducing the dielectric thickness and leakage current. [67] In the SAMs, the head groups are specially designed for attaching onto particular gate dielectric insulator or gate electrodes by chemical bonding, while the terminating groups on the other hand control the growth morphology and the packing of the organic semiconductors (OSC). As the packing of the organic semiconductor affects the leakage current of the OFETs, the terminating group hence also affects the leakage current. For example, the leakage current of pentacene transistor with acene group as the terminating group shows 100 times decreases while comparing with the aromatic group. [68] However, as the head and terminating groups of the SAMS may only work for particular gate electrodes, dielectric insulators and organic semiconductors, different SAMs are required for various transistors and furthermore, it is also difficult to apply SAMs in the OFETS with the top gate electrode configurations.

For clear comparance, Table 2.1 summarized different methods for fabrication of different high-*k* dielectric materials for low operation voltage OFETs. Several parameters are shown in the table for comparance, including processing environment, temperature and the substrates that are used for OFET devices fabrication. For both physical and solution processing methods for different high-*k* dielectric materials, usually higher temperature and special atomsphere are needed, which will limit the application of OFET on some flexible substrate with low glass temperature or some

fragile substrates calling for low cost. Then noveal methods and high-*k* dielectric materials processed at low temperature under no special atmosphere are needed.

Table 2.1 Summary of different methods for fabricating low voltage OFETs

Methods		Materials	Environment	Temperature (^{o}C)	Substrate
Physical methods	Atomic layer deposition	Al_2O_3[69]	N_2 or Ar	100	ITO glass
		HfO_2[61]	H_2O vapor	200	n+ silicon
		HfO_2+BCB[70]	Vapor for HfO_2 N_2 for BCB	200 for HfO_2 250 for BCB	n+ silicon
	RF magnetron sputtering	BZT[62]	Ar/O_2	RT	PC
	Sol-gel+heat treatment	HfO_x[71]	NA	600	n+ silicon
	Sol-gel+heat treatment Chemical solution	BTO[72]	Air	180	glass
Solution methods	Sol-gel+heat treatment Chemical solution Sol-gel+UV-Ozone	BST[73]	O_2	400	Pt/Ti/SiO_2/Si
		ZrO_x[74]	Air	RT	n+ silicon
	Spin-coating	P(VDF-TrFE-CFE)[28]	N_2	60	PET
	Spin-coating	P(VDF–TrFE)+PVP[63]	Air for P(VDF-TrFE) Vacuum for PVP	RT for P(VDF-TrFE) 175 for PVP	PES

2.5 Summary

This chapter introduced the basic concepts and working mechanisam of OFET devices. The focus was on gate dielectric part and many factors that affect the performance of OFET devices have been discussed. At last, the motivations for high-*k* materials are discussed in detailed and the current solution are reviewed. However, there are still some problems with the current solutions, like relatively high processing temperature of inorganic high-*k* dielectrics, vulnerability of polymer one in air or in high relative humidity environment and the limitation of SAMs.

Chapter 3. OFETs with $Ba_{0.7}Sr_{0.3}TiO_3$ (BST) thin film derived by pulsed laser deposition

High substrate temperature PLD is usually applied for growing crystalline BST with high dielectric constant (ε_r>200) and under low oxygen pressure environment. [75] Due to the ferroelectric properties of the crystalline BST films, they can be used as tunable capacitors, [76] optical modulator [77] or microwave circuit components. [78] However, as the crystal grains and the boundaries hinder the growth of the organic semiconductors, it is difficult to apply crystallined BST as the OFET dielectric insulators. Besides, as shown in Table 2.1, most of the physical methods used to deposit high-*k* dielectric materials, relatively high temperature and special atmosphere are adapted. To overcome the morphology induced problems by the crystallined BST and reduce the temperature as well as cost, amorphous BST fabricated by PLD technology at low temperature without any special atmosphere and it works well as gate dielectric in OFET.

3.1 PLD setup

Figure 3.1 shows the picture of the PLD equipment. Figure 3.2 shows the schematic drawing of the PLD setup. The PLD deposition of the BST is performed under pressure of 2×10^{-3} Pa while the substrate holder kept at constant temperature of 110^{o}C during the deposition process. And the subtrate holder keeps rotating during the deposition. Low pressure environment is for preventing the oxidization of the hydrofluoric acid treated silicon substrates (University wafers). The 248 nm KrF excimer laser with a repetition frequency of 10Hz, pulse width of 10-50ns and the corresponding energy per pulse of 250mJ is used as the source. Laser pulses are guided and focused by a series of lenses through a glass window of the chamber wall onto the target. In order to achieve high photon absorption by the oxide target, UV wavelengths are used. The distance between the target and the substrate holder is maintained at 5cm. There are many parameters that in the PLD setup to design materials, like laser frequency, substrate temperature, distance between target and substrate, atmosphere inside the deposition chamber (like O_2).

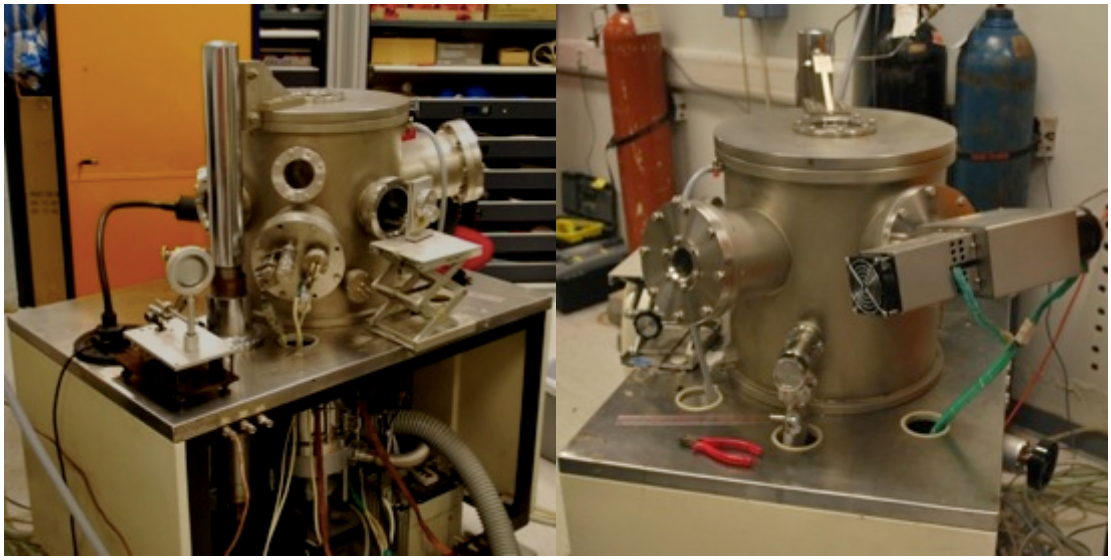

Figure 3.1 The photo of PLD equipment

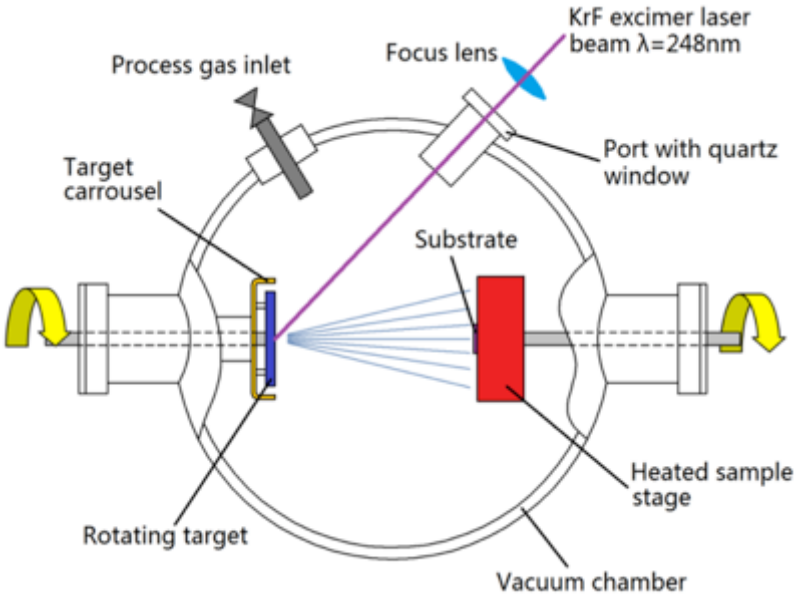

Figure 3.2 The work mechanism diagram of PLD

3.2 Characterizations

3.2.1 BST thin film characterizations

The surface roughness of the BST thin film deposited on various substrate and the surface morphology of pentacene deposited on top of BST are characterized by AFM (Digital Instrument, NanoScope VIII). The surface morphology of BST is characterized by Hitachi S-4800 FEG Scanning Electron Microscope (SEM). And the thickness of BST thin films on both Si and PEN substrates are measured by cross-sectional SEM. The crystallization properties of BST as well as pentacene are characterized by the X-ray diffraction (XRD) (Rigaku Smartlab 9KW). High resolution TEM (Philips Tecnai G220 S-TWIN) is used to study the cross sectional image of the interface between the BST and Si substrate. The capacitance versus frequency (C-F) and capacitance versus direct voltage (C-V) measurements are characterized with impedance analyzer Aglient 4294. The output and double-sweep transfer characteristics of the transistors are measured by two Keithley 2400 sourcemeters.

Figure 3.3 is tapping mode AFM 3-dimensional (3-D) roughness image of BST thin film deposited by PLD at 110^{o}C. The roughness is around 0.11nm. Figure 3.4 is the corresponding SEM images for BST thin film surface. From Figure 3.3 and Figure 3.4, it can be clearly seen that, the surface of the BST thin film is extremely smooth without any obvious particles or grains on the surface. BST thin film is deposited at 110^{o}C, which is far from the crystallization temperature. Both XRD and TEM are used

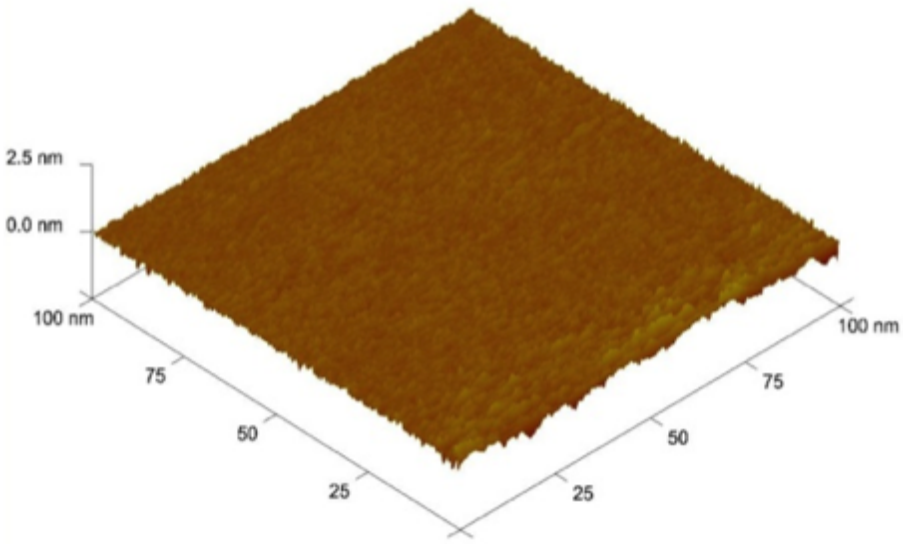

Figure 3.3 Tapping mode AFM 3-D roughness image of BST thin film

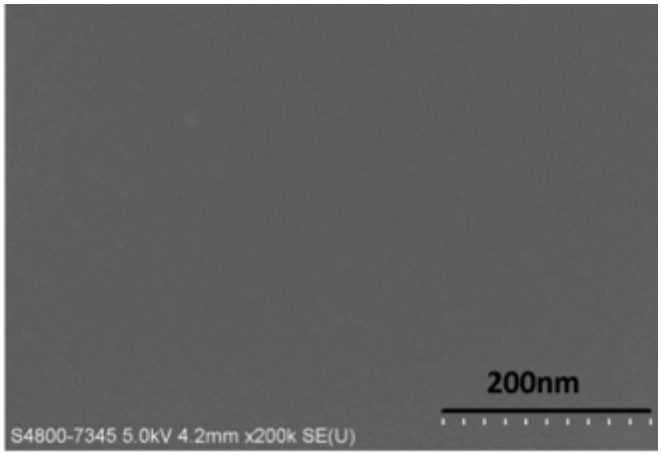

Figure 3.4 SEM images of BST thin film surface

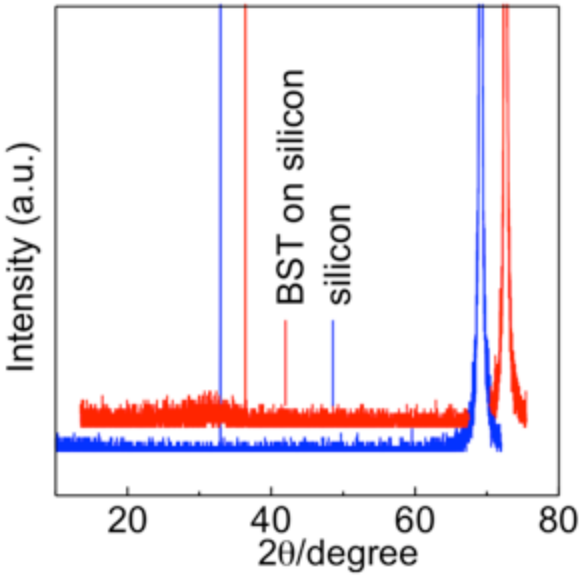

Figure 3.5 XRD pattern of BST thin film on silicon substrate and the silicon substrate.

to confirm the crystallinity of BST thin film. Figure 3.5 shows the XRD diffraction pattern for both silicon substrate and BST thin film on the same substrate. For the curves for just Si substrate, the (002) and (004) diffraction peaks appear. From the curve for BST thin film on silicon, except for very broad peak (halo), no extra diffraction peak appears compared with diffraction pattern for silicon substrate. The halo is for the amorphous phase of BST thin film.

Figure 3.6 (a) shows the TEM cross sectional of BST film deposited on HF etched Silicon substrate. The smooth surface can also be confirmed from this sectional view. (b) is high resolution TEM cross sectional image of the BST thin film as well as the silicon substrate. From the contrast of the strucute with the silicon lattice structure,

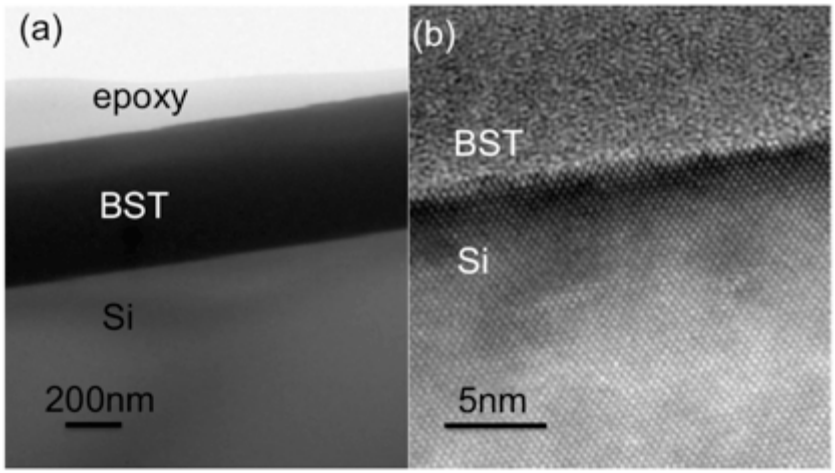

Figure 3.6 TEM cross sectional image of the same BST thin film deposited on silicon substrate as in Figure 3.4

it can be concluded that the BST thin film is amorphous without any crystallized grains in it. Actually, the thin films could not crystallize at such low temperature as 110°C.Just due to the amorphous nature, there are no crystal grains existing in the thin film which contributes to the extremely small surface roughness and smooth surface, as shown in Figure 3.3 and Figure 3.4.

Figure 3.7 is the dielectric properties of the BST thin films. The C-F measurements under the metal-insulator-metal (MIM) structure, in which 600μm diameter circular Ag top contacts are thermal evaporated onto the BST thin film through mechanical shadow masks on the n++Si substrate. As shown in the figure, the areal capacitances of the

thinner (96nm) and thicker (770nm) BST films studied in our experiment maintain at relative constant values in the high frequency regime from 10 K Hz to 1 M Hz. However, in the low frequency regime, the capacitance of the 96nm film increases from 180nFcm^{-2} at 1000 Hz to 261nFcm^{-2} at 40 Hz. The increase of capacitance at at lower frequency regime of the 770nm BST film is more significant and the capacitance increases from 46nFcm^{-2} at 1000Hz to 114nFcm^{-2} at 40Hz. The increase of capacitance at low frequency is attributed to the Maxwell–Wagner relaxations where the interface traps linked to the oxygen vacancies in the film, and similar frequency dependence on capacitance have been reported in zirconia (ZrO_2) film and titanium tantalum oxide

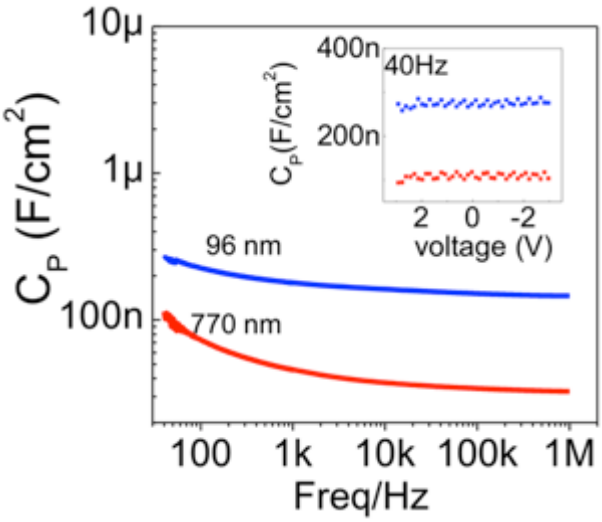

Figure 3.7 Cp versus frequency of BST thin film with different thickness of 96 nm and 770nm, respectively. And the inset is the corresponding Cp-Voltage plots for the corresponding BST thin film with same colar for the same film

(TiTaO) film by Mclntyre *et al* and Bartaudn *et al.*, respectively. [79, 80] Furthermore, the thicker amorphous BST film also contributes more internal defects and oxygen deficiencies, which would cause stronger space-charge polarization in the film and increase the capacitance at low frequency. [81] The inset is the capacitance versus voltage curve measured at 40Hz for the two different thickness thin BST thin films. With the electric voltage applied on gate electrode sweeping from -2.5V to 2.5V, the capacitance of the two thin films maintain constant almost, which can guarantees the stable performance of transistor and suggests that interface traps are not dominating in our samples. Besides, it is interesting to notice that the capacitance decrease of the films is not proportional to the film thickness, as shown in Figure 3.7 and Figure 3.8(a), which suggests varying combination in thicker films and dead layer effect may exist in the films. [82] The dielectric constant for different thickness of BST is calculated and shown in Figure 3.8(b), which confirms the dead layer existence and the effect on the dielectric constant of BST thin films.

Hwang and coauthers has used the Equation 3.1 shown below to confirm and study the dead layer effect of 400 and 480^{o}C deposited BST thin films. [82] They came to the conclusion that higher deposition temperature result in larger dielectric constant due to the better crystallinity and the smaller dead layer effect. Their conclusion explains our experimental result very well, including the dielectric constant is a lot lower than high

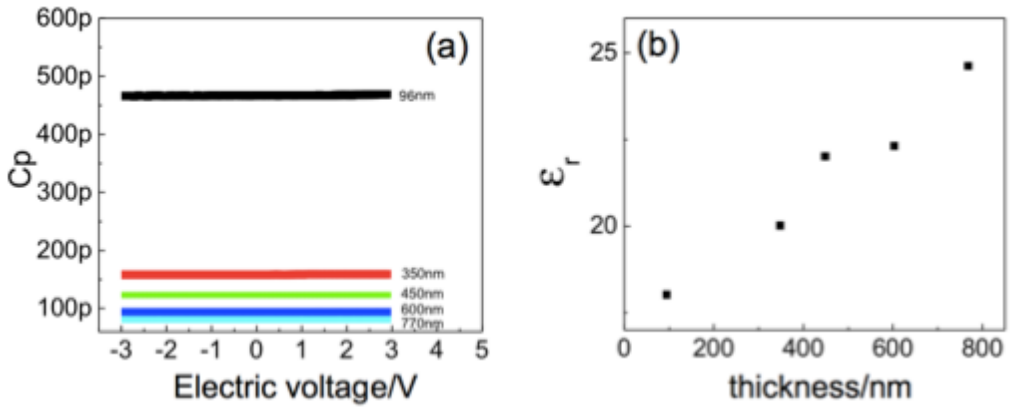

Figure 3.8(a) Measured capacitance versus direct voltage for BST thin films of different thickness. (b) Dielectric constant versus BST film thickness for the series of 5 different thickness

temperature deposited ones and dielectric constant becomes larger for thicker BST film. With Equation 3.1, the dead layer effect in BST thin films in this thesis is studied.

$$\frac{d_m}{\varepsilon_m} = \frac{d_b - d_i}{\varepsilon_b} + \frac{d_i}{\varepsilon_i} = \frac{d_b}{\varepsilon_b} + \frac{d_i}{\varepsilon_i} \qquad \text{Equation 3.1}$$

where, d stands for thickness, the subscript m is for measured ones, b for bulk, i for dead layer by assuming d_b is a lot larger than d_i. The calculated numbers for d_m / ε_m versus d_b of different BST thin films is ploted in Figure 3.9. Accoring to Equation 3.1, we can derive the dielectric constant of the bulk BST thin film, which is the reciprocal of the slope of the fitting line and the intercept d_i / ε_i is the term of the dead layer. From the fitting result as shown in Figure 3.9, the dielectric constant is around 25.8 and the d_i / ε_i is 2.7.

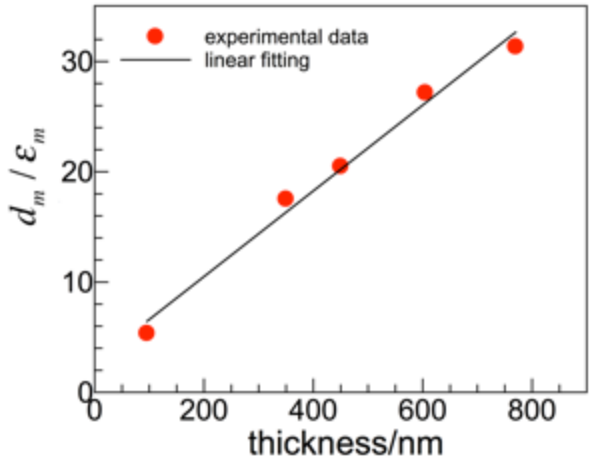

Figure 3.9 Depedence of d_m / ε_m on BST thin film thickness

3.2.2 The OFETs performance based on the BST thin films derived by PLD

Figure 3.10 (a) shows the schematic of OFET fabricated on BST thin film. (b) shows the schematic of the cross section of the whole device. (c) and (d) are output and transfer curves of the OFET with different BST thickness of 96nm and 770nm, respectively. The characteristic curves show pinch off and current saturation in these OFETs. In contrast to some of the solution processing which may generate unsatisfied chemical bonds and causes trap states between the dielectric and semiconductor interface, we do not observe significant hysteresis effect in our devices due to the

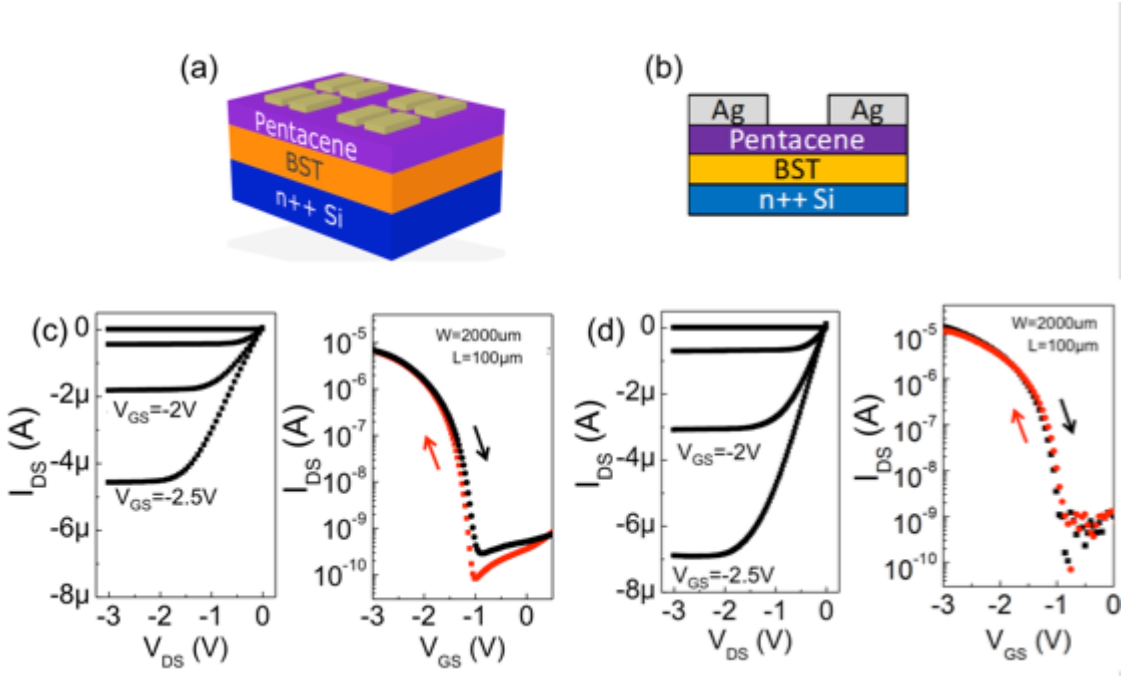

Figure 3.10 The output and transfer curves for OFET based on BST thin films with different thickness, (a) the schematic structure of OFET based on BST thin film. (b) Schematic of cross-sectinal of OFET device. (c) Out and transfer curves of OFET on 96nm BST. (d) Out and transfer curves of OFET on 770 nm BST.

interface traps. By using the low frequency areal capacitances obtained from extrapolation at low frequency around 0 Hz in Figure 3.7 are 0.53 $cm^2V^{-1}s^{-1}$ and 1.24 $cm^2V^{-1}s^{-1}$ for the transistor based on 96nm and 770nm thick BST film, respectively. The mobilities and other characteristic parameters including V_{th}, SS and on/off ratio of the petancene OFETs with different BST thin film in thicknesses on silicon substrate are listed in Table 3.1. Unlike the multilayer silica dielectric where the mobility decreases significantly while the areal capacitance increases due to the broadening of

Table 3.1 The different performance of OFETs based on different thickness of BST thin film

Thickness(nm)	Mobility($cm^2 V^{-1}s^{-1}$)	On/off	V_{th} (V)	SS(mv/decade)
96	0.53	4.88×10^4	-1.14	107
185	0.68	8.13×10^4	-1.18	100
500	0.95	7.45×10^4	-1.16	96.6
770	1.24	1.30×10^4	-1.11	160

the hole trap states under high polarizability[83], the mobilities of the current BST devices do not show significant variation while the capacitance increases which suggests most of the extra charge traps are located inside the dielectric rather than the dielectric/semiconductor interface. A possible explanation for the mobility drop in the thinner BST film is the larger roughness of the thinner BST thin film, which hinters the mobility of the induced carriers. [52] These values are highly comparable with other high-*k* metal oxides fabricated on silicon substrate by solution processing, atomic layer deposition or magnetron sputtering. [62, 65, 69] To confirm the origin of the mobility increase with thicker BST film. A series of BST thin films with increasing thicknesses were deposited. 2-D AFM for roughness and SEM for thickness for four BST thin films with different thickness are shown in Figure 3.11, Figure 3.12, Figure 3.13 and Figure 3.14. The roughnesses of different BST thin films are shown in Table 3.2. A

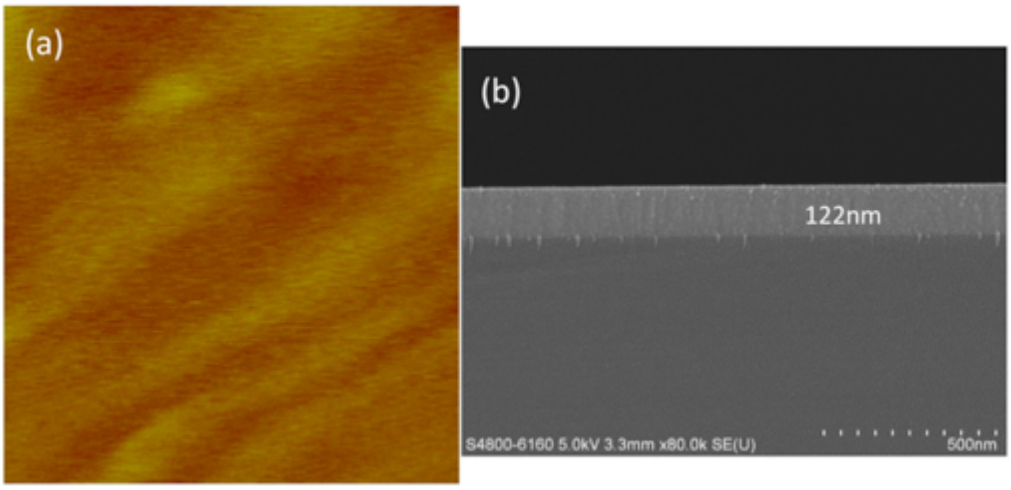

Figure 3.11 (a) 2-D AFM of BST thin film of 122nm in thickness; (b) Cross-sectional SEM of BST thin film of 122nm in thickness.

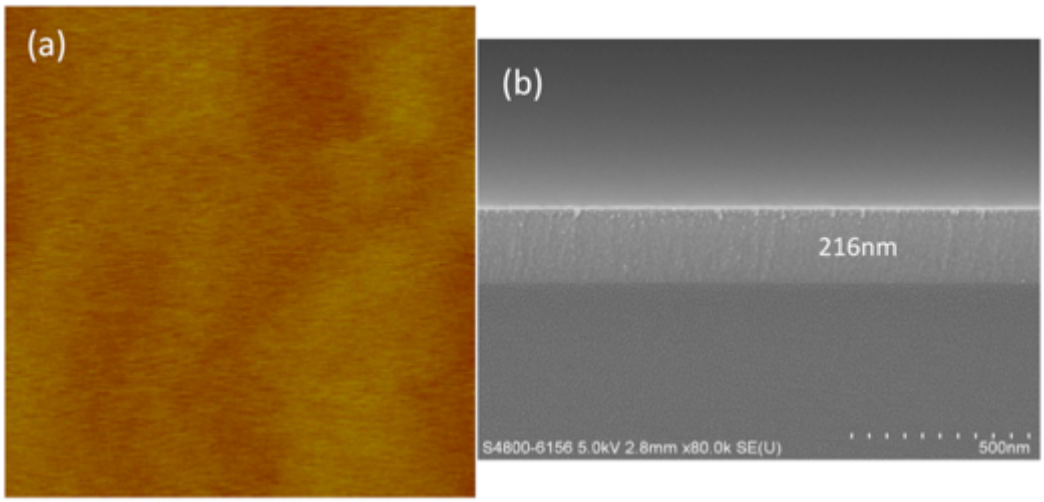

Figure 3.12 (a) 2-D AFM of BST thin film of 216nm in thickness; (b) Cross-sectional SEM of BST thin film of 216nm in thickness.

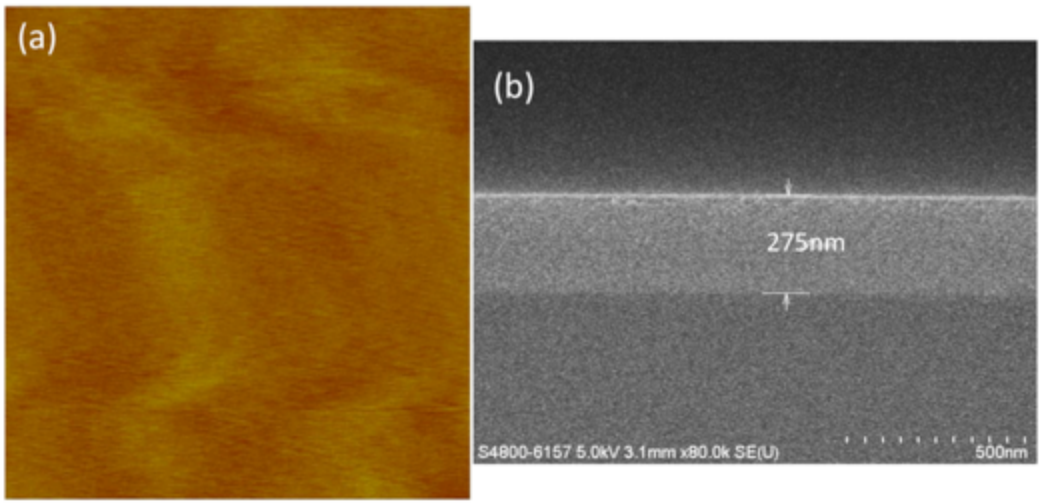

Figure 3.13 (a) 2-D AFM of BST thin film of 275 nm in thickness; (b) Cross-sectional SEM of BST thin film of 275nm in thickness.

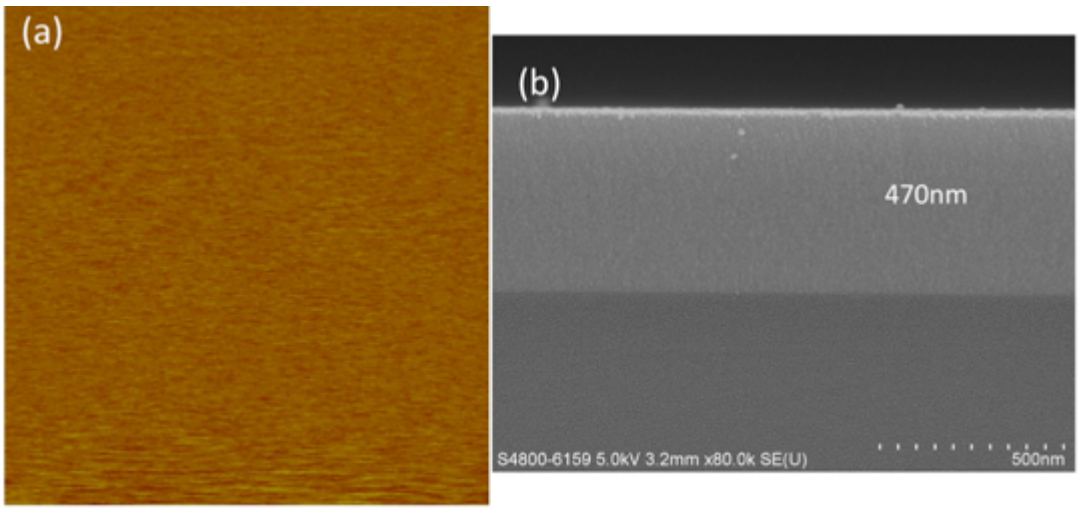

Figure 3.14 (a) 2-D AFM of BST thin film of 470 nm in thickness; (b) Cross-sectional SEM of BST thin film of 470nm in thickness.

Table 3.2 The summary of RMS of four different BST thin films

Thickness of BST thin film (nm)	The surface roughness(RMS/nm)
122	0.164
216	0.119
275	0.114
470	0.108

weak decreasing trend can be observed, which confirms the prediction. Besides, it has been reported that based on rougher dielectric, lower mobility is observed, as shown in Figure 3.15. And the corresponding mobility for pentacene on top of SiO_2 with different roughness is shown in Figure 3.16. For OFET with rougher SiO_2, holes will be located in deeper roughness "valleys" of the dielectric surface, V_{DS} only supports drift movement along the surface and cannot support a charge movement out of the roughness valley. In other words, the holes are "trapped" in the roughness minima and structure can be explained as shown in Figure 3.17. Usually, S-K growth mode will result in large crystals, less grain boundaries and further high mobility. The performance of the pentacene layer in the BST in our work has also been characterized by AFM, as shown in Figure 3.18. Large crystals of several micrometers can be clearly seen. Besides, the crystallinity of pentacene is also characterized by XRD, as shown in Figure 3.19, which confirrms the highly crystallized pentacene islands in the thin film which guarantee the high hole mobility.

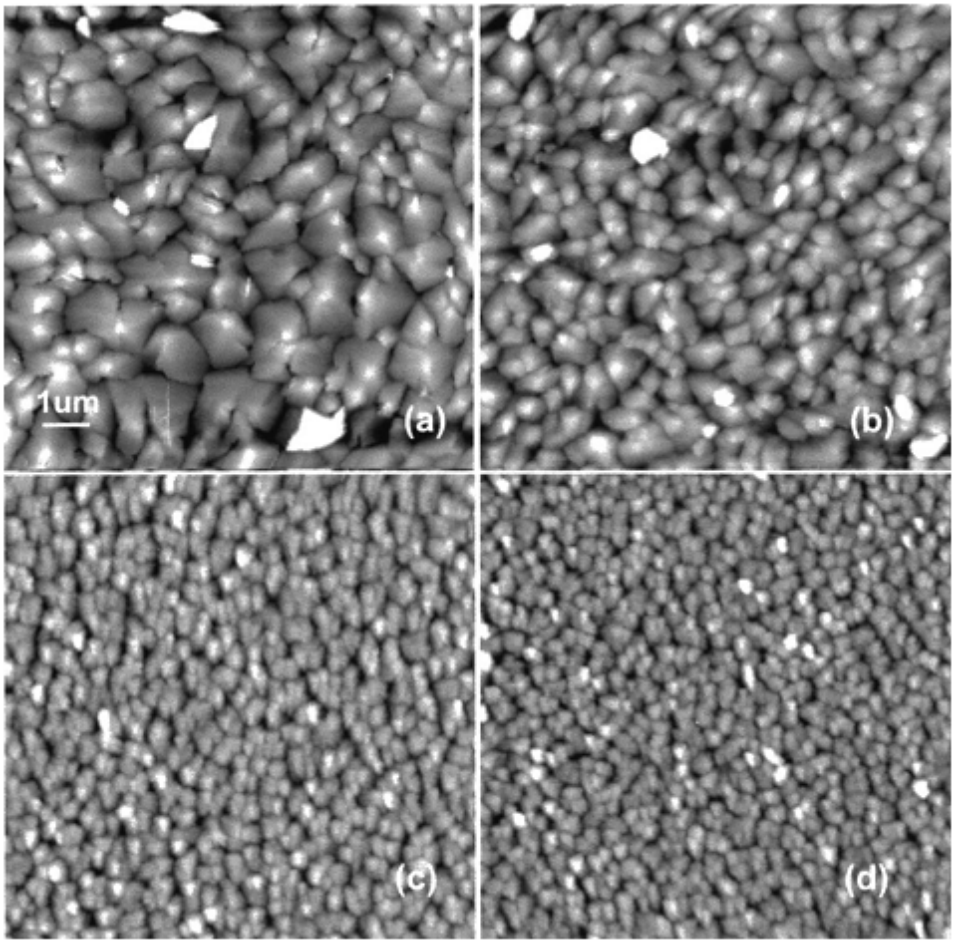

Figure 3.15 Pentacene on SiO_2 surfaces with different roughness: (a)1.7 Å, (b)7.6 Å, (c)54 Å and 92 Å, respectively.

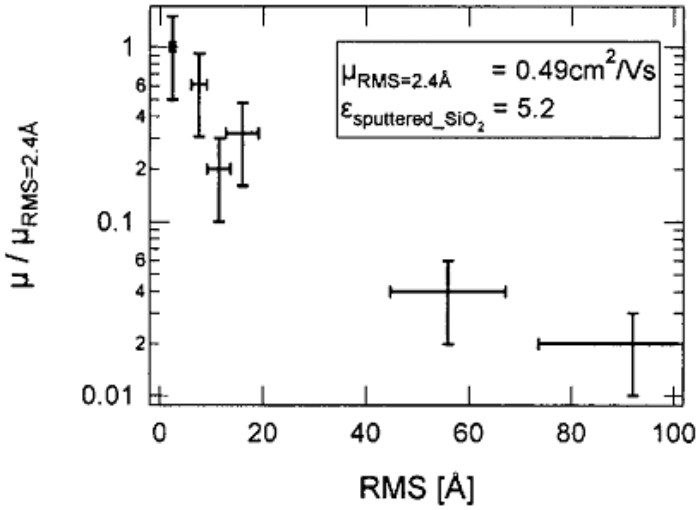

Figure 3.16 Mobility versus RMS of SiO_2

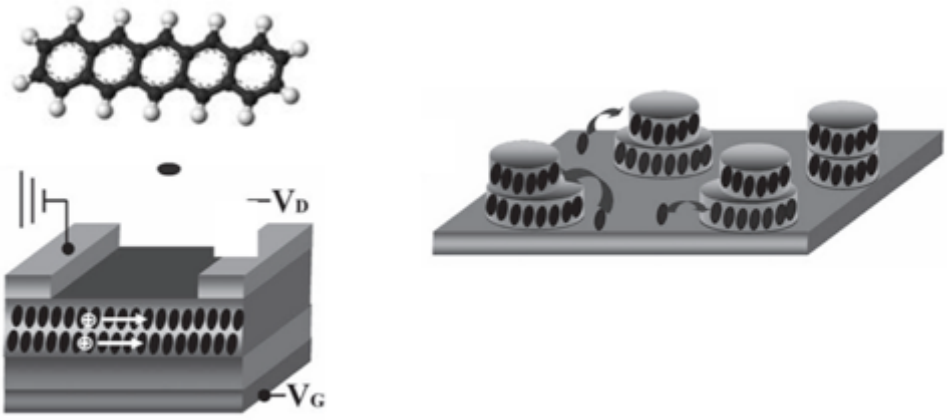

Figure 3.17 the S-K growth model of pentacene layer and the effect in OFET device[84].

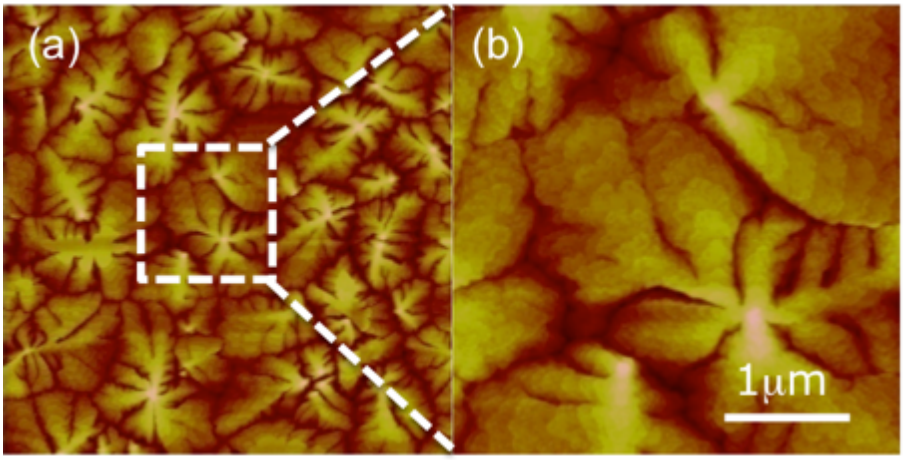

Figure 3.18 The AFM image of pentacene layer evaporated on BST thin film.

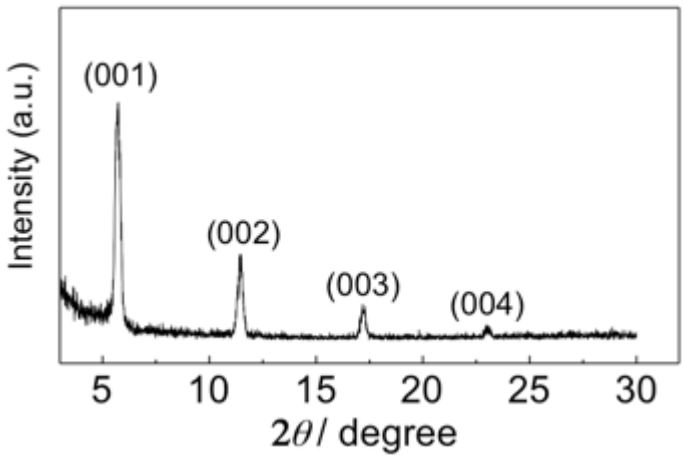

Figure 3.19 The corresponding XRD pattern of pentacene grown on BST thin film

3.3 Flexible device performance with BST deposited on PEN flexible substrate

Considering the BST is deposited at temperature of 110 ^{o}C and the low operating voltage of the BST OFET device, it is safe to say the device will be able to be incorporated onto the flexible substrate.

In order to confirm the applications of low temperature PLD growth BST film on flexible substrate, we deposited the amorphous BST film on 125μm PEN substrate (Good Fellow, maximum operating temperature ca. 150^{o}C) under the same conditions as the silicon based device and a 100nm thick of Ag is patterned as the bottom gate electrode. Figure 3.20 (a) shows the cross-sectional schematic structure (not in scale) of the OFET devices on PEN substrate. (b) is the SEM cross-sectional of OFET device on top of PEN substrate. The top layer is pentacene which is around 40nm monitored by quratz crystal microbalance (QCM). And BST is about 670nm thick. (c) is the 3-D AFM of pentacene thermal evaporated on top of BST deposited on PEN. The crystal size is just 1-2μm, which much smaller than that on BST deposited on silicon substrate, as shown in Figure 3.18. (d) is the C-F and C-V performance of corresponding BST as shown in (b). The electrical performance of a representative OFET device is shown in Figure 3.21. Same as the device on silicon substrate, the device can be saturated at -3V based on high-*k* BST thin film. Although the V_{th} (-0.68V) and the on/off ratio(1.37×10^{4}) of the flexible device are comparable with the

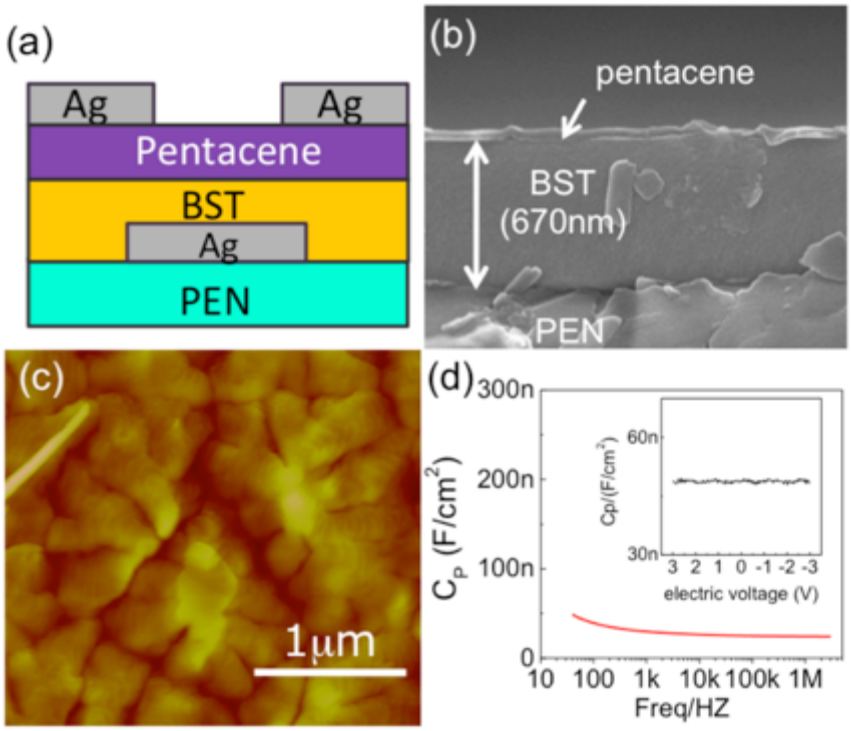

Figure 3.20 (a) Optical image of BST OFET device on flexible PEN substrate, (b) AFM 3-D image of pentacene grown on BST on PEN substrate, (c) The SEM cross sectional of BST thin film on PEN substrate. (d) The C-F and C-V measurement of BST thin film.

device on silicon, the subthreshold swing and the field effect mobility show degradation and the values are 260mV/dec, and 1.01cm^{2}V^{-1}s^{-1} respectively. Although the performance of the OFET on BST/PEN is not as good as the one on BST/silicon, the mobility, threshold voltage and subthreshold swing of the current flexible devices are highly comparable with the previous reported result. [85, 86] This shows the

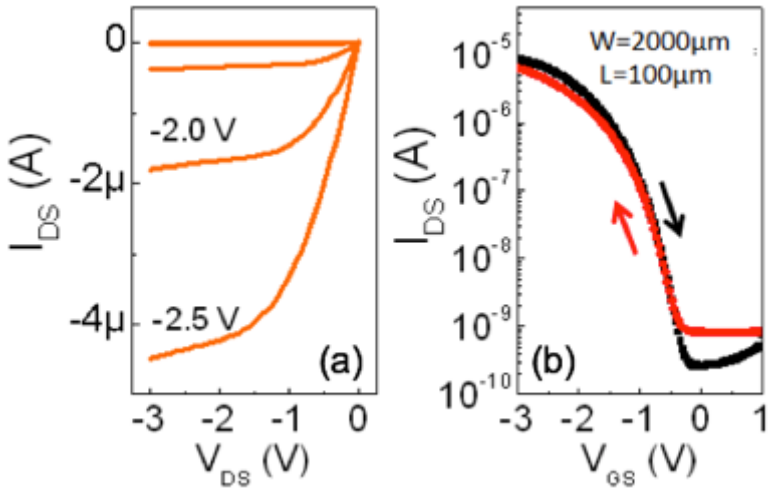

Figure 3.21 (a) Output curves of BST OFET fabricated on PEN substrate; (b) The corresponding transfer curves of the same device of (a).

potential of using PLD for low temperature dielectric deposition on flexible substrate. The decrease of the carrier mobility could be attributed to the large surface roughness of the PEN substrate which jeopardizes crystallization of pentacene(smaller crystals and more grain boudaries) (see Figure 3.20(c)) as well as the interface contact between the bottom gate electrode and the BST film.

The advantag of flexible devices are flexibility and the flexibility of OFETs based on BST fabricated on PEN substrate is studied. Figure 3.22 (a) shows optical photo of flexible OFETs on PEN substrate. (b) shows the picture of the experimental setup for the upward bending measurement on the BST/PEN OFET. The variation of the normalized mobility and threshold voltage as a function of upward (convex) and

downward (concave) bending radius, as shown in Figure 3.22 (c) and (d). The mobility of device keeps decreasing with decreaing the bending radius. With the bending radius decrasiing, the tensile strain in the active layer is increasing based on the thickness profile. Then pentacene is in increasing tensile strain and the distance between pentacene moleculers are getting larger, which will make it more and more difficult for the charges in the channel region to hop from one molecuar to another. However, the threshold voltage is decresing and approching 0V. Drain and source electrodes are also in larger tensile strain with the bending radius is decreasing, then the contact between drain-source electrode and the pentacene is improved, which decreases the contact resistance and improves the charge injection. [87] According to the equation for the strain S: $S=d_S/2D$, where d_S is the thickness of the substrate and D is the bending radius, the strain within the device is around 1.9% when the bending radius less is 3.25 mm.[24] The strain is close to a value where buckling and delamination of electrodes may occur.[88] For the downward bending test, the mobility increases first and then decreases. At first, the effect of the space decrease between pentacene moleculars dominates. After the bending radius of 5.0mm, the contacts, including drain-source with pentacene, pentacene with BST and BST with gate electrode, become poor and the mobility decreases. It is the same reason that the threshold voltage keeps increasing. The contacts are poor, then larger voltage is needed to induce more charges to the channel region to form the conducting channel and turn on the device. To further confirm that the reason for mobility and threthold voltage is in active layer of pentacene and contact, the investigation has been done on BST thin film with different

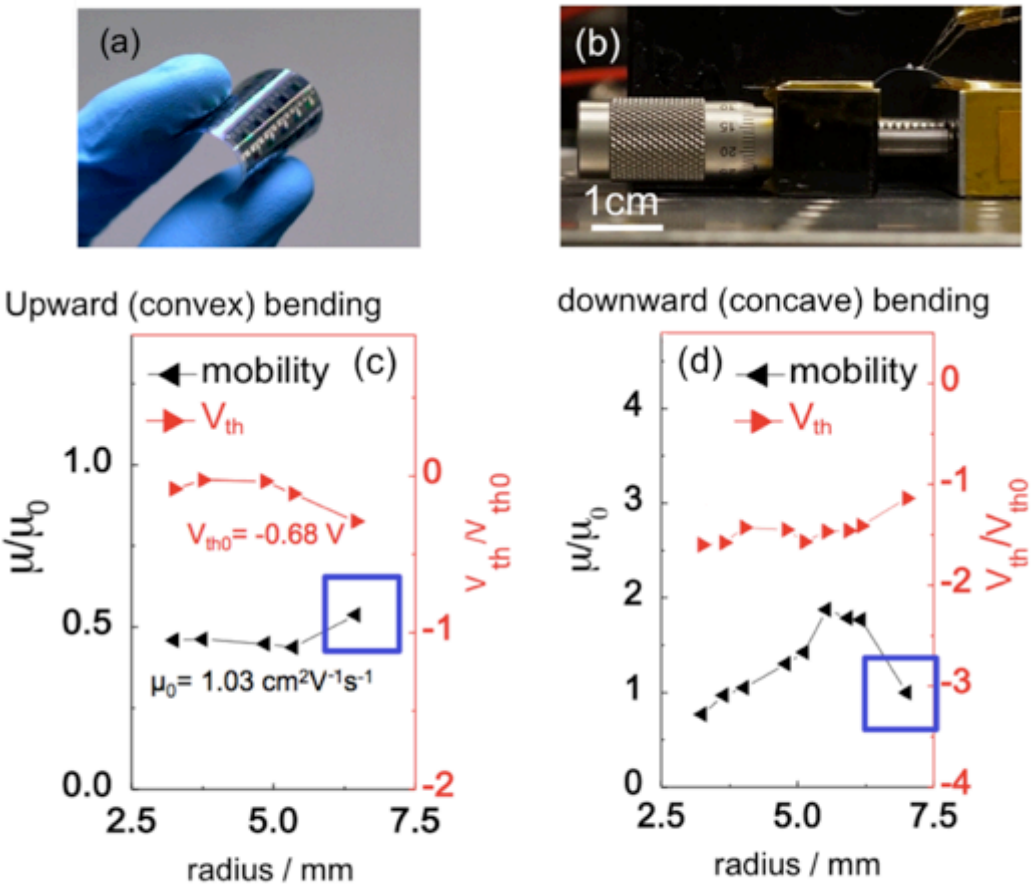

Figure 3.22 (a) The optical photo of OFETs on PEN substrate. (b) The photo of bending test setup. The normalized mobility and the threshold voltage versus bending radius of the (c) upward (convex) and (d) downward(concave) bending test.

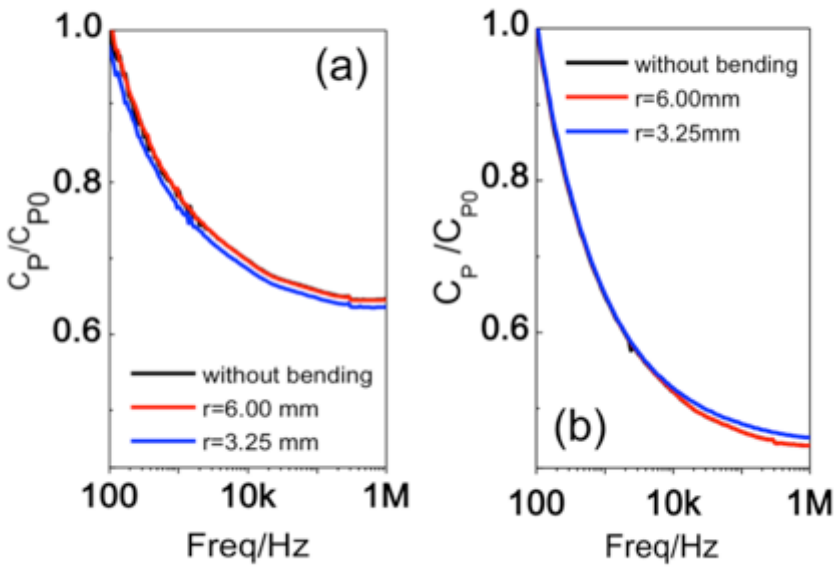

Figure 3.23 The capcitance versus frequency of BST thin film with different bending radius of (a) downward (b) upward bending

bending radius. The capacitor structure is adapted to examine the dielectric performance of BST thin film during bending test, with BST sanwiched between bottom and top Ag electrode and bottom Ag electrodes deposited on PEN substrate. The normalized c–f measurement results of a single BST dielectric thin film on PEN substrate under different bending radius are shown in Figure 3.23. It can be noticed that the capacitance of the BST thin film is independent of the bending radius and thus the mobility change in the device under two kinds of bending test is not due to the capacitance change of the dielectric layer.

3.4 Summary

In conclusion, we demonstrated the feasibility of low temperature PLD growth BST thin film as the high-*k* dielectric of the OFET, we successfully fabricated pentacene based OTFT on both silicon and PEN substrates with operating voltage less than 3 V. From the high resolution TEM and AFM image, we confirmed that the interface between silicon and BST is smooth and the pentacene layer shows excellent crystallization of islands with S–K growth mode. By transferring this dielectric growth method onto PEN flexible substrate, we demonstrated these OTFTs can operate with a voltage equals to 3 V with mobility 1.01 $cm^2 V^{-1} s^{-1}$ and subthreshold swing 260 mV/decade on flexible substrate. Also the bending test of the flexible device shows decent flexibility; the mobility can maintain at around 0.5 $cm^2 V^{-1} s^{-1}$ or higher while the bending radius is around 3mm for both upward and downward bending tests. These show the high application potentials of the low temperature PLD growth high-*k* metal oxide for the flexible circuits and portable electronics.

Although the current BST are deposited on silicon and PEN substrates with an area just 6.55 cm^2 (1 in.×1 in.), this method has been demonstrated for deposition of thin films with a much larger area before.[89] Furthermore, the BST dielectric is compatible with both top and bottom gate contact configurations, as well as various fabrication techniques other than thermal evaporation such as solution processing, vapor jet deposition.[90] To the best of our knowledge, it is the first demonstration of amorphous BST thin film grown by PLD at low temperature for flexible OFET

applications. The stable performance of the OFET under bending test shows its potential for flexible electronics.

Chapter 4. OFETs with BST thin film derived by sol-gel and UV-Ozone

4.1 BST thin film deposited by sol-gel and UV-Ozone

OFETs are playing an important role in many new generations of organic electronic devices, such as memories, bio-sensors, displays drivers and RFID.[91-94] Other than the lifetime and flexibility of the devices, one of the major challenges in these devices is to reduce the operating power for the portable or wearable electronic applications and make them compatible with dry cell powering. In the applications of OFETs, low operating power means sufficient charges can be accumulated at the semiconductor/dielectric interface to generate a conductive channel under a small voltage bias at the gate. The density of the induced charges Δn is proportional to the areal capacitance of dielectric insulator (C') and is given by $\Delta n = (V_G - V_{th})C'/q$, where V_G, V_{th} and q are the gate bias, threshold voltage and the electronic charge, respectively. To maintain Δn at sufficient large value while V_G-V_{th} is small for power operating, the areal capacitances of the dielectric thin films have to be large. Depending on the charge mobility of the organic semiconductors and other geometry parameters of the OFET, the dielectric film usually requires large areal capacitance, so that the operating voltage can be less than 5V. One of the possible methods to increase C' is by reducing the thickness of the dielectric layer, such as the ultrathin 3nm thick hafnium oxide (HfO_x)

layer reported by Jen *et al*.[71] A common drawback of the ultra thin dielectric is the high leakage current through the gate which plays a critical role in the device performance. To alleviate the defects, SAMs are usually employed,[37, 47] however, the functional head groups of the SAMs are usually dielectric specific which limits their applications on arbitrary dielectric or gate electrode over a large area. For example on SiO_2, strong Si–O–Si bonds connect the precursor silane to the surface silanol (–Si–OH) groups.[95] On the other hand, instead of oxide, noble metals requires SAMs with alkanethiols group head to form the monolayer on the surface directly.[96] Alternatively, the operating power of OFET can also be reduced by using high-*k* dielectric materials. The deposition of the high-*k* materials can be achieved by different methods as summarized in Table 2.1. Although the solution methods do not demand vacuum environment or expensive deposition equipment, they may still require inert environment (for high-*k* polymer dielectric) or high temperature annealing (annealing temperature of the traditional high-*k* dielectric formed by sol-gel method ranges from as 180^{o}C[72] to as high as 600^{o}C[71]), and thus they are not compatible with ambient air and room temperature deposition. As a result, a universal high-*k* dielectric material which can be spin-coated on different gate electrode on flexible substrate under air and low temperature would be extremely valuable for the development of next generation OFET devices.

Recently, a new UV-Ozone dielectric treatment method has been proposed for high quality sol-gel thin film fabrication. Jen and coauthors have fabricated ultra thin HfO_x

film of 5 nm on both silicon and Kapton substrate for the OFET applications. However, the temperature is as high as 200^{o}C, which is a lot higher than the glass transistion temperature of many commercial flexible substates.[97] Besides, Salleo and coauthors have also reported ultrathin ZrO_x of 6-7nm on silicon by UV irradiation (Ozone is proposed to oxidize the thin film) at room temperature and the OFET has an operating voltage of less than 3V. [74] Since the thickness of both HfO_x and ZrO_x are both less 10nm, it would be sensitive to surface roughness of the substrate which may cause leakage problem. Then. SAMs were needed on the ultrathin dielectric films for the OFET application.

Here, we propose a new kind of high-*k* amorphous $Ba_{0.62}Sr_{0.28}TiO_3$ (BST) material derived by layer-by-layer sol-gel method and solidified by UV-Ozone treatments under ambient air and room temperature environment.

4.2 Preparation of BST thin film

4.2.1 The sol-gel preparation process

Here we proposed a new kind of high-*k* amorphous $Ba_{0.7}Sr_{0.3}TiO_3$ material, also derived by sol-gel method also solidified by UV-Ozone methods at quite low temperature and at air atmosphere. To prepare the sol precursor of BST thin films, $Ba(CH_3COO)_2{\cdot}2H_2O$, $Sr(NO_3)_2$, $Ti(C_4H_9O)_4$ are raw materials. Acetylacetone (AcAc) is used as complexing agent and ethylene glycol monomethyl ether along with ethylene glycol as solvents. First, $Ba(CH_3COO)_2{\cdot}2H_2O$ and $Sr(NO_3)_2$ are dissolved in mixed solvents of ethylene glycol and ethylene glycol monomethyl ether and heated to 110^{o}C to get Ba-Sr solution. Regulating Ba to Sr ratio in the sol precursor will give different Ba/Sr in the thin film. $Ti(C_4H_9O)_4$ was diluted in the mixture of solvents of ethylene glycol monomethyl ether and ethylene glycol with complexing agent AcAc to make Ti solution at room temperature. Nitric acid was introduced to prevent the hydrolyzation of Ti. Finally, the cooled down Ba-Sr solution was added to the obtained Ti sol mixture to make final (Ba-Sr)-Ti sol precursors. The concentration was controlled to be about 0.1 mol/L in molarity of BST. The preparation of BST solution and BST thin film deposition process is shown inFigure 4.1. The BST sol precursors are deposited on both n++ silicon (University wafers)and PEN substrates (GoodFellow) by spin coating method and solidified by UV-Ozone(Jelight Company Inc. UVO-cleaner 42-220) Both silicon and PEN substrates are sonicated in deionized water, acetone and isopropanol, respectively. For silicon substrate, HF acid (40%) treatment is done on both sides by

immersing the substrate in HF for 15minutes. Before the substrate is put into chamber for the bottom Al electrode evaporation, the PEN is put into UV-Ozone chamber for 5 minutes for surface cleaning. The rotation speed is all 4000 rpm for two solution drops for one layer. The rotation time for the first drop is 10 seconds and 30 for the second drop. The wet films are treated in air atmosphere by UV-Ozone for 30 minutes for the first layer and 10 minutes for the following layers. To get the obtained thickness, the spin coating and the UV-Ozone treatment were repeated for 3 times in this contribution.

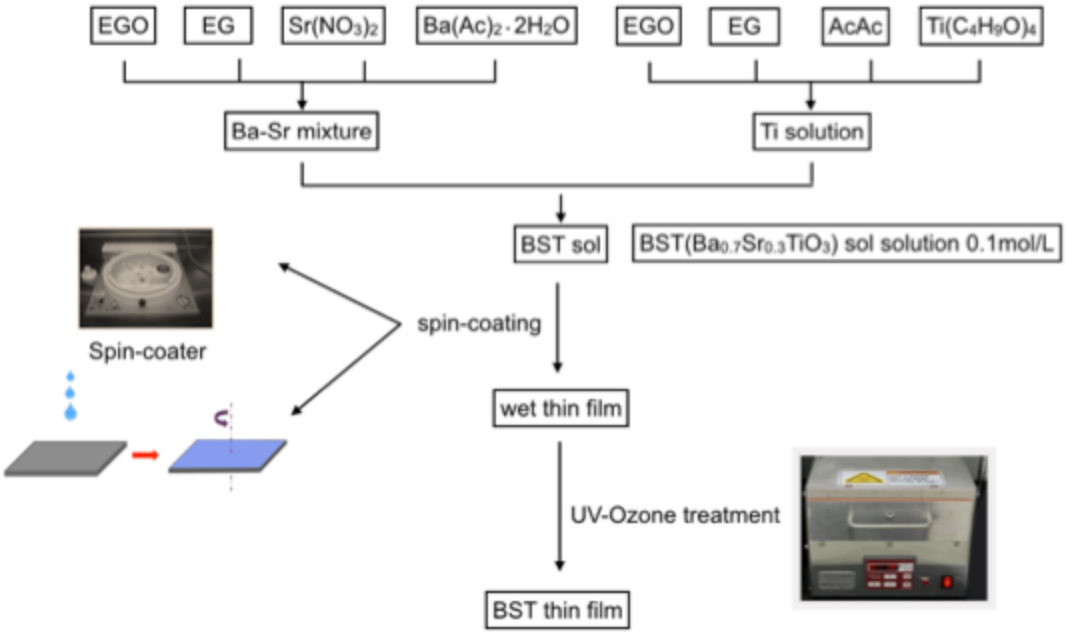

Figure 4.1 The preparation procedures of gate dielectric BST thin films.

4.2.2 Formation mechanism of BST thin film by UV-Ozone treatment

With the prepared BST sol-gel solution, wet thin film can be obtained by spin-coating on both different substrates, including silicon(as substrate and at the same time gate electrode for OFET devices) and PEN substrate(with patteren Al electrodes deposited as gate electrodes). Then the wet thin films are put into UV-Ozone chamber next to the spin-coater as soon as possible. The UV-Ozone treatment process is done in air atmosphere UVO cleaner (28~32 mW/cm^2 @ 253.7 nm) for 30 minutes for the first layer and 10 minutes for the following layers for capacitor and OFET devices. To get the obtained thickness, the spin coating and the UV-Ozone treatment were repeated for 3 times in this contribution.

(1) The short wavelength of UV light will make O_2 photolyze and result in two triplet state oxygen atoms ($O(^3p)$):

$$O_2 + h\upsilon\ (<240\ \text{nm}) \longrightarrow O(^3p) + O(^3p) \qquad \text{Equation 4.1}$$

(2)then, $O(^3p)$ combines with O_2 to form ozone (O_3):

$$O_2 + O(^3p) + M \longrightarrow O_3 + M\ (\text{M is a third body}) \qquad \text{Equation 4.2}$$

(3) The O_3 produced in Equation 3.2 go on to photolyze, generating singlet state reactive oxygen species ($O(^1D)$):

$$O_3 + h\upsilon\ (<320nm) \longrightarrow O_2 + O(^1D) \qquad \text{Equation 4.3}$$

(4) For the formation process of oxide layer of BST, the reactive $O(^1D)$ adsorb onto the thin film surface, diffuse into the it, accept electrons, and occupy oxygen vacancies (V_O^{2-}) in the BST thin film matrix resulting in lattice oxygen (O^{2-}):

$$O(^1D) + V^{2-} \longrightarrow O^{2-} \qquad \text{Equation 4.4}$$

Except for the low annealing temperature, the UV-Ozone process will help to fill up oxygen vacancies in the process of thin film fabrication compared with other solidification method, like just annealing at high temperature.

To get a whole picture of how UV-Ozone chamber works for the whole solidification process of BST thin film. The accompany thermal effect of the UV-Ozone chamber was investigated and the thermal effect on the formation process has been discussed too. We go through the whole fabrication process of BST thin film and record the temperature of tray in the UV-Ozone chamber by thermal couple using SABLE SYSTEMS INTERNATIONAL TC-2000 thermocouple meter. And the curve is shown below as Figure 4.2. The whole UV-Ozone process lasts 50 minutes. The time start point time 0 is around 40^{o}C which is after 5 minutes of pre-heat of the UV-Ozone machine. The blue dashed lines indicate the time drop for opening the chamber after the treatment of first layer and second layer respectively. Based on the temperature profile of the tray during the whole UV-Ozone treatment process, we fabricated OFET based on BST thin films treated just heat treated by the temperature programmed as

shown in Figure 4.2. The performance of device is shown below in Figure 4.3. It can be clearly seen that, the device based on BST just heat-treated show very poor performance. The leakage current I_{GS} is even larger than I_{DS}. Then it is safe to come to the conclusion that the UV-Ozone process is the dominate effect in the solidifying process of BST thin film and the resulted AlO_x thin layer can help to block the leakage current.

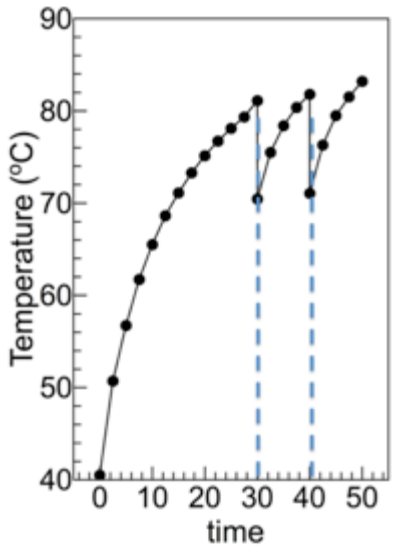

Figure 4.2 The temperature profile of tray in the UV-Ozone chamber during the whole thin film fabrication process.

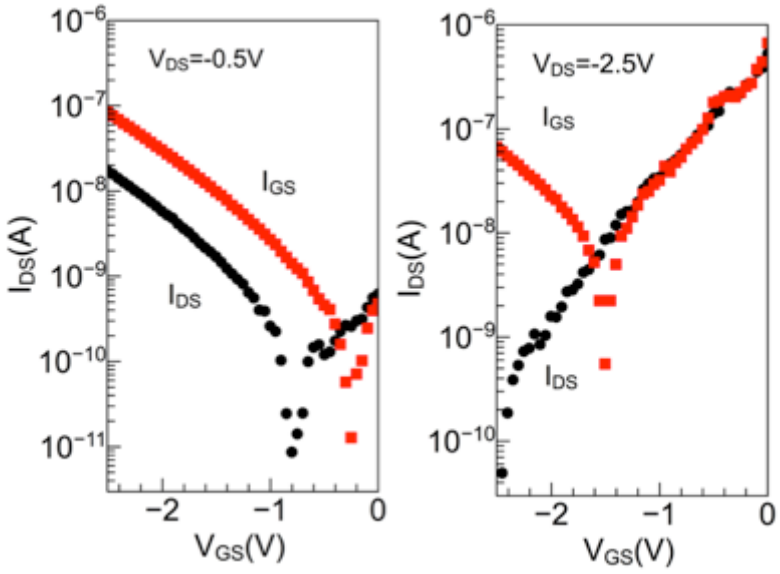

Figure 4.3 The transfer curves of OFET device based on just heat treate BST thin film on silicon substrate without UV-Ozone

4.2.3 The pentacene OFET devices based on the BST thin film derived by UV-Ozone

The pentacene OFET devices are fabricated with 40nm pentacene thermal evaporated on top of BST thin film directly after the UV-Ozone treatment. At last, the top source and drain electrodes were thermal evaporated through mechanical shadow masks. The capacitor devices are structured with BST thin film sandwiched between bottom Al electrode and top Ag electrode. The electrodes are all deposited by thermal evaporation.

Figure 4.4 (a) shows the picture of the OFET and the schematic structure of the device on flexible PEN substrate. The detailed device fabrication process and parameters are discussed in the experimental section. Transmission electron microscopy (TEM, Philips Tecnai G220 S-TWIN) is used to characterize the crystallization behavior and the actual thickness of the BST thin film on the n+ silicon electrode. Figure 4.4 (b) shows the cross-sectional images of the dielectric stack at different regions of the Al gate electrode (60nm) and silicon substrate. It can be noticed from the enlarged TEM image that there are thin layers of AlO_x and SiO_2 on the Al gate electrode and silicon substrate respectively. The oxide layers are believed to be formed during the UV-ozone treatment of the BST layer, similar to the effect reported in Ref.[14, 97]. The thicknesses of BST thin film and AlO_x are around 28 and 4 nm, respectively. The double layers of BST and AlO_x are like two capacitors in series. Based on the capacitance calculation equation and the dielectric constant of the reported ultra thin AlO_x (around 7.8),[98] the dielectric constant is calculated to be around 11 and the equations for calculation are shown below. The capacitance of the BST on Al gate electrode on PEN substrate is around 300nF/cm^2 and 358 nF/cm^2 on Si as both gate electrode and substrate. Considering the dead layer effect as discussed in Section 3.2.1, native oxide SiO_2 formed during the UV-Ozone process is thinner than AlO_x which will cause larger dead layer effect in this native oxide layer already. The smaller thickness of SiO_2 than AlO_x is probably due to the higher density of Si substrate then it is difficult for active O species to diffuse into further depth. To get more accurate dielectric constant, only dielectric constant of BST deposited on Al gate

electrode is calculated. The conductivity of the BST and the AlO_x dielectric are different, then the two dielectrics are just like two capacitors connected in series. The effective capacitance (C_e) can be calculated from capacitance and the thickness (d) of BST (B) as well as AlO_x (A) and by Equation 4.5 shown below.

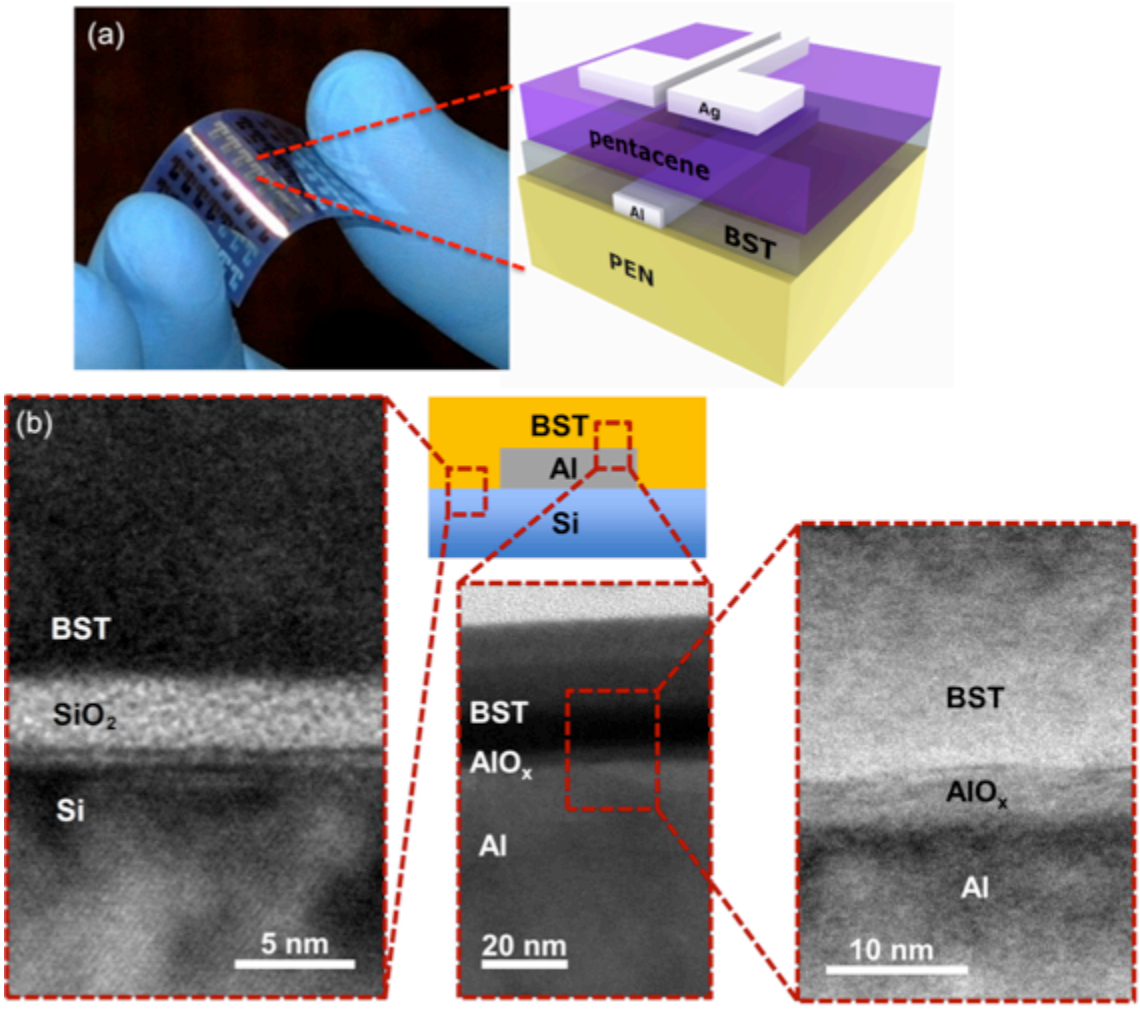

Figure 4.4 (a) is the schematic structure of the OFET device on PEN substrate. (b) TEM cross-sectional of BST thin film on Al bottom electrode evaporated on silicon substrate.

$$\frac{1}{C_e} = \frac{1}{C_A} + \frac{1}{C_B} \qquad \text{Equation 4.5}$$

$$C_e = \frac{\varepsilon_0 \varepsilon_e S}{d_A + d_B} \qquad \text{Equation 4.6}$$

then

$$\frac{d_A + d_B}{\varepsilon_e} = \frac{d_A}{\varepsilon_A} + \frac{d_B}{\varepsilon_B} \qquad \text{Equation 4.7}$$

In our thin film structure, d_A is the thickness of AlO_x of around 4 nm, d_B is the thickness of BST of 28nm. ε_A is assumed to be around 7.8 (amorphous and ultrathin).[98] ε_e was calculated from the measured Capacitance per area(about 300nF/cm^2), where C_e is the measured capacitance. Substituting the measure thickness and the measured capacitance as well as the constant ε_0(8.85*10^{-14}/cm), then the constant of BST can be estimated to be around 11. This value is a lot smaller than that of the PLD derived BST thin film. This is probably due to the a lot smaller thickness of UV-Ozone deposited thin film. Then far more dead layer effect will result in apparently small dielectric constant.

The thin layer of AlO_x plays important role in blocking the leakage current. The control sample with BST solution spin-coated on Al bottom electrode treated in air at the temperature same as the tray of the UV-Ozone tray but no UV-Ozone and there should be negligible AlO_x without reactive oxidizing species formed during Ozone

formation and decomposition process, which shows large leakage current and then confirms the dominating effect of UV-Ozone in the solidifying process of BST(see Figure 4.3). Different from the high temperature annealed BST thin film, it is important to point out that the current UV-ozone treated BST layer shows no diffraction lattice structure which shows the amorphous nature of the film, which will result in lower dielectric constant. Different from the high temperature annealed BST thin film, it is important to point out that the current UV-ozone treated BST layer shows no diffraction lattice structure which confirms the amorphous nature of the film.

The as prepared BST thin film was studied by XPS (Physical Electrics 5600 multi-technique system, Versa Probe II Scanning XPS) to verify the chemical states of different elements in the thin film. Figure 4.5 (a) shows survey scan of the BST thin film. The black, red and blue curves represent the as prepared BST thin film, BST thin film after first and second argon ion etching process respectively. The binding energy peaks of the three curves almost coincide. The identical peaks in two curves after the first and second ion milling suggest that the composition of the film is uniform. The four elements (Sr, Ti, O and Ba) were investigated separately, from low to high binding energy in the survey scan curves. The peaks at around 134.3eV and 136.1eV are for Sr 3d peaks, as shown in Figure 4.5 (b). The binding energies of these two peaks are slightly larger the Sr 3d peak value (133eV) in Ref. [99] in which the $SrTiO_3$ is hydrothermal treated in at 245^{o}C. The larger binding energy is believed to be due to the ozone effect, which converts the elements to the oxidized state, resulting in fewer

electrons in the outer orbitals and thus higher binding energy. The binding energy peaks around 459.2eV and 464.9eV are for the titanium 2p 3/2 and 2p 1/2 respectively (Figure 4.5 (c)). According to Ref.[100] (458.8 eV for Ti 2p 3/2, 464.6 eV for Ti 2p ½ in high temperature annealed barium titanate). It can be noticed in Figure 4.5(d) that there are two oxygen peaks at 530.9 eV and 532.6 eV respectively. The lower one at 530.9 eV should be for the O 1s state in the BST thin film. The higher binding energy

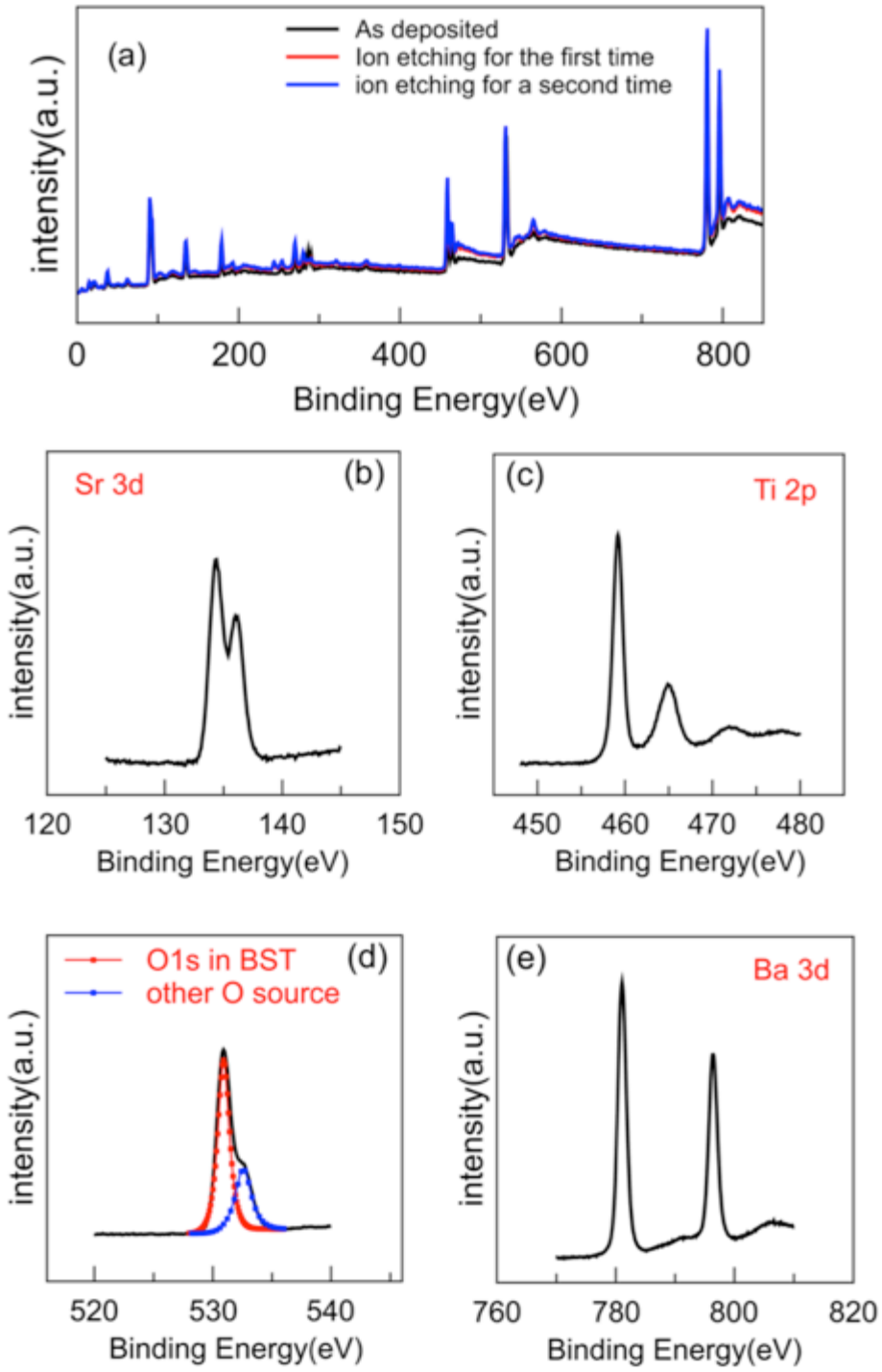

Figure 4.5 (a) X-ray photoelectron spectroscopy (XPS) survey scan of BST thin film derived by sol-gel method and UV-Ozone treatment. (b) XPS core level spectra of Sr 3d. (c) XPS core level spectra Ti 2p. (d) XPS core level spectra of O 1s. (e) XPS core level spectra of Ba 3d.

532.6 eV should be due to the O of the carbonyl group in residual complexing agent AcAc within the film, [101]and finally the doublet peaks around 781.1 and 796.4 eV in Figure 4.5 (e) are for Ba 3d. It could be ascribed to the splitting of the Ba 3d 5/2 and 3d 3/2 spin states as shown in Figure 4.5 (e) and they are comparable with the same peak in Ref.[72]. The XPS results confirmed that the UV-Ozone treatment is an alternative method to solidify the thin film, different from the high temperature annealing which requires purging of high purity oxygen during the annealing process. Furthermore, the UV-ozone treatment can help to fill up the oxygen vacancies to form high quality ultrathin film. By using the individual peak areas and sensitivity factors from XPS quantitative analysis data, the molar proportion of this BST thin film could be evaluated as $Ba_{0.62}Sr_{0.28}TiO_{3.03}$, which is quite close to the raw material ratio as discussed in part 4.2.1.

To verify whether the thin film can be exploited to OFET devices, we examine the surface morphology BST deposited on silicon substrate (after HF treatment) and pentacene molecules thermal deposited on top, as shown in Figure 4.6. The AFM surface morphology of the Al bottom electrode, BST thin film on Al and the pentacene on top of the BST thin film by atomic force microscopy (AFM) as shown in Figure 4.7. The root mean square (RMS) for of Al electrode and BST thin film on top of Al is about 5.9 and 3.3 nm, respectively. The thermal evaporated pentacene thin film (40nm) on top of BST thin film shows grain size larger than 1μm, and layer-by-island structure (Figure 4.7(d)). This is corresponding to the S–K growth mode and provides higher

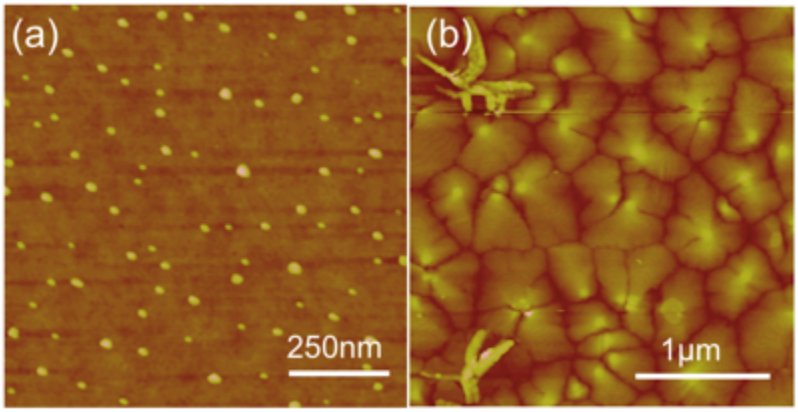

Figure 4.6 (a)2-D AFM of BST deposited on top of Si substrate. (b) pentacene crystals thermal evaporated on top of BST.

carrier mobility. After the deposition of the pentacene layer on the dielectric, source and drain electrodes are grown through mechanical shadow masks and the channel width and length are 2000 μm and 100 μm respectively. Basically, from these crystal morphology, high mobility would not be expected. To confirm this, OFET based on both BST deposited on Si and PEN were fabricated. Figure 4.8 shows that the electrical performance of the OFETs on silicon and PEN are highly comparable. On silicon substrate, the transistor device shows mobility, V_{th} and SS of 0.289 $cm^2V^{-1}s^{-1}$, -1.18V and 0.14V. For the PEN device, the output curves show typical field effect performance with the V_{th} equals -1.16 and SS equals 0.15V. At V_{DS} of -2.5V, the saturation field effect mobility can be determined to be 0.252$cm^2V^{-1}s^{-1}$. From both of output and transfer curves, the on current of OFET based on Si substrate and gate

electrode is higher than that of the device based on BST deposited on PEN substrate. However the mobility is not larger proportionally. Recalling measured capacitance silicon substrate and PEN substrate is 300 and 358nF/cm^2, respectively. On current is larger, but at the same time the areal capacitance is larger, which make the calculated mobility is not larger proportionally.

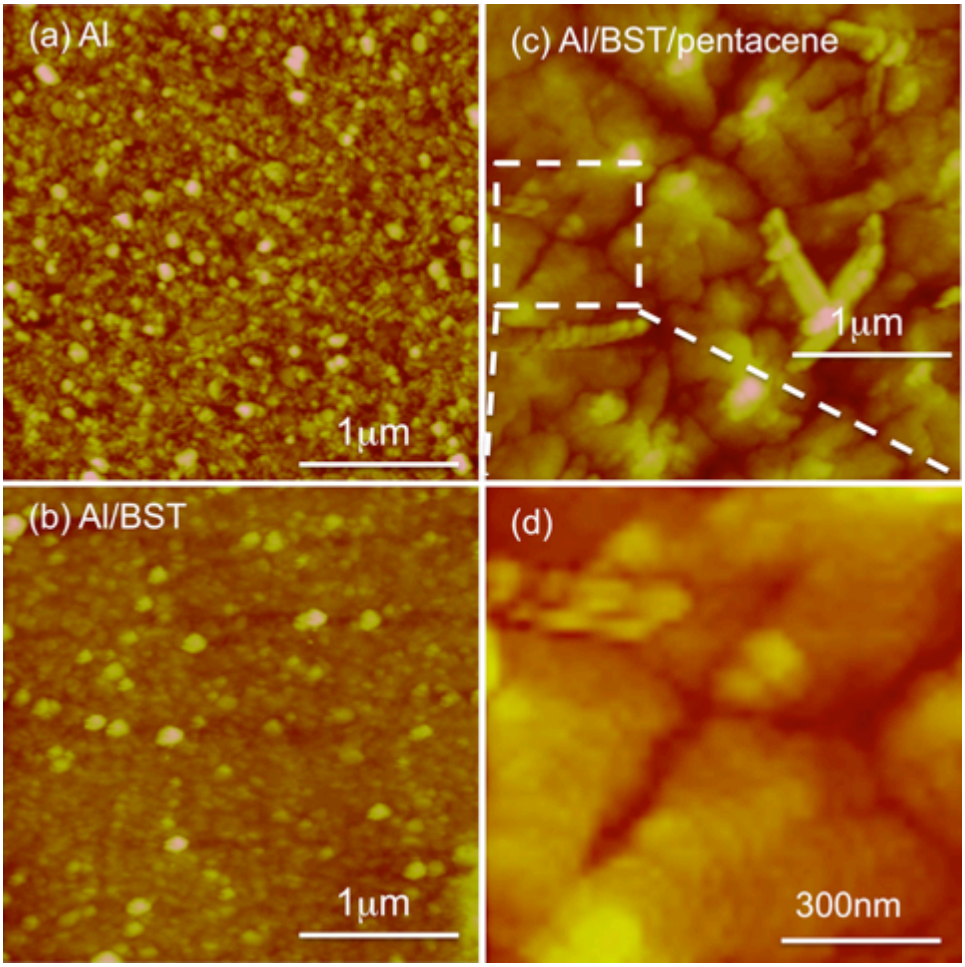

Figure 4.7 (a)2-D AFM of Al bottom electrode on PEN substrate. (b) BST on top of Al electrode. (c) pentacene crystals thermal evaporated on top of BST. (d)The magnification of the pentacene crystal shown as the square area marked by the white dashed line in (c)

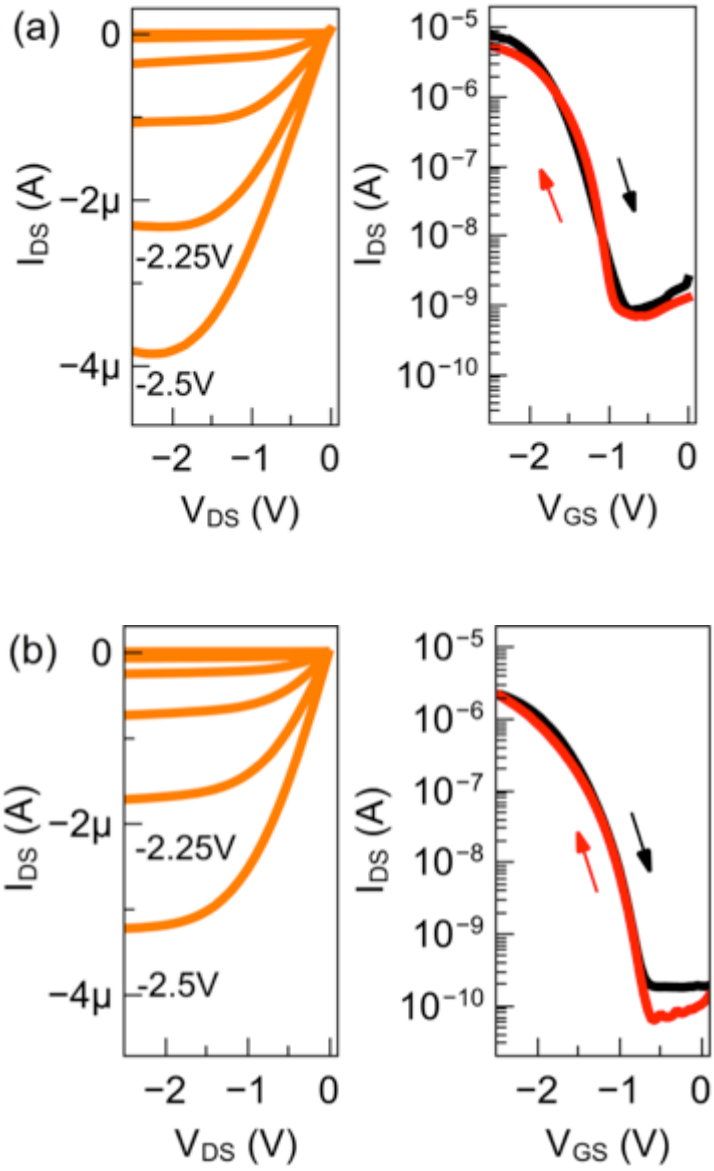

Figure 4.8 (a)The output for OFETs on silicon substrate. (b) The output and transfer curves of OFETs on PEN.

In Figure 4.9, we compared the thin film pentacene carrier mobility in different OFETs with various dielectric materials (only consists single layer of dielectric without SAM)

on flexible substrates. The pentacene mobility of our work is larger than most of the commonly solution-processed dielectric (including both low-*k* and high-*k*) such as low-*k* benzocyclobutene (BCB), [102] polyimide (PI)[24] or Poly(methyl methacrylate) (PMMA)[25] and higher *k* of polyvinyl-phenol (PVP),[23] CPVP-C_6,[103] and P(VDF-TrFE-CFE),[28] shown black circles in Figure 4.9. The mobility is also higher than that based on anodization derived Ta_2O_5, which is shown as triangle in Figure 4.9.[104]. Figure 4.9 also includes other high-*k* dielectric developed by the physical methods (blue cubes) such as RF sputtering derived and $TiSiO_2$, [105] BST [106] and BZN($Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$) derived by PLD.[107]. We directly fabricated OFET device on BST thin film right after the UV-Ozone solidification process under ambient air without any further SAM or annealing treatment. Although the mobility is smaller than the physical deposition methods, it is still significantly larger than the benchmark mobility of 0.1 $cm^2V^{-1}s^{-1}$ and sufficient for some commercial exploitation, like high resolution black and white display.[108]

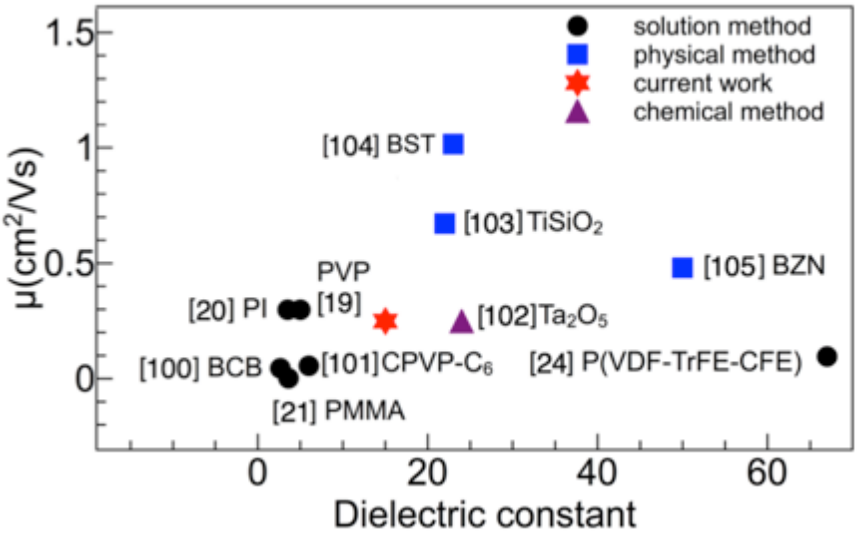

Figure 4.9 The comparison between the mobility of different flexible pentacene OFET with that of BST

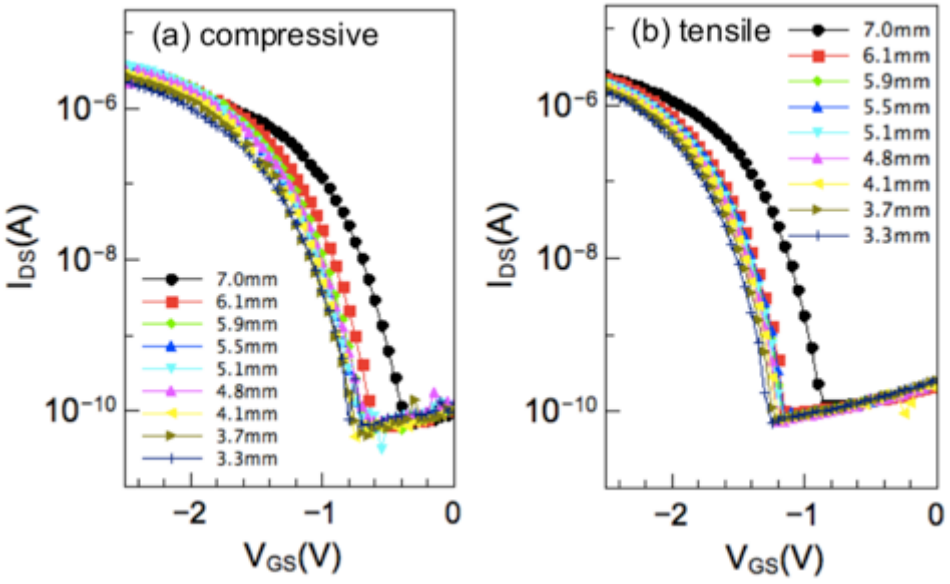

Figure 4.10 The dependence of I_{DS} on V_{GS} with different bending radius.

Since the OFETs devices have been fabricated on PEN substrate for the flexible electronic investigation, then the mechanical behaviors of the OFET devices under different bending stain have been studied, including both compressive and tensile stain. Figure 4.10 shows the transfer curves with different bending radius (different strain). For the dramatic difference in the thickness scale, the thickness of the PEN substrate is 125μm and the total thickness including BST, pentacene and the source and drain Ag electrode is around 100nm, then the neutral line (the position where there is no strain) should be in the PEN substrate. The downward and upward bending introduce compressive and tensile strain to the device while the centralized line will be in the PEN substrate as it thickness is three orders of magnitude larger than the active layers. The variation of the normalized saturation mobility and the V_{th} under different bending radius in downward bending and upward bending are shown in Figure 4.11(a) and (b) respectively. The filled circles in the both Figure 4.11(a) and (b) stand for the values without bending (bending radius equals to ∞). It can be noticed that although the variation is not significant, the V_{th} shifted to a more negative value upon both concave and convex bending. Furthermore, the mobility variation is also relatively stable under convex bending. On the other hand, while in under concave bending (compressive strain), it shows a more obvious increase and then decrease trend. For the increases of the mobility under compressive strain, it can be due to shorter distance between the pentacene molecules thus favor the hopping mechanism of the holes in the channel, or it can be due to the change of charge density in the channel resulting from the variation of the areal capacitance.[15] To further investigate the mechanism for causing the

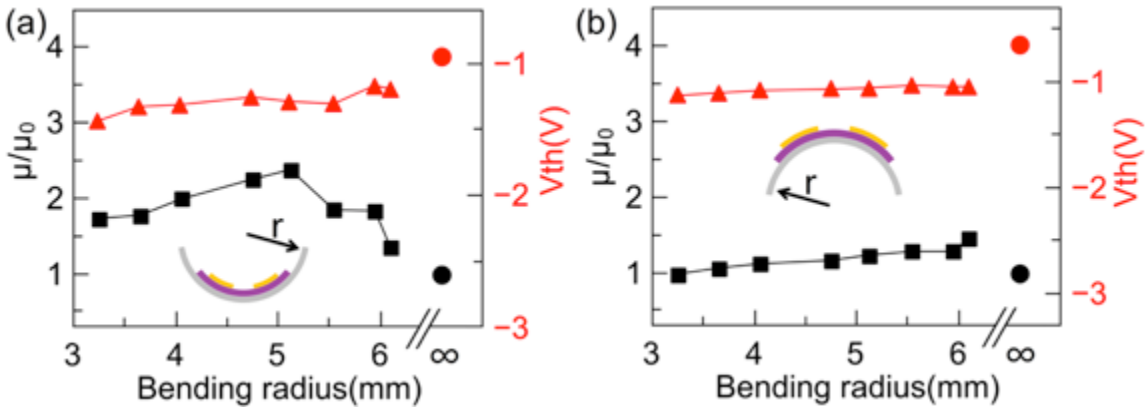

Figure 4.11 The change of mobility and threshold voltage of OFETs with (a) compressive and (b) tensile stain. The filled circles are representing the values without bending.

mobility and threshold voltage variation under compressive and tensile strain, we independently examined the dielectric properties of BST layer under both compressive and tensile strains without the pentacene layer. The capacitance of the gate dielectric layer of BST was investigated under different bending radius. Similar to the OFET structure, the BST was sandwiched between bottom Al electrode and top Ag electrode for the capacitance measurement. Figure 4.12 (a) and (b) are C-F measurements for downward and upward bending, respectively. From these two figures, it can be clearly observed that, the capacitance-frequency of the BST layer under different bending radii are almost constant, in the whole measurement frequency range. This observation is different from the polymer dielectric, in which Bao *et al* have demonstrated the dielectric properties of the polymer would also be altered by the strain-induced

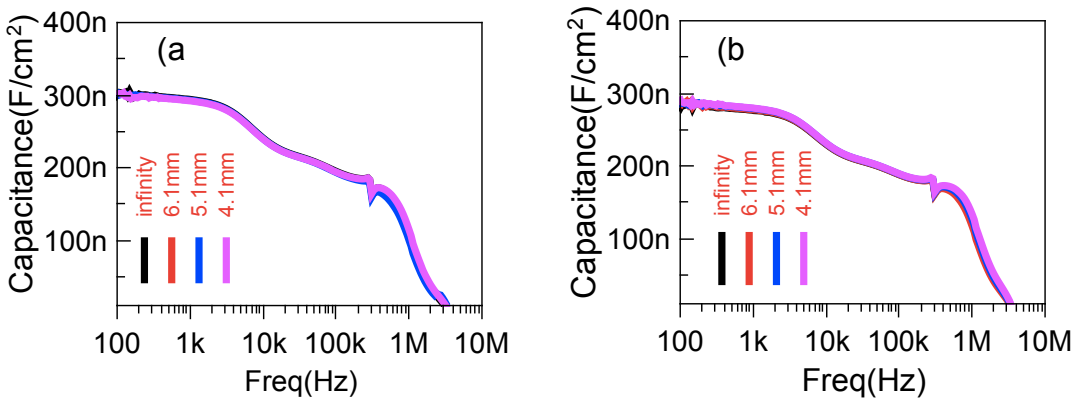

Figure 4.12 The capacitance change with (a) compressive and (b) tensile strain applied on capacitor

rearrangement of the polymer chains on the surface, such as in-plane reorientation of the phenyl group of polystyrene. As a result, the device performance of OFETs would also be affected.[109] Based on the almost constant capacitance per unit area, then it is safe to neglect the dielectric effects onto the mobility change under bending. The stable dielectric properties of the current BST thin film under bending suggests it can be used as the universal dielectric layer for flexible transistors.

OFETs devices based on BST derived by sol-gel and UV-Ozone are further exploited for the inverter application. Figure 4.13 (a) shows the circuit diagram that will be studied in this thesis. A resistor load is conncet to the drain electrode of the trannsistor device. A inverter device is used to reverse the input voltage signal and inhere inverter devices consist of a transistor and a resistor are presented. From the

circuit, with the same V_{dd} applied, if the resistor is small (several MΩ) and V_{in} is positive or 0 for p channel transistor, then the transistor is off and resistance is large. In this case, the V_{out} will be close to V_{dd}. However, when V_{in} is more negtive, which can turn on the transistor device, then the resistance of the transistor part is very small, like several MΩ. In that case, the V_{out} will be equal to $R_{transistor}/(R_{resistor}+R_{transistor})$, which will be far from V_{dd} for the similar value or the resistance of resistor and the transistor device and then can not fully reverse the V_{in}. Then the resistor connected in the circuit requires optimization. As shown in Figure 4.13, (b) shows V_{out} versus V_{in} with different resistor load connected. Considering both the V_{out} at on (V_{in} is more negtive)

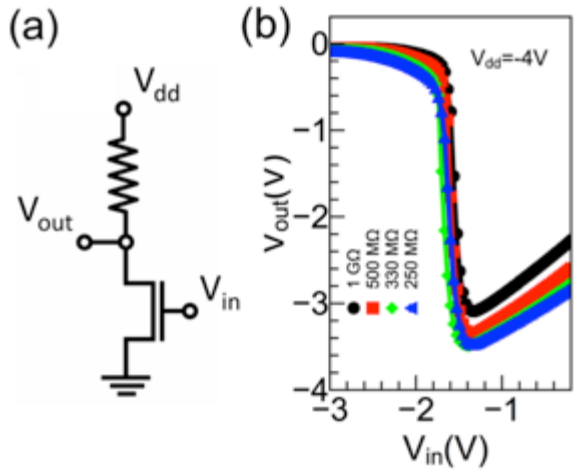

Figure 4.13 (a) The schematic circuit of the inverter device. (b)V_{out} versus V_{in} at Vdd of -4V with different resistor load

Figure 4.14 (a) shows the schematic of the inverter circuit. (b) and (c) give the V_{out} and the gain for each V_{dd}, ranging from -1 to -4V, respectively. The inverters show good switching behavior, which can switch the high potential V_{in} to the lower one and vice versa, which is shown as V_{out} in (b). The gain of the current inverters, defined as the maximum value of the slope of the V_{in} versus V_{out} curve, shows a maximum value around 20 and this is highly comparable with some of the depleted mode inverters[110]and complementary inverters.[111]

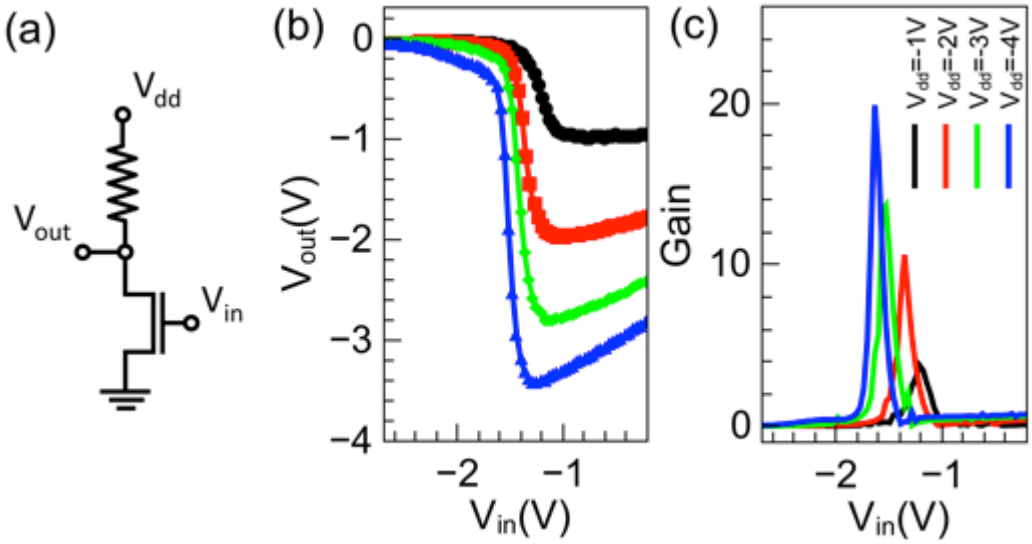

Figure 4.14 (a) The schematic circuit of the inverter device. (b) the V_{out} and (c) gain of inverter devices versus V_{in} and off end (V_{in} is less negtive) of transistor and gain, 330MΩ is chosen for the following experiments.

4.3 Summary

In conclusion, we demonstrated the feasibility of low temperature UV-Ozone derived BST thin film as the high-*k* dielectric of the flexible OFET. From the XPS results, the chemical states of all the elements in the thin film is similar as those in the thin film heat treated at high temperature, proving the UV-Ozone method is a good alternative to solidify the thin film instead of high temperature. From the high resolution TEM image, the amorphous characteristic of BST was confirmed and the thickness was around 28nm, which showed that UV-Ozone method derived thin films had good quality in spite they are extremely thin. On top of the BST thin film, pentacene layer shows islands morphology with S-K growth mode. For the OFET devices, they can be operated at voltage smaller than 3V with mobility 0.252$cm^2V^{-1}s^{-1}$. Also the inverter devices consisting of OFET and a resistor of 330 MΩ showed high gain of 20. These shows the high application potentials of the room temperature and ambient atmosphere sol-gel technology derived BST thin film for the low cost and portable electronics.

Chapter 5. The investigation of the surface energy of BST thin film

As the essential building blocks in the new generation of organic electronic devices such as flexible pressure sensors, memories, RFIDs, and display, [91-94] high performance OFETs are attracting great interests from the research community, especially in the battery-powered and portable application where the low operating voltage OFETs are required. Different high-*k* gate materials, like inorganic dielectric, polymers, and ultrathin metal oxide modified with SAMs. The problems that remain unsolved of the exsisting three solutions have been discussed in part 2.4.3 in Chapter 2. If relatively thin film is considered, like ultrathin matal oxide, SAMs become particularly to smooth out the surface and block the leakage current. However, not only the anchor group may be specific for special surface to which the SAMs will attach to. But also, terminal groups of SAMs are not universal. Ball and co-authors have reported that different SAMs surfaces show very different surface energy. It is challenging to develop a universal SAMs suitable for different dielectric insulators. More importantly, the SAM also modifies the surface energy[112], as shown in Figure 5.1. The main reason is the terminal group of different SAMs will result in different surface energy, as shown in Figure 5.2. It was reported that surface polarity is an important property, which determines a material's affinity for water molecules, normally higher polarity will give higher hydrophility. [113] Since, SAMs will affect the surface energy of

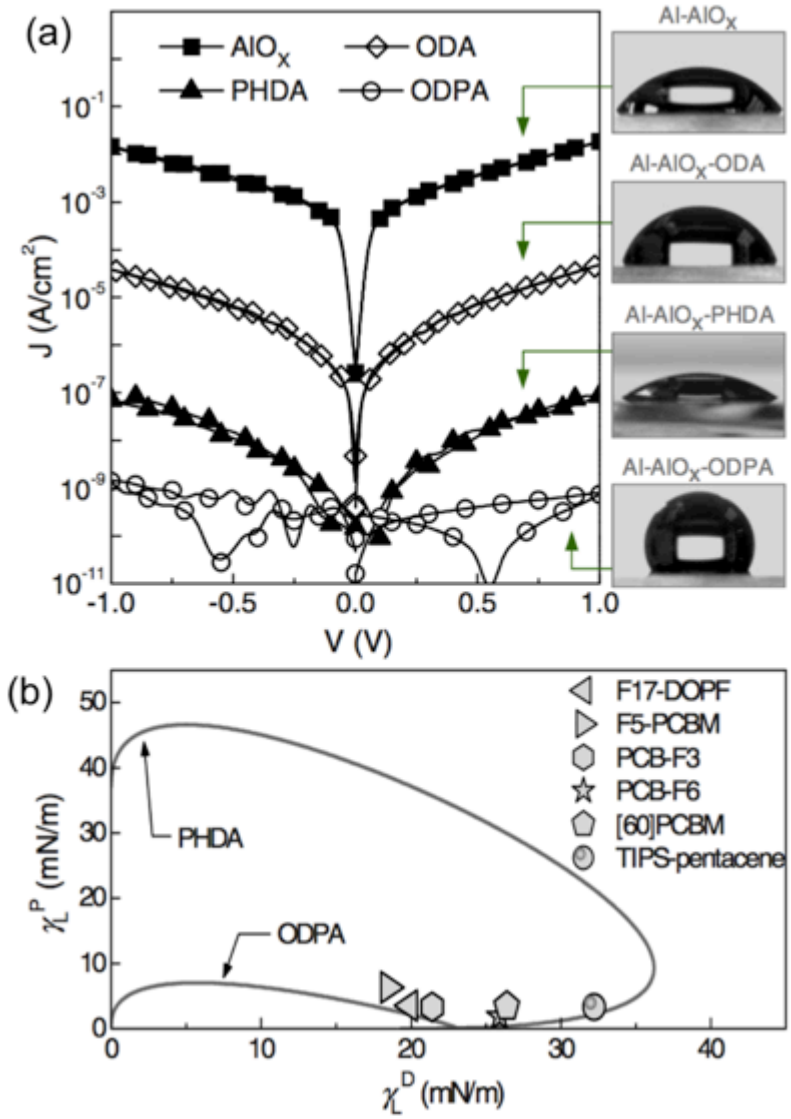

Figure 5.1 (a)Current density of MIM structure of Al-AlO$_x$-SAM-Al with area A = 2.5 10^{-3} cm^2. (b) 0^o contact angle wetting envelopes for ODPA and PHDA functionalized gate electrodes.[114]

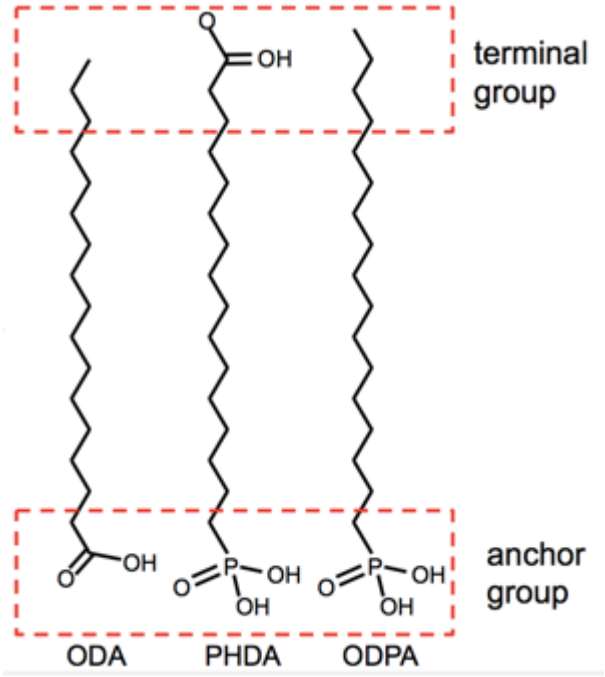

Figure 5.2 The molecular structures of octadecanoic acid (ODA), phosphonohexadecanoic acid (PHDA) and octadecylphosphonic acid (ODPA)

dielectric and the crystallinity of the organic semiconductors, it is necessary to employ a suitable SAM to achieve high crystallility and carrier mobility in the OFETs. [112]To date, it is still a great challenge in the research field to develop a universal high-k material which does not require SAM, and can be processed at moderate temperature, ambient air environment, and adjustable surface energy for both thermal evaporation and solution processing of organic semiconductors.

To address these challenges, we recently fabricated a high-k ($\epsilon_r = 11$) BST thin film treated by UV-Ozone and deposited by multi-layer spin coating deposition. The high-k

films are spin coated in ambient air and heated to a temperature of around 85^{o}C during the UV-Ozone process. The UV emits at 184.9 nm and 253.7 nm under ambient air conditions converts oxygen into reactive O species, which then diffuses into the amorphous BST thin film and reacts with the oxygen vacancies to form lattice oxygen. The reactive oxygen also removes the organic impurities in the film, which results in a high quality amorphous BST thin film with better stoichiometry. The compatibility with ambient air environment, low processing temperature, and no SAM requirement suggest the BST dielectric has extremely high potentials to be applied in developing low cost OFETs on plastic flexible substrates and have advantages over other polymers and inorganic materials. In the current study, we investigate the surface energy modification effect by varying the storage environment and time of the BST thin filmin order to achieve a universal high-*k* material for OFET fabrications without using SAM. Based on the contact angle measurements, we calculated the surface energy andthe wetting envelope of the BST high-*k* dielectric stored under different environments of five storage treatments. The fresh BST with hydrophilic surface is suitable for spincoating or drop casting of organic semiconductor deposition where surface wetting is needed for the alignment of organic molecules. On the other hand, the after storing BST thin films in evaporation chamber would reduce the surface energy of the dielectric and the work of adhesion between dielectric and the semiconductor. On the current BST high-*k* dielectric without SAM and further optimization, DNTT) and TIPS-pentacene organic transistors with average mobility of 1.51 $cm^2\ V^{-1}s^{-1}$ and $0.11cm^2\ V^{-1}s^{-1}$ are formed by thermal evaporation and drop casting solution processing.

The out-of-plane and in-plane XRD results suggest the crystallinity of DNTT thin film deposited on BST is similar to that of DNTT single crystals. With the high performance OFETs, depleted mode and saturation mode inverters with a gain higher than 25 is achieved.

BST derived by sol-gel and UV-Ozone has been shown that it is a promising high-*k* dielectric materials candidate for OFET. But it has only been used in thermal evaporation processed OFET. As a high-*k* materials derived by solution processing method at such a low temperature and in air atmosphere, if it can be used for the solution processing OFETs devices, it will be a better high-*k* dielectric candidate for both thermal evaporation and solution processing OFETs devices and the related electronic devices. In this chapter, we focused on the surface energy properties of BST thin film with different storage enviroment and time. The surface energy effect on the morphology of the semiconductor materials deposited on top of the BST and the performance of electronic devices built on that are also discussed.

5.1 Surface properties of BST thin film treated differently

5.1.1 BST thin film preparation and transistor devices fabrication

BST solution and thin film preparation:

BST solution preparation details are the same like mentioned in Chapter 4 part 4.1. The only difference is in the thin film solidification part. The UV-Ozone treatment is by UV cleaning machine from Kingo Electrical Enterprise Co., LTD. The rotation time for the first drop is 10 seconds and 30 seconds for the second drop. The wet films were treated in air atmosphere by UV-Ozone for 30 minutes for the first layer, 10 minutes for the second layer and 20 minutes for the third layers insead of 10 minutes for the UVO 42-220. Both the BST thin films on Si and PEN substrates are deposited following the same procedures.

Device fabrication

In the top contact OFETs fabricated on silicon substrate, the heavily-doped silicon (Silicon Quest) is used as the gate electrode and thermal evaporated silver source/drain electrodes (50nm) are deposited onto the DNTT thin film (45nm) (Luminescence Technology Corp., sublimated grade) by thermal evaporation. For the OFETs and inverter devices on PEN substrate (50 μm) (Goodfellow), 80 nm Al bottom electrodes were thermal evaporated through a mechanical shadow mask. Then the BST thin film

was prepared using the same procedure as that of the capacitor device on silicon. After BST was fabricated by UV-Ozone, 45 nm DNTT was also thermal evaporated through a mechanical shadow mask. At last 50nm top Ag drain and source electrodes are also thermal evaporated through shadow masks.

The bottom gate bottom OFET device was fabricated directly on UV-Ozone derived BST thin film with Si and evaporated Al working as gate electrode. Then the active layer of DNTT was thermal evaporation for DNTT devices. For TIPS-pentacene, it as grown by DPC method with TIPS-pentacene solution of 0.4 mg/ml of mixed solvent (m-xylene and carbon tetrachloride (CCl_4), volume ratio 1:1). The electrical performance of OFET devices on silicon substrate were measured in air atmosphere and that of the inverter devices was measured within a nitrogen glove box (H_2O, O_2<0.1 ppm). The contact angle was measured by 100SL contact angle meter of Sindatek company.

The interfaces play critical role in determining the morphology of the materials deposited on top of another, including interfaces of solid-solid and solid-liquid. For transistor devices studied in this thesis, they are all bottom gate top contact. In this case, the semiconductor will de deposited on top of BST dielectric, then the study of the BST surface energy will be critical in further studing the morphology of the semiconductor and the transistor devices performance.

Figure 5.3 (a) shows the contact angle of deionized water (DI water) and diiodomethane (DM) measured on 5 different BST thin film, including (i) fresh sample after UV-Ozone treatment, (ii) stored in ambient air for 5 hours and (iii) 2 days, (iv) stored in evaporation chamber for 5 hours to achieve a pressure of 1×10^{-6} torr and (v) stored in evaporation chamber for 24 hours. It can be noticed that the contact angle of DI water on fresh BST is 5^{o} while for the DM is 34^{o}. It suggests that the fresh deposited BST surface after UV-Ozone treatment is hydrophilic and have a high surface energy. By identifying the contact angles, the surface energy of the BST thin films stored under different environments are calculated by the well-established Wu (harmonic mean) method as follows:[112]

$$(b_1 + c_1 - a_1)\,\gamma_s^d\gamma_s^p + c_1(b_1 - a_1)\,\gamma_s^d + b_1(c_1 - a_1)\,\gamma_s^p - a_1 b_1 c_1 = 0 \qquad \text{Equation 5.1}$$

$$(b_2 + c_2 - a_2)\,\gamma_s^d\gamma_s^p + c_2(b_2 - a_2)\,\gamma_s^d + b_2(c_2 - a_2)\,\gamma_s^p - a_2 b_2 c_2 = 0 \qquad \text{Equation 5.2}$$

where $a_1 = \frac{1}{4}\gamma_{l,1}(\cos\theta_1 + 1)$, $b_1 = \gamma_{l,1}^d$, $c_1 = \gamma_{l,1}^p$ in Equation 5.1 and $a_2 = \frac{1}{4}\gamma_{l,2}(\cos\theta_2 + 1)$, $b_2 = \gamma_{l,2}^d$, $c_2 = \gamma_{l,2}^p$ in Equation 5.2. The subscript 1 and 2 represents the two liquid used deionized water and diiodomethane. γ_s^d, γ_s^p and γ_s represent the dispersion, polar and total surface energy, respectively. The subscripts s and l represents solid and liquid, respectively. The surface energy of five different BST thin films (shown in Table 5.1) can be obtained by measuring contact angles of two different solvent, polar term dominationg (DI water) and dispersion term dominating one (DM), respectively. The surface energy of the freshly formed BST thin film

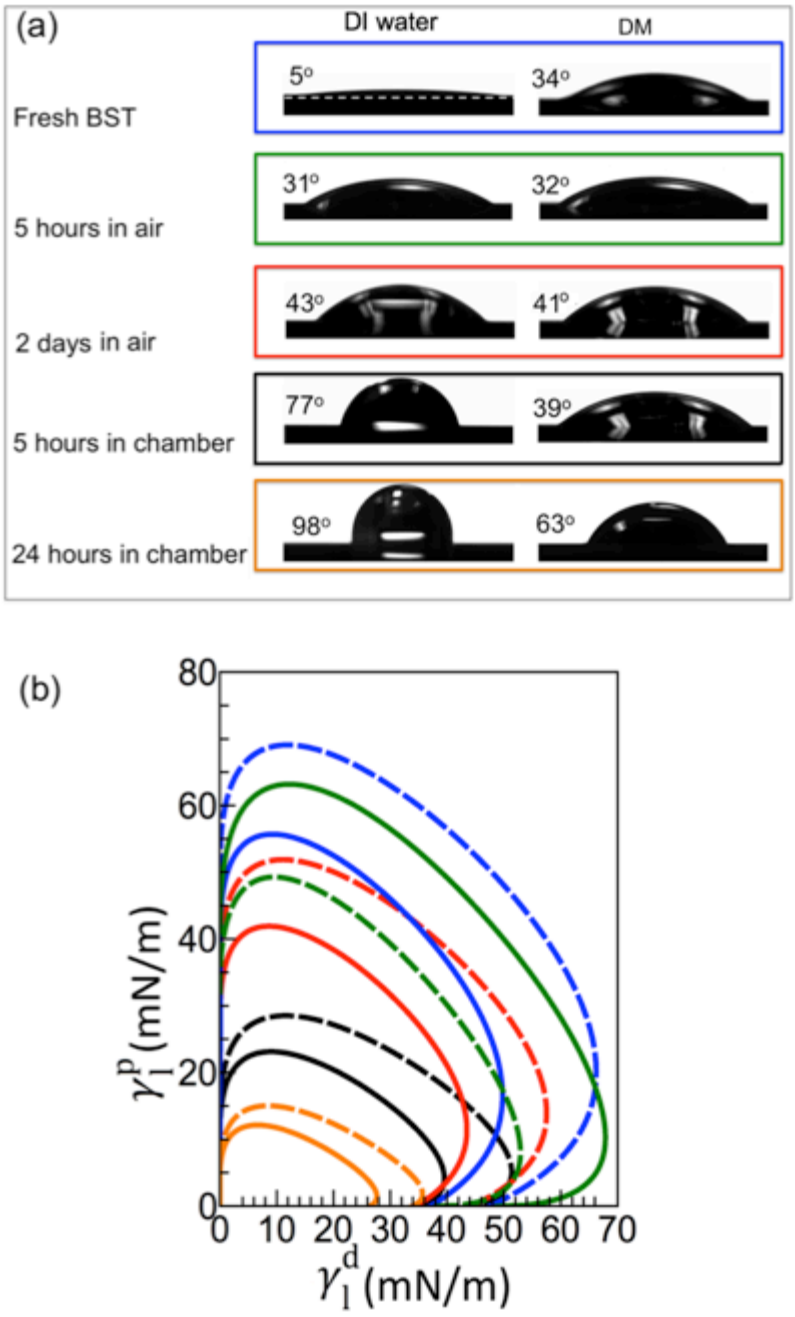

Figure 5.3 The contact angles of BST thin films under different treatment with DI and DM as probing solvent. (b) Wetting envelope of BST thin films stored under different conditions and time (the color is corresponding to the rectangular shown in (a) with contact angle = 0^o (solid lines) and 40^o (dashed lines), respectively.

Table 5.1 Surface energy of the BST thin films under different storage conditions

Different samples	Surface energy (dispersion term) γ_s^d(mJ/m^2)	Surface energy (polar term) γ_s^p (mJ/m^2)	Total surface energy $\gamma_s = \gamma_s^d + \gamma_s^p$(mJ/m^2)
Fresh BST	37.21	39.82	77.03
5hours in air	38.05	32.10	70.15
2 days in air	34.51	27.62	62.13
5 hours in chamber	36.10	10.15	46.25
24 hours in chamber	26.42	3.59	30.01

(77.03 mJ/m^2) changed rapidly after exposed to ambient air. It dropped to a value of 70.15 mJ/m^2 and 62.13 mJ/m^2 after in stored in ambient air for 5 hours and 2 days, respectively. On the other hand, keeping the samples in the evaporation chamber, we also noticed a drop of the surface energy from 46.25 mJ/m^2 to 30.01 mJ/m^2 while increasing the storage time 5 hours to 24 hours. It is believed that the fresh BST surface with high energy would adsorb organic materials or other low surface energy contaminants in the ambient air or evaporation chamber and result in a decrease of the surface energy.[115]From the X-ray photoelectron spectroscopy (XPS) results shown in the Figure 5.4 and Figure 5.5, a significant rise of the peak around 286eV (C1s) in the sample stored in the chamber for five hours. It suggests the decreases of the BST surface energy is related to the adventitious carbon from the environment. The reduction of the BST surface energy after stored in the chamber can be recovered by

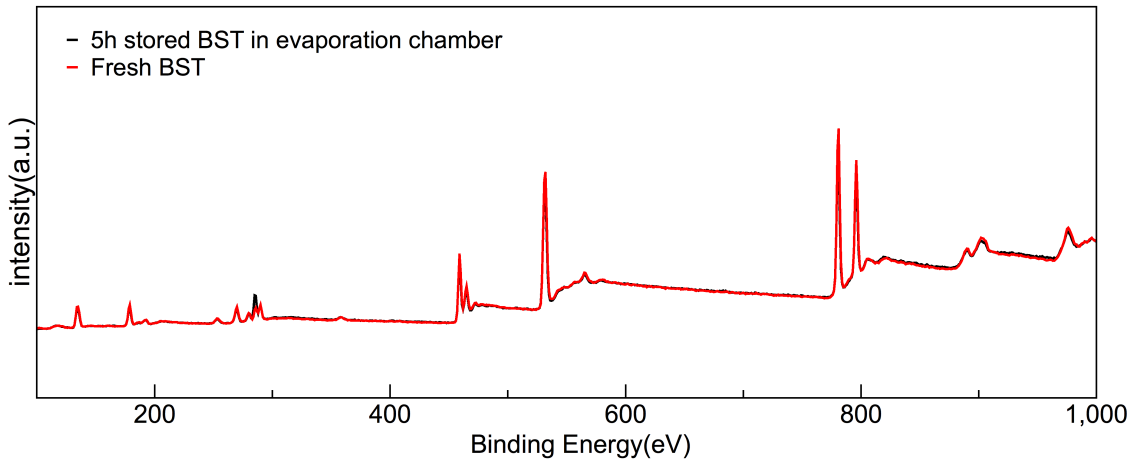

Figure 5.4 The survey scan of the BST fresh thin film (red line) and 5 hours stored in the evaporation chamber (black line).

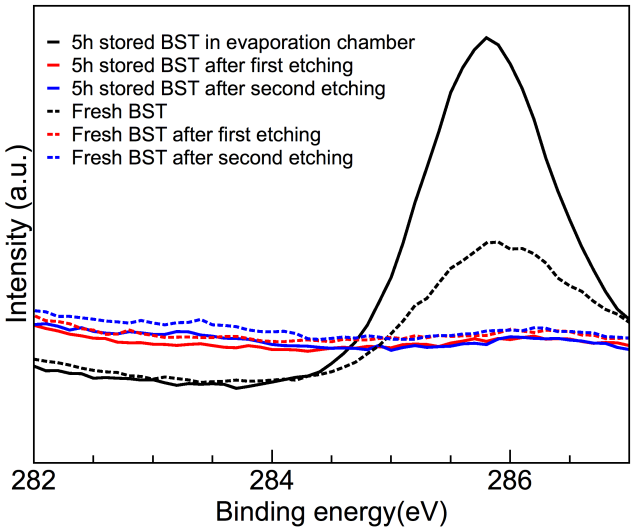

Figure 5.5. Zoom in of the XPS results at the C1s peak of the (i) 5h stored BST thin film in thermal evaporation chamber (solid black curve), (ii) 5h stored BST after first etching for around 5nm by Argon ion (solid red curve), (iii) 5h stored BST after first etching (around 5 nm) by Argon ion (solid blue curve). (iv) The XPS results of the fresh BST thin film (dotted black curve), (v) after first etching (dotted red curve) and (vi) second etching (dotted blue curve) are also shown.

performing 10 minutes UV-Ozone treatment again (see Figure 5.6). It suggests that the decrease of surface energy by adventitious on top of BST is reversible.

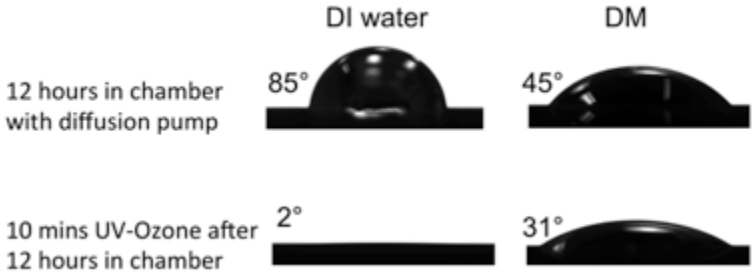

Figure 5.6 The contact angle of BST stored in chamber for 12h and UV-Ozone treated for 10min.

5.1.2 OFETs performance on BST of different surface energy

5.1.2.1 OFETs with solution processed organic semiconductor

With the surface energy tunable BST thin films, two different organic depositon methods are investigate on top of BST surfaces. From contact angle and wetting envelope of the BST film, as shown in Figure 5.3, it has been proved that the fresh BST right after UV-Ozone treatment is suitable for solution procesing. Here, for a instance, TIPS-pentacne OFETs are fabricated on top of fresh BST. In here, we employed a mixed solvent (m-xylene) and carbon tetrachloride (CCl_4) with a volume ratio 1:1 to form the TIPS-pentacene (0.4 mg mL^{-1}) solution.[21, 22] The solution is completely wetted on the BST surface and no contact angle can be measured due to the low surface tension of the solvents (see Figure 5.7). For the OFET device fabrication, TIPS-pentacene solution is deposited on BST dielectric by the DPC method as mentioned in Ref. [21] and [22]. The typical optical image of TIPS-pentacene ribbon crystals are shown as Figure 5.8. Figure 5.9 shows the zoomed in optical image of TIPS-pentacene cystals. The output and transfer curves of a representative TIPS-pentacene OFET device are shown in Figure 5.10 (a) and (b). It can be noticed that hysteresis effect is minor in the current devices. With the high-*k* BST, the operating voltage in only -2V. To get an accurate analysis that how good is the averaged performance and how aobut the repeatability. 20 OFETs on the same piece of substrate and the same BST thin film were fabricated. To realize that, highly packed mechanical shadow masks are designed and fabricated, with drain andsource electrods

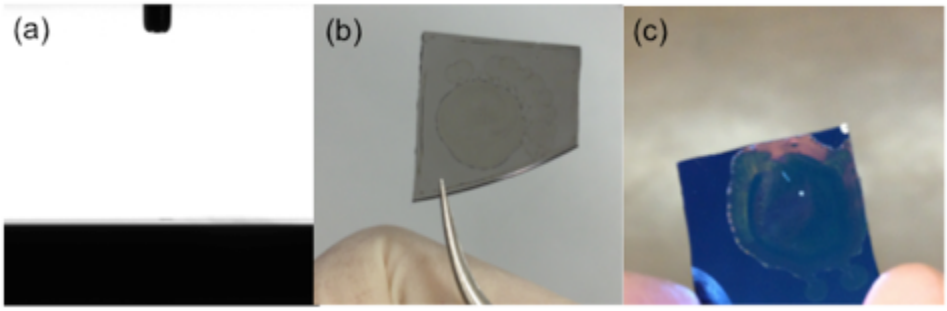

Figure 5.7 (a) No contact angle of TIPS-pentacene on top of fresh BST after UV-Ozone treatment can be tested. (b) Photo of TIPS-pentacene drop on top of BST which is spin-coated and UV-Ozone treated on n++ Si substrate. (c) Photo of TIPS-pentacene drop on top of BST which is spin-coated and UV-Ozone treated on top of SiO_2 for easier observation.

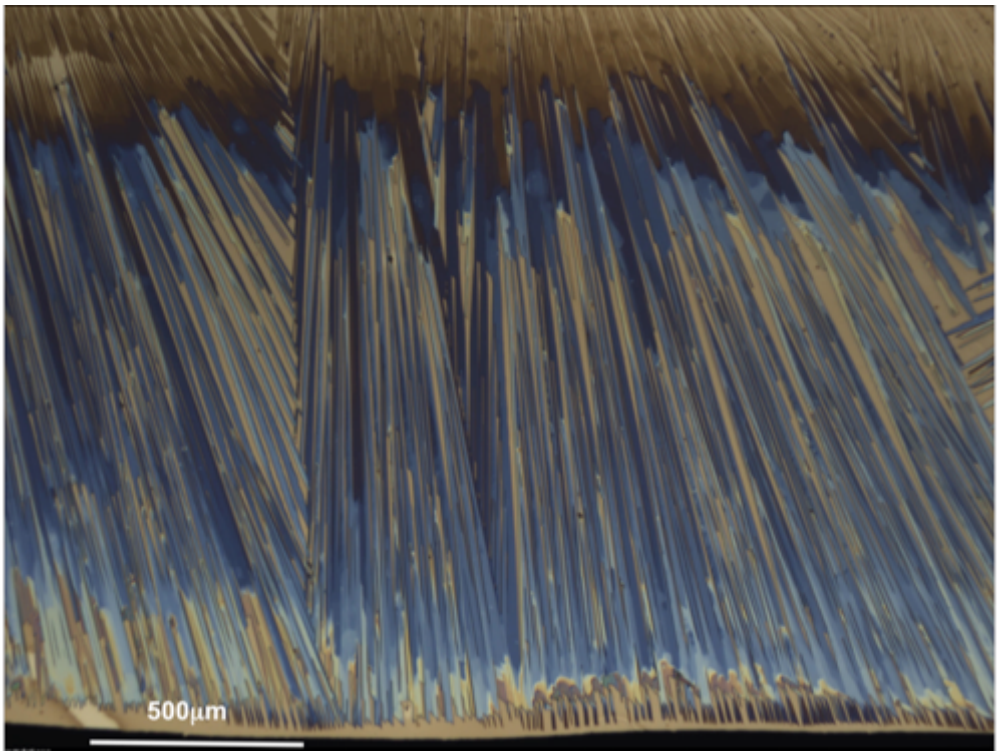

Figure 5.8 Typical TIPS-pentacene ribbon crystals at one edge of pinner

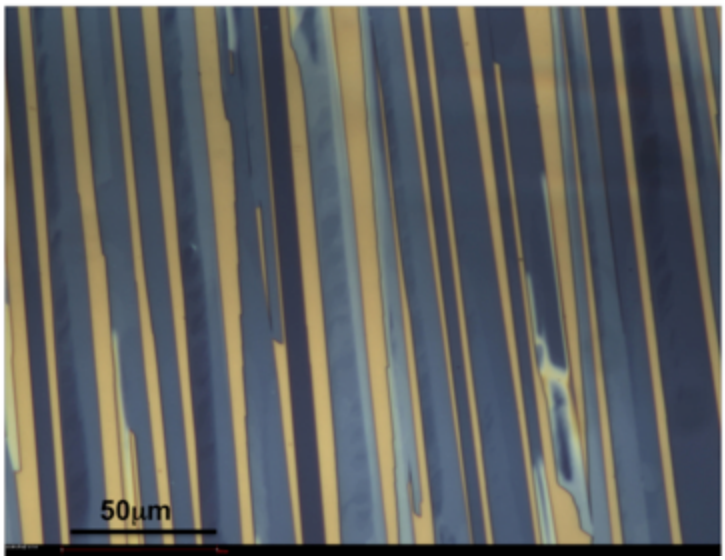

Figure 5.9 Zoomed in optical image of TIPS-pentacene crystals

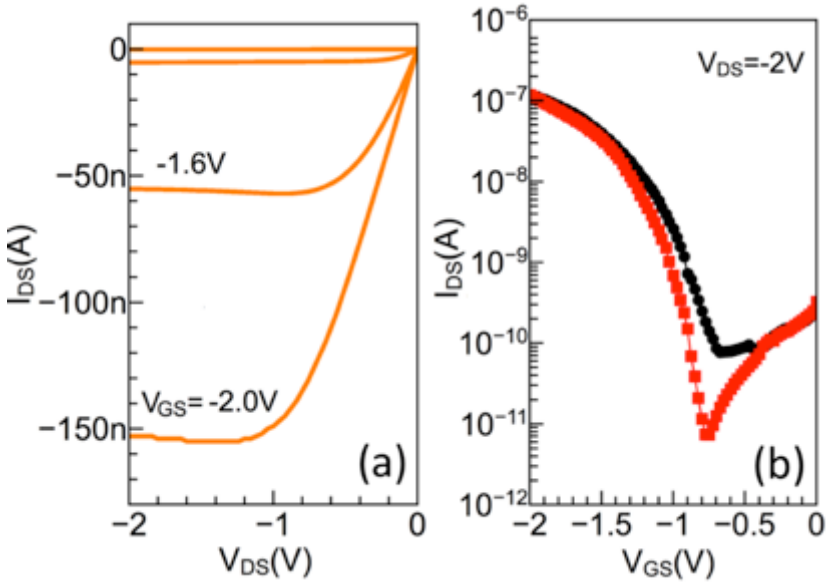

Figure 5.10 (a) Output curves for one representative TIPS-pentacene transistor device,

(b) The corresponding transfer curves of the device shown in (a).

area is only 450μm×500μmwith channel length of 50μm and W/L=10, as shown in Figure 5.11. The transfer curves of all 20 devices are shown in Figure 5.12(c). The mobility has been corrected after considering the TIPS-pentacene coverage area in the channel and the mobility histogram of the 20 devices is shown in Figure 5.12 (d). The averaged carrier mobility is 0.11 $cm^2 V^{-1}s^{-1}$ and on/off ratio is 3.76×10^4. The relatively low carrier mobility in the current OFETs is also related to

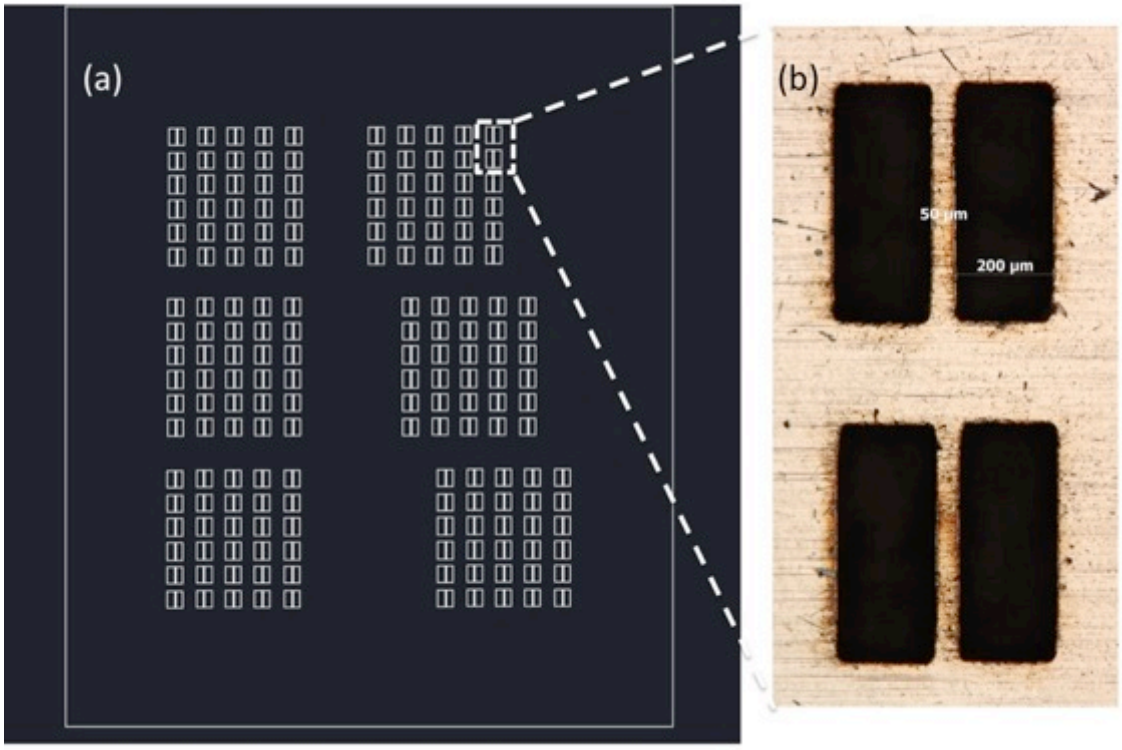

Figure 5.11 (a) The design drawing by Auto-CAD of the shadow masks for statistic study; (b) Optical images of drain and source for single devices.

the unstrained crystal structure of the TIPS-pentacene (the π-π stacking distance cannot be reduced) and the strong surface polarization effect in the high-*k* dielectric.[52, 116, 117]

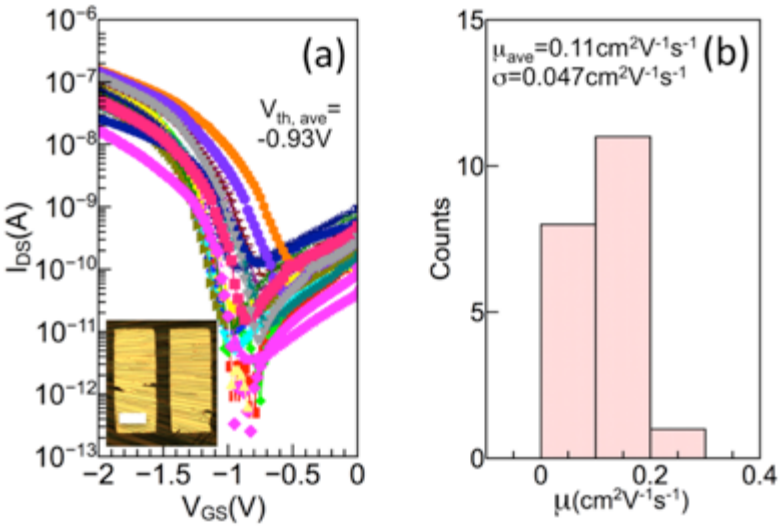

Figure 5.12 (c) Transfer curves of 20 TIPS-pentacene OFETs devices (W/L=10) and the inset is the optical image of one typical transistor device with the scale bar = 100 μm. The averaged V_{th} of -0.93V is shown. (d)The statistic study of corrected mobility of 20 TIPS-pentacene device after considering the actual channel coverage area.

5.1.2.2 OFETs with thermal evaporated organic semiconductor

Different from solution processing, physical depositing methods, like thermal evaporated, the quality and the growth mode of the organic thin film is usually governed by the work of adhesion (*W*) between the dielectric surface and the deposited

organic materials rather than wetting envelope. To get the work of adhesion between the gate dielectric and the semiconductor, surface energies of both of them are needed. The surface energies of BST thin films have been measured and summarized in Figure 5.3 and Table 5.1. The surface energy of DNTT as the organic semiconductor used here can also be determined by measuring the contact angle on top with two solvtens. The contact angle resutls and the surface energy are shown in Figure 5.13 and Table 5.2.

In general, if the work of adhesion is at least two times larger than the organic semiconductor surface energy, i.e. $W_{ad} > 2\gamma$, the thin film will grow in layer-by-layer (F-M Mode). On the other hand, if $W_{ad} < 2\gamma$, the film will grow in small islands Volmer-Weber Mode.[48] The growth mode of the thermal evaporated organic molecules would directly affect overall performance of the OFETs especially the carrier mobility. The layer-by-layer growth mode usually results in large and dendritic grains, while the island mode growth can provide a higher packing density it the first

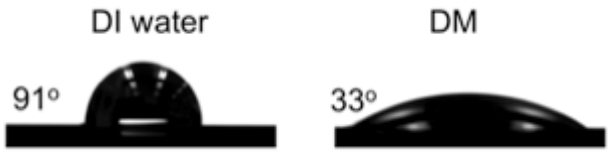

Figure 5.13 Contact angle of deionized water (DI) and diiodomethane (DM) on top of 45 nm DNTT deposited on BST under pressure of 10^{-6} Torr

Table 5.2 Surface energy of 45nm DNTT evaporated on BST after 5 hours pump down in evaporation chamber under pressure of 10^{-6} Torr

Sample	Surface energy (dispersion term) γ_s^d(mJ/m^2)	Surface energy (polar term) γ_s^p (mJ/m^2)	Total surface energy $\gamma_s = \gamma_s^d + \gamma_s^p$(mJ/m^2)
DNTT	40.15	3.72	43.87

few monolayers of organic semiconductors. The work adhesion of the DNTT thin film and the BST sample loaded into the evaporation chamber 5 hours is evaluated by:[48]

$$W_{\mathrm{DB}} = 4\left[\frac{\gamma_D^p \gamma_B^p}{\gamma_D^p + \gamma_B^p} + \frac{\gamma_D^d \gamma_B^d}{\gamma_D^d + \gamma_B^d}\right] \qquad \text{Equation 5.3}$$

where the superscripts *d* and *p* represent the dispersion and polar components of the surface energy, respectively. Subscripts *D* and *B* stand for DNTT and BST, respectively. By using the DNTT surface energy of 43.87 mJ/m^2 (γ_D^d =40.15 mJ/m^2, γ_D^p =3.72 mJ/m^2) (see for contact angle of both DI and DM on top of DNTT), the work of adhesion between the thermal evaporated DNTT and the BST is 86.8 mJ/m^2. Thus, it is expected that the DNTT grown on the BST would have the island structures with certain layer-by-layer properties because the W_{ad} is comparable with 2γ (see Figure 5.14). The black curve in the figure is for the critical value of $W_{\mathrm{DB}} = 2(\gamma_D^{\mathrm{d}} + \gamma_D^p)$. To

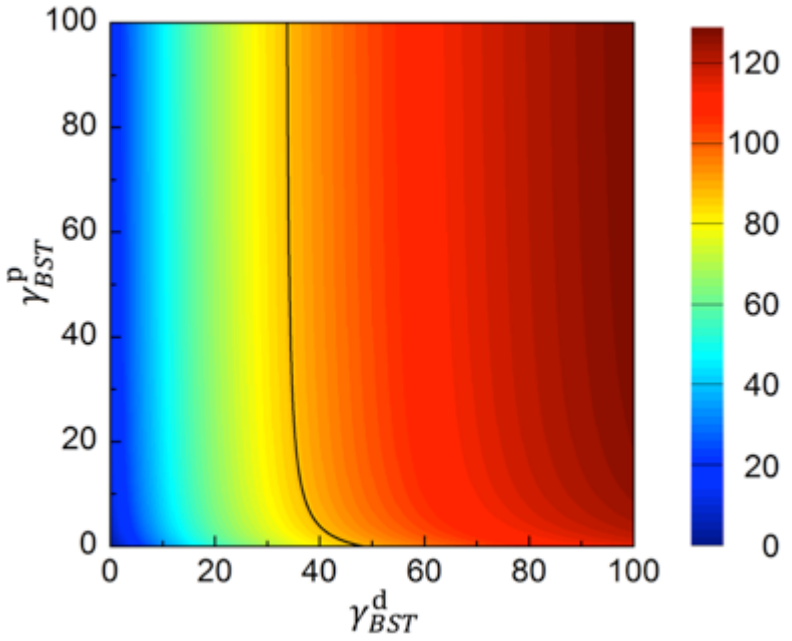

Figure 5.14 The Work of adhesion between DNTT and BST as a function of both dispersion and polar term of BST surface energy based on Equation 5.3

the left of the black curve, island growth mode of DNTT and to the right, layer by layer growth mode is expected, respectively.

To confirm that the work of adhesion will determine the morphlogy of DNTT on top of BST and the performance of OFET furthur, two sets of experiments are designed by storing BST thin film in the evaporation chamber for different times, 5 hours and 24 hours, respectively. Figure 5.15 (a) shows the AFM surface morphology of the thermal evaporated DNTT film on BST thin film stored in chamber for 5 hours, from which both island and layer structure can be observed and the average grain size is around

500nm. In the magnified AFM image in Figure 5.15 (b), layer-by-layer stacks can be observed on the upper part of the islands with a step height of around 2nm. When the storage time in evporation chamber is extended to 24 hours, the further reduction in the surface energy would result in smaller grain size of DNTT crystals as shown in the Figure 5.16 (a), where island structures can be clearly observed. From the zoomed in figure in Figure 5.16 (b), the averaged grain size is about 200nm and no obvious layer-by-layer structure can be observed. OFETs on Si are fabricated on top of the DNTT as shown in Figure 5.15 and Figure 5.16, respectively. The representative output and transfer characteristic curves of the DNTT transistors fabricated on BST under 5 hours and 24 hours of storage are shown in Figure 5.17 (a) and (b) and Figure 5.18(a) and (b) respectively. It can be seen that no significant hysteresis effect can be

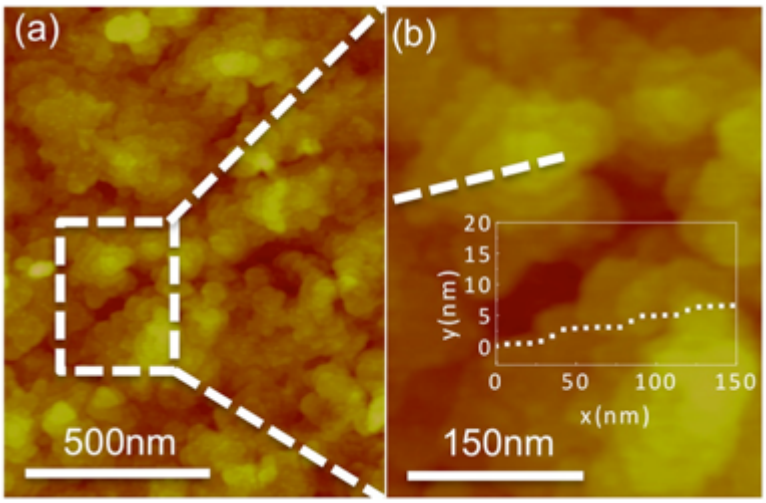

Figure 5.15 (a) AFM morphology of DNTT crystals on top of 5h stored BST. (b) The magnification image of DNTT crystal marked in (a). Inset is the step height of DNTT layers of one crystal island.

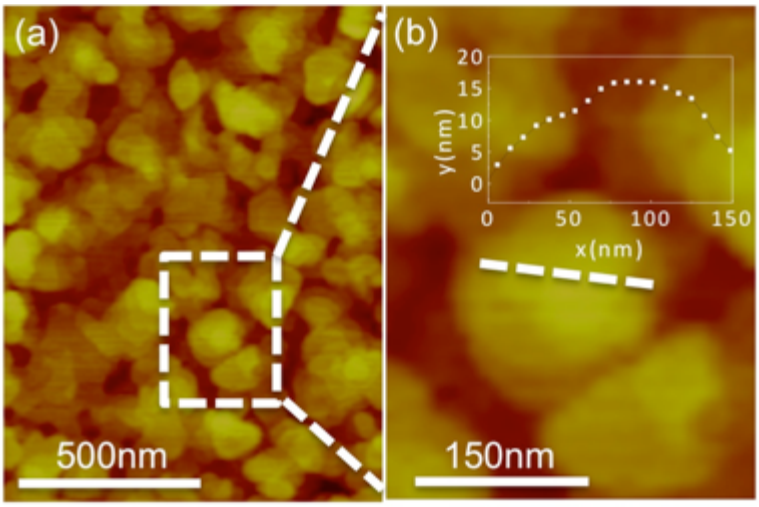

Figure 5.16 (a) AFM morphology of DNTT crystals on top of 24h stored BST. (b) The magnification image of DNTT crystal marked in (a).

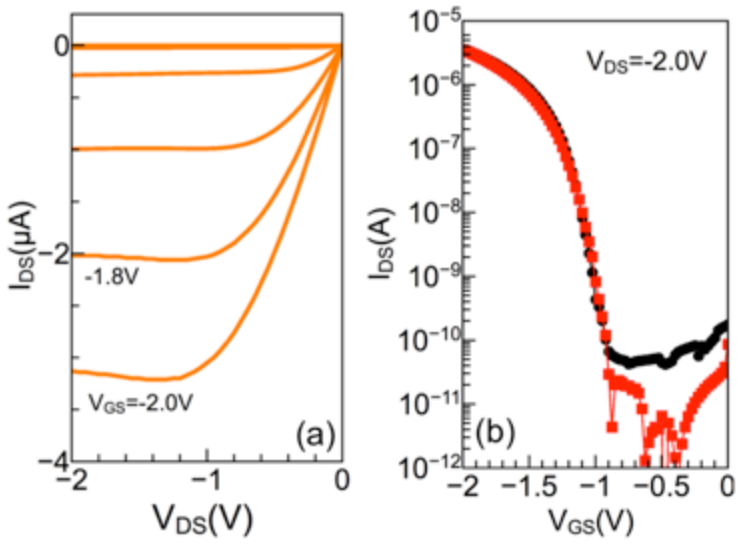

Figure 5.17 (a) Output curves of one representative OFET based on 5h stored BST. (b) The transfer curves of the same transistor device shown in (a).

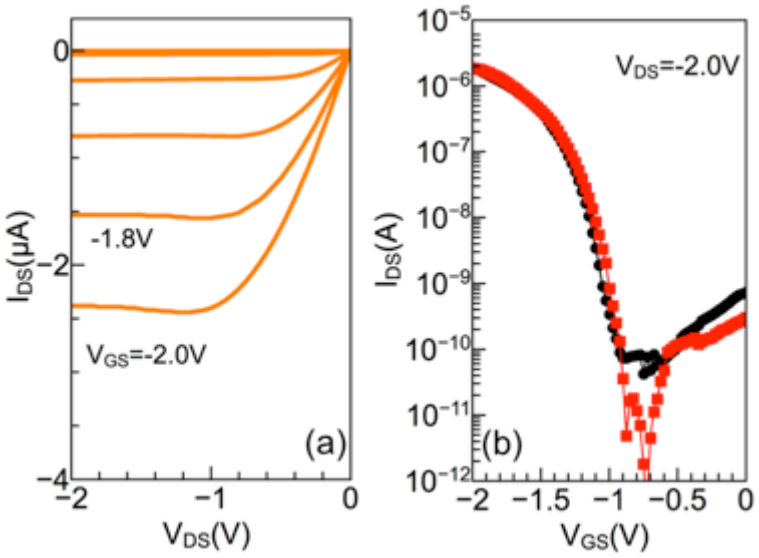

Figure 5.18 (a) The output and transfer of one representative OFET device based on 24h stored BST. (b) The corresponding transfer of the device shown in (a).

observed in both devices. Besides, the on current of device on BST of 5 hours storage is much higher, with the same geometry, which means the mobility is higher. The statistic studies of both 20 OFET devices based on 5h and 24h stored BST are shown in Figure 5.19 and Figure 5.20 to make fair and accurate comparsion of the performance. Transfer curves and mobility statistic are shown in Figure 5.19 and Figure 5.20 for OFETs on top of BST of 5 and 24 hours storage, respectively. From Figure 5.19, the averaged threshold of these two types of devices are -1.09 and -0.93V, respectively. From the statistic study of 20 OFET devices grown under these two conditions, we noticed the averaged saturation mobility of the larger grain size device

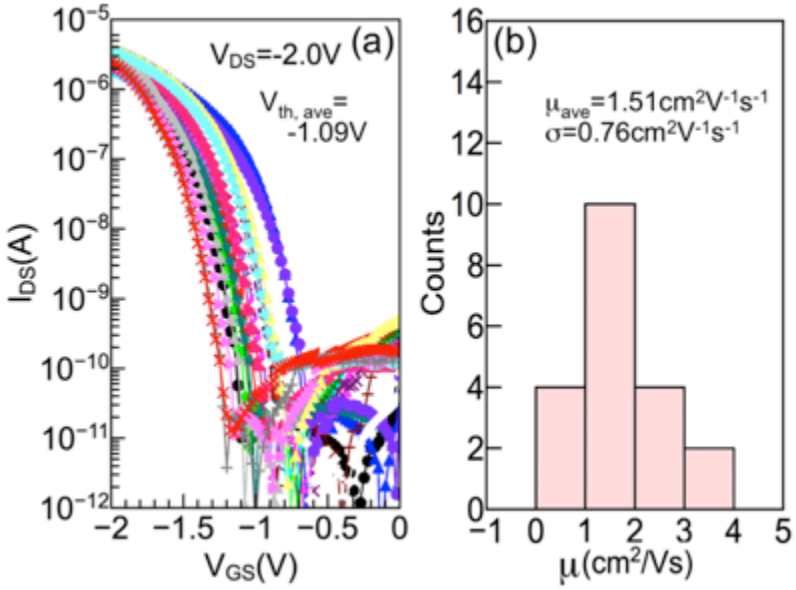

Figure 5.19 (a) All transfer curves of 20 transistor devices. The average threshold voltage $V_{th, ave}$ of -1.09V is shown. (b) shows the statistic of mobility of 20 devices. Average mobility m_{ave} of 1.51$cm^2V^{-1}s^{-1}$ and the standard derivation s is 0.76 $cm^2V^{-1}s^{-1}$.

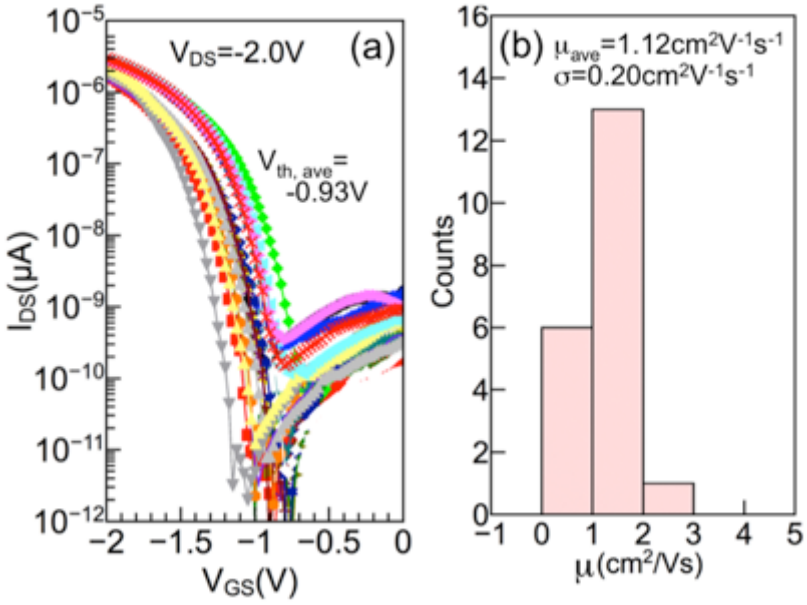

Figure 5.20 (a)All transfer curves of 20 transistor devices. The average threshold voltage $V_{th, ave}$ of -0.93V is shown. (b) shows the statistic of mobility of 20 devices shown in (a). Averaged mobility m_{ave} of 1.51$cm^2V^{-1}s^{-1}$ and the standard derivation is 0.20 $cm^2V^{-1}s^{-1}$.

is 1.51 $cm^2 V^{-1}s^{-1}$ while the small grain size device is decreased to 1.12$cm^2V^{-1}s^{-1}$. (Top source/drain contact OFETs have channel W/L ratio is equal to 20, the measured thickness and areal capacitance of the BST thin film are 36nm and 275nF/cm^2 respectively). Although the carrier mobility of the current DNTT device is promising, it is believed that mobility up to 2 $cm^2 V^{-1}s^{-1}$ or higher can be achieved by further device optimization.[31, 32, 118]

To further investigate the DNTT nature on the BST thin film, we employed XRD to investigate the crystal structure with both out of plane and in plane scanning. Figure 5.21 (a) shows the out of plan XRD pattern of the DNTT thin film and (b) shows the log scale of the intensity axis. From the log scale pattern, 6 diffractions peaks can be clearly observed and all are corresponding to the family of (00*l*) planes. The (001) peak located at around $2\theta=5.45^o$ is narrow and the intensity is high, which suggests the DNTT crystals are of high quality in the *a*-*b* plane where charge transport occurs assuring high mobility. The d-spacing between lattice planes parallel to the substrate was calculated to be 1.62nm, which is quite close to the AFM step height obtained in the inset of Figure 5.15 (b) and agrees well with the result of DNTT single crystals

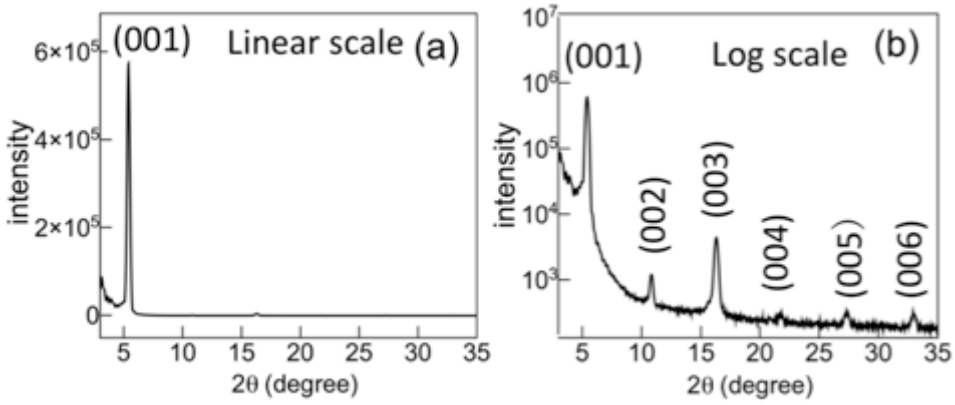

Figure 5.21 Out-of-plane XRD pattern (a) linear scale and (b) log scale of the DNTT thin film deposited on 5h stored BST by thermal evaporation.

result recently reported by Frisbie *et al.*[35]. Figure 5.22 shows the in-plane diffraction pattern of DNTT thin film. Three diffraction peaks correspond to the (110), (020) and (120) lattice planes of DNTT can be observed which suggests these sets of lattice planes are not parallel to each other and the DNTT thin film is in polycrystalline structure. DNTT has been previously shown to have excellent thermal stability and air stability, [37]the current high carrier mobility of the DNTT thin film transistor on the BST with no SAM treatment can further simplify the device fabrication procedures and such that it could be applied in large area processing.

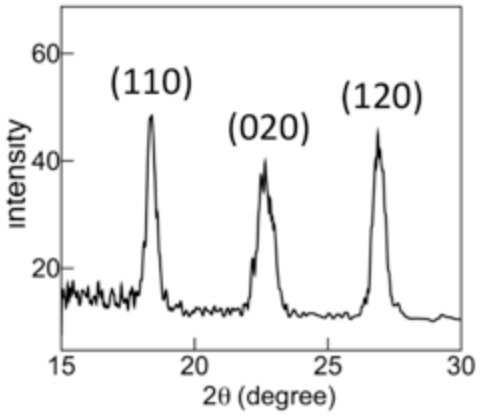

Figure 5.22 In-plane XRD of the DNTT thin film.

An additional advantage of BST thin film is the low processing temperature, which is compatible with flexible plastic substrates. To demonstrate the application of the BST in the flexible circuits, two working mode inverters: (i) saturated load; and (ii) depleted load based on two connected p-channel (DNTT) transistors were fabricated on 50 mm PEN substrate. Figure 5.23 (a), (b) and (c) are the schematic diagram, optical image and logic circuit of the saturated load inverter device, respectively. As shown in (b), the drain and gate electrodes of the OFET device with W/L=10 are connected together and function as a saturated load resistor with low resistance. The output and transfer curves of the driver transistor with W/L=40 are shown in Figure 5.24 (a) and (b), respectively. On the PEN substrate with 80nm of thermal evaporated Al and 36nm of BST dielectric, the field effect mobility is $1.6 cm^2V^{-1}s^{-1}$， with an on/off ratio of 4.36×10^5. Figure 5.25 (a) shows the V_{out} versus V_{in} and (b) shows the inverter gain

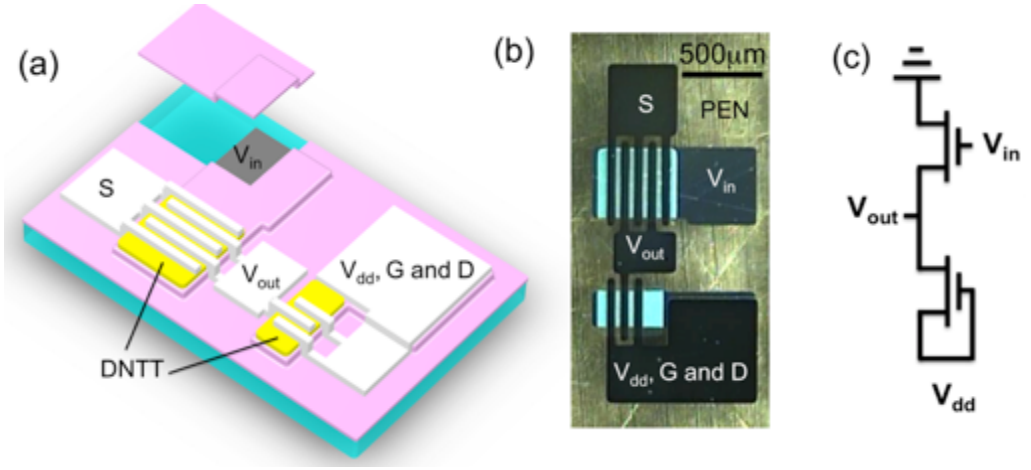

Figure 5.23 (a) Schematic structure of the saturated load inverter device. (b) The corresponding optical image with terminals marked. The W/L for the driver transistor is 40 and 10 for the saturated load transistor. (c) The corresponding logic circuit of the saturated load inverter.

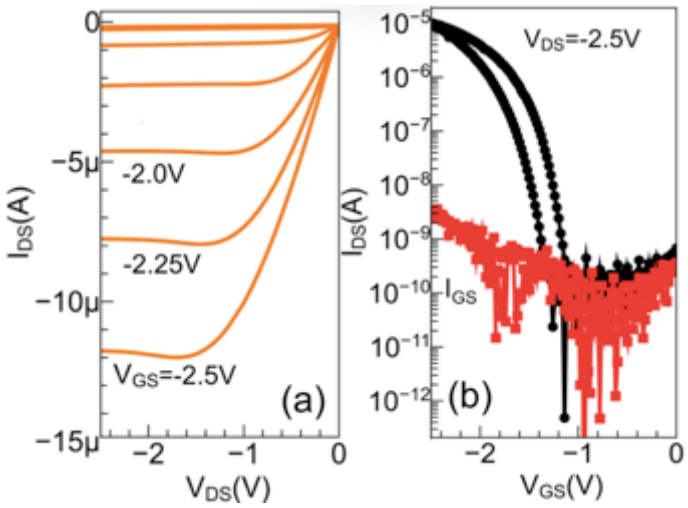

Figure 5.24 (a) Output and (b) transfer curves of the driver transistor of the inverter device. The sub-threshold swing (SS) and V_{th} of the transistor are 100mV and -1.68V.

versus V_{in} of the saturated load inverter. The inverter shows excellent full-swing inverting performance and V_{out} equals to V_{dd} when the V_{in} of driver transistor is off. The gain is around 25 at V_{dd} of -2V.

In the depleted load inverter, we used the transistor with W/L equals to 10 as the driver and the connection configuration is shown in Figure 5.26(a), (b) and (c). The

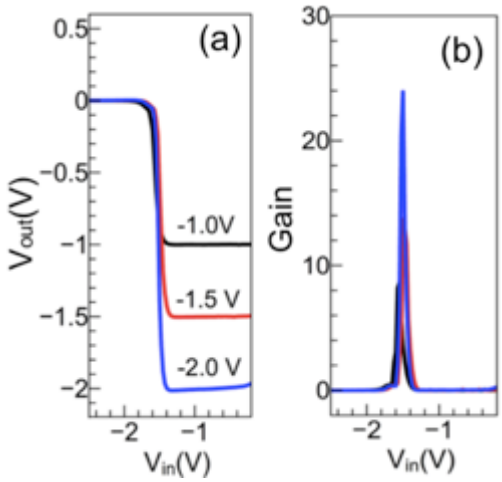

Figure 5.25 (a) V_{out} versus V_{in} of the depleted inverter. (b) Gain versus V_{in} for saturated inverters.

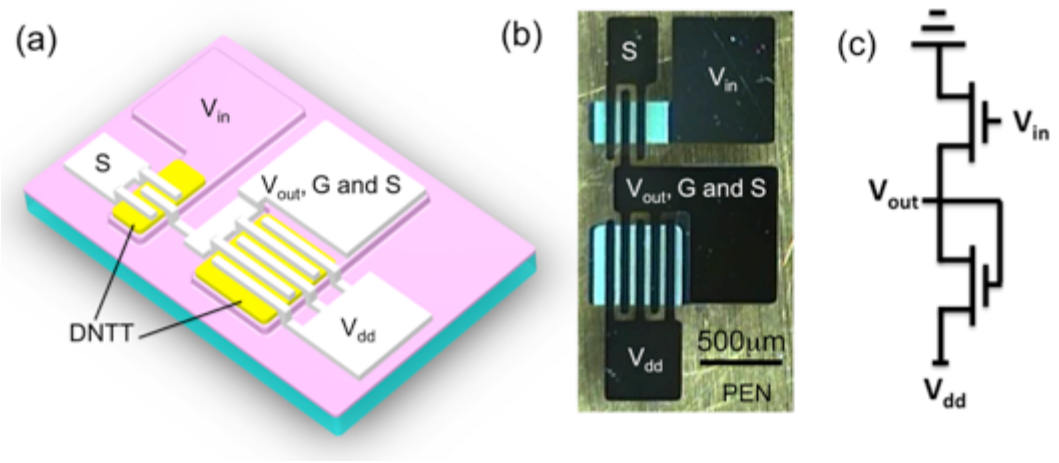

Figure 5.26 (a) Schematic structure of the depleted load inverter device. (b) The corresponding optical image with terminals marked. The W/L for the driver transistor is 10 and 40 for the saturated load transistor. (c) The corresponding logic circuit of the depleted load inverter.

source and gate electrode of the transistor with W/L equals to 40 are connected together and functions as a resistor with high resistance. The carrier mobility and the on/off ratio of the driver transistor with W/L of 10 are 1.55cm^2 V^{-1}s^{-1} and 8.63×10^5 (see Figure 5.27(a) and (b)). As expected, the depleted inverter performance is not as good as the saturated load inverter due to the large resistance of the load, shown in Figure 5.28. Based on the current W/L ratios of the driver, the resistance ratio between the driver transistor and the depleted load transistor is 4:1 and V_{out} would be just 80% of V_{dd} when the driver transistor is at off state (V_{in}=0V). It also explains the lower gain in the depletion load inverter.

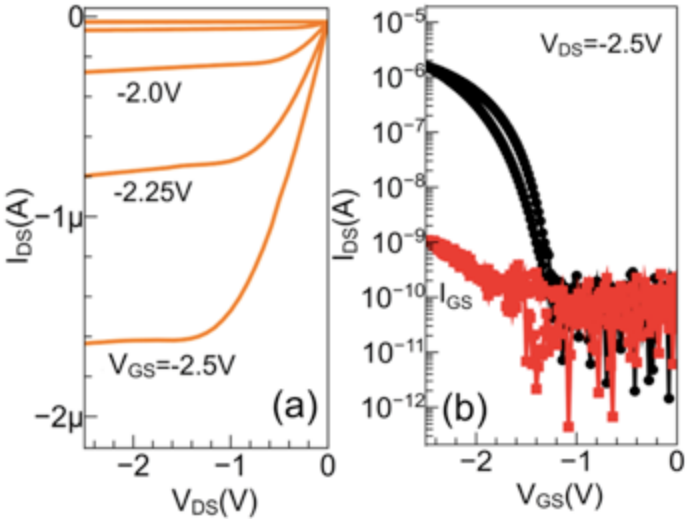

Figure 5.27 (a) Output and (b) transfer curves of the driver transistor of the inverter device.

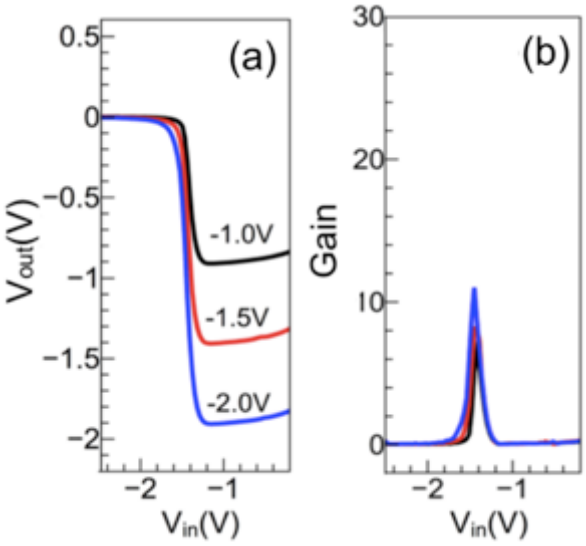

Figure 5.28 (c) V_{out} versus V_{in} of the depleted inverter. (d) Gain versus V_{in} for depleted inverters.

5.2 Summary

In summary, we studied the surface energy variation in the UV-Ozone treated metal oxide high-*k* thin film. The variation of the surface energy and thus the contact angle allows the high-*k* dielectric materials to be used in OFETs fabricated by solution processing as well as thermal evaporation. By loading the samples into the evaporation chamber for 5 hours and 24h, the work of adhesion between the BST and DNTT are around 86.8 and 71.02 mJ/m^2, respectively. This results in different growth mode of the DNTT, which gives different OFET device performance. The OFET devices based on 5h stored BST show higher average mobility of $1.51 cm^2V^{-1}s^{-1}$ than that of $1.12 cm^2V^{-1}s^{-1}$ of OFET devices based on 24h stored BST. The peaks in the out of plane and in-plane XRD results suggest the polycrystalline structure in the DNTT film and layer structure can also be observed in the island mode growth DNTT. We also fabricated saturated load and depleted load inverters based on the DNTT OFETs with different W/L ratio. The saturated load one shows full-swing performance and shows a high gain as 25. On fresh BST, TIPS-pentacene OFET devices are fabricated by DPC method and the averaged mobility is $0.11 cm^2V^{-1}s^{-1}$.

Chapter 6. Conclusion and future work

6.1 Conclusion

Low operating voltage OFET are highly needed in both scitific and industry fields. Gate dielectric is the key element in the OFET to determine the operaing voltage of the devices. There have been a lot of solutions for the low operating voltage, including high-*k* inorganic dielectric, high-*k* polymer dielectric and ultrathin inorganic dielectric with SAMs. This thesis mentioned many reported materials and summarized existing problems, like high temperature for inorganic ones, sensitivity to air and water of polymer ones and surface specific of the ultra oxide with SAMs.

In this thesis, two kinds of BST high-*k* gate dielectric materaial are proposed and studied in detail, including PLD and sol-gel with UV-Ozone. $Ba_{0.7}Sr_{0.3}TiO_3$ (BST-PLD) thin films of different thickness are deposited by the PLD at low temperature at 110^{o}C under vacuume environment. This is the lowest temperature of PLD applications for fabricating $Ba_xSr_{1-x}TiO_3$ family materails. The amorphous nature of the BST thin film was confirmed by TEM and XRD. This is also the first time amorphous BST-PLD thin film used for OFET application. OFETs devices based on BST-PLD thin films of different thin films are fabricated at the same. The key parameters are compared and the mobility is found to be higher with thicker BST-PLD thin film. The highest mobility 1.24$cm^2V^{-1}s^{-1}$ of OFET device based on 770nm BST-PLD film was obtained. Besides, the flexiblity of both the BST-PLD thin film and the OFET devices based on

BST-PLD. The dielectric performance of BST-PLD thin film kept stable till the bending radius down to 3mm. The mobility of the OFET device showed increase first and then decreae during downward bending and decrease during upward bending. The mobility can still maintain at around 0.5 $cm^2 V^{-1} s^{-1}$ or higher while the bending radius is around 3mm for both upward and downward bending tests.

To further meet the needs of low cost and large area applications, sol-gel processed and solidified by UV-Ozone $Ba_{0.62}Sr_{0.28}TiO_{3.03}$ (BST-UVO) was proposed. This thin film is deposited by spin coating with Ba-Sr-Ti sol solution and solidified with UV-Ozone at room temperature in ambient atmosphere. The tray inside the UV-Ozone chamber can be heated up to around 85^oC during the whole process, which is much lower than the Tg of almost all the commercial plastic substrates. OFETs on both Si and PEN substrates are fabricated based on BST-UVO thin film. The thickness of BST-UVO thin film was confirmed to be around 28nm, which is on top of SiO_2 or AlO_x ultra thin film derived by penetrated Ozone during the solidification process of BST-UVO on top. Pentacene OFETs on both Si and PEN substrates are fabricated. The mobility of OFET on Si and PEN substrate were 0.289 and 0.252$cm^2V^{-1}s^{-1}$. The mobility of pentacene with BST-UVO on PEN substrate was comparable with many reported values that based on solution processed high-*k* dielectric at much more high temperature.

Aside from the solution processed dielectric, this thesis make a step further to incorporate the BST-UVO with solution processed organic semiconductor. The surface

properties of BST-UVO thin films were studied in detail, including wetting envelop and work adhesion for solution processing and thermal evaporation applications, respectively. The contact angle of BST-UVO thin films stored in different enviroment and time were measured and the wetting envelops are plotted. It was found that the fresh BST-UVO of high surface energy is suitable for solution processing semiconductor on top of it. TIPS-pentacene OFETs are fabricated by DPC method, which is a brand new solution processing method. They showed averaged mobility of $0.11 cm^2V^{-1}s^{-1}$. Besides, after BST-UVO thin film is put into diffusion thermal diffusion chamber, the surface energy will decrease. And the longer it is stored in chamber, the smaller the surface energy will become. To investigate the effect of surfac energy of BST-UVO thin films on the morphology of the organic semiconductor deposited on top as well as the performance of the OFET devices, the BST-UVO thin films were loaded into the evaporation chamber for 5 hours and 24h. the work of adhesion between the BST and DNTT are around 86.8 and 71.02 mJ/m^2, respectively. This results in different growth mode of the DNTT, which gives different OFET device performance. The OFET devices based on 5h stored BST-UVO showed layer-island growth mode and higher average mobility of $1.51 cm^2V^{-1}s^{-1}$. The OFET devices based on 24h stored BST-UVO showed island growth mode and lower average mobility of that of $1.12 cm^2V^{-1}s^{-1}$. Two kinds of logic inverters consisting of two DNTT transistors are fabricated on PEN substrate. The saturated load one showed full-swing performance and shows a high gain as 25 and the depleted showed the gain of 12.

6.2 Future work

6.2.1 All solution process n-channel OFET devices

In the real application, complementary motal oxide semiconductor (CMOS), which operate with a high robustness, low power dissipation and a good noise margin, are dominating in the industry market. CMOS consist of silicon n and p channel transistors, which are not suitable for the large area and low cost applications, like flexible pressure sensors, memories, RFID, and display. [91-94] CMOS-like inverter devices based on OFETs are attracting great interests from the research communityand decent gain has been reported. [21, 119, 120] Li and coauthors have reported DPC method grown TIPS-pentacene and C_{60} single crystals and complementary inverters constructed with OFETs based on the these two kinds of crystals with decent gain of 155. That work demonstrated a solution processing method to study high performance complementary circuits. However, only devices based on Si substrate and SiO_2, which results in high operating voltage and limit the method in applications like flexible display or other portable applications.

This thesis has demonstrated OFET devices with solution processed BST-UVO high-*k* dielectric and TIPS-pentacene organic semiconductor active layer. The operating voltage is less than 3V, which is promising in realizing low operating voltage and all solution processed complementary circuits. C_{60} has also been proposed to be precessible by DPC method. Then the n channel (C_{60}) OFET device is the first step to

get fully solution processed COMS. The prelimitary result is shown in Figure 6.1. Further optimization is needed and the ultimate goal is to realize high performance low operating voltage all solution processed complementary circuit.

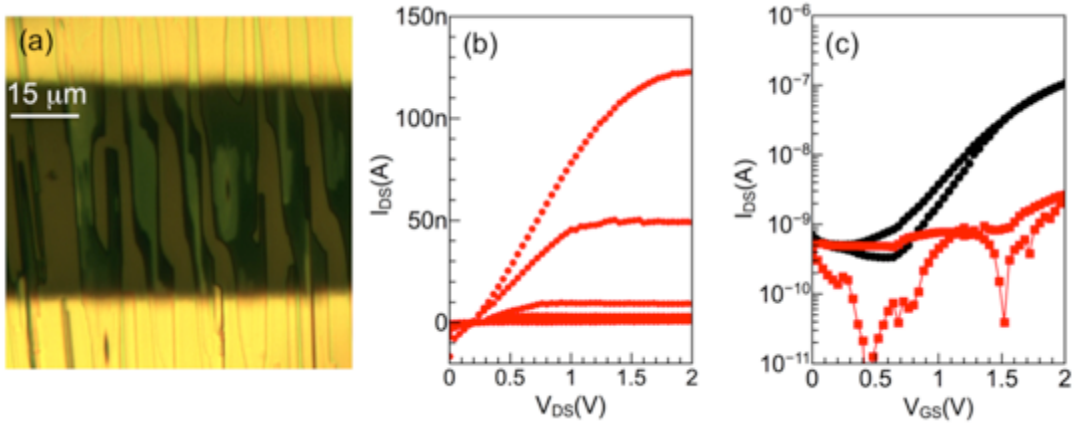

Figure 6.1 (a) Optical microscope of OFET device with C_{60} ribbon crystals. (b) The output of C_{60} OFET device shown in (a). (c)The corresponding transfer curve of (a).The device shows a mobiltiy of 0.07$cm^2V^{-1}s^{-1}$ after considering the crystal coverage area in the channel region.

6.2.2 Low operating voltage pressure sensor based on bilayers of high-*k* and the low-*k*

Due to many merits of OFET, it has attracted intense attention for its wide promising applications, including paper-like displays or e-paper, in which electric inks or other media are driven by organic transistor active matrix, [121] radio frequency identification tags, [122] sensors. [123-125]

Artificial intelligence has become a hot topic nowadays. To realize high sensitivity when it is directly contact with humans, high quality electric skin is highly needed. Besides, the production of electronic skin needs to be inexpensive and able to produce the skin with high throughput. In order to successfully mimic the properties of natural skin, Zhenan Bao group reported large arrays of pixel pressure sensors on flexible ITO/PET substrates.[3] The patterned silicon is used as the template to get the microstructured elastomennr polydimethylsiloxane (PDMS) thin film, which works as the pressure-sensitive dielectric thin films. For it has been reported that PDMS has good elastic properties, biomedical compliance with human tissue[126] and living cells [127] and high performance as a dielectric material in OFETs. [128]

Yet, the dielectric constant of PDMS is just around 3.0, then the operating voltage of the sensor based on the PDMS is very large, as high as 100V, as shown in Figure 6.2.

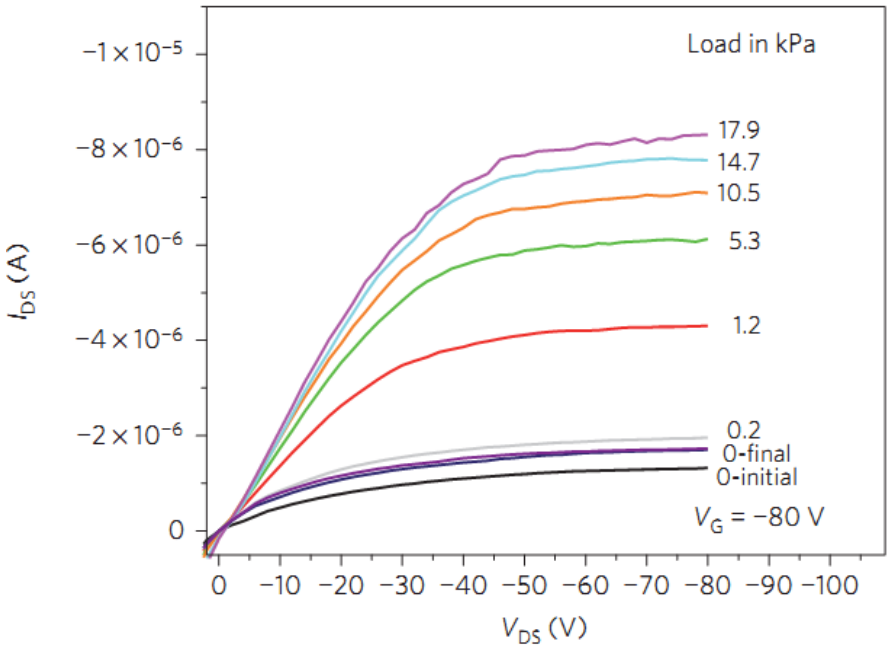

Figure 6.2 Output curves (I_{DS}-V_{DS}) of a transistor-based sensor with different external pressures applied. [3]

must be thick enough and occupies much larger portion in the whole dielectric thin film. And at the same time, the PDMS should not be too thin to eliminate pressure sensitive effect as a sensor of pressure. Then the optimized value of the fraction of BST thin film thickness in the whole dielectric part should be confirmed. The electric performance of the sensor based on the OFET fabricated on high-*k* BST thin film should be investigated also. Then low operating voltage single sensor device can be fabricated.

As discussed in sections above, it has been proved that the operating voltage can be decreased by the incorporation of high-*k* gate dielectric materials of OFET, then as well as the OFET based devices. The objective here is to incorporate the solution derived BST thin film as the gate dielectric layer and PDMS works as pressure sensitive dielectric. Then there will be two dielectric materials connected in series.

$$\frac{1}{C} = \frac{1}{C_B} + \frac{1}{C_P} \qquad \text{Equation 6.1}$$

$$C = \frac{\varepsilon_0 \varepsilon_e A}{(d_B + d_P)} \qquad \text{Equation 6.2}$$

$$\frac{d_B + d_P}{\varepsilon_e} = \frac{d_B}{\varepsilon_B} + \frac{d_P}{\varepsilon_P} \qquad \text{Equation 6.3}$$

$$\frac{1}{\varepsilon_e} = \frac{1}{\varepsilon_B} \cdot \frac{d_B}{d_B + d_P} + \frac{1}{\varepsilon_P} \cdot \frac{d_P}{d_B + d_P} \qquad \text{Equation 6.4}$$

Where B stands for BST and P for PDMS. When the two dielectric layers connected in series, the relationship between the effective capacitance and the effective is shown in Equations 6.1, 6.2, 6.3 and 6.4, It can be concluded from the equations that, to obtain high effective dielectric constant, the thickness ratio of high-*k* layer in the bilayer dielectric should be as large as possible. At the same time, the thickness of PDMS should be thick engouth to ensure the sensitivity.

To conlcude, for the bilayer structure of BST and PDMS, the thickness and other parameters should be optimized to get high sensitivity.

6.2.3 Low operating voltage pressure sensor high-k percolative composite thin film

Percolation effect has been proven to be effect in enhance the dielectric constant of the dielectric matrix. Conductive particles, carbon nanotubes and graphene dispersed in dielectric matrix have been proved to enhance the permittivity of the dielectric medium medium due to percolative behavior. Du and coauthors has proposed composite of PDMS with polypyrrole conductive nanowire, as shown in Figure 6.3. The composite with 5.3% volume ratio of conductive wire showed a dramatic increase of dielectric constant due to percolation effect. [129-132] The mearsure and the simulated dielectric performance of the composite with different volume ration of polypyrrole are shown in Figure 6.4 and Figure 6.5.

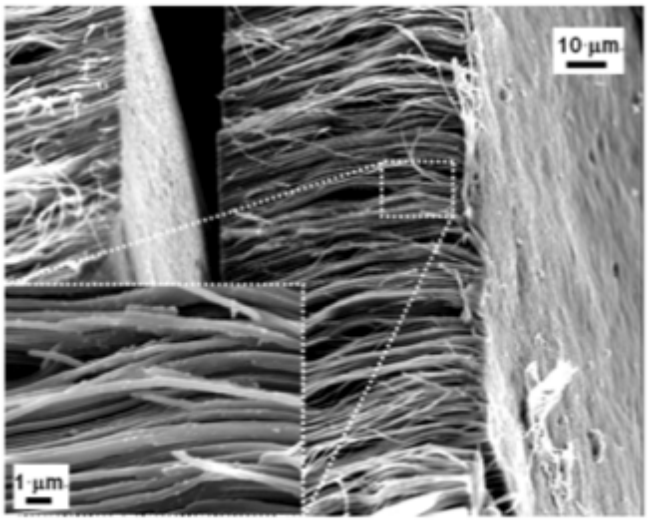

Figure 6.3 The SEM of polypyrrole nanowire[129]

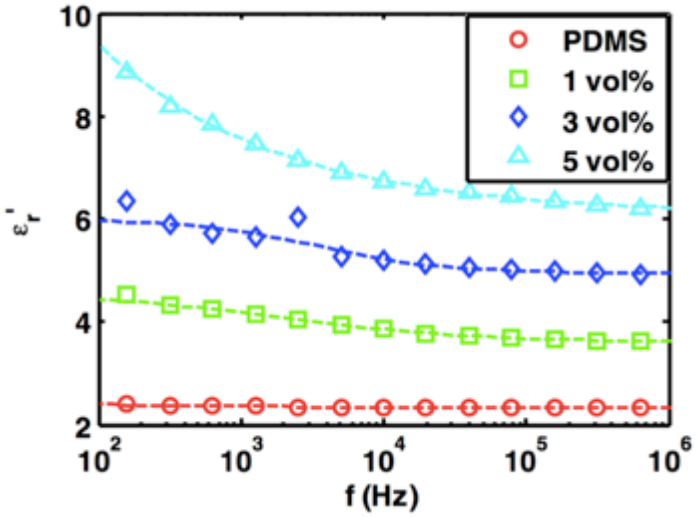

Figure 6.4 The measured dielectric constant real part of composite with different volume ratio of polypyrrole[129]

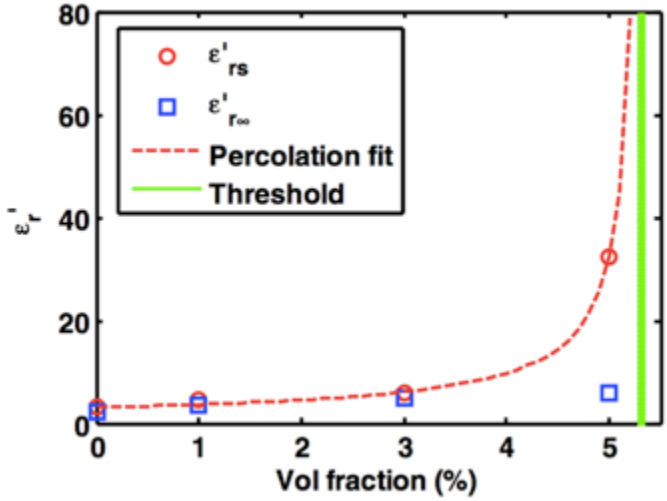

Figure 6.5 The measured dielectric constant real part of composite and the simulated curve with percolation theory[129]

This behavior can be described by the Equation 5.5.

$$\varepsilon_r = \varepsilon_0 \left| \frac{f_c - f}{f_c} \right|^{-q} \qquad \text{Equation 6.5}$$

where f_c is the percolation threshold, f is the volume fraction of conductive phase in the composite, ε_0 is the dielectric constant of the dielectric matrix, ε_r is dielectric constant of the composite, q is the critical exponent of the percolation system. The percolative composites are therefore promising candidates showing high dielectric constant which could be several orders higher than that of dielectric matrix when the volume ratio of conductive phase is appoaching the percolation threshold. [133, 134] The higher dielectric constant is obtained when the volume fraction of the conductive phase is getting closer to but does not exceed the percolation threshold. Since the existence of a large number of conductive particles or wires isolated by thin barriers of dielectric material in between, if the volume ratio of the conductive phase is large than the percolation threshold, leakage paths are likely for form and make the dielectric easily to break down. [134, 135]

Different conductive phase will be incorporated into PDMS and tuned the volume ratio to approach the percolation threshold to enhance the dielectric constant. Pressure sensors will be built on the percolative composite with PDMS as matrix, which works as both the dielectric and the pressure sensitive part. Low operating power of pressure sensor is expected.

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