LARGE-CONVERSION SWITCHED-CAPACITOR (SC) BASED DC-DC POWER CONVERTERS

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Large-Conversion Switched-Capacitor (SC) Based DC-DC Power Converters

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CERTIFICATE OF ORIGINALITY

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_____ (Signed)

Song XIONG (Name of Student)

To My Parents

Abstract

The increasing environmental concern on the green house gas generation and the continuous demand on increasing processing power of modern microprocessors have triggered the design of the central processing units toward a lower supply voltage down to the fundamental limit of semiconductor of less than 1 V to decrease power consumption and to increase the processing power by increasing the level of integration on semiconductors. However, the standard supply voltages are usually a multiple of 12 V. The performance of the traditional single-stage buck-based converter for the microprocessor at this large voltage gain (LVG) ratio becomes highly deteriorated. Efforts have been done to reduce the LVG ratio on the buck stage of the buck converter by utilizing the voltage step down characteristic of transformers and coupled inductors. However, transformers and inductors may decrease power density and incur additional loss on the overall buck converter. It has been demonstrated that for LVG power conversion, a two-stage converter can be better than a single-stage converter. The first-stage of the two-stage converter is a switched-capacitor (SC) converter which step down the input voltage to a "comfort" zone voltage of the second-stage traditional buck converter. The power saved by operating the second-stage buck converter at the comfort zone input voltage can be utilized for the first-stage SC converter for the voltage step down function. However, the optimization of this emerging two-stage SC-buck LVG ratio voltage converter is still in its infancy. Therefore, this thesis is intended to provide a systematic development on this LVG SC-buck converter.

The existing hybrid series-parallel SC-buck converter is studied in this thesis. The

parameters effecting the efficiency of this SC-buck converter are investigated. It is found that the optimization of this SC-buck converter can be done by selecting an appropriate stage number n, which is the number of flying capacitors of the series-parallel SC converter. The optimization of the SC-buck converter is continue by a newly proposed family of exponential SC (ESC) converter for the first stage SC converter, which can achieve LVG ratio with high efficiency and less number of switches. As this new ESC converter is topologically different from the previous SC converter, previous analytical calculation methods are found inadequate. An discrete-time analysis method is thus proposed to assist the property exploration of this newly proposed ESC converter. The analyses take into consideration of all practical parasitic circuit elements, including the electrostatic resistance of the capacitors for accurate calculation of the converter efficiency. The design is further optimized from the view of the number of energy flow which provides a high level systematic procedure for obtaining a better efficiency of the converter. All the theoretical findings in this thesis are verified with experimental measurements. The results obtained are used for the development of a design procedure for the LVG ESC power converter.

This thesis contains six chapters. The first chapter gives an introduction of the background and the literature review of converters for the LVG application and the type of step-down SC converter. The second chapter introduces the operating principles and provides information on SC converter, buck converter and two-stage converter. The following three chapters report the core results of the investigation of the SC-buck converters. The final chapter concludes this thesis and give some discusses on possible future works.

Publications

Journal Papers

1. S. Xiong, S.C. Wong, S.C. Tan and C.K. Tse, "A family of exponential step-down switched-capacitor converters and their applications in two-stage converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1870–1880, Apr. 2014.

2. S. Xiong, S.C. Tan and S.C. Wong, "Analysis and design of a high-voltage-gain hybrid switched-capacitor buck converter" *IEEE Transactions on Circuit and System I, Regular Papers*, vol. 59, no. 5, pp. 1132–1141, May. 2012.

3. S. Xiong, S.C. Wong, S.C. Tan and C.K. Tse, "Optimal design of a high efficiency ESC converter," *IEEE Transactions on Power Electronics*, submitted.

Conference Papers

1. S. Xiong, S.C. Wong and S.C. Tan "A series of exponential step-down switched-capacitor converters and their applications in two-stage converters," in *Proceedings of IEEE international Symposium on Circuits and Systems (ISCAS)*, pp. 701–704, May 2013, Beijing, China.

2. S. Xiong, S. C. Tan, and S. C. Wong, "Analysis of a high-voltage-gain hybrid

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Abbreviation List

Symbol	Description
LVG	Large-Voltage-Gain
SC	Switched Capacitor
IC	Integrated Circuit
VRM	Voltage Regulation Module
QSC	Quasi-Switched Capacitor
RMS	Root Mean Square
PFM	Pulse Frequency Modulation
PWM	Pulse Width Modulation
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistor
ESC	Exponential voltage step-down Switched Capacitor

Nomenclature List

Unless otherwise specified, some commonly-used symbols in the thesis are defined as follows.

Symbol	Description
D	Duty cycle
f_{s}	Switching frequency of a converter
T	Switching period of a converter
V_{in}, V_{o}	Input and output voltage of a converter
I_{in}, I_{o}	Input and output current of a converter
ΔI_{L}	The peak-to-peak current ripple of the inductor in Buck
P_{in}, P_{o}	Input and output power of a converter
R_{dson}	On resistance of a MOSFET
ESR	Equivalent series resistance in the circuit
η_{C}, η_{D}	Charging and discharging efficiency of series-parallel SC converter
η_1, η_2	The efficiency of first- and second-stage converter
η	Overall efficiency of a converter
(Φ_{10}, Φ_{11}) and (Φ_{20}, Φ_{21})	Two pairs of complementary PWM signals
F_{n}	Fibonacci numbers

Chapter 1

Introduction

1.1 Motivation

The supply voltage of modern microprocessors and ASIC chips is continuously reducing, targeting for lesser power dissipation and larger scale integration, to a level of less than 1 V [1]. The standard DC bus supply voltages are commonly 12 V, 24 V and 48 V. Large-voltage-gain (LVG) DC–DC converters stepping down from several tens of volts to less than 1 V for electronic product applications are therefore of high demand.

Buck-based step-down DC–DC converters are usually used in the industry as point-of-load converters, which are simple in structure and mature in control methods, for achieving the required voltage step-down conversion [2–5]. For applications in modern electronic devices, high power density and high efficiency are among the top considerations. Increasing the switching frequency is an effective way to reduce the size of bulky elements such as magnetic components and charge storage capacitors. However, the switching loss of the LVG buck converter increases dramatically due to the associated extreme small duty cycle $D = \frac{V_{\mathrm{o}}}{V_{\mathrm{in}}}$, which not only limits the switch-

ing frequency, but also complicates the implementation. Moreover, the extreme small duty cycle deteriorates the dynamic performance of the converter and further reduces its efficiency due to the very short on-time and very long freewheeling time within a switching cycle. The drawback can be readily observed from the efficiency versus input voltage curve, as shown in Fig. 1.1 of a buck converter available in the market, where the converter efficiency decreases rapidly with increasing input voltage. Converters with transformers would be a good choice to achieve LVG conversion. However, this decreases the power density and increases the cost, conflicting the requirement of modern electronic applications. Soft-switching technique can be used in the single stage buck converter to improve the converter's efficiency. However, the buck converter is still operating at extremely low duty ratio. Quadratic buck converter would operate at a relative high duty ratio. However, the converter control is difficult and it may present voltage or current overstresses. As a matter of fact, the single-stage buck-based converter may not be able to satisfy the requirements of applications requiring LVG conversion.

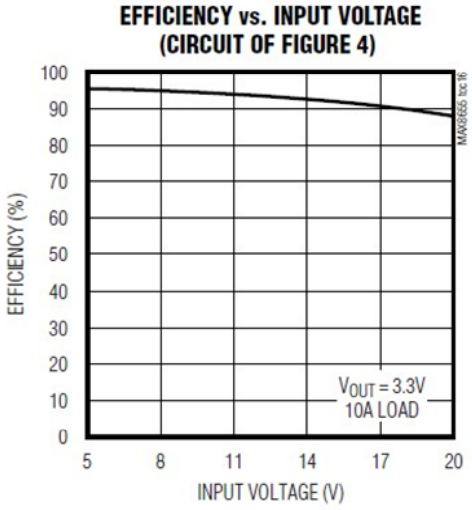


Figure 1.1: Typical efficiency curve of a buck converter (From datasheet of MAX8655).

Considering the size and weight requirements in modern electronic products, a good candidate power converter is the switched-capacitor (SC) DC–DC converter, which has the advantages of small size, light weight, high efficiency and high power density. SC converters, which consist exclusively of power switches and capacitors,

remove magnetic components from their topologies, become suitable for integrated circuit (IC) implementation. However, SC DC–DC converters achieve regulation by sacrificing the converters' efficiency.

The limitations of the single-stage converters have spurred the interests in developing a new kind of LVG two-stage DC–DC converters. Such a converter is implemented with a first-stage SC converter, followed by a second-stage buck converter as shown in Fig. 1.2. For this two-stage SC-buck converter, the first-stage SC converter steps down the input voltage while the second-stage buck converter mainly regulates the output voltage. This two-stage converter has an overall efficiency possibly higher than the single buck converter, because the second-stage buck converter operates at a lower input voltage with higher efficiency. The energy saved by the efficiency improvement of the second stage makes room for the first-stage converter to convert the voltage down. It is obvious that if the energy saved by the second-stage buck converter is higher than the energy loss consumed by the first-stage converter, then the overall efficiency will be improved. Recalling the consideration on power density, the possibility of integrated circuit implementation for the SC stage, and high switching frequency with robust control for the buck stage, it is highly possible that the overall two-stage SC-buck converter can be small in size and light in weight.

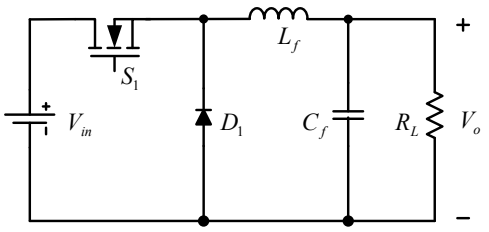


Figure 1.2: Buck topology.

1.2 Literature Review

The literature review is organized under several categories of discussions. We aim to provide a clear historical overview on the current development, as well as to provide

some hints on the future development of this research area.

1.2.1 Modified Single-stage Buck Converter

Buck converter is the most frequently used topology in the industry due to its simplicity, high efficiency and ease of control. However, as discussed in Section 1.1, its performance deteriorates to an unacceptable level for LVG applications which need extremely small duty cycle. Modifications of the buck converter are thus carried-out to meet the requirements of LVG applications.

1.2.1.1 Interleaved Buck Converter

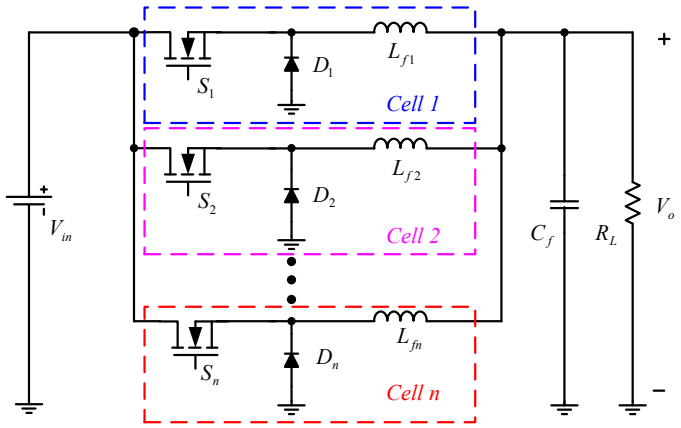
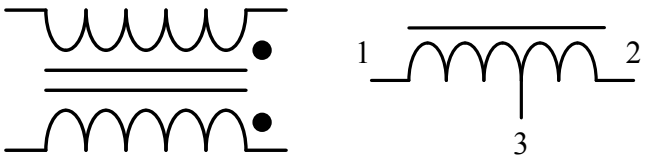


Figure 1.3: Interleaved buck converter.

In order to improve the efficiency and the transient response of converters, which are the key electrical requirements in the applications, the interleaving technique is applied to a buck converter [6–10] as shown in Fig. 1.3. Interleaving technique is implemented by paralleling several similar structure modules which are controlled by a series of interleaved driver signals. An additional advantage of the interleaved buck converter is the reduction of the filter inductances and capacitances, which reduce the size and the weight of the converter. In 1998, interleaved buck converter was first suggested for voltage regulation module (VRM) . Simultaneously, the freewheeling diode is also replaced by an active switch (e.g. MOSFET), hence the converter was

named interleaved synchronous rectifier buck converter. The results proved the benefits of the converter on improving the power density, efficiency, and transient response [6, 7]. With considering these advantages of interleaving technique, Miftakhutdinov [10] continued to investigate an approach for optimizing design of the slew rate of the transient response for an interleaved synchronous buck converter in 2001. Since the efficiency is also an very important criteria in converter design, Yuri Panov *et al.* [8, 9] proposed an design guideline for a general interleaved buck converter by balancing between the transient response and the efficiency. Besides, the variable-slope ramp signal [8, 9] is used instead of the traditional constant-slope ramp to further improved the transient response.

1.2.1.2 Modified Buck Converter:



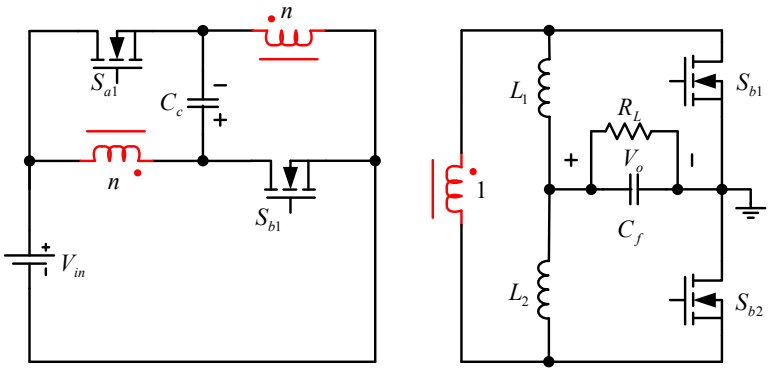
(a) Coupled inductor (b) Tapped inductor

Figure 1.4: Inductors used in the buck converter.

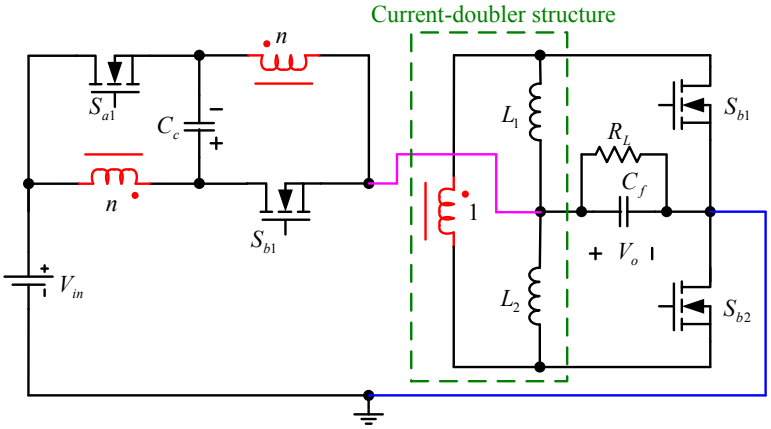
Although the interleaving technique improves transient performance of the buck converter, the converter efficiency becomes rather low in LVG applications due to the associated small operating duty cycle. To improve the efficiency, a larger operating duty cycle is needed. However, the steady-state duty cycle is fixed once the voltage gain of the buck converter is specified. An alternative technique is to employ the forward converter, a transformer isolated version of the buck converter, where the transformer takes care partly the voltage conversion requirement, allowing the duty cycle to be designed to some sweet spots by a proper selection of transformer turns ratio.

To take advantage of applications without the need of isolation, different types of inductors are employed, e.g. tapped inductor and coupled inductor as shown in Fig. 1.4, which act like the transformer of a forward converter and achieve a higher

overall voltage conversion ratio. As the voltage conversion is partly handled by the modified inductor, the duty cycle of buck convertor can operate at some less extreme conditions to improve efficiency.



(a) A push-pull Forward converter



(b) A push-pull buck converter

Figure 1.5: A push-pull Forward converter in (a) utilizes the capacitance C_c and the n:1 transformer to achieve a higher voltage conversion ratio of the converter. The push-pull buck converter in (b) connects the primary in series with the secondary output load to further increase the overall voltage conversion ratio.

In 2000, Lenk [11] suggested replacing the traditional inductor with a tapped inductor in the buck converter to increase the voltage conversion ratio. However, this topology, like the forward converter, will lead to a high voltage spike because of the associated transformer leakage inductance, which increased the voltage stress of the top switch. Then in 2001, Xu *et al.* [12] used an active-clamp coupling inductor to decrease the voltage spike of an buck converter and increase the voltage conversion ratio. In the next year, based on that topology, Xu *et al.* [13] further integrated the input

filter into the inductor of the converter using integrated magnetics to reduce the input current ripple and also decrease the filter size.

In 2002, Wei *et al.* [14] modified a push-pull forward converter shown in Fig. 1.5(a) to a push-pull buck converter shown in Fig. 1.5(b) to increase the converter voltage gain. The coupled inductor topology was applied to the interleaved buck converter [13,15] to have a higher duty ratio with the same voltage gain. Moreover, integrated magnetics is used to improve power density. However, these topologies [11, 13–15], which employ tapped-inductor or coupled inductor to partly increase voltage conversion ratio of the converter, will increase size and weight of the converter and reduce the buck inductance. The duel function of the modified inductor will decrease the inductance for the buck function and lead to a larger output voltage ripple with the same power density. The higher order modified inductor will have a higher possibility of instability if the control of the converter does not design properly.

1.2.2 Two-stage Converter

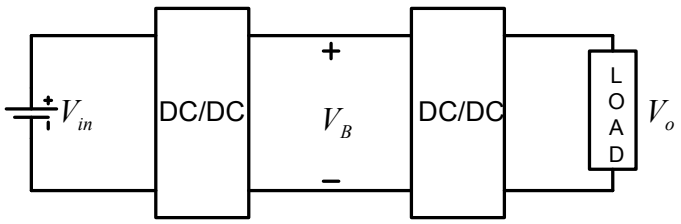


Figure 1.6: Block diagram of non-isolated two-stage converter.

In recent years, more and more scholars suggest to use two-stage converter as the topology for LVG conversion applications. At the beginning, the transformer was selected as a stage for the two-stage converter to provide partly the voltage conversion. Later, the two-stage converter concept, which was composed of two converters shown in Fig. 1.6, was also attracted research interest.

1.2.2.1 Topologies with Transformer

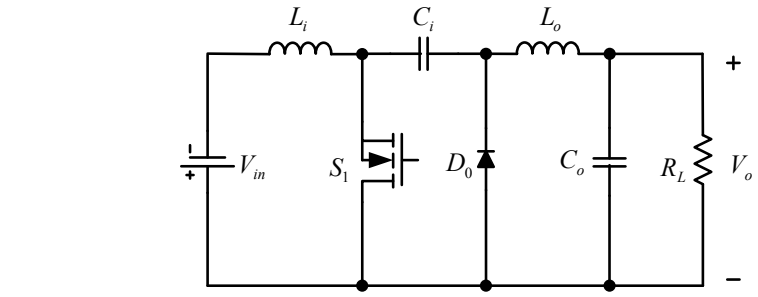
The earliest two-stage converter was reported in 2001 [16]. In this work, Alou *et al.* illustrated a two-stage topology of buck plus a half bridge converter for the LVG application. In this two-stage converter, by a proper design of the transformer turns ratio, the duty ratio of half bridge converter was designed to be 0.5 to obtain the best transient response. In 2003, Ren *et al.* [17] proposed two schemes of two-stage converter for LVG application. The two-stage converter is composed of a fixed voltage conversion stage with isolation and another stage to perform voltage regulation. Furthermore, the authors also proposed a guideline for the selection of intermediate voltage, V_B in Fig. 1.6, to optimize the overall efficiency of the converter.

1.2.2.2 Topologies without Transformer

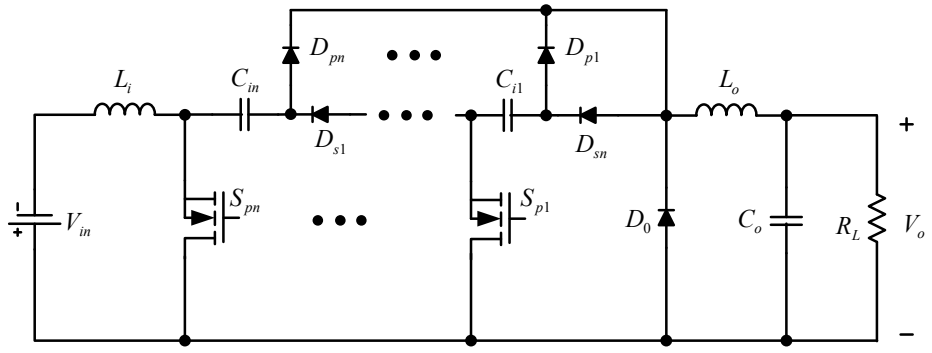
Considering that voltage isolation is not always required, many transformerless topologies were proposed. In 2004, Ren *et al.* [18] proposed a non-isolated two-stage concept, whose first-stage and second-stage were both synchronous buck converter. In 2006, Xu *et al.* [19] introduced a voltage divider as the first-stage converter of the two-stage converter. The first-stage steps down the input voltage and the second-stage regulate the output voltage. A design discussion [20] and a transient analysis [21] of the converter are also reported. In 2008, Pilawa-Podgurski *et al.* [22] suggested using soft-charging method to improve the SC-based two-stage converter. The effectiveness of the method was implemented and confirmed in 2012 [23]. In 2009, Qahouq *et al.* [24] provided a control scheme to select the output voltage of the first-stage converter, optimizing for the best overall efficiency. In 2010, Rong Guo *et al.* [25,26] published an adaptive conversion ratio SC-based two-stage converter, in which the conversion ratio of the first-stage SC converter is changed according to the input voltage to maximize the efficiency of the converter in a range of the input voltages.

1.2.3 Integrated-stages Converters

To obtain LVG, the voltage-link capacitor C_i in Fig. 1.7(a) of a Ćuk converter is replaced with a series-charged and parallel-discharged SC structure shown in Fig. 1.7(b) to increase the voltage conversion ratio in 1988 [27]. In 2008, Ioinovici *et al.* [28, 29] replace capacitor/inductor with the switched-capacitor/switched-inductor structures inside the buck or Ćuk converters to increase the converters conversion ratio. While, in 1991, paper [30] integrated the switch of a two-stage converter to provide a voltage conversion ratio varying with the square of the duty cycle for LVG application.



(a) Ćuk converter



(b) Ćuk converter

Figure 1.7: A non-isolated two-stage SC converter (b) modified from the Ćuk converter (a).

1.2.4 Switched-capacitor Converter

As this thesis is to investigate the two-stage step-down DC–DC converters which are based on switched-capacitor converter, the subsequent reviews here will focus on

the step-down DC–DC switched-capacitor converters.

In the traditional magnetic-based power electronics area, there are four types of converters: DC–DC converters, AC–DC converters, DC–AC inverters and AC–AC transformers. Similarly, a Japanese group from Tezuka [31] first developed a DC–DC switched-capacitor (SC) converter in 1983. Later in 1989, Marusarz presented a DC–AC SC inverters [32]. Then, these SC converters were soon followed by AC–DC converters [33] and AC–AC transformers [34].

1.2.4.1 Topologies of SC Converter

The series-parallel switched-capacitor converter, which only has two phase, series charging state and parallel discharging state for step-down operation, and vice versa for step-up operation, is the most simple and commonly used topology. It was among the earliest proposed topologies. The Japanese group, Tezuka *et al.* [31], proposed the first symmetrical series-parallel SC DC–DC converter in 1983. This first SC converter was composed of two series-parallel SC cells, which were controlled by two clocks with 180° phase shift. However, this series-parallel SC converter had high input pulse current and lack of output voltage regulation. Hence, a large part of efforts were done to improve the SC performances. In 1992, Cheong *et al.* [35] presented a symmetrical interleaved duty-ratio controlled SC converter, with regulated output voltage. In the converter, the output voltage was determined by the flying capacitor, which was charged to the objective output voltage by controlling of the charging time. In 1999, Zhu *et al.* [36] developed a symmetrical series-parallel SC converter with higher regulation capability and improved conversion ratio by adding the output capacitor into the charging path. In 1996, Chung *et al.* [37] designed a quasi-switched capacitor (QSC) to improve the input current. Traditionally, the active switches in power converter usually worked in the linear region. However, to remove the pulsed input current, Chung [37] drove a switch in the charging path to saturation region to make it produce a constant current. To reduce the output voltage ripple, Han *et al.* [38] introduced the interleaving technique into series-parallel SC converter, which implemented the series charging and

interleaved discharging of each flying capacitor to the load in 2004. Moreover, this method was implemented in an IC chip in 2005 [39]. In 2004, Thiele *et al.* [40] also used quasi-switch to improve the output voltage ripple, namely current controlled SC converter. In this converter, the flying capacitors were fully charged, while the discharging path was determined by a switch, which was driven to perform as a current source to reduce the voltage ripple of the output capacitor. In 2010, Tan *et al.* [41] employed interleaving technique to series-parallel SC to minimized both the input current and output voltage ripples. Later, the ripples were further reduced adaptively to the load level [42].

Besides the series-parallel SC converters, many topologies were also investigated. In 1990, Umeno *et al.* [43] illustrated an fixed conversion-ratio of 0.5 step-down SC converter, namely voltage divider, which can reduce the input current ripple compared with a single series-parallel SC converter. Later in 1998, Suzuki *et al.* [44] extended the voltage divider to a general voltage divider which can achieve one n-th step-down conversion. In 1995, Makowshi [45] provided a fibonacci SC converter, which uses least components in the same conversion ratio compared with a two-phase SC converter. Then, in 2011 Kushnerov [46] gave an algebraic synthesis method for the fibonacci SC converter. In 1998, Hara *et al.* [47] proposed a new SC, namely ring-type SC converter, to reduce the input inrush current. In the next year, the same group developed the ring-type SC to an multi-output SC converter by changing the control scheme of the switches [48]. In 2003, Eguchi *et al.* [49] proposed a control scheme, which made the ring-type SC a controllable conversion ratio SC converter. In 1999, Chung extended the symmetrical series-parallel SC converter [37] to a bi-directional SC converter [50] and an n-stage SC converter [51]. In 2007, Oraw *et al.* [52] proposed a ladder type switched capacitor. In order to further save the components, Chhawchharia *et al.* [53, 54] suggested cascading two SC converters to obtain a higher voltage conversion ratio. In 2001, Zou *et al.* [55] proposed a modular SC converter, in which many SC modular was series connected to obtain the desired voltage conversion ratio.

High efficiency is the core performance of power converters. In the SC converter,

improving the efficiency attracted many attentions. In 1998, Cheng [56] firstly introduced zero current switching to SC converter by inserting a small inductor to reduce the switching losses. Similar works were also done in papers [57,58]. In 2002, Cheng [59] extended the resonate SC converter to a multi-output converter. In 2007, Lee *et al.* [60] applied resonant switching into a bi-directional SC converter. In 2008, Keiser *et al.* [61] implemented the resonant SC converter in high power SC converter application. In 2009, Sano *et al.* [62] inserted a small inductor into a voltage divider [43] to achieve resonant switching. In 2011, Ko *et al.* [63] employed both interleaving technique and resonate switching to multi-phase SC converter. However, Ioinovici *et al.* [64] believe that inserting a small inductor cannot improve the SC efficiency and insisted that the overall efficiency was resistance independent and depended on the input voltage, output voltage and the conversion ratio [65]. In 2007, Oraw *et al.* [52] used current split technology to reduce the RMS current through capacitors of the ladder SC to reduce the loss. In 2010, Chen *et al.* proposed using PFM control to maximize the topology efficiency [66].

1.2.4.2 Analysis of SC Converters

Since Middlebrook proposed the state-space average model for switching converter in 1970s [67, 68], it becomes a general analytical method for the switching converter. Later, state-space average model was also used for the analysis of SC converter [31, 35, 37, 43, 69, 70, 70–75].

In 1992, Ngo *et al.* [69, 71] proposed the state-space model of series-parallel SC converter. The paper concluded that the converter's efficiency was $n\frac{V_o}{V_{\text{in}}}$, where n is the number of flying capacitor, V_{in} and V_o are the input and output voltage, respectively. Later, the research group proposed a modified state-space average model of SC by making an approximation of the exponential function [70, 72]. In 1996, Chung *et al.* [37] employed state-space average method and established a model for quasi-switched capacitor converter. In 1998, Chung *et al.* [73] applied the state-space average method into the multi-phase SC converter. In 2004, the state-space average method was also

extended to quasi-switched capacitor converter [74] and resonant switched capacitor converter [75].

Direct circuit analysis for the SC converters was also widely employed. In 1994, Tse *et al.* [76, 77] analyzed the losses mechanism of a capacitor in both charging and discharging states. In 1996, Zhu *et al.* [65, 78] analyzed the symmetrical SC converter by solving the equations of each state and got similar conclusion about efficiency with papers [69, 71], i.e., the converter's efficiency was $n\frac{V_o}{V_{in}}$. In 2004, Yeung *et al.* [79] derived and solved the equations of each state and concluded that using the zero-current-switching technique can reduce the converter loss. In 2005, Kimball *et al.* [80] deduced an simple model of quasi-resonant SC converter by developing and solving differential equations for all switching mode with the boundary conditions in steady state. In 2013, Cheung *et al.* [81] claimed that the resistance in the charging path did not affect the SC efficiency, while the resistance in the discharging path would. Consequently, the way to improve the SC converter was to improve the discharging efficiency.

Since a typical model of SC converter in steady state is a transformer with a rational-turns ratio connected with an equivalent resistance. Hence, scholars also established many models of such model. In 2006, Seeman *et al.* [82, 83] developed an SC model by an evaluation of the output impedance which is a function of frequency. In 2012, Salem *et al.* [84] extended the work into the resonant SC converter. The technique in paper [85] was suitable for the steady-state analysis without considering the parasitic resistors. However, this work was focus on either the low switching frequency or the high switching frequency, while the situation at medium switching frequency did not included. Henry et al. [86] provided a method useful at all frequency. In 2009, Ben-Yaakov *et al.* [87, 88] proposed an efficiency analysis method by expressing the losses as a function of capacitors' currents which are proportional to the output current. Later, Ben-Yaakov *et al.* [89, 90] developed the model with an average current compatible with many simulators in both dynamic and steady states. However, the method is limited to the converter that can reduce each operation state of the SC converter into an equivalent first-order RC network. This work was also confirmed in a hybrid boost-SC

conveter [91].

In 1999, Liu *et al.* [92] proposed a new analytical approach, namely charging balance, though the theory that the charges in the circuit cannot be produced nor removed, for SC converter. In 1995, Makowshi *et al.* [45] showed the limitation of the two-phase SC converter by using tools of linear algebra and graph theory. The analysis concluded that the Fibonacci SC converter has the highest voltage conversion ratio with the same number of flying capacitors in the two-phase SC converter. In 2012, Lopez *et al.* [93] proposed a general equivalent continuous model to obtain an accurate dynamic and steady state loss model in the ladder type SC converter.

1.2.5 Remarks

In concluding the survey of literature, the major developments of LVG converter as well as some comments on the possible directions of research are summarized as follows.

The original idea of LVG conversion applications is inherited from the application of traditional single-stage buck converter, using auxiliary techniques, e.g. interleaving technique. However, the critical issue of the buck converter in this application is the extremely low duty ratio, which not only limits the transient response, but also deteriorates the converter efficiency. The effort of applying the tapped and coupled inductor has solved the issue of the extremely low duty ratio. However, it has also introduced the issues of higher output voltage ripple and the associated right-half-plane zeros with the employment of the tapped or coupled inductor. Hence, in recent years, the trend of LVG applications migrates to utilize the two-stage converter, in which the first-stage converter is implemented for large voltage conversion and the second-stage converter is operating for voltage regulation. The SC converter, which is famous for its small size and high efficiency, has proved to be a good candidate for the first-stage voltage conversion of the two-stage converter. Much work has been devoted to the SC-based converter. However, it still exists confusion for the application of the SC-based two-stage converter.

Firstly, the two-stage converter based on the series-parallel SC converter, which is frequently used as the first-stage, has been proved to be a high efficiency converter in the LVG conversion as compared to the single-stage buck converter. It is important to find out the parameters affecting the efficiency when the two-stage converter is practically applied. Essentially, more explorations into this aspect are necessary.

Secondly, another type of two-stage converter attracted a large number of research effort is based on the first-stage voltage divider, which has a fixed conversion ratio of 0.5. Many advantages, such as super high efficiency and good transient performance, of this two-stage converter are experimentally confirmed. However, The fixed conversion ratio also raised the concern on the issues from the further increase of the input voltage and/or further decreasing of the output voltage, which forces the second-stage buck converter once again to operate at an extremely low duty ratio. On the other hand, it is also required a large number of switches and capacitors in the situation for the traditional series-parallel SC converter to be operated as the first stage of the two-stage converter. Hence, an alternative SC converter with smaller number of components and higher voltage conversion ratio is still required.

1.3 Objective of the Thesis

The main objective of this thesis is to investigate some proper first-stage SC converters for LVG application. This thesis will propose different types of SC-based two-stage converter. Moreover, the analysis and design methods are discussed. The aim is to provide some useful converters in LVG application and give a design guideline for the engineers.

1.4 Outline of the Thesis

The thesis is organized as follows:

Chapter 1 gives a comprehensive literature review about the previous and current works of LVG converters. The issues of the LVG converter are discussed. The motivations of the research and the objectives of the thesis are described.

Chapter 2 reviews two types of DC–DC step-down converters, which are SC and buck converters. The various topologies of SC DC–DC step-down converter and the analytical methods of SC converters are discussed. The various types of SC-based two-stage converters are also discussed.

Chapter 3 introduces a hybrid SC-buck converter that can be readily applied in the LVG application with high efficiency. To investigate the performance of the hybrid SC-buck converter, an analytical model of the hybrid SC-buck converter is derived. Based the model, the optimization and design methodologies are presented.

Chapter 4 proposes a family of exponential SC converter. To save the components and achieve LVG, an exponential SC converter is proposed. This chapter also proposes an analytical model suitable for the exponential SC converter.

Chapter 5 applies the proposed exponential SC converter in the two-stage converter. The analysis and design methodology are also discussed in the chapter.

Chapter 6 concludes this thesis. The major contributions are summarized in this chapter. Some suggestions for future research are also discussed.

Chapter 2

Overview of the Two-stage DC-DC Converters

2.1 Introduction

DC-DC converters are electronic building boards that facilitate the transfer of power from the source to the load with different requirements of DC input and output voltages or currents. The aim of the power conversion process is to achieve highest efficiency with best dynamic and steady-state performances, highest power density and lowest cost. According to the input and output voltage level, the DC-DC converters are divided into two categories, which are step-down and step-up types of converters. The following sections give a brief discussion of different topologies of step-down DC–DC converters.

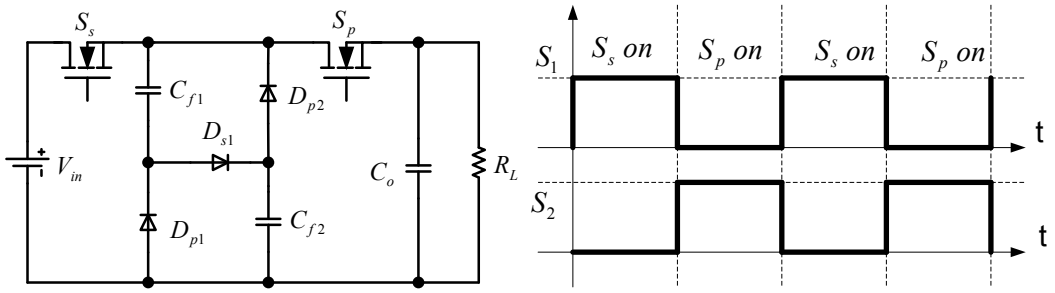
2.2 The Switched-capacitor Converter

The switched-capacitor converter, which is composed of switches and capacitors only, is famous for its small size and light weight because of the absence of magnetic components. In this section, the commonly used topologies are introduced.

2.2.1 Topologies of SC Converter

In this subsection, the most frequently used SC topologies are introduced.

2.2.1.1 Series-parallel SC Converter



(a) Topology (b) Timing Diagram

Figure 2.1: Series-parallel SC.

The series-parallel SC converter as shown in Fig. 2.1 [38, 39, 41, 42], which only has two states: series charging state and parallel discharging state, is the most frequently applied SC topology . At the charging state, S_s is 'ON', S_p is 'OFF' and D_{s1} is forward biased. In this state, all flying capacitors, which are C_{f1} and C_{f2} in Fig. 2.1, are series connected by S_s, D_{s1} and charged by the input voltage source V_{in}, while the power of the load R_L is supplied by connecting to the output capacitor C_o. During the discharging state, S_s is 'OFF', S_p is 'ON' and D_{p1}, D_{p2} are forward biased. In this state, the flying capacitors will be parallel connected by D_{p1}, D_{p2} and discharged to the load R_L and the output capacitor C_o. At the steady-state, the electronics charging

and discharging of each capacitor is balanced, hence, all voltages of the capacitors are stable. Furthermore, in some specific applications, the diodes can be replaced by active switches (e.g. MOSFET) to reduce the conduction loss.

Fig. 2.2 is a general series-parallel SC converter. The voltage conversion of the converter is given as

$$V_o = \frac{1}{n} \cdot V_{\text{in}}. \tag{2.1}$$

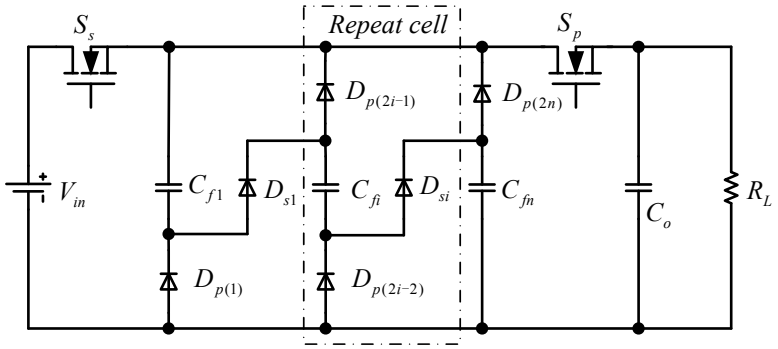
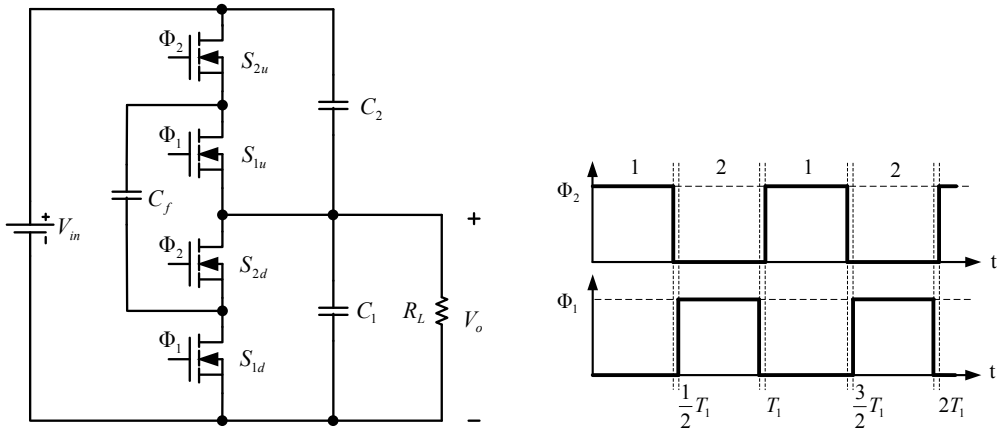


Figure 2.2: General series-parallel SC converter

2.2.1.2 Voltage Divider



(a) Topology (b) Timing Diagram

Figure 2.3: Voltage divider.

The voltage divider as shown in Fig 2.3 was first proposed by Unemo *et al* [43] in 1990. The function of the converter is to step down the input voltage to its half. To

make sure the voltages of the two bypass capacitors (C_1 and C_2) be reached half of the input voltage, the flying capacitor (C_f) is controlled alternatively in parallel with one of the two bypass capacitors (C_1 and C_2) for half of the switching period. The process can deliver the energy from the higher voltage capacitor (C_1 or C_2) to the lower voltage capacitor (C_2 or C_1) as well as deliver the energy from the source to the load. Hence, the voltages of the two bypass capacitors are eventually balanced to near half of the input voltage.

Fig. 2.4 shows a general topology of voltage divider [44]. The voltage conversion of the converter is given as

$$V_o = \frac{1}{n} \cdot V_{\text{in}}. \tag{2.2}$$

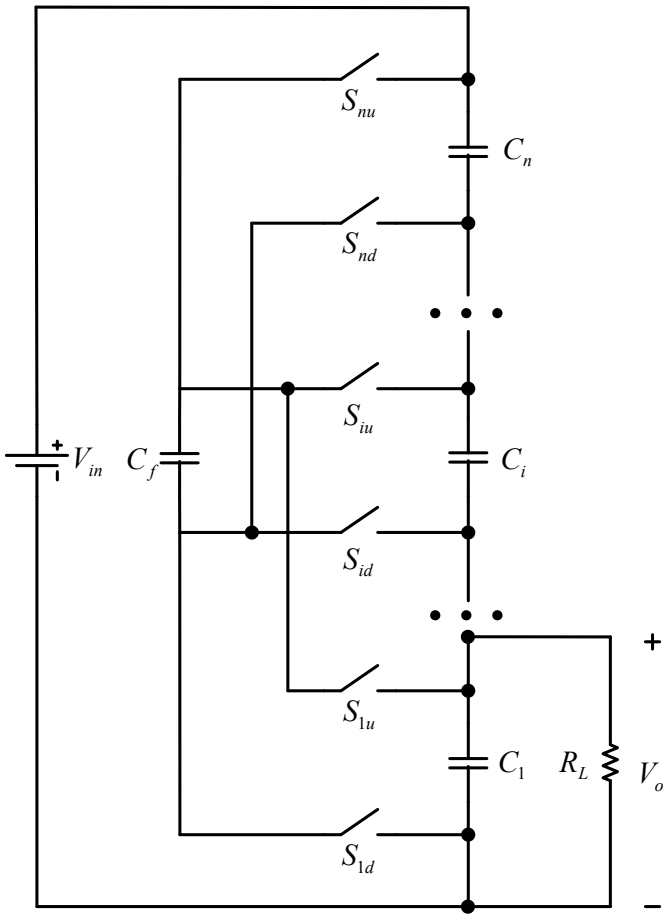
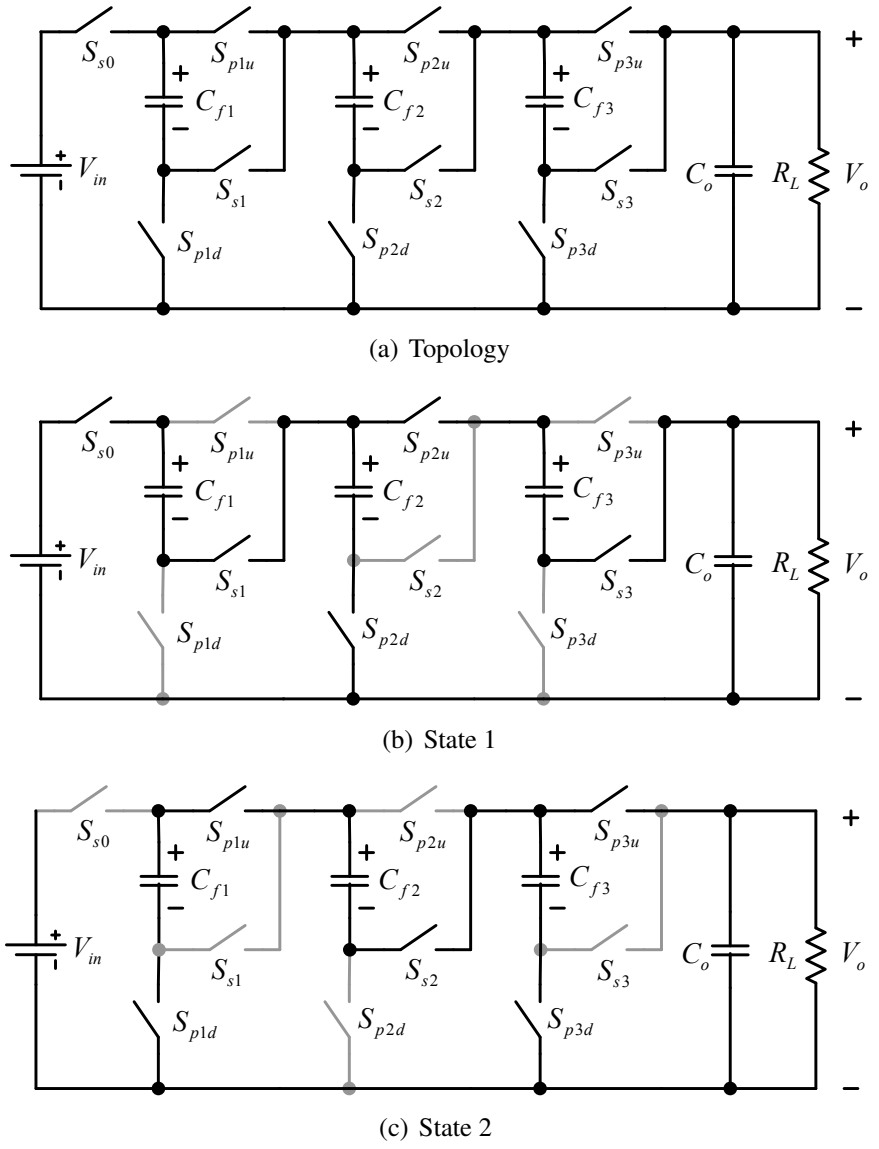


Figure 2.4: General voltage divider SC converter

2.2.1.3 Fibonacci Type SC Converter



(a) Topology

(b) State 1

(c) State 2

Figure 2.5: Fibonacci type SC converter.

Fig. 2.5 shows the topology of a step-down Fibonacci SC converter, which converts the input voltage to a voltage according to the Fibonacci number [45]. The operation of the converter is also shown in Fig. 2.5, which includes two states. In state 1, input voltage source V_{in} charges the series connected capacitors C_{f1} and C_{f2}. Concurrently, the flying capacitor C_{f2} discharges to the series connected capacitor C_{f3} and C_o. The following voltage equations can be obtained:

$$V_{\text{in}} = V_{cf1} + V_{cf2} \tag{2.3}$$

$$V_{cf2} = V_{cf3} + V_{co} \tag{2.4}$$

While in state 2, flying capacitor C_{f1} discharges to C_{f2} and C_{f3}, which gives

$$V_{cf1} = V_{cf2} + V_{cf3} \tag{2.5}$$

Simultaneously, the flying capacitor C_{f3} is discharging to the load. Hence, the output voltage (voltage at C_o) and the voltages of the three flying capacitors (C_{f1}, C_{f2}, C_{f3}) are $\frac{V_{\text{in}}}{5}$, $\frac{3V_{\text{in}}}{5}$, $\frac{2V_{\text{in}}}{5}$, and $\frac{V_{\text{in}}}{5}$ respectively.

Fig. 2.6 shows the general Fibonacci SC converter [46]. The voltage conversion of the converter is given as

$$V_o = \frac{1}{F_n} V_{\text{in}}, \tag{2.6}$$

where F_n is a series of Fibonacci numbers (i.e. $F_n = 1, 1, 2, 3, 5, 8, 13, 21 \cdots$ for $n = 1, 2, 3, 4, 5, 6, 7, 8, \cdots$)

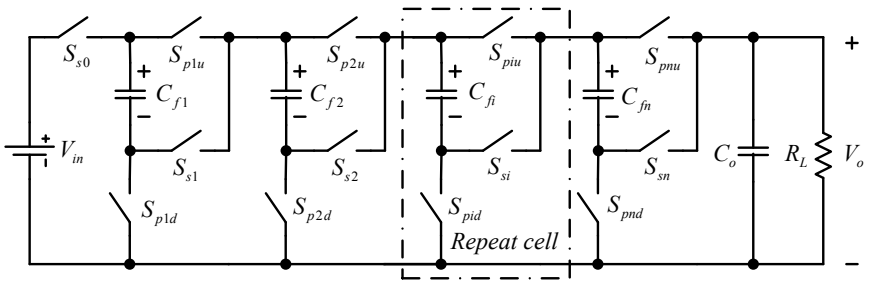
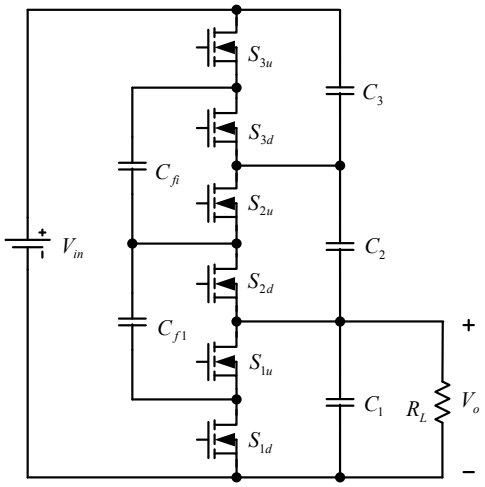


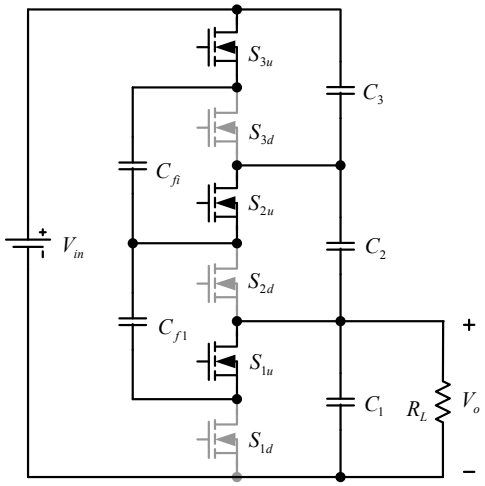
Figure 2.6: General Fibonacci SC converter.

2.2.1.4 Ladder Type SC Converter

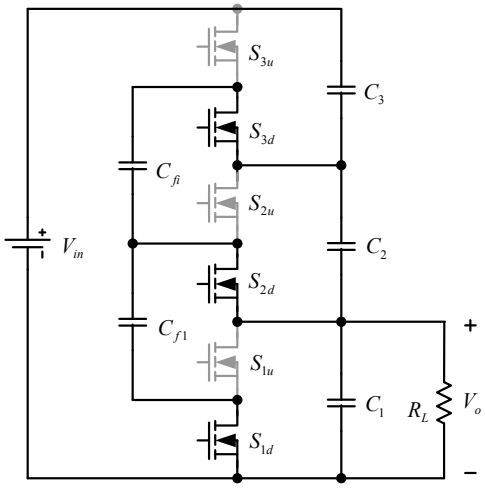
Ladder type SC converter is shown in Fig 2.7 [52]. This ladder SC converter is composed of three bypass capacitors (C_1, C_2 and C_3) and two flying capacitors (C_{f1} and C_{f2}), which can achieve 1/3 voltage conversion ratio. The flying capacitor C_{f2} is



(a) Topology



(b) State 1



(c) State 2

Figure 2.7: Ladder type SC.

paralleled with C_2 and C_3 in the two alternative states, which makes voltages of the two bypass capacitors (C_2 and C_3) equal to the voltage of the flying capacitor C_{f2}, e.g. $V_{c3} = V_{c2} = V_{cf2}$. Similarly, we have $V_{c1} = V_{c2} = V_{f1}$. Hence, the ladder SC converter will have three equalized voltages across C_1, C_2 and C_3 converging to one-third of the input voltage.

Fig. 2.8 is a general ladder SC topology. The voltage conversion of the converter is

$$V_o = \frac{1}{n} \cdot V_{\text{in}}. \tag{2.7}$$

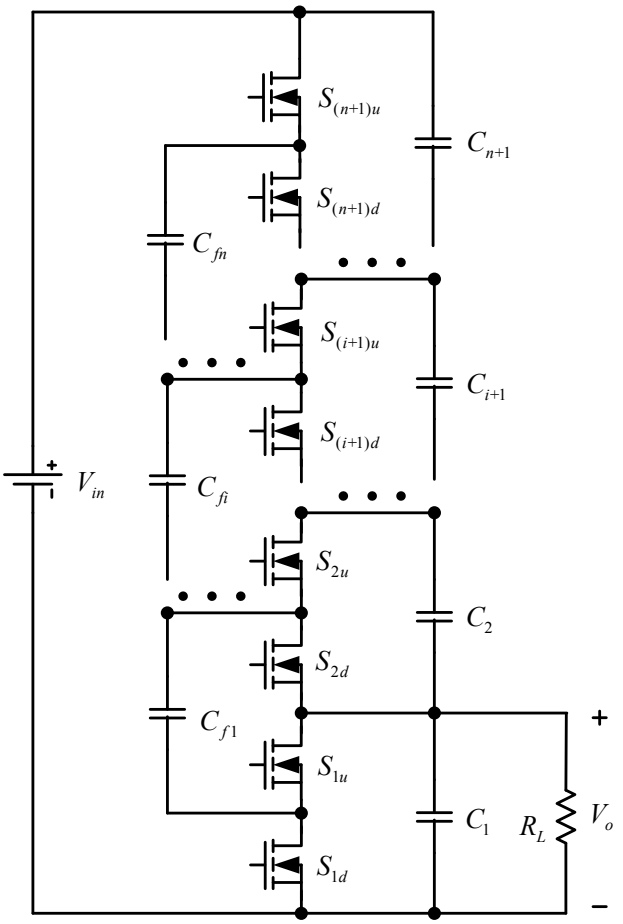
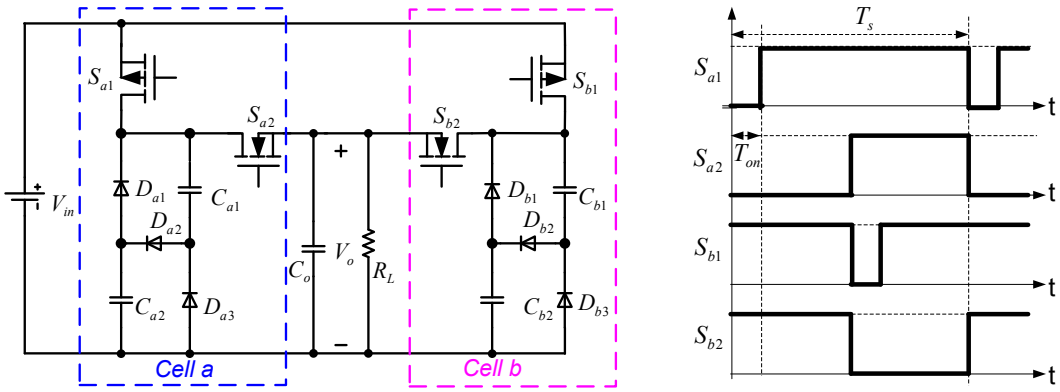


Figure 2.8: General ladder SC converter

2.2.1.5 Symmetrical SC Converter

The symmetrical SC converter, which is widely discussed, is composed of two parallel connected series-parallel SC converter as shown in Fig. 2.9 [31, 35–37, 50, 51]. The two parallel SC converters are controlled to have interleaved currents with 180° phase shift to reduce the input current ripple and output voltage ripple.



(a) Topology (b) Timing Diagram

Figure 2.9: Symmetrical SC.

2.2.2 Control of SC Converter

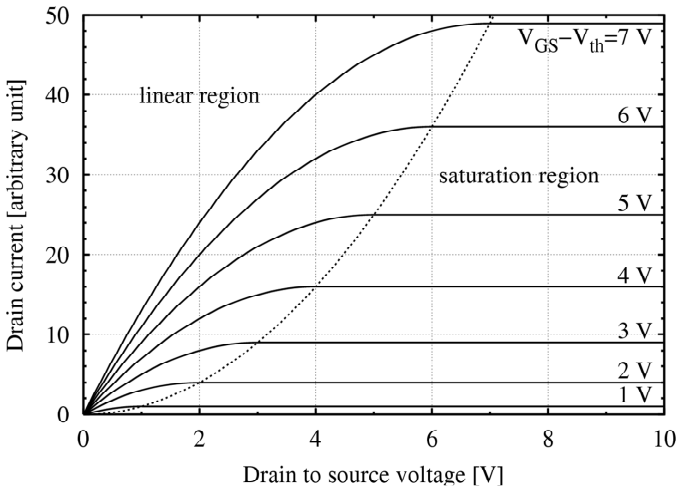
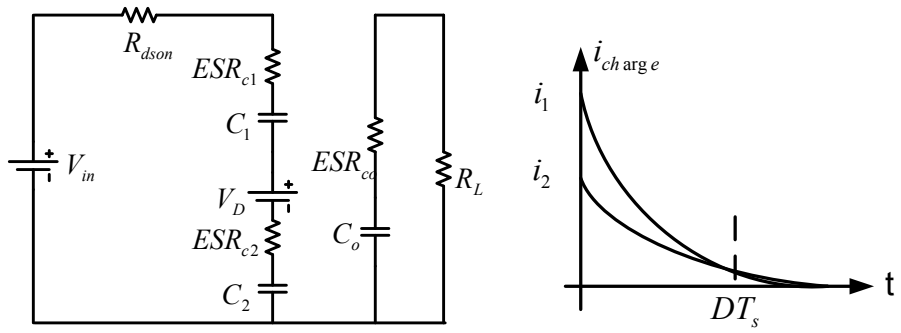


Figure 2.10: Characteristic of MOSFET.

MOSFET is the most widely used switch in power converters, especially in the

low power DC–DC converters. As Fig. 2.10 shown, generally, the operation of a MOSFET is separated into two different regions after turning on, which are linear (triode) and saturation (active) regions, depending on the voltages at the three terminals. Traditionally, considering the energy saving, switches in the basic converters (buck, boost, and buck-boost, etc.) always work at the linear region due to the lowest on resistance (R_{dson}). While in the SC converters, to reduce the voltages ripple and/or achieve voltage regulation, both the regions of linear and saturation are utilized. Accordingly, the control of the MOSFET is categorized as duty ratio control, on resistance control and current control. These three control techniques are briefly discussed in this subsection as follows.

As the series-parallel SC converter is a frequent used SC converter, this section uses the series-parallel SC converter as an example to illustrate the controls of this converter. An equivalent circuit of the series-parallel SC converter is shown in Fig. 2.11.



(a) Equivalent charging circuit (b) Charging current

Figure 2.11: Series-parallel SC equivalent circuit and the charging current.

2.2.2.1 Duty Ratio Control

Duty ratio is defined as the ratio of the time of a switch at on state over the whole period. In the SC converter, the duty ratio control is to adjust the ratio to produce a desired output voltage, and all MOSFET switches are driven to the linear region as resistors. Generally, to simplify the control, at least one parameter, e.g. switching period or the on time of a switch, is set to constant. Depending on the parameter being

kept constant, three control schemes are derived.

1. Constant switching frequency – PWM control

The PWM control is frequently used in the switching mode power converters. In this control, the converter contains approximately two states: the charging state and discharging state. The intermediate state with short dead-time is often neglected. The total time of the charging state and the discharging state, i.e., the switching period, is maintained constant. The control is achieved by adjusting the ratio of the charging time over the switching period, which is named duty ratio, to achieve a desired capacitor voltage [35].

In most SC converter, the charging state circuit can be modeled as a simple RC network as shown in Fig. 2.11(a). In this model, the capacitors in the SC converter are exponentially charged with voltage waveform as depicted in Fig. 2.11(b). This exponential property leads to a difficult control of the duty ratio for a desired charge-up voltage. To have a better control, the dead-time state can be used [35, 36]. In this control scheme, the period and the time duration for the discharging state are kept constant, while the ratio of charging time over the deadtime is adjusted for the desired capacitor voltage.

2. Constant charging time – PFM control

As aforementioned, the charge-up voltage is difficult to control due to its exponential relationship with the duty ratio as indicated in Fig. 2.11. The PFM (pulse frequency modulation) control uses a constant charging time and adjusts the discharging time for controlling the capacitor voltage. Obviously, this leads to a varying switching period. The PFM control has the merit of improved control accuracy. However, the varying switching frequency makes the design difficult.

3. Constant voltage ripple – Hysteresis control

The hysteresis control maintains the output voltage within a hysteresis band of $V_{\rm ref} \pm \frac{\Delta V_B}{2}$ by switching to an alternative state when the output voltage reach to the hysteresis

band [94].

The hysteresis control is a good option to have a tight control of the output voltage ripple. However, in the heavy load condition, the switching frequency can be too high to have good power conversion efficiency.

2.2.2.2 On Resistance Control

The on resistance $R_{d\mathrm{son}}$ of a MOSFET can be controlled by adjusting the transistor gate voltage V_{GS} as shown in Fig. 2.10. This provides a mean to control the voltage of flying capacitor, which in turn controls the output voltage.

2.2.2.3 Current Control

A MOSFET performances as a voltage controlled current source when it works at the saturation region [37, 40, 95]. By adjusting the gate voltage to have different charging current, the voltage of flying capacitors can be readily controlled. By using this current control, the charging current is bounded, which highly reduces the EMI of the circuit. However, it needs a complicate variable voltage gate driver circuit.

2.3 A Review of Buck Converter

The buck converter is widely adopted in the industry for voltage step down applications due to its high efficiency, good steady-state regulation and good transient response. However, the demand of voltage step down converter has reached to the regime of LVG voltage converter with high efficiency, high power density and good transient performance. Hence, efforts have been done to modify the buck converter for this new requirement. The efforts used will be highlighted in this section.

2.3.1 Challenges of Buck Converter in Large-voltage-gain Application

The modern electronics applications requires the power converter with high efficiency, high power density and high transient performance.

Inside the buck converter, the most volume occupied components are the charge-storage capacitors and inductors. However, as discussed in the Chapter 1, the supply voltage for most microprocessors is reaching 1 V and below that a much higher value filtering capacitance is needed for voltage regulation to maintain the required performance. Hence, the method of reducing the converter size is to reduce the values of filtering capacitors and inductors. This can be achieved by increasing the switching frequency. Since the switching frequency increases n times, the value of filtering inductor and capacitor can be reduced by a factor of $\frac{1}{n^2}$. Moreover, the value reduction of filtering inductor also improves converter transient response.

High conversion efficiency is another highly considered requirement of the power converter. The losses are coming from the switching, conduction and driver losses of the switches, and the conduction losses of inductors and the parasitic resistors within the circuit. The ways to reduce the losses include the reductions of the switching losses by lowering the switching frequency and the r.m.s. conduction losses by increasing the value of the filtering inductors.

Hence, the first challenge of the buck converter is the trade-off among high efficiency, high power density and high transient response by a balanced design of switching frequency and the values of filtering inductors and capacitors.

When the buck converter is utilized in the LVG applications, the buck converter must work at an extremely low duty ratio. This limits the switching frequency and deteriorates the transient response. Hence, the problem of extreme small duty ratio is the second challenge of the buck converter.

2.3.2 Multi-phase Interleaving Buck Converter

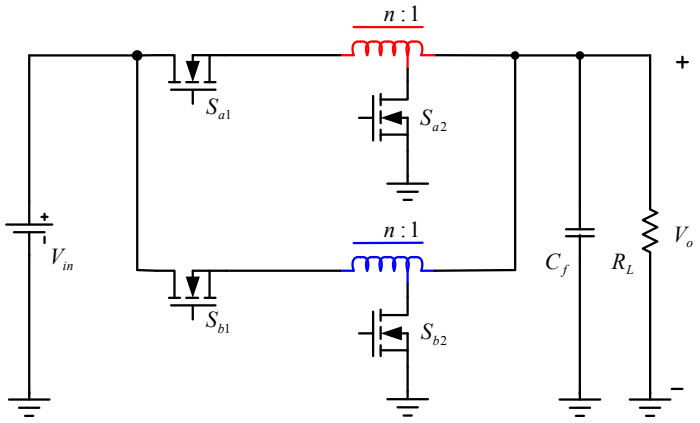
The multiphase buck converter is a parallel connection of n buck cells with the same structure, which are controlled by phase-shifting the switch gate drive signals as shown in Fig. 1.3. Compared with the single buck converter, power delivered by each cell shares one n-th of the original value. This allows a reduction of inductance of each cell. Moreover, the interleaving of n inductor currents is equivalent to the increase of switching frequency and the reduction of the output voltage ripple by n times. Therefore, keeping the same switching frequency, the multi-phase interleaving technique reduces the value of the output filtering capacitor by n times. Similarly, the input current ripple and the input capacitor can also be decreased by n times.

In summary, the multi-phase interleaving buck converter has the following advantages:
(1) filter inductance reduction, which has a certain improvement on transient response;
(2) input and output current ripple reduction, which dramatically reduces the input and output capacitors and the size of the converter;
(3) switching frequency maintenance, which does not increase the switching losses;
(4) power distribution to each cell, which is good for thermal design.

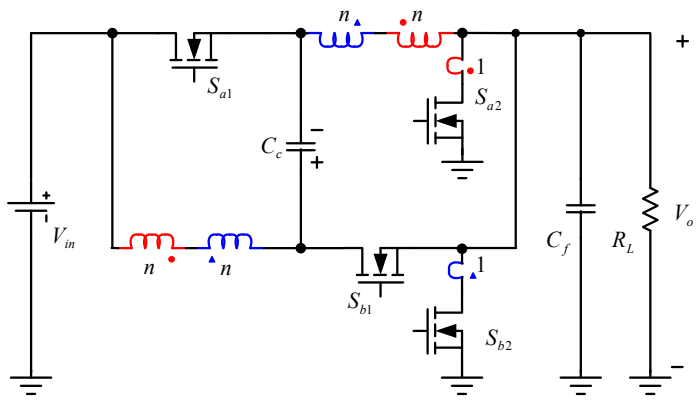
On the other hand, the approach leads to a few disadvantages:
(1) increased the cost due to component count increasing;
(2) the voltage ripple cancellation are not always effective [11, 12];
(3) the second challenge of extreme small duty ratio is still unsolved.

2.3.3 Modified Buck Converter with Interleaving Technique

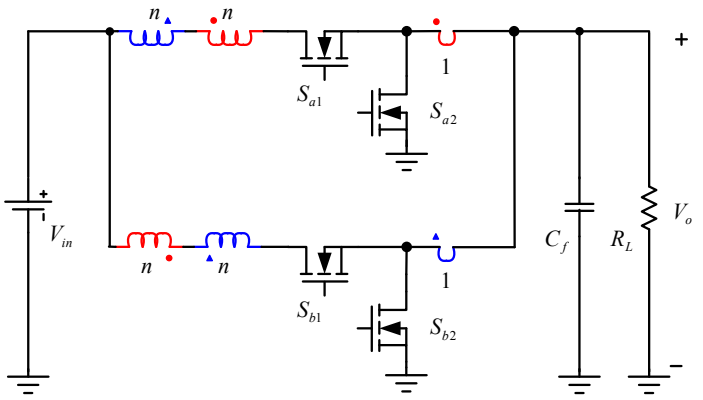
Since the interleaving technique partially solves the first challenge in Section 2.3.1, much research has been done on using the voltage step-down property of coupled inductors shown in Fig. 2.12 [13, 15] to mitigate the requirement of the extreme small duty ratio. However, the leakage inductor limited the maximum switching frequency.



(a) Tapped-inductor buck converter



(b) Active-clamp coupled-inductor buck converter



(c) Wing-coupled-inductor buck converter

Figure 2.12: Modified buck converters. Windings labeled with the same color are coupled with the same magnetic core.

2.4 Review of Two-stage Converters

Since the single-state buck converter cannot fully resolve the two challenges mentioned in Section 2.3.1, a two-stage converter is proposed, in which the second-stage converter uses buck topology. In the two-stage converter, the purpose of the first-stage converter is to step down the input voltage with an efficiency as high as possible, and the second-stage buck converter is implemented with high efficiency and good regulation. After the first stage stepping down the input voltage, the second-stage converter can work at some optimal voltages, leading to a lot of merits. Firstly, the second-stage converter can operate at a duty ratio far from the extreme, which is the key limits of the buck converter in LVG application. Secondly, the second-stage converter can work at a higher switching frequency that the values of the filtering inductors and the output capacitor can be reduced. Thirdly, as the first-stage converter only requires a high efficiency voltage step-down conversion, it has a wider range of topologies to chose from.

2.4.1 Cascaded Buck Two-stage Converter

The cascaded buck two-stage converter topology employed multiphase buck [18] converters for both the first and second stages. The first-stage buck converter performs good efficiency. Hence, the overall efficiency is also very high.

However, inductors involved in two buck converters make the overall converter large and heavy. Hence, the buck converter is not the optimized choice for the first-stage converter.

2.4.2 SC-Buck Two-stage Converter

The SC converter, which is famous for its small size and high efficiency, is chosen as the first-stage converter [19, 20, 22, 25]. However, the SC converter used is a voltage divider with fixed voltage conversion ratio of 0.5, leaving room for improvement if higher voltage gain conversion is needed.

The series-parallel SC converter is also widely used as the first-stage converter in the two-stage converter. Research in [22, 23] proposed a soft-charging concept for the SC converter to improve the first stage conversion efficiency. Research in [25] proposes a control strategy to adaptively control the voltage conversion ratio depending on the level of the input voltage of the SC converter for the best overall efficiency. However, when the SC converter is designed for LVG, the number of components used is very high.

2.5 Conclusion

In this chapter, we have discussed the basic topologies to compose a two-stage converter. The SC converter topologies and their controls are introduced. Similarly, the buck converter and its challenge for LVG conversion are discussed.

Chapter 3

A Hybrid Switched-Capacitor Buck Converter

3.1 Introduction

In the last chapter, we have discussed the basic topologies of a two-stage converter and the associated potential efficiency improvement for LVG applications. Fig. 3.1 shows a two-stage converter by cascading a series-parallel SC converter with a buck converter.

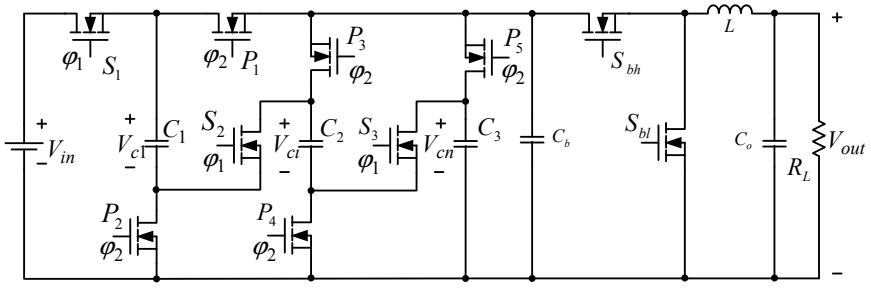


Figure 3.1: Two-stage converter composed of series-parallel SC and buck converters

Working synchronously by aligning the discharging state of SC converter with the charging state of the buck converter and the charging state of the SC converter with the

discharging state of the buck converter, these two-stage converter can be integrated to form a hybrid SC-buck converter as shown in Fig. 3.2 with the components S_{bh} and C_b in Fig. 3.1 reduced. In this chapter, this hybrid SC-buck converter will be studied.

3.2 Topology and Operation of the Hybrid Switched-capacitor Buck Converter

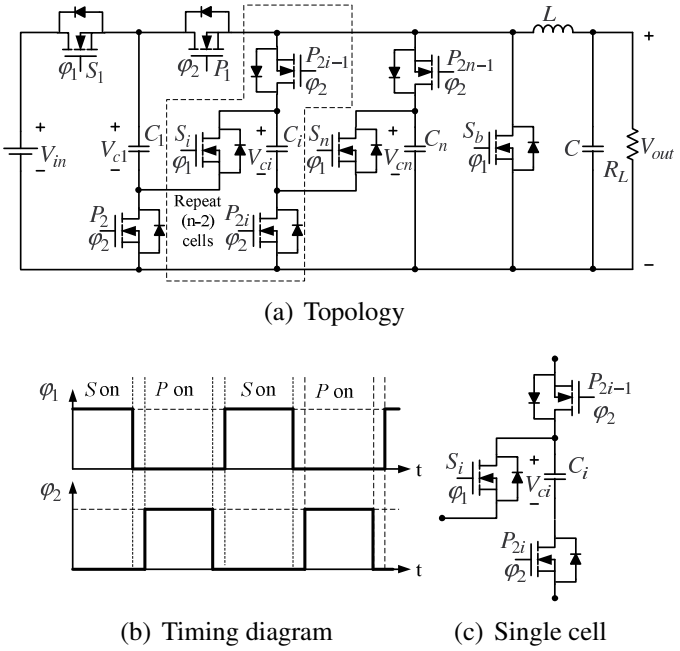


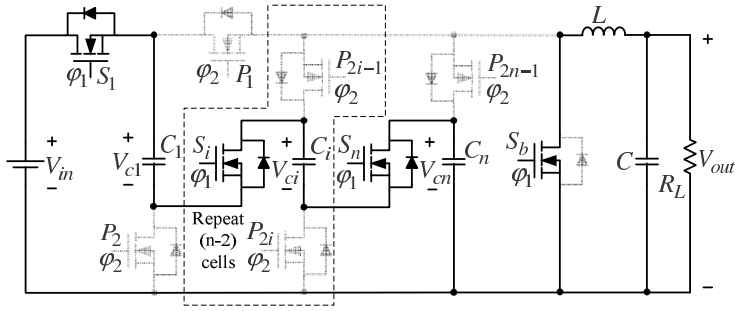
Figure 3.2: Overview of the modified SC-buck converter.

The modified hybrid SC-buck converter and its timing diagram are shown in Fig. 3.2. According to the timing diagram, the hybrid SC-buck converter has three operation states, which are depicted in Fig. 3.3. These states are,

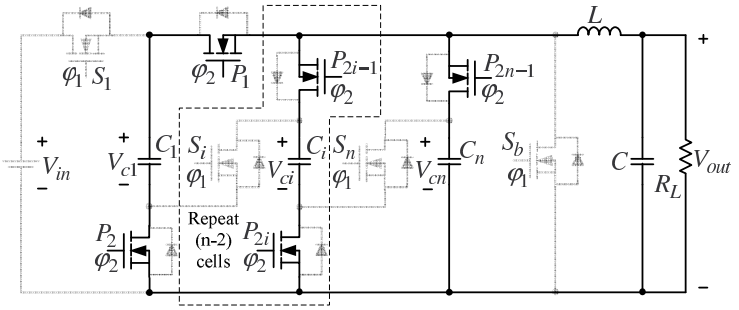
1. State 1: SC stage charging and buck stage freewheeling. In this state, all S switches are "ON" and all P switches are "OFF". V_{in} charges the flying capacitors $C_1, C_2, \cdots, C_n$, which are connected in series as illustrated in Fig. 3.3(a). Concurrently, the buck stage of the converter is in freewheeling mode, of which the current in L freewheels through S_b.

2. State 2: SC stage discharging to the load though the filter inductor. In this state, all S switches are "OFF" and all P switches are "ON". All the flying capacitors are connected in parallel and discharged to the buck stage of the converter as shown in Fig. 3.3(b).

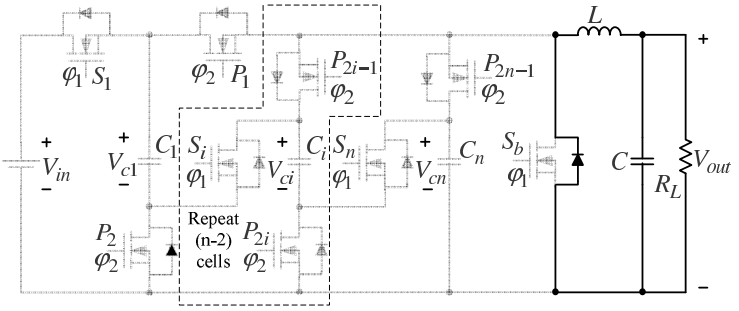
3. State 3: Dead-time state. In this state, all switches are "OFF" as indicated in Fig. 3.3(c). Flying capacitors are neither charging nor discharging. The current in L freewheels through the body diode of S_b.



(a) State 1



(b) State 2



(c) State 3

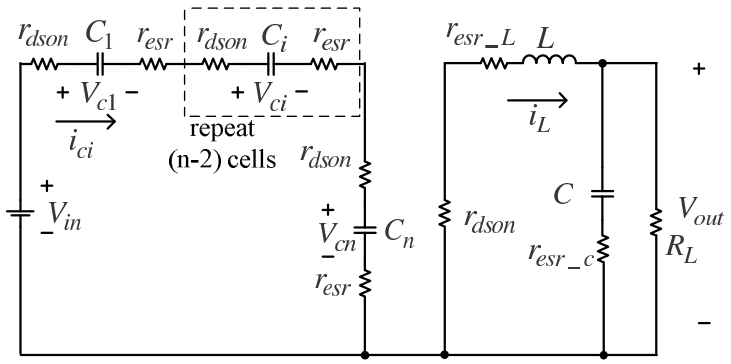
Figure 3.3: Operating states of the modified SC-buck converter.

3.3 Analysis of the Hybrid Switched-capacitor Buck converter

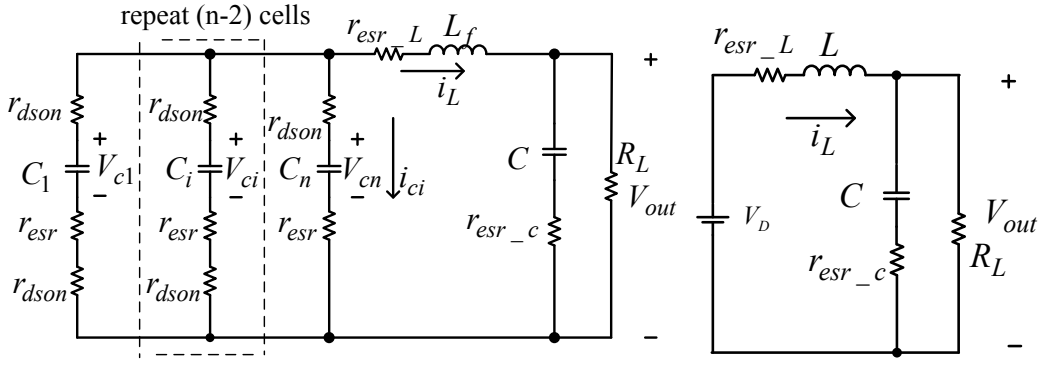
This section gives an analysis of the hybrid SC-buck converter, which involves two steps:

1. find the equivalent circuits of the converter corresponding to different operating states; and
2. analyze each equivalent circuit to optimize the overall operating efficiency.

3.3.1 State-space Equivalent Circuits



(a) State 1: Charging equivalent circuit

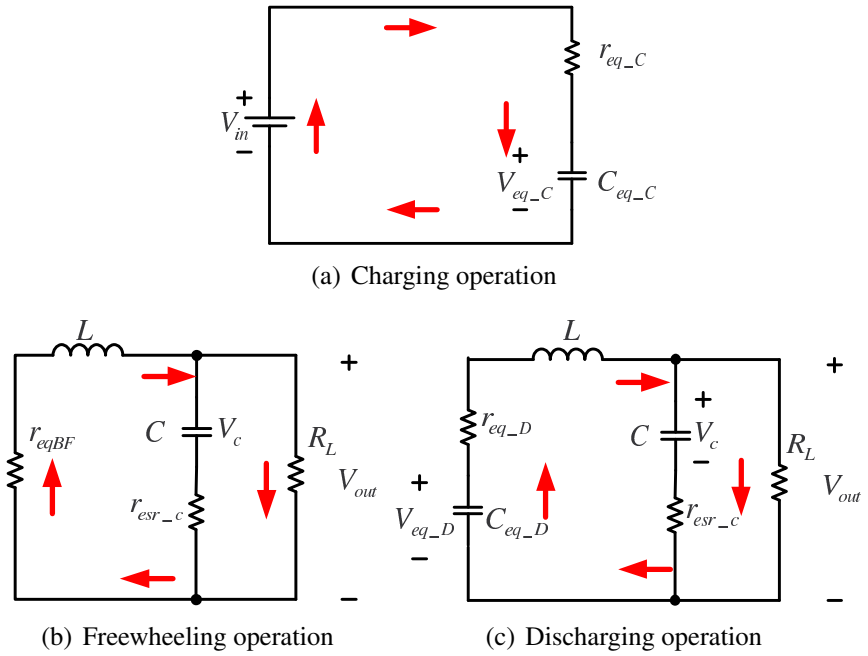


(b) State 2: Discharging equivalent circuit

(c) State 3: Dead-time state equivalent circuit

Figure 3.4: Equivalent circuit of the converter.

Generally, the on state of a power MOSFET is modeled as a resistance in the steady state. The practical inductor is modeled as an ideal inductor connected with an equivalent series resistor (ESR). Similarly, a practical capacitor is modeled as an ideal capacitor connected with an ESR.



(a) Charging operation

(b) Freewheeling operation

(c) Discharging operation

Figure 3.5: Simplified equivalent circuits of the charging, discharging and freewheeling operations of the SC-buck converter.

Using the above models, the equivalent circuits of State 1 and State 2 shown in Fig. 3.3 can be illustrated as given in Fig. 3.4(a) and Fig. 3.4(b), respectively, where r_{dson} is the turn-on resistance of the switch, r_{esr} is the ESR of each flying capacitor, r_{esr_C} is the ESR of the output capacitor C, and r_{esr_L} is the ESR of L. Considering the extremely short dead time, state 3 is neglect in the circuit analysis.

The circuit in Fig. 3.4(a) can be simplified to the circuits shown in Figs. 3.5(a) and 3.5(b). For Fig. 3.5(a), $C_{eq\_C} = C_1/n = C_{sum}/n^2$ and $r_{eq\_C} = n \cdot (r_{dson} + r_{esr})$. For Fig. 3.5(b), $r_{eqBF} = r_{dson} + r_{esr\_L}$.

Similarly, the parallel capacitors in Fig. 3.3(b) is modeled as an equivalent capacitor with a series connected resistor. Then a further simplified equivalent circuit is shown in Fig. 3.5(c). For Fig. 3.5(c), $C_{eq\_D} = n \cdot C_1 = C_{sum}/n$ and $r_{eq\_D} = (r_{dson} + r_{esr})/n$ by

neglecting the effect of unbalanced r_{dson} in one branch. Here, $C_{sum} = C_1 + \cdots + C_n$.

3.3.2 Energy Flow of Hybrid Switched-capacitor Converter

According to the simplified circuits in Fig. 3.5, the three circuits can be divided into two groups for stepwise efficiency calculations: the capacitor charging circuit (Fig. 3.5(a)) and the equivalent buck high-side switch 'ON' state (3.5(c)) and equivalent buck freewheeling state (3.5(b)). In the capacitor charging state, the energy is transferred to the flying capacitors from the voltage source. In the another circuit group, the energy stored in the flying capacitors discharged to the load through the equivalent buck circuit. Hence, the energy-flow mechanism of the SC-buck converter is illustrated as in Fig. 3.6. First, in State 1, energy is transferred from the power source V_{in} to the flying capacitors through the SC-stage with a "charging efficiency" of η_C. In this state, energy is temporarily stored in the flying capacitors. Then, in State 2, the energy stored in the capacitors will be transferred to the load through the buck-stage with a "discharging efficiency" of η_D. Averaged over a switching period, the energy in the flying capacitors is kept constant during steady state. The overall efficiency of SC-buck converter is the product of the charging efficiency and the discharging efficiency, i.e. $\eta_{\text{overall}} = \eta_C \cdot \eta_D$.

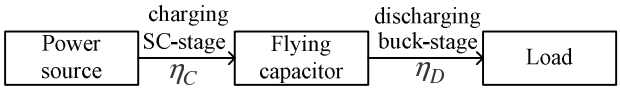


Figure 3.6: Energy-flow diagram of a SC-buck converter.

3.3.3 Charging Efficiency η_C

The charging efficiency η_C given by the energy-flow diagram in Fig. 3.6 can be obtained by analyzing the RC circuit as shown in Fig. 3.5(a). In this state, the energy stored in the flying capacitors will be transferred to the buck stage in the following state. The energy change would have an influence on the charging efficiency. The key point of calculating the charging efficiency is to obtain the initial voltage of the flying

capacitors. The method of deriving the charging efficiency of an equivalent RC circuit of an SC converter is given in [81]. Here, we apply the method to this converter.

According to the Fig. 3.5(a), there is

$$\begin{cases} i_c = C_{eq\_C}\frac{dV_{eq\_C}}{dt} \\ V_{in} = r_{eq\_C}\cdot i_c + V_{eq\_C} \end{cases}, \tag{3.1}$$

where i_c is the charging current.

Solving (3.1), the voltage across C_{eq_C} is

$$V_{eq\_C}(t) = V_{\text{in}}\left[1-(1-b)e^{-\frac{t}{\tau}}\right], \tag{3.2}$$

where $b = V_{eq\_C(i)}/V_{\text{in}}$, $\tau = r_{eq\_C}C_{eq\_C}$, and $V_{eq\_C(i)}$ is the initial voltage of the equivalent flying capacitor. The charging current is given as

$$i_c(t) = \frac{V_{in}(1-b)}{r_{eq\_C}}e^{-\frac{t}{\tau}}. \tag{3.3}$$

According to (3.3), the energy transferred from the power source is

$$\begin{aligned} E_{\text{in}}(t) &= -\int_0^t V_{in}i_{in}(t)dt = -\int_0^t V_{in}^2\frac{1-b}{r_{eq\_C}}e^{-\frac{t}{\tau}}dt \\ &= C_{eq\_C}V_{in}^2(1-b)(1-e^{-\frac{t}{\tau}}) \\ &= C_{eq\_C}V_{in}(V_{eq\_C}(t)-V_{eq\_C(i)}), \end{aligned} \tag{3.4}$$

and the total energy stored in C_{eq_C} in each switching period is

$$\Delta E_C(t) = \frac{1}{2}C_{eq\_C}\left(V_{eq\_C}^2(t)-V_{eq\_C(i)}^2\right). \tag{3.5}$$

Hence, the charging efficiency is

$$\eta_C(t) = \frac{E_C(t)}{E_{in}(t)} \times 100\% = \frac{\frac{1}{2}C_{eq\_C}\left(V_{eq\_C}^2(t) - V_{eq\_C(i)}^2\right)}{C_{eq\_C}V_{in}(V_{eq\_C}(t) - V_{eq\_C(i)})} = \frac{V_{eq\_C(t)} + V_{eq\_C(i)}}{2V_{in}}. \quad (3.6)$$

This stored energy will be discharged into the buck stage. We denote ΔE_T as the energy consumed by the buck stage in one period. Therefore, $\Delta E_C(T_{on}) = \Delta E_T$.

Assuming the input power of the buck stage of the SC-buck converter is P_{bin}. In one switching period, the input energy is

$$\Delta E_T = P_{\text{bin}}T = P_{\text{bin}}/f_S. \quad (3.7)$$

At steady state, for each period, the energy stored in C_{eq_C} is equal to this input energy, i.e., $\Delta E_C(T_{on}) = \Delta E_T$, giving

$$V_{eq\_C}^2(T_{on}) - V_{eq\_C(i)}^2 = \frac{2P_{\text{bin}}}{f_S C_{eq\_C}}. \quad (3.8)$$

By substituting (3.2) into (3.8) and solving the equation, we get

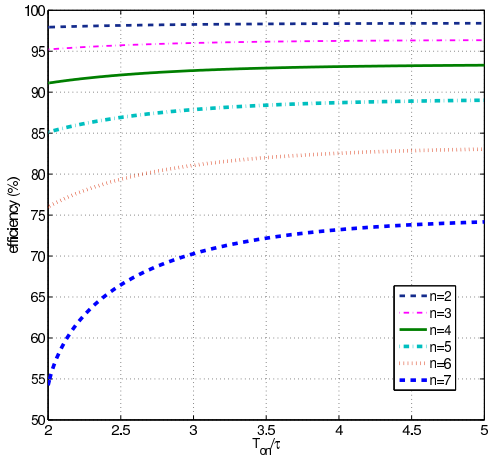
$$b = \frac{1}{1 + e^{-\frac{T_{on}}{\tau}}}\left[e^{-\frac{T_{\text{on}}}{\tau}} + \sqrt{1 - \frac{2P_{\text{bin}}(1 + e^{-\frac{T_{\text{on}}}{\tau}})}{f_S C_{eq\_C} V_{\text{in}}^2(1 - e^{-\frac{T_{on}}{\tau}})}}\right]. \quad (3.9)$$

By substituting $V_{eq\_C(i)} = bV_{\text{in}}$ into the charging efficiency equation (3.6), we get

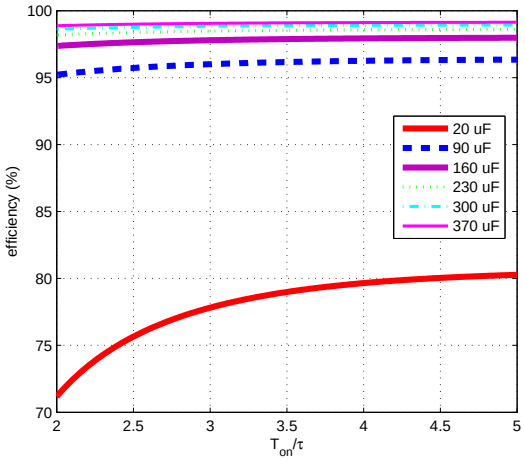
$$\eta_C = \frac{(1+b) - (1-b)e^{-\frac{T_{\text{on}}}{\tau}}}{2}. \quad (3.10)$$

Fig. 3.7(a) plots the charging efficiency obtained from (3.10) for different n of which the total capacitance is kept constant with $C_{\text{sum}} = 90$ μF at $P_{\text{bin}} = 20$ W and $f_S = 200$ kHz. Fig. 3.7(b) illustrates the charging efficiency for different values of C_{sum} at $f_s = 200$ kHz, $P_{\text{bin}} = 20$ W, $n = 3$, $V_{\text{in}} = 12$ V, and $V_o = 1$ V. Fig. 3.7(c) shows the charging efficiency for different P_{bin} at $f_s = 200$ kHz, $C_{\text{sum}} = 90$ μF, $n = 3$,

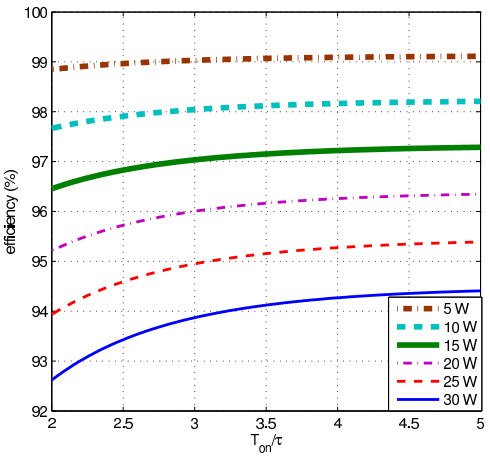
$V_{\text{in}} = 12$ V, and $V_o = 1$ V. Fig. 3.7(d) shows the charging efficiency for different switching frequency f_s with $C_{\text{sum}} = 90$ μF, $P_{bin} = 20$ W, $n = 3$, $V_{\text{in}} = 12$ V and $V_o = 1$ V.



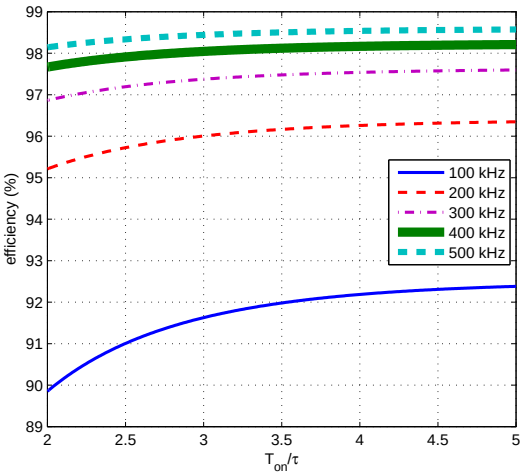
(a) Plot of calculated charging efficiency for different n.



(b) Plot of calculated charging efficiency for different C_{sum}.



(c) Plot of calculated charging efficiency for different P_{bin}.



(d) Plot of calculated charging efficiency for different switching frequency f_s.

Figure 3.7: Properties of SC-stage charging efficiency.

From the calculated results, the following conclusions can be deduced:

1. When the value of capacitor C_{sum} is fixed, having more flying capacitors gives a lower charging efficiency.

2. With a longer charging time T_{on} in (3.10), the charging efficiency η_C is higher.

3. A bigger C_{sum} value leads to a higher charging efficiency. However, the rate of increase in charging efficiency decreases with an increasing C_{sum}.

4. A heavier load gives a lower charging efficiency.

5. A faster switching frequency leads to a higher charging efficiency.

3.3.4 Discharging Efficiency η_D

The discharging efficiency of the SC-buck converter interacts with the buck stage of the converter, of which it is being used to process and deliver energy from the flying capacitors to the output. Our study shows that the buck-stage efficiency of the SC-buck converter is dominantly the efficiency of a conventional buck converter plus an additional parasitic capacitor charging loss that is not present in the buck converter. The power loss of buck converter is well documented in many papers. It includes the conduction loss, switching loss, and the ESR loss. In the SC-buck converter, the power loss includes the following losses.

3.3.4.1 Conduction Loss

i. Conduction loss on each SC stage switch:

$$\begin{cases} P_{c\_sw\_up} = R_{ds\text{on}} D \left(I_o^2 + \frac{\Delta I_L^2}{12} \right) & \text{(upper switch)} \\ P_{c\_sw\_dn} = R_{ds\text{on}} (1-D) \left(I_o^2 + \frac{\Delta I_L^2}{12} \right) & \text{(lower switch)} \end{cases}, \tag{3.11}$$

where I_o is the output current and ΔI_L is the inductor current ripple.

ii. Conduction loss on the buck-stage switches:

$$P_{c\_sw\_Sb} = R_{ds\text{on}} (1 - D - \frac{2T_{dt}}{T})(I_o^2 + \frac{\Delta I_L^2}{12}). \tag{3.12}$$

iii. Conduction loss on the body diode of buck-stage switch:

$$P_{c\_diode\_Sb} = 2f_S V_{fd} I_o T_{dt}, \tag{3.13}$$

where V_{fd} is the forward diode voltage of S_b and T_{dt} is the dead time. Thus, the total conduction loss is

$$P_c = nP_{c\_sw\_up} + (n-1)P_{c\_sw\_up} + P_{c\_sw\_Sb} + P_{c\_diode\_Sb}. \tag{3.14}$$

3.3.4.2 Switching Loss

i. Switching loss on switches of each branch, which includes the switching loss on the upper switches:

$$\begin{cases} P_{sw\_on\_up} = f_S V_{C\_on} I_{d\_on} \frac{t_{ri}+t_{fu}}{2} \\ P_{sw\_off\_up} = f_S V_{C\_off} I_{d\_off} \frac{t_{ru}+t_{fi}}{2} \end{cases}, \tag{3.15}$$

and the switching loss on the lower switches:

$$\begin{cases} P_{sw\_on\_dn} = f_S V_{C\_on} I_{d\_on} \frac{t_{ri}+t_{fu}}{2} \\ P_{sw\_off\_dn} = f_S V_{fd} I_{d\_off} \frac{t_{ru}+t_{fi}}{2} \end{cases}, \tag{3.16}$$

where I_{d_on} and I_{d_off} are branch currents of the capacitor when P is turned on and off respectively.

ii. Switching loss of the body diode of the buck-stage switch:

$$P_{sw\_diode\_Sb} = f_S C_{oss} V_{inb\_on}^2, \tag{3.17}$$

where V_{inb_on} is the voltage of flying capacitor when P is turned on. Thus, the

total switching loss is

$$P_{sw} = n(P_{sw\_on\_up} + P_{sw\_off\_up}) + (n+1) \times (P_{sw\_on\_dn} + P_{sw\_off\_dn}) + P_{sw\_diode\_Sb}. \quad (3.18)$$

3.3.4.3 ESR Loss

i. Loss on the ESR of inductor:

$$P_{esr\_L} = r_{esr\_L}(I_o^2 + \frac{\Delta I_L^2}{12}). \quad (3.19)$$

ii. Loss on the ESR of a flying capacitor:

$$P_{esr\_C} = r_{esr\_C} D(I_o^2 + \frac{\Delta I_L^2}{12}). \quad (3.20)$$

Thus, the total ESR loss is

$$P_{esr} = P_{esr\_L} + nP_{esr\_C}. \quad (3.21)$$

3.3.4.4 Parasitic Capacitor Charging Loss

When the SC-buck converter switches from State 3 to State 1, the voltage across all the P switches will change. This causes the parasitic capacitor of the P switches to charge up to a certain voltage level, generating an additional charging loss. Fig. 3.8 shows the simulation voltage and current waveforms of the SC-buck converter during the transition from State 3 to State 1, which introduces the additional power loss.

The equation describing the parasitic capacitor charging loss of each P switch is

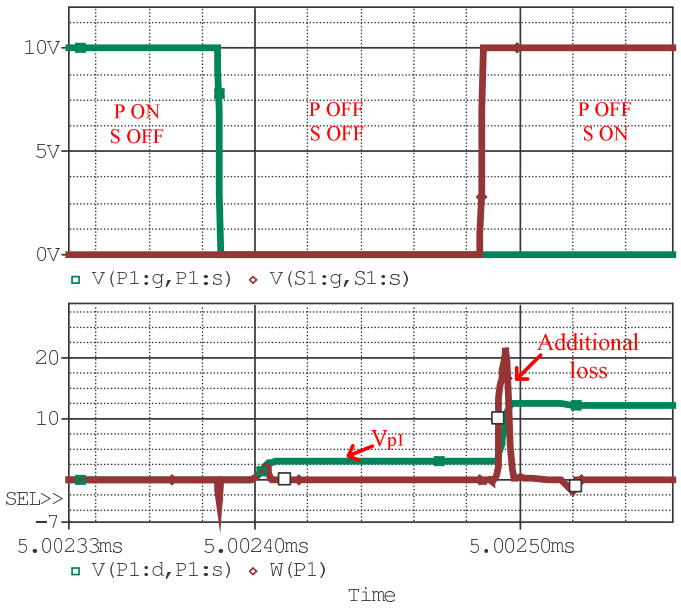


Figure 3.8: Waveforms of P switches during the transition from State 3 to State 1.

Table 3.1: Voltages of parallel switches at different states

	$S_{off}P_{on}$	$S_{off}P_{off}$	$S_{on}P_{off}$	$S_{off}P_{off}$
$V(P_1)$	0	V_{c1}	V_{in}	V_{in}
$V(P_3)$	0	V_{c2}	$V_{\text{in}} - V_{c1}$	$V_{\text{in}} - V_{c1}$
$\cdots$	0	$\cdots$	$\cdots$	$\cdots$
$V(P_{2n-1})$	0	V_{cn}	$V_{\text{in}} - V_{c1} - \cdots - V_{cn}$	$V_{\text{in}} - V_{c1} - \cdots - V_{cn}$
$V(P_2)$	0	V_D	$V_{c2} + \cdots + V_{cn}$	$V_{c2} + \cdots + V_{cn}$
$V(P_4)$	0	V_D	$V_{c3} + \cdots + V_{cn}$	$V_{c3} + \cdots + V_{cn}$
$\cdots$	0	V_D	$\cdots$	$\cdots$
$V(P_{2n})$	0	V_D	V_{cn}	V_{cn}

given as

$$\begin{cases} P_{ad\_up} = f_s C_{oss} V_{sw\_up}^2 \\ P_{ad\_dn} = f_s C_{oss} V_{sw\_dn}^2 \end{cases}, \tag{3.22}$$

where V_{sw_up} and V_{sw_dn} are respectively the voltages of the upper and lower switches of each branch. For n number of P switches, the parasitic capacitor charging loss is

$$P_{ad} = P_{ad\_up\_1} + \cdots + P_{ad\_up\_n} + P_{ad\_dn\_1} + \cdots + P_{ad\_dn\_(n-1)}. \tag{3.23}$$

Finally, the overall power loss of the buck-stage is

$$P_{dis\_loss} = P_c + P_{sw} + P_{esr} + P_{ad}. \tag{3.24}$$

Then, the discharging efficiency of the SC-buck converter is

$$\eta_D = \frac{P_o}{P_o + P_{dis\_loss}} \times 100\%. \tag{3.25}$$

3.4 Experimental Results

3.4.1 Experiment Results of SC-buck Converter

In order to verify the calculation method and the properties of the topology, a prototype has been built. The parameters are shown in Table 3.2. The driver circuit for the MOSFETs is shown in Fig. 3.9. The driver ICs used are MC33151 and MC33152. The isolated transformer is of magnetic powder core and the turn ratio is 22:22. The power meter is PM100 by Voltech company. An E-load with model number 3311c manufactured by Prodigit is used for the load. An input voltage filter of 330 μF electrolytic capacitor is connected for efficiency measurement. Fig. 3.10 shows the output voltage waveform of a SC-buck converter with 5 flying capacitors ($n = 5$) under a constant load of 15 A. In comparison to the flying capacitor voltage of the first-stage SC converter, the final output voltage waveform of the SC-buck converter contains a much smaller voltage ripple.

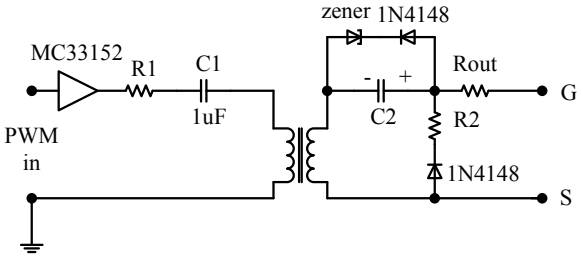


Figure 3.9: Driver circuit for the MOSFETs of the SC circuit.

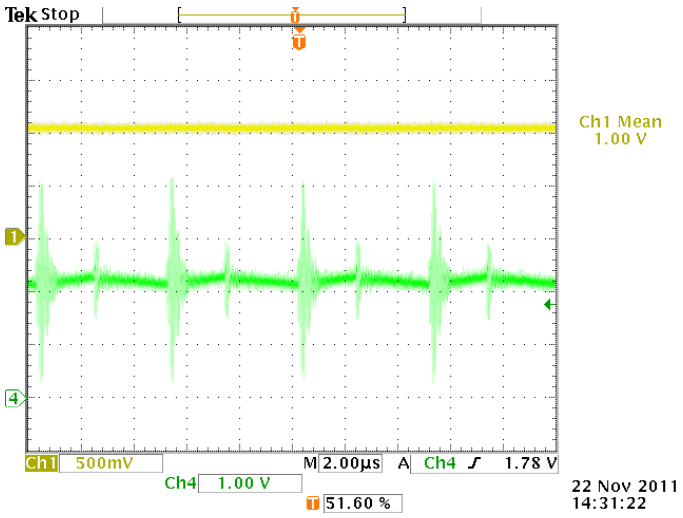


Figure 3.10: Output voltage waveform of a SC-buck converter with 5 flying capacitors ($n = 5$) (Ch1: buck output voltage; Ch4: SC flying capacitor voltage).

Fig. 3.11 gives the experimental efficiency curves at various output power levels using a different n. The results show that there is a best n to achieve a highest efficiency at different loading conditions.

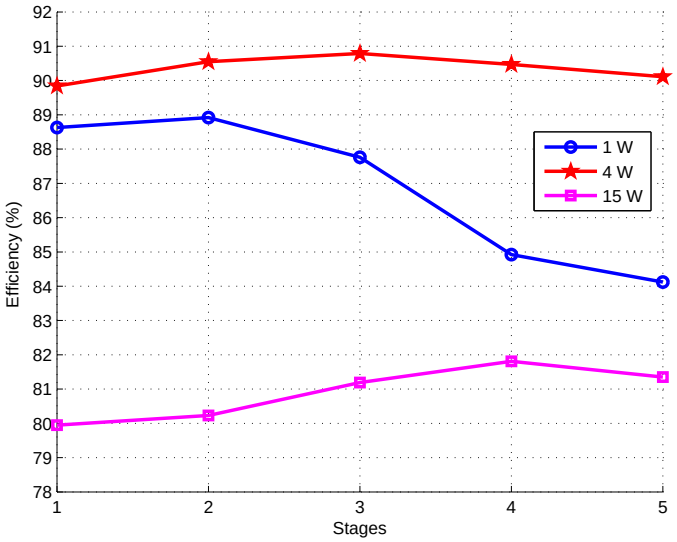


Figure 3.11: Experimental result of the SC-buck converter for 1 W, 4 W, and 15 W loading with different n.

3.4.2 Control Mechanism of the SC-buck Converter

As the buck stage of the SC-buck converter is switching between the freewheeling as in Fig 3.5(b) and the discharging as in Fig 3.5(c) operations, it behaves similarly to a simple duty-cycle controlled buck converter. Hence, only an ordinary voltage-mode controller will be needed for the control of the buck stage of the SC-buck converter. With this controller, the compensator can be designed using the pole placement approach. For this work, the adopted controller has a compensation network with the transfer function $G_c(s) = 5 + \frac{1}{0.00039s}$. Fig. 3.12 shows the implementation circuit of the compensation network used in the experimental prototype.

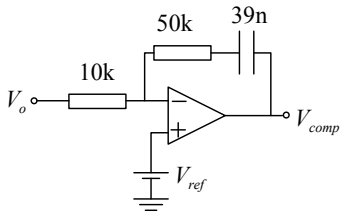


Figure 3.12: Compensation circuit of the controller in the experimental prototype.

Fig. 3.13 depicts the closed-loop output voltage waveforms of the SC-buck converter operating with an active load switching between 0 A and 5 A, showing that ordinary voltage-mode control can be applied to the SC-buck converter with good result.

3.4.3 Experiment Comparison with the Calculation Result

Fig. 3.14 gives a comparison of the calculated efficiencies and the experimental efficiencies at various output power levels and value of n. The efficiency curves fit well at higher power levels. The small discrepancy at lower power levels may be due to the relative higher measurement error at the lower power levels.

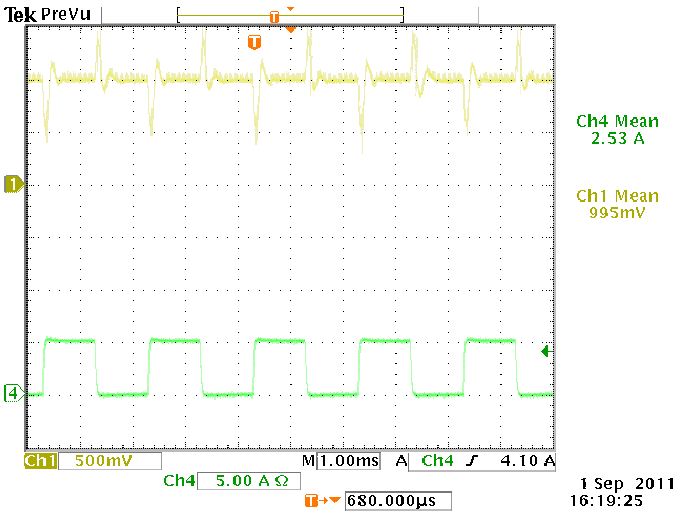
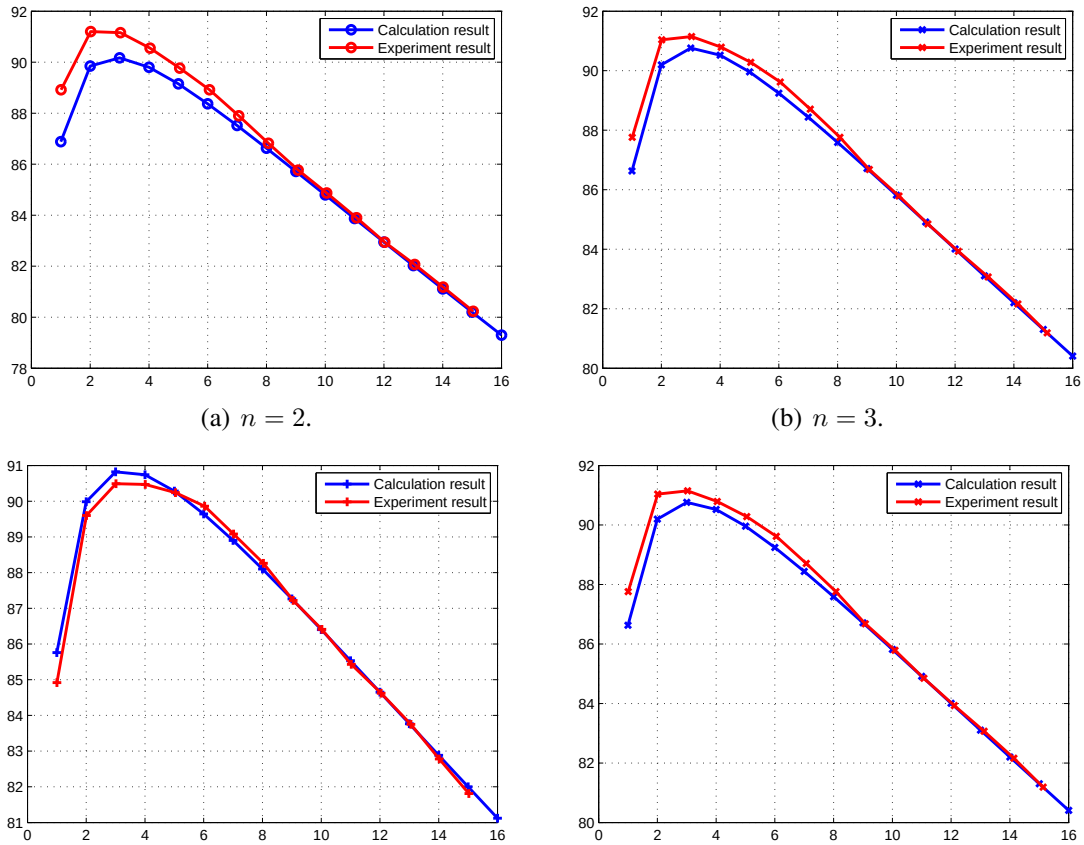


Figure 3.13: Output voltage waveform of the proposed converter with closed-loop control with an active load switching between 0 A and 5 A (Ch1: Output voltage; Ch4: Output current).



(a) $n = 2$. (b) $n = 3$.

(c) $n = 4$. (d) $n = 5$.

Figure 3.14: Plots of the experimentally measured efficiencies and calculated efficiencies for the SC-buck converter with (a) $n = 2$, (b) $n = 3$, (c) $n = 4$ and (d) $n = 5$.

3.4.4 Efficiency Comparison Between SC-buck and Single Buck Converter

Table 3.2: Parameters of SC-Buck Converter

V_{in} & V_{o}	f_S	MOSFET
12 V & 1 V	200 kHz	Si7356ADP
$C_1, C_2 \cdots C_n$	L	C
94 μF	13 μH	410 μF

A prototype based on the SC-buck topology ($n = 2, 3, 4$) given in Fig. 3.2 and parameters given Table 3.2 is constructed. The number n can be modified by connecting or bypassing the single-cell structure depicted in Fig. 3.2(c). Experiment is performed to compare the performance of this converter against a conventional buck converter. Both the buck converters have the same C and f_S. Operating at the same 12 V input and 1 V output condition, it can be seen from Fig. 3.15 that the SC-buck converter gives a better efficiency than the conventional buck converter, except when it is at very light-load condition, similar to what has been reported in [19, 20]. From Fig. 3.15, it is observed that a higher n of SC-buck converter always give a better efficiency at heavy load. However, depending on the loading condition, there is an optimal n that allows the SC-buck converter to achieve the best possible efficiency.

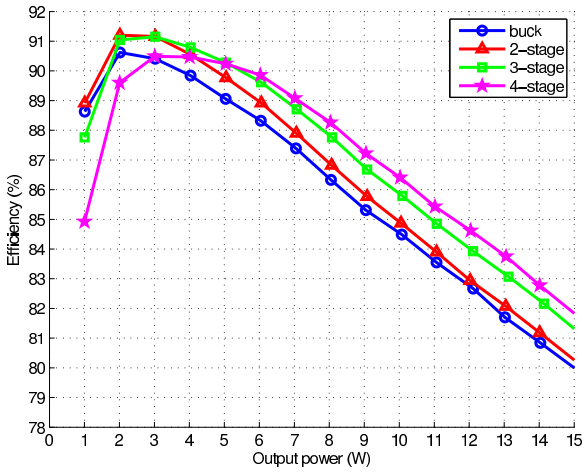


Figure 3.15: Comparison of experimentally measured efficiencies among SC-buck converters with $n = 2, 3, 4$ and a buck converter (i.e., n = 1).

Table 3.3: Comparison of different stages SC-Buck converter components used

Stages	Buck	2-stage	3-stage	$\cdots$	n-stage
Switches	2	6	6	$\cdots$	$3n$
Flying capacitors	none	2	3	$\cdots$	n
Inductor	1	1	1	$\cdots$	1
Output Capacitor	1	1	1	$\cdots$	1

3.5 Design and Optimization of the Hybrid Switched-Capacitor Buck Converter

Four parameters are needed to start a design: input voltage (V_{in}), output voltage (V_o), maximum output current (I_{o_Max}) and the switching frequency (f_s). With theses parameters, the design of the converter circuit can be carried out based on the number of capacitor n chosen, as given in the following subsection.

3.5.1 Components Selection

i. *Inductor:* Assuming that the switch of the buck is ideal, then

$$L = V_o \cdot (1 - \frac{V_o}{V_{\text{in}}}) \cdot \frac{1}{f_s} \frac{1}{\Delta I_L}. \tag{3.26}$$

where $\Delta I_L = p \cdot I_{o\_Max}$, and p is typically chosen as 0.3.

ii. *Output capacitor:* The output capacitor dictates the ripple of output voltage. The output voltage ripple is

$$\Delta V_o = \Delta I_L \cdot (ESR + \Delta T / C_o). \tag{3.27}$$

Rearranging (3.27), we have

$$C_o = \frac{\Delta T}{\frac{\Delta V_o}{\Delta I_L} - ESR}, \tag{3.28}$$

where $\Delta T = \max\left\{\frac{V_o}{V_{\text{in}}} \cdot \frac{1}{f_s}, (1 - \frac{V_o}{V_{\text{in}}}) \cdot \frac{1}{f_s}\right\}$, and ESR is the equivalent series resistance of output capacitor. Using (3.28), the value of the output capacitor is determined. Typically, the output voltage ripple is mainly contributed by the ESR of output capacitor.

iii. *Flying capacitor:* A proper value of the flying capacitor will improve the charging efficiency. Equation (3.9) gives the initial voltage b, which indicates the minimum voltage of the flying capacitors. Furthermore, it also dictates the charging efficiency. To obtain a high charging efficiency, b should be higher than 0.95. Although (3.9) can give an exact value of the flying capacitor, it is difficult to solve. A simplified version of this equation is desired. Assume the discharging efficiency is 100%. Then,

$$P_{o\_Max} = \frac{1}{2} f_s \cdot C_{\text{sum}} \cdot (\frac{V_{\text{in}}}{n} - \Delta V_f) \cdot \Delta V_f, \tag{3.29}$$

where ΔV_f is the voltage drop of flying capacitors. In (3.29), ΔV_f is relatively low compared with $\frac{V_{\text{in}}}{n}$. So, (3.29) can be simplified as

$$P_{o\_Max} = \frac{1}{2} f_s \cdot C_{\text{sum}} \cdot \frac{V_{\text{in}}}{n} \cdot \Delta V_f. \tag{3.30}$$

By rearranging (3.30) and setting $\Delta V_f = (1 - b) \cdot \frac{V_{\text{in}}}{n}$, the flying capacitor can be simplified as

$$C_{\text{sum}} = \frac{2 \cdot n^2 \cdot V_o \cdot I_{o\_Max}}{(1 - b) \cdot f_s \cdot V_{\text{in}}^2}. \tag{3.31}$$

iv. *Switch:* Essentially, the maximum voltage and current ratings of the switches can be determined using a scaling function of n multiplied by V_{in} or I_o, as shown in Table 3.4. Most of the scaling functions are simple factors of n. However, the charging currents passing through the switches ($S_1 \cdots S_n$) are controlled by the circuit. The maximum current passing through these switches is

$$I_{\max} = \frac{\Delta V_f}{R_{d\text{son}}}. \tag{3.32}$$

The parameter $R_{d\text{son}}$ not only affects the maximum charging current, but also dictates the time constant τ, which affects the charging time. In order to have a high charging efficiency, the charging time should be at least three times higher than the time constant τ. So,

$$R_{d\text{son}} = \frac{n}{3} \cdot \frac{1}{C_{\text{sum}}} \cdot (1 - \frac{n \cdot V_o}{V_{\text{in}}}) \cdot \frac{1}{f_s}. \tag{3.33}$$

Substitute (3.33) into (3.32), the maximum current passing through the switches $(S_1 \cdots S_n)$ is given as

$$I_{\max} = \frac{3 f_s C_{\text{sum}} \Delta V_f}{n \cdot (1 - \frac{n \cdot V_o}{V_{\text{in}}})}. \tag{3.34}$$

Table 3.4: Component parameters

Stages		2-stage	3-stage	$\cdots$	n-stage
Inductor		$V_o \cdot (1 - \frac{2 \cdot V_o}{V_{\text{in}}}) \cdot \frac{1}{f_s} \cdot \frac{1}{\Delta I_L}$	$V_o \cdot (1 - \frac{3 \cdot V_o}{V_{\text{in}}}) \cdot \frac{1}{f_s} \cdot \frac{1}{\Delta I_L}$	$\cdots$	$V_o \cdot (1 - \frac{n \cdot V_o}{V_{\text{in}}}) \cdot \frac{1}{f_s} \cdot \frac{1}{\Delta I_L}$
Output capacitor		$\frac{\max\{\frac{V_o}{V_{\text{in}}} \cdot \frac{1}{f_s}, (1 - \frac{V_o}{V_{\text{in}}}) \cdot \frac{1}{f_s}\}}{\frac{\Delta V_o}{\Delta I_L} - ESR}$	$\frac{\max\{\frac{V_o}{V_{\text{in}}} \cdot \frac{1}{f_s}, (1 - \frac{V_o}{V_{\text{in}}}) \cdot \frac{1}{f_s}\}}{\frac{\Delta V_o}{\Delta I_L} - ESR}$	$\cdots$	$\frac{\max\{\frac{V_o}{V_{\text{in}}} \cdot \frac{1}{f_s}, (1 - \frac{V_o}{V_{\text{in}}}) \cdot \frac{1}{f_s}\}}{\frac{\Delta V_o}{\Delta I_L} - ESR}$
Flying Capacitors		$\frac{4 \cdot V_o \cdot I_{o\_Max}}{(1-b) \cdot f_s \cdot V_{\text{in}}^2}$	$\frac{6 \cdot V_o \cdot I_{o\_Max}}{(1-b) \cdot f_s \cdot V_{\text{in}}^2}$	$\cdots$	$\frac{2 \cdot n \cdot V_o \cdot I_{o\_Max}}{(1-b) \cdot f_s \cdot V_{\text{in}}^2}$
Switch S_1:	$V_{\max}$	$\frac{1}{2} \cdot V_{\text{in}}$	$\frac{2}{3} \cdot V_{\text{in}}$	$\cdots$	$\frac{n-1}{n} \cdot V_{\text{in}}$
	$I_{\max}$	$\frac{3 f_s C_{sum} \Delta V_f}{2 \cdot (1 - \frac{2 \cdot V_o}{V_{\text{in}}})}$	$\frac{f_s C_{sum} \Delta V_f}{(1 - \frac{3 \cdot V_o}{V_{\text{in}}})}$	$\cdots$	$\frac{3 f_s C_{sum} \Delta V_f}{n \cdot (1 - \frac{n \cdot V_o}{V_{\text{in}}})}$
Switch S_i, $(i = 2 \cdots n)$.	$V_{\max}$	$\frac{1}{2} \cdot V_{\text{in}}$	$\frac{1}{3} \cdot V_{\text{in}}$	$\cdots$	$\frac{1}{n} \cdot V_{\text{in}}$
	$I_{\max}$	$\frac{3 f_s C_{sum} \Delta V_f}{2 \cdot (1 - \frac{2 \cdot V_o}{V_{\text{in}}})}$	$\frac{f_s C_{sum} \Delta V_f}{(1 - \frac{3 \cdot V_o}{V_{\text{in}}})}$	$\cdots$	$\frac{3 f_s C_{sum} \Delta V_f}{n \cdot (1 - \frac{n \cdot V_o}{V_{\text{in}}})}$
Switch S_b:	$V_{\max}$	$\frac{1}{2} \cdot V_{\text{in}}$	$\frac{1}{3} \cdot V_{\text{in}}$	$\cdots$	$\frac{1}{n} \cdot V_{\text{in}}$
	$i_{\max}$	I_o	I_o	$\cdots$	I_o
Switch P_1:	$V_{\max}$	V_{in}	V_{in}	$\cdots$	V_{in}
	$I_{\max}$	$\frac{1}{2} \cdot I_o$	$\frac{1}{3} \cdot I_o$	$\cdots$	$\frac{1}{n} \cdot I_o$
Switch P_{2i-1}, $(i = 2 \cdots n)$.	$V_{\max}$	$\frac{n-i+1}{2} \cdot V_{\text{in}}$	$\frac{n-i+1}{3} \cdot V_{\text{in}}$	$\cdots$	$\frac{n-i+1}{n} \cdot V_{\text{in}}$
	$I_{\max}$	$\frac{1}{2} \cdot I_o$	$\frac{1}{3} \cdot I_o$	$\cdots$	$\frac{1}{n} \cdot I_o$
Switch P_2:	$V_{\max}$	$\frac{1}{2} \cdot V_{\text{in}}$	$\frac{2}{3} \cdot V_{\text{in}}$	$\cdots$	$\frac{n-1}{n} \cdot V_{\text{in}}$
	$I_{\max}$	$\frac{1}{2} \cdot I_o$	$\frac{1}{3} \cdot I_o$	$\cdots$	$\frac{1}{n} \cdot I_o$
Switch P_{2i}, $(i = 2 \cdots n-1)$.	$V_{\max}$	$\frac{n-i}{2} \cdot V_{\text{in}}$	$\frac{n-i}{3} \cdot V_{\in}$	$\cdots$	$\frac{n-i}{n} \cdot V_{\text{in}}$
	$I_{\max}$	$\frac{1}{2} \cdot I_o$	$\frac{1}{3} \cdot I_o$	$\cdots$	$\frac{1}{n} \cdot I_o$

3.5.2 Design and Optimization of the SC-buck Converter

In the previous subsection, methods of selecting the components have been introduced. Here, the design and optimization procedure will be given as follows.

1. Preset the four design specifications of input voltage ($V_{\rm in}$), output voltage (V_o), maximum output current ($I_{o\_\rm Max}$) and the switching frequency (f_s).
2. The maximum number of stages $n_{\rm max} = \rm floor(\frac{V_{in}}{V_o})$ is calculated.
3. For $n = 2$ to $n_{\rm max}$, components are selected as illustrated in Subsection 3.5.1. A best efficiency of this n at a particular loading condition can be found as illustrated in Section 3.3.
4. Based on the results of different n's, an optimal n can be obtained.

3.6 Conclusion

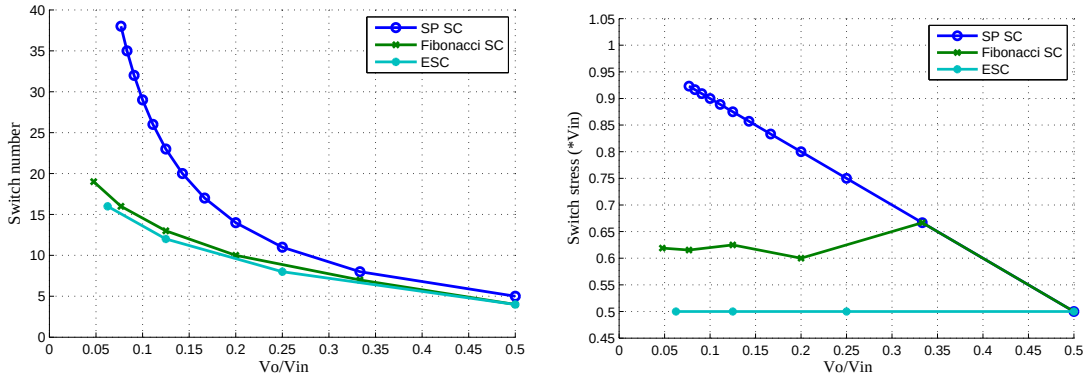
This chapter presents an analysis on the effect of having different number of flying capacitors n in the first-stage SC circuit of an improved SC-buck converter for high-voltage-gain conversion. The analysis shows that a higher n in the SC stage with the same overall capacitance leads to a lower charging efficiency. On the other hand, the buck-stage efficiency depends on the operating conditions and design parameters. A higher n leads to a higher discharging efficiency. Since the overall efficiency is the multiplication of the charging efficiency and the discharging efficiency, there will be an optimal n in terms of efficiency for each switched-capacitor buck converter at a particular load. The experimental results confirms the analytical findings. As such, a design and optimization procedure is developed for the hybrid switched-capacitor buck converter for choosing the optimal n. It is also shown that the converter can easily be controlled using ordinary voltage-mode control for buck converter.

Chapter 4

A Family of Exponential Switched-capacitor Converter

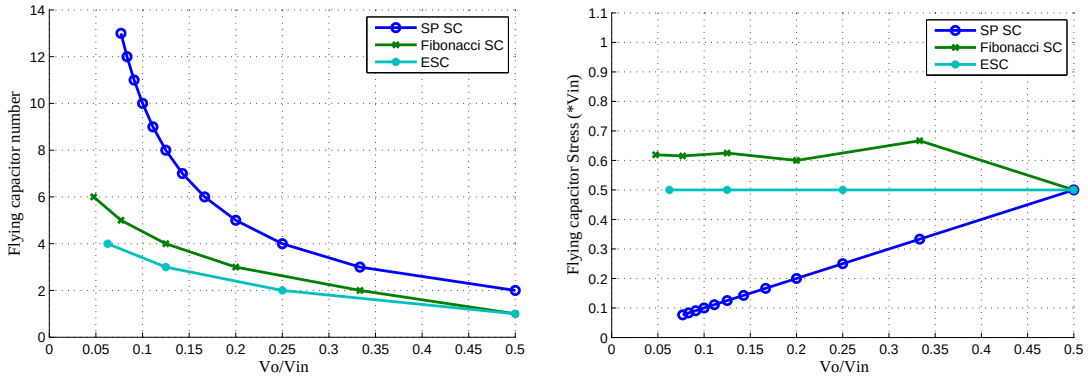
4.1 Introduction

Considering the demand of LVG step-down converters in the market, it is difficult to achieve the step-down requirement with good efficiency for a single-stage buck converter. The two-stage converter has been an effective solution for high-voltage-conversion step-down applications. The trend of two-stage converter is to use SC converter as the first-stage converter. Step-down SC topologies have been introduced in Chapter 2. However, SC converters consume a large number of capacitors and switches. Even using the Fibonacci SC converter, which is the most components saving SC converter [45], still uses a large number of components when the voltage conversion is high. Hence, a LVG SC converter with lower number of components is demanded. In this chapter, a family of exponential voltage step-down switched-capacitor (ESC) converters is proposed for solving the issue. Figs. 4.1 and 4.2 compare the number of switches, the number of capacitors, and the voltage stresses among the step-down SP SC, Fibonacci SC and proposed SC converters.



(a) (b)

Figure 4.1: Comparison of the switch (a) number and (b) maximum voltage stress among SP SC, Fibonacci SC and proposed ESC converters.



(a) (b)

Figure 4.2: Comparison of the flying capacitor (a) number and (b) maximum voltage stress among SP SC, Fibonacci SC and proposed ESC converters.

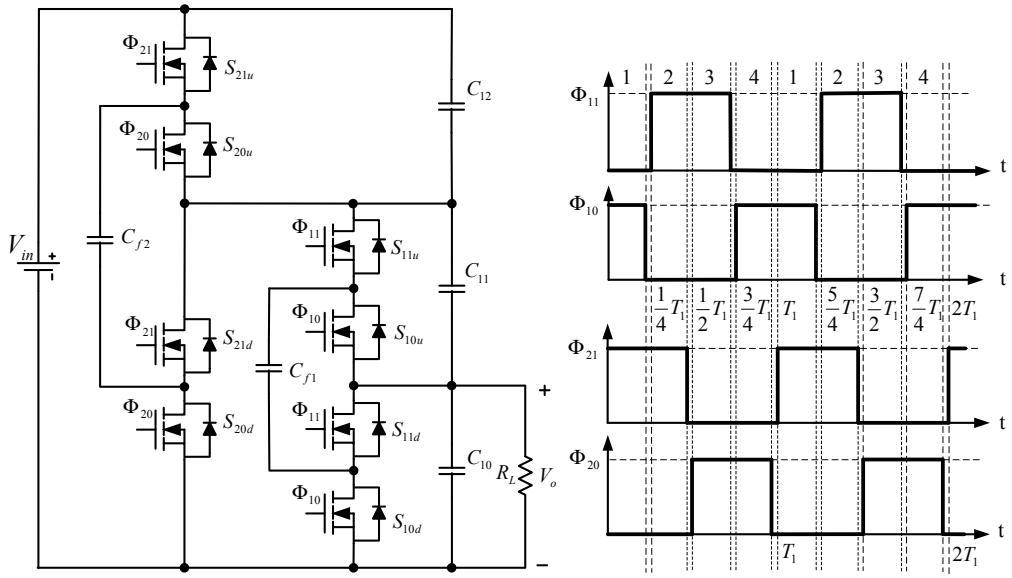
The efficiency figure is a very important performance parameter of a power converter. Hence, technique for efficiency analysis is demanded before a converter is actually designed. Papers [65, 78] give a calculation technique for the efficiency analysis of series-parallel SC converter. However, this technique cannot be used in this newly proposed ESC converter.

To obtain the efficiency information for a number of capacitors, the capacitor voltage has been assumed linear by designing the converter using a switching frequency

much higher than the reciprocal of the time constant of the switch topology [69, 71]. Then, traditional state-space averaging technique used in PWM converters was used. However, the technique cannot be used for the analysis when the time constants of the state variables are close to the switching period of the SC converter.

To solve this problem, the flying capacitors can be designed with identical components and the SC converter circuit can thus be readily simplified in its state-space operations as a set of first- or second-order RC networks. An average-current-based conduction loss model for the SC converter has been proposed in [89, 90]. Using some approximations, the model has successfully reduced each operation state of the SC converter into an equivalent first-order RC network which greatly simplifies the efficiency analysis of the original SC converter. Alternatively, without the calculation of the averaged current, RC networks of up to second order are used for the calculation of the efficiency of SC converters in [78, 81]. However, the family of ESC converters proposed in this paper has state-space RC subcircuits of order higher than two depending on the voltage step-down requirement. Therefore, a mathematical tool for the accurate calculation of efficiency of the ESC converter will be developed in this chapter.

4.2 Topology and Operation of the Exponential Switched-capacitor Converter



(a) Topology (b) Timing diagram

Figure 4.3: Proposed SC converter and its timing diagram.

In this section, a topology of exponential switched-capacitor step-down converter is introduced. Its topology and timing diagram is shown in Fig. 4.3. For this proposed converter, the output voltage is a quarter of the input voltage, i.e. $V_o = \frac{V_{in}}{4}$. In this SC converter, it is composed of two-stage structures, which are first-stage structure including bypass capacitors C_{10} and C_{11}, flying capacitor C_{f1} and switches S_{11u}, S_{10u}, S_{11d} and S_{10d}, and second-stage structure including bypass capacitor C_{12}, flying capacitor C_{f2} and switches S_{21u}, S_{20u}, S_{21d} and S_{20d}. The two structures are controlled by two signal groups, which are shown in Fig. 4.3(b), of ϕ_{10}, ϕ_{11} and ϕ_{20}, ϕ_{21}, respectively. As shown in the timing diagram, duty ratio of each signal is 0.5 and the first-stage structure timing (ϕ_{10}, ϕ_{11}) has a phase delay of $\frac{T}{4}$ relative to the second-stage structure timing (ϕ_{20}, ϕ_{21}). In the converter, the second-stage structure steps down the input voltage to a half, and the first-stage structure further steps down the half voltage into a quarter of

the input voltage.

According to the timing diagram shown in the Fig. 4.3(b), four main operating states of the SC converter are obtained and shown in Fig. 4.4, neglecting the much shorter deadtime state as indicated in Fig. 4.4. With reference to Fig. 4.4, the flying capacitor C_{f1} is in parallel with C_{11} in states 2, 3 and with C_{10} in states 1, 4. While the flying capacitor C_{f2} is in parallel with C_{12} in states 1, 2 and with the input of the next stage circuitry in states 3, 4.

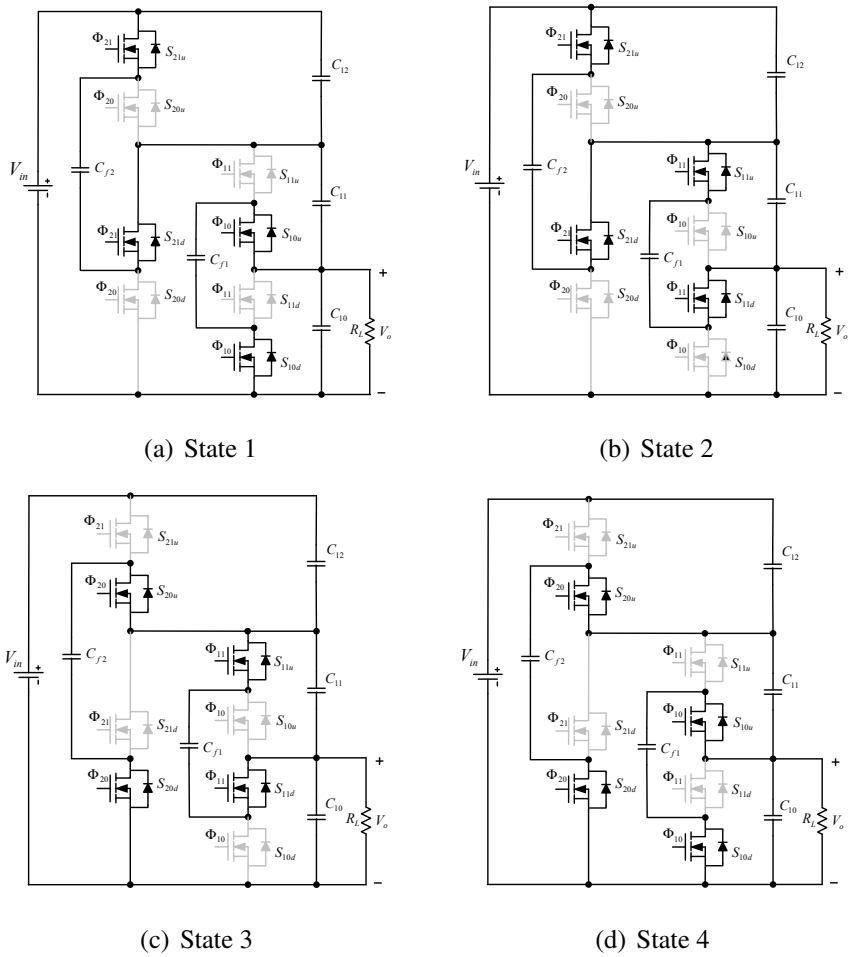


Figure 4.4: Four main states of the proposed SC converter.

A SPICE model of the exponential SC converter as shown in Fig. 4.5 with simulation parameters shown in Table 4.1 is built. The simulation results are shown in Fig. 4.6. The simulation results in Fig. 4.6(a) show that voltages of the first-stage structures are

close to a quarter of the input voltage, and the voltage of the lower bypass capacitor, C_{10}, is always lower than the voltage of higher bypass capacitor C_{11}. The voltage of the flying capacitor is always in between the voltages of the two bypass capacitors. Similarly, the voltages of capacitors in the second-stage structure are always near to a half of the input voltage. The voltage of the bypass capacitor, C_{12}, is always higher than the sum of the voltages of the first-stage bypass capacitors C_{10} and C_{11}. The voltage of the flying capacitor C_{f2} in the second-stage structure is always in between the bypass capacitor C_{12} and the sum of the bypass capacitors C_{10} and C_{11}.

Table 4.1: Simulation parameters of the proposed SC converter

Switching frequency f_s	200 kHz
flying caps C_{f1}, C_{f2}	94 μF
Capacitors C_1, C_2, C_3	188 μF
Input voltage	20 V
R_L	10 Ω
Switches	NTMFS4897

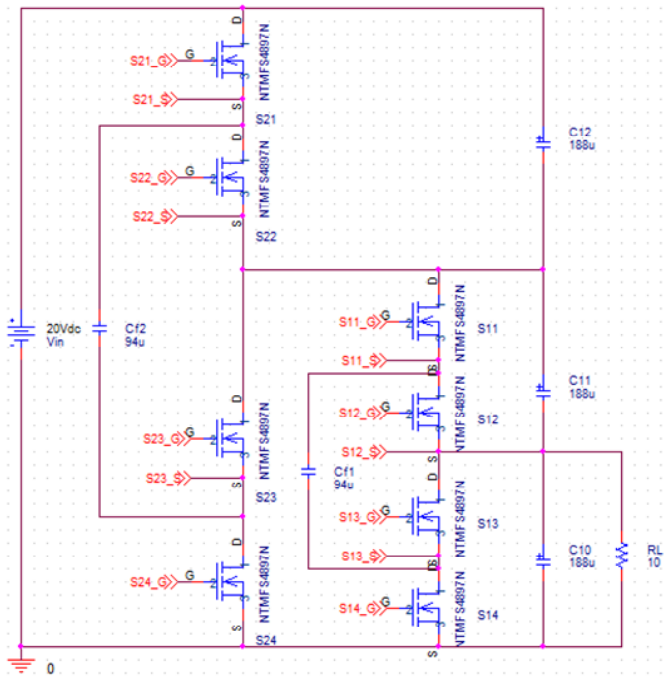
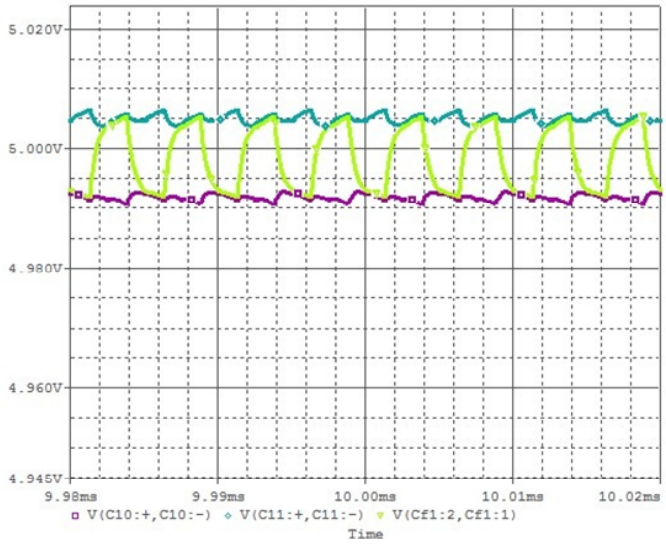
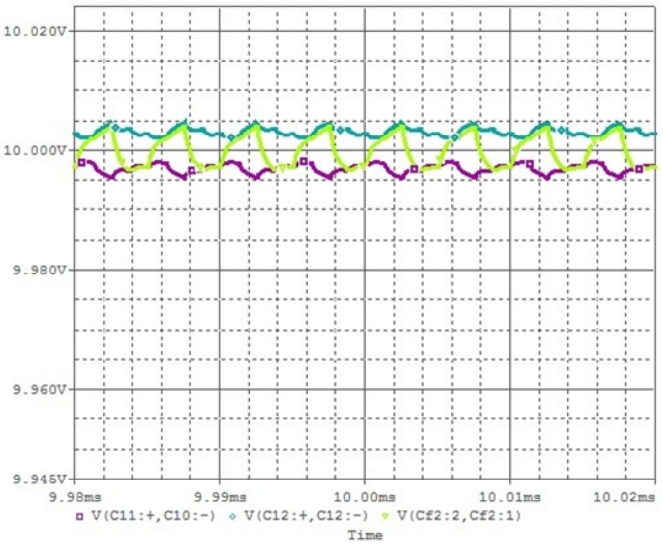


Figure 4.5: Simulation topology of exponential SC converter



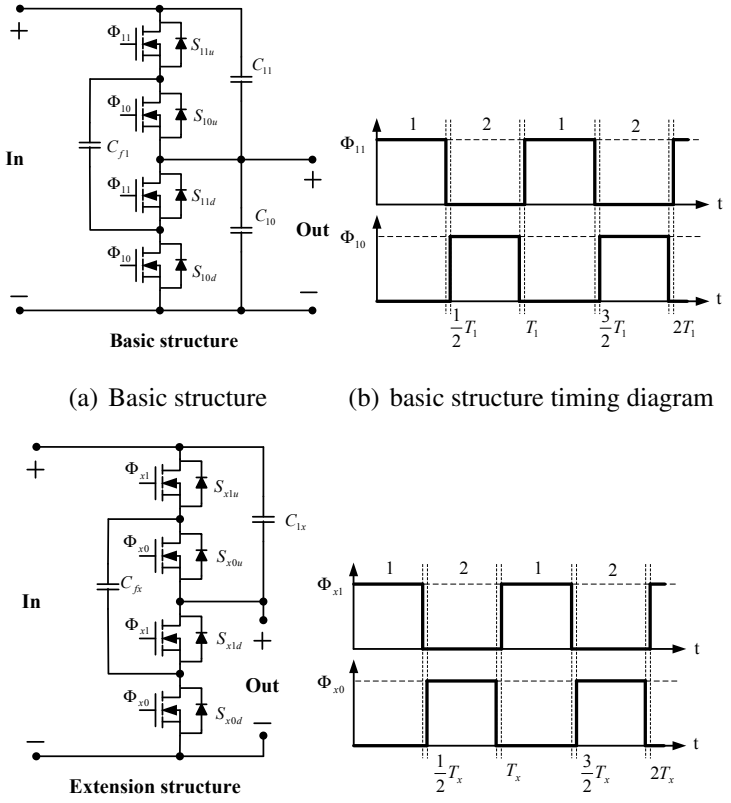
(a) Waveforms from top to bottom: V_{11}, V_{f1} and V_{10}.



(b) Waveforms from top to bottom: V_{12}, V_{f2} and $V_{11} + V_{10}$.

Figure 4.6: Simulation waveforms of each capacitor of the proposed SC converter.

4.3 Generalized Exponential Switched-capacitor Converter



(a) Basic structure (b) basic structure timing diagram

(c) Extension structure (d) Extension structure timing diagram

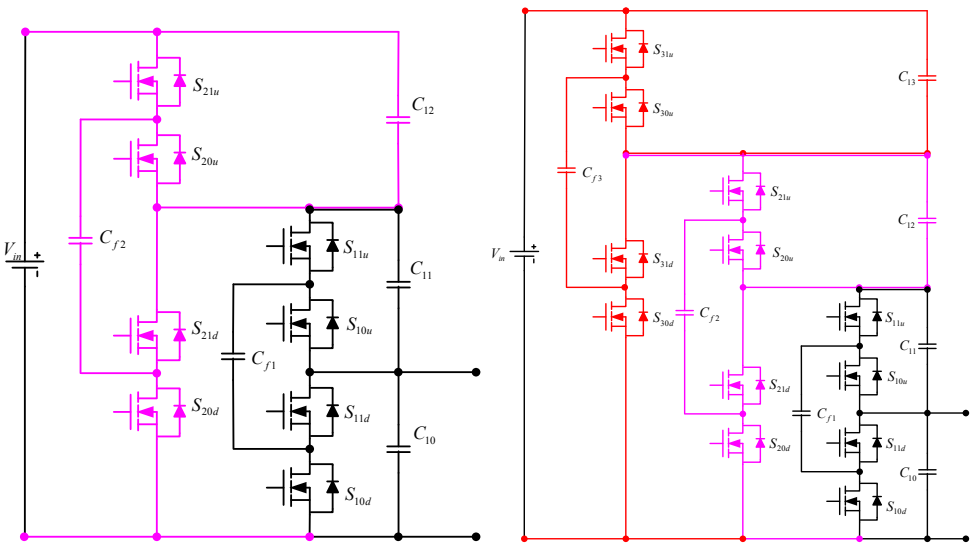
Figure 4.7: Generalized exponential SC converter's structures.

By comparing the proposed exponential SC converter topology shown in Fig. 4.3 with the voltage divider shown in Fig. 2.3, which is redrawn as the basic structure shown in Fig. 4.7(a) [43], the exponential SC converter is the voltage divider plus a second-stage structure. Here, the second-stage structure is defined as an extended structure as shown in Fig. 4.7(c). A general exponential SC converter is proposed by repeatedly applying the extension structure to a basic structure, which forms a series of exponential SC converters. The conversion ratio is $V_o = \frac{V_{in}}{2^n}$, where $n-1$ is the number of the

extension structures. Here, the exponential SC converter is called n^{th} order exponential SC for it is the number of basic structures and the order number of the conversion ratio $\frac{1}{2}$ as in (4.1). Fig. 4.8 shows the second-order and third-order exponential SC converters.

$$V_o = \left(\frac{1}{2}\right)^n V_{\text{in}}. \tag{4.1}$$

The control of each-stage structure can be varying from the same switching frequency to different switching frequencies. In this chapter, the constant frequency interleaved control method shown in Fig. 4.3(b) can be easily generalized to the n^{th}-order ESC converter. Each structure of the ESC converter is switching at a period of T. The timing (ϕ_{k1}, ϕ_{k2}) of the k^{th} structure has a phase delay of $\frac{T}{2n}$ relative to the timing of the $(k-1)^{\text{th}}$ structure, where $k = 2, 3, \cdots, n$.



(a) Second-order exponential SC converter. (b) Third-order exponential SC converter.

Figure 4.8: Generalized exponential SC converter.

4.4 Analysis of the Exponential Switched-capacitor Converter

Efficiency analysis is important for the design of an SC converter. Usually, state-space averaging is effective for the analysis of pulse-width-modulated power electronic converters, where the time constants of state variables are designed to be much longer than the reciprocal of the switching frequency and can be regarded as piece-wise linear within a switching period [67–69, 71]. The piece-wise-linear property of the state variables allows local linear averaging within each sub-state followed by an overall duty-cycle-weighted averaging of all sub-states to obtain an averaged system equation for a switching period. The state-space-averaged system equation is often considered as being continuous for the frequencies interested. However, state-space averaging cannot be directly applied to the switched-capacitor converter for the reason that the time constants of state variables are close to the switching period, and therefore, state variables are exponentially varying.

Although a full analytical equation can be difficult to obtain, this chapter prepares a discrete-time analysis formulated for high order capacitor circuits which can be difficult to analyze using methods in [78, 80, 81, 83, 86, 89, 90]. The discrete time analysis can be accurate by using a sufficiently small discrete time interval. The formulation will be illustrated as follows.

4.4.1 Discrete-time Analysis

Considering the time-varying capacitor voltage as shown in Fig. 4.9, the state equation is given as

$$I(t) = C\frac{dV(t)}{dt}, \tag{4.2}$$

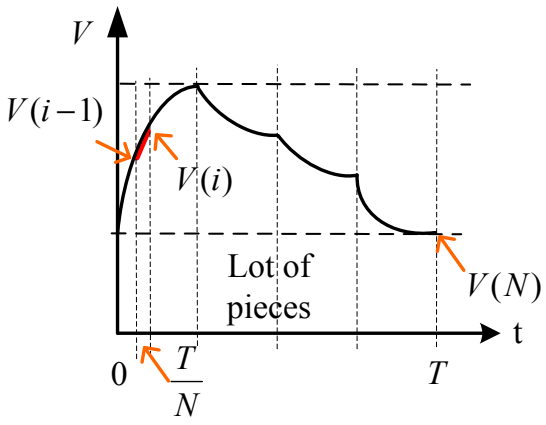


Figure 4.9: Capacitor voltage waveform

which can be approximated as

$$I(t) = C\frac{\Delta V(t)}{\Delta t} \tag{4.3}$$

for an interval $\Delta t = \frac{T}{N}$, where T is the switching period and N is a sufficiently large integer.

Within a period, the capacitor voltage is represented in the discrete-time domain with equal spacing Δt, as a sequence of $\{V(1), V(2), \cdots, V(i), \cdots, V(N+1)\}$. Using (4.3), a discrete-time state equation can be written as

$$V(i) = V(i-1) + R_{eq}I(i), \tag{4.4}$$

where

$$R_{eq} = \frac{T}{NC}. \tag{4.5}$$

To illustrate the discrete-time state-space analytical technique, the second-order ESC converter will be used as an example circuit in the next subsection.

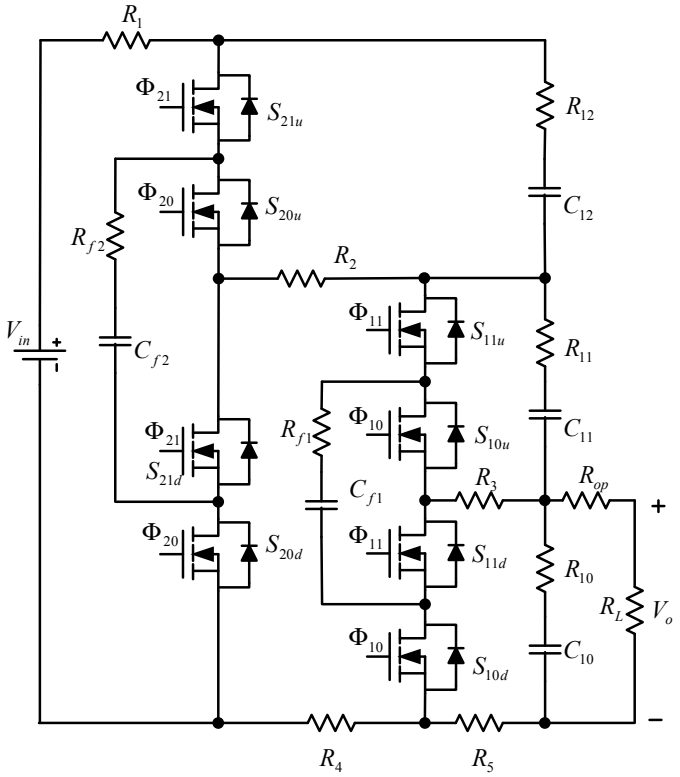


Figure 4.10: Second-order ESC converter with consideration of the ESRs.

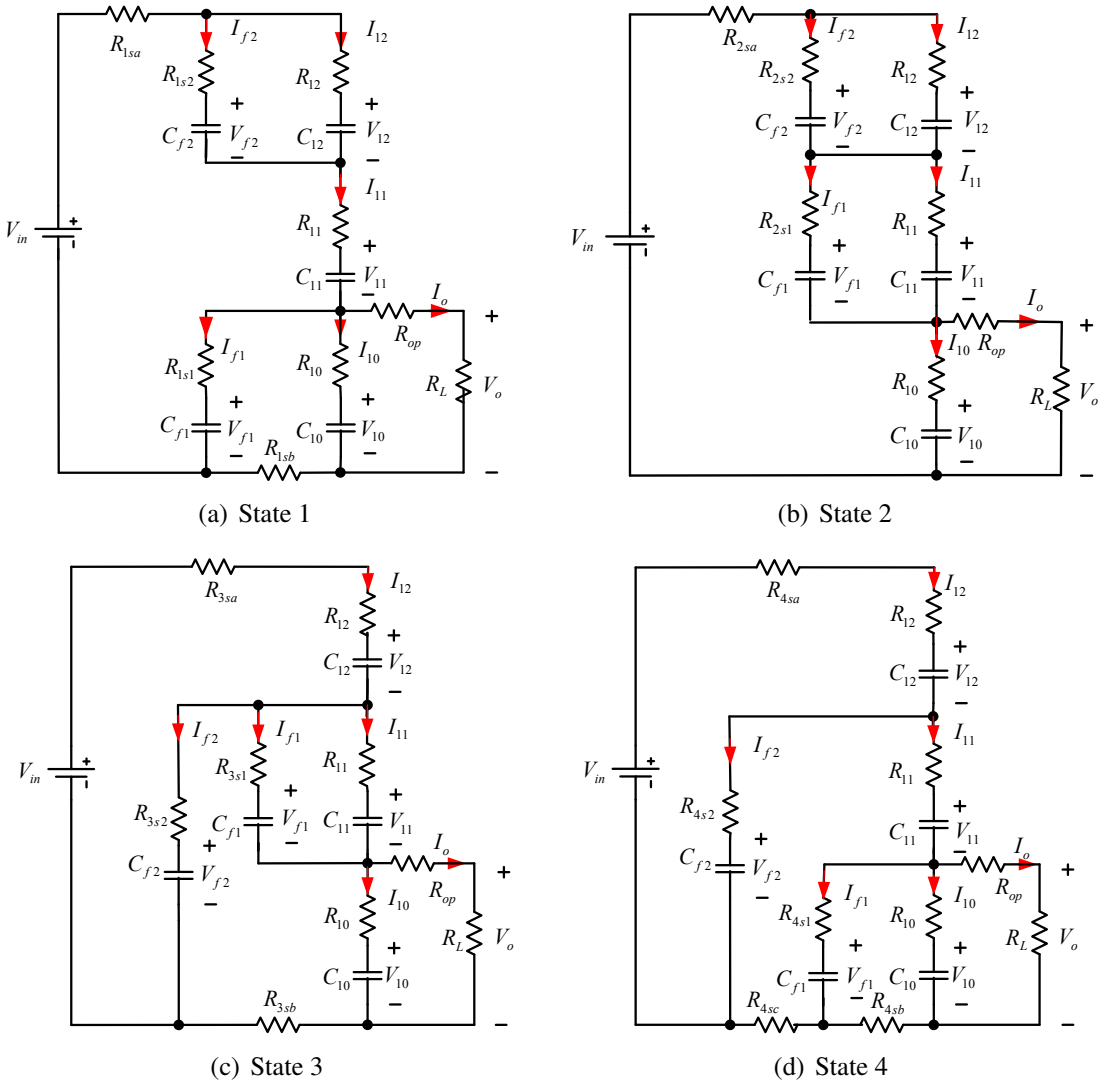
4.4.2 Analysis of Second-order ESC Converter

The second-order ESC circuit shown in Fig. 4.10 will be analyzed in this subsection.

4.4.2.1 Steady State Functions of Each State

All effective resistors including the capacitor ESRs are incorporated in the analysis for better accuracy in the efficiency calculation. For each discrete time i, the state equation is defined as

$$\mathbf{V}(i) = \mathbf{V}(i-1) + \mathbf{R}_{eq}\mathbf{I}(i), \tag{4.6}$$



(a) State 1 (b) State 2

(c) State 3 (d) State 4

Figure 4.11: Equivalent circuit of the four-stage of operation.

where

$$\mathbf{V}(i) = \Big[V_{10}(i), V_{11}(i), V_{12}(i), V_{f1}(i), V_{f2}(i)\Big]^T \text{ and} \tag{4.7}$$

$$\mathbf{I}(i) = \Big[I_{10}(i), I_{11}(i), I_{12}(i), I_{f1}(t), I_{f2}(i)\Big]^T \tag{4.8}$$

are the state-column vectors at time i, and

$$\mathbf{R}_{eq} = \begin{bmatrix} R_{eq10} & 0 & 0 & 0 & 0 \\ 0 & R_{eq11} & 0 & 0 & 0 \\ 0 & 0 & R_{eq12} & 0 & 0 \\ 0 & 0 & 0 & R_{eqf1} & 0 \\ 0 & 0 & 0 & 0 & R_{eqf2} \end{bmatrix} \tag{4.9}$$

is the equivalent-resistance diagonal matrix with element $R_{eqxx} = \frac{T}{NC_{xx}}$ given by (4.5), where the subscript $xx = 10, 11, 12, f1$, and $f2$. The ESC converter goes through four states in its normal operation, as shown in Fig. 4.11. For each state $k = 1, 2, 3, 4$, a general state equation can be formulated as

$$\mathbf{V}(i) = \mathbf{A}_k\mathbf{V}(i-1) + \mathbf{B}_k\mathbf{U}_k, \text{ where} \tag{4.10}$$

$$\mathbf{A}_k = \begin{bmatrix} a_{k,11} & a_{k,12} & a_{k,13} & a_{k,14} & a_{k,15} \\ a_{k,21} & a_{k,22} & a_{k,23} & a_{k,24} & a_{k,25} \\ a_{k,31} & a_{k,32} & a_{k,33} & a_{k,34} & a_{k,35} \\ a_{k,41} & a_{k,42} & a_{k,43} & a_{k,44} & a_{k,45} \\ a_{k,51} & a_{k,52} & a_{k,53} & a_{k,54} & a_{k,55} \end{bmatrix}, \mathbf{B}_k = \begin{bmatrix} b_{k,11} & b_{k,12} \\ b_{k,21} & b_{k,22} \\ b_{k,31} & b_{k,32} \\ b_{k,41} & b_{k,42} \\ b_{k,51} & b_{k,52} \end{bmatrix}, \text{and} \mathbf{U}_k = \begin{bmatrix} V_{\text{in}}(i) \\ I_o(i) \end{bmatrix}. \tag{4.11}$$

The matrix elements can be readily determined by nodal analysis for each state and therefore their expressions are omitted for brevity (The detail elements of the matrix is given by the appendix).

The number M of time points for each state is equally assigned, such that $N = 4M$. The end-point of state variables of each state can be calculated by successive applications of (4.10) for each time point. Eventually, we have for each k,

$$\begin{aligned}\mathbf{V}(kM) = \mathbf{A}_k^M \mathbf{V}((k-1)M) \\ + (\mathbf{A}_k - \mathbf{I})^{-1}(\mathbf{A}_k^M - \mathbf{I})\mathbf{B}_k\mathbf{U}_k.\end{aligned} \tag{4.12}$$

At steady-state, the condition

$$\mathbf{V}(4M) = \mathbf{V}(0) \tag{4.13}$$

holds. Hence, using (4.13), the steady-state solution is obtained as

$$\begin{aligned}\mathbf{V}(0) =&(\mathbf{I} - \mathbf{A}_1^M\mathbf{A}_2^M\mathbf{A}_3^M\mathbf{A}_4^M)^{-1}\Big[\\ &\mathbf{A}_4^M\mathbf{A}_3^M\mathbf{A}_2^M(\mathbf{A}_1 - \mathbf{I})^{-1}(\mathbf{A}_1^M - \mathbf{I})\mathbf{B}_1\mathbf{U}_1 \\ &+ \mathbf{A}_4^M\mathbf{A}_3^M(\mathbf{A}_2 - \mathbf{I})^{-1}(\mathbf{A}_2^M - \mathbf{I})\mathbf{B}_2\mathbf{U}_2 \\ &+ \mathbf{A}_4^M(\mathbf{A}_3 - \mathbf{I})^{-1}(\mathbf{A}_3^M - \mathbf{I})\mathbf{B}_3\mathbf{U}_3 \\ &+ (\mathbf{A}_4 - \mathbf{I})^{-1}(\mathbf{A}_4^M - \mathbf{I})\mathbf{B}_4\mathbf{U}_4\Big]\end{aligned} \tag{4.14}$$

The time points of state variables within a switching cycle at steady-state can readily be calculated using (4.14) and (4.10), and the calculated results will be used for the calculations of the loss in each resistor and the output power:

4.4.2.2 Efficiency Calculation of the Second-order ESC Converter

The losses in each resistor is calculated by

$$E_R = f_s \sum_{n=1}^{N} R_i I_R^2(n) \frac{T}{N} = \frac{1}{N} \sum_{n=1}^{N} R I_R^2(n). \tag{4.15}$$

The output power is calculated by

$$E_o = f_s \sum_{n=1}^{N} V_{10}(n) I_o \frac{T}{N} = \frac{1}{N} \sum_{n=1}^{N} I_o V_{10}(n). \tag{4.16}$$

Hence, the overall efficiency can be calculated as,

$$\eta = \frac{E_o}{E_o + \sum E_R} \times 100\%, \tag{4.17}$$

where $\sum E_R$ is the sum of all losses in resistors including the losses in $R_{ds\text{on}}$ of the switches.

4.5 Simulation and Experiment Verification of the Exponential Switched-capacitor Converter

In order to confirmed the properties of the exponential SC converter and the accuracy of the analytical method, simulations based on SPICE and experimental measurements are performed.

4.5.1 Verification of the Discrete-time Analysis

In order to verify the validity of the discrete-time calculation method, SPICE simulation waveforms and experimental measurements based on the second-order ESC converter are performed using the parameters given in Table 4.2. Fig. 4.12 shows the driver circuit of the second-order ESC converter. The driver IC is TPS2836 from the TI company. Similar driver circuit can be used for third-order ESC converter. The input power and output power measurement equipment is PM100 from Voltech. The E-load is 3311c from Prodigit. An input filtering electrolytic capacitor of 220 μF is connected for the efficiency measurement. Figs. 4.13 and 4.14 show comparisons of the waveforms

from SPICE simulations and discrete-time calculations. Fig. 4.13 shows the comparison of currents through the flying capacitors in a period at steady state. If we ignore the short state transition dead times which are not considered by the discrete-time calculation, the calculation current waveforms match well with the SPICE simulation currents waveforms. Similarly, Fig. 4.14 shows the comparison of voltages in the two-stage structures capacitors. The calculation waveforms are well matched with the SPICE simulation voltages waveforms.

Fig. 4.15 shows the efficiency of calculation and experiment waveforms of a second-order ESC converter. It shows that the ESC converter has a high conversion efficiency. In low power condition, lower switching frequency leads to higher conversion efficiency. While in high power condition, higher switching frequency leads to higher conversion efficiency. The main reason is that, in lower power output, the switching and driver losses occupy a large portion of the overall losses, hence, reducing the switching frequency has a good improvement for the conversion efficiency. While in the heavy load condition, the loss produced by the voltage ripple takes a large portion of the overall losses. Hence, increasing the switching frequency does not reduce the converter's conversion efficiency although the switching and driver losses are increasing.

On the other hand, Fig. 4.15 also shows that the calculation result well match with the experiment results.

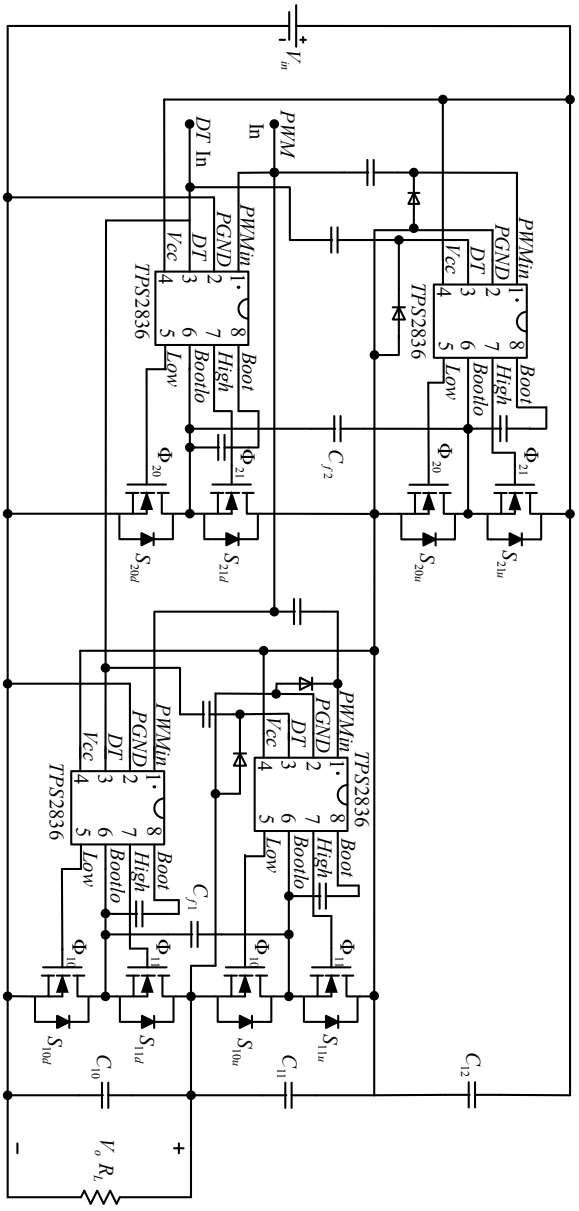
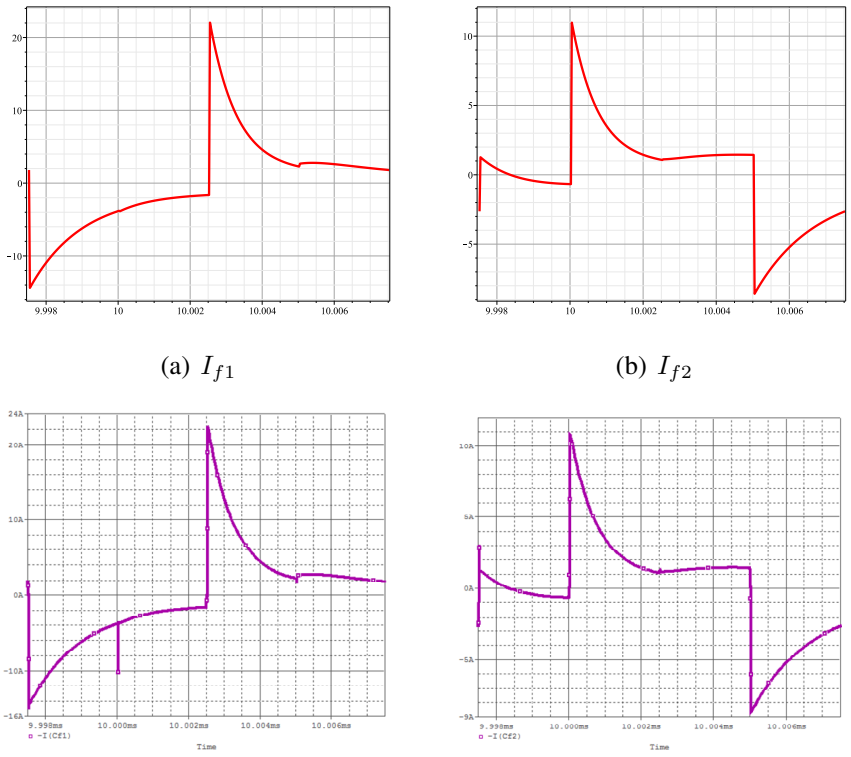


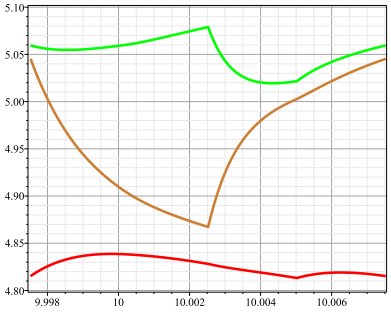
Figure 4.12: Second-order ESC converter with driver circuit.



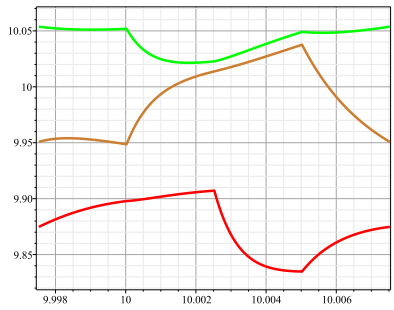
(a) I_{f1} (b) I_{f2}

(c) I_{f1} (d) I_{f2}

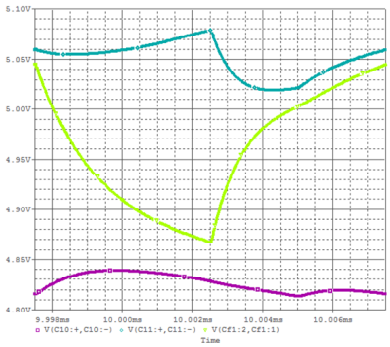
Figure 4.13: Comparisons of calculated and SPICE-simulated current waveforms. (a) and (b) are calculated results. (c) and (d) are SPICE simulated results.



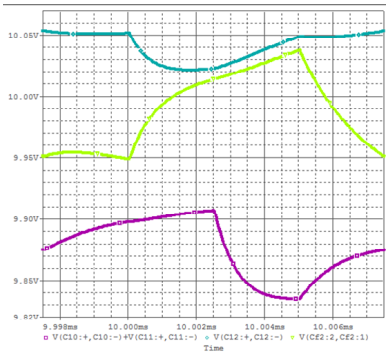
(a) V_{11},V_{f1}, and V_{10} from top to bottom respectively



(b) V_{12},V_{f2}, and $V_{11}+V_{10}$ from top to bottom respectively



(c) V_{11},V_{f1}, and V_{10} from top to bottom respectively



(d) V_{12},V_{f2}, and $V_{11}+V_{10}$ from top to bottom respectively

Figure 4.14: Comparisons of calculated and SPICE-simulated waveforms. (a) and (b) are calculated results. (c) and (d) are SPICE simulated results.

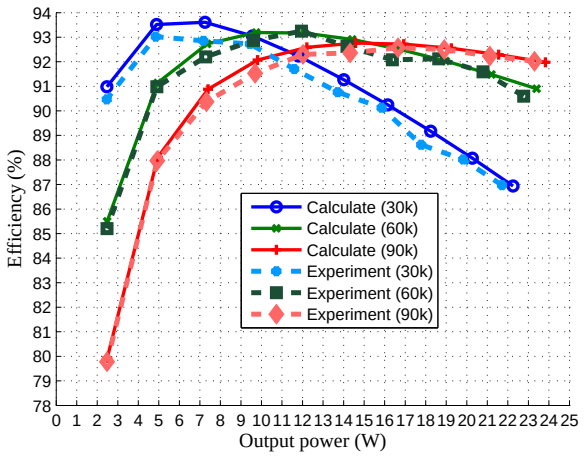


Figure 4.15: Comparison of results from experiment and discrete-time calculation at three switching frequencies.

Table 4.2: Experiment and simulation parameters

type	Experiment	Calculation
Input voltage	20 V	20 V
Switches	NTMFS4897	$R_{dson} = 1.12$ mΩ
C_{10}	Murata $6 \times 47\mu$F	From measurement
C_{11}, C_{12}	Murata $4 \times 47\mu$F	and confirmed
C_{f1}, C_{f2}	Murata $3 \times 47\mu$F	with datasheet
R_1, R_{op}	NA	20 mΩ, 3 mΩ
$R_2 \dots R_5$	NA	5 mΩ, 5 mΩ, 7 mΩ, 8 mΩ

4.6 Conclusion

In this chapter, a family of exponential SC converter is introduced. The experimental results shows the high efficiency energy conversion of the proposed exponential SC converter. Besides, a discrete-time analysis method is proposed. This method is applied to the exponential SC converters. The calculation waveforms are well matched with the simulation waveforms using SPICE simulation. Furthermore, the calculation results math well with the experiment results. Hence, both simulation and experiment results confirmed the accuracy of the discrete-time analysis for the exponential SC converter.

Chapter 5

Exponential Switched-capacitor Buck Converter

5.1 Introduction

Chapter 4 introduces a family of exponential SC converter with high efficiency and low cost. A comparison of high-voltage-gain step-down converters is shown in Table 5.1. In this chapter, the exponential SC converters are applied into the two-stage converter for large-voltage-gain conversion. The discrete-time analysis introduced in Chapter 4 is used for design a two-stage SC-based converter.

Table 5.1: Comparison of high voltage gain converters

	Quadratic buck	ESC	ESC-buck
Conversion ratio	D^2	$\frac{1}{2^n}$	$\frac{1}{2^n}D$
Regulation	Yes	No	Yes
Component numbers	low	high	high
Control	Difficult	Easy	Independent for the two converters; both are easy
IC Fabrication	No	Yes	Partial

5.2 Topology and Operation of Exponential Switched-capacitor Buck Converter

A family of ESC converters has been introduced in Chapter 4. It can be readily seen that the ESC converters have a fixed conversion ratio of $\frac{1}{2^n}$. The lack of voltage regulation will dramatically limit their applications. While papers [19,20,22,23,25–29] show that a two-stage converter can have a better efficiency than that of a single buck converter for large-voltage-gain conversion applications. The voltage regulation can be obtained from a second-stage buck converter. Here, the exponential SC converter can be used for this two-stage converter application, where the voltage conversion ratio is exponentially selectable and the conversion efficiency is properly maintained.

5.2.1 Topology of Exponential SC-buck Converter

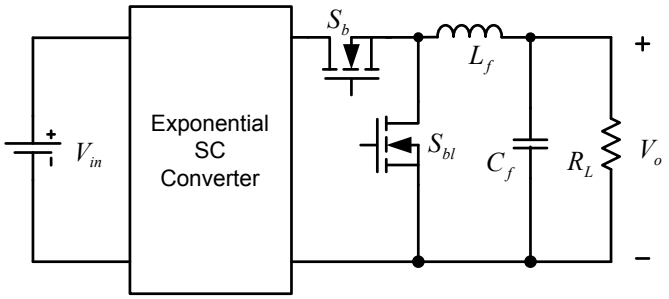
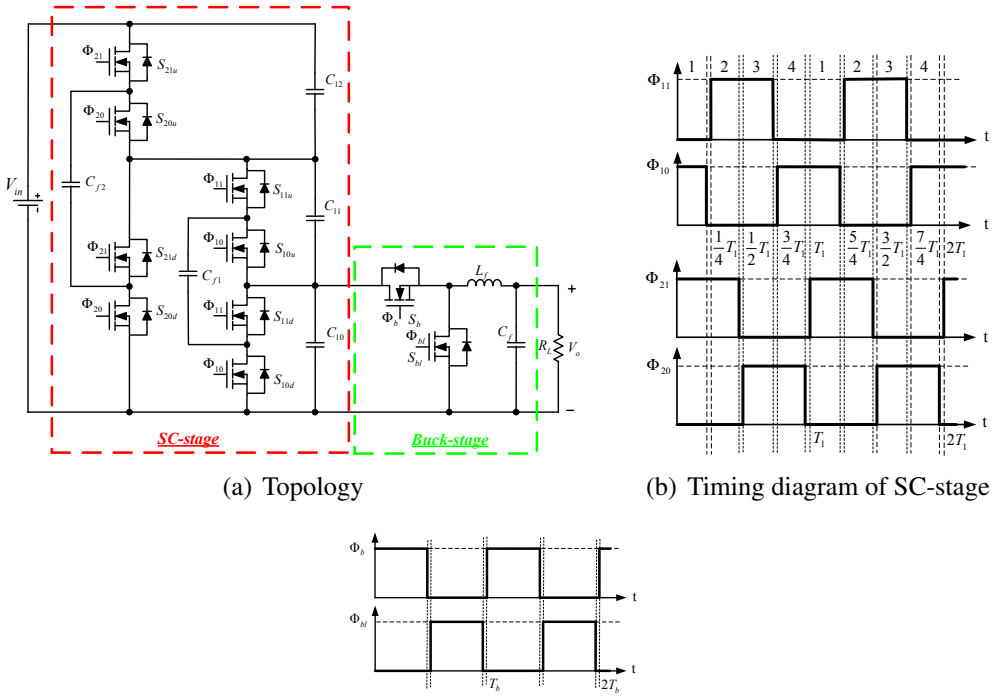


Figure 5.1: General ESC-buck converter.

Fig. 5.1 shows the general exponential SC-based two-stage converter. The converters, which are exponential SC and buck converter, are independently controlled. In this two-stage converter, the first-stage exponential SC converter is to step-down the input voltage to a lower voltage with very high efficiency, while the second-stage buck converter regulates the output voltage.

5.2.2 Operation of Second-order ESC-buck Converter

Here, the second-order ESC-buck converter is taken as an example for illustrating the operation of an ESC-buck converter, which is shown in Fig. 5.2.



(a) Topology

(b) Timing diagram of SC-stage

(c) Timing diagram of buck-stage

Figure 5.2: A second-order ESC-buck converter.

5.3 Analysis of the Exponential Switched-capacitor Buck Converter

The exponential SC-buck converter is composed of two independent converters, which are exponential SC and buck converter. They can be analyzed independently. Chapter 4 provides a discrete-time calculating method for the single exponential SC converter with good accuracy. In this chapter, the method will be used for the analysis of the SC converter. Chapter 3 provides an analysis method for a single buck converter.

However, in this chapter, direct experimental results of the buck stage will be used for the optimization of the SC converter, saving extra calculations.

5.3.1 Theoretical Limit of Efficiency Improvements of a Two-stage Converter Over a Single-stage Converter

In a two-stage converter, the overall efficiency is the product of the efficiencies of the two stages. Denoting the first-stage efficiency as η_1, and the second-stage efficiency as η_2, the overall efficiency of the two-stage converter is $\eta_1\eta_2$. If the first-stage converter is removed, then the second-stage converter will work at an undesirably higher input voltage that results in an efficiency reduction of $\Delta\eta_2$ leading to an overall efficiency of $\eta_2 - \Delta\eta_2$. The amount of efficiency improvement of the two-stage converter is given by

$$\begin{aligned} &\eta_1\eta_2 - (\eta_2 - \Delta\eta_2) > 0, \text{ i.e.,} \\ &\eta_1 > 1 - \frac{\Delta\eta_2}{\eta_2} \end{aligned} \tag{5.1}$$

Equation (5.1) indicates that a larger $\frac{\Delta\eta_2}{\eta_2}$ gives more headroom for a two-stage converter to have better efficiency. This property will be used for explaining the efficiency improvement of a two-stage converter over a single stage converter in the next section.

5.4 Experiment Efficiency Measurement of the Exponential Switched-capacitor Buck Converter

Several prototypes of the ESC-buck converters have been built to analyze the properties. The first stage ESC converter is built with discrete components with parameters shown in Table 5.2. Two commercially available ICs, MAX8655 and IR3820, are used for the second stage buck converter. The parameters of the two buck converters

are shown in Table 5.3.

Table 5.2: Parameters of the ESC converters

ESC type	First-Order	Second-Order
Flying cap C_{f1}	6×47 μF	6×47 μF
Flying cap C_{f2}	NA	6×47 μF
Capacitor C_{10}	1×47 μF	1×47 μF
Capacitor C_{11}	1×47 μF	1×47 μF
Capacitor C_{12}	NA	1×47 μF
Switches	NTMFS4897NF	NTMFS4897NF

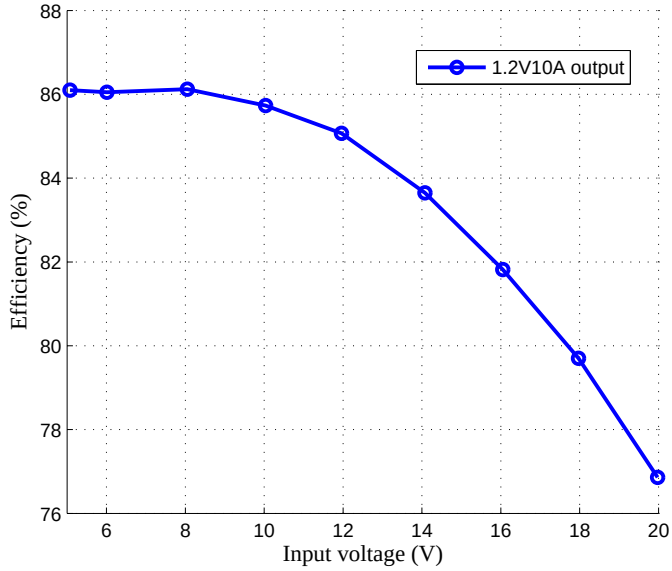
Table 5.3: Parameters of the two buck converters

IC type	IR3820	MAX8655
Input voltage	2.5–21 V	4.5–25 V
Output voltage	1.8 V	1.2 V
Switching frequency	300 kHz	400 kHz
Filter inductor	1.7 μH	0.82 μH
Output capacitor	2×47 μF	4×47 μF

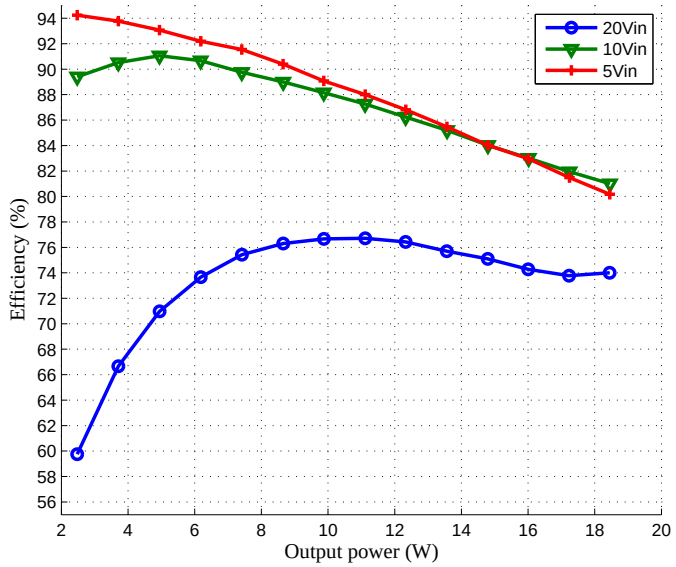
5.4.1 Efficiencies of Single-stage Buck Converters

Fig. 5.3(a) shows the measured efficiency versus input voltage of the buck converter using MAX8655. The efficiency measured is typical compared with that from the data sheet of the manufacturer. Fig. 5.3(b) shows the efficiency improvement for an input voltage reduction from 20 V to 10 V and 5 V. It is therefore expected from (5.1) that there will be efficiency improvement by inserting a first- or second-order ESC converter in front of the buck converter with the 20 V supply voltage. Furthermore, at low output power, the efficiency of the second-order ESC-buck converter can be better than the first-order ESC-buck converter.

Fig. 5.4 shows the efficiency of the buck converter using IR3820. From Fig. 5.4(a) and (5.1), the headroom of efficiency improvement by inserting a second-order ESC converter can be better than a first-order ESC converter, in front of the buck converter using IR3820.

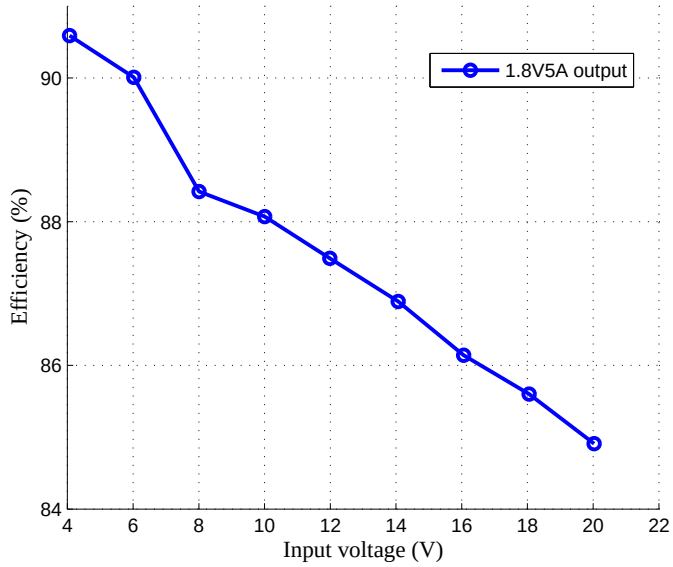


(a)

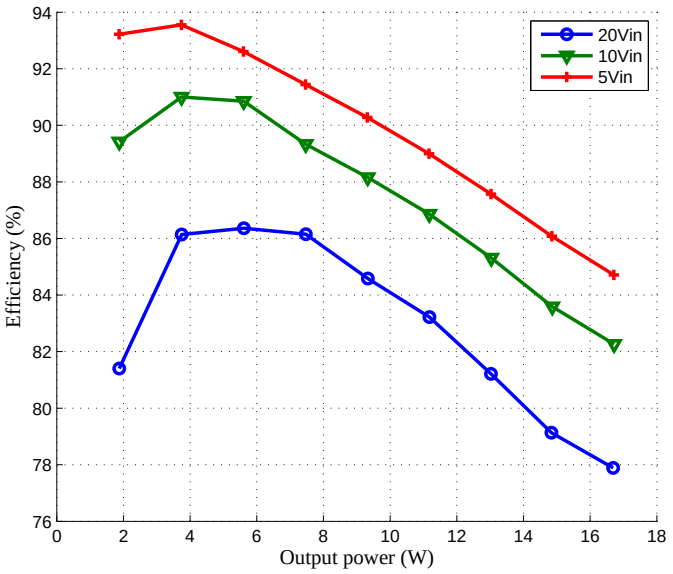


(b)

Figure 5.3: Efficiency curves of MAX8655 buck converter versus (a) input voltage, (b) output power.



(a)



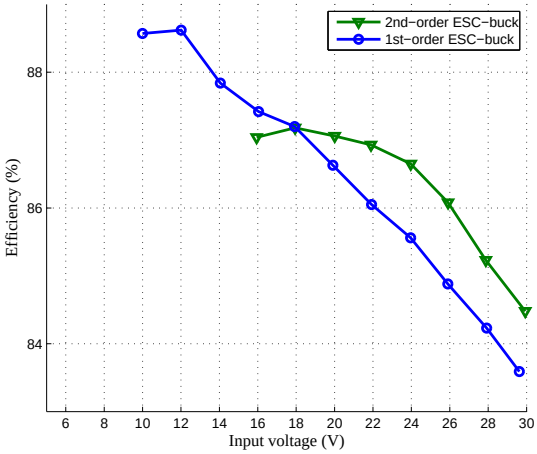
(b)

Figure 5.4: Efficiency curves of IR3820 buck converter versus (a) input voltage, (b) output power.

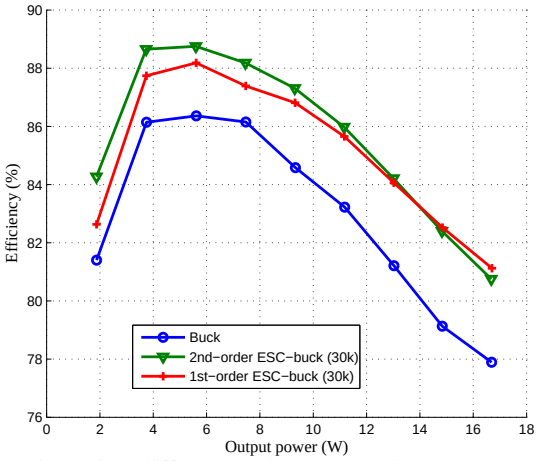
5.4.2 Efficiency of ESC-buck Converters

The buck converters analyzed in the last subsection are connected with a front end first- or second-order ESC converter for efficiency improvement. Fig. 5.5(a) gives the efficiency comparison of first-order and second-order ESC-buck converter using the buck IC MAX8655. The second-order ESC-buck converter has a better efficiency than the first-order ESC converter when the input voltage is higher than 26 V. In Fig. 5.5(b), as expected from the analysis in the last subsection, the two-stage first- or second-order ESC-buck converter can generally have higher efficiency than the single-stage MAX8655 buck converter for large-voltage-gain applications. The first- or second order ESC-buck converter excels at different loading conditions. However, when operating at an even higher input voltage of 30 V, which is over the input voltage ratings of a single-stage MAX8655 buck converter, the efficiency of the second-order ESC-buck converter is higher than that of the first-order ESC-buck converter for the load range specified.

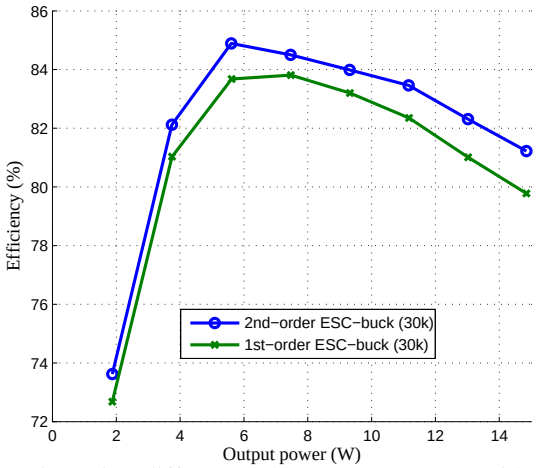
Fig. 5.6 shows that converters using IR3820 have similar efficiency properties. The only difference is that the second-order ESC-buck converter can have better efficiency than the first-order ESC-buck converter at a wider input voltage range due to the larger efficiency headroom.



(a) ESC-buck Efficiency versus input voltage at 30 kHz with 5 A output.

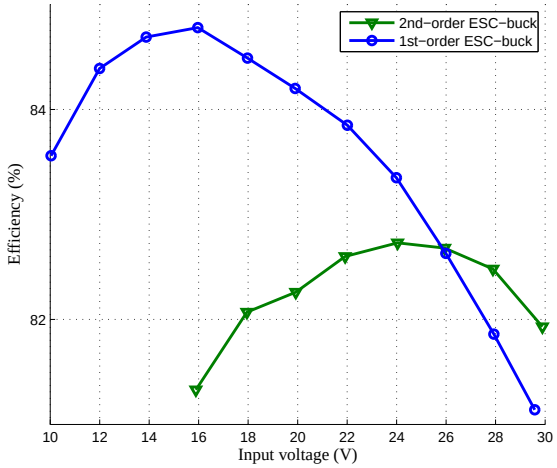


(b) Comparison of efficiencies using different order ESC-buck converters with front-end ESC operating at 30 kHz and an input voltage of 20 V.

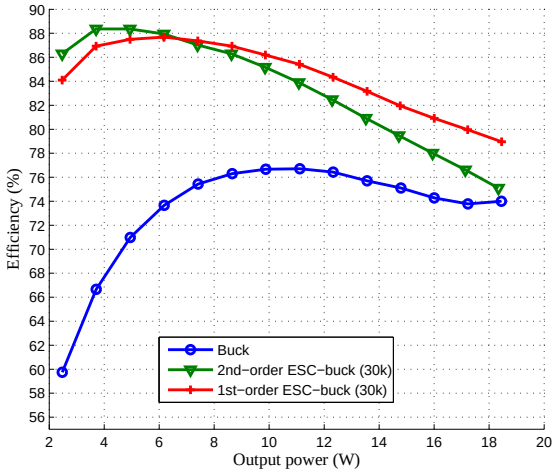


(c) Comparison of efficiencies using different order ESC-converters with front-end ESC operating at 30 kHz and an input voltage of 30 V.

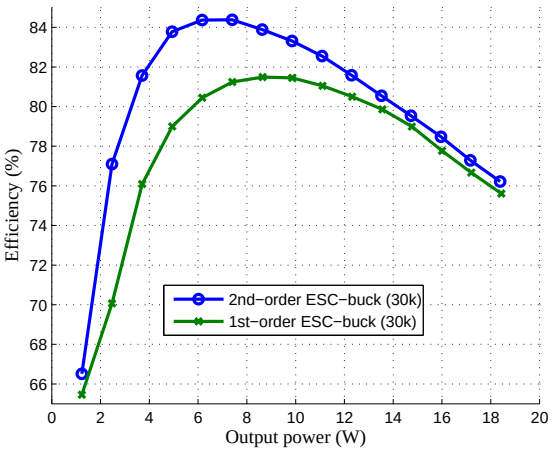
Figure 5.6: Efficiency analysis of ESC-buck converter using IR3820 at a regulated output voltage of 1.8 V.



(a) ESC-buck Efficiency versus input voltage at 30 kHz with 10 A output.



(b) Comparison of efficiencies using different order ESC-buck converters with front-end ESC operating at 30 kHz and an input voltage of 20 V.



(c) Comparison of efficiencies using different order ESC-buck converters with front-end ESC operating at 30 kHz and an input voltage of 30 V.

Figure 5.5: Efficiency analysis of ESC-buck converter using MAX8655 at an regulated output voltage of 1.2 V.

5.5 Optimize Order Selection of ESC stage in the ESC Buck Converter

Section 5.4 indicates that the application of the exponential SC converter in the two-stage SC-buck converter has better conversion efficiency than a single buck converter. Moreover, the second-order or higher-order ESC buck converter is shown to have better efficiency than the first-order ESC Buck converter, especially in the higher input voltage or lower output voltage conditions, which requires higher conversion ratio. In this section, the parameters which affect converter efficiency are investigated.

The SC converter is composed of capacitors and switches. Hence, the design of ESC converter includes the design of capacitor values, the selection of switches and the design of switching frequency.

However, in the two-stage ESC-buck converter, the selection of the order of the ESC converter is of concern. Hence, this section gives a selection guideline for choosing the order of ESC converter.

5.5.1 Power Flow Path Analysis

Power flow analysis has been used in [96] to analyze the efficiency of a converter looking for minimum power processing steps. For an SC converter, power flows through capacitors using a set of switch configurations within a switching cycle. Each switch configuration activates a new set of rules for the energy flow among the power source, capacitors and the load. Power loss via each capacitor is design to be small. However, if an amount of energy is kept circulating among a number of capacitors, the accumulative lose can be large. The power flow analysis of a first-order ESC converter is thus developed in this section.

Using the timing diagram of Fig. 4.7(b), the first-order ESC converter has three

operating states as shown in Fig. 5.9. Fig. 5.7 gives a circuit model for each operating state and Fig. 5.8 shows the simulated voltage waveform of each capacitor. State 3, being short compared with the other two states, is neglected in the analysis. According to the waveforms, states 1 and 2 include two sub-states with sub-state boundary happened at the instance when $\frac{dV_o}{dt} = 0$. At this instance, by neglecting the effect of ESRs in the branch as its extremely low value, we have

$$\frac{dV_{11}}{dt} = 0, \tag{5.2}$$

$$\frac{dV_{10}}{dt} = 0, \text{ and} \tag{5.3}$$

$$I_{f1} = I_o. \tag{5.4}$$

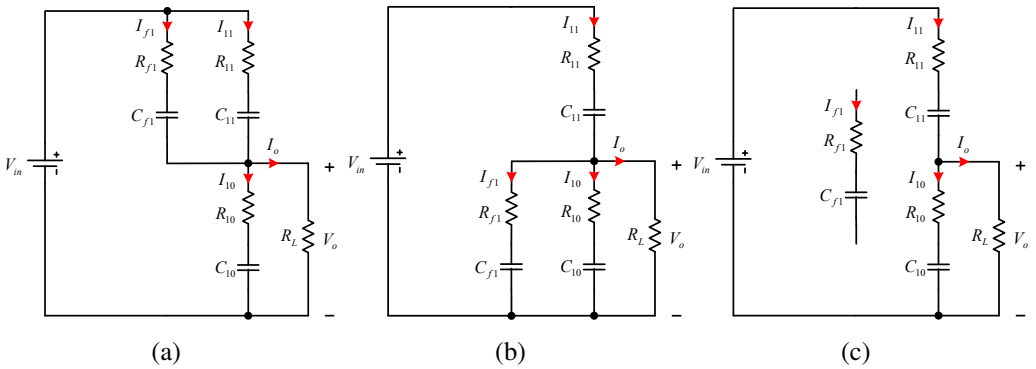


Figure 5.7: Equivalent circuits of three states of the first-order ESC converter: (a) state 1, (b) state 2, and (c) state 3.

Within the equations, we use the subscript x of the device shown in Fig. 5.7 to represent the voltage V_x across or the current I_x through the particular device D_x, where the D is either V, C or R. As x is uniquely defined, the subscript x can be used to identify the device without ambiguity. With these four states identified, four energy flow diagrams shown in Figs. 5.10 and 5.11 are identified. Within each switching period, a total accumulative energy increment E_x^+ and a total accumulative energy decrement E_x^- are defined for each device D_x shown in Figs. 5.10 and 5.11. It can be observed that $E_{\text{in}}^+ = 0$ and $E_L^- = 0$ within a switching cycle at steady state. To describe the

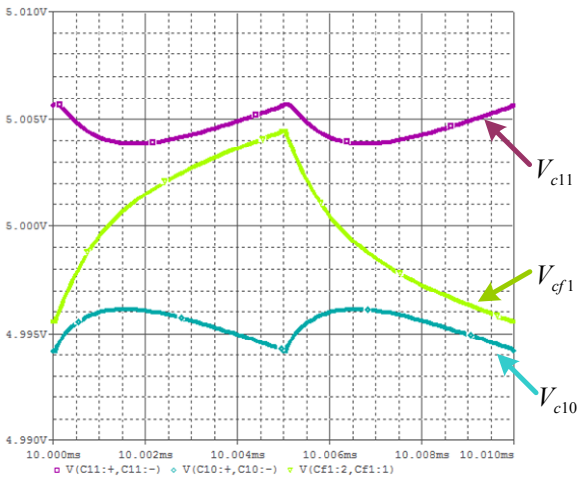


Figure 5.8: Capacitors waveform of first-order ESC converter

power flow, two scalar quantities ${}_xk_y^s$ and ${}_x\eta_y^s$ are defined for properties happened from device x to device y averaged over the sub-state s. The quantity $k \leq 1$ represents the portion of energy originated from device x. The quantity η represents the efficiency of the power flow from device x to y at sub-state s. The following equations can be derived for all sub-states shown in Figs. 5.10 and 5.11.

$$E_{11}^{+} = \left({}_{\text{in}}k_{11}^{1b}\,{}_{\text{in}}\eta_{11}^{1b} + {}_{\text{in}}k_{11}^{2b}\,{}_{\text{in}}\eta_{11}^{2b}\right) E_{\text{in}}^{-}, \tag{5.5}$$

$$\begin{aligned} E_{f1}^{+} = &\left({}_{\text{in}}k_{f1}^{1a}\,{}_{\text{in}}\eta_{f1}^{1a} + {}_{\text{in}}k_{f1}^{1b}\,{}_{\text{in}}\eta_{f1}^{1b}\right) E_{\text{in}}^{-} \\ &+ {}_{11}k_{f1}^{1a}\,{}_{11}\eta_{f1}^{1a} E_{11}^{+}, \end{aligned} \tag{5.6}$$

$$E_{10}^{+} = {}_{\text{in}}k_{10}^{1a}\,{}_{\text{in}}\eta_{10}^{1a} E_{\text{in}}^{-} + {}_{f1}k_{10}^{2a}\,{}_{f1}\eta_{10}^{2a} E_{f1}^{+}, \text{ and} \tag{5.7}$$

$$\begin{aligned} E_{L}^{+} = &\left({}_{\text{in}}k_{L}^{1}\,{}_{\text{in}}\eta_{L}^{1} + {}_{\text{in}}k_{L}^{2b}\,{}_{\text{in}}\eta_{L}^{2b}\right) E_{\text{in}}^{-} \\ &+ \left({}_{10}k_{L}^{1b}\,{}_{10}\eta_{L}^{1b} + {}_{10}k_{L}^{2b}\,{}_{10}\eta_{L}^{2b}\right) E_{10}^{+} \\ &+ {}_{f1}k_{L}^{2}\,{}_{f1}\eta_{L}^{2} E_{f1}^{+}, \end{aligned} \tag{5.8}$$

where ${}_xk_y^1 = {}_xk_y^{1a} + {}_xk_y^{1b}$ and ${}_xk_y^2 = {}_xk_y^{2a} + {}_xk_y^{2b}$, likewise for ${}_x\eta_y^1$ and ${}_x\eta_y^2$. Solving for E_L^+ using (5.5) to (5.7), we have

$$\begin{aligned} E_{L}^{+} = &\Big(k_1\eta_1^{(1)} + k_2\eta_2^{(2)} + k_3\eta_3^{(2)} \\ &+ k_4\eta_4^{(3)} + k_5\eta_5^{(3)} + k_6\eta_6^{(4)}\Big) E_{\text{in}}^{-}, \end{aligned} \tag{5.9}$$

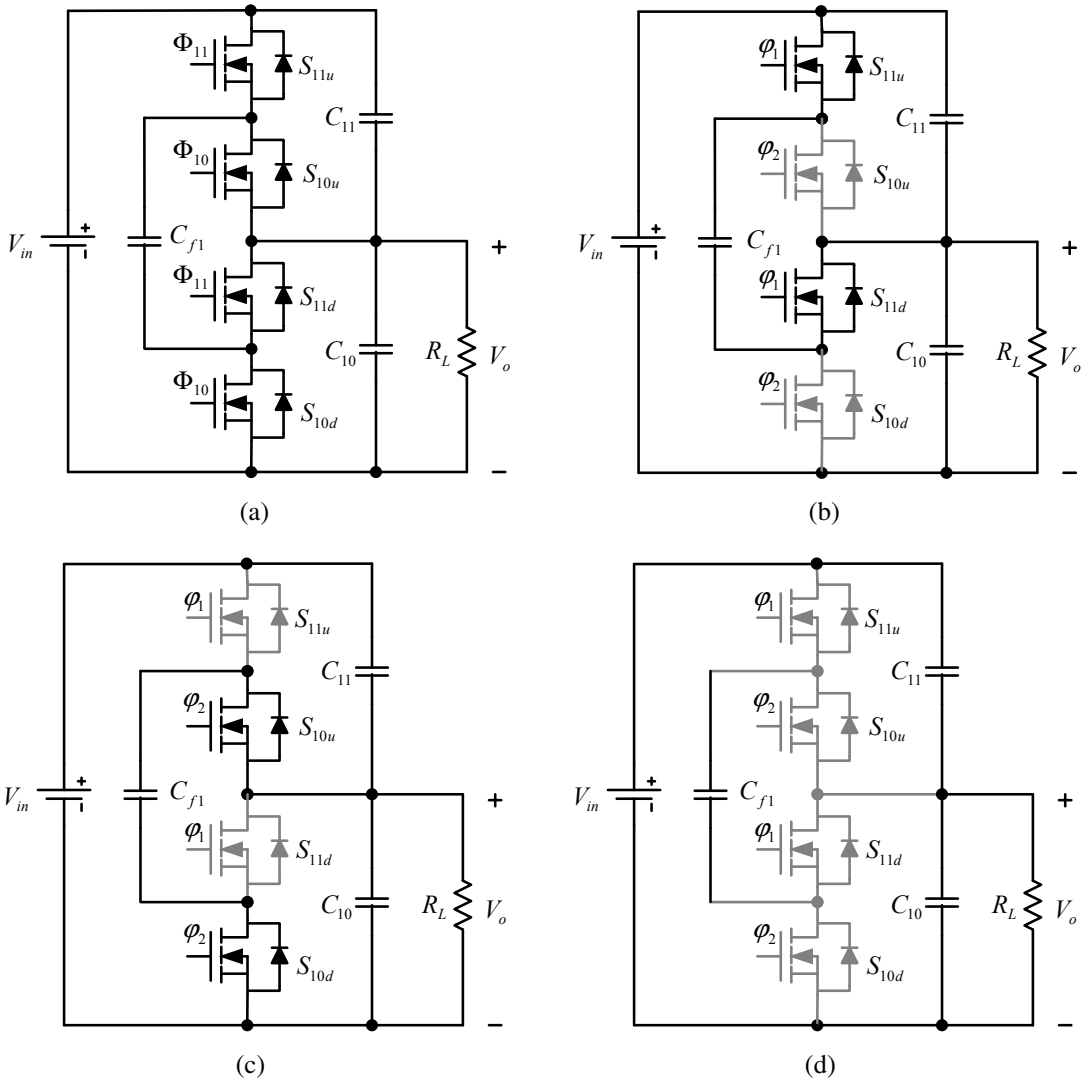


Figure 5.9: First-order exponential SC converter, as shown in (a), and its three states: (b) state 1: flying capacitor parallels with the C_{11}, (c) state 2: flying capacitor parallels with C_{10}, and (d) state 3: flying capacitor is floating.

where

$$k_1 = {}_{\text{in}}k_L, \tag{5.10}$$

$$\eta_1^{(1)} = {}_{\text{in}}\eta_L, \tag{5.11}$$

$$k_2 = {}_{\text{in}}k_{f1}\ {}_{f1}k_L, \tag{5.12}$$

$$\eta_2^{(2)} = {}_{\text{in}}\eta_{f1}\ {}_{f1}\eta_L, \tag{5.13}$$

$$k_3 = {}_{\text{in}}k_{10}\ {}_{10}k_L, \tag{5.14}$$

$$\eta_3^{(2)} = {}_{\text{in}}\eta_{10}\ {}_{10}\eta_L, \tag{5.15}$$

$$k_4 = {}_{\text{in}}k_{f1}\ {}_{f1}k_{10}\ {}_{10}k_L, \tag{5.16}$$

$$\eta_4^{(3)} = {}_{\text{in}}\eta_{f1}\ {}_{f1}\eta_{10}\ {}_{10}\eta_L, \tag{5.17}$$

$$k_5 = {}_{\text{in}}k_{11}\ {}_{11}k_{f1}\ {}_{f1}k_L, \tag{5.18}$$

$$\eta_5^{(3)} = {}_{\text{in}}\eta_{11}\ {}_{11}\eta_{f1}\ {}_{f1}\eta_L, \tag{5.19}$$

$$k_6 = {}_{\text{in}}k_{11}\ {}_{11}k_{f1}\ {}_{f1}k_{10}\ {}_{10}k_L, \text{ and} \tag{5.20}$$

$$\eta_6^{(4)} = {}_{\text{in}}\eta_{11}\ {}_{11}\eta_{f1}\ {}_{f1}\eta_{10}\ {}_{10}\eta_L, \tag{5.21}$$

where

$${}_{\text{in}}k_{11} = {}_{\text{in}}k_{11}^{1b} + {}_{\text{in}}k_{11}^{2b}, \tag{5.22}$$

$${}_{\text{in}}\eta_{11} = \frac{{}_{\text{in}}k_{11}^{1b}}{{}_{\text{in}}k_{11}}{}_{\text{in}}\eta_{11}^{1b} + \frac{{}_{\text{in}}k_{11}^{2b}}{{}_{\text{in}}k_{11}}{}_{\text{in}}\eta_{11}^{2b}, \tag{5.23}$$

$${}_{\text{in}}k_{f1} = {}_{\text{in}}k_{f1}^{1a} + {}_{\text{in}}k_{f1}^{1b}, \tag{5.24}$$

$${}_{\text{in}}\eta_{f1} = \frac{{}_{\text{in}}k_{f1}^{1a}}{{}_{\text{in}}k_{f1}}\ {}_{\text{in}}\eta_{f1}^{1a} + \frac{{}_{\text{in}}k_{f1}^{1b}}{{}_{\text{in}}k_{f1}}\ {}_{\text{in}}\eta_{f1}^{1b}, \tag{5.25}$$

$${}_{11}k_{f1} = {}_{11}k_{f1}^{1a}, \tag{5.26}$$

$${}_{11}\eta_{f1} = {}_{11}\eta_{f1}^{1a}, \tag{5.27}$$

$${}_{\text{in}}k_{10} = {}_{\text{in}}k_{10}^{2a}, \tag{5.28}$$

$${}_{\text{in}}\eta_{10} = {}_{\text{in}}\eta_{10}^{2a}, \tag{5.29}$$

$${}_{f1}k_{10} = {}_{f1}k_{10}^{1a}, \text{ and} \tag{5.30}$$

$${}_{f1}\eta_{10} = {}_{f1}\eta_{10}^{1a}. \tag{5.31}$$

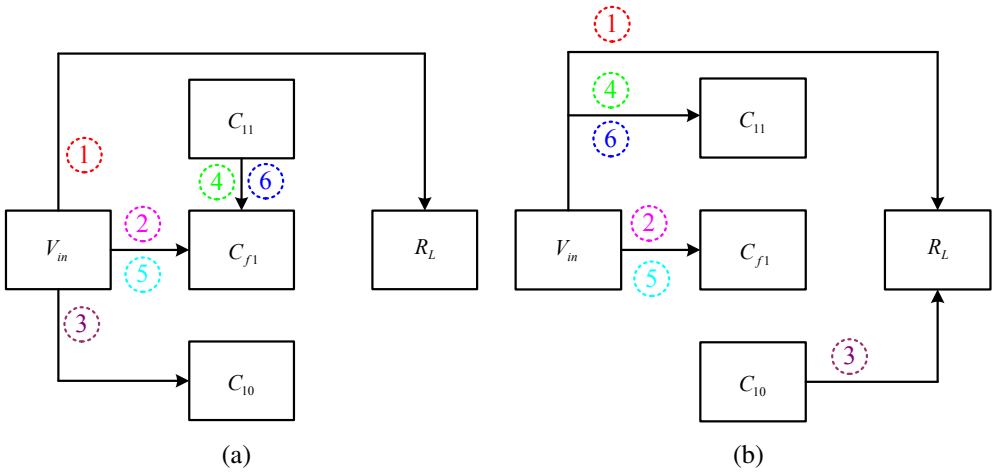


Figure 5.10: Energy flow paths of state 1 with (a) sub-state 1a and (b) sub-state 1b. Numbers drawn inside dotted circles will be explained by the end of this section.

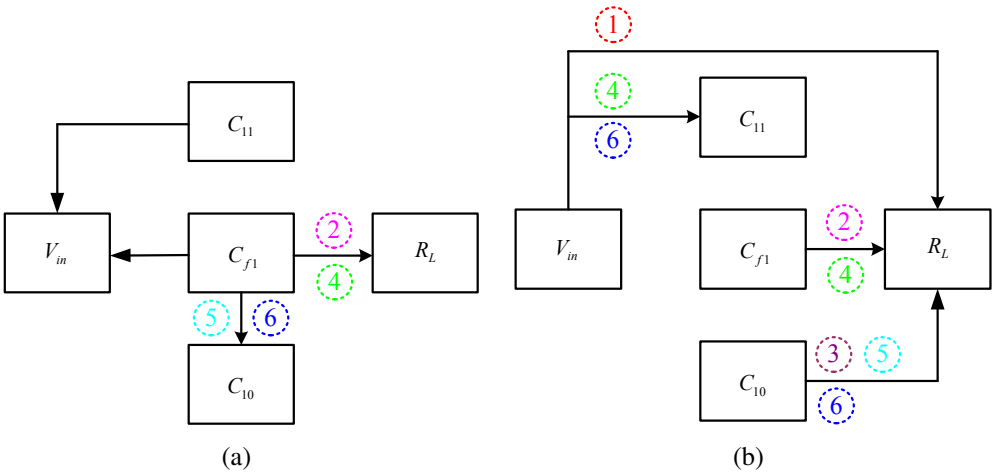


Figure 5.11: Energy flow paths of state 2 with (a) sub-state 2a and (b) sub-state 2b. Numbers drawn inside dotted circles will be explained by the end of this section.

From (5.9), the subscript p of k's and η's indicates the energy flow path as shown in Fig. 5.12. The index n of $\eta_p^{(n)}$ shows the number of power-processing steps of the energy flow path p. It can be readily observed that design should maximize k with lowest n and minimize k with higher n.

According to the energy path p shown in Fig. 5.12, the p's are also indicated in Figs. 5.10 and 5.11. By comparing Fig. 5.10 with Fig. 5.7(a) and Fig. 5.11 with Fig. 5.7(b), energy should be mainly carried via C_{f1} rather than the other two capacitors C_{10} and C_{11} for each switching period for best efficiency, i.e. $E_{f1}^{+} \gg E_{10}^{+}$ and $E_{f1}^{+} \gg$

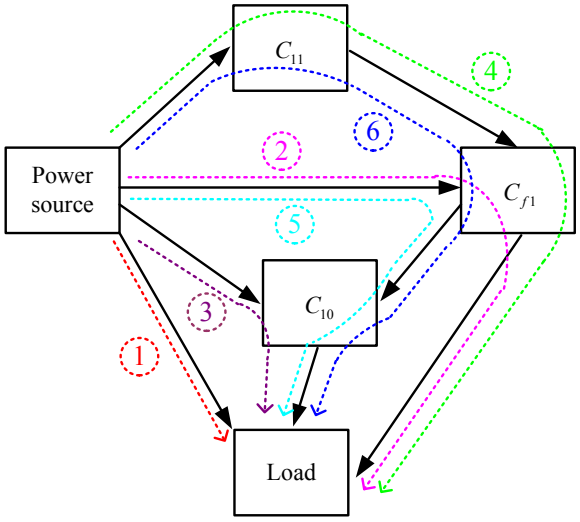


Figure 5.12: Energy flow path p, shown as a number drawn inside a dotted circle, of the first-order ESC converter.

E_{11}^{+}. In doing so, we have from Fig. 5.10,

$$k_2 + k_5 \gg k_3 + k_4 + k_6, \tag{5.32}$$

and from Fig. 5.11,

$$k_2 + k_4 \gg k_3 + k_5 + k_6. \tag{5.33}$$

If k_2 is not much larger than k_4 and k_5, then (5.32) and (5.33) cannot be satisfied simultaneously. Hence, we have

$$k_2 \gg k_3 + k_4 + k_5 + k_6. \tag{5.34}$$

The converter is optimized to have approximately at most two steps of power processing. As C_{f1} is either parallel with C_{10} or C_{11}, in the next section, we will derive design conditions for maximizing energy flow via one of the two paralleled capacitors.

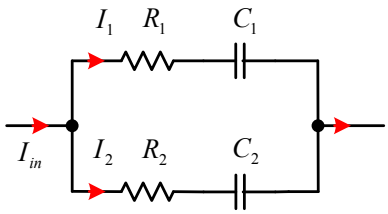


Figure 5.13: Structure of parallel capacitors

5.5.2 Energy Flow Distribution of Two Paralleled Capacitors

Fig. 5.13 shows a circuit of two paralleled capacitors being connected to a constant input voltage V_{in} at time $t_o = 0$. The energy changed after time $t > t_o$ can be calculated using $\Delta E_i(t) = \frac{1}{2}C_i\{V_{Ci}^2(t) - V_{Ci}^2(t_o)\}$ for $i = 1, 2$. Hence, we have

$$\frac{\Delta E_1(t)}{\Delta E_2(t)} = \frac{C_1\left\{(1-v_1^2) - (1-v_1)^2 e^{-x_1}\right\}(1-e^{-x_1})}{C_2\left\{(1-v_2^2) - (1-v_2)^2 e^{-x_2}\right\}(1-e^{-x_2})} \tag{5.35}$$

where $v_i = \frac{V_{Ci}(t_o)}{V_{\text{IN}}}$, $x_i = \frac{-t}{R_i C_i} = \frac{-t}{\tau_i}$ for $i = 1, 2$. For a high efficiency SC converter, we normally have $v_i \approx 1$ at steady state as indicated in Fig. 5.8. Therefore, $e_{12}(t)$, the ratio of energy absorbed or released by the two capacitors in (5.35) can be simplified to

$$e_{12}(t) = \frac{\Delta E_1(t)}{\Delta E_2(t)} \approx \frac{C_1(1-e^{-x_1})}{C_2(1-e^{-x_2})}, \text{ where} \tag{5.36}$$

$$\frac{(1-e^{-x_1})}{(1-e^{-x_2})} = \begin{cases} \frac{\tau_2}{\tau_1} \text{ as } t \to 0, \\ 1 \text{ as } t \to \infty, \text{ and} \\ e_t : e_t \text{ in between } \frac{\tau_2}{\tau_1} \text{ and } 1, \text{ otherwise.} \end{cases} \tag{5.37}$$

According to (5.36) and (5.37), the capacitance ratio is proportional to the energy flow ratio for $t \gg \max(\tau_1, \tau_2)$. To further increase the energy flow ratio, the ratio of the capacitor time-constant $\frac{\tau_2}{\tau_1}$ can be a reference to select the operating duration of the sub-states or the switching period. The sub-state operating time smaller than (or larger than) the unity multiple of τ_1 should be used if $\tau_2 \gg \tau_1$ (or $\tau_1 \gg \tau_2$). However, using

similar technologies of capacitors, $\frac{\tau_2}{\tau_1}$ of two different-value capacitors will not deviated much from unity. The deviation, however, can come from the undesired resistance from interconnections and pass switches. Therefore, the intrinsic capacitor time constant will not practically affect much of the energy flow by varying switching periods.

5.5.3 Simulation and Experimental Verification

We have qualitatively established the way to improve the efficiency of the SC converter in previous sections. In this subsection, discrete-time simulations of Chapter 4.4 and experimental measurements will be used to illustrate the qualitative technique applying to a second-order ESC converter. The detailed model of the second-order ESC converter is shown in Fig. 5.14 with nominal parameters given in Table 5.4. In the nominal design, the capacitor ratios are designed equal to 4. Two capacitors are grouped as G_1 and G_2 with capacitor ratios defined in (5.38) and (5.39) respectively for subsequent analysis.

$$G_1 \equiv \{C_{f1}, C_{11}\}, \quad K_{fb1} \equiv \frac{C_{f1}}{C_{11}} \tag{5.38}$$

$$G_2 \equiv \{C_{f2}, C_{12}\}, \quad K_{fb2} \equiv \frac{C_{f2}}{C_{12}} \tag{5.39}$$

Table 5.4: Experiment and simulation parameters

type	Experiment	Calculation
V_{in}	20 V	20 V
I_o	5 A	5 A
f_s	60 kHz	60 kHz
Switches	NTMFS4897	$R_{dson} = 1.12$ mΩ
C_{10}	Murata 47 μF	ESR = 4 mΩ
C_{11}, C_{12}	Murata 47 μF	4 mΩ
C_{f1}, C_{f2}	Murata $4 \times 47\mu$F	1 mΩ
R_1, R_{op}	NA	20 mΩ, 10 mΩ
$R_2 \ldots R_5$	NA	5 mΩ, 5 mΩ, 5 mΩ, 5 mΩ

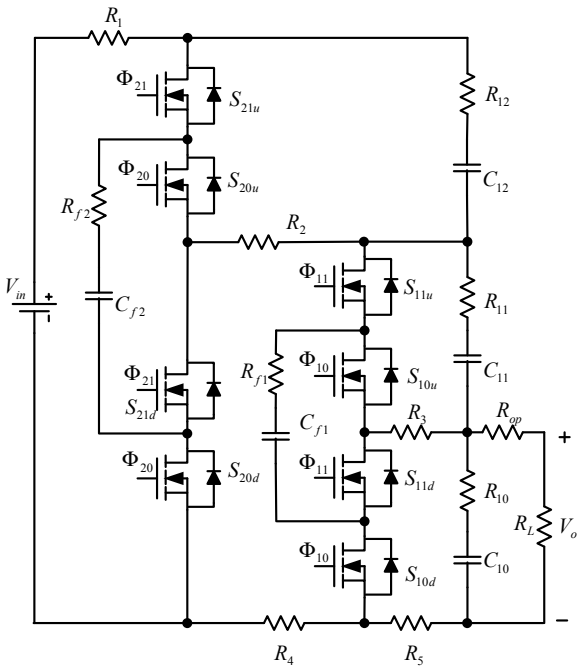


Figure 5.14: Second-order ESC converter with consideration of the ESRs.

In the following subsections, the sets of converter efficiency measurements are conducted. Unless specified or otherwise the components are kept at their nominal values as in Table 5.4.

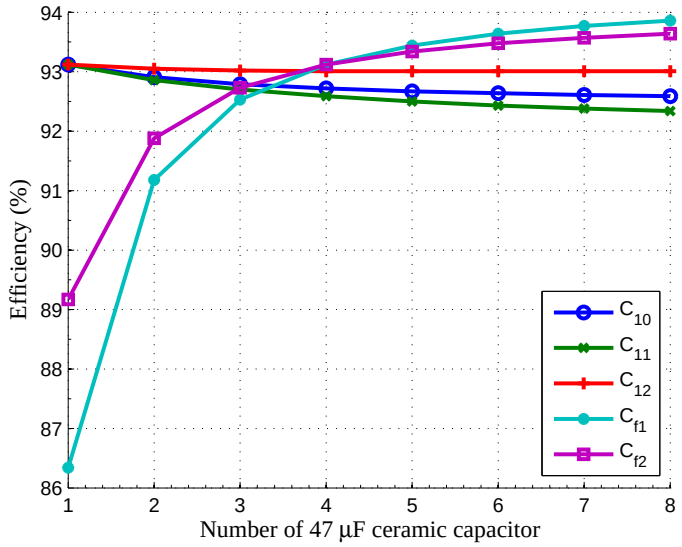
5.5.3.1 Efficiency versus Capacitance Variation

In this subsection, capacitance values are varied using the following methods:

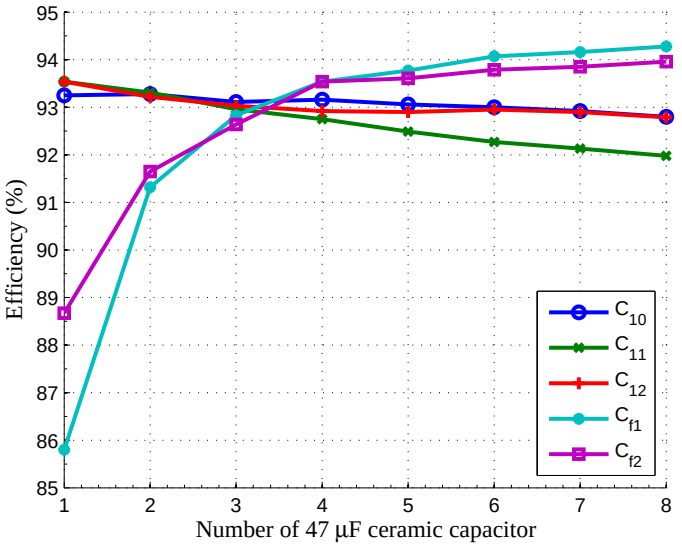
1. The number of each capacitor varies from one to eight paralleled 47 μF capacitors. Fig. 5.15 shows the efficiency of the second-order ESC converter when one of the capacitor value varies.

2. The number of capacitors contributing to G_1 or G_2 varies while K_{fb1} and K_{fb2} are kept constant. Fig. 5.16 shows the efficiency of the second-order ESC converter varies with the number of 47 μF capacitors contributing G_1 at a constant K_{fb1} in Fig. 5.16(a) and similarly contributing G_2 in Fig. 5.16(b).

3. K_{fbi} varies from 1 to 7 while the number of 47 μF capacitors in G_i is kept at 8,

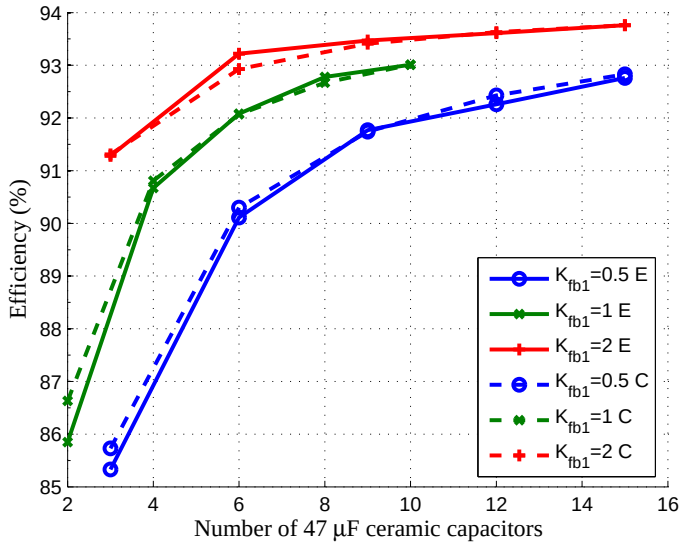


(a)

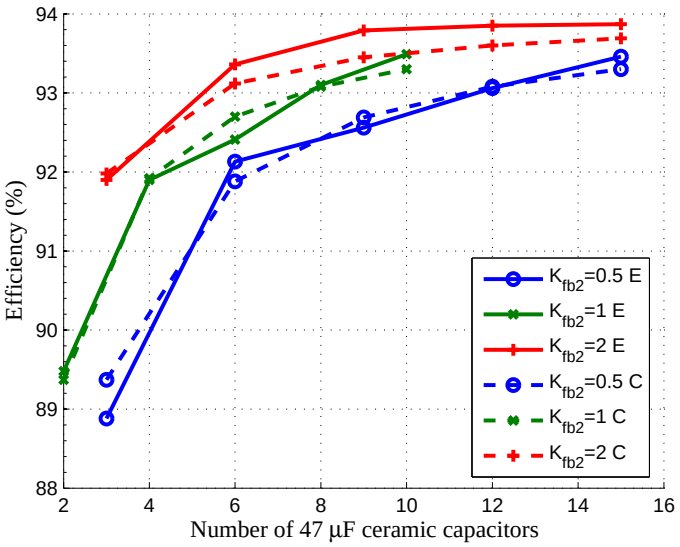


(b)

Figure 5.15: The efficiency of the second-order ESC converter simulated in (a) and measured in (b) versus the number of paralleled 47 μF ceramic capacitors for one of the capacitors. The other components are kept constant at their nominal values.



(a)



(b)

Figure 5.16: The efficiency of the second-order ESC converter versus the number of 47 μF ceramic capacitors contributing G_1 in (a) and G_2 in (b) while K_{fb1} and K_{fb2} are kept constant. The legends E and C present experimental and calculated results respectively.

where $i = 1, 2$. Fig. 5.17 shows the efficiency of the second-order ESC converter varies with K_{fb1} and k_{fb2}.

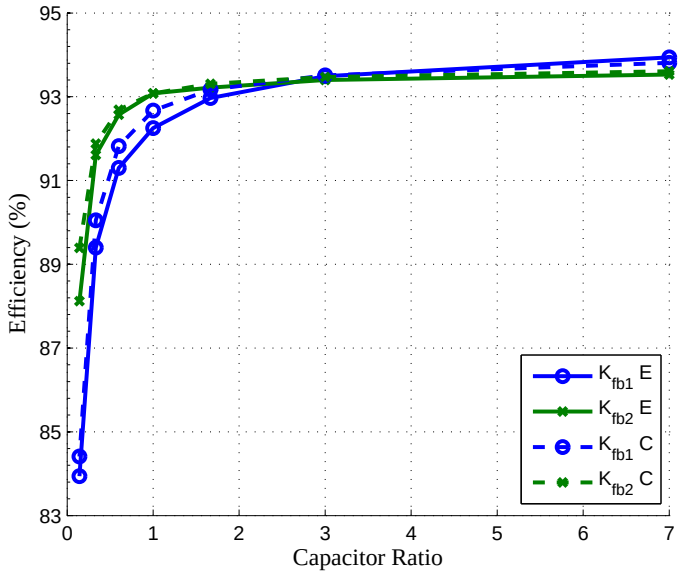


Figure 5.17: The efficiency of the second-order ESC converter versus K_{fbi} while the number of 47 μF capacitors in G_i is kept at 8, where $i = 1, 2$. The legends E and C present experimental and calculated results respectively.

5.5.3.2 Efficiency versus Resistance Variation

Here, the in-circuit parasitic resistances which will affect the converter efficiency is investigated by calculation.

1. Fig. 5.18 shows the sensitivity of the converter efficiency to each major resistance. The result indicates that the efficiency is most sensitive to R_3 and R_5, which are on the current path of the load. While the efficiency is least sensitive to R_1, which is on the current path of the input power source of a step-down converter.

2. Fig. 5.19 shows the sensitivity of the converter efficiency to each capacitor ESR resistance. According to the result, efficiency is least sensitive to bypass capacitor ESR. The bypass capacitor ESR can even have slight improvement on efficiency

as indicated by the sensitivity to R_{10} of C_{10} in Fig. 5.19. The converter efficiency is sensitive to the ESRs of C_{f1} and C_{f2} and proportional to the current flowing through the ESR.

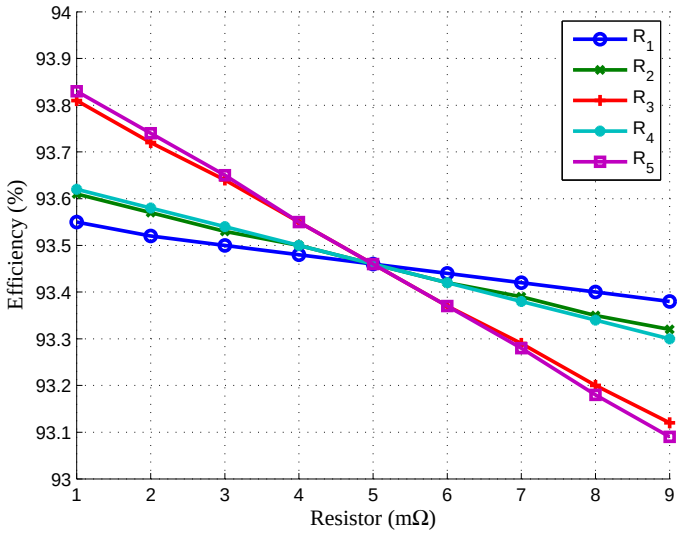


Figure 5.18: The parasitic resistors in the circuit effect on the second-order ESC converter's efficiency

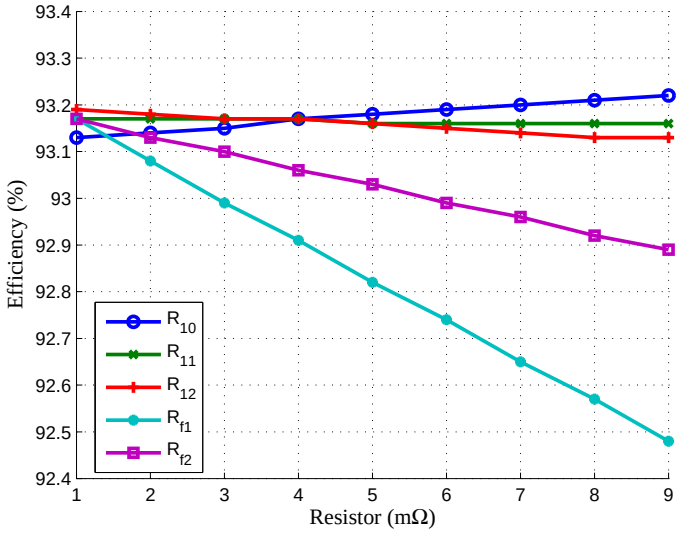


Figure 5.19: The ESR of each capacitors effects on the efficiency of second-order ESC converter.

In order to verify the sensitivity of efficiency to bypass capacitor ESR, C_{11} and C_{12} being originally ceramic capacitors are replaced by electrolytic capacitors. The experiment result shown in Fig. 5.20 confirms the calculation.

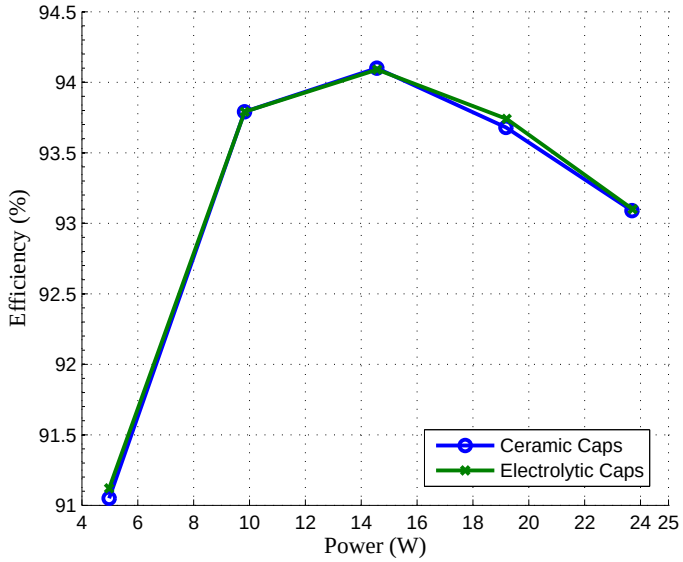


Figure 5.20: The experiment result of replacing the multi-layer ceramic capacitors of C_{11} and C_{12} with electrolytic capacitors.

5.5.3.3 Efficiency Impact from Switching Frequency

Fig. 5.21 shows the sensitivity of efficiency to the output load at various converter switching frequencies. Generally, losses due to switching is increasing with increasing switching frequency and nearly constant with increasing output loading. We can observe efficiency improvement at light load due to switching loss is relatively significant. On the other hand, at the heavy load, switching loss is relatively insignificant and thus efficiency is less sensitive to switching frequency. However, at heavy load, a higher switching frequency leads to a lower voltage ripples of the capacitors, thus, a relatively higher efficiency can be observed with higher switching frequency.

5.5.4 Design guideline

According to the properties of ESC converter, a design guideline is recommended as follows:

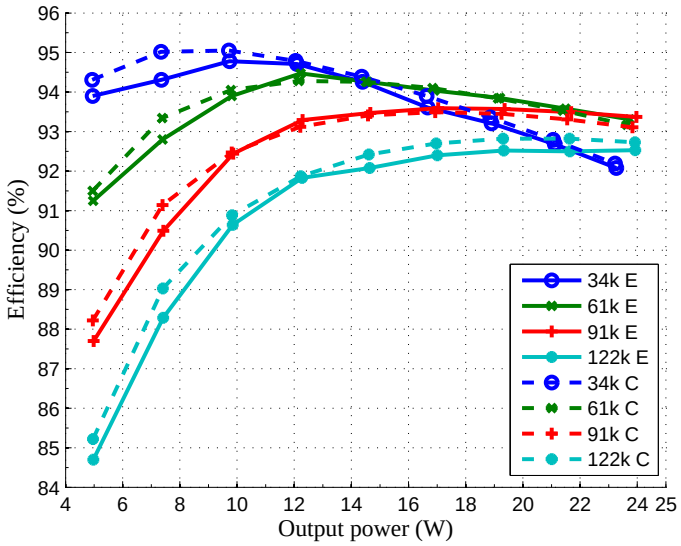


Figure 5.21: The experiment and calculation waveforms of switching frequency effects on the second-order ESC converter.

5.5.4.1 Design of Energy Flow using Capacitors

1. **Capacitor ratio.** According to the Fig. 5.16, select $K_{fb1} = 3.0$ and $K_{fb2} = 1.0$, as further increase of K_{fb1} and K_{fb2} cannot significantly increase the converter efficiency.

2. **Flying capacitor value.** In the flying capacitor discharging state, the flying capacitor provides the energy for the load for an amount given by

$$E_{cf2R} = \frac{TV_oI_o}{2}. \tag{5.40}$$

While in the flying capacitor charging state, the stored energy of each flying capacitor is given by

$$E_{st} = \frac{f_sC_{fx}(2 \cdot V_{fx} - \Delta V_{fx})\Delta V_{fx}}{2}, \tag{5.41}$$

where, $x = 1, 2$. As the voltage ripple is very small compared with the average of the flying capacitor voltage, (5.41) can be simplified to

$$E_{st} = f_s C_{fx} V_{fx} \Delta V_{fx}. \tag{5.42}$$

Equating $E_{cf2R} = Est$, selecting a proper ΔV_{fx}, the flying capacitor value can be calculated. A smaller ΔV_{fx} leads to a higher converter efficiency.

3. **Bypass capacitor values.** According to the capacitor ratio selected, the bypass capacitor can be calculated.

Table 5.5: Maximum voltage stress of the capacitors

C_{10}	C_{11}	C_{12}	C_{f1}	C_{f2}
$\frac{V_{in}}{4}$	$\frac{V_{in}}{4}$	$\frac{V_{in}}{2}$	$\frac{V_{in}}{4}$	$\frac{V_{in}}{2}$

5.5.4.2 Switches Selection

In ESC converter, the voltage stresses of switches are given in Table 5.6 which are mostly a fraction of the supplied voltage. Hence, in the ESC converter, the switch loss is small. However, the ON resistance R_{dson} of switches should be small as it has significant effect on the converter efficiency.

Table 5.6: Maximum voltage stress of the switches

	state 1	state 2	state 3	state 4
S_{10d}	0	$\frac{V_{in}}{4}$	$\frac{V_{in}}{4}$	0
S_{10u}	0	$\frac{V_{in}}{4}$	$\frac{V_{in}}{4}$	0
S_{11d}	$\frac{V_{in}}{4}$	0	0	$\frac{V_{in}}{4}$
S_{11u}	$\frac{V_{in}}{4}$	0	0	$\frac{V_{in}}{4}$
S_{20d}	$\frac{V_{in}}{2}$	$\frac{V_{in}}{2}$	0	0
S_{20u}	$\frac{V_{in}}{2}$	$\frac{V_{in}}{2}$	0	0
S_{21d}	0	0	$\frac{V_{in}}{2}$	$\frac{V_{in}}{2}$
S_{21u}	0	0	$\frac{V_{in}}{2}$	$\frac{V_{in}}{2}$

5.6 Conclusion

This chapter applies the exponential SC converter as a front stage of the two-stage converter. The experimental results show that the two-stage converter has a better performance compared with the single buck converter, especially in the extremely high input voltage situations, in which the input voltage is over the rated input voltage of the Buck converter. Moreover, the results also indicate that the second-order ESC-buck converter has a better efficiency than the first-order ESC-buck converter. The analysis shows that a proper capacitor ratio the flying capacitor and by-pass capacitors of the ESC converter can improve the efficiency with the same amount of components. Designing a exponential SC converter should try to reduce the resistance of the flying capacitor branch in the first-stage of the SC converter. For a heavy load output, higher switching frequency leads a higher efficiency. While in the light load output, it is better to choose a lower switching frequency.

Chapter 6

Conclusion

This chapter summarizes the contributions which have been achieved in this project. Also, some feasible suggestions and potential research areas will also be given for the future research extension.

6.1 Contributions of the Thesis

This thesis reports two major contributions. Firstly, it provides several topologies, which include modified hybrid SC-buck converter and exponential SC converter, for large-voltage-conversion applications with high performance. Both topologies are experimentally proven to have high efficiency compared with the traditional single-stage buck converter. Secondly, analytical or mixed analytical and numerical method are developed for the topologies. The analytical method, which is based on the energy flow paths, clearly shows the energy losses due to the number of energy conversions. This method can easily find the efficiency improvement for the converter. The mixed analytical and numerical method is effective and accurate for the complex circuit. Moreover, this method can obtain the sensitivity of each component parameter on the conversion efficiency. The developed prototypes are investigated to verify the topologies and the

analyzing methods.

Specifically, the contributions include the following:

1. A modified hybrid SC-buck converter which is highly efficient and easily integrated for high-voltage-gain applications has been introduced.

2. An analytical method based on the energy flow for the hybrid SC-buck converter has been conducted. The analytical method is applied for an effective design of an hybrid SC-buck converter.

3. A family of exponential SC converter which is suitable for high voltage gain conversion and low cost has been proposed. The lack of regulation of the exponential SC converter is compensated by a buck converter with good regulation to form an efficient two-stage high-voltage-gain converter. Experimental verifications of the topology have been provided.

4. A mixed analytical and numerical method named discrete-time analysis is presented for the exponential SC converter to solve the high-order differential equation of the ESC converter. Experiments to verify the effectiveness and accuracy of the method are provided.

6.2 Suggestions for Future Work

Based on the theoretical knowledge built up through the research, some suggestions are given for the future research extension.

6.2.1 Adaptive Exponential SC-buck Converter

Although the thesis provides a high efficiency exponential SC-buck converter with a fixed-voltage-ratio first-stage converter, it is worthwhile to design an adaptive conversion ratio exponential SC for the two-stage converter.

6.2.2 Inserting Small Inductor in the Exponential SC Converter

It is well known that zero-voltage/current switching technology is widely applied in converters to improve the converter efficiency. In SC converters, some switches may encounter high current stress during their turning on instance, inserting in small inductor or utilizing the parasitic inductor in the circuit to achieve zero-current switch on may be a way to further improve the converter efficiency.

6.2.3 Discrete-time Analysis Applied in Other Converter

This thesis has developed methods with verifications for the effective and accurate design of the exponential SC converter. It is worth to extend the method into the other complex circuits.

Appendix A

Parameters in Second-order ESC Analysis

In this appendix, according to the circuit analysis, the below equation is calculated first,

$$\mathbf{I}(i) = \mathbf{D}_k\mathbf{V}(i-1) + \mathbf{E}_k\mathbf{U}_k, \text{ where} \tag{A.1}$$

$$\mathbf{D}_k = \begin{bmatrix} d_{k,11} & d_{k,12} & d_{k,13} & d_{k,14} & d_{k,15} \\ d_{k,21} & d_{k,22} & d_{k,23} & d_{k,24} & d_{k,25} \\ d_{k,31} & d_{k,32} & d_{k,33} & d_{k,34} & d_{k,35} \\ d_{k,41} & d_{k,42} & d_{k,43} & d_{k,44} & d_{k,45} \\ d_{k,51} & d_{k,52} & d_{k,53} & d_{k,54} & d_{k,55} \end{bmatrix}, \text{ and} \tag{A.2}$$

$$\mathbf{E}_k = \begin{bmatrix} e_{k,11} & e_{k,12} \\ e_{k,21} & e_{k,22} \\ e_{k,31} & e_{k,32} \\ e_{k,41} & e_{k,42} \\ e_{k,51} & e_{k,52} \end{bmatrix} \tag{A.3}$$

Where $k = 1, 2, 3, 4$, refer to the four states.

Then according to 4.10, so the value of $\mathbf{A}_k$ and $\mathbf{B}_k$ can be calculated by equations,

$$\mathbf{A}_k = \mathbf{I}_5 + \mathbf{R}_{eq}\mathbf{D}_k, \text{ and} \tag{A.4}$$

$$\mathbf{B}_k = \mathbf{R}_{eq}\mathbf{E}_k. \tag{A.5}$$

where: $\mathbf{I}_5$ is unit matrix.

A.1 State 1

State 1 equivalent circuit is shown in Fig. 4.11(a). In state 1, there are such equations,

$$I_{12}(i) + I_{f2}(i) = I_{11}(i) \tag{A.6}$$

$$I_{10}(i) + I_{f1}(i) = I_{11}(i) - I_o \tag{A.7}$$

$$R_{1s2} \cdot I_{f2}(i) + V_{f2}(i) = V_{12}(i) + R_{12} \cdot I_{12}(i) \tag{A.8}$$

$$R_{1s1} \cdot I_{f1}(i) + V_{f1}(i) = V_{10}(i) + R_{10} \cdot I_{10}(i) \tag{A.9}$$

$$\begin{aligned} &V_{10}(i) + V_{11}(i) + V_{12}(i) + R_{10} \cdot I_{10}(i) + R_{11} \cdot I_{11}(i) \\ &+ R_{12} \cdot I_{12}(i) + R_{1sa} \cdot I_{11}(i) + R_{1sb} \cdot (I_{10}(i) + I_o) = V_{in} \end{aligned} \tag{A.10}$$

Where: $R_{1sa} = R_1 + R_4$, $R_{1sb} = R_5$;
$R_{1s1} = 2 \cdot R_{dson} + R_{f1} + R_3$, $R_{1s2} = 2 \cdot R_{dson} + R_{f2} + R_2$.

According to equation A.9 and 4.6, there is

$$I_{f1}(i) = \frac{\Delta V_{1s1}(i) + R_{b10} \cdot I_{10}(i)}{R_{b1}} \tag{A.11}$$

Where: $R_{b1} = R_{1s1} + R_{eqf1}$, $R_{b10} = R_{10} + R_{eq10}$;
$\Delta V_{1s1}(i) = V_{10}(i-1) - V_{f1}(i-1)$.

According to equations A.8 and 4.6, there is

$$I_{f2}(i) = \frac{\Delta V_{1s2}(i) + R_{b12} \cdot I_{12}(i)}{R_{b2}} \tag{A.12}$$

Where: $R_{b2} = R_{1s2} + R_{eqf2}$, $R_{b12} = R_{12} + R_{eq12}$;
$\Delta V_{1s2}(i) = V_{12}(i-1) - V_{f2}(i-1)$.

Substitute equation A.11 into equation A.7, there is

$$I_{10}(i) = \frac{R_{b1}}{R_{1l1}} \cdot I_{11}(i) - \frac{R_{b1}}{R_{1l1}} \cdot I_o - \frac{1}{R_{1l1}} \cdot \Delta V_{1s2}(i) \tag{A.13}$$

Where: $R_{1l1} = R_{b1} + R_{b10}$.

Substitute equation A.12 to equation A.6, there is

$$I_{12}(i) = \frac{R_{b2}}{R_{1l2}} \cdot I_{11}(i) - \frac{1}{R_{1l2}} \cdot \Delta V_{1s2}(i) \tag{A.14}$$

Where: $R_{1l2} = R_{b2} + R_{b12}$.

Substitute equations 4.6, A.14 and A.13, there is

$$\begin{aligned} I_{11}(i) = {} & \frac{R_{b10} + R_{1sb}}{R_{1a}R_{1l1}}\Delta V_{1s1}(i) + \frac{R_{b12}}{R_{1a}R_{1l2}}\Delta V_{1s2}(i) \\ & + \frac{\Delta V_{1s}(i)}{R_{1a}} + (\frac{R_{1b}(R_{b10} + R_{1sb})}{R_{1a}R_{1l1}} - \frac{R_{1sb}}{R_{1a}})I_o \end{aligned} \tag{A.15}$$

Where:
$\Delta V_{1s}(i) = V_{in} - V_{10}(i-1) - V_{11}(i-1) - V_{12}(i-1)$;
$R_{1a} = \frac{(R_{b10} + R_{1sb})R_{b1}}{R_{1l1}} + R_{b11} + R_{1sa} + \frac{R_{b12}R_{b2}}{R_{1l2}}$.
Substitute equation A.15 to equations A.12– A.13, 4.6, we can get all capacitors' voltages and currents where i from 1 to M.

According to above analysis, the parameter in A.1 can be calculated as follows,

$$d_{1,11} = -\frac{R_{1a}R_{1l1} + (R_{b1} - R_{1sb})R_{b1}}{R_{1a}R_{1l1}^2},$$
$$d_{1,12} = -\frac{R_{b1}}{R_{1a}R_{1l1}},$$
$$d_{1,13} = -\frac{R_{b1}R_{b2}}{R_{1a}R_{1l1}R_{1l2}},$$
$$d_{1,14} = \frac{R_{1a}R_{1l1} - (R_{b10} + R_{1sb})R_{b1}}{R_{1a}R_{1l1}^2},$$
$$d_{1,15} = -\frac{R_{b1}R_{b12}}{R_{1a}R_{1l1}R_{1l2}},$$
$$d_{1,21} = -\frac{R_{b1} - R_{1sb}}{R_{1a}R_{1l1}},$$
$$d_{1,22} = -\frac{1}{R_{1a}},$$
$$d_{1,23} = -\frac{R_{b2}}{R_{1a}R_{1l2}},$$
$$d_{1,24} = -\frac{R_{b10} + R_{1sb}}{R_{1a}R_{1l1}},$$
$$d_{1,25} = -\frac{R_{b12}}{R_{1a}R_{1l2}},$$
$$d_{1,31} = -\frac{(R_{b1} - R_{1sb})R_{b2}}{R_{1a}R_{1l1}R_{1l2}},$$
$$d_{1,32} = -\frac{R_{b2}}{R_{1a}R_{1l2}},$$
$$d_{1,33} = -\frac{R_{b2}^2 + R_{1a}R_{1l2}}{R_{1a}R_{1l2}^2},$$
$$d_{1,34} = -\frac{(R_{b10} + R_{1sb})R_{b2}}{R_{1a}R_{1l1}R_{1l2}},$$
$$d_{1,35} = \frac{R_{1a}R_{1l2} - R_{b2}R_{b12}}{R_{1a}R_{1l2}^2},$$
$$d_{1,41} = -\frac{(R_{b1} - R_{1sb})R_{b1}R_{b10} - R_{1a}R_{1l1}R_{b1}}{R_{1a}R_{1l1}^2R_{b1}},$$
$$d_{1,42} = -\frac{R_{b10}}{R_{1a}R_{1l1}},$$
$$d_{1,43} = -\frac{R_{b2}R_{b10}}{R_{1a}R_{1l1}R_{1l2}},$$
$$d_{1,44} = -\frac{(R_{b10} + R_{1sb})R_{b10} + R_{1a}R_{1l1}}{R_{1a}R_{1l1}^2},$$
$$d_{1,45} = -\frac{R_{b10}R_{b12}}{R_{1a}R_{1l1}R_{1l2}},$$
$$d_{1,51} = -\frac{(R_{b1} - R_{1sb})R_{b12}}{R_{1a}R_{1l1}R_{1l2}},$$
$$d_{1,52} = -\frac{R_{b12}}{R_{1a}R_{1l2}},$$

$$d_{1,53} = -\frac{R_{b2}^2 R_{b12} + R_{1a} R_{1l2} R_{b12}}{R_{1a} R_{1l2}^2 R_{b2}},$$
$$d_{1,54} = -\frac{(R_{b10} + R_{1sb}) R_{b12}}{R_{1a} R_{1l1} R_{1l2}},$$
$$d_{1,55} = \frac{R_{1a} R_{1l2} R_{b12} - R_{b2} R_{b12}^2}{R_{1a} R_{1l2}^2 R_{b2}},$$
$$e_{1,11} = \frac{R_{b1}}{R_{1a} R_{1l1}},$$
$$e_{1,12} = \frac{(R_{b10} - R_{1a}) R_{b1}^2 - (R_{1a} + R_{1sb}) R_{b1} R_{b10}}{R_{1a} R_{1l1}^2};$$
$$e_{1,21} = \frac{1}{R_{1a}},$$
$$e_{1,22} = \frac{(R_{b1} - R_{1sb}) R_{b10}}{R_{1a} R_{1l1}};$$
$$e_{1,31} = \frac{R_{b2}}{R_{1a} R_{1l2}},$$
$$e_{1,32} = \frac{(R_{b1} - R_{1sb}) R_{b10} R_{b2}}{R_{1a} R_{1l1} R_{1l2}};$$
$$e_{1,41} = \frac{R_{b10}}{R_{1a} R_{1l1}},$$
$$e_{1,42} = \frac{(R_{b1} - R_{1sb}) R_{b10}^2 - R_{1a} R_{1l1} R_{b10}}{R_{1a} R_{1l1}^2};$$
$$e_{1,51} = \frac{R_{b12}}{R_{1a} R_{1l2}},$$
$$e_{1,52} = \frac{(R_{b1} - R_{1sb}) R_{b10} R_{b12}}{R_{1a} R_{1l1} R_{1l2}};$$

A.2 State 2

State 2 equivalent circuit is shown in Fig. 4.11(b). In state 2, there are such equations:

$$I_{12}(i) + I_{f2}(i) = I_{10}(i) + I_o \tag{A.16}$$

$$I_{11}(i) + I_{f1}(i) = I_{10}(i) + I_o \tag{A.17}$$

$$R_{2s2} \cdot I_{f2}(i) + V_{f2}(i) = V_{12}(i) + R_{12} \cdot I_{12}(i) \tag{A.18}$$

$$R_{2s1} \cdot I_{f1}(i) + V_{f1}(i) = V_{11}(i) + R_{11} \cdot I_{11}(i) \tag{A.19}$$

$$\begin{aligned} &V_{10}(i) + V_{11}(i) + V_{12}(i) + R_{10} \cdot I_{10}(i) + R_{11} \cdot I_{11}(i) \\ &+ R_{12} \cdot I_{12}(i) + R_{2sa} \cdot (I_{10}(i) + I_o) = V_{in} \end{aligned} \tag{A.20}$$

Where: $R_{2sa} = R_1 + R_4 + R_5$;
$R_{2s1} = 2 \cdot R_{dson} + R_{f1} + R_3$, $R_{2s2} = 2 \cdot R_{dson} + R_{f2} + R_2$.

According to equation A.19 and 4.6, there is

$$I_{f1}(i) = \frac{\Delta V_{2s1}(i) + R_{b11} \cdot I_{11}(i)}{R_{b1}} \tag{A.21}$$

Where: $R_{b1} = R_{2s1} + R_{eqf1}$, $R_{b11} = R_{11} + R_{eq11}$;
$\Delta V_{2s1}(i) = V_{11}(i-1) - V_{f1}(i-1)$.

According to equations A.18 and 4.6, there is

$$I_{f2}(i) = \frac{\Delta V_{2s2}(i) + R_{b12} \cdot I_{12}(i)}{R_{b2}} \tag{A.22}$$

Where: $R_{b2} = R_{2s2} + R_{eqf2}$, $R_{b12} = R_{12} + R_{eq12}$;
$\Delta V_{2s2}(i) = V_{12}(i-1) - V_{f2}(i-1)$.

Substitute equation A.21 into equation A.17, there is

$$I_{11}(i) = \frac{R_{b1}}{R_{2l1}} \cdot I_{10}(i) + \frac{R_{b1}}{R_{2l1}} \cdot I_o - \frac{1}{R_{2l1}} \cdot \Delta V_{2s1}(i) \tag{A.23}$$

Where: $R_{2l1} = R_{b1} + R_{b11}$.

Substitute equation A.22 to equation A.16, there is

$$I_{12}(i) = \frac{R_{b2}}{R_{2l2}} \cdot I_{10}(i) + \frac{R_{b2}}{R_{2l2}} \cdot I_o - \frac{1}{R_{2l2}} \cdot \Delta V_{2s2}(i) \tag{A.24}$$

Where: $R_{2l2} = R_{b2} + R_{b12}$.

Substitute equations 4.6, A.24 and A.23, there is

$$\begin{aligned} I_{10}(i) = {} & \frac{R_{b11}}{R_{2a}R_{2l1}}\Delta V_{2s1}(i) + \frac{R_{b12}}{R_{2a}R_{2l2}}\Delta V_{2s2}(i) \\ & + \frac{\Delta V_{2s}(i)}{R_{2a}} - (\frac{R_{2sa}}{R_{2a}} + \frac{R_{b1}R_{b11}}{R_{2a}R_{2l1}} + \frac{R_{b2}R_{b12}}{R_{2a}R_{2l2}})I_o \end{aligned} \tag{A.25}$$

Where:

$\Delta V_{2s}(i) = V_{in} - V_{10}(i-1) - V_{11}(i-1) - V_{12}(i-1)$;

$R_{2a} = R_{2sa} + R_{b10} + \frac{R_{b1}R_{b11}}{R_{2l1}} + \frac{R_{b2}R_{b12}}{R_{2l2}}$.

Substitute equation A.25 to equations A.22– A.23, 4.6, we can get all capacitors' voltages and currents of state 2.

According to above analysis, the parameter in A.1 can be calculated as follows,

$d_{2,11} = -\frac{1}{R_{2a}}$,

$d_{2,12} = -\frac{R_{b1}}{R_{2a}R_{2l1}}$,

$d_{2,13} = -\frac{R_{b2}}{R_{2a}R_{2l2}}$,

$d_{2,14} = -\frac{R_{b11}}{R_{2a}R_{2l1}}$,

$d_{2,15} = -\frac{R_{b12}}{R_{2a}R_{2l2}}$,

$$
\begin{aligned}
d_{2,21} &= -\frac{R_{b1}}{R_{2a}R_{2l1}},\\
d_{2,22} &= -\frac{R_{b1}^2 + R_{2a}R_{2l1}}{R_{2a}R_{2l1}^2},\\
d_{2,23} &= -\frac{R_{b1}R_{b2}}{R_{2a}R_{2l1}R_{2l2}},\\
d_{2,24} &= -\frac{R_{b1}R_{b11} - R_{2a}R_{2l1}}{R_{2a}R_{2l1}^2},\\
d_{2,25} &= -\frac{R_{b1}R_{b12}}{R_{2a}R_{2l1}R_{2l2}},\\
d_{2,31} &= -\frac{R_{b2}}{R_{2a}R_{2l2}},\\
d_{2,32} &= -\frac{R_{b1}R_{b2}}{R_{2a}R_{2l1}R_{2l2}},\\
d_{2,33} &= -\frac{R_{b2}^2 + R_{2a}R_{2l2}}{R_{2a}R_{2l2}^2},\\
d_{2,34} &= -\frac{R_{b2}R_{b11}}{R_{2a}R_{2l1}R_{2l2}},\\
d_{2,35} &= -\frac{R_{b2}R_{b12} - R_{2a}R_{2l2}}{R_{2a}R_{2l2}^2},\\
d_{2,41} &= -\frac{R_{b11}}{R_{2a}R_{2l1}},\\
d_{2,42} &= -\frac{R_{b1}R_{b11} - R_{2a}R_{2l1}}{R_{2a}R_{2l1}^2},\\
d_{2,43} &= -\frac{R_{b11}R_{b2}}{R_{2a}R_{2l1}R_{2l2}},\\
d_{2,44} &= -\frac{R_{2a}R_{2l1} + R_{b11}^2}{R_{2a}R_{2l1}^2},\\
d_{2,45} &= -\frac{R_{b11}R_{b12}}{R_{2a}R_{2l1}R_{2l2}},\\
d_{2,51} &= -\frac{R_{b12}}{R_{2a}R_{2l2}},\\
d_{2,52} &= -\frac{R_{b1}R_{b12}}{R_{2a}R_{2l1}R_{1l2}},\\
d_{2,53} &= -\frac{R_{b2}^2R_{b12} + R_{2a}R_{2l2}R_{b12}}{R_{2a}R_{2l2}^2R_{b2}},\\
d_{2,54} &= -\frac{R_{b11}R_{b12}}{R_{2a}R_{2l1}R_{2l2}},\\
d_{2,55} &= -\frac{R_{b2}^2R_{b12} - R_{2a}R_{2l2}R_{b12}}{R_{2a}R_{2l2}^2R_{b2}},\\
e_{2,11} &= \frac{1}{R_{2a}},
\end{aligned}
$$

$$e_{2,12} = \frac{R_{2sa}R_{2l1}R_{2l2} + R_{2l2}R_{b1}R_{b11} + R_{2l1}R_{b2}R_{b12}}{R_{2a}R_{1l1}R_{2l2}};$$
$$e_{2,21} = \frac{R_{b1}}{R_{2a}R_{2l1}},$$
$$e_{2,22} = -\frac{(R_{2sa} - R_{2a})R_{b1}}{R_{2a}R_{2l1}} - \frac{R_{b1}^2 R_{b11}}{R_{2a}R_{2l1}^2} - \frac{R_{b1}R_{b2}R_{b12}}{R_{2a}R_{2l1}R_{2l2}};$$
$$e_{2,31} = \frac{R_{b2}}{R_{2a}R_{2l2}},$$
$$e_{2,32} = -\frac{(R_{2sa} - R_{2a})R_{b2}}{R_{2a}R_{2l2}} - \frac{R_{b1}R_{b2}R_{b11}}{R_{2a}R_{2l1}R_{2l2}} - \frac{R_{b2}^2 R_{b12}}{R_{2a}R_{2l2}^2};$$
$$e_{2,41} = \frac{R_{b11}}{R_{2a}R_{2l1}},$$
$$e_{2,42} = -\frac{(R_{2sa} - R_{2a})R_{b11}}{R_{2a}R_{2l1}} - \frac{R_{b1}R_{b11}^2}{R_{2a}R_{2l1}^2} - \frac{R_{b2}R_{b11}R_{b12}}{R_{2a}R_{2l1}R_{2l2}};$$
$$e_{2,51} = \frac{R_{b12}}{R_{2a}R_{2l2}},$$
$$e_{2,52} = -\frac{(R_{2sa} - R_{2a})R_{b12}}{R_{2a}R_{2l2}} - \frac{R_{b1}R_{b11}R_{b12}}{R_{2a}R_{2l1}R_{2l2}} - \frac{R_{b2}R_{b12}^2}{R_{2a}R_{2l2}^2};$$

A.3 State 3

State 3 equivalent circuit is shown in Fig. 4.11(c). In state 3, there are such equations:

$$I_{12}(i) - I_{f2}(i) = I_{10}(i) + I_o \tag{A.26}$$
$$I_{11}(i) + I_{f1}(i) = I_{10}(i) + I_o \tag{A.27}$$
$$\begin{aligned} &R_{3s2} \cdot I_{f2}(i) + V_{f2}(i) \\ &= V_{in} - V_{12}(i) - (R_{12} + R_{3sa}) \cdot I_{12}(i) \end{aligned} \tag{A.28}$$
$$R_{3s1} \cdot I_{f1}(i) + V_{f1}(i) = V_{11}(i) + R_{11} \cdot I_{11}(i) \tag{A.29}$$
$$\begin{aligned} &V_{10}(i) + V_{11}(i) + V_{12}(i) + R_{12} \cdot I_{12}(i) + \\ &R_{3sa} \cdot I_{12}(i) + R_{3sb} \cdot (I_{10}(i) + I_o) = V_{in} \end{aligned} \tag{A.30}$$

Where: $R_{3sa} = R_1$, $R_{3sb} = R_4 + R_5$;

$R_{3s1} = 2 \cdot R_{dson} + R_{f1} + R_3$; $R_{3s2} = 2 \cdot R_{dson} + R_{f2} + R_2$.

According to equation A.29 and 4.6, there is

$$I_{f1}(i) = \frac{\Delta V_{3s1}(i) + R_{b11} \cdot I_{11}(i)}{R_{b1}} \tag{A.31}$$

Where: $R_{b1} = R_{3s1} + R_{eqf1}$, $R_{b11} = R_{11} + R_{eq11}$;
$\Delta V_{3s1}(i) = V_{11}(i-1) - V_{f1}(i-1)$.

According to equations A.28 and 4.6, there is

$$I_{f2}(i) = \frac{\Delta V_{3s2}(i) - (R_{b12} + R_{3sa}) \cdot I_{12}(i)}{R_{b2}} \tag{A.32}$$

Where: $R_{b2} = R_{3s2} + R_{eqf2}$, $R_{b12} = R_{12} + R_{eq12}$;
$\Delta V_{3s2}(i) = V_{in} - V_{12}(i-1) - V_{f2}(i-1)$.

Substitute equation A.31 into equation A.27, there is

$$I_{11}(i) = \frac{R_{b1}}{R_{3l1}} \cdot I_{10}(i) + \frac{R_{b1}}{R_{3l1}} \cdot I_o - \frac{1}{R_{3l1}} \cdot \Delta V_{3s1}(i) \tag{A.33}$$

Where: $R_{3l1} = R_{b1} + R_{b11}$.

Substitute equation A.32 to equation A.26, there is

$$I_{12}(i) = \frac{R_{b2}}{R_{3l2}} \cdot I_{10}(i) + \frac{R_{b2}}{R_{3l2}} \cdot I_o + \frac{1}{R_{3l2}} \cdot \Delta V_{3s2}(i) \tag{A.34}$$

Where:$R_{3l2} = R_{b2} + R_{b12} + R_{3sa}$.

Substitute equations 4.6, A.34 and A.33, there is

$$I_{10}(i) = \frac{R_{b11}\Delta V_{3s1}(i)}{R_{3a}R_{3l1}} - \frac{R_{3p2}\Delta V_{2s2}(i)}{R_{3a}R_{3l2}} + \frac{\Delta V_{3s}(i)}{R_{3a}} + (\frac{R_{b1}R_{b11}}{R_{3a}R_{3l1}} + \frac{R_{b2}R_{3p1}}{R_{3a}R_{3l2}} - \frac{R_{3sb}}{R_{3a}})I_o \tag{A.35}$$

Where: $R_{3p1} = R_{b10} + R_{3sb}$, $R_{3p2} = R_{b12} + R_{3sa}$;

$\Delta V_{3s}(i) = V_{in} - V_{10}(i-1) - V_{11}(i-1) - V_{12}(i-1)$;

$R_{3a} = R_{3sb} + R_{b10} + \frac{R_{b1}R_{b11}}{R_{3l1}} + \frac{(R_{b12} + R_{3sa})R_{b2}}{R_{3l2}}$.

Substitute equation A.35 to equations 4.6, A.32– A.33, we can get all capacitors' voltages and currents of state 3.

According to above analysis, the parameter in A.1 can be calculated as follows,

$d_{3,11} = -\frac{1}{R_{3a}}$,

$d_{3,12} = -\frac{R_{b1}}{R_{3a}R_{3l1}}$,

$d_{3,13} = -\frac{R_{b2}}{R_{3a}R_{3l2}}$,

$d_{3,14} = -\frac{R_{b11}}{R_{3a}R_{3l1}}$,

$d_{3,15} = \frac{R_{b12} + R_{3sa}}{R_{3a}R_{3l2}}$,

$d_{3,21} = -\frac{R_{b1}}{R_{3a}R_{3l1}}$,

$d_{3,22} = -\frac{R_{b1}^2 + R_{3a}R_{3l1}}{R_{3a}R_{3l1}^2}$,

$d_{3,23} = -\frac{R_{b1}R_{b2}}{R_{3a}R_{3l1}R_{3l2}}$,

$d_{3,24} = -\frac{R_{b1}R_{b11} - R_{3a}R_{3l1}}{R_{3a}R_{3l1}^2}$,

$d_{3,25} = \frac{R_{b1}R_{b12} + R_{b1}R_{3sa}}{R_{3a}R_{3l1}R_{3l2}}$,

$d_{3,31} = -\frac{R_{b2}}{R_{3a}R_{3l2}}$,

$d_{3,32} = -\frac{R_{b1}R_{b2}}{R_{3a}R_{3l1}R_{3l2}}$,

$d_{3,33} = -\frac{R_{b2}^2 + R_{3a}R_{3l2}}{R_{3a}R_{3l2}^2}$,

$$d_{3,34} = -\frac{R_{b2}R_{b11}}{R_{3a}R_{3l1}R_{3l2}},$$
$$d_{3,35} = \frac{R_{3l2}R_{b2} - R_{b2}^2 - R_{3a}R_{3l2}}{R_{3a}R_{3l2}^2},$$
$$d_{3,41} = -\frac{R_{b11}}{R_{3a}R_{3l1}},$$
$$d_{3,42} = -\frac{R_{b1}R_{b11} - R_{3a}R_{3l1}}{R_{3a}R_{3l1}^2},$$
$$d_{3,43} = -\frac{R_{b11}R_{b2}}{R_{3a}R_{3l1}R_{3l2}},$$
$$d_{3,44} = -\frac{R_{b11}^2 + R_{3a}R_{3l1}}{R_{3a}R_{3l1}^2},$$
$$d_{3,45} = \frac{R_{b11}R_{b12} + R_{b11}R_{3sa}}{R_{3a}R_{3l1}R_{3l2}},$$
$$d_{3,51} = \frac{R_{b12} + R_{3sa}}{R_{3a}R_{3l2}},$$
$$d_{3,52} = \frac{R_{b1}(R_{b12} + R_{3sa})}{R_{3a}R_{3l1}R_{3l2}},$$
$$d_{3,53} = \frac{R_{3l2}(R_{b2} - R_{3a}) - R_{b2}^2}{R_{3a}R_{3l2}^2},$$
$$d_{3,54} = \frac{R_{b11}(R_{b12} + R_{3sa})}{R_{3a}R_{3l1}R_{3l2}},$$
$$d_{3,55} = -\frac{(R_{b12} + R_{3sa})^2 + R_{3a}R_{3l2}}{R_{3a}R_{3l2}^2},$$
$$e_{3,11} = \frac{R_{b2}}{R_{3a}R_{3l2}},$$
$$e_{3,12} = \frac{(R_{b12} + R_{3sa})R_{b2}}{R_{3a}R_{3l2}} + \frac{R_{b1}R_{b11}}{R_{3a}R_{3l1}} - \frac{R_{3sb}}{R_{3a}}$$
$$e_{3,21} = \frac{R_{b1}R_{b2}}{R_{3a}R_{3l1}R_{3l2}},$$
$$e_{3,22} = \frac{(R_{b12} + R_{3sa})R_{b1}R_{b2}}{R_{3a}R_{3l1}R_{3l2}} + \frac{R_{b1}^2R_{b11}}{R_{3a}R_{3l1}^2} + \frac{(R_{3a} - R_{3sb})R_{b1}}{R_{3a}R_{3l1}}$$
$$e_{3,31} = \frac{R_{3a}R_{3l2} + R_{b2}^2}{R_{3a}R_{3l2}^2},$$
$$e_{3,32} = \frac{(R_{b12} + R_{3sa})R_{b2}^2}{R_{3a}R_{3l2}^2} + \frac{R_{b1}R_{b2}R_{b11}}{R_{3a}R_{3l1}R_{3l1}} - \frac{(R_{3a} - R_{3sb})R_{b2}}{R_{3a}R_{3l2}}$$
$$e_{3,41} = \frac{R_{b11}R_{b2}}{R_{3a}R_{3l1}R_{3l2}},$$
$$e_{3,42} = \frac{(R_{b12} + R_{3sa})R_{b11}R_{b2}}{R_{3a}R_{3l1}R_{3l2}} + \frac{R_{b11}^2R_{b1}}{R_{3a}R_{3l1}^2} + \frac{(R_{3a} - R_{3sb})R_{b11}}{R_{3a}R_{3l1}}$$
$$e_{3,51} = \frac{R_{3a}R_{3l2} - R_{b2}(R_{b12} + R_{3sa})}{R_{3a}R_{3l2}^2},$$

$$e_{3,52} = \frac{(R_{3a} - R_{3sb})(R_{b12} + R_{3sa})}{R_{3a}R_{3l2}}$$

$$- \frac{(R_{b12} + R_{3sa})^2 R_{b2}}{R_{3a}R_{3l2}^2} - \frac{R_{b1}R_{b11}(R_{b12} + R_{3sa})}{R_{3a}R_{3l1}R_{3l2}}$$

A.4 State 4

State 4 equivalent circuit is shown in Fig. 4.11(d). In state 4, there are such equations:

$$I_{12}(i) - I_{f2}(i) = I_{11}(i) \tag{A.36}$$

$$I_{10}(i) + I_{f1}(i) = I_{10}(i) - I_o \tag{A.37}$$

$$R_{4s2} \cdot I_{f2}(i) + V_{f2}(i) = V_{in} - V_{12}(i) - (R_{12} + R_{4sa}) \cdot I_{12}(i) \tag{A.38}$$

$$R_{4s1} \cdot I_{f1}(i) + V_{f1}(i) = V_{10}(i) + R_{10} \cdot I_{10}(i) \tag{A.39}$$

$$\begin{aligned} &V_{10}(i) + V_{11}(i) + V_{12}(i) + R_{10} \cdot I_{10}(i) + R_{11} \cdot I_{11}(i) \\ &+ R_{12} \cdot I_{12}(i) + R_{4sa} \cdot I_{12}(i) + R_{4sc} \cdot I_{11}(i) + R_{4sb} \cdot (I_{10}(i) + I_o) = V_{in} \end{aligned} \tag{A.40}$$

Where: $R_{4sa} = R_1$, $R_{4sb} = R_5$, $R_{4sc} = R_4$;
$R_{4s1} = 2 \cdot R_{dson} + R_{f1} + R_3$, $R_{4s2} = 2 \cdot R_{dson} + R_{f2} + R_2$.

According to equation A.39 and 4.6, there is

$$I_{f1}(i) = \frac{\Delta V_{3s1}(i) + R_{b10} \cdot I_{10}(i)}{R_{b1}} \tag{A.41}$$

Where: $R_{b1} = R_{4s1} + R_{eqf1}$, $R_{b11} = R_{11} + R_{eq11}$;
$\Delta V_{4s1}(i) = V_{10}(i-1) - V_{f1}(i-1)$.

According to equations A.38 and 4.6, there is

$$I_{f2}(i) = \frac{\Delta V_{4s2}(i) - (R_{b12} + R_{4sa}) \cdot I_{12}(i)}{R_{b2}} \tag{A.42}$$

Where: $R_{b2} = R_{4s2} + R_{eqf2}$, $R_{b12} = R_{12} + R_{eq12}$;
$\Delta V_{4s2}(i) = V_{in} - V_{12}(i-1) - V_{f2}(i-1)$.

Substitute equation A.41 into equation A.37, there isp

$$I_{10}(i) = \frac{R_{b1}}{R_{4l1}} \cdot I_{11}(i) - \frac{R_{b1}}{R_{4l1}} \cdot I_o - \frac{1}{R_{4l1}} \cdot \Delta V_{4s1}(i) \tag{A.43}$$

Where: $R_{4l1} = R_{b1} + R_{b10}$.

Substitute equation A.42 to equation A.36, there is

$$I_{12}(i) = \frac{R_{b2}}{R_{4l2}} \cdot I_{11}(i) + \frac{1}{R_{4l2}} \cdot \Delta V_{4s2}(i) \tag{A.44}$$

Where: $R_{4l2} = R_{b2} + R_{b12} + R_{4sa}$.

Substitute equations 4.6, A.44 and A.43, there is

$$\begin{aligned} I_{11}(i) = {} & \frac{R_{4p1}\Delta V_{4s1}(i)}{R_{4a}R_{4l1}} - \frac{R_{4p3}\Delta V_{4s2}(i)}{R_{4l2}} \\ & + \frac{\Delta V_{4s}(i)}{R_{4a}} + (\frac{R_{b1}R_{4p1}}{R_{4a}R_{4l1}} - \frac{R_{4sb}}{R_{4a}})I_o \end{aligned} \tag{A.45}$$

Where:
$R_{4p1} = R_{b10} + R_{4sb}$,
$R_{4p2} = R_{4sc} + R_{b11}$, $R_{4p3} = R_{b12} + R_{4sa}$;
$\Delta V_{4s}(i) = V_{in} - V_{10}(i-1) - V_{11}(i-1) - V_{12}(i-1)$;
$R_{4a} = \frac{(R_{b10} + R_{4sb})R_{b1}}{R_{4l1}} + R_{b11} + R_{1sc} + \frac{(R_{b12} + R_{4sa})R_{b2}}{R_{4l2}}$.
Substitute equation A.45 to equations 4.6, A.42– A.43, we can get all capacitors' voltages and currents of state 4.

According to above analysis, the parameter in A.1 can be calculated as follows,

$$d_{4,11} = \frac{(R_{4sb} - R_{b1})R_{b1} - R_{4a}R_{4l1}}{R_{4a}R_{4l1}^2},$$
$$d_{4,12} = -\frac{R_{b1}}{R_{4a}R_{4l1}},$$
$$d_{4,13} = -\frac{R_{4l2}R_{b1} + R_{b12}R_{b1} + R_{4sa}R_{b1}}{R_{4a}R_{4l1}R_{4l2}},$$
$$d_{4,14} = -\frac{(R_{4sb} + R_{b10})R_{b1} - R_{4a}R_{4l1}}{R_{4a}R_{4l1}^2},$$
$$d_{4,15} = \frac{R_{b1}R_{b12} + R_{4sa}R_{b1}}{R_{4a}R_{4l1}R_{4l2}},$$
$$d_{4,21} = \frac{R_{4sb} - R_{b1}}{R_{4a}R_{4l1}},$$
$$d_{4,22} = -\frac{1}{R_{4a}},$$
$$d_{4,23} = -\frac{R_{4l2} + R_{b12} + R_{4sa}}{R_{4a}R_{4l2}},$$
$$d_{4,24} = -\frac{R_{b10} + R_{4sb}}{R_{4a}R_{4l1}},$$
$$d_{4,25} = -\frac{R_{b12} + R_{4sa}}{R_{4a}R_{4l2}},$$
$$d_{4,31} = \frac{(R_{4sb} - R_{b1})R_{b2}}{R_{4a}R_{4l1}R_{4l2}},$$
$$d_{4,32} = -\frac{R_{b2}}{R_{4a}R_{4l2}},$$
$$d_{4,33} = -\frac{R_{4l2}R_{b2} + (R_{b12} + R_{4sa})R_{b2} + R_{4a}R_{4l2}}{R_{4a}R_{4l2}^2},$$
$$d_{4,34} = -\frac{R_{b2}R_{b10} + R_{b2}R_{4sb}}{R_{4a}R_{4l1}R_{4l2}},$$
$$d_{4,35} = \frac{(R_{b12} + R_{4sa})R_{b2} - R_{4a}R_{4l2}}{R_{4a}R_{4l2}^2},$$
$$d_{4,41} = \frac{(R_{4sb} - R_{b1})R_{b10} + R_{4a}R_{4l1}}{R_{4a}R_{4l1}^2},$$
$$d_{4,42} = -\frac{R_{b10}}{R_{4a}R_{4l1}},$$
$$d_{4,43} = -\frac{R_{4l2}R_{b10} + R_{b12}R_{b10} + R_{4sa}R_{b10}}{R_{4a}R_{4l1}R_{4l2}},$$
$$d_{4,44} = -\frac{(R_{4sb} + R_{b10})R_{b10} + R_{4a}R_{4l1}}{R_{4a}R_{4l1}^2},$$
$$d_{4,45} = \frac{R_{b10}R_{b12} + R_{4sa}R_{b10}}{R_{4a}R_{4l1}R_{4l2}},$$
$$d_{4,51} = -\frac{(R_{4sb} - R_{b1})(R_{b12} + R_{4sa})}{R_{4a}R_{4l1}R_{4l2}},$$

$$d_{4,52} = \frac{R_{b12} + R_{4sa}}{R_{4a}R_{4l2}},$$
$$d_{4,53} = \frac{(R_{4l2} + R_{b2})(R_{b12} + R_{4sa}) - R_{4a}R_{4l2}}{R_{4a}R_{4l2}^2},$$
$$d_{4,54} = \frac{(R_{b10} + R_{4sb})(R_{b12} + R_{4sa})}{R_{4a}R_{4l1}R_{4l2}},$$
$$d_{4,55} = -\frac{(R_{b12} + R_{4sa})^2 + R_{4a}R_{4l2}}{R_{4a}R_{4l2}^2},$$
$$e_{4,11} = \frac{R_{b1}R_{b2}}{R_{4a}R_{4l1}R_{4l2}},$$
$$e_{4,12} = -\frac{(R_{4sb} - R_{b1})R_{b10}R_{b1} + R_{4a}R_{4l1}R_{b1}}{R_{4a}R_{4l1}^2};$$
$$e_{4,21} = \frac{R_{b2}}{R_{4a}R_{4l2}},$$
$$e_{4,22} = \frac{R_{b1}R_{b10} - R_{4sb}R_{b10}}{R_{4a}R_{4l1}};$$
$$e_{4,31} = \frac{R_{b2}^2 + R_{4a}R_{4l2}}{R_{4a}R_{4l2}^2},$$
$$e_{4,32} = \frac{(R_{b1} - R_{4sb})R_{b2}R_{b10}}{R_{4a}R_{4l1}R_{4l2}};$$
$$e_{4,41} = \frac{R_{b10}R_{b2}}{R_{4a}R_{4l1}R_{4l2}},$$
$$e_{4,42} = -\frac{(R_{4sb} - R_{b1})R_{b10}^2 + R_{4a}R_{4l1}R_{b10}}{R_{4a}R_{4l1}^2};$$
$$e_{4,51} = -\frac{R_{b2}^2(R_{b2} + R_{4sa}) - R_{4a}R_{4l2}R_{b2}}{R_{4a}R_{4l2}^2R_{b2}},$$
$$e_{4,52} = -\frac{R_{b10}(R_{b1} - R_{4sb})(R_{b12} + R_{4sa})}{R_{4a}R_{4l1}R_{4l2}};$$

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