SIMULATION AND CHARACTERIZATION OF SEMICONDUCTOR GaAs COMPATIBLE FERROELECTRIC DEVICES FOR MONOLITHIC INTEGRATION TECHNOLOGY

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CERTIFICATE OF ORIGINALITY

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MAK Kwong Wai (Name of candidate)

ABSTRACT

Semiconductor gallium arsenide (GaAs) is preferred substrate material in the commercial microwave circuit due to its high frequency response of the signal and relatively insensitive to heat during signal transmission. Besides GaAs, ferroelectric titanates are popular functional materials, not only because of their high dielectric constant, but also their tunable properties. The behavior of ferroelectric titanates is modified when applying an electrical field on it. This property makes devices able to process the signal continuously without replacing devices or redirect the signals to other components. To enhance the benefit of using both materials, ferroelectric microwave devices can be integrated onto GaAs wafer to form a monolithic integrated circuit. A typical example is tunable interdigital capacitors (IDCs) capacitor containing the barium strontium titanate (BST) active layer fabricated on a GaAs substrate.

The performances of IDCs are usually described through the traditional analytical model. Such as Gevorgin's model and Igreja's model, which are commonly used for estimating IDCs integrated with monocrystalline silicon or oxide substrate. However the great difference is found between the results of calculation by these conventional models and characterization by experiments.

In this thesis, these traditional models are modified by considering the specific parameters associated with GaAs substrate. Another distinct modification in this work is an inclusion of phenomenological (thermodynamic) models for the displacement type of ferroelectric materials. This approach has created the complete picture of modifying the capacitance

of the IDC through applying additional DC voltages. During the modifying model, the software Ansoft Maxwell 2D (cross section) and HFSS (3D) were used to simulate IDCs by using the finite element method of numerical electromagnetic simulation. They provide evidence for modifying the conventional models. With the modified model, the behavior of IDC with BST was simulated in this work. The mathematical simulation was performed by using MATLAB. In addition, the graphical user interface was also created to provide convenient input of IDC parameters.

The IDCs with $Ba_{0.7}Sr_{0.3}TiO_3$-STO-GaAs Heterostructure is employed for the simulation and fabricated using laser molecular beam epitaxy. The thickness of the BST layer in these IDCs is 250-nm and 400-nm. The 1 GHz frequency and the bias voltage are applied directly to the IDCs. They are investigated experimentally by using Agilent/HP 4291B RF impedance/material analyzer, with an ACP40-GS-100 probe mounted on the Cascade probe station. The capacitance and tunability of these IDCs are also provided by the simulation using the modified model in this work. With reasonable material parameters setting, the tunability is calculated as 26.98% and 28.68%, for the 250-nm BST at 3V DC biasing and for the 400-nm BST at 4V DC biasing respectively. In contrast, Gevorgin's model, one of the traditional models, in ideal cases gives tunability 56.33% and 64.25%, which is greatly different compared to experimental results which are 25.4% and 28.5%.

PUBLICATIONS

Journal Paper

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TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Chapter 1 Introduction

1.1 Phenomena of ferroelectric materials

The characteristic property of ferroelectric materials is the spontaneous polarization exhibiting inside the materials without any initializing process. The polarization is the stable net dipole moment in lattices. The original of dipole moment is non-zero distance of the centers of positive and negative charges in lattices. The asymmetry of lattice structures ensures fulfilling this condition. All lattice structures categorizes into 32 kinds of crystallographic point groups, while 21 kinds of point groups have non-centrosymmetric structures [1]. The dipole moment of materials in 20-kind non-centrosymmetric structures responses to the application of an external stress. These materials are piezoelectric materials. 10 kinds of piezoelectric materials are pyroelectric because temperature changes their properties. Some pyroelectric materials exhibit a finite permanent value of polarization in the absence of an applied electric field or stress, then they are ferroelectric.

Among ferroelectric materials, there is one type called perovskite oxides. [2] The simple form of this ferroelectric is based on the formula of ABO_3, where both A and B are metallic elements with oxidation states +2 and +4. Common perovskite oxides include $BaTiO_3$(BTO), $SrTiO_3$(STO) and $PbTiO_3$ etc. This kind of lattice structure is presented in Figure 1-1. The most important feature of perovskite oxide is that it possesses an oxygen-vertices octahedron in the unit cell. Once the center of this oxygen octahedron overlaps the center of cations, there is no permanent spontaneous dipole moment. It just exhibits paraelectricity with induced dipole moment by applying external electric fields. However,

once the lattice structure is deformed, spontaneous dipole is created obviously, and it turns into a ferroelectric state. This deformation can be accomplished by changing the temperature, applying stress or poling with electric field.

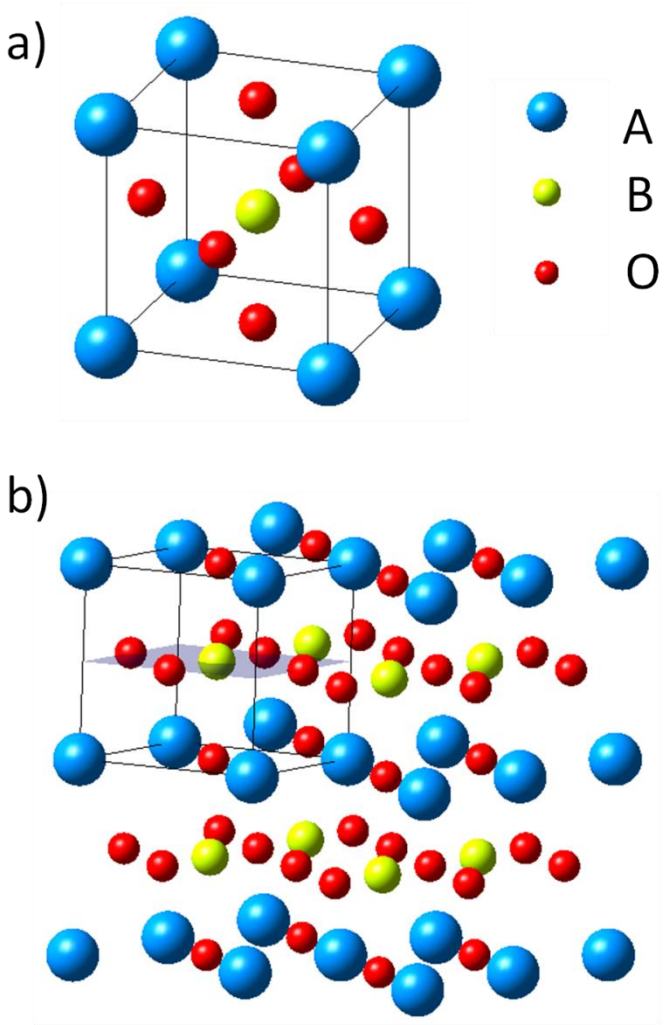
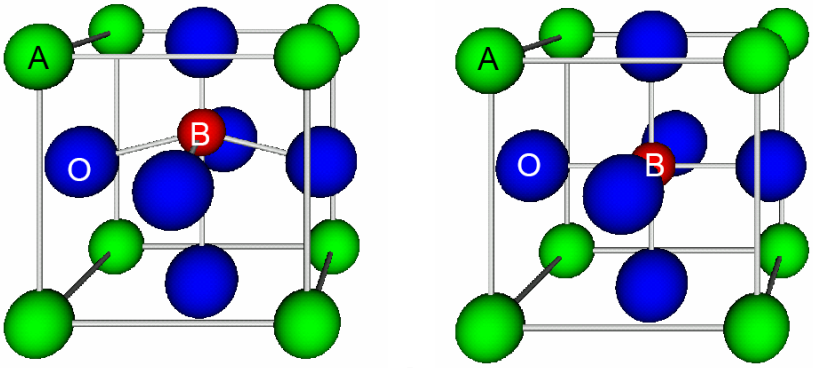


Figure 1-1 Schematic diagram of the perovskite oxide ABO_3 structure.
(a) One cubic unit cell of perovskite oxide consist of 8 x 1/8 A ions at the corners, a B ion at the center of the cube, and 4 x 1/2 O ions at the center of every face;
(b) ABO_3 structure can also be described as a stacking of AO and BO_2 atomic planes.



(a) (b)

Figure 1-2 Schematic diagram of the perovskite oxide ABO_3 cubic structure in (a) ferroelectric state and (b) paraelectric state.

Among these approaches of deformation lattice, changing temperature is the distinct method. The temperature of transition between ferroelectric-paraelectric phases is so-called Curie temperature T_C. Below the Curie temperature, there is a displacement of central metal cations with respect to oxygen anions to minimize the energy of the system even in the cubic structure [3]. Figure 1-2 (a) shows this displacement in a perovskite ABO_3 lattice. Thus, the offset between the electrical center of cations and anions causes the net dipole moment. Hence, the perovskite material is a kind of displacement type ferroelectric. Since this Columbic interactions between dipoles of lattices are available in the long range, the ferroelectricity is present in macroscopic scale [4]. But once the temperature increases, this asymmetric structure disappears and transforms back to symmetric cubic structure as shown in Figure 1-2 (b). This important behavior is able to be modified with minor changes in composition or structure, which has ever attracted much attention in theoretical research.

1.2 General properties of barium strontium titanate

Barium strontium titanate $Ba_xSr_{1-x}TiO_3$ (BST or BSTO in short) is a typical perovskite oxides. The variable x is in the entire range from 0 to 1. BST, in considering its electrical properties, is often treated as a solid solution of barium titanate (BTO) and strontium titanate (STO). [5, 6] The main reason of inter-solubility is the same titanate-related perovskite structure. Ba^{2+} and Sr^{2+} occupy the same A-site in the ABO_3 structure [7]. Also the rigidity of the oxygen octahedral network causes the lattice constant of these perovskites is approximately to maintain 4 Å. [8] Thus the properties of BST could be roughly considered as the linear combination of BTO and STO as a function of barium to strontium ratio which obeys the level rule of the solution. Ghosez *et al.* [9] proves the lattice stabilities by using first-principles calculation.

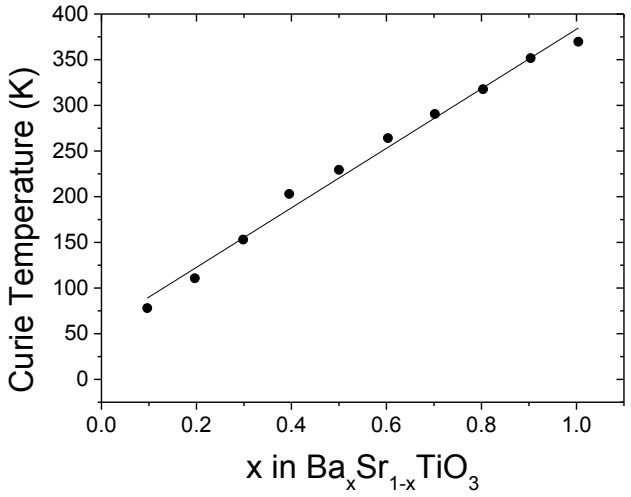


Figure 1-3 The Curie temperature as a function of barium-strontium ratio in bulk BST [7]

The typical property in BST which obeys such behavior is Curie temperature. The temperature increases from about 50 K of pure STO to 400 K of pure BTO as shown in Figure 1-3. The most attractive point is one for $Ba_{0.7}Sr_{0.3}TiO_3$. The ferroelectric transition takes place near room temperature. It makes that the device containing $Ba_{0.7}Sr_{0.3}TiO_3$ could be operated in its paraelectric state at room temperature.

1.3 Characteristic properties of BST in thin film form

However, the behaviors of BST thin films are much complicated compared with that in bulk BST. Composition, substrate, defects can influence the properties of BST thin films more obviously than ones of bulk BST. In addition, when the thickness of BST thin film reached to a specific value, the thickness itself becomes one of the factors. And external biasing fields behaves more important role in altering the properties.

The composition of BST is a dominant factor determining the properties of thin films as the same way of bulk materials, such as the Curie temperature of BST. The higher the barium concentration, the Curie temperature is higher. But the temperature change in BST thin films by changing the Ba-Sr ratio is quantitatively inconsistent with bulk ceramics as shown in Figure 1-4.

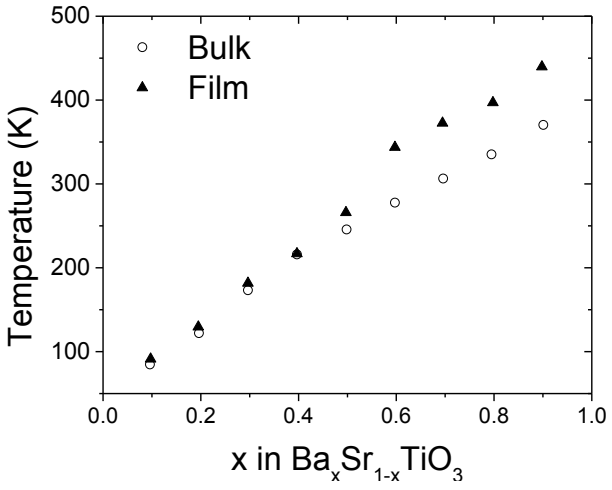


Figure 1-4 The peak of Curie temperature with respect to Ba-Sr ratio in bulk and film forms of BST. [7, 10]

Another noticeable difference is the lattice constants between thin films and bulk ceramics as shown in Figure 1-5. Then the substrate supporting the BST thin films has significant influence on lattice structure and properties of BST thin films. Since the BST thin films have grown on the surface of the substrate, the crystal structure and surface morphology of the substrate influence the microstructure of BST thin film because the different parameters of lattice constancies. The strain caused by it makes the internal stress build at the interface. Moreover, the electrical properties are clamped by the substrate and thus cannot respond freely to external stimulations.

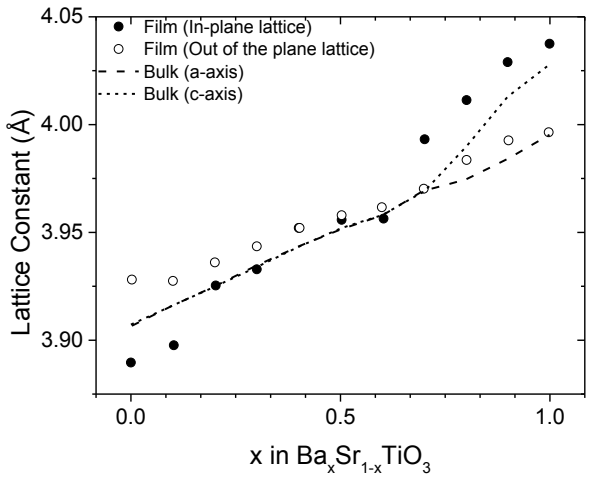


Figure 1-5 The lattice constant change with respect to Ba-Sr ratio in bulk and film forms of BST. [7, 10]

Thirdly, there are unavoidable defects occurring in BST thin films, making significant influences on the properties of BST thin films. In most cases, BST thin films are grown in an oxygen-deficient environment to avoid oxidizing the substrate. Consequently, the as-deposited BST thin films usually contain a large number of oxygen vacancies. Post-

annealing of samples in air or oxygen can reduce the concentration but cannot fully remove the oxygen vacancies. Other defects, such as dislocations and grain boundaries have also important influences on thin film properties. These changes in thin films clearly depend on the thickness of BST.

The field dependence of the dielectric constant in ferroelectrics was discovered in the 1950's. The dependence of BST thin films can be shown in a nonlinear dielectric response under DC voltage biasing. This response is characterized by measuring dielectric response by applying a small amplitude AC signal with DC bias voltage as the result shown in Figure 1-6. [11]

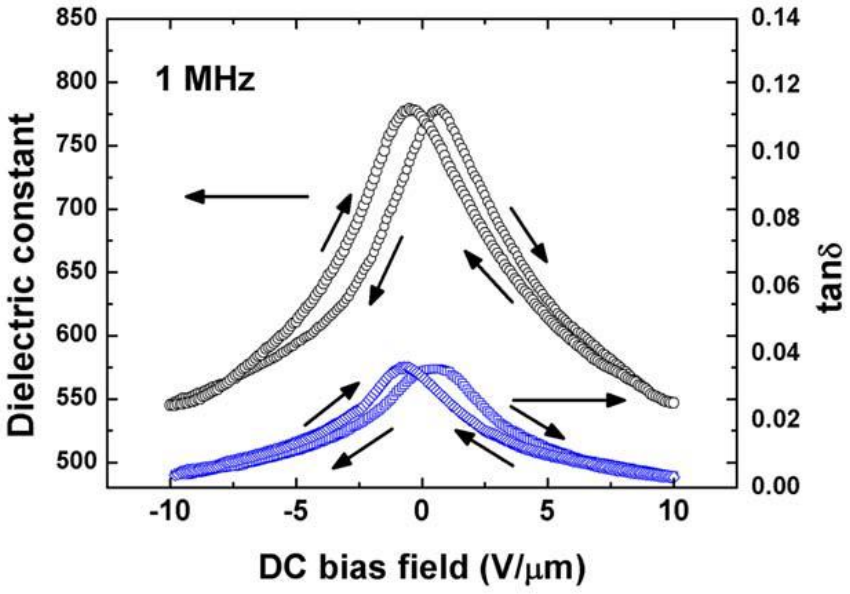


Figure 1-6 The typical non-linear dielectric response of BST under DC voltage biasing with 1 MHz AC signal.

1.4 Application of BST thin films

The application with BST in device tends to fabricating it into thin film forms. The motivation to investigate BST thin films is to minimize the size and operational power consumption of the microelectronic components and devices. Most devices employ high dielectric constant of BST, such as infrared sensors and thermal imagers, dynamic random access memory.

However, because the nonlinear dielectric behavior of ferroelectric materials have been investigated since the 1960's, there has been more effort to develop devices, including tunable components using different aspects of ferroelectric properties. [12-14] The typical devices are tunable microwave devices, although most ferroelectric materials are fabricated in bulk form at that time. [15]

For the usage in tunable microwave devices, the active material is required to exhibit a tunable dielectric constant and small loss tangent. In general, the active material is ferroelectric. These materials are used as dielectric layers in capacitors for microwave circuits. [16] The capacitance is proportional to the dielectric constant of the dielectric material; therefore it can be conveniently changed by changing the voltage applied to the capacitor. When varying the capacitance, the impedance and phase of the circuit involving the capacitor are changeable.

In this case, BST is a good candidate for such applications mainly because of the following two reasons.

First, major dielectric properties of BST can be easily modified by adjusting the Ba-Sr ratio. Second, BST is relatively "soft", especially when it works around the Curie temperature. The mechanism for the dielectric behaviors has been investigated. The presence of the soft mode is not only the underlying mechanism for the ferroelectric phase transition itself, but also the cause of the large non-linear dielectric response of BST. [2, 17] As the mode softens, it becomes easier for a small electric field to separate the Ti and O sublattices, leading to a divergence of the small signal dielectric constant.

Furthermore, applying a larger DC electric field changes the dynamics of the soft mode or stiffens its frequency, and thereby decreases the dielectric constant by changing the shape of the potential well in which the soft mode vibrates. In general, the effects of the applied field are to decrease the overall dielectric constant and to cause the temperature of maximum dielectric constant to slightly increase. This physical picture is helpful for understanding the tunable dielectric behavior in BST. Nevertheless, the use of BST ceramic bulks in tunable components is rather limited mainly because the very large DC voltage should be required in order to obtain certain electric field and drive the ceramics to exhibit a good tunability.

Thus, for the applications in tunable devices, BST thin films are more attractive than bulk materials due to its relatively lower operation voltage, smaller size and higher level of integration. [18-20]. Firstly the tunable devices are investigated with superconductor electrodes. [21-23] Then in the last a few decades, there has been extensive research on the development of BST thin film-based microwave devices with general metals [24],

including varactors [25], phase shifters, voltage control oscillators, tunable filters [26-28], reconfigurable antennas, and RF MEMS switches [20, 29]. Among these devices, microwave phase shifter is typical and widely studied, and the major components in a microwave phase shifter are tunable capacitors.

1.5 BST thin film devices integrating into the gallium arsenide substrate

In previous decades, the BST thin films are studied on an oxide substrate such as Al_2O_3 [30, 31], MgO [12, 32], $LaAlO_3$ [10], SiO_2 [33], or an oxide buffered substrate like TiO_2. And also Zhang *et al.* [34] provided the comparison of the microwave performance of BST thin films fabricated on these substrates to provide the choice of substrates used in microwave devices. However, due to the high cost and the size limit of these oxide substrates, it is still of great interest to integrate BST onto gallium arsenide (GaAs) wafer. Because GaAs wafer is more affordable and large-size available, and has been widely used in the commercial microwave circuit. Compared to oxide substrates, GaAs has a higher saturated electron velocity and higher electron mobility, allowing the device function at microwave frequencies. It also makes devices relatively insensitive to heat and robust under external signal noise, owing to the wide bandgap of GaAs.

Unfortunately, the work of integration of BST device on GaAs is limited because the formation of the heterostructure of BST thin film with GaAs has proven to be a challenging task, although Losego *et al.* [35] reports a successful case of fabricating BST on even complex crystals like GaN, also Reshmi *et al.* [36] reports a case of fabricating BST on perovskite oxide substrate. The major issue is caused by the great difference of the lattice structure and parameters between perovskite type ferroelectric and GaAs. Another problem is instable of GaAs surface. It was partially resolved by introducing MgO buffered layer, but the Breton [37] reported that the effect of $BaTiO_3$-MgO interface strongly depends on the thickness of BTO. In addition, the high charge injection form MgO to GaAs would occur under reverse bias voltage. It also makes the ferroelectric

oxides to exhibit weaker properties, which are reported by Murphy. [38] Until Hao *et al.* effect [39] have studied on the interface properties of STO-Si and Huang *et al.* [40] have measured interface properties of ZnO-STO-GaAs heterostructure. STO nano-scale thin film was used as the buffer layer between the BST layer and GaAs substrate to reduce the leakage current.

Therefore, the formation of ferroelectric material grown on GaAs would be done with a suitable buffer layer. By combining the electrodes or other microwave elements with the ferroelectric thin films, the basic tunable device is formed. The tunability could be easily controlled by additional DC biasing. In this case, the ferroelectric material would exhibit the in-plane properties instead of the out-of-plane one. The in-plane properties are seldom discussed. These properties are reported by Simon *et al.* [41] and Yang *et al.* [42] . Also, there is a lack of the analytical model for the specific heterostructure device based on GaAs wafer, although there are some existing analytical models for multilayer structure for oxide wafer mentioned in the above section. Thus in this work, an analytical model of tunable interdigital capacitors (IDCs) with a BST active layer integrated onto the GaAs wafer is established to simulate the device performances and make the estimation of the influence of BST-GaAs heterostructures.

1.6 Significance of modeling for BST-GaAs-based devices

The performance of devices, including general ferroelectric devices, can be simulated by computer software. The software analyzes the complex structures using different method. For example, ANSYS's high frequency structure simulator (HFSS) uses 3D finite element method, Sonnet software uses fast Fourier transform-based analysis, and Agilent's Momentum uses method of moments.

A critical issue of computer simulation is time-consuming. The first step of the simulation is to slice the structure of devices into pieces. Then various methods are applied to each piece. The number of pieces determines the major part of computational time. The smaller the pieces are sliced, obviously more time and computational power is required, and accuracy is higher. However, the increment of accuracy by increasing piece number is limited while the piece size reduced to a certain value. In the case of devices involving extremely thin ferroelectric films (*e.g.*, down to 0.1 micrometer) and commercially available substrates (*e.g.*, several hundred micrometers), to get 5% accuracy using HFSS, several hours are required for nowadays workstations.

Besides simulation, analyzing the structure of devices has another approach. The aim of this approach is to create a suitable model to describe performance information using the basic parameters of devices, mainly material and dimensions. Models created are often presented in the closed form expressions. The accuracy is determined by the model itself.

But the analytical approach for BST-GaAs-based devices has another issue compared to general devices, the material properties of BST thin film on GaAs are not independent factors. Most current analytical models for general devices are just to cooperate with independent material properties. This defect of analytical models remains till nowadays.

1.7 Key results of modeling for tunable devices

The basic parameter characterizing ferroelectrics for applications in tunable devices is tunability. [43] The tunability of a particular material means how much the dielectric constant changes. It is conventionally defined as the following equation:

$$n = \frac{\Delta\varepsilon}{\varepsilon} = \frac{\varepsilon_{max} - \varepsilon_{min}}{\varepsilon_{max}} \tag{1.1}$$

Since the dielectric constant is a function of external field E, Eq. (1.1) can be rewritten into:

$$n(E) = \frac{\Delta\varepsilon}{\varepsilon} = \frac{\varepsilon(0) - \varepsilon(E)}{\varepsilon(0)} \tag{1.2}$$

As the core component of tunable device is ferroelectrics capacitors, Eq. (1.2) can be further transformed into:

$$n(E) = \frac{\mathrm{C}(0) - \mathrm{C}(E)}{\mathrm{C}(0)} \tag{1.3}$$

Another parameter to describe properties of ferroelectric materials is loss tangent. The intrinsic loss tangent serves to dissipate or absorb the microwave energy, and therefore is desired to be lower. It correlated with complex permittivity and operation frequency, while the dielectric constant ε is the real part of complex permittivity ε' and the conductivity σ is related to the imaginary part of complex permittivity ε''. The loss tangent of ferroelectrics is:

$$\tan\delta = \frac{\varepsilon''}{\varepsilon'} = \frac{\sigma}{\omega\varepsilon} \tag{1.4}$$

The loss tangent of device, considering the conductance of device G:

$$\tan\delta(E) = \frac{\omega C(E)}{G(E)} \tag{1.5}$$

Thus the figure of merit of device:

$$FoM(E) = \frac{(n(E)-1)^2}{n(E)\tan\delta(0)\tan\delta(E)} \tag{1.6}$$

To achieve optimum electronic properties, the tunability for practical devices should range from at least 10%, depending upon the dielectric constant and the loss tangent. Precise control of composition and microstructure for the production of BST thin films is challenging critical task to get the precise value of capacitance and loss tangent. Fortunately, since the usage of tunable device is to change value relatively, also BST has a high dielectric constant, the exact value of capacitance is less important. In high frequency application, the change of loss tangent due to external field is small. Thus the main results of modeling for tunable devices is to find the tunability of the devices rather than exact values of capacitance.

1.8 Scope of the present study

As discussed above, BST has been extensively investigated, but there are still a number of questions that remain unanswered, especially the properties under the influence of GaAs substrates. Also the lack of analytical model fits tunable devices fabricated on GaAs wafers. Thus, the primary objective of this dissertation is to study the influence of interface between BST thin film and GaAs substrate and, the ferroelectric behaviors and dielectric properties of BST films operating in microwave frequency; derived the model suitable for BST-GaAs heterostructures; make BST-GaAs based prototype microwave devices. The multi-layered interdigital capacitors (IDCs) containing BST-GaAs is used as the typical tunable devices for discussion.

Followed by the introduction given in this Chapter, the thesis involves several chapters as below:

Chapter 2 is to estimate the current analytical models mainly used for estimating the capacitance of IDCs with oxide substrates, such as Gevorgin's model and Igreja's model. The investigation of these device-oriented models provides the implicit conditions and methods for modeling BST-GaAs-based IDCs. These implicit conditions have changed in BST-GaAs devices.

Chapter 3 is to derive a model suitable for BST-GaAs heterostructures, combing both device model of IDCs and theoretical material model of BST, based on the investigation in Chapter 2. First part of this chapter will give a semi-quantitative explanation for the

tunable properties of BST. Subsequently, device-independent finite element simulation using computer software to verify whether BST-GaAs fulfills implicit conditions. Finally, the modified model will be given.

Chapter 4 gives the detailed simulation on tunable BST-GaAs capacitors using the modified model derived in Chapter 3.

Chapter 5 describes the experimental work on microwave characterization of tunable BST-GaAs capacitors.

Conclusions and suggestion for future work are given in Chapter 6.

Chapter 2 Estimating current models for multi-layered IDCs

2.1 Current analytical models of multi-layered IDCs

Till nowadays, Gevorgian's analytical model [19] has widely been used for estimating the capacitances of interdigital capacitors (IDCs) and also measuring dielectric properties of ferroelectric films deposited on metal oxide substrates. Although Gevorgian's model is dominant in these studies, some analytical models have been proposed, such as Wei's model [44], Igreja's model [29, 45], Dib [46] and Vendik [47, 48]. Besides for IDC specific model, Starkov *et al.* [49] introduced a theoretical model using Weiss mean field theory to study the dependence of the properties of a ferroelectric film on its thickness in multiple layer substrates. However, the condition of applying these models was often ignored inadvertently, thus the results between charactering and applying ferroelectric materials were fluctuating in certain aspects. In this section, Gevorgian's and Igreja's models will be discussed as the starting point of developing the analytical model which could suitable for estimating the performance of BST-based microwave IDCs fabricated on GaAs substrates.

2.2 IDE structure

The IDE structure is the starting point of analyzing IDCs. It is because the effective capacitance of IDCs is formed between in-plane electrode fingers of IDEs when the external voltage is applied across IDEs.

The basic structure of IDEs is a comb-like as shown in Figure 2-1. To describe the structure, geometrical parameters are used. These parameters include finger number N, finger width W, overlapping finger length L and the separation between each finger G. Also, additional parameters are used in some models, such as electrode thickness T, terminal width W_T and gaps at the end of the fingers G_{end}. The effect of these physical parameters is reported in Zhang's work [50].

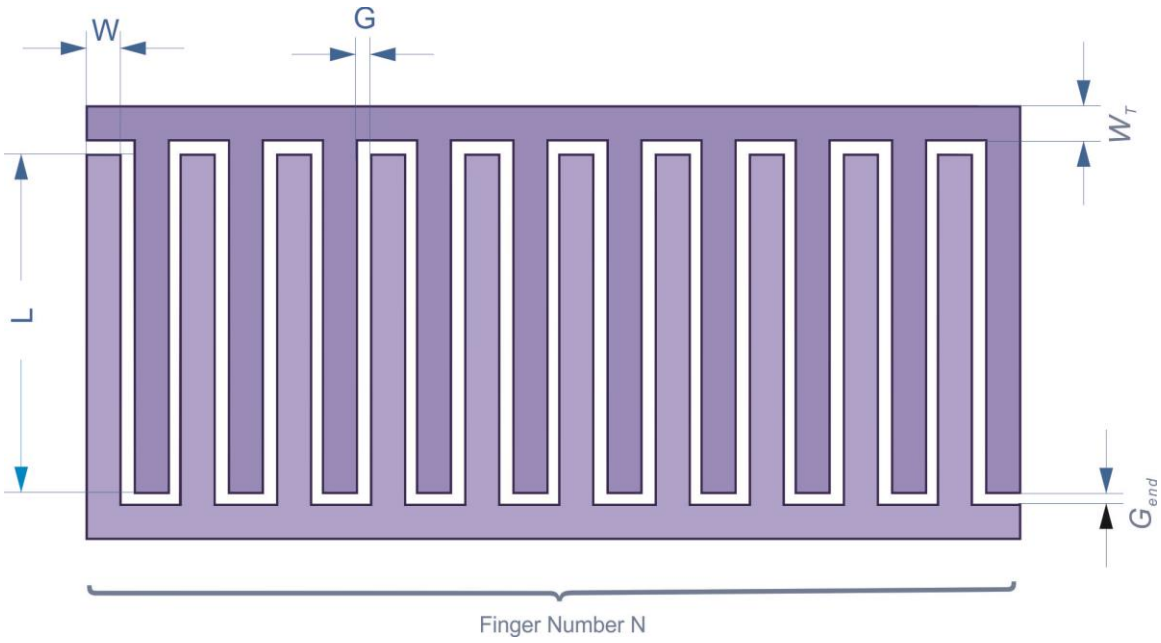


Figure 2-1 The scheme of interdigital electrodes

2.2.1 IDE properties

If geometrical parameters reach the same scale of IDE thickness, the thickness effect should be accounted by using Wheeler's first order approximation [51]. The effective finger width W is:

$$W = W_{phy} + \left(\frac{T}{\pi}\right)\left[1 + \ln\left(\frac{4\pi W}{T}\right)\right] \tag{2.1}$$

Where

W_{phy} is the physical (geometric) width of electrode fingers.

This case is common in IC technology, as parameters are in submicron scale. For example, electrode thickness is 0.1 μm and the separation is between 2 to 5 μm, the difference of physical and separation is about 5% to 10% due to this thickness effect. Thus it should be considered in analytic models when using the geometrical parameters of IDEs.

Furthermore, when the electronic signal passes through IDCs, Rautio [52] suggests that for film thickness less than three times its skin depth, the equivalent line resistances due to the losses in metal strips may be approximated by:

$$r = \frac{1}{W\sigma_m\delta_s(1 - e^{-\frac{T}{\delta_s}})} \tag{2.2}$$

Where

σ_m (S/m) is conductivity of the electrode metal,

δ_s is skin depth of metal.

$$\delta s = \frac{1}{\sqrt{\pi \mu_o \sigma_m f}} \tag{2.3}$$

where

μ_o is the magnetic constant of vacuum,

and f is the operation frequency.

2.2.2 Conformal mapping

The difficulty of analyzing the structure of IDCs is that the electric field in the IDE is not straightly distributed between electrodes fingers like parallel capacitors.

Fortunately in common cases, there is no additional free charge in IDEs, the electrical potential outside the IDE satisfies Laplace's equation:

$$\nabla^2\varphi = -\frac{\rho_f}{\varepsilon} = 0 \tag{2.4}$$

where

φ is electrical potential,

ρ_f is free charge density

A mathematical approach called conformal mapping (CM) becomes powerful tool to analyze the electrical potential distribution of whole IDCs.

The conformal mapping transforms a well-chosen region of the IDCs, bounded by equipotential and continuous flux lines, into an equivalence of a parallel plate capacitor with the same electrical potential in a new coordinate system. To describe the conformal mapping independently in different models in the following sections, the analysis is simplified in the case that voltage U is applied to a pair of two adjacent fingers in IDEs with length L on a single layer substrate with thickness h. Figure 2-2(a) shows the cross-section; and (b) shows the final result of the transformation after applying CM technique.

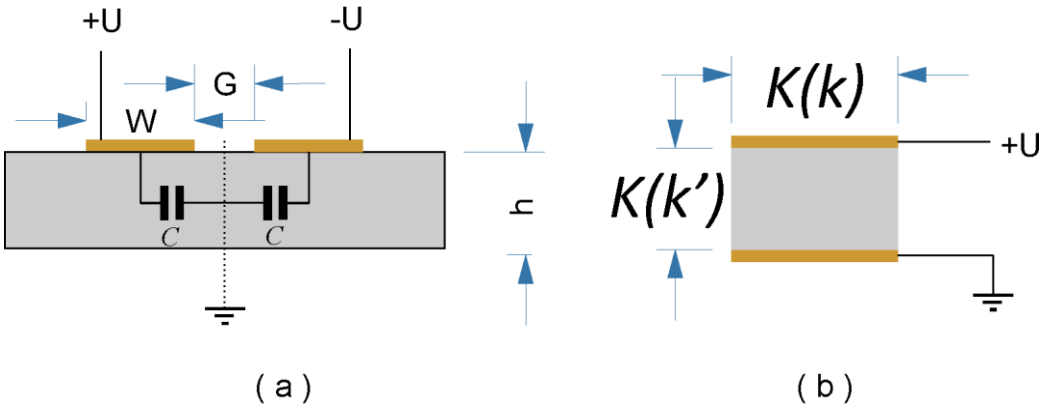


Figure 2-2 (a) Scheme for a pair of two adjacent fingers in IDEs, (b) The result of final transformation

Because of the symmetry of the electric field in the layer generated by the applied voltage, the middle plane can be treated as a magnetic wall, *i.e.* virtual ground. Thus the half side is an analog to a parallel plate capacitor after the final step which is the Schwarz-Christoffel transformation. The ratio of "parallel plate width" to "thickness" would be the ratio of the complete elliptic integral of first kind, with different modulus k and complementary modulus k'. The modulus k would be the function of W, G and interface position h relative to the electrode plane.

$$C(h) = \varepsilon_0 \varepsilon_{eff} L \frac{K(k)}{K(k')} \tag{2.5}$$

In this expression, ε_{eff} is effective permittivity of the layer. $k' = \sqrt{1-k^2}$ and $K(k)$ is the elliptic integrals of the first kind for the modulus k. The models use different CM steps, so there are different moduli k in the Eq. (2.5).

2.3 Multi-layered structure

The analysis of IDEs may lead to forming models for IDCs with a single substrate. However, it is still not able to analyze IDCs with multiple substrates or with materials covering IDEs. The common structure of these IDCs is a multi-layered structure. All substrates or materials covering IDEs are treated as layers.

A multi-layered structure of IDCs can be divided into two half-planes by IDEs, since the total effective properties can be equivalent to a single device formed by two half-plane devices connected in parallel.

The case will be discussed in this section similar to previous analysis of IDEs for simplifying discussion, but the IDCs with multiple substrates are used here. Figure 2-3 shows a cross-section of two adjacent fingers of IDEs in a three-layered structure IDC. The parameters of layers in analytic models include the interface position h, and the permittivity ε.

Figure 2-3 The cross-section of two adjacent fingers in IDEs with three-layered structure

In capacitance calculation, the final capacitance is the sum of contributions from both half-planes. The half-plane capacitance is the superposition of each layer in the half-plane.

It reflects the fact that an electric field of positive electrodes of IDEs passes through each layer to reach the negative ones. However, the boundary of each layer causes different methods when one superposing the effect of each layer, due to their permittivity difference. Then, according the method of superposition, various techniques are used and will be discussed.

2.3.1 Parallel partial capacitance technique

In general use of ferroelectric material on a commercially available substrate, the permittivity monotonic decreases from the inner layer to outer layer away from the electrode plane. Since the permittivity of the inner layer is higher, the electric field is more concentrated in inner layer, but not all the electric field passes through the inner layer. The effective permittivity of inner layer would be smaller than the value of its native property. The effective value is the result of the native property value subtracts the value of the outer adjacent layer. Therefore, this technique is called parallel partial capacitance (PPC) technique as shown in Figure 2-4.

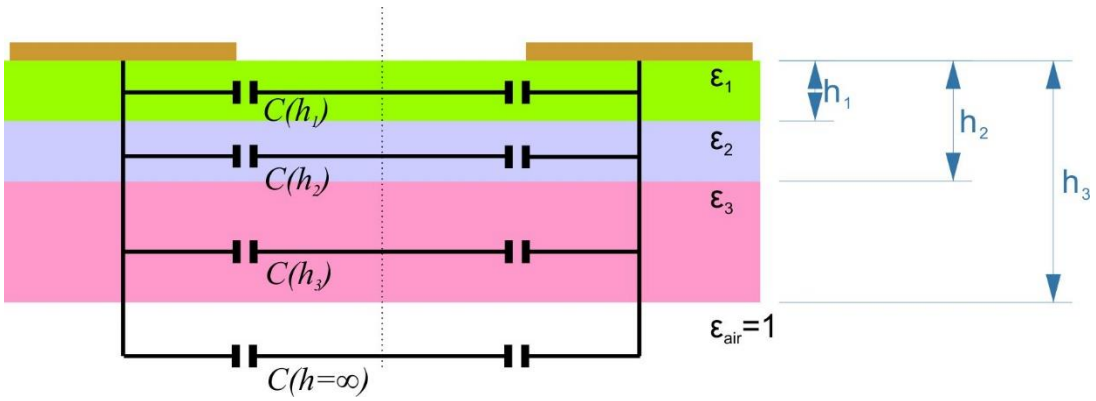


Figure 2-4 The scheme of parallel partial capacitance for three layer IDCs

This technique was first proposed by Kochanov [53] for the study of transmission lines on dielectric exposing in the air. The contribution of capacitances due to the dielectric is assumed that it has a relative permittivity $\varepsilon_r - 1$. It indicates that the interface between the dielectric layer and the air layer between dielectric and air satisfies a Neumann boundary (NB) condition. The NB condition for electric field is $\frac{\partial \varphi}{\partial \hat{n}} = \vec{\nabla}\varphi \cdot \hat{n} = 0$, where φ is the electric potential and $\hat{n}$ is a normal vector to the boundary. It was also applied by Veyres *et al.* [54] to express the capacitance of coplanar waveguides as a weighted sum of the capacitances of several layers. Then, Gevorgian *et al.* and Igreja and Dias both use this technique to obtain models for multi-layered structure IDCs.

2.3.2 Series partial capacitance technique

There are a few cases that the permittivity monotonic increases from the inner layer to outer layer away from the electrode plane. Kitsara *at el.* [55] reported that case happened in a sensor of IDC with SiO_2-Si structure. Since the permittivity of the outer layer is higher, the electric field is more concentrated in the outer layer, and penetrates though the interface between inner and outer layers. In this case, the electric field near the interface between two adjacent dielectric layers tends to be normal to the interfaces. Instead of NB condition, it is considered as a Dirichlet boundary (DB) condition. The DB condition for electric field is that the electric potential is a constant value along the boundary.

Ghione *et al.* [56] proposed series partial capacitance (SPC) technique for co-planar waveguide while Igreja and Dias [45] applied it to modeling the IDCs in this case. Compare to PPC technique, the effective permittivity of the inner layer is the reciprocal result of the reciprocal native property value subtracts the reciprocal value of the outer adjacent layer. Also, the capacitance of the half-plane is reciprocal of the sum of the reciprocal capacitance of each layer, and utmost outer layer is calculated consistently as other inner layers.

2.3.3 Image strips technique

Besides SPC technique, there is a different method to resolve the DB problem. Gevorgian [57] proposed "image strips" method. The electric field penetrates though the interface, it forms a virtual parallel capacitor between the IDE and its projected "image strip" on interface as shown in Figure 2-5. This virtual parallel capacitor contains material with relative permittivity $\varepsilon_r - 1$, *i.e.* the difference between the permittivity of the layer and air. Moreover, the effective layer thickness, $h_{ef} = h\left(1 - \frac{\varepsilon_{inner}}{\varepsilon_{outer}}\right)$ is used to reduce the errors associated with the imperfect electric wall approximation at the interface. These virtual parallel capacitors of all layers excluding furthest layer, are connected in series. The capacitance of furthest layer is calculated as same as PPC.

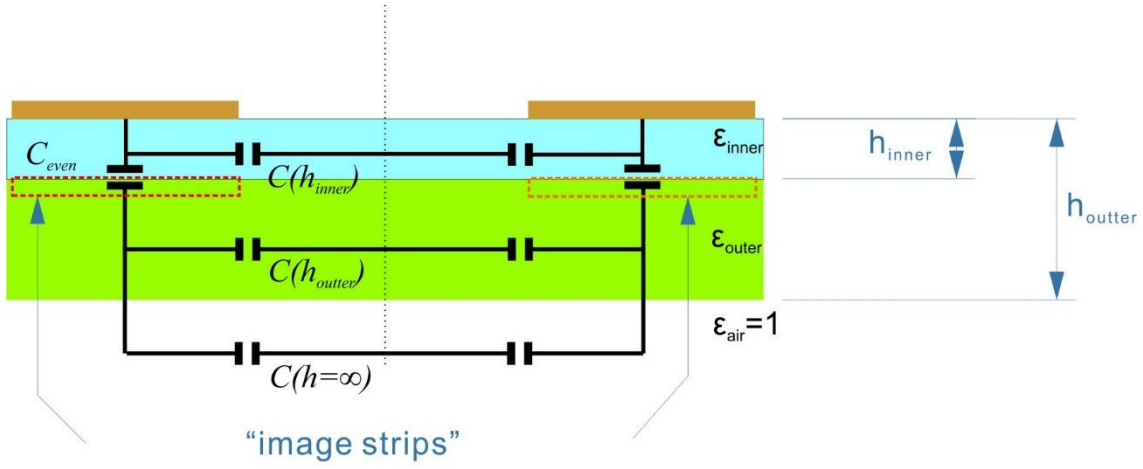


Figure 2-5 The scheme of "image strips" used in Gevorgian's model

2.4 Current Models of IDCs

With analysis of both IDE and multi-layer structure discussed above, three major models for multi-layer IDCs will be briefly presented here.

2.4.1 Wu's model

The first model taking into account a finite layer in multi-layered structure was proposed by Wu *et al.* [23] in 1994. It is a typical model combining CM and PPC technique. The model simply considers the "periodical section" formed by two adjacent fingers shown in Figure 2-6.

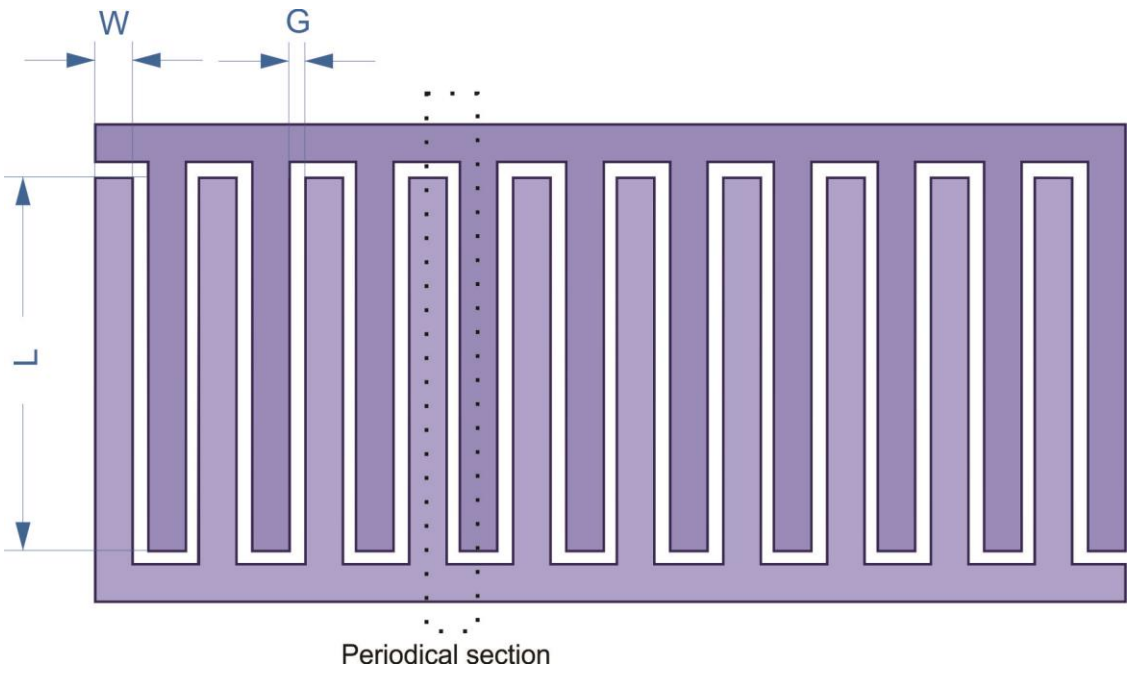


Figure 2-6 Scheme of different sections used in Wu's model

The total capacitance of IDCs:

$$C = (N-1)C_{periodical} \tag{2.6}$$

where $C_{periodical}$ is the capacitance of periodical section.

This capacitance of one half-plane is:

$$C_{periodical} = \sum_{i}^{n} \varepsilon_0(\varepsilon_i - 1)L\frac{K(k_i)}{K(k'_i)} \tag{2.7}$$

where k_i and ε_i is the CM modulus and permittivity for each substrate respectively with further interface position h.

For another half-plane which is often air layer with infinite height, the capacitance of periodical section becomes:

$$C_{periodical} = \varepsilon_0\varepsilon_{air}L\frac{K(k_0)}{K(k'_0)} \tag{2.8}$$

where k_0 the modulus of CM for air.

The CM transformation includes two steps. The first step is to transform the half side of two adjacent fingers in z-plane into t-plane with:

$$t = \sinh\left(\frac{\pi z}{2h_i}\right) \tag{2.9}$$

And then to transform t -plane to w -plane following the Schwarz-Christoffel transformation.

Thus the modulus k_i:

k_i

$$= \frac{\sinh\left(\pi\frac{W}{2}\right)}{\sinh\left(\frac{\pi\left(\frac{W}{2}+G\right)}{2h_i}\right)}\sqrt{\frac{\sinh^2\left(\frac{\pi\left(\frac{W}{2}+G+W\right)}{2h_i}\right)-\sinh^2\left(\frac{\pi\left(\frac{W}{2}+G\right)}{2h_i}\right)}{\sinh^2\left(\frac{\pi\left(\frac{W}{2}+G+W\right)}{2h_i}\right)-\sinh^2\left(\pi\frac{W}{2}\right)}} \quad (2.10)$$

For infinite layer, $h \to \infty$, Eq. (2.10) becomes:

$$k_0 = \frac{W}{W+2G}\sqrt{\frac{2W}{2W+G}} \quad (2.11)$$

2.4.2 Gevorgian's model

After Wu's model, Gevorgian *et al.* [19] suggested another model. In his model, the IDE is divided into three parts: "periodical section", "three finger section" and "finger terminals".

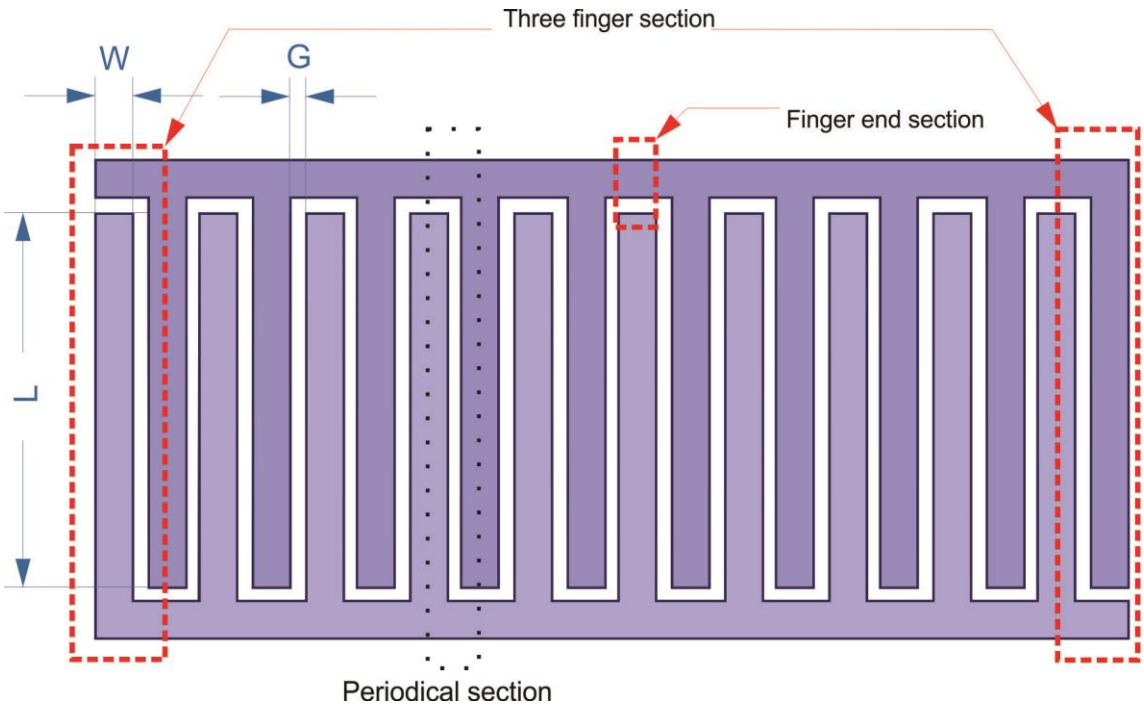


Figure 2-7 Scheme of different sections used in Gevorgian's model

Then total capacitance of one half-plane is the summation of all parts:

$$C = (N-3)C_{periodical} + C_{threefinger} + C_{terminals} \qquad (2.12)$$

These capacitances of one half-plane are:

$$C_{periodical} = \varepsilon_0 L\left(\frac{K(k_0)}{K(k'_0)} + (\varepsilon_n - 1)\frac{K(k_n)}{K(k'_n)} + \sum_{i}^{n-1}(\varepsilon_i - \varepsilon_{i+1})\frac{K(k_i)}{K(k'_i)}\right) \tag{2.13}$$

$$C_{threefinger} = 4\varepsilon_0 L\left(\frac{K(k_{0,threefinger})}{K(k'_{0,threefinger})} + (\varepsilon_n - 1)\frac{K(k_{n,threefinger})}{K(k'_{n,threefinger})} + \sum_{i}^{n-1}(\varepsilon_i - \varepsilon_{i+1})\frac{K(k_{i,threefinger})}{K(k'_{i,threefinger})}\right) \tag{2.14}$$

$$C_{terminals} = 2NW(2+\pi)\varepsilon_0 L\left(\frac{K(k_{0,terminals})}{K(k'_{0,tterminals})} + (\varepsilon_n - 1)\frac{K(k_{n,terminals})}{K(k'_{n,terminals})} + \sum_{i}^{n-1}(\varepsilon_i - \varepsilon_{i+1})\frac{K(k_{i,terminals})}{K(k'_{i,terminals})}\right) \tag{2.15}$$

For another half-plane:

$$C_{periodical} = \varepsilon_0\varepsilon_{air} L\frac{K(k_0)}{K(k'_0)} \tag{2.16}$$

$$C_{threefinger} = 4\varepsilon_0\varepsilon_{air} L\frac{K(k_{0,threefinger})}{K(k'_{0,threefinger})} \tag{2.17}$$

$$C_{terminals} = 2NW(2+\pi)\varepsilon_0\varepsilon_{air} L\frac{K(k_{0,terminals})}{K(k'_{0,tterminals})} \tag{2.18}$$

The CM transformation includes two steps similar to Wu's model, but the function of transforming *z*-plane into *t*-plane becomes:

$$t = \cosh^2\left(\frac{\pi z}{2h_i}\right) \tag{2.19}$$

And the final formula of modulus k:

$$k_i = \frac{\sinh\left(\pi\frac{W}{2}\Big/2h_i\right)}{\sinh\left(\pi\left(\frac{W}{2}+G\right)\Big/2h_i\right)}\sqrt{\frac{\cosh^2\left(\pi\left(\frac{W}{2}+G\right)\Big/2h_i\right)+\sinh^2\left(\pi\left(\frac{W}{2}+G\right)\Big/2h_i\right)}{\cosh^2\left(\pi\frac{W}{2}\Big/2h_i\right)+\sinh^2\left(\pi\left(\frac{W}{2}+G\right)\Big/2h_i\right)}} \tag{2.20}$$

$$k_{i,threefinger} = \frac{\sinh\left(\pi\frac{W}{2}\Big/2h_i\right)}{\sinh\left(\pi\left(\frac{W}{2}+G\right)\Big/2h_i\right)}\sqrt{\frac{1-\sinh^2\left(\pi\left(\frac{W}{2}+G\right)\Big/2h_i\right)\Big/\sinh^2\left(\pi\left(\frac{W}{2}+W_T+G\right)\Big/2h_i\right)}{1-\sinh^2\left(\pi\frac{W}{2}\Big/2h_i\right)\Big/\sinh^2\left(\pi\left(\frac{W}{2}+W_T+G\right)\Big/2h_i\right)}} \tag{2.21}$$

$$k_{i,terminals} = \frac{\sinh\left(\pi\frac{W}{2}\Big/2h_i\right)}{\sinh\left(\pi\left(\frac{W}{2}+G\right)\Big/2h_i\right)}\sqrt{\frac{1-\sinh^2\left(\pi\left(\frac{W}{2}+G\right)\Big/2h_i\right)\Big/\sinh^2\left(\pi\left(\frac{3W}{2}+G\right)\Big/2h_i\right)}{1-\sinh^2\left(\pi\frac{W}{2}\Big/2h_i\right)\Big/\sinh^2\left(\pi\left(\frac{3W}{2}+G\right)\Big/2h_i\right)}} \tag{2.22}$$

For infinite layer, $h \to \infty$, Eq. (2.20)-(2.22) become simple equations:

$$k_0 = \frac{W}{W+2G} \tag{2.23}$$

$$k_{0,threefinger} = \frac{W}{W+2G}\sqrt{\frac{1-\left(\frac{W+2G}{W+2W_T+2G}\right)^2}{1-\left(\frac{W}{W+2W_T+2G}\right)^2}} \quad (2.24)$$

$$k_{0,terminals} = \frac{W}{W+2G}\sqrt{\frac{1-\left(\frac{W+2G}{3W+2G}\right)^2}{1-\left(\frac{W}{3W+2G}\right)^2}} \quad (2.25)$$

2.4.3 Igreja's model

Igreja and Dias [29] selected "interior" (periodical) and "external" sections shown in Figure 2-8 for investigation. According to the permittivity of substrates, PPC or SPC technique is combined with CM technique.

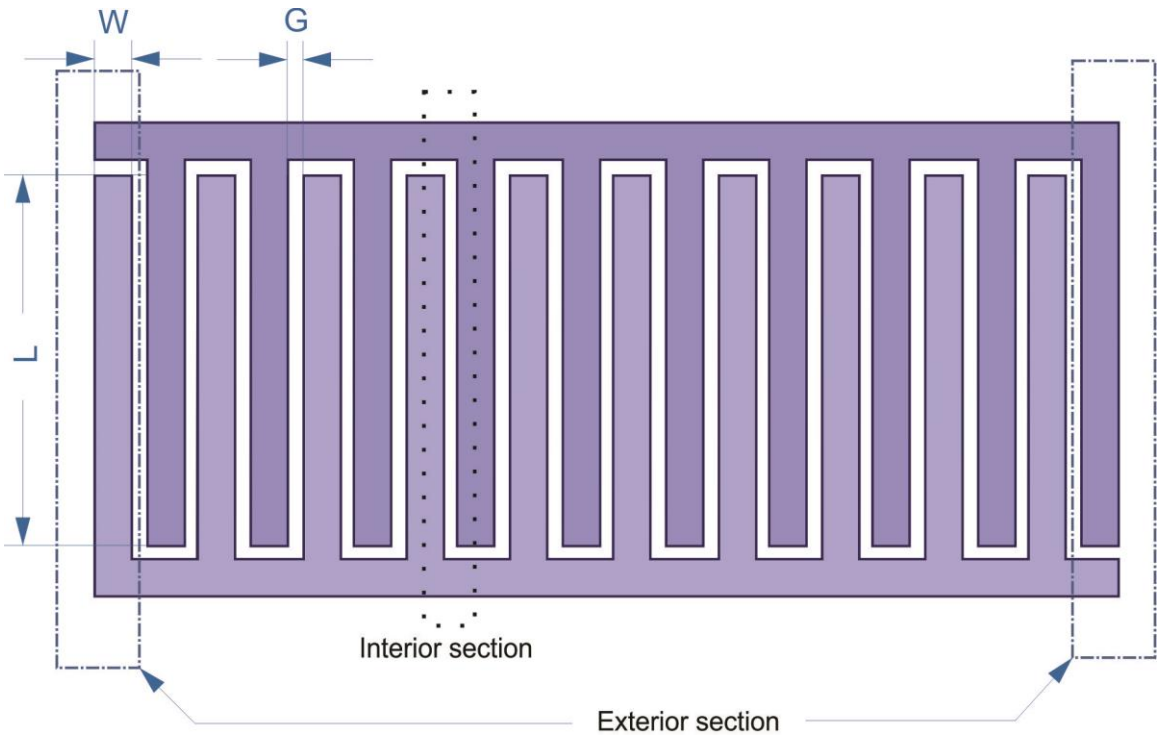


Figure 2-8 Scheme of different sections used in Igreja's model [29]

The total capacitance of one half-plane:

$$C = (N-3)C_I + 2\left(\frac{C_I C_E}{C_I + C_E}\right) \tag{2.26}$$

where C_I and C_E are the capacitances of interior and external sections. These capacitances in the PPC situation, the permittivity monotonic decreases, are:

$$C_{I,PPC} = \varepsilon_0 L\left(\varepsilon_n \frac{K\left(k_{n,I,PPC}\right)}{K\left(k'_{n,I,PPC}\right)} + \sum_{i}^{n-1}(\varepsilon_i - \varepsilon_{i+1})\frac{K\left(k_{i,I,PPC}\right)}{K\left(k'_{i,I,PPC}\right)}\right) \quad (2.27)$$

$$C_{E,PPC} = \varepsilon_0 L\left(\varepsilon_n \frac{K\left(k_{n,E,PPC}\right)}{K\left(k'_{n,E,PPC}\right)} + \sum_{i}^{n-1}(\varepsilon_i - \varepsilon_{i+1})\frac{K\left(k_{i,E,PPC}\right)}{K\left(k'_{i,E,PPC}\right)}\right) \quad (2.28)$$

In the SPC situation, these capacitances are:

$$\frac{1}{C_{I,SPC}} = \frac{1}{\varepsilon_0 L}\left(\frac{1}{\varepsilon_n}\frac{K\left(k'_{i,I,SPC}\right)}{K\left(k_{i,I,SPC}\right)} + \sum_{i}^{n-1}\left(\frac{1}{\varepsilon_i} - \frac{1}{\varepsilon_{i+1}}\right)\frac{K\left(k'_{i,I,SPC}\right)}{K\left(k_{i,I,SPC}\right)}\right) \quad (2.29)$$

$$\frac{1}{C_{E,SPC}} = \frac{1}{\varepsilon_0 L}\left(\frac{1}{\varepsilon_n}\frac{K\left(k'_{i,E,SPC}\right)}{K\left(k_{i,E,SPC}\right)} + \sum_{i}^{n-1}\left(\frac{1}{\varepsilon_i} - \frac{1}{\varepsilon_{i+1}}\right)\frac{K\left(k'_{i,E,SPC}\right)}{K\left(k_{i,E,SPC}\right)}\right) \quad (2.30)$$

For another half plane, these capacitances are simplified as:

$$C_I = \varepsilon_0 \varepsilon_{air} L \frac{K(k_{0,I})}{K(k'_{0,I})} \quad (2.31)$$

$$C_E = \varepsilon_0 \varepsilon_{air} L \frac{K(k_{0,E})}{K(k'_{0,E})} \quad (2.32)$$

To get the CM modulus for PPC case, Igreja and Dias [29] transform the selected region in four steps. When placing the half side of two adjacent fingers in *x*-plane, the points inside this half side are transformed into *z*-plane with function:

$$z = \frac{4K(c)}{2(W+G)}x \quad (2.33)$$

Where

$$c = \left(\frac{v_2\left(0, e^{-4\pi\frac{h_i}{2(W+G)}}\right)}{v_3\left(0, e^{-4\pi\frac{h_i}{2(W+G)}}\right)} \right)^2 \tag{2.34}$$

And transforming *z*-plane into *t*-plane with:

$$t = sn(z, c) \tag{2.35}$$

Before using Schwarz-Christoffel transformation, the *t*-plane is transformed into *y*-plane with:

$$y = \frac{t}{t_2}\sqrt{\frac{t_4^2 - t_2^2}{t_4^2 - t^2}} \tag{2.36}$$

Where

$$t_2 = \mathrm{sn}\left(K(c)\frac{W}{W+G}, c\right) \tag{2.37}$$

$$t_4 = \frac{1}{c} \tag{2.38}$$

Then after Schwarz-Christoffel transformation,

$$k_{i,I,PPC} = t_2\sqrt{\frac{t_4^2 - 1}{t_4^2 - t_2^2}} \tag{2.39}$$

In Eq. (2.34)-(2.39), $\mathrm{sn}(a, b)$ is the Jacobi elliptic function of modulus b; v_2 and v_3 are the Jacobi 2nd and 3rd theta functions.

For infinite layer, $h \to \infty$, Eq. (2.39) becomes:

$$k_0 = \sin\left(\frac{\pi}{2}\frac{W}{W+G}\right) \tag{2.40}$$

Later, Igreja and Dias [29] extended the model using SPC with replacing Eq. (2.39) with:

$$k_{i,I,SPC} = t_2 \tag{2.41}$$

The calculation of t_2 is the same as PPC. And the CM modulus of external section becomes:

$$k_{i,E,SPC} = \frac{1}{t_3}\sqrt{\frac{t_5^2 - t_3^2}{t_5^2 - 1}} \tag{2.42}$$

where,

$$t_3 = \cosh\left(\frac{\pi G}{8\frac{h_i}{W}}\right) \tag{2.43}$$

$$t_5 = \cosh\left(\frac{\pi(2W+G)}{8\frac{h_i}{W}}\right) \tag{2.44}$$

2.5 Comparison and applications of models

The models in the previous section synthesize the analysis of both IDE and multi-layered structures. The distinct difference among these models is the selection of regions except the periodical section. There is only periodical section in Wu's model, but there are external sections in the other two. Gevorgian's model treats two external sections into "three-finger" sections and directly sums its capacitance into total capacitance. On the contrary, Igreja's model leaves two external sections individual and connects them to the periodical section in parallel.

Furthermore, modeling of the periodical section has various processes. Wu's and Gevorgian's models use two-step transformation, but with different transformation functions before applying CM technique. Therefore the final expressions are dissimilar. And Igreja's model uses four-step transformation, making the geometrical parameters adimensional.

Besides the models themselves, the intention of developing models is different. In past years, IDCs are frequently used in lumped elements for microwave integrated circuits. With ferroelectric thin-film, IDCs can also be used as a voltage-controlled tunable device. [23] At that age, although the integrated circuit design including IDCs may be performed by computer software, it is time-consuming. Thus, Wu's and Gevorgian's models aim to be tools for computer-aided design of microwave integrated circuits. Later, Gevorgian's model becomes a useful tool for extraction of dielectric properties of the ferroelectric layers using the measured impedances of tunable microwave devices. [41, 42, 58] In

contrast, Igreja's model aims to the extraction of information as a chemocapacitor sensor with IDEs. [55, 59]

Chapter 3 Modeling BST-based IDCs on GaAs substrates

3.1 Modeling BST

There are several aspects to describe dielectric properties of the ferroelectric materials, including the appearance of spontaneous polarization, a large value of dielectric constant, and dependence of the dielectric constant on temperature and applied voltage.

3.1.1 Temperature effects of BST films

The temperature effect is elementary for ferroelectricity, thus fair enough theoretical and experimental studies have examined the relationship. [60-63] In this section, BST is chosen as a typical representative of perovskite type ferroelectrics. And it is characterized by the spontaneous polarization at the temperature around the temperature of the phase transition, the spontaneous polarization is the start point to create the phenomenon model of it.

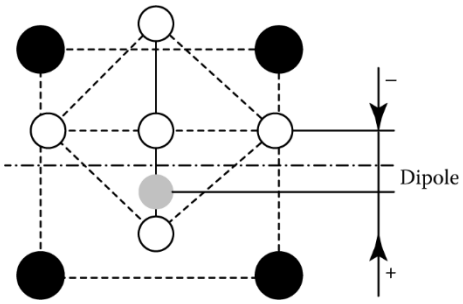


Figure 3-1 Mutual displacement of Ti (gray dot) and O (circles) sublattices bound by Ba (Black dot) sublattice.

In order to investigate the spontaneous polarization and the dielectric nonlinearity of BST, the phenomena in the crystal lattice of the material has been considered. As the description in the previous chapter, polarization of BST is a result of displacement of Ti and O sublattices as shown in Figure 3-1. Mutual displacement of Ti and O sublattices is followed by the formation of an electric dipole. And then the polarization in ferroelectric is defined as

$$P = \frac{qx}{V_c} \tag{3.1}$$

where

q is the charge,

x is the displacement,

V_c is the volume of the crystal cell.

Because the ferroelectric-paraelectric phase transition is the second-order phase transition which does not involve a latent heat, then Landau theory of the second-order phase transition could be applied to this system to describe the appearance of the spontaneous polarization. Landau theory uses free energy to represent the state of a system in the thermodynamic aspect. There is an order parameter introduced as a main feature of the phase transition in Landau theory. [64-67] In ferroelectric material case, the order parameter is the polarization. [68] And the applicable range of temperature is much wider because the dipole polarization dominants the state of the ferroelectric material, so it is

still valid outside of the transition temperature. The free energy density of a ferroelectric sample is taken as a power series with respect to the polarization:

$$F(P,T) = \frac{1}{2}a(T)P^2 + \frac{1}{4}b(T)P^4 + \cdots \tag{3.2}$$

where $a(T)$ and $b(T)$ are the expansion coefficients.

This Eq. (3.2) for free energy density, as a function of a ferroelectric polarization up to the terms of its power 4, is known as the Ginzburg–Devonshire equation. The system would reach equilibrium if the free energy density reaches the extreme, thus the derivative of Eq. (3.2) with respective to polarization should be zero:

$$\frac{\partial F(T,P)}{\partial P} = a(T)P + b(T)P^3 + \cdots = 0 \tag{3.3}$$

When considering the first two terms,

$$P(a(T) + b(T)P^2) = 0 \tag{3.4}$$

The polarization would be:

$$P = \begin{cases} 0, & \frac{a(T)}{b(T)} \geq 0 \\ 0 \text{ or } \pm\sqrt{-\frac{a(T)}{b(T)}}, & \frac{a(T)}{b(T)} < 0 \end{cases} \tag{3.5}$$

This solution implied that the ratio of the coefficients of the first two terms should be related to the phase of ferroelectric materials. In fact, by analyzing the potential energy of the 1D model of perovskite which states in Gevorgian's work, once the ratio is positive,

the ferroelectric material will be in paraelectric state. Conversely, it is in a ferroelectric state when the ratio is negative. Furthermore, since electric field strength is the derivative of free energy, *i.e.*

$$E(T,P) = \frac{\partial F(T,P)}{\partial P} = a(T)P + b(T)P^3 + \cdots \tag{3.6}$$

The higher order terms indicate that the non-linear properties of the ferroelectricity. [69] Also, the inverse dielectric susceptibility is the derivative of electric field strength with respective to polarization:

$$\frac{1}{\varepsilon_0 \chi} = \frac{\partial E(T,P)}{\partial P} \tag{3.7}$$

For a ferroelectric sample with a high permittivity, such as BST, the dielectric susceptibility is practically equal to the permittivity, *i.e.* $\chi = \varepsilon_{\mathrm{r}} - 1 \cong \varepsilon_{\mathrm{r}}$. Thus, the permittivity can be found as

$$\frac{1}{\varepsilon_0 \varepsilon_r} = \frac{\partial^2 F(T,P)}{\partial P^2} \tag{3.8}$$

$$\varepsilon_r = \frac{1}{\varepsilon_0} \frac{1}{a(T) + 3b(T)P^2} \tag{3.9}$$

By considering the Eq. (3.6) and Eq. (3.9), the coefficient $a(T)$ should be:

$$a(T) = \frac{1}{\varepsilon_0 \varepsilon(T)} \tag{3.10}$$

And supposed that the coefficient $a(T)$ should be linear function of temperature with the difference between Curie temperature:

$$a(T) = \alpha_T (T - T_C), \alpha_T = \frac{1}{C_C} \tag{3.11}$$

With Curie constant C_C, and also

$$b(T) = \beta = \text{const.} \tag{3.12}$$

Thus, the relation so-called Curie–Weiss law is derived from the combination of Eq. and Eqs. (3.10) to (3.12):

$$\varepsilon(T) = \begin{cases} C_C \dfrac{1}{T - T_C}, & T > T_C \\ -\dfrac{C_C}{2} \dfrac{1}{T - T_C}, & T < T_C \end{cases} \tag{3.13}$$

This dependence of the dielectric constant on temperature in form Eq. (3.13) could be adequate to the perfect defectless ferroelectric crystal. Plotting the inverse of Eq. (3.13) results in Figure 3-2.

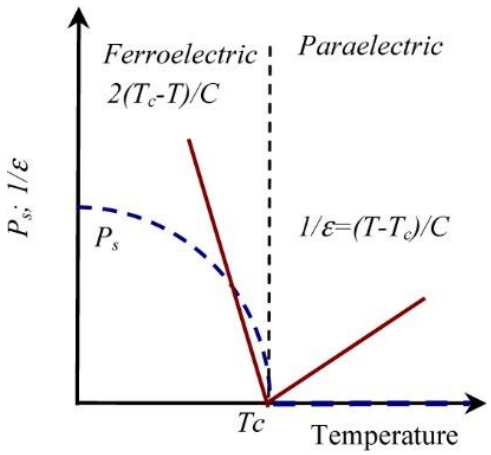


Figure 3-2 2nd order paraelectric to ferroelectric phase transition. Temperature dependences of the polarization and inverse permittivity

Since the dielectric constant is still a function of temperature with Curie constant C_C, the temperature function $\eta(T)$ could be factorized out from Eq. (3.13):

$$\eta(T) \equiv \frac{T}{T_C} - 1 \tag{3.14}$$

And for the paraelectric state, the temperature unrelated dielectric constant ε_{00} could be defended as:

$$\varepsilon_{00} \equiv \frac{C_C}{T_C} \tag{3.15}$$

This temperature function $\eta(T)$ is originally raised from Barrett to describe the temperature dependence of the dielectric constant with quantum consideration. Eq. (3.15) is the approximation of simplified form of Debye integral [70, 71]:

$$\eta(T) = \frac{\theta_F}{T_C}\sqrt{\frac{1}{16} + \left(\frac{T}{\theta_F}\right)^2} - 1 \tag{3.16}$$

where $\theta_F = \frac{h\upsilon_F}{k_B}$ is an analog of the Debye temperature for the sublattice oscillations, responsible for the ferroelectric polarization, υ_F is the cut-off frequency for the Debye spectrum of the crystal sublattice mentioned. With the equations deduced above, the relationship of dielectric constant with receptive to additional biasing field will be derived in the next section.

3.1.2 Biasing field effects of BST films

To investigate the dielectric response of general ferroelectric including BST, it is convenient to simulate a simple sandwich capacitor formed as a planar layer of a ferroelectric with normal metal electrodes as shown in Figure 3-3. The usage of this capacitor structure is suggested by both Vendik [70] and Bratkovsky [72]. On the other hand, according to Zubko *et al.* [73] and Vendik *et al.* [74], the space charge originally located at the electrodes and film results in a lowering of the polarization. Nevertheless, at this section the space charge is not considered, also the fringing fields is not taken into account due to the large ratio between the electrode width and thickness of BST.

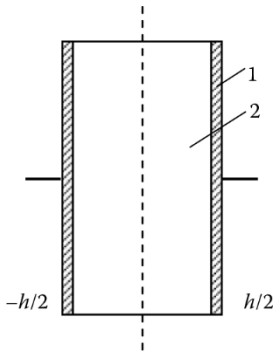


Figure 3-3 Parallel-plate capacitor as a simplified general structure, 1, electrodes; 2, ferroelectric layer

The operation of this tunable capacitor is the same way in microwave circuit. The small amplitude microwave signal would be an AC signal. And then relative large DC voltage shift is added into the signal simultaneously to modify the properties of BST. As BST is a dielectric material, there should be few free charges inside the film. That is a typical case of zero volume charge density, thus the electric displacement field in BST film does

not depend on the coordinates. The total displacement is the sum of induced displacement due to AC signal and DC voltage shift:

$$D = D_{DC} + D_{AC} \tag{3.17}$$

where the terms D_{DC} and D_{AC} are connected with the components of the charge Q_{DC} and Q_{AC} on the capacitor electrodes constant and alternating in time, respectively:

$$D_{DC} = \frac{Q_{DC}}{S}, D_{AC} = \frac{Q_{AC}}{S} \tag{3.18}$$

where S is the area of the capacitor electrodes.

The polarization in horizontal direction (x-direction) created due to the charge generated by AC signal is

$$P_{AC}(x) = D_{AC} - \varepsilon_0 E_{AC}(x) = \frac{Q_{AC}}{S} - \varepsilon_0 E_{AC}(x) \tag{3.19}$$

Because the electric displacement field is proportionate to electric field in dielectric materials, the effect of modified permittivity is presented by the charge accumulated at the electrodes by considering Eq. (3.18). Thus, Q_{DC} is a function of the DC bias voltage U_B applied to the electrodes of the capacitor. From Ginzburg–Devonshire Eq. (3.2), after taking derivative with respect to *P*, because the polarization approximately is equal to the electric displacement field when dielectric constant is much greater than 1, the following equation is given:

$$E_{DC} = aP_{DC} + bP_{DC}{}^3 \approx aD_{DC} + bD_{DC}{}^3 \tag{3.20}$$

and putting the relation Eq. (3.18) the relation of Q_{DC} and DC bias voltage U_B is found as:

$$\frac{Q_{DC}}{S} + \frac{{Q_{DC}}^3}{S^3}\frac{\varepsilon(T)}{{D_N}^2} = \varepsilon_0\varepsilon(T)\frac{U_B}{h} \tag{3.21}$$

where D_N is the normalizing displacement.

To reach the stable state of the system, the free energy stated in Eq. (3.2) should be the minimum. Since Eq. (3.21) is the derivative with respect to P, the roots of the cubic equation correspond to the free energy extreme. For simplifying Eq. (3.21) to dimensionless one, the reduced polarization is defined as:

$$y = \frac{Q_{DC}}{D_N S}\sqrt{3\varepsilon_{00}} \tag{3.22}$$

Also the corresponding normalizing electric field and reduced electric field are as follows:

$$E_N = \frac{2D_N}{\varepsilon_0(3\varepsilon_{00})^{\frac{3}{2}}} \tag{3.23}$$

$$\xi_B = \frac{U_B}{E_N h} \tag{3.24}$$

Eq. (3.21) can be transformed as:

$$y^3 + 3\eta(T)y - 2\xi_B = 0 \tag{3.25}$$

By the nature of Eq. (3.6), this cubic equation has three complex roots corresponding the polarization which is a function of temperature T and biasing field E. Factorizing out y, the condition determining the separation between a high temperature paraelectric phase

and a low temperature ferroelectric phase of the ferroelectric material is the inequalities determining the number of real roots. In addition, the reduced polarization can be calculated out from this equation. However, the goal of calculating the dielectric constant including the biasing field is still unreached. Because the relation $C = \frac{dQ_{DC}}{dU_B}$ hold, differentiating Eq. (3.21) with respect to U, one obtains the capacitance of the capacitor with respect to the small alternating voltage:

$$C(U) = \left(\frac{\varepsilon_0 S}{h}\right)\left(\frac{1}{\varepsilon(T)} + \frac{3{Q_{DC}}^2}{{D_N}^2 S^2}\right)^{-1} \tag{3.26}$$

And substituting Eq. (3.22) into the equation,

$$C(U) = \left(\frac{\varepsilon_0 \varepsilon_{00} S}{h}\right)(\eta + y^2)^{-1} \tag{3.27}$$

Thus finally moving the factor $\frac{\varepsilon_0 S}{h}$ to the left, the effective dielectric constant in a function of both temperature and biasing field shown as below:

$$\varepsilon(E,T) = \frac{\varepsilon_{00}}{y^2 + \eta(T)} \tag{3.28}$$

Hence with Eq.(3.25) and Eq. (3.28), the dielectric constant due to the additional biasing field could be calculated without the geometric of electrode in a parallel capacitor. The non-linearity of dielectric response is major due to the effect of changing polarization by external electric field. Under the applied field, the dielectric permittivity decreases and the maximum of permittivity is shifted to higher temperatures. Nonlinearity of ferroelectrics allows building electrically tunable microwave devices. In addition, when

a BST film is in ferroelectric state, there are three real roots including a trivial one, then there are two peaks in the graph of the permittivity versus applied electric field.

3.1.3 Other Factors Influence Properties of BST films

Previous sections discussed the effect of temperature (in section 3.1.1) and biasing field (in section 3.1.2), in the real device containing BST films, there are other factors influencing the properties. These factors include microstructure [75], the different defects, surface stress of ferroelectric [76-78], the boundary conditions due to electrode and thickness effect of BST [79].

In the fabrication of BST thin films, the oxygen vacancy is unavoidably presented in films. Also, the misfit mechanical stresses due to lattice mismatch between BST films and substrates existed. Form the Pertsev *et al.* report [80], the phase of BST is modified. Thus the result of these defects leads to additional loss while the biasing field is small. This similar result for STO had been discussed in Ang's work [81].

The inhomogeneity factors responded the external field could be analog to "reduced electric field" stated in Eq. (3.24). Then this factor is defined as ξ_S to consist the response derived above. Because the "inhomogeneity field" would influence the polarization as the same time with biasing field, also the dielectric constant is in terms of the square of reduced polarization, then it is a good start point from the square of reduced polarization. While the device operated in paraelectric phase, from Eq. (3.25) reduced polarization could be solved directly:

$$y^2 = \left(\sqrt{\xi_B^2 + \eta^3} + \xi_B\right)^{\frac{2}{3}} + \left(\sqrt{\xi_B^2 + \eta^3} - \xi_B\right)^{\frac{2}{3}} - 2\eta \qquad (3.29)$$

By extracting ξ_B from above equation, and average it with whole biasing field with Gaussian distribution function:

$$f(\eta,\xi_B,\xi_S)=\frac{1}{2\xi_S\sqrt{\pi}}\int_{-\infty}^{\infty}\left\{\left[\sqrt{p^2+\eta^3}+p\right]^{\frac{2}{3}}+\left[\sqrt{p^2+\eta^3}-p\right]^{\frac{2}{3}}\right\}e^{-(\frac{p-\xi_B}{2\xi_S})^2}dp \tag{3.30}$$

Since the both "inhomogeneity field" and biasing field should obey Gaussian distribution, thus the quadratic mean of these fields is expressed as

$$\xi=\sqrt{{\xi_B}^2+{\xi_S}^2} \tag{3.31}$$

The integral part in Eq. (3.30) can be replaced as:

$$f(\eta,\xi_B,\xi_S)=\left[\sqrt{\xi^2+\eta^3}+\xi\right]^{\frac{2}{3}}+\left[\sqrt{\xi^2+\eta^3}-\xi\right]^{\frac{2}{3}} \tag{3.32}$$

Then with considering "inhomogeneity field", the reduced polarization in paraelectric phase is:

$$y^2=\left(\sqrt{\xi^2+\eta^3}+\xi\right)^{\frac{2}{3}}+\left(\sqrt{\xi^2+\eta^3}-\xi\right)^{\frac{2}{3}}-2\eta \tag{3.33}$$

Another factor influencing the polarization is the boundary conditions at the interface between the electrode and BST thin films. The ferroelectric materials are very sensitive to electromechanical boundary conditions due to the long-range nature of their underlying electrostatic interactions and to the strong coupling between the polarization and the strain.

Thus the influence of surfaces and other boundary conditions on their collective behavior is very pronounced. In this case, Devonshir modified the power series by adding the Ginzburg term $|\nabla P|^2$ [82, 83] :

$$F(P,T) = \frac{1}{2}a(T)P^2 + \frac{1}{4}b(T)P^4 + \delta|\nabla P|^2 + \cdots \tag{3.34}$$

To get the boundary condition for the interface, the total free energy could be calculated by integrating density to the volume of the thin films:

$$F_{\text{system}} = \iiint_V dV\left[\frac{1}{2}a(T)P^2 + \frac{1}{4}b(T)P^4 + \delta|\nabla P|^2\right] \tag{3.35}$$

The total free energy includes the integration of gradient term which is the square of gradient of polarization. As free energy is a scalar function and only concerning the magnitude of polarization, *i.e.* scalar, Green's first identity can be used to split the gradient term. Green's first identity is:

$$\oiint_{\partial V} \psi(\hat{n}\cdot\vec{\nabla}\varphi)dS = \iiint_V (\psi\nabla^2\varphi + \nabla\psi\cdot\nabla\varphi)dV \tag{3.36}$$

where ψ and φ are scalars.

For applying to Eq. (3.35), Eq. (3.36) is transformed to:

$$\iiint_V (\nabla\psi\cdot\nabla\varphi)dV = \oiint_{\partial V} \psi(\hat{n}\cdot\vec{\nabla}\varphi)dS - \iiint_V (\psi\nabla^2\varphi)dV \tag{3.37}$$

where $\hat{n}$ is the normal unit vector to the surface.

Plug the magnitude of polarization into Eq. (3.37):

$$\iiint_V (\vec{\nabla}P \cdot \vec{\nabla}P)dV = \iint_S (\hat{n} \cdot \vec{\nabla}P)P\, dS - \iiint_V (P\nabla^2 P)dV \qquad (3.38)$$

The integration of gradient term can be split into two terms. The first term is the surface or interface term, and the second term is the interior term. As the result, the total free energy could be split into the interior term and surface or interface term:

$$F_{\text{interior}} = \iiint dV \left[\frac{1}{2}a(T)P^2 + \frac{1}{4}b(T)P^4 - \delta P\nabla^2 P\right] \qquad (3.39)$$

$$F_{\text{surface}} = \iint dS \left[\frac{1}{2}a(T)P^2 + \frac{1}{4}b(T)P^4 + \delta(\hat{n} \cdot \nabla P)P\right] \qquad (3.40)$$

With the 1D-situation described in previous section, the free energy density of interior is:

$$F = \frac{1}{2}a(T)P(x)^2 + \frac{1}{4}b(T)P(x)^4 - \delta P(x)\frac{\partial^2 P(x)}{\partial x^2} \qquad (3.41)$$

together with the boundary condition by the free energy density of surface:

$$F_{\text{surface density}} = \frac{1}{2}a(T)P(x)^2 + \frac{1}{4}b(T)P(x)^4 + \delta\frac{\partial P(x)}{\partial x} \qquad (3.42)$$

Vendik suggested that the dynamic components of ferroelectric polarization must be zero at the surface of metal electrode. This was proven by the existence of a large crystalline field on the boundary between the ferroelectric and the metals. The "zero" boundary conditions are the fact of blocking of the dynamic ferroelectric polarization. [84] And it was experimentally observed by electron diffraction experiment as a consequence of the distortion of the periodicity of the ferroelectric crystal. This field takes place in a thin layer with the thickness of a few lattice constants. [85] In Eq. (3.42), this boundary condition led to the fact:

$$P_{AC}(x)|_{x=\pm\frac{h}{2}} = 0 \tag{3.43}$$

From Eq. (3.41), neglecting the higher power of AC components, the differential equation would become:

$$E_{AC}(x) - \delta\frac{d^2E_{AC}(x)}{dx^2} = \frac{Q_{AC}}{\varepsilon_0 S}\left(\frac{1}{\varepsilon(T)} + \frac{3{Q_{DC}}^2}{{D_N}^2 S^2}\right) \tag{3.44}$$

For the differential equation, there is a particular solution:

$$E_{AC}(x) = A\sinh(\alpha x) + B\cosh(\alpha x) + \frac{Q_{AC}}{\varepsilon_0 S}\left(\frac{1}{\varepsilon(T)} + \frac{3{Q_{DC}}^2}{{D_N}^2 S^2}\right) \tag{3.45}$$

With Eq. (3.43) and the symmetry of the capacitor:

$$E_{AC}(x) = \frac{Q_{AC}}{S}\left\{\left(\frac{1}{\varepsilon(T)} + \frac{3{Q_{DC}}^2}{{D_N}^2 S^2}\right) + \left(\frac{\cosh(\alpha x)}{\cosh\left(\alpha\frac{h}{2}\right)}\right)\left[1 - \left(\frac{1}{\varepsilon(T)} + \frac{3{Q_{DC}}^2}{{D_N}^2 S^2}\right)\right]\right\} \tag{3.46}$$

Integrating Eq. (3.46) with respect to x form $-\frac{h}{2}$ to $\frac{h}{2}$ gives

$$U_{AC}(x) = \frac{Q_{AC}h}{S}\left\{\left(\frac{1}{\varepsilon(T)} + \frac{3{Q_{DC}}^2}{{D_N}^2 S^2}\right) + \left(\frac{\tanh(\alpha x)}{\alpha\frac{h}{2}}\right)\left[1 - \left(\frac{1}{\varepsilon(T)} + \frac{3{Q_{DC}}^2}{{D_N}^2 S^2}\right)\right]\right\} \tag{3.47}$$

Then with approximation $\varepsilon(T) \gg 1$of and $\alpha h \gg 1$:

$$U_{AC}(x) = \frac{Q_{AC}h}{S}\left\{\left(\frac{1}{\varepsilon(T)} + \frac{3{Q_{DC}}^2}{{D_N}^2 S^2}\right) + \frac{2}{\alpha h}\right\} \quad (3.48)$$

differentiating Eq. (3.48) with respect to U, and compared to Eq. (3.26), the effective dielectric constant:

$$\varepsilon(E,T) = \frac{\varepsilon_{00}}{y^2 + \eta(T) + a^2_{\text{Corelation}}} \quad (3.49)$$

where

$$a^2_{\text{Corelation}} = \frac{2\varepsilon_{00}}{\alpha h} \quad (3.50)$$

Moreover, compared to Eq. (3.28), Eq. (3.49) could be rewritten as:

$$\varepsilon(E,T,h) = \frac{\varepsilon(E,T)}{1 + \frac{r_c}{h}} \quad (3.51)$$

where

$$r_c = \frac{2\varepsilon(E,T)}{\alpha} \quad (3.52)$$

The value of r_c is call the correlation radius of the ferroelectric. For BST, correlation parameter depends on the composition factor x. In the general case, the size effect parameter α of the displacive ferroelectric BSTO can be found from dielectric measurements.

3.1.4 Microwave Properties of BST

In the simple model described in the above section, there is not any dissipation of the microwave energy included, and no frequency-related loss mechanism discussed yet. Thus in this section, the main physical phenomena responsible for dissipation in the ferroelectric material will be described. By the results given by Silverman [86], Smolenskii [87], R. Blinc and B. Zheksh [4], the response function of a ferroelectric can be written in the form of dielectric susceptibility

$$\chi(\omega) = \frac{\chi(0)\omega_C^2}{\omega_C^2 - \omega^2 - i\omega\gamma + \frac{\delta^2}{1 + i\omega\tau}} \tag{3.53}$$

where

ω is the angler frequency,

ω_c is the eigenfrequency of the ferroelectric mode,

γ is the intrinsic dissipation factor of the ferroelectric mode,

τ is the relaxation time of an additional relaxation mechanism responsible for the dissipation of the ferroelectric mode oscillation energy,

δ is the coupling coefficient of the relaxation mechanism and the ferroelectric mode.

When the temperature of the ferroelectric crystal is near to the Curie temperature, elasticity of the sublattice displacement becomes softer. That leads to increase in the dielectric permittivity $\varepsilon_f(T)$ and decrease in value of the eigenfrequency of the ferroelectric mode of crystal lattice oscillation $\omega_c(T)$. The well-known Lidden-Sakse-Teller relation [88] claims that

$$\omega_C^2(T)\varepsilon_f(T) = \text{const.} \tag{3.54}$$

Smaller ω_C, permittivity and tunability of the ferroelectric material is higher. Because of a small value of elasticity of the sublattice displacement responsible for the value of the eigenfrequency, the ferroelectric mode is called the soft mode. In actual application of BST, the operation frequency is much smaller than eigenfrequency which is in order 100 GHz. Thus once the numerator and denominator in Eq. (3.53) are divided by the square of eigenfrequency, the ratio $\frac{\omega^2}{\omega_C^2} \approx 0$. Then as the same treatment Eq. (3.7) and Eq. (3.8), permittivity of a ferroelectric material, the permittivity may be supposed to be equal to susceptibility, Eq. (3.53) could be rewritten as

$$\varepsilon(E,T,\omega) = \frac{\varepsilon(E,T,0)}{R(E,T) + I(E,T,\omega)} \tag{3.55}$$

where $R(E,T)$ is the real part and $I(E,T,\omega)$ is the imagery part of the denominator divided by the square of eigenfrequency in Eq. (3.53). Fortunately, Vendik had given the major frequency-related loss mechanisms [70, 89], and Eq. (3.55) could be extended as following:

$$\varepsilon(E,T,\omega) = \frac{\varepsilon_{00}}{y^2 + \eta(T) + \sum_{q=1}^{4} \Gamma_q(E,T,\omega)} \tag{3.56}$$

In Eq.(3.56), beside the DC response relates to $y^2 + \eta(T)$ which does not depend on the frequency, the remaining part is the sum of four different loss mechanisms. This sum is the complex functions of the frequency. Then the loss factor is:

$$\tan\delta(E,T,\omega) = \frac{\mathrm{Im}[\varepsilon(E,T,\omega)]}{\mathrm{Re}[\varepsilon(E,T,\omega)]} \tag{3.57}$$

These four different loss mechanisms can be classified into two groups: phonon scattering loss and defect loss. The phonon scattering includes the multiphonon scattering in the ferroelectric soft mode and quasi-Debye scattering. The fundamental channel of the soft mode energy dissipation is a nonlinear interaction between soft mode oscillations and thermal oscillations of the crystal lattice. It is so-called multi-phonon interaction.[47, 90] The nonlinear interactions of the optical phonons are responsible for the ferroelectric phase transition, revealing a high value of dielectric constant of the ferroelectrics. It means that the interactions between the soft mode oscillations and thermal oscillations of the crystal lattice, which are responsible for the dissipation, determine at the same time the ferroelectric nature of the material. That is the reason that this loss mechanism is called the fundamental one. Ryen [91] had demonstrated the analysis of the high-frequency dielectric properties on a microstructural using electron energy-loss spectroscopy in transmission electron microscopy. Meanwhile, the numerical characteristics of the fundamental loss are described by the same qualitative parameters, which are responsible for the ferroelectric properties of the crystal. In accordance with the Lidden-Sakse-Teller relation, the eigenfrequency of the soft mode is:

$$\omega_C(E,T) = \omega_{00}\sqrt{y^2 + \eta(T)} \tag{3.58}$$

Moreover, the maximum frequency in the spectrum of optical phonons in the crystal ω_M should be involved. There is the relation between this frequency and the Debye temperature:

$$\hbar\omega_M = k_B\theta_F \tag{3.59}$$

Thus, according to Vendik's [89] and Tagantsev's [90]work, this kind of loss is given as:

$$\Gamma_1(E,t,\omega) = -i\frac{\pi}{8}\frac{\omega_{00}}{{\omega_M}^2}\left(\frac{T}{T_C}\right)^2 \omega\sqrt{y^2+\eta(T)} \tag{3.60}$$

The coefficient $\omega_{00}(x)$, ω_M can be found from inelastic neutron scattering. In Vendik's work, these values are given as: $\omega_{00}(x) = 0.67(1+6x)\times 10^{13}/\mathrm{s}$; $\omega_M = 2.6\times 10^{13}/\mathrm{s}$, where x is Ba concentration.

In other Tagantsev's work, the quasi-Debye mechanism of loss is explained as the relaxation of the crystal phonon distribution. When the DC biasing field is applied to the BST crystals while there is already transmitting the AC signals, the phonon distribution of lattice is changed. There is time modulation for varying the DC field to make the system reaches a new equilibrium state. The dielectric response is inevitably delayed for a certain time interval, which is called the relaxation time. The relaxation of the phonon distribution function gives rise to the dielectric loss in a similar way as the relaxation of the gas of dipoles gives rise to the loss in the Debye theory. That is why the loss mechanism considered is called the quasi-Debye one. And the contribution of the quasi-Debye mechanism into the dielectric response of the sample is found in the form:

$$\Gamma_2(E,t,\omega) = \frac{A_2}{1+i\frac{\omega}{2\pi f_2}}\frac{y^2(E,T)}{1+\xi^2(E)} \tag{3.61}$$

where

$f2 = 30$ GHz is the inverse relaxation time of change of the phonon distribution function,

$A_2(x) = 0.8\,(1 + 20x)^{-1}$ is a coefficient characterizing the rate of the contribution of the mechanism considered.

On the other hand, the properties of real ferroelectric samples differ from an ideal single crystal sample dramatically. It had been reported by Zhang's team [92]. The potential wall of the lattice, in relaxation aspects, the ability of freezing relaxation has the simple relationship to the BST grain size up to 1 μm. Moreover, the presence of charged defects results in additional losses in material. Using the ferroelectrics in a capacitor as a thin film leads to excitation of loss mechanism associated with the transformation of energy into high frequency acoustic waves.

The electrostriction under the static electric field produced by the charged defects leads to an induced piezoelectric effect and is followed by the excitation of acoustic vibrations in the sample. The frequency dependence of the energy dissipation has a character of the relaxation process. The relaxation time is determined by the characteristic size of the defect configuration, which depends on the growing process of the sample. Vendik and Platonova [93] investigated the contribution of the charged defects into losses in ferroelectrics. The result of the investigation can be presented as follows:

$$\Gamma_3(E,t,\omega) = \frac{A_3 {\xi_S}^2}{1 + i\frac{\omega}{2\pi f_3}} \tag{3.62}$$

Vendik supposed the most reasonable value of the inverse relaxation time is $f_3 \cong 10$GHz. [89] The contribution rate of the mechanism considered is proportional to the density of the charged defects. In Eq. (3.62), ξ_S is substituted instead of the defect density reasoning that parameter ξ_S as a characteristic of the crystal quality is connected with the defect density. Also he supposed that $A_3 \cong 0.05$ on the basis of comparison results obtained with the formulas developed in his work.[89]

Since the quasi-Debye and charge defect mechanisms of losses are both related to the relaxation, the difference is the dependence on the applied voltage or polarization. In the case of the quasi-Debye loss, the energy of the microwave field is immediately transformed into the heat of the crystal lattice. The higher is polarization, being spontaneous or induced by the applied voltage, the higher is the energy dissipation through the quasi-Debye mechanism. In the case of the charge defect mechanism, the microwave field is transformed first into the high frequency acoustic waves. And then the acoustic waves are dissipated by the crystal lattice. The intensity of the induced piezoelectric transformation does not depend on polarization. The applied voltage suppresses the inverse dielectric permittivity and as a result of that, the higher the applied voltage, the smaller is the contribution of charge defect mechanism to losses.

The last loss mechanism is low-frequency relaxation, although this effect is less obvious when the device operates at high frequency. The nature of that is not properly explained till now. In phenomenological view, it can be attributed to a relaxation process and described by the following formula:

$$\Gamma_4(E,t,\omega) = \frac{A_4}{1 + i\frac{\omega}{2\pi f_4}} \tag{3.63}$$

where

ω is the frequency at which the dielectric characteristics of the material are measured,

A_4 and f_4 are the parameters of the model: $A_4 = 0.005$, $f_4 = 10\text{MHz}$.

3.1.5 Summary

The properties of BST films used in a microwave circuit depend on temperature, applied DC voltage and operating frequency. The core of developing the relation is needed to use the free energy density of ferroelectric. Because the order parameter in free energy density is the polarization, the dielectric response in fact is the result of altering the polarization by these dependence factors. Mathematically calculated the dielectric constant of BST with known or most probably reasonable "inhomogeneity field" ξ_S and correlation parameter α (or the correlation radius r_C), Eq. (3.56) is the starting point, with solving Eq. (3.25)to get "reduced polarization" y.

At this stage of modelling BST thin films, the in-plane properties of BST have been presented through the function used in the parallel capacitor and without detailed consideration of mismatch stress, because the "inhomogeneity field" ξ_S is included this effect. However, it would be an important and solid relationship to consider any factors modifying the dielectric response of BST in modelling microwave device.

3.2 Modeling BST-GaAs-based IDCs

The techniques for current models are described in the section 2.3 above. The usage of these techniques depends on the boundary condition of the interface.

Nevertheless, the more accurate model should be developed by re-analyzing the condition by the help of numerical electromagnetism simulation in finite element method. The modification of these models is derivation from the material properties. The condition of BST-GaAs interface is verified through the finite element simulation using computer software ANSYS's high frequency structure simulator (HFSS). For reducing the complexity and focusing the interface, two adjacent electrode fingers in an IDE replace the whole IDC to be used in the simulation. In fact, the origin of modeling the IDCs is to slice the whole IDC into coupled micro strip lines and coplanar waveguides [21, 46, 94, 95], because there is a period pattern of a pair adjacent micro strip alike electrodes.

In addition, using coupled microstrip lines instead of whole IDCs, the dielectric properties of BST thin film are calculated using the model stated above, before entering the material properties in the simulation.

3.2.1 Verifying Neumann boundary condition of BST-GaAs interface

The GaAs substrate has relatively low dielectric constant compared to conventional oxide wafers. It could reduce the electric field penetration into the substrate, thus the applied field can be more effective in excitation the in-plane ferroelectricity of the BST films. Figure 3-4 shows the electrical potential distribution between positive and negative electrodes of coupled micro strip lines on BST-GaAs substrates.

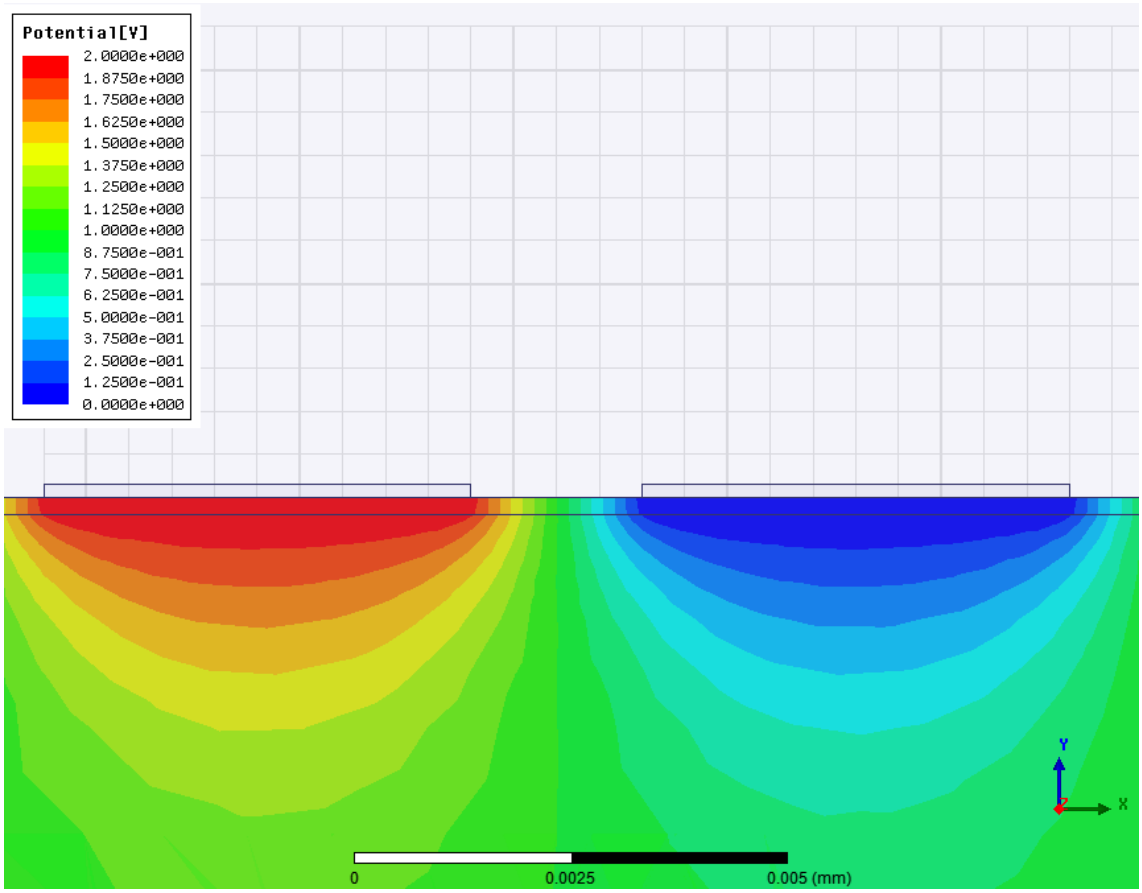


Figure 3-4 The electrical potential distribution between positive (+2 V) and negative (grounded) electrodes by using finite element simulation

The electric potential gradient between the BST-STO interfaces and between the STO-GaAs interfaces are zero vertically. These results fulfill the Neumann boundary condition. It indicated that the total contribution from all M layers should be computed as the sum of each layer.

3.2.2 Verifying electric fields of BST-GaAs interface

The electrical potential gradient between the interfaces is zero as shown in Figure 3-4, which indicates that the interface should be considered as the Neumann boundary condition, it is not a perfect electric wall to reject any electric field entering to the GaAs layer.

It is important to notice that field penetration in the vertical direction is still not negligible. Figure 3-5 and Figure 3-6 shows that the horizontal and vertical components of electric fields instead of potential, while the condition is same as one in Figure 3-4. The vertical components are strong at the edge of the electrodes. It is inevitable and normal in the BST layer, but it is obviously interesting that the same behaviors happen in GaAs layer. Also the finite element simulation shows that the maximum value of the horizontal and vertical components is about 15 times different.

In addition, the electric field in BST layer would be concentrated in the separation of the electrodes. The effect of changing the dielectric properties of BST would be greatly occur in this region. It is the similar result reported in Kageyama's simulation and experiment. [96] The average electric field of inner ferroelectric could be approximately to, but slightly less than the electric field between electrodes.

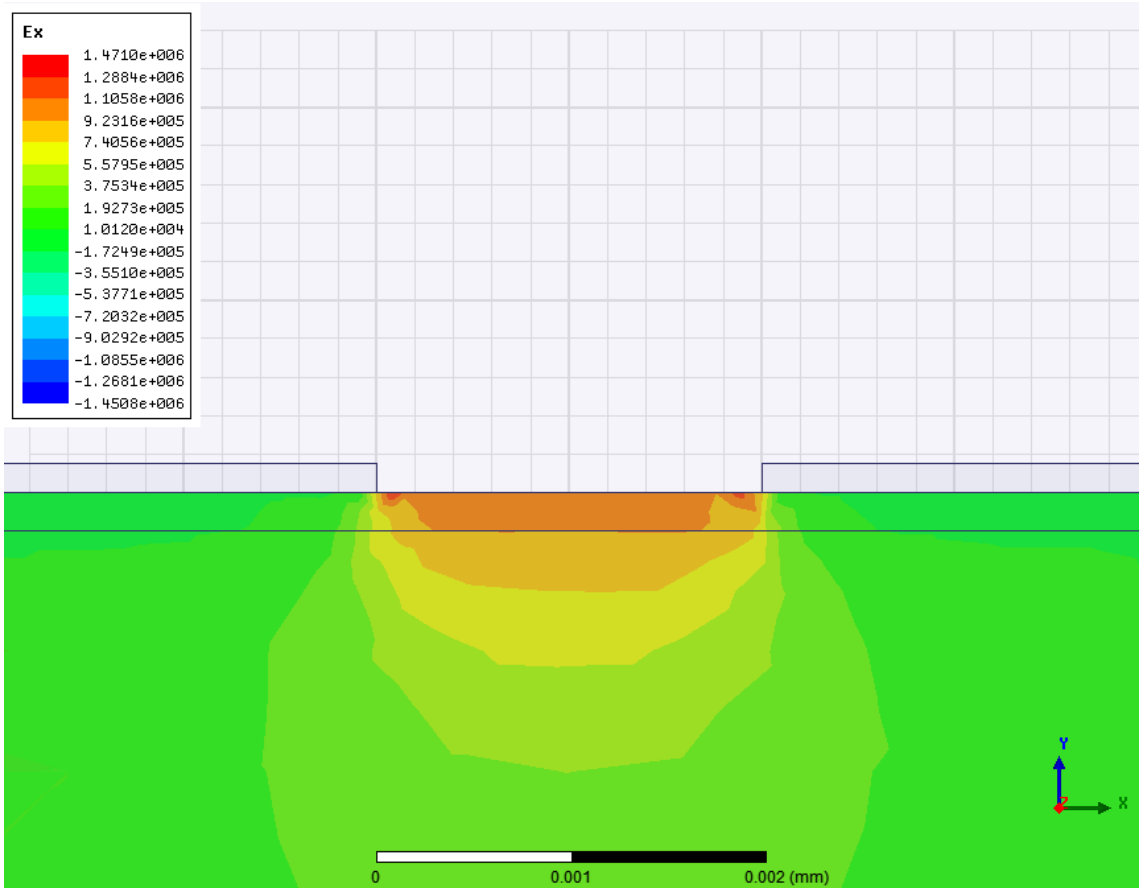


Figure 3-5 The horizontal component of electric field between positive (+2 V) and negative (grounded) electrodes by using finite element simulation

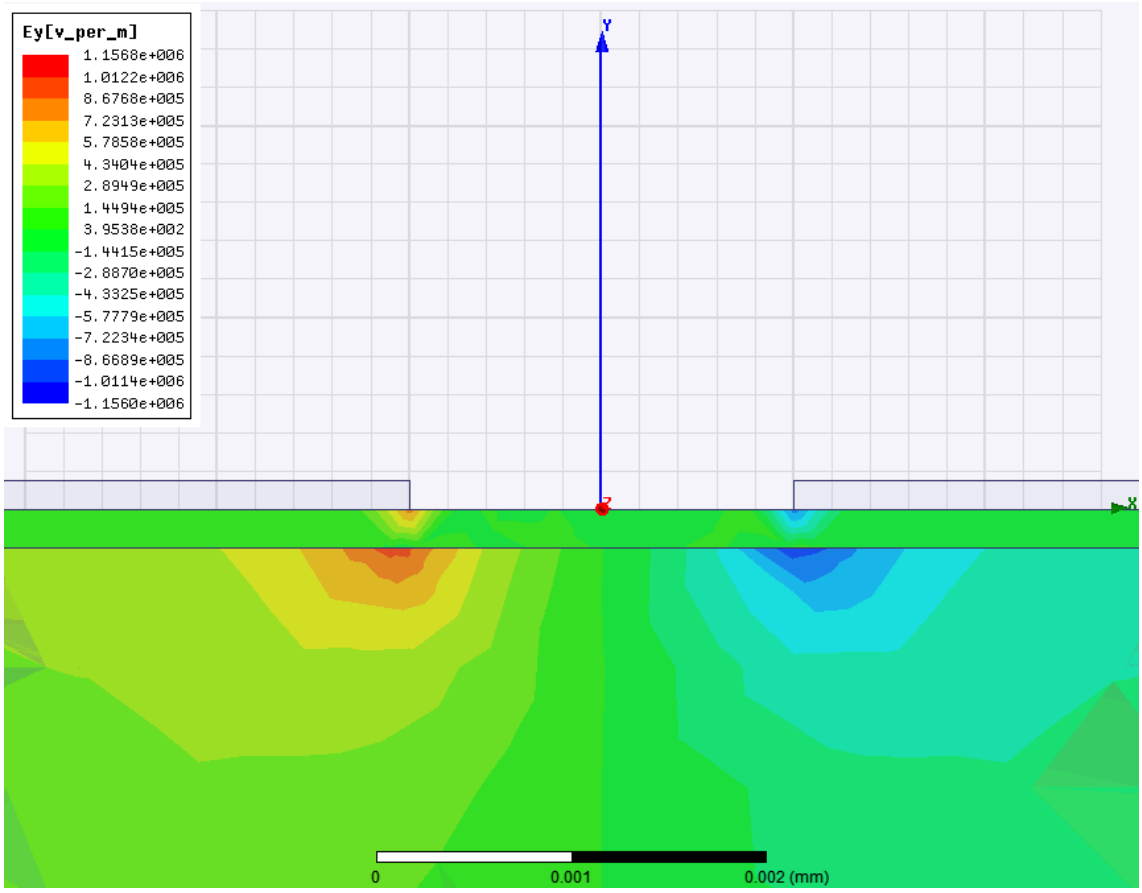


Figure 3-6 The vertical component of electric field between positive (+2 V) and negative (grounded) electrodes by using finite element simulation

Once the electric field in the substrate behaves the same as BST layer, but the mobility of the substrate is much higher, then electrons in the substrate may oscillate between the "virtual electrodes" when applying AC on top electrodes. That is the main reason for "current leakage" in different substrates, especially for low resistance ones. This effect had been reported by Panakhov *et al.* [97]. Hence, the interface effect should be modelled individually.

3.2.3 Establishing a model by considering applied electric field in BST layer

After verifying the potential of BST-GaAs for choosing a suitable main technique for multi-layered structure, and the electric fields in both BST and GaAs layers for reviewing the interface effects, now the designated IDCs with BST-STO-GaAs heterostructure are modeled by applying these conditions for modifying current models.

First, the condition of applying the confirmation mapping is the satisfaction of Laplace's equation in each layer. Second, the condition of applying the partial capacitance technique is the monotonically decreasing of dielectric permittivity. For BST dielectric layers, there are few free elections in ionic lattice, even applying the external electric field on it. Also the permittivity of BST layer is obviously greater than GaAs substrate. No matter the thickness of BST layer, according to the discussion above, the permittivity of BST would be larger than a hundred. The difference between adjacent layers is always a positive number. Thus, most conditions required in both models mentioned above are fulfilled. These analytical models for the IDCs should be valid in some aspects.

In above analytical models, the electric field is applied on the BST surface between the electrodes. The distribution of electric field line inside the ferroelectric films is much less uniform like a parallel plate capacitor. Nevertheless the electric field concentrated in the region of a ferroelectric layer between the vertical edges of the electrodes. This region reflects the behaviors of in-plane dielectric properties of BST thin films.

The electrode thickness should be considered when evaluating the exact value of the electric field applied to the BST layer in IDC as Eq. (2.1), which reduce the effective separation between electrodes to increase the electric field. And also the minimization of the free energy accumulated in ferroelectrics, which lead to reduce the electric field in ferroelectrics, should be considered in this case. In the samples considered, by using Vendik's suggested effective electric field calculation methods [98]:

$$E_{eff} = \frac{U}{G + \zeta\, h_{ferro}} \tag{3.64}$$

where

h is the thickness of the ferroelectric layer adjacent to the electrodes;

the parameter ζ should be in a range $0.7 < \zeta < 1$.

Besides for the modification of the applied electric field in BST, the interface between the electrode and BST layer is notable. The polarization must be zero at the surface of metal electrode as the discussion of the other factors influence BST. Because the boundary conditions are hold in this case, when the thickness of BST is comparable to certain dimension, which is considered as a correlation radius, the size effect is suffering from in BST thin films. The final dielectric constant of BST would be the factor of bulk's one as Eq. (3.51). For convenience, this equation could be rewritten as:

$$\frac{1}{\varepsilon_{\text{film}}} = \frac{1}{\varepsilon_{\text{bulk}}} + \frac{2}{\alpha h} \tag{3.65}$$

This is the size effect stated in the Vendik's paper [99].The origin of Eq. (3.65) is emphasized in Lookman's paper [100]. Because once the thickness is considered as a

factor of modifying the phase transition temperature, Lookman *et al.* point out that is not the simple case. Thus Eq. (3.65) is listed here to indicate more device-oriented usages.

3.2.4 Establishing a model by considering layer conductance

On the other hand, the substrate itself has certain conductance and would influence the high frequency response.

In the Gevorgian's model, the conductance of each layer would be modeled similarity as the capacitance. And the total line conductance is then the sum of all partial conductance:

$$G = \frac{1}{2}\left(\sigma_1 \frac{K(k_1)}{K(k_1')} + \sum_{i=2}^{M}(\sigma_i - \sigma_{i-1})\frac{K(k_i)}{K(k_i')}\right) \tag{3.66}$$

where σ is the electrical conductivity of a substrate layer.

Also the conductance could be written in terms of loss tangents:

$$G = \frac{1}{2}\varepsilon_0\omega\left(\varepsilon_1\tan(\delta_1)\frac{K(k_1)}{K(k_1')} + \sum_{i=2}^{M}(\varepsilon_i\tan(\delta_i) - \varepsilon_{i-1}\tan(\delta_{i-1}))\frac{K(k_i)}{K(k_i')}\right) \tag{3.67}$$

In Igreja's model, the effect of the conductance would be presented by using complex permittivity in his final expressions. However, using complex permittivity directly in modified model would cause the difficulty of calculation in total capacitance including the interface effect.

3.2.5 Establishing model by considering the interface

The value of such interfacial component could be calculated as the even mode capacitance in Gevorgian's work [22]. There is a different confirmation mapping in the region between the electrode and the STO(BST)-GaAs interface, the modulus $k_{\text{interface}}$ could be calculated:

$$k_{\text{interface}} = \frac{\cosh\left(\pi\frac{\frac{G}{2}}{2h_2}\right)}{\cosh\left(\pi\frac{\frac{W+G}{2}}{2h_2}\right)} \tag{3.68}$$

Where h_2 is the position from the electrode to the STO(BST)-GaAs interface. And the interfacial capacitance is:

$$C_{\text{Interface}} = \varepsilon_0 L(\varepsilon_{\text{STO}} - \varepsilon_{\text{GaAs}})\frac{K(k'_{\text{interface}})}{K(k_{\text{interface}})} \tag{3.69}$$

Since the distribution of vertical components at the interface between ferroelectrics and substrate is similar to that between ferroelectrics and electrodes, it could be modelled that there are "virtual electrodes" projected to the interface as shown in Figure 2-5. This technique was once used in Gevorgian's work to resolve the circumstances that the dielectric constant of an active layer was less than of substrates, but not like this case which is the "normal" one.

3.3 Summary of modelling BST-GaAs-based IDC

Finally, the equivalent lump component circuit of a periodical section would be shown as Figure 3-7. The major difference between modified model and current models are the treatment of the BST-GaAs interface. In either Gevorgian's or Igreja's models, there is no interfacial component. Similar to the previous section, the interface capacitance would be applied to remaining part, according to the analytical models used. It would be connected between the equivalent capacitors of ferroelectric and its substrate. The total calculated capacitance is suggested by Miller [101]. In the calculation of substrate capacitance, the height should be replaced by in the calculation.

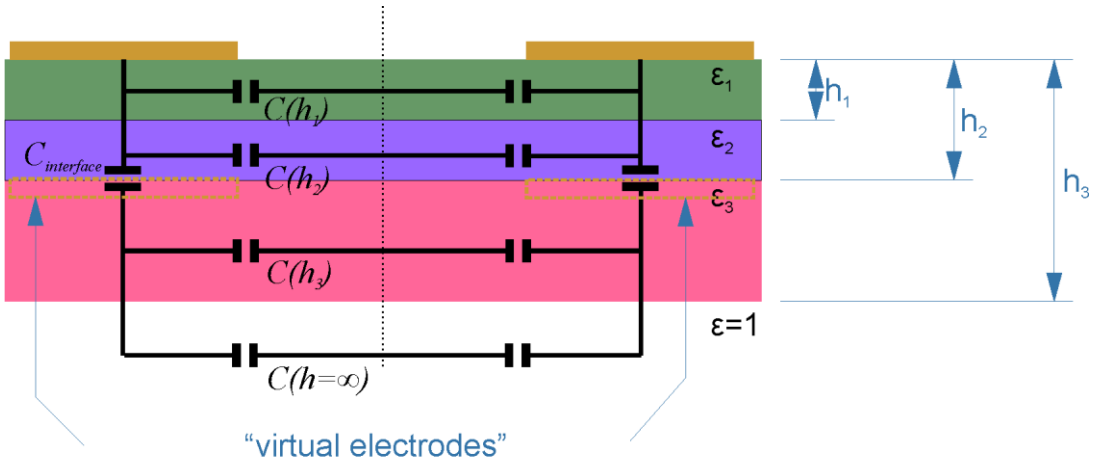


Figure 3-7 Final modified multi-layer structure of the capacitance between adjacent fingers in periodical section

In this model, the total capacitance of two adjacent electrodes in IDCs is in three parts: capacitance formed by BST and STO layer, interfacial capacitance and capacitance formed by GaAs:

$$C = C_{\text{Ferro}} + ((C_{\text{Sub}})^{-1} + (C_{\text{Interface}})^{-1})^{-1} \quad (3.70)$$

To calculate the capacitance formed by BST and STO layer, the normal way as the current models is demanded:

$$C_{\text{Ferro}} = \frac{1}{2}\varepsilon_0 L\left((\varepsilon_{\text{BST}} - \varepsilon_{\text{STO}})\frac{K(k_1)}{K(k_1')} + (\varepsilon_{\text{STO}} - \varepsilon_{\text{GaAs}})\frac{K(k_2)}{K(k_2')}\right) \quad (3.71)$$

When calculating the capacitance formed by GaAs, the "virtual IDC" is considered, thus the capacitance could be:

$$C_{\text{Sub}} = \frac{1}{2}\varepsilon_0 L\left((\varepsilon_{\text{GaAs}} - 1)\frac{K(k_3)}{K(k_3')} + \frac{K(k_0)}{K(k_0')}\right) \quad (3.72)$$

Chapter 4 Simulation of BST-based IDCs on GaAs Substrates

4.1 Introduction of the simulation process

The modified model for BST-based IDCs fabricated on GaAs substrates has been derived and discussed in Chapter 2. The microwave performance of IDCs can be simulated by substituting different parameters in the model. In this chapter, there are two IDCs to be performed for the simulation. They are both $Ba_{0.7}Sr_{0.3}TiO_3$-STO-GaAs heterostructures. The STO buffer layer in both samples is about 10 nm, but the BST layers have different thickness, namely about 250 nm and 400 nm. They share the same layout and parameters of IDEs. The IDEs have a total of 21 fingers with figure length of 925 μm, a finger width of 5 μm, and a finger gap of 2 μm. Also it can be assumed that the thickness is 100 nm, and terminal width is 50 μm.

To provide reusable simulation for these different IDCs, the related formulas were programmed in to MATLAB scripts. Although the model can be given by the closed-form expressions, the certain equations, especially the partial differential equations related to the polarization in a BST layer, can be used to reconstruct the electrical field distribution and dynamic dielectric response.

4.2 The process of simulation by using closed-form expressions

For the fast approach of simulation with acceptable accuracy in IDCs, the closed-form expressions in the modified model can be used. The total capacitance is calculated according to Gevorgian's or Igreja's model with the modification in this work. These equations should be the entry points for programming the simulation. The key geometrical parameters of the IDCs then is set to the designated value.

The microwave properties of IDCs are majorly determined by the BST layer under the influence of both frequency and biasing electric field. The "inhomogeneity field" ξ_S and correlation parameter α should be chosen as proper values for indicating the quality of BST layers. These values, principally are gotten from the physical experiment. In this chapter, it is reasonable to assume $\xi_S = 1.4$ and $\alpha = 22600$ μm^{-1}[71].

4.3 The visual presentation of the simulation

To provide the visualized presentation of the progress for the simulation, the graphical user interface was created. Then the interface was programed with the Windows Presentation Foundation (WPF) which is a computer-software graphical subsystem for rendering user interfaces in Windows-based applications. It is chosen because these two reasons:

(1) It provides a fast development due to the interface can be programmed as like web pages.

(2) It is based on the .NET Framework which is similar to JAVA libraries for making the program easier to be handled by others whom are not rough programmers.

Thus Figure 4-1 shows a flow chart to present the project progress. A system engineering process makes tasks in this work more clear to be traced. Figure 4-2 shows the complete program. The complete program can then be used for the simulation.

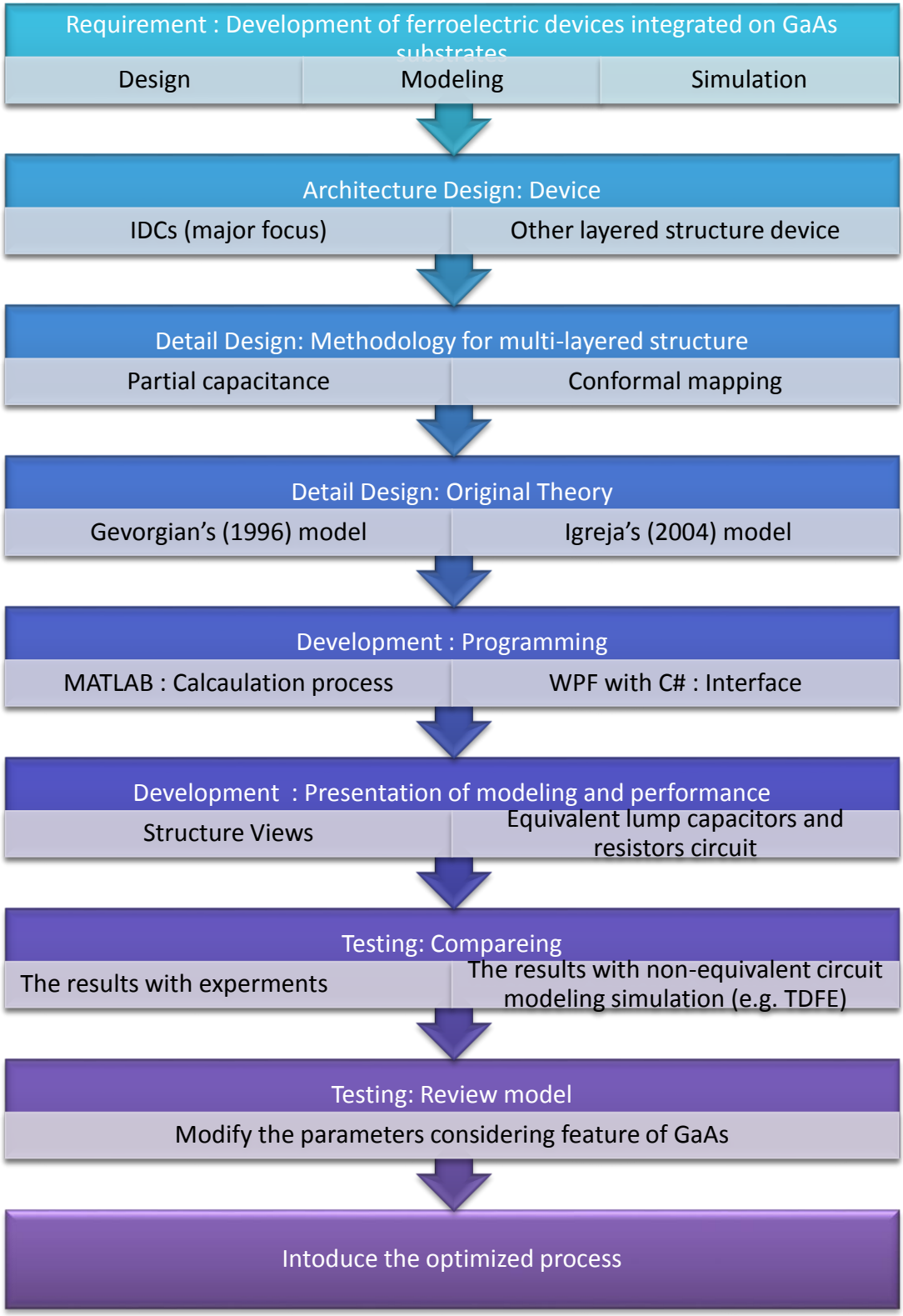


Figure 4-1 The system engineering process for simulation

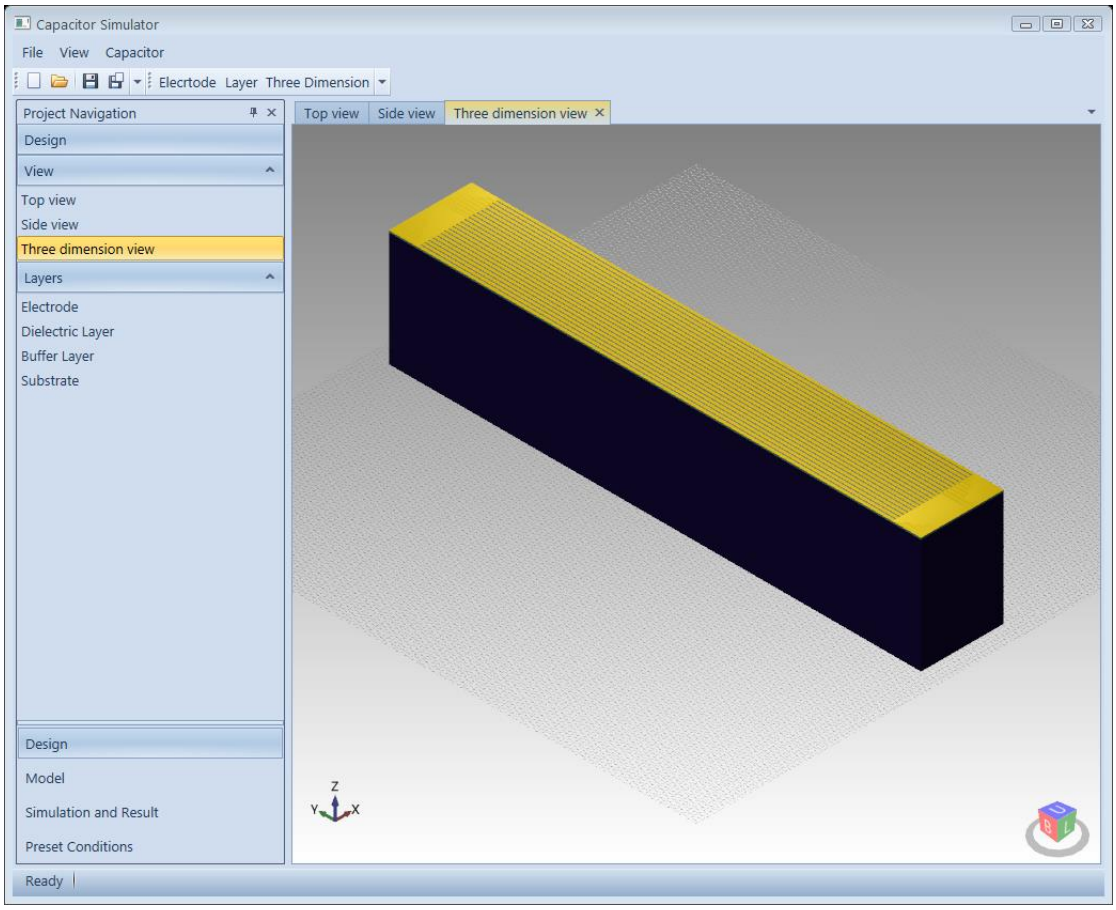


Figure 4-2 The simulation program with demonstration of IDCs

4.4 Results of simulation

4.4.1 The simulation in ideal cases

The ideal case of IDCs is that the electric field generated by the electrodes distributes in whole BST and STO buffer layer. This distribution is not uniform but in elliptical shape between the positive and negative electrodes. The IDCs with BST(7:3)(250nm)-STO(10nm)-GaAs substrates are simulated with the modified Igreja's Model. With the default parameters of BST states above, the model suggests the capacitance of this IDC can be changed from around 110pF to 50pF. Figure 4-3 shows this result. Figure 4-3 suggests that the tunability is 56.33%. When the thickness of BST increased to 400 nm, the tunability increases to 64.25% with applying a maximum 4V biasing. Figure 4-4 shows this result.

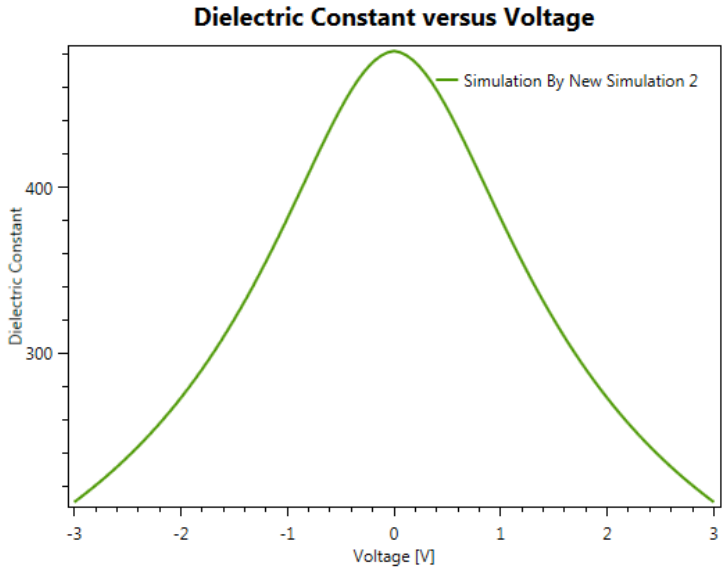


Figure 4-3 The dielectric constant vary from -3V to 3V of BST(7:3)(250nm)-STO(10nm)-GaAs with IDE using Igreja's Model

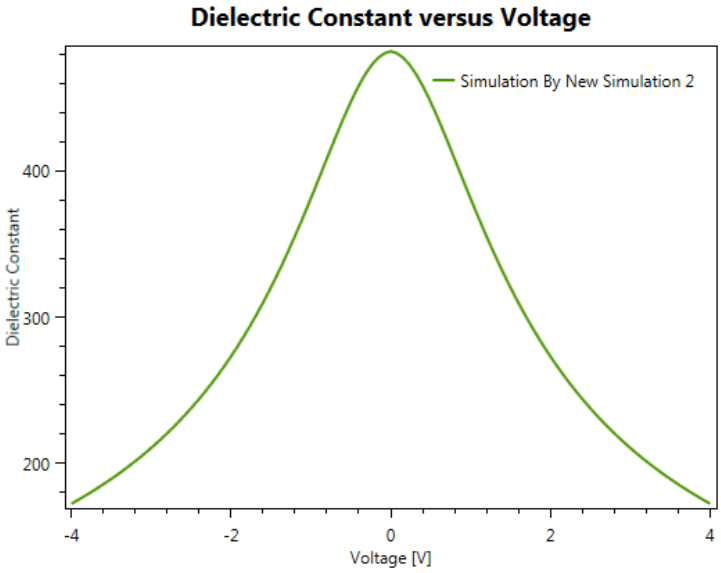


Figure 4-4 The dielectric constant vary from -4V to 4V of BST(7:3)(400nm)-STO(10nm)-GaAs with IDE using Igreja's Model

4.4.2 The simulation when considering distribution in BST

However, in the real IDCs, the distribution of electric field is concentrated in the separation of electrodes instead of the whole layer. Eq. (3.64) should be also used. The parameters in the fabricated samples are 0.68 for 250-nm-BST sample and 0.6 for 400-nm-BST sample, although should be in a range. Also the parameter is about 25840 μm^{-1} for both sample to get reasonable dielectric constant. With these additional information, for the IDC with 250-nm BST, the in-plane tunability is 25.4% at maximum biasing with 3V biasing as shown in Figure 4-5. For the IDC with 400-nm BST, the IDC requires at least 4V biasing to reach 28.5% in-plane tunability as shown in Figure 4-6.

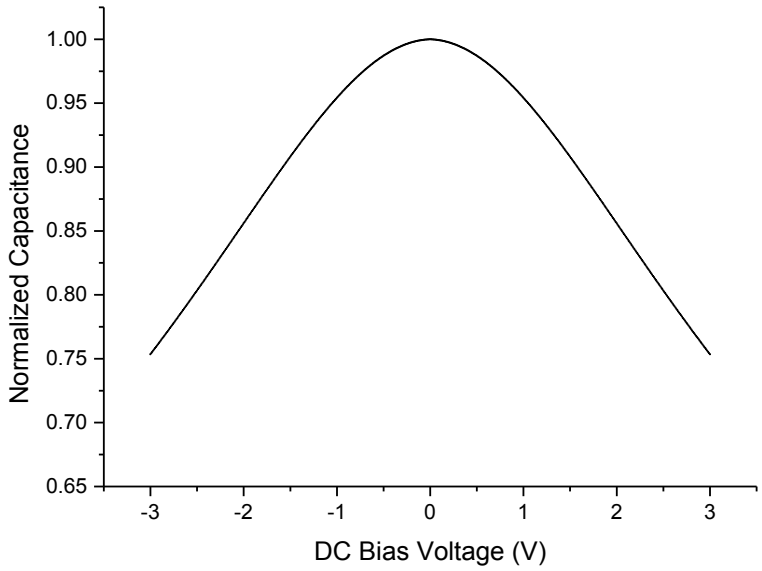


Figure 4-5 The dielectric constant vary from -3V to 3V of BST(7:3)(250nm)-STO(10nm)-GaAs IDC using Igreja's Model with considering electric field distribution in BST layer

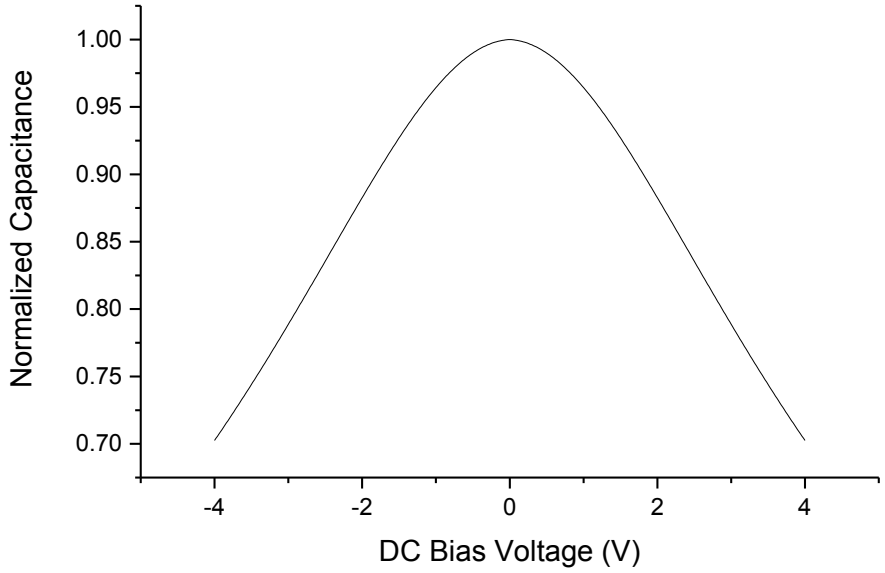


Figure 4-6 The dielectric constant vary from -4V to 4V of BST(7:3)(400nm)-STO(10nm)-GaAs IDC using Igreja's Model with considering electric field distribution in BST layer

In addition to tunability, the FoM and loss tangent of the BST-STO-GaAs heterostructure is majorly determined by the dielectric loss of BST thin film. In simulation with modified model, the result is listed in Table 4-1.

Table 4-1 FoM and loss tangent of the BST-STO-GaAs heterostructure simulated with modified model

BST thickness	FoM simulated with modified model	loss tangent simulated with modified model
250 nm (at maximum biasing with 3V DC)	~450	0.031 to 0.038
400 nm (at maximum biasing with 4V DC)	~500	0.029 to 0.037

Chapter 5 Characterization and comparison with simulation

5.1 Fabrication of BST-based IDCs on GaAs Substrate for Characterization

The IDCs with the same substrates and IDE geometry in simulation for estimating this model were fabricated with layer molecular beam epitaxy. [11, 77] In the literature, various techniques have been employed in the deposition of BST thin films on different substrates, for example, sol-gel deposition [102], pulsed laser deposition[11, 36], chemical vapor deposition [103], RF sputtering [104]. However, there has been a few reports on the deposition of BST thin films on GaAs substrates. In this study, BST thin films are required to be chemically stoichiometric and epitaxially aligned on GaAs substrates. In order to achieve good control of thin film composition and quality, pulsed laser deposition and laser molecular beam epitaxy (laser MBE) are chosen as the main techniques for the deposition of thin films. Basically, the process of fabricating BST films on GaAs substrates was similar as fabricating on oxide substrates in terms of the growth mechanism of thin films and process control. Zhu *et al.* [105] reported that the growth temperature influence the quality on silicon substrates. Similarly, Li *et al.* [106] provided the improvement for growing STO films. Therefore, a short description of the PLD method is given in this section.

The BST-STO-GaAs heterostructure substrates for fabricating IDCs were grown in two stages using laser MBE. First the STO buffer layer was deposited on GaAs substrates. The distance between STO or BST target of evaporation and the GaAs substrate was 5 cm. The GaAs substrates were heated up to 600 ℃ for stabilizing the deposited STO. To

prevent the oxidation of GaAs, the chamber was evacuated to a base pressure of 5×10^{-5} Pa during the STO thin-film deposition. The STO target was irradiated KrF laser beams with a wavelength (λ) of 248nm. Once the STO layer was grown about 5 to 10 nm, the target was switched to BST and the buffered GaAs was further heated up to 650 ℃. Because the STO buffer layer was employed to protect the GaAs substrate; and reduce the oxygen vacancy in grown samples, there was O_2 flowing into the system for maintaining atmosphere at 1 Pa till BST was reached certain thickness. After deposition, the films were then in situ annealed in an ambient of 200 Pa oxygen pressure for 1 hour before being cooled down to room temperature in order to further reduce the oxygen vacancies. Figure 5-1 shows a schematic setup and process of PLD for fabricating BST-STO-GaAs heterostructure.

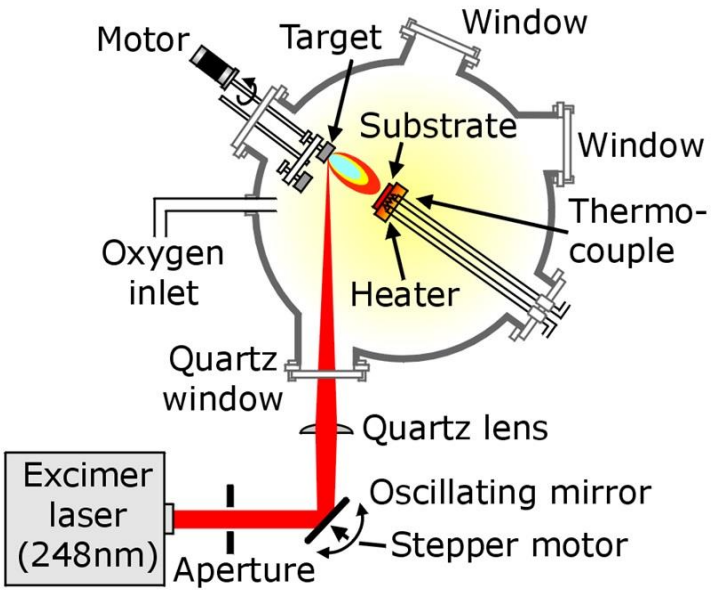


Figure 5-1 Schematic setup (vacuum chamber) of pulsed laser ablation

Once the substrates of IDCs were ready, the electrode can be fabricated on the substrates. The process of fabricating electrodes includes photo-mask design and photo-lithography. The photo-mask design process is shown in Figure 5-2.

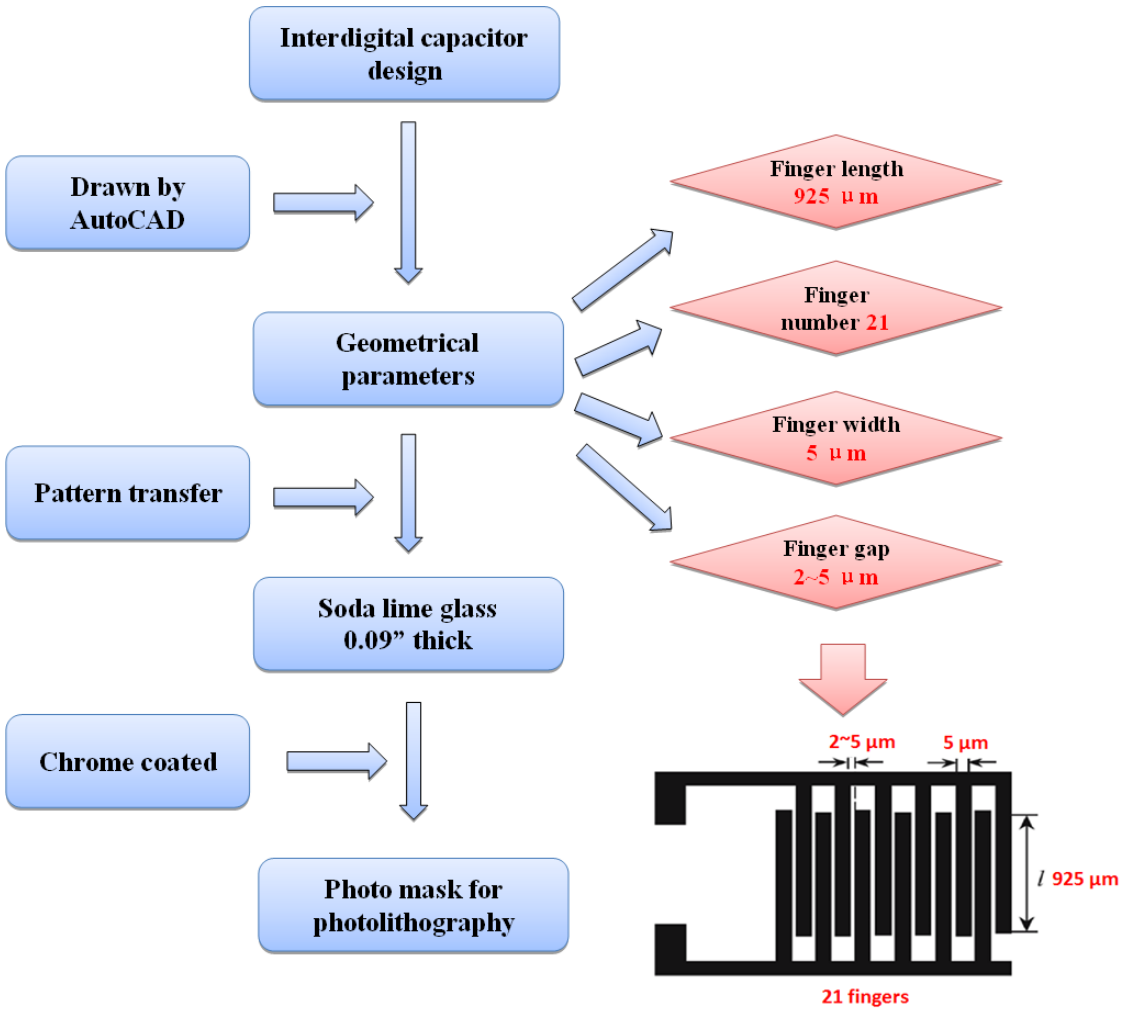


Figure 5-2 The process of making a photo mask for fabricating electrodes

With made photo-mask, the electrodes of IDCs would be fabricated by magnetron sputtering. The conditions of gold sputtering are shown in Figure 5-3. The detail of

photolithography process was also shown in Figure 5-4. It is noticed that the thickness of gold deposited as about 150 nm which is in the same order of the BST thin films.

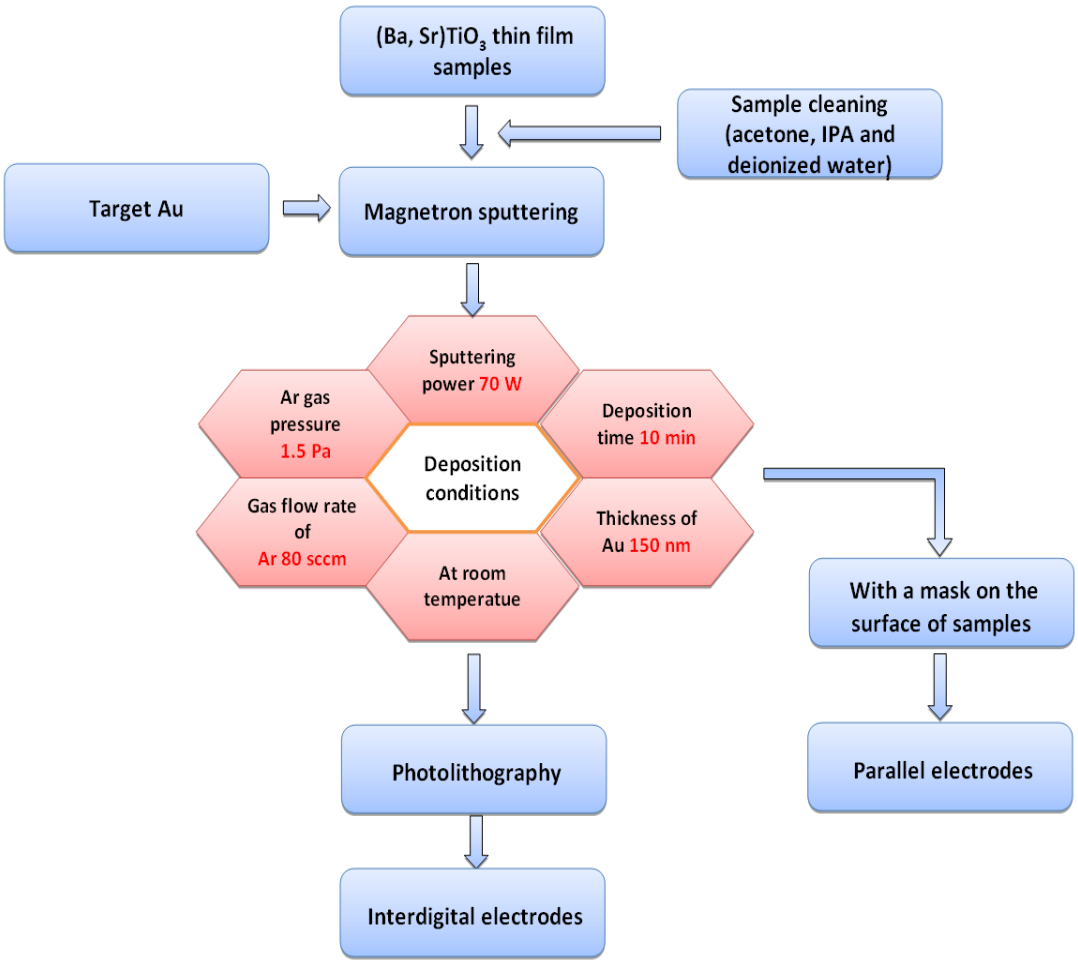


Figure 5-3 The process of electrode fabrication by magnetron sputtering

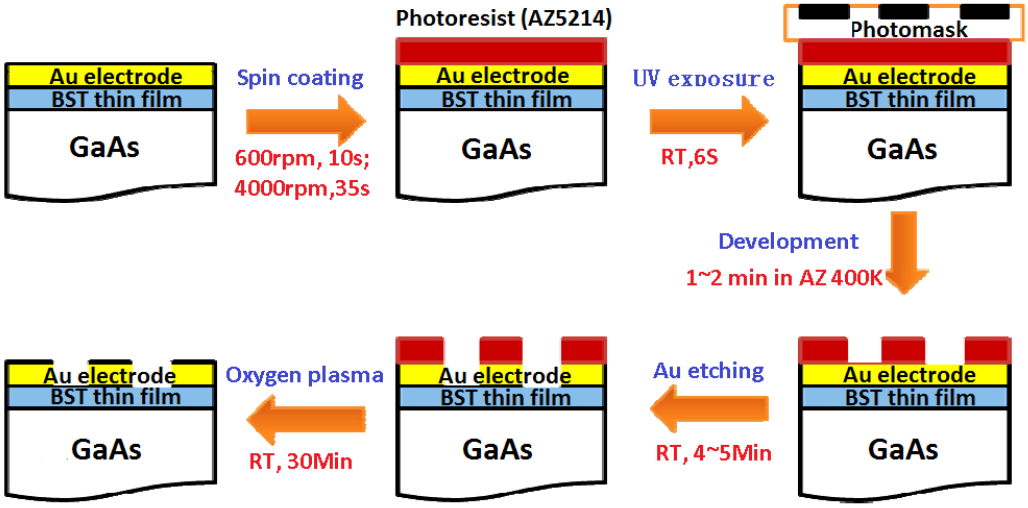
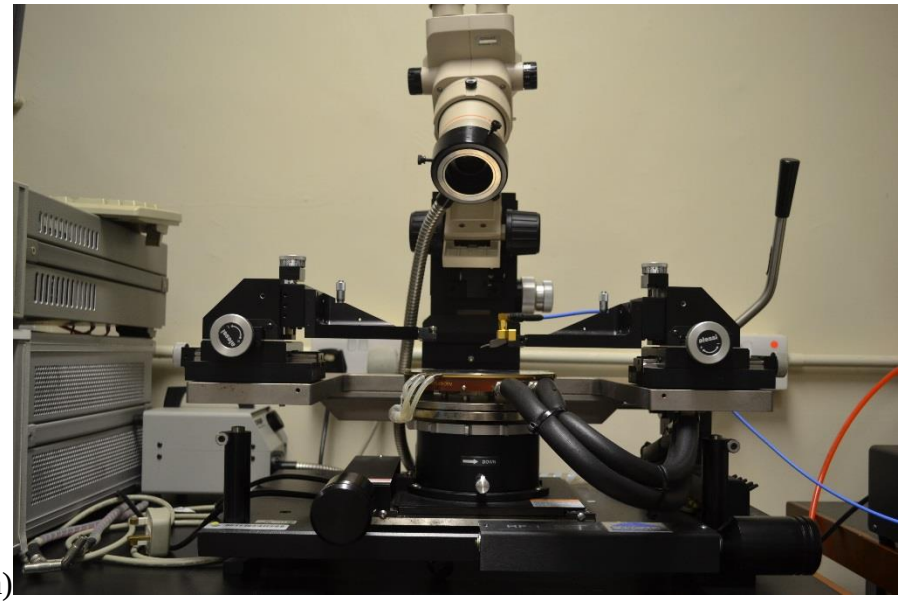


Figure 5-4 The optimized process parameters for photolithography

5.2 Preparation for microwave measurement

Once the IDCs fabricated, they would be investigated by using an Agilent/HP 4291B RF impedance/material analyzer (Figure 5-5 (b)) with an ACP40-GS-100 probe mounted at Cascade probe station Microtech RF-1 (Figure 5-5 (a)). There were several important issues for executing the characterization of the IDCs. Because the IDCs were co-planar structures with gold IDE, the connection of IDCs should be also suitable for these structures. For this purpose, the co-planar Cascade ground-signal (GS) microprobe was used. The tips of the microprobe are made of beryllium copper (BeCu), which are suitable for the use with a gold pad as the contact substrate. After the probe was installed in the station, it is needed to calibrate the planarization to ensure the tips are fully contacted. To reach the planarization of the tips, the testing samples with gold films deposited would be involved. The testing samples were placed under the microscope, the microprobe was moved down to the gold films. Once the tips were in focus in the microprobe, they should probably touch the substrate. Then a slight movement of the probe would leave scratches on the gold films. For truly planarized probes, the scratches should be in parallel and the same depth. Otherwise, the level of the probes should be adjusted by turning the leveling screw until all tips made even contact on the contact substrate.

(a)



(b)

Figure 5-5 (a) Cascade probe station Microtech RF-1
(b) Agilent/HP 4291B RF impedance/material analyzer

After the planarization of the tips was done, the next calibration was the one-port calibration for the impedance analyzer. Because there was parasitic electrical impedance of the probes and connection wires of the measurement system, the measurement result would become unreliable without the one-port calibration in the system. The example

capacitance of IDCs including parasitic electrical impedance as shown in Figure 5-6. There are many resonance peaks with enveloping the capacitance of the IDCs while the signal frequency increased from 1 MHz to 1.8 GHz.

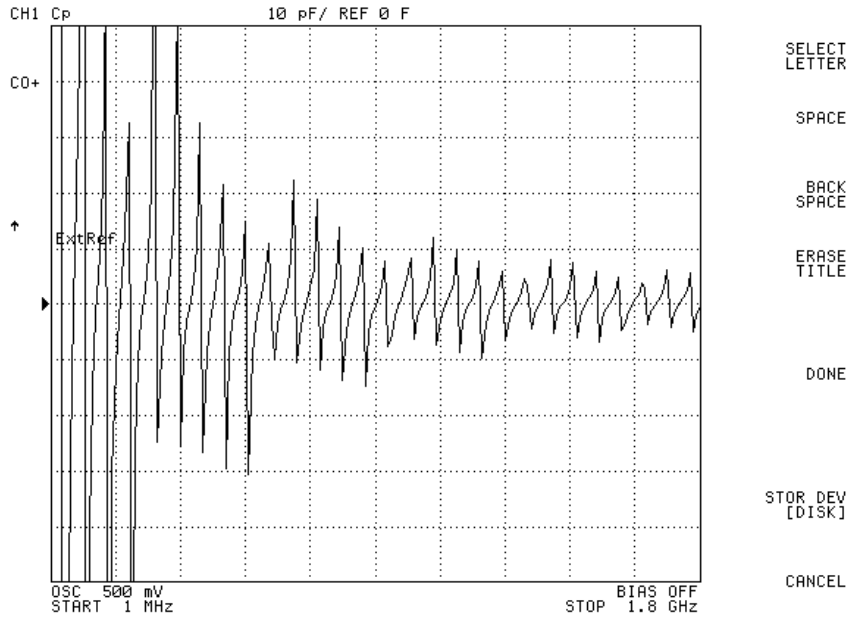


Figure 5-6 the unreliable result due to the measurement without one-port calibration

Thus to do the one-port calibration, the impedance standard substrates (ISS) with "short", "open" and "50 Ω load" standards provided by the probe station manufacturer were used. The impedance analyzer operated stable for around 30 min, these ISS would be used to provide the information of calibration coefficient used in the impedance analyzer. For example, “open” has negative capacitance and “short” and “load” have inductance. After the one-port calibration was done, the IDCs would be placed as the device under test (DUT) at the probe station as shown in Figure 5-7.

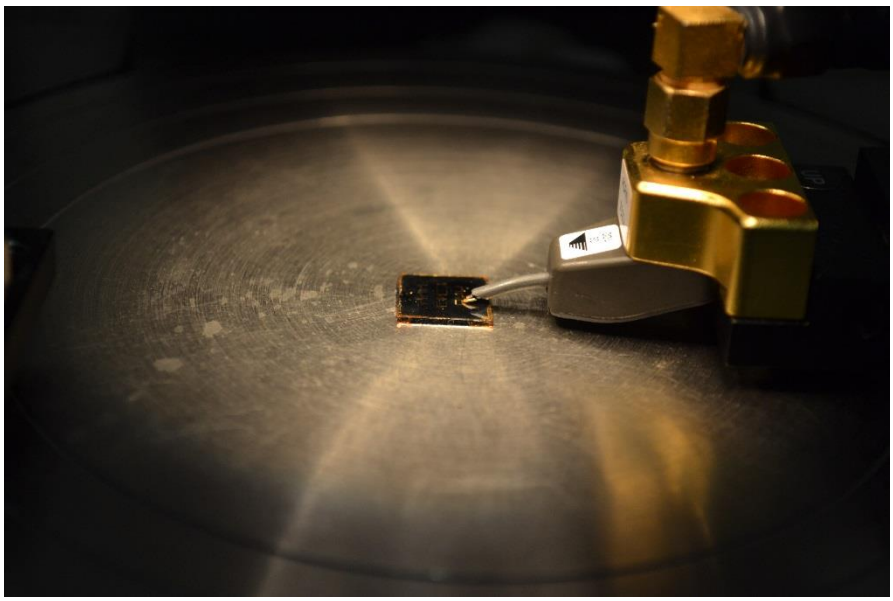


Figure 5-7 The IDCs under testing with ACP40-GS-100 probe

5.3 Results of Microwave Measurement

The measurement of fabricated IDCs would be done in common process. The sinusoidal microwave signal with small amplitude in mV scale was applied to the IDC. The frequency response of IDCs would be investigated by varying the signal frequency from 100 MHz to 1.2 GHz without additional DC voltage shift. The biasing field response of IDCs would be studied by the fixed signal frequency 1 GHz. Meanwhile, the signal was also shifted with certain DC biasing to modify the permittivity of BST. The capacitance and phase shift of IDCs can be read directly from the impedance analyzer and saved to the text files. For the further analysis the behaviors of BST thin films grown on GaAs substrates, the permittivity of BST was calculated thought the capacitance by using the original Gevorgian's Model.

The first set of IDCs is ones with 250-nm $Ba_{0.7}Sr_{0.3}TiO_3$. The dielectric constant of BST thin film deposited on STO-GaAs was plotted as a function of frequency from 100 MHz to 1.8 GHz in Figure 5-8. The dielectric constant almost remained the same value of about 305. While the dielectric constant was plotted as a function of applied bias voltage, the result was shown in Figure 5-9. The maximum permittivity of BST calculated was about 325. The in-plane tunability was 25.4% at maximum biasing with 3 V biasing.

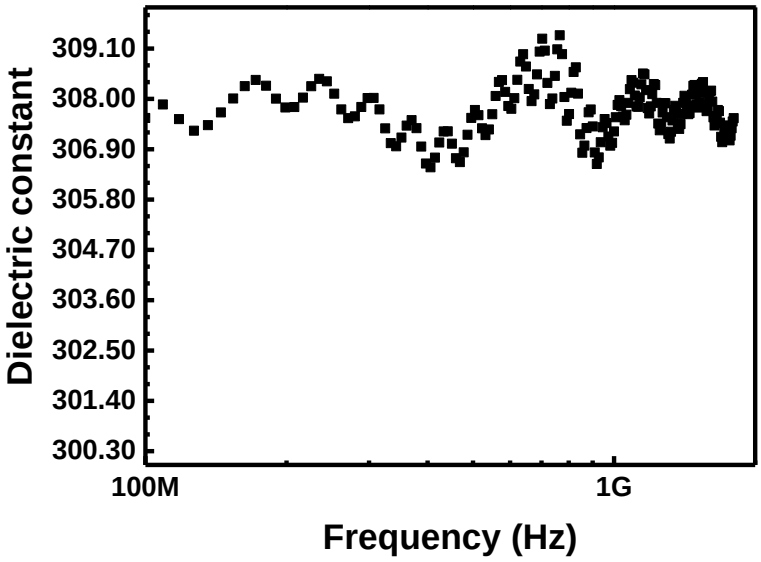


Figure 5-8 **The relationship between the frequency and dielectric constant in 250-nm BST-STO-GaAs substrates**

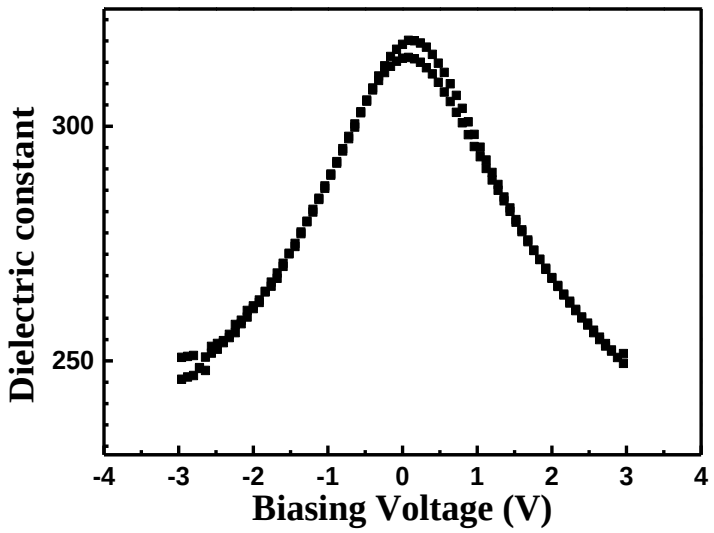


Figure 5-9 **The relation between the bias voltage and dielectric constant in 250-nm BST-STO-GaAs substrates**

The first set of IDCs is ones with 400-nm $Ba_{0.7}Sr_{0.3}TiO_3$. The dielectric constant was plotted as a function of frequency from 100 MHz to 1.8 GHz in Figure 5-10. The dielectric constant decreased dramatically from above 350 to 275. The dielectric constant plotted as a function of applied bias voltage was shown in Figure 5-12. The permittivity of BST was decreased to 318. And this IDC required at least 4V biasing to reach 28.5% in-plane tunability.

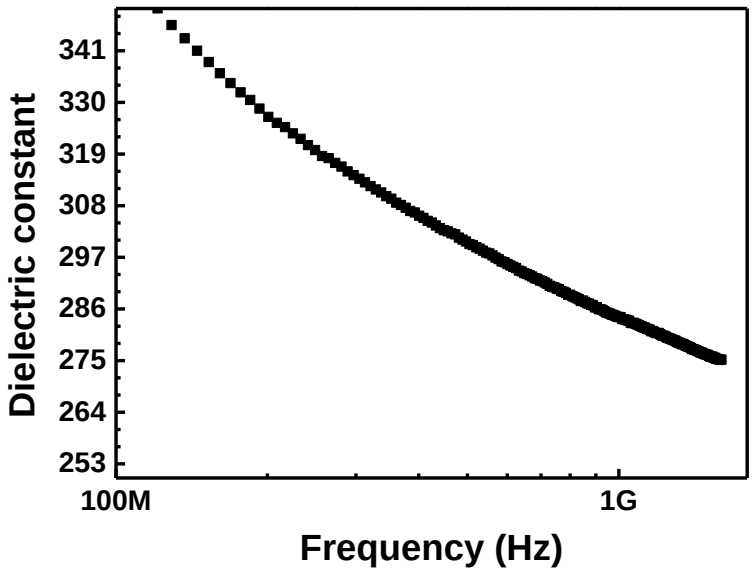


Figure 5-10 The relationship between the frequency and dielectric constant in 400-nm BST-STO-GaAs substrates

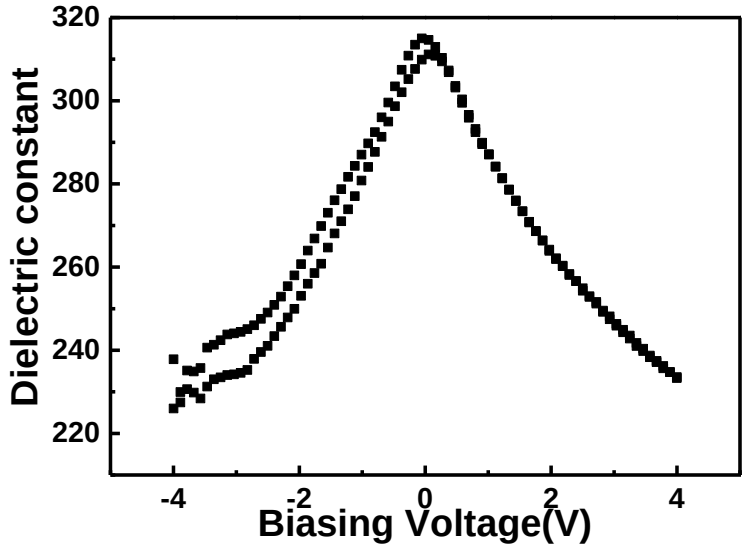


Figure 5-11 The relation between the bias voltage and dielectric constant in 400-nm BST-STO-GaAs substrates

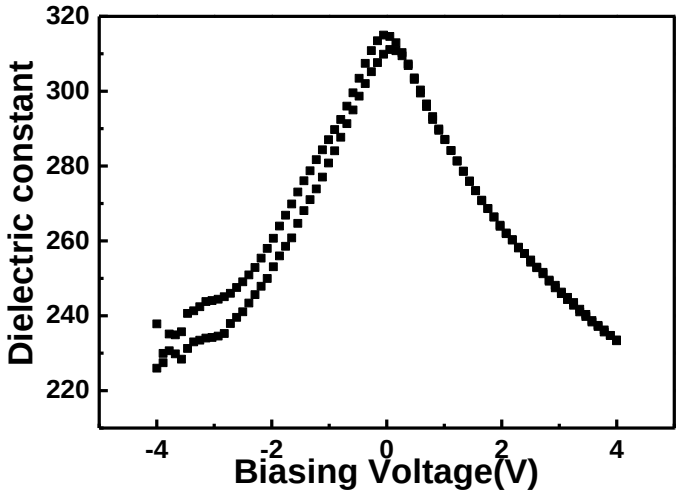


Figure 5-12 The relation between the bias voltage and dielectric constant in 400-nm BST-STO-GaAs substrates

5.4 Summary of the different in simulation and measurement

Table 5-1 shows the major results of simulation with the electric field consideration and experimental measurement of IDCs with BST-STO-GaAs heterostructure substrates. The graphs of normalized capacitance suggest that the trend of biasing field effect in simulations is in almost accordance with the experiment. The maximum tunability of IDCs is larger than experiment under the medium biasing electric field. However, for the very small biasing field, the tunability is less than the experiment. The main reason of this phenomenon may be that the "inhomogeneity field" is the primary effect when the external biasing field is less the certain value.

Table 5-1 Comparison of tunability between measurement and simulation

BST thickness	Tunability in measurement	Tunability simulated with modified model	Tunability simulated with traditional model
250 nm (at maximum biasing with 3V DC)	25.4%	26.98%	56.33%
400 nm (at maximum biasing with 4V DC)	28.5%	28.68%	64.25%

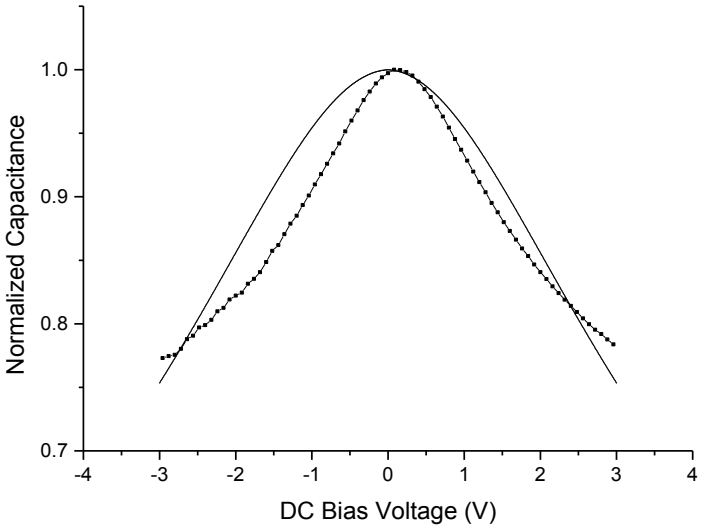


Figure 5-13 comparison of the normalized capacitance of 250-nm BST-STO-GaAs substrates

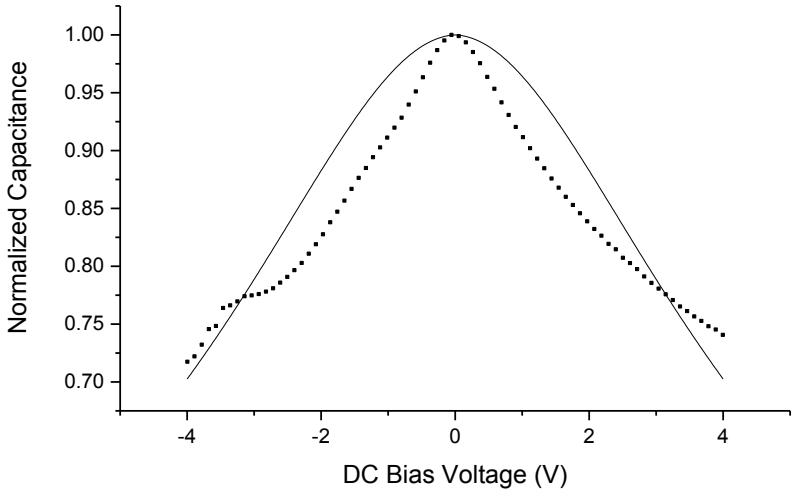


Figure 5-14 comparison of the normalized capacitance of in 400-nm BST-STO-GaAs substrates

Chapter 6 Conclusion and future work suggestion

6.1 Conclusion

This study shows the investigation of interdigital capacitors consisting of $Ba_{0.7}Sr_{0.3}TiO_3$ thin film on STO-buffered GaAs substrates, and provides modification of existing analytical models for general interdigital capacitors. Moreover, a visualized program was created for simplifying the calculation of tunability of interdigital capacitors. Then the integration of perovskite material on GaAs was characterized, demonstrating the potential of integrating perovskite ferroelectrics with III-V semiconductor wafer.

The investigation bases on the properties of BST at its ferroelectric-paraelectric phase transition process. The phase transition is influenced by temperature, biasing field and other factors. These effects change the polarization in BST perovskite lattices and modifies the dielectric properties. The phenomenological model describes the relationship between the properties and factors by introducing free energy with respect to its polarization. The free energy introduced by Landau is a fundamental tool to provide a clear relationship between system state and its principal parameter. The effect of temperature and electric field in BST had been studied separately. Then the expression of free energy and dielectric constant is rewritten into the combination of individual functions of temperature and normalized electric field. The normalized electric field is a key factor in the analytical model of interdigital capacitors. The other factors, including inhomogeneity of BST are reflected thought it.

And following modification of traditional models, such as Gevorgian's and Igreja's models, is the result of altering normalized electric field in BST film when GaAs acts as the substrate. The electric field applied to the BST layer is related to its thickness and the boundary condition of its interfaces. With proven using finite element simulation, the electric field distribution in BST layer is similar to in GaAs layer. Thus, the BST-GaAs interface forms "virtual electrodes". Also, the high mobility of charge carriers in GaAs layer leads to the stronger effect of "leakage currents". The quantitative result of this effect is the interfacial capacitance equivalent to one of co-planar waveguide in even mode.

The simulation in traditional model, Gevorgian's model, for example, shows that the tunabilities of an interdigital capacitor with 250nm and 400 nm BST layer are as high as 56.33% at 3V bias voltage and 64.25% at 4V bias voltage. But the characterization of these capacitors shows their tunabilities are 25.4% and 28.5% respectively. The great difference causes difficulty in designing microwave circuits. The modified model overcomes this issue and giving closer results, 26.98% and 28.68%.

6.2 Future work suggestion

A modified model for BST-based IDCs intergraded in GaAs substrates has been developed in this thesis. However, when this model is extended to other analysis model for different lumped element microwave circuits in the future, the limitation of this model still exists. The major limitation is that the effect of "inhomogeneity field" is not clearly formulated in this work due to the limitation of characterizing the microstructure of BST-STO-GaAs samples. It provides the route of deeper investigation for providing quantitative relationship of different defeats in BST thin films. Also, the FoM and loss tangent of BST-GaAs-based devices are still not the major direct outcomes in previous models.

On the other hand, the properties of BST are studied, though the parallel capacitor sandwiched with BST thin films. Although the interdigital electrodes can be analogue to the parallel capacitor with conformal mapping, it is another method to directly study the performance of co-planar devices such as IDCs. This method is started from directly used the free energy from Eq. (3.2) and the electrical potential Eq.(2.4), with considering the BST-GaAs interface effect by using finite element method. The model of BST-GaAs interface effect is potential topics for developing the devices integrating on GaAs substrates forming monolithic integration microwave circuits.

In the characterization of BST-GaAs-based devices, to have a precise tunable microwave devices in thin film forms is challenging tasks. The importance and repeatability for testing FoM and loss tangent of IDC samples is limited by the accuracy and functions of

Agilent/HP 4291B RF impedance/material analyzer. Reliability of using the experimental results may be questionable. It is believed that this issue can be resolved by using the advanced instrument.

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