INVESTIGATION OF LOAD SIDE POWER CONVERSION FOR HIGH FREQUENCY AC DISTRIBUTION SYSTEMS

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Investigation of Load Side Power Conversion for High Frequency AC Distribution Systems

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Certificate of Originality

I hereby declare that this thesis has been written based on my own work and that, to the best of my knowledge, it reproduces no material previously published or written nor material that has been accepted for the award of any other degree or diploma, except where due acknowledgement has been made in the text.

_____(Signed)

__Xu Cuidong____(Name of student)

To my family

Abstract

Nowadays, power systems have been going through a revolution due to the development of renewable energy and modern electronic systems. The existing power architecture is no longer effective in meeting the competing requirements in the aspects of performance, efficiency and cost. A high frequency alternating current distributed system (HFAC-DS), developed by NASA as an alternative power delivery for space crafts in the 1980s, has recently attracted much attention based on rapid developments in semiconductor technologies. By operating with a high frequency link, the system can be made to be compact and flexible, in order to meet the individual needs of loads/source in the system, speed up response, and reduce noise. It offers an alternative method for high frequency power conversion to variable renewable energy and modern power electronics systems. The high frequency has been embedded on the high frequency transformer link in all the DC-Dc power converters. The proposed work is to examine high frequency AC link for distribution. The objective of this research is to provide a solution to the load side power conversion through investigations of new topologies for the revolutionary HFAC distribution system. Firstly, a topology of resonant step up switched-capacitor-based ac-ac converter is introduced to convert the ac input voltage level to a double ac voltage level. Zero

current switching can be achieved; high current stress can be relieved. The topology also extends the switched-capacitor converter family to another ac-ac application and provides an alternative electronic conversion method to the ac transformer.

A resonant switched-capacitor based step up/down ac-dc power converter with high frequency switching is explored. Step down voltage is achieved in the circuit by simply introducing cascaded stages, which will be much more convenient for integration. Corresponding analysis is derived to verify the performance of the converter, which provides an ac-dc power transfer method.

Then an improved version of resonant switched capacitor step up/down with high frequency switching is proposed. This circuit provides cascaded step up and step down voltage in one circuit. It is easy to have parallel configuration and easy to change the output voltage by inserting or replacing a cascaded step up or step down module. A voltage gain of integer ratio in the style of 2n/m is achieved, with n and m being the cascade stage of step up and step down respectively. The proposed circuit provides a solution of voltage step up/ down for the HFAC distribution system.

For current source conversion, switched-inductor power converters with current conversions 2, 1/2 and -1 have been developed. To reduce the power loss, resonant soft-switching technique is introduced to improve the power conversion efficiency. Small resonant capacitors are paralleled with the switches to achieve zero voltage

switching.

Two families of zero-voltage switching step down switched inductor power converters are presented which can improve the voltage spike issue. They are able to extend to high order step down of 1/2 1/3, 1/4 ….1/n and -1, -1/2, -1/3 … -1/n conversion ratios by using only two switches.

The proposed new concept of switched-inductor current source power converter provides an alternative method to power conversion and is a new concept in topology and resonant technique.

The boundary of maximum storage energy is analyzed to be an alternative to study the instability of the system by bifurcation and chaos of the storage energy. Zero energy is obtained in stable period one and the storage energy with the same value and opposite direction is obtained in period two. These results can provide a new guideline to design a stable system and provide a new control algorithm for power electronic system.

To sum up, this research has accomplished comprehensive analysis and in-depth studies in various aspects, including topological investigation, mathematical modeling, and practical applications of load side power conversion. The research outcomes provide meaningful theoretical findings as well as the feasible application of solutions of power transferring for HFAC distribution system.

List of Publications

[1]. **C. D. Xu,** K. W. E. Cheng, Y. M. Ye, Y. J. Bao, "AC-AC Power Conversion Without Transformers and DC Link and its Family of Circuits" Submitted to_IEEE Jounal of emerging and selected in Power Electronics(JESTPE-2015-07-0254).

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[3]. **C. D. Xu**, K. W. E. Cheng, Y. M. Ye, K. Ding, D. H. Wang , "Cascaded Module Investigation of AC/DC Resonant converter for High Frequency AC Distribution", Energies-91276

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[7]. Y. M. Ye, K.W. E. Cheng, J. F. Liu, and **C. D. Xu**, “Family of Dual-Phase-Combined Zero-Current Switching Switched-Capacitor Converters” IEEE Transactions on Power Electronics, 2014, 29(8), 4209–4218.

[8]. **C.D. Xu**, K.W.E. Cheng, "A survey of distributed power system - AC versus DC distributed power system", 4th International Conference on Power Electronics Systems and Applications, Hong Kong, 8-10th June 2011.

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List of Abbreviations

AC	Alternating Current
AC-DC	Alternating Current to Direct Current
APWM	Asymmetrical pulsewidth-modulated
C	Capacitor
CHB	Cascade H Bridge
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
DPS	Distributed power system
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
FC	Flying capacitor
HF	High Frequency
HFAC	High frequency AC
L	Inductor
NPC	Neutral point clamp
PF	Power factor
PFC	Power factor correction
PWM	Pulse wide modulation

RC	Resistor capacitor
RLC	Resistor inductor and capacitor
RMS	Root mean square
SC	Switched capacitor
SI	Switched inductor
SIPC	Switched inductor power converter
SMPS	Switch mode power supply
SVM	space-vector modulation
THD	Total harmonic distortion
UPQC	Unified Power Quality Conditioner
VRM	Voltage regulator module
YBCO	YBa2Cu3O7
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

List of Symbols

i_L	Inductor current
E_{inj}	The Jth cycle input energy
E_{oj}	The Jth cycle output energy
f_0	Resonant frequency
f_s	Switching frequency
f_l	Line frequency
η	Efficiency
i_{Lr}	Current flowing through resonant inductor
I_{in}	Input current
I_{oj}	The jth cycle output current
I_{p1}	The peak value of the current
I_{p2}	The peak value of the current
jth	The jth cycle
L_r	Resonant inductor
P_o	Output power
P_{loss}	The power of loss
R_{DS}	The on resistance of the Mofet
ω_1	Resonant angular frequency of State 1 in swictehd inductor converters

ω_2	Resonant angular frequency of State 3 in switched inductor converters
ω_o	Resonant angular frequency
S_P	Positive maximum variation of storage energy
S_N	Negative maximum variation of storage energy
T_s	Period of the switching frequency
V_o	output voltage
V_{in}	Input voltage
V_{oj}	The j^{th} cycle's output voltage
V_j	The j^{th} cycle's input voltage
$V_{c\max}$	The maximum value of the capacitor
v_C	The voltage of capacitor
v_x	Resonant voltage of capacitor in State 1 of switched-inductor converters
v_y	Resonant voltage of capacitor in State 3 of switched-inductor converters

Chapter 1

Introduction

1.1 Introduction and Motivation for HFAC-DS

1.1.1 Existing Distributed Power System

Since Westinghouse first used Tesla's poly-phase ac power system to distribute power to both lights and electric machines in 1893, the AC system has already become massive, mature, developed, and standardized. This might be due to its advantage of easy transmission, voltage transformation, flexibility at different loads and low transmission loss. The low frequency (50 Hz or 60 Hz) power distribution has been used for more than a century in utility systems [1]. It is a mature technology and standardized for all power processing units with safety and protection well developed. However, the existing power architectures in power electronic systems are not effective in meeting the competing requirements in performance, efficiency and cost following the new development in modern electronic systems [2]. On the other hand, the demand also affords an alternative solution for a popular DC distributed system and a high frequency alternating current distributed system (HFAC-DS) [3].

It should be noted that the comparison between DC and AC distributed power systems in all aspects is still a hot topic in research area [4-8]. The DC distribution system is

used widely in a large portion of loads, especially in some motors, which accept DC voltage only. The voltage is converted into a DC voltage first, is then passed through a DC-DC conversion, and is supplied to equipment and apparatuses finally. A high frequency switching power signal is generated in the centre of DC-DC conversion. This frequency is usually high, chosen between 20kHz and 1MHz, which depends on the applications, designs and power levels. High frequency transformer is usually used for voltage transformation or isolation. Fig. 1-1 presents a typical DC distribution network, which has a number of well-known advantages as compared to conventional AC distribution. It has been used in distance power transmission because of financial advantages and the solutions in such applications [9]. The DC distribution has been reported to be widely applied in computer networks, general buildings [10], navy shipboard systems [11] and the aerospace environment [12].

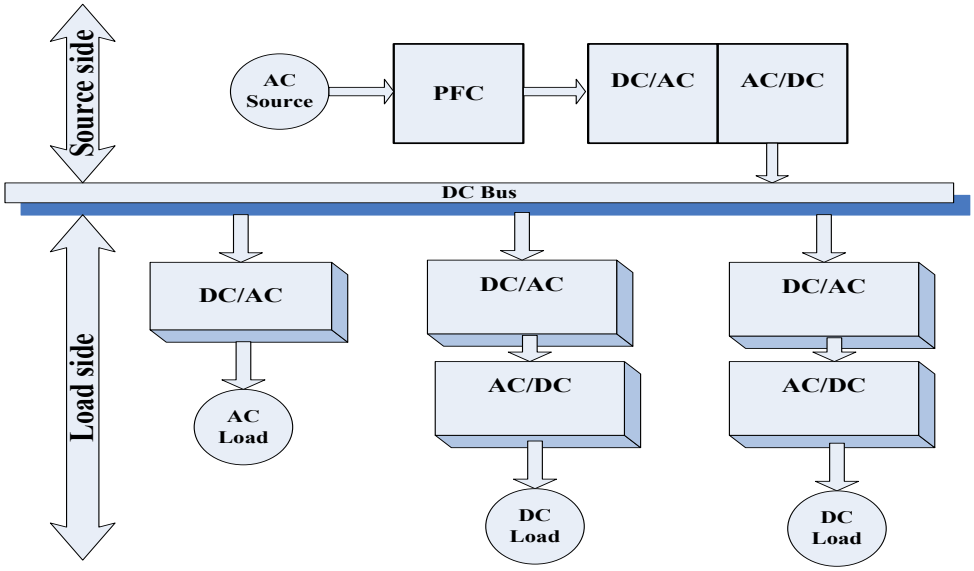


Fig. 1-1 Typical DC distribution power system architecture.

However, some researches [4-8] verified that power systems with fewer number of power conversion stages can improve the efficiency of the whole system. There are some discussions on the replacement of DC distribution with HFAC distribution, especially in micro grid areas [13]. The typical DC distribution architecture is shown in Fig. 1-1, which achieves ideal electrical specifications to meet load demand by five power conversion stages. The DC-DC converter stage consists of an intermediate high frequency AC link. It is obvious that the system can be simplified if AC link is used. Fig 1-2 shows the high frequency AC distribution network. The overall system is now simpler with a lower stage count. Its advantages are lower cost in maintenance and initial investment, potential high efficiency and high reliability.

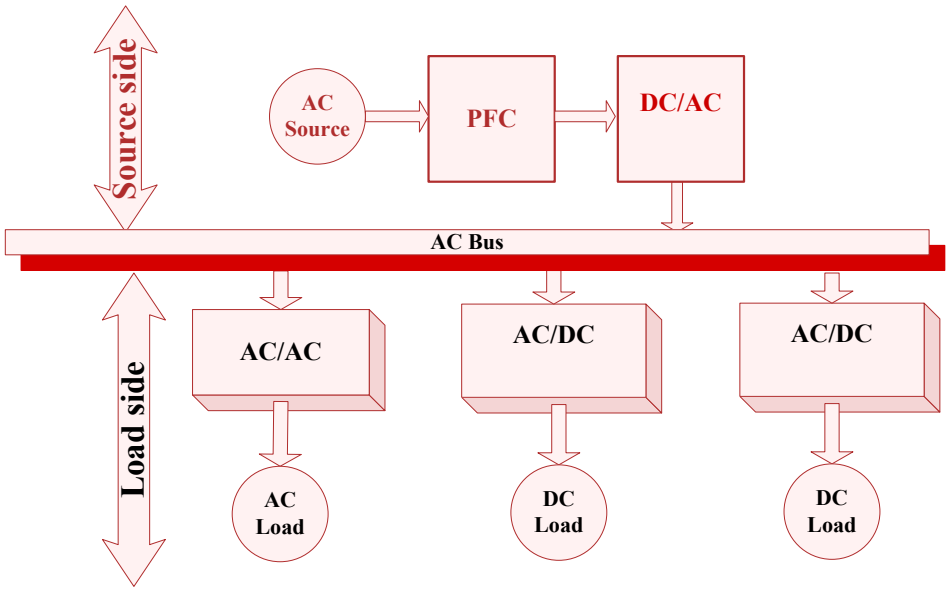


Fig. 1-2 Typical high frequency AC distribution power system architecture.

The comparison among common AC, DC and HFAC distributed power systems indicates that, for most users, it is necessary to change from AC to DC or HFAC on

micro grids when considering efficiency, cost compatibility, reliability and safety [6].

1.1.2 HFAC Distributed Power System

The high frequency AC power distribution, which was firstly developed by NASA as an alternative power delivery for space crafts in the 1980s, was investigated in the late 1900s in avionics and for space stations [14-16]. In most aerospace applications, 400Hz is a standard because of the needs for lightweight applications and is a compromise between high frequency loss and power density [13], but this can be changed now because of the advancement in power electronics. The use of 700Hz, based on YBCO, has also been reported [17]. NASA has considered 20kHz distribution [15] and 20kHz AC power distribution in space stations are reported in [16]. It is obvious that for enclosed systems, power can be directly delivered from the conventional means so long distance transmission can be avoided. High frequency AC distribution has prominent advantages. The high frequency AC current power distribution has been proposed by [18] in telecommunications, which provides a detailed comparison with powering schemes. The comparison between HF AC distribution system and centralized DC/DC conversion indicates that the overall efficiency of the power conversion is greater than centralized DC/DC conversion with a corresponding reduction of the total heat

dissipations, and improves the overall reliability and reduce maintenance required.

There are two important factors which impact AC distribution system design: 1) bus frequency, and 2) bus voltage and current waveform shapes. The bus frequency range can be from 20kHz to around 1MHz, based on the available power conversion technologies and power devices. As the skin-effect increases bus resistance at high-frequencies, past research on AC distribution has been focused on the design of sub-100kHz bus frequency range [19-21]. Reference [22] made an effort to apply 300kHz AC distribution system.

There are reports on the use of high frequency AC distribution for the general public and industry. The AC distribution requires the generation of the high frequency AC. There are discussions on the type of the waveforms used for the high frequency AC link. The typical ones are square wave, sine wave and trapezoidal. In classical switched mode power conversion, generation of square waves is simple and straight forward; however, the harmonic content is high and will affect system loss and stability [2]. The Trapezoidal waveform is a compromise between the square and sinusoidal. It has fewer harmonics than square wave and a special circuit is needed [2]. The sinusoidal waveform has been proposed and developed using APWM [23]. Its main advantage is that its fundamental waveform produces no harmonics, even though complex issues with regards to inverter and load converter circuit designs are involved [24-26].

Because of the poor noise performance and unacceptable EMI in variable frequency distribution, a fixed frequency and voltage become a premise of high frequency system design. Considering the ease of step up and down in AC system, the bus voltage is determined by the requirement of higher distribution efficiencies. Traditionally, the higher distribution voltage with lower distribution current can effectively cut down distribution losses. Hence, the tendency of voltage selection is as high as possible under the considerations of safety requirements, regulatory, and insulation.

There are two significant factors affect the selection of power transmission and distribution for high frequencies system. One is the power losses is increased and the other one is the voltage drop is rising. Line length and frequency increase affect the two factors. When the total length of the distribution line is longer than about 1/10 of wavelength; The transmission model has been considered and more sections has to be adopted to model the line correctly. The distribution distance is determined by tolerable losses at the different operation frequency. meanwhile, the allowable regulation of voltage drop is around 5%. For example, computer and telecom's distribution system's frequency is close to 1MHz due to short range, the frequency of power distribution system in an electric vehicle is 20kHz or so due to moderate range, and the frequency of distribution system for Micro grid is below 1kHz due to long

range, It is noticed that the higher frequencies for the allocation, the lower power rating is employed. In a word, many factors, such as distribution distance, power capacity, count of power converters and load conditions, etc. affect the bus frequency and voltage Therefore, a 50k Hz, 50 V high frequency small scale power distribution system is suitable for home use or EV's low power applications

In the receiving end, the high frequency AC is needed to be converted into DC for many applications. The high frequency power factor correction is not straight forward. General power factor correction based on boost converter is not suitable as the switching frequency is 1000 times higher than the fundamental HFAC disttribution. A series-resonant converter circuit has been proposed [27]. Another important area of development is the parallel operation of the high frequency AC loads [28].

In the load side AC distribution power systems, it usually uses high frequency transformers or bridge rectifiers to achieve AC-AC and AC-DC power conversion. The use of power electronic modules and the associated transformer design using low profile approach has been described [29]. Effective design for high frequency high power transformer of other geometry with low losses has not been reported widely.

Nowadays, the high frequency AC distribution system is utilized in systems that integrate renewable energy sources such as hydro, wind, photovoltaic, diesel, and fuel cells, to form a power system interface defined as "High frequency AC Microgrid" [30].

Related studies, including the application of Unified Power Quality Conditioner (UPQC) [31, 32] and test and evaluation of lighting system in high frequency AC Microgrid [33], have been reported.

High EMI level is one of the main concerns for the high frequency AC distribution system. A general method of analyzing the EMI problem of high frequency AC distribution system has been reported in [34]. EMI noise coupled into CMOS logic circuits by a high frequency AC bus carrying square wave has been studied by [35]. A specific solution should be further investigated for the EMI elimination.

It is clear that the existing research and market have started to consider seriously the high frequency AC distribution power system[27-34]. However, the associated EMC standards, transformer design, power factor correction, waveforms of the distribution, optimized bus structure for high frequency application, modeling, analysis and design of the system, AC-AC direct power conversion, AC-DC and AC-DC-AC conversions have not been explored thoroughly. Power companies also demand accurate measurement of power usage and good EMI measures. The proper design of the measurement of voltage, current and power should therefore also be addressed. Careful examination of the EMI in the AC bus and the associated power conversion stages is an important research topic.

1.1.3 Load Side Power Conversion for HFAC Power System

The load converter is one of the interfacing stages in the DPS. High performance, fast transient and tight voltage regulated converters have been developed to supply specified loads, such as microprocessors, computers, telecommunications, etc. In this case, several techniques have been developed to improve the performance and the characteristics of the load converters.

Traditional rectifier is simply converting AC to DC, which widely uses H-Bridge or Half-Bridge rectifier following PFC and DC/DC converter or only a bulk capacitor, as shown in Fig. 1-1 to achieve the energy conversion. It is wildly in use because it is simple, economic or high power factor, low harmonic and reliable in the past few decades. With the demand in green environment and renewable energy source, the power conversion processing triggered the higher requirement in circuit, AC-DC conversion and optimized use of power devices. Therefore, researchers are devoted in the simplifying and improving the overall system's performance which includes the harmonic elimination [36-44], power factor and efficiency improvement[45-49], multilevel output[50-51], current balancing[52-53] and cost reduction. The methods which improve the input current wave shape can be classified as passive or active.

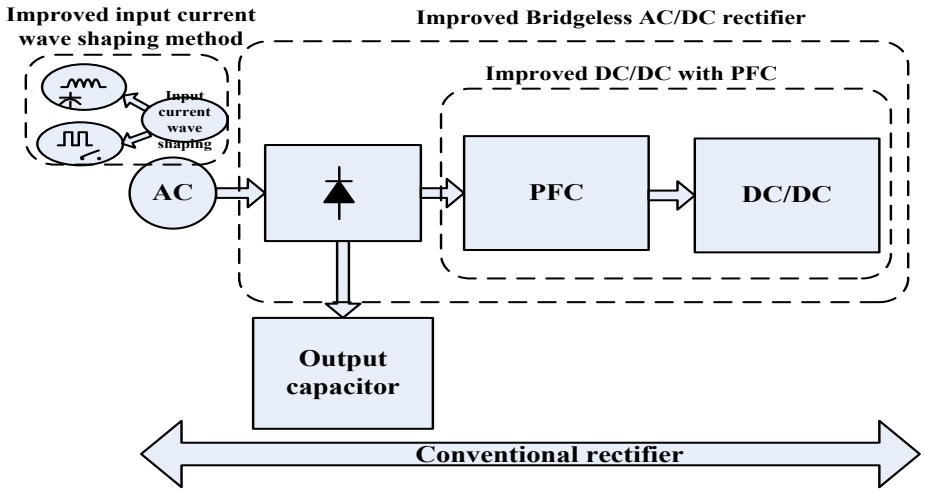


Fig. 1-3 The conventional AC/DC conversion and the improved solutions

The passive input current methods are simple, easy to implement, and reliable which may generate higher EMI and in the past extensive work has devoted to this direction. In [36, 38, 40, 45], one or two inductors and capacitors connected in series or parallel are incorporated in the front or following the bridge to increase input power factor and power density as compared with the conventional diode rectifier without using any controlled power switches, auxiliary power supply, and control boards.

The active switches using for example MOSFET have been developed for PFC solutions. Unity power factor and sinusoidal input current waveform with extremely low harmonic distortion can be achieved. However, the typical topology is a half or full bridge rectifier following with a high frequency switching mode converter that significantly reduces the overall efficiency and reliability and increases the overall costs and EMI, because there are increases in the number of components and the

power is processed twice. In [37, 39, 43, 44, 47], bridgeless ac/dc rectifier have been proposed, which eliminates the diode bridge rectifier and increases the power efficiency because the conversion only consists of one stage.

In order to further improve the performance of the ac/dc converter, multilevel converters are also reviewed in [51-52], which has been applied to multilevel rectifier. In [53-54] double current rectifier is investigated by using soft switching technique which can reduce the power loss of the switches when they are turned on and off. Soft switching technique has been applied to high frequency AC power architecture [55-58]. Using resonant circuit, unity power factor can be achieved.

Interleaving techniques combined with synchronous rectification are capable of reducing the size of the output inductor to make energy transfer much faster. The interleaving approach can reduce the ripple current and also increase the ripple frequency, which enables a reduction in output capacitance, thereby improves the transient response and increases the Voltage Regulator Module (VRM) efficiency. Using integrated magnetic components can reduce the complexity, simplify the circuit and also reduce the flux ripple in the center leg; therefore, core loss can be reduced and overall efficiency can be improved. VRM has also been proposed for high input voltage low output voltage specification, which is a challenge for the converter design. Therefore, a tapped-inductor buck converter [59-62] is proposed to compromise the

small duty ratio using tapping. Besides, an active-clamp coupled buck converter [63] is proposed to improve topology to use a larger duty cycle with a clamped and coupled structure. It is verified that the active-clamp coupled buck VRM demonstrates a better performance in improvement of efficiency. In addition, a further high input 48V is supplied to the load converter. A push-pull forward topology with a modified version with a clamped capacitor is proposed and can improve transient response, reduce profile and increase package density. In this structure, the magnetic components are integrated into a single core. On the other hand, the multichannel interleaving techniques are also expected to apply to the topologies to further improve the power density and transient response [64-66].

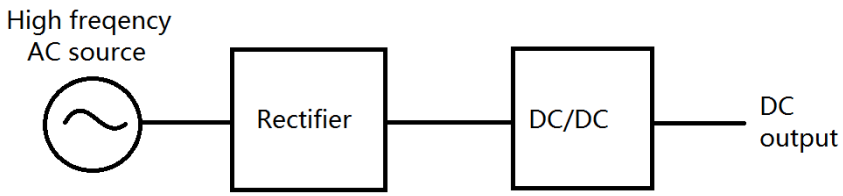
Even though the research work mentioned above provides a fast transient response, some other techniques are still explored because low profile, high efficiency power electronics are in high demand. A resonant network is used to reduce the harmonics and the power loss. Series and parallel resonant networks [24, 67-68] have been used in the circuit to reduce the power loss, increase power efficiency and improve the power factor. In the 1980s, I. Oota, T. Inoue, F. Ueno., and R. Marusarz brought up switched capacitor based AC/DC power converters [69-70]. It has been thoroughly studied by C. K. Tse etc.[71], O. C. Mak etc.[72], A. Ioinovici[73], K.W.E. Cheng[74-77]. On the other hand, a new solution of the voltage regulation based on switched capacitor

AC/DC power converters has developed to improve the power efficiency. This version, namely, transformer-less and rectifier-less AC-DC converters have been proposed in [78-81]. Switched capacitor based power converters have been proposed to replace traditional converters [82-86]. In such circuits, the absence of magnetic elements can highly reduce the size of the device as compared with those conventional switched power converters. To further improve the conversion, a soft switching technique is employed to reduce the EMI, that significantly reduces power loss and increases efficiency and power density [87-89]. Therefore, SC based bridgeless or transformer-less power conversion has become a hot research topic [79-86], which is extremely suitable for the HFAC power distribution system.

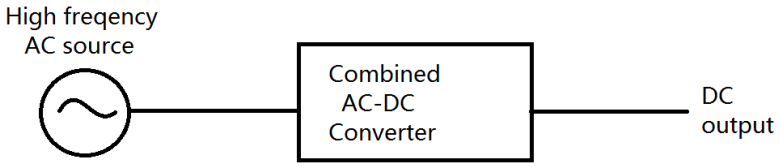
1.2 Rectifier

1.2.1 Research discussion for high frequency AC link

Rectifier, or AC-DC converter, are the front-end converter for the high frequency load side converter. The study could explore the separate cascade of a rectifier and a DC-DC converter, or a combined version of AC-DC converter. The study in the field has been explored and discussed in the previous section. The combined version will be discussed using a switched-capacitor based system that has both rectifier and DC conversion characteristics in the chapters 3 and 4. Fig 1-4 shows two possible topologies of the connection.



(a) Separate rectifier and DC/DC converter

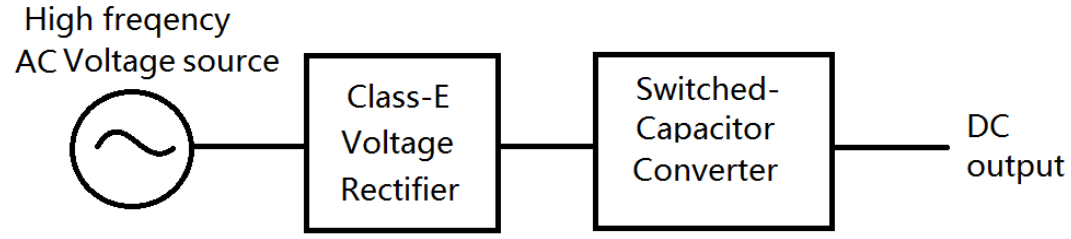


(b) Combined circuit for AC-DC converter

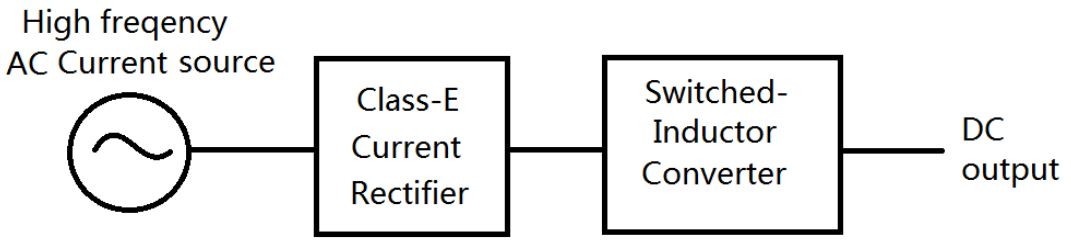
Fig. 1-4 AC-DC high frequency converter topologies

For high frequency AC distribution, the rectifier can be made simple because the filter capacitor can be reduced in size as it basically depends on the input frequency. The alternative version is the Class-E rectifier that has been a hot topic 20 years ago. It is of low harmonic in the AC side and therefore it is most suitable for the proposed system under high frequency AC distribution. The voltage mode of AC-DC rectifier can be configured by cascade connection of AC-DC Class-E rectifier [90-91] and a switched-capacitor voltage converter [71-77] and both of them have been reported extensively in the past. As induction motors turn at a speed proportional to frequency, so a high frequency power supply allows more power to be obtained for the same motor volume and mass. That can be realized by the current source power converter, which will be described in chapters 5 and 6. It will be used to Fig 1-5 shows the two possible topologies under the topic of high frequency AC-DC converters. They are basically a

cascade of rectifier and DC-DC converter. The study in this research will concentrate on the class-E current mode rectifier and the current mode switched-inductor DC-DC converter as shown in the topologies of Fig 1-5b. Current mode source is a popular energy source such as photovoltaic system. Fig 1-5a is a voltage mode conversion and is a built up research field and is not explored in this research work. In Fig 1-5b, the rectifier can also be simple bridge rectifier, but its pulsation voltage is not favorable and of low power factor and high low order harmonics.



(a) Cascaded of Class-E voltage rectifier with switched-capacitor converter



(b) Cascaded of Class-E current rectifier with switched-inductor converter

Fig. 1-5 Rectifier cascaded with switched-passive component converter topologies

1.2.2 Class-E rectifier for current mode

The well-known class-E has been actively researched over years. It can be applied for AC-DC rectifier with low harmonics in the output side. It is originated from a Class E amplifier [91], and the former work has been done on the AC voltage source. For the current source, a duality method can be used to apply to transfer The Class-E voltage mode into a current mode. Similarly, the voltage mode switched-capacitor converter can also be changed into a switched-inductor converter. Fig 1-6 shows a current mode Class-E rectifier. It is drawn by computer simulation software Saber. The circuit is then simulated under a current source of 20A and 50kHz. The resonant

components are designed using the same frequency as the input source. The output current sink is a 0.5Ω load with a large inductor 1mH as the filter. Fug 1-7 shows the simulated waveforms of single phase.The input waveforms are of low harmonics and the overall size of the rectifier is small because the high frequency AC distribution allows the use of small passive components. This section is to confirm the use of high frequency rectifier with a DC-DC converter will facilitate an AC-DC converter system under a high frequency AC distribution.

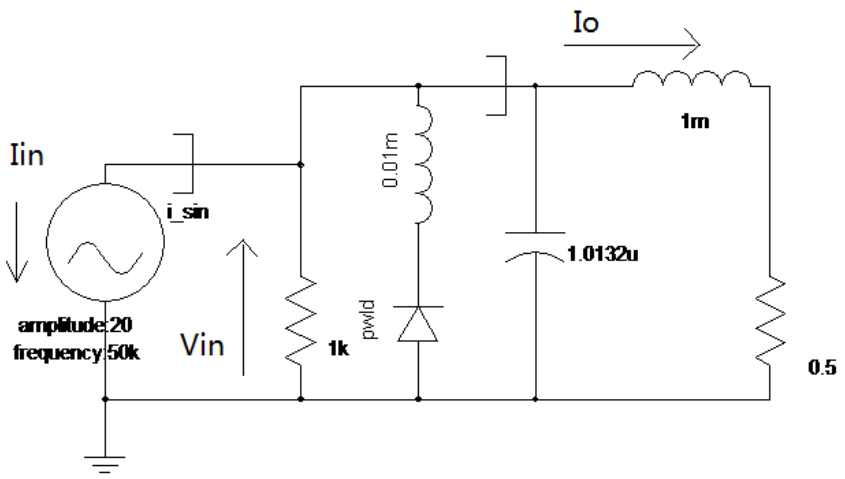


Fig 1-6 Schematic diagram of the Class-E rectifier under current mode

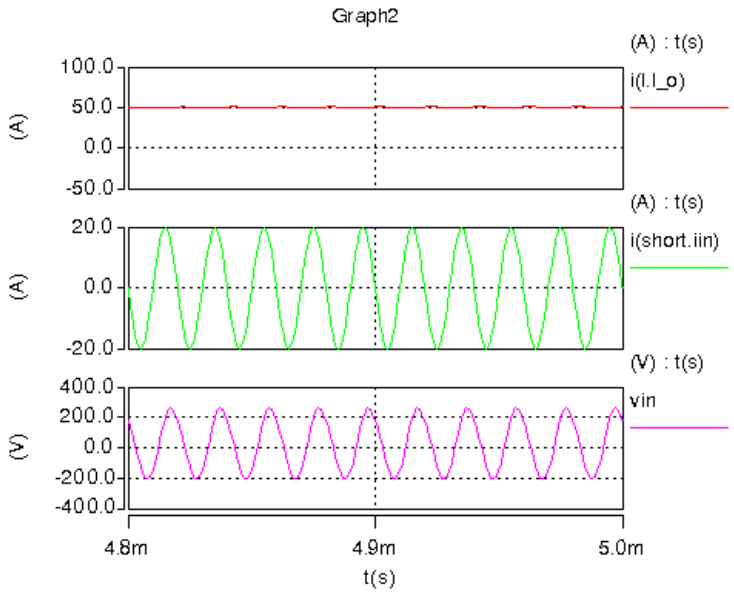


Fig 1-7 The simulated waveforms of the Class-E rectifier

(Top: output current Io, Mid: Input current from the source, Bottom: Input voltage)

1.3 Research Objectives and Methodology

1.3.1 Research Objectives

A. key issues and problems in the current system

The existing AC distribution has been used for hundred years. However, as the power demand and load dynamics are increased, the low frequency power source is not able to adapt current need. The following issues are the main problem:

(a) The passive components including transformer, inductor and capacitor are too large under 50-60Hz mains. The material cost is high compared to high frequency system and not environment friendly.

(b) The power electronic converter is needed to connect to the mains for DC output.

The DC distribution requires many components and not economic. The DC converter or AC/DC converter has an internal high frequency AC. This is duplicated and wastes the materials.

(c) The dynamic performance of low frequency is also low. Under power interruption or voltage dip, it needs long period or long cycle to recover. In high frequency AC, a few cycles only refers to fraction of ms.

(d) The low frequency AC mains does not catch up with the high frequency industry in last 20 years. All computing processor speed, communication devices, other power conversion has increased the processing or operational speed by several to 100 times and the existing AC distribution has not done anything. The research in high frequency distribution line prepares for the possible reduction in high frequency material cost and advancement in the future.

(e) The overall high frequency AC system design is unclear. No extensive research has been studied including the stability, protection, power conversion, systemic modeling, EMI elimination and equipment.

B. Significance of HFAC PDS:

1） The use of high frequency AC distribution decreases the materials cost and increases dynamic performance.

2） It has a significant impact to all distribution systems. It will change all the

front-end converter of all electric loads and reduce the size and cost.

3） It is a revolution of the global power distribution. It is expected that the materials cost will be reduced by at least 30% and power units and the efficiency can be increased by 10%.

4） The devices and power converters' life will be extended.

5） The maintenance and cost will be significally reduced.

C. In this thesis, the main objectives are the investigation on load side high frequency power conversion, so as to obtain a stable power conversion of load side power conversion for the HFAC power distribution system.

The research will examine the existing power conversion topologies for HFAC-DS. A study on SC based step up/ down power conversion topologies will be conducted. An improved soft-switching method to reduce the high charging and discharging current pressure, which also reduces the EMI, will be investigated.

To sum up, the research is expected to achieve the following objectives:

a) The first is to introduce a low cost, high efficiency, reliable solution for AC load. The conventional power transfer method is firstly converted AC power into DC power using AC-DC power converter. This method requires a front-ended converter for power factor correction and an inverter for AC power conversion. It is expected that a new AC-AC topology that directly converts AC power to AC power

can be developed and compared with the traditional power conversion method.

b) The second is to develop an AC-DC power conversion for the DC output load of the HFAC distribution system. The conventional AC-DC converter uses a bridge rectifier and DC-DC converter to achieve the power transferring. No bridge AC-DC is being investigated and new topologies are expected to be developed and analyzed to provide power conversion for DC load.

c) The third is to develop a solution of AC-DC rectifier, which is of high efficiency, low harmonic, and has multilevel outputs. Traditional AC-DC rectifier cannot satisfy the requirement of high power, high efficiency and multiple output for high frequency. Especially the switching frequency will be much higher than traditional PFC. A simple, high efficiency and reliable, multiple output rectifier will be studied.

d) The forth is to present a family of zero-voltage switching step up/down switched inductor power converters which can improve the voltage spike issue. They are able to extend to high order step down of 1/2 1/3, 1/4 ….1/n and -1, -1/2, -1/3 … -1/n conversion ratios by using only two switches to step down the input current.

e) Finally the overall system is discussed for the stability. The switched inductor is fundamental stable but the switched-mode converter is not. The study makes use of classical state-space analysis [79] and bifurcation [69] to obtain the boundary of

stability and an energy modelling is then used.

1.3.2 Methodology

The methodology employed includes modelling, simulation, and analytical analysis. Experimental examination is used to verify the performance of the proposed circuit. These techniques are described below.

a) Modelling and simulation is used to obtain a better understanding of the operation of power electronic circuits for HFAC-DS. The main purpose is to observe the performance characteristics of the power circuit modules, such as the current rise time, the power capability or the voltage/current strain on the circuit elements. Also, modelling and simulation have also been applied to gain an insight into the potential efficiency of the module.

b) The tool used to conduct the modelling and simulation is the proprietary Mathworks environment, namely MATLAB, Simulink, Sable and PSIM 9.0. Specifically, the electrical circuits presented throughout this study have been building upon the components within the Simulink SimPowerSystems toolbox and PSIM 9.0.

c) The technique employed to suppress the EMI is soft-switching; as the frequency of AC link is high, the use of soft-switching with quasi-resonance, zero-voltage switching and extended-period resonance is examined [68]. Conventional

zero-voltage and zero-current switching was used to suppress the EMI for the power conversion circuit.

1.4 Thesis Outline

The main subjects of this research are to develop a reliable, high efficiency and low cost solution to the load side power conversion. Analysis and experiment are conducted to verify the performance of the proposed solutions. The organization of this thesis is briefly introduced as follows:

In Chapter 1, a simple introduction and motivation for the HFAC power distribution system is shown. A review of recent studies is carried out, in a system-level approach to determine the viability of the HFAC bus in replacing the present AC and DC systems. The aim of this chapter is to highlight the advantages of HFAC power and provide a theoretical basis to the following studies.

In Chapter 2, a novel topology of step up switched-capacitor-based AC-AC converter is introduced to convert ac input voltage level to a double AC voltage level. Incorporating the merit of the traditional AC-AC converter, the main attraction of the topology is its simple design and wide availabilities of components. There is no bulky magnetic component; therefore, it is of low cost, small size and more commercially viable. An improved version is also constructed by introducing a small resonant inductor or making use of a parasitic inductance. The proposed topology realizes the

zero current switching and reduces high EMI that originated from high charging and discharging currents for the voltage difference of the switching capacitors, and improves the efficiency of the circuit. Due to the merit of the topology, the circuit is easy to fabricate and integrate. Simulation verifies the theory of the topology, and experimental results agree well with the simulation. The topology extends the switched-capacitor converter family to another AC-AC application for voltage inversion and voltage halved and provides an alternative electronic conversion method to AC transformer.

In Chapter 3, a switched capacitor based step up/down AC-DC power converter with high frequency feed is proposed. In this chapter, a step down structure is studied in detail. The operational principle of the circuits and the design considerations are described. The main advantage of the circuit is that the voltage and current stresses of most components are smaller than those of conventional converters. By using a buffer capacitor to store energy, there are no magnetic energy storage elements in the circuits. Weight and size are highly reduced due to high frequency power line introduced that is emulated by a signal generator and a high frequency amplifier. Step down voltage can be achieved in the circuit by simply introducing cascaded stages, which will be much more convenient for packaging and fabrication. Zero current switching is achieved by introducing small resonant inductors. Therefore, higher efficiency and power density

can be achieved. The performance of the converter has been demonstrated by an experiment with a 50 kHz 50V power source which is emulated by a signal generator and high frequency amplifier to prove the concept.

In Chapter 4, an improved version of the bridgeless resonant switched capacitor based ac-dc power converter with high supply frequency is proposed. The circuit provides cascade step up and step down voltage in one circuit by inserting step up/down modules. It is easy to maintain by replacing a faulty module. The module comprises only capacitors and diodes which makes integration much more achievable. It is easy to be paralleled to change the output voltage stages or provide multiple output voltages. The proposed circuit contains a voltage multiplier in series with a step down converter. The voltage gain of 2n/m is achieved, in which n and m are the number of cascade stages of step up and step down, n, m is 1, 2, 3, 4….. Resonant inductors are introduced to reduce the current spike and achieve zero current switching. Therefore, high efficiency and high power density can be achieved. The operation principle of the circuits is described in detail. In order to demonstrate the performance of the converter, an experiment is carried out in the end.

In Chapter 5, further development on the basic switched-inductor converters with current conversion 2, 1/2 and -1 is derived by duality principle between switched-inductor power converter and the conventional switched–capacitor. To

reduce the power loss, resonant soft-switching technique is introduced to improve the power conversion efficiency. Small capacitors are paralleled with the switches to achieve zero voltage switching. The operation principle and conversion method have been illustrated in detail. Simulation and experiment have been conducted and agree well with theory. The proposed new concept of switched-inductor current source power converter provides an alternative method to power conversion and is a new concept in topology and resonant technique.

In Chapter 6 Current stress is the main concern in the conventional switched capacitor power converter because the capacitor is shorted to be charged without series resistance. While voltage stress is also high to have to be eliminated in the switched-inductor power converter when the inductor is *shorted* to be charged up and released. In this chapter, two families of zero-voltage switching step down switched inductor power converters are presented which can improve the voltage spike issue. They are able to extend to high order step down of 1/2 1/3, 1/4 ….1/n and -1, -1/2, -1/3 … -1/n conversion ratios by using only two switches. Principle of operations, computer simulation and experimental results of the proposed circuits are presented. The experimental results agree well with the simulation. The measured efficiency is high and all the switches are working under zero voltage switching. The proposed new concept of switched-inductor current source power converter could provide an

alternative method to power conversion.

In Chapter 7, the storage energy of high frequency reactive component for switched mode power converter is a new factor to assess the performance. The instability of the switched-mode converter under the peak current control mode is examined for its storage energy. Bifurcation and chaos of the storage energy in the inductor and capacitor are observed based on the stroboscopic map. The boundary of maximum storage energy is given to be an alternative to study the instability of the system in this chapter. Zero energy is obtained in stable period one and the storage energy with the same value and opposite direction is obtained in period two. Simulation results of bifurcation and chaos of energy are obtained under different parameters. The boundary of instability of energy stored in reactive component under various parameters is formulated and a single equation can be used to indicate the factors. These results can provide a new guideline to design a stable system and provide a new control algorithm for power electronic system.

Finally, Chapter 8 presents the conclusions of the present investigation and includes recommendations for further work. These contributions include development of the solution of load side power conversion for HFAC-DS, which has been verified by the experiment result.

Overall the thesis concentrates on the development of switched-capacitor and switched-inductor converters om high frequency load side application. Interesting topologies are developed.

Chapter 2

An AC-AC Convertor Topology for Step Up Operation Based on High Frequency Resonant Switched-capacitor Method

2.1 Introduction

The DC-DC converter is one of the research main streams in power electronic conversion. On the other hand, the AC-AC converter still plays an important role in the power supply research area, especially when AC load or distribution is needed. In the last few decades, high frequency AC distribution systems have drawn much attention, and a new concept of AC-AC converter has emerged to suit the market[77,78]. Moreover, light weight, small size and high efficiency are still the main concerns of the power supply design.

The switched-capacitor converter has gained enormous attention in the last two decades, because it has few components, is easy to be fabricated and creates high power density. Referring to prior research [71, 72], the switched capacitor was used to replace the inductor or the transformer as an intermediate energy storage component, which dominates the weight and size of the circuit; hence, IC chip fabrication could be realized and magnetic component cost was reduced. However, the main drawback

of the circuit is high current spikes when the capacitor is charged or discharged which results in high EMI and hard switching power loss. In reference [92], the researchers used two parallel switched-capacitor cells to improve input current waveform by making it constant and continuous. This method reserves the traditional switched capacitor's advantage; meanwhile, it reduces the EMI and improves the operational performance of the converter. However, the switching devices still operate on hard switching which introduces much power loss under high frequency. In references [74, 76, 81, 93], soft switching technique was applied to the switched-capacitor converter [75, 77, 94] to allow softer turning on and off of the switching devices when the current reached zero, which reduced the power in switching loss and improved the performance of the converter. Nowadays, the switched capacitor is widely used in low power applications, especially in telecommunications, handheld and portable consumer products such as cell phones, digital cameras, MP3 players and PDAs [95], electric vehicles [96], and onboard computer power distribution systems [97]. The High power high efficiency switched-capacitor converter applied to a wide area [98] by applying a peak current limitation control.

The Switched-capacitor (SC) based ac-ac converter was first put forward by F. Ueno in [99] in 1993. Later, a new SC AC-AC converter was proposed and proved to be useful for electroluminescent lamps [100] in 1995. Meanwhile, the investigation of

the SC converter was extended to a wide research area, which included the rectifier-inverter types [101-102]. Recently, more researchers have been devoted to the SC converter to AC power field [103-106]. The performance of the SC converter, such as the predetermined conversion ratio, the output voltage ripple, the output voltage regulating ability and the small power, have been greatly improved. However, the structures of the proposed converter are mostly rectifier-inverter types or power transfers in cascade of AC to DC then to AC [97]. In this chapter, a converter is proposed that makes use of SC concept to achieve power transfer from AC to AC directly without any DC link. The efficiency of the converter is high as it operates under soft-switching. The circuit is under the soft switching technique. That reduces the high EMI problem, due to the charging and discharging current spikes as usually seen in classical circuit, by introducing a small resonant inductor.

The circuit topology and system operation are described in detail. Its four operation states and the relationships of resonant current, voltage and output current are analyzed in this chapter. It provides the basis for the design of the circuits. The simulation and experiment of non-resonant and resonant conversion circuits are completed to verify the circuit performance.

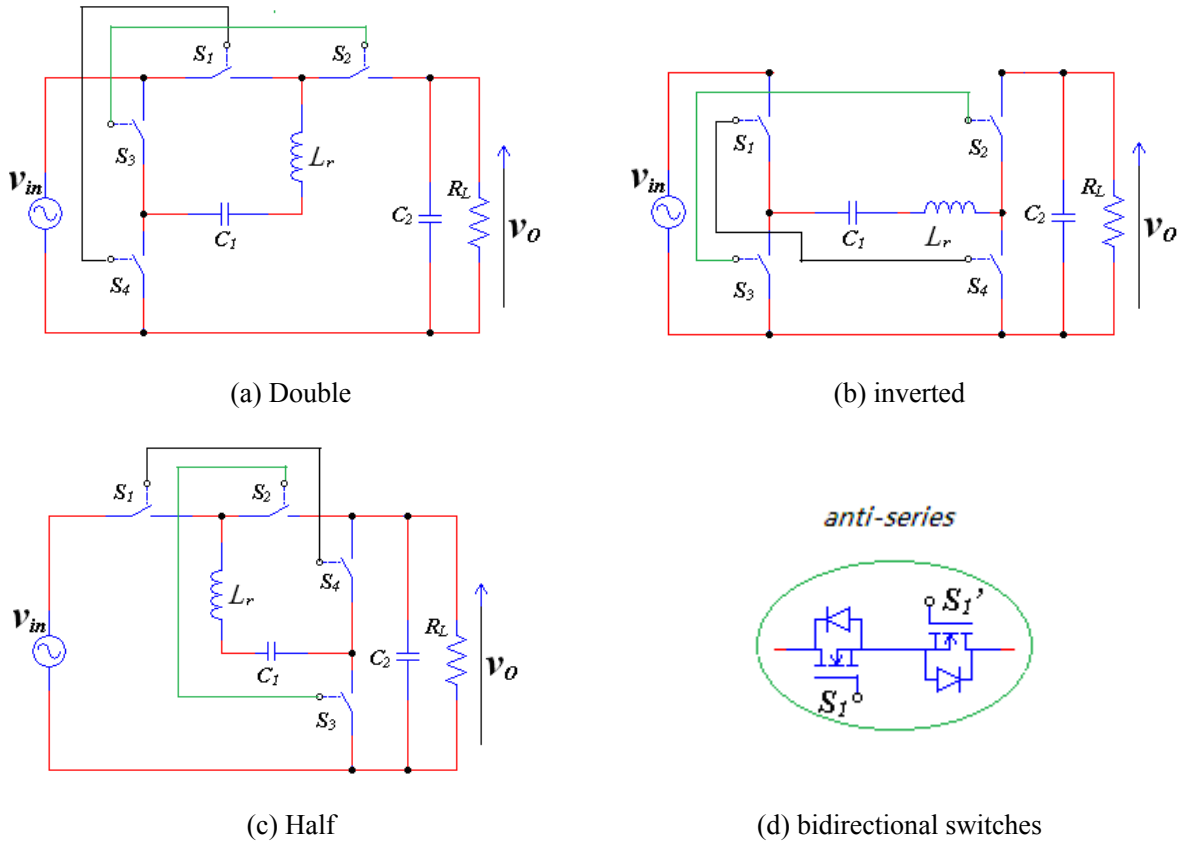
2.2 The Structure and Operation Principle of the Proposed Converter

The family of the proposed circuit is shown in Fig 2-1. All the switches are bi-directional switches which are realized with discrete unidirectional semiconductor devices variously arranged to allow AC input as shown in Fig. 2-1(d). Fig 2-1(a) is the circuit which will be examined in this chapter. Fig. 2-1(b) is the inverted version which provides 180° phase inversion. Fig 2-1(c) is the half version which converts the input voltage to 50%. The concept can be easily applied to other extensions including the higher order step down [8-9], step up [23], summation and subtraction of two sources [24] and multiple inputs [25-26]. The discussion starts with the double mode SC AC-AC converter. The operational principle of the proposed circuit without a resonant circuit is shown in Fig. 2-2.

As shown in Fig 2-2, C_1 is the intermediate energy storage capacitor, C_2 is the output capacitor.

The switches S_1, S_2, S_3 and S_4 are actually four sets of bidirectional switches of S_1 and S_1', S_2 and S_2', S_3 and S_3', S_4 and S_4' shown in Fig 2-1(d) , which allow AC input and also prevent the short circuit by the body diodes of S_3 and S_4 when the system operates in the negative half cycle of the source. These trigger signals are simple and alternatively turn on and off the switches, which transfer energy from the power source to loads.

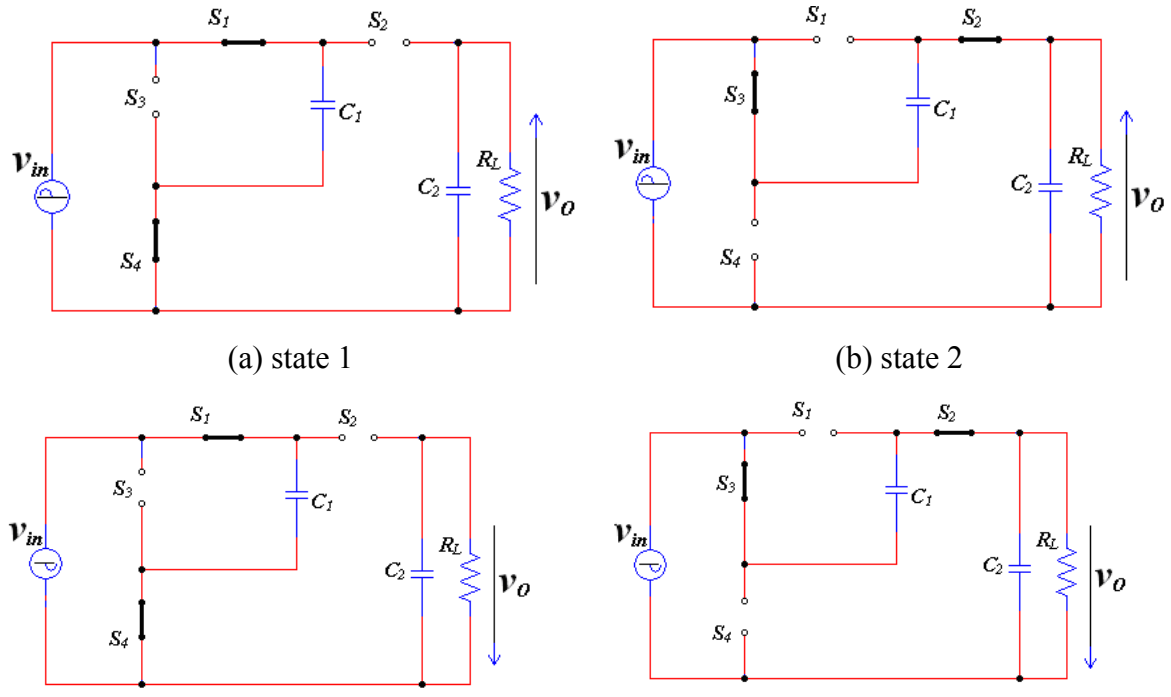
There are four working states. Two states are for positive cycle and two are for negative cycle of the input AC sine wave. Fig. 2-2 (a) and (b) show the working states when the circuit operates in the positive half cycle of the source; Fig. 2-2(c) and (d) are the working states when the circuit operates in the negative half cycle. In the operation state 1, S_1 and S_4 are turned on, and S_2 and S_3 are turned off. The current flows through S_1, C_1, and S_4, and forms a closed loop with v_{in} ($=V_{in}\sin\omega t$). Energy is transferred from the power source and stored in the capacitor C_1. In State 2, S_2 and S_3 are turned on, and $S_1$and S_4 are turned off. The current flows through S_3, C_1, S_2, and C_2 to form a closed loop with v_{in} ($=V_{in}\sin\omega t$). C_1 is connected in series with $V_{in}\sin\omega t$ and delivers total energy to C_2, so the voltage on capacitor C_2 is $2V_{in}\sin\omega t$. Meanwhile, energy is transferred from the power supply and the capacitor C_1 to the load, therefore, the output voltage is double of the input voltage. These trigger signals alternately turn on and off the switches, which transfer energy from the power source to loads. Fig. 2-2 (c) and (d) show the working states when the power supply is providing the negative half cycle.



(a) Double (b) inverted

(c) Half (d) bidirectional switches

Fig.2-1 The family of proposed ac-ac switched capacitor power converter and switches



(a) state 1 (b) state 2

(c) state 3 (d) state 4

Fig. 2-2 Operational states of the ac-ac step-up switched capacitor power converter without resonant inductor

2.3 The System Circuits Performance and case study

The AC-AC converter is considered as DC-DC converter in each switching cycle, since the switching frequency is much higher than the line frequency. In each cycle, the output current I_{oj} is considered constant, the output voltage V_{oj} is the average of output voltage of v_{c2} with j being the j^{th} switching cycle. In order to study the topology in detail, the circuit is studied in three cases:

Case 1: There is a parasitic resistance in series with capacitor C_1.

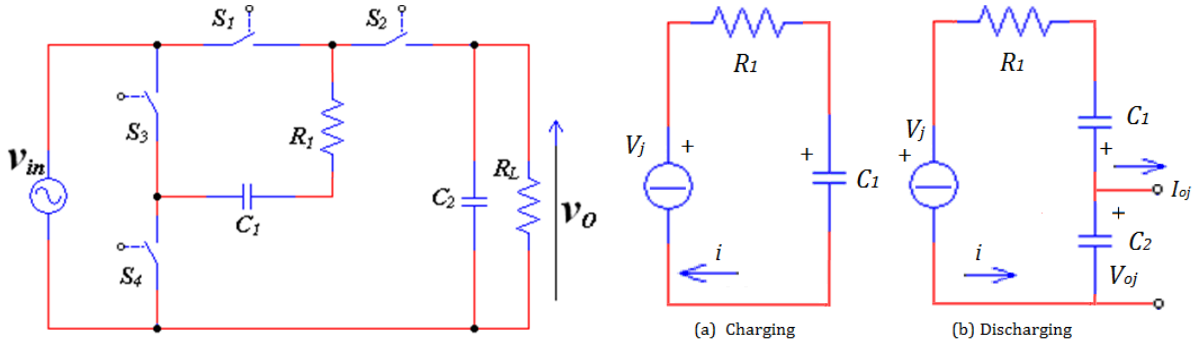
Case 2: Resonant inductor is introduced, in order to reduce the switching loss, and EMI. All components are ideal.

Case 3: A parasitic resistance of component is considered. A resonant inductor is introduced. Therefore, it forms an RLC tank when capacitor C_1 is charging and discharging

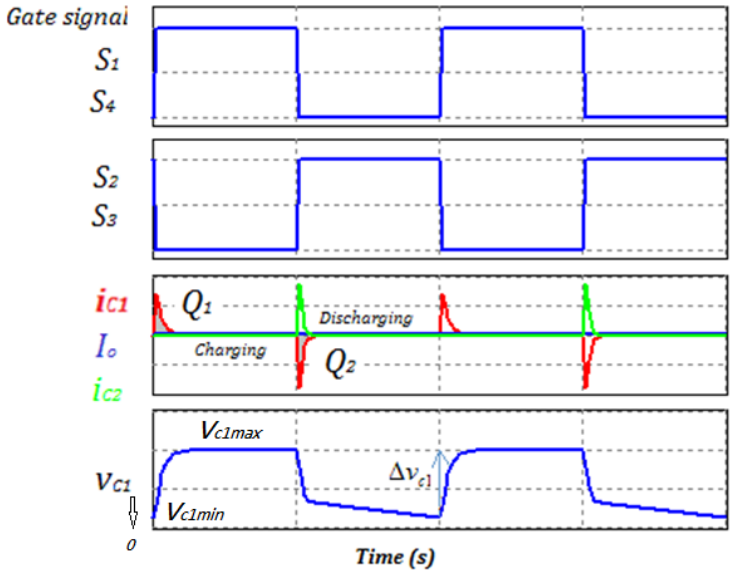
The circuit analysis is based on steady-state. The input voltage v_{in} is $V_{in}\sin\omega t$, the switching frequency f_s is 100 kHz.and is much higher than the line frequency f_l . Therefore the power source voltage is about constant in the switching period T_s. Since the circuit is working similar in negative half wave, the analysis only focuses on positive half wave, and is illustrated as follows.

2.3.1 Case 1: RC equivalent

When the circuit is working in the positive half wave, the switches $S_{1\&}$ S_4 and S_2 & S_3 are turned on and off alternately. When S_1 S_4 are turned on, voltage source is charging the capacitor C_1; when S_2 S_3 are turned on, both voltage source and capacitor C_1 are charging the capacitor C_2. Then the capacitor C_1 is in the discharging state. The circuit, equivalent circuit and the waveform of the variables are shown in Fig. 2-3.



(a) Proposed circuit with ideal component (b) equivalent circuits



(c) waveforms of the circuit in steady state.

Fig. 2-3. The circuit system, equivalent circuit system and the waveforms of the circuit

As it is shown in Fig. 2-3 (b), when switch S_1 and S_4 are turned on, the capacitor C_1 is

charging up, then the state equations are:

$$v_{C1} + R_1 i = V_j \quad (V_j = V_{in} \sin j\omega T) \tag{2-1}$$

$$i = C_1 \frac{dv_{C1}}{dt} \tag{2-2}$$

Then

$$v_{C1} = V_j - (V_j - V_{c\min}) e^{-\frac{t}{R_1 C_1}} \quad (0 < t \le T_s / 2) \tag{2-3}$$

$$i_L = \frac{V_j - V_{c\min}}{R_1} e^{-\frac{t}{R_1 C_1}} (0 < t \le T_s / 2) \tag{2-4}$$

when switches S_2 and S_3 are turned on, the capacitor C_1 is discharging, then the state equations are:

$$V_j + v_{C1} + Ri = V_{Oj} \tag{2-5}$$

$$i = C_1 \frac{dv_{C1}}{dt} \tag{2-6}$$

Then:

$$v_{C1} = V_{Oj} - V_j - (V_{Oj} - V_j - V_{c\max}) e^{-\frac{t}{R_1 C_1}} \quad (T_s / 2 < t \le T_s) \tag{2-7}$$

$$i_L = -\frac{V_{Oj} - V_j - V_{c\max}}{R_1} e^{-\frac{t}{R_1 C_1}} \quad (T_s / 2 < t \le T_s) \tag{2-8}$$

Based on the charge conservation theory, the charge going in and out of capacitor C_1 is equal, as shown in Fig. 2-3(c). Then :

$$Q_1 = \int_0^{T_s/2} \frac{V_j - V_{c\min}}{R_1} e^{-\frac{t}{R_1 C_1}} dt \tag{2-9}$$

$$Q_2 = \int_{T_s/2}^{T_s} -\frac{V_{Oj} - V_j - V_{c\max}}{R_1} e^{-\frac{t}{R_1 C_1}} dt \tag{2-10}$$

$$Q_1 = Q_2 = \Delta V_{C1} C_1 = I_{oj} T_S \tag{2-11}$$

$$\Delta V_{C1} = (V_{c\max} - V_{c\min}) = \frac{I_{oj} T_S}{C_1} \tag{2-12}$$

Then the following equation can be achieved

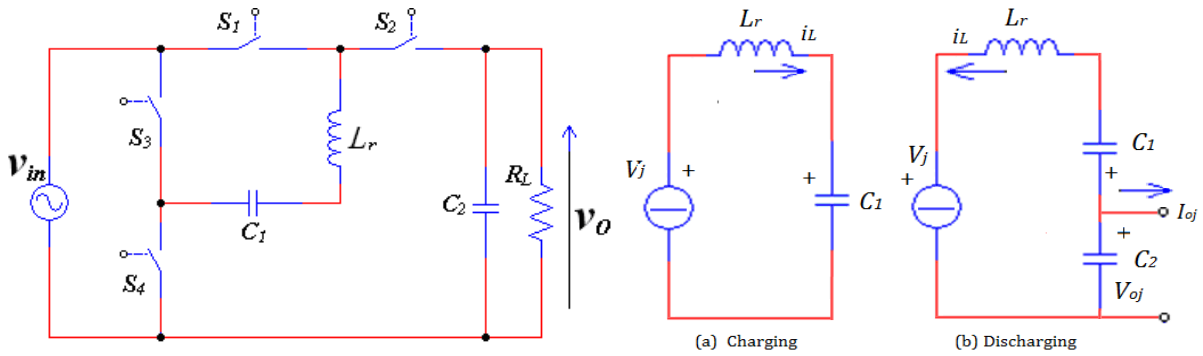
$$V_{Oj} = 2V_j - 2\left(\frac{1}{e^{\frac{T_s}{2R_1C_1}} - 1}\right)\frac{I_{oj} T_S}{C_1} \tag{2-13}$$

Then the voltage conversion ratio is

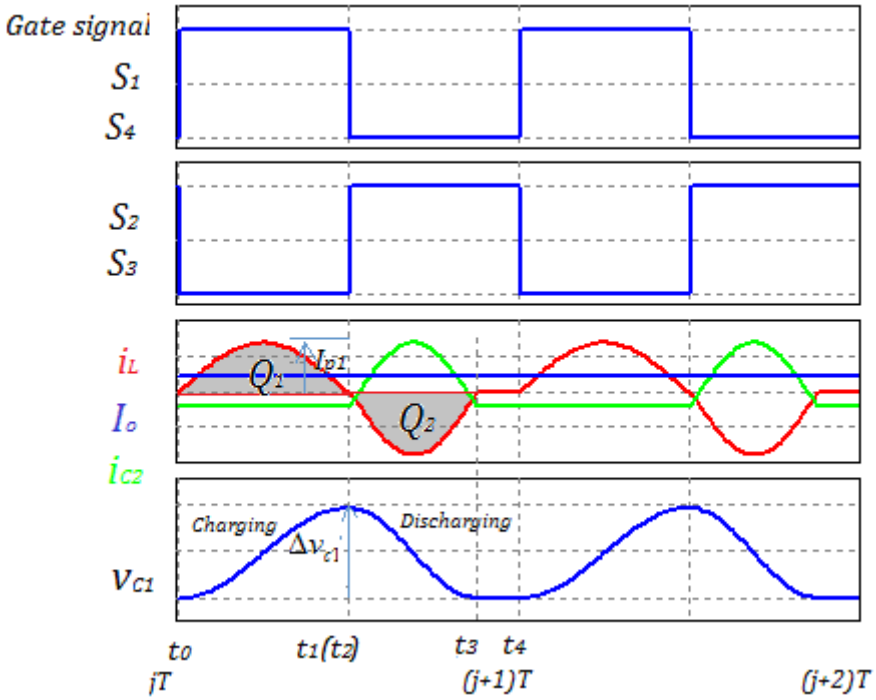
$$M = \frac{V_{oj}}{V_j} = 2 - 2\left(\frac{1}{e^{\frac{T_s}{2R_1C_1}} - 1}\right)\frac{I_{oj} T_S}{C_1 V_j} \tag{2-14}$$

2.3.2 Case 2: LC equivalent

To improve the high frequency circuit and component switching performance of the above circuit, a small inductor is introduced and connected in series with C_1 as shown in Fig. 2-4. The small inductor L_r and C_1 are connected in series to form a resonant tank with a resonant frequency $f_O = 1/(2\pi\sqrt{L_r C_1})$. When the switch is turned on, energy is steadily transferred from the power source to capacitor, and the current gradually increases from zero. When the switching frequency $f_S \le f_O$, the current reaches zero before the switch is turned off. Therefore, the switches can be turned-on and off under zero current condition. The equivalent circuit is shown in Fig. 2-4 (b).



(a) Proposed circuit with resonant inductor (b) equivalent circuits



(c) waveforms of the circuit in steady state.

Fig. 2-4. The circuit system, equivalent circuit system and the waveforms of the circuit

As it is shown in Fig. 2-4 (b), when switches S_1 and S_4 are turned on, the capacitor C_1 is charging up, then the state equations are:

$$L_r \frac{di_L}{dt} + v_{C1} = V_j \quad (V_j = V_{in} \sin j\omega T) \tag{2-15}$$

$$i_L = C_1 \frac{dv_{C1}}{dt} \tag{2-16}$$

Then, the solutions are

$$v_{C1} = V_j - I_{p1} Z \cos \omega_0 t \tag{2-17}$$

$$i_L = I_{p1} \sin \omega_0 t \tag{2-18}$$

where, $\omega_0 = \frac{1}{\sqrt{L_r C_1}}$, $Z = \sqrt{\frac{L_r}{C_1}}$, $0 < t < T_0 / 2$ and $T_o=1/f_o$.

I_{p1} is the amplitude of the resonant current, after half a resonant cycle, the resonant stops at t_2, which is the same instance t_1 when the resonant frequency is equal to switching frequency, the current will fall to zero and the voltage of capacitor C_1 will remain the maximum value when it is at t_2 till half switching cycle. Then there are formulas

$$v_{C1} = V_j + I_{p1} Z \tag{2-19}$$

$$i_L = 0 \tag{2-20}$$

In this case, the resonant cycle is equal to switching cycle during the capacitor C_1 is charging up.

As it is shown in Fig. 2-4 (b), when switches S_2 and S_3 are turned on, the capacitor C_1 is discharging, then the state equations are:

$$V_j + v_{C1} + L_r \frac{di_L}{dt} = V_{Oj} \tag{2-21}$$

$$i_L = C_1 \frac{dv_{C1}}{dt} \tag{2-22}$$

Then, the solutions are:

$$v_{C1} = V_j + I_{p2} Z \cos \omega_0 (t - t_2) \tag{2-23}$$

$$i_L = -I_{p2} \sin \omega_0 (t - t_2) \tag{2-24}$$

I_{p2} is the amplitude of the resonant current during the capacitor discharging, after half a resonant cycle, the resonance stops at t_3, the current will fall to zero and the voltage of capacitor C_1 will remain the maximum value until the end of half switching cycle. Then:

$$v_{C1} = V_j + I_{p2} Z \tag{2-25}$$

$$i_L = 0 \tag{2-26}$$

When the system reaches to the steady state, charge going in and out of C_1 is the same and equal to the charge releasing to the load, as shown in Fig. 2-4(c), which can be described as equation (11). then

$$I_{p1} = I_{p2} = \frac{Q_1 \pi}{T_0} = \frac{\pi I_{oj} T_s}{T_0} \tag{2-27}$$

Where, the two half resonant periods T_0 and T_{01} are equal when C_2 is much larger than C_1.

Then the voltage conversion ratio can be derived by the following formulas based on the energy conservation theory

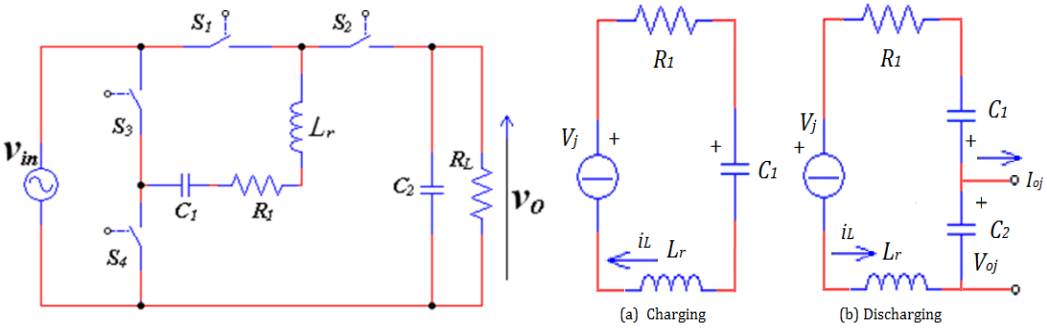
$$E_{inj} = 2V_j I_{0j} = E_{oj} = V_{oj} I_{0j} \tag{2-28}$$

Then

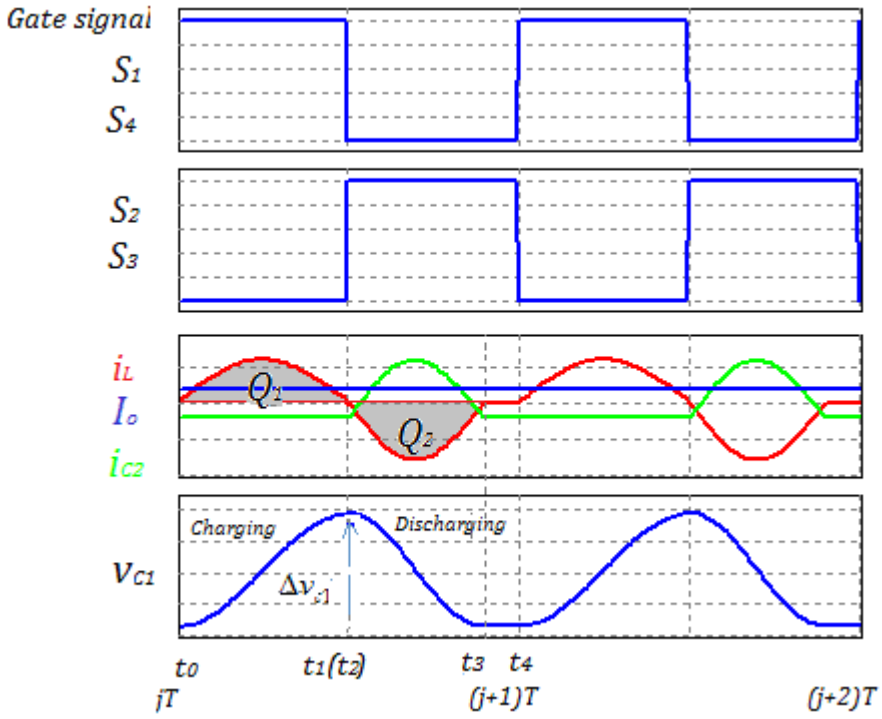
$$M = \frac{V_{oj}}{V_j} = 2 \tag{2-29}$$

2.3.3 Case 3: RLC equivalent circuit

A resistance in series with the charging and discharging circuit is studied that includes the on state resistance of the Mosfet and the series resistance of the capacitor and all the resistance of the wire during charging and discharging.



(a) Proposed circuit with parasitic resistance (b) Equivalent circuits



(c) Waveforms of the circuit in steady state.

Fig. 2-5. The circuit system, equivalent circuit system and the waveforms of the circuit

As it is shown in Fig. 2-5 (b), when switches S_1 and S_4 are turned on, the capacitor C_1 is charging up, then the state equations are:

$$L_r \frac{di_L}{dt} + v_{C1} + R_1 i_L = V_j \quad (V_j = V_{in} \sin j\omega T) \tag{2-30}$$

$$i_L = C_1 \frac{dv_{C1}}{dt} \tag{2-31}$$

Then, the solutions are

$$v_{C1} = (V_{C1\min} - V_j) e^{-\alpha t} \left(\sqrt{1 + (\frac{\alpha}{\omega_d})^2}\right) \cos(\omega_d t + \varphi) + V_j \tag{2-32}$$

$$i_L = -\omega_d C_1 (1 + (\frac{\alpha}{\omega_d})^2)(V_{C1\min} - V_j) e^{-\alpha t} \sin(\omega_d t) \tag{2-33}$$

where $0 < t < T_0 / 2$, $\omega_0 = \frac{1}{\sqrt{L_r C_1}}$, $\alpha = \frac{R_1}{2L_r}$, $\omega_d = \sqrt{\omega_0^2 - \alpha^2}$, $\varphi = \tan^{-1}(\frac{\alpha}{\omega_d})$

$V_{C1\min}$ is the minimum value of the voltage of capacitor C_1 and it will reach the maximum value when it reaches t_1 till half switching cycle. T_0 is the resnonant cycle when the capacitor C_1 is charging. Then:

$$v_{C1} = V_{C1\max} \tag{2-34}$$

$$i_L = 0 \tag{2-35}$$

As it is shown in Fig. 2-5 (b), when switches S_2 and S_3 are turned on, the capacitor C_1 is discharging, then the state equations are:

$$V_j + v_{C1} + L_r \frac{di_L}{dt} - R i_L = V_{Oj} \tag{2-36}$$

$$i_L = C_1 \frac{dv_{C1}}{dt} \tag{2-37}$$

Then the equations are solved as

$$v_{C1} = (V_{C1\max} - V_{Oj} + V_j)e^{\alpha t}(\sqrt{1+(\frac{\alpha}{\omega_d})^2})\cos(\omega_d t + \varphi) + V_{Oj} - V_j \quad (2\text{-}38)$$

$$i_L = -\omega_d C_1(1+(\frac{\alpha}{\omega_d})^2)(V_{C1\max} - V_{Oj} + V_j)e^{\alpha t}\sin(\omega_d t) \quad (2\text{-}39)$$

where $0 < t < T_{01}/2$, $\omega_0 = \frac{1}{\sqrt{L_r C_1}}$, $\alpha = \frac{R_1}{2L_r}$, $\omega_d = \sqrt{\omega_0{}^2 - \alpha^2}$, $\varphi = \tan^{-1}(-\frac{\alpha}{\omega_d})$, T_{01} is the resnonant cycle when the capacitor C_1 is discharging.

Similarly, as shown in Fig.2-5(c), based on the charge conservation theory equation (2-11) and the following equations (2-40) and (2-41),

$$Q_1 = \int_0^{T_0} -\omega_d C_1(1+(\frac{\alpha}{\omega_d})^2)(V_{c1\min} - V_j)e^{-\alpha t}\sin(\omega_d t)dt \quad (2\text{-}40)$$

$$Q_2 = \int_0^{T_{01}} -\omega_d C_1(1+(\frac{\alpha}{\omega_d})^2)(V_{c1\max} - V_{Oj} + V_j)e^{\alpha t}\sin(\omega_d t)dt \quad (2\text{-}41)$$

Assume $T_0 = T_{01}$, Then:

$$V_{Oj} = 2V_j - 2(\frac{1}{e^{\alpha T_0/2} - 1})\frac{I_{oj}T_S}{C_1} \quad (2\text{-}42)$$

Then the voltage conversion ratio is

$$M = \frac{V_{oj}}{V_j} = 2 - 2(\frac{1}{e^{\alpha T_0/2} - 1})\frac{I_{oj}T_S}{C_1 V_j} \quad (2\text{-}43)$$

2.4 Simulation and Experimental Results

The experiment is completed to verify the performance of the proposed resonant circuit. The MOSFETs used are IRF540. The amplitude of input voltage is 10V. The switching frequency is set to 100 kHz. Two capacitors are both 2.2μF. The resonant inductance is derived partly from the parasitic inductance in the resonant loop and is

equal to 1.2μH, the equivalent resistant in the charging and discharging circuit is equivalent to 0.8 Ω measured in circuit The simulation of the proposed circuit is conducted by PSIM9.0. The switching signal, charging and discharging currents of C_1 and the output voltage are examined, which is shown on the right of the experiment results.

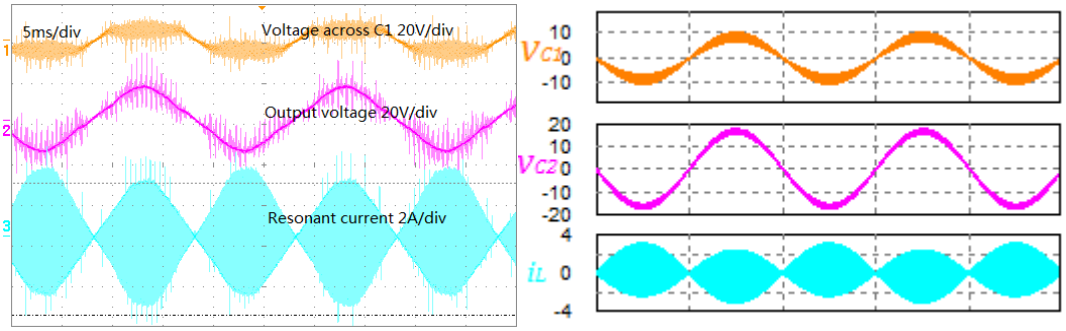
The experimental and simulation results are shown in Figs 2-6-Fig. 2-8, which verifies the operational principle of the proposed resonant circuit, which is called zero-current quasi-resonance [92-93].

Fig.2-6 describes the performance of the system with different loads. As is shown in Fig. 2-6(a), the output voltage is slightly less than double of the input voltage because of the voltage drop in the components. As the load resistance is reduced from R=47 Ω to 20 Ω, the resonant current increases, but the output voltage remains unchanged and is still double of the input voltage. Fig. 2-6(b) shows when the switch is turned on, the current increases from zero in a sinusoidal manner. The current reaches zero after the resonance and before the switch is turned off, that realizes the zero current switching and reduces the power loss. The resonant current waveform is close to sinusoidal, which means that f_0 is close to f_s. In such resonant manner, the capacitor transfers most energy as it can.

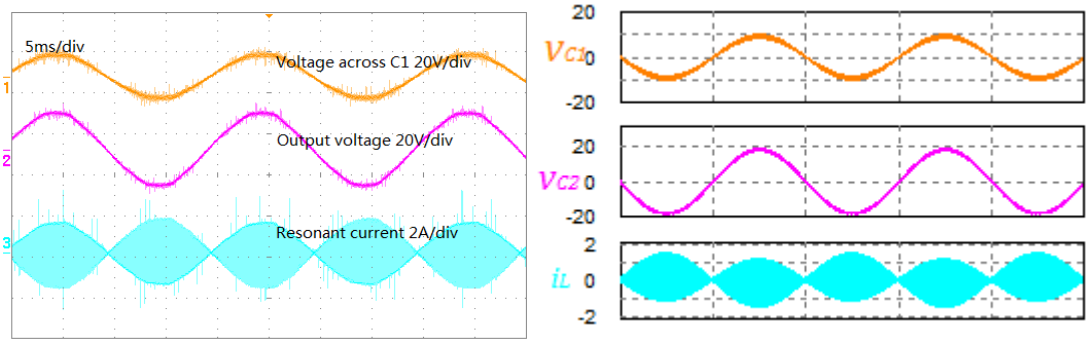
Higher input voltage has also been applied to the circuit to verify the performance of

the proposed resonant step-up switched capacitor converter, which is shown in Fig.2-7. Input voltages of 30V and 50 V are applied to the circuit. The system is stable. The practical power efficiency versus input voltage and conversion ratio versus output power is shown in the experimental results in Fig.2-8. As shown in Fig. 2-8 (a)-(b), the power efficiency is above 98%, the conversion ratio is above 1.85, and the output power is from 25 to 350W. The conduction loss of the power converter is high at high voltage wich leads to the efficiency drop at high voltage in Fig. 2-8.

The experimental results agree with the simulation results well, as shown in the following figures.

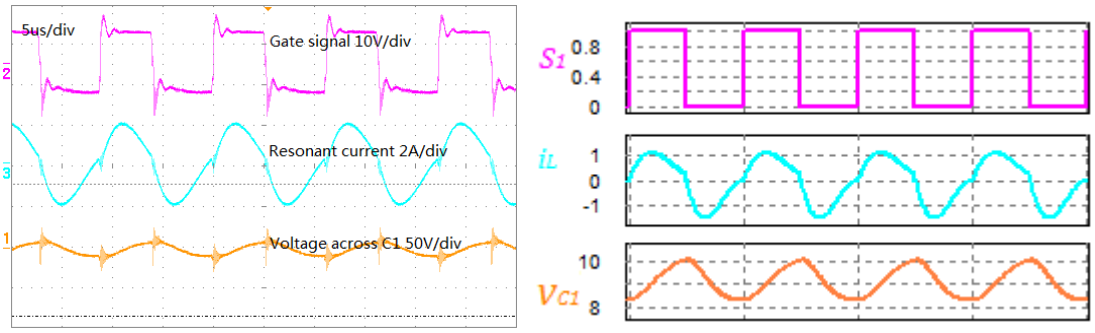


(i) R = 20Ω,



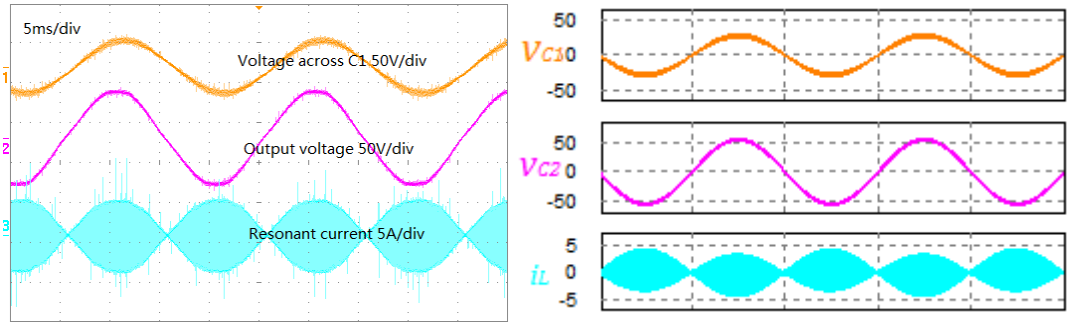
(ii) R =47Ω

(a) The voltage across C_1, output voltage, resonant current

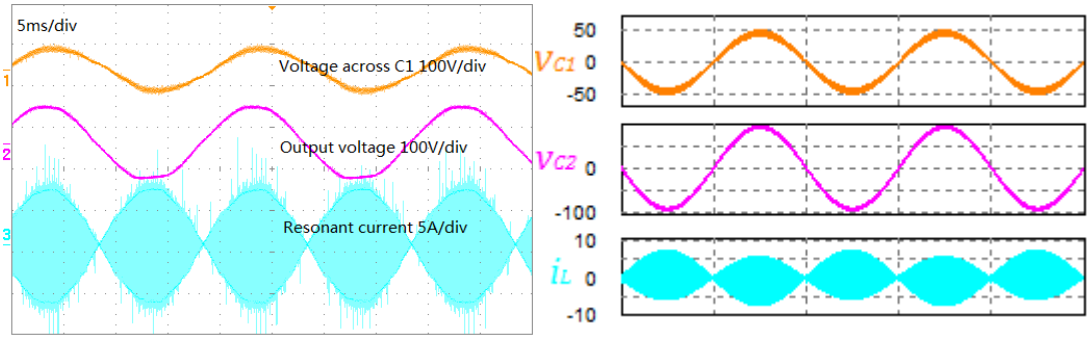


(b) The gate signal, resonant current, voltage across C_1 when R=47Ω

Fig. 2-6 Experimental results of the proposed resonant circuit with different loads, when V_{in}=10V, L_r=1.2μH, C_1=C_2=2.2μF(left: experiment, right: simulation)

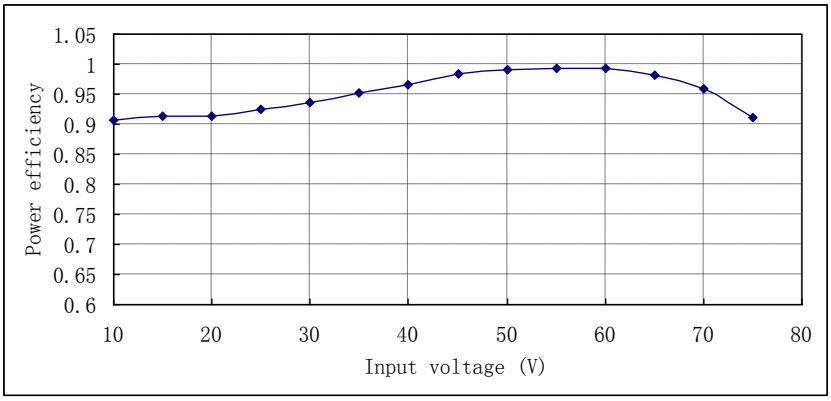


(i) V_{in}=30V

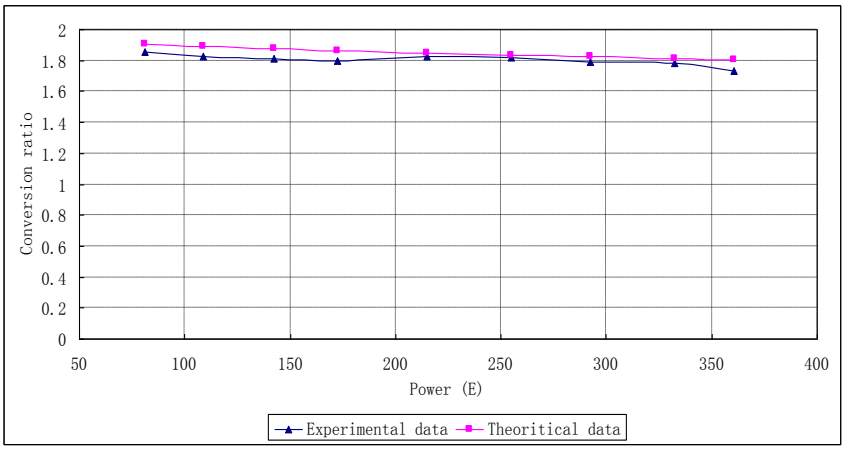


(ii) Vin=50V

Fig.2-7 The performance of the proposed topology with different input voltages, when R=47Ω, L_r=1.2μH, C_1=C_2=2.2μF (left: experiment, right: simulation)



(a) power efficiency versus input voltage



(b) conversion ratio versus output power

Fig.2-8 Experimental results of power efficiency and conversion ratio

Experimental results in Table 2-2 indicated that the power converter can output very stable voltage with high power. The power efficiency is up to 0.98. RL load has also been tested. The effect is the same as any AC source with RL load. The AC source frequency is much lower than the resonant frequency, it obviously there is no special concern.

Table 2.1. Comparison between simulation and experiment

	Simulation	Experiment
Conversion ratio	2	1.75~1.85
Power efficiency (Resonant mode)	1	0.9~0.98

Power efficiency (Non-Resonant mode)	1	0.79~0.92

The comparison of the proposed converter with the matrix converter and the back to back converter has been illustrated in Table 3 based on single phase operation.

Table 2.2. Comparison with Matrix and Back to Back converter

	Proposed AC-AC SC converter	Matrix AC-AC converter	Conventional back to back converter	Quantum Series resonant converter
Active components count	• 4 idirectional switches or 8 Mosfets • Result: **moderate**	• 4 idirectional switches or 8 Mosfets • Result: **moderate**	• 8 Mosfets or switches • Result: **moderate**	• 3bidirectional switches or 6Mosfets • Result: **moderate**
Passive component count	• No input filter, and output filter, Small size of LC resonant tank • No DC filter • Result: **(better)**	• Normal size of input and output AC LC filter is required • No DC filter • Result: **moderate**	• Less size of input and output AC LC filter is required, • but large DC filter is required • Result: **worse**	• Two capacitors as input filter, and output filter, Small size of LC resonant tank • No DC filter • Result: **(better)**
Complexity of control	• Open loop, no control • Result: **better**	• Complex closed-loop control strategy • Result: **worse**	• Simple closed loop sinusoidal PWM control • Result: **moderate**	• Open loop, no control • Result: **better**
Regulation of output	• Fixed conversion	• Regulated by duty ratio	• Regulated by duty ratio	• Fixed conversion

voltage	ratio • Result: **worse**	• Result: **better**	• Result: **better**	ratio • Result: **worse** • Result: **worse**
Stability of output voltage	• Absolutely stable • Result: **best**	• Stable • Result: **better**	• Stable • Result: **better**	• Absolutely stable • Result: **best**
Efficiency	• Soft switching • Result: **best**	• Hard switching • Result: **moderate**	• Hard switching • Result: **moderate**	• Soft switching • Result: **better**

2.5 Summary

The switched capacitor based AC-AC converter is an AC power supply which has a simple structure, small size, light weight and can double the input voltage. The topology is suitable for portable products and is possible to be made into IC chips. A small resonant inductor is introduced to limit current and it avoids the shortcomings of current spikes. Switches are turned on and off under zero-current, so the switching loss and EMI are very low. The trigger circuit is simple. Therefore, it is expected that it could contribute to the application of AC distribution development.

Experimental results indicated that the power converter can provide very stable voltage with high power. The resonant current is controlled and has a smooth transition during turn-on and turn-off. The resonant inductor can also be partly or completely replaced by the parasitic inductance of the circuit, and is a quantified value rather than uncertain leakage inductance, which can further reduce the cost, size and simplify the circuit.

Chapter 3

A Topology of Step Down Resonant Switched Capacitor Based ACDC Converter for High Frequency AC Distribution

3.1 Introduction

Power supply modules are well-known techniques and have become a hot research topic since the mid–‘80s when the technical concept and design of modular converters was first developed [107]. Function-module application solutions support effective development of electronic systems. Each function comes with a high performance module. For example, high performance MCUs, driving controllers, rectifier bridges, and modular SMPS have become basic elements in the design of devices and the electronic power systems (EPS) used in many applications – from commercial to aerospace [108], which shorten system development time, reduce the number of parts, and help their system engineers build higher performance and greater functionality into new products. Standardization and unification are important components of pricing policy, and should serve as crucial factors in improving the specifications of power supplies, and should reduce the prices of devices and equipment in general. Also, it is known that the optimal size of a transformer depends on its switching frequency; therefore, there can be a significant decrease in transformer size whilst

increasing the frequency to the 20kHz – 180kHz range.

Nowadays, the operation frequency of the power devices is increasing rapidly and the size of the power circuit is becoming much more compact, which pushes the power line frequency much higher than usual. The use of 50/60Hz is now too conventional and has to be increased to match higher frequency techniques that have been available for years. Since a few decades ago, the frequency of ac power line has increased to 20kHz in spacecraft [3, 16], and now the power line in aircraft is usually 400Hz or 700Hz [17, 108-109]. The increasing high frequency of the power line allows the load side power converter to become more compact; meanwhile, new circuit topology allows fewer numbers of switches to be used and the circuit control to become simplified, which reduces costs and space. Higher efficiency, power density and lower cost can be obtained. Integration of the power circuit can be achieved due to the higher line frequency.

In recent years, the switched capacitor (SC) based power converter has been an important research topic [17, 71-72, 74-75, 81]. In such circuits, the absence of magnetic elements can significantly reduce the overall size as compared with conventional switched mode power converters, which also makes the power converter much more compact since there are only switches, diodes, capacitors in the circuit. High charging and discharging current spikes are decreased by introducing small

resonant inductors [76-77], which significantly reduces the power loss and increases efficiency and power density. Line regulation strategies and output ripple reduction methods are also incorporated to SC converters to improve the performance of the power circuits [82, 84]. The widely used resonant and output regulation techniques extend SC applications. Especially, the diode capacitor multiplier and divider can be integrated into single module respectively.

The principles between the resonant switched-capacitor and the other resonant converters [110] are similar; however, the resonant storage energy is different. In the resonant switched-capacitor converter [76-77], nearly the whole period of switching is under the resonance. This is also referred to quasi-resonant [111-112]; however, these conventional quasi-resonant converters have the capacitor under the total resonance and their DC level is usually zero or its resonant amplitude is on the same level as output or input voltage. The resonant transition, such as the phase-shifted H-bridge [113], for which energy of the resonant inductor is not used wholly for the resonance whereas the resonant inductor's energy for resonant switched-capacitor is used totally for the resonance. The classical load resonant [114] converter is a fully resonant circuit, but its transistors are under resonant transition for zero-voltage switching and the resonant components of L and C are under total resonance energy transferred. In contrast, in the proposed resonant switched-capacitor converter, only the L is under

total resonant energy transfer and the C has a large DC level and a small resonant level. Traditionally, the AC-DC converter is built up with a bridge rectifier, filter, and DC-DC converter. It is complicated in operation with a number of stages. It is a popular and hot research topic to address the sinusoidal input current or high power factor, low input harmonics and high power density. There are several AC-DC converter topologies proposed for high frequency power distribution [24, 80, 83, 115-118], and resonant circuits have been adopted. However, diode bridges and filters are still used for the interface between AC and DC. Recently, AC-AC, AC-DC converters and controlled rectifiers have also been implemented with SC elements or in a cascaded stage to step-down the input voltage [79, 85-86]. Cascaded SC dividers and multipliers implemented in the power converters significantly improve the performance of the circuit which is more efficiency and component life extended. However, the bridge rectifier and inductor are still playing important roles in the front-end of the converter on power processing.

In this chapter, it is intended to propose AC-DC step up/down topology with cascade stages, which can be fabricated into a compact module and easy to replace and maintain. Meanwhile, it will contain a simple control circuit and a bridge rectifier but a buffer inductor will be excluded. The circuit includes one energy buffer capacitor, two switches, and cascaded step down SC elements. In order to reduce the large current

spike during charging and discharging and to reduce the switching loss, small parasitic inductors are used to form a resonant loop circuit. Therefore, zero current switching (ZCS) is achieved. A general topology of the AC-DC converter is presented that is based on switched-capacitor techniques [77]. Both step up and step down can be derived from this topology. This chapter concentrates on the step down conversion.

3.2 General Model of the Resonant AC-DC Switched Capacitor Converter

A proposed circuit consisting of one cascaded SC element is firstly presented in Fig. 3-1(a), which would be a simple AC input doubler benefitting from a high frequency feeder. For the first order of the voltage step up, only a capacitor and a diode are need. It is much more simple than the traditional step up power converter. The AC element in (b) which usually in DC-DC converter can be added indefinitely to provide other conversion ratios in the proposed AC-DC converter.

The driving signal of the MOSFET is shown in Fig. 3-1(c). Two switches are turned on and off alternatively in a cycle. After the transient period, S_1 is turned on and S_2 is turned off in the positive half cycle of the source; both the source and capacitor C_s are charging the capacitor C_1. The output capacitor C_o is releasing energy to the load. In the negative cycle of the source, S_1 is turned off, and S_2 is turned on; the voltage source is charging capacitor C_s. The voltage across capacitor C_s is increasing. At the same time,

the capacitor C_1 is releasing energy to the load. The voltage has been stepped up. Fig.3-1(b) illustrates one SC element. Step-down voltage can be achieved by simply introducing cascaded SC elements. In this case, cascaded SC dividers can be integrated onto a chip or low profile circuit to achieve a higher power density step-down voltage converter, as is shown in Fig. 3-2. It is noted that there are only two operation states which are simple and without complex control circuit.

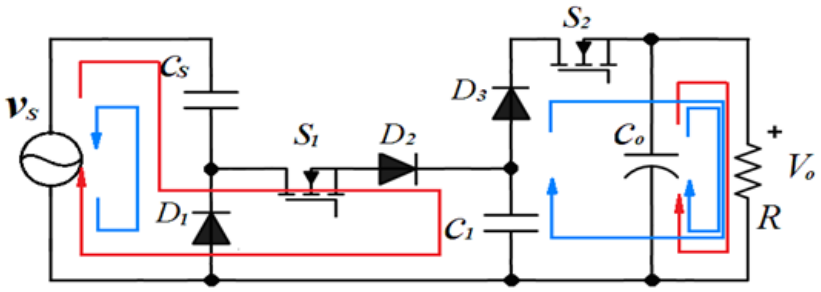


Fig. 3-1 (a) The ac voltage doubler

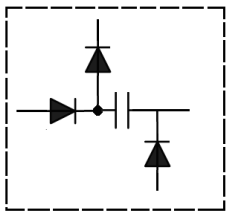


Fig. 3-1 (b) SC element

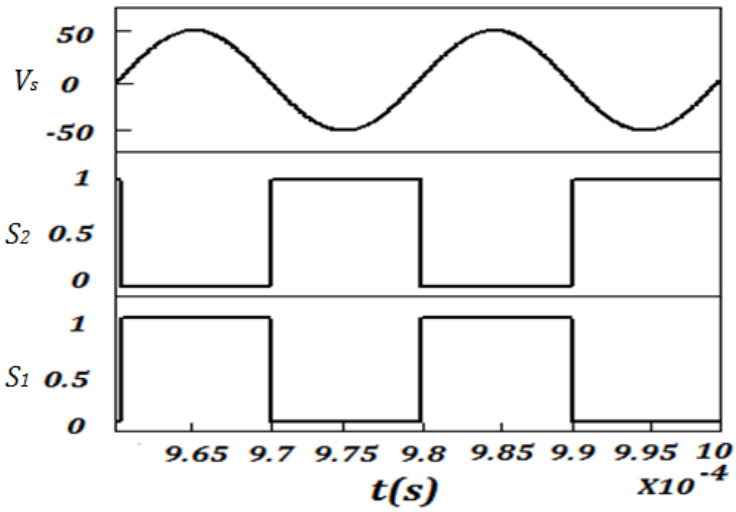


Fig. 3-1 (c) The source voltage and the driving signal

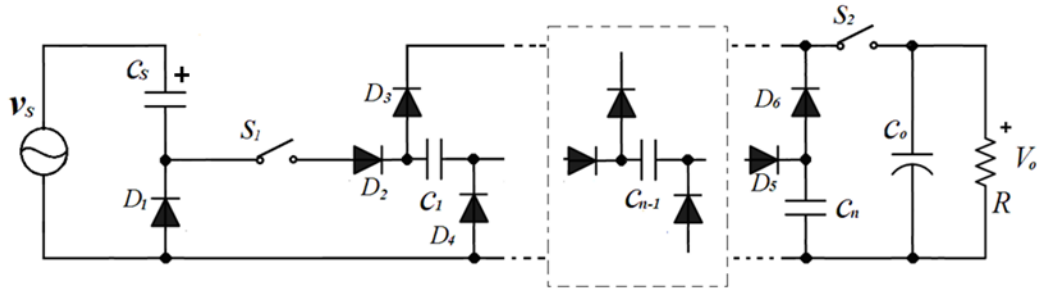


Fig. 3-2 Proposed circuit consisting cascaded SC elements to step down the voltage

The following analysis will focus on a three-cascaded-step-down-SC circuit, which is presented in Fig. 3-3. In order to reduce the current spikes, small inductors have been added into the circuit; therefore, all of the switches and the diodes are working under the zero current switching. The steady state operation and the design consideration are also analyzed in the following sections. Finally, an experiment is carried out to verify the analysis.

3.3 Proposed Converter Structure, Operation Principle and Steady State

Analysis

3.3.1 Proposed Converter Structure

The proposed circuit, including three-cascaded step down SC elements, is presented in Fig. 3-3(a). It consists of two switches, two small resonant inductors and three SC elements to obtain step down voltage. There are only two operation modes in the circuit, which is shown in Fig. 3-3(b) and (c). Assume that all of the components are ideal.

When the system reaches the steady state, the key waveform is shown in Fig. 3-4 (a), (b) and (c). The parameters of the circuit are illustrated as follows: the amplitude and frequency of the voltage source is 50V and 50kHz respectively, the capacitances of C_s, C_1, C_2 and C_3 are all 6.8μF, the filter capacitance C_0 is 47μF, and the resonant inductance of L_s and L_r is 6.0μH and 0.5μH respectively. The resistance of the load is 20 Ω. Only the voltage and current of step down capacitor C_1 are illustrated in Fig. 3-4. (a). Since the capacitances of C_1, C_2 and C_3 are the same, the voltages and currents in capacitors C_1, C_2 and C_3 are all the same, which are shown in Fig. 3-4. (b) and (c).

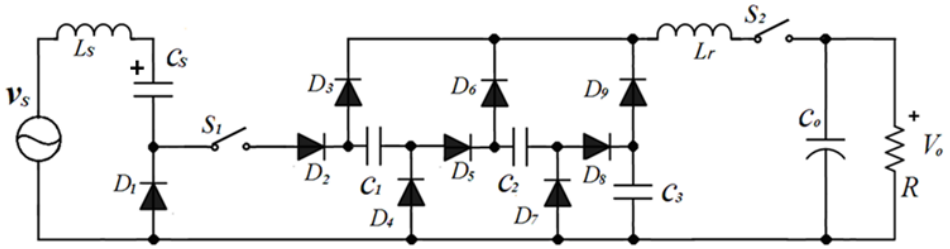


Fig. 3-3 (a) The proposed circuit consisting three cascaded step down SC elements

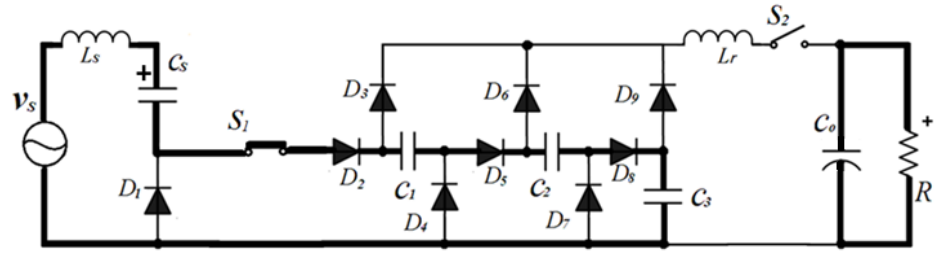


Fig. 3-3 (b) The operation states working in positive half wave (S_1 is on and S_2 is off).

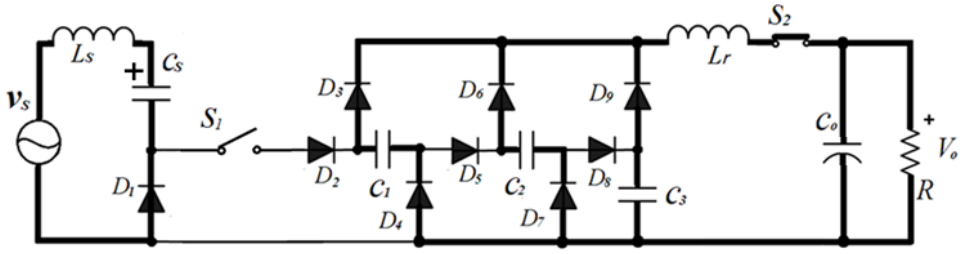


Fig. 3-3 (c) The operation states working in negative half wave (S_1 is off and S_2 is on).

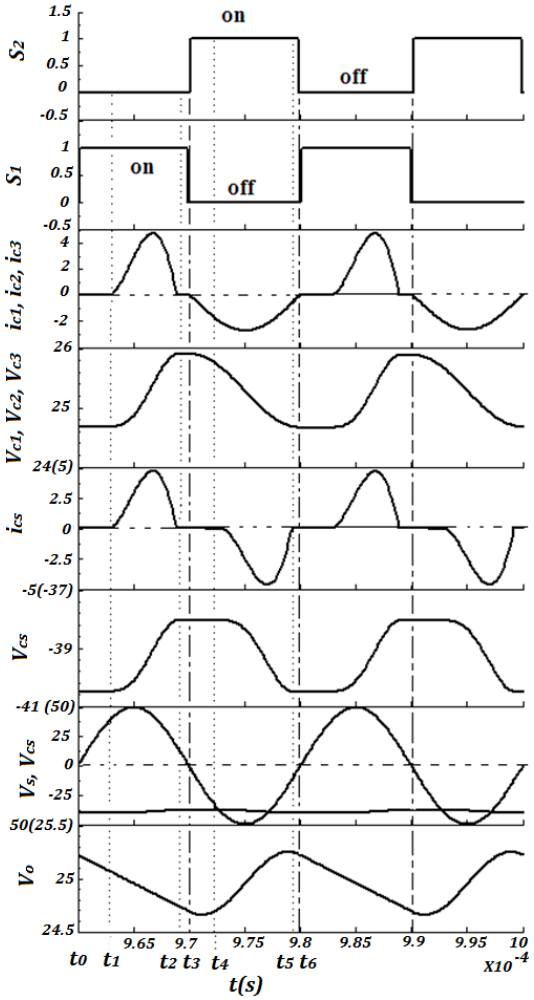


Fig. 3-4 (a) The key waveforms of the proposed circuit

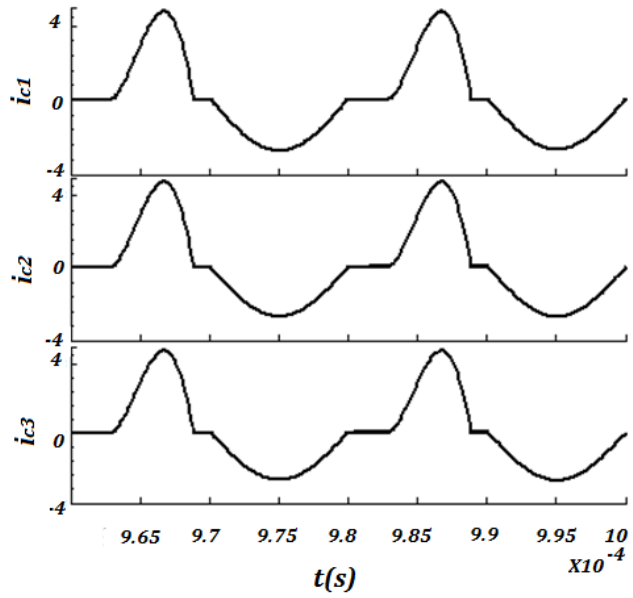


Fig. 3-4 (b) The current flowing through capacitors C_1, C_2 and C_3

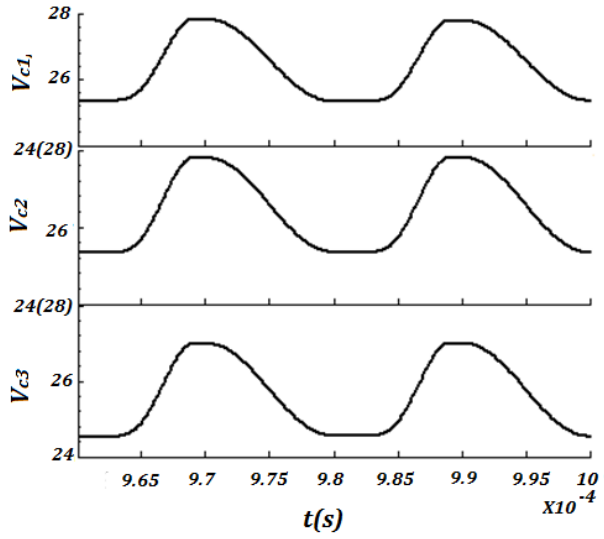


Fig. 3-4 (c) The voltage across capacitor C_1, C_2 and C_3

3.3.2 Operation Principle

Mode A: in the positive half cycle, as shown in circuit Fig. 3-3(b), switch S_1 is turned on and S_2 is turned off. The voltage source and capacitor C_s are charging C_1, C_2 and C_3. C_o is releasing energy to the load. In this mode, it can be divided into three stages, as is shown in Fig. 3-4(a), which are t_0 to t_3

a) Stage 1(t_0-t_1): when the system is operating in the steady state, there is an initial negative voltage across capacitor C_s and also an initial voltage across capacitors C_1, C_2 and C_3. The voltages across capacitors C_s, C_1, C_2, C_3 keep constant between t_0 and t_1 due to reversed D_2 even though S_1 is on, until the sum of the source voltage v_s and the voltage across buffer capacitor v_{cs} is greater than the sum of the voltages across capacitors C_1, C_2 and C_3 ,which is v_{c1}, v_{c2}, and v_{c3} respectively. There is no current flowing through any of

capacitors. Meanwhile, the output capacitor C_o is releasing energy to the load.

b) Stage 2(t_1-t_2): when the sum of the source voltage v_s and the voltage across buffer capacitor v_{cs} is greater than the sum of the voltages across capacitors C_1, C_2 and C_3, source voltage and the capacitor C_s start to charge capacitor C_1, C_2 and C_3, the current is increased slowly due to the resonant inductor L_s . The voltage v_{cs} decreases while v_{c1}, v_{c2} and v_{c3} increase until time instance t_2, when the resonance stops. In this stage, the output capacitor C_o is releasing energy to the load.

c) Stage 3(t_2-t_3): the resonant current reaches zero at t_2 when the resonance stops, and stays at zero until the switching cycle ends, then S_1 is off and S_2 is on.

The waveform is illustrated in Fig. 3-4(a).

Mode B: in the negative cycle, as shown in Fig. 3-3(c), the switch S_1 is turned off and S_2 is turned on. Capacitor C_s is charged by the voltage source. Capacitors C_1, C_2 and C_3 are parallel connected and release energy to the load. In this mode, it can be divided into three stages, which is illustrated in Fig. 3-4(a) from t_4 to t_6.

a) Stage 1(t_3-t_4): The capacitors C_1, C_2 and C_3 are parallel connected and start to release energy into the load. The current is increasing slowly due to the

resonant inductor $L_{r.}$. The voltages v_{c1}, v_{c2}, and v_{c3} decrease until the time instance t_5, when the resonance stops. Meanwhile, the voltage of v_{cs} keeps constant from t_3 to t_4 due to the reversed diode D_1, because the source voltage is less than the voltage v_{cs}.

b) Stage 2(t_4-t_5): when the source voltage v_s is greater than v_{cs}, the capacitor C_s is charged. The current increases slowly due to the presence of resonant inductor L_s. The voltage v_{cs} also increases until the time instance t_5, when the resonance stops.

c) Stage 3(t_5-t_6): The resonant current reaches zero at t_5 and is unchanged until t_6 when the switching cycle ends. Then S_1 is off and S_2 is on. The waveform is presented in Fig. 3-4(a).

3.4 Steady State Analysis

The operation modes of the circuit are illustrated in Fig. 3-5(a) and (b). The steady state analysis is as follows. The steady voltage on C_s is negative.

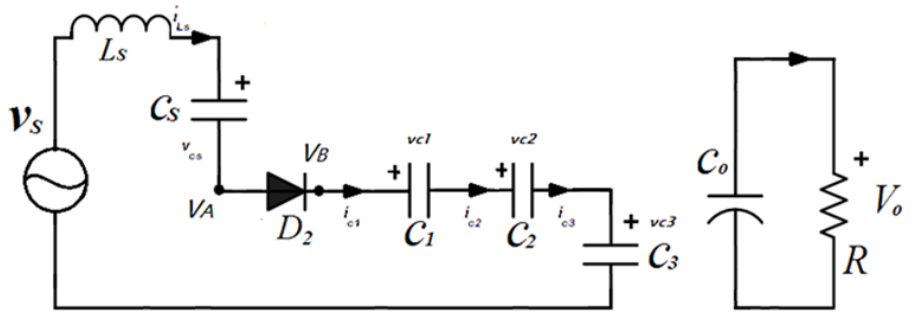


Fig. 3-5 (a) The operation of mode A

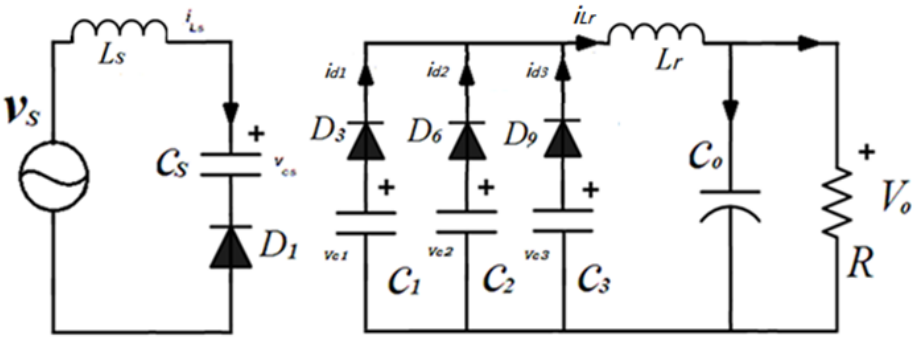


Fig. 3-5 (b) The operation of mode B

a) Mode A: L_s is one of the resonant inductors. The capacitances of C_1, C_2 and C_3 are equal and are named as C in the analysis. The source voltage is $v_s\sin\omega t$. i_{Ls} is the current flowing through L_s, C_s, C_1, C_2 and C_3; therefore, i_{Ls} is equal to i_{c1}, i_{c2} and i_{c3}. When the sum of voltages of the source v_s and capacitor v_{cs} is greater than the sum of voltage of capacitor v_{c1}, v_{c2} and v_{c3}, i_{Ls} starts to increase from zero. v_{c1}, v_{c2} and v_{c3} are the voltages across the capacitors and are equal to v_c, since the capacitance are equal. When the system reaches steady state, there is:

$$\begin{cases} V_s\sin\omega t = L_s\frac{di_{Ls}}{d(t-t_1)} + v_{cs} + 3v_c \\ i_{Ls} = C_s\frac{dv_{cs}}{d(t-t_1)} = c\frac{dv_c}{d(t-t_1)} \end{cases} \tag{3-1}$$

$$\begin{cases} i_{Ls}(t_1) = 0 \\ {i_{Ls}}'(t_1) = 0 \end{cases} \tag{3-2}$$

The solutions are:

$$i_{Ls} = A(k_1 \cos \omega_{01}(t - t_1) + k_2 \sin \omega_{01}(t - t_1) + k_3 \cos \omega\, t) \quad (3\text{-}3)$$

$$v_{cs} = \frac{A}{C_s}\left(\frac{k_1}{\omega_{01}} \sin \omega_{01}(t - t_1) - \frac{k_2}{\omega_{01}} cos\omega_{01}(t - t_1) + \frac{k_3}{\omega} sin\omega t\right) \quad (3\text{-}4)$$

$$v_c = \frac{A}{C}\left(\frac{k_1}{\omega_{01}} \sin \omega_{01}(t - t_1) - \frac{k_2}{\omega_{01}} cos\omega_{01}(t - t_1) + \frac{k_3}{\omega} sin\omega t\right) \quad (3\text{-}5)$$

where, $k_1 = -\frac{\omega}{\omega_{01}{}^2 - \omega^2} \cos\omega t_1$, $k_2 = \frac{\omega^2}{\omega_{01}(\omega_{01}{}^2 - \omega^2)} \sin\omega t_1$, $k_3 = \frac{\omega}{\omega_{01}{}^2 - \omega^2}$, $A = \frac{V_s}{L_s}$, t_1, t_2 are determined by the following equations, which can be solved by numerical method.

$$\begin{cases} 3\int_{t_1}^{t_2} i_{Ls}(t)dt = I_o T_s \\ i_{Ls}(t_2) = 0 \end{cases} \quad (3\text{-}6)$$

ω is the angular frequency of the source voltage which is $\omega = 2\pi f_s$, f_s is the frequency of input voltage, and T_s is the switching cycle. ω_{01} is the resonant angular frequency when the source voltage and the capacitor C_s is charging C_1, C_2, and C_3, which is $\omega_{01} = \sqrt{\frac{1}{L_s}\left(\frac{3}{C} + \frac{1}{C_s}\right)}$. I_o is the output current.

b) Mode B: i_{C1}, i_{C2} and i_{C3} are equal and are the current flowing through the capacitors respectively, due to the equal LC paths and resonant inductance L_r. i_{Lr} is the current flowing through the resonant inductor. When S_1 is turned off and S_2 is turned on, the source voltage is charging the capacitor C_s; meanwhile, capacitors C_1, C_2, and C_3 are parallel connected and start to resonate with L_r and discharge. Then there is

$$\begin{cases} V_s \sin\omega t = L_s \frac{di_{Ls}}{d(t-t_4)} + v_{cs} \\ i_{Ls} = C_s \frac{dv_{cs}}{d(t-t_4)} \end{cases} \tag{3-7}$$

$$\begin{cases} i_{Ls}(t_4) = 0 \\ {i_{Ls}}'(t_4) = 0 \end{cases} \tag{3-8}$$

The solutions are:

$$\mathrm{i_{Ls}} = \mathrm{A}(\mathrm{k'_1}\cos\omega_{02}(\mathrm{t}-\mathrm{t_4}) + \mathrm{k'_2}\sin\omega_{02}(\mathrm{t}-\mathrm{t_4}) + \mathrm{k'_3}\cos\omega\,\mathrm{t}) \tag{3-9}$$

$$\mathrm{v_{cs}} = \frac{\mathrm{A}}{\mathrm{C_s}}\left(\frac{\mathrm{k'_1}}{\omega_{02}}\sin\omega_{02}(\mathrm{t}-\mathrm{t_4}) - \frac{\mathrm{k'_2}}{\omega_{02}}\cos\omega_{02}(\mathrm{t}-\mathrm{t_4}) + \frac{\mathrm{k'_3}}{\omega}\sin\omega t\right) \tag{3-10}$$

$$\mathrm{v_c} = \frac{\mathrm{A}}{\mathrm{C}}\left(\frac{\mathrm{k'_1}}{\omega_{02}}\sin\omega_{02}(\mathrm{t}-\mathrm{t_4}) - \frac{\mathrm{k'_2}}{\omega_{02}}\cos\omega_{02}(\mathrm{t}-\mathrm{t_4}) + \frac{\mathrm{k'_3}}{\omega}\sin\omega t\right) \tag{3-11}$$

where, $\mathrm{k'_1} = -\frac{\omega}{{\omega_{02}}^2-\omega^2}\cos\omega t_1$, $\mathrm{k'_2} = \frac{\omega^2}{\omega_{02}({\omega_{02}}^2-\omega^2)}\sin\omega t_1$, $\mathrm{k'_3} = \frac{\omega}{{\omega_{02}}^2-\omega^2}$, $\mathrm{A} = \frac{\mathrm{v_s}}{\mathrm{L_s}}$, ω_{02} is the resonant frequency, which is $\frac{1}{\sqrt{\mathrm{L_s C_s}}}$. $\mathrm{t_1}$, and $\mathrm{t_2}$ are determined by the following equations, which can be solved by the numerical solution method.

$$\begin{cases} 3\int_{t_4}^{t_5} i_{Ls}(t)dt = Q \\ i_{Ls}(t_5) = 0 \end{cases} \tag{3-12}$$

However, there is

$$\begin{cases} V_o = L_r \frac{di_{Lr}}{dt} + v_c \\ i_{Lr} = C\frac{dv_c}{dt} \end{cases} \tag{3-13}$$

The solutions are:

$$i_{Lr} = \frac{I_0 T_s \omega_{03}}{2}\sin\omega_{03}t \tag{3-14}$$

$$v_c = V_o - \frac{ZI_0 T_s \omega_{03}}{2}\cos\omega_{03}t \tag{3-15}$$

where, ω_{03} is the resonant frequency, which is $\frac{1}{\sqrt{3L_rC}}$, $\mathrm{Z} = \sqrt{\frac{L_r}{3C}}$. V_o is the output voltage. Z is the impedance.

3.5 Design Consideration

1) It is noted that when the voltage source is working in the negative half cycle, capacitors C_1, C_2 and C_3 are in parallel connection. When the voltage source is working in the positive half cycle, capacitors C_1, C_2 and C_3 are in series connection. Therefore, the voltage source and energy buffer capacitor will charge capacitors C_1, C_2 and C_3 only when the sum of voltages of the source and capacitor C_s is greater than the sum of the voltages of capacitor C_1, C_2 and C_3, which is $V_A > V_B$, as shown in Fig. 3-5(a)
2) At the start of the positive half cycle of the voltage source, the sum of the voltage of capacitors C_1, C_2 and C_3 may be greater than the sum of the source and capacitor C_s, which is $V_A > V_B$. Then a diode is needed to block the current from flowing back to the source because the switch MOSFET S_1 has an antiparallel body diode which allows the current flowing back to the source.
3) At the negative half cycle, when the capacitor C_s is charged, while S_2 is on, the voltage of point A may be greater than that of point B. The capacitor C_s may start to release energy into the load. Therefore, a switch is necessary between them. So, both a switch and diode are needed between points A and B.
4) The determination of the capacitor: The equivalent circuit of the system is as shown in Fig. 3-5(b). When the system reaches to the steady state, the

waveform of current i_{cs}, i_c and the output voltage V_o are presented in Fig. 3-6. The Charge going in and out of C_o and C_s is the same, which equals the total charge going in and out of C_1, C_2, C_3. Then there is $\Delta V_{Co} * C_o = \frac{Vo}{R} T_s$, which gives $C_o = \frac{Vo}{\Delta V_{Co} R f_s} = \frac{I_o T_s}{\Delta V_{Co}}$, where ΔV_{Co} is the output voltage ripple, V_o is the average output voltage, T_s is the period of the switching frequency, and f_s is the frequency of source voltage. For equalizing the charge, there is

$$3\int_{t_1}^{t_2} i_{Ls}(t)dt = 3\int_{t_3}^{t_6} i_c(t)dt = I_o T_s \tag{3-16}$$

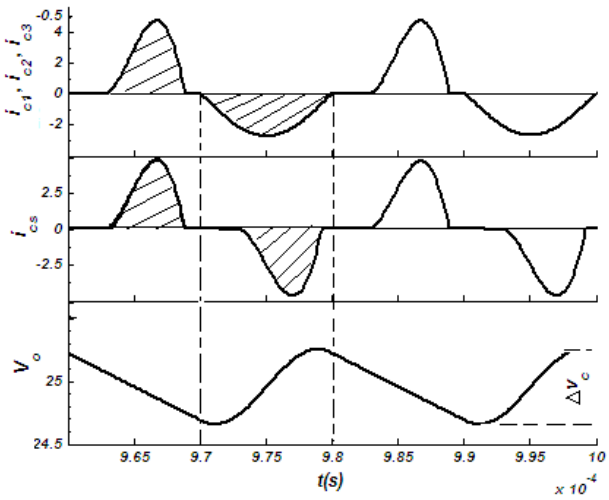


Fig. 3-6 The waveform of current ics, ic and the output voltage Vo

5) The determination of the resonant inductor L_s and L_r:

Based on the principle of zero current switching of resonant SC circuit [7], the resonant frequency should not be less than switching frequency, Therefore, when $f_{03} \geq f_S$, ZCS can be achieved from $\omega_{03} = \frac{1}{\sqrt{3L_r C}}$, there is $L_r \leq \frac{1}{12\pi^2 f_s^2 C}$. The current following through the switches S_1 and S_2 with the resonant inductor is shown in Fig. 3-7. As is shown, there is no current spike flowing through all the diodes and switches. Therefore,

the switches are turned on and off under zero current; hence, ZCS is achieved.

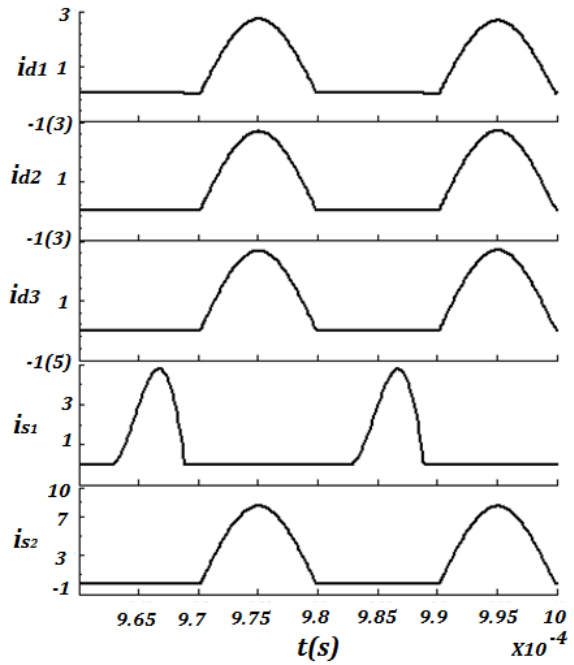


Fig. 3-7 The current flowing through the diodes and switches

6) Power efficiency

In order to simplify the power efficiency analysis of the proposed circuit, only power loss of diodes, MOSFETS and equivalent series resistor of the capacitor in a cycle are considered. For the capacitors, as shown as equation (3-16), the average current of i_{cs} and i_c are only 1/3 of the output current; meanwhile, each diode only conducts the current in half cycle, and low forward voltage diodes are selected. The total loss in a cycle will be

$$P_{loss} = 9 \times \frac{1}{2} V_F \frac{I_o}{3} + \frac{1}{2} {I_o}^2 R_{DS} + \frac{1}{2} (\frac{I_o}{3})^2 R_{DS} + 4 \times \frac{1}{2} (\frac{I_o}{3})^2 R_{esr} \qquad (3\text{-}17)$$

In this chapter, forward voltage V_F is low and $= 0.5V$. Therefore, the power efficiency will be

$$\eta = \frac{P_o}{P_o + P_{loss}} \tag{3-18}$$

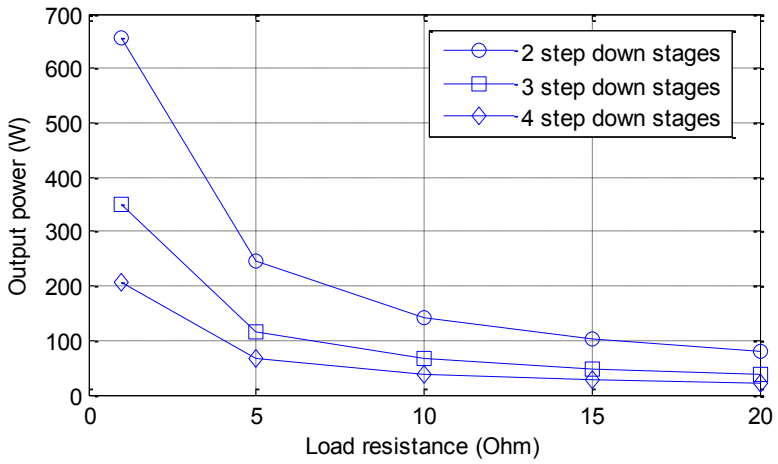
Based on equation (3-17), a more general principle can be drawn as follows:

$$P_{loss} = 3m\frac{1}{2}V_F\frac{I_o}{m} + \frac{1}{2}I_o{}^2R_{DS} + \frac{1}{2}(\frac{I_o}{m})^2R_{DS} + (m+1)\frac{1}{2}(\frac{I_o}{m})^2R_{esr} \tag{3-19}$$

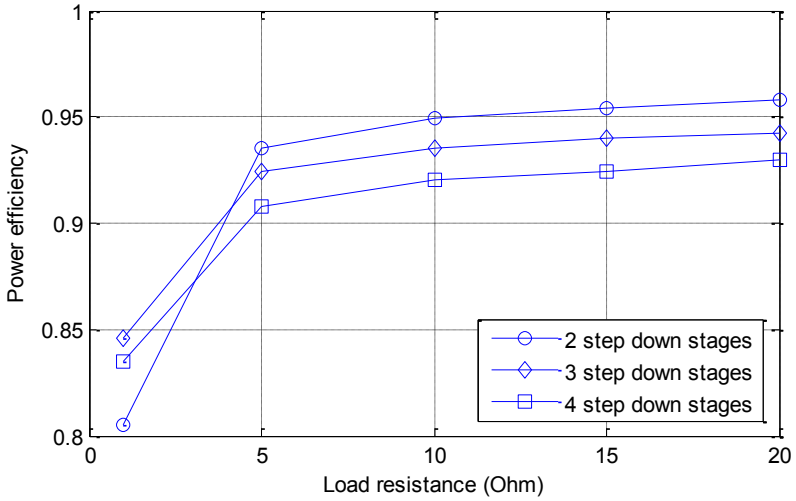
and it is reduced to:

$$P_{loss} = \frac{I_o{}^2}{2}[\frac{1}{m^2}R_{DS} + \frac{m+1}{m^2}R_{esr}] + \frac{I_o}{2}(3V_F + I_oR_{DS}) \tag{3-20}$$

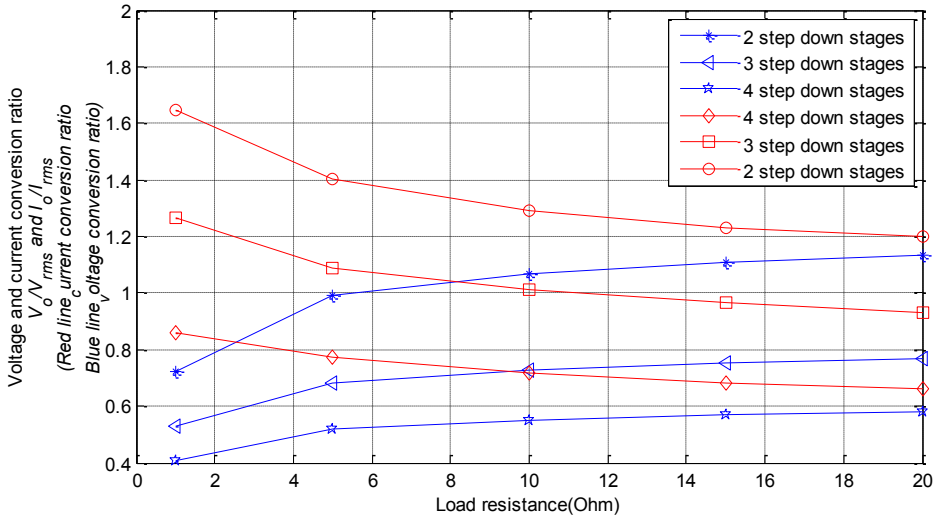
where, m is the number of SC elements. As it can be seen, increasing step down cascades does not increase the power loss in theoretical analysis. As shown in Fig. 3-8, output power, power efficiency, current and voltage conversion ratio are illustrated. Fig. 3-8 (a) shows that the step down stages when small load resistance affects the output power much more than when the load resistance is large. Power efficiencies of different stages are shown in Fig. 3-8(b). It also shows that the number of step down cascades do not affect the power efficiency very much. Power efficiency of three step down stages is only around 1.5% lower than that of two step down stages. Power efficiency of four step down stages is also around 1.5% lower than that of three step down stages, when the load resistance is larger than 4 Ω. Power efficiency decreases quickly when the load resistor is smaller than 5 Ω, because when the circuit operates under heavy load, the inductor L_s is also playing the role of storage and transferring energy, which introduces additional power consumption, and may make the voltage conversion more than 1 when there are two step down stages as shown in Fig. 3-8 (c).



(a) Output power versus load resistance in different step down stages



(b) Power efficiency versus load resistance in different step down stages

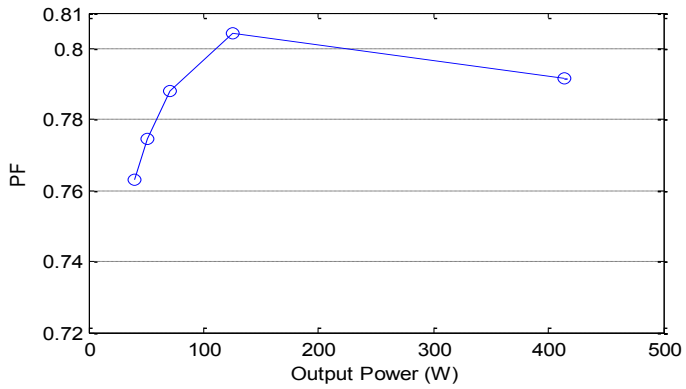


(c) Current and voltage conversion ratio versus load resistance in different step down stages.

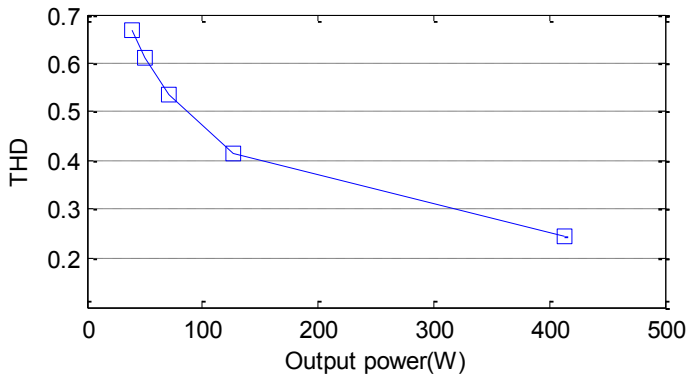
Fig. 3-8 Output power, power efficiency, current and voltage conversion ratio in different step down stages.

7) Power factor and THD

The input current is non-sinusoidal because of the nonlinear characteristics of the circuit with two resonant frequencies f_{01} and f_{02}. The input current is equal to three different amplitudes and frequencies in superposition. Because of a conduction angle of the input current and the buffer capacitor C_s, the power factor of the proposed circuit is not very good. The PF and THD of the proposed circuit are shown in Fig. 3-9. When the output power is around 125W, the PF is the largest as shown in Fig. 3-9 (a). The THD is shown in Fig. 3-9(b). Comparing Fig. 3-8 and Fig. 3-9, the best performance is at 125W. The power efficiency is above 90% as shown in Fig. 3-8.



(a) The PF of proposed circuit



(b) The THD of input current

Fig. 3-9 The THD and PF of proposed circuit

3.6 Experimental Results

The performance of the proposed circuit is verified by the experiment. The source is emulated by a signal generator and a high frequency amplifier which is programmed to generate a frequency of 50kHz and an amplitude of 50V. The value of the switch capacitor is 6.8μF, and the buffer capacitor is also 6.8μF. Resonant inductor L_r is 0.5μH, which is formed by parasitic inductance of the capacitors with each around 1.5μH and connected in parallel. The load is variable and ranges from 1 to 20 Ω. The circuit is simple with a few components. Low forward voltage diodes and low on resistance MOSFET are used to reduce the power loss in the experiment. The ESR of capacitor is 0.02 Ω, the on-state resistance of MOSFET is around 0.033 Ω, and the forward voltage drop of the diode is less than 0.5V. Specifications and the part numbers are shown in Table 3-1. The prototype is shown in Fig. 3-14.

Table 3- 1. Specifications of the proposed circuit

Specifications	Input voltage	Frequency: 100kHz
		Amplitude: 50V
	Output voltage	25V
	Suggested power	125W
Part number	MOSFET: STP40 Diode2-9: VT4045 Didoe1: STPS40H100 Capacitor: 6.8μF	

Figs. 3-10, 3-11 and 3-12 show the experimental results. The source voltage and the switching signals are as shown in Fig. 3-10(a). When the source voltage is in the positive half cycle, the switch S_1 is turned on, and S_2 is turned off. When the source voltage is in the negative half cycle, S_1 is turned off and S_2 is turned on. Deadtime is not critical for the proposed circuit but has been added and achieved by RC delay circuit in the gate circuit driver.

Fig. 3-10(b) shows the current following through the capacitors C_s and C_1 and D_3. As it can be seen, at the start of a new switching cycle, in the positive half cycle, the current is zero, then the current increases slowly from zero and resonates back to zero in a resonant manner. At the start of the negative half cycle, there is no current following through capacitor C_s because the voltage across capacitor C_s at this moment is larger than the source voltage, then it starts resonance in a resonant cycle, which agrees with the theoretical analysis in Fig. 3-4.

The current waveform of C_1, and D_3 are also shown in Fig. 3-10(b). It is found that the current flowing through C_1 is the same as i_{cs} in the positive half wave, and is the same as the current flowing through the diode in the negative half wave, which is the same as the simulation according to the operating principle. As shown in Fig. 3-10 (b), all the diodes and switches are operated under zero current switching, while ZCS is realized

for the switches and diodes, which verified that the proposed circuit can reduce the switching energy loss.

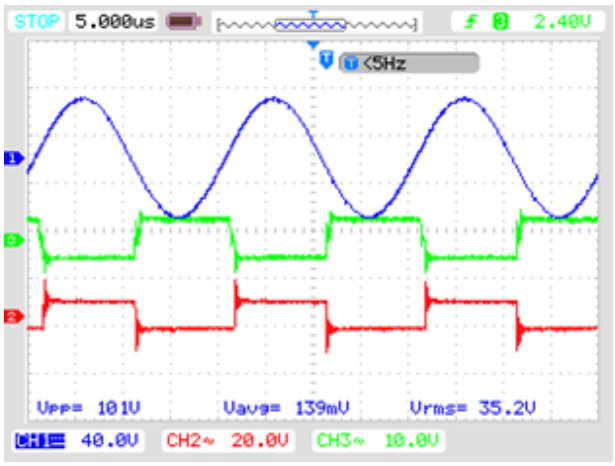
The voltage across capacitors C_s and C_1 and the output voltage V_o are measured as shown in Fig. 3-10 (c), in which the output voltage is 25.6V, the voltage across buffer capacitor C_s is about 40V, and the voltage across capacitor C_1 is the same as the output voltage V_o which is about 1/3 the sum of source voltage and the voltage across the buffer capacitor. In other words, the experimental results verified the theoretical analysis.

The experimental and the theoretical results of the output power and power efficiency are shown in Fig. 3-11 and Fig. 3-12. On-state resistance of MOSFETs and forward voltage of diodes are considered in the simulation analysis for comparison.

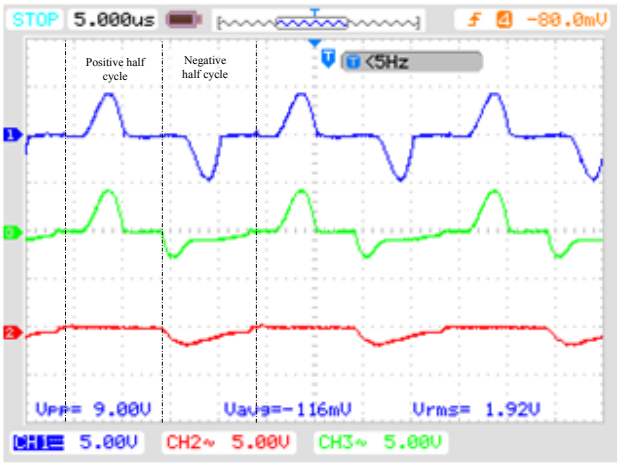
Fig. 3-11 shows the conversion ratio of the proposed circuit. The voltage and current conversion ratio between output and the rms of input is measured when the load varies from 1-20 Ω. The conversion voltage regulation range increases from 0.53 to 0.77 when the output power ranges from 37.1W to 349.6W for the theoretical analysis, which is from 36.3W to 341.2W in the experiment, as shown in Fig. 3-12.

Power efficiency of the proposed circuit is measured when the load varies from 1-20 Ω, as shown in Fig. 3-13. The efficiency of the total electrical system is measured, which is 94.2% to 84.6% in the simulation result. Comparing the experimental result with the

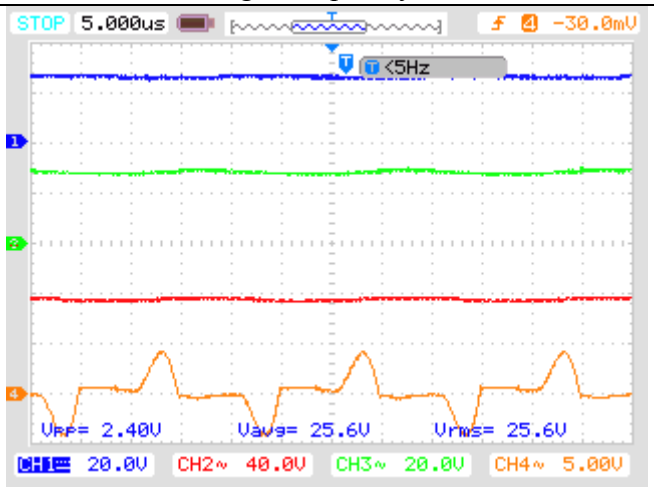
theoretical analysis, which is from 91.6% to 84.1%, the difference between the two numbers is less than 3%. The power efficiency could be further improved when the system is integrated into a chip in future.



(a) Ch 1: V_s, Ch2: Switching signal S_1; Ch3: Switching signal S_1)



(b) The current following through capacitors C_s, C_1, and D_3



(c) The voltage across capacitors C_s and C_1 and the output voltage Vo and current flowing through Ls (Ch1: V_o; Ch2: V_{cs}; Ch3: V_{c1}； Ch4: i_{Ls})

Fig 3-10. Experimental waveforms of the proposed converter

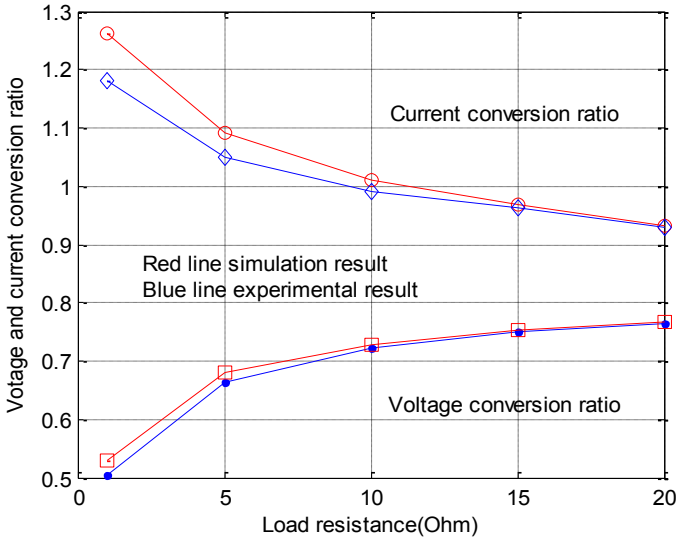


Fig. 3-11 Voltage and current conversion ratios versus load resistance

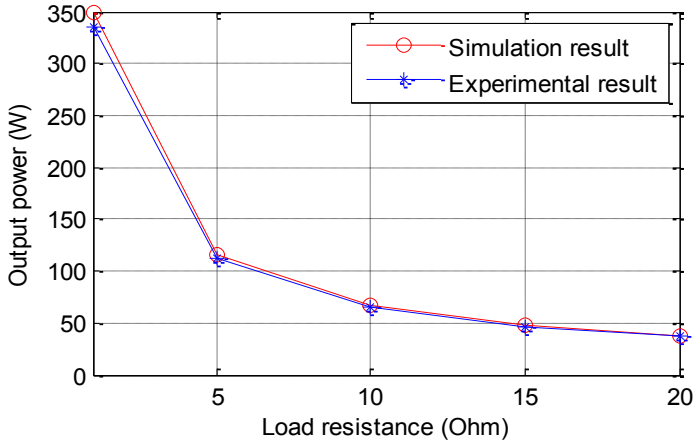


Fig. 3-12 Output power versus load resistance

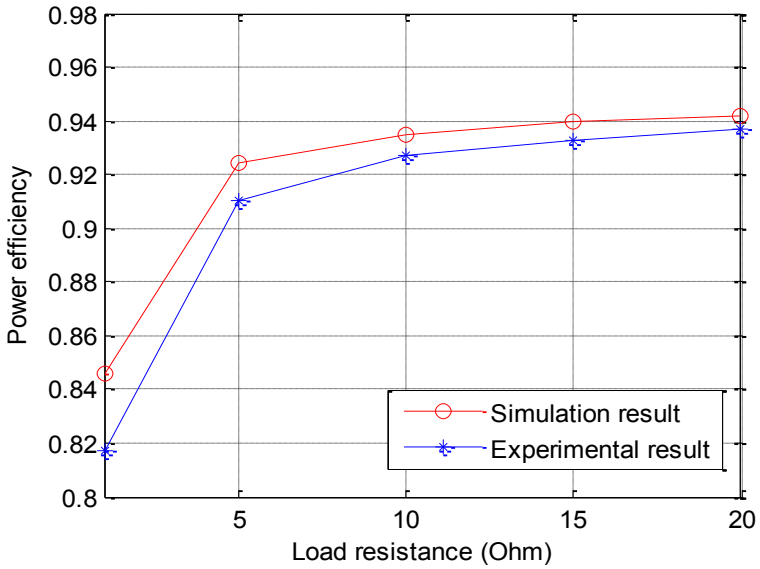


Fig. 3-13 Power efficiency versus load resistance

3.7 Summary

An ac-dc cascade step up/down converter based on switched-capacitor principle has been proposed. In the proposed circuit, capacitor and diode are integrated into step up/down module, which can be replaced and plugged in and out of the converter. Therefore, it is easy to maintain and to adjust the output voltage by this modular connection. Design and test up to 50kHz has been examined. Resonant inductors are used to reduce the current spike which highly reduce the current stress of the component and extend the life of the converter. The transistor gate signal is simple and easy to achieve. Only a pair of complementary signals which synchronize with the input voltage. Overall result is promising for the future high frequency AC distribution.

Chapter 4

Resonant Cascade Step Up/Down AC/DC Converter for High Frequency Distribution

4.1 Introduction

The conventional 400Hz AC power distribution system cannot satisfy the high power demands of the latest space applications. 20kHz AC distribution was proposed by NASA for space application decades ago [3]. The advantages of highly efficient, reliable and fewer conversion steps as compared with other power distribution architectures are the main features. Due to the significant merit of the high frequency AC power distribution system, it has been proposed for space applications [3, 16, 87], electrical vehicles [88], telecommunication and computers [2, 119], lighting [120], aircraft [109], ships [17] and many other power applications [121-123] to achieve small size, low cost, high power density, high efficiency and fewer components. The high frequency sinusoidal wave power line has been studied widely to be a potential development due to small EMI, effective reduction of components and production size, and high efficiency and power density [21, 124].

AC-DC power conversion is always an important research for power conversion. A new method in filters and circuits has been proposed [125-126]. AC-AC and DC-AC

power converter topologies for high frequency have been proposed for front end power transfer [24, 127]. A resonant network was used to reduce harmonics and power loss. Meanwhile, at a point of high frequency loading, AC-DC power converter topologies are also investigated for the high frequency power line [24, 68, 116]. Series and parallel resonant networks have been used in the circuit to reduce the power loss and increase power efficiency and also to improve the power factor. However, many different power levels from 5V to hundreds of Volt have been reported in different power application areas in EV, HID, LED, telecommunications, and battery charging systems that challenge traditional power converters. Most traditional AC-DC power converters are constructed with an AC-DC and a DC-DC converter, which contains a bridge rectifier, filter, and DC-DC converter, which is quite mature, but still, there are unsuitable applications and substantial update on designs and conversion flexibility is needed. In the 1980s, Oota and Marusarz brought up switched capacitor based AC-DC power converters [70, 128]. It has been thoroughly studied by Tse [71], Mak [72], Ioinovici [73], and Cheng [74, 76, 77, 129]. They proposed solutions to voltage regulation and high current spikes. Various SC based AC-DC power converters were developed and improved the power efficiency. The resonance method of [74, 76, 77, 129] is derived from quasi-resonance [76]. Meanwhile, transformerless and rectifierless AC-DC converters have been proposed in [78, 80, 85], in which an inductor as an energy

storage component is used as buffer energy devices. Recently, the high power switched-capacitor has been revisited and is using non-inductor based version [81-85]. The switch capacitor based power converter has been proposed to replace traditional converters. In such circuits, the absence of magnetic elements can highly reduce the size of the device compared with conventional switched power converters. High charging and discharging current spikes are decreased by introducing small resonant inductors [74, 77, 129], which significantly reduce power loss and increase efficiency and power density. Line regulation strategies and the output ripple reduction method are also incorporated into SC converters to improve the performance of power circuits [81, 83]. The AC-AC, and AC-DC converters are also implemented with SC elements or a cascade stage to step down the input voltage [78, 80-85]. The widely used resonant and output regulation techniques have prompted new areas of SC application. Especially, the diode capacitor multiplier and divider are easily integrated to realize high power density and lower profile power converters.

This chapter proposes a concept of AC-DC step up/down circuit for different output voltage levels, creating a low cost, high efficiency and easy to maintain AC-DC step up/down circuit. A capacitor and diode module form resonant SC capacitor circuit with simple driving and no bridge and buffer inductor are used.

4.2 The Construction of the Proposed Circuit

The proposed circuit consists of a step up pre-stage, step down post-stage and output filter capacitor, which are connected in series by using two MOSFETS, as shown in Fig. 4-1. The two switches are turned on and off alternately. S_1 is turned on in the positive half cycle of the source; S_2 is turned on in the negative half cycle of the source, which is shown in Fig. 4-2(a). Both operation states and switching controller is simple.

The voltage is stepped up by introducing a cascaded step up module, as shown in Fig.4-2(b) and stepped down by a cascaded step down module, as shown in Fig. 4-2(c). Both cascaded step up and step down modules are constructed by capacitors and diodes, which can be integrated and are easy to replace, plugged in and out. The voltage level is different with different cascaded modules, which are also able to give multiple outputs. The voltage gain of the step up module is 2n and the voltage gain of the step down module is 1/m. The overall voltage gain is then 2n/m in which n and m are positive integers. The detail of the voltage conversion of each module is described in Section 4.3.1 and 4. 3.2.

The converter size and cost are possible to be reduced due to the potential compact structure. In order to reduce the current stress upon the components during charging and discharging the capacitors, three small inductors are used to form a resonant circuit in order to achieve zero current switching (ZCS) [27].

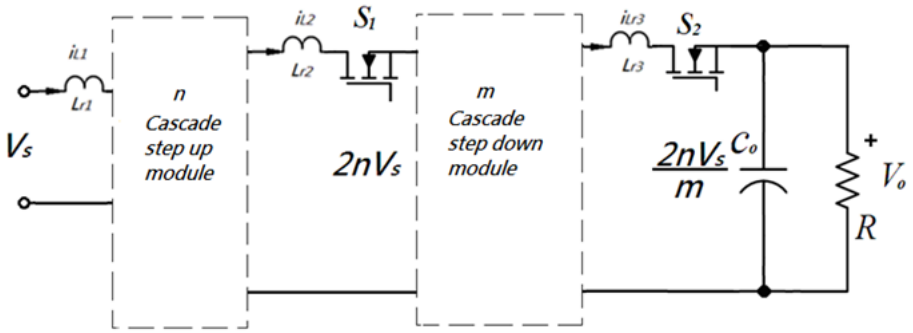
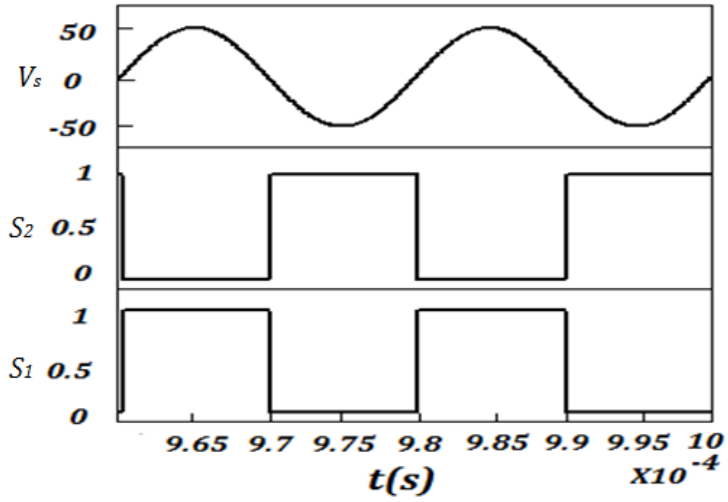
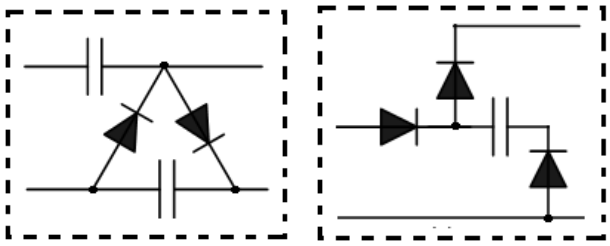


Fig. 4-1 Block diagram of the proposed circuit



(a) The source voltage and the driving signal



(b) Step up cell (c) Step down cell

Fig. 4-2 The source voltage, the driving signal and cascade module

4.3 Construction and Principle of the Proposed Circuit

A step up cell of double conversion ratio and step down cell of 1/3 conversion circuits are presented in Fig. 4-3. The circuit can be split into a cascaded step up module and a

cascaded step down module, which is a voltage multiplier and a switched capacitor step down converter including the output filter. Small resonant inductors provide quantified values rather than unknown leakage circuit inductances are introduced to reduce the current stress of the components.

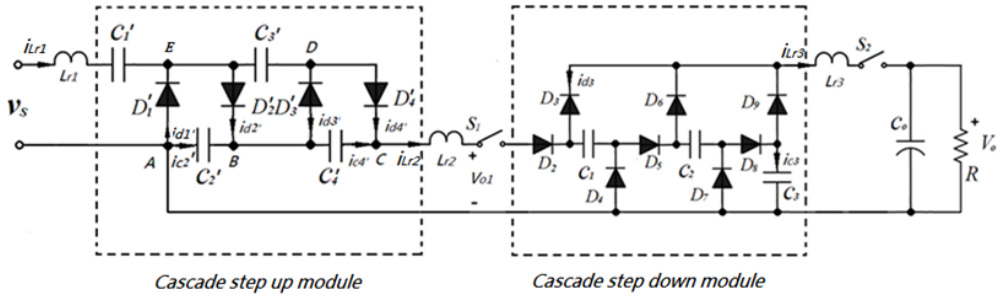


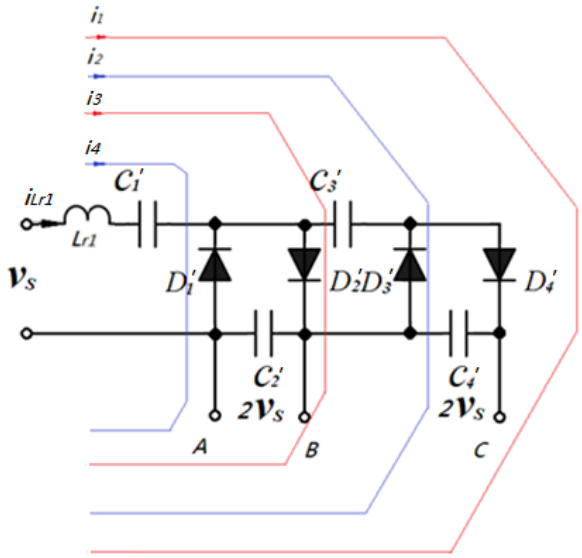
Fig. 4-3 A two step up cells, three step down cells switched capacitor ac/dc converter

4.3.1 Cascaded Step Up n Module

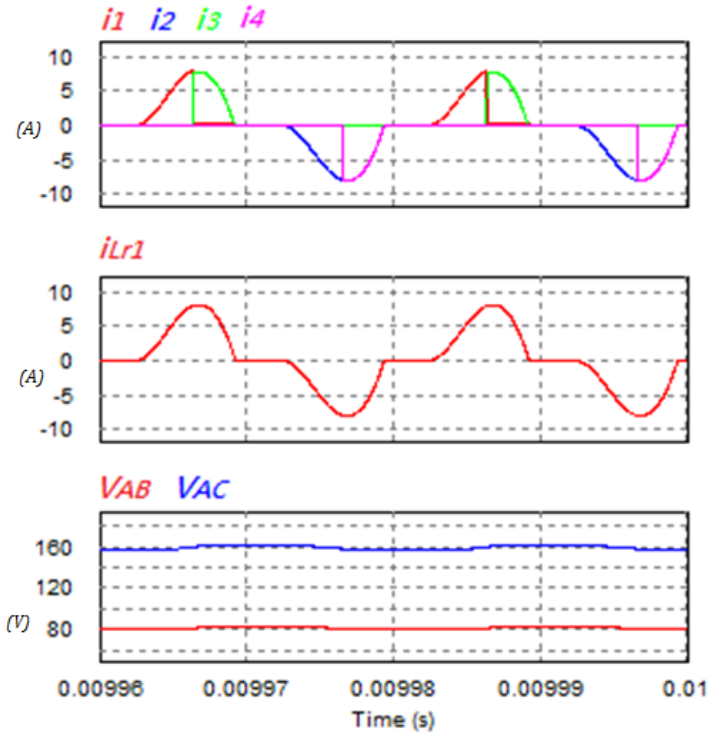
As shown in Fig. 4-3, the cascaded step up module is a half-wave series voltage multiplier, which is chosen as the pre-stage to step up the input voltage as shown in Fig. 4-4(a) with no driving signal needed. By plugging in different cascade stages, the 50V, 50 kHz high frequency ac input voltage should be step up to different voltages. As shown in Fig. 4-4 (a), by flexibly choosing different connection point AB or AC, the step down converters can be easily connected to achieve different output voltages.

The capacitors C_1' and C_3' are slowly charged through diodes D_1' and D_3' in turn, the current increases slowly from zero and resonates back to zero as shown in Fig. 4-4 (b), which reduces the stress to the diodes and capacitors. The input voltage is stepped up

through the stepping effect of coupling capacitors C_1', C_3', C_2' and C_4'. The stepped up voltage is an even multiple of input voltage. The voltages between A, B and A, C are $2V_s$ and $4V_s$ respectively, shown in Fig. 4-4(b). i.e. the conversion ratio is 2n.



(a) A two stage ac voltage multiplier



(b) The current and voltage of a two step up cells module

Fig. 4-4 The construction and waveforms of voltage multiplier

4.3.2 Cascaded Step Down m Module

The cascaded step down module is actually a multistage switched capacitor divider converter including the output filter, as shown in Fig. 4-3. The input voltage is stepped down by voltage dividers which are constructed by capacitors and diodes shown in Fig. 4-2(c).

The input voltage and driving signal are turned on and off complementarily, as shown in Fig. 4-2(a). The step down cells are connected in series and the capacitors C_1, C_2 and C_3 are charged in series when S_1 is turned on in the positive half cycle of the input voltage, the charging currents i_{Lr2} which is also the current passing through the switch 1. S_1 is zero when the switch 1, S_1, is turned off as shown in Fig. 4-5(b), then ZCS is achieved because resonant inductor L_{r2} is added. Simultaneously, the capacitors C_1, C_2 and C_3 release energy in parallel when S_2 is turned on in the negative half cycle of the input voltage, as shown in Fig. 4-5(a). The voltage is stepped down to $4V_s/3$, i.e. the conversion ratio is $1/m \times 4V_s$. The discharging current i_{Lr3} is also zero at the point when the switch 2 is turned on and off because the resonant inductor L_{r3} is introduced as shown in Fig. 4-5(b). Therefore, all of the switches are working under zero current switching modes and the current stress of the diodes is also released.

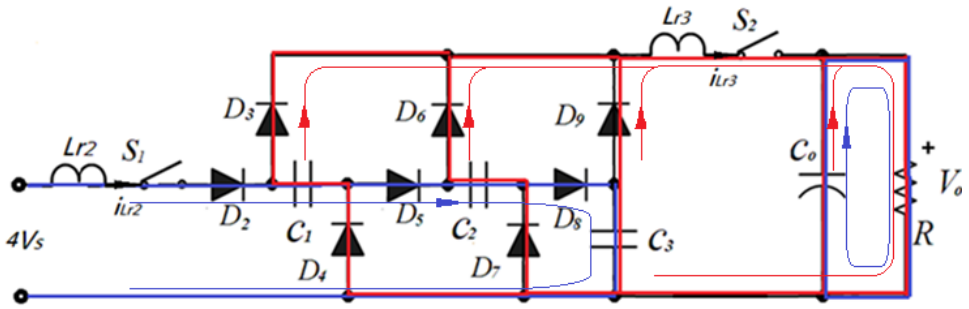


Fig. 4-5 (a) Three stages step down converter

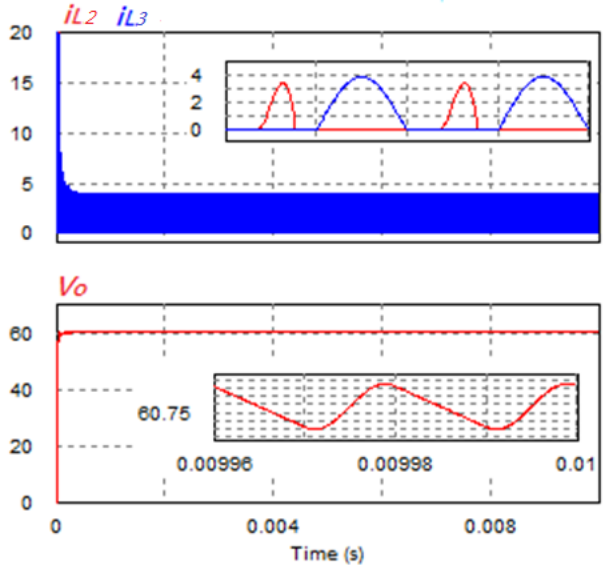


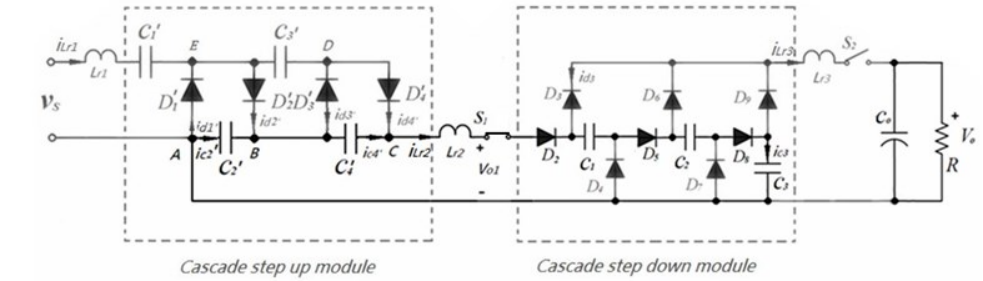
Fig. 4-5(b) The current of resonant inductor and the output voltage

Fig. 4-5 The construction and waveform of voltage divider

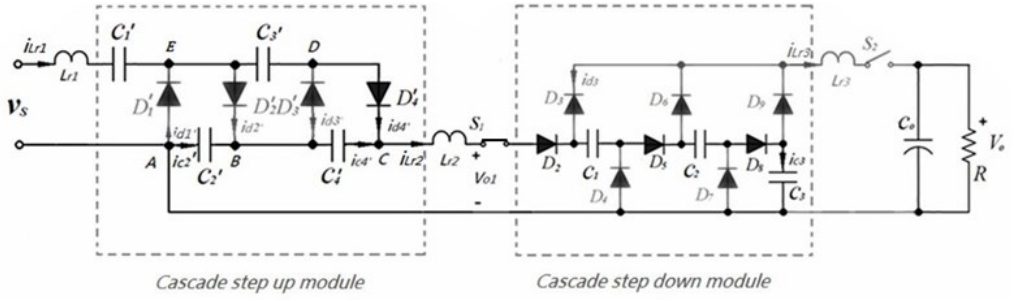
4.3.3 Operation Principle and Analysis of the Proposed Circuit

The operation modes and the operation states are shown in Fig. 4-6. The waveforms of the current and voltage of the proposed circuit are illustrated in Fig. 4-7. As it can be seen in Fig. 4-7(a), the voltage is firstly stepped up by the cascaded step up module to $4V_s$, and then is stepped down by the cascaded step down module mentioned above to $4V_s/3$. The input current, which is also the current flowing through resonant inductor L_{r1}, increases slowly and then resonates back to zero in half cycle of the source voltage. A similar operation is found in next half cycle of source voltage, as shown in Fig.

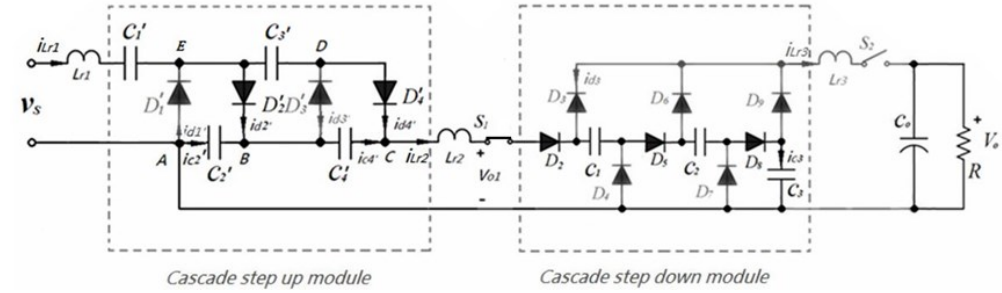
4-7(b).



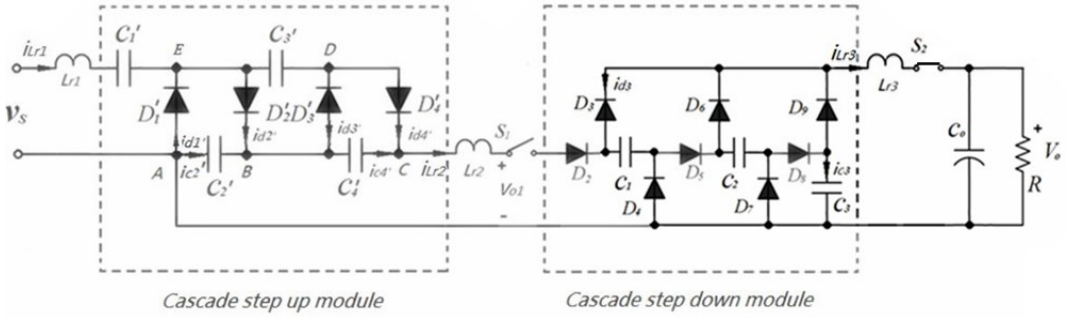
(a) State 1



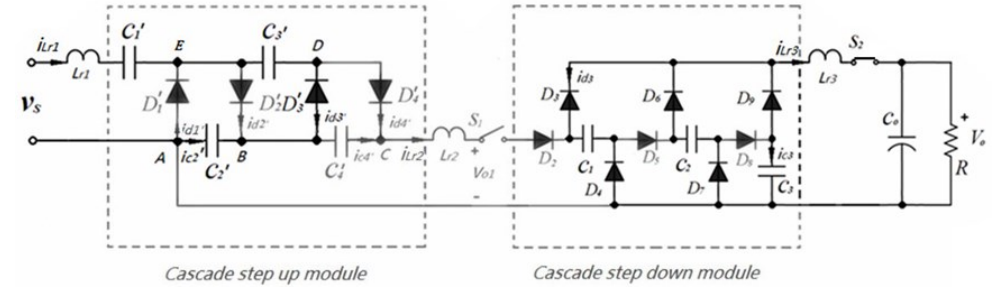
(b) State 2



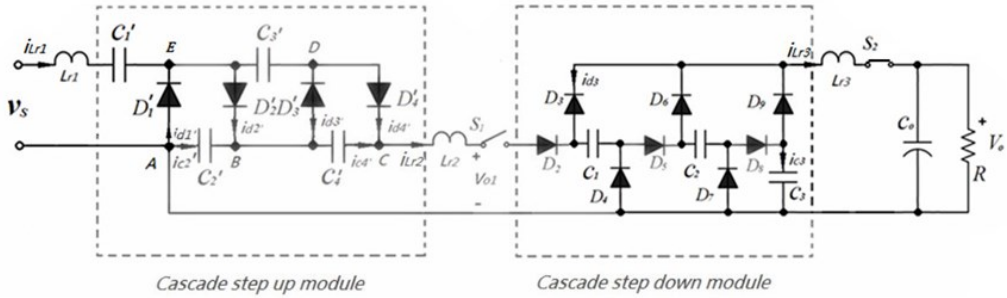
(c) State 3



(d) State 4

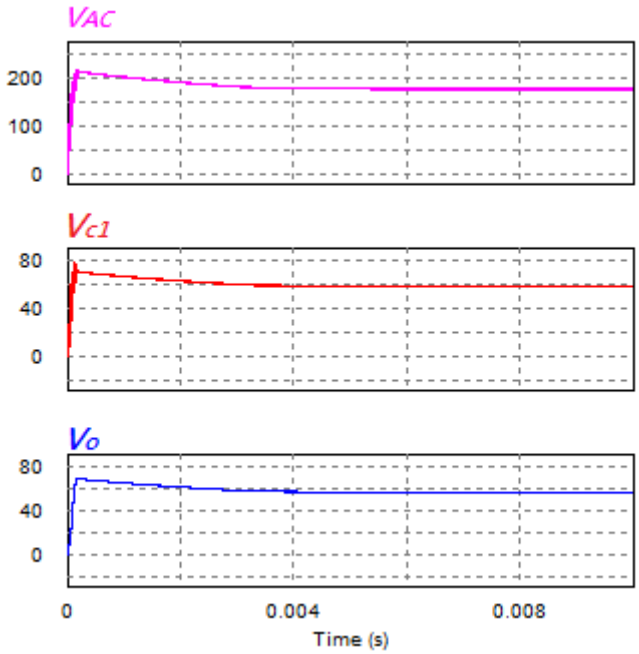


(e) State 5

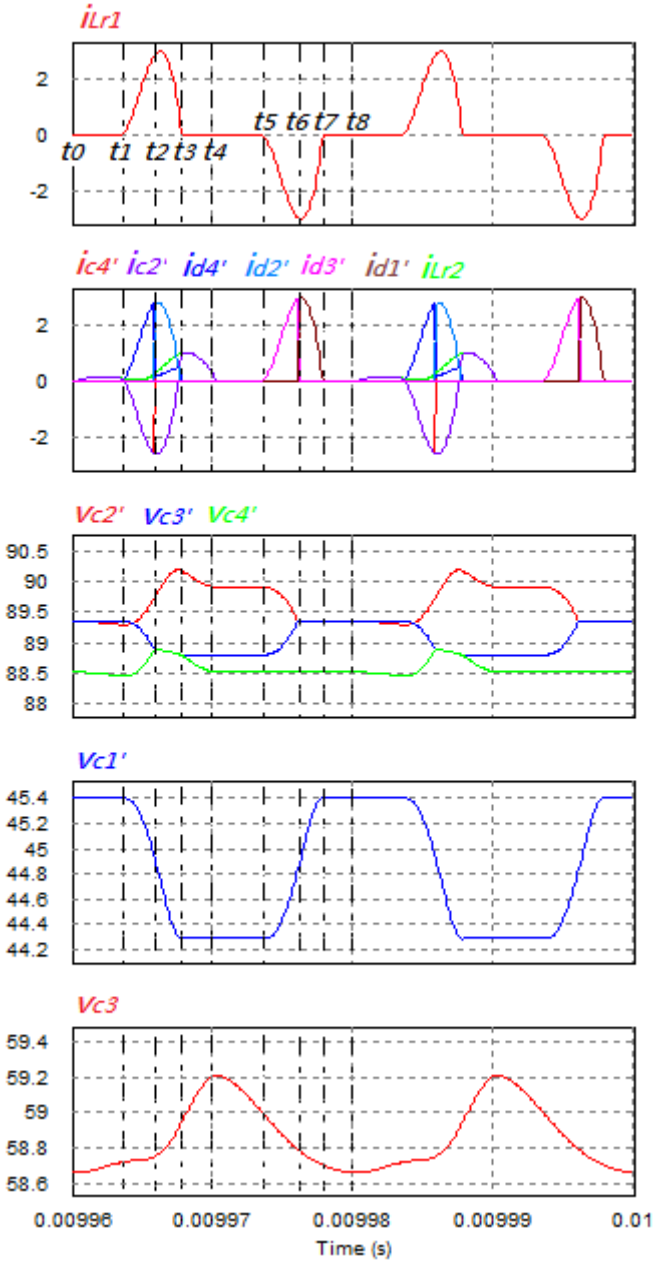


(f) State 6

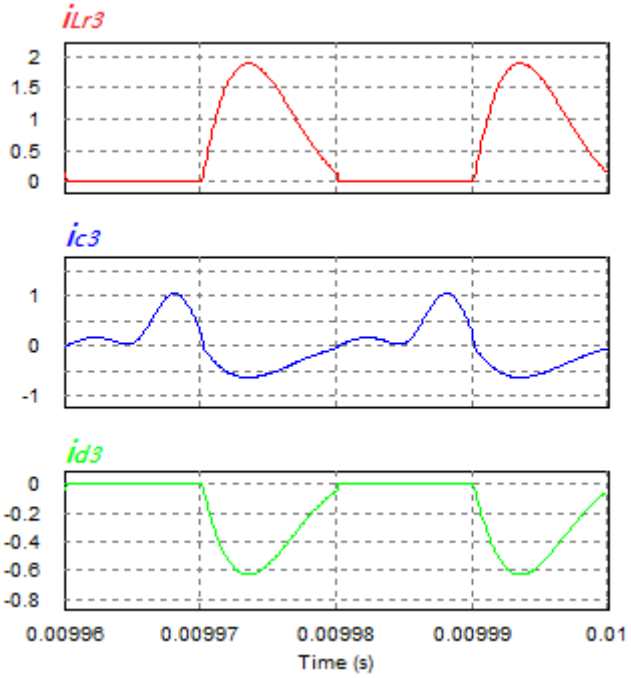
Fig. 4-6 The detailed operation states of the proposed circuit



(a)


iLr1
2
0
-2
t0 t1 t2 t3 t4 t5 t6 t7 t8
ic4' ic2' id4' id2' id3' id1' iLr2
2
0
-2
Vc2' Vc3' Vc4'
90.5
90
89.5
89
88.5
88
Vc1'
45.4
45.2
45
44.8
44.6
44.4
44.2
Vc3
59.4
59.2
59
58.8
58.6
0.00996
0.00997
0.00998
0.00999
0.01
Time (s)

(b)



(c)

Fig. 4-7 The waveform of the current and voltage of the proposed circuit

The detailed description of the operation and analysis is as follows. Assume $V_s \sin\omega t$ is the source voltage; i_{Lr1}, i_{Lr2}, i_{Lr3}, i_{c2}', i_{c4}' i_{d1}', i_{d2}' i_{d3}', i_{d4}', $i_{d3,}$ i_{c3} are the currents flowing through the inductors $L_{r1,}$ L_{r2}, L_{r3}, and the capacitors C_2', C_4', C_3 and the diodes D_1', D_2', D_3', D_4', $D_{3,}$ respectively. L_{r1}, L_{r2} are the resonant inductors. The capacitances of C_1', C_2' C_3', C_4', C_1, C_2 and C_3 are assumed equal to C. The steady state operation can be classified into two modes: Mode A, the source is working in the positive half cycle and Mode B, the source is working in the negative half cycle.

1) Mode A (t_0-t_4): S_1 is on and S_2 is off. The circuit is working in the positive half cycle of the source voltage. There are four stages but only three operation states in this period. The circuit is going through state 1 to state 2 and 3 and back to

state 1.

a) Stage 1(t_0-t_1): the circuit is working in state 1. As shown in Fig. 4-6(a), when the sum of source voltage and voltage across C_1' is smaller than the voltage across C_2', both D_1' and D_2' are reverse biased. When the sum of source voltage, voltage across C_1' and voltage across C_3' are smaller than V_{AC}, which is larger than the sum of voltages of the capacitors C_1, C_2 and C_3, then D_3' and D_4' are reverse biased. Then the currents following through diode L_{r1}, and D_1', D_2', D_3', and D_4' are zero, as shown in Fig. 4-7(b), till the sum of source voltage and voltage of capacitors C_1' and C_3' is larger than V_{AC}. Capacitors C_2' and C_4' are charging capacitors C_1, C_2 and C_3 in series. The current of the inductor i_{c2}' which is equal to i_{c4}' and the current of the inductor i_{Lr2} starts to increase slowly from zero, and the voltages of v_{c2}' and v_{c4}' are decreasing slowly, $i_{c2'} = i_{c4'} = i_{Lr2}$, which is shown in Fig. 4-7(b), then there is

$$\begin{cases} v_{c2'} + v_{c4'} - 3\left(L_{r2}\frac{di_{Lr2}}{dt} + v_{c1}\right) = 0 \\ i_{c2'} = -C\frac{dv_{c2'}}{dt} \\ i_{c4'} = -C\frac{dv_{c4'}}{dt} \\ i_{Lr2} = C\frac{dv_{c1}}{dt} \end{cases} \tag{4-1}$$

b) Stage 2 (t_1-t_2): the circuit is working in state 2. As shown in Fig. 4-6(b), when the sum of source voltage and voltage across C_1' is smaller than the

voltage across C_2', both D_1' and D_2' are reversely biased; meanwhile, when the sum of source voltage and voltages across C_1', C_3' is larger than V_{AC}, and V_{AC} is equal to the sum of voltage of the capacitors C_1, C_2 and C_3, then the source and the capacitors C_1' and C_3' are connected in series and start to charge capacitors C_2' and C_4'. Capacitors C_1, C_2, C_3 are now in parallel. The current of the inductor i_{Lr1} starts to increase slowly from zero, which is equal to the sum of currents of the inductor i_{c2}' and i_{Lr2}, the voltages of v_{c1}' and v_{c3}' are decreasing slowly. The voltages of v_{c2}' and v_{c4}' are increasing, $i_{Lr2} = i_{d4}' + i_{c2}'$, $i_{d4}' = i_{Lr1}$, $i_{c2}' = C\frac{dv_{c2}'}{d(t-t_1)}$, $i_{Lr1} = C\frac{dv_{c3}'}{d(t-t_1)}$, which is shown and Fig. 4-7(b), then there is

$$\begin{cases} V_s\sin\omega t + (L_{r1}\frac{di_{Lr1}}{d(t-t_1)} + v_{c1'}) + v_{c3'} - (L_{r2}\frac{di_{Lr2}}{d(t-t_1)} + 3v_{c1}) = 0 \\ L_{r2}\frac{di_{Lr2}}{d(t-t_1)} + 3v_{c1} = v_{c2'} + v_{c4'} \\ i_{Lr1} = C\frac{dv_{c1}'}{d(t-t_1)} \\ i_{Lr2} = c\frac{dv_{c1}}{d(t-t_1)} \end{cases} \quad (4\text{-}2)$$

c) Stage 3(t_2-t_3): The circuit is working in state 3. The source voltage is increasing and the sum of source voltage and voltage across C_1', is larger than the voltage across C_2'. The diode D_2' is on, and the voltage across C_3' and C_4' is the same. Then D_4' is on. The source voltage and capacitor C_1' start to charge capacitor C_2'. Meanwhile, capacitors C_3' and C_4' in parallel are charging capacitors C_1, C_2 and C_3 in series, the current of the inductor

i_{Lr1} starts to decrease slowly, and resonant back to zero, which equals to sum of $i_{d2}{}'$ and $i_{d4}{}'$. The current $i_{d4}{}'$ is equal to $i_{c4}{}'$. The current $i_{d2}{}'$ is equal to the sum of current flowing through capacitor $C_2{}'$ and the capacitor $C_4{}'$. $i_{d4}{}' = i_{d2}{}' + i_{c2}{}'$, $i_{Lr1} = i_{d4}{}' + i_{d2}{}'$, $i_{Lr2} = i_{d4}{}' + i_{dc4}{}'$, $i_{d4}{}' = C\frac{dv_{c3}{}'}{d(t-t_1)}$, $i_{c2}{}' = C\frac{dv_{c2}{}'}{d(t-t_1)}$, $i_{c4}{}' = C\frac{dv_{c4}{}'}{d(t-t_1)}$, as shown in Fig. 4-6(c) and Fig. 4-7(b), the equations of operation are

$$\begin{cases} V_s\sin\omega t + (L_{r1}\frac{di_{Lr1}}{d(t-t_1)} + v_{c1'}) + v_{c3'} - (L_{r2}\frac{di_{Lr2}}{d(t-t_1)} + 3v_{c1}) = 0 \\ v_{c3'} + L_{r2}\frac{di_{Lr2}}{d(t-t_1)} + 3v_{c1} = v_{c2'} \\ v_{c3'} = v_{c4'} \\ i_{Lr1} = C\frac{dv_{c1}{}'}{d(t-t_1)} \\ i_{Lr2} = c\frac{dv_{c1}}{d(t-t_1)} \end{cases} \quad (4\text{-}3)$$

d) Stage 4(t_3-t_4): The circuit is working back on state 1. When the source voltage is decreasing and the sum of source voltage and voltage across $C_1{}'$, $C_3{}'$ is smaller than V_{AC}, then all the diodes are reverse biased, the current following through diodes $D_2{}'$ and $D_4{}'$ is zero. V_{AC} is larger than the sum of voltages of the capacitors C_1, C_2 and C_3 because of the resonant inductor, the current of the inductor i_{Lr2} starts to decrease slowly, and resonates back to zero. The input current i_{Lr1} is zero, because there is no current flowing through. The capacitors $C_2{}'$ and $C_4{}'$ start to charge capacitors C_1, C_2 and C_3 in series again, as shown in Fig. 4-7(b). then

$$\begin{cases} v_{c2'} + v_{c4'} - 3\left(L_{r2}\frac{di_{Lr2}}{d\mathrm{t}} + v_{c1}\right) = 0 \\ i_{c2'} = -C\frac{dv_{c2'}}{d\mathrm{t}} \\ i_{c4'} = -C\frac{dv_{c4'}}{d\mathrm{t}} \\ i_{Lr2} = C\frac{dv_{c1}}{d\mathrm{t}} \\ i_{c2'} = i_{c4'} = i_{Lr2} \end{cases} \tag{4-4}$$

2) Mode B (t_4-t_8): the switch S_2 is on and S_1 is off, and it is working on the negative half cycle. During the entire negative half cycle, the capacitor is in parallel and releases energy into the load. The current is increasing slowly because of the resonant inductor L_{r3}, then resonates back to zero at the time instant t_8. The equations of operation is:

$$\begin{cases} V_o = L_{r3}\frac{di_{Lr3}}{dt} + v_{c1} \\ i_{Lr3} = 3C\frac{dv_{c1}}{dt} \end{cases} \tag{4-5}$$

The solutions are:

$$\begin{cases} i_{Lr3} = I_{m3}\sin\omega_{03}t \\ v_c = V_o - \Delta\mathrm{V}_3\cos\omega_{03}t \end{cases} \tag{4-6}$$

where, $I_{m3} = \frac{I_0 T_S \omega_{03}}{2}$, $\Delta\mathrm{V}_3 = \frac{ZI_0 T_S \omega_{03}}{2}$, ω_{03} is the resonant frequency, which is $\frac{1}{\sqrt{3L_rC}}$, $\mathrm{Z}_{03} = \sqrt{\frac{L_{r3}}{3C}}$. V_o is the output voltage. Z_{03} is the impedance.

a) Stage5 (t_4-t_5): The circuit is working on state 4. As shown in Fig. 4-6 (d), when the sum of source voltage and voltage across C_2' is smaller than the voltages across C_1' and C_3', and the source voltage is smaller than the voltage across capacitor C_1', all diodes are reversely biased. There is no current flowing through pre-stage module; all the variables keep constant.

b) Stage 6 (t_5-t_6): The circuit is working on state 5. As shown in Fig. 4-6 (e), the sum of source voltage and voltage across C_2' is larger than the voltages across capacitors C_1' and C_3', but the source voltage is still smaller than the voltage across C_1', source voltage and capacitor C_2' start to charge capacitors C_1' and C_3'. The current of the inductor i_{Lr1} starts to increase slowly, which is equal to the current flowing through capacitor C_2' and diode D_3'. The voltage across C_2' is decreasing, the voltages across C_1' and C_3' are increasing, untill v_{c2}' is equal to v_{c3}', as shown in Fig. 4-7(b). Hence ,

$$\begin{cases} V_s \sin\omega t + L_{r1}\frac{di_{Lr1}}{d(t-t_1)} + v_{c1'} + v_{c3'} + v_{c2'} = 0 \\ i_{Lr1} = i_{d3}{}' \\ i_{c2}{}' = C\frac{dv_{c2}{}'}{d(t-t_1)} \\ i_{Lr1} = C\frac{dv_{c1}{}'}{d(t-t_1)} \\ i_{Lr1} = C\frac{dv_{c3}{}'}{d(t-t_1)} \end{cases} \quad (4\text{-}7)$$

c) Stage 7 (t_6-t_7): The circuit is working on state 6, as shown in Fig. 4-6 (f). When the voltage across C_2' is equal to the voltage across C_3', which makes diodes D_1' on and D_3' off. The source is charging capacitor C_1', the current of the inductor i_{Lr1} starts to decrease slowly, and resonates back to zero. The voltage across C_1' is increasing, Voltages across C_2', C_3' and C_4' keep constant, $i_{Lr1} = i_{d1}{}'$, is shown in Fig. 4-7(b). Then,

$$\begin{cases} V_s \sin\omega(t + t_6) + L_{r1}\frac{di_{Lr1}}{dt} + v_{c1'} = 0 \\ i_{Lr1} = C\frac{dv_{c1}{}'}{dt} \end{cases} \quad (4\text{-}8)$$

d) Stage 8 (t_7-t_8): The circuit is working back on state 4. When the source voltage is decreasing and the sum of source voltage and voltage across C_2', is smaller than the voltage across C_1' and C_3', source voltage is smaller than the voltage across capacitor C_1', all diodes are reversely biased. There is no current flowing through pre-stage module; all the variables is kept constant, as shown in Fig. 4-7(b).

All the differential equations can be solved by numerical method according to the boundary conditions.

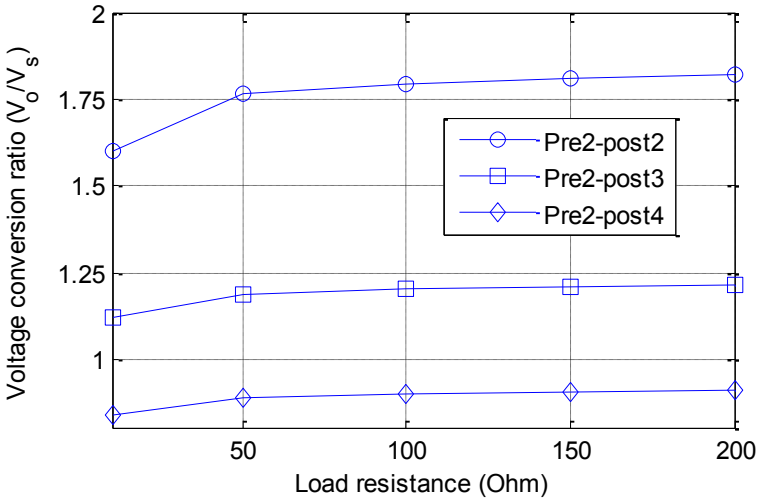
4.3.4 Performance of Different Step Up/Down Cascades

The study of different combinations of cascade modules n= 2, 3, 4 pre-step-up-stage and m=2, 3, 4 post-step-down-stage of the circuits have been carried out by PSIM 9.0 to verify the concept of the proposed circuit. As shown in Fig. 4-8 and Fig. 4-9, the voltage conversion ratio, the output power, the power efficiency for different cascades module have been presented.

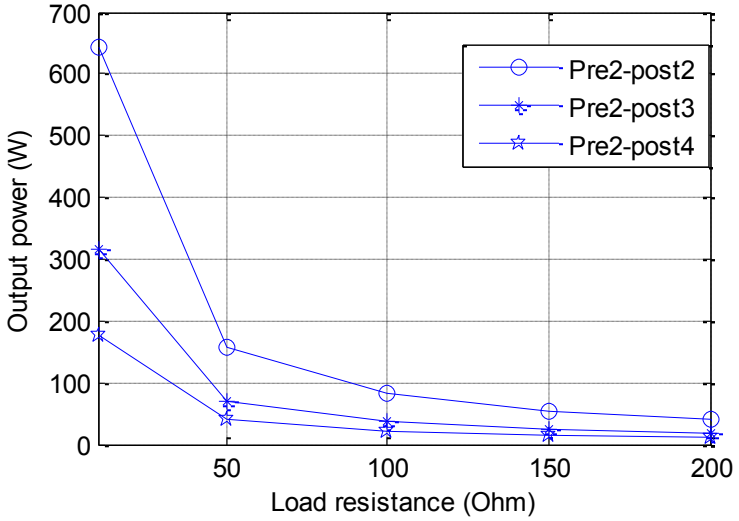
As it can be seen in Fig. 4-8, the conversion ratio, output power and power efficiency are decreasing with the number of step down stages increasing. In a fixed number of stage circuits, for example, n=2 for step-up cascades, and m=3 for step-down cascades,

the output power decreases quickly. Meanwhile, the conversion ratio and the power efficiency increase quickly when the load resistance increases from 0 to 50 Ω. Output power decreases slowly and stably. The voltage conversion ratio and the power efficiency increase slowly and stably when the load resistance increases from 50-200 Ω. Vice versa, the conversion ratio, output power and power efficiency increase with the number of pre-stages (step up stages) increasing. The more the number of step-up cascades, the quicker the output power decreases. The conversion ratio and the power efficiency increase quickly when the load resistance increases from 0 to 50 Ω. As it can be seen, when there is only one step-up cascade, the voltage conversion ratio, the output power, the power efficiency all changed more slowly than 2 and 3 step-up cascades. Output power decreases slowly and stably. Meanwhile, the voltage conversion ratio and the power efficiency increase slowly and stably when the load resistor is increasing from 50 to 200 Ω. To conclude, the proposed circuit works stable when the power is below 170W.

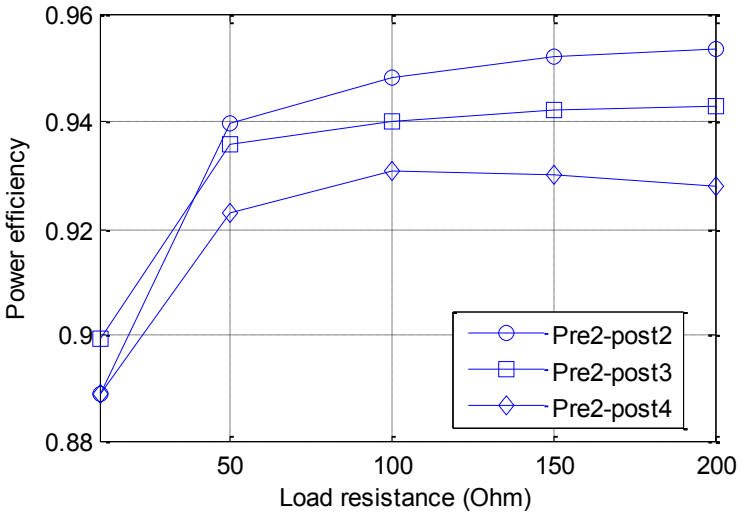
The simulation result also shows the power efficiency is above 90% and neither pre-stage or post- stage increasing will induce the power efficiency decreasing.



(a) Voltage conversion ratio versus load resistance

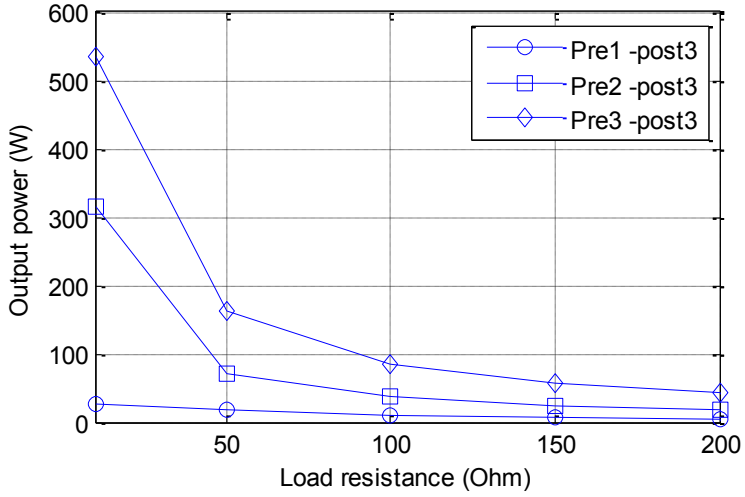


(b) Output power versus load resistance

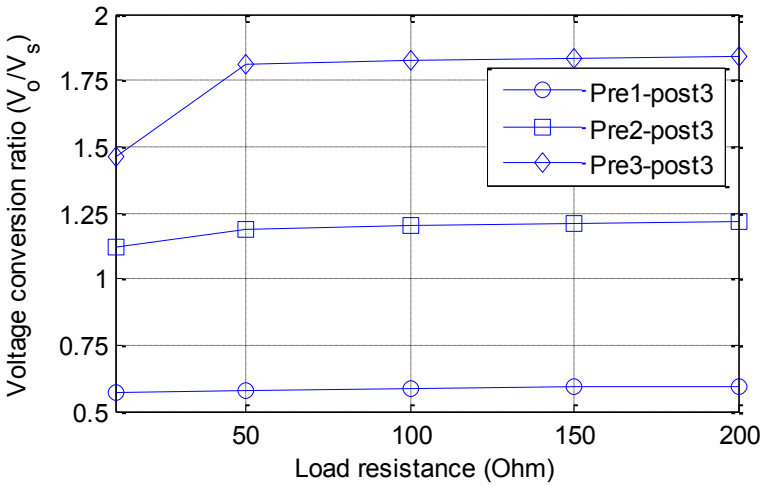


(c) The power efficiency versus output current

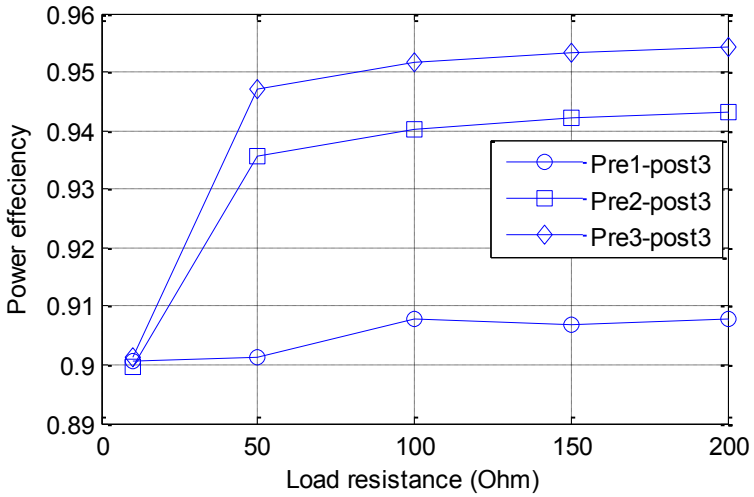
Fig. 4-8 The output power, voltage conversion ratio and power efficiency versus load resistance of n=2 to pre-stage, m=2, 3, 4 to post-stage.



(a) The output power versus load resistance



(b) conversion ratio versus load resistance



(c) The power efficiency versus output current of 1, 2, 3 pre-stage, 3 post-stage.

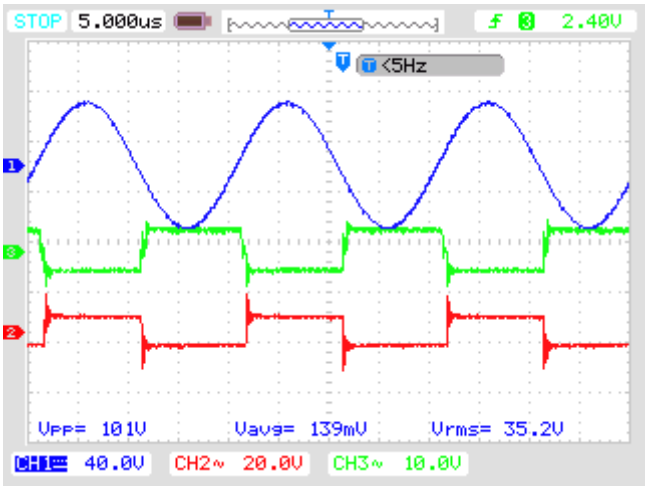
Fig. 4-9 The output power, voltage conversion ratio and power efficiency versus load resistance of n=1, 2, 3 to pre-stage, m=3 to post-stage.

4.4 Experimental Results

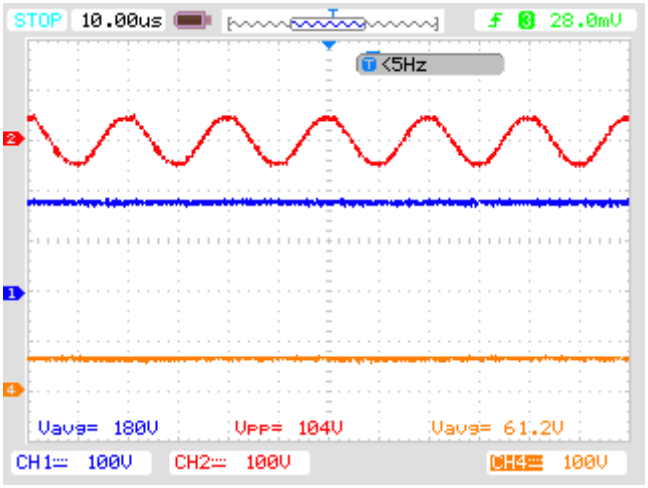
The performance of the proposed circuit is verified by the experiment. An n=2 for pre-stage, and m=3 for post-stage circuit is built to verify the performance of the circuit. The waveforms of the input voltage, output voltage, input current, resonant inductor current, power efficiency, and the power versus different loads are shown in Figs. 4-10~4-12. The power source is emulated by a signal generator and a high frequency amplifier which is programed to a frequency of 50kHz and an amplitude of 50V. The value of step down switching capacitor is 6.8μF, the capacitance of the voltage multiplier is also 6.8μF. The resonant inductors L_{r1}, L_{r2} are designed to be 3.5μF and 1.5 μF, respectively. However, in the experiment, the resonant inductor is realized by the parasitic inductor of the capacitors to achieve ZCS; the output capacitor is 47 μF. The load resistor is variable. Therefore, the circuit is very simple. The specifications and part numbers are illustrated in Table 4-1.

Table 4-1 Specifications of the proposed circuit

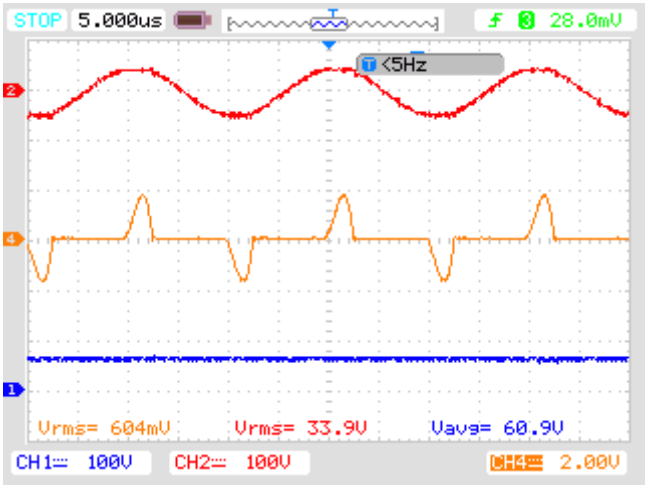
Input voltage	50kHz, 50V
Output voltage	DC 60 V
Power	100W
MOSFET	IRF640
Diode 2-9	MBR20100
Diode 1	MBR20200
All capacitors	6.8μF



(a) Ch1: input voltage; Ch2: switched signal S1; Ch3: switched signal S2

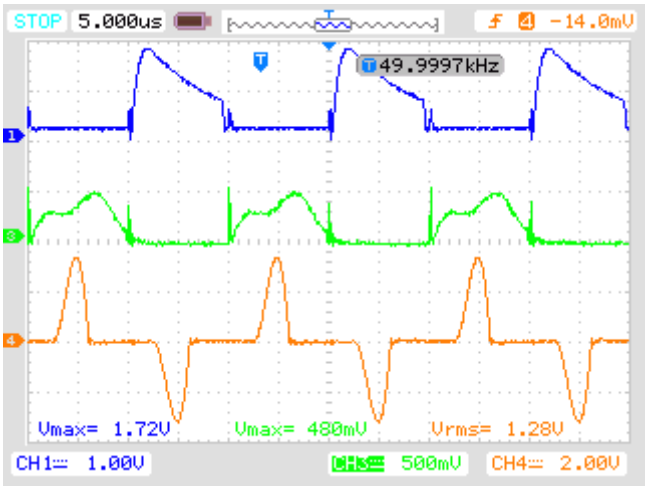


(b) Ch1: stepped up voltage Vo1; Ch2: input voltage; Ch4: output voltage

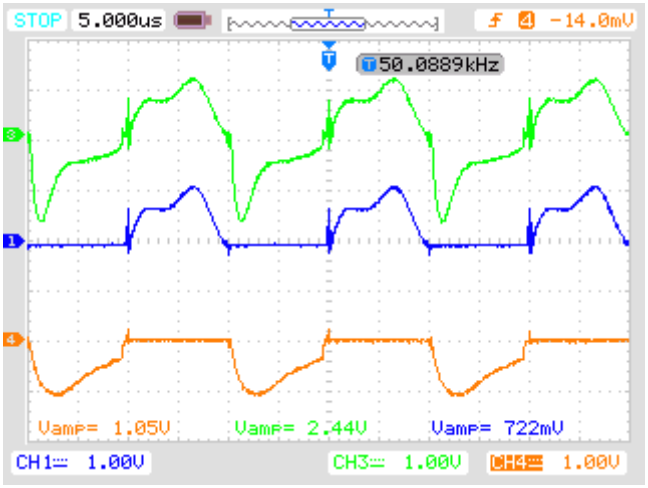


(c) Ch1: output voltage; Ch2: input voltage; Ch4: input current

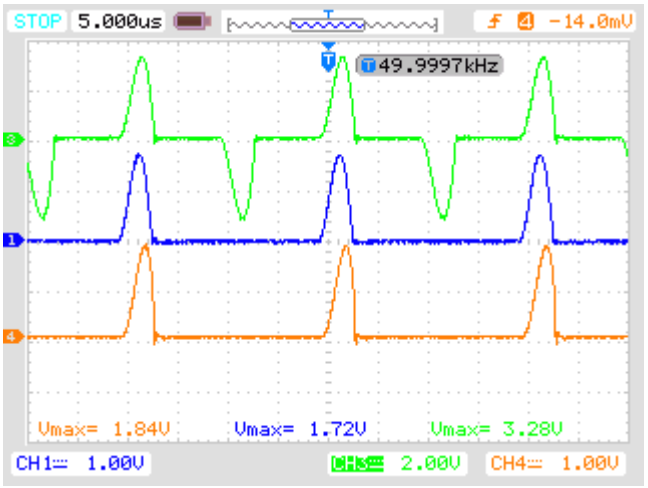
Fig. 4-10 The waveform of switched signal, input and output voltage, input current (load resistance is 200 Ω)



(a) Ch1: inductor current i_{Lr3}; Ch3: inductor current i_{Lr2}; Ch4: i_{Lr1}



(b) Ch1: inductor current iLr2; Ch3: current flowing through C3; Ch4: current flowing through D3



(c) Ch1: current flowing through D4'; Ch3: inductor current iLr1; Ch4: current flowing through D2'

(d) Ch1: current flowing through C_4'; Ch3: inductor current i_{Lr2}; Ch4: current flowing through D_4'

Fig. 4-11 The waveform of current flowing through resonant inductor, diode and capacitor (load resistance is 100 Ω)

Fig. 4-10 and Fig. 4-11 show the waveforms of the input voltage, output voltage, input current, resonant inductor current and current flowing through the diodes, respectively, when the load resistance is 200 Ω.

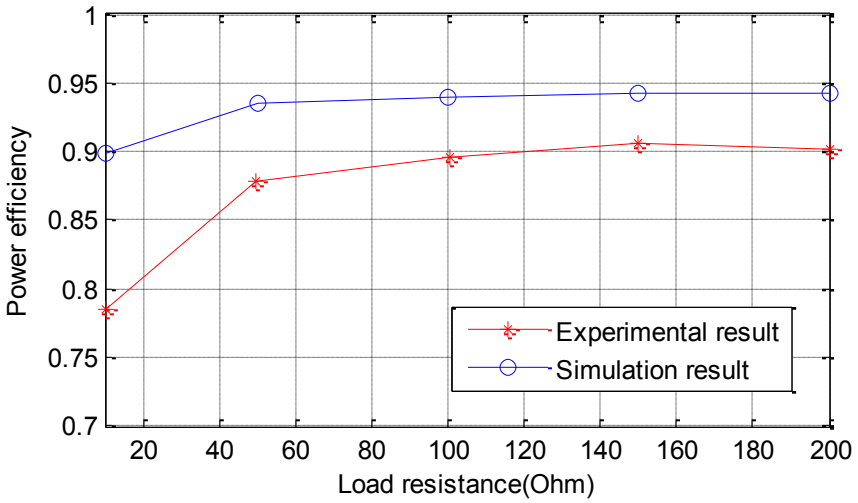
Fig. 4-10 shows the switched signal and input output voltage and current. Fig. 4-10 (a) shows that the control signal is a pair of complementary signals and is easy to achieve. As it can be seen, the switch S_1 is on when the input voltage is working on the positive half wave, and the switch S_2 is on when the input voltage in working on negative half cycle. The signals shown in Fig. 4-10 (b) and (c) are input voltage, stepped up voltage, output voltage, input current, which shows that the input voltage is first stepped up to 180V, then stepped down to 61.2V, which confirms the concept and the performance of the proposed circuit. Fig. 4-10 (c) shows the input and output voltages. In the half cycle,

the current increases from zero and resonates back to zero again because of the resonant inductors, and the input voltage is converted to $2n/mV_s$, i,.e. $2\times2/3\ V_s$

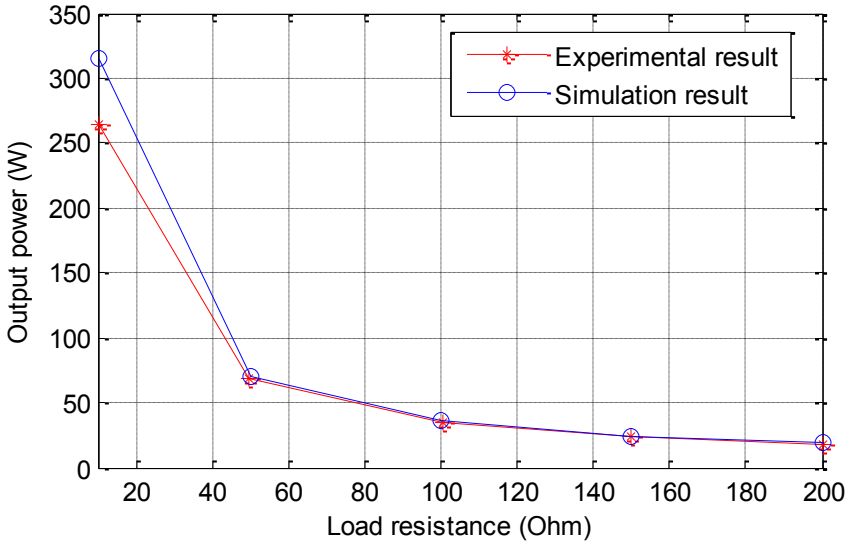
Fig. 4-11 shows the current flowing through the diodes, capacitors and inductors. In Fig. 4-11 (a), it shows the current flowing through the resonant inductor L_{r1}, L_{r2} and L_{r3}. The introduced resonant inductors reduce the current spikes, which reduce the current pressure of the components and extend their life time. Meanwhile, it keeps the MOSFETs turning on and off at zero current, and ZCS is achieved. Fig. 4-11(b) shows the current flowing through inductor L_{r2}, capacitor C_3 and diode D_3. It shows that the switches and diodes are working on ZCS. Fig. 4-11(c) shows that current flowing through $D_4^{'}$, $D_2^{'}$ and inductor current i_{Lr1}. According to Fig. 4-11(d), the input current is equal to the sum of currents flowing through diodes $D_4^{'}$, $D_2^{'}$, it also shows that the diode $D_4^{'}$ conducts first and then diode $D_4^{'}$ conducts. Meanwhile, the inductor current i_{Lr2} is equal to the sum of currents flowing through capacitor $C_4^{'}$ and the diode $D_4^{'}$. There is a slight difference between the simulation result and the experiment result as compared with Fig. 4-7 (b). The current in experiment as shown in Fig. 4-11 (c) is a resonant current because the resonant inductor in experiment is the parasitic inductance, which exists in each capacitor.

Fig. 4-12 shows the measured and simulated power efficiency and output power versus the load resistor. In Fig. 4-12 (a), the simulation power efficiency of the proposed

circuit is high, up to 94%, and the experimental result is around 90%. Due to the power loss of the switches, the diodes, and the wires, the power efficiency decreased quickly when the load resistor decreased, especially in the experiment.



(a) Simulation and experimental result of power efficiency



(b) Simulation and experimental result of output power

Fig. 4-12 Simulation and experimental result of power efficiency and output power of the proposed circuit

The output power is shown in Fig. 4-12(b). The output power is over 300W in the simulation result and is 270W in the experimental result. The output power decreased

quickly when the load resistance increased to 50 Ω, and then decreased slowly. Therefore, the suggested maximum power has been limited to 100W. In addition, the power efficiency is higher compared with Fig. 4-12(a)

4.5 Summary

An AC-DC cascade step up/down converter based on switched-capacitor principle has been proposed. In the proposed circuit, a capacitor and diodes are integrated into a step up/ down module, which is convenient to replace and plugged in and out of the converter. Therefore, it is easy to maintain and to adjust the output voltage. Design and tests up to 50kHz have been examined. Resonant inductors are used to reduce the current spikes, which significantly suppress the current stress of the component and extend the life of the converter. The transistor gate signal is simple and easy to achieve. Only a pair of complementary signals which synchronize with the input voltage is required. Overall, the result is promising to future high frequency AC distribution.

Chapter 5

Zero-voltage Switching Switched-inductor Resonant Current Source Converter

5.1 Introduction

The topology of switched mode power converter (SMPC) [130]-[131] has been extraordinarily developed in the last few decades. It consists of switches and energy storage devices. By turning on and off the switches on different duty ratios, the energy is delivered through energy storage element to the load continuously. For AC-DC converter, classical power factor correction (PFC) such as using Boost converter is a promising method, however, under high frequency AC distribution, the switching frequency in the boost converter will be even higher and therefore it is not suitable for present application. Following the analysis in Chapter 1.2, the proposed topology is an AC-DC rectifier using simple rectifier or Class-E rectifier in cascade with a DC-DC converter. The voltage mode will be described here as it is well-known topology. The current mode is developed here using duality and the Class-E current mode has been described in Chapter 1.2. The DC-DC converter is explored here under a new family of circuit.

Recently, a family of switched capacitor power converter is reported [73],

[132]-[133]. It uses only capacitors as the energy storage element for energy transfer [73], [132]. Now, capacitor based power converter named as switched capacitor power converter (SCPC) has obtained substantial attention and evolves rapidly in the field. This concept can combine with classical switched-mode power converter [133] and also can be applied to multiple voltage conversion [133], and fractional [132], multiple inputs [106]. The concept of switched-capacitor has also been discussed by researchers in Luo converter [134], hybrid DC-DC converter [135], RC type [136] and chain structure [137].

A new type of switched-inductor power converters (SIPCs) for current conversion applications is firstly proposed by Cheng [138] based on duality principle between switched-inductor power converter and the conventional SCPCs. Only inductors and switching devices are employed. Similarly to conventional SCPCs, there are several current conversion ratio combinations including double-, half-, inverted-, high order types etc.

The SIPC is carried out using fast semiconductor switching devices which is under hard switching. A fast switching operation generates signals with high dv/dt and high current rate di/dt, consequently generates much loss and EMI. In conventional SCPC, soft switching technique is an effective method to reduce the switching loss and to push the frequency to higher range [76], [111], [114]. They use a relatively large

capacitor and a small inductor to form a resonance tank to achieve zero-current switching. The qualified inductance eliminates the current spike during the switching [62], [139].

In this chapter, soft switching technique is applied to the SIPC to suppress the high voltage spike during the switches operation. A small capacitor is paralleled with switches to achieve zero voltage switching that can be generated by zero-voltage switching techniques [140]-[141] and duality principle between conventional SCPC and SIPC. The three basic versions resonant SIPC are analyzed in detail. Simulation and experimental tests agree well and provide the lead to a new type of power conversion.

The switched capacitor converter and switched capacitor cell have been employed in to many applications. The various switched capacitor based dc- dc converters which provide step up, step down inverted, multiple inputs or output for summation or subtraction have been presented [74, 82, 84, 142, 143, 144, 145, 146]. There are some applications of AC-DC rectifier [147-148], ac-ac converter [85, 145-151]. The proposed resonant switched-inductor will have the potential to fulfill the function of above converters.

SIPCs find applications in current-based loads such as light-emitting diode. They can be employed in photovoltaic systems as the front end converter feeding grid-tie

inverters. SIPCs do not use electrolytic capacitors, as in the case of SCPCs, for energy storage. This feature makes it an attractive option as there is no need to replace the aging capacitors. Generally, photovoltaic systems are installed in roof tops or in large solar farms away from the city. For such applications, SIPC is very useful as there is no need for replacing any component. Current mode controlled electrical machine can also be realized easily by the proposed circuit. These converters can also be effectively employed in battery or super-capacitor based charger systems as it is easier to realize constant output current with such topologies.

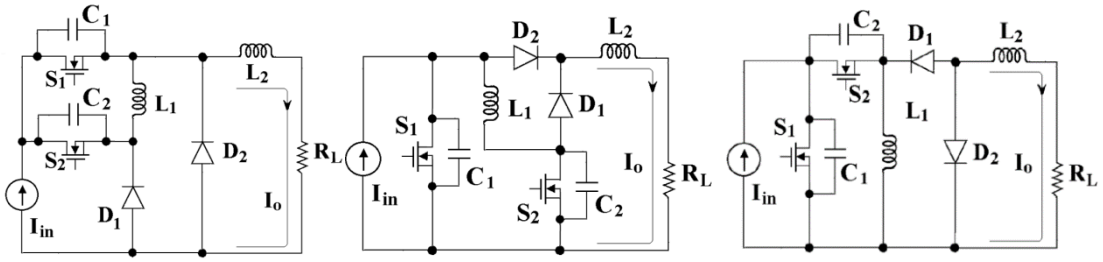
5.2 Operation principle of three basic resonant SIPC

Three basic switched-inductor current source power converters are proposed by Cheng in ref [138] as shown in Fig.5-1, derived from switched capacitor power converter based on the duality principle in [138]. Soft switching technique of zero voltage switching could be derived by zero current switching using the duality principle on switched-capacitor converters. The specific duality relationship is just the exchange between parallel and series, and star and delta and the zero-voltage switching can be generated by ZCS circuit.

The new family of SIPCs shown in Fig. 5-1 consists of two transistors, two diodes, two inductors and two resonant capacitors for each circuit. The inductor L_1 is the switched inductors. Meanwhile, inductor L_2 is the current filter for the load. It is

similar to the filter capacitor in classical DC-DC converter. Two small capacitors resonate with inductors to obtain zero voltage switching. When the switching frequency is high, the inductor will behave as a constant current source or sink. The analysis are done below with the assumption that output inductors L_2 are large enough and current ripples flowing through them are negligible and the output current can be assumed to be constant. The switching devices, the inductors and capacitor are ideal and no parasitic components.

Equivalent circuits to show the 4 states of operation are shown in Fig 5-2, Fig 5-4 and Fig 5-6 and the simulation waveforms of switching signal, inductor currents, capacitor voltage, output current, output voltage, and input voltage are shown in Fig.5-3, Fig.5-5 and Fig. 5-7 for each circuit in Fig 5-1. Simulation parameters for the circuit are listed as: inductors L_1=L_2=500μH, switching frequency f_S=50 kHz, the resonant capacitor C_1=C_2=0.02μF, output power is 27W and the input current I_{in}=6A.



(a) Double-mode (b) Half-mode (c) Inverted-mode

Fig.5-1 Resonant switched-inductor converters

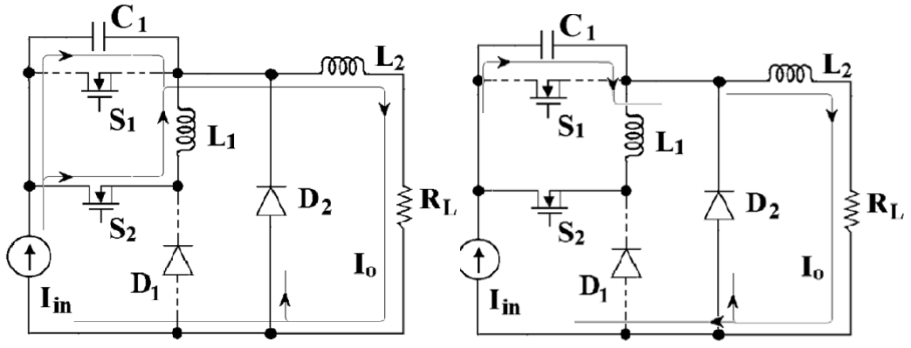
5.2.1 Double-Mode Resonant Switched-Inductor Converter

The double-mode resonant circuit is shown in Fig. 5-1(a). It could be seen that

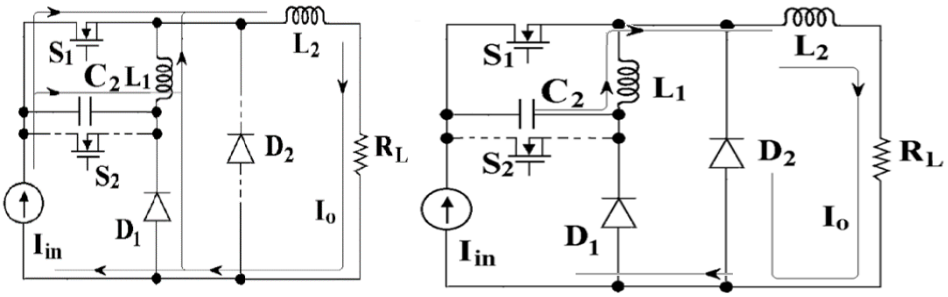
capacitor C_1 and C_2 is paralleled with switches S_1 and S_2 respectively and resonate with inductor L_1 to obtain zero voltage switching in that S_1 and S_2 are turned on and off in alternate manner. For C_1 equal to C_2, the resonant frequency is $f_0 = 1/(2\pi\sqrt{LC_1})$. The resonance allows the voltage across switches gradually to vary with a sinusoidal waveform. In this chapter, the switching frequency f_s is tested at 50 kHz. When the resonant frequency f_O is higher than the switching frequency f_S, the voltage across the two switches reaches zero before the switch is turned on. Therefore, the switches can be turned-on and off under zero voltage condition.

Two transistors S_1 and S_2 are turned on and off in alternative manner and the duty cycle is 50%. In order to avoid voltage spike from the inductor, the deadtime of the two switches is negative. That is there is a slight overlapping between the switching signals and the duty ratio of the switches are slightly larger than 50%.

Because of two diode and two switches, there are 4 working states. The operation waveforms are shown in Fig. 5-3.

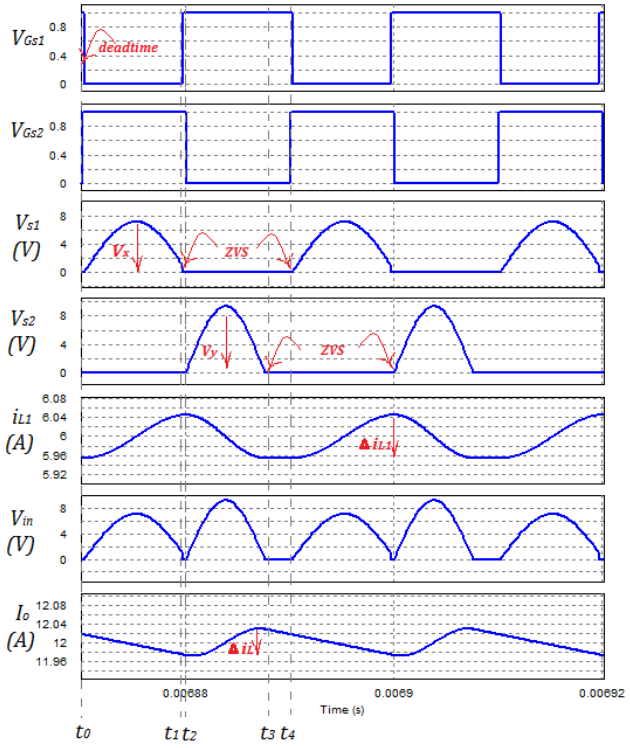


(a) State I: S_2 on and S_1 off (b) State II: freewheeling stage (S_2 on and S_1 off)



(c) State III: S_2 off and S_1 on (d) State IV: freewheeling stage (S_2 off and S_1 on)

Fig. 5-2 The operation stages of double-mode resonant SIPC



Double-mode resonant SICP

Fig. 5-3Simulation result of the three resonant SICP (L_1=L_2=500μH, f_S=50 kHz, I_{in}=6A)

a) ***State I*** $[t_o-t_1]$: At t_0, switch S_1 is turned off while S_2 is turned on, the state circuit is shown in Fig. 5-2(a). The current source I_{in} is in series with inductor L_1 through switch S_2. The inductor is charging up to I_{in}. The capacitor C_1 is paralleled with the inductor L_1 and form a resonant tank. The current flowing through inductor L_1 is gradually increased from minimum at t_0 to maximum at

t_1. The voltage across capacitor C_1 which is equal to voltage cross the switch S_1 (Vs_1) resonates from zero at t_0 to the peak value and back to zero at t_1 in sinusoidal waveform. Therefore, switch S_1 is turned off under zero voltage switching and is turned on under zero voltage switching. The state equation is as follows.

$$\begin{cases} C_1 \frac{dv_{s1}}{dt} + i_{L1} = I_{in} \\ v_{s1} = L_1 \frac{di_{L1}}{dt} \end{cases} \quad (5\text{-}1)$$

Started from $v_{s1} = \mathrm{V}_x sin\omega_0 t$

Substitute to equation (5-1), the following equations can be derived.

$$C_1 \frac{dv_{s1}}{dt} = \omega_0 C_1 \mathrm{V}_x cos\omega_0 t \quad (5\text{-}2)$$

$$\omega_0 C_1 \mathrm{V}_x cos\omega_0 t + i_{L1} = I_{in} \quad (5\text{-}3)$$

Then the solution is

$$\begin{cases} \mathrm{v_{s1}} = \mathrm{V_x sin\omega_0 t} \\ \mathrm{i_{L1}} = \mathrm{I_{in}} - \frac{\mathrm{V_x}}{\mathrm{Z_0}} \mathrm{cos\omega_0 t} \end{cases} \quad (5\text{-}4)$$

To simplify the analysis, the value of capacitance C_1=C_2, L_1=L_2.

Therefore, $\omega_0 = \sqrt{\frac{1}{L_1 C_1}}$, $Z_0 = \frac{1}{\omega_0 C_1}$. (5-5)

b) ***State Ⅱ [t1-t2]:*** S_2 keeps on, S_1 is still off. The state circuit is shown in Fig. 5-2(b). The voltage v_{s1} across capacitor C_1 reaches zero at t_1 and remains zero to the end of the half switching cycle t_2. The L_1C_1 tank stops resonance at t_1. The inductor current i_{L1} reaches maximum at t_1 and remains the maximum value till

the rest of the half switching cycle t_2. The state equation is

$$\begin{cases} v_{s1} = 0 \\ i_{L1} = I_{in} + \frac{V_x}{Z_0} \end{cases} \quad (5\text{-}6)$$

c) ***State Ⅲ [t2-t3]:*** Switch S_1 is turned on whereas S_2 is switched off. The state circuit is shown in Fig. 5-2(c). The switched inductor L_1 acts like a current source is delivering the energy to the load together with the current source I_{in}. The inductor L_1 is in series with capacitor C_2 and forms a resonant tank. The current flowing through inductor L_1 is gradually decreased from maximum at t_2 to minimum value at t_3. The voltage across capacitor C_2 which is equal to voltage cross the switch S_2 (Vs_2) resonates from zero at t_2 to the peak value and back to zero at t_3 in sinewave. Hence, switch S_2 is turned off and on under zero voltage switching. The state equation is as follows.

$$\begin{cases} -C_2 \frac{dv_{s2}}{dt} + i_{L1} + I_{in} = I_o \\ -v_{s2} = L_1 \frac{di_{L1}}{dt} \end{cases} \quad (5\text{-}7)$$

The following equations can be derived.

$$C_2 \frac{dv_{s1}}{dt} = \omega_1 C_2 V_y cos\omega_1 t \quad (5\text{-}8)$$

$$i_{L1} = -I_{in} + I_o + \frac{V_y}{Z_1} cos\omega_1 t \quad (5\text{-}9)$$

Then the solution is

$$\begin{cases} v_{s2} = V_y sin\omega_1 t \\ i_{L1} = -I_{in} + I_o + \frac{V_y}{Z_1} cos\omega_1 t \end{cases} \quad (5\text{-}10)$$

where, $Z_1 = \frac{1}{\omega_1 C_2}$, $\omega_1 = \sqrt{\frac{1}{L_1 C_2}}$. (5-11)

To simplify the analysis, if the values of capacitance C_1=C_2,

$$\omega_1 = \omega_0 = \sqrt{\frac{1}{L_1 C_2}} = \sqrt{\frac{1}{L_1 C_1}} \quad (5\text{-}12)$$

$$Z_1 = Z_0 = \frac{1}{\omega_1 C_2} = \frac{1}{\omega_0 C_1} \quad (5\text{-}13)$$

d) ***State IV*** $[t_3\text{-}t_4]$***:*** Switch S_1 is still turned on whereas S_2 is still being off. The state equivalent circuit is shown in Fig. 5-2(d). Similar to state II, the voltage across capacitor C_2 stops resonance at t_3 and remains zero till the half switching cycle t_4. The current flows through inductor L_1 reaches minimum at t_3 remains the minimum value till the end of half switching cycle t_4.

The state equation is

$$\begin{cases} v_{s2} = 0 \\ i_{L1} = I_o - I_{in} + \frac{V_y}{Z_1} \end{cases} \quad (5\text{-}14)$$

The four states operate alternatively with high switching frequency. The output current is provided by the input current source I_{in} and the switched inductor L_1. It flows through L_1C_1 network and the freewheeling diode.

From above mentioned, the dc and ac components of current flowing through the inductor in equations (5-4) and (5-9) respectively should be equal. Combine with equations (5-12), (5-13), the following relationship can be derived

$$I_o = 2I_{in} \quad (5\text{-}15)$$

$$V_x = V_y \quad (5\text{-}16)$$

By using input and output power balancing, equation (5-18) is achieved as follows.

$$I_{in}V_{in} = V_oI_o \tag{5-17}$$

$$I_{in}V_{in} = \frac{I_{in}}{T_s}\int_0^{T_s} v_{in}\,dt = \frac{I_{in}}{T_s}\int_0^{\frac{T_0}{2}} V_x sin\omega_0 t\,dt + \frac{I_{in}}{T_s}\int_0^{\frac{T_1}{2}} V_y sin\omega_1 t\,dt \tag{5-18}$$

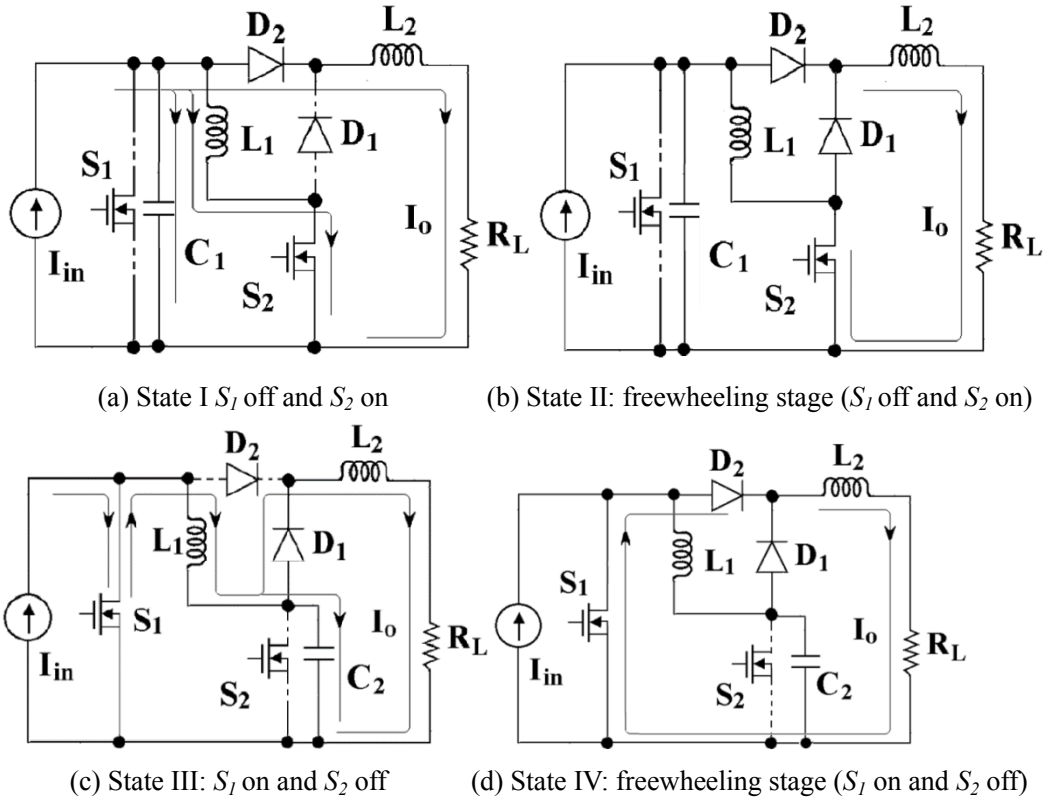
Substitutes equations (5-15) and (5-16) into equations (5-17) and (5-18), the value of voltage V_x can be derived as

$$V_x = \frac{\pi V_o T_s}{T_o} \tag{5-19}$$

where, T_s is the switching cycle, T_o, T_1 are the resonant cycles for ω_o and ω_1 respectively.

5.2.2 Half-Mode Resonant Switched-Inductor Converter

The half-mode resonant circuit is shown in Fig. 5-1(b). The inductor L_1 is used to share the input current I_{in} with the inductor L_2. Then energy stored in the inductor L_1 is delivered to the load by alternatively turning on and off the two transistors S_1 and S_2. The capacitor C_1 or C_2 is paralleled with inductor L_1 and forms a resonant tank to obtain zero voltage switching. Similarly, there are also four working stages found in the half-mode circuit as shown in Fig. 5-4. The operation waveforms are shown in Fig. 5-5.



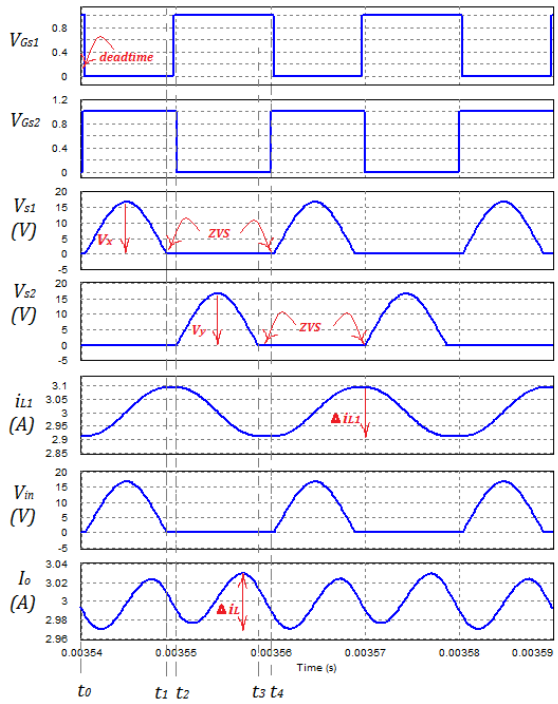
(a) State I S_1 off and S_2 on

(b) State II: freewheeling stage (S_1 off and S_2 on)

(c) State III: S_1 on and S_2 off

(d) State IV: freewheeling stage (S_1 on and S_2 off)

Fig. 5-4 The four operation states of half-mode resonant SIPC



Half-mode resonant SICP

Fig. 5-5 Simulation result of the three resonant SICP (L_1=L_2=500μH, f_S=50 kHz, I_{in}=6A)

(a) ***State I [t_0-t_1]***: At t_0, switch S_1 is turned off whereas S_2 is turned on, the

state circuit is shown in Fig. 5-4(a). The current source is charging the inductor L_1 and load R_L in parallel. Inductor L_2 is filtering the output current. The capacitor C_1 is connected in paralleled with inductor L_1 and forms a resonant tank. The current flowing through inductor L_1 is gradually increased from minimum at t_0 to maximum at t_1. The voltage Vs_1 across capacitor C_1 resonates from zero at t_0 to the peak value and back to zero at t_1 in sinewave. Therefore, switch S_1 is working under zero voltage switching. The state equation is as follows.

$$\begin{cases} I_{in} = C_1 \frac{dv_{s1}}{dt} + i_{L1} + I_o \\ v_{s1} = L_1 \frac{di_{L1}}{dt} \end{cases} \tag{5-20}$$

Similarly with the above derivation, the solution is

$$\begin{cases} v_{s1} = \mathrm{V}_x sin\omega_0 t \\ i_{L1} = I_{in} - I_o - \frac{\mathrm{V}_x}{Z_0} cos\omega_0 t \end{cases} \tag{5-21}$$

where, v_{s1} is voltage across the switch S_1 (equal to the voltage across capacitor C_1), $\mathrm{Z}_0 = \frac{1}{\omega_0 C_1}$, $\omega_0 = \sqrt{\frac{1}{L_1 C_1}}$. (5-22)

(b) ***State II [t_1-t_2]:*** switch S_1 is turned off while S_2 being on. t_1 is the end of half resonant cycle. The voltage across capacitor C_1 stops resonance at t_1 and remains zero till the end of the half switching cycle t_2 because the antiparallel body diode (not drawn in the circuit) is on. The current flows through inductor L_1 reaches the maximum at t_1 remains the maximum

value till the end of half switching cycle t_2.

The state equation is

$$\begin{cases} v_{s1} = 0 \\ i_{L1} = I_{in} - I_o + \frac{V_x}{Z_0} \end{cases} \tag{5-23}$$

(c) ***State Ⅲ [t_2–t_3]:*** At t_0, Switch S_1 is turned on while S_2 is switched off. The state circuit is shown in Fig. 5-4(c). The current source is shorted by the switch S_1. Inductor L_1 and Capacitor C_2 are in parallel through S_1, *to* form a resonant tank with a parallel the output which is an L_2 connected with load R_L. Inductor L_1 is releasing energy to the load gradually and resonates with C_2 at the same time. The inductor current decreases from maximum at t_2 to minimum at t_3. The voltage across capacitor C_2 resonates from zero at t_2 to the peak and back to zero at t_3 in a sinusoidal manner. Therefore, switch S_2 is working under zero voltage switching. The state equation is:

$$\begin{cases} i_{L1} - C_2 \frac{dv_{s2}}{dt} = I_o \\ v_{s2} = -L_1 \frac{di_{L1}}{dt} \end{cases} \tag{5-24}$$

The solution can be derived as

$$\begin{cases} v_{s2} = V_y sin\omega_1 t \\ i_{L1} = I_o + \frac{V_y}{Z_1} cos\omega_1 t \end{cases} \tag{5-25}$$

where, $Z_1 = \frac{1}{\omega_1 C_2}$, $\omega_1 = \sqrt{\frac{1}{L_1 C_2}}$. (5-26)

In particular, C_1=C_2, ω_0=ω_1

(d) ***State IV[t_3-t_4]:*** After half resonant cycle at t_3, the voltage across capacitor C_2 stops resonance at t_3 because the body diode conducts and v_{s2} remains zero till the end of the half switching cycle at t_4. The current flows through inductor L_1 to reach the minimum at t_3 and remains the minimum value till the end of the half switching cycle at t_4.

The state equation is

$$\begin{cases} v_{s2} = 0 \\ i_{L1} = I_o - \frac{V_x}{Z_1} \end{cases} \tag{5-27}$$

By equating the DC part of eqns (5-27) and (5-23), the current conversion ratio is:

$$I_o = I_{in}/2 \tag{5-28}$$

Similarly, sum the above analysis of four stages, combine the input output power balancing theory (5-17):

$$I_{in}V_{in} = \frac{I_{in}}{T_s}\int_0^{T_s} v_{in}\,dt = \frac{I_{in}}{T_s}\int_0^{\frac{T_0}{2}} V_x sin\omega_0 t\,dt = I_o V_o \tag{5-29}$$

The amplitude of voltages V_x and V_y can be calculated.

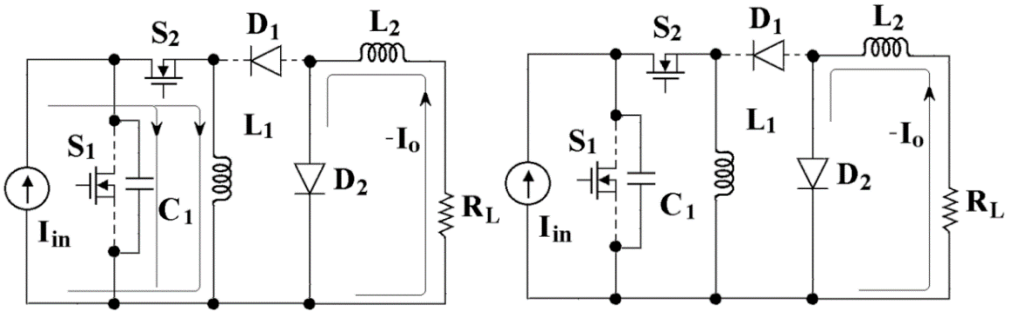
$$V_x = V_y = \frac{\pi V_o T_s}{2T_o} \tag{5-30}$$

5.2.3 Inverted-Mode Resonant Switched-Inductor Converter

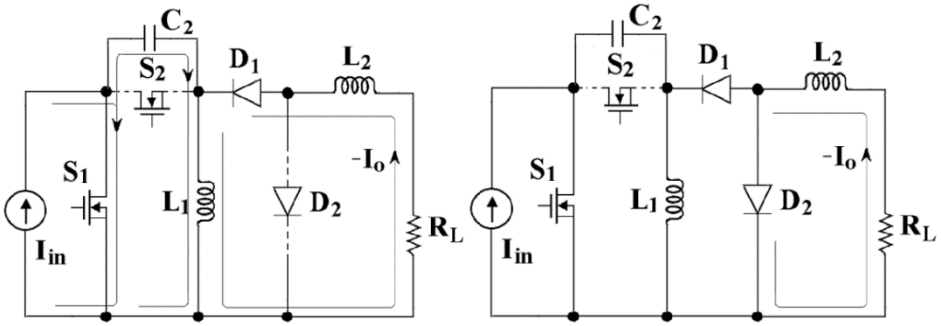
The inverted resonant mode SIPC is shown in Fig 5-1(c). The topology inverts the direction of the source current through inductor L_1 by alternatively turning on and off two transistors S_1 and S_2. The capacitor C_1 or C_2 is paralleled with

inductor L_1 and forms a resonant tank. Zero voltage switching is therefore obtained to improve the circuit performance.

Similarly, there are also four working states according to different switches and didoes' states and resonant condition. The equivalent circuit and the operation principle are shown in Fig. 5-6 and Fig. 5-7, respectively.

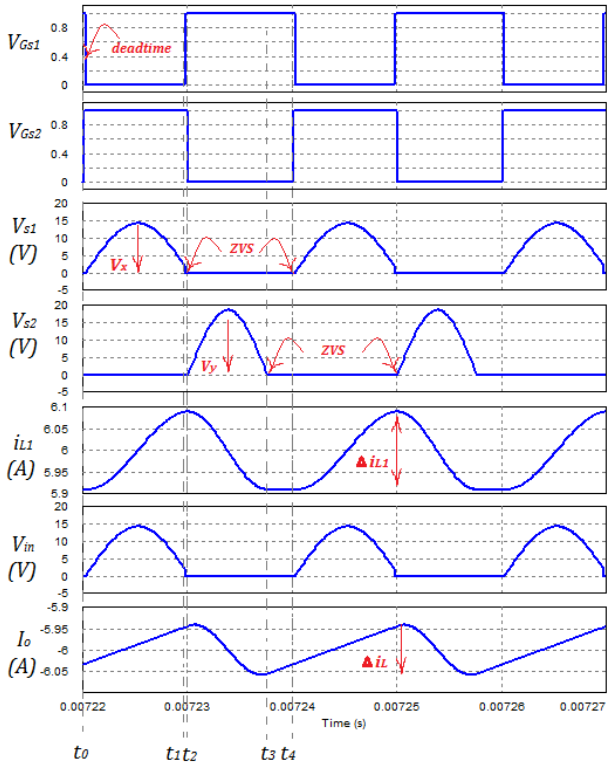


(a) State I: S_2 on and S_1 off (b) State II: freewheeling stage (S_2 *on and* S_1 *off*)



(c) State III: S_2 off and S_1 on (d) State IV: freewheeling stage (S_1 on and S_2 off)

Fig. 5-6 The four operation states of inverted-mode resonant SIPC



Inverted-mode resonant SICP

Fig. 5-7 Simulation result of the three resonant SICP (L_1=L_2=500$_\mu$H, f_S=50 kHz, I_{in}=6A)

(a) ***State Ⅰ[to-t1]:*** At t_0, the switch S_1 is turned off while S_2 is switched on. The state circuit is shown in Fig. 5-6(a). The switched inductor L_1 is charging up by the input current source through the switch S_2. The inductor L_1 and capacitor C_1 form a resonant tank and resonate a half cycle from t_o to t_1. The output current I_O flows through the freewheeling diode D_2 and the diode D_1 is reverse biased.

The state equation is as follows.

$$\begin{cases} C_1 \dfrac{dv_{s1}}{dt} + i_{L1} = I_{in} \\ v_{s1} = L_1 \dfrac{di_{L1}}{dt} \end{cases} \tag{5-31}$$

The solution is

$$\begin{cases} v_{s1} = \mathrm{V}_x sin\omega_0 t \\ i_{L1} = I_{in} - \frac{\mathrm{V}_x}{Z} cos\omega_0 t \end{cases} \quad (5\text{-}32)$$

where $Z_0 = \frac{1}{\omega_0 C_1}$, $\omega_0 = \sqrt{\frac{1}{L_1 C_1}}$. (5-33)

(b) ***State Ⅱ[t_1-t_2]:*** After half resonant cycle, the voltage across capacitor C_1 stops resonance at t_1 and remains zero till the end of half switching cycle t_2. The current flows through inductor L_1 , reaches the maximum at t_1 and remains the maximum value till the half switching cycle at t_2.

The state equation is

$$\begin{cases} v_{s1} = 0 \\ i_{L1} = I_{in} + \frac{\mathrm{V}_x}{Z_0} \end{cases} \quad (5\text{-}34)$$

(c) ***State Ⅲ[t_2-t_3]:*** At t_2, The switch S_1 is turned on while S_2 being off. The state circuit is shown in Fig. 5-6(c). The input current source is shorted by the switch S_1. Meanwhile, inductors L_1 and L_2 as well as the load R_L are connected in series manner through the diode D_1. Capacitor C_2 is connected in parallel with inductor L_1 as well and resonates for a half resonant cycle. Compared with the double- and half-mode, the output current I_O in this circuit flows through the load in reverse direction.

The state equation is:

$$\begin{cases} C_2 \frac{dv_{s2}}{dt} = i_{L1} + I_o \\ v_{s2} = -L_1 \frac{di_{L1}}{dt} \end{cases} \quad (5\text{-}35)$$

Then the solution is

$$\begin{cases} v_{s2} = \mathrm{V}_y sin\omega_1 t \\ i_{L1} = -I_o + \frac{\mathrm{V}_y}{Z_1} cos\omega_1 t \end{cases} \quad (5\text{-}36)$$

where, $Z_1 = \frac{1}{\omega_1 C_2}$, $\omega = \sqrt{\frac{1}{L_1 C_2}}$. (5-37)

(d) ***State IV[t_3-t_4]:*** After half resonant cycle, the voltage across capacitor C_2 stops resonance at t_3 and remains zero till the half switching cycle at t_4. The current flows through inductor L_1 remains the minimum value from t_3 to t_4.

The state equation is

$$\begin{cases} v_{s2} = 0 \\ i_{L1} = -I_o + \frac{\mathrm{V}_y}{Z_1} \end{cases} \quad (5\text{-}38)$$

Based on the above analysis and input output power balancing theory, the current transfer relationship of the inverted-mode circuit can been derived as

I_O=-I_{in} (5-39)

The amplitude of voltage V_x and V_y can be mathematically described by equating the input and output energy:

$$I_{in}V_{in} = \frac{I_{in}}{T_s}\int_0^{T_s} v_{in}\, dt = \frac{\mathrm{I}_{in}}{T_s}\int_0^{\frac{T_0}{2}} \mathrm{V}_x sin\omega_0 t\, dt = I_o V_o \quad (5\text{-}40)$$

Hence,

$$\mathrm{V}_x = \mathrm{V}_y = \frac{\pi V_o T_s}{T_o} \quad (5\text{-}41)$$

5.3 Design

Using the equations in section 5.2, the design of a half-mode step-down resonant

converter is shown below:

(a) First, the design specifications are:

I_{in}=6A, I_o=3A P_o=27 W, f_s=50 kHz.

(b) The design criteria is that the resonant frequency f_o is higher than the switching frequency f_s to ensure the complete resonance can be achieved. Resonant frequencies ω_1, ω_2 are equal in present mode , but in general it may not be equal for other modes of the family of SIPC resonant circuits. A 10% higher value is used for the selection.

$$\omega_2 = 1.1(2\pi f_s) \tag{5-41}$$

The resonant frequency f_2=$55kHz$.

(c) A small percentage of ripple is designed to be present on the current flowed in inductors L_1 and L_2 The peak to peak value from equations (5-22) , (5-26) and (5-30)

$$\Delta i_{L1=} \frac{\pi V_o T_s}{Z_2 T_2} \tag{5-42}$$

where, $Z_2 = \frac{1}{C_2\omega_2}$, $\omega_2 = \sqrt{\frac{1}{L_2 C_2}}$ (5-43)

For 5% ripple as compared with dc level, it results in Z_2 =171.36Ω

(d) The L and C resonant components are just obtained from the frequency and impedance expression :

L_1 = 0.493mH

C_1=C_2= C=0.017μF

L_1 and C are chosen to be 0.02μF and 0.5mH

(e) The inductor L_2 is selected to be large and is with low ripple as well. The ripple current on L_2

$$\Delta i_{L2} = \frac{2v_x}{\omega_o L_2} + \frac{\mathrm{i}_{L2}\mathrm{R}_L\mathrm{T}_o}{2L_2} \quad (5\text{-}44)$$

For 10% ripple on maximum current of 3A, L_2=0.5mH

(f) The rated voltage of the semiconductor can be calculated by equation (5-30), In this case, $\mathrm{V}_x = \mathrm{V}_y = 12.85V$. This is the rated voltage for Mosfets and diodes.

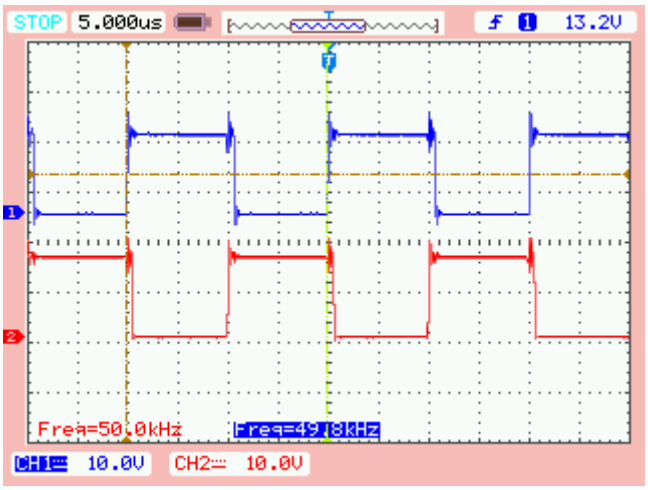
5.4 Experimental Results

The half-mode switched-inductor current source converter with zero voltage soft switching technique applied has been built in the laboratory as an example. The experimental specification and the component values of the converter have been outlined in Table 5-1. The designed Half-mode resonant converter is working with output power around 27W. The typical experimental waveforms are obtained as shown in Fig.5-8. It is noticed a small negative deadtime is needed between the two complementary gate signals $\mathrm{V_{GS1}}$ and $\mathrm{V_{GS2}}$ as shown in Fig. 5-8 (a) Compared with the proposed SIPC before, the voltage spike under switches S_1 and S_2 has been eliminated. The voltage of Vs_1 and Vs_2 gradually change in sinusoidal waveform. Therefore, both transistors are turned on and off under zero

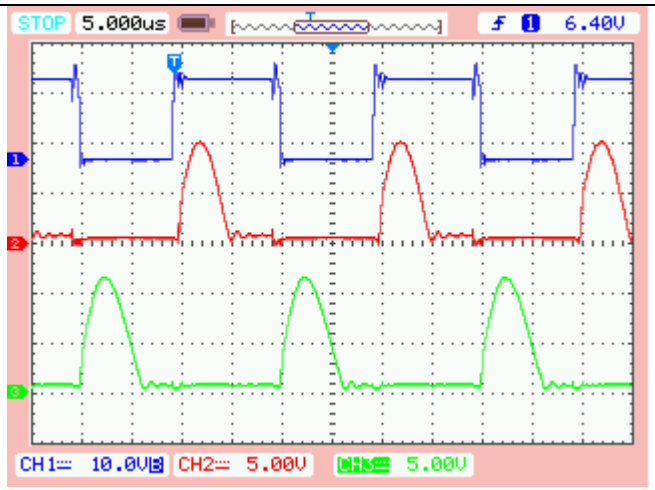
voltage switching shown in Fig. 5-8 (b). The waveforms of inductor currents i_{L1} and I_o are shown in Fig. 5-8 (c). As it can be seen, it is an I_{in}/2 dc component with a small ripple on the current of $i_{L1.}$ There is small deviation because of the energy loss in the circuit. It agrees well with the theoretical analysis. The waveforms of input current I_{in} and output current I_o are also given in Fig.5-8 (d). As is shown, output current I_o is very close to 1/2 of the input current I_{in}.

Table 5-1Specification and components of the Half-mode resonant SIPC

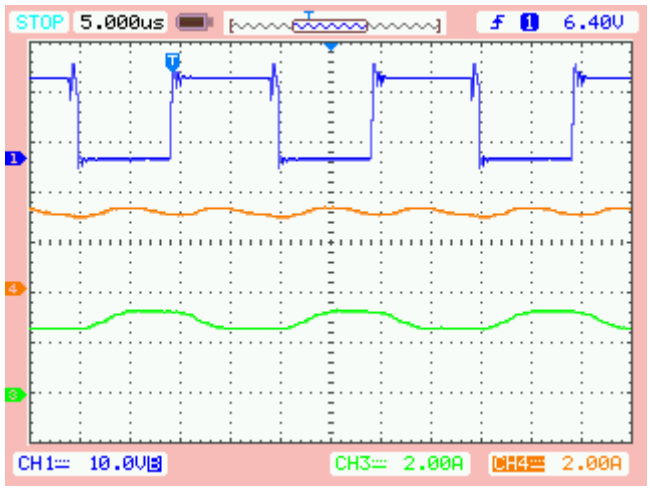
Input current I_{in}	6A
Output current I_o	3A
Output power	27W
Switching Frequency (f_s)	50kHz
L_1	0.5mH
L_2	0.5mH
C_1	0.02uF
C_2	0.02uF
D_1 and D_2 (Schottky diode)	*MBR1645*
S_1 *and* S_2 *(*N channel MOSFET*)*	*IRFB4410*



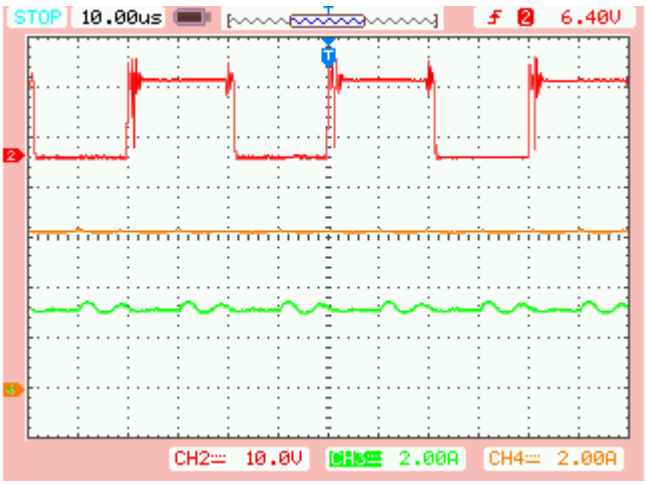
(a) Ch1: V_{GS1}; Ch2: V_{GS2};



(b) Ch1: V_{GS2}; Ch2: V_{S1}; Ch3: V_{S2}



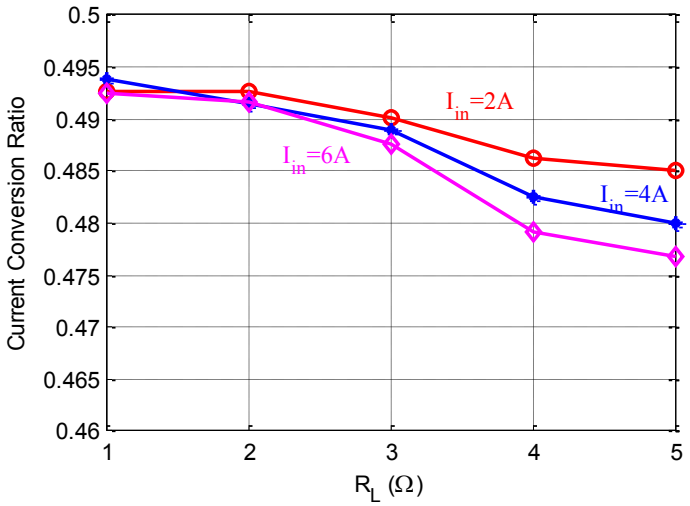
(c) Ch1: V_{GS1}; Ch3: i_{L1}; Ch4: I_o



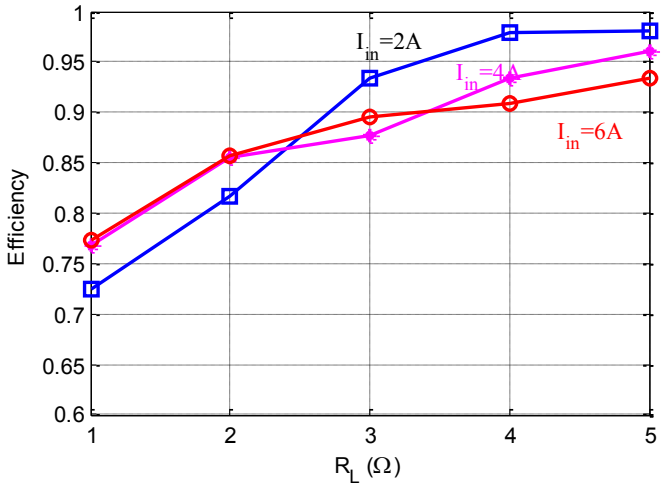
(d) Ch2: V_{GS2}; Ch3: I_o; Ch4: I_{in}

Fig. 5-8 Experimental waveforms for half-mode resonant SIPC with 6A constant input current and 3.Ω pure-resistive load.

The steady state conversion ratio of the half-mode prototype SIPC is measured as shown in Fig. 5-9(a). With the input current I_{in}= 6A, the conversion ratio is illustrated in Fig. 5-9(a). It can be seen that it can reach around values of 0.492 to 0.477, instead of the theoretical value 0.5. Increasing load resistance R_L also decreases the conversion ratio slightly due to the handling of higher power.



(a) Current ratio versus load



(b) Measured efficiency versus load

Fig. 5-9 Experimental results of the Half-mode SIPC with and without resonant tank

Fig. 5-9(b) plots efficiency versus output power of the half-mode resonant SIPC, through testing the load between 1-5Ω. The power efficiency is 93.4% when the load resistance is 5Ω. Fig. 5-9 shows the highest efficiency around 98% when the load resistance is 5Ω, and the input current is 2A. At light load, power loss in the circuit is mainly due to the diode, which has forward bias voltage drop. At high load, the power loss is mainly because of conducting loss of the transistors and the diodes.

The switching loss is reduced significantly because all the switches are under soft-switching shown in Fig. 5-9 (b). The efficiency of the prototype without zero voltage switching is up to 85% as shown in other publication [152] whereas the efficiency of the proposed prototype with zero voltage switching is up to 98%. Resonant soft-switching technique is confirmed to improve the power conversion efficiency significantly.

5.5 Application to High frequency AC-DC Converter

The above switched-inductor, as suggested in Chapter 1, can be applied to a front-end rectifier. The front-end rectifier can be simply a bridge rectifier or a Class-E rectifier. Fig 5.10 shows a cascade operation of Class-E current rectifier with a half-mode Switched-inductor resonant converter. The simulation result is shown in Fig 5.11, it can be seen that the input current is 20 A, the rectifier current I_f is 40A and the output

of the switched-inductor converter is 20A. This clearly demonstrates the operation of the circuit, the input AC 50kHz harmonic is basic fundamental at 50Hz with negligible harmonics. The zoom in figure is shown in Fig. 5-12, it shows the output current is stable with a small ripple.

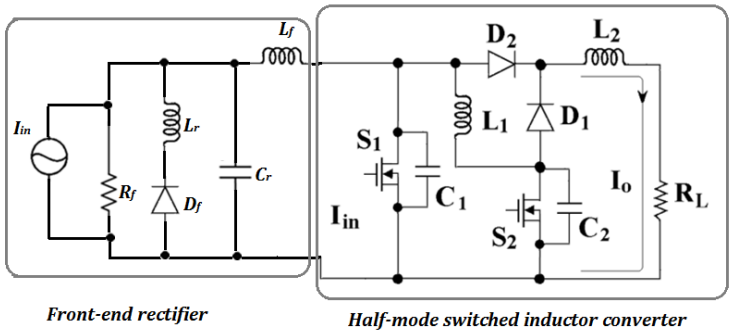


Fig. 5-10 A class-E rectifier with a Half-mode switched inductor power converter

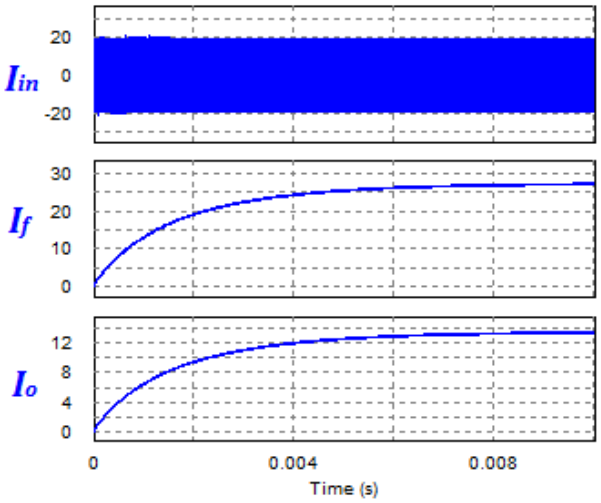


Fig. 5-11 The input current, current after rectifier, output current

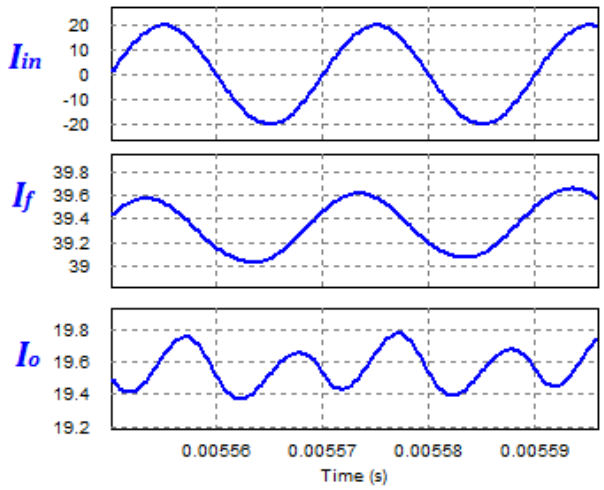


Fig. 5-12 Zoom in of input current, current after rectifier, output current

5.6 Conclusions

Double-, half- and inverted-modes of SIPCs have been generated by using the duality principle on switched-capacitor converters. Soft switching technique is applied to the new family of switched-inductor power converter that provides an effective method to eliminate voltage spike under the hard switching. It can also reduce the switching loss and improve power efficiency significantly. The circuit configuration and operation principle of the proposed current conversion circuits are analyzed in detail. Simulation and experimental results are also provided to confirm the feasibility of the novel current conversion technique. The soft switching technique provides an effective method to improve the new circuit's performance and have potential to apply in high order SIPCS furthermore.

Chapter 6

Design and analysis of resonant switched-inductor step down current type converter

6.1 Introduction

The AC-DC load side converter consists of an AC rectifier and a DC-DC converter as shown in Fig 1-4a and Fig 1-5b for current source. The rectifier may be a simple rectifier or a Class E rectifier as shown in Chapter 1.2. The DC-DC using switched-inductor is the theme of this chapter. A new type of switched-inductor power converters (SIPCs) for current conversion applications is firstly proposed by K. W. E. Cheng[138] based on duality principle between switched-inductor power converter and the conventional switched capacitor power converter (SCPC)s.

The conventional SCPC [73, 132, 133, 153, 154] uses only capacitors as the energy storage element for energy transfer [73], [132]. This concept can combine with classical switched-mode power converter [133] and also can be applied to multiple voltage conversion [133], and fractional [132], multiple inputs [143]. The concept of switched-capacitor has also been discussed by researchers in Luo converter [134], hybrid DC-DC converter [135, 155], RC type [136] and chain structure [137].

Similarly to the SCPCs, in the SIPCs, Only inductors and switching devices are

employed.

The switches generate signals with high *dv/dt* and high current rate *di/dt,* consequently generates much loss and EMI when it is carried out using fast semiconductor switching devices. In conventional SCPC, soft switching technique is an effective method to reduce the switching loss and to push the frequency to higher range [144, 156-160]. The other resonant versions like step down [161], step up [143, 162-164], inverted [74], multiple output [165], multiple inputs for summation and subtraction [146, 147, 167, 169]. It is even extended the application to AC-DC rectifier [139], and AC-Ac power converter [168-169] They use a relatively large capacitor and a small inductor to form a resonance tank to achieve zero-current switching. The qualified inductance eliminates the current spike during the switching [62].

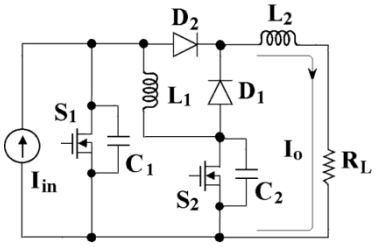
With the similar derivation principle, soft switching technique of zero voltage switching could be derived by zero current switching using the duality principle on switched-capacitor converters. The specific duality relationship is listed Table 6-1.

Table 6-1 Duality relationship of wiring connection in power converter

Parallel	↔	Series
zvs	↔	zcs

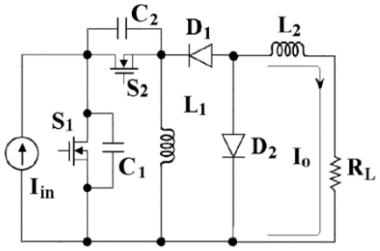
In this chapter, two families SIPCs which provide several of current conversion ratios including double-, half-, inverted-, high order etc. 1/2, 1/3, 1/4… to 1/n and -1, -1/2,

-1/3… to -1/n current conversion ratios have been proposed. Meanwhile, zero voltage switching is applied to the two families SIPCs to suppress the high voltage spike during the switches operation. Two small capacitors are paralleled with switch to achieve zero voltage switching based on duality principle between conventional SCPC and SIPC. The basic non-inverting half-mode and inverting-mode resonant switched inductor power converter are presented in Fig. 6-1 and Fig. 6-2. All the switches are operated under zero voltage switching. They have no high voltage spike problem, and can operate at high frequency.



(a) Half-mode

Fig. 6-1 Proposed basic non-inverting-mode resonant switched-inductor converters



(b) Inverting-mode

Fig. 6-2 Proposed basic inverting-mode resonant switched-inductor converters

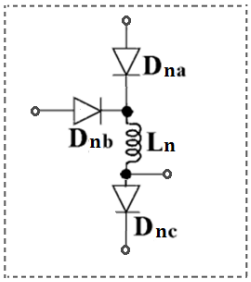


Fig. 6-3 Proposed switching inductor cell

6.2 Concepts of proposed step down resonant switched-inductor power onverters

The proposed non-inverting mode resonant step down switched-inductor current source power converters which provide 1/3, 1/4…1/n mode step down conversion ratio are shown in Fig. 6-4. And the inverting-mode resonant steps down of -1/2, -1/3…-1/n SIPCs are shown in Fig. 6-5.

The output current is dependent on the number of inductor cells. Each inductor cell proposed in Fig. 6-3 is formed by inductor and diodes. The output current is -1/n or 1/n of input current by applying on the inductor cells on the converter circuit; n is the number of inductor. The inductor cells are for sharing the input current together in parallel. Each inductor is charged by the input current, shares the input current in paralleled and releases to the load in series later. The diodes are used to decide the direction of the current flow which charges the inductor and releases the energy.

When the circuit is under operating, two transistors S_1 and S_2 are turned on and off in alternative manner and the duty cycle is 50%. The deadtime needed for the two transistors are negative which allows a small overlapping of the turn-on time of S_1 and S_2 in order to eliminate any incident of high voltage spike due to discontinuous conduction by S_{1a} and S_{1b} to I_{in}. To facilitate the following analysis, however, the small negative deadtime is ignored and the duty cycle is still considered as 50%. Taking inverting mode resonant step down SIPC as example, When switch S_1 is

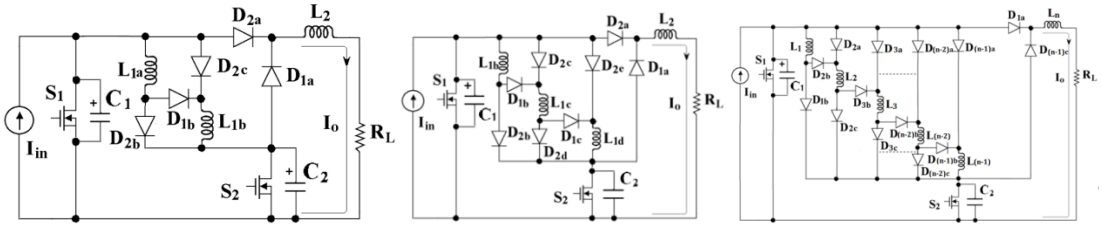
turned off while S_2 is turned on, the current source is charging inductor L_{1a}, in paralleled with the inductor L_{1b} to L_{1n}. The capacitor C_1 is paralleled with L_{1a}, L_{1b} to L_{1n} and form a resonant tank. L_2 is in series with the load and filtering the current ripple. When switch S_1 is turned on while S_2 is turned off, the current source is shorted by the switch S_1. The inductors L_{1a}, L_{1b} to L_2 are connected in series and acts releasing energy to the load. Capacitor C_2 resonates with inductor L_{1a}, L_{1b} …and L_2 .

To simplify the analysis, assume

--The values of both switched inductors L_2 is large enough to keep the current constant

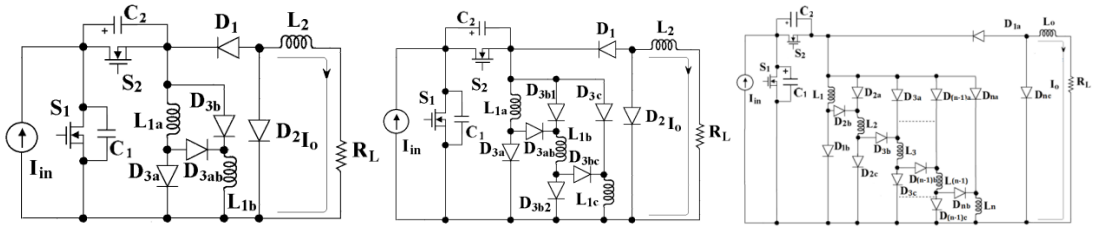
--All the switching devices are ideal, i.e. no parasitic components.

--The input power source I_{in} is ideal, i.e. constant and no parallel impedance.



(a) 1/3-mode (b) 1/4-mode (c) 1/n-mode

Fig. 6-4 Proposed non-inverting resonant step down switched-inductor converters



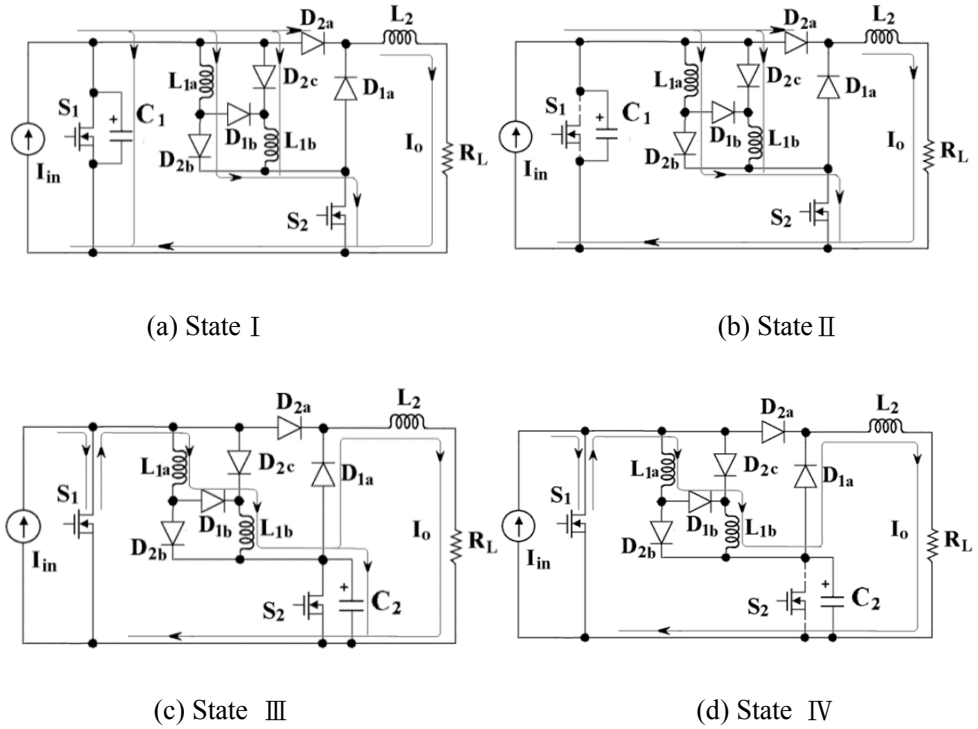
(a) -1/2-mode (b) -1/3-mode (c) -1/n-mode

Fig. 6-5 Proposed inverting resonant step down switched-inductor converters

6.3 Operation principles

6.3.1 Non-inverting mode resonant step down resonant converters

1) The non-inverting mode 1/3-mode resonant step down SIPC is analyzed. There are four operation states in each switching period. The state equivalent circuits are shown in shown in Fig. 6-6. Assuming all the devices are ideal and no parasitic component. Simulation parameters for the circuit are listed as: inductors L_{1a}=L_{1b}=500μH, switching frequency f_S=50 kHz, the resonant capacitor C_1=C_2=0.01uF, the Load R_L=8Ω and the input current I_{in}=6A. The simulation waveforms of is shown in Fig. 6-7.



(a) State Ⅰ (b) State Ⅱ

(c) State Ⅲ (d) State Ⅳ

Fig. 6-6 The operation states of 1/3-mode resonant SIPC

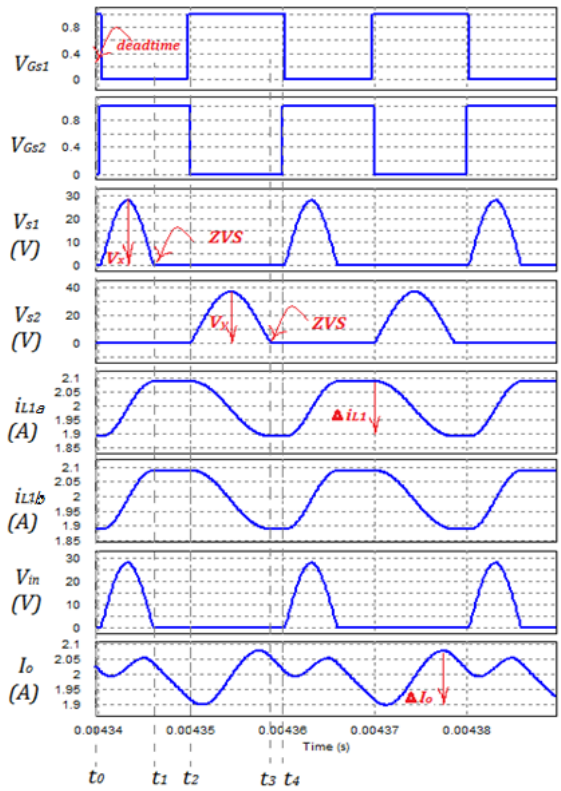


Fig. 6-7 Simulation waveform of 1/3-mode resonant SICP (L_{1a}=L_{1b}=500µH, f_S=50 kHz, I_{in}=6A)

a) ***State I [t_o-t_1]:*** At t_0, the switch S_1 is turned off while S_2 is turned on, the state circuit is shown in Fig. 6-6(a). The input current source I_{in} is charging the inductor L_{1a}, L_{1b} and L_2 in parallel through S_2 and D_2. The inductor L_2 is connected in series with load R_L to filter the current ripple. The capacitor C_1 is connected in paralleled with inductor L_{1a}, L_{1b} and forms a resonant tank. The current flowing through inductor L_{1a}, L_{1b} is gradually increased from minimum at t_0 to maximum at t_1. The voltage across capacitor C_1 which is equal to voltage cross the switch S_1 (Vs_1) resonates in sinewave from zero at t_o to the peak value and back to zero at t_1 in a half resonant cycle. Therefore, switch S_1 is turned on and off at zero voltage.

The state equation is as followed.

$$\begin{cases} I_{in} = C_1 \frac{dv_{s1}}{dt} + i_{L1a} + i_{L1b} + I_o \\ v_{s1} = L_1 \frac{di_{L1}}{dt} \\ i_{L1} = i_{L2} \end{cases} \quad (6\text{-}1)$$

Assuming $v_{s1} = \mathrm{V}_x sin\omega_1 t$ (6-2)

Substitute (6-2) to equation (6-1), the following equations can be derived.

$$C_1 \frac{dv_{s1}}{dt} = \omega_1 C_1 \mathrm{V}_x cos\omega_1 t \quad (6\text{-}3)$$

$$\omega_1 C_1 \mathrm{V}_x cos\omega_1 t + 2i_{L1a} + I_o = I_{in} \quad (6\text{-}4)$$

Then the solution is derived as

$$\begin{cases} v_{s1} = \mathrm{V}_x sin\omega_1 t \\ i_{L1a} = \frac{1}{2}(I_{in} - I_o - \frac{\mathrm{V}_x}{Z_1} cos\omega_1 t) \end{cases} \quad (6\text{-}5)$$

where, $Z_1 = \frac{1}{\omega_1 C_1}$, $\omega_1 = \sqrt{\frac{2}{L_{1a} C_1}}$, C_1=C_2, L_{1a}=L_{1b}.

b) ***State II [t_1-t_2]:*** At t_1, the switch S_1 is turned off whereas S_2 still being on. The equivalent circuit is shown in Fig. 6-6(b). The voltage across capacitor C_1 stops resonance at t_1 and remains zero till the half switching cycle t_2. The current flows through inductor reach the maximum at t_1 and remain the maximum value till t_2.

The state equation is

$$\begin{cases} v_{s1} = 0 \\ i_{L1a} = I_{in} - I_o + \frac{\mathrm{V}_x}{Z_1} \end{cases} \quad (6\text{-}6)$$

c) ***State III [t_2-t_3]:*** At t_2, switch S_1 is turned on whereas S_2 is switched off. The

state circuit is shown in Fig. 6-6(c). The input current source is shorted by the switch S_1. Inductors L_{1a}, L_{1b} and L_2 act like current source connected in series to transfer the energy to the load R_L. The capacitor C_2 is connected in paralleled with inductor L_{1a} and L_{1b} and forms a resonant tank. The current flowing through inductor L_{1a} and L_{1b} is gradually from maximum at t_2 decreased to minimum at t_3 in a half resonant cycle. The voltage across capacitor C_2 which is equal to voltage cross the switch $S_2(Vs_2)$ resonates from zero at t_2 , reaches to the peak value and back to zero at t_3 in sinusoidal waveform in a half resonant cycle

The state equation is as followed.

$$\begin{cases} i_{L1a} - C_2 \frac{dv_{s2}}{dt} = I_o \\ v_{s2} = -2L_{1a} \frac{di_{L1a}}{dt} \end{cases} \tag{6-7}$$

Assuming $v_{s2} = \mathrm{V}_y sin\omega_2 t$ (6-8)

Substitute (6-8) to equation (6-7),

Similarly to the above analysis, the following equations can be derived.

$$C_2 \frac{dv_{s1}}{dt} = \omega_2 C_2 \mathrm{V}_y cos\omega_2 t \tag{6-9}$$

$$i_{L1a} = I_o + \frac{\mathrm{V}_y}{Z_2} cos\omega_2 t \tag{6-10}$$

Then the solution is.

$$\begin{cases} v_{s2} = \mathrm{V}_y sin\omega_2 t \\ i_{L1a} = I_o + \frac{\mathrm{V}_y}{Z_2} cos\omega_2 t \end{cases} \tag{6-11}$$

Where, $Z_2 = \frac{1}{\omega_2 C_2}$, $\omega_2 = \sqrt{\frac{1}{2L_{1a}C_2}}$, C_1=C_2, L_{1a} =L_{1b}

d) ***State IV [t_3-t_4]:*** At t_3, switch S_1 is still being on whereas S_2 is turned off. The voltage across capacitor C_2 stops resonance at t_3 and remains zero at t_4 the end of half switching cycle. The current flows through inductor L_{1a} and L_{1b} reach the minimum value at t_3 and remain it till t_4 the half switching cycle.

The state equation is

$$\begin{cases} v_{s2} = 0 \\ i_{L1a} = I_o - \frac{V_y}{Z_2} \end{cases} \quad (6\text{-}12)$$

The two stages operate alternatively with high switching frequency. The output current is provided by the input current source and the energy storage part. It flows through L_{1a} , L_{1b} , C_1 and C_2network and the freewheeling diode.

2) Generalized Equations of 1/3 mode resonant switched-inductor power converters

From above mentioned, the dc component of the current flowing through the inductor L_{1a}

same as L_{1b} in equation (6-5) and (6-11) respectively should be equal, then there is

$$I_o = \frac{1}{2}(I_{in} - I_o) \quad (6\text{-}13)$$

Therefore, the following relationship can be derived

$$I_{in} = 3I_o \quad (6\text{-}14)$$

By using input output power balancing.

$$I_{in}V_{in} = \frac{I_{in}}{T_s}\int_0^{T_s} v_{in}\,dt = \frac{I_{in}}{T_s}\int_0^{\frac{T_1}{2}} V_x sin\omega_1 t\,dt + \frac{I_{in}}{T_s}\int_0^{\frac{T_2}{2}} V_y sin\omega_2 t\,dt = V_o I_o \quad (6\text{-}15)$$

The value of voltageV_x and V_y can be solved

$$V_x = \frac{\pi V_{in} T_s}{T_1} \quad (6\text{-}16)$$

$$V_y = \frac{2\pi V_{in} T_s}{T_2} \quad (6\text{-}17)$$

Where, I_{in} is the input current, $I_o$is the output current, T_s is the switching cycle, T_1 and T_2 are the resonant cycle.

Therefore, the generalized equation of 1/3 mode resonant SIPC is

For ***State I [t_o-t_1]:***

$$\begin{cases} v_{s1} = \frac{\pi V_o T_s}{3T_1} sin\omega_1(t-t_0) \\ i_{L1a} = \frac{1}{2}(I_{in} - I_o - \frac{\pi V_o T_s}{3Z_1 T_1} cos\omega_1(t-t_0)) \end{cases} \quad (6\text{-}18)$$

where, $Z_1 = \sqrt{\frac{L_{1a}}{2C_1}}$, $\omega_1 = \sqrt{\frac{2}{L_{1a}C_1}}$, C_1=C_2, L_{1a} =L_{1b}.

For ***State II [t_1-t_2]:***

$$\begin{cases} v_{s1} = 0 \\ i_{L1a} = I_{in} - I_o + \frac{\pi V_o T_s}{3Z_1 T_1} \end{cases} \quad (6\text{-}19)$$

For ***State III [t_2-t_3]:***

$$\begin{cases} v_{s2} = \frac{\pi V_o T_s}{3T_2} sin\omega_2(t-t_2) \\ i_{L1a} = I_o + \frac{\pi V_o T_s}{3Z_2 T_2} cos\omega_2(t-t_2) \end{cases} \quad (6\text{-}20)$$

$Z_2 = \sqrt{\frac{2L_{1b}}{C_2}}$, $\omega_2 = \sqrt{\frac{1}{2L_{1b}C_2}}$, C_1=C_2, L_{1a} =L_{1b}.

For ***State IV[t_3-t_4]:***

$$\begin{cases} v_{s2} = 0 \\ i_{L1a} = I_o - \frac{\pi V_o T_s}{3 Z_2 T_2} \end{cases} \tag{6-21}$$

3) Generalized Equations of 1/n-mode resonant SIPCs

The extension of the non-inverting step down resonant SIPC is shown in Fig. 6-4. As noticed, the current of the inductor L_{1a}, L_{1b}, L_{1c},…L_{1n} is denoted by $i_{L1a}, i_{L1b,}\, i_{L1c}\ldots. i_{L1n}$, respectively. For 1/n mode resonant SIPC, there is (n-1) switched inductor cells. The generalized equation of 1/n mode resonant SIPC can be described as follows.

For ***State I [t_o-t_1]:***

$$\begin{cases} v_{s1} = \frac{\pi V_o T_s}{n T_1} sin\omega_1 (t - t_0) \\ i_{L1n} = \frac{1}{n}(I_{in} - I_o - \frac{\pi V_o T_s}{n Z_1 T_1} cos\omega_1 (t - t_0)) \end{cases} \tag{6-22}$$

where, $Z_1 = \sqrt{\frac{L}{(n-1)L}}$, $\omega_1 = \sqrt{\frac{(n-1)}{LC}}$, C_1=C_2=C, L_{1a} =L_{1b}=L_{1c}=…= L_{1n}=L.

For ***State II [t_1-t_2]:***

$$\begin{cases} v_{s1} = 0 \\ i_{L1n} = I_{in} - I_o + \frac{\pi V_o T_s}{n Z_1 T_1} \end{cases} \tag{6-23}$$

For ***State III [t_2-t_3]:***

$$\begin{cases} v_{s2} = \frac{\pi V_o T_s}{n T_2} sin\omega_2 (t - t_2) \\ i_{L1a} = I_o + \frac{\pi V_o T_s}{n Z_2 T_2} cos\omega_2 (t - t_2) \end{cases} \tag{6-24}$$

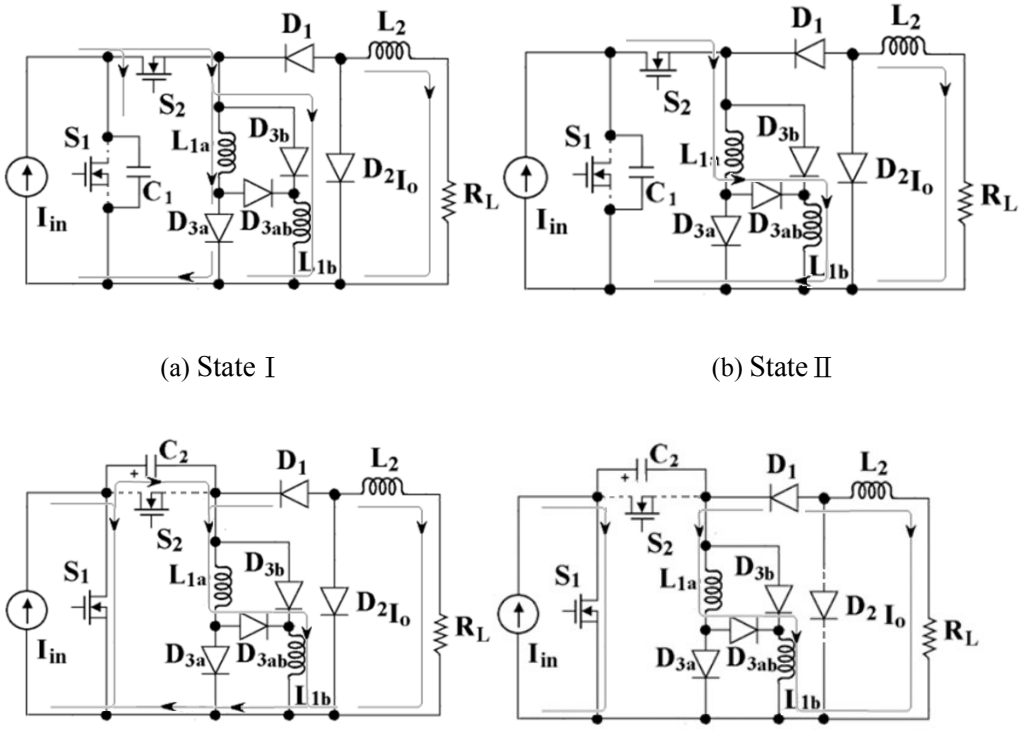
where, $Z_2 = \sqrt{\frac{(n-1)L}{C}}$, $\omega_2 = \sqrt{\frac{1}{(n-1)LC}}$, C_1=C_2=C, L_{1a} =L_{1b}=L_{1c}=…= L_{1n}=L.

For ***State IV[t_3-t_4]:***

$$\begin{cases} v_{s2} = 0 \\ i_{L1n} = I_o - \frac{\pi V_o T_s}{n Z_2 T_2} \end{cases} \tag{6-25}$$

6.3.2 Inverting mode resonant step down switched inductor power converters

1） The operation states of the -1/2-mode resonant SIPC is analyzed. The equivalent circuits are shown in Fig.6-8. The computer simulation waveform is shown in Fig. 6-9. Simulation parameters for the circuit are listed are as same as 1/3-mode resonant step down SIPC. It is assuming the converter is lossless and the output current maintains constant, the calculations of the converter are given below.



(a) State Ⅰ (b) State Ⅱ

(c) State Ⅲ (d) State Ⅳ

Fig. 6-8 The operation states of -1/2 -mode resonant SIPC

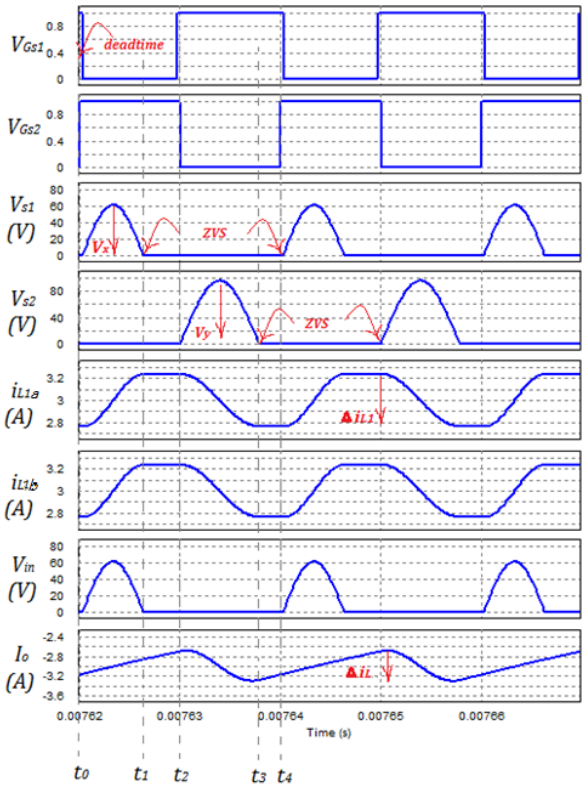


Fig. 6-9 Simulation waveform of -1/2-mode resonant SICP (L_{1a}=L_{1b}=500μH, f_S=50 kHz, I_{in}=6A)

(a) ***State I [t_o-t_1]:*** The switch S_1 is turned off while S_2 is turned on, the equivalent circuit is shown in Fig. 6-8(a). The inductor L_{1a} is connected in parallel with L_{1b} through S_2 and D_{3a}, D_{3b}. The inductor L_2 is connected in series with load R_L to filter the current ripple. The input current I_{in} is divided by the L_{1a}, L_{1b} two parallel branches. The capacitor C_1 resonates with inductor L_{1a}, L_{1b} in paralleled. The inductor current i_{L1a}, i_{L1b}, are gradually increasing to maximum. The voltage Vs_1 across capacitor C_1 resonates in sinewave from zero at t_o to the peak value and back to zero at t_1 in a half resonant cycle. Therefore, switch S_1 is turned on and off at zero voltage. The inductor L_2 and the load R_L is connected in series and freewheeling through

D_2 in an opposite direction.

The state equation is as followed.

$$\begin{cases} I_{in} = C_1 \frac{dv_{s1}}{dt} + i_{L1a} + i_{L1b} \\ v_{s1} = L_{1a} \frac{di_{L1a}}{dt} \\ i_{L1a} = i_{L1b} \end{cases} \quad (6\text{-}26)$$

Assuming $v_{s1} = \mathrm{V}_x sin\omega_1 t$ (6-27)

Substitute (6-27) to equation (6-26), the following equations can be derived.

$$C_1 \frac{dv_{s1}}{dt} = \omega_1 C_1 \mathrm{V}_x cos\omega_1 t \quad (6\text{-}28)$$

$$\omega_1 C_1 \mathrm{V}_x cos\omega_1 t + 2i_{L1a} = I_{in} \quad (7\text{-}29)$$

Then the solution is derived as

$$\begin{cases} v_{s1} = \mathrm{V}_x sin\omega_1 t \\ i_{L1a} = \frac{1}{2}(I_{in} - \frac{\mathrm{V}_x}{Z_1} cos\omega_1 t) \end{cases} \quad (6\text{-}30)$$

where, $Z_1 = \frac{1}{\omega_1 C_1}$, $\omega_1 = \sqrt{\frac{2}{L_{1a} C_1}}$, C_1=C_2, L_{1a} = L_{1b} =L_2.

(b) ***State II [t_1-t_2]:*** The switch S_1 is turned off whereas S_2 still being on. The equivalent circuit is shown in Fig. 6-8(b). The voltage across capacitor C_1 stops resonance at t_1 and remains zero till the half switching cycle t_2. The current flows through inductor reach the maximum at t_1 and remain the maximum value till t_2. The inductor L_2 and the load R_L is connected in series and freewheeling through D_2 in an opposite direction.

The state equation is

$$\begin{cases} v_{s1} = 0 \\ i_{L1a} = I_{in} + \frac{V_x}{Z_1} \end{cases} \quad (6\text{-}31)$$

(c) ***State Ⅲ [t_2-t_3]:*** Switch S_1 is turned on whereas S_2 is switched off, as shown in Fig. 6-8(c). The input current source is shorted by the switch S_1. Inductors L_{1a} and L_{1b} as well as L_2 are connected in series with the load R_L and form a close loop. Inductors L_{1a} and L_{1b} as well as L_2 are delivering the energy to the load R_L in an opposite direction. The capacitor C_2 is connected in paralleled with inductor L_{1a} and L_{1b} and forms a resonant tank. The current flowing through inductor L_{1a} and L_{1b} are gradually decreasing from maximum at t_2 decreased to minimum at t_3 in a half resonant cycle. The voltage Vs_2 across capacitor C_2 resonates from zero at t_2, reaches to the peak value and back to zero at t_3 in sinusoidal waveform.

The state equation is as followed.

$$\begin{cases} C_2 \frac{dv_{s2}}{dt} = i_{L1a} + I_o \\ v_{s2} = -2L_{1a} \frac{di_{L1a}}{dt} \\ i_{L1a} = i_{L1b} \end{cases} \quad (6\text{-}32)$$

Assuming $v_{s2} = V_y sin\omega_2 t$ (6-33)

Substitute (6-33) to equation (6-32),

Similarly to the above analysis, the following equations can be derived.

$$C_2 \frac{dv_{s1}}{dt} = \omega_2 C_2 V_y cos\omega_2 t \quad (6\text{-}34)$$

$$i_{L1a} = -I_o + \frac{V_y}{Z_2} cos\omega_2 t \quad (6\text{-}35)$$

Then the solution is.

$$\begin{cases} v_{s2} = \mathrm{V}_y sin\omega_2 t \\ i_{L1a} = -I_o + \frac{\mathrm{V}_y}{Z_2} cos\omega_2 t \end{cases} \quad (6\text{-}36)$$

Where, $Z_2 = \frac{1}{\omega_2 C_2}$, $\omega_2 = \sqrt{\frac{1}{2L_{1b}C_2}}$, C_1=C_2, L_{1a} = L_{1b}=L_2.

(d) ***State Ⅳ [t_3-t_4]:*** Switch S_1 is still being on whereas S_2 is turned off. The voltage across capacitor C_2 stops resonance at t_3 and remains zero at t_4 the end of half switching cycle. The current flows through inductor L_{1a} and L_{1b} reach the minimum value at t_3 and remain it till t_4 the half switching cycle. The inductor L_2 and the load R_L is connected in series and freewheeling through D_2 in an opposite direction.

The state equation is

$$\begin{cases} v_{s2} = 0 \\ i_{L1a} = -I_o - \frac{\mathrm{V}_y}{Z_2} \end{cases} \quad (6\text{-}37)$$

2） Generalized Equations of inverting -1/2 mode resonant SIPCs

From above mentioned, the dc component of the current flowing through the inductor L_1 (same as L_2) in equation (6-30) and (6-36) respectively should be equal, then there is

$$-I_o = \frac{1}{2} I_{in} \quad (6\text{-}38)$$

Therefore, the following relationship can be derived

$$I_o = -\frac{1}{2} I_{in} \quad (6\text{-}39)$$

By using input output power balancing.

$$I_{in}V_{in} = \frac{I_{in}}{T_s}\int_0^{T_s} v_{in}\,dt = \frac{I_{in}}{T_s}\int_0^{\frac{T_1}{2}} V_x sin\omega_1 t\,dt + \frac{I_{in}}{T_s}\int_0^{\frac{T_2}{2}} V_y sin\omega_2 t\,dt = V_o I_o \quad (6\text{-}40)$$

The value of voltageV_x and V_y can be solved

$$V_x = \frac{\pi V_{in} T_s}{T_1} \quad (6\text{-}41)$$

$$V_y = \frac{\pi V_o T_s}{T_2} \quad (6\text{-}42)$$

Where, I_{in} is the input current, $I_o$is the output current, T_s is the switching cycle, T_1 and T_2 are the resonant cycle.

Therefore, the generalized equations of -1/2 mode resonant SIPC are

For ***State I [t_o-t_1]:***

$$\begin{cases} v_{s1} = \frac{\pi V_o T_s}{2T_1} sin\omega_1(t-t_0) \\ i_{L1a} = \frac{1}{2}(I_{in} - \frac{\pi V_o T_s}{2Z_1 T_1} cos\omega_1(t-t_0)) \end{cases} \quad (6\text{-}43)$$

where, $Z_1 = \sqrt{\frac{L_{1a}}{2C_1}}$, $\omega_1 = \sqrt{\frac{2}{L_{1a}C_1}}$, C_1=C_2, L_{1a}= L_{1b} =L_2.

For ***State II [t_1-t_2]:***

$$\begin{cases} v_{s1} = 0 \\ i_{L1a} = I_{in} + \frac{\pi V_o T_s}{2Z_1 T_1} \end{cases} \quad (6\text{-}44)$$

For ***State III [t_2-t_3]:***

$$\begin{cases} v_{s2} = \frac{\pi V_o T_s}{2T_2} sin\omega_2(t-t_2) \\ i_{L1a} = -I_o + \frac{\pi V_o T_s}{2Z_2 T_2} cos\omega_2(t-t_2) \end{cases} \quad (6\text{-}45)$$

$Z_2 = \sqrt{\frac{2L_{1b}}{C_2}}$, $\omega_2 = \sqrt{\frac{1}{2L_{1b}C_2}}$, C_1=C_2, L_{1a}= L_{1b} =L_2.

For ***State IV[t_3-t_4]:***

$$\begin{cases} v_{s2} = 0 \\ i_{L1a} = -I_o - \frac{\pi V_o T_s}{2Z_2 T_2} \end{cases} \quad (6\text{-}46)$$

3） Generalized Equations of inverting mode -1/n-mode resonant SIPCs

The extension of the inverting-mode step down resonant SIPC is shown in Fig. 6-5. As noticed, the current of the inductor L_{1a}, L_{1b}, L_{1c},…L_{1n} is denoted by $i_{L1a}, i_{L1b,}\ i_{L1c}\ldots.\ i_{L1n}$, respectively. For -1/n mode resonant SIPC, there is n switched inductor cells. The generalized equation of -1/n mode resonant SIPC can be described as follows.

For ***State I [t_o-t_1]:***

$$\begin{cases} v_{s1} = \frac{\pi V_o T_s}{nT_1} sin\omega_1(t - t_0) \\ i_{L1n} = \frac{1}{n}(I_{in} - \frac{\pi V_o T_s}{nZ_1 T_1} cos\omega_1(t - t_0)) \end{cases} \quad (6\text{-}47)$$

where, $Z_1 = \sqrt{\frac{L}{2C}}$, $\omega_1 = \sqrt{\frac{2}{LC}}$, C_1=C_2=C, L_{1a} =L_{1b}=L_{1c}=…= L_{1n}=L_2=L.

For ***State II [t_1-t_2]:***

$$\begin{cases} v_{s1} = 0 \\ i_{L1n} = \frac{1}{n}(I_{in} + \frac{\pi V_o T_s}{nZ_1 T_1}) \end{cases} \quad (6\text{-}48)$$

For ***State III [t_2-t_3]:***

$$\begin{cases} v_{s2} = \frac{\pi V_o T_s}{nT_2} sin\omega_2(t - t_2) \\ i_{L1n} = -I_o + \frac{\pi V_o T_s}{nZ_2 T_2} cos\omega_2(t - t_2) \end{cases} \quad (6\text{-}49)$$

$Z_2 = \sqrt{\frac{nL}{C}}$, $\omega_2 = \sqrt{\frac{1}{nLC}}$, C_1=C_2=C, L_{1a} =L_{1b}=L_{1c}=…= L_{1n}=L_2=L.

For ***State IV[t_3-t_4]:***

$$\begin{cases} v_{s2} = 0 \\ i_{L1n} = -I_o - \frac{\pi V_o T_s}{nZ_2 T_2} \end{cases} \quad (6\text{-}50)$$

6.3 Design

The design of a 1/3-mode resonant step-down converter is shown in the following as an example.

(a) Design the specifications:

I_{in}=6A, P_o=30 W, switching frequency=50 kHz.

(b) The resonant frequency f_o is chosen to be higher than the switching frequency f_s to achieve zero voltage switching. From equation (6-5) and (6-11), there are two resonant frequency ω_1, ω_2. The worse case ω_2 is used for the calculation. A 10%-20% higher frequency is used to ensure zero voltage switching.

$$\omega_2 = 1.1(2\pi f_s) \tag{6-51}$$

$$f_2 = 1.1 f_s \tag{6-52}$$

This gives a resonant frequency f_2=$55kHZ$.

(c) The current ripple flowing through the inductor L_{1a}, L_{1b} must be small compared with dc level. The peak to peak value from equations (6-5) and (6-11)

$$\Delta i_{L1a} = \frac{4\pi V_{in} T_s}{Z_2 T_2} \tag{6-53}$$

where, $Z_2 = \frac{1}{C_2\omega_2}$, $\omega_2 = \sqrt{\frac{1}{2L_{1b}C_2}}$

A maximum ripple of 10% of the dc component is allowed on the inductor. Hence it gives Z_2 =345.6Ω

(d) The resonant component can be therefore calculated by the angular frequency and

impedance from above equation

$L_{1a}= L_{1b}= L_2=L=$ 0.5mH

$C_1=C_2= C=$0.0084μF

L and C are chosen to be 0.01μF and 0.5mH

(e) The inductor L_3 is selected to be large and is with low ripple as well.

(f) The transistor rating voltage can be calculated by equation (6-16) and (6-17), In this case, $V_x = 34.56V$, $V_y = 34.56V$. Therefore, they are chosen a rating of at least 50V.

6.4 Experimental Results

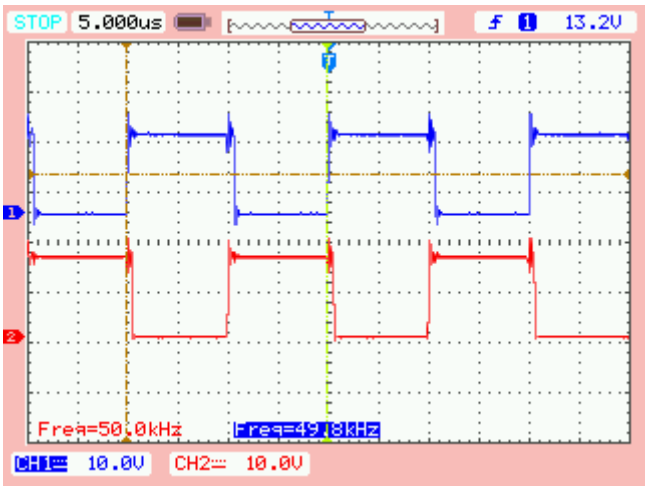
The 1/3-mode resonant switched-inductor current source converter as shown in Fig. 6-1 (b) has been built in the laboratory. The experimental specification and the component values of the converter have been outlined in Table 6-2.

Table 6-2 Specification and components of the 1/3-mode resonant SIPC

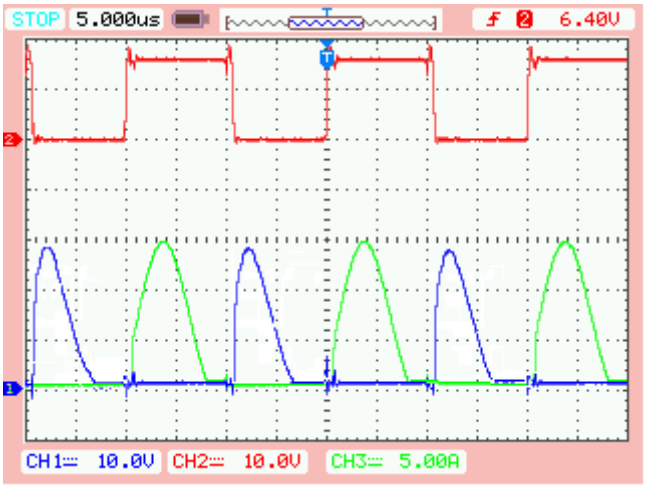
Input current I_{in}	6A
Output current I_o	2A
Output power	32W
Switching Frequency (f_s)	50kHz
L_{1a}	0.5mH
L_{1b}	0.5mH
C1	0.01μF
C2	0.01μF
D_1 and D_2 (schottky diode)	*MBR1645*
S_1 *and* S_2 (N channel MOSFET)	*IRFB4410*

The designed 1/3-mode resonant converter is working with output power around 32W. The typical experimental waveforms are obtained as shown in Fig.7-6. It is noticed a small negative deadtime is need between the two complementary gate signals V_{GS1} and V_{GS2}. The voltage spike under switches S_1 and S_2 has been eliminated as shown in Fig. 6-6(a). The voltage of Vs_1 and Vs_2 gradually change in sinusoidal manner. Therefore, both transistors are turned on and off under zero voltage switching shown in Fig. 6-6 (b).The waveforms of inductor currents i_{L1a}, i_{L1b} and I_o are shown in Fig. 6-6 (c) and (d). As it can be seen, it is a I_{in}/3 dc component with a small ripple on the current of i_{L1a}, $i_{L1b.}$ There is small deviation because of the energy loss in the circuit, It agrees well with the theoretical analysis in Section Ⅲ-Ⅵ.

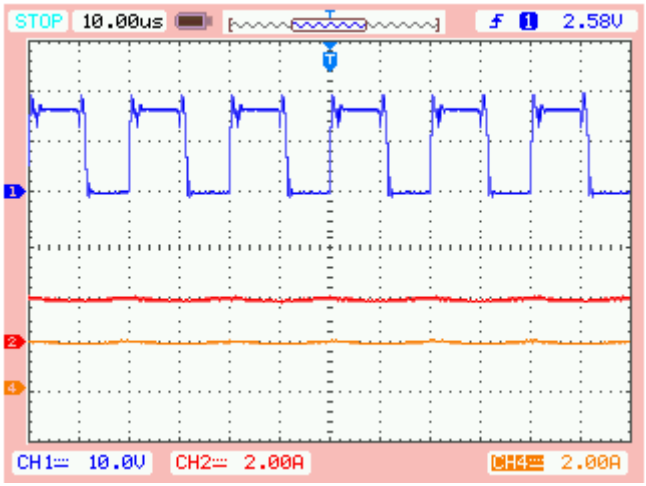
The waveforms of inductor currents with different time bases are also given in Fig.6-7. The same as the result found in simulation results, the current flowing through both inductors are almost the same and are close to 2A which is 1/3 of the input current.



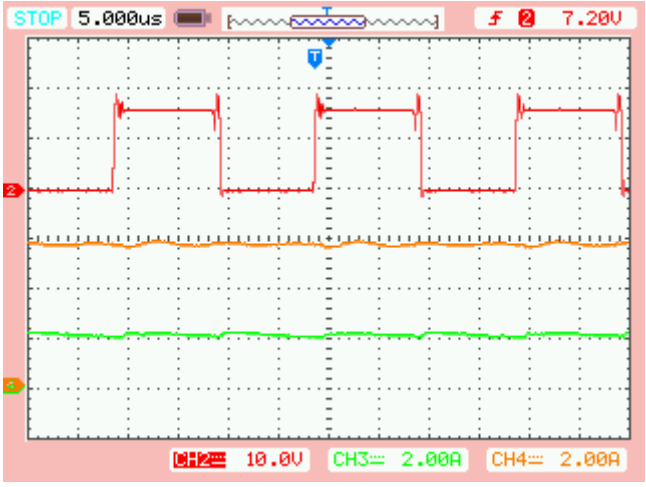
(a) Ch1: V_{GS1}; Ch2: V_{GS2};



(b) Ch1: V_{S2}; Ch2: V_{GS1}; Ch3: V_{S1};



(c) Ch2: V_{GS1}; Ch3: i_{L1a}; Ch4: i_{L1b}



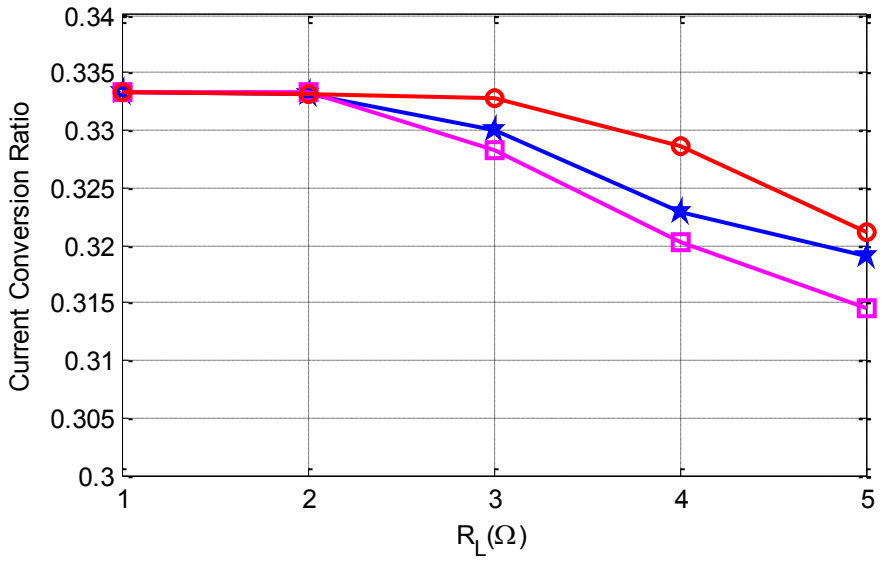
(d) Ch2: V_{GS2}; Ch3: I_o; Ch4: I_{in}

Fig. 6-10 Experimental waveforms for 1/3-mode resonant SIPC with 6A constant input current and 3.Ω pure-resistive load.

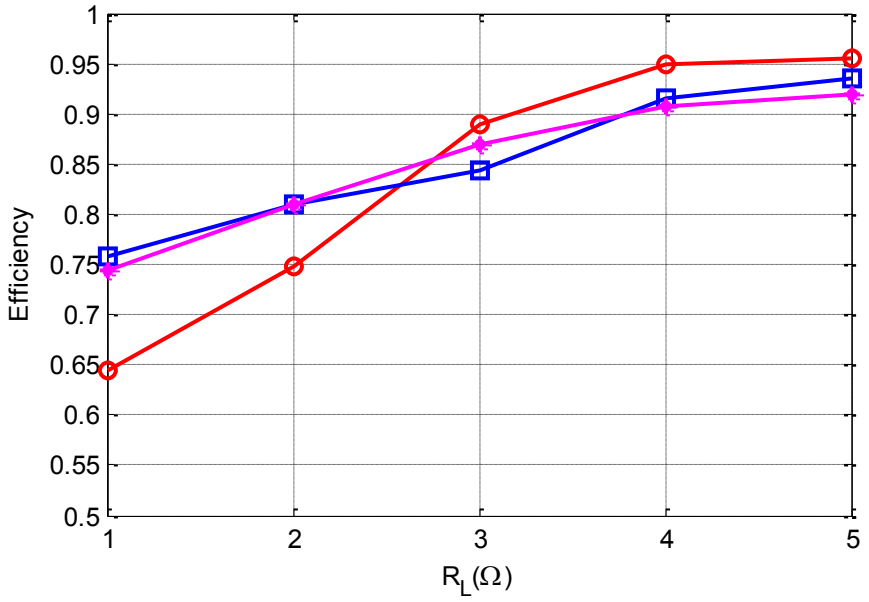
Fig. 6-11 plots the current conversion ratio and efficiency versus load resistant of the 1/3-mode resonant SIPC. By testing the load resistor between 1-5Ω, the conversion ratio is 0.333 when load resistor is 1Ω. With the input current I_{in}= 6A, it can be seen that can maintain around values of 0.315 to 0.333, instead of the theoretical value 1/3. Increasing load resistance R_L also decreases the conversion ratio slightly due to the handling of higher power.

The power efficiency is 92% when load resistor is 5Ω with input current I_{in}= 6A. Fig. 6-11(b) the efficiency of the prototype with zero voltage switching is up to 95.6% for higher load resistance for higher power

At light load, power loss in the circuit is mainly due to the diode, which have forward bias voltage drop. At high load, the power loss is mainly because of conducting loss of the drain to source resistance of the transistors. Fig. 6-11 (a) shows the current conversion ratio decreases when the output power increases. Other than the voltage drop on the diodes, when the current increases, the voltage drop on both transistors increases, hence the voltage conversion ratio decreases. The switching loss is reduced significantly because all the switches are under soft-switching shown in Fig. 6-11. Resonant soft-switching technique is introduced to improve the power conversion efficiency to some extent [14]. And employing inductors with larger inductance and switches with smaller on-resistance can also improve the efficiency as well.



(a) Current ratio versus load



(b) Measured efficiency versus load

Fig. 6-11 Measured current conversion ratio and efficiency of the resonant 1/3-mode SIPC

6.6 Conclusions

This chapter has proposed two families of step down switched inductor power converter, one is inverting converters, the other is non-inverting power converter.

Both families are operating under zero voltage switching. The high voltage spike across the transistors has been eliminated. Both switching loss and EMI have been reduced. The output current can be fractional of the input current and only two transistors needed. The detailed analysis including mathematical modeling, generalized equation, computer simulation and experiment have been presented. The experimental result has confirmed the theoretical prediction.

Chapter 7

Theoretical Modeling of the Storage Energy Envelope of High Frequency AC Reactive Components to Predict Chaos Boundary

7.1 Introduction

By definition, a qualitative change in the dynamics that occurs as a system parameter is changed is called bifurcation [170]. Bifurcation is a nonlinear phenomenon that some of nonlinear systems exist in their nonlinear switching operation. Generally, chaos is an uncertain behavior after bifurcation. Some reports have reviewed that the ubiquitous chaotic phenomena can also occur in a switched capacitor circuit [171-172]. Discrete maps were simulated using digital computer to analyzing the chaos and bifurcation phenomena. Since the simulation of such circuit gives real-time solutions, it is ideally suited for carrying out a comprehensive multi-parameter bifurcation analysis. In this chapter, a new method to study the nonlinear dynamics of the power electronic is first developed in conventional SMPC, which will further applied in switched capacitor power converter.

Power electronics system consists of high frequency AC and also DC components. The energy storage components are impressed with high frequency AC signal in the switched-mode power converters. The ability of the voltage conversion for the

converter is based on the energy storage in the passive components which are mainly the inductor and capacitor. Energy is stored temporary in the components and then released to output through the transistor's on and off operations. The output voltage is therefore regulated.

The energy storage of the devices is an interesting parameter to understand the efficiency and stability. In 2003, the new concept of energy storage factor in DC converters was firstly introduced by Cheng in reference [173-174]. In these papers, storage energy of inductor and capacitor is defined as the difference between maximum energy and minimum energy in one cycle. Another new concept is the Energy Factor that is an analogy to power factor in AC system and is defined to be the ratio of storage energy to output energy in one cycle. These new concepts provide a new measurement on the characteristics of dc converters. Evolvement of the new concepts have not done to analyze the circuit or to facilitate the design of the power electronic system. On the other hand, new control algorithm to analyze the stability of the system based on energy balance has been reported [175, 176], and a new energy based switching scheme for controlling DC-DC converter circuit has been proposed and to analyze its stability by Pawan Gupta and Amit Patra based on the energy balance theory in 2005 [177, 178], however, the stability of the energy stored in capacitor and inductor, and how the energy evolves as the parameters vary, that is

meaningful to designers, has not been explored The recent research on stability has concentrated on Border Collision Analysis [179], Path Necessary Conditions [180] and rectifier [181-182]. It is interesting now to study the correlation between the bifurcations and the energy storage factor for high frequency power conversion.

The study of bifurcation in switched mode power converter has been conducted for years [183-184]. Prediction of the bifurcation in Cuk converter using bifurcation diagram [185] and buck-boost using correlation techniques [186] has attracted much attention.

The converters presented in this thesis are based on switched-passive converter with inductor or capacitor as the energy storage. It can be seen that the switched-inductor is inherently stable as the transistors are all operated under a fixed 50% duty ratio. The duty ratio does not vary with load, frequency, source voltage and other parameters. Therefore the converters are stable [74, 82, 84, 142, 138]. On the other hand, the classical DC-DC converter such as Buck, Boost and Buck-boost may exhibit stability concern, various analyses have been done extensively in the past, the present work is biased to a new energy storage stability analysis for the SMPS and using Buck-boost as an example study.

In this chapter the storage energy in DC system is used to investigate the instability of the buck-boost converter. In the past the parameter sensitivity [187] and autonomous

chaotic system[188] have been investigated for stability. Bifurcation and chaos are observed based on the discrete map. Stability and equilibrium point for electric circuit have been examined in Ref [189]. Zero energy is clearly obtained in stable period one, and the same value and opposite direction are obtained in period two. The maximum storage energy has been obtained and is shown in the chapter. Simulations of bifurcation and chaos of energy are examined with the variation of different parameters. These results can provide a new guideline to design a stable system and provide a new control algorithm for power electronic system.

7.2 Buck-boost Converter

7.2.1 Circuit and Mathematic Description

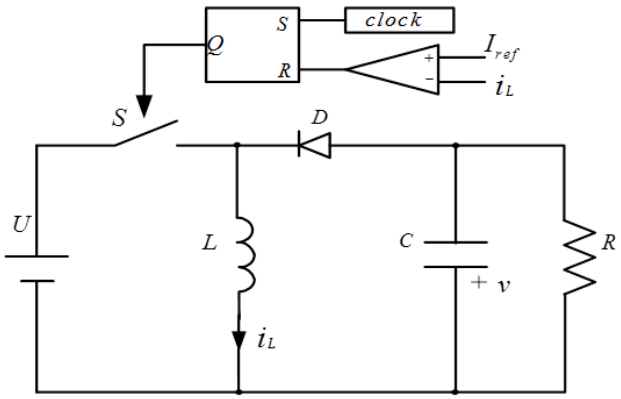


Fig. 7-1 Peak current mode control of Buck-boost converter

Fig. 7-1 shows a typical buck-boost converter under peak current mode control. It is also assumed that the components in the circuit are ideal and no parasitic effects are considered. The equations can be summarized as follows when the

buck-boost converter operates in discontinuous mode.

(1) State 1: S is on, D is off,

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -1/(RC) \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} + \begin{bmatrix} U/L \\ 0 \end{bmatrix} \tag{7-1}$$

(2) State 2: S is off, D is on,

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} 0 & -1/L \\ 1/C & -1/(RC) \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{7-2}$$

(3) State 3: S is off, D is off,

$$\begin{bmatrix} \dot{i}_L \\ \dot{v}_c \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & -1/(RC) \end{bmatrix} \begin{bmatrix} i_L \\ v_c \end{bmatrix} \tag{7-3}$$

7.2.2 Piecewise Discrete Map Derivation

In the following, T_s is the switching cycle, and the sample time is nT_s, then $i_n = i(nT_s),\ v_n = v(nT_s)$, $n = 1,2,3,\cdots$, where $i_n,\ v_n$ is the current through inductor and the voltage in the capacitor respectively. Then the following equations (7-4), (7-5), (7-6) can represent equations (7-1), (7-2) and (7-3) [181].

It is assumed that t_n is the time such that the inductor current i reaches I_{ref} from the nT_s at state 1, t_d is the time that the inductor current reaches 0 from $(nT_s + t_n)$ in state 2.

If $t_n \geq T_s$, from nT_s to $(n+1)T_s$, the converter operates in state 1, the equation (7-1) can be solved as follows

$$\begin{cases} i_{n+1} = i_n + \dfrac{UT_s}{L} \\ v_{n+1} = v_n e^{-T_s/RC} \end{cases} \tag{7-4}$$

If $(t_n + t_d) \geq T_s$, from nT_s to $(n+1)T_s$, the system operates in state 1 and state 2, he inductor current and the capacitor voltage in $(n+1)T_s$ is solved as:

$$\begin{cases} i_{n+1} = e^{\delta(T_s - t_n)}\left[a\cos\omega(T_s - t_n) + b\sin\omega(T_s - t_n)\right] \\ v_{n+1} = -Le^{\delta(T_s - t_n)}\left[(a\delta + b\omega)\cos\omega(T_s - t_n) + (b\delta - a\omega)\sin\omega(T_s - t_n)\right] \end{cases} \tag{7-5}$$

And if $(t_n + t_d) < T_s$, in nT_s to $(n+1)T_s$, the system operates in state 1, 2 and comes into state 3. Then the solution of equation (7-3) is:

$$\begin{cases} i_{n+1} = 0 \\ v_{n+1} = v_2(t_d)e^{-(T_s - t_n - t_d)/RC} \end{cases} \tag{7-6}$$

Where, $t_n = \dfrac{L}{U}(I_{ref} - i_n)$, $\delta = -1/2RC$, $\omega = \sqrt{1/LC - 1/4R^2C^2}$, $a = I_{ref}$,

$b = -\dfrac{1}{\omega}\left(\dfrac{v_n e^{-t_n/RC}}{L} + \delta I_{ref}\right)$, $t_d = \dfrac{1}{\omega}arctg\left(-\dfrac{a}{b}\right)$,

$v_2(t_d) = -Le^{\delta t_d}\left[(a\delta + b\omega)\cos\omega t_d + (b\delta - a\omega)\sin\omega t_d\right]$

7.3 Definition of Energy Storage

The stroboscopic map of the inductor current and output voltage are as shown in Fig. 7-2. The storage energy in the inductor and capacitor is calculated based on the stroboscopic map of Fig.7-2.

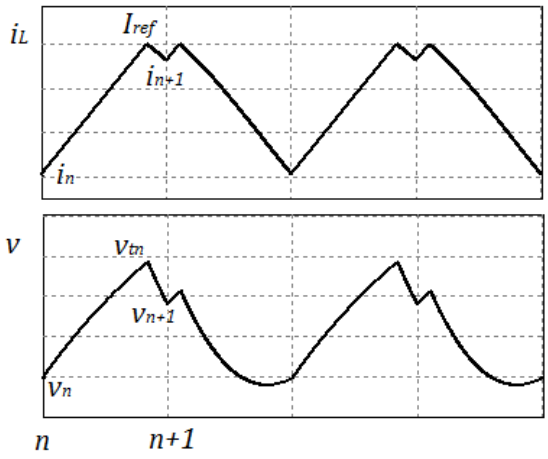


Fig. 7-2 the stroboscopic map of the inductor current and output

7.3.1 Storage Energy for Inductor

The positive maximum variation of storage energy for the inductor in one switching cycle of the buck-boost converter under peak current control mode is defined as S_{LP} :

$$S_{LP} = \frac{1}{2} L(I_{ref}{}^2 - i_n{}^2) \tag{7-7}$$

The negative maximum variation of storage energy for the inductor in one switching cycle of the buck-boost converter under peak current control mode defined as S_{LN} :

$$S_{LN} = \frac{1}{2} L(i_{n+1}{}^2 - I_{ref}{}^2) \tag{7-8}$$

The variation of the storage energy for the inductor in one switching cycle in buck-boost converter of peak current mode is defined as S_L, which can be calculated by $S_L = S_{LP} + S_{LN}$, incorporating equation (7-7) and equation (7-8), then there is

$$S_L = \frac{1}{2} L(i_{n+1}{}^2 - i_n{}^2) \tag{7-9}$$

where i_{n+1}, i_n can be calculated by equations (7-4), (7-5) and (7-6).

7.3.2 Storage Energy for Capacitor

The positive maximum variation of storage energy for the capacitor in one switching cycle of the buck-boost converter under peak current control mode is defined as S_{CP} and is given as follows,

$$S_{CP} = \frac{1}{2} C(v_{tn}{}^2 - v_n{}^2) \tag{7-10}$$

where v_{tn} is the voltage of capacitor when the current reaches to I_{ref}.

The negative maximum variation of storage energy for the capacitor in one switching cycle of the buck-boost converter under peak current control mode defined as S_{CN} and is given as follows,

$$S_{CN} = \frac{1}{2} C(v_{n+1}{}^2 - v_{tn}{}^2) \tag{7-11}$$

where v_{tn} is the voltage of capacitor when the current reaches to I_{ref}.

The variation of the storage energy for the capacitor in one switching cycle in buck-boost converter of peak current mode is defined as S_C, which can be calculated by $S_C = S_{CP} + S_{CN}$, incorporating equation (7-10) and equation (7-11), then there is

$$S_C = \frac{1}{2} C(v_{n+1}{}^2 - v_n{}^2) \tag{7-12}$$

where, v_{n+1}, v_n can be calculated by equations (4), (5) and (6).

7.4 Storage Energy Characteristic

7.4.1 Simulation results for Different Source Voltage

The simulation is firstly to examine the different source voltage values for U. The circuit parameters are used for the examination of the possible bifurcation phenomena: T_s=50μs, L=0.3mH, C=4μF, R=40Ω and I_{ref}=4A. The citcuit is simulated by Matlab 7.5, numerical results of the evolvement of the storage energy are given based on the stroboscopic maps as follows.

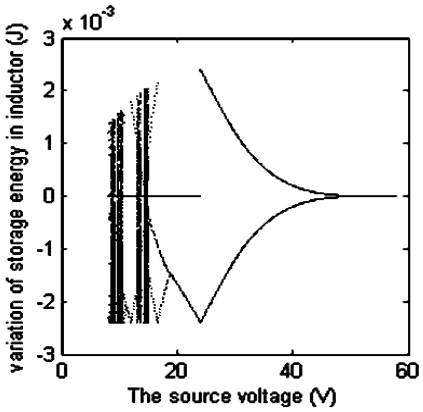


Fig. 7-3 (a)

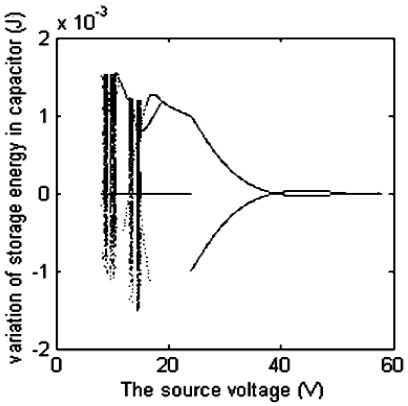


Fig. 7-3 (b)

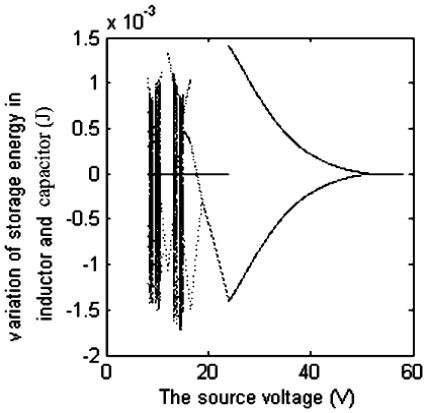


Fig. 7-3 (c)

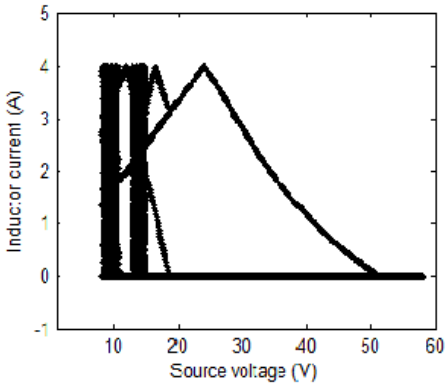


Fig. 7-3 (d)

Fig. 7-3 (a), (b), (c), Bifurcation diagram of storage energy in inductor, capacitor , the sum of inductor and capacitor, respectively (d)traditional bifurcation diagram of inductor current (the source voltage is the bifurcation parameter).

In Fig 7-3(a), one of the most salient dynamical features of the circuit is that the variation of the storage energy in inductor is zero when the system operates in stable period one, then period two happens when the source voltage is about 52V. The interesting point is that the storage energy has the same value and opposite direction against the zero axis. When the storage energy is about 1.5×10^{-3} J, anther period two occurs, and then more complex bifurcation occurs, until the system goes into chaos. Similar phenomena are observed in Fig. 7-3 (b) and (c). Fig. 7-3 (d) shows traditional bifurcation diagram of inductor current. Compared with Fig. 7-3. (a), (b), (c), it has the same bifurcation point and characteristic.

7.4.2 Simulation Results for Different Capacitors

The simulation is then to examine the instability of the different capacitance values. The circuit parameters are used for as follows: T_s=50μs, *U=35V,* L=0.3mH, R=40Ω and I_{ref}=4A. Bifurcation diagrams of the evolvement of the storage energy are given as below.

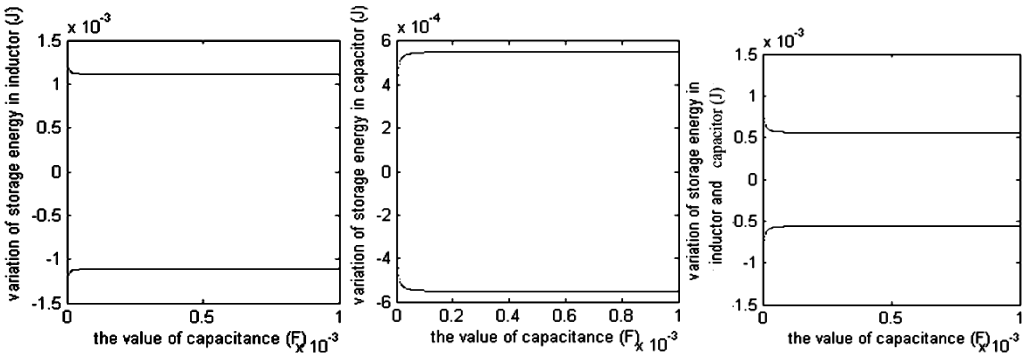


Fig. 7-4 (a) Fig.7-4 (b) Fig. 7-4(c)

Fig. 7-4 (a), (b), (c) Bifurcation diagram of storage energy in inductor, capacitor and the sum of inductor and capacitor respectively (the value of capacitance is the bifurcation parameter).

The storage energy in capacitor always operates in period two under given parameters, which is shown in Fig. 7-4 (a), (b), (c).

7.4.3 Simulation Results for Different Inductors

Different inductor values are used to investigate the characteristics of the storage energy of the system. The circuit parameters are given as: T_s=50μs, U=35V, C=4μF, R=40Ω and I_{ref}=4A. Dynamic behaviours of bifurcation and chaos of storage energy are observed as shown in Fig. 7-5.

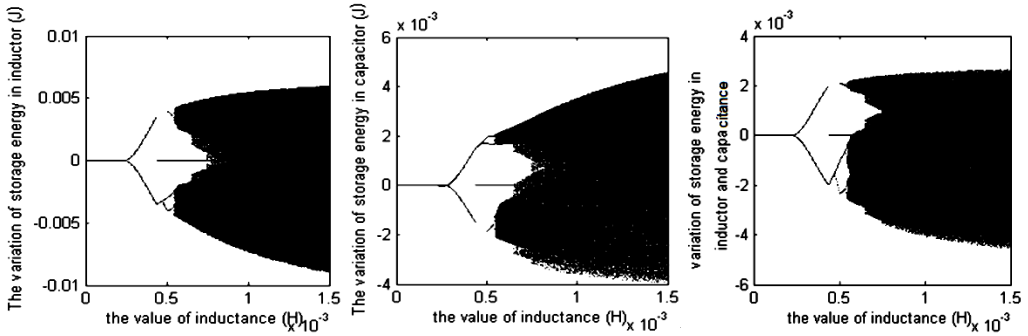


Fig. 7-5(a) Fig. 7-5 (b) Fig. 7-5(c)

Fig. 7-5 (a), (b), (c) Bifurcation diagram of storage energy in inductor, capacitor and the sum of inductor and capacitor respectively (the value of inductance is the bifurcation parameter).

In Fig 7-5. (a), (b), (c), the variation of the storage energy in inductor is zero when the system operates in stable period one, then period two happens when the value of inductance is 0.3 mH, and the storage energy has the same value and opposite direction when goes smoothly to period 2, and through more complex bifurcation to the storage energy in inductor and capacitor goes into chaos.

7.4.4 Simulation Results for Different Loads

The simulation is to study the characteristic of storage energy under different loads. The circuit parameters are given as below: T_s=50μs, U=35V, L=0.3mH, C=4μF and I_{ref}=4A. Numerical results of the evolvement of the storage energy are given as following diagram.

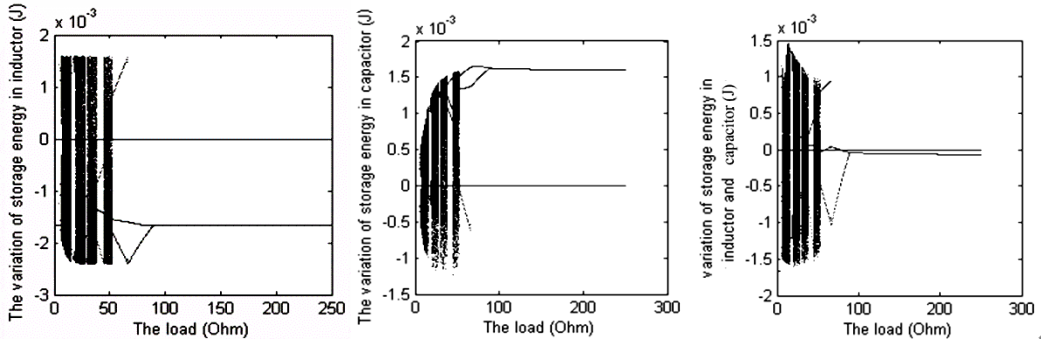


Fig. 7-6(a) Fig.7-6 (b) Fig. 7-6(c)

Fig. 7-6 (a), (b), (c) Bifurcation diagram of storage energy in inductor, capacitor and the sum of inductor and capacitor respectively (the value of the load is the bifurcation parameter).

In Fig. 7-6 (a), (b), (c), the variation of the storage energy in inductor is in period two and through complex bifurcation to chaos under given parameters when the

load is varied from 0-250 Ω. Under the given parameters, the system is operating in chaos to bifurcation alternatively 4 times when the load is varied from 0-50 Ω.

7.5 The boundary of stability of the energy in reactive components

7.5.1 Boundary of chaos of Storage Energy versus inductance with various capacitance

Different capacitance values are used to investigate the envelope of the storage energy of the system, which represents the boundary of the storage energy in (a) inductor, (b) capacitor, (c) sum of inductor and capacitor. The circuit parameters are given as follows: T_s=50μs, U=35V, R=40Ω and I_{ref}=4A. Envelope of storage energy is obtained in Fig. 7-7 shown.

As is shown in Fig. 7-7(a), (b) and (c), the envelope of stored energy under chaos which means that the maximum variation of the storage energy in inductor, capacitor and sum of inductor and capacitor is illustrated respectively with different capacitors when chaos happens. The value of inductance is the bifurcation parameter. As it can be seen, in Fig. 7-7(a), (b), (c), the upper envelope of the storage energy which means positive maximum storage energy nearly the same when capacitor varies; the lower envelope of the storage energy which means negative maximum storage energy only has slightly change when capacitor varies when chaos happens, which indicates that even the system

operates in chaos, storage energy still operates in a limited area, and the storage energy does not vary very much.

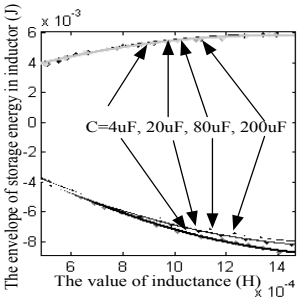


Fig. 7-7(a)

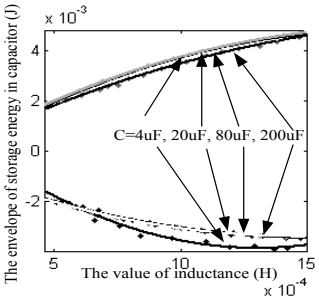


Fig. 7-7(b)

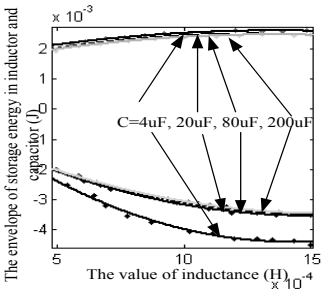


Fig. 7-7(c)

Fig. 7-7 (a), (b), (c) Boundary of chaos of storage energy in inductor, capacitor and the sum of inductor and capacitor respectively with different capacitors (the value of inductance is the bifurcation parameter).

7.5.2 Boundary of chaos storage energy versus inductance with various load

Different loading resistances are used to investigate the characteristic of the maximum storage energy of the system. The circuit parameters are given as follows: T_s=50μs, U=35V, C=20μF and I_{ref}=4A. Envelope of storage energy in (a) inductor, (b) capacitor, (c) sum of inductor and capacitor is observed as Fig. 7-8 shown.

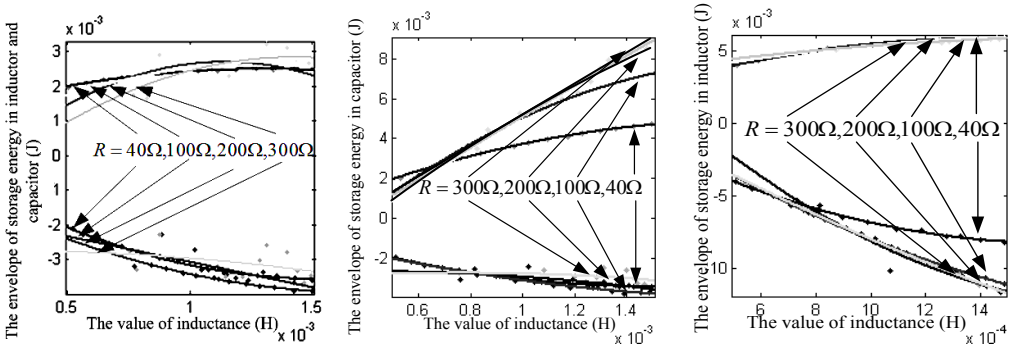


Fig. 7-8(a) Fig. 7-8 (b) Fig.7-8(c)

Fig. 7-8 (a), (b), (c) Boundary of chaos of storage energy in inductor, capacitor and the sum of inductor and capacitor respectively with different loads (the value of inductance is the bifurcation parameter).

Fig. 7-8(a), (b), (c) shows the chaos boundary of storage energy, which means the maximum variation of the storage energy in inductor, capacitor and inductor and capacitor respectively with different loadings when chaos happens, and the value of inductance is the bifurcation parameter. As we can see, in Fig. 7-8(a), (b), (c), the upper envelope of storage energy which means positive maximum storage energy and the lower envelope of storage energy which means negative maximum storage energy both have slightly changes when load varies during chaos happens, which indicates that even the system operates in chaos, storage energy still operates in a limited area.

7.6 Generalized characteristics of chaos boundary

7.6.1 Chaos boundary storage energy with specific capacitance range

As mentioned before, the maximum variation in the passive component is confided in a specific area before entering the chaos, which facilitates the design

of a stable system. The maximum storage energy in passive components has been simulated and it is observed that they all follow a maximum energy boundary. The boundary of maximum storage energy can be unified by a single equation. The boundary equation has been obtained in each chaos case which outlines the maximum storage energy variation when the parameter of the circuit is in a certain range.

Fig. 7-9(a), (b) and (c) show the equation of the boundary of chaos of storage energy in inductor, with the capacitor fixed in a range of capacitance from 4μF to 200μF. Since the capacitance is not a sensitive parameter to the instability of the circuit which is as shown in Fig. 7-4, the boundary of the chaos of the storage energy in the inductor has small change when the capacitance varies from 4μF to 200μF. even though, when the capacitance is smaller, the boundary is larger. This is important information for the definition of energy in reactive component during the boundary of the chaos. The envelop equation can be found out by curving fitting and the equation for Fig 7-9(a), (b) and Fig 7-9(c) are obtained. Each is defined as the storage energy boundary in inductor during chaos. Fig 7-9(a)-(c) will provide a simple representation to the boundary of chaos. It provides a useful information to design a power converter by looking into its energy envelop to avoid falling into chaos rather than going through the detailed

simulation of bifurcation which is tedious and time consuming. By only calculating the energy stored in the inductor using the equation representing the boundary can predict chaos instead of simulation or calculating the complex state equation

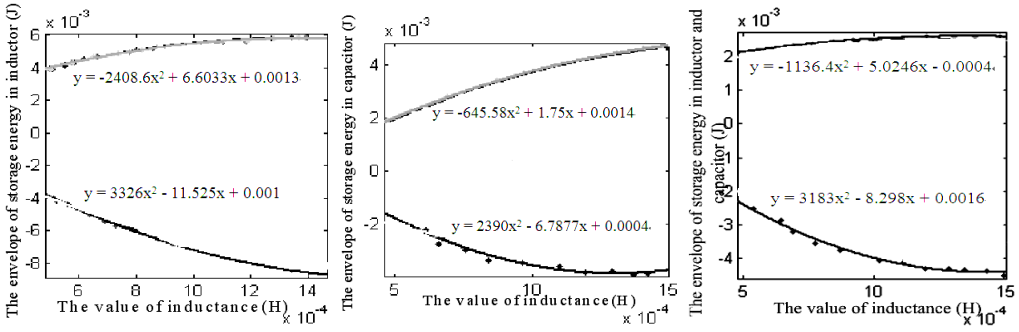


Fig.7-9(a) Fig. 7-9(b) Fig. 7-9(c)

Fig. 7-9 The equations of the stability boundary for storage energy in inductor, capacitor and the sum of inductor and capacitor respectively with capacitor range 4μF to 200 μF.

7.6.2 Maximum storage energy with specific loading range

Fig. 7-10 (a), (b) (c) show the envelope of the maximum storage energy against inductance with a specific loading range. The boundary of chaos represents an unstable region of the system, which should be avoided by the designers when a system is designed. The region of chaos can be simply avoided by the given information.

This model allows a single equation to represent the maximum energy storage that will make the design of high frequency power converter simple. When the circuit is operating in period 1, the storage energy in inductor or capacitor in one

switching cycle is zero; when the circuit is operation in period 2, the storage energy in inductor or capacitor is two value with same value and opposite direction; when the circuit is operation under chaos, the storage energy in inductor or capacitor has two boundaries. By obtaining the equation of boundary in advance can predict the characteristic of the circuit avoiding the detail simulation and calculation. As the calculation from period 1 to chaos is a very time consuming process, the proposed method of chaos equation based on energy storage can now be used for the prediction of the circuit design and understanding. The proposed method is a simplified approach to give a quick design method to avoid circuit chaos.

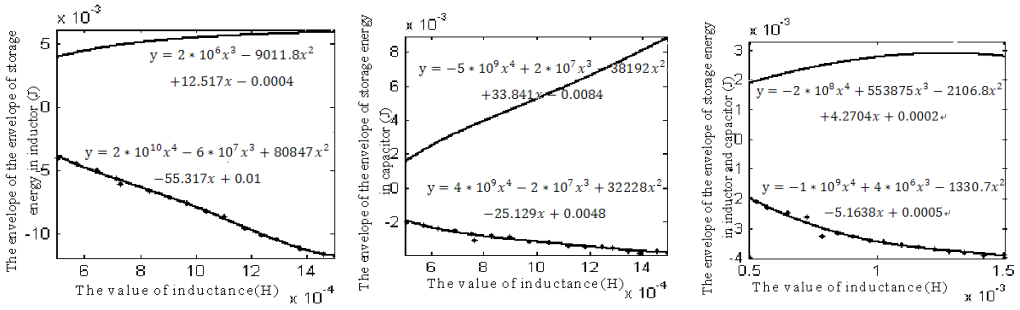


Fig. 7-10 (a) Fig. 7-10 (b) Fig. 7-10 (c)

Fig. 7-10 The equations of the stability boundary for storage energy in inductor, capacitor and the sum of inductor and capacitor respectively with load range 40 Ω to 300 Ω.

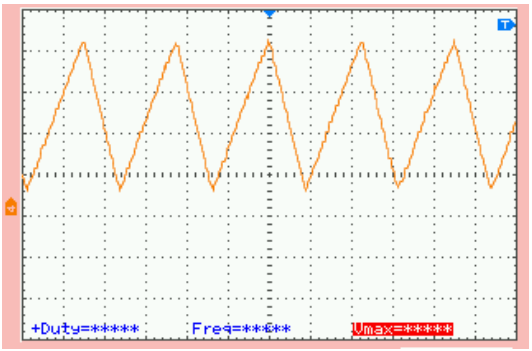
7.7 Experimental Results

The experimental result is shown in Fig. 7-11, which shows the inductor current under period 1, 2, 4 and chaos. The parameter is illustrated as:

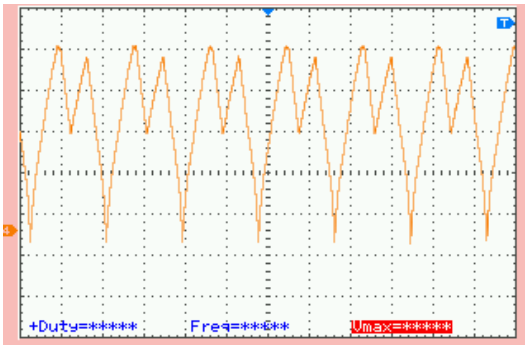
T_S=50μS, U=35V, R=40Ω , C=33μF, and I_{REF}=4A. The inductor is 22μH, 33μH, 47μH, 82μH respectively.

The simulation results as shown in Fig. 7-11 agree with the simulation results as shown in Fig. 7-5 (a).

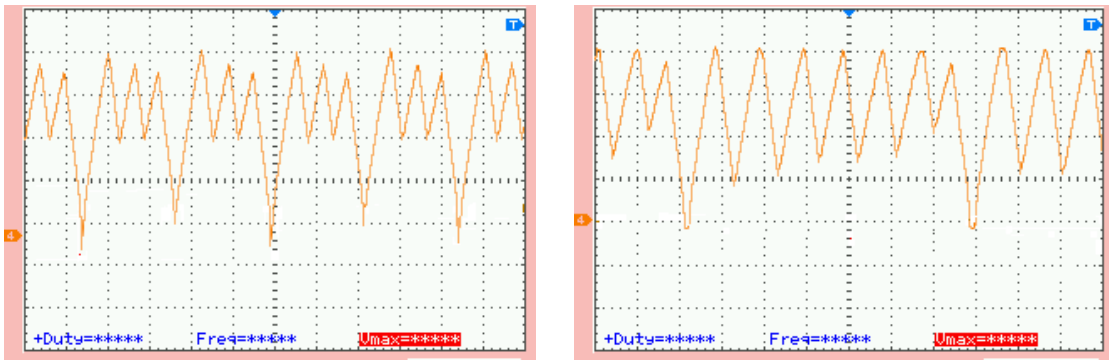
Fig. 7-12 shows the experimental result of boundary for storage energy in inductor versus inductance. It agrees with the simulation result of Fig. 7-9(a).



(a) inductor current under Period 1



(b) inductor current under period 2



(c) inductor current under Period 3 (d) inductor current under Chaos

Fig. 7-11 The inductor current under period 1(a), period 2(b), Period 3(c) and chaos (d) when the inductor is 22μH, 33μH, 47μH, 82μH respectively .

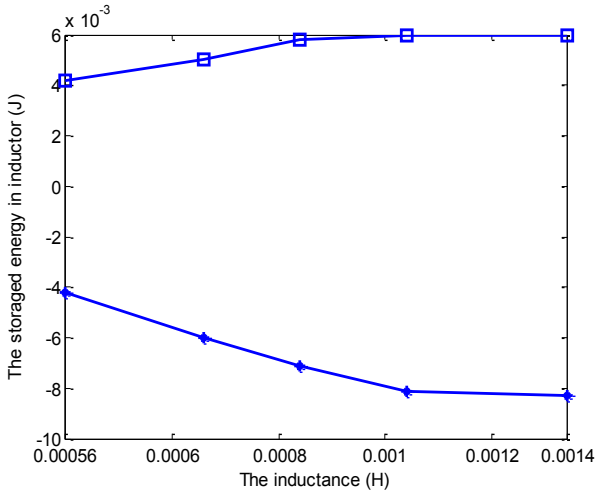


Fig. 7-22 Experimental result of boundary for storage energy in inductor

7.8 The Application of Energy factor theory to resonant SIPC

The double mode resonant SIPC's state equation is shown in chapter 5. The discrete map of the state equation is derived based on equation (5-1) to (5-19) as follows.

The maximum voltage of the capacitor C_1 is

$$v_2 = V_x \tag{7-13}$$

The minimum voltage of the capacitor C_1 is

$$v_1 = 0 \tag{7-14}$$

The minimum current of the inductor L_1 is

$$i_{L1} = I_{in} - \frac{V_x}{Z_0} \tag{7-15}$$

The maximum current of the inductor L_1 is

$$i_{L2} = I_{in} + \frac{V_x}{Z_0} \tag{7-16}$$

7.8.1 Storage Energy for Inductor L_1

To apply the energy factor theory to resonant switched inductor power converter, and based on the definition of equation (7-7), the positive maximum variation of storage energy for the inductor L_1 in one switching cycle of double mode SIPC is:

$$S_{LP} = \frac{1}{2} L((I_{in} + \frac{V_x}{Z_0})^2 - (I_{in} - \frac{V_x}{Z_0})^2) \tag{7-17}$$

The negative maximum variation of storage energy for the inductor L_1 in one switching cycle of double mode SIPC is:

$$S_{LN} = -\frac{1}{2} L((I_{in} + \frac{V_x}{Z_0})^2 - (I_{in} - \frac{V_x}{Z_0})^2) \tag{7-18}$$

The variation of the storage energy for the inductor L_1 in one switching cycle in double mode SIPC is defined as S_{L1}, which can be calculated by $S_{L1} = S_{LP} + S_{LN}$, incorporating equation (7-17) and equation (7-18), then there is

$$S_{L1} = 0 \tag{7-19}$$

7.8.2 Storage Energy for Capacitor C_1

The positive maximum variation of storage energy for the capacitor C_1 in one switching cycle of double mode SIPC is:

$$S_{CP} = \frac{1}{2} C V_x^{\,2} \tag{20}$$

The negative maximum variation of storage energy for the capacitor C_1 in one switching cycle of double mode SIPC is:

$$S_{CN} = -\frac{1}{2} C V_x^{\,2} \tag{7-21}$$

The variation of the storage energy for the capacitor C_1 in one switching cycle in double mode SIPC is defined as S_{C1}, which can be calculated by $S_{C1} = S_{CP} + S_{CN}$, incorporating equation (7-20) and equation (7-21), then there is

$$S_{C1} = 0 \tag{7-22}$$

Based on the energy factor theory, when zero energy appears the circuit will operate in stable period one, this will provide a new method to verify the stability of the resonant SIPC.

7.8 Conclusions

The application of the storage energy in dc converter is newly investigated in this paper with the special consideration of bifurcation and chaos and some interesting phenomenon occurs in the bifurcation diagram when different circuit and operational parameters are studied. Zero energy appears when the circuit operates in stable period

1, which will develop new control algorithm when a stable power electronic system is designed. It presents a new angle to understand the dynamic behavior of the circuit rather than the conventional bifurcation diagram. The maximum storage energy when chaos happened nearly does not vary with the parameters of inductance and capacitance. An estimated equation can be used to formulate storage energy under the boundary of bifurcation. The equation is a single equation that defines the boundary of the stable region and will make circuit design easy rather than going through a timely and tedious simulation.

Chapter 8

Conclusions

In this thesis, various configurations which are adaptable to high frequency AC distribution system have been comprehensively investigated and studied, they are the AC-AC switched capacitor converter, the AC-DC switched capacitor converter and the multilevel AC-DC converter. The research provides theoretical analysis, simulations as well as experimental solutions, which verify the theoretical analysis. The proposed circuits present a solution to the load side power convertion. In this chapter, the main contributions and the limitation of the research are briefly summarized. Furthermore, the potential research areas that extend from the research in this thesis are suggested.

8.1 Main Contributions and limitations

Various configurations in developing AC-AC converters and AC-DC converters for high frequency AC distribution system have been explored and implemented in this thesis. Through the study of high frequency AC-DC network, the number of new topology and analysis has been explored. It then leads to interesting and new topology development. Therefore the main contributions of the research are described

as follows:

Switched-inductor power converter is a duality counter part of the conventional switched–capacitor converter. DC-DC and AC-AC power conversion and the conversion of step up, step down and inversion can be generated by the concept. In this thesis, the AC-AC step up switched–inductor power converter is presented. Bi-directional switches are used to realize the bi-directional power flow. Step down and inversion topology are also presented. Experimental test has confirmed the proposed new concept of power conversion.

A switched capacitor based step down AC-DC power converter with high frequency feed without rectifier and step down structure is proposed and studied in detail in this thesis. The operational principle of the circuits and the design considerations are described. The main advantage of the circuit is that step down voltage can be achieved in the circuit by simply configuring with cascaded stages, which will be much more convenient to modular development and easy for replacement and maintenance. The voltage and current stresses of most components are smaller than conventional converters. Using buffer capacitors to reserve energy, there are no magnetic energy storage elements in the circuits. Weight and size can be further reduced due to high frequency power line operation. Zero current switching is achieved by introducing small resonant inductors. Therefore, high efficiency and power density can be

achieved. The performance of the converter has been demonstrated by an experiment with 50 kHz 50V power source which is emulated by a signal generator and a high frequency amplifier to prove the concept.

An improved version of a bridgeless resonant switched capacitor based AC-DC power converter with high frequency feed is proposed next. The circuit provides cascaded step up and step down voltage in single circuit by step up/down modules. The module consists of capacitors and diodes only which makes integration much more achievable and easy to maintain. The output voltage stages or multi-output voltages can be varied through modular connection. The proposed circuit contains a voltage multiplier in series with a step down converter and a simple integer-fractional ratio for the conversion ratio can be resulted. Resonant inductors are introduced to reduce the current spikes and to achieve zero current switching to enhance power density and efficiency. The performance of the converter is demonstrated by a prototype converter for verification of the theoretical analysis.

Table 8.1 Comparsion of the 3 categray topologies proposed in the thesis

	AC-AC	AC-DC step up/ Down	DC-DC switched inductor up/down
Basic concept	Switched-cap Direct AC-AC conversion；resonant	Cascaded Switched-capacitor module；resonant	switched inductor ； resonant
Input Current harmonics	Low	medium	Low
Capacitor	Low	Low	Low

current harmonics			
Efficiency	High	High	High
High frequency input	Need high speed power devices	Suitable	Suitable
Control circuit	simple	simple	simple
Components	Switches and capacitors	Switches and capacitors	Switches and inductors

To sum up, a family of AC-AC switched capacitor converter configurations are proposed in chapter 2, the experimental solution verified the simulation results. Configurations of AC-DC rectifierless switched capacitor converter is studied in Chapters 3 and 4. The experiment was conducted in each proposed circuit to verify the theoretical analysis and simulation. Chapter 5 and 6 explored the switched-inductor topology that have found applications in the AC-DC converter. The new topology is an extension of the switched-capacitor system. Finally Chapter 7 describes a new stability examination of power converter to finish the whole piece of AC-DC converter study. The proposed converter has the advantage of low current hamonics, high efficiency, simple controller and simple configuration, it is suitable for the load side power conversion for HF PDS.

Since all the power converters are proposed based on switched capacitor power converter, the limit of the SC power converter is also the limit of the proposed power converter, which is fixed conversion ratio, non-adjustable. To overcome the limitation,

control strategies and circuits have to be added in the circuits to obtain the regulation of the output voltage.

The limit also includes the characteristic of semiconductors especially the on-resistance of the transistor and the forward bias voltage of the diode. Because when the circuit works under high order conversion ratio, there will be more switched capacitor cells employed. The conducting loss will be increased. To reduce the total loss of the power converter, low on-resistance transistor and low forward bias voltage diode have to be chosen.

8.2 Future Research

The research plan of the project is concentrated on system, sub-circuit, power qualities and the magnetics development and stability for high frequency AC distribution. In order to tackle the above problems, the following methodologies are proposed:

1） High frequency magnetics

a) Conventional magnetics

Isolation transformers in the load side converters are needed in many designs. The design is not difficult as it is based on the classical high frequency transformer. However, as the AC distribution system is of high frequency and high power. The

performance of available magnetic products for high frequency and high power application will be examined. The study of high efficiency magnetic devices will be conducted as losses may become the main issue in this high power and high frequency application area. To further improve the efficiency of the magnetic devices, a new topology of transformers or parallel-series of transformers should be considered that is suitable for the switched-capacitor type of current condition. The research will also examine the integrated magnetics and leakage field of different magnetic topologies. Finite element design will be used for the study. The circuit topology of parallel and series connection of transformers are part of the study. Examination of the design under different AC bus waveforms will be included.

b) Polymer-bonded magnetics

The new polymer-bonded magnetic material is composed of polymer matrices and special magnetic powders, which will have extremely low eddy current losses during high frequency operation. It has been reported to be very useful for high frequency power conversion and it can form any size and shape easily using simple press machines, and is suitable for the application in this proposed project. The core can be made in factories or laboratories within one day rather than the 4 days for ferrites. The polymer-boned magnetic core can be made integrated with the high frequency rectifier as a module. A new magnetic topology can be developed that will make the

integration easier with consideration of power, geometry and frequency.

2） High frequency AC bus structure

a) The AC bus cable for the high frequency application should be specially and carefully designed. Low-loss low-reactance, good screening characterization cable geometry and structure will be studied and designed.

b) Displacement between the line and neutral, effect of the leakage components to the distribution may be examined and modeled using the finite element method. 1-D and 2-D field analysis could be used for the study. The HF circuit breaker design should be re-designed and the EMI implication of the breaking current can be further explored.

3） High frequency AC-AC converter

The power conversion from 50/60-Hz AC to high frequency AC bus requires an AC-AC power converter and the conversion from HFAC to HFAC needs AC-AC converter. The following investigations are suggested:

a) Waveforms: The study of different types of the HF waveforms including the sine, square and trapezoidal is interesting for further examination. A filter may be added to reduce the harmonics in the AC bus.

b) The classical switched-mode power conversion such as H-bridge version including the phase-shifted, load resonant and phase-shift-resonant can be applied for

voltage conversion and their component sizes can be further reduced. With the emerge of high frequency switching devices such as Silicon Carbide and Gallium Arsenide, the development in this field will be very promising. The associated high frequency power conversion should be further re-visited to upgrade and create topologies for such work.

4) A switched capacitor rectifier with multilevel voltage output for high frequency AC distribution. Multilevel converter has provided an effective solution of energy conversion. In high frequency distribution system, energy is processing faster and more effective. Multilevel converter provides a reliable and efficiency solution to the energy conversion. In future study, a simple switched capacitor based with an independent energy balancing system is proposed, which has lower current distortion, high reliability and simple controller. The aim is to use multi-level based switching in order not to use conventional boost converter type PFC that is too high frequency for HFAC. The multi-level provides a better control of the AC side current and the THD and power factor can be improved with lower switching frequency.

5) Study of nonlinear dynamics and chaos in the HFAC power conversion. Nonlinear is an older and broader field in power electronics. It is used as a technique to analyze the power electronics circuit. Energy factor has been used to study the stability of the conventional SMPC in Chapter 7. It will be extended to study the stability and energy

storage formulation of the switched capacitor power converter in further research.

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