SYSTEMATIC STUDY OF A NEW FAMILY OF SWITCHED-RESISTOR-CIRCUIT-BASED RIPPLE ESTIMATION/CANCELLATION METHODS FOR FAST-RESPONSE PFC PRE-REGULATOR

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Systematic Study of a New Family of Switched-Resistor-Circuit-Based Ripple Estimation/Cancellation Methods for Fast-Response PFC Pre-regulator

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Abstract

Power Factor Correction (PFC) pre-regulator has been widely used for converting ac power into dc power for the consumption of mains-connected dc loads while limiting the amount of current harmonics being injected to the mains. Typically, its control circuitry consists of an inner current control loop and an outer voltage control loop. The bandwidth of the inner current control loop is typically configured to be large, which causes the input current of PFC pre-regulator to closely track the reference signal generated by the outer voltage loop. For the outer voltage loop, which regulates the average output voltage of PFC pre-regulator, a narrow bandwidth is commonly utilized in order to significantly attenuate the sampled double-line frequency component. Such a two-loop configuration leads to high power factor and input current with extremely low THD. However, the resultant narrow bandwidth also gives rise to poor dynamic response of PFC pre-regulator.

Various methods have been proposed to achieve high power factor and fast dynamic response simultaneously. One of the well-developed strategies is the ripple cancellation approach. The main idea of this approach is that the double-line frequency component that exists in the sampled output voltage is eliminated by subtracting a replica of the sampled output voltage ripple from the actual one to generate a ripple-free signal to be further processed by the voltage error amplifier. As a result, an undistorted and sinusoidal input current can be obtained even if the bandwidth of the voltage error amplifier is increased considerably

compared to conventional design.

By comparing the graphical representation of the actual PFC pre-regulator's output voltage with that of the idealized output voltage's equation, it is shown that the output voltage ripple does not match the description of the idealized equation when a PFC pre-regulator operates outside certain range of operating conditions. In view of this, a new ripple estimation network consisting of an amplitude tuner and a phase shifter is proposed for generating an ideal replica of the sampled output voltage ripple. The proposed amplitude tuner and phase shifter are derived from switched-resistor circuits with adjustable gain and phase angle realized by controlling the duty cycle of the switched-resistor circuits. The proposed ripple estimation network is tested by implementing it on a boost PFC pre-regulator. It is shown that the proposed ripple estimation network provides an accurate ripple estimation/cancellation over a wide range of operating conditions, thus producing minimum global cancellation error, and consistently gives rise to near-unity power factor and fast dynamic response of PFC pre-regulator under these conditions.

Considering the complexity of the precise ripple estimation network proposed above, its circuitry is simplified as inferred from the main figures of merit of PFC pre-regulator under the action of ripple cancellation. Another ripple estimation method is suggested to minimize the local (instead of global) cancellation error, which is derived and found to be a function of the phase difference between the sampled and the estimated output voltage ripple signal. The simplified ripple estimation network is verified experimentally on a boost PFC pre-regulator. It is demonstrated that under this method the estimated output voltage ripple is consistently operated at its optimum amplitude that gives rise to the minimum local cancellation error in the presence of phase estimation error. This method also results in high power factor and low THD of PFC pre-regulator's input current.

Finally, the last and the simplest ripple estimation method is developed by simply equalizing the amplitudes of the sampled and estimated output voltage ripples and imposing a constant phase angle to the estimated signal. The performances of these three proposed ripple estimation/cancellation methods are investigated and compared by implementing them on the same boost PFC pre-regulator power stage. By comparing the experimentally measured figures of merit, it is shown that the first method provides the most precise ripple estimation/cancellation which leads to near-unity power factor over a wide range of operating conditions, while the simplest method provides an economical solution for achieving high (but not unity) power factor and fast dynamic response of PFC pre-regulator.

Publications

Journal papers

- **K. H. Leung**, K. H. Loo, Y. M. Lai, "Unity-Power-Factor Control Based on Precise Ripple Cancellation for Fast-Response PFC Preregulator," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 3324-3337, 2016.

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Chapter 1

Introduction

1.1 Introduction

Power factor correction (PFC) pre-regulators have been increasingly used for limiting the level of harmonic currents injected into the mains power line, and converting ac power into dc power for mains-connected dc loads. In order to regulate the amount of harmonic currents injected by mains-connected non-linear loads, there are different kinds of international standards, such as EN 61000-3-2 [1] and IEEE STD 519-1992 [2], which specify the limitations on the harmonic content of the line current being drawn from the mains. To conform with these industry standards, PFC pre-regulators have become indispensable as the interfacing converter between the mains and the loads. Although PFC pre-regulators are very effective in controlling the harmonic content of line current, its dynamic response is typically sluggish since their bandwidths are typically designed to be small in order to achieve high power factor and fulfill the requirements outlined in international standards.

In this chapter, the basic concepts of power factor and total harmonic distortion are briefly reviewed, and subsequently the requirements of the international standards related to the regulation of harmonic current content are given.

Subsequently, the basic operation of a typical PFC pre-regulator with average current-mode control is analyzed, and the trade-off between power factor and dynamic performance of PFC pre-regulator is demonstrated by means of simulation results. Finally, the objectives of this research work are outlined.

1.2 Power Factor and Total Harmonic Distortion

The power factor (PF) of an ac circuit is defined as the ratio between the real power delivered to the load and the apparent power delivered to the circuit, as expressed by Eq. (1.1). Real power, P_{avg}, in turn, is defined as the average value of the product of instantaneous input voltage $v_{in}(t)$ and instantaneous input current $i_{in}(t)$ over an ac period T, whereas apparent power is defined as the product of the root-mean-square (rms) values of the input voltage V_{irms} and input current I_{irms}.

$$PF = \frac{\text{Real power}}{\text{Apparent power}} \tag{1.1}$$

$$P_{avg} = \frac{1}{T}\int_0^T v_{in}(t) i_{in}(t) dt \tag{1.2}$$

$$V_{irms} = \sqrt{\frac{1}{T}\int_0^T v_{in}^2(t) dt} \tag{1.3}$$

$$I_{irms} = \sqrt{\frac{1}{T}\int_0^T i_{in}^2(t) dt} \tag{1.4}$$

For a mains-connected system, the input voltage $v_{in}(t)$ is the same as the mains voltage, which is ideally a pure sinusoidal voltage given by the following form.

$$v_{in}(t) = \sqrt{2} V_1 \sin(\omega_{line} t) \tag{1.5}$$

where V_1 and ω_{line} is the rms value and the angular frequency of the line voltage,

respectively.

The input current $i_{in}(t)$, on the other hand, has a waveform that depends on the characteristic of the load connected to the mains, therefore it is assumed to comprise of the fundamental and harmonic components. As a result, the input current can be expressed by the following general form.

$$\begin{aligned} i_{in}(t) &= \sqrt{2}I_1 \sin(\omega_{line}t + \delta_1) + \sqrt{2}I_2 \sin(2\omega_{line}t + \delta_2) \\ &+ \sqrt{2}I_3 \sin(3\omega_{line}t + \delta_3) + ... \end{aligned} \tag{1.6}$$

where I_1, I_2, I_3, ... are the rms values of the fundamental (I_1) and harmonic components (I_2, I_3, ...), and δ_1, δ_2, δ_3, ... are the corresponding phase shifts relative to the input voltage $v_{in}(t)$.

From Eq. (1.2)–Eq. (1.4), the real power, rms value of the input voltage and input current can be calculated as Eq. (1.7), Eq. (1.8), and Eq. (1.9), respectively.

$$P_{avg} = V_1 I_1 \cos\delta_1 \tag{1.7}$$

$$V_{rms} = V_1 \tag{1.8}$$

$$\begin{aligned} I_{rms} &= \sqrt{I_1^2 + I_2^2 + I_3^2 + ...} \\ &= I_1\sqrt{1 + \left(\frac{I_2}{I_1}\right)^2 + \left(\frac{I_3}{I_1}\right)^2 + ...} \end{aligned} \tag{1.9}$$

By substituting Eq. (1.7)–Eq. (1.9) into Eq. (1.1), the resultant power factor (PF) is given by Eq. (1.10).

$$PF = \frac{V_1 I_1 \cos\delta_1}{V_1 I_1\sqrt{1 + \left(\frac{I_2}{I_1}\right)^2 + \left(\frac{I_3}{I_1}\right)^2 + ...}} = \frac{\cos\delta_1}{\sqrt{1 + \left(\frac{I_2}{I_1}\right)^2 + \left(\frac{I_3}{I_1}\right)^2 + ...}} \tag{1.10}$$

Another important parameter for measuring input current's quality is the total harmonic distortion (THD) of the current, which is defined as the ratio between the root-sum-square of the rms values of the higher harmonic components (I_i, $i \geqslant 2$) and the rms value of the fundamental component. Mathematically, it can be expressed as

$$THD = \frac{\sqrt{I_2^2 + I_3^2 + ...}}{I_1} = \sqrt{\left(\frac{I_2}{I_1}\right)^2 + \left(\frac{I_3}{I_1}\right)^2 + ...} \tag{1.11}$$

By substituting Eq. (1.11) into Eq. (1.10), the definition of power factor (PF) can be rewritten as

$$PF = (\cos \delta_1) \cdot \frac{1}{\sqrt{1 + THD^2}} \tag{1.12}$$

From Eq. (1.12), it can be seen that the value of power factor depends on two variables, one being the phase difference between the input voltage and the fundamental component of the input current δ_1, and the other being the total harmonic distortion (THD) of the input current. In order to attain a unity power factor, i.e. $PF = 1$, the values of both δ_1 and THD should be minimized, i.e. $\delta_1 = 0$ and THD $= 0$. In fact, these two requirements can be fulfilled by means of interfacing power loads to the mains terminal using power-factor-correction (PFC) pre-regulators, as will be discussed later.

1.3 International Regulations and Standards

In this section, the content of some international standards focusing on limiting the harmonic content of the input current of mains-connected devices will be briefly reviewed. Power electronics engineers are required to design power converters that fulfill these regulations and standards. For universal 50/60 Hz applications, the most popular international standards concerning the regulation of input current's harmonic content and, hence, power factor of mains-connected

devices are EN 61000-3-2 [1] and IEEE STD 519-1992 [2].

1.3.1 EN 61000-3-2

The European standard EN 61000-3-2 is applicable to the electrical and electronic equipments having an input current up to 16 A per phase, and which are intended to be connected to the low-voltage ac mains [1]. Under this standard, electronic equipments are classified into four different classes with each class having specific limitations on harmonic current content. The criteria for classification are given below, and the harmonic current limits for different classes of equipments are listed in Table (1.1), Table (1.2) and Table (1.3).

- **Class A** – All other equipments.
- **Class B** – Portable equipments; arc welding equipments that is not professional equipment.
- **Class C** – Lighting equipments.
- **Class D** – Computers, monitors, radio, and television receivers with input power ranging from 75 W to 600 W.

Table 1.1: Maximum permissible harmonic current content for Class A and Class B equipments.

	Class A	**Class B**
Harmonic order	Maximum permissible harmonic current	
n	A	
Odd harmonic		
3	2.3	3.45
5	1.4	1.71
7	0.77	1.155
9	0.40	0.60
11	0.33	0.495
13	0.21	0.315
$15 \leq n \leq 39$	$0.15 \times 8/n$	$0.225 \times 8/n$
Even harmonic		
2	1.08	1.62
4	0.43	0.645
6	0.30	0.45
$8 \leq n \leq 40$	$0.23 \times 8/n$	$0.345 \times 8/n$

Table 1.2: Maximum permissible harmonic current content for Class C equipments.

Harmonic order	Maximum permissible harmonic current % of the input current at the fundamental frequency
n	%
Odd harmonic	
3	$30 \times \lambda$
5	10
7	7
9	5
$11 \leq n \leq 39$ (odd harmonics only)	3
Even harmonic	
2	2

Note: λ is the circuit power factor.

Table 1.3: Maximum permissible on harmonic current content for Class D equipments.

Harmonic order n	Maximum permissible harmonic current per watt mA/W	Maximum permissible harmonic current A
Odd harmonic		
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
$13 \leq n \leq 39$ (odd harmonics only)	$3.85/n$	$0.23 \times 8/n$

1.3.2 IEEE STD 519-1992 Standard

Besides the European standard EN 61000-3-2, IEEE STD 519-1992, published by the Institute of Electrical and Electronics Engineers (IEEE), specifies some recommendations and requirements on controlling the level of harmonic current injected into the utility system [2]. Table (1.4) shows the harmonic current limits stated in IEEE STD 519-1992. Under this standard, the maximum permissible harmonic current distortion is classified based on the ratio between the maximum short-circuit current I_{sc} and the maximum demanded load current (fundamental frequency component) I_L at the point of common coupling (PCC).

Table 1.4: Harmonic current distortion limits for general distribution systems (120 V through 69000 V) specified by IEEE STD 519-1992.

Maximum Harmonic Current Distortion in Percent of I_L						
	Individual Harmonic Order (Odd Harmonics), n					
I_{sc}/I_L, %	< 11	$11 \leq n < 17$	$17 \leq n < 23$	$23 \leq n < 35$	$35 \leq n$	TDD
< 20	4.0	2.0	1.5	0.6	0.3	5.0
20-50	7.0	3.5	2.5	1.0	0.5	8.0
50-100	10.0	4.5	4.0	1.5	0.7	12.0
100-1000	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0

Note: TDD = Total demand distortion.

1.4 Basic Operation of PFC Pre-regulator

To comply with the above regulations or standards, the use of power-factor-correction (PFC) pre-regulators are popular due to their capability to control input current waveform and provide output voltage regulation [3], [4]. By using appropriate control circuitry, the input current of PFC pre-regulator can be regulated to be sinusoidal and in phase with the mains line voltage. As a result, the total harmonic distortion of the input current can be significantly reduced, thus giving rise to high power factor, hence the name power factor correction.

1.4.1 Power Stage of PFC Pre-regulator

Three fundamental non-isolated switch-mode power supply topologies – buck, boost and buck-boost converter – are commonly chosen to realize power-factor correction [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21], [22], [23]. However, by comparing their characteristics, it is found that boost converter is particularly suitable for this function [24], [25], [26], especially for medium-to-high power applications, since it offers a direct control of the converter's input current by controlling the inductor current [27], [28], [29], [30]. On

the contrary, for buck and buck-boost converter, their input current is characterized by higher level of EMI due to its discontinuous/pulsating nature, which results in higher total harmonic current distortion and lower power factor. Therefore, in the following sections, discussions will be mainly focused on boost-derived PFC pre-regulators.

1.4.2 Standard Control Strategy for PFC Pre-regulator

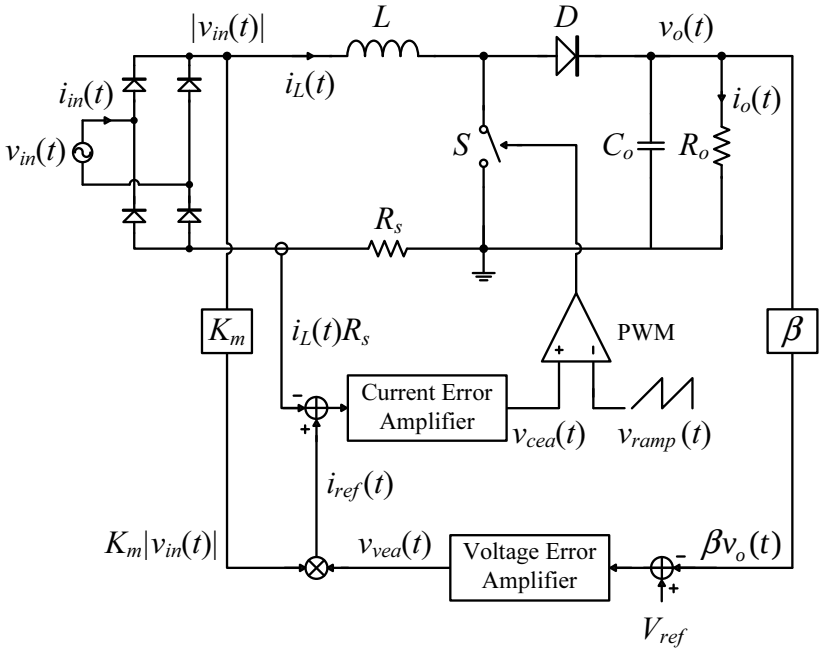


Figure 1.1: Configuration of standard boost PFC pre-regulator with ACM control.

Average current mode (ACM) control has been widely used in medium-to-high power PFC pre-regulator due to the resulting low level of THD generated. Fig. 1.1 shows the standard configuration of a boost PFC pre-regulator under ACM control [31], [32], [33]. Its control circuitry consists of two feedback loops, one inner current control loop and one outer voltage control loop. The inner current loop is typically designed to have a large bandwidth so that the inductor current is controlled to closely track the reference current signal $i_{ref}(t)$, which is generated by multiplying the rectified input voltage $K_m\,|v_{in}(t)|$ by the output signal of the

voltage error amplifier $v_{vea}(t)$. Since the sampled input voltage is purely sinusoidal, the only factor that can affect the inductor current waveform, and hence, the PFC pre-regulator's input current waveform and power factor, is the output signal of the voltage error amplifier. The outer voltage control loop is responsible for regulating the PFC pre-regulator's output voltage by comparing the sampled output voltage $\beta v_o(t)$ to the reference voltage V_{ref}, and the resulting error voltage is amplified by the voltage error amplifier. In practice, due to the pulsating nature of the PFC pre-regulator's input power, low-frequency voltage ripple at double-line frequency will be constantly present in the PFC pre-regulator's output voltage. If the double-line frequency component is not sufficiently attenuated by the voltage error amplifier, a significant portion of it will exist at the output of the voltage error amplifier. As a result, the reference current waveform $i_{ref}(t)$ will be significantly distorted due to the presence of higher harmonic components resulting from the multiplication of two time-varying waveforms, $K_m \left|v_{in}(t)\right|$ and $v_{vea}(t)$, and the power factor will be degraded.

In order to maintain a near-unity power factor, the crossover frequency of the PFC pre-regulator's loop gain is typically limited to 1/10 to 1/5 of the double-line frequency (between 10 Hz and 20 Hz) in order to provide a sufficient attenuation of the double-line frequency component [34], [35], [36]. When this condition is met, the output voltage of the voltage error amplifier will be approximately constant, hence the current reference signal and the PFC pre-regulator's input current will be approximately sinusoidal. The main drawback in limiting the unity-gain frequency of the loop-gain function to low value is, however, the resulting poor dynamic response of the PFC pre-regulator.

1.5 Trade-off between Power Factor and Dynamic Performance of PFC Pre-regulator

To demonstrate the effects of unity-gain frequency of the loop-gain function on the input current waveform and dynamic response of PFC pre-regulator, an ACM-controlled boost PFC pre-regulator is simulated in PSIM and the simulation results are shown in Fig. 1.2 (for step load decrease from 100% to 50%) and Fig. 1.3 (for step load increase from 50% to 100%). The PFC pre-regulator is simulated with an input voltage of 110 V_{rms}/60 Hz, nominal output voltage of 400 V, and nominal load resistance of 800 Ω. The value of the inductor L and output capacitor C_o are chosen to be 1 mH and 16 μF, respectively.

Fig. 1.2 shows the input current and output voltage waveforms of the PFC pre-regulator under a step load decrease from 100% to 50%. For Fig. 1.2(a) and Fig. 1.2(b), the unity-gain frequency of the PFC pre-regulator's loop-gain function is designed to have a small value of 10 Hz, whereas for Fig. 1.2(c) and Fig. 1.2(d), it is designed to have a larger value of 60 Hz. It can be seen from Fig. 1.2(a) that the input current is approximately sinusoidal with a measured PF of 0.993 when the unity-gain frequency of the loop-gain function is low, while it is significantly distorted with measured PF of 0.93 when the crossover frequency is increased, as shown in Fig. 1.2(c). However, by comparing the simulated output voltage waveform shown in Fig. 1.2(b) and in Fig. 1.2(d), a lower unity-gain frequency of the loop-gain function is seen to cause a larger overshoot in output voltage with a longer settling time, which constitutes the main drawbacks of this control strategy since some components will have to withstand high voltage stress during transient state.

In addition, the PFC pre-regulator is also simulated under the condition of a step load increase from 50% to 100%, and the results are shown in Fig. 1.3.

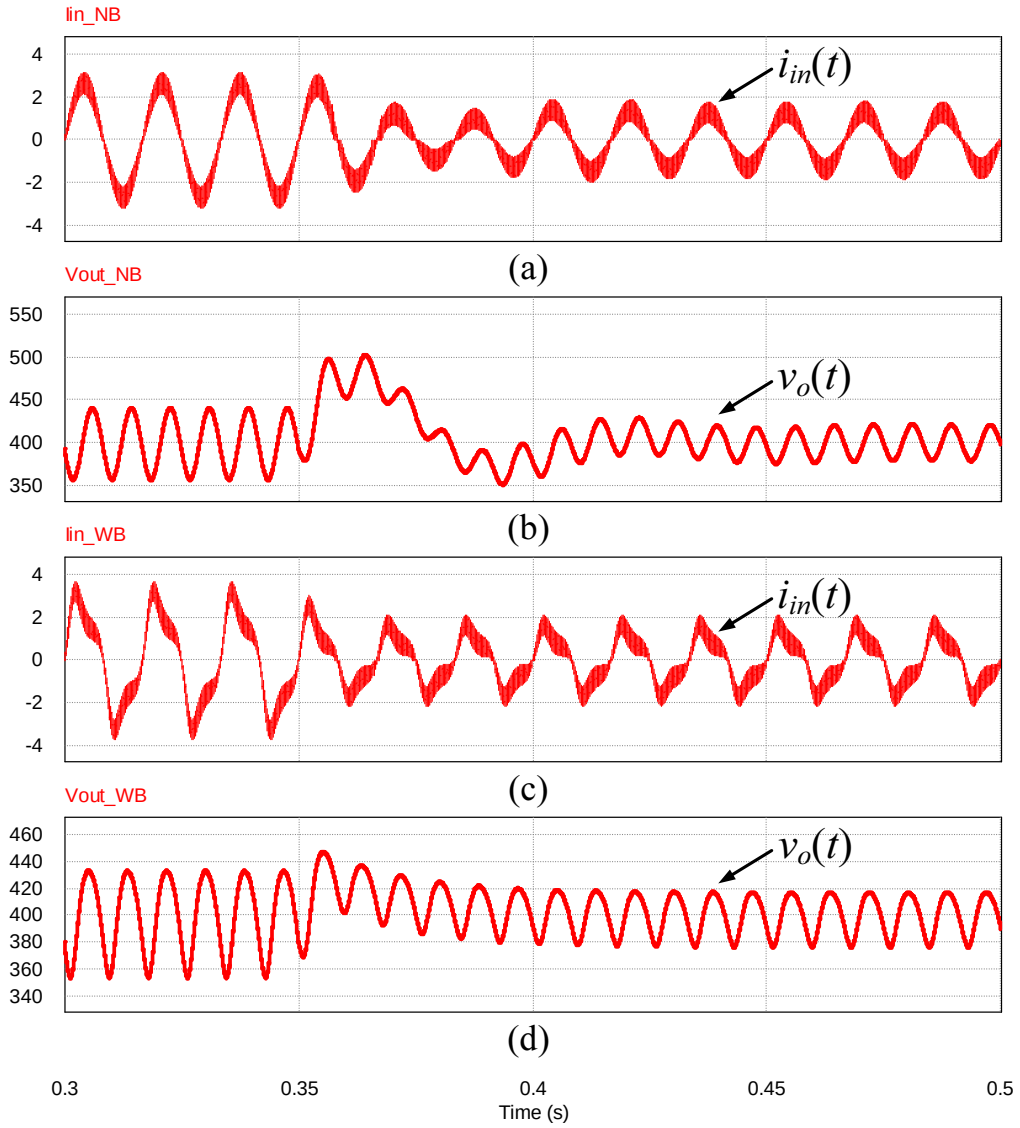


Figure 1.2: Input current and output voltage of boost PFC pre-regulator with narrow bandwidth [(a) and (b)] and wide bandwidth [(c) and (d)] under step load decrease, from 100% to 50%.

A similar effect of reduced unity-gain frequency of the loop-gain function on the dynamic response of the PFC pre-regulator's output voltage can be observed, that is, it results in a larger undershoot with a longer settling time. Thus, from these simulation results, it can be concluded that there is a performance trade-off between the power factor and dynamic response of PFC pre-regulator.

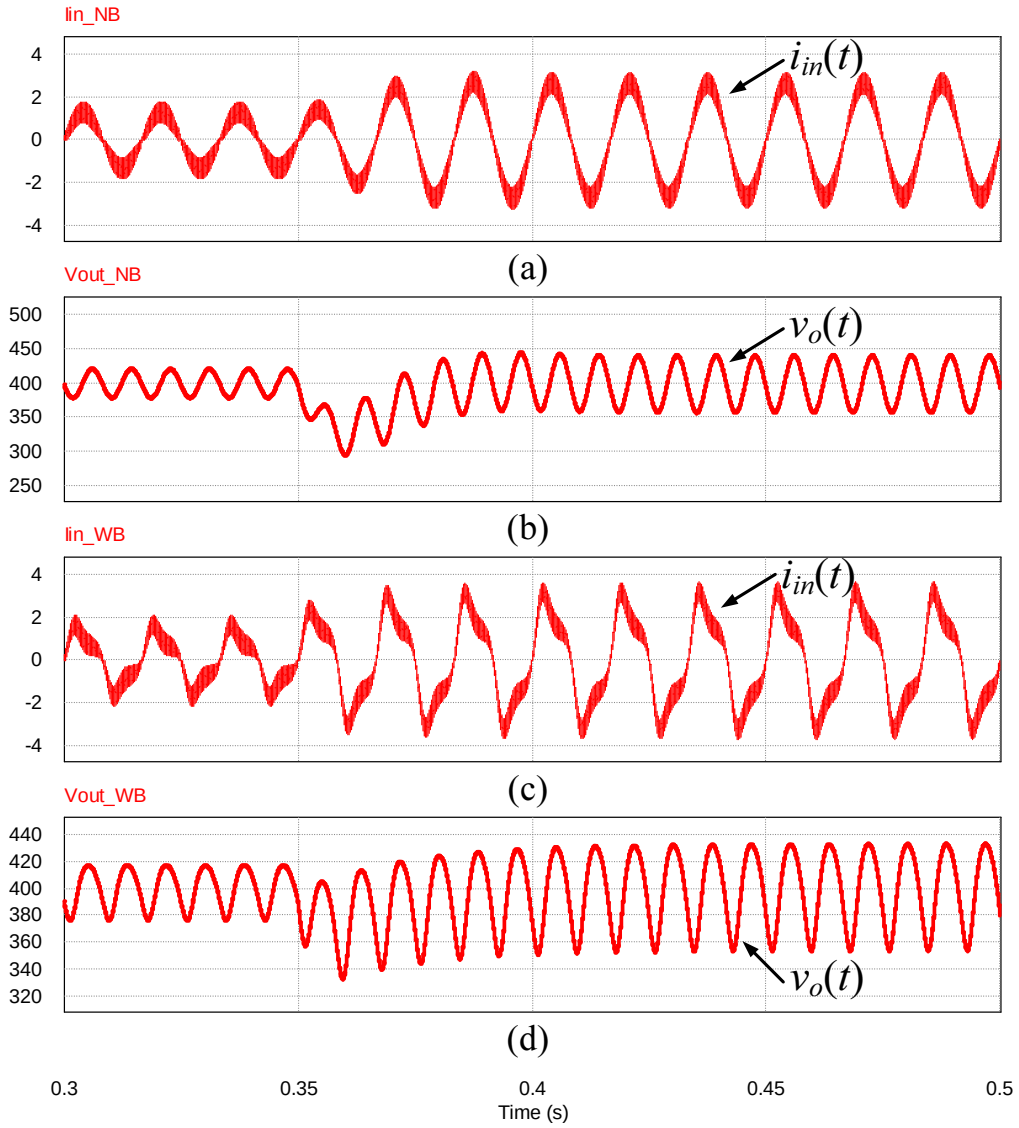


Figure 1.3: Input current and output voltage of the boost PFC pre-regulator with narrow bandwidth [(a) and (b)] and wide bandwidth [(c) and (d)] under step load increase, from 50% to 100%.

1.6 PFC Pre-regulator with High Power Factor and Fast Dynamic Response: A Literature Survey

Many researchers have proposed various control strategies, both analog and digital implementations, to achieve a near-unity power factor without sacrificing

the dynamic response of PFC pre-regulator. In this section, we will explore these prior works and make a comparison between them, and reveal their respective advantages and disadvantages.

1.6.1 Two-Stage Solution

As discussed, conventional PFC pre-regulator usually suffers from the problem of slow dynamic response. Attempting to improve the dynamic response unavoidably leads to degradation in power factor, and vice versa. In order to satisfy both power factor and dynamic response requirements, it is suggested that a dc-dc converter having fast dynamic response is cascaded with the slow-responding PFC pre-regulator [37], [38]. A block diagram showing the two-stage solution is depicted in Fig. 1.4. The first stage is an ACM-controlled boost PFC pre-regulator that is designed to shape a sinusoidal input current for attaining a high power factor, while the second stage is a large-bandwidth dc-dc converter. By designing the bandwidth of the second-stage dc-dc converter to be large, a tight regulation of the output voltage can be achieved. However, it is well known that the cost incurred by this approach is high and the overall efficiency is low, approximately 80% [39], [40], since the power delivered to the load is processed twice [41], and the number of switching components is higher, which results in a higher switching loss. Therefore, two-stage solution generally suffers from high cost and low efficiency, making it unsuitable for low-power applications.

To compensate for these disadvantages, researchers had proposed a number of single-stage isolated power-factor correctors power supplies (S^2IP^2), with the aim of combining the two converters involved in two-stage solution into a new, single-stage converter [42]. By appropriately repositioning the active switches of the two cascaded converters and, subsequently, sharing a single switch, the switching loss can be considerably reduced. Two S^2IP^2 topologies are depicted

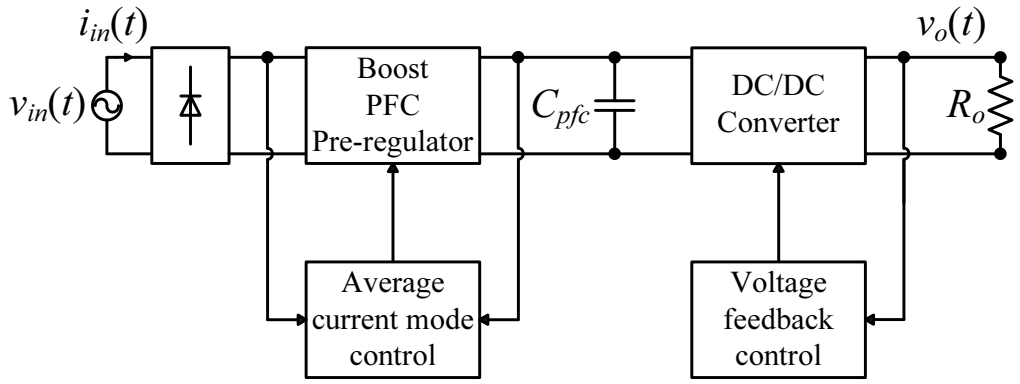


Figure 1.4: Configuration of two-stage solution.

in Fig. 1.5 [43], [44], [45]. The common drawback of S^2IP^2 is that a high voltage stress maybe imposed on the dc-link capacitor (C_1 indicated in both Fig. 1.5(a) and Fig. 1.5(b)) and the adjacent components. This may lead to the use of devices with high voltage rating and, subsequently, reduction in converter's efficiency. Since the voltage applied on the dc-link capacitor is a function of the switching frequency, variable frequency control has been suggested in order to keep the voltage stress of the dc-link capacitor low [46]. However, the additional control circuit, which varies the switching frequency according to the dc-link capacitor's voltage, increases the complexity of the feedback controller. On the other hand, since it is difficult to regulate both input current waveform and output voltage simultaneously by controlling a single switch, it has been proposed that the input stage (PFC) (usually implemented by boost or buck-boost converter) is operated in discontinuous-conduction mode (DCM) for natural power factor correction. However, DCM operation mode is not suitable for medium- to high-power applications due to the presence of high peak input current and associated high copper and core losses.

1.6.2 Sliding-Mode Control

Sliding-mode (SM) control, a non-linear control method applied to variable structure systems, is often employed to control dc-dc converter due to its su-

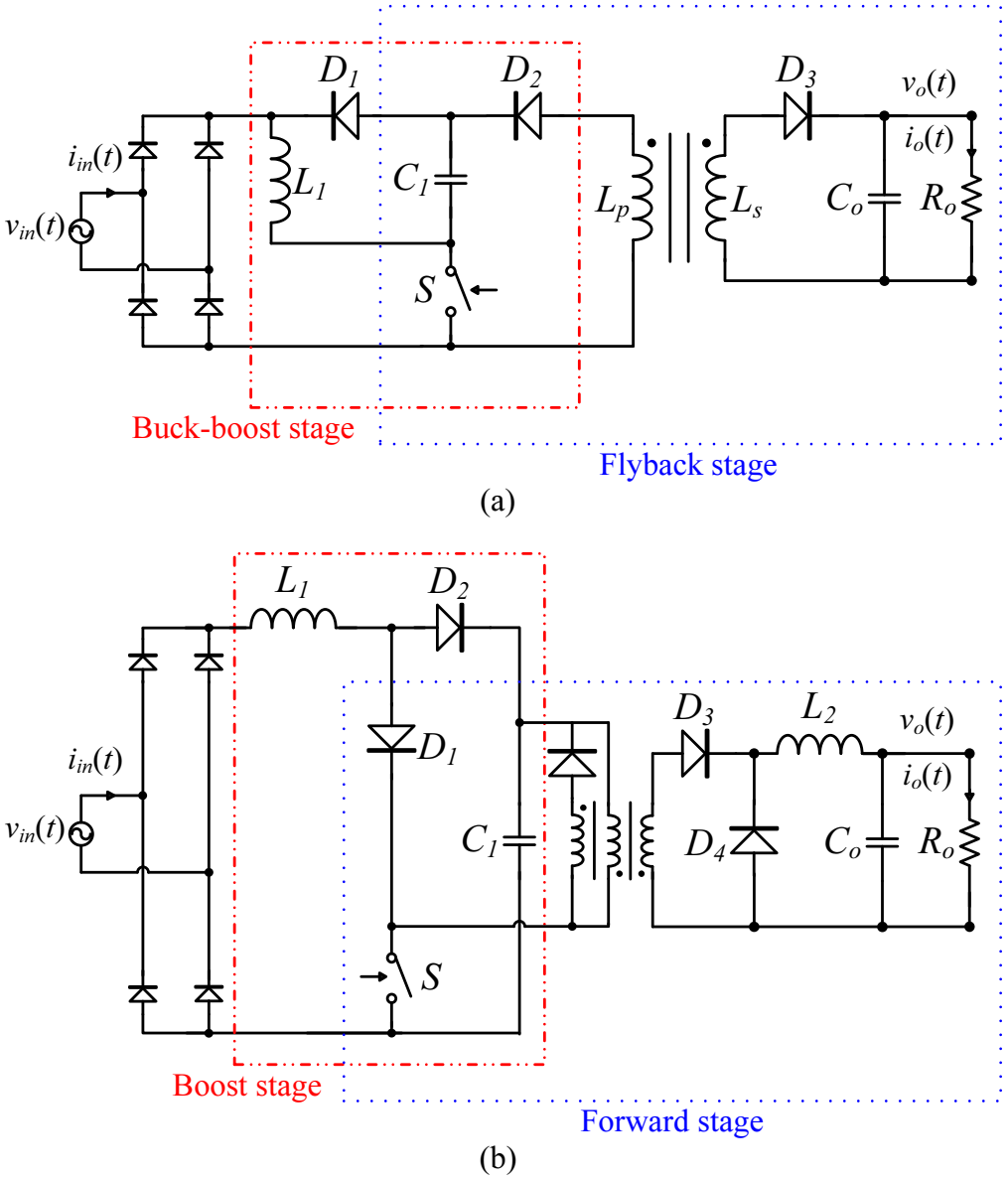


Figure 1.5: Examples of S^2IP^2 topologies. (a) buck-boost PFC + flyback regulator proposed by Wu *et al.* [43], (b) boost PFC + forward regulator proposed by Lee *et al.* [44] and Siu *et al.* [45].

perior stability and robustness against uncertain parameters [47], [48]. In [49], the authors applied SM control based on hysteresis-modulation for improving the dynamic response of PFC pre-regulator. A simplified block diagram of SM-controlled PFC pre-regulator is shown in Fig. 1.6. The major difference between SM control and conventional ACM control is that the voltage error signal is amplified and added to the current error signal to form a sliding function ψ. The

sliding function is passed as input to a hysteretic block which is responsible for generating the switching signal that causes the resultant value of the sliding function ψ to equal zero.

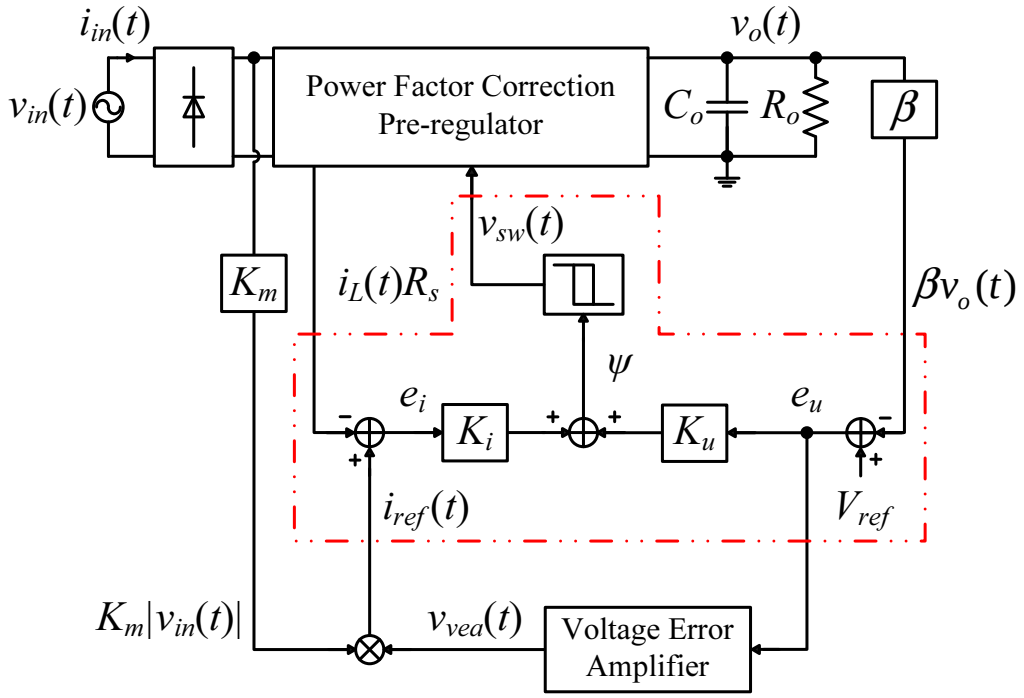


Figure 1.6: Configuration of sliding-mode control scheme for achieving both high power factor and fast dynamic response.

It is reported in the literature that the dynamic performance of the output voltage of PFC pre-regulator can be further improved if the ratio between K_u and K_i (as indicated in Fig. 1.6) is made high, or, in other words, when the voltage error term dominates the sliding function ψ. The only benefit of doing so is, however, that the overshoot/undershoot of the PFC pre-regulator's output voltage is reduced during transient state. The settling time still depends on the design of the outer voltage loop and the input current waveform will be distorted.

1.6.3 Boundary Control

Besides sliding-mode control, boundary control which utilizes a second-order switching surface is another non-linear control scheme used to achieve both sinu-

soidal input current and fast dynamic response in PFC pre-regulator [50], [51]. With this control scheme, the relationship between state variables (i.e. i_L, v_o) is first derived and plotted on state-space plane in order to identify the target operating trajectory of the converter. Fig. 1.7 shows the target operating trajectory of a boost PFC pre-regulator, discussed in [51]. Having known the target trajectory, the PFC pre-regulator's switch is controlled in such a way that the instantaneous values of the state variables are varying along the target operating trajectory. Whenever there is a step load change, a new trajectory is formed and the state variables are controlled to follow the new trajectory. In this way, the converter can reach the new steady state within one to two switching cycles. Since PFC pre-regulator usually operates from the mains voltage which has a frequency that is much smaller than the switching frequency, it will take less than one line cycle to reach the new steady state. Although this control scheme exhibits an extremely fast dynamic response, it requires a large amount of computational power for analyzing complex system equations, and some calibration processes are needed to compensate for the variances in the converter's components.

1.6.4 Regulation-Band Approach

Regulation-band approach is another control scheme devised for achieving sinusoidal input current and fast dynamic response in PFC pre-regulator. Rathi *et al.* [52] proposed a circuitry, shown in Fig. 1.8, that realizes the regulation band approach. It is a control strategy that switches between a slow and a fast voltage control loop for meeting different control objectives. The slow voltage control loop is employed in steady state to limit the total harmonic distortion of input current and maintain a high power factor, while the fast voltage control loop is used in transient state to achieve a fast dynamic response. The main challenge of this technique is, however, the synchronization between the switching time of the

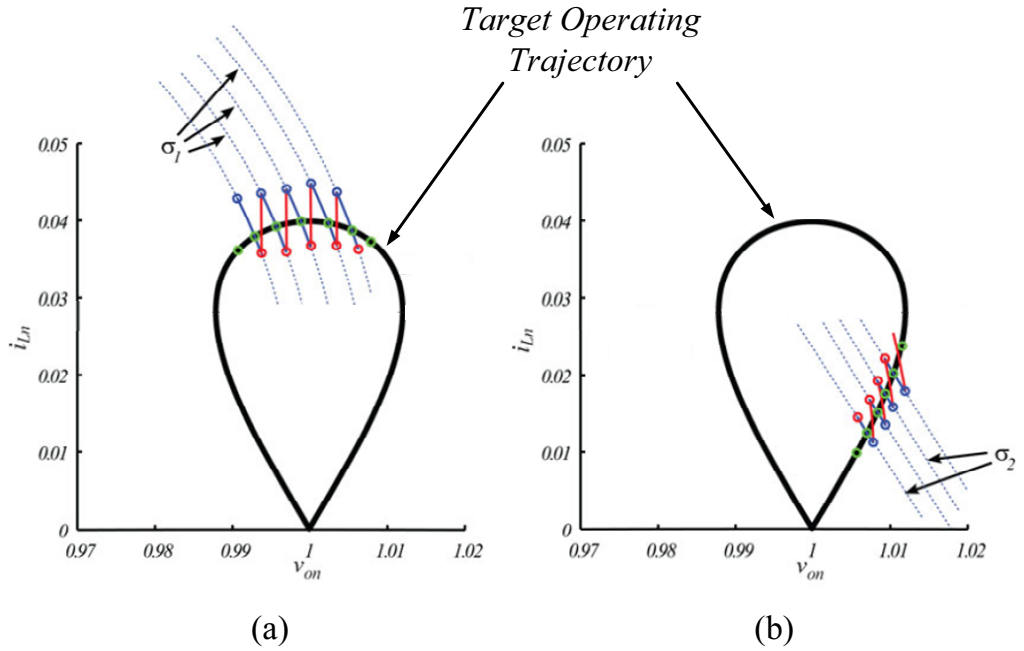


Figure 1.7: Conceptual evolution of the actual and target operating trajectories of a boost-derived PFC pre-regulator, in normalized state-variable plane.

controllers and the line frequency. Similarly, in the work of Nasirian *et al.* [53], it is found that the conversion ratio of the selected converter topology is a function of both switching frequency and duty ratio, thus, the converter's output voltage can be regulated in transient state using a fast control loop associated with switching frequency variation and in steady state using a slow control loop associated with duty cycle variation. However, the main difficulty is the requirement of costly sensing components with high measurement accuracy and speed.

1.6.5 Notch-Filter Approach

The cascading of notch filter in series with the voltage error amplifier is a control strategy that is aimed at eliminating the sampled output voltage ripple before it is processed by the voltage error amplifier. Due to the imbalance between the instantaneous input power and the average output power, the output voltage of PFC pre-regulator constantly contains double-line-frequency voltage ripple. If a notch filter is designed to have its band-stop frequency coinciding with the

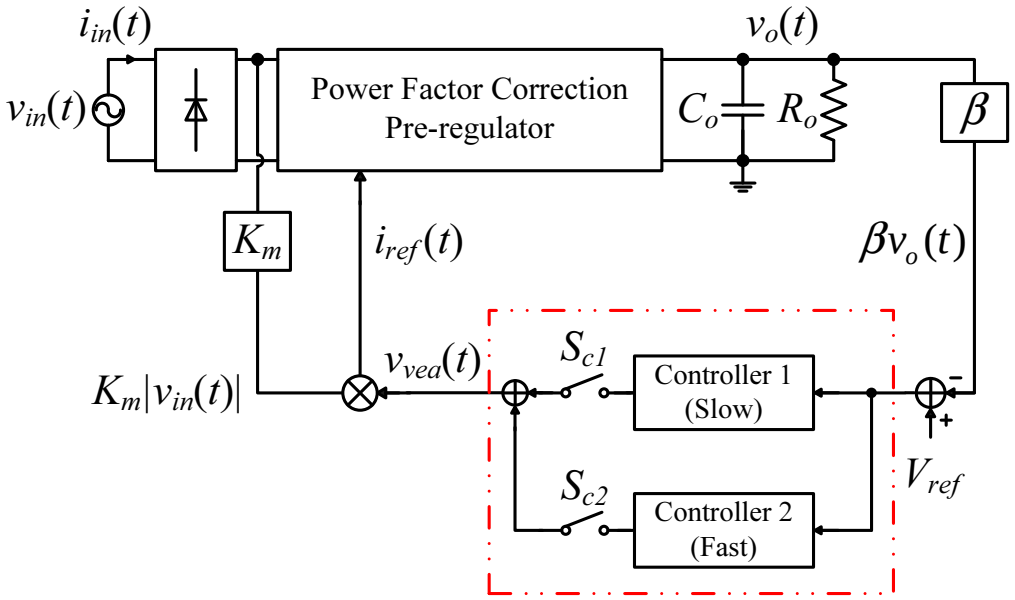


Figure 1.8: Configuration of regulation-band approach in PFC pre-regulator.

double-line frequency, the sampled output voltage ripple can be significantly attenuated before it is processed by the voltage error amplifier. When the voltage error amplifier's input signal is ripple free, its voltage gain can be increased (for improving the PFC pre-regulator's dynamic response) while its output signal remains ripple free. Therefore, a sinusoidal inductor current reference signal and input current waveform can be obtained. In general, the transfer function of the notch filter is given by

$$H_{notch}(s) = \frac{s^2 + {\omega_{notch}}^2}{s^2 + s\frac{\omega_{notch}}{Q} + {\omega_{notch}}^2} \tag{1.13}$$

where ω_{notch} and Q is the notch-frequency and the quality factor, respectively.

In order to have a strong attenuation at the double-line frequency, the quality factor of the notch filter should be high and the center frequency must be accurately tuned. In [54], an analog notch filter is realized using the circuit shown in Fig. 1.9. However, as shown in Fig. 1.10, the quality of the notch filter will be degraded when component tolerances are present, which cannot be avoided in practice.

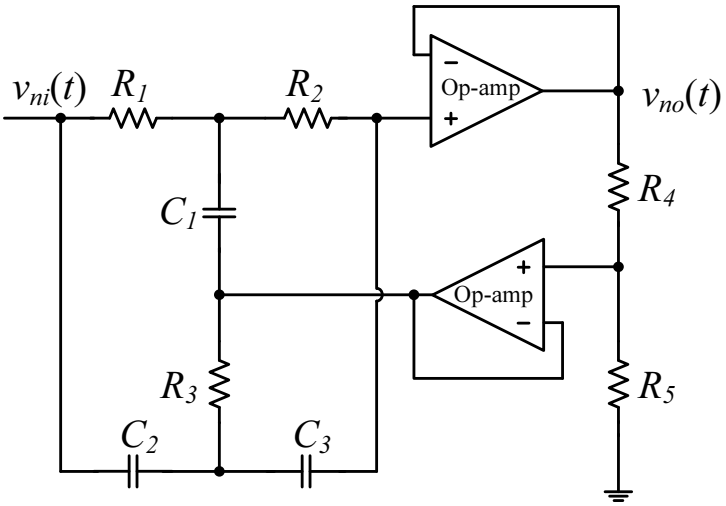


Figure 1.9: Notch filter realized by analog circuit.

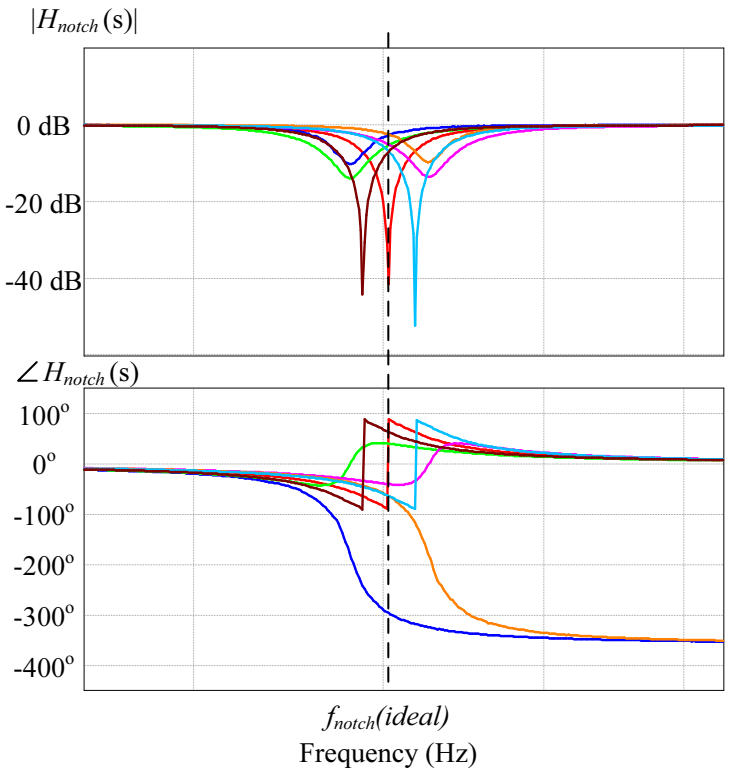


Figure 1.10: Bode plot of analog notch filter in the presence of component tolerances.

Instead of analog implementation, digital controller represents a better tool for realizing high-quality notch filter [55], [56], [57] due to its better stability, higher precision and adaptiveness [58]. When the higher harmonic components appear in the output voltage of PFC pre-regulator, more advanced solutions such as digital

comb filter [59] and MAF filter [60] having multiple notch frequencies can be used. These filters are capable of adjusting the notch frequency/ies automatically in response to variation in line frequency (usually ranging from 50 Hz to 60 Hz). However, the need for digital implementation and higher cost make notch-filter-based approaches not economically feasible for all applications.

1.6.6 Ripple Cancellation Approach

Another family of solution based on ripple estimation/cancellation has been proposed to eliminate ripple from the error voltage [61], [62], [63]. With this solution, an estimated reproduction of the sampled output voltage ripple is generated by additional circuitry and subtracted from the feedback output voltage with the aim to produce a ripple-free error signal for further processing by the voltage error amplifier. As a consequence, the bandwidth of the voltage control loop can be increased without amplifying the double-line frequency component and, hence, a near-unity power factor can be attained.

Assume that an ideal PFC pre-regulator has a power factor of unity, and its input current is sinusoidal and in phase with the input voltage. Its instantaneous input power is equal to its instantaneous output power as given by the following power balance equation.

$$P_{in} - P_{in}\cos\left(2\omega_{line}t\right) = C_o V_o \frac{dv_o(t)}{dt} + \frac{v_o(t)^2}{R_o} \tag{1.14}$$

where P_{in} and ω_{line} is the average input power and the angular line frequency, respectively, $v_o(t)$ is the instantaneous output voltage of the PFC pre-regulator.

Under the assumptions that efficiency is 100% and output capacitor C_o is very large such that all harmonic current at the double-line frequency $2\omega_{line}$ flows through the output capacitor, the output voltage ripple $\tilde{v}_o(t)$ can be described by the idealized formula given by Eq. (1.15), where P_o is the average output power

of the PFC pre-regulator.

$$\tilde{v}_o(t) = -\frac{P_o}{2\omega_{line} C_o V_o} \sin(2\omega_{line} t) \tag{1.15}$$

Based on this equation, various circuitries have been proposed to estimate the output voltage ripple and subtract it from the sampled output voltage. In [64], a ripple estimation network consisting of a bandpass filter, an amplifier with fixed gain, and a 90° phase shifter was presented, and a reproduction of the circuit diagram is shown in Fig. 1.11. The advantage of this circuit is its simplicity. However, any inaccurate estimation of the input parameters to the idealized equation, for example, efficiency, output capacitance and line frequency, will cause an inaccurate estimation of the output voltage ripple and results in a distortion of the input current waveform. To alleviate this problem, an adaptive ripple estimator was proposed in [65], and its configuration is shown in Fig. 1.12. The amplitude of the estimated output voltage ripple is forced to track the amplitude of the sampled output voltage ripple. However, the main drawbacks of this more accurate ripple estimator are the needs for phase locked loop (P.L.L.) and the additional high-pass filters being used are required to be identical.

1.6.7 Other solutions

Besides the main categories of solutions discussed above, some researchers demonstrated other ways to achieve good dynamic performance without degrading the power factor. One of these methods is line-voltage-feedforward, which improves the dynamic response of PFC pre-regulator under line-voltage variations [28], but it will not compensate for load changes and fast-scale line-voltage variations [4]. Another method is load-current-feedforward which provides fast compensation for load changes [66]. However, it tends to lower the efficiency of PFC pre-regulator, particularly in high-power applications, due to the insertion

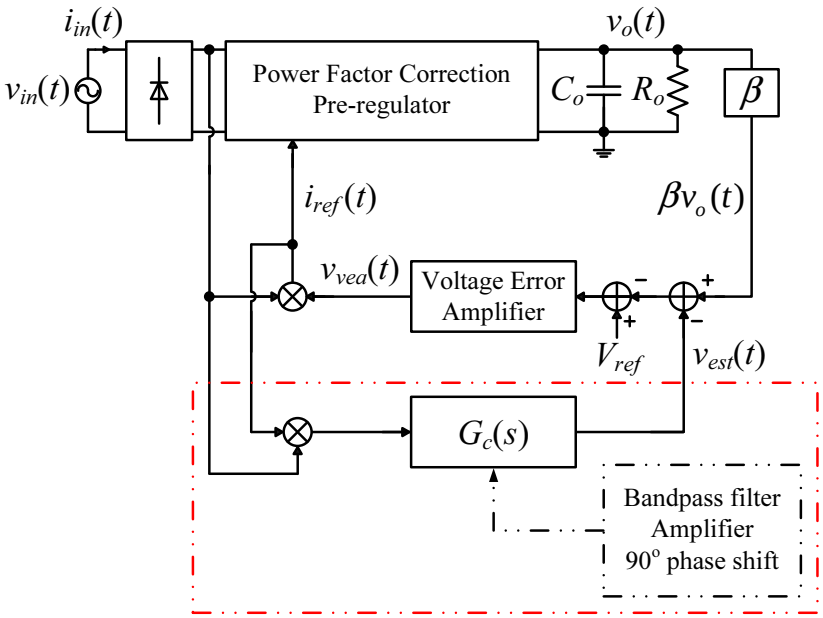


Figure 1.11: Ripple compensation network proposed by Spiazzi *et al.* [64].

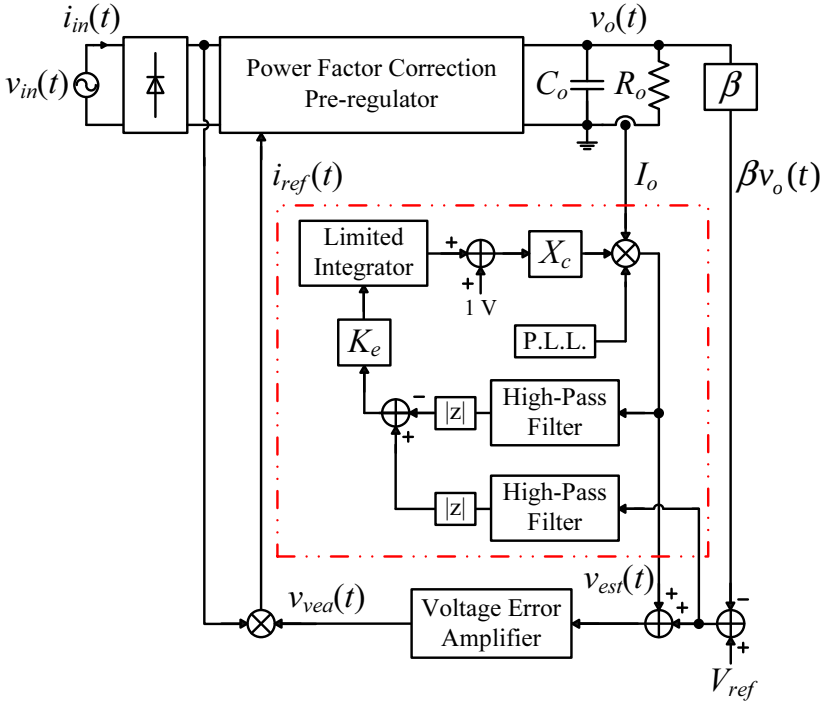


Figure 1.12: Ripple compensation network proposed by Wall *et al.* [65].

of current-sense resistor in the load current's path.

Another solution is to add a sample-and-hold (S/H) circuit between voltage error amplifier and multiplier [67]. Despite that a high power factor is achieved, the S/H circuit usually suffers from noise problem and the maximum bandwidth of

the outer voltage loop is limited to the line frequency. Similar technique has been suggested in [68] but more samples are obtained within one line cycle. However, a more complex circuit is necessary unless a digital controller is used.

Alternatively, in the works of Zheng *et al.* [69], [70], the authors proposed a method to decouple the current control loop from the voltage control loop, and monitor them by means of two independent controllers and switches. Besides the requirement of an extra data-mapping process, the overall efficiency of the proposed converter is reduced compared to a standard boost converter due to the utilization of more switches.

Besides increasing the closed-loop bandwidth, it is reported in [71] that the dynamic response of PFC pre-regulator can be improved by reducing its output impedance. This can be achieved by including an additional inner loop designed with reference to the PFC pre-regulator's reference model obtained by frequency-domain analysis. However, as stated in [54], the resulting improvement in dynamic response is less significant compared to the aforementioned methods.

1.7 Research Objectives

In the current research work, main focus is directed at ripple estimation and cancellation, which provides a practical and economical solution to achieve near-unity power factor and fast dynamic response of PFC pre-regulator simultaneously. As discussed before, the existing ripple estimation methods are all formulated based on an idealized equation, i.e. Eq. (1.15), which can give rise to accurate ripple estimation over a limited range of operating conditions only. In view of this limitation, a new ripple estimation/cancellation circuit that overcomes the limitation is desirable and will be proposed in this research work. In the first stage, attention will be given to ripple estimation network that will generate an accurate replica of the sampled output voltage ripple, and give rise to

perfect ripple cancellation. The performances of the proposed ripple estimation network are investigated by implementing it on a PFC pre-regulator and testing it under a wide range of operating conditions. Next, in the second stage, efforts will be dedicated to reduce the complexity of the proposed ripple estimation network, while maintaining satisfactory power factor and dynamic response performances. Based on mathematical derivation of the main figures of merit, two other ripple estimation/cancellation methods will be proposed. Finally, the performances of these ripple estimation/cancellation methods will be compared and analyzed in terms of power factor and THD of PFC pre-regulator's input current. Based on the comparisons, suggestions will be given on the preferred ripple estimation/cancellation method based on user's power-factor and THD requirements.

1.8 Outline of the Thesis

The contents of this thesis are organized as follows:

In Chapter 1, the definitions of power factor of ac circuit and total harmonic distortion of input current are discussed. Several international regulations and standards aimed at limiting the harmonic content of current drawn by mains-connected devices are briefly reviewed. By means of simulation results, the trade-off between power factor and dynamic response of PFC pre-regulator is demonstrated and discussed. Following this, a literature review of existing solutions aimed at achieving both high power factor and fast dynamic response is presented. Finally, the research objectives and the organization of this thesis are given.

In Chapter 2, a new ripple estimation network consisting of an amplitude tuner and a phase shifter is proposed and its operating principle is thoroughly discussed. The performances of the proposed ripple estimation network are investigated

by implementing it on an ACM-controlled boost PFC pre-regulator and testing it under a wide range of operating conditions. The resulting improvements in measured power factor and input current's THD are demonstrated by comparison with a similar boost PFC pre-regulator without ripple estimation/cancellation.

In Chapter 3, the main figures of merit of PFC pre-regulator with ripple cancellation is derived mathematically, and the results suggest the existence of an optimum amplitude of estimated output voltage ripple that leads to minimum local cancellation error in the presence of phase estimation error. Based on this finding, an alternative ripple estimation method is proposed and is verified experimentally by implementation on a boost PFC pre-regulator. Similar to Chapter 2, the performances of this alternative ripple estimation/cancellation method are tested and analyzed in depth.

In Chapter 4, the two ripple estimation methods proposed in Chapter 2 and 3 are briefly reviewed and compared with one that adopts further simplified amplitude and phase estimation approaches. Through the performance comparison between the three ripple estimation/cancellation methods, suggestions are made in relation to the preferred choice of method based on user's power-factor and THD requirements.

In Chapter 5, conclusions and suggestions for future research are given.

Chapter 2

A Ripple Estimation Method Based on Minimum Global Cancellation Error

2.1 Introduction

In Chapter 1, it has been shown that the crossover frequency of PFC pre-regulator's loop gain is commonly configured to be very small in order to achieve near-unity power factor, and this inevitably gives rise to poor dynamic response. Ripple estimation/cancellation method is used to eliminate the double-line frequency component from the sampled output voltage before it propagates into the voltage control loop, hence the requirement of small bandwidth is not mandatory. The method based on ripple estimation/cancellation is attractive in the fact that it is located external to the voltage control loop and hence can be designed independently without affecting the dynamic response of PFC pre-regulator. The existing ripple estimation circuits, however, are only accurate under specific conditions, beyond which power factor will be degraded. In view of this, a new ripple estimation/cancellation network consisting of an amplitude tuner and a

phase shifter based on switched-resistor circuits is proposed and verified experimentally on a 200-W boost PFC pre-regulator. It is shown that the proposed ripple estimation network not only provides accurate ripple estimation over a wide range of operating conditions such as variation in load power, line voltage, line frequency, and output capacitor's value, it also gives a way to decouple the power factor of PFC pre-regulator from its controller bandwidth. With the aid of the proposed ripple estimation network, the desired features of fast dynamic response and unity power factor are both achieved.

In this chapter, a mathematical expression of the output voltage of a generic PFC pre-regulator is first derived in Section 2.2. In Section 2.3, the working principles of the proposed ripple estimation network, including the generation of ripple template, amplitude tuning, and phase shifting, are discussed in detail. Simulation results will be presented in Section 2.4 in order to verify the operation of the proposed ripple estimation method and its method of implementation. The proposed estimation circuit is then implemented and verified experimentally on a 200-W ACM-controlled boost PFC pre-regulator under different operating conditions in Section 2.5. In this section, comparisons are made with a conventional PFC pre-regulator without ripple estimation network. Finally, conclusion is given in Section 2.6.

2.2 Mathematical Description of PFC Pre-regulator's Output Voltage

Since the function of ripple estimation circuit is to generate a replica of the sampled output voltage ripple, a mathematical description of a generic PFC pre-regulator's output voltage is useful to aid the analysis of the circuit's operation. Assuming that the line voltage is $v_{in}(t)$, and the PFC pre-regulator's input current

$i_{in}(t)$ is closely regulated to track the line voltage waveform, i.e. at unity power factor, we have

$$v_{in}(t) = V_p \sin(\omega_{line} t) \tag{2.1}$$

$$i_{in}(t) = I_p \sin(\omega_{line} t) \tag{2.2}$$

where V_p and I_p is the peak value of the line voltage and the PFC pre-regulator's input current, respectively, and ω_{line} is the angular line frequency.

Under this condition, the instantaneous input power $p_{in}(t)$ of the PFC pre-regulator is given by

$$p_{in}(t) = v_{in}(t) i_{in}(t) = V_p I_p \sin^2(\omega_{line} t) = P_{in} - P_{in} \cos(2\omega_{line} t) \tag{2.3}$$

where $P_{in} = V_p I_p / 2$.

Assuming that the PFC pre-regulator has an efficiency of 100%, this instantaneous power is delivered to the output RC network formed by the output capacitor C_o and load resistor R_o, and the power balance is described by the following differential equation.

$$P_{in} - P_{in} \cos(2\omega_{line} t) = C_o v_o(t) \frac{dv_o(t)}{dt} + \frac{v_o(t)^2}{R_o} \tag{2.4}$$

Solving Eq. (2.4) gives the exact solution of the PFC pre-regulator's output voltage $v_o(t)$ as

$$v_o(t) = V_o \sqrt{1 - \frac{1}{\sqrt{1 + (\omega_{line} R_o C_o)^2}} \cos(2\omega_{line} t - \tan^{-1}(\omega_{line} R_o C_o))} \tag{2.5}$$

The normalized output voltage $v_o(t)/V_o$ is plotted in Fig. 2.1 for different values of k, where $k = \omega_{line} R_o C_o$. On the same plots, the idealized output voltages described by Eq. (1.15) are plotted for the same values of k for comparison. It

can be seen that the output voltage ripple can be described satisfactorily by a sinusoidal function over a wide range of k. Compared to the generalized solution given by Eq. (2.5), it can be shown that the output voltage ripple as described by Eq. (1.15) is valid only when k is large. For small to medium value of k, the phase shift introduced by the RC network will deviate from 90°, hence Eq. (1.15) cannot provide an accurate ripple estimation under these conditions. Therefore, to enable a more concise presentation of the analysis in the following sections without sacrificing accuracy, the PFC pre-regulator's output voltage is assumed to be represented by the more general form given by Eq. (2.6), with $-90^{\circ} \leq \theta_r \leq 0^{\circ}$, where V_o and V_r is the PFC pre-regulator's average output voltage and output voltage ripple's amplitude, respectively, and $\theta_r = -\tan^{-1}(\omega_{line} R_o C_o)$.

$$v_o(t) = V_o + \tilde{v}_o(t) = V_o - V_r \cos(2\omega_{line} t + \theta_r) \tag{2.6}$$

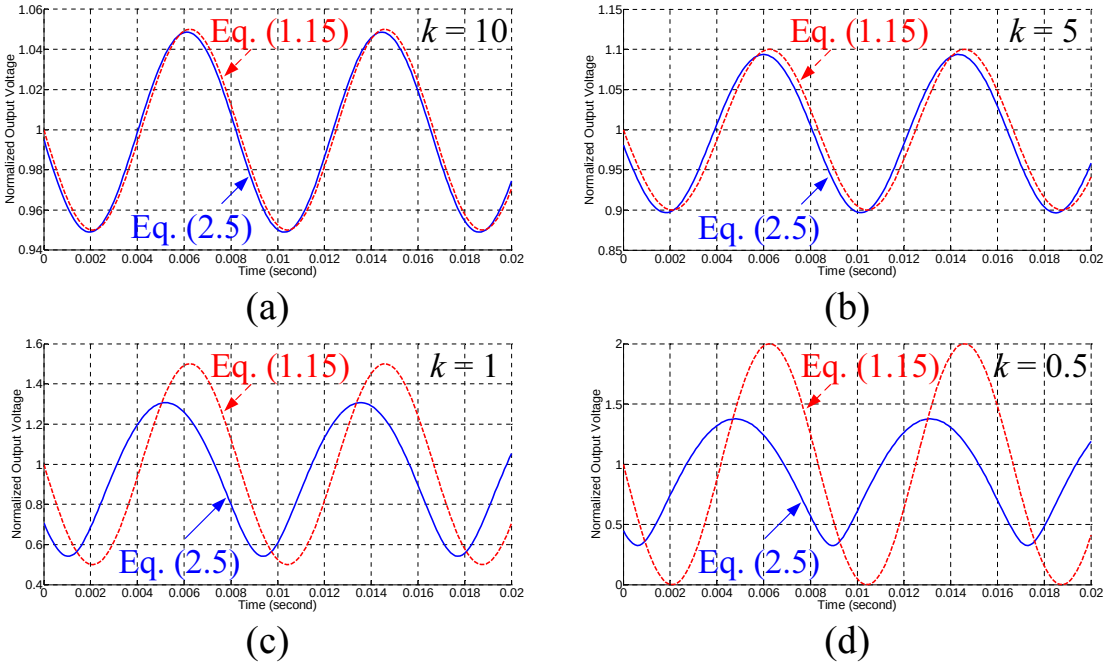


Figure 2.1: Comparison of the normalized PFC pre-regulator's output voltages for different values of k plotted using Eq. (1.15) (idealized) and Eq. (2.5) (actual) with f_{line} =60 Hz.

2.3 Proposed Ripple Estimation Circuit

In this section, the proposed ripple estimation/cancellation circuit is discussed in detail. Fig. 2.2 shows the complete block diagram of the PFC pre-regulator system consisting of the PFC pre-regulator's power stage (refer to Fig. 1.1) and the proposed ripple estimation circuit. Initially, the ripple template $\tilde{v}_{rt}(t)$ is generated from the sampled rectified line voltage $K_m\,|v_{in}(t)|$ and the reference signal for the PFC pre-regulator's input current $i_{ref}(t)$. The output voltage ripple $\tilde{v}_o(t)$, which acts as the reference for adjusting the amplitude and phase of the ripple template, is sampled by stepping down the PFC pre-regulator's output voltage $v_o(t)$ by a factor of α. The dc component in the sampled output voltage is removed by a High-Pass Filter (HPF), and the resulting sampled output voltage ripple is described by Eq. (2.7).

$$\alpha\tilde{v}_o(t) = -\alpha V_r \cos(2\omega_{line}t + \theta_r) \tag{2.7}$$

By taking the sampled output voltage ripple $\alpha\tilde{v}_o(t)$ as reference, the ripple template $\tilde{v}_{rt}(t)$ is modified in amplitude by the amplitude tuner, and subsequently in phase by the phase shifter. The sampling gains α and β are chosen to be different in value, where $\alpha > \beta$, to improve the signal-to-noise ratio of the sampled output voltage ripple $\alpha\tilde{v}_o(t)$ for more accurate processing by the ripple estimation circuit. To correct for this difference, the modified ripple template $\tilde{v}''_{rt}(t)$ is adjusted by a gain of $\lambda = \beta/\alpha$ before it is subtracted from the sampled output voltage $\beta v_o(t)$. The modified ripple template $\lambda\tilde{v}''_{rt}(t)$ should be identical to the sampled output voltage ripple $\beta\tilde{v}_o(t)$ and the subtraction of one by the other will ideally produce a ripple-free signal for further processing by the voltage error amplifier. Since no ripple is to be attenuated by the voltage error amplifier, it can be designed to provide more voltage gain at high frequencies for meeting the

requirement for fast dynamic response. Since the estimated output voltage ripple $v_{est}(t)$ only affects the input signal of the voltage error amplifier, while the line voltage feedforward function, which is typically implemented in commercial PFC controllers, only acts on the output signal of the voltage error amplifier, the proposed ripple estimation network is inherently compatible with the existing PFC controller architecture.

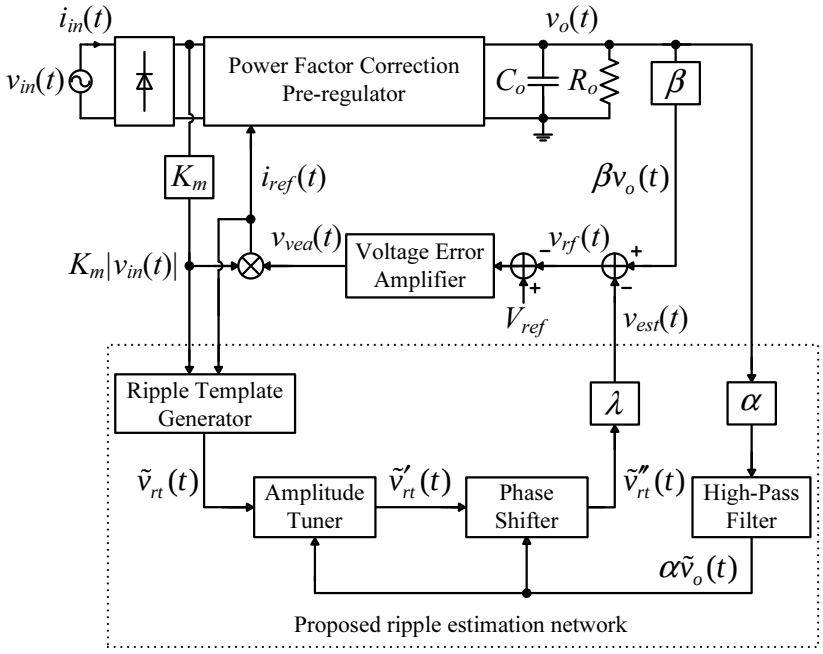


Figure 2.2: PFC pre-regulator system with proposed ripple estimation circuit.

2.3.1 Ripple Template Generation

Fig. 2.3 shows the block diagram of the ripple template generator which is used to produce a ripple template from the sampled rectified line voltage $K_m\,|v_{in}(t)|$ and the inductor's current reference $i_{ref}(t)$. Since a unity power factor is assumed, these signals can be described by $K_m V_p\,|\sin(\omega_{line}t)|$ and $I_p\,|\sin(\omega_{line}t)|\,R_s$, respectively, where K_m is the line-voltage step-down ratio and R_s is the current sense resistor's value. The desired ripple template $\tilde{v}_{rt}(t)$ is generated by multiplying these two signals, followed by high-pass filtering which removes the resulting

dc component. In order to avoid the introduction of additional phase shift, the high-pass filter's cut-off frequency is configured to be approximately 1 Hz, i.e. two decades lower than the double-line frequency. The overall ripple template generation process is described by Eq. (2.8), where G_1 and G_2 is the amplification gain for $K_m\,|v_{in}(t)|$ and $i_{ref}(t)$, respectively, and V_{rt} is the ripple template's amplitude given by $V_{rt} = P_{in}K_mR_sG_1G_2$. Since the amplitudes of the sampled rectified line voltage $K_m\,|v_{in}(t)|$ and the inductor's current reference $i_{ref}(t)$ are typically small, these signals are pre-amplified using non-inverting amplifier before undergoing multiplication.

$$\begin{aligned} v_{mult}(t) &= [G_1K_m\,|v_{in}(t)|]\cdot[G_2i_{ref}(t)] = V_{rt}(1-\cos(2\omega_{line}t)) \\ &\xrightarrow{\text{HPF}} \tilde{v}_{rt}(t) = -V_{rt}\cos(2\omega_{line}t) \end{aligned} \tag{2.8}$$

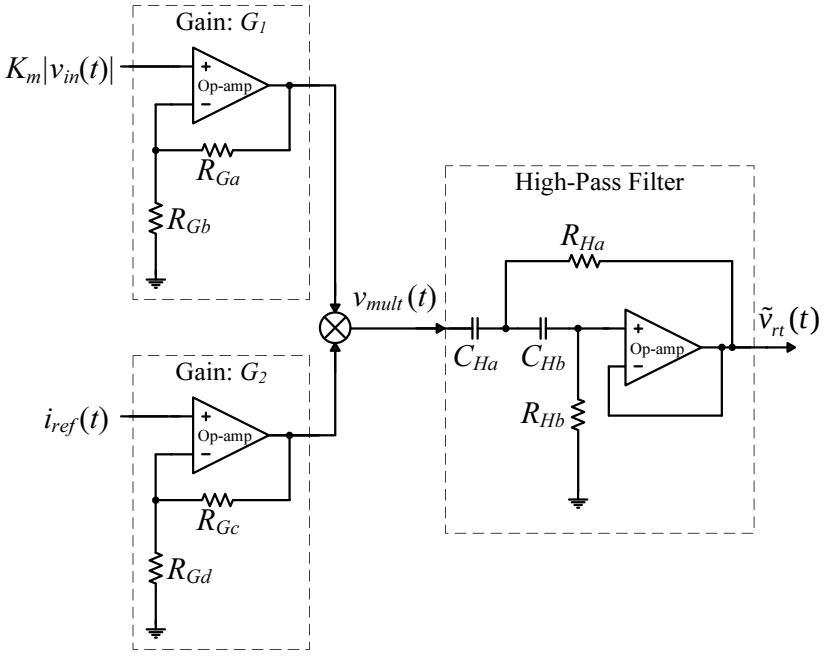


Figure 2.3: Block diagram of the proposed ripple template generator.

2.3.2 Amplitude Tuner

In order to generate a replica of the sampled output voltage ripple $\alpha\tilde{v}_o(t)$ described by Eq. (2.7), the ripple template $\tilde{v}_{rt}(t)$ is fed to the input of the amplitude tuner circuit, which will equalize the amplitude of the ripple template $\tilde{v}_{rt}(t)$ with that of the sampled output voltage ripple $\alpha\tilde{v}_o(t)$. The schematic diagram of the amplitude tuner circuit is shown in Fig. 2.4. It is mainly an inverting amplifier with adjustable gain, the value of which is determined by the amplitude difference between $\tilde{v}_{rt}(t)$ and $\alpha\tilde{v}_o(t)$. To realize an electronically adjustable gain, the fixed feedback resistance used in conventional inverting amplifier is replaced by two resistors R_{2a} and R_{2b}, each connected in series with a switch having a turn-on time of dT_s and $(1-d)\,T_s$, respectively, where d is the duty cycle of switch S_{2a} and $1/T_s$ is the switching frequency which is significantly higher than the double-line frequency. A switching frequency of 20 kHz is chosen but its choice can be further optimized by taking into consideration other factors including the inverting amplifier's bandwidth, switching delays, and component size (R_{LPF} and C_{LPF}) of the output Low-Pass Filter (LPF). The duty cycle d is derived from the pulse-width modulator according to the output of the error amplifier, which compares the amplitude of $\tilde{v}'_{rt}(t)$ to that of $\alpha\tilde{v}_o(t)$ (sampled using standard peak detector circuit respectively).

Fig. 2.5 shows the main waveforms of the amplitude tuner. It operates by amplifying the ripple template signal $\tilde{v}_{rt}(t)$ with a gain of $-R_{2a}/R_1$ and $-R_{2b}/R_1$ during dT_s and $(1-d)\,T_s$, respectively, where R_1 is the input resistance of the amplitude tuner. Its instantaneous output signal $\tilde{v}_{at}(t)$ is smoothed by an LPF for obtaining an amplitude-modified version of the input ripple template, but shifted 180° in phase. Since the ripple template has the largest amplitude under full-load condition, the inverting amplifier's gain should be chosen such that its output does not saturate under the same condition. By the principle of duty-cycle

averaging, the average voltage gain of the inverting amplifier $H_v(d)$ is given by

$$H_v(d) = -\frac{R_2(d)}{R_1} \tag{2.9}$$

$$R_2(d) = dR_{2a} + (1-d)\,R_{2b} \tag{2.10}$$

After the ripple template $\tilde{v}_{rt}(t)$ is processed by the amplitude tuner circuit, the amplitude of the modified ripple template $\tilde{v}'_{rt}(t)$ should be equal to that of the sampled output voltage ripple $\alpha\tilde{v}_o(t)$, and its phase should be inverted compared to $\tilde{v}_{rt}(t)$ due to the inverting amplifier's negative voltage gain. Although the LPF will introduce additional phase shift to the filtered signal, the amount of phase shift is generally small and negligible since the filter's cut-off frequency is designed to be significantly higher than the double-line frequency $2\omega_{line}$. Hence, in steady state, the output signal of the amplitude tuner can be closely approximated by Eq. (2.11).

$$\tilde{v}'_{rt}(t) = \alpha V_r \cos(2\omega_{line}t) \tag{2.11}$$

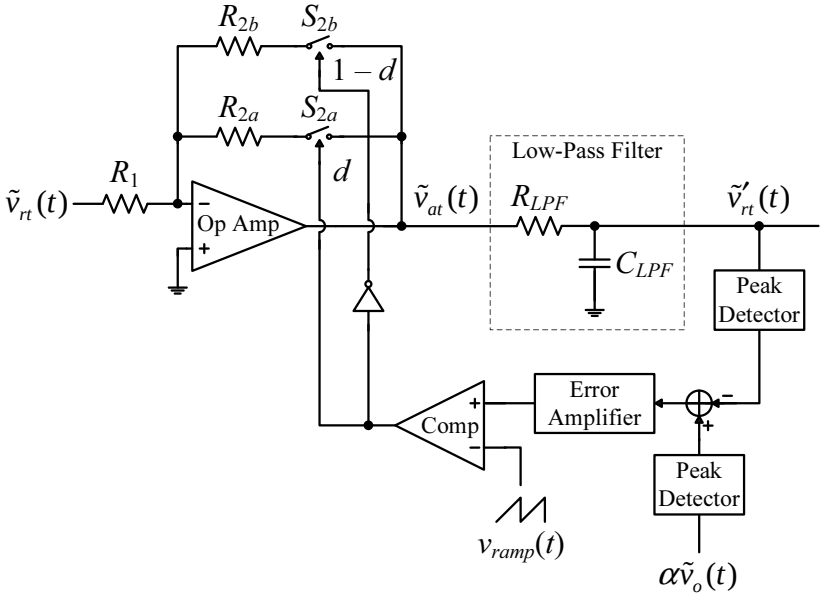


Figure 2.4: Schematic diagram of the proposed amplitude tuner.

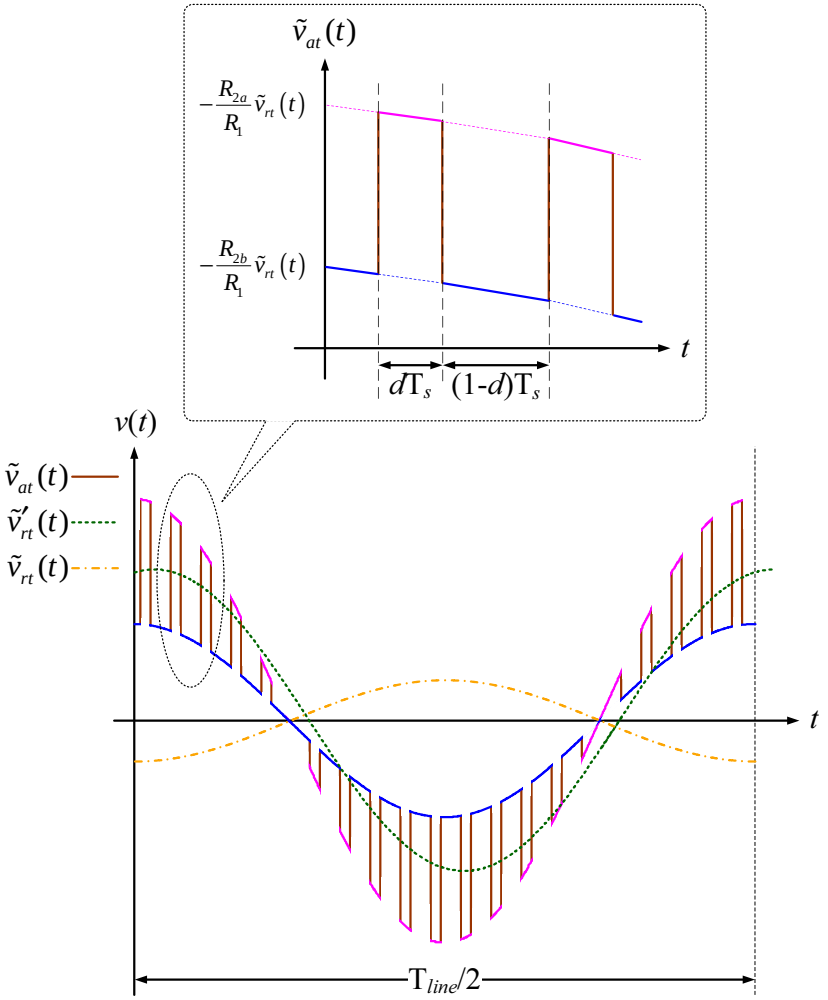


Figure 2.5: Operation waveforms of the proposed amplitude tuner.

2.3.3 Phase Shifter

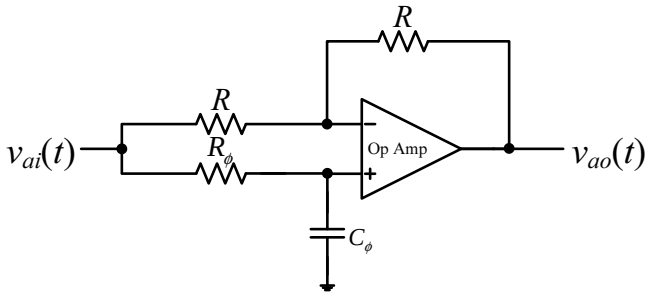


Figure 2.6: A standard All-Pass Filter (APF).

After the amplitude of the ripple template has been adjusted, the modified ripple template $\tilde{v}'_{rt}(t)$ is fed to the input of the phase shifter for phase adjustment.

The proposed phase shifter is derived from a standard All-Pass Filter (APF) as depicted in Fig. 2.6, which has a transfer function $H_\phi(s)$ given by Eq. (2.12).

$$H_\phi(s) = \frac{1 - sR_\phi C_\phi}{1 + sR_\phi C_\phi} = \frac{1 - s/\omega_o}{1 + s/\omega_o} \tag{2.12}$$

where

$$\omega_o = \frac{1}{R_\phi C_\phi} \tag{2.13}$$

$$|H_\phi(s)| = 1 \tag{2.14}$$

$$\angle H_\phi(s) = -2\tan^{-1}(\omega R_\phi C_\phi) \tag{2.15}$$

When an input signal at frequency ω passes through the APF, a frequency-dependent phase shift of $-2\tan^{-1}(\omega R_\phi C_\phi)$ is introduced by the filter, and the signal will emerge at the output as a phase-shifted version of the input with no change in amplitude. This implies that, when ω is fixed, the amount of phase shift introduced will also be fixed. For our purpose, the amount of phase shift should be made adjustable for a fixed ω, and this is done by replacing R_ϕ with two resistors $R_{\phi a}$ and $R_{\phi b}$ arranged to switch alternately at high frequency, as depicted in Fig. 2.7. Similar to the amplitude tuner, the switching frequency of the phase shifter is chosen to be 20 kHz. It can be deduced that, when the duty cycle d is 0 and 1, the amount of phase shift introduced will be $-2\tan^{-1}(\omega R_{\phi b} C_\phi)$ and $-2\tan^{-1}(\omega R_{\phi a} C_\phi)$, respectively. If the two resistors are chosen such that $R_{\phi a} \gg R_{\phi b}$ or $R_{\phi a} \ll R_{\phi b}$, a phase shift of 0^o to 180^o is realizable when d is varied between 0 and 1. As shown in Fig. 2.8 for the case of $\omega = \omega_{line}$, this is equivalent to adjusting the phase shift contribution along the vertical line $\omega/\omega_{line} = 1$ when d is varied. It can also be seen that, for realizing a phase shift of 0^o to 180^o, $R_{\phi a}$ and $R_{\phi b}$ should differ by at least four orders of magnitude.

The output signal of the APF $\tilde{v}_{ps}(t)$ is a phase-shifted version of its input

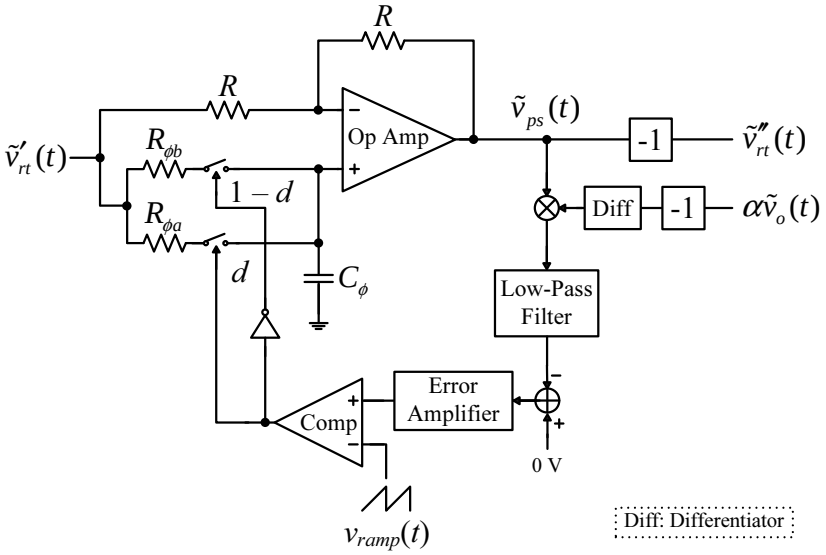


Figure 2.7: Schematic diagram of the proposed phase shifter.

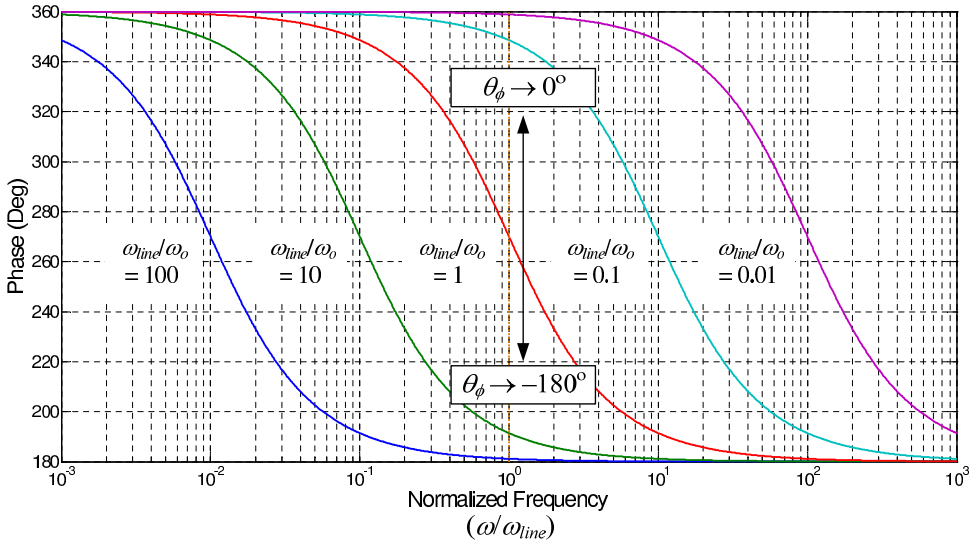


Figure 2.8: Phase curves of $H_\phi(s)$ for different values of ω_{line}/ω_o.

with no change in amplitude. Hence, it should take the following form, with $-180^o \leq \theta_\phi \leq 0^o$.

$$\tilde{v}_{ps}(t) = \alpha V_r \cos\left(2\omega_{line}t + \theta_\phi\right) \tag{2.16}$$

Recall that the sampled output voltage ripple $\alpha\tilde{v}_o(t)$ is given by $-\alpha V_r \cos\left(2\omega_{line}t + \theta_r\right)$. Since the maximum phase contribution from the APF is 180^o, $\alpha\tilde{v}_o(t)$ should be first inverted in order to limit the phase difference between $-\alpha\tilde{v}_o(t)$ and $\tilde{v}'_{rt}(t)$

to within the desired range. Next, their phase difference can be obtained by multiplication and low-pass filtering as described by Eq. (2.17).

$$\begin{aligned} -\alpha\tilde{v}_o(t)\tilde{v}_{ps}(t) &= \frac{(\alpha V_r)^2}{2}\left[\cos\left(4\omega_{line}t+\theta_r+\theta_\phi\right)+\cos\left(\theta_r-\theta_\phi\right)\right] \\ &\xrightarrow{\text{LPF}} \frac{(\alpha V_r)^2}{2}\cos\left(\theta_r-\theta_\phi\right) \end{aligned} \tag{2.17}$$

One problem associated with the use of $\cos(\theta_r - \theta_\phi)$ is that it is impossible to distinguish between the two cases: $(\theta_r > \theta_\phi)$ and $(\theta_r < \theta_\phi)$. This problem can be solved by adding a phase shift of 90° to $-\alpha\tilde{v}_o(t)$ before the multiplication is performed. The 90° phase shift is realized using an *RC* HPF. This modifies the above calculations to

$$\begin{aligned} -\alpha\tilde{v}_o(t+\frac{\pi}{2\omega_{line}})\tilde{v}_{ps}(t) &= \frac{(\alpha V_r)^2}{2}\left[\cos\left(4\omega_{line}t+\theta_r+\theta_\phi+90^\text{o}\right)+\cos\left(\theta_r-\theta_\phi+90^\text{o}\right)\right] \\ &\xrightarrow{\text{LPF}} \frac{(\alpha V_r)^2}{2}\sin\left(\theta_\phi-\theta_r\right) \end{aligned} \tag{2.18}$$

The plot of $\sin(x)$ versus x, where $x = \theta_\phi - \theta_r$, is shown in Fig. 2.9. It can be seen, therefore, that the signal emerging from the LPF is positive when $\theta_\phi > \theta_r$, negative when $\theta_\phi < \theta_r$, and zero when $\theta_\phi = \theta_r$. This signal is compared to zero and the difference is regarded as the phase error signal and is used to adjust the phase contribution from the phase shifter by means of pulse-width modulation.

In steady state, the condition $\theta_\phi = \theta_r$ holds and the output signal of the APF $\tilde{v}_{ps}(t)$ will be 180° out-of-phase compared to the sampled output voltage ripple $\alpha\tilde{v}_o(t)$. Thus, a unity-gain inverting amplifier is added to correct the phase difference. The resulted output signal of the phase shifter $\tilde{v}''_{rt}(t)$ will be in phase

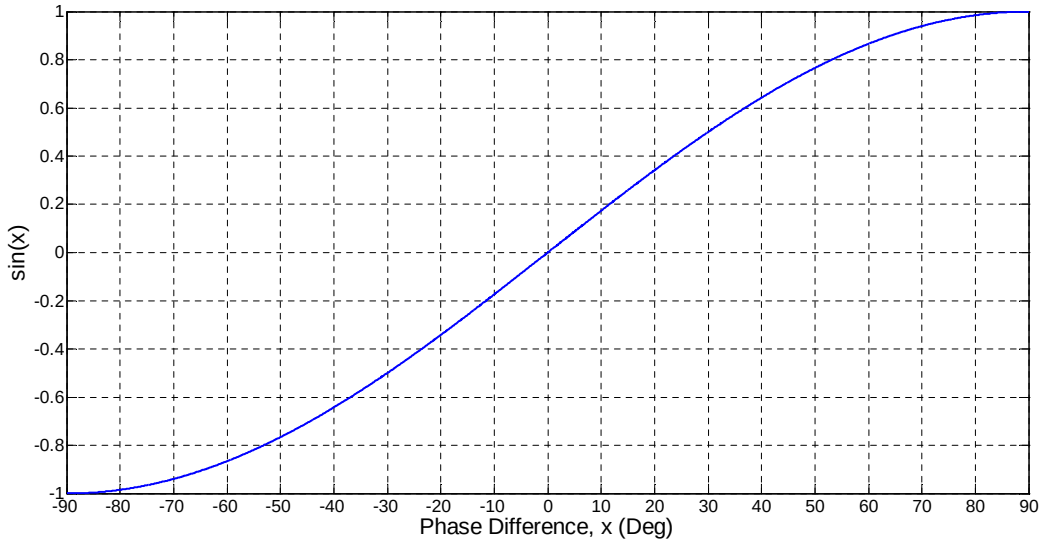


Figure 2.9: Plot of $\sin(x)$ versus x, where $x = \theta_\phi - \theta_r$.

and equal in magnitude with the sampled output voltage ripple $\alpha\tilde{v}_o(t)$, that is,

$$\begin{aligned} \tilde{v}''_{rt}(t) &= -\alpha V_r \cos(2\omega_{line}t + \theta_\phi) \\ &= -\alpha V_r \cos(2\omega_{line}t + \theta_r) \\ &= \alpha\tilde{v}_o(t) \end{aligned} \tag{2.19}$$

Finally, the estimated ripple $\tilde{v}''_{rt}(t)$ is stepped down by a factor of $\lambda = \beta/\alpha$ and subtracted from the sampled output voltage $\beta v_o(t)$ in the voltage control loop. The result of subtraction should produce a ripple-free signal for further processing by the voltage error amplifier as described by Eq. (2.20).

$$\begin{aligned} & \beta(V_o + \tilde{v}_o(t)) - \lambda\tilde{v}''_{rt}(t) \\ = \;& \beta V_o + \beta\tilde{v}_o(t) - (\frac{\beta}{\alpha})\alpha\tilde{v}_o(t) \\ = \;& \beta V_o \end{aligned} \tag{2.20}$$

2.4 Simulation Results

The proposed ripple estimation/cancellation circuit is simulated with PSIM in the context of a boost PFC pre-regulator designed to have a nominal output power of 200 W. The PFC pre-regulator is simulated with an input voltage of 110-Vrms/60-Hz and an average output voltage of 400 Vdc. The value of the boost inductor is 1 mH and the output capacitor C_o is intentionally selected to be small (16 μF). A similar boost PFC pre-regulator without ripple estimation circuit is simulated for comparison. In order to have a fair comparison, both PFC pre-regulators are designed to have the same closed-loop bandwidth. The loop gain's crossover frequencies of both PFC pre-regulators (with and without any ripple estimation network) are increased to the point where the output signal of the voltage error amplifier of the PFC pre-regulator without ripple estimation/cancellation begins to saturate, as shown in Fig. 2.11(b). Based on this requirement and the control-to-output transfer function derived in [72] and [73], the closed-loop bandwidth of both boost PFC pre-regulators are approximately 60 Hz. The uncompensated and compensated loop gains of both boost PFC pre-regulators are plotted in Fig. 2.10.

The simulated (i) output voltages, (ii) scaled-down input voltages and input currents, and (iii) voltage error amplifier's output signals of both PFC pre-regulators (with and without ripple estimation network) under nominal operating conditions are shown in Fig. 2.11(a) and Fig. 2.11(b). The average output voltages $v_o(t)$ of both PFC pre-regulators are 400 Vdc. By comparing the simulated input currents in both cases, it can be seen that the input current waveform is significantly improved and resembles an ideal sinusoidal one with the inclusion of the proposed ripple estimation network. The improvement is mainly due to the reduction in amplitude of the ripple component in the output signal of the voltage error amplifier $v_{vea}(t)$.

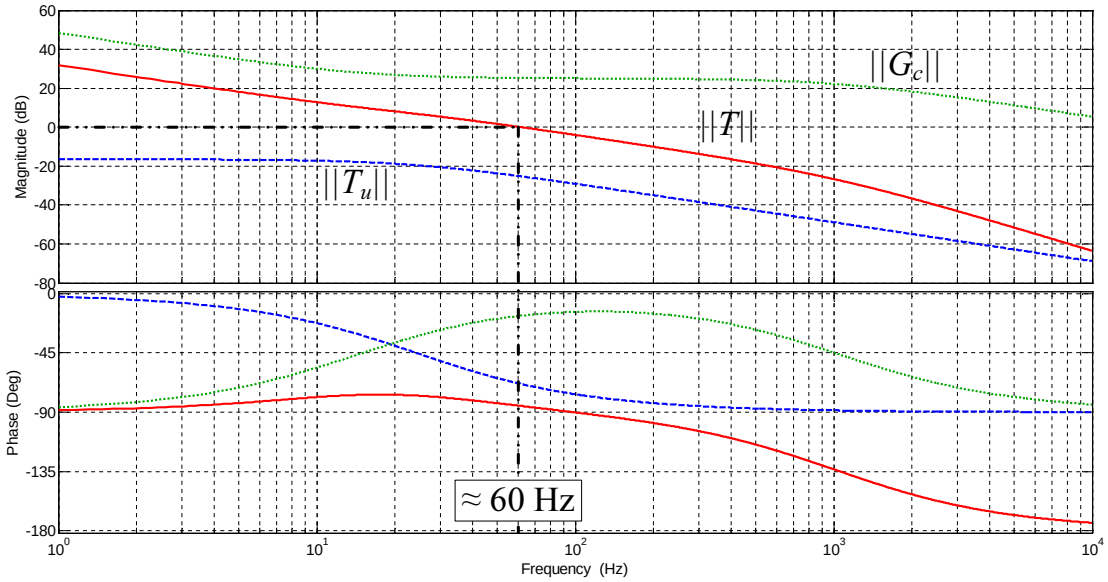


Figure 2.10: Design of compensation network for boost PFC pre-regulator prototype (T_u: uncompensated loop gain, G_c: compensation network, T: compensated loop gain).

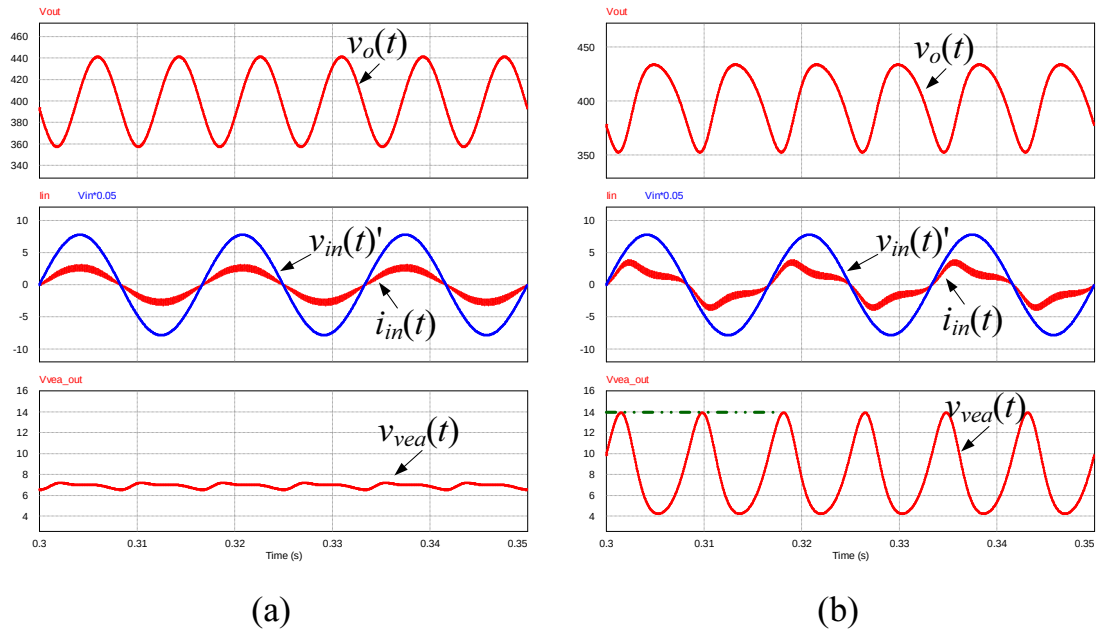


Figure 2.11: Simulated input and output waveforms of boost PFC pre-regulator (a) with and (b) without ripple estimation/cancellation under nominal operating conditions ($v_o(t)$: output voltage, $v_{in}(t)'$: scaled-down input or line voltage, $i_{in}(t)$: input or line current, $v_{vea}(t)$: output signal of voltage error amplifier).

Next, the simulated operating waveforms of the amplitude-tuner and phase-shifter circuits are shown in Fig. 2.12 and Fig. 2.13, respectively. Initially, an

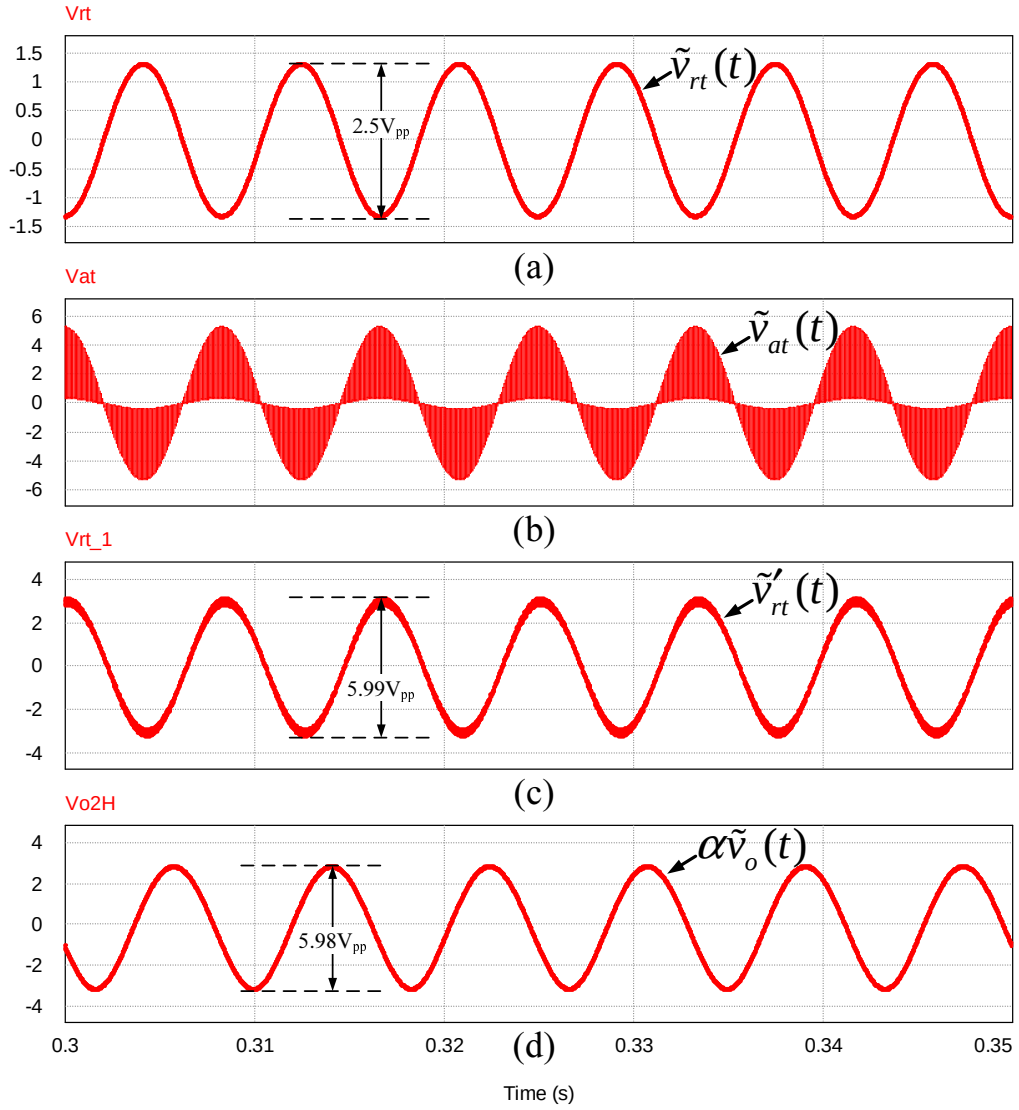


Figure 2.12: Simulated operating waveforms of amplitude tuner ((a) $\tilde{v}_{rt}(t)$: unmodified ripple template, (b) $\tilde{v}_{at}(t)$: unfiltered amplitude-tuned ripple template, (c) $\tilde{v}'_{rt}(t)$: filtered amplitude-tuned ripple template, (d) $\alpha\tilde{v}_o(t)$: sampled output voltage ripple).

unmodified ripple template $\tilde{v}_{rt}(t)$ having a simulated peak-to-peak voltage of 2.5 V_{pp} is injected into the amplitude tuner (which has a maximum gain R_{2a}/R_1 of 4 and a minimum gain R_{2b}/R_1 of 0.3), whereas the sampled output voltage ripple $\alpha\tilde{v}_o(t)$ is simulated to have a peak-to-peak voltage of 5.98 V_{pp}. Despite the large amplitude difference between the ripple template $\tilde{v}_{rt}(t)$ and the sampled output voltage ripple $\alpha\tilde{v}_o(t)$, the amplitude tuner is capable of equalizing the amplitudes of the modified ripple template $\tilde{v}'_{rt}(t)$ and the sampled output voltage

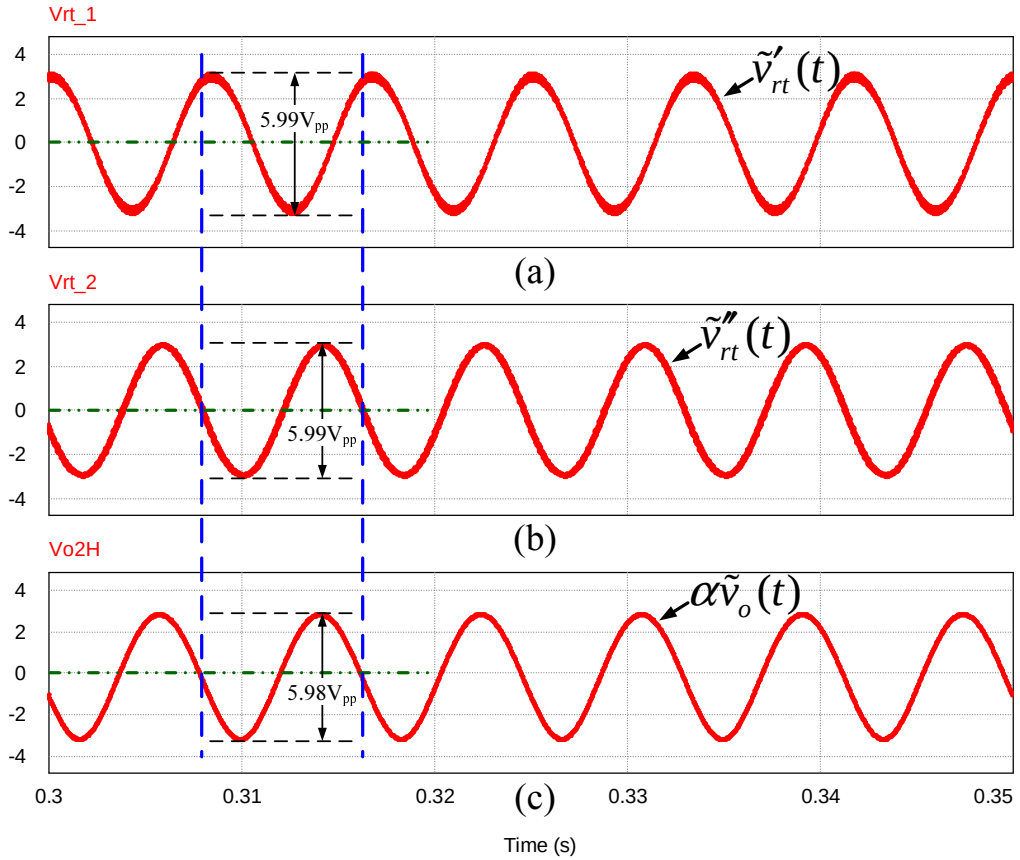


Figure 2.13: Simulated operating waveforms of phase shifter ((a) $\tilde{v}'_{rt}(t)$: amplitude-tuned ripple template, (b) $\tilde{v}''_{rt}(t)$: amplitude-and-phase-tuned ripple template or estimated output voltage ripple, (c) $\alpha\tilde{v}_o(t)$: sampled output voltage ripple).

ripple $\alpha\tilde{v}_o(t)$. After amplitude tuning, however, there still exists a phase difference between the modified ripple template $\tilde{v}'_{rt}(t)$ and the sampled output voltage ripple $\alpha\tilde{v}_o(t)$, as shown in Fig. 2.13. This problem can be solved by further processing the amplitude-tuned ripple template $\tilde{v}'_{rt}(t)$ through a phase shifter. From Fig. 2.13, it can be observed that the phase shifter has successfully minimized the phase difference between the output signal of the phase shifter $\tilde{v}''_{rt}(t)$ and the sampled output voltage ripple $\alpha\tilde{v}_o(t)$ without altering its amplitude. As a result, the output signal waveform of the phase shifter $\tilde{v}''_{rt}(t)$ is nearly identical to that of the sampled output voltage ripple $\alpha\tilde{v}_o(t)$.

In order to account for the difference in sampling ratios (α and β), the esti-

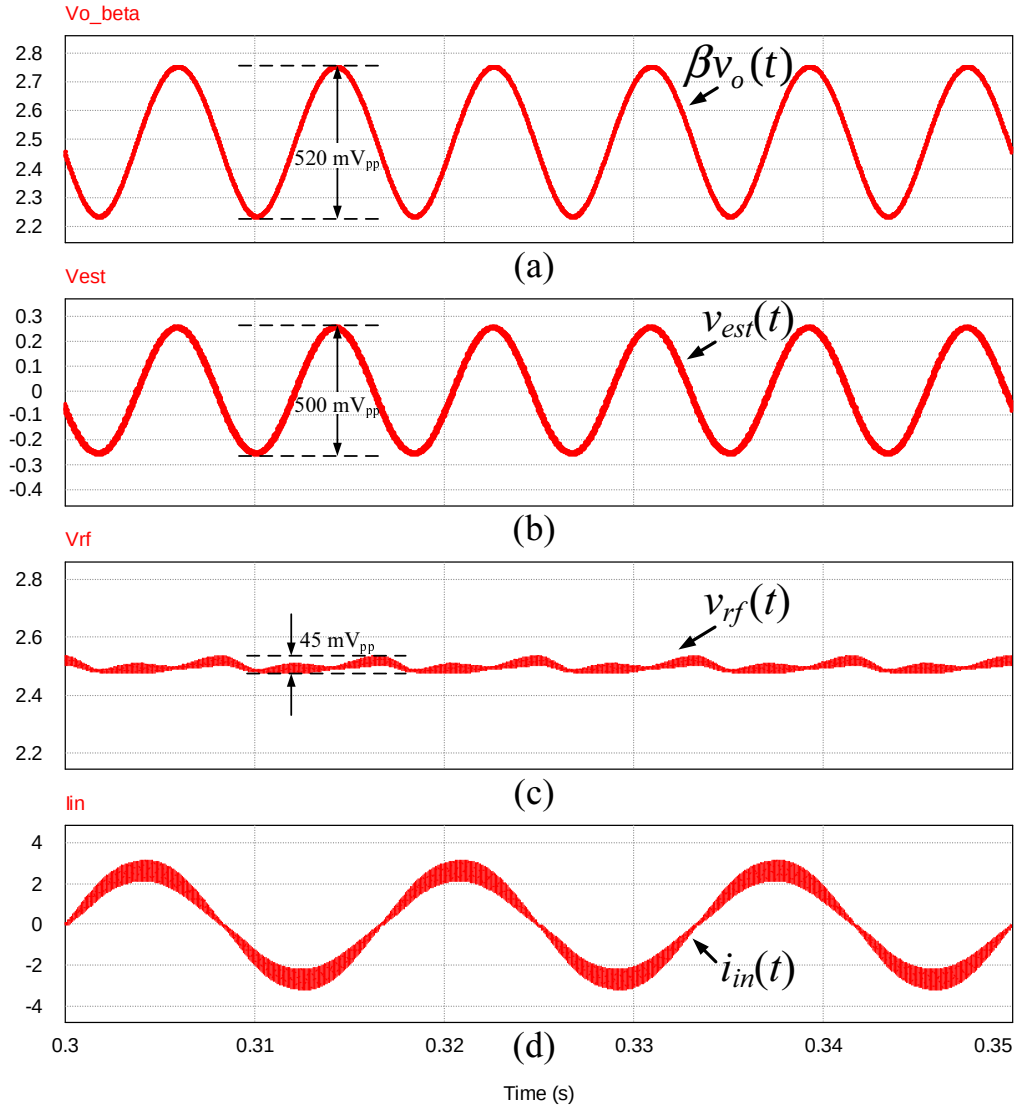


Figure 2.14: Simulated input and output waveforms of difference amplifier ((a) $\beta v_o(t)$: sampled output voltage, (b) $v_{est}(t)$: estimated output voltage ripple, (c) $v_{rf}(t)$: difference amplifier's output signal, (d) $i_{in}(t)$: input or line current).

mated output voltage ripple $v_{est}(t)$ is obtained by stepping down the output signal of phase shifter by a factor of $\lambda = \beta/\alpha$ before it is subtracted from the sampled output voltage using difference amplifier. The simulated operating waveforms of the difference amplifier are shown in Fig. 2.14. It can be seen that the amplitude of the estimated output voltage ripple $v_{est}(t)$ (with a peak-to-peak voltage of 500 mV_{pp}) closely matches that of the sampled output voltage ripple (with a peak-to-peak voltage of 520 mV_{pp}). After subtraction, the sampled output volt-

age ripple is greatly reduced in amplitude and the resultant signal $v_{rf}(t)$, which will be further processed by the voltage error amplifier, is nearly ripple-free. As a result, even with an increased bandwidth of the voltage control loop, the output signal of the voltage error amplifier $v_{vea}(t)$ is almost always ripple-free as depicted in Fig. 2.11(a), which leads to a near sinusoidal input current waveform as shown in Fig. 2.14.

2.5 Experimental Verification

Table 2.1: Specifications of boost PFC pre-regulator prototype.

Description	**Parameter**	**Value**
Nominal input or line voltage (rms)	V_{in}	110 V_{rms}
Nominal input or line frequency	f_{line}	60 Hz
Nominal output voltage	V_o	400 V
Nominal output power	P_o	200 W
Nominal load resistance	R_o	800 Ω
Output capacitance	C_o	16 μF
Maximum gain of amplitude tuner	R_{2a}/R_1	4
Minimum gain of amplitude tuner	R_{2b}/R_1	0.3

In this section, the proposed ripple estimation/cancellation circuit is verified by its implementation in an ACM-controlled boost PFC pre-regulator with the specifications listed in Table 2.1. The PFC pre-regulator's unity-gain-bandwidth is designed to be approximately 60 Hz in order to emulate the worst-case scenario where the output voltage ripple is large and the unity-gain-bandwidth is significantly larger than that encountered in conventional design ($\leq$ 10 Hz) for achieving fast dynamic response. To demonstrate the improvement in power factor as a result of implementing the proposed ripple estimation/cancellation circuit, a second PFC pre-regulator is constructed with the same specifications but with no the ripple estimation/cancellation circuit implemented.

Fig. 2.15 shows the steady-state input and output waveforms of the boost PFC pre-regulator prototype implemented with the proposed ripple estimation/cancellation circuit. The measured average output voltage and current is 402.9 V and 513.6 mA, respectively, and the efficiency is 90 %. The power factor was measured to be 0.999 by using Voltech Single-Phase Power Meter PM100. The total harmonic distortion (THD) of the PFC pre-regulator's input current is calculated to be 4.62 % from the FFT spectrum shown in Fig. 2.20(a). The near-unity power

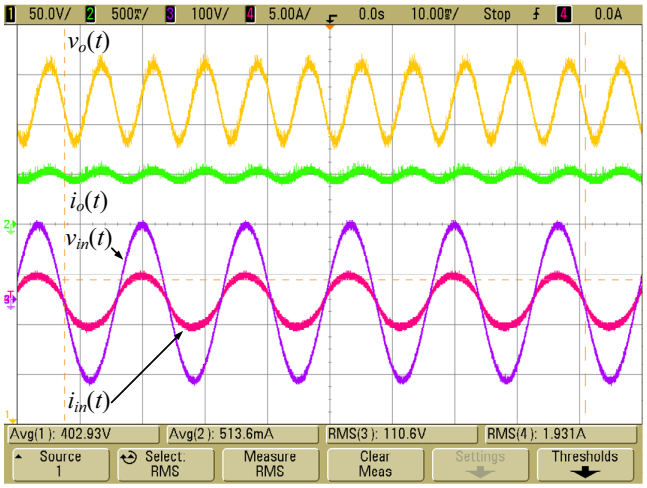


Figure 2.15: Input and output waveforms of boost PFC pre-regulator prototype ($v_{in}(t)$: input or line voltage, $i_{in}(t)$: input or line current, $v_o(t)$: output voltage, $i_o(t)$: output current).

factor as well as low THD verify that the PFC pre-regulator's input current $i_{in}(t)$ is very close to an ideal sinusoidal waveform and is in phase with the line voltage $v_{in}(t)$. Considering that the prototype was designed to have a large unity-gain-bandwidth and therefore insufficient attenuation at the double-line frequency, the achievement of near-unity power factor implies that the effect of the double-line frequency component has been successfully attenuated by ripple estimation/cancellation, and that the PFC pre-regulator's unity-gain-bandwidth can be designed independently from its power factor requirement.

Next, the operation of the proposed ripple estimation/cancellation circuit is verified by probing into the main operating waveforms of its individual parts, beginning with the amplitude tuner. Fig. 2.16 shows the input and output waveforms of the amplitude tuner. Recall that $\tilde{v}_{rt}(t)$ is the unmodified ripple template, $\alpha\tilde{v}_o(t)$ is the sampled output voltage ripple based on which the amplitude of $\tilde{v}_{rt}(t)$ is tuned, and $\tilde{v}_{at}(t)$ and $\tilde{v}'_{rt}(t)$ is the unfiltered and filtered amplitude-tuned ripple template, respectively, where $|\tilde{v}'_{rt}(t)| = |\alpha\tilde{v}_o(t)|$. From the measured waveforms, it can be seen that the unmodified ripple template $\tilde{v}_{rt}(t)$ has a peak-to-peak voltage of 2.31 V_{pp} while the sampled output voltage ripple $\alpha\tilde{v}_o(t)$ has a peak-to-peak

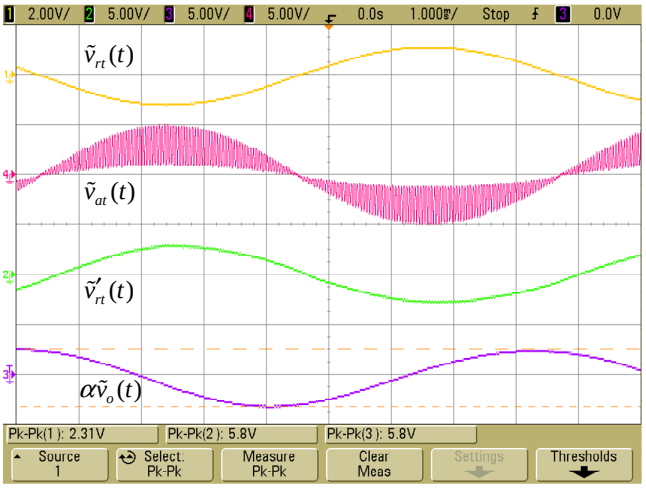


Figure 2.16: Main operating waveforms of amplitude tuner ($\tilde{v}_{rt}(t)$: unmodified ripple template, $\tilde{v}_{at}(t)$: unfiltered amplitude-tuned ripple template, $\tilde{v}'_{rt}(t)$: filtered amplitude-tuned ripple template, $\alpha\tilde{v}_o(t)$: sampled output voltage ripple).

voltage of 5.8 V_{pp}. At the output of the amplitude tuner, the amplitude of the modified ripple template $\tilde{v}'_{rt}(t)$ has been tuned to the same value as that of the sampled output voltage ripple $\alpha\tilde{v}_o(t)$, *i.e.* 5.8 V_{pp}. Fig. 2.16 also shows that the additional phase shift caused by the LPF at the amplitude tuner's output is small and negligible.

The amplitude-tuned ripple template $\tilde{v}'_{rt}(t)$ is further processed by the phase shifter that equalizes its phase with that of the sampled output voltage ripple $\alpha\tilde{v}_o(t)$. The main operating waveforms of the phase shifter are shown in Fig. 2.17. It can be observed that despite the initial large phase difference between the amplitude-tuned ripple template $\tilde{v}'_{rt}(t)$ and the sampled output voltage ripple $\alpha\tilde{v}_o(t)$ (the reference waveform), the phase shifter has correctly matched the phase of the former to that of the latter. In other words, the output of the phase shifter $\tilde{v}''_{rt}(t)$ represents a near-ideal replica of the sampled output voltage ripple $\alpha\tilde{v}_o(t)$. Before it is subtracted from the sampled output voltage $\beta v_o(t)$, the output of the phase shifter $\tilde{v}''_{rt}(t)$ is stepped down by a factor of $\lambda = \beta/\alpha$ to account for the different sampling gains used in the ripple estimation network (α) and voltage control loop (β).

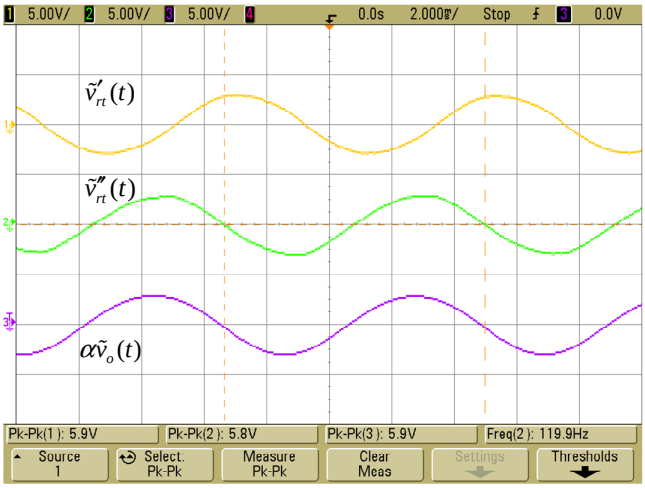


Figure 2.17: Main operating waveforms of phase shifter ($\tilde{v}'_{rt}(t)$: amplitude-tuned ripple template, $\tilde{v}''_{rt}(t)$: amplitude-and-phase-tuned ripple template or estimated output voltage ripple, $\alpha\tilde{v}_o(t)$: sampled output voltage ripple).

The accuracy of the estimated output voltage ripple $v_{est}(t)$ [$= \lambda\tilde{v}''_{rt}(t)$] can be evaluated by measuring the output of the difference amplifier that performs the subtraction between the sampled output voltage $\beta v_o(t)$ and the estimated output voltage ripple $v_{est}(t)$. Fig. 2.18 shows the input and output waveforms of the difference amplifier, from which it can be seen that despite the presence of a significant amount of double-line frequency component (with a peak-to-peak voltage of 520 $\mathrm{mV_{pp}}$) in the sampled output voltage, the output of the difference amplifier $v_{rf}(t)$ [$= \beta v_o(t) - v_{est}(t)$] is near ripple-free (with a peak-to-peak voltage of 50 $\mathrm{mV_{pp}}$) with an average value of 2.53 V. Since it forms the input signal to the voltage error amplifier, it can be deduced that the output of the voltage error amplifier is also near ripple-free, hence the input current $i_{in}(t)$ of the boost PFC pre-regulator, as shown in Fig. 2.18, is an undistorted, near-ideal sinusoidal waveform.

Next, two boost PFC pre-regulators, one with ripple estimation/cancellation and the other without, are compared in terms of their power factor and dynamic response performances when both are subjected to step changes in operating conditions. Fig. 2.19(a) and (b) shows the measured input and output waveforms of

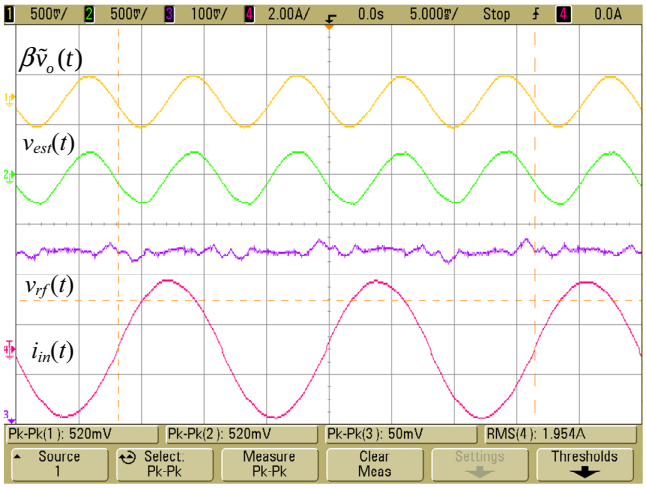


Figure 2.18: Input and output waveforms of difference amplifier ($\beta\tilde{v}_o(t)$: sampled output voltage ripple, $v_{est}(t)$: estimated output voltage ripple, $v_{rf}(t)$: output of difference amplifier, $i_{in}(t)$: input or line current).

the PFC pre-regulator with ripple estimation/cancellation when subjected to a step load decrease and increase, respectively. Fig. 2.19(c) and (d) shows the same waveforms of the PFC pre-regulator without ripple estimation/cancellation under the same step load changes. Since both PFC pre-regulators are designed to have the same unity-gain-bandwidth, they exhibit very similar dynamic characteristic in response to the step load changes, with a settling time of approximately 38 ms. However, in the former case, the PFC pre-regulator operates consistently with a near-unity power factor of 0.999 before and after the step load changes, while in the latter case, the PFC pre-regulator's power factor varies as the load condition changes (0.952 at nominal load and 0.92 at half-load). Fig. 2.20 shows the FFT spectra of the PFC pre-regulator's input current with and without ripple estimation/cancellation under full-load and half-load conditions. With the aid of the proposed ripple estimation/cancellation network, the THD of the input current has been reduced from 25.17 % to 4.62 % at full load and from 31.05 % to 3.31 % at half load. Fig. 2.21 shows that even when the operating conditions have changed significantly with a 50% reduction in load, the ripple estimation/cancellation circuit is able to generate an accurate replica of the sampled output voltage ripple,

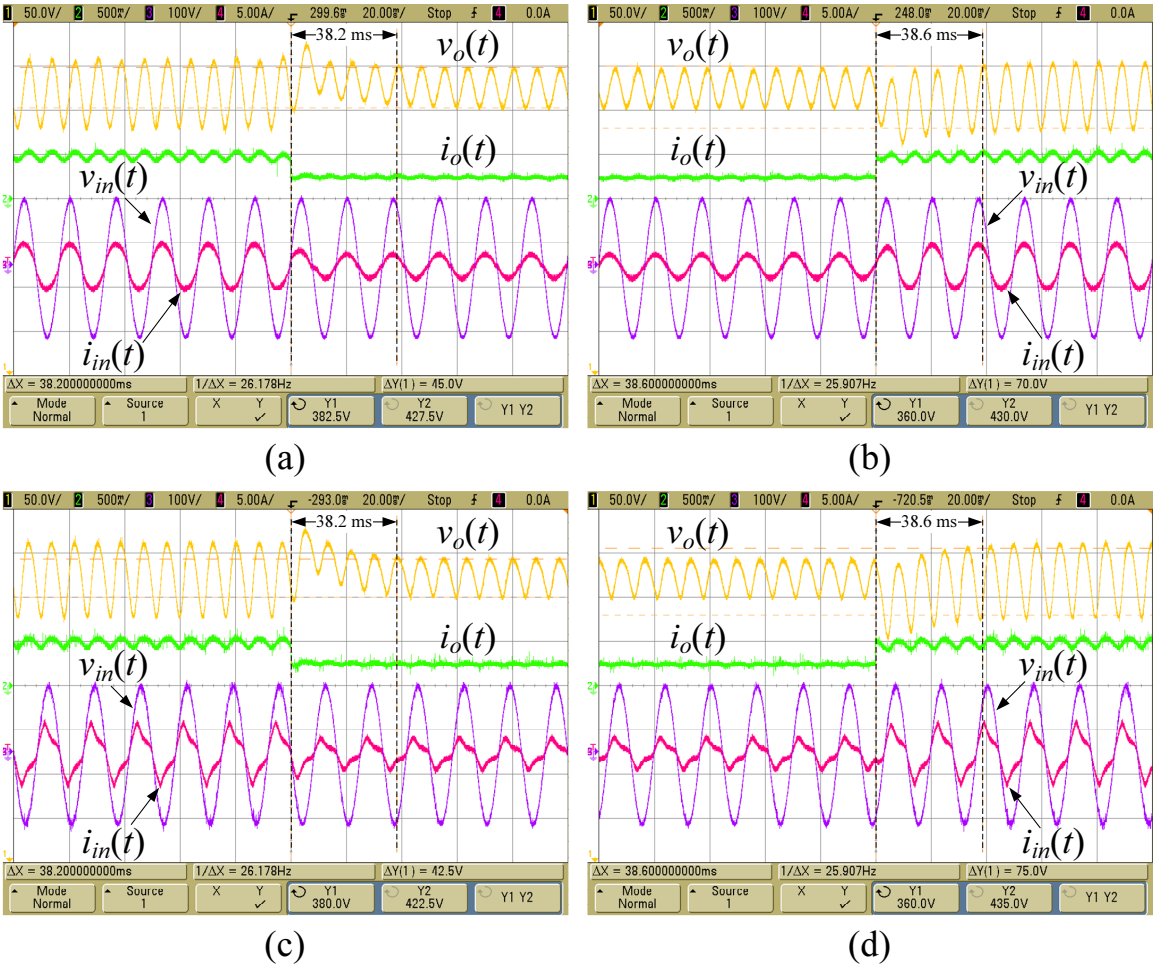


Figure 2.19: Input and output waveforms of boost PFC pre-regulator with [(a) and (b)] and without [(c) and (d)] ripple estimation/cancellation under step decrease [(a) and (c)] and increase [(b) and (d)] in load.

and hence eliminates it before it propagates through the voltage error amplifier. With the implementation of ripple estimation/cancellation, the double-line frequency component at the input of the voltage error amplifier has been reduced in amplitude from 269 mV_{pp} to 32 mV_{pp}.

Subsequently, the two boost PFC pre-regulators are subjected to step changes in line voltage and frequency, both of which are commonly encountered in practice by PFC pre-regulators. In the former case, the line voltage is stepped from the nominal value of 110 V_{rms} to 150 V_{rms} and back to 110 V_{rms}, while in the latter case, the line frequency is stepped from the nominal value of 60 Hz to 50 Hz and

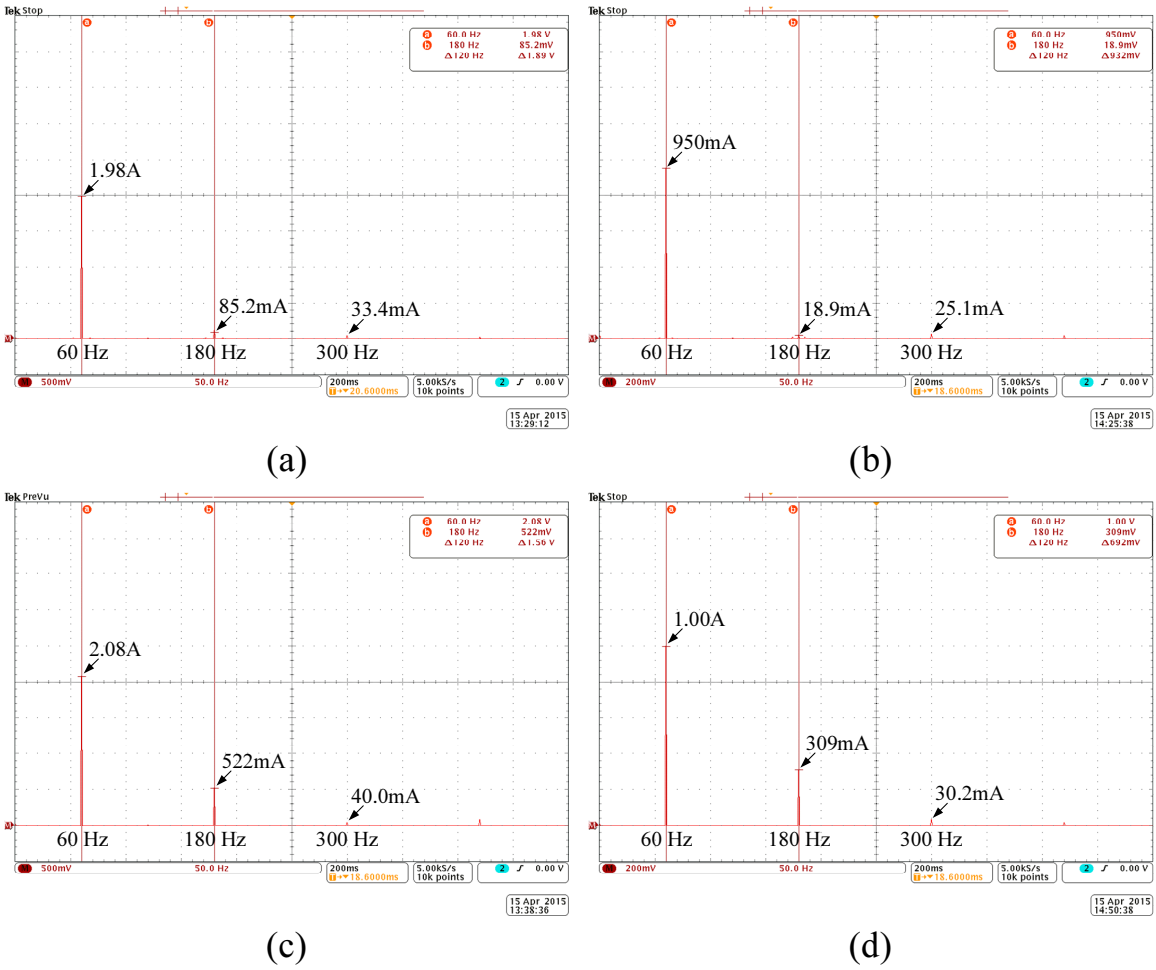


Figure 2.20: FFT spectra of the input current of boost PFC pre-regulator prototype with [(a) and (b)] and without [(c) and (d)] ripple estimation/cancellation under full-load [(a) and (c)] and half-load [(b) and (d)] conditions.

back to 60 Hz. The measured input and output waveforms for both cases are shown in Fig. 2.22 and Fig. 2.23, respectively.

In the case of line voltage variation, the PFC pre-regulator with ripple estimation/cancellation operates with a power factor of 0.999 at V_{in} =110 V_{rms} and 0.998 at V_{in} =150 V_{rms}. Near-unity power factor is achieved under both line voltages due to the elimination of the double-line frequency component from the voltage control loop by means of ripple cancellation. As depicted in Fig. 2.24, the THD of the input current at V_{in} =150 V_{rms} has been reduced from 45.74 % to 5.09 % with the aid of proposed ripple estimation/cancellation network. As

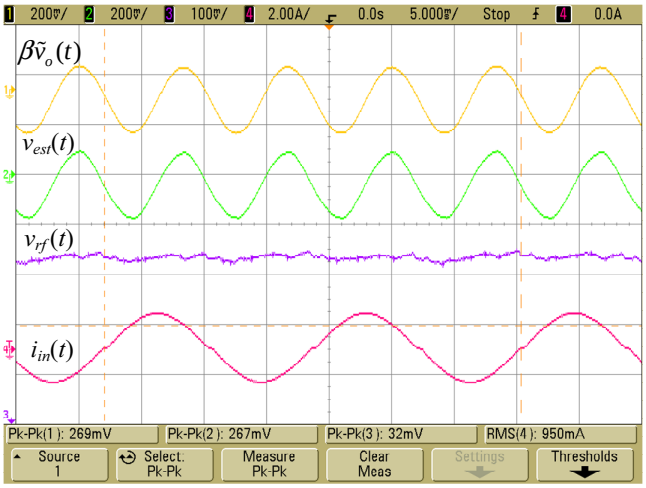


Figure 2.21: Input and output waveforms of difference amplifier under half-load condition ($\beta\tilde{v}_o(t)$: sampled output voltage ripple, $v_{est}(t)$: estimated output voltage ripple, $v_{rf}(t)$: output of difference amplifier, $i_{in}(t)$: input or line current).

shown in Fig. 2.25, the double-line frequency component at the input of the voltage error amplifier has been reduced in amplitude from 500 $\mathrm{mV_{pp}}$ to 48 $\mathrm{mV_{pp}}$ after ripple cancellation. On the contrary, the power factor of the PFC pre-regulator with no ripple estimation/cancellation has decreased from 0.952 at V_{in} =110 $\mathrm{V_{rms}}$ to 0.862 at V_{in} =150 $\mathrm{V_{rms}}$. Once again it is shown that the implementation of ripple estimation/cancellation can significantly reduce the sensitivity of PFC pre-regulator's power factor to changes in operating conditions.

In the case of line frequency variation, the PFC pre-regulator with ripple estimation/cancellation operates with a power factor of 0.999 at both f_{line} =50 Hz and f_{line} =60 Hz, while the power factor of the PFC pre-regulator with no ripple estimation/cancellation has decreased slightly from 0.952 at f_{line} =60 Hz to 0.951 at f_{line} =50 Hz. It can be calculated from the FFT spectra shown in Fig. 2.26 that the THD of the PFC pre-regulator's input current at f_{line} =50 Hz is reduced by approximately 83 % with the aid of ripple estimation/cancellation. Fig. 2.27 shows that the proposed ripple estimation/cancellation circuit is capable of tracking the line frequency variation and producing an accurate estimation of the sampled output voltage ripple. With the aid of ripple estimation/cancellation, the

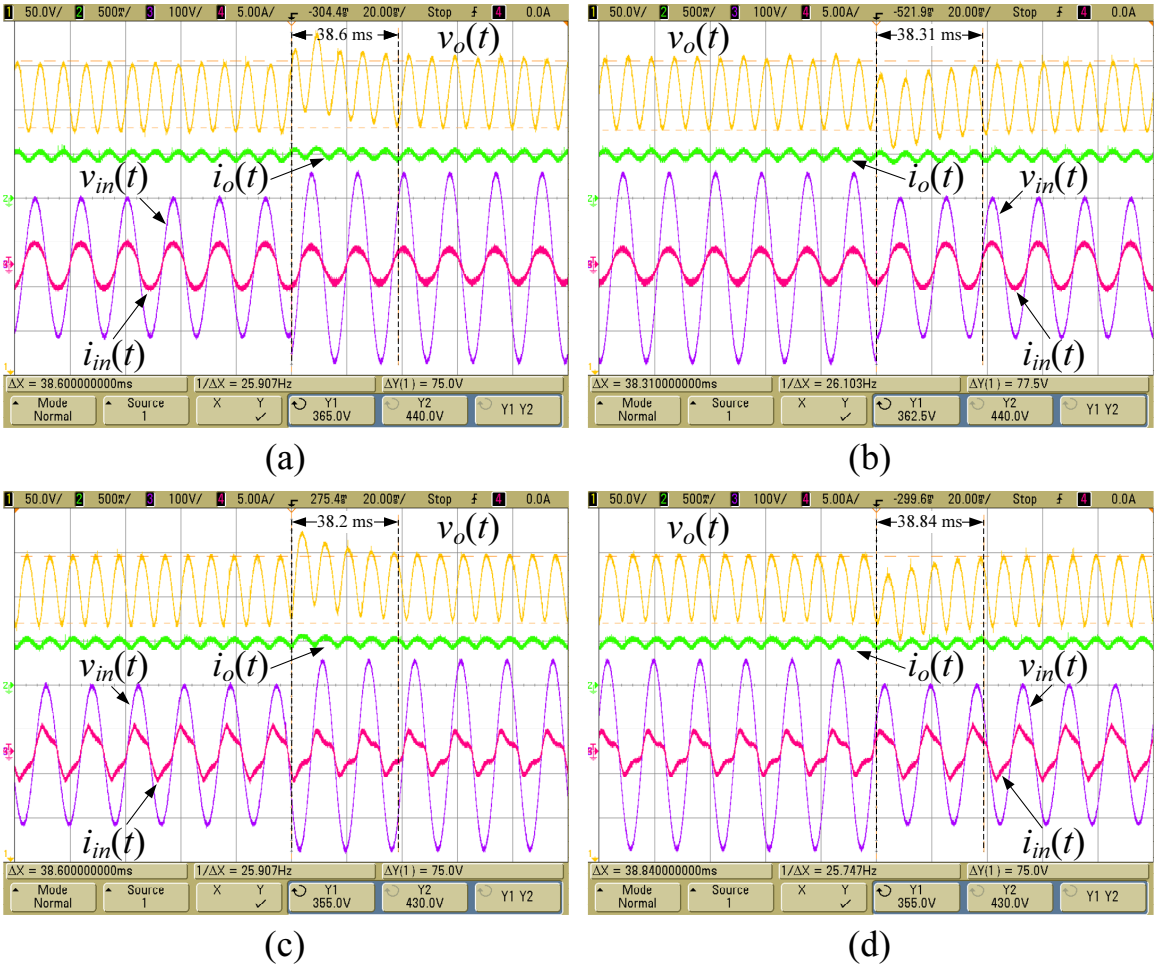


Figure 2.22: Input and output waveforms of boost PFC pre-regulator with [(a) and (b)] and without [(c) and (d)] ripple estimation/cancellation under step increase [(a) and (c)] and decrease [(b) and (d)] in line voltage.

double-line frequency component at the input of the voltage error amplifier has been reduced in amplitude from 590 $\mathrm{mV_{pp}}$ to 59 $\mathrm{mV_{pp}}$ after ripple cancellation.

Finally, the influence of output capacitor's size on the performance of boost PFC pre-regulator with ripple estimation/cancellation is investigated by doubling its output capacitance from 16 μF to 32 μF. In general, increasing output capacitance has the effect of increasing the phase shift θ_r (towards -90°) of the output voltage ripple $\tilde{v}_o(t)$ relative to the ripple template $v_{rt}(t)$, and vice versa, hence altering output capacitance provides a useful test to check if the ripple estimation/cancellation circuit can adaptively adjust and match the phase of the

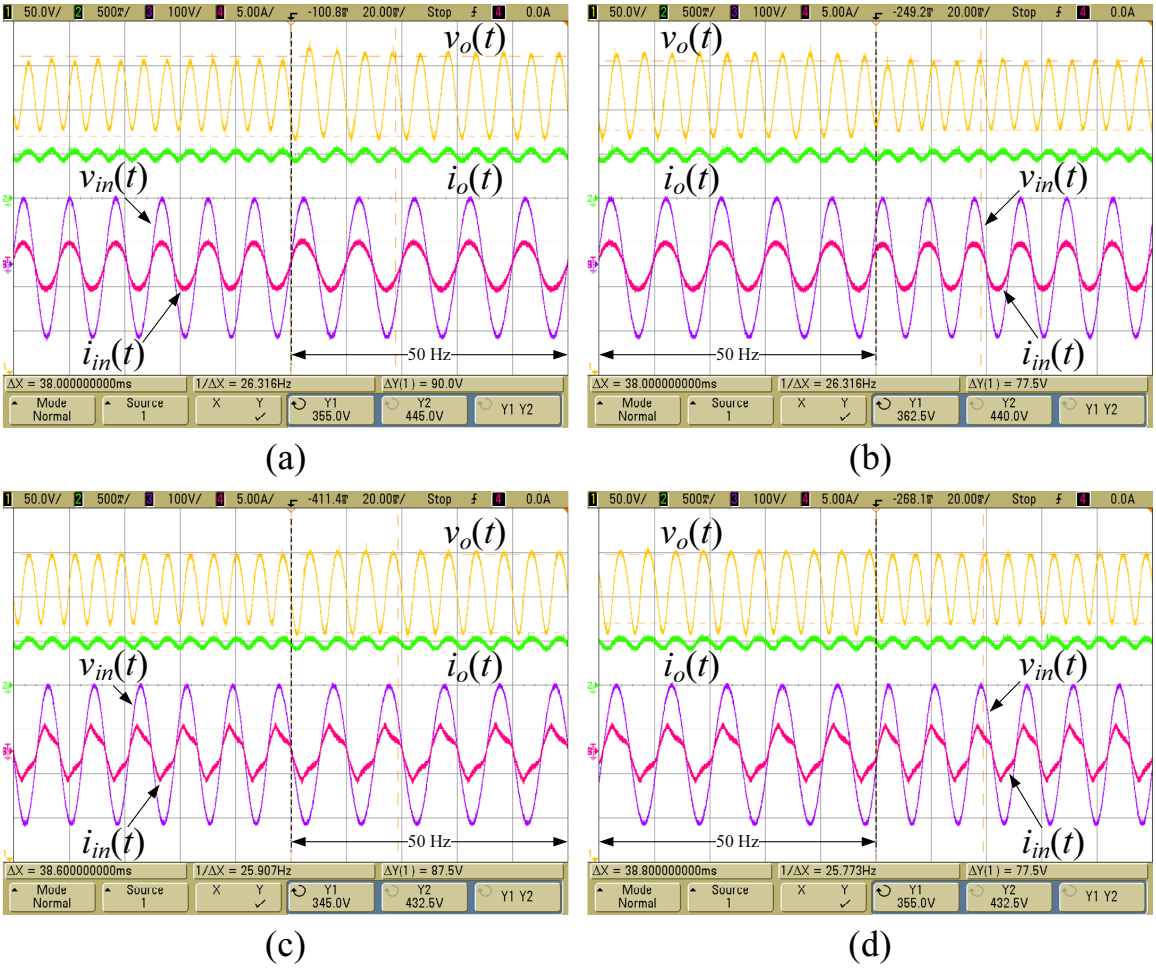


Figure 2.23: Input and output waveforms of boost PFC pre-regulator with [(a) and (b)] and without [(c) and (d)] ripple estimation/cancellation under step decrease [(a) and (c)] and increase [(b) and (d)] in line frequency.

ripple template to that of the output voltage ripple correctly. In addition, the output capacitance of PFC pre-regulators may change during their operation due to temperature change or aging, thus it is important that the ripple estimation/cancellation circuit will consistently produce accurate estimation of the output voltage ripple under these varying conditions. Such feature is impossible with the non-adaptive ripple estimation/cancellation circuit based on the use of Eq. (1.15). Fig. 2.28 shows that the double-line frequency component at the input of the voltage error amplifier has been reduced in amplitude from 257 mV_{pp} to 35 mV_{pp} after ripple cancellation. Hence, the desired near-unity power factor

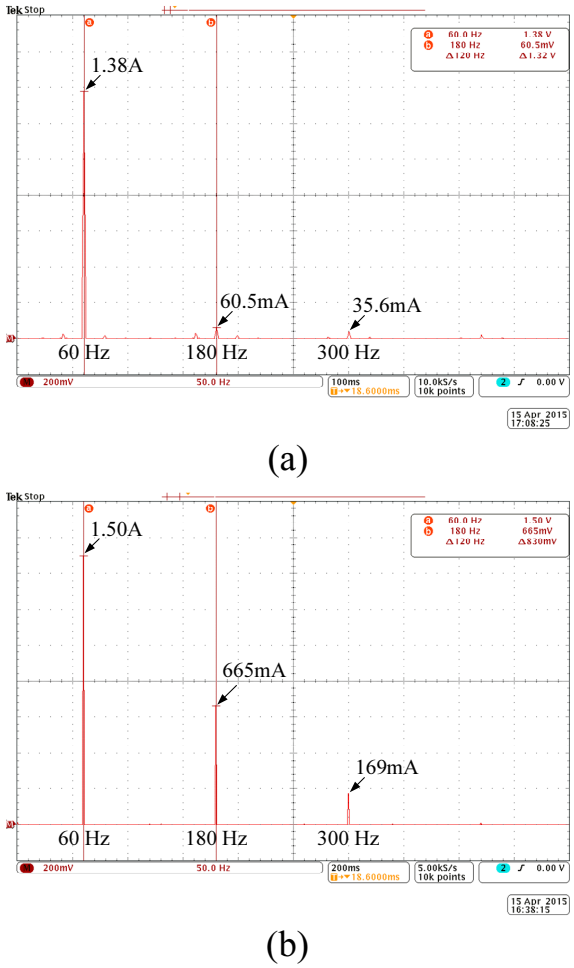


Figure 2.24: FFT spectra of the input current of boost PFC pre-regulator prototype (a) with and (b) without ripple estimation/cancellation at V_{in} =150 V_{rms}.

and low THD of the PFC pre-regulator's input current (3.46% calculated from the FFT spectrum shown in Fig. 2.29) are unaffected by a significant change in output capacitance.

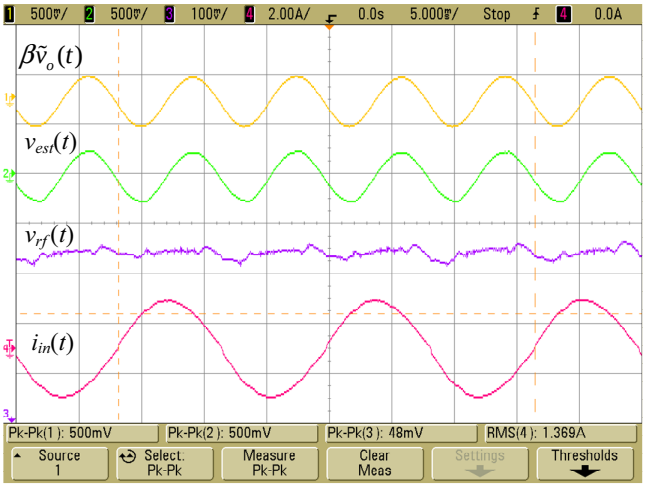


Figure 2.25: Input and output waveforms of difference amplifier at V_{in} =150 V_{rms} ($\beta\tilde{v}_o(t)$: sampled output voltage ripple, $v_{est}(t)$: estimated output voltage ripple, $v_{rf}(t)$: output of difference amplifier, $i_{in}(t)$: input or line current).

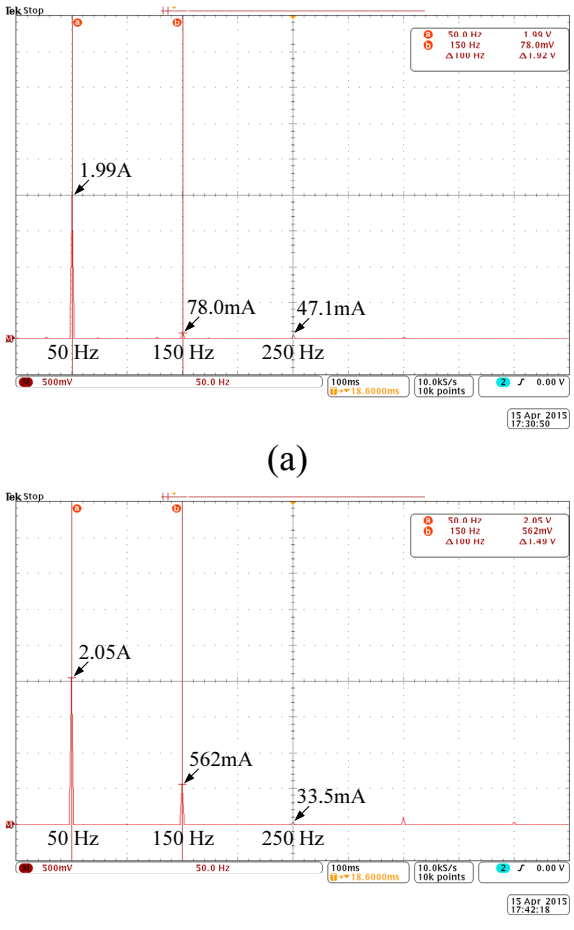


Figure 2.26: FFT spectra of the input current of boost PFC pre-regulator prototype (a) with and (b) without ripple estimation/cancellation at f_{line} =50 Hz.

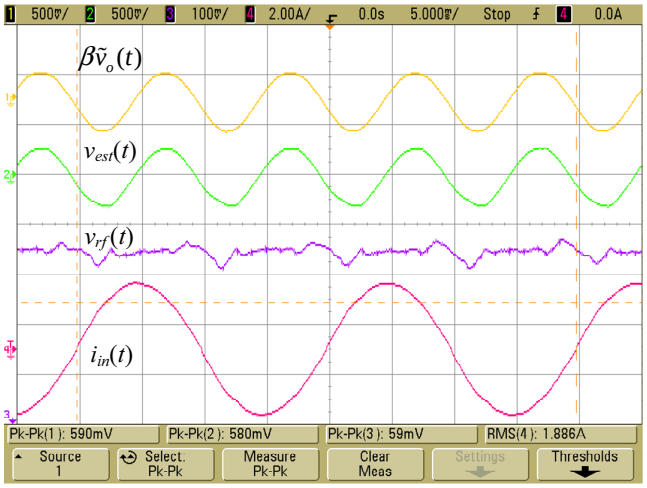


Figure 2.27: Input and output waveforms of difference amplifier at f_{line} =50 Hz ($\beta\tilde{v}_o(t)$: sampled output voltage ripple, $v_{est}(t)$: estimated output voltage ripple, $v_{rf}(t)$: output of difference amplifier, $i_{in}(t)$: input or line current).

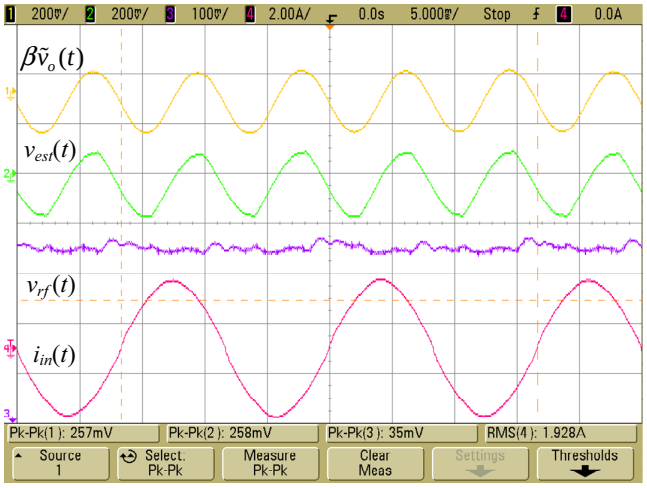


Figure 2.28: Input and output waveforms of difference amplifier at C_o =32 μF ($\beta\tilde{v}_o(t)$: sampled output voltage ripple, $v_{est}(t)$: estimated output voltage ripple, $v_{rf}(t)$: output of difference amplifier, $i_{in}(t)$: input or line current).

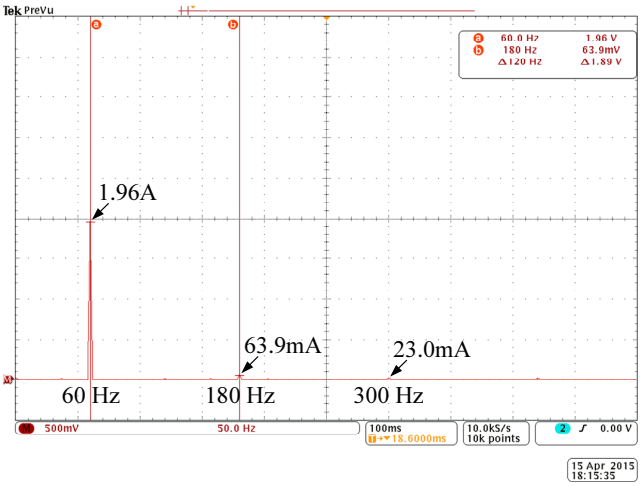


Figure 2.29: FFT spectrum of the input current of boost PFC pre-regulator prototype with ripple estimation/cancellation at C_o =32 μF.

2.6 Conclusion

In this chapter, a ripple-free fast controller for PFC pre-regulator was proposed. The PFC pre-regulator acquires its fast response from a wideband (compared to conventional PFC controller), ripple-free controller enabled by the elimination of the double-line frequency component from the feedback loop by means of ripple estimation/cancellation. In contrary to the previously reported versions of ripple estimation/cancellation circuits, which depend on several fundamental assumptions that inherently limit their accuracy and range of applicability, the proposed one is based on the reproduction of the actual output voltage ripple by tuning the amplitude and phase of a ripple template using switched-resistor circuits. Although the proposed circuit is more complex compared to the basic version reported in [64], this generalized two-step approach enables accurate estimation of the output voltage ripple under a wide range of operating conditions, and its effectiveness was experimentally verified on a 200-W boost PFC pre-regulator under changes in load power, line voltage, line frequency, and output capacitance. It was demonstrated that, when compared to a conventional PFC pre-regulator having the same unity-gain bandwidth, the one implemented with the proposed ripple estimation/cancellation circuit can achieve near-unity power factor while exhibiting fast dynamic response. Finally, integration of the proposed ripple estimation/cancellation circuit with the existing commercial PFC controllers is expected to lead to significantly improved power-factor and dynamic performances at the expense of small additional cost.

Chapter 3

A Ripple Estimation Method Based on Minimum Local Cancellation Error

3.1 Introduction

In Chapter 2, a precise ripple estimation/cancellation circuit that consists of an amplitude tuner and a phase shifter was proposed. The estimated output voltage ripple is capable of tracking the sampled output voltage ripple closely both in magnitude and in phase angle over a wide range of operating conditions. As a result of precise ripple cancellation, both input and output signals of the voltage error amplifier are approaching ripple-free, which leads to near-unity power factor and low THD of input current. Although near-ideal ripple estimation/cancellation is achievable, the proposed ripple estimation network is very complex as it involves many switching components and their control and drive circuitries. In this chapter, attempt will be made to find ways to reduce the complexity of the proposed ripple estimation/cancellation circuit, while maintaining high power factor and fast dynamic response of the PFC pre-regulator.

In this chapter, the figures of merit of PFC pre-regulator implemented with ripple cancellation are first derived in Section 3.2. Based on the results obtained, an equation describing the optimum amplitude of estimated output voltage ripple that leads to minimum local cancellation error is obtained in Section 3.3. In Section 3.4, a new ripple estimation method that tracks the optimum amplitude and minimizes local cancellation error is proposed. Simulation results will be presented in Section 3.5 to verify the operation of the proposed ripple estimation method and its method of implementation. Following this, an experimental prototype is constructed and tested under different operating conditions in Section 3.6 using a 200-W boost PFC pre-regulator as power stage. Finally, conclusion is given in Section 3.7.

3.2 Derivation of Main Figures of Merit of PFC Pre-regulator with Ripple Cancellation

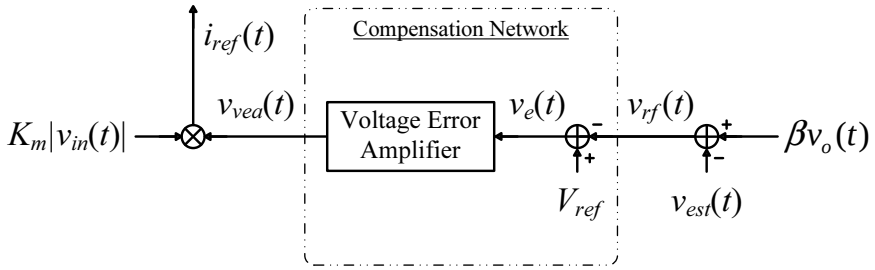


Figure 3.1: Basic configuration of the PFC pre-regulator's outer voltage control loop including ripple estimation/cancellation.

Fig. 3.1 shows the basic configuration of a PFC pre-regulator's outer-voltage control loop including ripple estimation/cancellation, where $\beta v_o(t)$ and $v_{est}(t)$ is the sampled output voltage and the estimated output voltage ripple, respectively. In the voltage control loop, the estimated output voltage ripple $v_{est}(t)$ is first subtracted from the sampled output voltage $\beta v_o(t)$ in order to produce an (ideally) ripple-free output voltage signal $v_{rf}(t)$. Next, the error voltage,

$v_e(t) = V_{ref} - v_{rf}(t)$, is amplified by the compensation network, and its output voltage $v_{vea}(t)$ is subsequently multiplied by the rectified line voltage template $K_m |v_{in}(t)|$ to obtain the input current reference signal $i_{ref}(t)$, which, essentially, determines the line current waveform.

Assume that the PFC pre-regulator is operating with a unity power factor and its output voltage (with respect to line voltage) contains a dc component and a double-line frequency component, as described by Eq. (3.1), where ω_{line} is the angular line frequency and $\theta_o = \tan^{-1}(\omega_{line} R_o C_o)$ varies in the range of $0^o \leq \theta_o \leq 90^o$. The resulting sampled output voltage $\beta v_o(t)$ is given by Eq. (3.2).

$$\begin{aligned} v_o(t) &= V_o + \tilde{v}_o(t) \\ &= V_o - V_r \cos(2\omega_{line} t - \theta_o) \end{aligned} \tag{3.1}$$

$$\begin{aligned} \beta v_o(t) &= \beta (V_o + \tilde{v}_o(t)) \\ &= \beta V_o - \beta V_r \cos(2\omega_{line} t - \theta_o) \end{aligned} \tag{3.2}$$

where V_o and V_r is the average output voltage and the amplitude of the output voltage ripple, respectively.

Assume that the estimated output voltage ripple has an amplitude of V_{est} and a phase angle of θ_{est}, (with respect to line voltage), it can be written mathematically as

$$v_{est}(t) = -V_{est} \cos(2\omega_{line} t - \theta_{est}) \tag{3.3}$$

where $0^o \leq \theta_{est} \leq 90^o$.

By subtracting the estimated output voltage ripple $v_{est}(t)$ from the sampled output voltage $\beta v_o(t)$, the resultant signal $v_{rf}(t)$ with reduced ripple size, which

constitutes the input of the compensation network, is given by Eq. (3.4).

$$\begin{aligned} v_{rf}(t) &= \beta v_o(t) - v_{est}(t) \\ &= [\beta V_o - \beta V_r \cos(2\omega_{line} t - \theta_o)] - [-V_{est} \cos(2\omega_{line} t - \theta_{est})] \\ &= \begin{cases} \beta V_o + A_1 \cdot \beta V_r \cdot \cos(2\omega_{line} t - \theta_{rf}) & \text{if } \rho > \frac{\cos\theta_o}{\cos\theta_{est}} \\ \beta V_o - A_1 \cdot \beta V_r \cdot \cos(2\omega_{line} t - \theta_{rf}) & \text{if } \rho \leq \frac{\cos\theta_o}{\cos\theta_{est}} \end{cases} \end{aligned} \tag{3.4}$$

where

$$\rho = \frac{V_{est}}{\beta V_r} \tag{3.5}$$

$$A_1 = \sqrt{[\rho - \cos(\theta_{est} - \theta_o)]^2 + \sin^2(\theta_{est} - \theta_o)} \tag{3.6}$$

$$\theta_{rf} = \tan^{-1}\left(\frac{\rho \sin\theta_{est} - \sin\theta_o}{\rho \cos\theta_{est} - \cos\theta_o}\right), \text{ where } -90^o \leq \theta_{rf} \leq 90^o \tag{3.7}$$

Commonly, θ_o is close to 90^o for most PFC pre-regulators with reasonably large output capacitor in order to create a low impedance path for the flow of the double-line frequency component. In fact, this condition is imposed in all existing ripple estimation methods and, therefore, θ_{est} is typically set to be 90^o (i.e. $\theta_{est} = 90^o$) such that the phase difference between the estimated output voltage ripple $v_{est}(t)$ and the sampled output voltage ripple $\beta\tilde{v}_o(t)$ is (ideally) equal to zero, i.e. $(\theta_{est} - \theta_o) \rightarrow (90^o - 90^o) = 0^o$. Based on this assumption, the value of ρ is always less than $\frac{\cos\theta_o}{\cos\theta_{est}}$ and, hence, only the case of $\rho \leq \frac{\cos\theta_o}{\cos\theta_{est}}$ ($\theta_{est} = 90^o$) as given by Eq. (3.4) is considered in the following analysis.

After the subtraction, $v_{rf}(t)$ is further processed by the compensation network, which includes a reference voltage V_{ref} and a voltage error amplifier. Let $G_{2\omega_{line}}$ and $\theta_{2\omega_{line}}$ be the gain and the phase shift introduced by the compensation network at the double-line frequency, respectively, the output signal of the

voltage error amplifier is given by Eq. (3.8).

$$\begin{aligned} v_{vea}(t) &= V_{vea} + \tilde{v}_{vea}(t) \\ &= V_{vea} + G_{2\omega_{line}} \cdot A_1 \cdot \beta V_r \cdot \cos\left(2\omega_{line}t - \theta_{rf} + \theta_{2\omega_{line}}\right) \\ &= V_{vea}\left[1 + \frac{G_{2\omega_{line}} \cdot A_1 \cdot \beta V_r}{V_{vea}} \cos\left(2\omega_{line}t + (\theta_{2\omega_{line}} - \theta_{rf})\right)\right] \end{aligned} \quad (3.8)$$

where V_{vea} is the average value of voltage error amplifier's output signal.

Subsequently, $v_{vea}(t)$ is multiplied by the rectified line voltage template $K_m V_p \left|\sin\left(\omega_{line}t\right)\right|$ to obtain the input (or line) current reference waveform $i_{ref}(t)$, which is given by Eq. (3.9), where K_m is the line-voltage-step-down ratio and V_p is the peak value of the line voltage.

$$i_{ref}(t) = K_m V_p \left|\sin\left(\omega_{line}t\right)\right| V_{vea}\left[1 + \frac{G_{2\omega_{line}} \cdot A_1 \cdot \beta V_r}{V_{vea}} \cos\left(2\omega_{line}t + (\theta_{2\omega_{line}} - \theta_{rf})\right)\right] \quad (3.9)$$

The input current reference waveform $i_{ref}(t)$ is then compared with the sensed inductor current $i_L(t)R_s$ through the inner current control loop, where $i_L(t)$ and R_s is the inductor current and inductor current sensing resistor, respectively. As the bandwidth of the inner current loop is typically large, the sensed inductor current is assumed to closely track the input current reference waveform, i.e. $i_L(t)R_s = i_{ref}(t)$. Hence, the switching-cycle-averaged inductor current is given by

$$i_L(t) = \frac{K_m V_p V_{vea}}{R_s} \left|\sin\left(\omega_{line}t\right)\right| \left[1 + \frac{G_{2\omega_{line}} \cdot A_1 \cdot \beta V_r}{V_{vea}} \cos\left(2\omega_{line}t + (\theta_{2\omega_{line}} - \theta_{rf})\right)\right] \quad (3.10)$$

Since the inductor current is equal to the rectified input current, the input

current waveform can be obtained as follows.

$$\begin{aligned} i_{in}(t) &= \frac{K_m V_p V_{vea}}{R_s} \sin(\omega_{line} t) \left[1 + \frac{G_{2\omega_{line}} \cdot A_1 \cdot \beta V_r}{V_{vea}} \cos(2\omega_{line} t + (\theta_{2\omega_{line}} - \theta_{rf})) \right] \\ &= i_{in1}(t) + i_{in3}(t) \end{aligned} \tag{3.11}$$

where

$$\begin{aligned} i_{in1}(t) &= \frac{K_m V_p V_{vea}}{R_s} \sqrt{1 - (k_1 A_1) \cos(\theta_{2\omega_{line}} - \theta_{rf}) + \left(\frac{k_1 A_1}{2} \right)^2} \\ &\quad \sin\left[\omega_{line} t - \tan^{-1} \left(\frac{k_1 A_1 \sin(\theta_{2\omega_{line}} - \theta_{rf})}{2 - k_1 A_1 \cos(\theta_{2\omega_{line}} - \theta_{rf})} \right) \right] \end{aligned} \tag{3.12}$$

$$i_{in3}(t) = \frac{K_m V_p V_{vea}}{R_s} \left(\frac{k_1 A_1}{2} \right) \sin(3\omega_{line} t + (\theta_{2\omega_{line}} - \theta_{rf})) \tag{3.13}$$

and

$$k_1 = \frac{G_{2\omega_{line}} \beta V_r}{V_{vea}} \tag{3.14}$$

By using Eq. (3.11)–Eq. (3.14), the total harmonic distortion (THD) of the input current and power factor (PF) of the PFC pre-regulator can be derived as given by Eq. (3.15) and Eq. (3.16), respectively. The total harmonic distortion (THD) and power factor (PF) are plotted as a function of $(\theta_{2\omega_{line}} - \theta_{rf})$ with $k_1 A_1$ as parameter in Fig. 3.2 and Fig. 3.3, respectively. Assuming that PI-controller is chosen for the compensation network of the voltage control loop, and since $\theta_{2\omega_{line}}$ ranges from -90^o to 0^o, the resultant phase angle $(\theta_{2\omega_{line}} - \theta_{rf})$ is bounded by -180^o and 90^o.

$$\text{THD} = \frac{k_1 A_1}{\sqrt{4 - 4(k_1 A_1) \cos(\theta_{2\omega_{line}} - \theta_{rf}) + (k_1 A_1)^2}} \tag{3.15}$$

$$\text{PF} = \frac{\sqrt{2}\,(1 - 0.5\,(k_1 A_1) \cos(\theta_{2\omega_{line}} - \theta_{rf}))}{\sqrt{2 + (k_1 A_1)^2 - 2\,(k_1 A_1) \cos(\theta_{2\omega_{line}} - \theta_{rf})}} \tag{3.16}$$

From Eq. (3.15) and Eq. (3.16), it can be seen that both THD and PF are related to the values of k_1, A_1, $\theta_{2\omega_{line}}$ and θ_{rf}. However, as depicted in Fig. 3.2 and Fig. 3.3, it can be observed that when the resultant value of k_1A_1 is small, a small total harmonic distortion as well as a high power factor are obtained. In other words, they imply that small values of the product k_1A_1 are desirable for achieving high power factor.

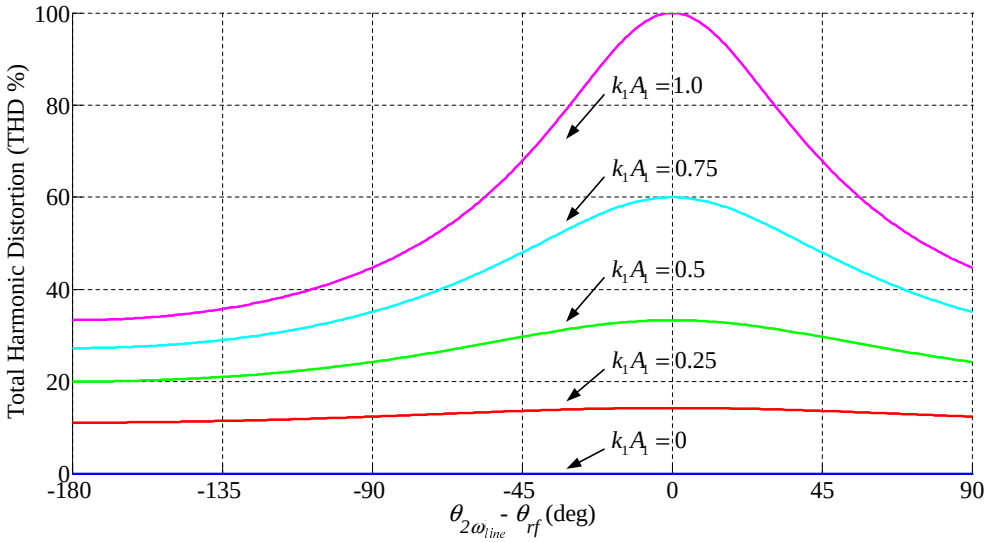


Figure 3.2: Total harmonic distortion (THD %) versus $(\theta_{2\omega_{line}} - \theta_{rf})$ with different values of k_1A_1.

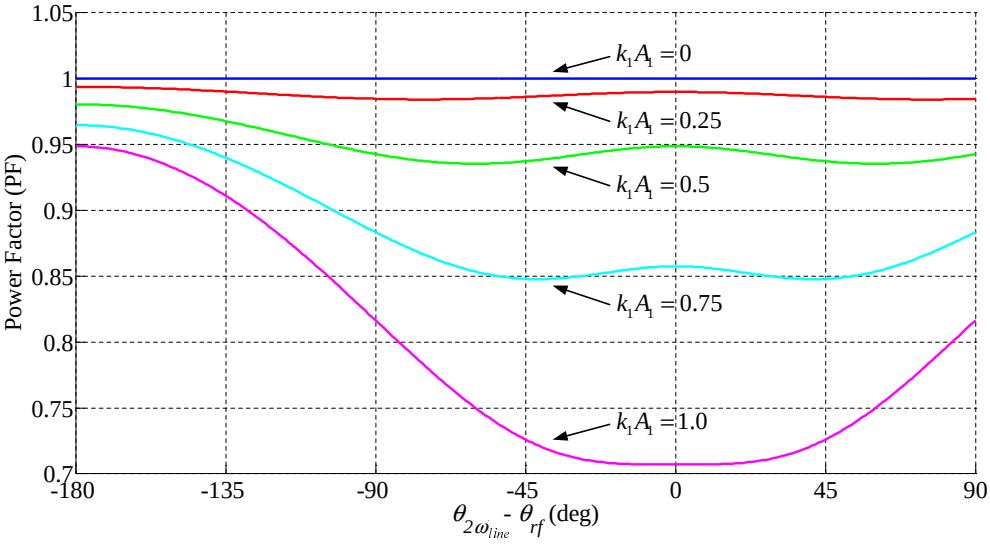


Figure 3.3: Power factor (PF) versus $(\theta_{2\omega_{line}} - \theta_{rf})$ with different values of k_1A_1.

3.3 Optimum Amplitude of Estimated Output Voltage Ripple in the Presence of Phase Estimation Error

As discussed in the previous section, in order to achieve a high power factor, it is necessary to minimize the value of the product $k_1 A_1$. However, from Eq. (3.14), it can be observed that k_1 is directly proportional to $G_{2\omega_{line}}$, which is related to the closed-loop bandwidth of the PFC pre-regulator. This implies that when the bandwidth of the PFC pre-regulator is extended for improved dynamic response, k_1 will also be increased accordingly. In this case, A_1 should be minimized in order to reduce the value of the product $k_1 A_1$ as much as possible so that both fast dynamic response and high power factor can be accomplished simultaneously.

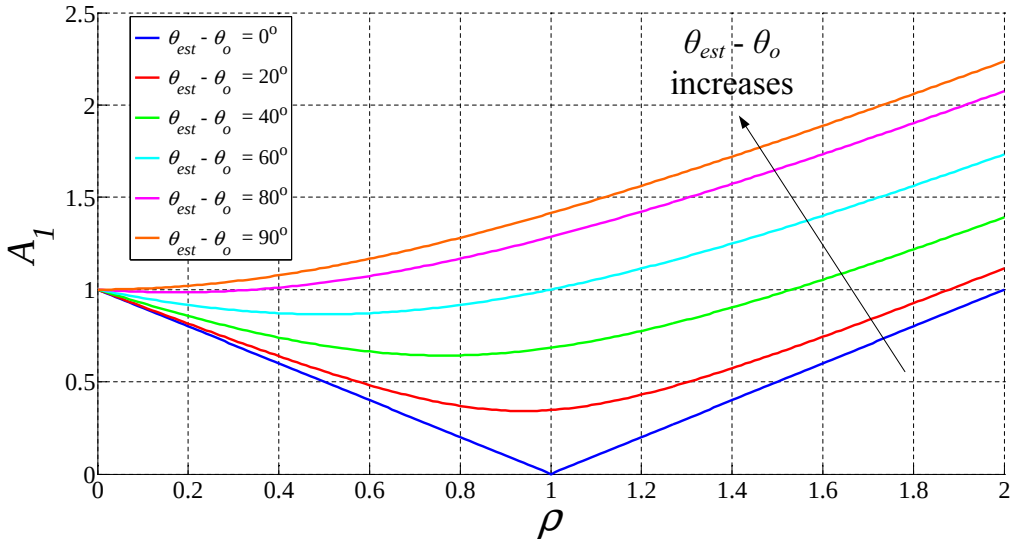


Figure 3.4: Plot of A_1 versus ρ, where $\rho = V_{est}/\beta V_r$.

Recall that A_1 is a function of ρ and the phase difference between θ_{est} and θ_o as given by Eq. (3.17). A graphical representation of A_1 plotted against ρ for different values of $(\theta_{est} - \theta_o)$ is shown in Fig. 3.4. By differentiating A_1 with respect to ρ, as is done in Eq. (3.18), it can be solved that A_1 is at its minimum value when $\rho = \cos(\theta_{est} - \theta_o)$, which gives $A_1 = \sin(\theta_{est} - \theta_o)$ as given by Eq. (3.19).

$$A_1 = \sqrt{\left[\rho - \cos\left(\theta_{est} - \theta_o\right)\right]^2 + \sin^2\left(\theta_{est} - \theta_o\right)} \tag{3.17}$$

$$\frac{dA_1}{d\rho} = \frac{\rho - \cos\left(\theta_{est} - \theta_o\right)}{\sqrt{\rho^2 - 2\rho\cos\left(\theta_{est} - \theta_o\right) + 1}} = 0 \tag{3.18}$$

$$\begin{aligned} \left\|A_{1(min)}\right\| &= \sqrt{\left[\left(\cos\left(\theta_{est} - \theta_o\right)\right) - \cos\left(\theta_{est} - \theta_o\right)\right]^2 + \sin^2\left(\theta_{est} - \theta_o\right)} \\ &= \sqrt{\sin^2\left(\theta_{est} - \theta_o\right)} \\ &= \left|\sin\left(\theta_{est} - \theta_o\right)\right| \end{aligned} \tag{3.19}$$

Since $\rho = V_{est}/\beta V_r$, it can be deduced that, when $\theta_{est} \neq \theta_o$, the estimated output voltage ripple $v_{est}(t)$ should have an amplitude of $\beta V_r \cos\left(\theta_{est} - \theta_o\right)$, i.e. $V_{est} = \beta V_r \cos\left(\theta_{est} - \theta_o\right)$, in order to achieve minimum A_1. The overall estimated output voltage ripple that results in minimum A_1 is given by Eq. (3.20).

$$v_{est}(t) = -\left[\beta V_r \cos\left(\theta_{est} - \theta_o\right)\right] \cos\left(2\omega_{line}t - \theta_{est}\right) \tag{3.20}$$

Eq. (3.20) serves as the basis for an alternative ripple estimation method that results in minimum cancellation error when the phase estimation is non-zero. The idea is to eliminate the use of phase shifter, as in done in Chapter 2, and hence gives rise to a simplified ripple estimation circuit. A more detailed description of the proposed ripple estimation method and its implementation is given in the next section.

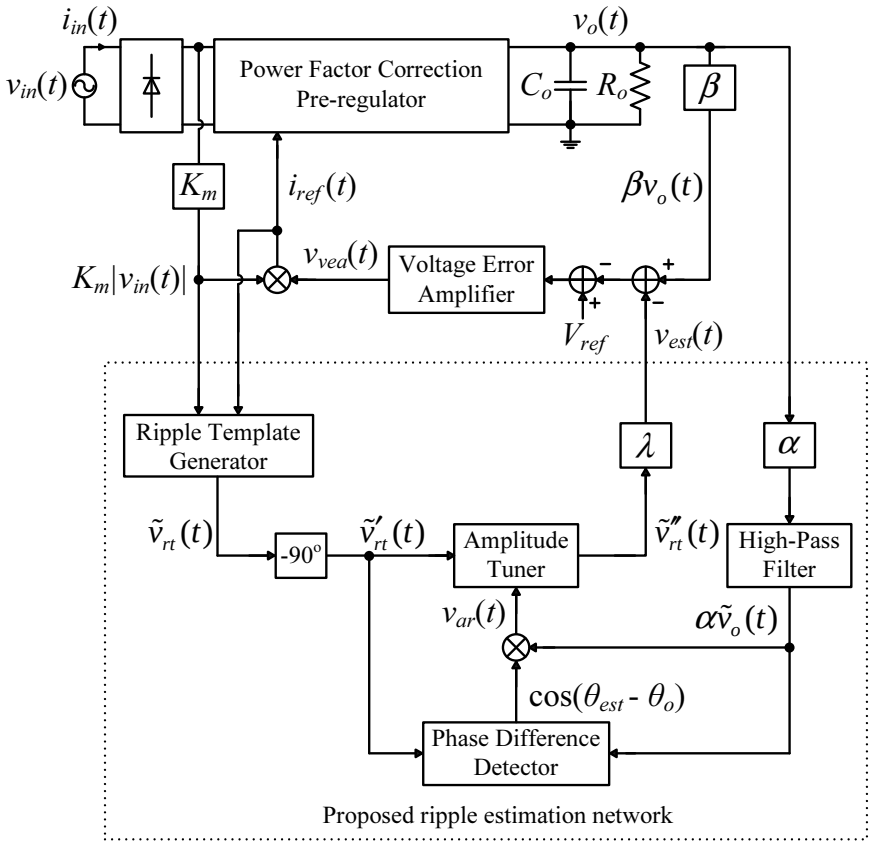


Figure 3.5: PFC pre-regulator system with proposed ripple estimation circuit.

3.4 Ripple Estimation Based on Minimum Local Cancellation Error and Its Implementation

Fig. 3.5 shows the block diagram of a general PFC pre-regulator implemented with the proposed ripple estimation/cancellation circuit. An unmodified ripple template $\tilde{v}_{rt}(t)$ is obtained by the ripple template generator, which multiplies the stepped-down rectified line voltage $K_m\,|v_{in}(t)|$ and the input current reference signal $i_{ref}(t)$, followed by high-pass filtering that removes the dc component. Assuming that unity power factor is achieved, these two signals can be written as $K_m V_p\,|\sin(\omega_{line}t)|$ and $I_p\,|\sin(\omega_{line}t)|\,R_s$, respectively, where I_p is the peak value of the PFC pre-regulator's input current. Thus, the ripple template $\tilde{v}_{rt}(t)$ is

generated by the process described by Eq. (3.21).

$$\begin{aligned} & [G_1 K_m \left|v_{in}(t)\right|] \cdot [G_2 i_{ref}(t)] \\ = \; & [G_1 K_m V_p \left|\sin(\omega_{line} t)\right|] \cdot [G_2 I_p \left|\sin(\omega_{line} t)\right| R_s] \\ = \; & V_{rt}(1 - \cos(2\omega_{line} t)) \\ \xrightarrow{\text{HPF}} \tilde{v}_{rt}(t) = \; & -V_{rt} \cos\left(2\omega_{line} t\right) \end{aligned} \tag{3.21}$$

where G_1 and G_2 is the amplification gain for $K_m \left|v_{in}(t)\right|$ and $i_{ref}(t)$, respectively, and $V_{rt} = P_{in} K_m R_s G_1 G_2$.

As discussed earlier, the output voltage ripple of PFC pre-regulators has a typical phase shift that approaches 90° in the presence of a reasonably large output capacitor, a condition that is generally met by PFC pre-regulators for achieving small output voltage ripple size. Hence, in the proposed ripple estimation method, the ripple template $\tilde{v}_{rt}(t)$ is constantly shifted by 90° and the phase-shifted ripple template $\tilde{v}'_{rt}(t)$ is given by Eq. (3.22).

$$\tilde{v}'_{rt}(t) = -V_{rt} \cos\left(2\omega_{line} t - 90^{\circ}\right) \tag{3.22}$$

The phase-shifted ripple template $\tilde{v}'_{rt}(t)$ is then fed into the amplitude tuner, which will equalize the amplitude of the phase-shifted ripple template $\tilde{v}'_{rt}(t)$ with that of the reference signal $v_{ar}(t)$. According to Eq. (3.20), the amplitude of the estimated output voltage ripple should be made proportional to $\cos\left(\theta_{est} - \theta_o\right)$, which in turn is related to the phase difference between the estimated and sampled (actual) output voltage ripple, i.e. $(\theta_{est} - \theta_o)$. The rest of this section describes the method to obtain $(\theta_{est} - \theta_o)$ from the output voltage ripple. The output voltage ripple is first sampled from the PFC pre-regulator's output with a sampling gain of α followed by high-pass filtering. The sampled output voltage ripple is

given by Eq. (3.23).

$$\begin{aligned} \alpha v_o(t) &= \alpha V_o - \alpha V_r \cos\left(2\omega_{line}t - \theta_o\right) \\ \xrightarrow{\text{HPF}} \alpha \tilde{v}_o(t) &= -\alpha V_r \cos\left(2\omega_{line}t - \theta_o\right) \end{aligned} \tag{3.23}$$

Next, the sampled output voltage ripple $\alpha\tilde{v}_o(t)$ and the phase-shifted ripple template $\tilde{v}'_{rt}(t)$ are passed to the phase difference detector, which generates the phase difference signal and the value of $\cos\left(\theta_{est} - \theta_o\right)$. The output of the phase difference detector, i.e. $\cos\left(\theta_{est} - \theta_o\right)$, is multiplied by the sampled output voltage ripple $\alpha\tilde{v}_o(t)$ to obtain the reference signal for the amplitude tuner, as given by Eq. (3.24).

$$v_{ar}(t) = -\alpha V_r \cos\left(\theta_{est} - \theta_o\right) \cos\left(2\omega_{line}t - \theta_o\right) \tag{3.24}$$

By modifying the amplitude of the phase-shifted ripple template $\tilde{v}'_{rt}(t)$ through the action of the amplitude tuner, it $(\tilde{v}''_{rt}(t))$ will acquire the same amplitude as the reference signal $v_{ar}(t)$, i.e. $|\tilde{v}''_{rt}(t)| = \alpha V_r \cos\left(\theta_{est} - \theta_o\right)$. Considering that θ_{est} equals to 90^o as discussed earlier, the output signal of the amplitude tuner is therefore given by Eq. (3.25).

$$\tilde{v}''_{rt}(t) = -\alpha V_r \cos\left(90^o - \theta_o\right) \cos\left(2\omega_{line}t - 90^o\right) \tag{3.25}$$

Finally, due to the difference between the sampling ratios α and β, as illustrated in Fig. 3.5, the output signal of the amplitude tuner $\tilde{v}''_{rt}(t)$ is adjusted by a gain of $\lambda = \beta/\alpha$ before it is subtracted from the sampled output voltage $\beta v_o(t)$.

3.4.1 Phase Difference Detector

The schematic diagram of the proposed phase difference detector is shown in Fig. 3.6. It is used to detect and generate a signal that represents the phase

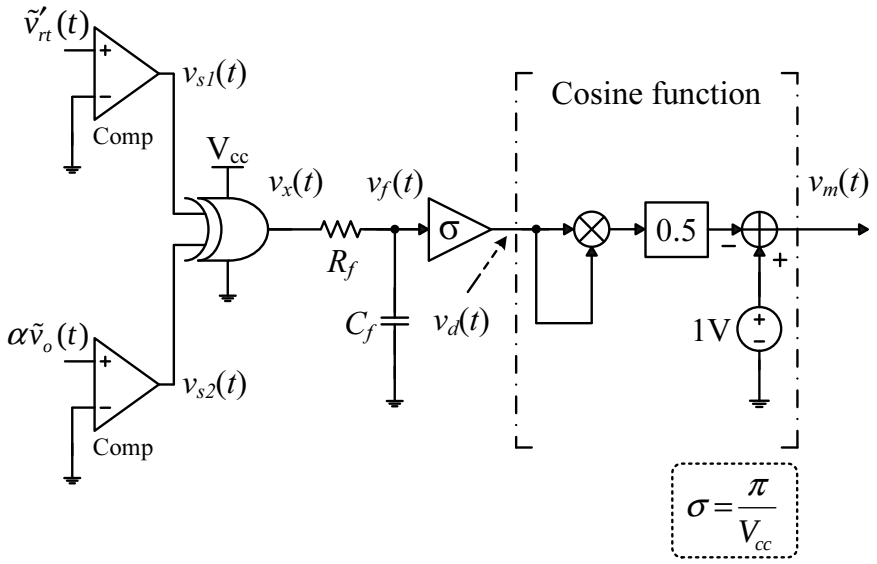


Figure 3.6: Schematic diagram of the proposed phase difference detector.

difference between the phase-shifted ripple template $\tilde{v}'_{rt}(t)$ and the sampled output voltage ripple $\alpha\tilde{v}_o(t)$, and subsequently approximates the cosine value of the phase difference. The key operating waveforms of the phase difference detector are depicted in Fig. 3.7.

The operation of the phase difference detector is described as follows. It takes the two input signals, $\tilde{v}'_{rt}(t)$ and $\alpha\tilde{v}_o(t)$, and compares them individually with 0 V to detect the zero crossing points (ZCP) of each signal. By comparing the comparator's output signals, $v_{s1}(t)$ and $v_{s2}(t)$, through an exclusive-or (XOR) gate, the phase difference between $\tilde{v}'_{rt}(t)$ and $\alpha\tilde{v}_o(t)$, i.e. $\theta_p = \theta_{est} - \theta_o$, is reflected by the duty cycle of the XOR-gate's output signal $v_x(t)$. The sequence of actions described are shown in Fig. 3.7(c)–(e).

Recall that the objective of the phase difference detector is to calculate the cosine value of the phase difference between the input signals, i.e. $\tilde{v}'_{rt}(t)$ and $\alpha\tilde{v}_o(t)$. This is achieved by adding a low-pass filter ($R_f - C_f$) and a gain stage of σ to convert the phase difference information from duty cycle to radian, and subsequently use the result to approximate its cosine value, i.e. $v_m(t) = \cos(v_d(t))$, where $v_m(t)$ is the output signal of the phase difference detector. Considering

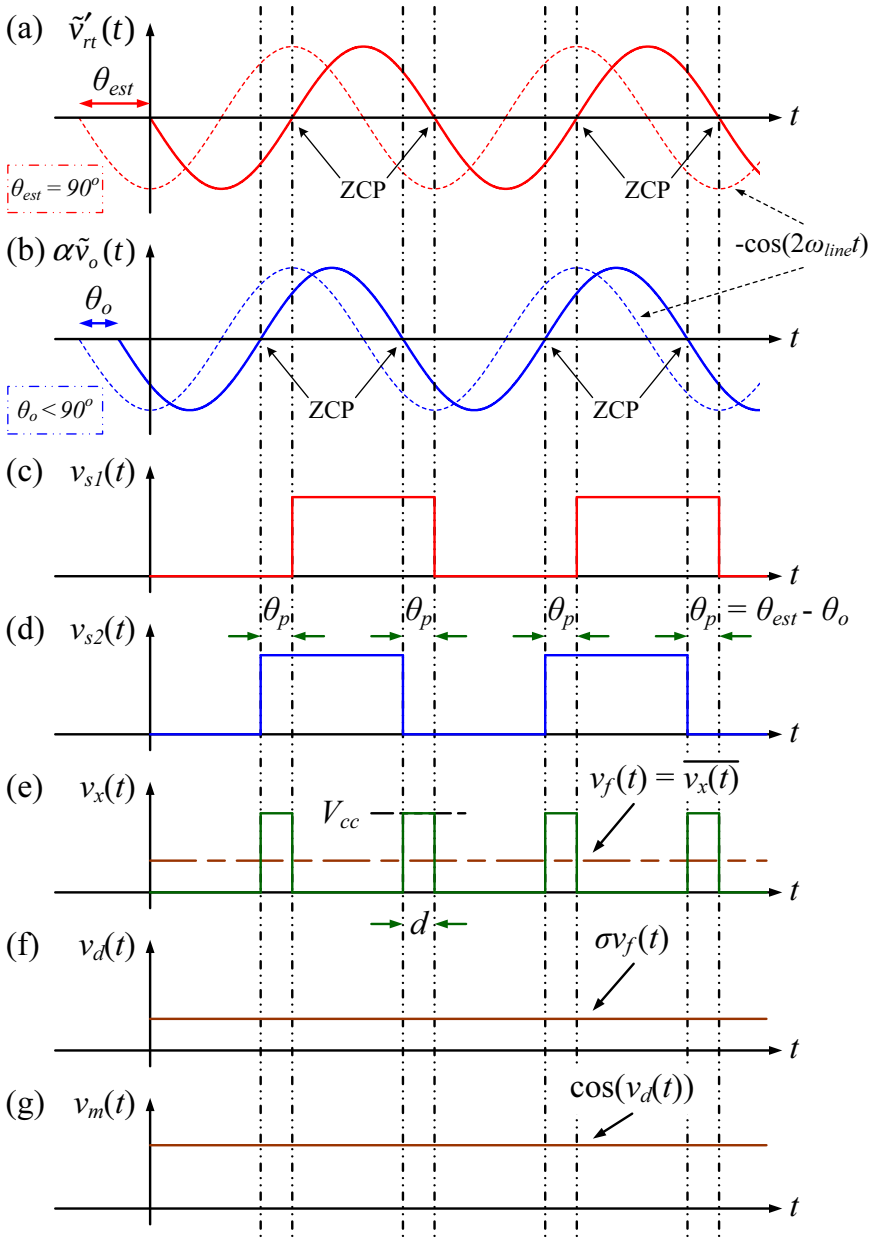


Figure 3.7: Operating waveforms of the proposed phase difference detector.

that $(\theta_{est} - \theta_o)$ is usually small, as $\theta_o \rightarrow 90^o$ for reasonably large output capacitor, the cosine function can realized using small-angle approximation, as given by Eq. (3.26), in order to realize it using analog circuit.

$$\cos(\phi) \approx 1 - \frac{\phi^2}{2} \tag{3.26}$$

where ϕ is in radian.

Finally, the output signal of the phase difference detector $v_m(t)$ is multiplied by the sampled output voltage ripple $\alpha\tilde{v}_o(t)$ to generate the reference signal for the amplitude tuner $v_{ar}(t)$, as described by Eq. (3.27).

$$\begin{aligned} v_{ar}(t) &= v_m(t) \cdot \alpha\tilde{v}_o(t) \\ &= [\cos(\theta_{est} - \theta_o)] \cdot [-\alpha V_r \cos(2\omega_{line}t - \theta_o)] \\ &= -\alpha V_r \cos(\theta_{est} - \theta_o)\cos(2\omega_{line}t - \theta_o) \end{aligned} \tag{3.27}$$

3.4.2 Amplitude Tuner

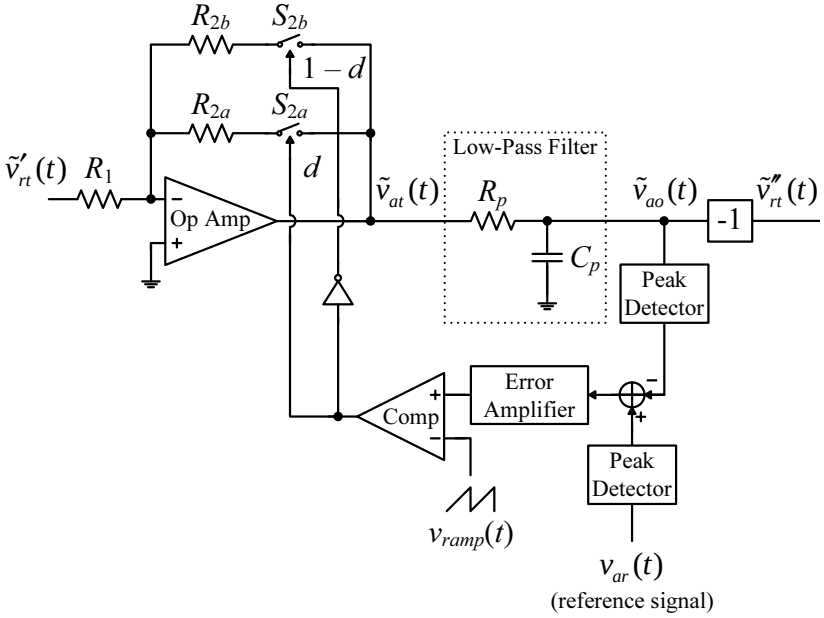


Figure 3.8: Schematic diagram of the proposed amplitude tuner.

By using $v_{ar}(t)$ as the reference signal, the phase-shifted ripple template $\tilde{v}'_{rt}(t)$ is modified in amplitude through the action of the amplitude tuner. The schematic diagram of the amplitude tuner is shown in Fig. 3.8. It is essentially an inverting amplifier with an adjustable gain as determined by the amplitude difference between $\tilde{v}'_{rt}(t)$ and $v_{ar}(t)$. To realize an electronically adjustable gain, the fixed feedback resistance used in a conventional inverting amplifier is replaced by two resistors R_{2a} and R_{2b}, each connected in series with a switch having a turn-on

time of dT_s and $(1-d)\,T_s$, respectively, where d is the duty cycle of switch S_{2a} and $1/T_s$ is the switching frequency. The output signal of the inverting amplifier $\tilde{v}_{at}(t)$ is then smoothed by a low-pass filter $(R_p - C_p)$ (having a cut-off frequency that is much lower than the switching frequency but higher than the double-line frequency) to obtain an amplitude-modified version of the phase-shifted ripple template. By the principle of duty-cycle averaging, the average voltage gain of the inverting amplifier $H_v(d)$ is given by

$$H_v(d) = -\frac{R_2(d)}{R_1} \tag{3.28}$$

$$R_2(d) = dR_{2a} + (1-d)\,R_{2b} \tag{3.29}$$

At steady state, the amplitude of the modified ripple template $\tilde{v}_{ao}(t)$ is equal to that of the reference signal $v_{ar}(t)$, i.e. $|\tilde{v}_{ao}(t)| = \alpha V_r \cos(\theta_{est} - \theta_o)$, while its phase is inverted compared to its input signal $\tilde{v}'_{rt}(t)$. Recall that $\tilde{v}'_{rt}(t) = -V_{rt}\cos(2\omega_{line}t - 90^{\text{o}})$. The filtered amplitude-tuned ripple template is therefore given by Eq. (3.30).

$$\begin{aligned} \tilde{v}_{ao}(t) \quad &= \quad \alpha V_r \cos(\theta_{est} - \theta_o)\cos(2\omega_{line}t - 90^{\text{o}}) \\ &\xrightarrow{\theta_{est}=90^{\text{o}}} \quad \alpha V_r \cos(90^{\text{o}} - \theta_o)\cos(2\omega_{line}t - 90^{\text{o}}) \end{aligned} \tag{3.30}$$

In order to provide the required phase inversion, a unity-gain inverting amplifier is added after the low-pass filter. The result, as given by Eq. (3.31), is the desired estimated output voltage ripple signal given by Eq. (3.20), except for a difference in gain, i.e. α vs β.

$$\tilde{v}''_{rt}(t) = -\alpha V_r \cos(90^{\text{o}} - \theta_o)\cos(2\omega_{line}t - 90^{\text{o}}) \tag{3.31}$$

To account for this difference in gain, the output signal of the amplitude tuner $\tilde{v}''_{rt}(t)$ is modified by a gain of $\lambda = \beta/\alpha$ before it is subtracted from the sampled output voltage $\beta v_o(t)$. This produces the estimated output voltage ripple $v_{est}(t)$ as given by Eq. (3.32), which agrees with Eq. (3.20).

$$\begin{aligned} v_{est}(t) &= \left(\frac{\beta}{\alpha}\right) \cdot \tilde{v}''_{rt}(t) \\ &= \left(\frac{\beta}{\alpha}\right) \cdot [-\alpha V_r \cos(90^{\text{o}} - \theta_o) \cos(2\omega_{line} t - 90^{\text{o}})] \\ &= -\beta V_r \cos(90^{\text{o}} - \theta_o) \cos(2\omega_{line} t - 90^{\text{o}}) \end{aligned} \tag{3.32}$$

3.5 Simulation Results

In this section, the proposed ripple estimation/cancellation circuit, which mainly consists of a constant-90$^{\text{o}}$ phase-shifter, an amplitude tuner and a phase difference detector, is simulated with a 200-W boost PFC pre-regulator as power stage. The nominal input voltage is 110-Vrms/60-Hz, while the boost inductor and the output capacitor is 1 mH and 16 μF, respectively. The loop gain crossover frequency of the PFC pre-regulator is configured to be 60 Hz.

Fig. 3.9(a) and Fig. 3.9(b) shows the simulated (i) output voltages, (ii) scaled-down input voltages and input currents, and (iii) voltage error amplifier's output signals of PFC pre-regulators with and without ripple estimation/cancellation, respectively, operating under nominal conditions. The average output voltages of both PFC pre-regulators are 400 Vdc. With the aid of the proposed ripple estimation/cancellation circuit, it can be seen that the amplitude of the ripple component in the voltage error amplifier's output signal $v_{vea}(t)$ is reduced, which leads to a near-sinusoidal input current waveform.

The simulated operating waveforms of the phase difference detector are shown in Fig. 3.10. A ripple template $\tilde{v}_{rt}(t)$ with an initial amplitude of 2.5 V_{pp} is

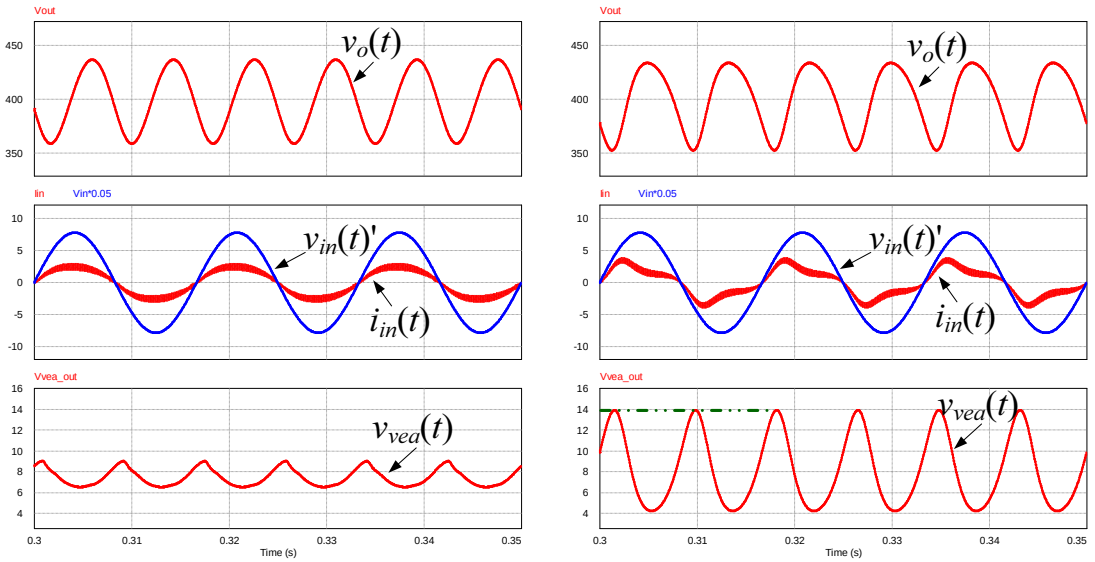


Figure 3.9: Simulated input and output waveforms of boost PFC pre-regulator (a) with and (b) without ripple estimation/cancellation under nominal operating conditions ($v_o(t)$: output voltage, $v_{in}(t)'$: scaled-down input or line voltage, $i_{in}(t)$: input or line current, $v_{vea}(t)$: output signal of voltage error amplifier).

first shifted by 90° to form a phase-shifted ripple template $\tilde{v}'_{rt}(t)$ as shown in Fig. 3.10(a). Through the actions of the comparators and an XOR gate, the phase difference between $\tilde{v}'_{rt}(t)$ and $\alpha\tilde{v}_o(t)$ is reflected by the duty cycle of the XOR gate's output signal $v_x(t)$. By measuring its duty cycle as indicated in Fig. 3.10(c), it can be calculated that the (average) phase difference between the phase-shifted ripple template and the sampled output voltage ripple is approximately 13°, i.e. $\theta_{est} - \theta_o = 13°$. Using the small-angle approximation circuit, its cosine value is calculated to be 0.975, which matches the average value of the phase difference detector's output signal $v_m(t)$ as shown in Fig. 3.10(d).

The output signal of the phase difference detector $v_m(t)$ is then multiplied by the sampled output voltage ripple $\alpha\tilde{v}_o(t)$ to obtain the reference signal for the amplitude tuner $v_{ar}(t)$, which has a peak-to-peak voltage of 5.40 V_{pp} as shown in Fig. 3.11(d). From Fig. 3.11(a)–(c), it can be seen that the phase-shifted ripple template $\tilde{v}'_{rt}(t)$ is modified in amplitude such that the filtered amplitude-tuned

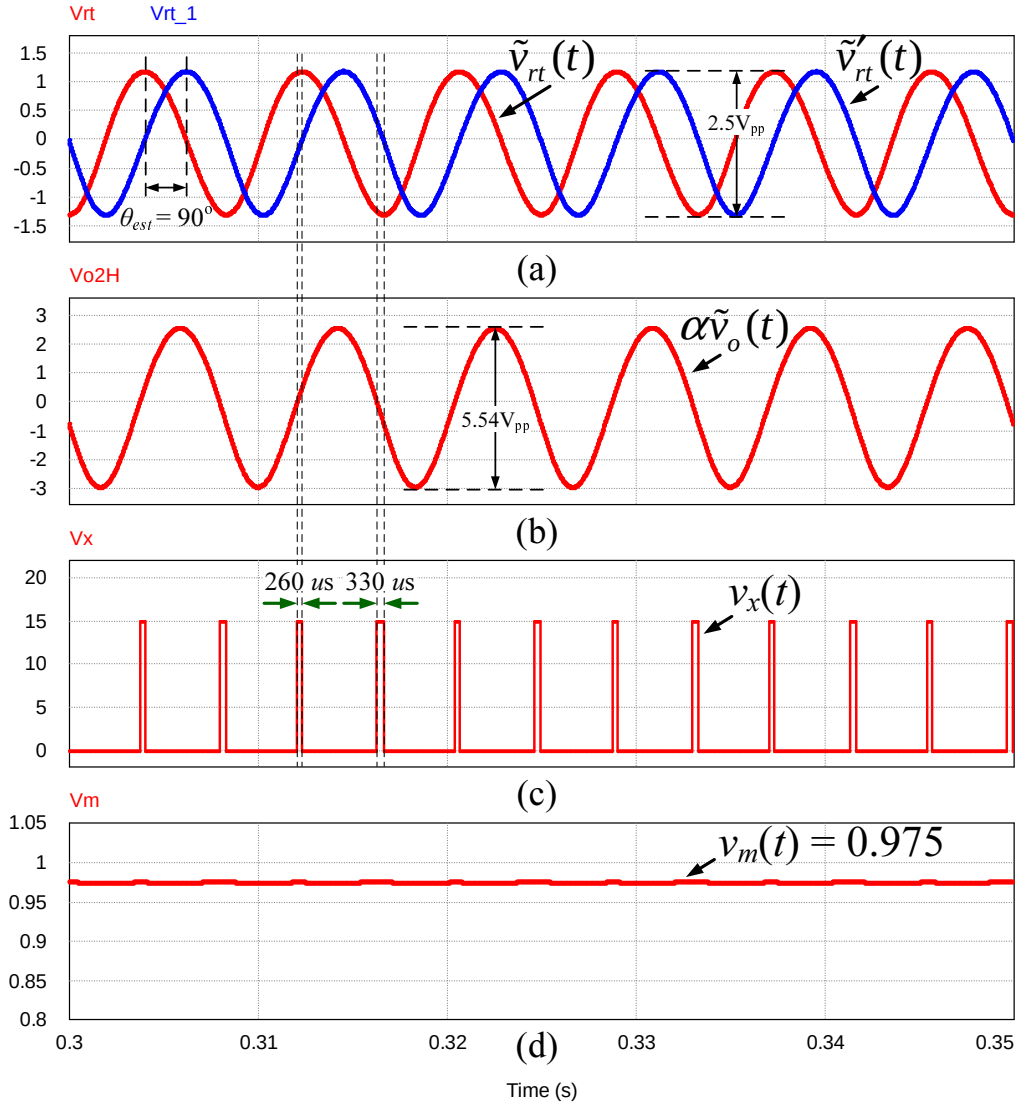


Figure 3.10: Simulated operating waveforms of phase difference detector ((a) $\tilde{v}_{rt}(t)$: unmodified ripple template, $\tilde{v}'_{rt}(t)$: phase-shifted ripple template, (b) $\alpha\tilde{v}_o(t)$: sampled output voltage ripple, (c) $v_x(t)$: exclusive-OR (XOR) gate's output signal, (d) $v_m(t)$: phase difference detector's output signal).

ripple template $\tilde{v}_{ao}(t)$ and the reference signal $\tilde{v}_{ar}(t)$ are nearly equal in amplitude. However, since $\tilde{v}_{ao}(t)$ is out of phase with $\tilde{v}_{ar}(t)$ (as well as the sampled output voltage ripple $\alpha\tilde{v}_o(t)$), $\tilde{v}_{ao}(t)$ is subsequently inverted by a unity-gain inverting amplifier and the resultant signal $\tilde{v}''_{rt}(t)$ is shown in Fig. 3.11(c).

After the amplitude tuner, its output signal $\tilde{v}''_{rt}(t)$ is stepped down by a factor of λ due to the difference in sampling ratios (α and β) before it is subtracted from the sampled output voltage $\beta v_o(t)$ using a difference amplifier, as shown in

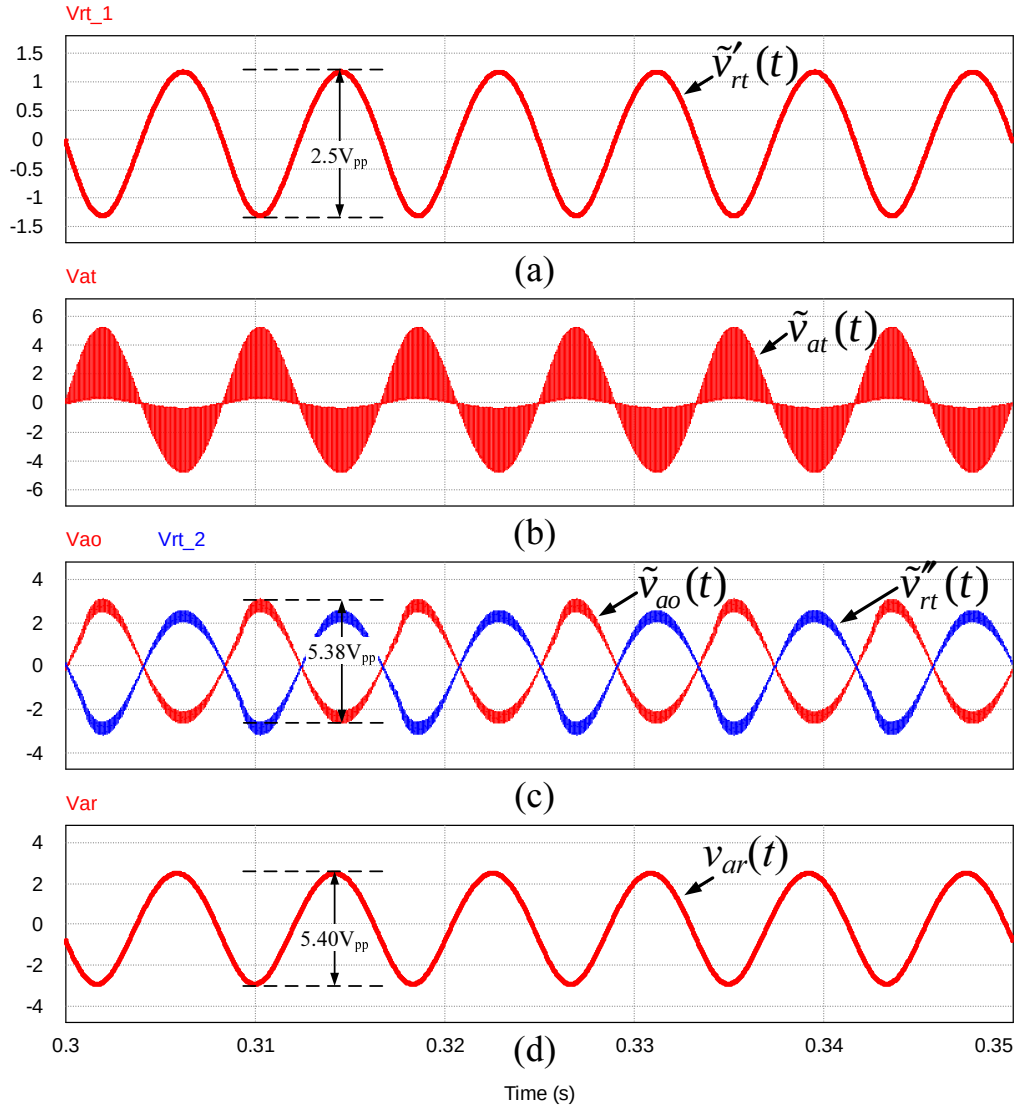


Figure 3.11: Simulated operating waveforms of amplitude tuner ((a) $\tilde{v}'_{rt}(t)$: phase-shifted ripple template, (b) $\tilde{v}_{at}(t)$: unfiltered amplitude-tuned ripple template, (c) $\tilde{v}_{ao}(t)$: filtered amplitude-tuned ripple template, $\tilde{v}''_{rt}(t)$: inverted filtered amplitude-tuned ripple template, (d) $v_{ar}(t)$: reference signal for the amplitude tuner).

Fig. 3.12. Recall that the phase difference between the sampled output voltage ripple and the phase-shifted ripple template (as well as the output signal of amplitude tuner $\tilde{v}''_{rt}(t)$) is 13°, i.e. $\theta_{est} - \theta_o = 13°$. By comparing the amplitude of both the sampled output voltage ripple $\beta\tilde{v}_o(t)$ and the estimated output voltage ripple $v_{est}(t)$, as shown in Fig. 3.12(a) and Fig. 3.12(b), respectively, it can be deduced that the estimated output voltage ripple $v_{est}(t)$ is operating with an amplitude

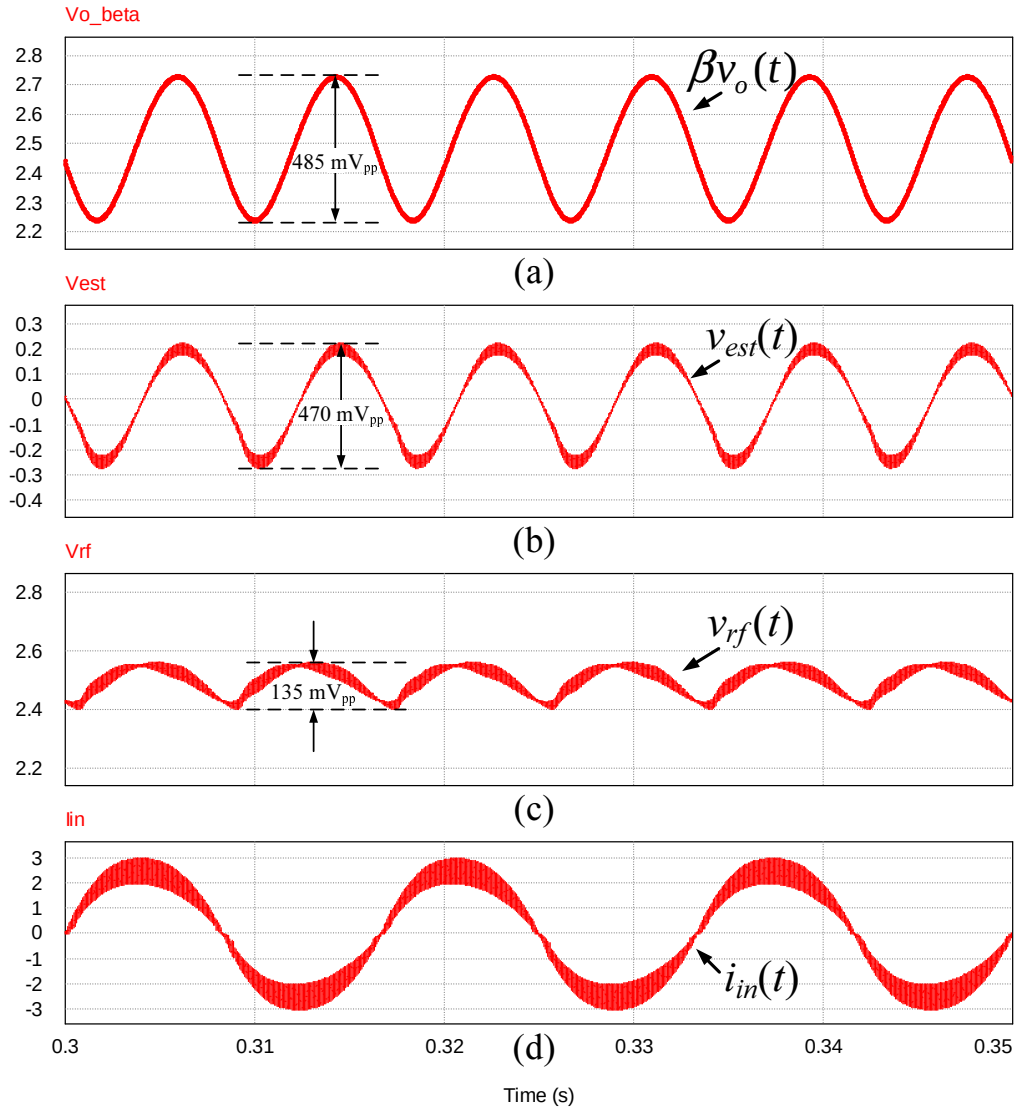


Figure 3.12: Simulated input and output waveforms of difference amplifier ((a) $\beta v_o(t)$: sampled output voltage, (b) $v_{est}(t)$: estimated output voltage ripple, (c) $v_{rf}(t)$: difference amplifier's output signal, (d) $i_{in}(t)$: input or line current).

close to $\beta V_r cos(\theta_{est} - \theta_o)$. After subtraction, the amplitude of the sampled output voltage ripple is reduced from 485 $\mathrm{mV_{pp}}$ to 135 $\mathrm{mV_{pp}}$, as shown in Fig. 3.12(c), which leads to a near sinusoidal input current.

Table 3.1: Specifications of boost PFC pre-regulator prototype.

Description	**Parameter**	**Value**
Nominal input or line voltage (rms)	V_{in}	110 V_{rms}
Nominal input or line frequency	f_{line}	60 Hz
Nominal output voltage	V_o	400 V
Nominal output power	P_o	200 W
Nominal load resistance	R_o	800 Ω
Output capacitance	C_o	16 μF
Maximum gain of amplitude tuner	R_{2a}/R_1	4
Minimum gain of amplitude tuner	R_{2b}/R_1	0.3

3.6 Experimental Verification

In this section, the proposed ripple estimation/cancellation circuit is verified by its implementation in an ACM-controlled boost PFC pre-regulator with the specifications listed in Table 3.1. The PFC pre-regulator's unity-gain-bandwidth is designed to be approximately 60 Hz, which is larger than that encountered in conventional design ($\leq$ 10 Hz) for achieving fast dynamic response. To demonstrate the improvement in power factor as a result of implementing the proposed ripple estimation/cancellation circuit, a second PFC pre-regulator is constructed with the same specifications but without ripple estimation/cancellation circuit implemented.

Fig. 3.13 shows the steady-state input and output waveforms of the boost PFC pre-regulator prototype implemented with the proposed ripple estimation/cancellation circuit. The measured average output voltage and current is 401.89 V and 516.0 mA, respectively. The power factor was measured to be 0.995, and the total harmonic distortion (THD) of the PFC pre-regulator's input current is 7.78 % as given by the FFT spectrum shown in Fig. 3.18(a). The high power factor and low THD verify that the PFC pre-regulator's input current $i_{in}(t)$ is very close to an ideal sinusoidal waveform and is in phase with the line voltage $v_{in}(t)$. Be-

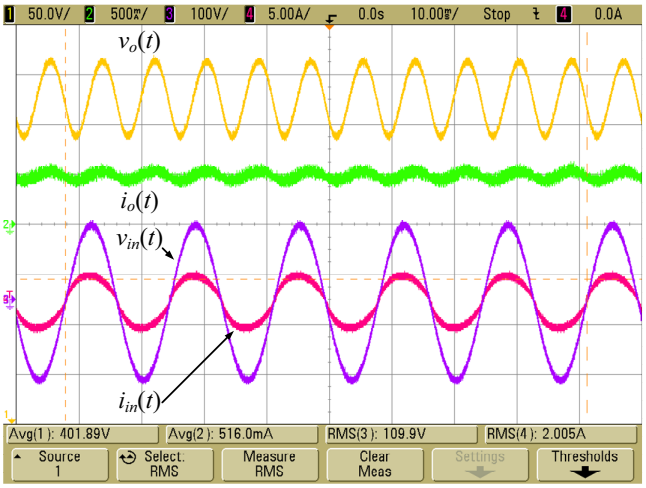


Figure 3.13: Input and output waveforms of boost PFC pre-regulator prototype ($v_{in}(t)$: input or line voltage, $i_{in}(t)$: input or line current, $v_o(t)$: output voltage, $i_o(t)$: output current).

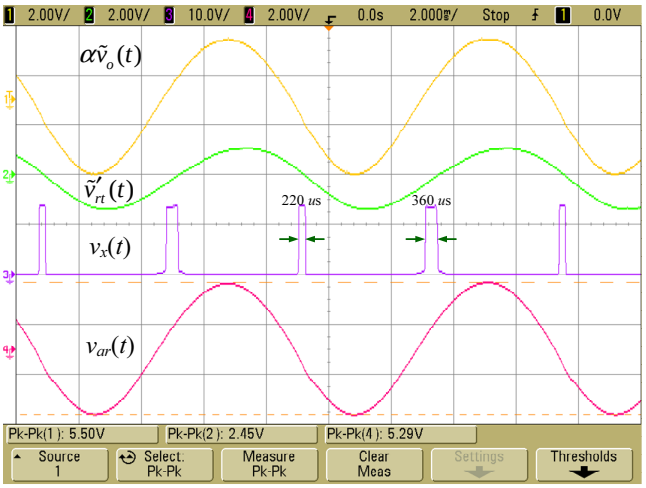


Figure 3.14: Main operating waveforms of phase difference detector ($\alpha\tilde{v}_o(t)$: sampled output voltage ripple, $\tilde{v}'_{rt}(t)$: phase-shifted ripple template, $v_x(t)$: exclusive-or (XOR) gate's output signal, $v_{ar}(t)$: reference signal for the amplitude tuner).

sides, it implies that the effect of the double-line frequency component has been successfully attenuated by ripple estimation/cancellation.

Fig. 3.14 shows the main operating waveforms of the phase difference detector. As mentioned in Section 3.3, the amplitude of the estimated output voltage ripple signal is designed to be $\beta V_r \cos(\theta_{est} - \theta_o)$. Hence, the phase-shifted ripple template $\tilde{v}'_{rt}(t)$ is compared with the sampled output voltage ripple $\alpha\tilde{v}_o(t)$, and the (average) phase difference between them is approximately 13°, which is

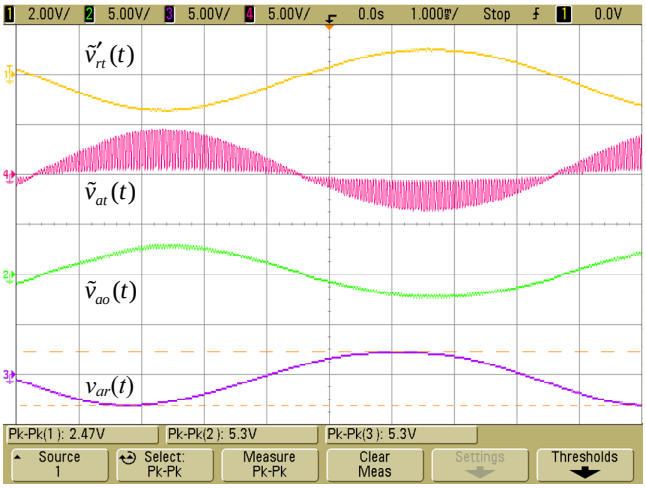


Figure 3.15: Main operating waveforms of amplitude tuner ($\tilde{v}'_{rt}(t)$: phase-shifted ripple template, $\tilde{v}_{at}(t)$: unfiltered amplitude-tuned ripple template, $\tilde{v}_{ao}(t)$: filtered amplitude-tuned ripple template, $v_{ar}(t)$: reference signal for the amplitude tuner).

calculated by measuring the high-level time interval of the exclusive-or (XOR) gate's output signal. From the measured waveforms, it can be calculated that the sampled output voltage ripple $\alpha\tilde{v}_o(t)$ is stepped down by a factor of 0.96 ($= 5.29\ V_{\rm pp}/5.50\ V_{\rm pp}$), which is close to $\cos(\theta_{est} - \theta_o)$, and is further used as the reference signal of the amplitude tuner $v_{ar}(t)$.

Subsequently, the phase-shifted ripple template $\tilde{v}'_{rt}(t)$ (with a peak-to-peak voltage of 2.47 $V_{\rm pp}$) is modified in amplitude by the amplitude tuner, which equalizes the amplitude of its input signal with that of its reference signal $v_{ar}(t)$ (with a peak-to-peak voltage of 5.3 $V_{\rm pp}$). The operating waveforms of the amplitude tuner are depicted in Fig. 3.15. It can be seen that the filtered amplitude-tuned ripple template $\tilde{v}_{ao}(t)$ is equal in amplitude but out-of-phase with that of the reference signal $v_{ar}(t)$. Hence, the filtered amplitude-tuned ripple template $\tilde{v}_{ao}(t)$ is first inverted by an unity-gain inverting amplifier, before it is stepped down by a factor of $\lambda = \beta/\alpha$ and subtracted from the sampled output voltage $\beta v_o(t)$ through a difference amplifier.

Fig. 3.16 shows the input and output waveforms of the difference amplifier under full-load condition. Recall that the phase difference between the sampled

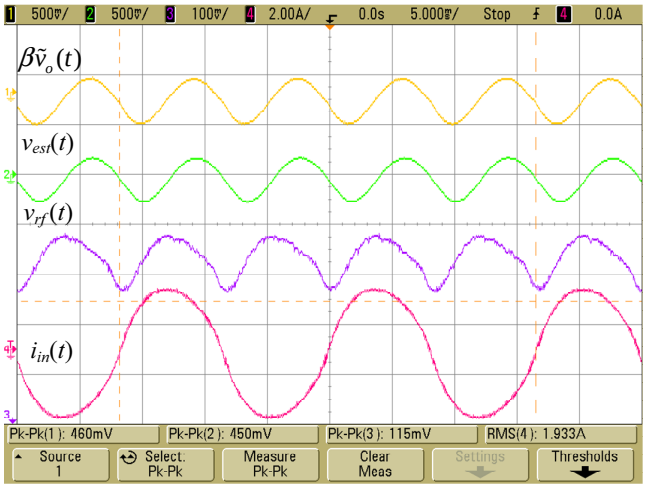


Figure 3.16: Input and output waveforms of difference amplifier ($\beta\tilde{v}_o(t)$: sampled output voltage ripple, $v_{est}(t)$: estimated output voltage ripple, $v_{rf}(t)$: output of difference amplifier, $i_{in}(t)$: input or line current).

output voltage ripple $\beta\tilde{v}_o(t)$ and the output signal of the amplitude tuner $\tilde{v}''_{rt}(t)$ is approximately 13°. By measuring the amplitude of both the sampled output voltage ripple $\beta\tilde{v}_o(t)$ and the estimated ripple $v_{est}(t)$, it can be deduced that the estimated output voltage ripple $v_{est}(t)$ $[= \lambda\tilde{v}''_{rt}(t)]$ is of an amplitude close to $\beta V_r \cos(\theta_{est} - \theta_o)$, which is the optimum operating amplitude suggested by Eq. (3.20). After subtraction, the amplitude of the sampled output voltage ripple is reduced to 115 $\mathrm{mV_{pp}}$ before it is further processed by the voltage error amplifier. As a result, a near-unity power factor as well as an input current with low THD is obtained.

Next, two boost PFC pre-regulators, one with ripple estimation/cancellation and the other without, are compared in terms of their power factor and dynamic performances when both are subjected to step changes in operating conditions. Fig. 3.17(a) and (b) shows the measured input and output waveforms of the PFC pre-regulator with ripple estimation/cancellation when subjected to a step load decrease and increase, respectively. Fig. 3.17(c) and (d) shows the same waveforms of the PFC pre-regulator without ripple estimation/cancellation under the same step load changes. The settling time of both PFC pre-regulators are sim-

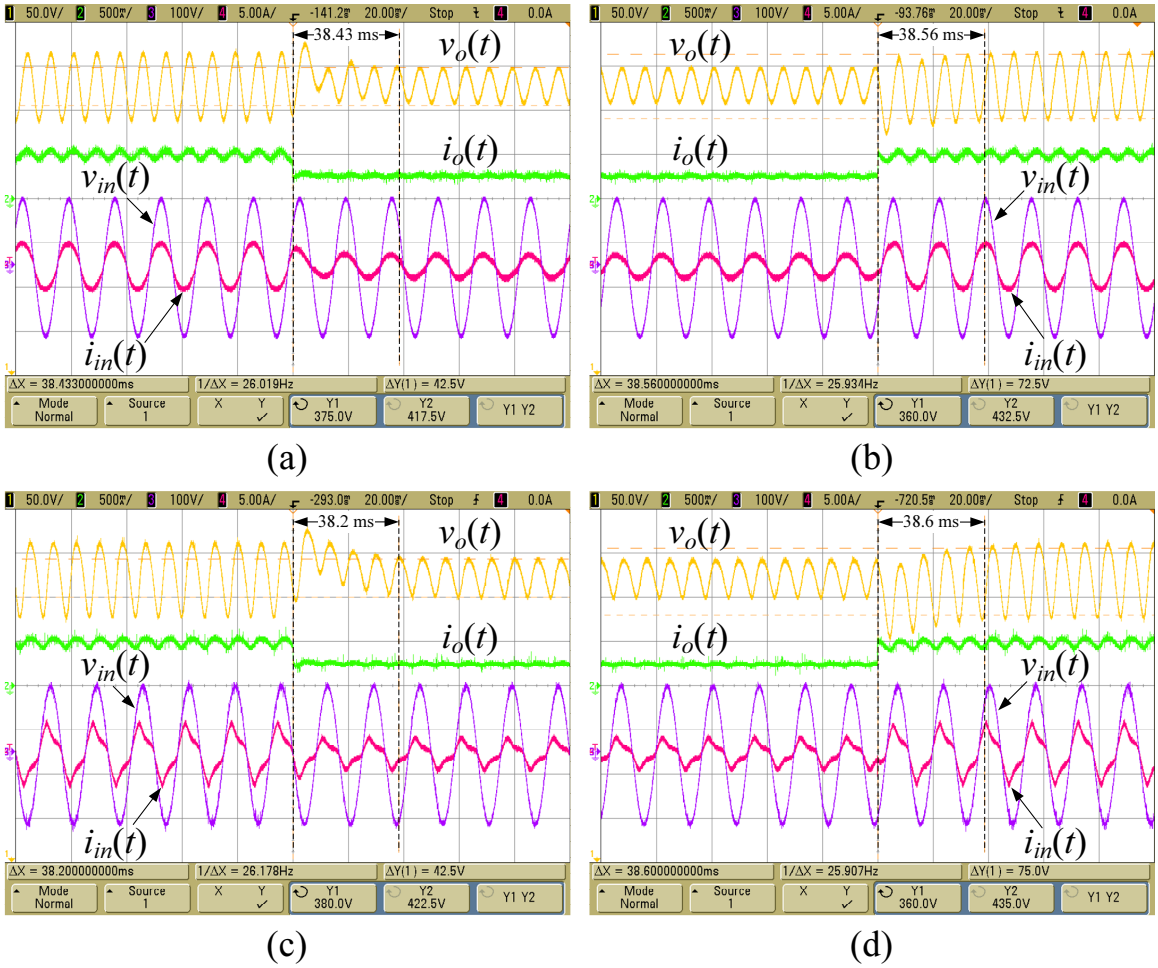


Figure 3.17: Input and output waveforms of boost PFC pre-regulator with [(a) and (b)] and without [(c) and (d)] ripple estimation/cancellation under step decrease [(a) and (c)] and increase [(b) and (d)] in load.

ilar (approximately 38 ms) as their loop gain's crossover frequency are designed to be the same. With the aid of ripple estimation/cancellation, the PFC pre-regulator operates with a power factor of 0.995 and of 0.997 under the conditions of full-load and half-load, respectively, whereas the power factor of the one without ripple estimation/cancellation decreases to 0.952 at nominal load and 0.92 at half-load without any ripple estimation/cancellation. Fig. 3.18 shows the FFT spectra of the PFC pre-regulator's input current with and without ripple estimation/cancellation under full-load and half-load conditions. With the aid of the proposed ripple estimation/cancellation, the THD of the input current has

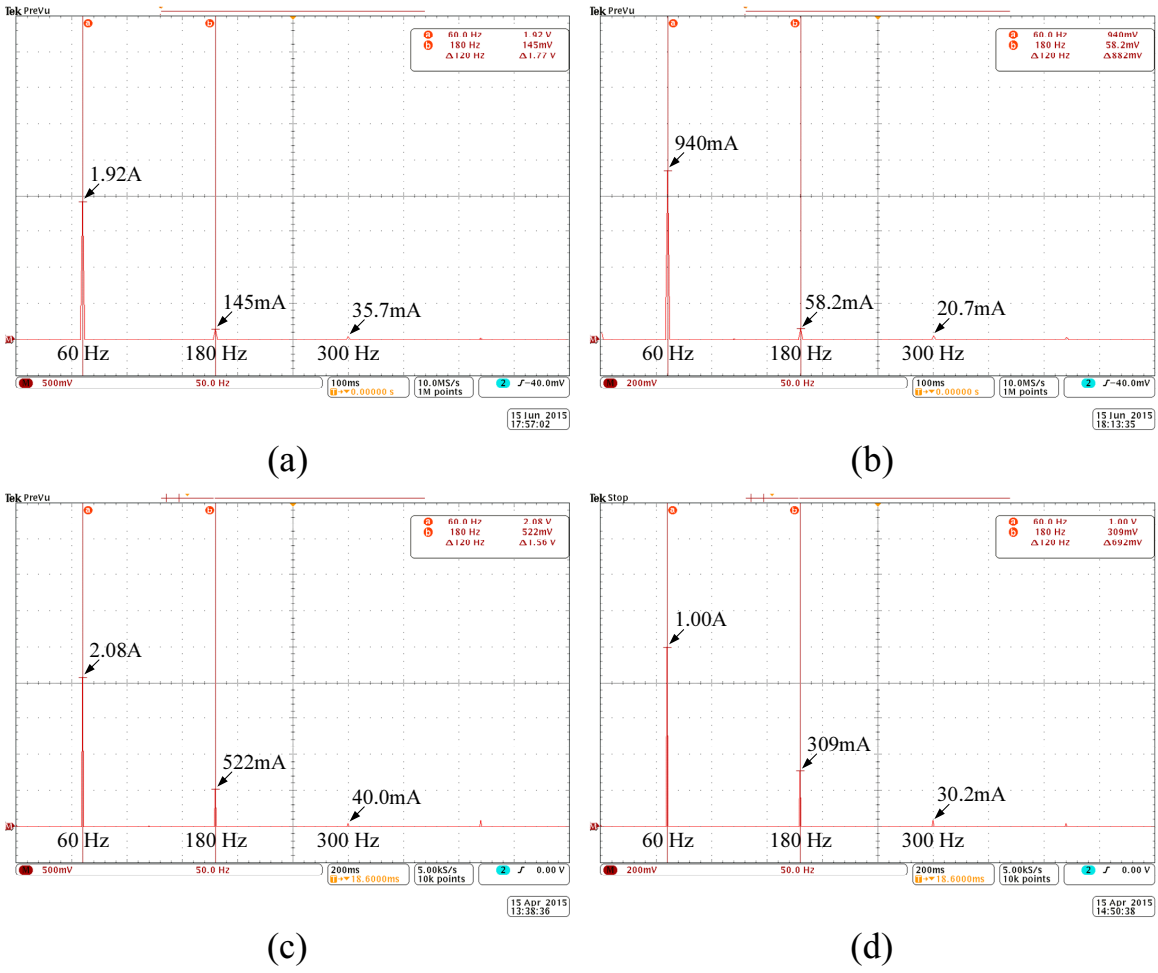


Figure 3.18: FFT spectra of the input current of boost PFC pre-regulator prototype with [(a) and (b)] and without [(c) and (d)] ripple estimation/cancellation under full-load [(a) and (c)] and half-load [(b) and (d)] conditions.

been reduced from 25.17 % to 7.78 % at full-load and from 31.05 % to 6.57 % at half-load.

Fig. 3.19 shows the input and output waveforms of the difference amplifier when the PFC pre-regulator is operating under half-load condition. It can be seen that the amplitudes of both the sampled output voltage ripple $\beta\tilde{v}_o(t)$ and the estimated output voltage ripple $v_{est}(t)$ are nearly equal (238 $\mathrm{mV_{pp}}$ and 239 $\mathrm{mV_{pp}}$). After subtraction (i.e. $v_{rf}(t) = \beta v_o(t) - v_{est}(t)$), the double-line frequency component at the input of the voltage error amplifier has been reduced in amplitude from 238 $\mathrm{mV_{pp}}$ to 30 $\mathrm{mV_{pp}}$. The amplitude of the estimated output voltage rip-

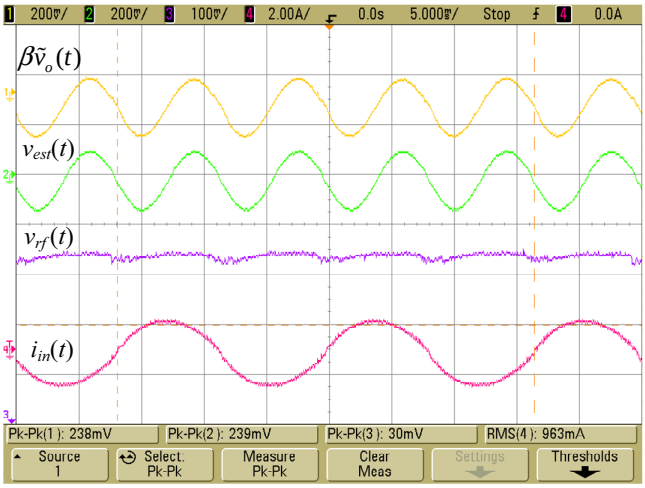


Figure 3.19: Input and output waveforms of difference amplifier ($\beta\tilde{v}_o(t)$: sampled output voltage ripple, $v_{est}(t)$: estimated output voltage ripple, $v_{rf}(t)$: output of difference amplifier, $i_{in}(t)$: input or line current).

ple can be determined and explained by Eq. (3.33). When the load is halved, the phase angle of the output voltage ripple θ_o, as suggested by Eq. (3.1) and Eq. (3.2), will tend to 90°. Recall that θ_{est} is made constant and equal to 90°, hence, according to Eq. (3.20), the estimated output voltage ripple $v_{est}(t)$ should have an amplitude that is equal to that of $\beta\tilde{v}_o(t)$.

$$\begin{aligned} & \beta V_r \cos(\theta_{est} - \theta_o) \\ \xrightarrow{\theta_{est}=\theta_o=90^\circ} \quad & \beta V_r \cos(90^\circ - 90^\circ) \\ = \quad & \beta V_r \cos(0^\circ) \\ = \quad & \beta V_r \end{aligned} \tag{3.33}$$

Next, the dynamic response of the PFC pre-regulators under the step changes in line voltage and frequency are investigated. Fig. 3.20 and Fig. 3.21 shows the input and output waveforms of both PFC pre-regulators (with and without ripple estimation network) in response to these step changes, respectively. From Fig. 3.20 and Fig. 3.22, it can be measured that the power factor at V_{in} =150 V_{rms} has been improved from 0.862 to 0.990 in the presence of the proposed ripple

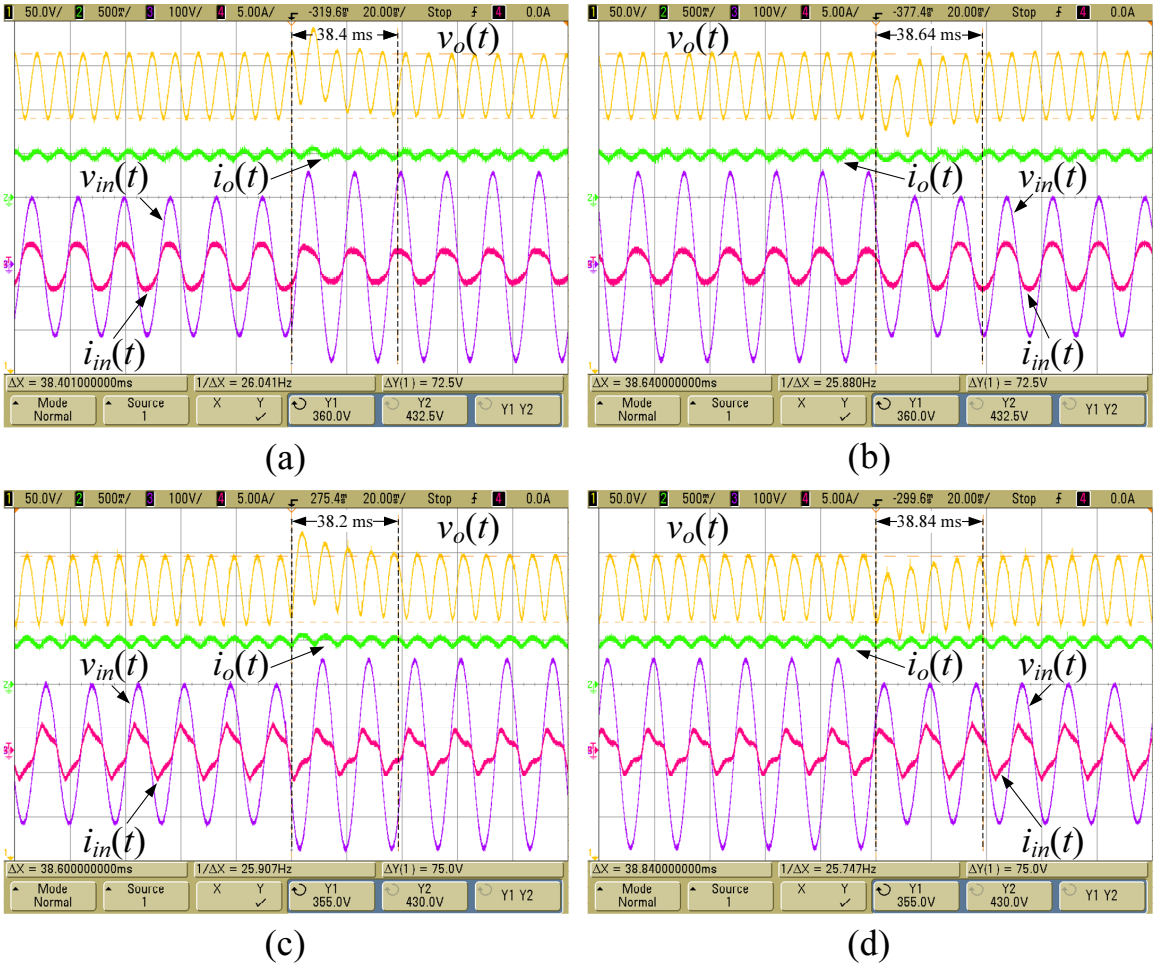


Figure 3.20: Input and output waveforms of boost PFC pre-regulator with [(a) and (b)] and without [(c) and (d)] ripple estimation/cancellation under step increase [(a) and (c)] and decrease [(b) and (d)] in line voltage.

estimation network, while the THD of input current decreases by approximately 70 %. These improvements can be explained by means of Fig. 3.23, which shows that the amplitude of the sampled output voltage ripple is reduced from 440 $\mathrm{mV_{pp}}$ to 118 $\mathrm{mV_{pp}}$ after subtracting the estimated output voltage ripple $v_{est}(t)$ having a peak-to-peak voltage of 430 $\mathrm{mV_{pp}}$. Same as before, the estimated output voltage ripple $v_{est}(t)$ is operating with an amplitude of $\beta V_r \cos(\theta_{est} - \theta_o)$.

In the case of line frequency variation, both PFC pre-regulators reach their steady state immediately after the line frequency is stepped from f_{line} =60 Hz to f_{line} =50 Hz and back to f_{line} =60 Hz, as shown in Fig. 3.21. From the key

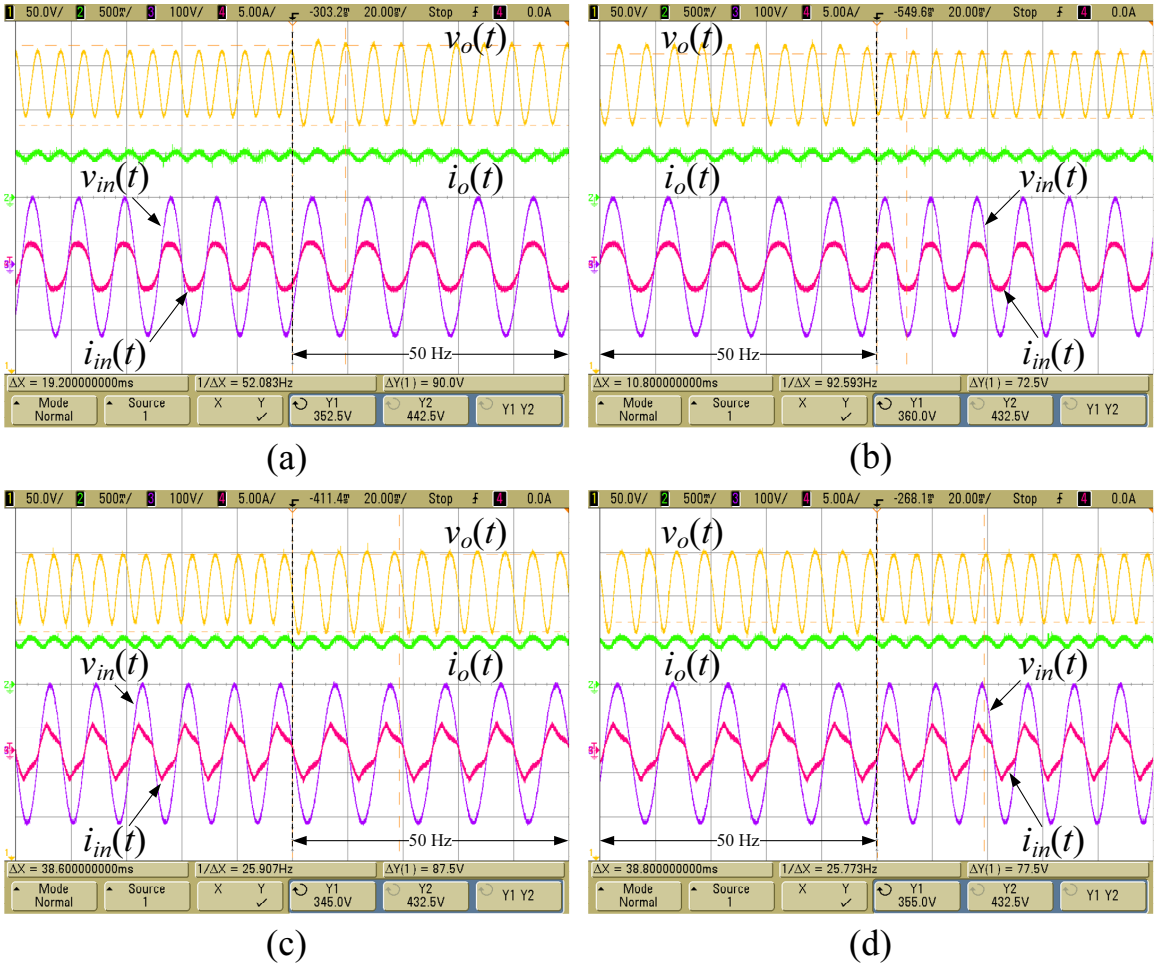


Figure 3.21: Input and output waveforms of boost PFC pre-regulator with [(a) and (b)] and without [(c) and (d)] ripple estimation/cancellation under step decrease [(a) and (c)] and increase [(b) and (d)] in line frequency.

waveforms of the difference amplifier at f_{line} =50 Hz depicted in Fig. 3.25, it can be seen that the amplitude of both the sampled output voltage ripple $\beta\tilde{v}_o(t)$ and the estimated output voltage ripple $v_{est}(t)$ are increased when the line frequency is reduced. However, with the aid of the proposed ripple estimation/cancellation, the measured power factor is near-unity and the THD of input current is reduced from 27.46 % to 10.08 %, which can be calculated from Fig. 3.24.

Finally, the proposed ripple estimation/cancellation network is tested by doubling the output capacitance, i.e. $C_o \rightarrow 32\ \mu F$. Similar to the case of half-load condition, the amplitude of the sampled output voltage ripple $\beta\tilde{v}_o(t)$ is reduced

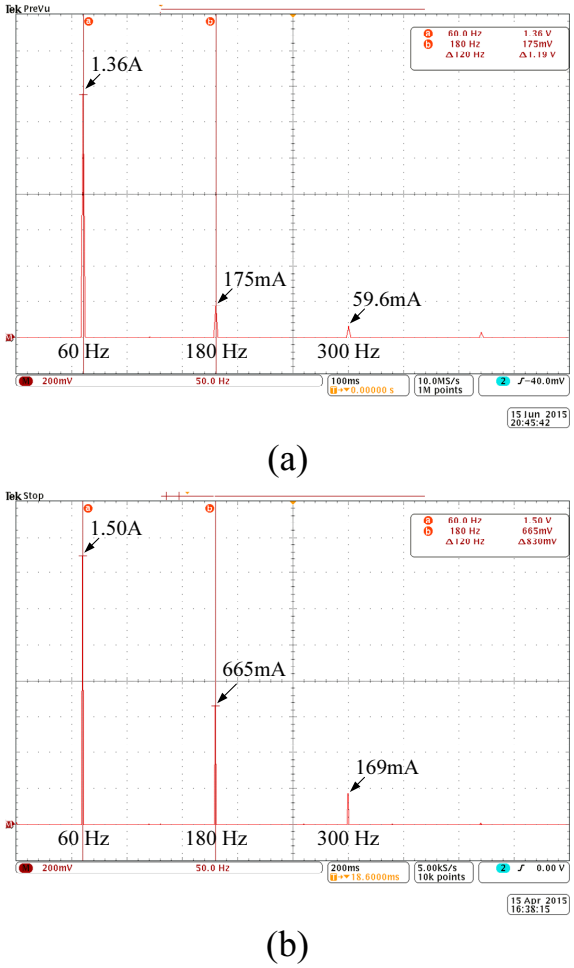


Figure 3.22: FFT spectra of the input current of boost PFC pre-regulator prototype (a) with and (b) without ripple estimation/cancellation at V_{in} =150 V_{rms}.

and its phase angle θ_o is towards 90°. As depicted in Fig. 3.26, both the sampled output voltage ripple $\beta\tilde{v}_o(t)$ and the estimated output voltage ripple $v_{est}(t)$ are nearly equal in amplitude, i.e. $|v_{est}(t)| \approx |\beta\tilde{v}_o(t)|$, while the peak-to-peak voltage of the resulting signal $v_{rf}(t)$ after ripple cancellation is only 45 mV_{pp}. This reduction in amplitude results in a near-unity power factor of 0.995 and a low THD of the input current of 7.60 % as measured by Fig. 3.27.

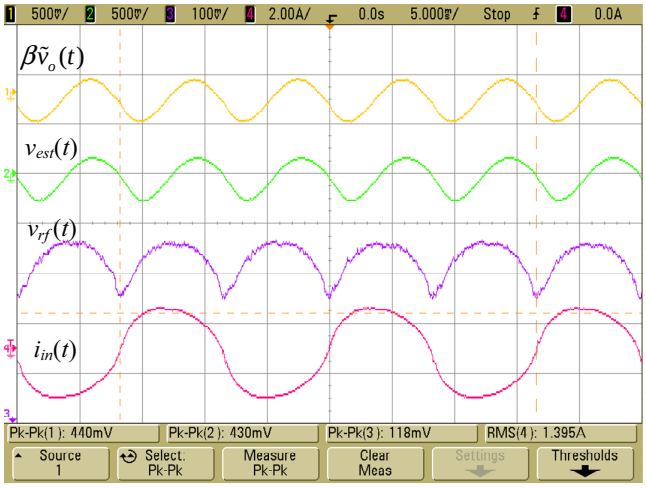


Figure 3.23: Input and output waveforms of difference amplifier at V_{in} =150 V_{rms} ($\beta\tilde{v}_o(t)$: sampled output voltage ripple, $v_{est}(t)$: estimated output voltage ripple, $v_{rf}(t)$: output of difference amplifier, $i_{in}(t)$: input or line current).

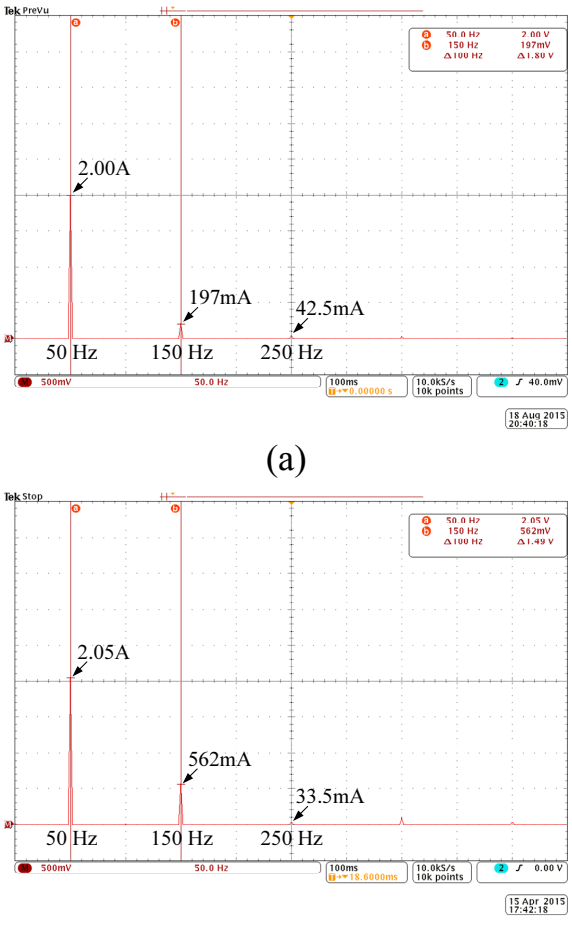


Figure 3.24: FFT spectra of the input current of boost PFC pre-regulator prototype (a) with and (b) without ripple estimation/cancellation at f_{line} =50 Hz.

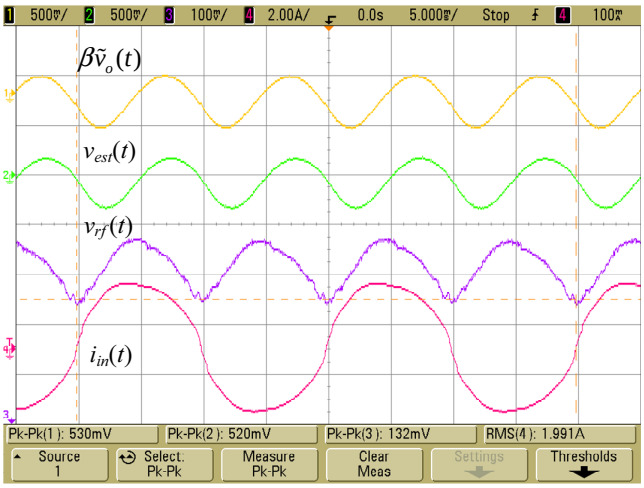


Figure 3.25: Input and output waveforms of difference amplifier at f_{line} =50 Hz ($\beta\tilde{v}_o(t)$: sampled output voltage ripple, $v_{est}(t)$: estimated output voltage ripple, $v_{rf}(t)$: output of difference amplifier, $i_{in}(t)$: input or line current).

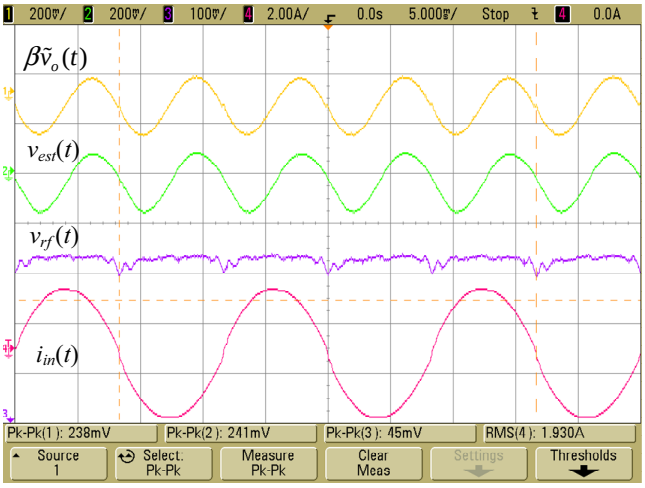


Figure 3.26: Input and output waveforms of difference amplifier at C_o =32 μF ($\beta\tilde{v}_o(t)$: sampled output voltage ripple, $v_{est}(t)$: estimated output voltage ripple, $v_{rf}(t)$: output of difference amplifier, $i_{in}(t)$: input or line current).

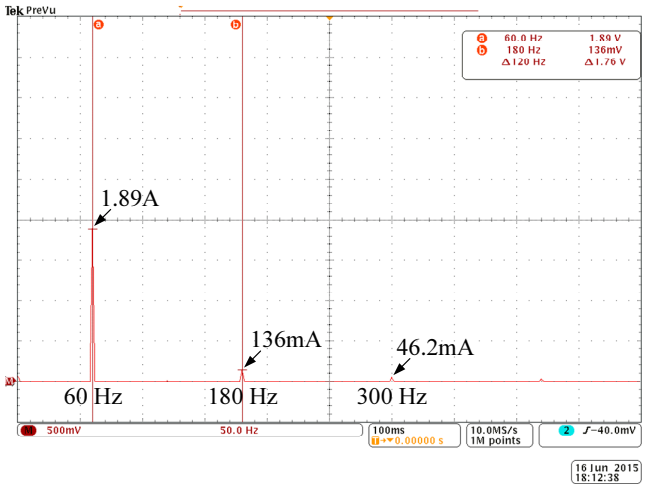


Figure 3.27: FFT spectrum of the input current of boost PFC pre-regulator prototype with ripple estimation/cancellation at C_o =32 μF.

3.7 Conclusion

In this chapter, a ripple estimation method based on minimum local cancellation error was proposed. From the presented mathematical analysis, the estimated output voltage ripple $v_{est}(t)$ is suggested to operate with an amplitude that is proportional to the phase difference between the sampled output voltage ripple and the phase-shifted ripple template, i.e. $\beta V_r \cos(\theta_{est} - \theta_o)$. A ripple estimation network, which mainly consists of a phase difference detector and an amplitude tuner, is proposed. The main function of the phase difference detector is to approximate the cosine value of the phase difference between the phase-shifted ripple template $\tilde{v}'_{rt}(t)$ and the sampled output voltage ripple $\alpha\tilde{v}_o(t)$. For the amplitude tuner, it equalizes the amplitude of the phase-shifted ripple template with that of its reference signal. The proposed ripple estimation network is tested under different operating conditions with a 200-W boost PFC pre-regulator as power stage having a large loop gain's crossover frequency. It was demonstrated that the amplitude of the estimated output voltage ripple $v_{est}(t)$ is configured to closely track the optimum value of $\beta V_r \cos(\theta_{est} - \theta_o)$ in response to variations in load, line voltage, line frequency and output capacitor's value. From the experimental results, it was verified that near-unity power factor and low THD of input current are achieved with the aid of the proposed ripple estimation network.

Chapter 4

Performance Comparison and Analysis of Three Ripple Estimation Methods

4.1 Introduction

In Chapter 2, a precise ripple estimation method based on amplitude and phase angle tuning is proposed. By estimating amplitude and phase individually, it enables an accurate estimation of the output voltage ripple under a wide range of operating conditions. In this chapter, this method is defined as Method 1 with $\rho = 1$ and $\theta_{est} = \theta_o$. It was shown that the THD of input current is very low and near-unity power factor is achieved despite the use of large unity-gain-bandwidth for achieving fast dynamic response in PFC pre-regulator compared to conventional design. A block diagram representing this ripple estimation method is shown in Fig. 4.2(a). Its aim is to produce a minimum global cancellation error by minimizing both amplitude and phase estimation errors. However, high complexity is the major drawback of this two-step approach.

In Chapter 3, the tunable phase shifter used in Method 1 is replaced by a

constant phase shift of 90° of the ripple template in order to produce a ripple estimation circuit having a simpler structure. In the presence of phase estimation error, the optimum amplitude of the estimated output voltage ripple has been modified from βV_r to $\beta V_r \cos(90^\circ - \theta_o)$, where θ_o is the actual phase angle of the output voltage ripple. An amplitude tuner is used to regulate the amplitude of the ripple template to the desired value, i.e. $\beta V_r \cos(90^\circ - \theta_o)$. The aim is to minimize the amplitude of the error signal processed by the voltage error amplifier in the presence of phase estimation error. In this chapter, this method is defined as Method 2 with $\rho = \cos(\theta_{est} - \theta_o)$ and $\theta_{est} \neq \theta_o$, where $\theta_{est} = 90^\circ$. Although the design of the phase shifter is simplified, the complexity of the overall ripple estimation circuit is not reduced significantly due to the requirement of a phase difference detector.

Recall from Eq. (3.6) that A_1 determines to the amplitude of $\tilde{v}_{rf}(t)$ $[= \beta\tilde{v}_o(t) - v_{est}(t)]$, which is a function of ρ and $(\theta_{est} - \theta_o)$. By plotting the graph of A_1 against ρ with $(\theta_{est} - \theta_o)$ as parameter, as shown in Fig. 4.1, it can be observed that the value of A_1 at $\rho = 1$ is close to that at $\rho = \cos(\theta_{est} - \theta_o)$, unless when $(\theta_{est} - \theta_o)$ is large. Since A_1 is closely related to both the THD of input current and power factor, as suggested by Eq. (3.15) and Eq. (3.16), the performance of PFC pre-regulator is expected to be similar if A_1 does not vary significantly. As θ_o does not deviate significantly from 90° in most PFC pre-regulators, the phase estimation error $(\theta_{est} - \theta_o)$ is usually small when θ_{est} is set to 90°. In this case, the value of A_1, and hence, the difference in performance of PFC pre-regulator with the amplitude of estimated output voltage ripple being $V_{est} = \beta V_r$ and $V_{est} = \beta V_r \cos(\theta_{est} - \theta_o)$ is expected to be small. Based on this analysis, the phase measurement performed by phase difference detector may be omitted and the sampled output voltage ripple $\alpha\tilde{v}_o(t)$ can be used directly as the reference signal for the amplitude tuner. As a result, the estimated output voltage ripple $v_{est}(t)$ will be of the same amplitude as the sampled output voltage ripple $\beta\tilde{v}_o(t)$,

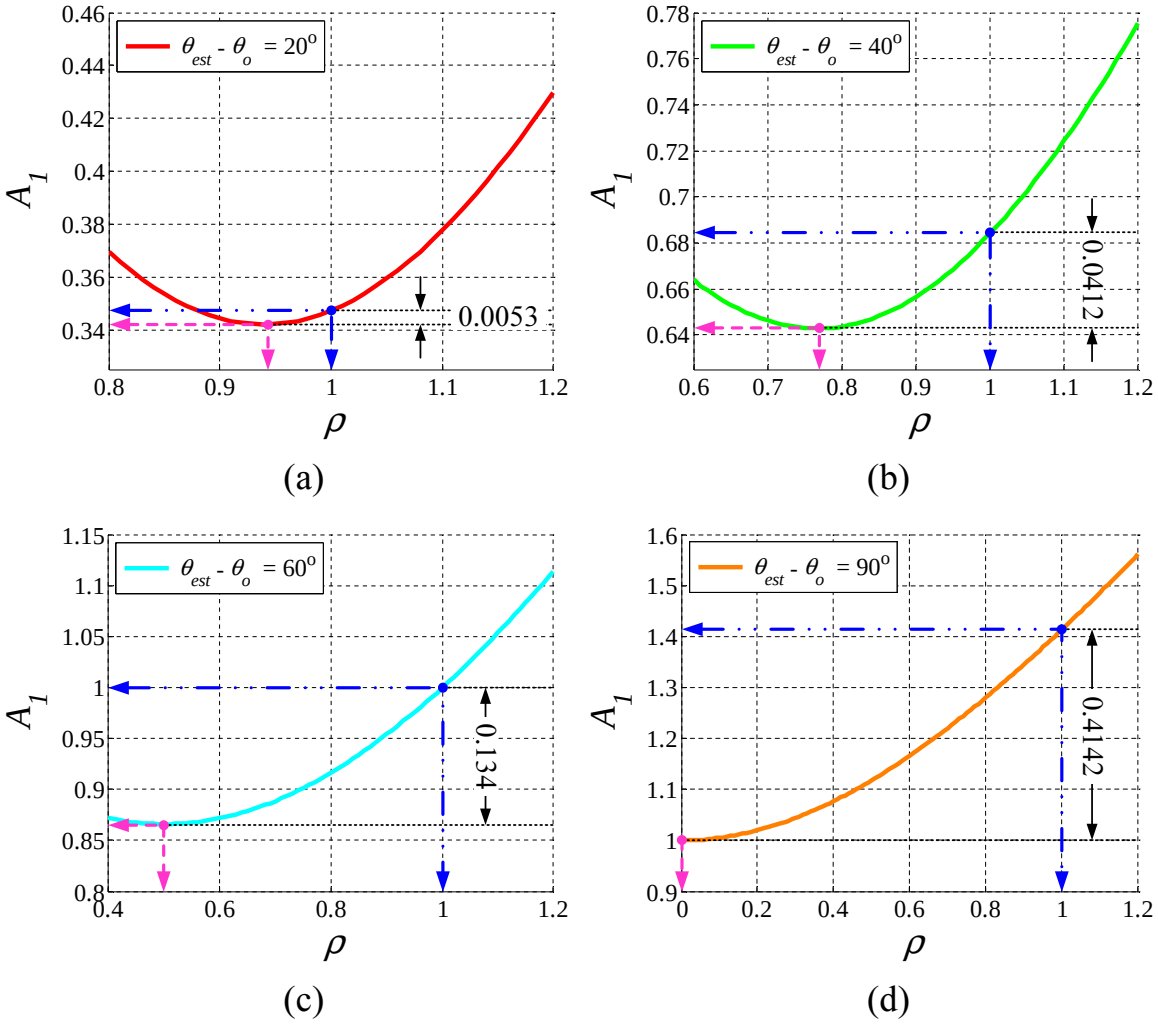


Figure 4.1: Plot of A_1 versus ρ for different values of $(\theta_{est} - \theta_o)$, where $\rho = V_{est}/\beta V_r$.

i.e. $V_{est} = \beta V_r$. In this chapter, this method is defined as Method 3 with $\rho = 1$ and $\theta_{est} \neq \theta_o$. Since the phase difference detector is eliminated, the complexity of the overall ripple estimation circuit can be reduced significantly.

In this chapter, the performance of these three ripple estimation methods will be tested and compared by implementing them in a 200-W boost PFC pre-regulator. The methods of implementation are illustrated by the block diagrams shown in Fig. 4.2(a), (b), and (c). Simulation and experimental results are presented and discussed in Section 4.2 and Section 4.3, respectively, followed by Conclusion given in Section 4.4.

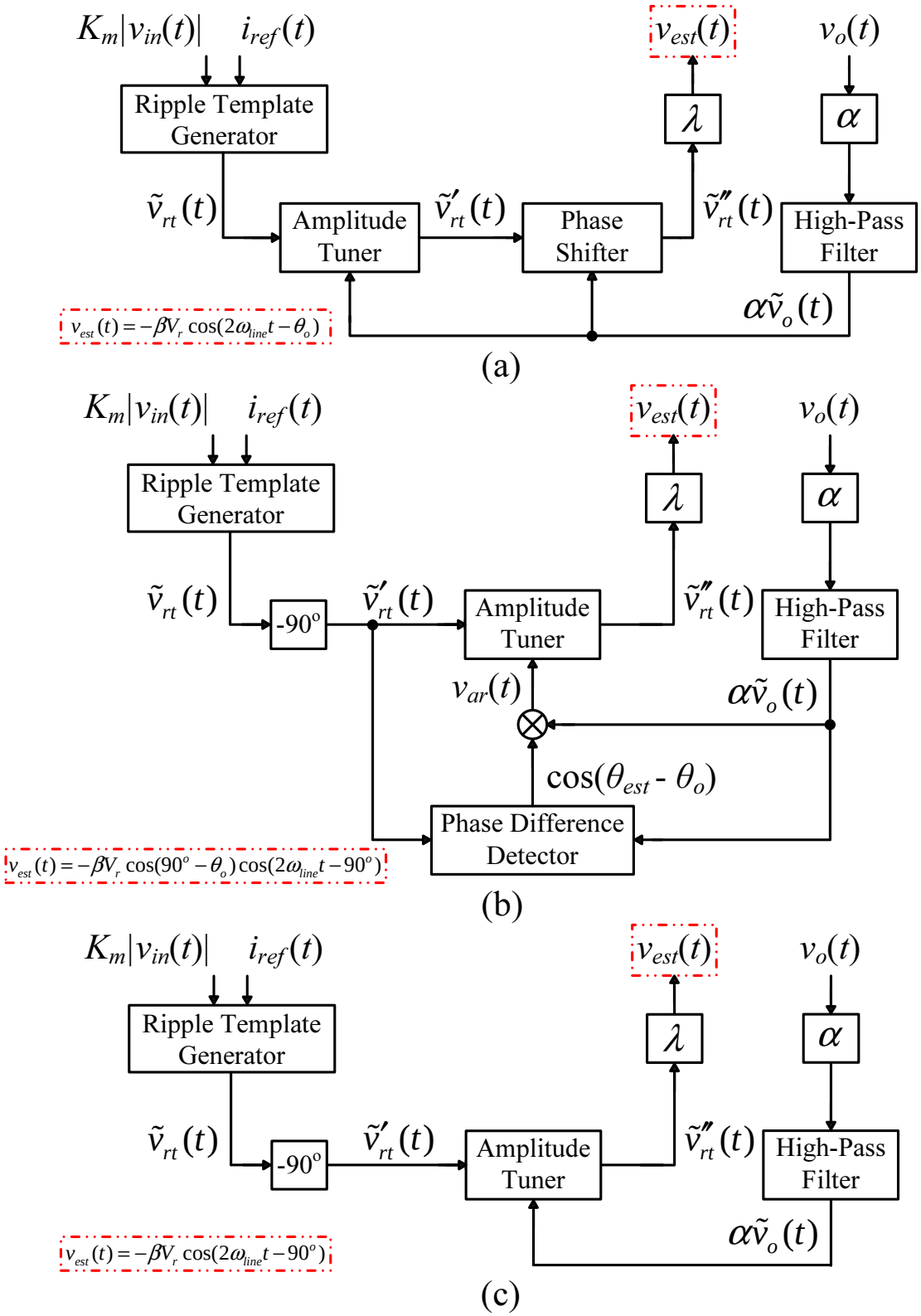


Figure 4.2: Basic configurations of three ripple estimation/cancellation methods (a) Method 1: $\rho = 1$ and $\theta_{est} = \theta_o$, (b) Method 2: $\rho = \cos(\theta_{est} - \theta_o)$ and $\theta_{est} \neq \theta_o$, (c) Method 3: $\rho = 1$ and $\theta_{est} \neq \theta_o$.

4.2 Simulation Results

In this section, the three ripple estimation/cancellation circuits depicted in Fig. 4.2 are simulated with a 200-W boost PFC pre-regulator as power stage. The specifications of the boost PFC pre-regulator are the same as those adopted in the previous chapters. Fig. 4.3(a), (b), and (c) shows the simulated key waveforms of the PFC pre-regulator when the estimated output voltage ripple is produced by Method 1, 2 and 3, respectively. With the aid of ripple estimation/cancellation circuit, the peak-to-peak voltage of the voltage error amplifier's output signal $v_{vea}(t)$ is significantly reduced, which results in a near-sinusoidal input current as shown in Fig. 4.3(a)–(c). However, it can be observed that the degree of reduction realized by Method 1, involving both amplitude tuner and phase shifter, is the most significant, resulting in the highest power factor. On the other hand, when the estimated output voltage ripple is produced by Method 2 and 3, the peak-to-peak voltages of the voltage error amplifier's output signals have increased, although remained considerably smaller compared to the case of no ripple estimation/cancellation, which is depicted in Fig. 4.3(d), which causes the input current to become strongly distorted. From the simulation results, it can be seen that the input current of the PFC pre-regulator and voltage error amplifier's output signal corresponding to Method 2 and 3 are not significantly different.

Next, the simulated operating waveforms of difference amplifier under the actions of the three ripple estimation/cancellation circuits are shown in Fig. 4.4. Fig. 4.4(a) shows the smallest peak-to-peak voltage of the difference amplifier's output signal $v_{rf}(t)$ when Method 1 is used, since the estimated output voltage $v_{est}(t)$ is of the same amplitude and phase angle as the sampled output voltage ripple $\beta\tilde{v}_o(t)$. As a consequence, the double-line frequency component that is present at the input of the voltage error amplifier is significantly reduced in amplitude from 520 $\mathrm{mV_{pp}}$ to 45 $\mathrm{mV_{pp}}$. Fig. 4.4(b) and Fig. 4.4(c) shows the

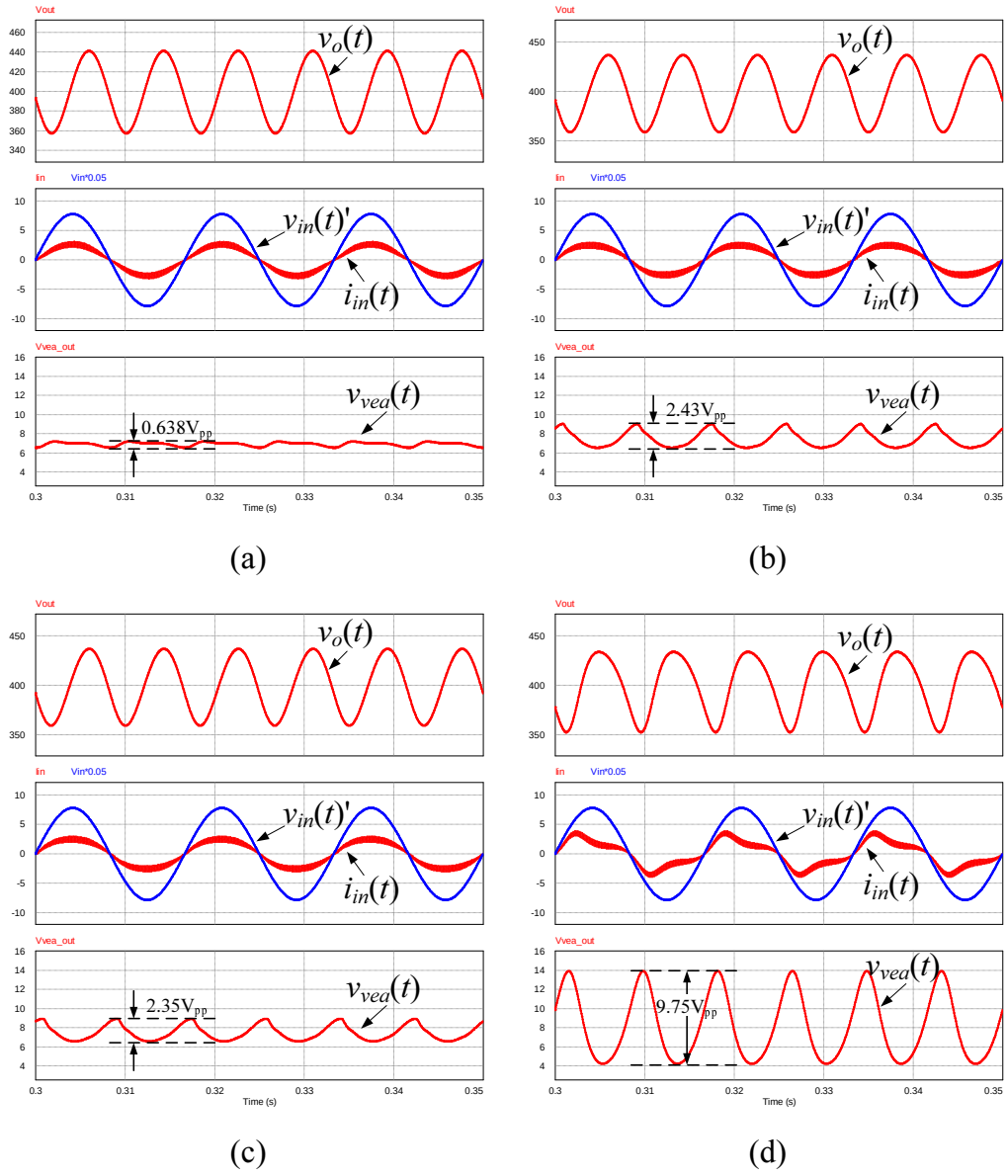


Figure 4.3: Simulated input and output waveforms of boost PFC pre-regulator [(a)-(c)] with and (d) without the ripple estimation/cancellation under nominal operating conditions ((a) Method 1: $\rho = 1$ and $\theta_{est} = \theta_o$, (b) Method 2: $\rho = \cos(\theta_{est} - \theta_o)$ and $\theta_{est} \neq \theta_o$, (c) Method 3: $\rho = 1$ and $\theta_{est} \neq \theta_o$).

same waveforms when the ripple estimation/cancellation circuits corresponding to Method 2 and 3 are used. Both circuits apply a fixed phase angle θ_{est} of 90° to the ripple template, while the amplitude of the estimated output voltage ripple is tuned to $\beta V_r \cos(\theta_{est} - \theta_o)$ and βV_r for Method 2 and 3, respectively. After performing subtraction (i.e. $\beta v_o(t) - v_{est}(t)$), the resultant signals $v_{rf}(t)$ are

similar in appearance and amplitude for both methods, although Method 3 results in a slightly smaller amplitude of $v_{rf}(t)$ compared to Method 2. Nevertheless, this small difference in amplitude is shown to have negligible impact on the input current and power factor of the PFC pre-regulator.

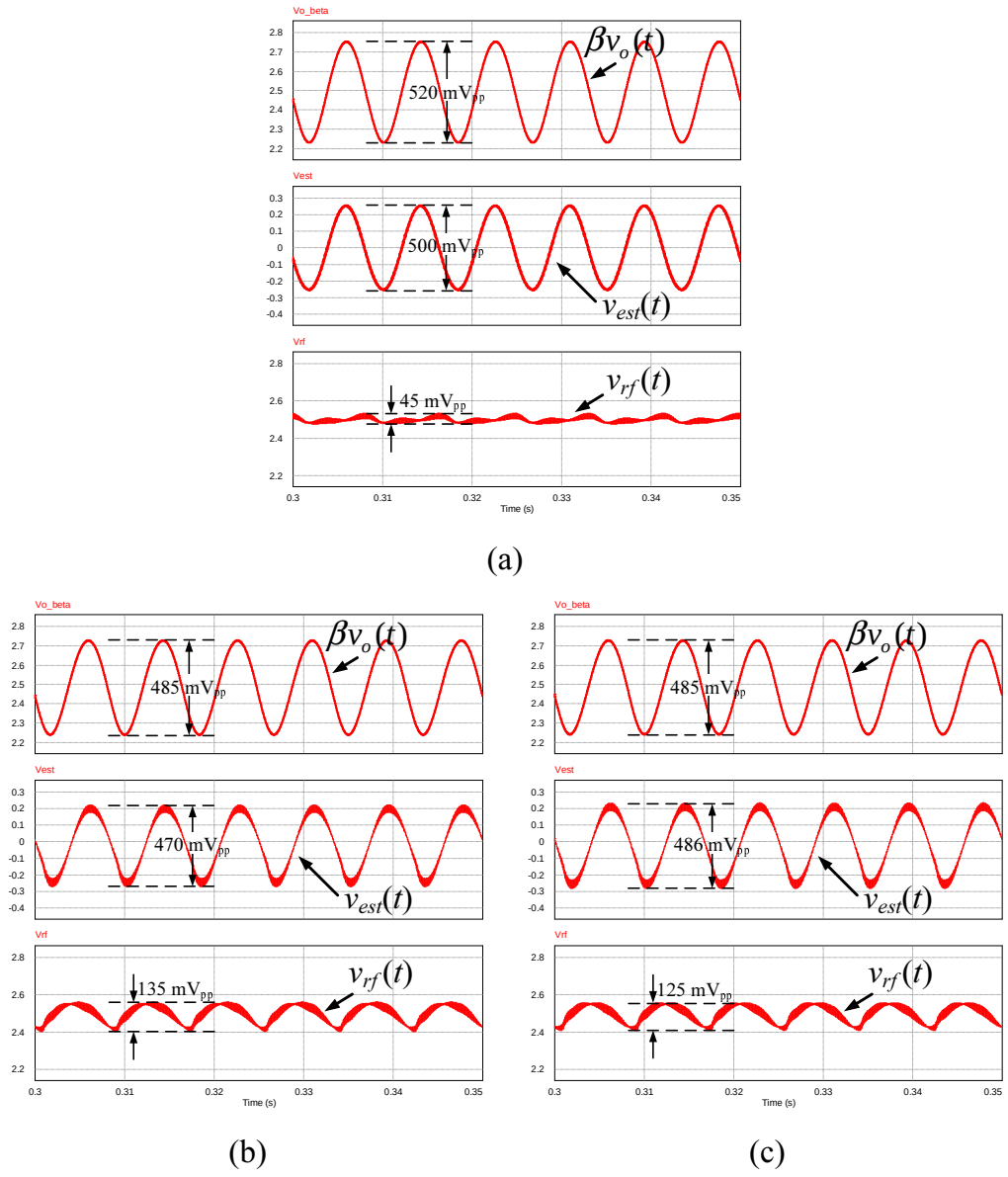


Figure 4.4: Simulated input and output waveforms of difference amplifier under the actions of three ripple estimation/cancellation methods, respectively, under nominal operating conditions ((a) Method 1: $\rho = 1$ and $\theta_{est} = \theta_o$, (b) Method 2: $\rho = \cos(\theta_{est} - \theta_o)$ and $\theta_{est} \neq \theta_o$, (c) Method 3: $\rho = 1$ and $\theta_{est} \neq \theta_o$).

Subsequently, the PFC pre-regulator under the actions of three different rip-

ple estimation/cancellation circuits is also simulated for load power, line voltage, line frequency, output capacitor size different from the nominal values. The simulated waveforms of difference amplifier and PFC pre-regulator's input current for these cases are shown in Fig. 4.5. It can be seen that ripple estimation based on Method 1 is precise in both amplitude and phase angle, which gives an undistorted and near-ideal sinusoidal input current. Although some estimation errors occur in the estimated output voltage ripple produced by Method 2 and 3 (i.e. Method 2: $\rho = \cos(\theta_{est} - \theta_o)$ and $\theta_{est} \neq \theta_o$, and Method 3: $\rho = 1$ and $\theta_{est} \neq \theta_o$), the simulated input current waveforms for both cases do not become significantly distorted. After performing subtraction, it can be observed that the output signal of the difference amplifier $v_{rf}(t)$ are similar for both Method 2 and 3, resulting in similar PFC pre-regulator's input currents and THD performances. Therefore, when consideration is given to the complexity of ripple estimation/cancellation circuit, it is evident that Method 3 is more economically viable and hence more practical as it consists of an amplitude tuner and a conventional 90^o phase shifter only, and is thus more preferable compared to Method 2. However, under very stringent THD and power factor requirements, the ripple estimation/cancellation circuit based on Method 1, having independent amplitude tuning and phase shifting actions, is the ideal solution.

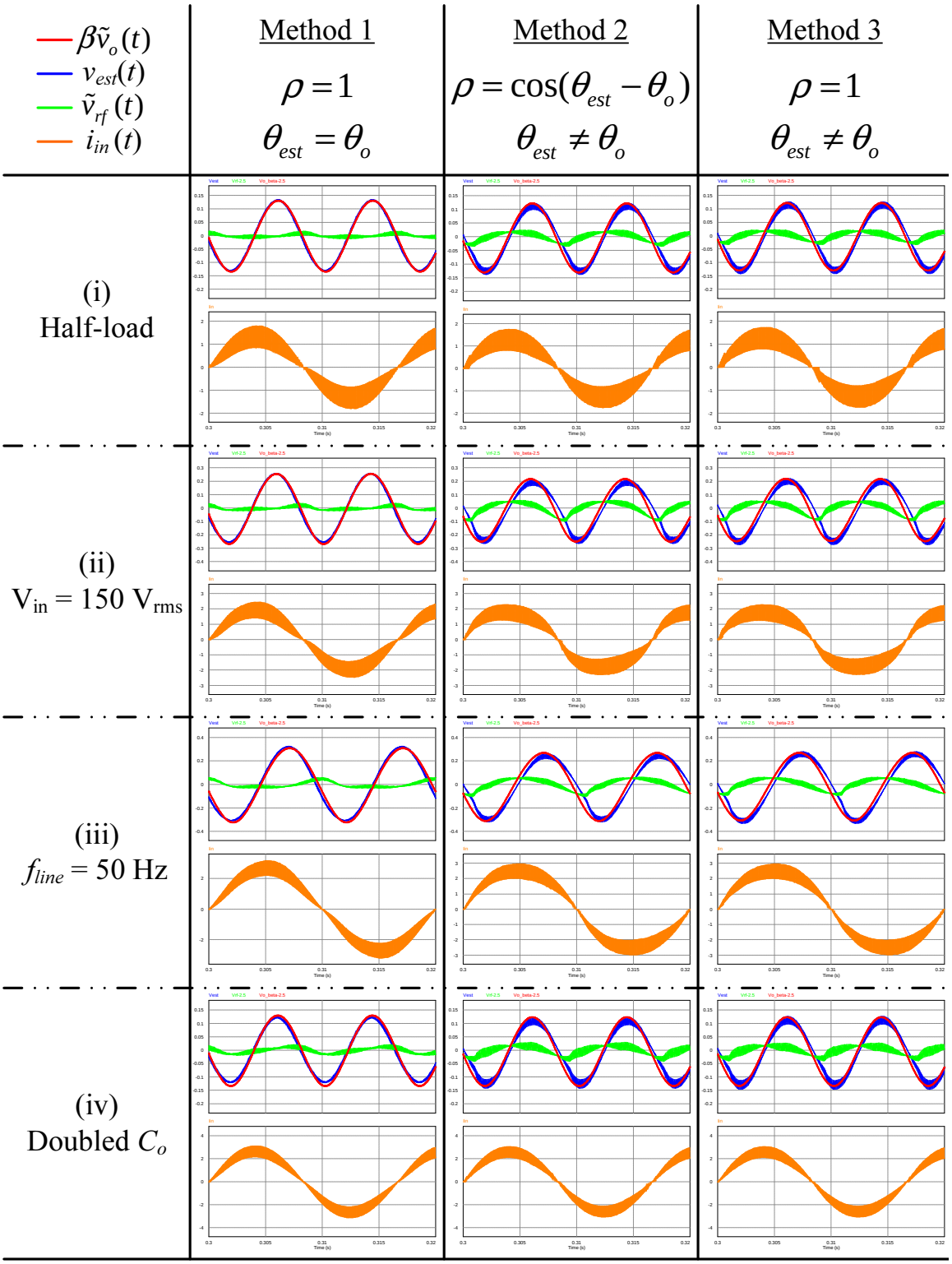


Figure 4.5: Simulated input and output waveforms of difference amplifier and PFC pre-regulator's input current waveforms under the actions of three ripple estimation/cancellation methods under various operating conditions.

4.3 Experimental Verification

In this section, the three proposed ripple estimation/cancellation circuits are implemented and tested experimentally. The power stage used in the experiment is a 200-W boost PFC pre-regulator having a unity-gain-bandwidth of 60 Hz. With this setup, the THD and power factor performances of the PFC pre-regulator under the actions of the three ripple estimation/cancellation methods will be investigated individually. The dynamic response of the PFC pre-regulator in the presence of the proposed ripple estimation/cancellation circuits will also be studied by subjecting it to step load variations.

Fig. 4.6 shows the input and output waveforms of difference amplifier and the FFT spectra of input current under nominal conditions. With the aid of both amplitude tuner and phase shifter, the estimated output voltage ripple $v_{est}(t)$ produced by Method 1 is of the same amplitude and phase angle as the sampled output voltage ripple $\beta\tilde{v}_o(t)$, which results in a precise cancellation of the sampled output voltage ripple and reduces its amplitude to 50 $\mathrm{mV_{pp}}$ before it propagates through the voltage error amplifier. As a consequence, a near-ideal sinusoidal input current $i_{in}(t)$ with a very low THD of 4.62 % is obtained, and the measured power factor is 0.999. In comparison to Method 1, the presence of phase estimation error generated by Method 2 and 3 caused the measured power factor to decrease to 0.995, and the THD of PFC pre-regulator's input current to increase to 7.78 % and 7.33 % for Method 2 and 3, respectively, as a result of larger ripple present in the difference amplifier's output signal. Moreover, it can be observed that both Method 2 and 3 show similar performances in terms of power factor and THD of input current, hence both methods resulted in similar input current waveforms.

Fig. 4.7 shows the main operating waveforms when the load is reduced to 50% of the nominal value, i.e. 200 W $\rightarrow$ 100 W. It can be seen that all three

ripple estimation/cancellation circuits are able to generate an accurate replica of the sampled output voltage ripple. Under half-load condition, both the estimated output voltage ripple signals $v_{est}(t)$ produced by Method 2 and 3 are of the same amplitude as the sampled output voltage ripple $\beta\tilde{v}_o(t)$, and since the actual phase angle θ_o tends to 90° under half-load condition, which is close to the estimated phase angle (90°), the resulted phase estimation error therefore approaches zero and the estimated output voltage ripple matches the sampled output voltage ripple more closely. As a result, the peak-to-peak voltage of the difference amplifier's output signal under the actions of all three methods is about 30 $\mathrm{mV_{pp}}$, which resulted in input current with reduced THD (compared to the case of full-load condition) and near-unity power factor.

Next, the performances of the three ripple estimation/cancellation methods are investigated under increased line voltage and decreased line frequency. Fig. 4.8 shows the key waveforms of difference amplifier and the FFT spectra of PFC pre-regulator's input current at V_{in} =150 $\mathrm{V_{rms}}$, while Fig. 4.9 shows the same waveforms at f_{line} =50 Hz. Similar as before, the ripple estimation/cancellation circuit based on Method 1 always produces estimated output voltage ripple $v_{est}(t)$ that is equal in amplitude and phase angle to the sampled output voltage ripple $\beta\tilde{v}_o(t)$, hence the difference amplifier's output signal is approximately ripple-free in both cases. This is confirmed by the low measured THD of input current, amounting to 5.09 % and 4.58 % at V_{in} =150 $\mathrm{V_{rms}}$ and at f_{line} =50 Hz, respectively. However, when the estimated output voltage ripple $v_{est}(t)$ is produced by Method 2 at V_{in} =150 $\mathrm{V_{rms}}$ and f_{line} =50 Hz, a ripple component (of 118 $\mathrm{mV_{pp}}$ at V_{in} =150 $\mathrm{V_{rms}}$ and 132 $\mathrm{mV_{pp}}$ at f_{line} =50 Hz) exists in the difference amplifier's output signal $v_{rf}(t)$, and caused the THD of input current to increase from 5.09 % to 13.59 % at V_{in} =150 $\mathrm{V_{rms}}$ and from 4.58 % to 10.08 % at f_{line} =50 Hz. Similar results were obtained when the estimated output voltage ripple $v_{est}(t)$ is produced by Method 3. Fig. 4.8(e) and Fig. 4.9(e) show that the difference

amplifier's output signal is not ripple-free but has an amplitude of 111 mV_{pp} at V_{in} =150 V_{rms} and 129 mV_{pp} at f_{line} =50 Hz, which are similar to those obtained with Method 2. The imperfect cancellation is predominantly caused by the phase estimation error between θ_{est} and θ_o.

Finally, the proposed ripple estimation/cancellation methods are examined under increased output capacitance of PFC pre-regulator, which leads to reduction in the amplitude of sampled output voltage ripple and its phase angle θ_o to tend to 90°. Under increased output capacitance, the behaviour of the sampled output voltage ripple is similar to that under half-load condition. From the measured FFT spectra of input current, as depicted in Fig. 4.10, it was measured that the THD of input current with Method 1 is 3.46 %, while with Method 2 and 3 it increased to 7.60 % and 6.19 %, respectively. The reason for having achieved low THD of input current and near-unity power factor is due to the fact that the estimated output voltage ripple $v_{est}(t)$ is of the same magnitude as the sampled output voltage ripple $\beta\tilde{v}_o(t)$ in all three cases, and the phase difference $(\theta_{est} - \theta_o)$ approaches zero. As a result, the ripple cancellation error is small and the output signal of the voltage error amplifier is approximately ripple-free and, hence, a near-ideal sinusoidal input current reference signal is obtained, which leads to an undistorted sinusoidal input current.

The measured amplitudes of the input and output signals of difference amplifier and the measured THD of input current under the aforementioned operating conditions are summarized in Table 4.1 and Table 4.2 for all three ripple estimation/cancellation methods. It can be seen that, when both amplitude tuner and phase shifter are used to generate the estimated output voltage ripple $v_{est}(t)$, the power factor of PFC pre-regulator is consistently unity and the THD of input current is very low under various operating conditions. However, if the estimated phase angle θ_{est} is fixed at 90°, the THD of input current increases and the power factor is slightly degraded, and the degradation in performance is similar for both

Method 2 and 3. By comparing the measurement results obtained for Method 2 and 3, the peak-to-peak voltages of the resultant signals after subtraction, i.e. $v_{rf}(t)$, and the THD of input currents resulting from both methods are generally similar. Therefore, it can be concluded that when unity power factor and extremely low THD of input current is required, Method 1 provides an ideal solution. Otherwise, Method 3 should be adopted given the simplicity of implementation and acceptable level of performance in terms of power factor and THD of input current. Finally, the dynamic response of the boost PFC pre-regulator implemented with three ripple estimation/cancellation methods was investigated by subjecting it to step load decrease and increase. The results are shown in Fig. 4.11. The time taken for the PFC pre-regulator to reach steady state after step load change is about 38 ms for all three methods. From the above steady-state and the dynamic tests, it can be concluded that all three ripple estimation/cancellation methods offer practical solutions to achieve near-unity power factor and fast dynamic response simultaneously.

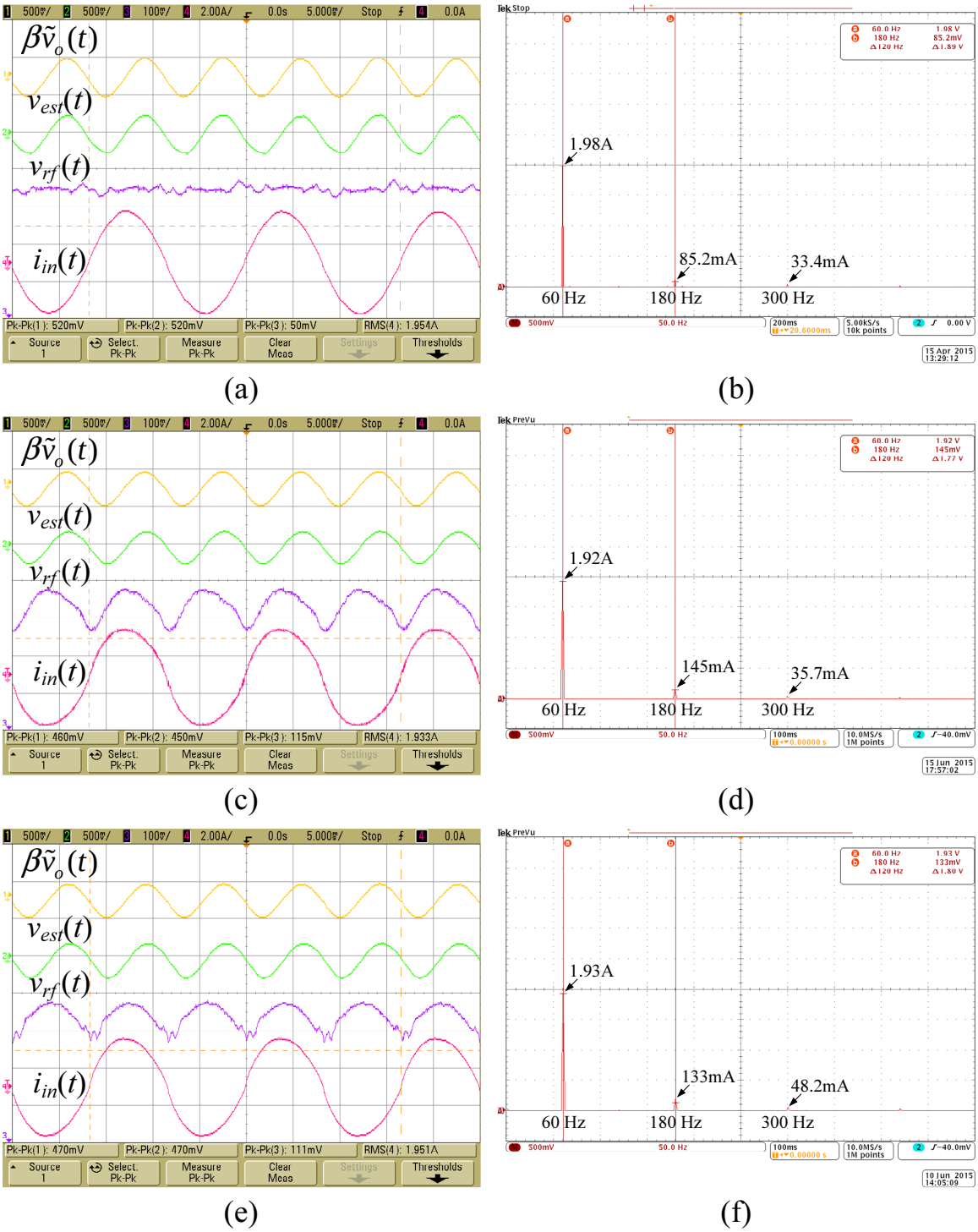


Figure 4.6: Measured input and output waveforms of difference amplifier under nominal condition ($\beta\tilde{v}_o(t)$: sampled output voltage ripple, $v_{est}(t)$: estimated output voltage ripple, $v_{rf}(t)$: output of difference amplifier, $i_{in}(t)$: input or line current) and the FFT spectra of input current under the actions of three ripple estimation/cancellation methods ([(a) and (b)] Method 1: $\rho = 1$ and $\theta_{est} = \theta_o$, [(c) and (d)] Method 2: $\rho = \cos(\theta_{est} - \theta_o)$ and $\theta_{est} \neq \theta_o$, [(e) and (f)] Method 3: $\rho = 1$ and $\theta_{est} \neq \theta_o$).

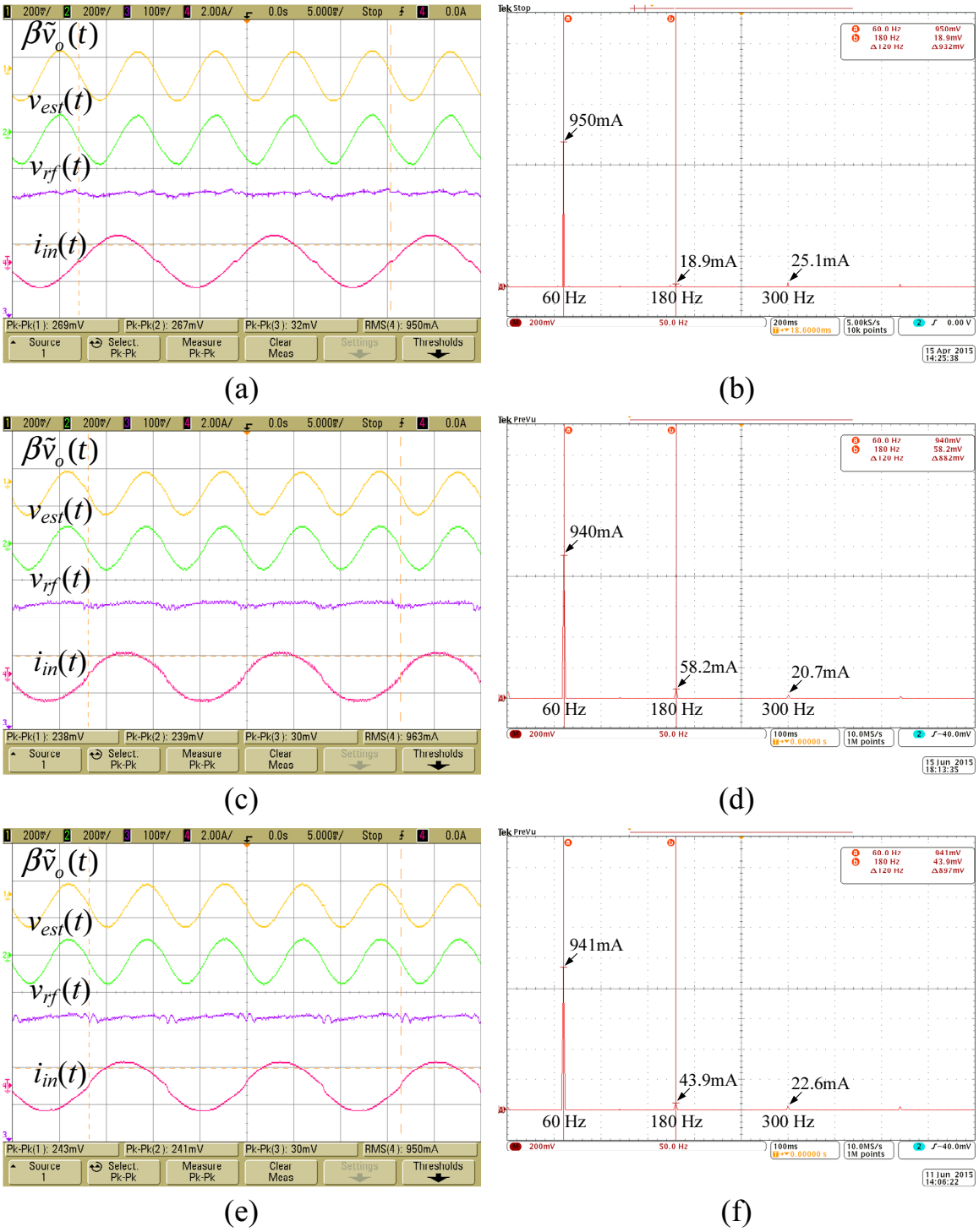


Figure 4.7: Measured input and output waveforms of difference amplifier under half-load condition ($\beta\tilde{v}_o(t)$: sampled output voltage ripple, $v_{est}(t)$: estimated output voltage ripple, $v_{rf}(t)$: output of difference amplifier, $i_{in}(t)$: input or line current) and the FFT spectra of input current under the actions of three ripple estimation/cancellation methods ([(a) and (b)] Method 1: $\rho = 1$ and $\theta_{est} = \theta_o$, [(c) and (d)] Method 2: $\rho = \cos(\theta_{est} - \theta_o)$ and $\theta_{est} \neq \theta_o$, [(e) and (f)] Method 3: $\rho = 1$ and $\theta_{est} \neq \theta_o$).

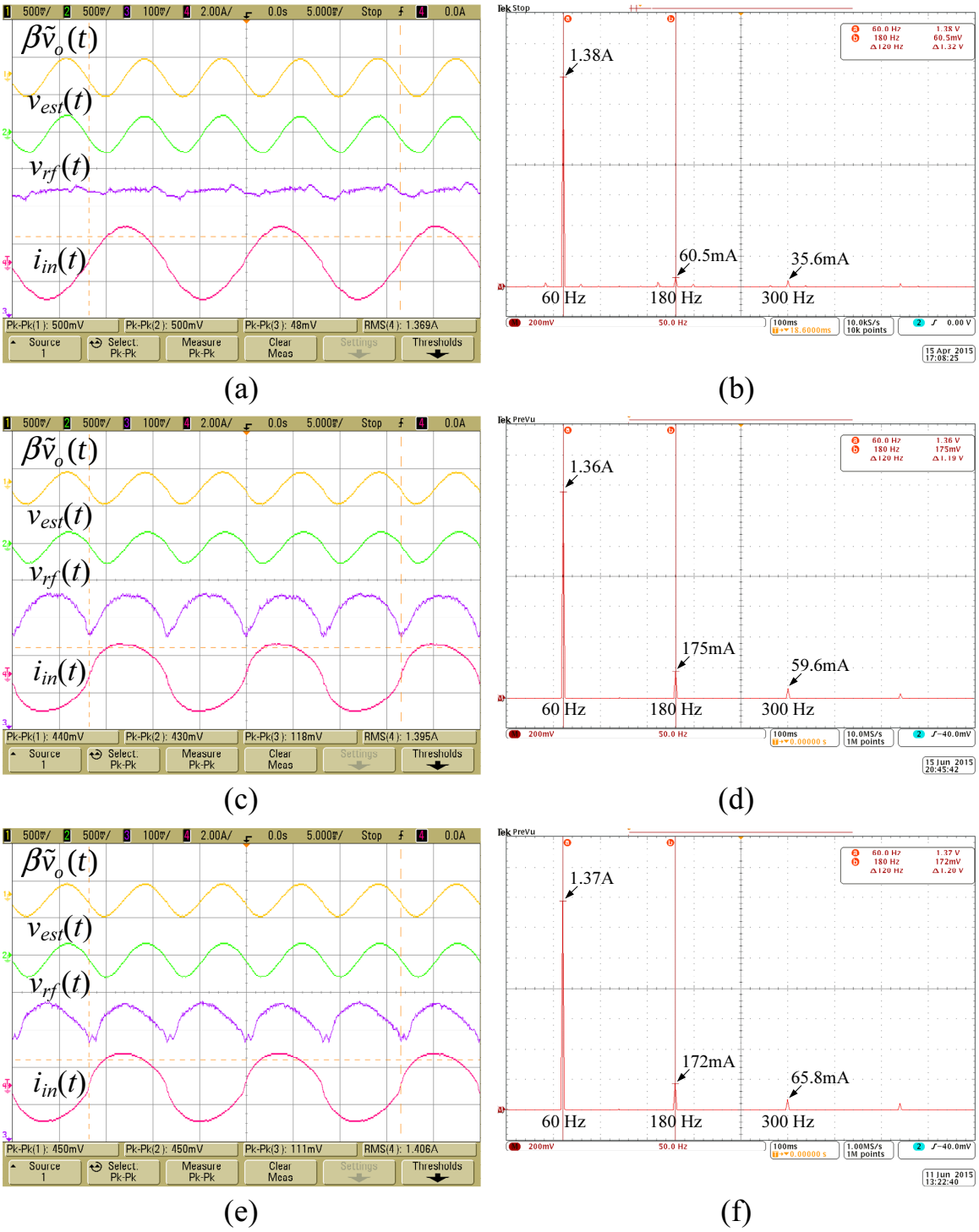


Figure 4.8: Measured input and output waveforms of difference amplifier at V_{in} =150 $V_{\rm rms}$ ($\beta\tilde{v}_o(t)$: sampled output voltage ripple, $v_{est}(t)$: estimated output voltage ripple, $v_{rf}(t)$: output of difference amplifier, $i_{in}(t)$: input or line current) and the FFT spectra of input current under the actions of three ripple estimation/cancellation methods ([(a) and (b)] Method 1: $\rho = 1$ and $\theta_{est} = \theta_o$, [(c) and (d)] Method 2: $\rho = \cos(\theta_{est} - \theta_o)$ and $\theta_{est} \neq \theta_o$, [(e) and (f)] Method 3: $\rho = 1$ and $\theta_{est} \neq \theta_o$).

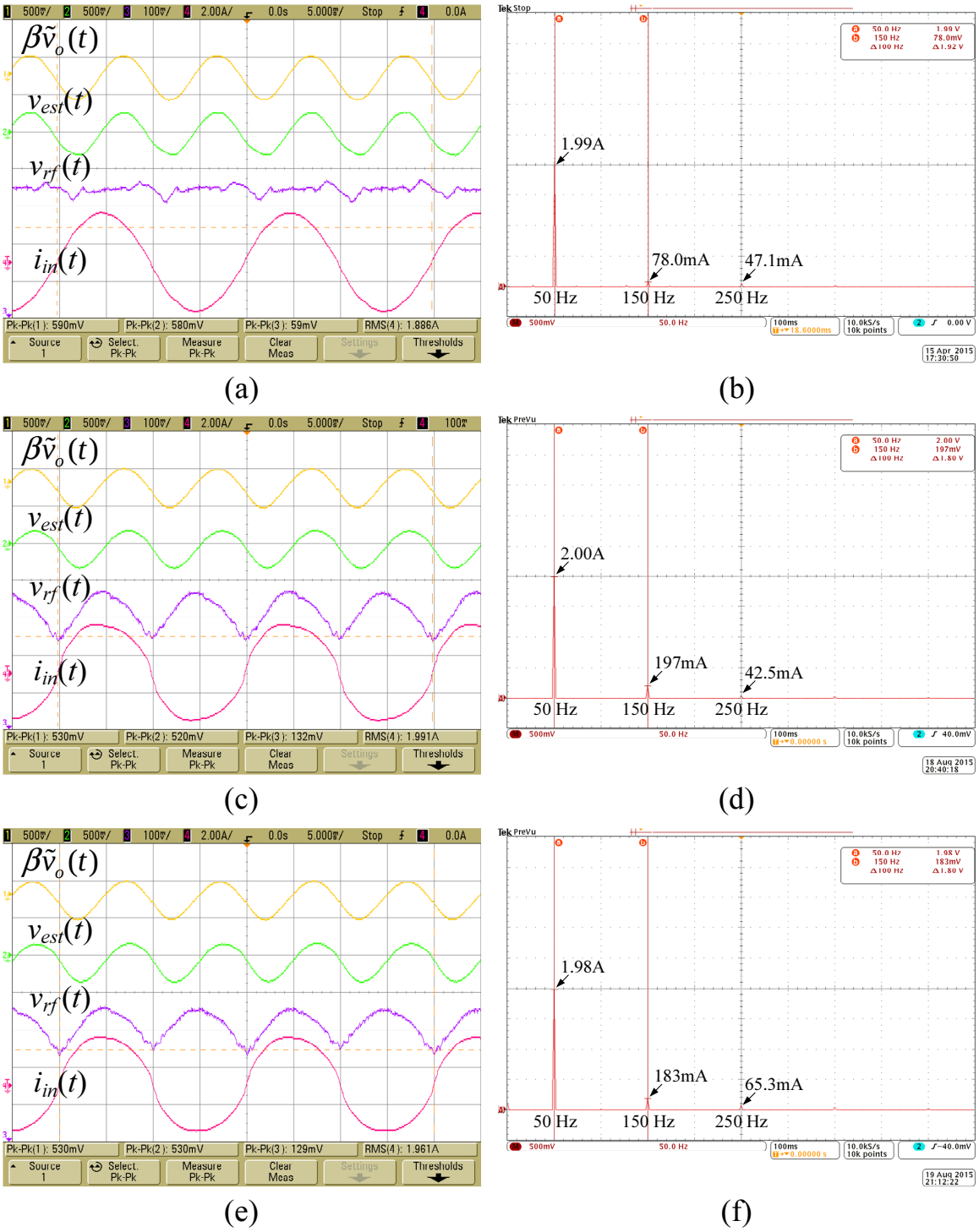


Figure 4.9: Measured input and output waveforms of difference amplifier at f_{line} =50 Hz ($\beta\tilde{v}_o(t)$: sampled output voltage ripple, $v_{est}(t)$: estimated output voltage ripple, $v_{rf}(t)$: output of difference amplifier, $i_{in}(t)$: input or line current) and the FFT spectra of input current under the actions of three ripple estimation/cancellation methods ([(a) and (b)] Method 1: $\rho = 1$ and $\theta_{est} = \theta_o$, [(c) and (d)] Method 2: $\rho = \cos(\theta_{est} - \theta_o)$ and $\theta_{est} \neq \theta_o$, [(e) and (f)] Method 3: $\rho = 1$ and $\theta_{est} \neq \theta_o$).

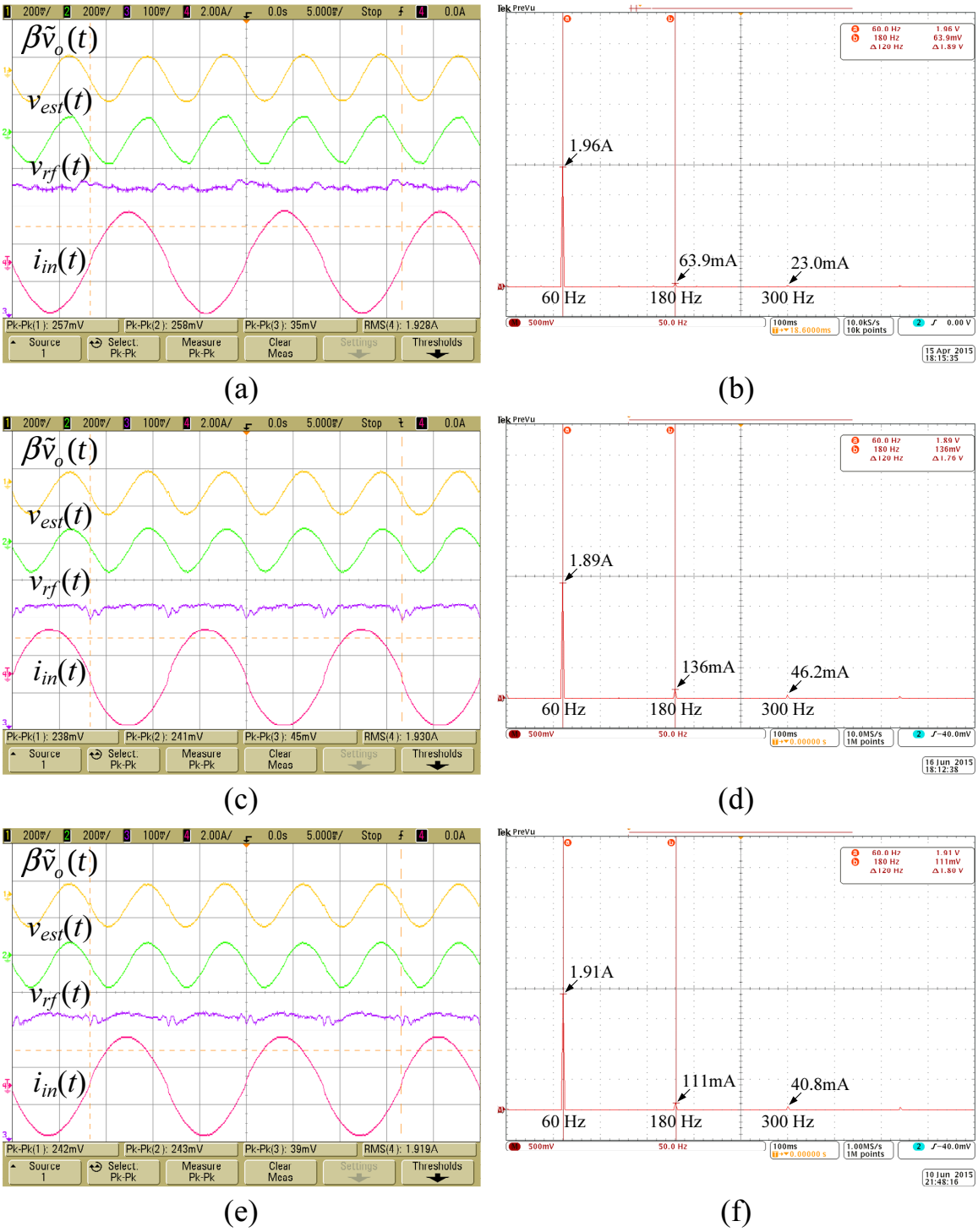


Figure 4.10: Measured input and output waveforms of difference amplifier at C_o =32 μF ($\beta\tilde{v}_o(t)$: sampled output voltage ripple, $v_{est}(t)$: estimated output voltage ripple, $v_{rf}(t)$: output of difference amplifier, $i_{in}(t)$: input or line current) and the FFT spectra of input current under the actions of three ripple estimation/cancellation methods ([(a) and (b)] Method 1: $\rho = 1$ and $\theta_{est} = \theta_o$, [(c) and (d)] Method 2: $\rho = \cos(\theta_{est} - \theta_o)$ and $\theta_{est} \neq \theta_o$, [(e) and (f)] Method 3: $\rho = 1$ and $\theta_{est} \neq \theta_o$).

Table 4.1: Measured amplitudes of ripple signals associated with three ripple estimation/cancellation methods.

		$\lvert\beta\tilde{v}_o(t)\rvert$	$\lvert v_{est}(t)\rvert$	$\lvert v_{rf}(t)\rvert$	**PF**
Nominal condition					
Method 1	$\rho = 1$ $\theta_{est} = \theta_o$	520 mV_{pp}	520 mV_{pp}	50 mV_{pp}	0.999
Method 2	$\rho = \cos(\theta_{est} - \theta_o)$ $\theta_{est} \neq \theta_o$	460 mV_{pp}	450 mV_{pp}	115 mV_{pp}	0.995
Method 3	$\rho = 1$ $\theta_{est} \neq \theta_o$	470 mV_{pp}	470 mV_{pp}	111 mV_{pp}	0.995
Half load					
Method 1	$\rho = 1$ $\theta_{est} = \theta_o$	269 mV_{pp}	267 mV_{pp}	32 mV_{pp}	0.999
Method 2	$\rho = \cos(\theta_{est} - \theta_o)$ $\theta_{est} \neq \theta_o$	238 mV_{pp}	239 mV_{pp}	30 mV_{pp}	0.997
Method 3	$\rho = 1$ $\theta_{est} \neq \theta_o$	243 mV_{pp}	241 mV_{pp}	30 mV_{pp}	0.998
V_{in} =**150** V_{rms}					
Method 1	$\rho = 1$ $\theta_{est} = \theta_o$	500 mV_{pp}	500 mV_{pp}	48 mV_{pp}	0.998
Method 2	$\rho = \cos(\theta_{est} - \theta_o)$ $\theta_{est} \neq \theta_o$	440 mV_{pp}	430 mV_{pp}	118 mV_{pp}	0.990
Method 3	$\rho = 1$ $\theta_{est} \neq \theta_o$	450 mV_{pp}	450 mV_{pp}	111 mV_{pp}	0.991
f_{line} =**50 Hz**					
Method 1	$\rho = 1$ $\theta_{est} = \theta_o$	590 mV_{pp}	580 mV_{pp}	59 mV_{pp}	0.999
Method 2	$\rho = \cos(\theta_{est} - \theta_o)$ $\theta_{est} \neq \theta_o$	530 mV_{pp}	520 mV_{pp}	132 mV_{pp}	0.992
Method 3	$\rho = 1$ $\theta_{est} \neq \theta_o$	530 mV_{pp}	530 mV_{pp}	129 mV_{pp}	0.993
C_o =**32** μ**F**					
Method 1	$\rho = 1$ $\theta_{est} = \theta_o$	257 mV_{pp}	258 mV_{pp}	35 mV_{pp}	0.999
Method 2	$\rho = \cos(\theta_{est} - \theta_o)$ $\theta_{est} \neq \theta_o$	238 mV_{pp}	241 mV_{pp}	45 mV_{pp}	0.995
Method 3	$\rho = 1$ $\theta_{est} \neq \theta_o$	242 mV_{pp}	243 mV_{pp}	39 mV_{pp}	0.997

Table 4.2: Measured total harmonic distortion of input current resulting from three ripple estimation/cancellation methods.

		1st Harmonic	3rd Harmonic	5th Harmonic	THD
Nominal condition					
Method 1	$\rho = 1$ $\theta_{est} = \theta_o$	1.98 A	85.2 mA	33.4 mA	4.62 %
Method 2	$\rho = \cos(\theta_{est} - \theta_o)$ $\theta_{est} \neq \theta_o$	1.92 A	145 mA	35.7 mA	7.78 %
Method 3	$\rho = 1$ $\theta_{est} \neq \theta_o$	1.93 A	133 mA	48.2 mA	7.33 %
Half load					
Method 1	$\rho = 1$ $\theta_{est} = \theta_o$	950 mA	18.9 mA	25.1 mA	3.31 %
Method 2	$\rho = \cos(\theta_{est} - \theta_o)$ $\theta_{est} \neq \theta_o$	940 mA	58.2 mA	20.7 mA	6.57 %
Method 3	$\rho = 1$ $\theta_{est} \neq \theta_o$	941 mA	43.9 mA	22.6 mA	5.25 %
V_{in} =**150 V**$_{\text{rms}}$					
Method 1	$\rho = 1$ $\theta_{est} = \theta_o$	1.38 A	60.5 mA	35.6 mA	5.09 %
Method 2	$\rho = \cos(\theta_{est} - \theta_o)$ $\theta_{est} \neq \theta_o$	1.36 A	175 mA	59.6 mA	13.59 %
Method 3	$\rho = 1$ $\theta_{est} \neq \theta_o$	1.37 A	172 mA	65.8 mA	13.44 %
f_{line} =**50 Hz**					
Method 1	$\rho = 1$ $\theta_{est} = \theta_o$	1.99 A	78.0 mA	47.1 mA	4.58 %
Method 2	$\rho = \cos(\theta_{est} - \theta_o)$ $\theta_{est} \neq \theta_o$	2.00 A	197 mA	42.5 mA	10.08 %
Method 3	$\rho = 1$ $\theta_{est} \neq \theta_o$	1.98 A	183 mA	65.3 mA	9.81 %
C_o =**32** μ**F**					
Method 1	$\rho = 1$ $\theta_{est} = \theta_o$	1.96 A	63.9 mA	23.0 mA	3.46 %
Method 2	$\rho = \cos(\theta_{est} - \theta_o)$ $\theta_{est} \neq \theta_o$	1.89 A	136 mA	46.2 mA	7.60 %
Method 3	$\rho = 1$ $\theta_{est} \neq \theta_o$	1.91 A	111 mA	40.8 mA	6.19 %

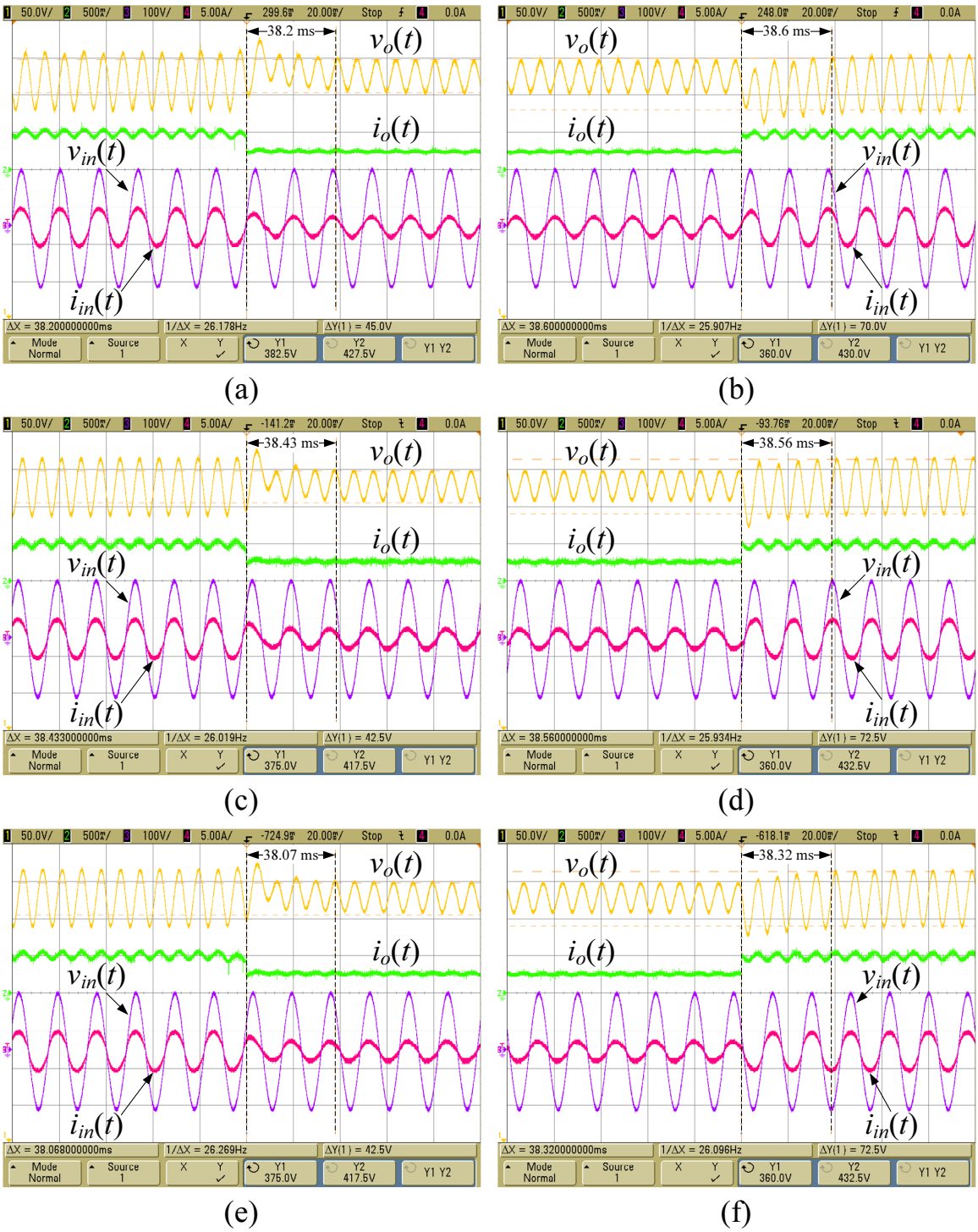


Figure 4.11: Measured input and output waveforms of boost PFC pre-regulator under step decrease [(a),(c) and (e)] and increase [(b), (d) and (f)] in load ([(a) and (b)] Method 1: $\rho = 1$ and $\theta_{est} = \theta_o$, [(c) and (d)] Method 2: $\rho = \cos(\theta_{est} - \theta_o)$ and $\theta_{est} \neq \theta_o$, [(e) and (f)] Method 3: $\rho = 1$ and $\theta_{est} \neq \theta_o$).

4.4 Conclusion

In the beginning of this chapter, the two ripple estimation/cancellation methods proposed in the previous chapters were reviewed. The possibility of obtaining a further simplified ripple estimation/cancellation circuit by means of imposing a fixed amount of phase shift (of 90°) and equalizing the amplitudes of the sampled and estimated output voltage ripples was discussed. By comparing the experimentally measured figures of merit, it was demonstrated that Method 1, which utilizes both amplitude tuner and phase shifter, provides the most accurate estimation under different operating conditions, which leads to undistorted sinusoidal input current of PFC pre-regulator and unity power factor. From the mathematical analysis presented in Chapter 2, the amplitude of the estimated output voltage ripple is suggested to be $\beta V_r \cos(\theta_{est} - \theta_o)$ in order to achieve a minimum local cancellation error and high power factor in the presence of phase estimation error. However, from the simulation and experimental results obtained in this chapter, it was shown that there is no significant difference on the overall power-factor and THD performances of PFC pre-regulator when the estimated output voltage ripple is tuned to $\beta V_r \cos(\theta_{est} - \theta_o)$ or βV_r. Therefore, by taking power-factor performance (or THD performance) and circuit complexity into consideration simultaneously, it is suggested that Method 1 is chosen when strict power factor and THD requirements must be fulfilled. Otherwise, Method 3 provides a simple yet sufficiently good solution for achieving satisfactory power factor and dynamic response performances.

Chapter 5

Conclusions and Suggestions for Future Work

This chapter summarizes the main contributions of this research project and some suggestions for future work will be given.

5.1 Contribution of this thesis

PFC pre-regulators are typically required to have low loop gain's crossover frequency to give sufficient attenuation of the double-line frequency component in the feedback control loop, which is aimed to produce near-unity power factor and low THD of input current. However, the main drawback of this configuration is that the dynamic response of PFC pre-regulator becomes sluggish. Ripple cancellation approach is a solution that aims to eliminate the double-line frequency component in the sampled output voltage by subtracting a replica of the sampled output voltage ripple from the actual one. As a result, input and output signals of the voltage error amplifier are ideally ripple-free, which gives rise to near-unity power factor while the closed-loop bandwidth of the PFC pre-regulator can be kept large. However, the existing ripple estimation methods typically suffer from

the problem of non-adaptivity, the objective of this thesis is to investigate improved ripple estimation/cancellation methods that have high flexibility to adapt to various operating conditions.

From the power balance equation, a generalized equation describing the output voltage of PFC pre-regulator was first obtained. It was found that the output voltage of PFC pre-regulator does not always behave as that suggested by the idealized equation adopted by previous researchers. In order to have a precise ripple estimation/cancellation under a wide range of operating conditions, a new ripple estimation circuit, which consists of a ripple template generator, an amplitude tuner and a phase shifter, both are based on switched-resistor circuits, was proposed. By implementing it in a 200-W boost PFC pre-regulator configured with the closed-loop bandwidth of 60 Hz, it was shown by both simulation and experimental results that the estimated output voltage ripple and the sampled output voltage ripple can be made nearly identical. After subtraction between the two, a near-ripple-free signal was obtained and serves as the input to the voltage error amplifier. It was also shown that the quality of ripple estimation is not degraded under large variations of load, line voltage, line frequency and output capacitor's value. By subjecting the PFC pre-regulator (with and without ripple estimation/cancellation) to various step changes in operating conditions, it was demonstrated that near-unity power factor and low THD of PFC pre-regulator's input current are achieved with the aid of the proposed ripple estimation/cancellation circuit, while the PFC pre-regulator exhibits fast dynamic response with settling time of about 38 ms.

Although near-unity power factor and fast dynamic response of PFC pre-regulator are achievable, high complexity is the major drawback of the proposed ripple estimation/cancellation circuit. In order to simplify the proposed ripple estimation network, the main figures of merit of PFC pre-regulator under the action of ripple cancellation were derived mathematically. From the results obtained, it

was shown that high power factor and low THD of input current can be attained if the estimated output voltage ripple is operated at its optimum amplitude of $\beta V_r \cos(\theta_{est} - \theta_o)$ in the presence of phase estimation error. Besides, since the phase angle of the PFC pre-regulator's output voltage ripple usually approaches 90°, the design of phase shifter involved in the proposed ripple estimation circuit can be simplified. The simplified ripple estimation network was tested experimentally with a 200-W boost PFC pre-regulator as power stage that is designed to have a loop gain's crossover frequency of 60 Hz. It was demonstrated that the phase angle of the estimated output voltage ripple is constantly 90°, while its amplitude is closely tracked to be $\beta V_r \cos(\theta_{est} - \theta_o)$. Although the estimation is not as accurate as that achieved with both amplitude tuner and phase shifter, the amplitude of the sampled output voltage ripple is significantly attenuated before it propagates into the voltage error amplifier. Hence, from the experimental results, it was verified that near-unity power factor and weakly-distorted input current are attained by means of the simplified ripple estimation network.

After deriving the previous two ripple estimation methods (labelled as Method 1 and 2, respectively), another ripple estimation method (labelled as Method 3) was developed to employ an amplitude tuning method that promotes further reduced complexity. While the phase angle of the estimated output voltage ripple is 90°, its amplitude is tuned to βV_r instead of $\beta V_r \cos(\theta_{est} - \theta_o)$ as with Method 2. Among the three methods, the configuration of Method 3 is the simplest since it essentially consists of an amplitude tuner only. By comparison of experimentally measured figures of merit, it was found that the first ripple estimation method, which consists of separate amplitude tuner and phase shifter, provides the most accurate ripple estimation/cancellation under a wide range of operating conditions, which results in near-unity power factor and input current with very low THD. Although there are some estimation errors produced by Method 2 and 3, they do not cause a significant degradation in power factor of PFC pre-regulator

and the input current waveform. From the operating waveforms of difference amplifier and the measured input current obtained with Method 2 and 3, it was demonstrated that the overall performances of these two methods are similar. Hence, it can be concluded that Method 1 is an ideal solution when unity power factor and an input current with extremely low THD are required. Otherwise, Method 3 should be adopted since it provides a simple yet sufficiently good solution for achieving satisfactory power factor and dynamic response performances.

5.2 Suggestions for Future Work

Besides the conventional 50–60 Hz utility applications, PFC pre-regulators are used in airborne systems operating at 350–800 Hz for compliance with more restricted regulations, such as RTCA DO-160, which demand an extremely low THD of input current. Besides the problem of input current distortion around the zero crossings of input voltage, PFC pre-regulators in these applications are required to have an undistorted sinusoidal input current while exhibiting fast dynamic response. As discussed, Method 1 produces THD of input current that is extremely low over a wide range of operating conditions. Hence, this ripple estimation method is highly preferred for airborne systems that require both undistorted input current and fast dynamic response performances.

In this work, the performances of PFC pre-regulator (with and without ripple estimation/cancellation) have been investigated for resistive load only. In some applications, PFC pre-regulators are utilized to power non-linear loads, such as LEDs. To conduct a comprehensive analysis of the performance of the proposed ripple estimation methods, non-linear loads should be used and tested experimentally. LEDs will serve as a good choice of non-linear load due to their non-linear voltage-current characteristic that is sensitive to ambient conditions, with which the robustness of the proposed ripple estimation methods can be subjected to

more stringent tests.

As presented, the main challenge in realizing a notch filter using analog circuit is that the quality of the notch filter will be degraded in the presence of component tolerances. Since variable effective resistance can be achieved by the method of switched resistor, the effects of component tolerances can be compensated by replacing fixed resistors by switched-resistors in analog notch filter. With this modification, high quality factor and accurately-tuned notch frequency can be obtained.

Appendix A

Low-Frequency Small-Signal Model of Ideal PFC Pre-regulator

The small-signal model and transfer function of PFC pre-regulator are derived as follows. As usual, in small-signal analysis, all switching processes are averaged over a complete half-cycle of the input voltage. Hence, the input voltage of PFC pre-regulator is considered as dc source having an amplitude corresponding to its root-mean-square (rms) value.

Fig. A.1 shows the standard configuration of a boost PFC pre-regulator under ACM control. Before deriving its small-signal model and transfer function, some assumptions need to be made:

- The bandwidth of the inner current control loop is much wider than that of the outer voltage control loop, which causes the sensed inductor current to closely track its reference signal.

- The output voltage of PFC pre-regulator is assumed to be constant over one switching cycle.

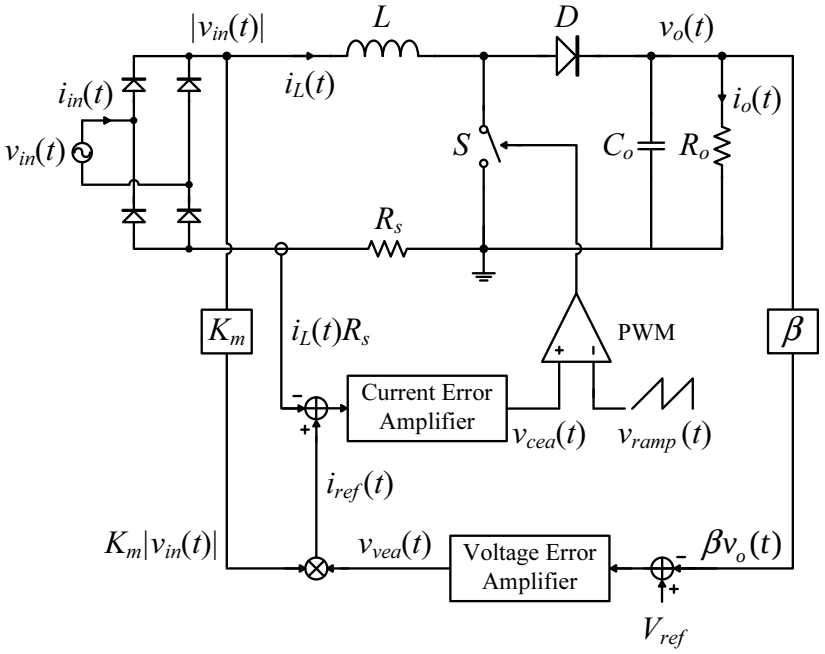


Figure A.1: Configuration of standard boost PFC pre-regulator with ACM control.

- All components are ideal.

Assume that the PFC pre-regulator is operating with an efficiency of 100 %, hence from the principle of power balance,

$$V_{irms} I_{irms} = V_o I_o \tag{A.1}$$

where V_{irms} and I_{irms} are the rms values of PFC pre-regulator's input voltage and input current, respectively, and the average output voltage and average output current of the PFC pre-regulator are denoted by V_o and I_o, respectively.

Since the reference signal for the PFC pre-regulator's input current is obtained by multiplying the output signal of voltage error amplifier with the sampled rectified input voltage $K_m V_{irms}$, the PFC pre-regulator's input current can be described by Eq. (A.2), where K_m and R_s is the line-voltage step-down ratio and the current sense resistor's value, respectively, and V_{vea} is the average value of

the voltage error amplifier's output signal.

$$I_{irms} = \frac{K_m}{R_s} V_{irms} V_{vea} \tag{A.2}$$

By substituting Eq. (A.2) into Eq. (A.1), Eq. (A.3) is obtained.

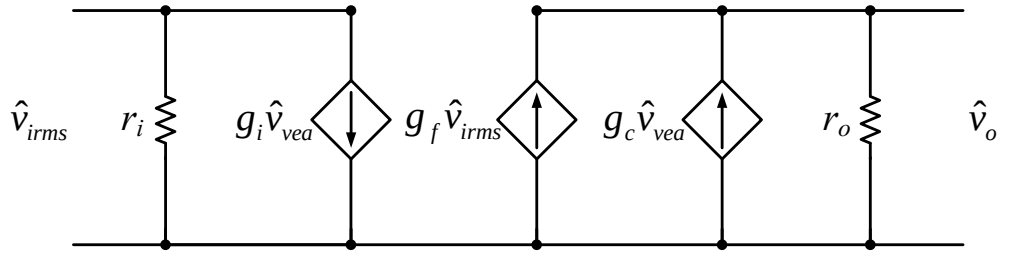
$$\frac{K_m}{R_s} V_{irms}^2 V_{vea} = V_o I_o \tag{A.3}$$

By introducing small perturbations into the variables in Eq. (A.2) and Eq. (A.3) and, subsequently, eliminating the DC and the second-order terms, two small-signal equations of PFC pre-regulator can be obtained as described by Eq. (A.4) and Eq. (A.5), which leads to the small-signal model depicted in Fig. A.2. Based on the small-signal model, the control-to-output transfer function of the PFC pre-regulator can be obtained as given by Eq. (A.6), assuming that the perturbation to input voltage $\hat{v}_{irms}$ is zero.

$$\hat{i}_{irms} = \left(\frac{K_m}{R_s} V_{vea}\right) \hat{v}_{irms} + \left(\frac{K_m}{R_s} V_{irms}\right) \hat{v}_{vea} \tag{A.4}$$

$$\hat{i}_o = \left(\frac{K_m}{R_s} \frac{V_{irms}^2}{V_o}\right) \hat{v}_{vea} + \left(2\frac{K_m}{R_s} \frac{V_{irms} V_{vea}}{V_o}\right) \hat{v}_{irms} - \left(\frac{I_o}{V_o}\right) \hat{v}_o \tag{A.5}$$

$$\frac{\hat{v}_o}{\hat{v}_{vea}} = \frac{K_m}{R_s} \frac{V_{irms}^2}{V_o} \frac{R_o}{2} \frac{1}{1 + s\frac{C_o R_o}{2}} \tag{A.6}$$



$$r_i = \frac{R_s}{K_m V_{vea}} \qquad r_o = \frac{V_o}{I_o}$$

$$g_i = \frac{K_m V_{irms}}{R_s} \qquad g_f = \frac{2K_m V_{irms} V_{vea}}{R_s V_o} \qquad g_c = \frac{K_m V_{irms}^{\ 2}}{R_s V_o}$$

Figure A.2: Small-signal model of boost PFC pre-regulator with ACM control.

Appendix B

List of Components

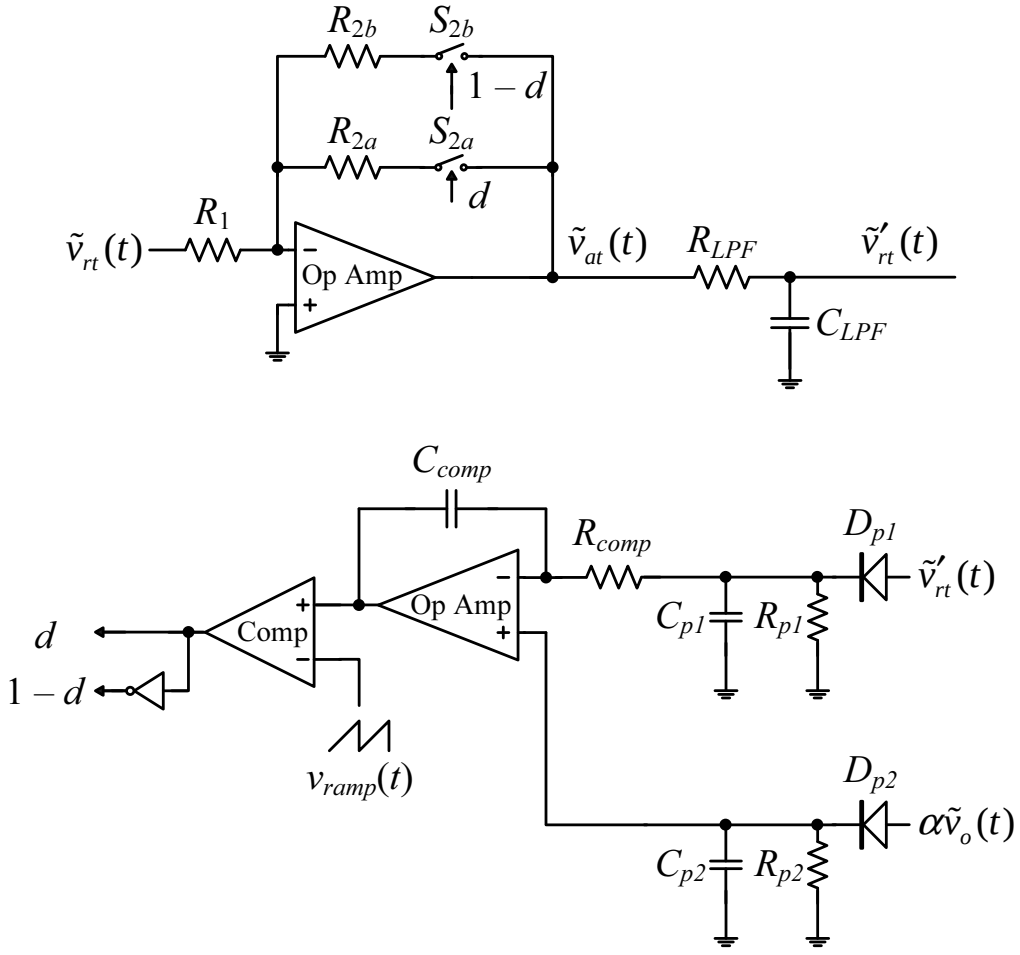


Figure B.1: Schematic diagram of the proposed amplitude tuner.

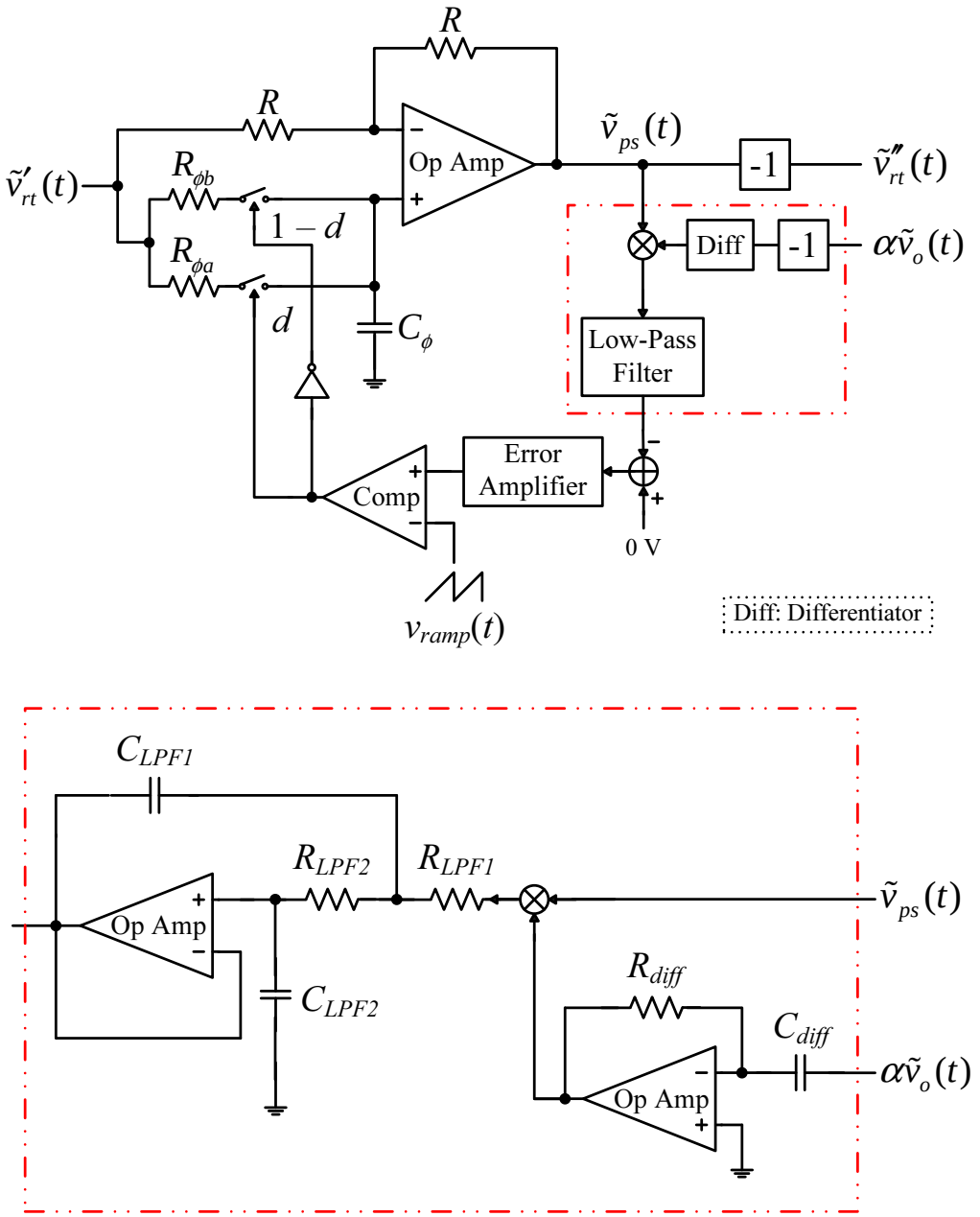


Figure B.2: Schematic diagram of the proposed phase shifter.

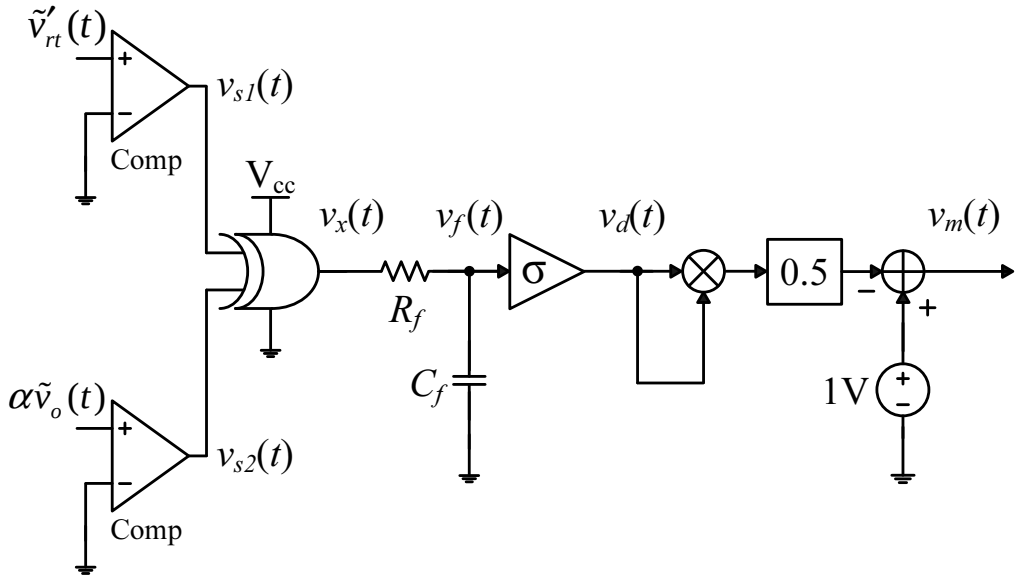


Figure B.3: Schematic diagram of the proposed phase difference detector.

Table B.1: List of components.

Amplitude tuner [refer to Fig. B.1]	
Name	**Value**
R_1	300 Ω
R_{2a}	1.2 $k\Omega$
R_{2b}	90 Ω
R_{LPF}	800 Ω
C_{LPF}	0.22 μF
D_{p1}, D_{p2}	1N4001
R_{p1}, R_{p2}	12 $k\Omega$
C_{p1}, C_{p2}	2.2 μF
R_{comp}	8 $k\Omega$
C_{comp}	2.2 μF
Operational amplifier, Op Amp	TL082
Comparator, Comp	LM311
Phase shifter [refer to Fig. B.2]	
Name	**Value**
R	10 $k\Omega$
$R_{\phi a}$	300 Ω
$R_{\phi b}$	31.6 $k\Omega$
C_{ϕ}	680 nF
R_{diff}	1.33 $k\Omega$
C_{diff}	1 μF
R_{LPF1}, R_{LPF2}	10 $k\Omega$
C_{LPF1}	0.56 μF
C_{LPF2}	0.27 μF
Operational amplifier, Op Amp	TL082
Comparator, Comp	LM311
Phase difference detector [refer to Fig. B.3]	
Name	**Value**
R_f	2.43 $k\Omega$
C_f	4.7 μF
Comparators, Comp	LM393
Exclusive-or (XOR) gate	CD4030

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