THE STUDY OF SILICON/ POLY(3,4-ETHYLENEDIOXYTHIOPHENE): POLY(STYRENESULFONATE) (PEDOT:PSS) HYBRID SOLAR CELLS

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The Study of Silicon/Poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS) Hybrid Solar Cells

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CERTIFICATE OF ORIGINALITY

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ABSTRACT

Polymer/silicon hybrid solar cells have been introduced to tackle the expensive fabrication problem of conventional p-n junction silicon solar cells. The idea arisen in the polymer/silicon hybrid solar cells is that by replacing the high temperature processed silicon doping layer (by diffusion) to a low temperature processed polymeric layer. By eliminating the diffusion step of the p-n junction, it has been estimated that energy input into the solar cell production process could be 35% lower. The polymer/silicon hybrid solar cells have the advantages of low equipment cost and low temperature fabrication to cut down the expensive cost in the conventional silicon solar cells.

However, organic materials are less efficient than inorganic materials. The best power conversion efficiency of polymer/silicon hybrid solar cells is lower than that of conventional p-n junction silicon solar cells. Some factors have been hindering the performance of the polymer/silicon hybrid solar cells. Therefore, the aim of this work attempts to explore some methods to enhance the power conversion efficiency of the polymer/silicon hybrid solar cells. In this thesis, (i) a surface texturization structure was adopted for the silicon layer and (ii) an acid treatment was applied for the polymer layer. These approaches may be of importance in achieving better carrier separation and collection in the hybrid solar cells. Moreover, the efficiency enhancing methods are simple and low cost, that are favorable to be used without paying a huge extra cost.

Firstly, poly(3,4-ethylenedioxythiophene):poly(4-styrenesulfonate) (PEDOT:PSS) was used for the polymer layer in the hybrid solar cells because of its high work function and convenient solution processibility. The polymer/silicon hybrid solar cells with ITO/PEDOT:PSS/Silicon/GaIn architecture were fabricated. The silicon/PEDOT:PSS junctions were processed at 110 ºC in air with a spin-coating and a wet etching process. Advanced equipment (high temperature and high vacuum) was not necessary. The elimination of the high temperature manufacturing step proposed a way to achieve inexpensive solar cells. Furthermore, with the aim of improving the charge collection at the solar junction, the silicon nanowires (SiNWs) array was utilized to lower the optical reflection from the shiny planar silicon surface. The power conversion efficiency (PCE) of the solar cell was improved from 1.1% to 6.67% by converting the planar silicon surface into the 390 nm height SiNWs array at the solar junction by the metal assisted electroless etching method. The optimal length of SiNWs in the experiments was around 390 nm. There was an optimal length for the SiNWs array because the polymeric PEDOT:PSS aggregated at the top portion of the long SiNWs array but could not infiltrate into the interspacing between the long SiNWs array. In the long SiNWs solar cells, poor carrier collection as well as high recombination rate suppressed the PCE to improve further.

Secondly, the low conductivity of pristine PEDOT:PSS film has been a limitation for high efficiency devices. The low conductivity of PEDOT:PSS is due to the insulating PSS matrix attracted between the conductive PEDOT grains. Hence, the conductive PEDOT grains are separated by the PSS and become less interlinking.

It was reported that the positive charged hydrogen atoms in the formic acid could neutralize the negative charged PSS chains. The absence of coulombic attraction between the positively charged PEDOT chains and neutral PSSH chains resulted in the phase segregation between PEDOT and PSS and hence the conductivity of PEDOT:PSS film was enhanced after the formic acid treatment. Therefore, the formic acid treated PEDOT:PSS film was used to improve the PCE of silicon nanowires/PEDOT:PSS hybrid solar cells. The formic acid treatment suppressed the reverse saturation current and reduced the series resistance of the hybrid solar cells. Finally, a 16.4% PCE enhancement was recorded after the formic acid treatment.

Thirdly, this study also showed that thin silicon sheets were applicable to fabricate flexible hybrid silicon/PEDOT:PSS hybrid solar cells. Thin silicon sheets not only provided higher bending flexibility of the solar cells but also allowed less use of silicon material. The flexible 15 μm silicon sheet/PEDOT:PSS hybrid solar cell yielded a PCE of 5.56%. We employed a bending test apparatus to study their bending stability. Bending cycle test showed a good recovery of the original efficiency after 5000 cycles under a bending radius of 7 mm that the estimate bending stress in the silicon sheet was around 217 MPa. The ability of bending repeatedly without varying much in the power conversion efficiency of the solar cells hold a significant importance for the development in the lightweight and rollable applications.

Last but not the least, moisture is always a challenge for most of the organic materials. With the help of an environmental chamber to control the humidity level, lower relative humidity would cause slower device degradation. By comparing the

devices' overall performances with the individual study of the ITO, silicon nanostructure and PEDOT:PSS layer, we confirmed that the major causes of the PCE drop in the degraded devices were due to the decrease of the PEDOT:PSS conductivity and the increase of the ITO interface resistance. The results suggested that humidity is a critical degradation factor in the hybrid silicon/PEDOT:PSS solar cells. We also demonstrated that the efficiency of the device could be almost recovered by re-depositing the fresh PEDOT:PSS layer onto a fresh ITO and recycling the silicon in the degraded device.

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CHAPTER 1 INTRODUCTION

1.1. Motivation

Fossil fuels are well-established sources to produce electrical energy. However, pollutants emitted from burning fossil fuels are harmful to human health. Figure 1.1 shows the dominant emitters from power plants are mercury, acid gases and many toxic metals [1]. Moreover, around 21.3 billion tons of greenhouse gases (carbon dioxide CO_2) are produced from burning of fossil fuels in power plants every year [2]. The emitted CO_2 can lead to climate change such as extremely hot and cold weather, increased mean sea level, flooding, loss of crop yield as well as the earthquakes, may even bring economical loss or disasters.

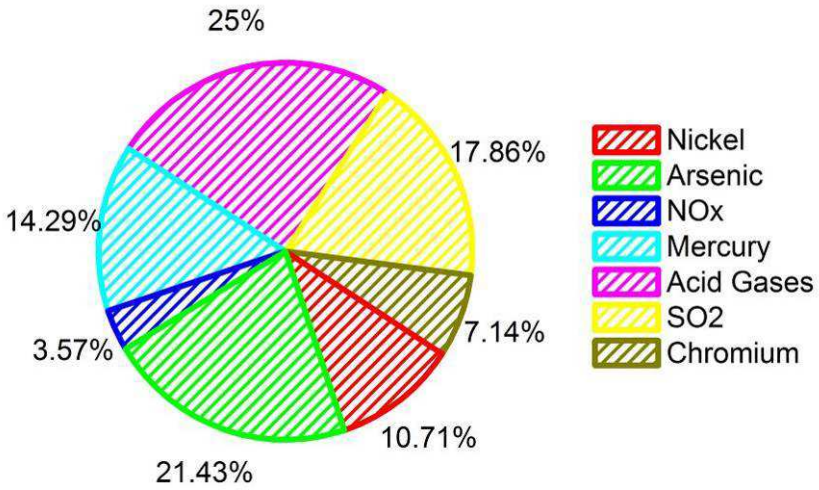


Figure 1.1 A pie chart showing the pollutants emitted from the power plant.

Despite fossil fuels cause pollution problem and climate change, it is still difficult to stop using them because our growing demand for electrical energy. The United State Energy Information Administration foresees that the world energy consumption will grow by 56% between 2010 and 2040 [3]. On the contrary, oil, coal and natural gas, together supplying 85% of the world's energy supply, are just enough to last 42, 133 and 61 years respectively [4]. We should aware that fossil fuels are non-renewable energy sources and they will be used up in the near future.

Therefore, the generation of clean and renewable energy sources as alternatives to fossil fuels not only help retarding the pollution problems but also meet the increased energy need. Photovoltaic energy is a promising candidate because sunlight is abundant around us. Photovoltaic is also a safe method for electricity generation different from nuclear power plant in which radioactive waste is danger and causes long-term disposal problems. Furthermore, solar electricity can make localized with the electrical appliances to avoid the transmission power losses over long distances from large power plants to the consumers via extensive cables and networks [5].

The application of photovoltaic devices to produce electricity will become more important in the coming decades. The European Union has already set a goal of meeting 20% of energy demand through the use of renewable sources by 2020, in which 12% of the electricity produced from photovoltaic power [6]. Moreover, a large solar energy project has been planned in India to produce 5 gigawatts of power [7]. For photovoltaic energy, conventional p-n junction crystalline silicon solar cells

have attractive features of their good (up to 25%) power conversion efficiency as well as sophisticated and well-developed device fabrication techniques. Crystalline silicon solar cells are currently dominating with 80% [8] in current photovoltaic market because of their clean energy production with low environmental impact, non-toxicity, and abundant in silicon material. But the limitations of their high temperature doping process and low throughput manufacturing steps result in expensive energy cost and advanced equipment investment that hindered the progress of photovoltaics.

1.2. This work

As aforementioned, silicon-based solar cells are efficient but they are expensive to produce that limited their applications. The direct costs for solar and coal are 18.12 and 3.14 cents per kilowatt hour respectively [9]. Energy generated from light is nearly 6 times more expensive than that from coal.

One of the strategies to reducing the cost of solar cells is to eliminate the high temperature steps in solar cell fabrication. Conventional p-n junction silicon solar cells require diffusion or ion implantation to control the amount of dopants into the semiconductors and to alter the conductivity type. For the common dopants, such as boron, arsenic and phosphorus, their diffusion temperature range is between 800 and 1200 °C [10] and the diffusion step should be processed in an ultra-clean furnace. This solar cell fabrication involves expensive energy cost and high capital cost. By eliminating the p-n diffusion step, it is estimated that energy input into the solar cell

production process is 35% lower [11]. Besides, the elimination of the high temperature steps in solar cell fabrication offers many advantages [12]: First, the activation of silicon wafers' impurities under high temperature can be avoided, preventing the reduction of minority carrier lifetimes and device efficiency. Second, the low temperature fabrication will be compatible to the trend of using thin silicon substrates. Low temperature process can avoid the undesirable warping effects and low thermal stresses in thin silicon.

Another strategy to reducing the cost of solar cells is to reduce the expensive material cost. Thinner wafers are being increasingly developed in silicon technology. For instance, double side polished wafers and single side polished wafers as thin as 8-10 μm and 90 μm respectively have been supplied commercially having diameter ranging from 25.4 to 150 mm [13]. Around 40% of the module cost is attributed to the silicon wafer cost. The cell cost can be lowered to $0.3/W per volume production by 25 μm ultra-thin silicon semiconductor on metal substrates [14].

It would be attractive to implement convenient fabrication approaches to cut down the expensive energy cost and yet high power conversion efficiency for the silicon based solar cells. Low-cost high-efficiency photovoltaics can be potentially achieved with the emergence and commercialization of conducting polymer which is usually processed by simple spin-coating from aqueous solution at room temperature. Organic polymeric materials enable large area production in a cost-effective manner by solution process or printing technique. These techniques have low energy and temperature demand compared to conventional semiconductor diffusion process and can reduce cost by a factor of 10 or 20 [15]. Moreover, their low temperature

fabrication is compatible with a variety of substrates, especially the flexible plastic substrate which is favorable in the high throughput roll-to-roll technology.

The basic concept underlying any photovoltaic device is charge separation by a built-in electric field at the junction (or interface). Band engineering together with this basic concept, a "hybrid silicon/polymer solar cell" is an alternative choice to the conventional p-n junction silicon solar cell. The main difference between "hybrid silicon/polymer solar cell" and the conventional p-n junction silicon solar cell is at the junction (or interface). For the former, junction is formed between silicon and polymer by spin-coating polymer onto the silicon substrate at room temperature. For the latter, junction is formed between p-type silicon and n-type silicon by high temperature diffusion of acceptor dopants into the n-type silicon substrate. Hence, the fabrication of silicon/polymer hybrid solar cell does not require high temperature processing like diffusion. The idea in this hybrid silicon/polymer junction is that by replacing the inorganic doped silicon layer (by diffusion) to a polymeric semiconductor layer (by spin-coating). In this way, the processing cost is reduced with the silicon/polymer hybrid solar cell.

The "hybrid silicon/polymer solar cell" combines advantages of both organic (polymer) and inorganic (silicon) semiconductors. The hybrid cell consists an organic material such as the conjugated polymer that transports holes. Inorganic silicon is used for the light absorption material in the hybrid cell. The hybrid photovoltaic devices have advantages of not only low-cost solution processing but also possible for flexible solar power applications.

1.3. Objectives

The aim of this study is to explore efficient silicon solar cells in a low-cost approach. The specific objectives of this thesis are:

1. To improve the power conversion efficiency in silicon/PEDOT:PSS solar devices by solving the problems such as high light reflection from silicon surface and low conductivity of polymer.
2. To investigate the bending flexibility and the humid stability of the silicon/PEDOT:PSS solar devices. Thin film silicon substrates are utilized in the fabrication of flexible silicon/PEDOT:PSS solar devices.

1.4. Thesis Overview

In this work, hybrid silicon/PEDOT:PSS heterojunction solar cells are studied for the photovoltaic application. This thesis contains eight chapters and they are organized as follows.

In chapter 2, the silicon/PEDOT:PSS heterojunction is introduced. The underlying physics of the semiconductor and the operating principle of the silicon/PEDOT:PSS heterojunction solar cells are described. The recent developments of silicon/PEDOT:PSS solar cells are also reviewed.

In chapter 3, the materials preparation and experimental setups for the hybrid solar cells are summarized. The physics for the hybrid silicon/PEDOT:PSS solar

cells is described with the aid of the energy band diagram for a better understanding of the device's photovoltaic mechanism. A characteristic model which is used to analyze the photovoltaic parameters of the solar cell is described as well. Also, the characterization methodologies in this work are introduced, which include Scanning Electron Microscopy (SEM), Transmission Electron Microscopy (TEM), Atomic Force Microscopy (AFM), solar simulation and Current density-Voltage (J−V) measurement, Capacitance-Voltage (C−V) measurement, reflectance and transmittance measurement, four probes resistivity testing and thin film thickness measurement.

In chapter 4, silicon wafers are purchased as the starting material. The as-received silicon wafers are usually planar and surface-polished because the current electronics industries rely on the planar technology to build a vast array of high precision and complex integration circuit chips on one wafer simultaneously [16]. However, the shiny planar silicon surface reflects a large portion of light due to the high reflective index of silicon (reflective index of silicon = 3.42). The silicon solar cells with planar silicon surface suffer high optical loss problem. To address this issue, we texture the silicon surface from planar into nanowires morphology by metal assisted electroless etching method to reduce the optical reflectance. In addition, the optimal length of nanowires for the hybrid silicon/PEDOT:PSS solar cells is revealed in this chapter.

In chapter 5, the low conductivity problem of pristine PEDOT:PSS is investigated. The low conductivity of the PEDOT:PSS can suppress the carrier collection, promote joule heating induced lifetime reduction and lower the device

efficiencies. This chapter studies the effect of different concentration of formic acid treatment on the power conversion efficiency (PCE) of the silicon nanowires/ PEDOT:PSS hybrid solar cells. After the treatment, the conductivity of the PEDOT:PSS film enhances around two times and PCE enhances 16.4%.

In chapter 6, flexible silicon nanowires/PEDOT:PSS hybrid solar cells are implemented by overcame the limitation of brittle property of monocrystalline silicon wafers. Normally, the brittle property of silicon wafers makes them difficult to curvature. By thinning the silicon wafers to a few to a few ten micrometer thickness using the potassium hydroxide solution etching method, flexible silicon/PEDOT:PSS hybrid solar cells are fabricated on polyethylene terephthalate (PET) plastic substrates and the photovoltaic performances are studied. In addition, bending cycle tests are carried out to understand the bending stability of the flexible hybrid solar cells.

Humidity has long been the enemy to optoelectronic devices. In chapter 7, the effects of humidity on the photovoltaic performance of the silicon nanowires/ PEDOT:PSS hybrid solar cells are studied. The hybrid solar cells are kept in different levels of relative humidity that controlled by an environment chamber. The power conversion efficiencies of the hybrid solar cells are recorded periodically to obtain a trend of degradation due to humidity. Furthermore, the reasons for the degradation of the devices are investigated.

In chapter 8, a summary of all the results in this project are drawn. Some ideas on the possible future work will also be presented in this chapter.

CHAPTER 2 LITERATURE REVIEWS

2.1. Introduction

In the current chapter, underlying physics of semiconductors is used to explain how silicon solar cells can convert light energy to electrical energy. It is worth noting that conventional p-n junction and Schottky junction are two important concepts in photovoltaic devices. Then, we will be familiar with the architecture and operation principle of the hybrid silicon/PEDOT:PSS heterojunction solar cells. Low cost fabrication techniques are introduced. Finally, we will discuss the progress and limitation of the current hybrid silicon/PEDOT:PSS solar cells.

2.2. The physics of silicon solar cells

The electrical conductivities of semiconductor materials are between conductors and insulators. At zero Kelvin, pure silicon behaves like an insulator. The semi-conductivity of silicon can be modified by the addition of impurities during manufacturing so that it can partially conduct electricity for different types of applications. When the addition of impurities is high enough, it can even behave like a conductor. Silicon is a widely used semiconductor in photovoltaics, optoelectronics

and integrated circuit devices.

2.2.1. N-type and p-type silicon

Silicon can be n-type or p-type, determining by the type of impurities in the lattice structure of the semiconductor crystal. Common p-type impurity materials include boron, aluminum, indium and n-type impurity materials include phosphorus, arsenic and antimony [17].

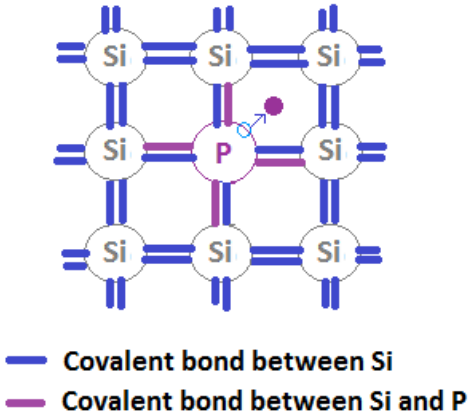
The common n-type impurities have five outermost electrons. Four of them combine with silicon atoms, while the fifth electron can move freely to transport charges in the lattice (Figure 2.1(a)). N-type semiconductors are electrically neutral. The positively charged impurities are fixed in the lattice and emitted free electrons. As the free electrons can move freely with relatively low energy into the conduction band of silicon, this little energy is schematically represented by a "donor energy level" near the conduction band edge of silicon (Figure 2.1(b)). When more impurities are added, this donor energy band gap to overcome will be smaller so that the conductivity of the semiconductor increases.

Similarly, the common p-type impurities have only three outermost electrons. Holes are leaving near the valence band of silicon atoms. In this way, the holes can be filled by the mobile electrons in the valence band of silicon (Figure 2.2(a)). The holes movement can be interpreted by the opposite movement direction to the electrons. With the acceptation of electrons from silicon atoms, the impurities become negatively charged. Electrons from the valence band of the silicon occupy

the holes at low energy that is denoted by an "acceptor energy level" (Figure 2.2(b)). The "donor energy level" and "acceptor energy level" are also called the Fermi level of n-type and p-type silicon respectively.

For n-type semiconductors, free electrons are named as majority carriers, and holes are named as the minority carriers. For p-doped semiconductors, the free holes are the majority carriers, electrons are the minority carriers.

(a)



(b)

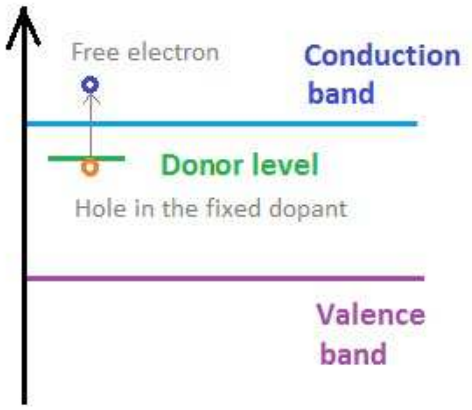


Figure 2.1 (a) A free electron is emitted from phosphorous (b) Donor level is near the conduction band in the n-type semiconductor (Modified from [17]).

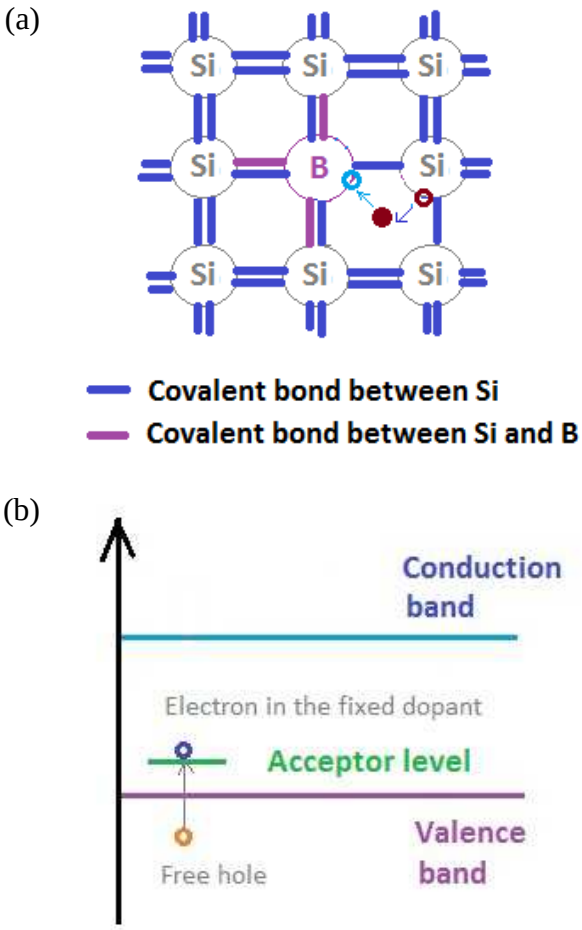


Figure 2.2 (a) A neighborhood electron moves to fill the vacancy of hole in the boron-doped silicon. A new hole is formed at the original location of the electron. (b) Acceptor level is near the valence band in the p-type semiconductor (Modified from [17])

2.2.2. P-N junction

In the operation of a solar cell, the generation of the electrical current from the sun's photons energy relies on an intrinsic electric field to separate charges. So, how can this electric field be provided? One of the major components in the silicon solar

cell is the "p-n junction". A p–n junction is the interface between a p-type and a n-type semiconductor, as shown in Figure 2.3. This junction can be made by diffusion at high temperature from 800 to 1200 ºC or ion implantation by the bombardment of a high-velocity beam. In diffusion process, the dopant impurties move from the surface into silicon substitutionally or interstitially under high temperature [18]. In ion implantation process, the dopant atoms are forced to add into silicon by high energetic ion beam bombardment [18]. Figure 2.4 and Figure 2.5 are the schematic diagrams showing the diffusion systems and the ion implanter respectively. Photos of the equipment for diffusion process and ion implantation are shown in Figure 2.6.

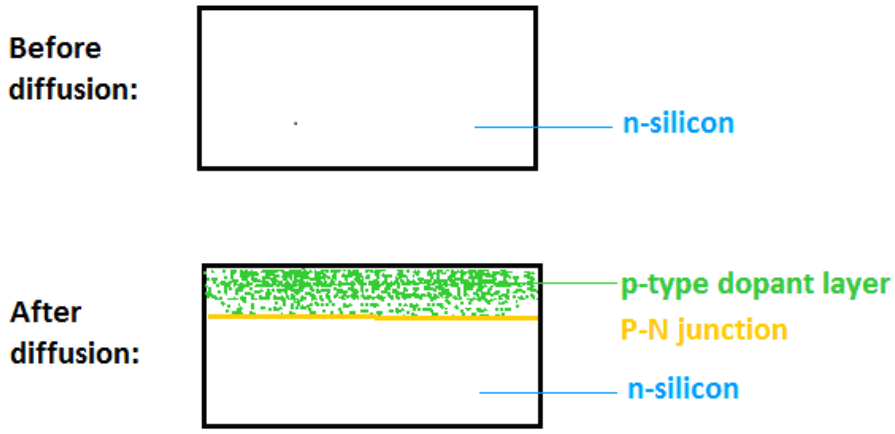


Figure 2.3 Schematic diagram of a p-n junction.

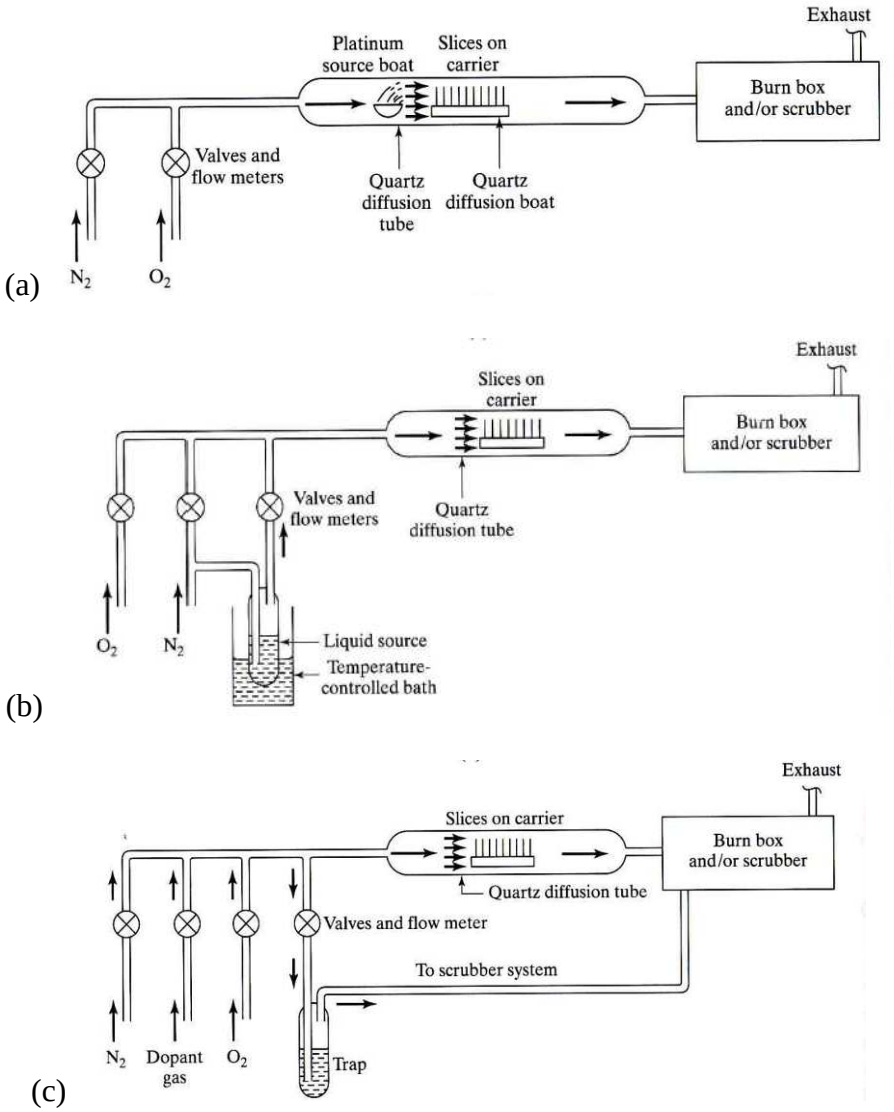


Figure 2.4 The open-furnace-tube diffusion systems for (a) solid, (b) liquid and (c) gaseous impurities source. Wafers are heated to high temperature in a quartz boat and the impurities are transported to the silicon surface and diffused into the wafer. (Photos captured from [19])

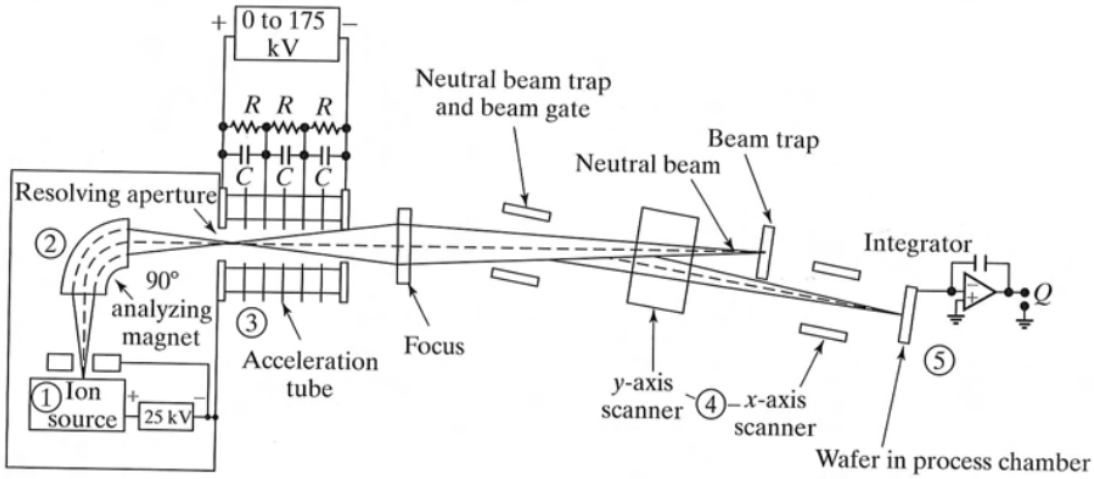


Figure 2.5 The ion implanter system. A high velocity beam of impurity ions was x-y scanned across the silicon wafer to penetrate the entire surface of silicon target wafers. (Photo captured from [19])

When p-type silicon is in contact with n-type silicon, the mobile electrons from the n-type silicon near the p–n junction will diffuse into the p-type silicon, leaving positively charged impurities in the n-type silicon near the p–n junction. Similarly, holes from the p-type silicon near the p–n junction will diffuse towards n-type silicon, resulting fixed impurities with negative charges in the p-type silicon near the p–n junction. The neutrality at the region nearby the p–n interface is lost along with the accumulated diffusion charges, the space charge region or depletion layer is formed. This potential difference across the junction is called built-in potential V_{bi}. The diffusion process results in generate more space charges, but the electric field produced by the space charge region opposes the diffusion process for both electrons and holes. Eventually, the electric field is strong enough to balance the diffusion process at equilibrium, as shown in Figure 2.7.

Figure 2.6 Equipments for (a) diffusion process and (b) ion implantation [20]

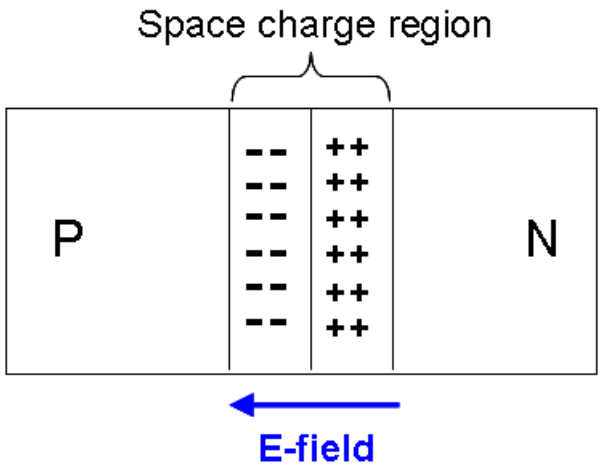


Figure 2.7 Space charge region is formed in p-n junction at equilibrium

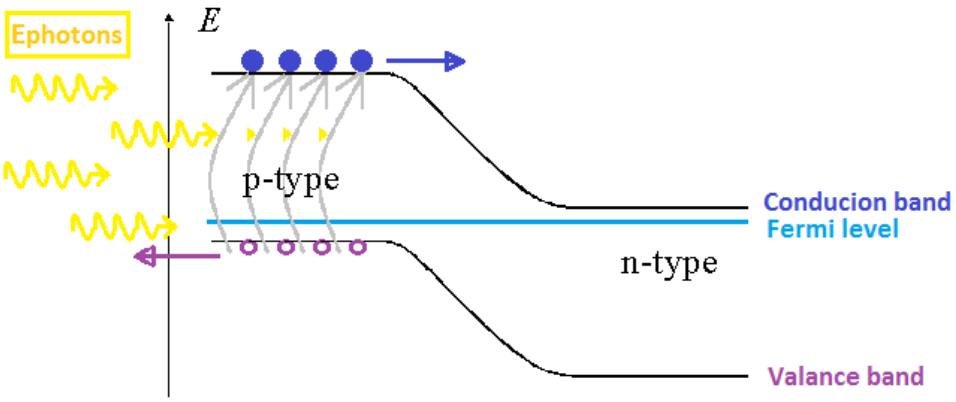


Figure 2.8 Energy band diagram of a p-n junction. Photocurrent is generated by the absorption of photons energies.

When light illuminates the p-n junction, electrons will be excited from the valence band into the conduction band. Holes are left behind in the valance band. (Figure 2.8). At this circumstance, the electric field is important to separate the electrons and holes to the "correct" electrodes. The electric field at the p-n junction can prevent hole-electron recombination and direct the electrons to flow in one

direction. The negative electrons move to the cathode and the positive holes migrate to the anode. In this way, the light energy is converted into the electrical energy.

2.2.3. Schottky junction

The Schottky junction is similar to the p–n junction, where metal serves the role of either the p-type or n-type semiconductor.

Figure 2.9 (a) illustrates the ideal metal/semiconductor junction for a n-type semiconductor and a high work function metal, after contact. If the n-type semiconductor and the high work function metal are in contact, electrons will flow from the semiconductor to the metal. Positively charged donors are left in the space charge region nearby the interface. Similarly, for a p-type semiconductor in contact with a low work function metal, electrons will flow from the metal to the semiconductor, as depicted in Figure 2.10 (a). Negative charged acceptors are formed in the space charge region nearby the interface.

The band diagram for metal/n-type and metal/p-type semiconductor Schottky barriers at equilibrium are given in Figure 2.9 (b) and Figure 2.10 (b) respectively. Across the space charge region (SCR), an electric field is formed. The electric field generates a built-in potential, which is equal to the difference between the work function of metal and the Fermi level of semiconductor when they are separated. The potential difference leads to a rectifying Schottky barrier near the interface.

When light shines at the Schottky junction, electron-hole pairs are formed in the n-doped or p-doped silicon. The electric field at the Schottky junction can prevent

hole-electron recombination and direct the electrons and holes to flow to the cathode and the anode respectively.

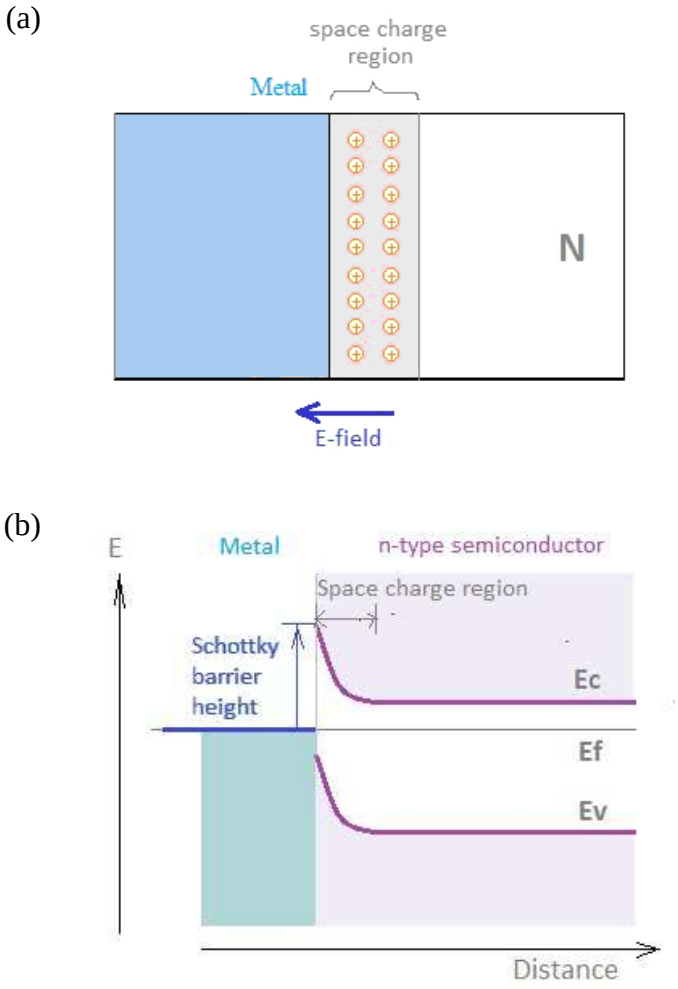


Figure 2.9 (a) Space charge region is formed in metal/n-type semiconductor Schottky junction at equilibrium and (b) the band diagram.

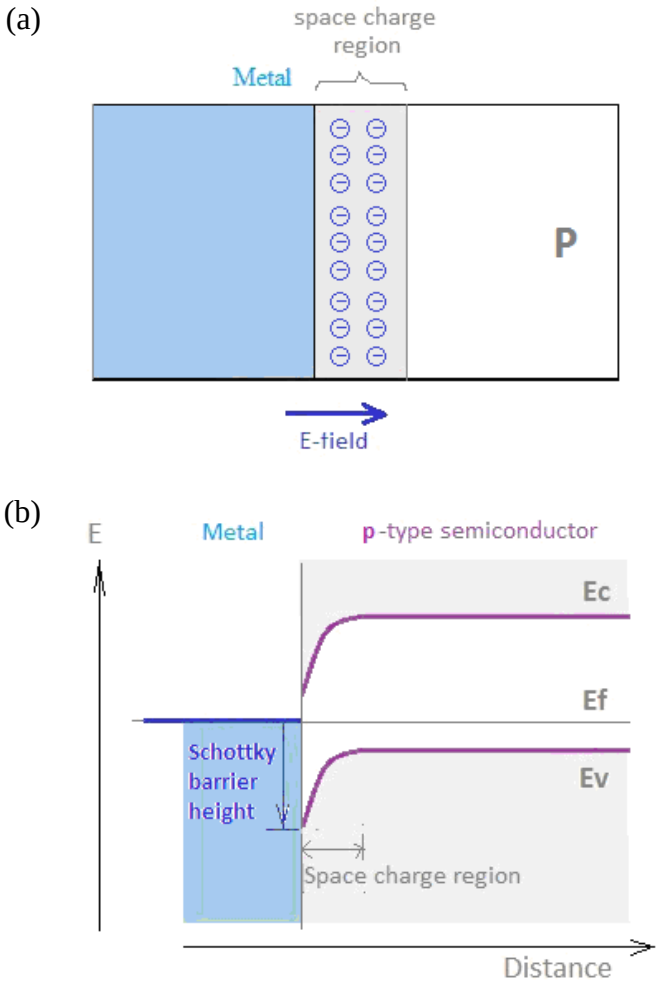


Figure 2.10 (a) Space charge region is formed in metal/p-type semiconductor Schottky junction at equilibrium and (b) the band diagram.

2.2.4. The evolution of Schottky junction solar cells

The metal top-electrode of the Schottky structure can be replaced by the degenerate semiconductor [21]. Degenerate semiconductors have low resistivity and wide band gap so they are transparent in the visible wavelength. Ideally, they can reduce the reflectance losses or the shading losses by the metal layer. Tin-doped

indium oxide (ITO) is commonly used for the upper electrode. ITO film usually consists of 90% indium oxide (In_2O_3) and 10% tin oxide (Sn_2O_3) by weight. It is a degenerate semiconductor with a wide band gap which is tunable with deposition properties. For ITO/n-type silicon solar cells, they could achieve the ideal J_{sc} of around 33 to 36 mA/cm^2 at AM1.5 or 40 mA/cm^2 at AM0 illumination conditions [21].

Another proposed degenerate semiconductor is the conductive polymer poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate), PEDOT:PSS. It is usually a hole transporting material and has more than 90% transparency over the entire visible spectrum into the near-infrared for thin PEDOT:PSS films. High work function of around 5.2 eV of PEDOT:PSS lets the lateral conduction of holes to be efficient at the solar junction.

2.2.5. Advantages of Schottky junction over p-n junction

Schottky junction has advantages over p-n junction for solar devices in three areas: First, the formation of Schottky junction eliminates a high-temperature diffusion step. A 35% input energy is saved from production process of Schottky junction solar cells in comparison to that of the conventional p-n junction solar cells [11]. Hence, the production cost per cell is lowered. Second, collecting junction of the Schottky solar cells is located right at the surface so that the charge collection is efficient [22]. Third, no loss of silicon crystallinity perfection in the product due to the elimination of the high temperature diffusion process. For p-n junction solar cells,

the open-circuit voltage is limited to typically ~600−630 mV. The Schottky junction monocrystalline silicon solar cell achieved an open-circuit voltage, as high as 655 mV in 1979 [23].

In the last couple of years, there had an increasing number of reports on Schottky barrier monocrystalline n-type silicon/PEDOT:PSS solar cells. Their relatively simple fabrication in ambient atmosphere and at rather low processing temperatures, is very appealing for low-cost yet high-efficiency photovoltaics.

2.3. Operating principle of monocrystalline n-type silicon/PEDOT:PSS hybrid solar cells

A hybrid solar cell is formed by associating an organic material with an inorganic semiconducting material so it can acquire both the distinct properties from them. The general structure for n-type silicon/PEDOT:PSS hybrid solar cells is in sandwiched geometry as shown in Figure 2.11. The substrate may be glass or plastics.

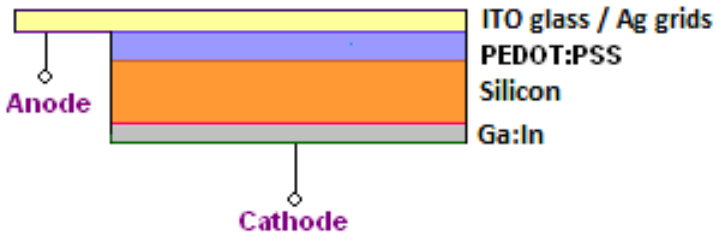


Figure 2.11 The architecture of the hybrid solar cell.

Indium tin oxide (ITO) is an anode material in the hybrid solar cells, due to its high transparency and commercial availability. Another common anodic material is silver (Ag). The silver grid pattern can be done by the convenient screen-printing method.

Poly(ethylene-dioxythiophene) doped with polystyrenesulfonic acid, PEDOT:PSS, is applied between the top electrode and the silicon wafer by solution processing (drop-casting or spin-coating). The conductive polymer PEDOT:PSS layer roles as a hole transporter layer. Moreover, it can reduce the surface roughness of ITO, protect the active layer from oxidation, and prevent the unwanted trap sites by blocking the diffusion of anode material into the active layer [24]. In addition, the work function can be changed by redox reactions of the PEDOT layer [25].

The bottom electrode (cathode) can be made by evaporating metal with a shadow mask or simply depositing eutectic gallium-indium (GaIn) paint with a cotton pad. Cathode materials should be ohmic contact with silicon to ensure a good charge collection.

Photovoltaic cells convert light energy to electrical energy. The silicon semiconducting layer absorbs sunlight and generates free holes and electrons, which are separated and diffuse to the corresponding electrodes. The electrons and holes separation is served by the internal electric field and the collected charges at the electrodes produce a current in the external circuit. Solar cells generate direct current electricity to loads or electrical apparatuses.

The general operating principle of the hybrid solar cells involves three important processes: (i) light absorption (ii) charge diffusion and separation and (iii)

charge transport.

2.3.1. Light absorption

Incident photons with energies greater than the band gap energy of the semiconductor are absorbed and the electrons at the ground states are excited. The band gap of silicon is 1.12 eV. The photon energy (E) and the wavelength of the light (λ) is related by: $E = \frac{hc}{\lambda}$, where h is Planck's constant (6.626×10^{-34} Js) and c is the speed of light (2.998×10^{8} m/s). Thus, $\lambda = \frac{(6.626\times10^{-34})(2.998\times10^{8})}{(1.12)(1.602\times10^{-19})} = 1.107$ μm. Hence, light with wavelengths below 1110 nm is absorbed and the theoretical maximum photocurrent is 43.8 mA/cm^2 [26]. Organic PEDOT:PSS thin film contributes very little to the light absorption, but its role was more significantly to enhance charge separation and provide good charge transport.

2.3.2. Charges diffusion and separation

Charge diffusion and separation are difficult in organic materials. First, the average exciton diffusion lengths of most of the organic semiconductors are short (smaller than 20 nm). However, the exciton diffusion lengths in inorganic materials such as silicon could reach several hundred nanometers. Thus, different from inorganic materials, most of the excitons are easily recombined in the organic materials before the carriers are diffused to reach the electrodes. Second, the binding

energies of excitons in organics materials are in the range 200 – 400 meV [27]. Thermal energy at room temperature of around 26 meV is not large enough for the dissociation of excitons into holes and electrons. On the other hand, the binding energies in most inorganic semiconductor materials are in the range of 2–40 meV. Therefore, the charges separation in organic materials is much difficult than that in inorganic materials.

As a result, exciton dissociation must be carried out at the interface with the help of an inner electrical field built by organic and inorganic components with proper highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) energy levels. The total area of the interface and the intensity of the built-in electrical field at the interface dominate the exciton dissociation efficiency.

Two common configurations of polymer/inorganic hybrid solar cells are bilayer and core-sheath, as in Figure 2.12. Charge separation occurs at the interface. Due to the short exciton diffusion length in conjugated polymers, bilayer structure seriously limits exciton dissociation because only one interface is provided for the exciton dissociation between the materials. This implies that only the photoexcitation nearby the interface and within an excitonic diffusion length can produce free charge carriers. In order to enlarge the interface area and benefit carrier transportation, ordered core-sheath nanostructures were applied to the conjugated polymer/inorganic hybrid solar cells [28].

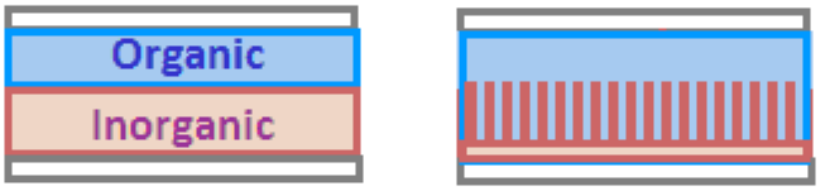


Figure 2.12 Bilayer (left) and core-sheath (right) architecture of the polymer-inorganic solar cells.

2.3.3. Charges transport

The charges are transported and collected through the electrodes. The electrode configurations are commonly silver grids or transparent conductive oxide layers. For silver grids, the separation distance between fingers should be optimized to favor the charge collection and avoid large area shading of light. Alternatively, transparent conductive oxides allow sufficient light absorption because of the high transmittivity of materials. However, indium (one of the elements in transparent conductive oxides) is rare and its price is increasing.

2.3.4. Alternative materials for silicon or for PEDOT:PSS

In silicon/PEDOT:PSS solar cells, an alternative material for PEDOT:PSS is graphene (Gr). Gr has high carrier mobility, high optical transparency and tunable work function. In the silicon/graphene (Si/Gr) solar cell, the Gr film forms Schottky junction with silicon and functions as a carrier separating layer. The efficiency of the

Si/Gr solar cell can be improved from 0.014% to 1.45% by thermal annealing process at 450 ºC for one hour [29]. Doping graphene film with nitric acid can increase the work function of graphene and increase the efficiency to 3.55% [30]. Another alternative material for PEDOT:PSS is carbon nanotubes (CNTs). The high mobility and large surface area of CNTs could be favorable to carrier dissociation and transportation, offering great promise in the development of high efficiency solar cells [31 , 32]. CNTs served as both photogeneration sities and carrier collection/transport layer. Silicon/CNTs heterojunction solar cells have an efficiency of 5-7% [33].

For silicon, an alternative material is gallium arsenide (GaAs). GaAs is a promising solar cell material due to its high optical absorption coefficient. A reasonable power conversion efficiency can be provided with a relatively thin thickness in comparison with other materials. Based on a heterojunction between vertically aligned GaAs nanowires and PEDOT:PSS with incorporating an electron blocking poly(3-hexylthiophene) layer, the fabricated hybrid solar cell exhibits an power conversion efficiency of 9.2% [34].

2.4. Low cost fabrication methods

2.4.1. Spin-coating and screen-printing for organic thin film

A group of widely used organic materials are polymers. Polymers cannot be deposited by vacuum evaporation due to their large molar mass and decomposable

character under excessive heat [25]. Therefore, most polymer-based materials are usually solution processed at low temperature. After the wet film formed on the substrate, annealing or ultraviolet curing are usually carried out. Subsequently, another film is allowed to be deposited on top of them.

Common printing/coating techniques for the production of polymer solar cells are spin-coating and screen-printing. The schematic diagram of spin-coating and screen-printing are shown in Figure 2.13 and Figure 2.14 respectively. These techniques provide the possibility for large scale production with low energy consumption.

For spin-coating, the substrate is stuck on the disc and followed by dropping excess amount of coating solution onto the substrate. Then the substrate rotates at high speed so that the excess solution is spread by a radial outward force. The volatile solvent in the coating solution could evaporate throughout the spinning. Eventually, a thin film is left on the substrate. Higher the rotation speed of spinning, the thinner the film.

For screen printing, a screen stencil is put on top of the substrate. Most area on the screen stencil is ink-blocking except the area of pattern to be printed. A squeegee is moved across the screen stencil, the ink will print the pattern of the screen onto the substrate.

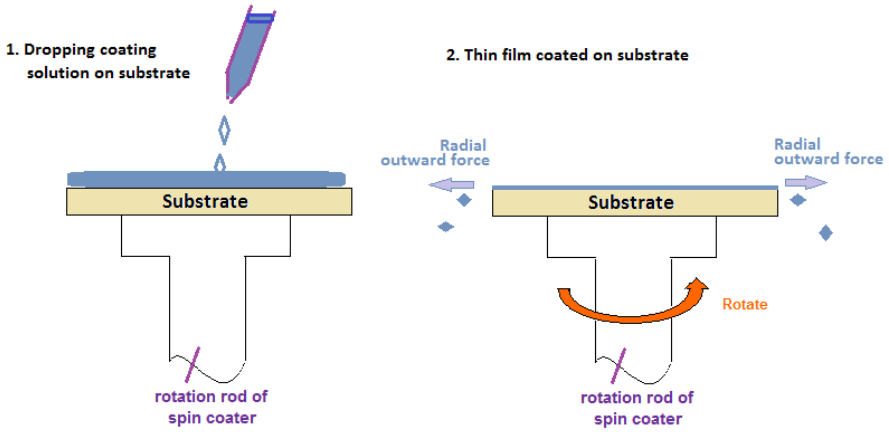


Figure 2.13 Schematic of spin-coating processing of a thin film on a substrate.

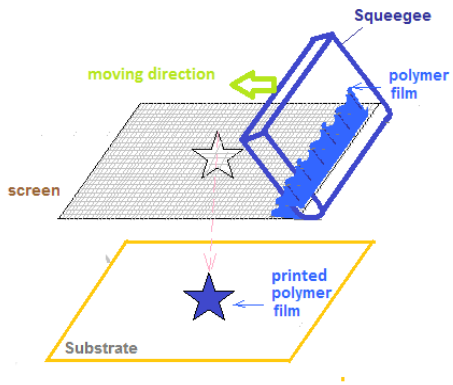


Figure 2.14 Schematic of screen-printing processing.

2.4.2. Electroless etching for silicon nanowires

Commonly used silicon nanowires fabrication methods [35] include vapor-liquid-solid (VLS) method, laser ablation, solution phase, molecular beam epitaxy (MBE) growth, and metal-assisted electroless etching (EE). These nanowires fabrication methods are compared and summarized as shown in Table 2. 1.

Methods	Advantages	Disadvantages
VLS	Diameter and growth rate control; Allowing epitaxial deposition	Contamination of catalyst; (degrades minority-carrier lifetime & diffusion length in SiNWs)
Laser ablation	High purity, yield and quality; Fast growing rate; Uniform smooth curving of NWs	High temperature (~1200 ℃) target heating
Solution phase	Defect free SiNWs; Nearly uniform diameter (as low as 4-5 nm)	Solvent heating and pressurizing
MBE	Epitaxial deposition; Vertically aligned ordered array	High-purity solid Si source heating; Ultrahigh vacuum; Metal contamination; Only NWs with diameters greater than 40nm was obtained; Low growth rate
EE	Rapid fabrication of large-area; Highly oriented SiNWs array	Hard to control wire diameter

Table 2. 1 Comparison table for commonly used growth methods of silicon nanowires (SiNWs). [Information extracted from Ref.35]

Generally, the fabrication of silicon nanowires proceeds in high temperature (VLS, laser abalation, solution phase) or high vacuum (MBE). However, the advantage of metal-assisted electroless etching (EE) is that silicon etching occurs

rapidly at room temperature when the silicon substrates covered with silver nanoparticles are immersed in the hydrofluoric (HF) acid based solution. It is reported that high-quality, upright-orientation silicon nanowires (SiNW) arrays can be rapidly fabricated on silicon substrates with large-area homogeneity and controllable depth of nanowires [36]. Growth of SiNW arrays could be carried out on p-type or n-type crystalline silicon wafers as well as on a selected active area [37].

The working principle of EE is a displacement reaction. The metal induces oxidation and the silicon dioxide beneath the metal catalyst dissolves in hydrofluoric acid solution. At the surface of the silicon wafer, reduction of metal ions and oxidation of silicon atoms are simultaneously taken place [38].

By the injection of holes into the valence band of silicon, the displacement reaction on silicon with silver ions (with highly positive reduction potential) is carried out. The presence of HF acid brings about the succeeding dissolution of the silicon wafer. As a result, the silicon-silicon bonds give out the electrons to reduce the silver ions into silver nanoparticles on the silicon surface. Silver nanoparticles cannot move horizontally and they are pinned by the pits on the silicon surface. Subsequently, local etching occurs (Figure 2.15 (a)). Some silver dendrites would be formed on the silicon surface during the etching process [39]. The cathode reaction is the reduction of silver ions:

$$Ag^{+} + e^{-} \rightarrow Ag(s)$$

The silicon beneath the silver nanoparticles is oxidized by the injected holes and dissolved at the silicon/silver interface by HF. The silicon under the noble metal is etched by HF much faster than the region without the coverage by the metal. Owing

to the continuous etching away of the silicon dioxide below the silver metal, the silver nanoparticles sink and generate pores into the silicon substrate. (Figure 2.15 (b)). The anode reaction is the oxidation of silicon [39]:

$$Si + 2H_2O \rightarrow SiO_2 + 4H^+ + 4e^-$$

$$SiO_2 + 4HF \rightarrow H_2SiF_6 + 2H_2O$$

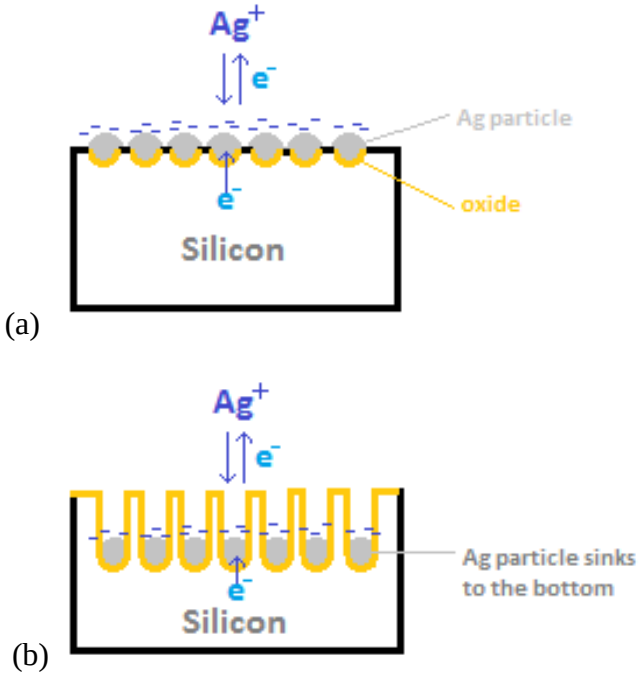


Figure 2.15 Mechanism of the lateral dissolution of silicon.

The continuous etching around the pores would result in the final formation of silicon (nanowires and nanoribbons) nanostructures. A longer and thinner silicon nanowires arrays would be fabricated if the silver particles covered silicon wafers were immersed in the HF-based etching solution for a longer duration. The etching

of silicon would continue until the exhaustion of the supply of oxidizing ions. Finally, some nanowires may form bundles by sharpening the top-ends of the nanowires.

To control the silicon nanowires' diameter or density, some methods are summarized as follows:

Nanowires with random diameters from 30 to 200 nm can be formed by high density of silver particles on the silicon substrate [40]. Silver particle density is controlled by the duration of silver nucleation. In the two-step electroless etching method, the first step is to immerse the samples in a solution of 0.03 M silver nitrate ($AgNO_3$) and 5.6 M HF for a short period of time for the formation of silver particles. The second step is to immediately soaked them into the solution of 56 M HF and 0.3 M H_2O_2 for 3 hours to form silicon nanowires. The duration of immersion in the first step plays an important role in the silver nucleation. Low density and high density silver particles are formed on the silicon substrates after 10 and 65 seconds respectively. The high density silver particles can obtain nanowires with diameters from 30 to 200 nm and the low density silver particles obtain porous silicon.

The density or diameter of nanowires from 100 to 252 nm could be accurately controlled by the template method [41]. In this method, polystyrene spheres are used as the template. First, the spheres are self-assembled on the silicon substrate. The desired diameter and density of nanowires are controlled by the diameter of the spheres that are reduced by a reactive ion etching process. Next, thermal evaporation process is carried out to deposit a silver film as catalyze for the subsequent electroless etching. Due to the masking of the silicon substrate by the spheres, a silver film with holes array is formed on the silicon substrate. Consequently, the

silicon beneath the silver film is etched away and nanowires array is formed by the metal-assisted electroless etching. The polystyrene spheres and the silver film are removed by chloroform and boiling aqua regia respectively.

Another approach for accurate controlling the density of nanowires is using anodic aluminum oxide (AAO) membrane [42]. This approach can fabricate silicon nanowires with diameter as small as 8 nm and density as high as 10^{10} wires/cm^2. First, the 300 nm thick AAO membrane with 20 nm pore diameter is solution transferred onto the silicon substrate. Then, reactive ion etching (RIE) is performed followed by the removal of the ultrathin AAO mask. Hence, the hexagonal pores array pattern on AAO membrane is transferred onto the underlying silicon substrate. Next, silver or gold metal is deposited on the patterned silicon substrate. Consequently, the ordered array of nanowires is obtained by performing metal assisted etching of silicon. The density of the nanowires is determined by the density of pores of the AAO membrane and the deposited metal thickness. Due to the shrinkage effect, the diameter of nanowires decreases with increasing mesh thickness.

The strong trapping of light by nanowires can increase light absorption and improve cell performance. One possible alternative of the nanowires for light trapping was the plasmonic metal nanospheres incorporated at the interface between air and silicon. The common plasmonic metals are silver and gold. Silver is much better than gold because of its cheaper cost. The sunlight can be effectively guided within the absorbing layer due to the collective oscillation of electrons at the surface of the metal nanospheres [43]. The plasmonic nanoparticles effectively trap sunlight

into the underlying silicon by forward scattering. When the silicon pyramid surface was optimally 35% covered by spherical silver nanoparticles (average radii around 68 nm), the reduction in the total reflectance was around 3.4% [44]. Although the introduction of plasmonic nanoparticles can decrease light reflection, they also induce light loss due to absorption within the nanoparticles themselves. After integrating 200 nm diameter silver nanoparticles on top of the silicon wafer, the measured efficiency of the solar cell reduced from 17.47 to 17.1% for low area coverage (~1−5%) and from 17.47 to 16.8% for high area coverage (~5−10%) [45]. On the other hand, the parasitic absorption is neglectable in the dielectric nanoparticles. The efficiency enhanced slightly from 17.47 to 17.7% with the application of 100 nm diameter silica nanoparticles.

2.4.3. Anisotropic etching of silicon

Anisotropic etching of silicon refers to the direction-dependent etching of silicon [46]. For single crystalline silicon solar cells, anisotropic etching is utilized to form pyramidal structure on the surface of the silicon wafers. The pyramidal morphology can re-collect the reflected light and trap the light more efficiently inside the solar cells [47].

Because of the strong dependence of the etch rate on the direction of crystallity and the concentration of etchant, silicon structure can be produced in a well-control and reproducible way, according to Figure 2.16 [48]. The mixture of sodium hydroxide solution or potassium hydroxide solution mixed with isopropyl alcohol

are the most common etchant for silicon. The temperature range of 70−90 ºC is widely used in the etching process [47]. Seidel et al. studied the silicon etch rate by potassium hydroxide solution in details and the results are summarized in Figure 2.16. A chemical equation of anisotropic etching of silicon is as follows [49]:

$$Si + 2OH^- + 2H_2O \rightarrow SiO_2(OH)_2^{2-} + 2H_2$$

Isopropyl alcohol is used for an effective mixture to potassium hydroxide solution influencing the smoothness of resulted silicon surfaces [50]. Isopropyl alcohol can help removing the hydrogen bubbles in the etching solutions [47]. It also promotes the formation of large pyramids because it increases the wettability of the silicon surface. However, with increasing isopropyl alcohol concentration, the silicon etching rate decreases significantly.

	Temperature [°C]								
% KOH	20°	30°	40°	50°	60°	70°	80°	90°	100°
10	1.49	3.2	6.7	13.3	25.2	46	82	140	233
15	1.56	3.4	7.0	14.0	26.5	49	86	147	245
20	1.57	3.4	7.1	14.0	26.7	49	86	148	246
25	1.53	3.3	6.9	13.6	25.9	47	84	144	239
30	1.44	3.1	6.5	12.8	24.4	45	79	135	225
35	1.32	2.9	5.9	11.8	22.3	41	72	124	206
40	1.17	2.5	5.3	10.5	19.9	36	64	110	184
45	1.01	2.2	4.6	9.0	17.1	31	55	95	158
50	0.84	1.8	3.8	7.5	14.2	26	46	79	131
55	0.66	1.4	3.0	5.9	11.2	21	36	62	104
60	0.50	1.1	2.2	4.4	8.4	15	27	47	78

Figure 2.16 Silicon (100) etch rates in [μm/h] for various KOH concentrations and etch temperatures. [48]

2.5. Recent development in silicon/PEDOT:PSS hybrid solar cells

Without any efficiency enhancement methods, the silicon/PEDOT:PSS heterojunction solar cell efficiency can be very low (<0.1% [51]). However, it had a gradual increase in its power conversion efficiency in recent years and could be a promising candidate for future low cost solar cells.

Currently, the silicon/PEDOT:PSS hybrid solar cells have already exceeded 10% efficiency [52]. Various feasible methods for devices efficiency improvement are reviewed from the literature. First, devices efficiency improvement can be achieved by enhanced optical absorption of silicon. The textured (micropyramids and nanowires) silicon surface increased junction area for optical absorption and thus enhanced carrier separation/collection and PCE [53]. Various types of textured silicon surface have been achieved, such as nanocone [54], nanorod [55] or nanopillar [56]. The silicon/PEDOT:PSS hybrid solar cell with the hierarchical surface (nanowires on micropyramids) obtained a power conversion efficiency of 11.48% [53]. Compared to the efficiency of planar (7.59%) and only micropyramid (10.37%) surface devices, the hierarchical surface achieved higher efficiency. Moreover, the generated power density by the hybrid cell with hierarchical silicon surface enhanced from 51.9% to 253.8% at all angles of incidence (AOI). This efficiency enhancement in ominidirection is practical because sunlight shines on the solar cell from a variety of direction during the day. The hierarchical surface increased internal multiple reflection and provided an intermediate refractive index

between air, PEDOT:PSS, and silicon, broadbandly and omnidirectionally to suppress the undesired surface reflection in the silicon/PEDOT:PSS hybrid solar cell.

Second, studies were also conducted on the interface passivation of silicon. Materials such as ferroelectric poly(vinylidene fluoridetetrafluoroethylene) P(VDF-TeFE) [57], graphene oxide (GO) [58,59,60], aluminum oxide (Al_2O_3) [56] and 1,1-bis[(di-4-tolylamino)phenyl]cyclohexane (TAPC) [52] were reported and acted as a thin organic interfacial layer in between n-type silicon and PEDOT:PSS. This enhanced the electric field or electron barrier at the crystalline silicon/PEDOT:PSS interface and suppressed the electron recombination at the anode, for the purpose of device efficiency improvement. However, too thick interface layer imposed higher barrier potential for charge carriers to tunnel through, retarding the collection efficiency of the device. Thus, most thickness of interfacial passivation layers were around 2-5 nm.

Third, better adhesion of PEDOT:PSS on hydrophobic silicon were also reported to improve the devices efficiency. The result of higher efficiency was interpreted in terms of the better adhesion (or pore-filling ability) of PEDOT:PSS on the planar (or gap between) nanostructured silicon. As more contact area between PEDOT:PSS and silicon, the charges separation would be more efficient. Liu et al [61] mixed 0.1% Zonyl fluorosurfactant in PEDOT:PSS and fabricated 11.3% crystalline silicon/PEDOT:PSS photovoltaic devices, due to the good adhesion of Zonyl-treated PEDOT:PSS on silicon surface. For textured pyramid surfaces, Yu et al [52] pointed out that the spin-coated organic polymer layer was always inhomogeneous and it was hard to coat uniformly on textured surfaces. Thus, they

utilized electrospray deposition (ESD) which is a dry process with a solution precursor to achieve a uniform film coating. The products were formed preferentially at the valley region of each pyramidal structure. Thus, the EDS was demonstrated effective to improve the interfacial properties. Similarly, for nanowires array textured silicon surface, the spin-coated organic polymer was difficult to infiltrate into the gaps among the nanowires. Still, the pore-filling ability of small molecular size of Spiro-OMeTAD into the gaps between the SiNWs was reported to increase its junction area and improve SiNWs surface passivation [62]. Spiro-OMeTAD stands for 2,20,7,70-tetrakis(N,N-di-4-methoxyphenylamino)- 9,90-spirobifluorene, that is a small molecule organic material. The SiNWs/Spiro-OMeTAD/PEDOT:PSS cells exhibited a power conversion efficiency of 10.3%, which was higher than the 7.7% of SiNWs/PEDOT:PSS cells.

The silicon/PEDOT:PSS heterojunction solar cell has shown gradual increase in its power conversion efficiency in recent years and revealed a promising candidate for the future low cost solar cell. In 2013, the highest power conversion efficiency reached 13.01% [52], with a short circuit current of 34.76 mA/cm^2, open circuit voltage of 0.54 V and fill factor of 69.5%.

2.6. Effect of nanowires length on device efficiency

Texturization is a simple way to improve optical absorption and increase junction area. Although silicon surface texturization by nanowires has been investigated for the efficiency improvement in the hybrid silicon/ PEDOT:PSS solar cells, the optimal length of the nanowires for the best performance is uncertain. For

instance, Lin et al. [63] studied the SiNWs length effect on the PCE of the hybrid solar cells. Their devices with 370 nm SiNWs achieved PCE of 8.4%. On the other hand, Lai et al. [64] showed that devices with 350 nm SiNWs can only obtain 7.7%, whereas the devices with 900 nm SiNWs can achieve a PCE of 9%. However, another literature from Lin et al. [65] showed that devices with 780 nm SiNWs can only obtain 0.93%, whereas the devices with 3.67 μm SiNWs can achieve a PCE of 3.82%. These differences may be due to a wide range of reasons such as the variation in optical absorption, charge recombination, silicon−PEDOT:PSS adhesion, etc. Therefore, it is worthy to study the reasons of specific nanowires length contributed to the efficiency improvement of silicon/ PEDOT:PSS solar cells. The factors studied here could serve as the basis for the development of high efficiency silicon/PEDOT:PSS hybrid solar cells.

2.7. Enhancement of carrier separation efficiency

Pristine PEDOT:PSS suffered low conductivity problem of less than 1 S/cm. The low conductivity of the PEDOT:PSS can suppress carriers collection, promote joule heating induced lifetime reduction and lower the device efficiency. Therefore, in the fabrication of silicon/PEDOT:PSS hybrid solar cells, it is customarily added 5 wt% dimethyl sulfoxide (DMSO) into PEDOT:PSS for conductivity enhancement. The conductivity of DMSO-added PEDOT:PSS film is around 850 S/cm. DMSO is a polar organic solvent with high dielectric constant. Addition of DMSO into PEDOT:PSS solution can introduce a screening effect that suppresses the electrostatic interaction between PEDOT and PSS [66]. The phase separation of

PEDOT and PSS polymer chains promotes interactions among PEDOT molecules that improve the crystallinity of the PEDOT phase. Recently, it was reviewed that PEDOT:PSS films employing film treatment (together with additives) showed better conductivity than only the additives in the PEDOT:PSS aqueous solution. This is because the film treatment method not only leads to better connected PEDOT chains but also facilitates significant removal of excess PSS from the film surface. Among the film treatment methods of PEDOT:PSS, the conductivity of PEDOT:PSS film was enhanced three order of magnitude to 2050 S/cm through the formic acid treatment. Therefore in this thesis, we take a step further and investigate the effect of different concentration of formic acid on the PEDOT:PSS film for the purpose of the conductivity as well as the power conversion efficiency enhancement. This study aims at developing silicon/PEDOT:PSS hybrid solar cells for high efficiency in a cost-effective approach.

2.8. Bending flexibility of hybrid Si/PEDOT:PSS solar cells

In recent years, the development of solar cells moves toward wearable and flexible devices. Monocrystalline silicon is a popular material for high efficiency solar cells. However, the brittle property of silicon wafers makes them difficult to be curvature. Methods for fabricating crystalline silicon thin film possessed of bending flexibility have been reported [67,68]. Among them, potassium hydroxide etching of silicon wafers can fabricate ultrathin crystalline silicon films that can be cut with scissors like a piece of paper and direct handled without a supporting substrate [67]. This flexible silicon fabrication method is simple and inexpensive. Therefore, the

flexible silicon fabrication method is utilized to obtain some thin film silicon sheets in this work. The thin film silicon substrates are investigated to demonstrate the feasibility of thin film silicon/PEDOT:PSS solar cells. Thin film solar cells with increased bending flexibility and light in weight which will be favorable for wider applications.

2.9. Stability of Si/PEDOT:PSS/ITO hybrid solar cells

For silicon/PEDOT:PSS devices, most of the published work was focusing on the optimization of the device performances [69 ,70 ,55], and not much work has focused on investigating the degradation mechanism of the silicon/PEDOT:PSS devices and the possible approaches to recover the efficiency.

Previously for the organic photovoltaic (OPV) devices, the degradation of their efficiency has been studied with P3HT:PCBM as the active region materials and PEDOT:PSS as the hole transporting layer. It has been shown that the hygroscopic property of PEDOT:PSS film will absorb moisture and cause morphological changes in the film which are irreversible after drying and thus the conductivity of the PEDOT:PSS film will decrease [71, 72]. Degradation was also obvious in the PEDOT:PSS/MDMO-PPV:PCBM organic solar cells illuminated under humid conditions (> 40% relative humidity) either in air or in nitrogen [73]. Furthermore, while exposing the PEDOT:PSS layer to illumination wavelength shorter than 315 nm, it has been shown that strong oxidation would occur in the PEDOT:PSS thin film added with 5wt% dimethylsulfoxide (DMSO) [74]. Another circumstance that

can also cause degradation of the devices is the instability of the ITO/PEDOT:PSS interface. The acidic property of PEDOT:PSS layer under high humidity environment has shown to cause the liberation of indium and tin from the ITO [75]. The indium-containing etching products will be trapped in the PEDOT:PSS layer and affect the transportation of charges. To overcome the liberation, Lau et al., have suggested to use self assembly monolayer (SAM) formed by alkylsiloxanes to interfere the diffusion of the indium and tin [76]. Beside this, reducing tendency of water uptake from air can increase the environmental stability of the PEDOT:PSS film, such as adding sorbitol solution into PEDOT:PSS dispersion [6].

In the current study, the coil conformation of PEDOT:PSS turns into linear or expanded-coil conformation after the adding of ethylene glycol (EG), it can benefit the delocalization of charges in the PEDOT:PSS and the electrical conductivity [77] and it has been shown by Yang et al that the conductivity the EG treated-PEDOT:PSS can increase from 0.4 to 160 S/cm by using 1:1 volume ratio [78]. We employ an environmental chamber to store the devices under different relative humidity while maintaining the temperature constant. By detaching the ITO glass from the silicon substrate, we individually study the degradation effects on the ITO, PEDOT:PSS and silicon nanostructure. The findings can explain the major causes of the PCE drop in the current silicon/PEDOT:PSS devices.

2.10. Concluding remarks

Recent solar cell development aims at lower production cost and higher power

conversion efficiency. Silicon/PEDOT:PSS hybrid solar cells are promising for future low cost solar cells due to the relatively convenient solution fabrication process at room temperature and in air environment. Silicon is abundance, non toxicity and strong absorption in the ultraviolet region, acting as a light absorption material. Moreover, polymer PEDOT:PSS has high optical transparence, good thermal stability and low temperature processing, served as a hole transporting layer. In this thesis, we will improve the power conversion efficiency in silicon/PEDOT:PSS solar devices by solving the problems of high light reflection from silicon surface and low conductivity of polymer. Then, work will be carried out to investigate thin film silicon substrates and demonstrate the feasibility of flexible silicon/PEDOT:PSS solar cells. Finally, the stability of the hybrid solar cells under humidity condition is investigated. The longer service time of the solar cell is also a key for energy cost reduction.

CHAPTER 3 EXPERIMENTAL SETUP AND CHARACTERIZATION TECHNIQUES

3.1. Materials preparation for the hybrid solar cells

3.1.1. Silicon wafers

Four inches diameter' single-crystalline (100) n-type silicon wafers with resistivity of 1-10 Ω-cm (Guv Team) were used as the substrate. The n-type wafers were doped with phosphorus concentration around 6×10^{14} cm^{-3}.

3.1.2. PEDOT:PSS solution

Aqueous PEDOT:PSS solution was used as the hole transporting polymer film. The solution was applied on the substrates by spin-coating. The molecular structure of PEDOT:PSS is given in Figure 3.1 and the work function of PEDOT is around 5.2 eV. The technical data of PEDOT:PSS solution is summarized in Table 3. 1.

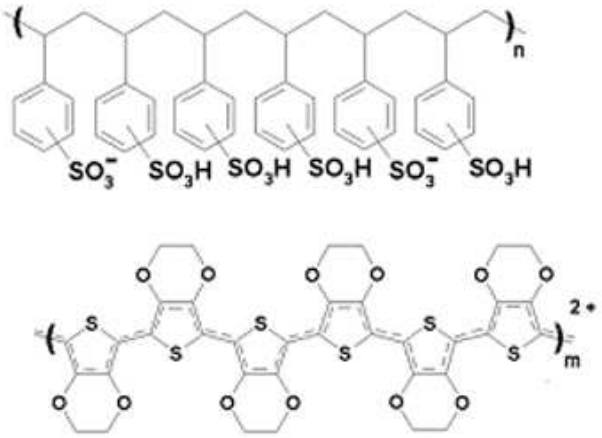


Figure 3.1 Molecular structure of PEDOT:PSS [79]

	Clevios PH1000
Conductivity (S/cm)*	1164
Viscosity (mPa・s)	15-50
Solid content (%)	1-1.3
PEDOT:PSS ratio	1:2.5

Table 3. 1 Technical data of PEDOT:PSS solution [79]

3.1.3. Indium Tin Oxide (ITO) glass

Indium tin oxide (ITO) is a ternary composition of 74% indium, 8% tin and 18% oxygen by weight. ITO-coated glass (Guv Team) of sheet resistivity of 7 Ω/sq was used as transparent anodes. The transmittance of the ITO glass was around 82% at wavelength 550 nm.

3.1.4. Gallium Indium eutectic

The gallium indium eutectic (99% metal basis) paste was purchased from Alfa Aesar. It was deposited on the back surface of silicon wafers as the cathode material.

3.2. Physics for the hybrid silicon/PEDOT:PSS solar cells

Figure 3. 2 shows the energy diagram of the silicon/PEDOT:PSS heterojunction solar cell. The work function of PEDOT:PSS is around 5.0 − 5.2 eV [79], which is close to the valence band energy (E_v) of silicon. Because of the advantages of the high work function, PEDOT:PSS is a potential hole conducting polymer and serves as a high quality Schottky contact on n-type silicon semiconductors. The solution based spin-coating process of PEDOT:PSS may reduce the formation of the interfacial trap states (possibly due to small physical and chemical stresses at the interface), giving rise to better junction properties [80]. Thus, PEDOT:PSS layer attached on a clean n-type silicon substrate will from a Schottky barrier for electron-hole pairs separation.

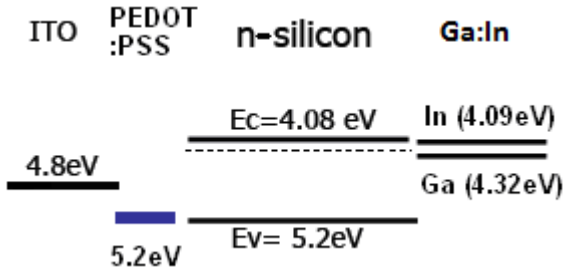


Figure 3. 2 Energy diagram of the active layers in the n-silicon/PEDOT:PSS heterojunction solar cell.

The band diagram for non-contact PEDOT:PSS and n-type silicon is shown in Figure 3. 3(a). Given that the band gap of silicon E_G = 1.12 eV; doping concentration of n-type silicon $N_d = 6\times10^{14}\text{cm}^{-3}$ and T = 300 K, the Fermi level (E_f) of the n-type silicon is

$$E_f = E_C + [\frac{E_G}{2} - kT\ln(\frac{N_d}{n_i})] \cong 4.08 + 0.56 - (0.0259)\ln(\frac{6\times10^{14}}{1.45\times10^{10}}) = 4.36 \text{ eV}.$$

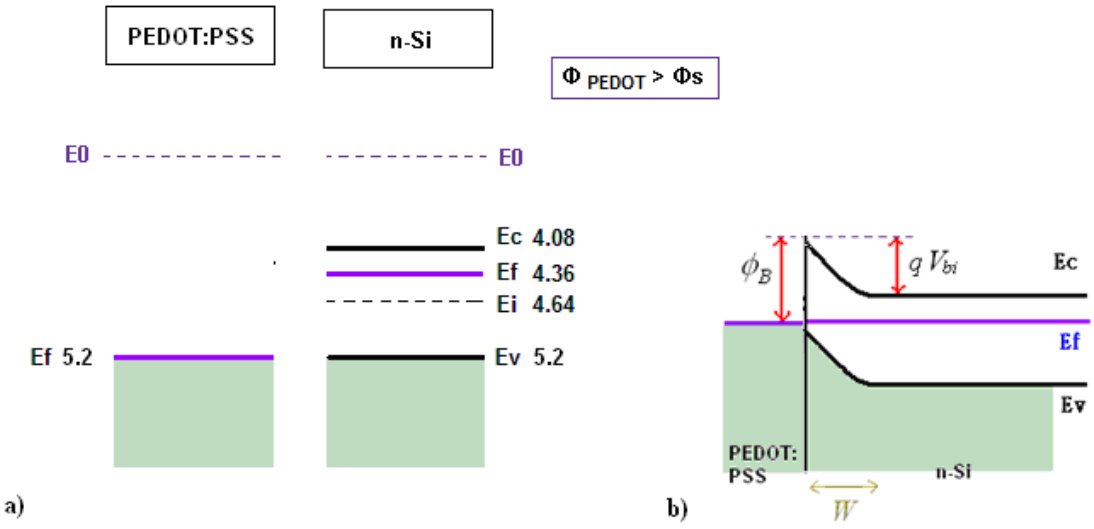


Figure 3. 3 The band diagram for (a) non-contacted PEDOT:PSS and n-type Si (b) PEDOT:PSS and n-Si after contact.

As the work function of PEDOT:PSS (Φ_{PEDOT}) is higher than that of n-silicon (Φs = 4.36 eV), rectifying Schottky contact will be formed [81]. Just after the contact formation, electrons will begin to flow from the n-silicon to the conductive PEDOT:PSS as shown in Figure 3. 3(b). As the electrons are removed from the n-type silicon, uncompensated donors were left behind and hence creating a depletion layer with a width (W) and a built-in electric field (V_{bi}) [82]. Under equilibrium, the Fermi-level will be constant and no current flows because a barrier (Φ_B) stops electrons flowing from conductive PEDOT:PSS to semiconductor silicon. Electrons in the semiconductor will confront an energy barrier equal to $\Phi_{PEDOT} - \Phi_S$ while flowing from silicon to PEDOT:PSS layer.

In the dark, the dominant flow in forward bias of a Sckottky junction is the diffusion current that flows from PEDOT:PSS to silicon. The forward bias reduces the barrier height. As a result, a large forward current can flow across the interface and the forward current increases exponentially with applied voltage [Figure 3. 4(left)]. Under reverse bias, the current flowing from PEDOT:PSS to silicon is restricted by the enlarged barrier height. The dominated current flow will be a small reverse leakage tunnelling current [Figure 3. 4(right)]. The schematic band diagrams of the silicon/PEDOT:PSS heterojunction under forward bias and reverse bias are shown in Figure 3. 4.

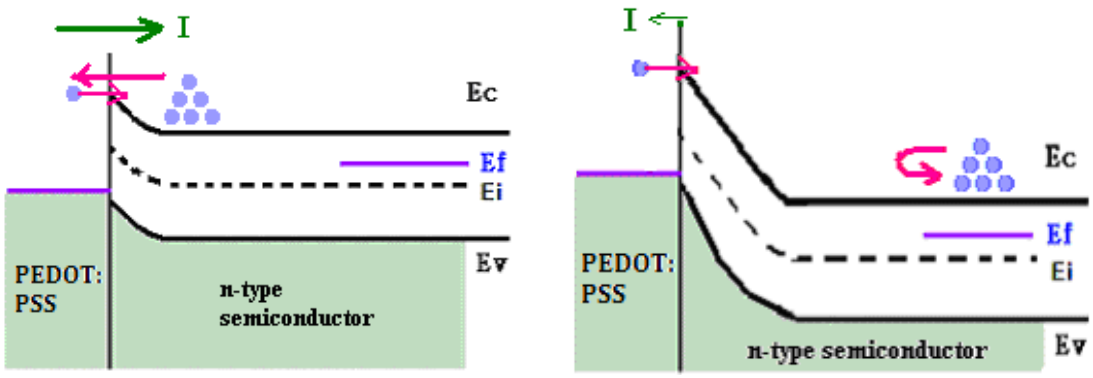


Figure 3. 4 Schematic band diagrams of the silicon/PEDOT:PSS heterojunction under forward bias (left) & reverse bias (right). (modified from [82])

For hybrid silicon/PEDOT:PSS heterojunction solar cell, the dominant current transport mechanism is thermionic emission of majorities over the Schottky barrier ($q\Phi_B$). The total dark current density (J_d) is expressed as [83]: $J_d = \left\{ A^* T^2 \exp\left(-\frac{q\phi_B}{kT} \right) \right\} \left[\exp\left(\frac{qV}{kT} \right) - 1 \right]$ where A^* is the effective Richardson constant, k is the Boltzmann constant, T is the absolute temperature and V is the applied voltage.

When light is incident on the silicon/PEDOT:PSS interface of the hybrid solar cell with photon energy larger than the band gap energy of silicon, electrons in the valence band of silicon will be excited to the conduction band. Holes generated by light absorption in the silicon are injected into PEDOT:PSS and hence into the ITO electrode. The work function of PEDOT:PSS is larger than the Fermi level of the n-type silicon so that electrons generated in silicon should be collected efficiently at the In:Ga eutectic cathode. Finally, a current flows from silicon to PEDOT:PSS. The band diagram of the silicon/PEDOT:PSS heterojunction under illumination is

schematically illustrated in Figure 3. 5.

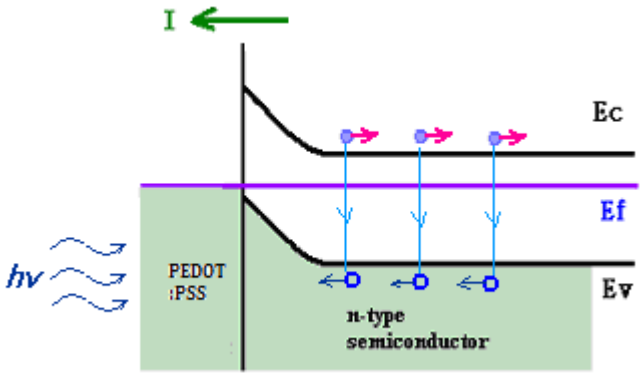


Figure 3. 5 Schematic band diagram of the Si/PEDOT:PSS heterojunction under illumination.

Literature reported that the PEDOT:PSS/inorganic interface may include an thin interfacial dipole layer [80, 84 ,85]. The effects of the interfacial dipole [86] are the increase of the upward band bending in silicon near the interface and reduction of the reverse-bias leakage current. Hence, higher quality of Schottky junction will be formed.

3.3. Characteristic model of solar cell

The equivalent circuit of a solar cell is shown in Figure 3. 6.

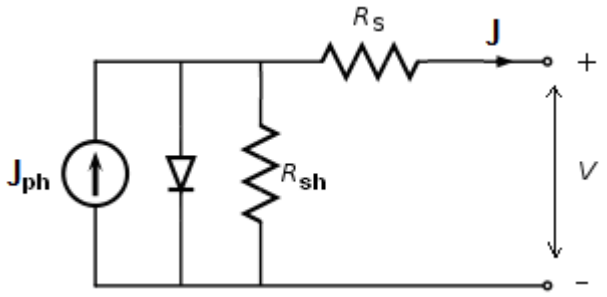


Figure 3. 6 Equivalent circuit of a solar cell.[87]

The practical photovoltaic model consists of a single diode connected in parallel with a photo-generated current (J_{ph}), parasitic series resistance (R_s) and shunt resistance (R_{sh}). Ideally, series resistance is small and shunt resistance is large. Applying Kirchhoff's law to the node where J_{ph}, diode, R_{sh} and R_s met, and get the output current J:

$$J = J_{ph} - J_d - J_{sh} \qquad \text{Eq 3. 1}$$

$$J = J_{ph} - J_0\left\{\exp\left[\frac{V + JR_s}{nV_{th}}\right] - 1\right\} - \left[\frac{V + JR_s}{R_{sh}}\right] \qquad \text{Eq 3. 2}$$

where J_d = diode current

J_{sh} = shunt current

where J_0 = saturation dark current

n = ideality factor

V_{th}= thermal voltage = kT/q =0.0259

k = Boltzmann's constant (1.38×10^{-23} J/K)

T = cell's working temperature

q = electron charge (1.6×10^{-19} C)

V = applied voltage

The model characteristic parameters can be obtained from the measured $J-V$ data by the curve fitting method with the following equation [88]:

$$J = n \cdot \frac{V_{th}}{R_s} \cdot lambertw\left(\frac{J_0 R_s}{n \cdot V_{th} \cdot (1 + R_S G_p)} \times e^{\frac{V + R_S (J_0 + J_{ph})}{n V_{th} (1 + R_S G_p)}} \right) + \frac{V G_p - (J_0 + J_{ph})}{1 + R_S G_p} \qquad \text{Eq 3. 3}$$

where G_p is the parallel parasitic conductance = $1/R_{sh}$.

The series (R_s) and shunt resistance (R_{sh}) can be interpreted from the shape of $J-V$ curve. The effect of R_s and R_{sh} on the $J-V$ curve are simulated according to Eq 3. 3 and the results are plotted in Figure 3. 7. In order to obtain the ideal diode curve for the largest fill factor, R_s should be as small as possible and R_{sh} should be infinitely large.

Series resistance (R_s) is closely related with the intrinsic resistance, morphology, and thickness of the semiconductor layer [89]. Series resistance in the hybrid silicon/PEDOT:PSS solar cell can be stemmed from: firstly, the flow of current through the junction of the solar cell; secondly, the contact resistance between cathode and silicon, and that between PEDOT:PSS and anode; and finally the material resistances of the top and rear electrodes. The main evidence of series resistance is the reduction of the fill factor and may also a reduction of the short circuit current in case of excessively high series resistance.

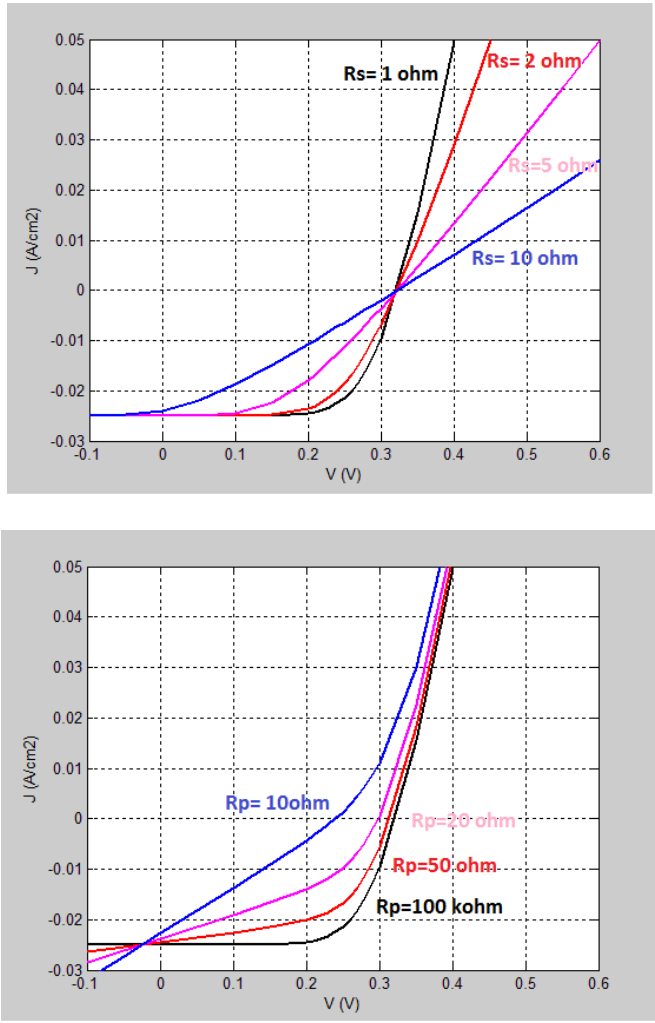


Figure 3. 7 The upper and lower graphs show the impact of the series resistance (R_s) and shunt resistance (R_{sh}) on the shape of IV curve, respectively. The graphs is simulated by using Eq.3.3.

Shunt resistances (R_{sh}) is correlated with the amount and character of the impurities and defects in the active semiconductor layer because impurities and defects cause charge recombination and leakage current [89]. Also, as the shunt resistance decreases, the current flown through the shunt resistor increases for a certain junction voltage and results in a slight decrease in V_{oc}. Shunt resistance is generally due to manufacturing defects, rather than poor solar cell design [90]. When

the solar cell's shunt resistance is low, an alternate current path that causes power losses will be created for the light-generated current.

3.4. Simulation and control of the environmental condition

In order to simulate illumination approximating to the natural sunlight, a class A solar simulator is used in this project to provide a controllable and standardized equipment in the laboratory for the efficiency testing of the solar cells. In addition, for the purpose of studying the humidity effect of the solar cells, an environmental chamber, which the temperature and humidity level can be controlled, was utilized. Moreover, for the testing of durability and stability of the flexible hybrid solar cells under bending strain, a bending test apparatus is used in the study.

3.4.1. Solar simulation and $J-V$ curve

The power conversion efficiency is a characteristics property of solar cells and is revealed from the current density-voltage ($J-V$) curve. The $J-V$ curves of solar cells were measured in air at condition of both dark and 1 sun (AM1.5) 100 mW/cm^2, simulated by the solar simulator (SUN2000, Abet Technologies, Inc.). The photo of the solar simulator is given in Figure 3. 8. Before measurement, the solar simulator was calibrated by a NREL certified monocrystalline silicon reference cell (Figure 3. 9). A sample stage was set so that the solar cells can be clamped at the same location every measurement. The light fell normally on the silicon/PEDOT:PSS

heterojunction. The $J-V$ characteristic curves of the solar cells were measured by a Keithley 2400 sourcemeter and the reading values were recorded via a LABVIEW interface.

Feature	**Specification**[91]
Type of lamp	Ozone-free Xe Arc Lamp
Lamp power	150 W
Lamp lifetime	1500 Hours
Light source	Continuous (Shutter)
Intensity adjustment	AM1.5, 100 mW/m^2
Working distance	50-200 mm
Illumination area	35 mm diameter

Table 3. 2 Specifications of the solar simulator model SUN2000.

Figure 3. 8 The solar simulator SUN2000, Abet.

Figure 3. 9 The NREL certified monocrystalline silicon reference cell.

A current density against voltage ($J-V$) curve represents the photovoltaic characteristics of a solar cell. In the dark, the curve shows diode behavior. When light shines on the cell, the $J-V$ curve shifts downwards.

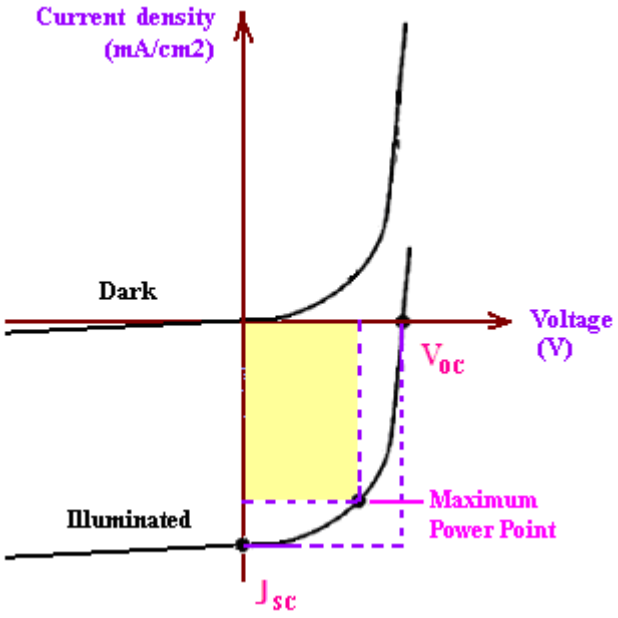


Figure 3. 10 $J-V$ characterization curve.

On the $J-V$ curve, there are three important points to notice: 1.Open-circuit voltage (V_{oc}), 2. Short-circuit current (J_{sc}) and 3. the maximum power point (*MPP*). These values imply the efficiency of the solar cells.

Open-circuit voltage (V_{oc}) is the voltage across the output electrodes when the cell in open circuit (i.e. when current $J = 0$) [84]. Short-circuit current (J_{sc}) is the current through the electrodes when the cell is operated at short circuit (i.e. when voltage $V = 0$) [92]. Maximum power point (*MPP*) is the point on the $J-V$ curve where maximum power is generated. Power is the product of current and voltage. Hence, it is equal to the area of the rectangle formed between a point on the $J-V$ curve and the axes. At *MPP*, the area of the resulting yellow rectangle in Figure 3. 10 is the largest.

Power conversion efficiency (PCE) of a solar cell is calculated by the ratio of maximum power output (i.e. power produced by a solar cell P_{MPP}) to power input

(i.e. incident solar radiation P_{IN}). Thus, $PCE = \frac{P_{MPP}}{P_{IN}}$. P_{IN} is the sum over all wavelengths and is generally standardized at 1000 W/m^2 when the solar simulator is used.

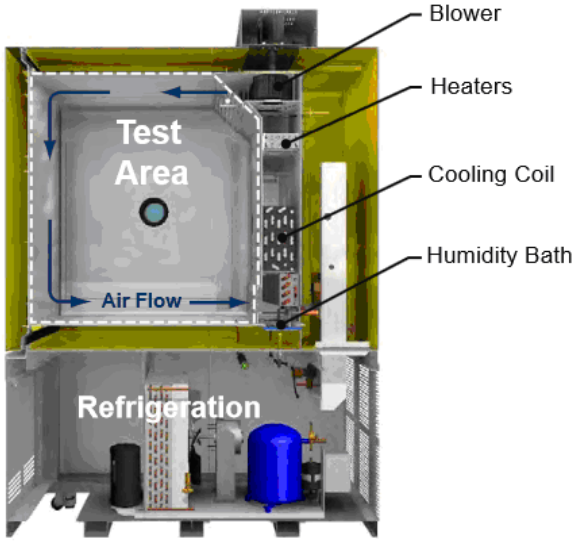
Another representation of the efficiency of a solar cell is by the fill factor (FF). FF is the ratio of the maximum power point to the product of open circuit voltage (V_{oc}) and the short circuit current (J_{sc}) [92] so that the equation is: $FF = \frac{P_{MPP}}{V_{OC} J_{SC}}$. The fill factor is how well the (yellow) rectangle area under the $J-V$ curve "fills" the maximum possible rectangle area with length of V_{oc} and width of J_{sc}.

3.4.2. Temperature and humidity chamber

A temperature and humidity chamber (Espec Corp.) was utilized in the humidity test of the solar cells in this project (Figure 3. 11(a)). In the chamber, the humidity bath heats water up and there is a re-circulating airflow by the blower for optimum performance. The detailed chamber construction is given in Figure 3. 11(b) [93]. The temperature and humidity levels are inputted by user via a touch-screen panel (Figure 3. 11(c). When the temperature and humidity conditions are reached, the batches of solar cells were placed in the middle of the chamber for the experiments.

(a)

(b)



(c)

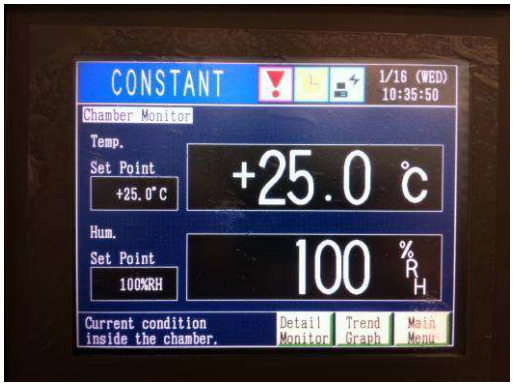


Figure 3. 11 (a) The environment chamber used in this project and (b) its interior construction and (c) the level of humidity can be set via a touch-screen control panel.

3.4.3. Bending test apparatus

A home-made bending test setup was used. The 1.5 cm width × 4 cm length plastic substrate was clamped at the two edge on the bending test setup. The flexible hybrid solar cell of around 1 cm × 0.8 cm was stuck at the middle of the plastic substrate. The left edge of the bending fixture was fixed and the right edge was moved to and fro by a rotating rod. The frequency and the number of the bending cycles were controlled by the rotating speed (rpm) of a motor and monitored by a counter, respectively. The bending radius at the center of the substrate can be controlled by varying the end-to-end length of the flexible bending substrate. By shorten the end-to-end length of the flexible substrate, the device would be bent into a curve shape at the middle of the substrate. We applied a compressive load axially at the two clamped edges of the substrate until the end-to-end length of the substrate decreased from the initial 40 mm to the final 30 mm in the bending experiments.

3.5. Material Characterization techniques

3.5.1. Scanning Electron Microscopy (SEM)

Scanning Electron Microscopy (SEM) is a convenient technique to obtain the surface morphologies or cross sectional images. Figure 3. 12 shows the photos of the SEM equipment used in this project (Photos ref from: [94]). Field emission scanning electron microscopy (Hitachi S4800 and Leo 1530) features high resolution of 1-2

nm and was used in this project to examine the silicon nanowires and PEDOT:PSS-covered silicon nanowires. The samples are stuck horizontally on flat sample holders and upright on L-shape sample holders by conductive tapes for obtaining surface morphologies and the cross sectional thickness respectively. To prevent accumulation of surface charges which cause scanning image faults, the surfaces of the samples were coated with an ultrathin layer of gold by sputtering. The specimens were placed into the vacuum chamber in the SEM, the electron beam was focused and deflected so that it raster-scanned the sample surface. When the primary electrons interact with the sample surface, they will loss energy and emit as secondary electrons. The detector collected the secondary electrons to generate morphology images.

SEM was also used in this project to examine the elements coated on the silicon nanowires array during the electroless etching process. Energy dispersive X-ray spectroscopy (EDX) was used to identify the elements contained in the materials. In the vacuum chamber of SEM, characteristic X-rays are emitted by the sample bombarded with the high-energy beam of electrons. EDX analyzed the dispersed energy of the characteristic X-rays to obtain a localized chemical analysis.

(a)

(b)

Figure 3. 12 Photos of the SEM used in this project: (a) Hitachi S-4800 FEG Scanning Electron Microscope (b) LEO 1530 FEG Scanning Microscope.

3.5.2. Transmission Electron Microscope (TEM)

Scanning Transmission Electron Microscope (TEM) was used in this project to study the crystallinities of the silicon nanostructures and their sidewalls. Figure 3. 13 shows the TEM equipment (Photos ref from: [94]). In the sample preparation, the silicon nanowires were scratched directly from the silicon substrate. The sample of

silicon nanowires were then transferred and supported on a mesh grid and a small screw ring was used to hold the grid in place on the TEM stage. In the vacuum column of TEM, a beam of high-energy electrons was transmitted through an ultra-thin specimen. There would be an interaction of the electrons when it was passing through the specimen. TEM analyzed the information contained in the electron waves collected from the sample. The bright field and diffraction pattern of the sample were obtained to give its information on morphology and crystallinity of material respectively.

Figure 3. 13 Photo of the TEM, FEI Tecnai G2 20 S-TWIN Scanning Transmission Electron Microscope, used in this project.

3.5.3. Capacitance-voltage ($C-V$) measurements

The capacitance-voltage ($C-V$) measurements were done with semiconductor Device Analyzer (Agilent B1500A) in this project. The photo of the equipment is given in Figure 3. 14. The frequency of 100 kHz was used for the $C-V$

measurements because it has better accuracy than 1 MHz test frequency and reduces errors due to cabling or device series resistance [95]. $C-V$ method is a non-destructive measurement of the depletion layer capacitance of semiconductor junction. The built-in voltage V_{bi} of the junction is at the explolated intersection point of the $1/C^2$ line with the horizontal axis. When $1/C^2 = 0$, $V = V_{bi} - kT/q$. The capacitance C can be lowered by reducing the junction area and increasing depletion width W by reducing the doping concentration and/or applying a reverse bias [96]. The depletion-layer thickness W can be calculated by equation [96]: $W = \sqrt{\frac{2\varepsilon_s (V_{bi} - V)}{qN_d}}$ where ε_s is the permittivity of semiconductor, V is the applied bias voltage and q is the elementary charges. From the slope of the line, $Slope = \frac{2}{qN_d \varepsilon_S A^2}$, the dopants concentration of the semiconductor N_d can be determined. A is the contact area.

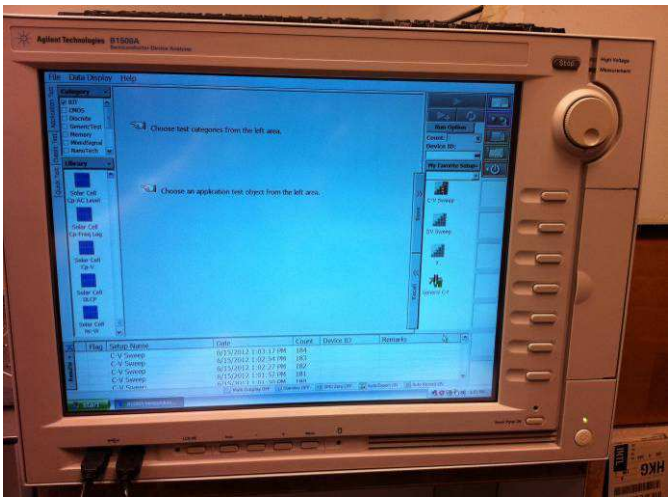


Figure 3. 14 Semiconductor Device Analyzer (Agilent B1500A) was used to obtained the built-in voltages of the solar cells.

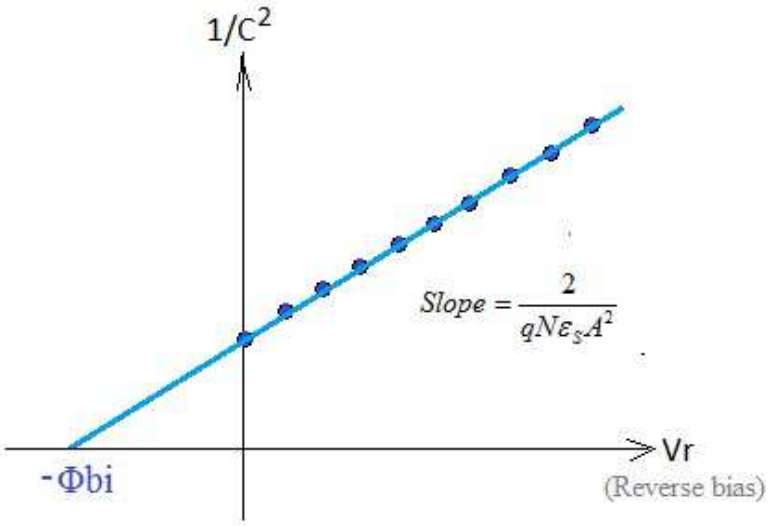


Figure 3. 15 The barrier height can be extracted from C-V measurement.

3.5.4. Reflectance and transmittance measurement

The reflectance measurement of the silicon wafers as well as the transmittance measurement of the PEDOT:PSS thin films on plastic substrates were handled with the Cary 4000 UV-Vis Spectrophotometer. The equipment allows quick sample fixture and alignment by using the spectrophotometer's accessory tools. Before the reflectance measurements began, it was calibrated by the reference halon plate. With the help of the Cary WinUV software, the reflectance and the transmittance spectrum of the specimens were measured in the range of 300−800 nm.

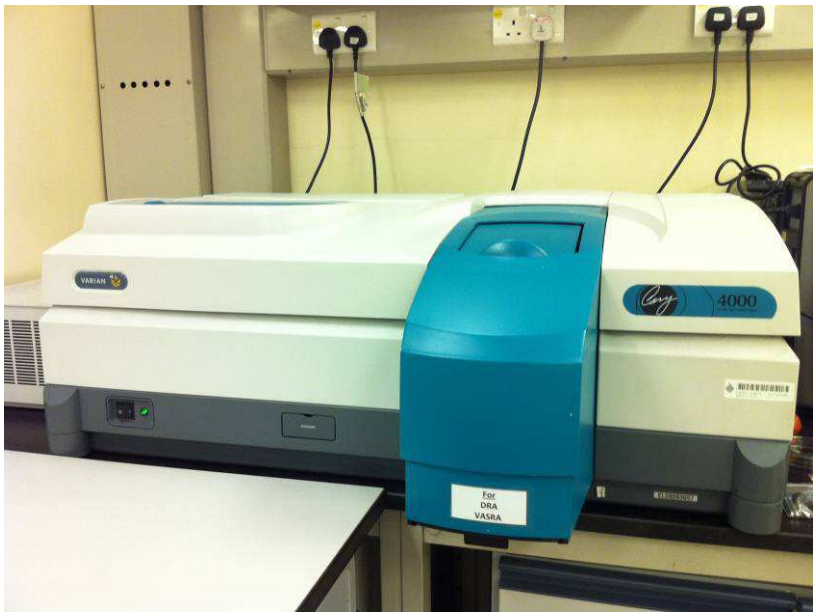


Figure 3. 16 Cary 4000 UV-Vis Spectrophotometer was used for reflectance and transmittance measurement.

3.5.5. Sheet resistance measurement

The sheet resistances of ITO substrates were measured with the four-point probe method (Lucas Labs 302), where the distance between two adjacent probes was 1 mm. By passing a current through two outer probes and measuring the voltage through the two inner probes allow the measurement of the substrate's resistivity [97]. Using the voltage and current readings across the probes, the sheet resistivity ρ can be calculated by the equation: $\rho = \frac{\pi}{\ln(2)} \cdot \frac{V}{I} = 4.53 \cdot \frac{V}{I}$. The unit for sheet resistivity is Ω/sq.

(a) (b)

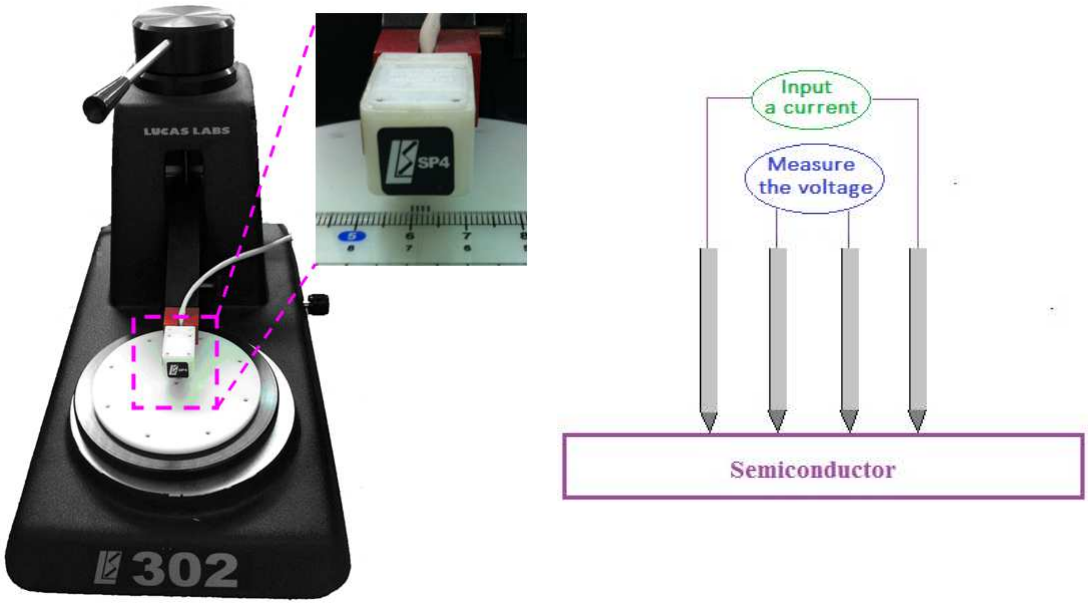


Figure 3. 17 (a) The four-point probe equipment was used to measure the sheet resistance of the ITO substrates and polymer thin film. (b) Schematic of the four point probe measurement.

3.5.6. Atomic force microscopy (AFM)

The surface morphologies of polymer films were examined by atomic force microscopy (AFM, Nanoscope V with Multimode 8 controller) in this project. The AFM equipment was shown in Figure 3. 18. During AFM measurement, a cantilever with a sharp tip at its end was used to scan the surface of the specimen. When the tip was brought into proximity of a sample surface, there are forces between the tip and the sample. Hence, there is a deflection of the cantilever according to Hooke's law. The deflection signal was transformed into surface morphology image.

As tapping mode AFM was used, the phase images were also obtained for the information of the variations in composition of the samples.

Figure 3. 18 Scanning Probe Microscope (Digital Instruments NanoScope IV).

Figure 3. 19 The cantilever tip scanned the surface of a polymer film coated on a glass substrate.

3.5.7. Thin film thickness measurement

The Tencor P-10 surface profiler was used to measures the film thickness of the samples. Some steps on the sample were created by scratching a few thin lines on it by a cutter. The step height was measured by the highly-sensitive cantilever tip in the profiler, scanning across the steps of the sample. In the experiment, the scan length was 200 μm at a scan speed of 10 μm/sec. The sampling rate was 50 Hz.

Figure 3. 20 The Tencor P-10 surface profiler was used to measure the thickness of thin films in this project.

CHAPTER 4 SURFACE TEXTURIZATION EFFECT ON SILICON/PEDOT:PSS HYBRID SOLAR CELLS

4.1. Introduction

Silicon wafer is the light absorption layer for the silicon/PEDOT:PSS hybrid solar cell. However, there are two main problems in the planar silicon. First, the planar and surface-polished surfaces of the commercial silicon wafers are usually shiny. The high reflective index of silicon results in a large portion of light reflected away from the surface of planar silicon. The silicon solar cell with planar silicon surface suffers high optical loss problem. This problem directly reduces the amount of available photons for photocurrent conversion. Second, in the hybrid silicon solar cell with planar junction, some minority carriers in deeper material region have to diffuse a long distance to reach the junction. This hinders the dissociation and extraction of light-induced charge carriers, which could potentially reduce the power conversion efficiency of the solar cells.

Silicon nanowires (SiNWs) array is attractive to improve optical absorption and increase junction area for the purpose of efficient light to electrics conversion. SiNWs can suppress reflection loss from the front surface and significantly enhance

light absorption over a wide spectrum range. Moreover, SiNWs can form radial junction so that the junction area is enlarged. The dissociation and collection of the photogenerated minority charge carriers could be effective as long as the diffusion length is larger than the wire radius. Hence, the SiNWs array was fabricated on the planar silicon wafer for the efficiency improvement in the silicon/PEDOT:PSS solar cell. In this chapter, we textured the silicon surface from planar into nanowires morphology by metal assisted electroless etching method. The light reflectivity, carriers recombination and silicon−PEDOT:PSS adhesion were studied to explain the effect of SiNWs in the hybrid silicon/PEDOT:PSS solar cell. The factors studied here could serve as the basis for the design and development for high efficiency silicon/PEDOT:PSS hybrid solar cells.

4.2. Experimental procedures

4.2.1. Texturization of silicon surface by electroless etching

Silicon wafers were cleaved into area of 1 cm × 1 cm. The cleaved silicon wafers were cleaned in detergent water, de-ionized water, acetone and 1,2-propanol for five minutes in an ultrasonic cleaner sequentially. Then, the wafers were UV ozone treated for 15 minutes to remove the organic impurities on their surfaces. Afterwards, the wafers were etched in a 5% hydrofluoric (HF) acid solution for 60 minutes to remove the oxide on the surfaces.

Silicon nanowires (SiNWs) were prepared by metal assisted electroless etching process. The mechanism of electroless etching process was described in chapter 2.4.2. Silicon wafers were immersed and etched in a 0.023 M silver nitrate ($AgNO_3$) and 5.6 M HF solution at room temperature. The silver ions reduced to silver atoms to assist HF etching vertically with respect to the silicon (100) surface. The length of NW corresponds to the etching time. Texturization of silicon surfaces were done by etching time of 5, 30, 60, 90 and 120 min respectively. After etching, the textured wafers were rinsed clean with deionized water. Then, they were soaked into concentrated nitric acid (65%). Finally, the textured wafers were immersed into 5% HF solution to remove the oxide layer on the SiNWs. They were dipped and rinsed clean with deionized water, and kept in desiccant box before use.

4.2.2. Si/PEDOT:PSS Device fabrication

The small pieces of ITO glass were cleaned in detergent water, de-ionized water, acetone and 1,2-propanol for five minutes sequentially in ultrasonic cleaner.. The ITO glass were treated with UV ozone for 15 minutes. Afterwards, they were collected for the subsequent spin-coating process.

Mixture of PEDOT:PSS and ethylene glycol solution was spin-coated on the UV ozone treated ITO glass at 750 rpm for 10 seconds. Next, the silicon wafer was put on top of the wet PEDOT:PSS film and then kept in desiccant box. Afterwards, the device was annealed at 110 ºC for 15 minutes in an oven in air. Back cathode

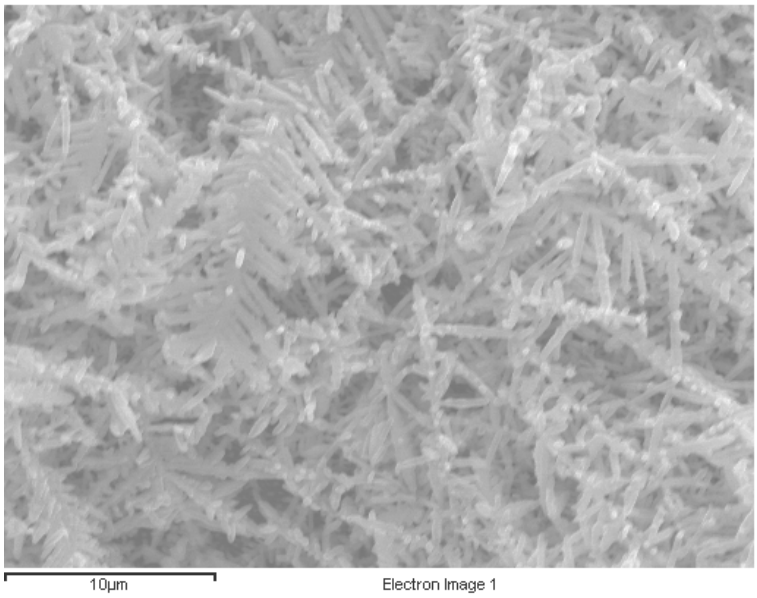
ohmic contact was made by depositing a thin layer of GaIn eutectic alloy on the back side of silicon.

4.3. Surface texturization of silicon

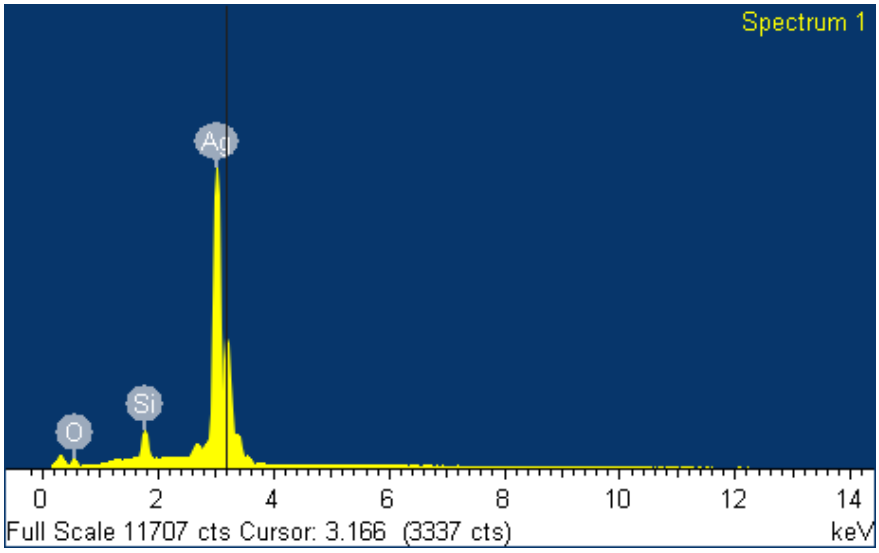
The experimental results on the relationship between the texturization process duration and the solar cell's power conversion efficiency are reported in this section.

4.3.1. SEM characterization of the morphology of the texturized silicon surface

When conducting the etching process on a silicon substrate, a silvery color coating was found on the surface of the silicon substrate. The morphology of this silvery color coating was characterized by SEM and it was a dendrite-like structure (Figure 4. 1(a)). EDX analysis (Figure 4. 1(b)) confirmed that the composition of the coating was silver (Ag).



(a)



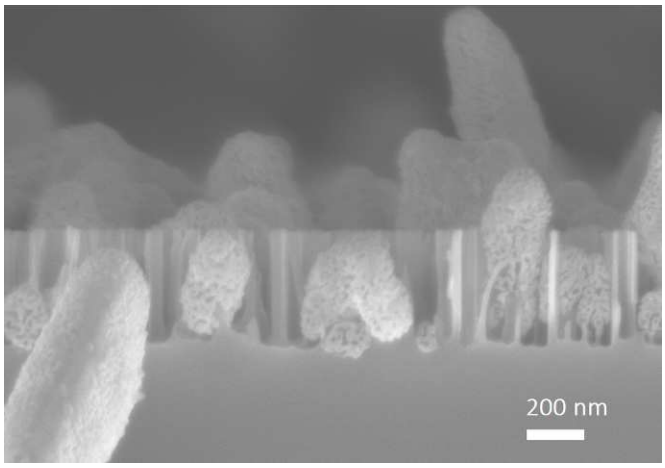
(b)

Figure 4. 1 (a) SEM image of the silver dendrites and (b) the EDX analysis.

To understand how the planar silicon surface was etched into nanostructures, the cross-sectional SEM images were captured to get more information. These images implied that at first, shallow pits containing the Ag particles were formed due to the etching of the beneath silicon dioxide. As the reaction proceeds, some small Ag particles sunk into the deep pits (Figure 4. 2 (a)), but further Ag particles that

cannot enter the pits grew towards specific favorable directions, branched Ag dendrites eventually covered a large portion of the surface of the silicon wafer (Figure 4. 2 (b)). Subsequent growth consumed a large quantity of the surplus Ag atoms and the deposition of Ag occurred on these silver dendrites at particular directions. This prevented the formation of a compact Ag granular film. Because the Ag particles were trapped by the pits and cannot move horizontally on the silicon surface, highly localized and site-specific etching occurred beneath these trapped Ag particles. Under these circumstances, the initial shallow pits deepened when the underlying silicon dioxide dissolved and SiNWs were formed. The top view and cross-sectional view of the SiNWs were shown in Figure 4. 3.

(a)



(b)

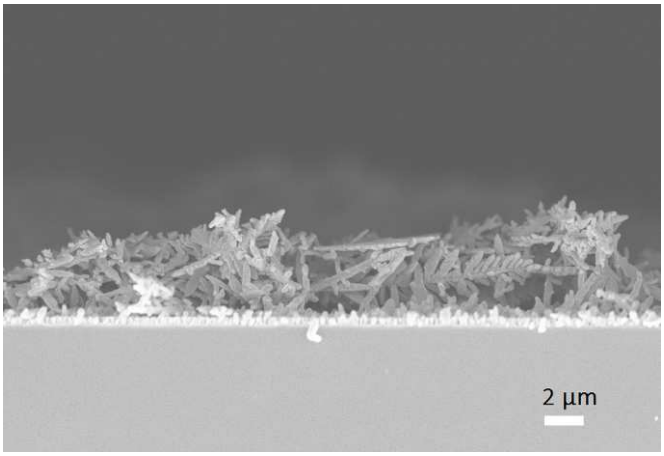
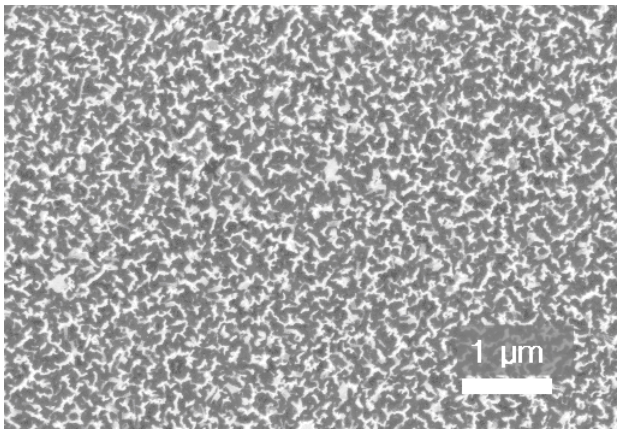
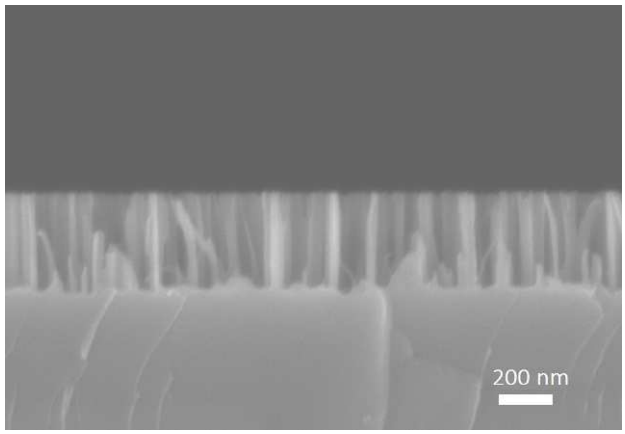


Figure 4. 2 (a) Shallow pits contained with Ag particles, but (b) the aggregation of Ag particles grew into branched silver dendrites.



(a)



(b)

Figure 4. 3 (a) Top view and (b) cross-sectional view of SiNWs grown by electroless etching.

Experimental results indicated that the length of the SiNWs was proportional to the etching duration. The cross-sectional SEM images of various length of SiNWs were recorded in Figure 4.4(a-f). Results shown that etching time of 3, 5, 30, 60, 90 and 120 min obtained nanostructures with length of 0.2, 0.39, 2.47, 3.87, 4.33 and 5.87 μm respectively. Figure 4.4(g) shows the etching rate of silicon nanostructure was around 83 nm/min initially and decreased to 33 nm/min after 1 hour etching. The rate decrement might be due to the consumption of the etchant.

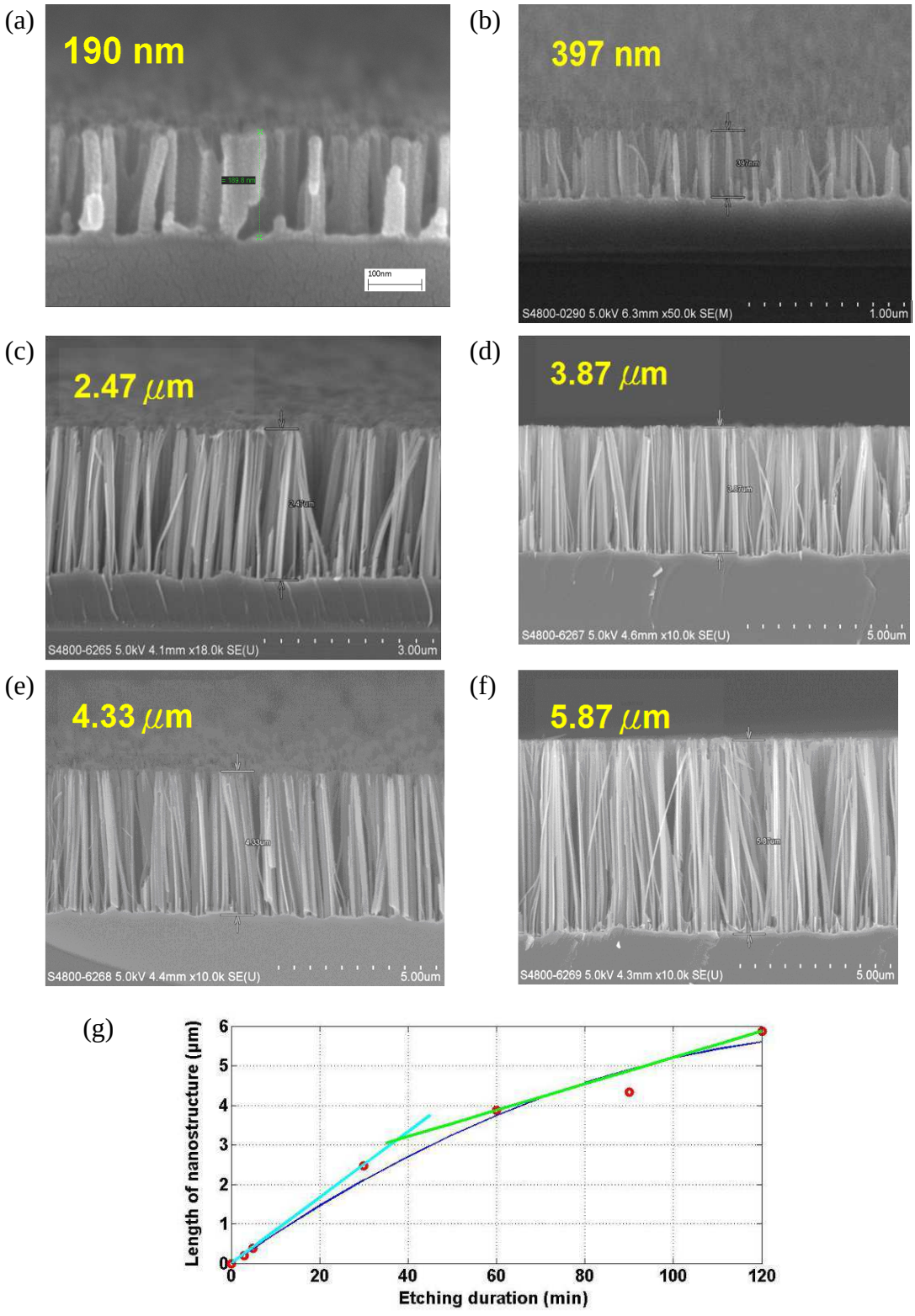


Figure 4.4 SEM cross section images of silicon nanostructures fabricated by underwent an etching time of (a) 3, (b) 5, (c) 30, (d) 60, (e) 90 and (f) 120 min.

4.3.2. IV characterization

The effect of surface texturization on device efficiency was studied. The solar cell fabrication procedures were described in section 4.2.2. Referred to the summarized results in Table 4.1, the power conversion efficiency (PCE) of the planar silicon hybrid solar cell was 1.1%, with open-circuit voltage (V_{oc}) of 0.5 V, short circuit current (J_{sc}) of 8.5 $mAcm^{-2}$ and fill factor (FF) of 26.8%. On the other hand, the solar cell with SiNWs' length of 0.39 μm had the highest PCE of 6.67%, with V_{oc} of 0.55 V and J_{sc} of 24.13 $mAcm^{-2}$. The J−V characteristic curves of the devices were plotted in Figure 4.5. With longer SiNWs length from 0.2 to 3.87 μm, the device efficiency performances maintained at around 6−7%. But there was a gradual J_{sc} decrease from 24.13 to around 20 $mAcm^{-2}$. The FF of the SiNWs hybrid solar cells were around 50 to 60%. With longer SiNWs length from 3.87 to 5.87 μm, the device efficiency performances decreased gradually from 6.21 to 3.55%. J_{sc} decreased from 21.48 to 14.94 $mAcm^{-2}$. The photovoltaic output characteristics in Figure 4. 6 shows that all J_{sc}, FF and PCE of the SiNWs devices were better than those of the planar devices. However, there was a lower V_{oc} in SiNWs devices than the planar device if the SiNWs was longer than 3.87 μm.

Etching time (min)	Length of SiNWs (μm)	V_{oc} (V)	J_{sc} ($mAcm^{-2}$)	FF (%)	PCE (%)
0	**planar**	0.50	8.50	26.80	1.10
3	**0.20**	0.54	23.39	43.52	5.45
5	**0.39**	0.55	24.13	50.15	6.67
15	**1.25**	0.55	24.96	46.81	6.42
30	**2.47**	0.53	19.88	58.60	6.14
60	**3.87**	0.49	21.48	59.25	6.21
90	**4.33**	0.43	17.67	54.79	4.20
120	**5.87**	0.43	14.94	54.87	3.55

Table 4.1 Summary of the J-V performances of the planar and nanostructured devices

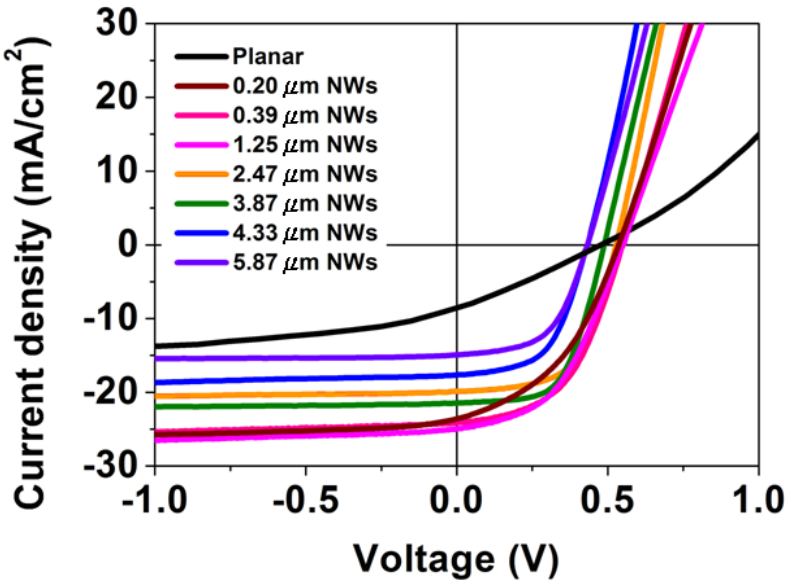


Figure 4.5 J-V characteristic curves of the planar and surface textured devices

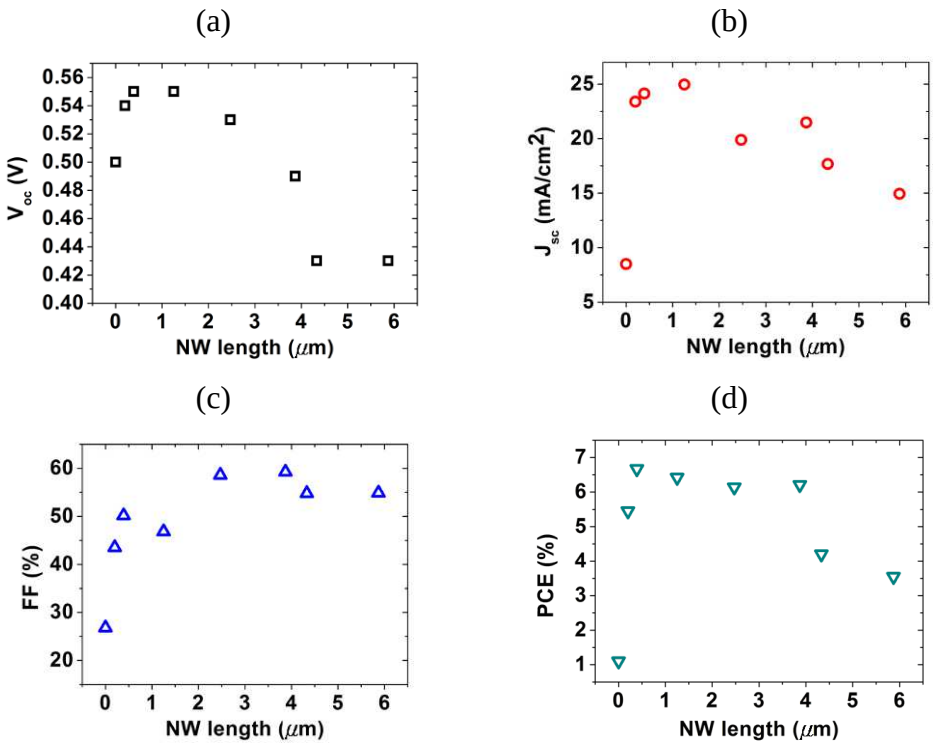


Figure 4. 6 The photovoltaic output characteristics of the planar and surface textured devices. (a) open circuit voltage (V_{oc}), (b) short circuit current (J_{sc}), (c) fill factor (FF), (d) power conversion efficiency (PCE).

4.3.3. Reflectance measurement

Comparisons were being made between planar silicon and SiNWs-texturized hybrid solar cells. Referring to Table 4.1, the PCE of the planar silicon hybrid solar cell was around 1.1% and the performance was worse than all of the SiNW-texturized solar cells. Moreover, its J_{sc} and FF were also worse than all of the SiNW-texturized solar cells. To explain this circumstance, we compared the reflectance of the planar silicon and the nanostructured silicon substrates to explain the relative low PCE of the planar device. Regarding to Figure 4.7, there was an

obvious decrease of reflectance of the SiNWs surfaces compared to the planar silicon surface. For planar silicon surface, the reflectance was around 40−70% in the 300−500 nm region and around 30−40% in 500−800 nm region, whereas the purple curve in Figure 4.7 shows that the reflectance of the SiNWs surface with 5.87 μm SiNWs-texturization fell below 8% within the entire visible spectrum. Referring to the optical images, the planar silicon surface was a silvery shiny surface (Figure 4.8 (a)) whereas the SiNWs surface was dull black color (Figure 4.8 (b)). The relative low PCE of planar silicon device than the SiNWs devices should be due to the poor light absorption.

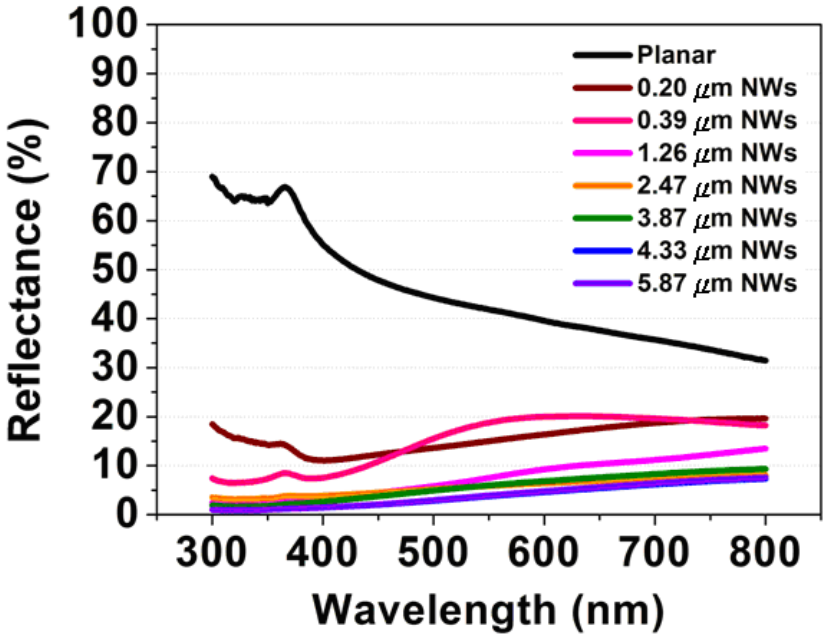
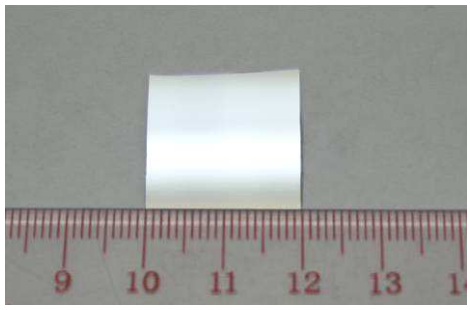


Figure 4.7 Reflectance of the planar silicon surface and SiNWs-texturized silicon surfaces. The reflectance for a 5.87μm SiNWs-texturized silicon wafer is below 8% in the visible spectrum.

(a)



(b)

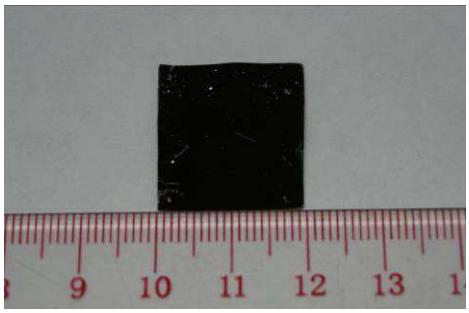


Figure 4.8 Optical images of (a) planar silicon surface and (b) nanostructure silicon surface after 120 min etching.

The poor light absorption in the planar silicon device can be explained by the mismatch of refractive indexes of silicon material (n_s) and air medium (n_a). When light moves from the air medium into the silicon medium, the amount of light reflection (R) can be calculated from the refractive indexes by the Fresnel reflection:

$$R=\frac{1}{2}\cdot\left(\left(\frac{n_a\cos\theta_a-n_S\sqrt{1-\left(\frac{n_a}{n_S}\sin\theta_a\right)^2}}{n_a\cos\theta_a+n_S\sqrt{1-\left(\frac{n_a}{n_S}\sin\theta_a\right)^2}}\right)^2+\left(\frac{n_a\sqrt{1-\left(\frac{n_a}{n_S}\sin\theta_a\right)^2}-n_S\cos\theta_a}{n_a\sqrt{1-\left(\frac{n_a}{n_S}\sin\theta_a\right)^2}+n_S\cos\theta_a}\right)^2\right) \qquad \text{Eq 4. 1}$$

where θ_a is the angle between incident light to the normal of the air−silicon interface as shown in Figure 4. 9. When the light falls normally onto the silicon surface, $\cos\theta_a=1$. Eq. 4.1 is simplified to $R=\left|\frac{n_a-n_s}{n_a+n_s}\right|^2$. The refractive index of air (n_a) is 1. The refractive index for planar silicon (n_s) is 4.08 at 550 nm (Table 4. 2). Hence,

the calculated light reflection from the planar silicon surface is 37%. If the silicon surface was texturized with 10 μm silicon nanowires array by metal-assisted electroless etching, the effective refractive index at 550 nm reduced strongly to 1.26 [98], by referring to Table 4. 2. Hence, the calculated light reflection from the SiNWs surface is 1.3% for the 10 μm SiNWs textured silicon surface. This result showed that the decrease of the refractive index in the NWs structure would promote more light trapping. SiNWs significantly reduced the light reflection as well as the optical loss in the hybrid silicon solar cells.

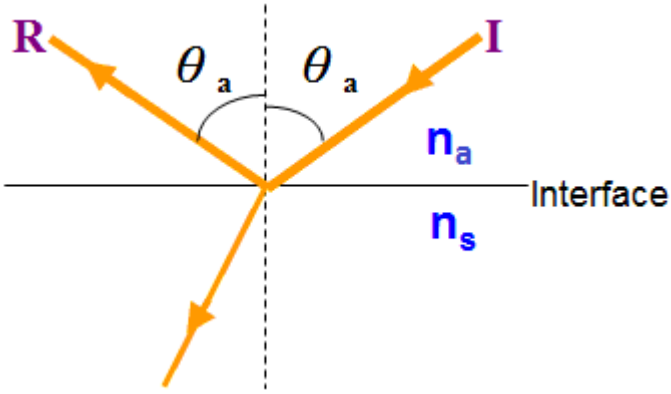


Figure 4. 9 The reflection and transmission of light at the air-silicon interface.

Wavelength (nm)	**Planar n_s**	**10 μm SiNWs n_s**
300	5.06	1.26
350	5.48	1.28
400	5.59	1.30
500	4.29	1.28
550	4.08	1.26
600	3.94	1.26

650	3.84	1.26
700	3.77	1.26
750	3.72	1.26
800	3.68	1.26

Table 4. 2 Refractive indexes of planar silicon [99] and 10μm silicon nanowires [98]

4.3.4. Recombination current

Generally, more light was trapped in the long SiNWs array than the short array and this should lead to higher J_{sc} as well as better PCE of the long SiNWs devices due to better light absorption. However, the PCE results recorded in Table 4.1 did not show this trend and there was a decrease of PCE in the long SiNWs devices than the short 390 nm NWs device. The polymeric nature of PEDOT:PSS caused aggregation at the top portion of the SiNWs array throughout the film drying process. Figure 4. 10 showed that a thin layer was coated onto the short SiNWs array. However, the bottom part of the SiNWs was not fully covered by PEDOT:PSS. It was found that the PEDOT:PSS covered the top surface of nanowires instead of infiltrate into the small spacing between SiNWs thoroughly. The infiltration became more difficult for the long NWs (Figure 4.11). Carriers were collected less efficiently to the electrode of the long SiNWs than the short SiNWs. The poor carrier collection was because of the higher recombination rate in the long SiNWs solar devices. [100]

The higher recombination rate can be revealed from the larger reverse saturation current (J_0) values. J_0 values were estimated by

equation $V_{oc} = (kT/q)\ln[J_{sc}/J_0]$ [101]. The J_0 values of the silicon hybrid solar cells, with and without nanowires texturization process, were summarized in Table 4. 3. J_0 of the device with 3.87 μm SiNWs was 1.1×10^{-7} $mAcm^{-2}$, that was about one order of magnitude higher than the J_0 of the device with short 400 nm SiNWs (1.2×10^{-8} $mAcm^{-2}$). A large J_0 value corresponds to a larger recombination in the device. Hence, the leakage of carriers across the junction in the long SiNWs was larger than that in the short 400 nm SiNWs.

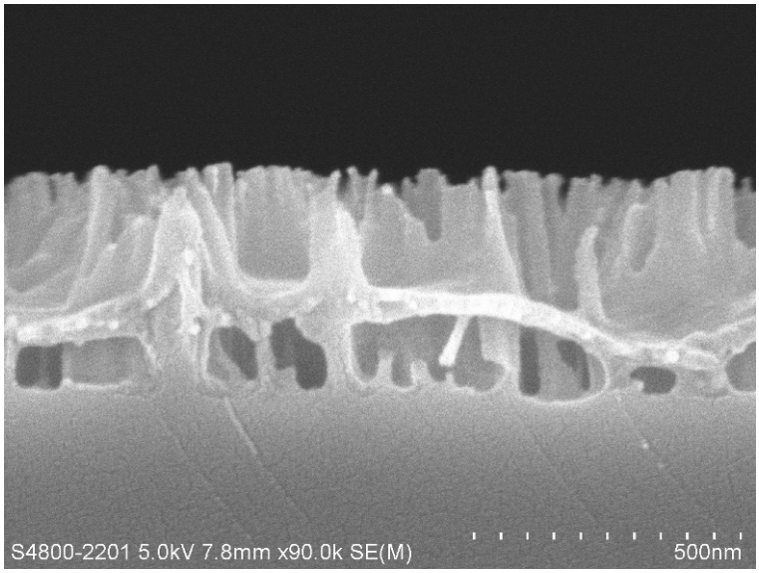


Figure 4. 10 A thin layer of PEDOT:PSS is coated onto the short SiNWs.

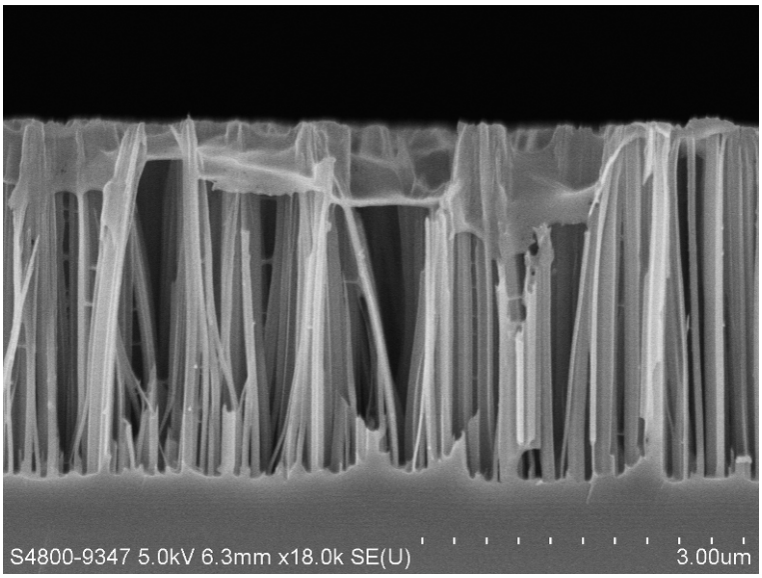


Figure 4.11 Difficult infiltration of PEDOT:PSS into the bottom of long SiNWs.

Length of SiNWs (μm)	**J_0 ($mAcm^{-2}$)**
planar	2.95×10^{-8}
0.20	1.71×10^{-8}
0.39	1.20×10^{-8}
1.25	1.24×10^{-8}
2.47	2.15×10^{-8}
3.87	1.10×10^{-7}
4.33	9.39×10^{-7}
5.87	7.94×10^{-7}

Table 4. 3 The calculated leakage current J_0 at various devices with different length of nanowires.

4.4. Conclusions

In this chapter, the results showed that the SiNWs−texturized surfaces were better than the planar silicon surface for higher power conversion efficiency of the hybrid silicon/PEDOT:PSS solar cells. The metal assisted electroless etching technique was used to texture silicon surface and the etching rate on silicon by $HF/AgNO_3$ solution was around 83 nm/min. After a 5 min etching of the silicon substrate, the solar cell with a 390 nm SiNWs−texturized surface performed the best PCE among the cells with various SiNWs lengths. The 390 nm SiNWs−texturized device had the PCE of 6.67% whereas the planar device had the PCE of just 1.1%. SiNWs surfaces had lower light reflection than the planar surface. This favored better light-to-electricity conversion. However, NWs lengths longer than 390 nm were not as good PCE as the 390 nm NWs. This was because of the poor adhesion of PEDOT:PSS film at the bottom of the long SiNWs, leading to the higher charge recombination in the long SiNWs solar cells.

CHAPTER 5 EFFICIENCY IMPROVEMENT IN SILICON NANOWIRES/PEDOT:PSS HYBRID SOLAR CELLS BASED ON FORMIC ACID TREATMENT

5.1 Introduction

In the hybrid silicon solar cell, the poly(3,4-ethylenedioxythiophene): poly(styrenesulfonate) (PEDOT:PSS) was deposited onto silicon to form the Schottky junction. PEDOT:PSS has many advantages such as high optical transparency, good thermal stability, and convenient solution processability. However, the pristine PEDOT:PSS also suffers the low conductivity problem of less than 1 S/cm. The low conductivity of the PEDOT:PSS can reduce the carrier collection, lifetime and the performance of the devices [102]. That is why in the fabrication of silicon/PEDOT:PSS hybrid solar cells, it is customarily added 5 wt% dimethyl sulfoxide (DMSO) into PEDOT:PSS for conductivity enhancement [103-107]. DMSO is a common secondary doping solvent and the conductivity of DMSO-added PEDOT:PSS film is around 850 S/cm [108]. The DMSO molecules can screen and reduce the coulombic attraction between PEDOT and PSS. Since PEDOT and PSS have different hydrophilicities and hence phase segregation can

occur between them. Therefore, greater conductive PEDOT grain size and better connected PEDOT chains are observed in the DMSO-added PEDOT:PSS film after conductivity enhancement [109]. Most importantly, it was shown that the reduction in PSS/PEDOT composition ratio at the surface with appropriate amount of DMSO in PEDOT:PSS, which affected the sheet resistance, front carrier collection and the solar cell properties [110]. According to the XPS S 2p spectra of the PSS/PEDOT composition ratio at the surface decreased from 3.25 (without DMSO) to 3.15 (5 wt% DMSO addition), the PCE of the silicon/PEDOT:PSS hybrid solar cell improved from 2.4 (without DMSO) to 10.8% (5wt% DMSO addition). The lower PSS/PEDOT composition ratio at the surface of the conductivity enhanced PEDOT:PSS film means that the ratio of insulating PSS to the conductive PEDOT decreases and hence the conductivity improves at the surface resulted in better PCE of the silicon/PEDOT:PSS hybrid solar cells. Literature also reviewed that co-addition of DMSO and an organic substance into PEDOT:PSS solution could further improve the performance of the silicon/PEDOT:PSS hybrid solar cells. For example, Liu et al mixed 0.1% Zonyl fluorosurfactant and 5 wt% DMSO into PEDOT:PSS solution to reduce the resistivity of PEDOT:PSS film, the series resistance of the device decreased 24% and reported a 9.7% increment in PCE in silicon/PEDOT:PSS hybrid solar cells [61]. Despite mixing the additives such as DMSO and Zonyl into the PEDOT:PSS solution, treatments on the annealed PEDOT:PSS films with polar organic compounds effectively enhanced the conductivity of PEDOT:PSS films. Film treatment method not only led to better connected PEDOT chains but also facilitated significant removal of excess PSS from

the film surface [111]. Hence, methods employing film treatment or both (film treatment and additives in the solution) show better conductivity than only the additives in the PEDOT:PSS aqueous solution. Zhao et al showed that the PCE improved nearly twice after nitric acid vapour treatment to reduce the resistivity of the PEDOT:PSS by nearly 40% [112]. These seem probable that a low resistivity of PEDOT:PSS plays a critical role on the power conversion efficiency of such kind of hybrid solar cell. Recently, Mengistie et al reported the conductivity of PEDOT:PSS (PH1000) can be enhanced to 2050 S/cm by treated the PEDOT:PSS film with 98 wt% formic acid at 140 ºC and showed that it was a promising high conductive material to replace the ITO electrode on flexible substrate [113]. The protonation of PSS by acid led to a neutral PSSH chains. The absence of coulombic attraction between the positively charged PEDOT chains and neutral PSSH chains resulted in the phase segregation between PEDOT and PSS and hence the conductivity of PEDOT:PSS was enhanced three order of magnitude through the formic acid treatment. The formic acid treatment was a simple and low-cost method to reduce the resistivity of PEDOT:PSS film.

In this chapter, we studied the effect on the efficiency of SiNWs/PEDOT:PSS hybrid solar cells based on formic acid treatment. The treatment was carried out by dropping formic acid onto the annealed 5 wt%−DMSO−added PEDOT:PSS film which was the active layer of the hybrid solar cell. The PCE improved from 8.00 to 9.31% in the 98 wt% formic acid treated devices, and the improvement was attributed to an increase in open circuit voltage (V_{oc}) and fill factor (FF). To understand the efficiency improvement, we analyzed the characteristic parameters of

the SiNWs/ PEDOT:PSS hybrid solar cell model with the Lambert's W-function and discussed the effect of the formic acid treatment on the photovoltaic characteristics of the hybrid solar cells. We also studied the conductivity of the formic acid treated PEDOT:PSS films, it was found that higher film conductivity would lead to higher PCE.

5.2 Materials and methods

First of all, the silicon nanowires were fabricated on silicon substrate and the procedures were given in chapter 4.2.1. Next, the nanowires textured silicon wafers were immersed in HF for 3 minutes. Then, they were exposed in ambient air for 15 minutes to improve the surface wetting. PEDOT:PSS solution (Clevios PH1000 mixed with 5 wt% DMSO) was filtered via 0.45 μm filters and dropped on the nanowires textured silicon wafers. In order to avoid gas bubbles and make good contact between PEDOT:PSS and nanowires, the PEDOT:PSS solution was at rest on the silicon nanowires surface for 1 minute before the spin-coating process. Then, the PEDOT:PSS solution was spin-coated on the nanowires textured silicon wafers at 3000 rpm for 30s. The wet PEDOT:PSS films were annealed at 140 ºC for 5 minutes. Afterwards, 100 μl of different concentration of formic acid was dropped onto the annealed PEDOT:PSS film and then dried at 140ºC for 5 minutes. Finally, gallium indium (GaIn) eutectic alloy was deposited on the backside of the silicon wafers as cathode. Silver paste was screen printed at the front side of the silicon wafers and the exposure area was 40 mm^2.

5.3 Results and discussion

The schematic diagram of the SiNWs/PEDOT:PSS hybrid solar cell is given in Figure 5.1(a). Spin-coated PEDOT:PSS thin film had high transmittance so that light could be transmitted to the SiNWs/PEDOT:PSS interface. Figure 5.1(b) shows that the band alignment of silicon matched well with PEDOT:PSS such that PEDOT:PSS on the n-type crystalline silicon formed a Schottky contact at the junction. The role of PEDOT:PSS was a hole transport layer with work function around 5.2 V. When light shone on the solar cell, hole-electron pairs generated at the SiNWs/PEDOT:PSS interface. The built-in electric field separated holes and electrons, holes were transported to the anode via the PEDOT:PSS layer and electrons were transported to the cathode. For better light absorption, SiNWs array with a length of around 390 nm was fabricated on the top surface of silicon (Figure 5.1(c)). Referring to chapter 4, this length was optimized for the silicon nanowires array in the hybrid solar cells.

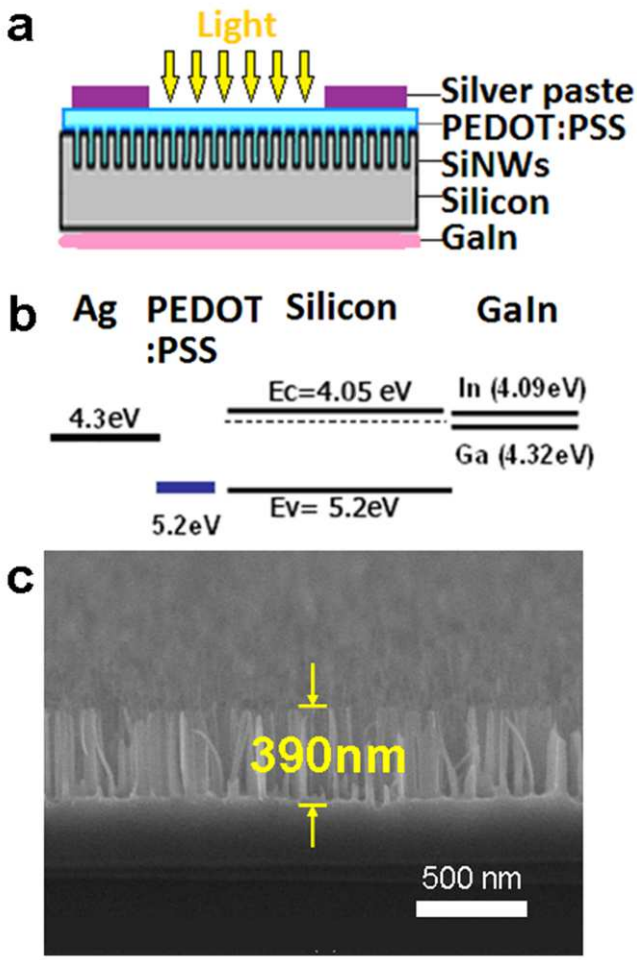


Figure 5.1(a) Schematic diagram and (b) the band diagram of the architecture of the SiNWs/PEDOT:PSS hybrid solar cell. (c) The cross-sectional SEM image shows the 390 nm silicon nanowires array after 5 minutes of electroless etching.

5.3.1 Efficiency improvement by formic acid treatment

The annealed 5 wt%−DMSO−added PEDOT:PSS films of the hybrid solar cells were treated by different concentration of formic acid solution, and it was found that the cell had the highest PCE when 98 wt% formic acid solution was used.

Figure 5.2(a) shows the current density−voltage (J−V) curves of the untreated and

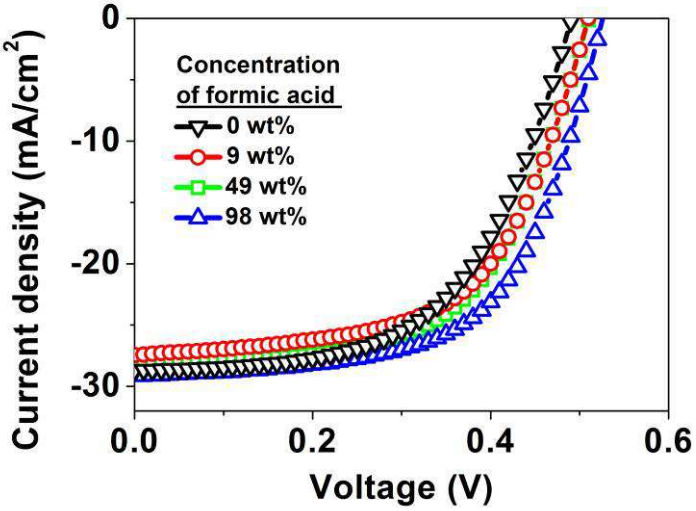
treated hybrid solar cells under different concentration (9, 49 and 98 wt%) of formic acid treatment. The PCE of the device, without formic acid treated, was 8.00% (Table 5.1). After formic acid treatment, there was an gradual increase in open circuit voltage (V_{oc}) from 0.491 to 0.526 V and fill factor (FF) from 56.9% to 60.8%. The short circuit current (J_{sc}) of the hybrid solar cells after formic acid treatment were nearly unimpaired, kept at around 28 mA/cm^2. This was a large extent due to the high transmittance of the formic acid treated PEDOT:PSS film that retained a good light absorption at the SiNWs/PEDOT:PSS interface. As shown in

Figure 5.2(b), the transmittance of the films at 550 nm wavelength, without and after 98 wt% formic acid treatment, were 97.2 and 96.5% respectively. The formic acid treatment retained the high transmittance of the untreated PEDOT:PSS film. The PCE reached 9.31% with V_{oc} of 0.526 V, J_{sc} of 29.1 mA/cm^2 and FF of 60.8% when 98 wt% formic acid solution was used (Table 5.1). There was a 16.4% PCE improvement in the SiNWs/PEDOT:PSS hybrid solar cells by carried out the PEDOT:PSS film treatment with 98 wt% formic acid.

FA concentration (wt%)	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	PCE (%)
0	0.491	28.68	56.85	8.00
9	0.510	27.44	59.07	8.26
49	0.511	28.19	60.00	8.64
98	0.526	29.14	60.81	9.31

Table 5.1 Summary of the photovoltaic performances of the SiNWs /PEDOT:PSS hybrid solar cells treated with different concentration of formic acid (FA).

(a)



(b)

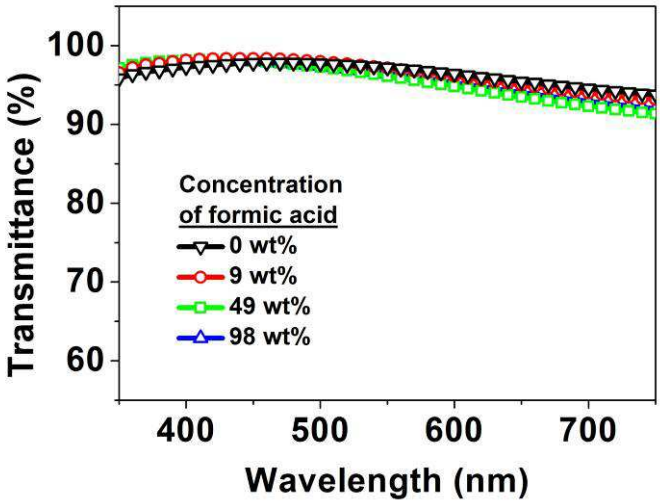


Figure 5.2 (a) The current density-voltage (J-V) curves show that the PCE is improved with higher concentration formic acid (FA) treated PEDOT:PSS films. (b) The transmittances of the FA treated and untreated films are around 97% at 550nm wavelength. The films with high transmittance allow most of the light to pass through to the light absorption material.

5.3.2 Photovoltaic characteristic parameters

In order to understand the improvement in V_{oc} and FF of the formic acid treated devices, we obtained the characteristic parameters of the solar cell model by curve fitting experimental J-V data into the Lambert's W-function [88]:

$$J = n \cdot \frac{V_{th}}{R_s} \cdot lambertw\left(\frac{J_0 R_s}{n \cdot V_{th} \cdot (1 + R_S / R_{sh})} \times e^{\frac{V + R_S (J_0 + J_L)}{n V_{th} (1 + R_S / R_{sh})}} \right) + \frac{V / R_{sh} - (J_0 + J_L)}{1 + R_S / R_{sh}} \quad \text{Eq 5. 1}$$

where J and V are the measured current density and voltage of the solar cell respectively; J_L, J_0, n , R_s ,R_{sh} are the light generation current density, reverse saturation current density, ideality factor, series resistance and the shunt resistance of the solar cell respectively. V_{th} is the thermal voltage that is equal to kT/q = 0.0259. The obtained characteristic parameters of the hybrid solar cell were summarized in Table 5.2.

FA concentration (wt%)	J_0 (A/cm^2)	n	R_s (Ωcm^2)
0	2.90×10^{-5}	2.48	2.23
9	3.79×10^{-6}	2.19	1.51
49	3.62×10^{-6}	2.17	1.44
98	2.12×10^{-6}	2.02	1.51

Table 5.2 Summary of the reverse saturation currents and the series resistances of the SiNWs /PEDOT:PSS hybrid solar cells treated with different concentrations of formic acid (FA).

Table 5.2 shows that the reverse saturation current J_0 was decreased from 2.90×10^{-5} (untreated) to 2.12×10^{-6} A/cm^2 (98 wt% formic acid treated). A smaller J_0 described lower carrier recombination in the solar cell, which can be explained by the equation of reverse saturation current in the thermionic emission model [114]:

$$J_0 = AA^*T^2 \exp(-\Phi_B/kT) \qquad \text{Eq. 5. 2}$$

where A is the area of solar cell, A^* is the effective Richardson constant (for n-type silicon, $A^*\approx252$ Acm^{-2}K^{-2}), T is the absolute temperature (298K), Φ_B is the barrier height and k is the Boltzmann constant.

From Eq. 5.2, the barrier height Φ_B of the Schottky junction was increased from 0.71 (untreated) to 0.77 V (treated). The 0.06 V higher Φ_B allowed better charges separation at the solar junction.

5.3.3 Relationship between ideality factor and built-in voltage

To further understand the mechanism of charge separation at the junction in the hybrid solar cells, $C-V$ measurement was carried out. In Figure 5. 3, the doping concentration of the silicon substrate was constant throughout the depletion region, therefore a straight line of $1/C^2-V$ curve was recorded. From the extrapolation at the x-axis intercept of the $1/C^2-V$ curve, the built-in voltage (V_{bi}) could be extracted. The V_{bi} inferred from the x-intercept of the CV plot was 0.59−0.63 V for the 98 wt%

formic acid treated device and 0.57−0.63 V for the pristine device. Both V_{bi} (pristine and treated) devices were around 0.6 V. They were similar because $C-V$ measurement predicted the built-in voltage in the absence of interface states, i.e. n=1 [115]. In our case, n were equal to 2.48 and 2.02 for the pristine and formic acid treated PEDOT:PSS respectively. These values greater than 1 meant that the effect of interface states in the silicon/PEDOT:PSS hybrid solar cells should not be ignored in determining V_{bi} so that the fundamental V_{bi} obtained from C−V measurement cannot represent the actual V_{bi} in the devices. Figure 5. 3(c) shows totally 50 devices with and without formic acid treatment that the built-in voltage was inversely proportional to the ideality factor. As the average value of n decreased from 2.48 to 2.02, the plot revealing that the built-in voltage increased from 0.43 V to 0.48 V after the formic acid treatment. The correlation between the built-in voltage (V_{bi}) and the ideality factor (n) of the silicon/PEDOT:PSS hybrid solar cells could be represented by the equation: $n = 9.186(0.706 - V_{bi})$.

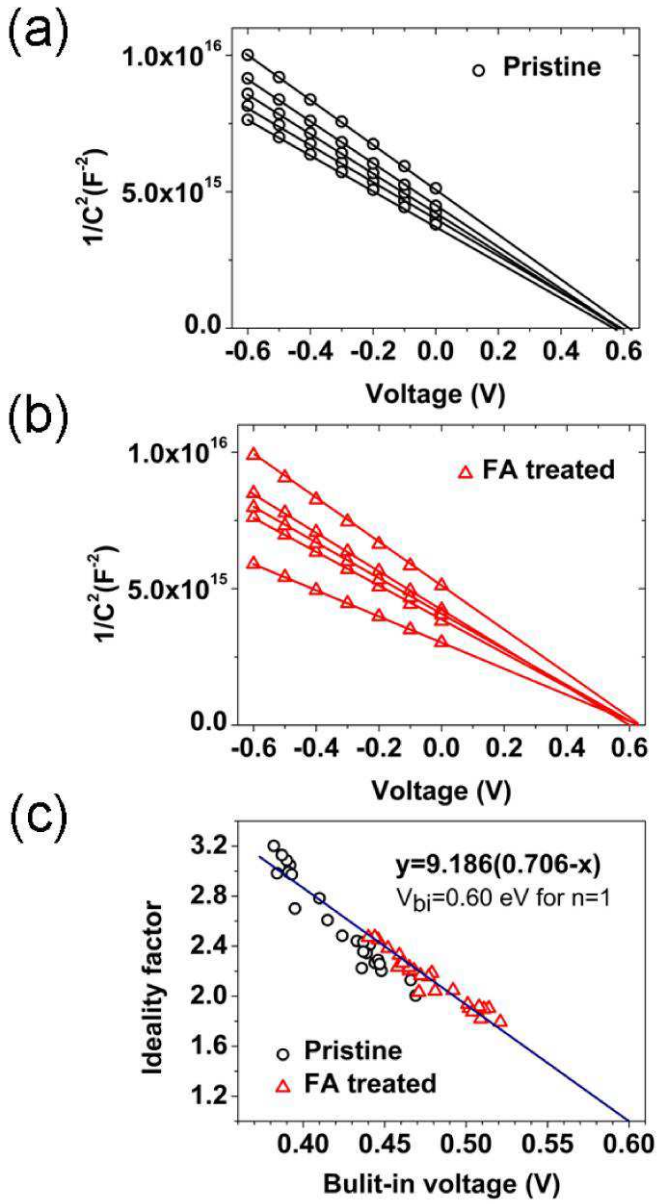


Figure 5. 3 $C-V$ measurement for the bulit-in voltage at the silicon/PEDOT:PSS interfaces of the (a) untreated and (b) formic acid treated devices. (c) The relationship between ideality factor and built-in voltage.

5.3.4 Conductivity measurement

It was noticed in Table 5.2 that the series resistance R_s decreased from 2.23 to 1.51 Ωcm^2 in the SiNWs/PEDOT:PSS hybrid solar cells after the 98 wt% formic acid treatment, and contributed to the improvement of FF. The decrease in R_s in the treated devices should probably relate to the increased conductivity of the PEDOT:PSS film. The conductivities of different concentrations of formic acid-treated PEDOT:PSS films were summarized in Figure 5. 4. For the as-prepared 5 wt%−DMSO−added PEDOT:PSS films, the conductivity was around 683 S/cm. There was a gradual increase in the conductivity of PEDOT:PSS film by using higher concentration formic acid in the treatment. The average conductivity of the PEDOT:PSS films after treatment by 9, 49 and 98 wt% formic acid were 962, 1456 and 1582 S/cm respectively. The conductivity enhancement of the PEDOT:PSS films after formic acid treatment should be ascribed to the more orderly oriented and aggregated conductive PEDOT chains. In the AFM phase images, the brighter area and darker area corresponded to PEDOT content and PSS-rich matrix respectively [116]. Figure 5.5(a) shows that the customary 5 wt% DMSO-added PEDOT film had some phase separation between PEDOT and PSS chains. For 98wt% formic acid treated 5% DMSO-added PEDOT film, the phase separation became even more obvious (Figure 5.5(b)). The phase separation between the conductive PEDOT grains and the insulating PSS matrix helped more interconnection between the conductive PEDOT grains such that the conductivity of the film improved. Height images showed that both the formic acid treated and untreated films were smooth.

The root mean square roughness of the treated and untreated films were 1.3 nm (Figure 5.5(c)) and 1.9 nm (Figure 5.5(d)) respectively. The significances of the high conductivity PEDOT:PSS film were enhancing charges transfer and lowering the series resistance. As a consequence, the 98wt% formic acid treatment doubled the conductivity of 5 wt%−DMSO−added PEDOT:PSS film and led to better PCE in the silicon/PEDOT:PSS hybrid solar cells.

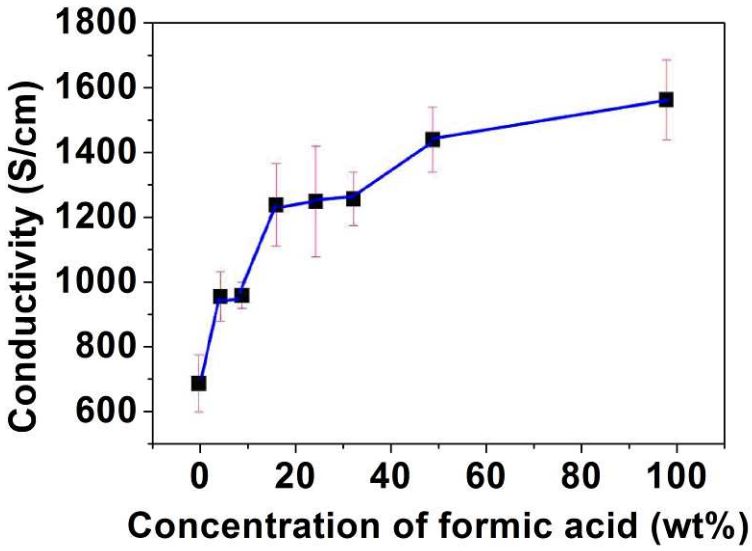


Figure 5. 4 Average conductivities of PEDOT:PSS films after treatment with different concentrations of formic acid. There are five samples for each concentration and the red lines show the error bars. The blue dotted lines are added as the aid for easy sight to the trend of conductivities improvement with higher formic acid concentrations.

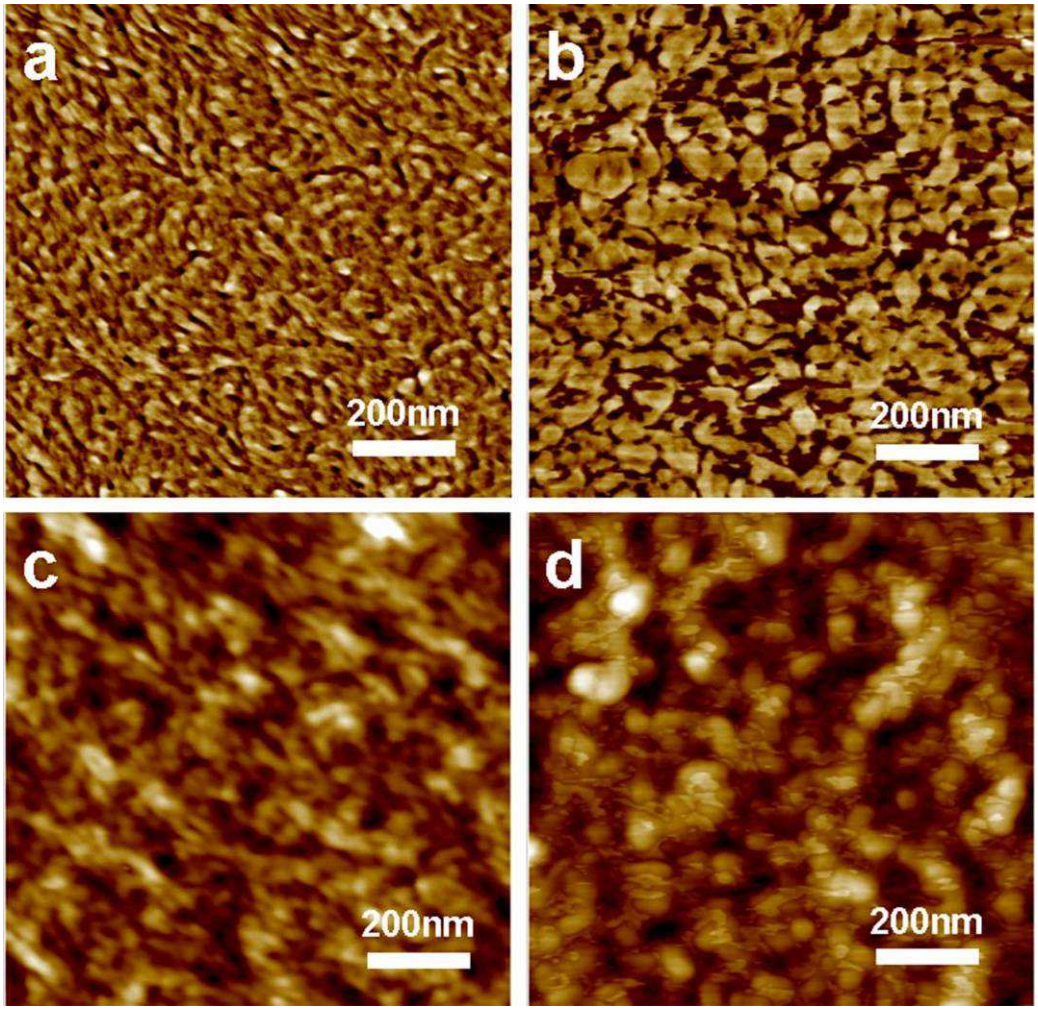


Figure 5.5 AFM phase and height images of (a,c) 5% DMSO-added PH1000 film and (b,d) Formic acid treated 5% DMSO-added PH1000 film. The upper is the phase image and the bottom is the height image. All images are 1μm × 1μm size.

To confirm the origin of the increase in conductivity, we used XPS to examine the chemical composition at the surface of the PEDOT:PSS films. PEDOT:PSS is a polymer mixture of two ionomers, PEDOT and PSS. The contents of PEDOT:PSS can be known by checking the content of sulphur because both PEDOT and PSS contain one sulphur atom per repeat unit. The sulphur atom in PEDOT is within the thiophene ring, whereas in PSS, it is included in the sulfonate moiety [117]. From

XPS sulphur 2p spectra of the PEDOT:PSS film, the sulphur atoms in PSS are relevant to the binding energy peaks at 169 and 167.8 eV and the sulphur atoms in PEDOT are relevant to those at 164.6 and 163.4 eV. By calculating the areas of the energy peaks, the composition ratio of PSS to PEDOT in the PEDOT:PSS film can be known. By comparing the areas of the energy peaks in Figure 5.6, it can be calculated that the compositional ratio of PSS to PEDOT decreased from 2.94 (pristine) to 1.22 (treated). The reduction in the proportion of PSS suggested that a greater amount of hole-transporting PEDOT was able to connect with the silver grid anode, which would be expected to reduce the R_s of the device.

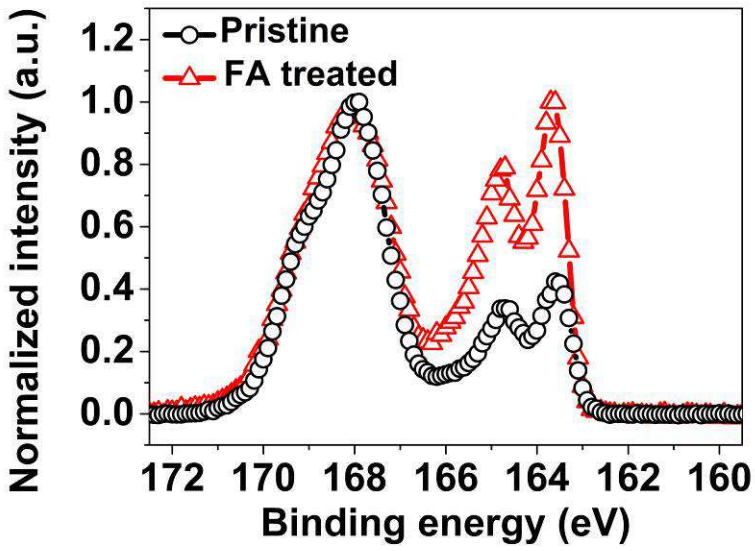


Figure 5.6 XPS sulphur 2p spectra of the PEDOT:PSS film showing the decrease of the PSS-to-PEDOT compositional ratio after FA treatment.

5.4 Conclusions

In conclusion, the PCE of SiNWs/PEDOT:PSS hybrid solar cells were enhanced based on formic acid treatment. The treatment was carried out by dropping formic acid onto the annealed 5 wt%−DMSO−added PEDOT:PSS film at 140 ºC for 5 min. The higher concentration of the formic acid, the higher conductivity of the PEDOT:PSS film as well as higher PCE of the hybrid solar cell were observed. The optimal device was obtained after 98 wt% formic acid treatment, PCE of 9.31%, V_{oc} of 0.526 V and FF of 60.81%. Formic acid treatment was effective to suppress the carrier recombination loss and reduce the series resistance loss in the hybrid solar cells. Furthermore, the formic acid treated PEDOT:PSS film retained its high transmittance so that J_{sc} of the hybrid solar cell was nearly unimpaired after the treatment. The results implied that the high conductivity and transparent formic acid treated PEDOT:PSS film was significant to achieve high efficiency SiNWs/ PEDOT:PSS hybrid devices. This study also demonstrated high efficient SiNWs/PEDOT:PSS hybrid solar cells by low cost solution processing and low temperature fabrication (<140 ºC).

CHAPTER 6 FLEXIBLE THIN FILM SILICON/PEDOT:PSS HYBRID SOLAR CELLS

6.1. Introduction

Monocrystalline silicon is a popular material for solar cells. However, the brittle property of silicon wafers make them difficult to curvature. In recent years, it is noted that the development of solar cells moves toward thinner wafer thickness and flexible products. Thus, it is attractive to develop flexible crystalline silicon solar cells for boarder use such as curved surfaces or streamline bodies. Methods for fabricating crystalline silicon thin film possessed the bending flexibility have been reported [118,119]. Among them, potassium hydroxide etching of silicon wafer can fabricate ultrathin crystalline silicon film that can be cut with scissors like a piece of paper and direct handled without a supporting substrate [118]. Based on this flexible silicon fabrication method, Lin et al. demonstrated 12% efficiency of nanohole and micro-desert silicon/PEDOT:PSS solar cells, with the flexible silicon thickness of 60 μm. In the same year, Ayon et al also reported ultrathin flexible silicon/PEDOT:PSS solar cells with silicon thickness from 5.7 to 8.6 μm. They obtained PCE of 6.33% by a 8.6 μm thick silicon that surface textured with silicon nanowires. However, they hadn't carried out the bending test so the bending flexibility of the flexible silicon based solar cells under bending is uncertain. In this

chapter, we employed an bending cycle test apparatus to study the bending ability of the flexible silicon/PEDOT:PSS hybrid solar cells. We also calculated the stress in the flexible silicon/PEDOT:PSS hybrid solar cell under uniaxial compressive loads by using the bending equation and COMSOL simulation. Bending flexibility was studied in this work because the flexible solar cell can be a kind of portable device, such as a flexible solar charger for mobile phones. It might be roll up and store inside a container when traveling and pull out when charging mobile devices. Thus, it is significant to understand the bending flexibility of the flexible thin film hybrid solar cells.

6.2. Experimental procedures

6.2.1. Fabrication of thin silicon film

The n-type silicon (100) wafers with resistivity of 1−10 Ωcm and thickness of 525 μm were cleaved into square with size of 10 mm width and 10 mm length. They were cleaned in soapy water, de-ionized water, acetone and isopropanol sequentially with an ultrasound cleaner. To obtain the thin silicon film, they were then immersed in potassium hydroxide solution (20%) at 60 ºC for around 10 hours. Afterwards, silicon nanowires were fabricated on the thin silicon film by metal-assisted electroless etching. Before the etching process, a series of cleaning steps were carried out. First, the thin silicon films were UV-ozone treated for 15 minutes to remove organic residues on the silicon surface. Then, they were underwent standard silicon cleaning process in 1:1:5 parts of ammonia water: hydrogen peroxide: de-ionized water for 30 minutes at 80 ºC and also in 1:1:5 parts of hydrochloric acid:

hydrogen peroxide: de-ionized water for 30 minutes at 80 ºC. These cleaning processes could clean up the potassium hydroxide residue on the surface of the thin silicon film.

6.2.2. Fabrication of silicon nanowires array

The thin silicon films were dipped in the hydrofluoric acid (HF) solution to remove the surface native oxide for the subsequent electroless etching process. Silicon nanowires were formed on the thin silicon film surface by electroless etching in the 0.023M silver nitrate ($AgNO_3$) and 5.6M HF solution for 5 minutes. Finally, the silver nanoparticles were removed by nitric acid.

6.2.3. Preparation of silver network electrode

Silver network electrode was fabricated on the flexible polyethylene terephthalate (PET) substrate. This fabrication method was introduced by Han et al [120]. In our anode fabrication, the PET substrates were cleaned in acetone with an ultrasound cleaner. Then, the acrylic emulsion polymer gel solution was spin-coated onto the PET substrate at 800 rpm for 30 s. It was dried in air at room temperature until cracks network of the polymer gel film was observed under an optical microscope. 100 nm silver was thermal evaporated on the polymer coated PET substrate in the vacuum chamber. Finally, a simple polymer lift-off process was carried out by immersing the silver coated PET into chloroform, followed by rinsing with ethanol and blown dry under nitrogen gas. The silver network coated flexible

PET substrate was cut into a rectangular size of 40 mm long and 15 mm wide for the subsequent device fabrication.

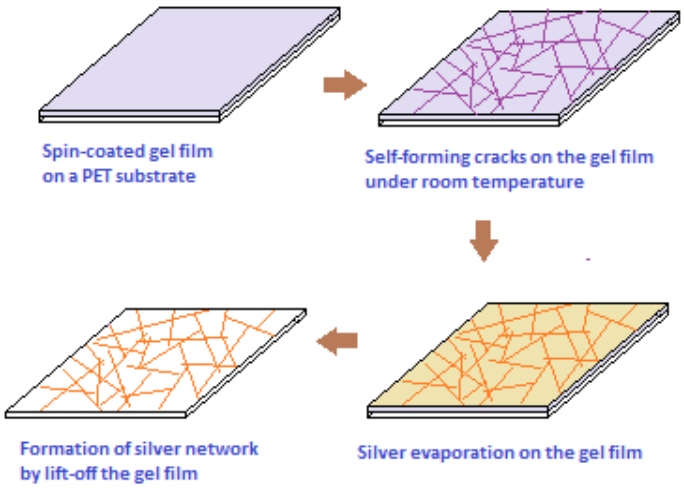


Figure 6.1 A schematic diagram showing the fabrication procedures of the silver network. [Modified from 120]

6.2.4. Preparation of the silver network/PEDOT:PSS electrodes

Conductive grade PEDOT:PSS solution (Clevios PH1000 mixed with 5% ethylene glycol) was filtered through a 0.45 μm syringe membrane and then spin-coated at 3000 rpm for 60 s on the silver network. The film was then annealed on a hot plate in the air atmosphere at 130 °C for 5 minutes. Afterwards, the film was dipped into ethylene glycol for 30 minutes, and annealed at 130 °C for 5 minutes.

6.2.5. Devices fabrication

In hybrid solar cells fabrication process, ethylene glycol was first mixed with the PEDOT:PSS (Clevios P) solution in a ratio of 3:1. The PEDOT:PSS solution was spin-coated on the silver network (and PH1000) coated flexible PET substrates at 750

rpm for 10 s. Then the thin film silicon was put on the spin-coated solution layer at the center of the substrate. The thin film silicon would be stuck on the PET substrate via the PEDOT:PSS film. The devices were annealed at 110 ºC for 15 minutes. Finally, GaIn eutectic alloy was deposited on the backside of the silicon film as cathode. The silver network (and PH1000) coated flexible PET substrate was an anode in the hybrid solar cell. The schematic diagram and optical image of the thin film silicon/PEDOT:PSS solar cell is given in Figure 6.2(a) and (b) respectively.

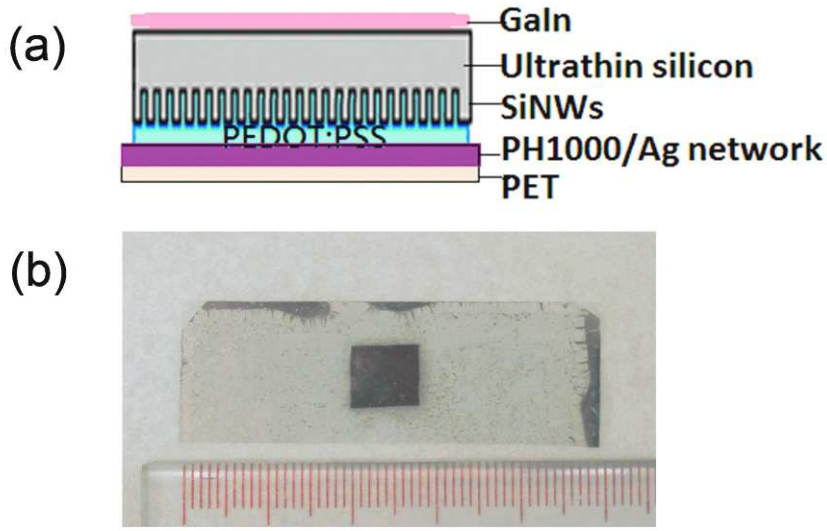


Figure 6.2(a) Schematic diagram and (b) the band diagram of the architecture of the flexible thin film silicon/PEDOT:PSS hybrid solar cell.

6.3. Results and discussion

6.3.1. Characterization of the thin film silicon

The as-received 525 μm thick crystalline silicon wafers were rigid and bulky. The thin silicon films were made by a wet etching process in potassium hydroxide solution. The thickness of our KOH-etched silicon thin films in the experiment were around 15 μm, by referring to Figure 6.3(a). The ultrathin silicon could be bendable into a curve shape as shown in Figure 6.3(b). In order to improve the light absorption of the thin film silicon, we fabricated a silicon nanowires array on the thin silicon film by metal-assisted electroless etching. The optical image of the thin silicon film after the electroless etching is shown in Figure 6.3 (d). The length of the silicon nanowires on the silicon thin film was around 450 nm (Figure 6.3 (e)).

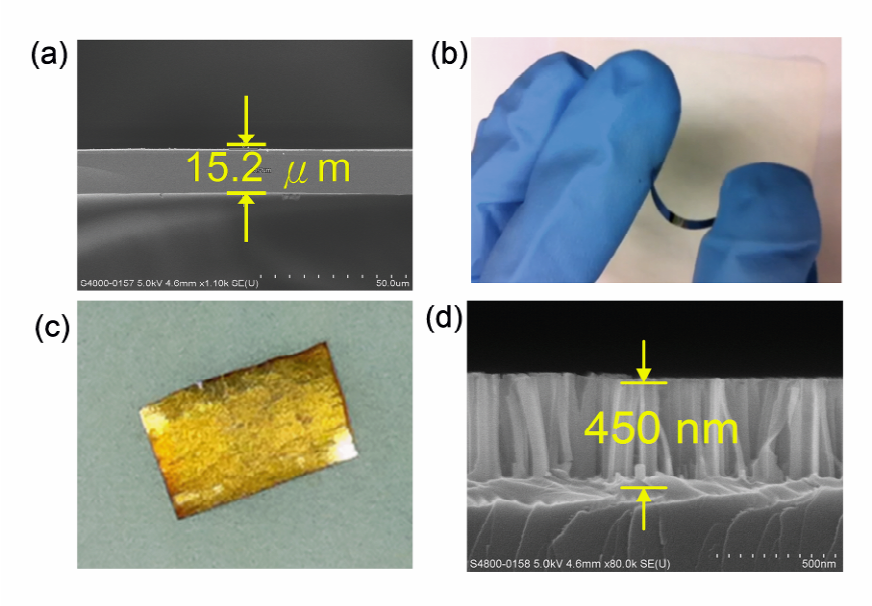


Figure 6.3(a) Cross-sectional SEM images showing the thickness of the thin silicon film is around 15μm. (b) The thin silicon sheet allow certain bending flexibility. Silicon nanowires on the silicon wafer substrate and (c) shows the optical image and (d) shows the length of SiNWs on the thin silicon film of around 450nm.

To ensure the single crystallinity in the silicon thin film was not affected after the wet etching process in potassium hydroxide solution, TEM characterization was carried out. TEM images in Figure 6. 4 revealed that the wet-etched silicon nanowires were single crystalline structure which ensured good carrier mobility in the device. A thin native oxide layer of around 2 nm was found on the surface of the nanowire, this thin oxide layer served as a perseveration layer and prevent the leakage current.

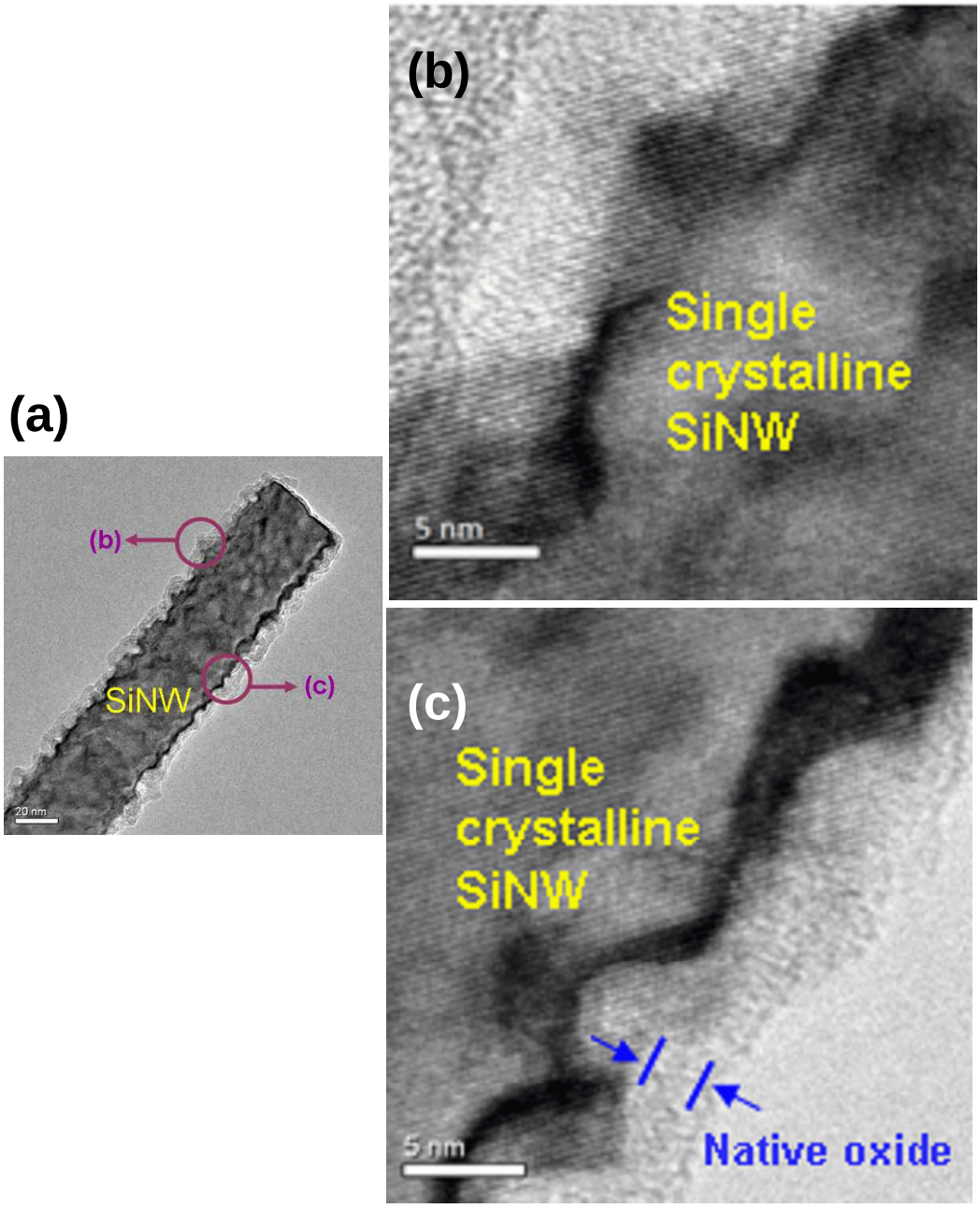


Figure 6. 4 TEM images reveal the crystallinity of SiNWs.

6.3.2 Characterization of the silver network

The silver network anode of the solar cells was characterized. The SEM images of the silver network morphology were given in Figure 6. 5, the width of the silver line was around 5-30 μm. The silver network area coverage on the transparent PET substrate was around 15%. The transmittance curve in Figure 6.6(a) shows that its transparency was 82% at wavelength 550 nm. Figure 6.6(b) is the optical image of the silver network on PET. The sheet resistance of the silver network anodes was 12 Ω/sq by four-point probes measurement.

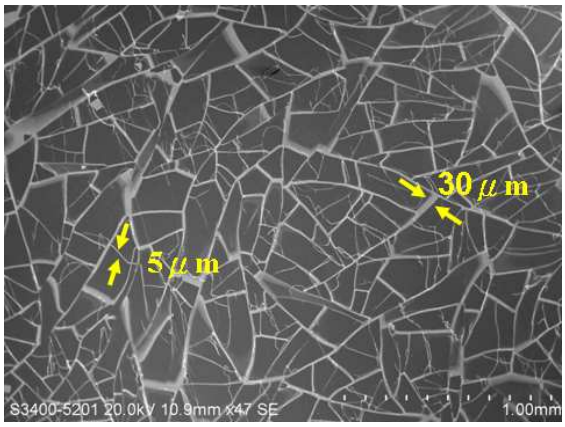
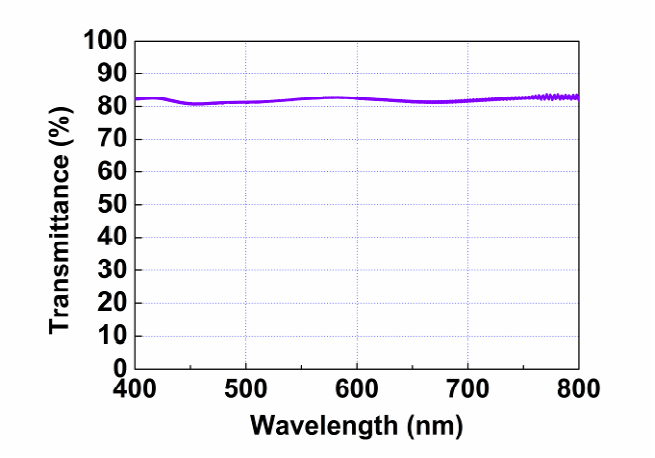


Figure 6. 5 Top view SEM images of the silver network structures.

(a)



(b)

Figure 6.6 (a) Transmittance result and (b) optical image of the silver network on a PET substrate, the green lines at the two corners help the visual observation of the silver network on PET.

Figure 6. 7 recorded the J−V characteristics of the flexible devices. The flexible solar cells achieved a power conversion efficiency (PCE) of 5.56% with open circuit voltage (V_{oc}) and short circuit photocurrent (J_{sc}) of 0.51 V and 16.96 mA/cm^2 respectively. The fill factor (FF) of the solar cell was around 64.4%.

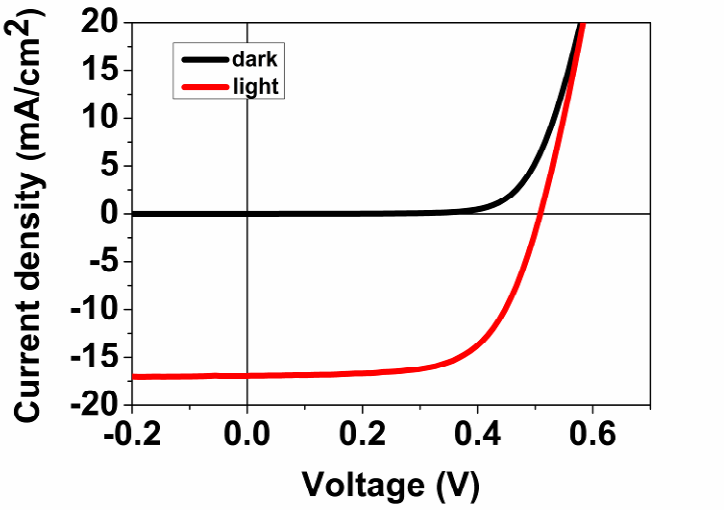


Figure 6. 7 J-V characteristics of the flexible thin film silicon /PEDOT:PSS hybrid solar cells.

6.3.3 Calculation of the strain/stress in the silicon thin film

The bending stress of the flexible solar cell was calculated in this section. A schematic cross sectional diagram for the bending of the flexible solar cell was given in Figure 6. 8. We measured the maximum deflection ω_0 and bending radius R under various substrate's final end-to-end length (i.e. l_3 =38, 35, 32 and 30 mm).

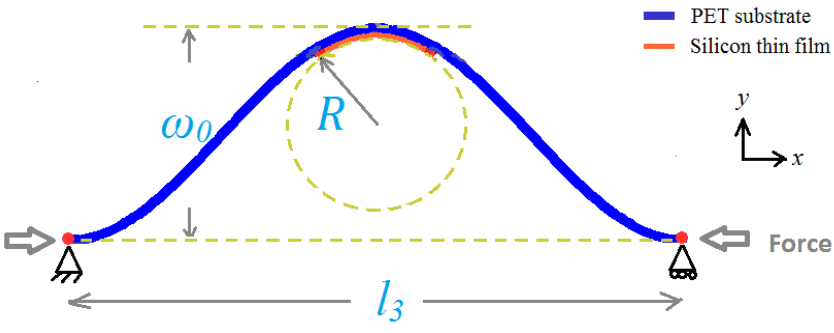


Figure 6. 8 Schematic cross-sectional diagram for the bending of the flexible solar cell.

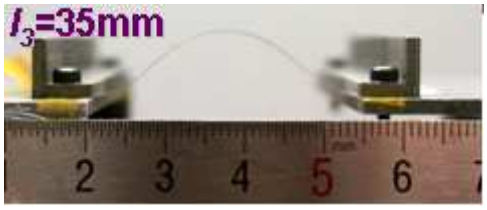
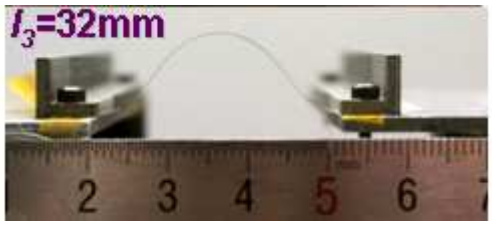
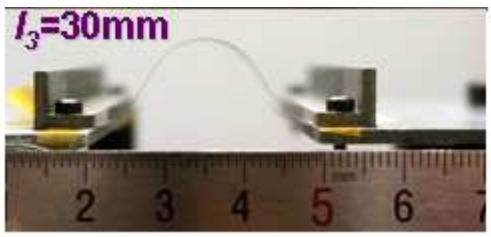
Substrate's final end-to-end length (mm)	**Optical images of the cross sectional mode shape of the flexible solar cell**	**ω_0 (mm)**	***R* (mm)**
38		6.0	21.0
35		8.5	13.0
32		10.5	9.0
30		11.8	7.0

Table 1 Experimental maximum deflections and the bending radii.

In the buckling of the flexible solar cell, the maximum compressive strain (ε_{bot}) and stress (σ_{bot}) was at the bottom surface of the thin film silicon layer, which are given as follows [121]:

$$\varepsilon_{bot} = -\frac{D_s^2 E_s + D_t^2 E_t + D_p^2 E_p + 2D_s D_t E_t + 2D_t D_p E_p + 2D_p D_s E_p}{2R\left(D_s E_s + D_t E_t + D_p E_p\right)} \quad \text{Eq 6. 1}$$

$$\sigma_{bot} = E_s \varepsilon_{bot} \quad \text{Eq 6. 2}$$

where R is the bending radius of curvature obtained from Table 1. E_p, E_t, E_s and v_p , v_t, v_s are the effective Young's modulus and Poisson's ratio of PET substrate, PEDOT:PSS adhesive film and the silicon film respectively. (i.e. E_p = 4 GPa, E_t = 1 GPa, E_s = 150 GPa; v_p = 0.44, v_t = 0.33, v_s = 0.27). D_p , D_t and D_s are the thickness accordingly. (D_p = 50 μm, D_t = 0.1 μm, D_s = 15 μm). A schematic diagram of the three layers in the flexible solar cell under buckling is given in Figure 6. 9. The dimension and the mechanical properties of PET substrate, PEDOT:PSS and silicon thin film [122, 123] are summarized in Table 6. 1.

Material	Width (mm)	Thickness (μm)	Length (mm)	Young's Modulus (GPa)	Poisson's ratio
PET	15	50	40	4	0.44
PEDOT:PSS	6.5	0.1	9	1	0.33
Silicon	6.5	15	9	150	0.27

Table 6. 1 Materials' dimensions and mechanical properties used in the calculation.

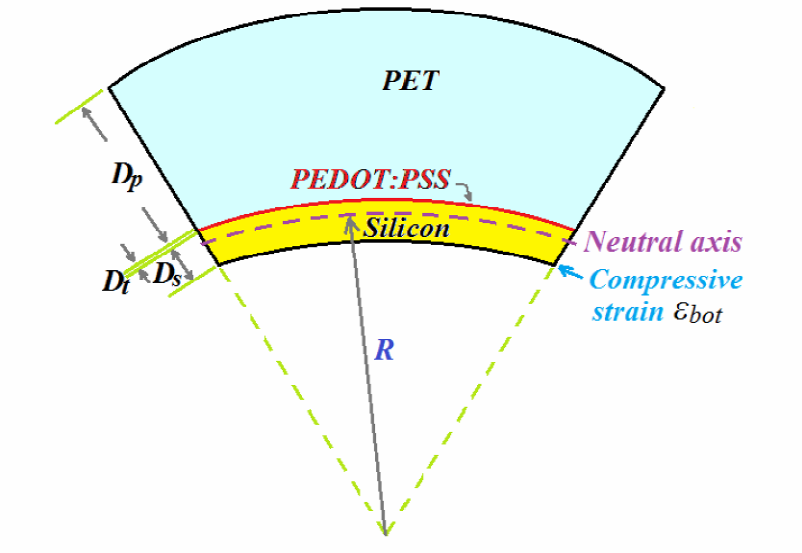


Figure 6. 9 Diagram of the three layers under bending.

The parameter values for Eq 6. 1 and Eq 6. 2 are given in Table 6. 1. The results of the compressive strain (ε_{bot}) and stress (σ_{bot}) at the bottom surface of silicon under various substrate's final end-to-end length were plotted in Figure 6. 10.

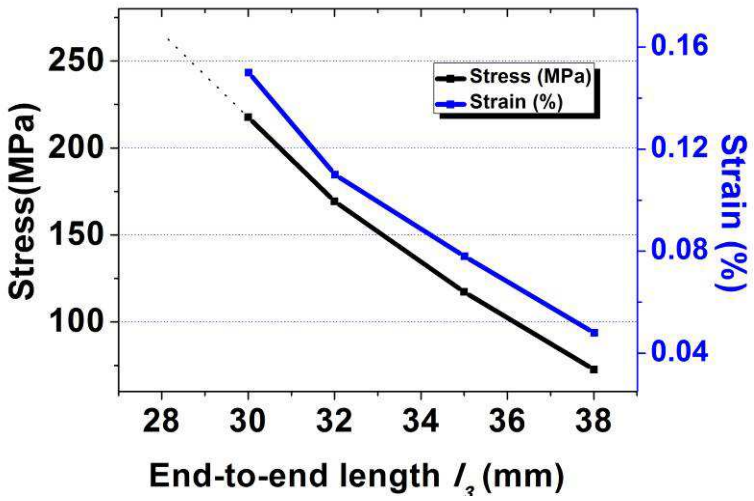
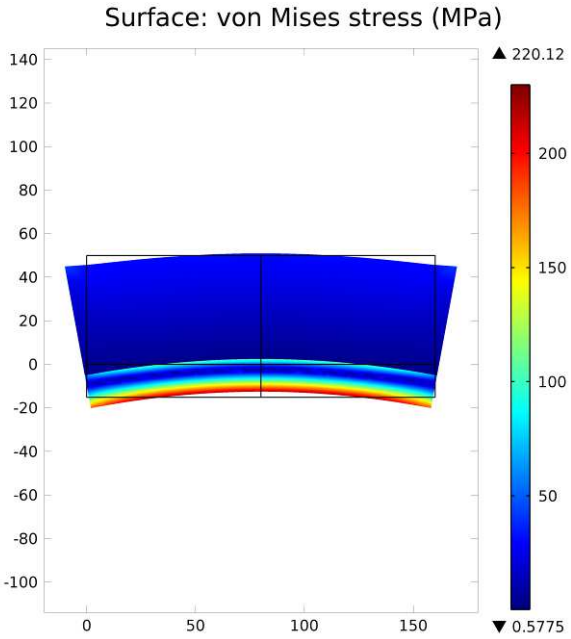


Figure 6. 10 Relationship of strain or strain against the substrate's final end-to-end length. The dotted line is the extrapolation line for the determination of the shortest end-to-end length according to the failure stress of silicon of around 254 MPa.

6.3.4 Finite element simulation of the effect of nanowires on the bending stress

The buckling equations of Eq 6. 1 and Eq 6. 2 assumed the thin film silicon surface being planar. In our flexible solar cell, a thin layer of silicon nanowires was fabricated on the upper silicon surface to improve the light absorption. Thus, it was study to know the effect of the silicon nanowires layer on the maximum stress in the thin silicon film. When nanowires were included in silicon, the stress distribution of the flexible hybrid solar cell under a bending moment was simulated using COMSOL Multiphysics 4.2a. A comparison was being made between the two structures: planar thin film silicon and 500 nm thick silicon nanowires grown on the top surface of the 15 μm thin film silicon. Simulation results in Figure 6. 11 and Figure 6.12 show the stress distribution in the device with planar thin film silicon and 500 nm thick silicon nanowires structure respectively. From Figure 6.12(a), the maximum stress was at the bottom surface of silicon of around 217 MPa and the stress at the foot of the nanowires was around 88 MPa, as shown in Figure 6.12(b). For planar thin film silicon structure, simulation results in Figure 6. 11(a) showing the maximum stress at the bottom surface of silicon was 219 MPa for planar silicon structure. Hence, the effect of the 500 nm nanowires on the change in the maximum stress of the planar structure was less than 1%.

(a)



(b)

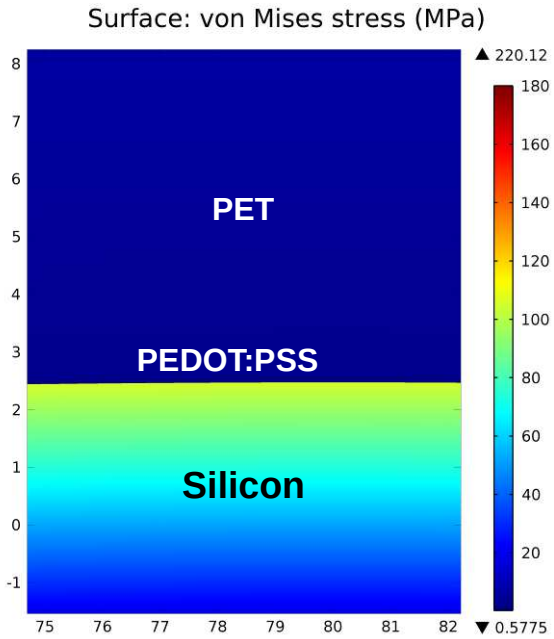
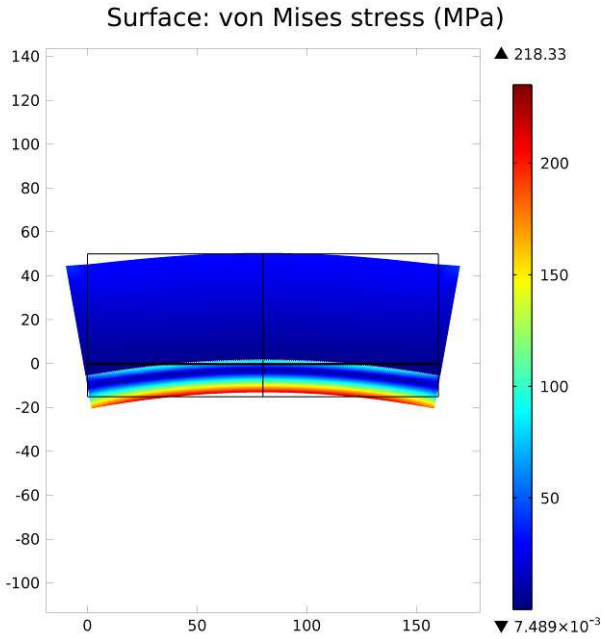


Figure 6. 11 Cross sectional simulation showing (a) the stress distribution of a planar structure and (b) stress distribution of the planar top surface of the silicon thin film.

(a)



(b)

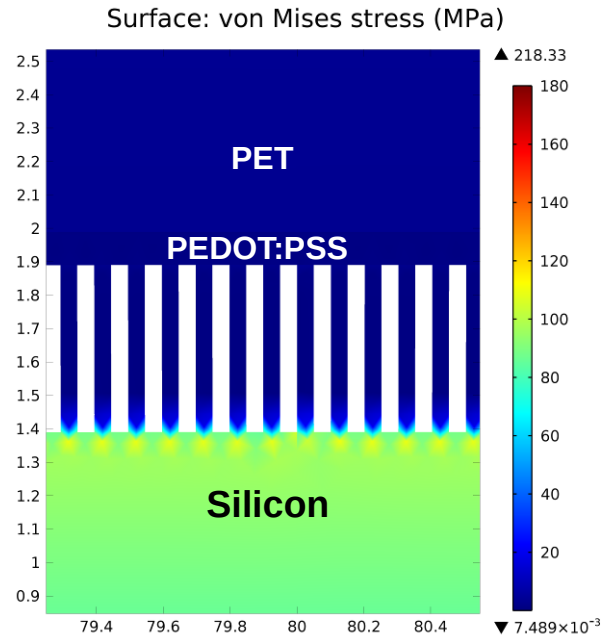


Figure 6.12 Cross sectional simulation showing (a) the stress distribution of a nanowire structure and (b) stress distribution of the silicon nanowires at the top surface of the silicon thin film.

L-dL = 30mm	**Planar**	**Nanowires**
Stress at the center of the bottom surface of silicon	219 MPa	217 MPa

Table 6. 2 Comparison of the bending stress in a planar and a nanowires structure.

6.3.5 Failure stress of silicon material

In order to avoid failure in the thin film silicon layer, it was necessary to design the working stress for 99% reliability of the silicon material in our flexible solar cells. Applying Weibull equation, $A_v(\sigma) = e^{-\left(\frac{\sigma}{\sigma_0}\right)^m}$ where $A_v(\sigma)$ is the reliability of material, σ is the working stress, σ_0 is the characteristic fracture stress and m is the Weibull modulus. For square monocrystalline (100) silicon wafers, σ_0 = 372 MPa and m = 12 [124]. Thus, the working stress σ to obtain 99% reliability of our silicon thin film, i.e. $A_v(\sigma) = 0.99$, was around 254 MPa. Referring to Figure 6. 10, l_3 = 29 mm was the threshold end-to-end length to fulfill the 99% reliability of silicon, having the maximum compressive stress (σ_{bot}) of 249 MPa. However, this value was a bit close to 254 MPa. In order to eliminate the uncertainty in the loading on the flexible solar cell, we chose l_3 = 30 mm in the bending cycle test where the compressive strain (ε_{bot}) and stress (σ_{bot}) at the bottom surface of silicon were 0.15% and 217 MPa respectively. This stress value was lower than 254 MPa and hence the

reliability of the silicon thin film should achieve 99% when the end-to-end length of the substrate, l_3 , was longer than 30 mm.

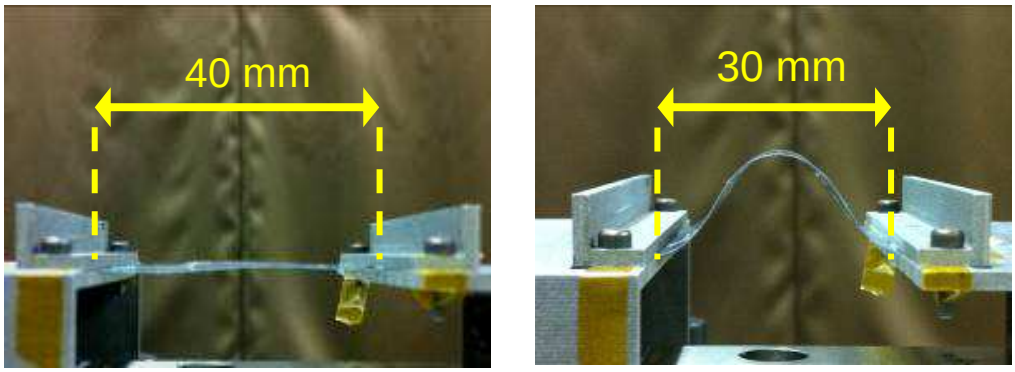


Figure 6. 13 Reliability of the flexible 15μm silicon thin film is assured when the end-to-end length of the substrate is longer than 30mm

6.3.6 Bending test

The architecture of the flexible solar cells in our work was PET/hybrid Ag network/PEDOT:PSS/Si/GaIn. The PET substrate was 40 mm long, 15 mm wide and 50 μm thick. The 10 mm × 8 mm area silicon thin film with around 15 μm thickness was stuck at the center of the substrate by PEDOT:PSS. The PET substrate was clamped on two edges and exerted a compressive force axially. The bending setup is shown in Figure 6. 14.

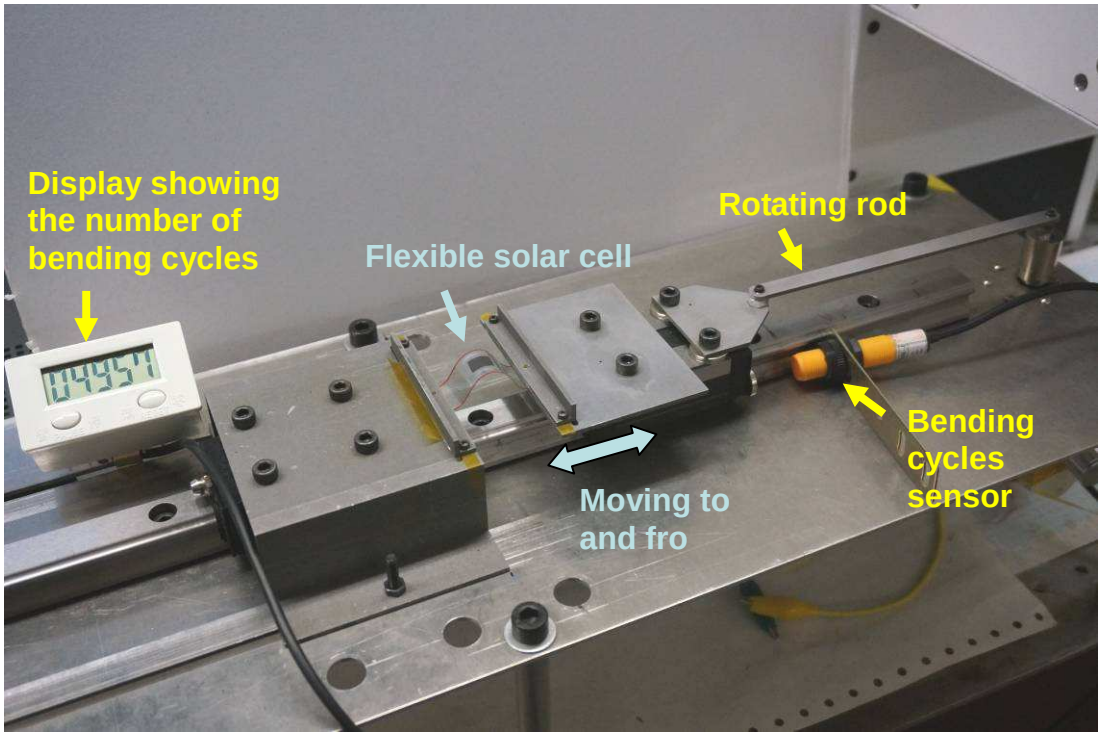


Figure 6. 14 The flexible solar cell is carrying a bending cycle test.

The results showed that the devices were flexible and bendable. When the axial compressive force was removed so that the end-to-end length of the flexible substrate returned to its original flat condition, the power conversion efficiency returned to almost its original efficiency. The maximum stress of the flexible hybrid solar cell under a bending radius of 7 mm was at the bottom surface of silicon of around 217 MPa. Bending cycle test showed a good recovery of the original efficiency after 5000 cycles under a bending radius of 7 mm. The results were recorded in Figure 6.16.

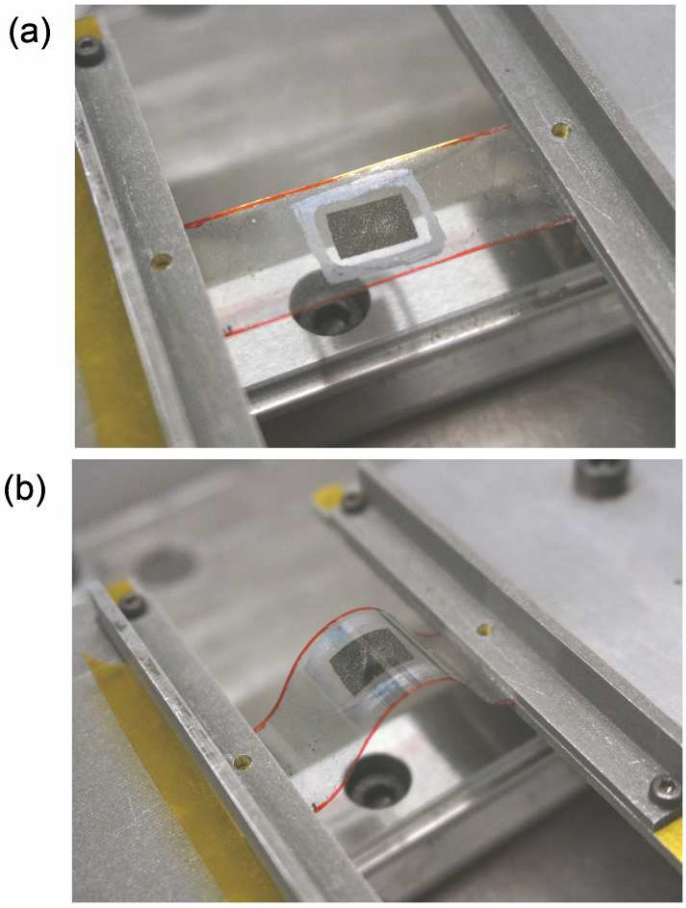


Figure 6.15(a) The flexible device is clamped and rested at the original flat position (b) the device is bent into a curvature of radius of 7mm.

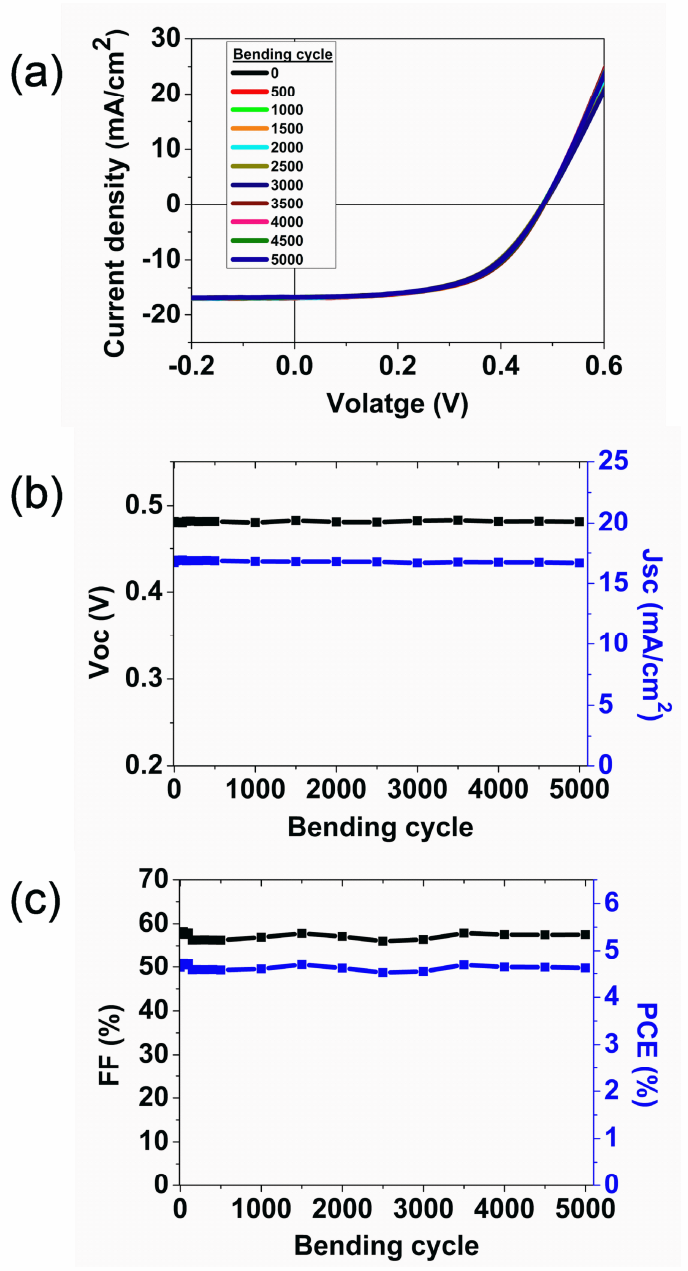


Figure 6.16 (a-c) Bending cycle test result shows the photovoltaic performance of the flexible solar cells after 5000 bending cycles is as good as the initial performance.

6.4 Conclusions

We studied flexible hybrid solar cells with a thin crystalline film silicon/ (poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) (PEDOT:PSS) Schottky junction. The crystalline silicon wafers were etched by potassium hydroxide solution until a thickness around 15 μm and became flexible. A silver network structure was used for the anode with high electrical conductivity (12 Ω/sq) and good light transmittance (82%). The flexible hybrid solar cell yielded a power conversion efficiency of 5.56%. In the bending cycle test, the flexible hybrid cell showed a good recovery of the original efficiency after 5000 cycles under a bending radius of 7 mm that the estimate maximum bending stress of silicon was around 217 MPa. The ability of bending repeatedly without varying much in the power conversion efficiency of the solar cells held a significant importance for the development in the lightweight and flexible applications.

CHAPTER 7 HUMIDITY EFFECT OF THE SILICON/PEDOT:PSS DEVICES

7.1. Introduction

Over the past decade, a large amount of work have been done for achieving high power conversion efficiency in silicon/PEDOT:PSS solar cells. Other than power conversion efficiency, stability is also a critical factor for the practical application of the solar cells. Hence, device lifetime and degradation mechanism would shift more concerns. Organic materials are not as stable as the inorganic silicon. They can easily degrade in humid conditions. Only the understanding of these degradation mechanisms can ensure the stability and service lifetime of the solar cells.

In this chapter, the devices were stored under different relative humidity in a environmental chamber at a constant temperature. The degradation effects on the ITO, PEDOT:PSS and silicon nanostructure were studied individually.

7.2. Experimental procedures

The silicon/PEDOT:PSS devices were fabricated according to the procedures stated in section 4.2.2. The silicon surface was textured to obtain a array of nanowire with length around 340 nm. The effect of moisture on the degradation of SiNW/

PEDOT:PSS hybrid solar cell was investigated with a controlled humidity chamber (Espec Corp). The description on the chamber could be referring to section 3.4.2. In the degradation test, the devices were unencapsulated and stored under different relative humidity (RH) varied from 15% to 100%, accumulatively at 25 ºC for 3 hours. In each batch, ten hybrid solar cells were fabricated for the humidity test.

7.3. Results and discussions

7.3.1. Efficiency degradation of devices due to moisture

The averaged PCE of the devices under different RH condition are given in Figure 7.1 (a). The degradation rates was the fastest when the devices were stored in 15%RH environment. The average PCE of the initial efficiency of the devices was around 6 − 6.5%, the PCE dropped to 5.49, 3.12 and 1.27% for those devices kept at 15, 60 and 100% RH respectively (Figure 7.1 (a)).

To look more detail into the consequence of humidity, the PCE of the ten devices under different RH were plotted in the histograms. The PCE count of fresh devices at t = 0 were shown in Figure 7.1(b,d,f) while the PCE count of the degraded devices at t=3h were shown in Figure 7.1(c,e,g). From the histogram showing the performance of each individual device, there was a clear trend that the devices degrade faster in a higher relative humidity. However, their rate of degradation was not the same although they were stored in the same humidity condition. The reason could be due to the thickness unevenness of the PEDOT:PSS layer in between the silicon nanowires and the ITO glass that caused the inhomogeniety of the device

degradation rate. Therefore some irregular interference fringes could be observed as shown in Figure 7.2.

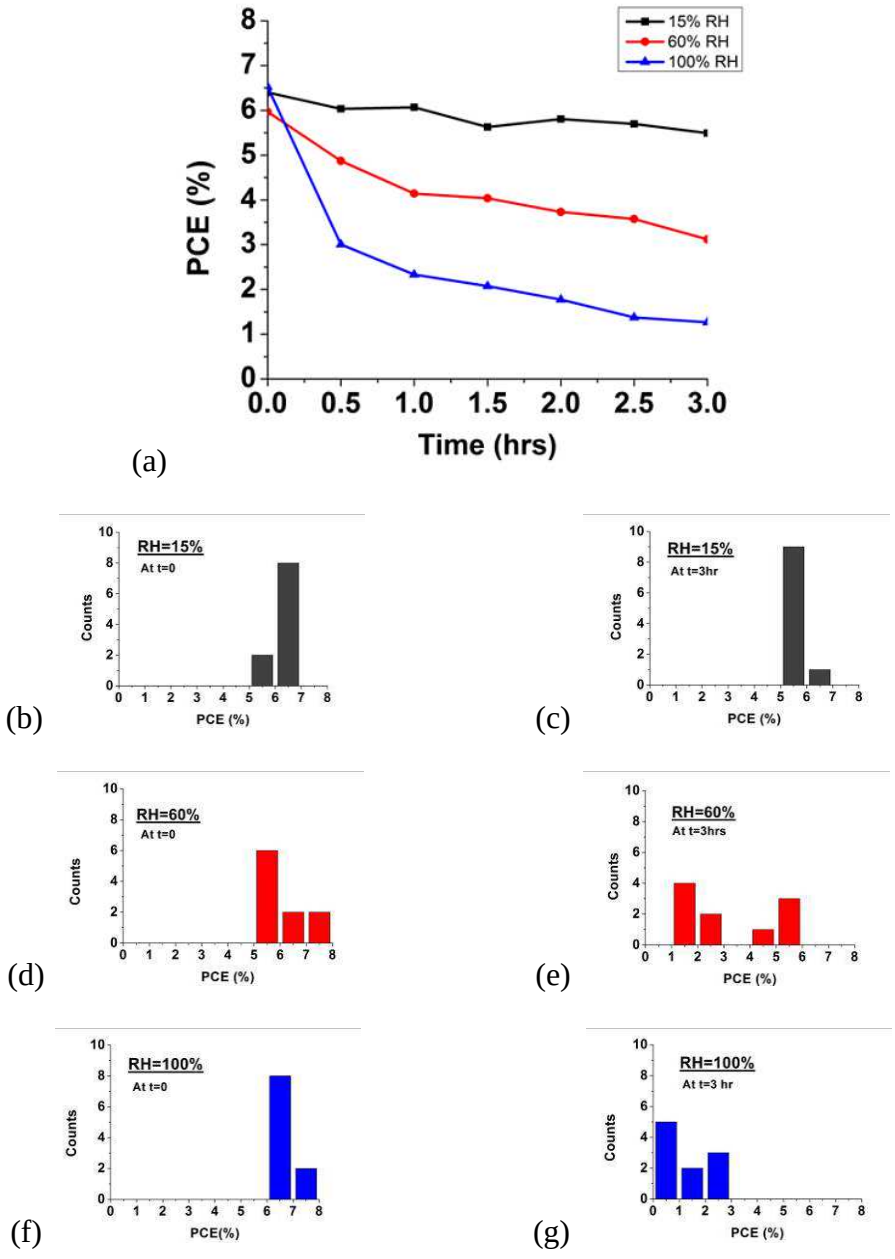


Figure 7.1 (a) Summary graph of PCE degradation of devices at different humidity; (b,d,f) are the histogram showing the PCE of the as-fabricated devices; (c,e,g) are the histogram showing the PCE of the degraded devices.

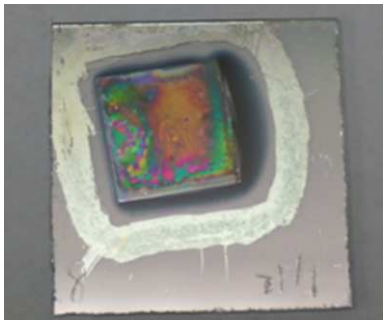


Figure 7.2 Interference fringes are observed at the PEDOT:PSS layer of the SiNW/PEDOT:PSS hybrid solar cell.

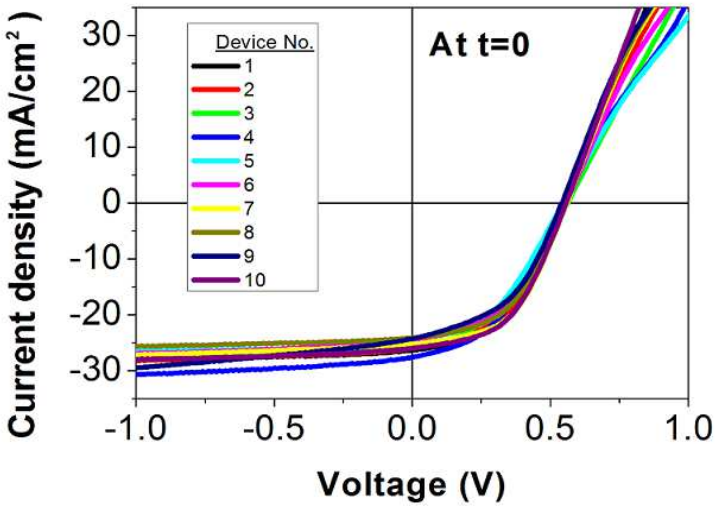
The degradation was most severe for the 10 devices kept in 100% relative humidity, and thus their J−V characteristic curves were shown in Figure 7.3 for further study. In the as-fabricated devices, the V_{oc} of the devices were around 0.54−0.56 V and they were quite consistent (Figure 7.3(a)). The J_{sc} varied from around 24−28 mA/cm^2. This variation may due to the uneven of PEDOT:PSS thickness between the ITO and SiNW among the devices as discussed before. After 3 hours storage in 100%RH, open circuit voltage, short circuit current and fill factor in the J−V curves of these 10 devices had obviously degraded as shown in Figure 7.3(b).

Increase in the PEDOT:PSS resistance [71] may be one of the degradation causes of the solar devices. However, the PEDOT:PSS layer was sandwiched between the ITO and silicon nanowires so that a non-destructive in-situ study of the PEDOT:PSS layer inside the device was difficult. Thus, the PEDOT:PSS samples were prepared by spin-coating 1:1 PEDOT:PSS:EG mixture onto glass substrates at 3000 rpm for 60 s and then dry films were obtained after an annealing process at 110 ºC for 15 minutes. Prior and after storing these PEDOT:PSS layers in a humid environment, their sheet resistances were recorded by four point probes

measurement (Lucas Labs 302). The sheet resistance of the as-fabricate film was 7 kΩ/sq. After storing the film in a >98%RH environment for 60 min, the sheet resistance reading of the film fluctuated during the four point probe measurement and the relatively stable sheet resistance reading was 7.8 kΩ/sq. However, after a 10 seconds nitrogen gas blow on the PEDOT:PSS film, its sheet resistance returned to a stable reading of 7 kΩ/sq. The results reflected that probably some trapped moisture in the film led to the increase sheet resistance of PEDOT:PSS in the humidity environment. If the humidity exposure duration was short, the resistance might be reversible by using a nitrogen gas blow to dry the film. Nevertheless, different from this uncovered film used in the sheet resistance measurement, the solar cell architecture was that the PEDOT:PSS film was sandwiched between a silicon wafer and a ITO glass so that the trapped moisture cannot easily blow dry by nitrogen gas. Under high humidity, EG doped PEDOT:PSS layer was unstable.

Next, four point probe measurement was carried out to study ITO conductivity and tunneling electron microscopy (TEM) was used to characterize the growth of the silicon dioxide layer on the silicon nanostructures. These work was carried out for the understanding the cause of the device degradation at the interface [125].

(a)



(b)

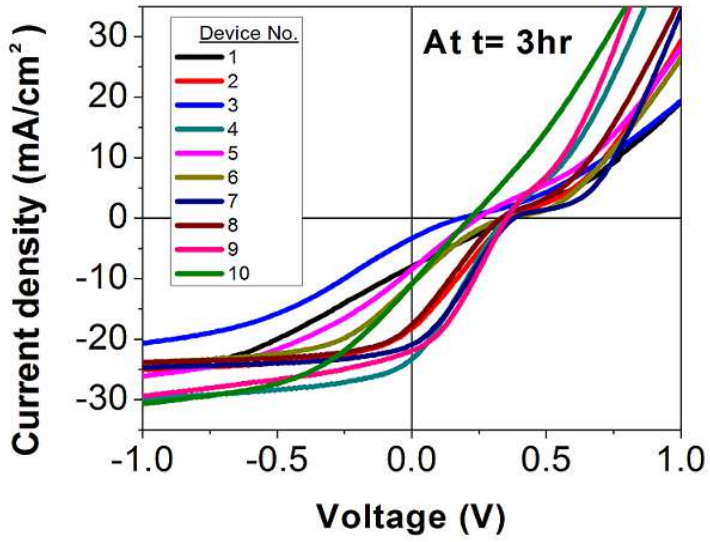


Figure 7.3 Current density-voltage curves showing (a) the fresh devices (b) the degraded devices (after storing in a 100%RH environment for 3 hours)

7.3.2. Sheet resistance of the ITO-glass after devices' degradation

Further investigation of ITO degradation effect was done. Some degraded devices which have been stored in 100%RH for 3 hours were detached and measured for the variation in their sheet resistance. Before the four-probe measurements, the dry PEDOT:PSS residues attached on the ITO-glass were cleaned by cotton pads soaked with isopropanol manually and then ultrasonic cleaning procedures. Table 7.1 shows the averaged sheet resistances of the ITO glass after the degradation experiment. Results showed that the ITO layer was degraded after the storage in the high humidity condition. For the fresh ITO, the averaged sheet resistances was around 5.83 ohm/sq. After the degradation study, the sheet resistance in sample 5 of the ITO glass increased to 6.6 ohm/sq. In addition, an obvious semi-transparent greenish mark was observed on the ITO-glass at the contact area between the ITO and the silicon wafer, as shown in Figure 7.4. Moreover, SEM images on the right hand side of Figure 7.4 shows that the thickness of ITO at the contact area between the ITO and the silicon wafer was thinner than the original ITO thickness, this revealed the etching of the ITO by the PEDOT:PSS film that became acidic after absorbed the water from the high humidity environment. The degraded ITO film became thinner than its original ITO thickness such that the etched ITO might not tightly hold onto the silicon nanowires and led to the device degradation. The etching process may be inhomogeneous, therefore the rate of ITO degradation was not the exactly same. Sample 1 and 3 had similar sheet resistivities with the fresh ITO which was around 5.83 Ω/sq, which suggested little or no ITO degradation in them. Yet,

ITO degradation was observed in sample 2 and 4 and severe ITO degradation occurred in sample 5.

In the fabrication steps, first, the PEDOT:PSS was spin-coated on the ITO glass. Then, the silicon wafer was placed on top of the wet PEDOT:PSS film so that the nanostructured silicon can stick into the ITO via PEDOT:PSS after the annealing process. The rate of the solidification process of PEDOT:PSS could be affected by many factors, for example: solvent evaporation rate of PEDOT:PSS, the surface energy of the nanostructure silicon and the infiltration of PEDOT:PSS into the nanostructure. All of the above factors would lead to the uneven thickness of PEDOT:PSS film between ITO and silicon wafer. Hence, the diffusion path of moisture into the PEDOT:PSS film as well as the etching of ITO would be varied among different devices. The varied degradation rate of ITO of the devices resulted in different sheet resistances in the pieces of degraded ITO glass as shown in Table 7.1.

Sample No.	**Fresh ITO (Ω/sq)**	**ITO from degraded devices (At t=3hr)(Ω/sq)**
1	5.80	5.82
2	5.83	5.96
3	5.82	5.85
4	5.85	5.92
5	5.83	6.60

Table 7.1 Sheet resistance of fresh ITO and degraded devices' ITO

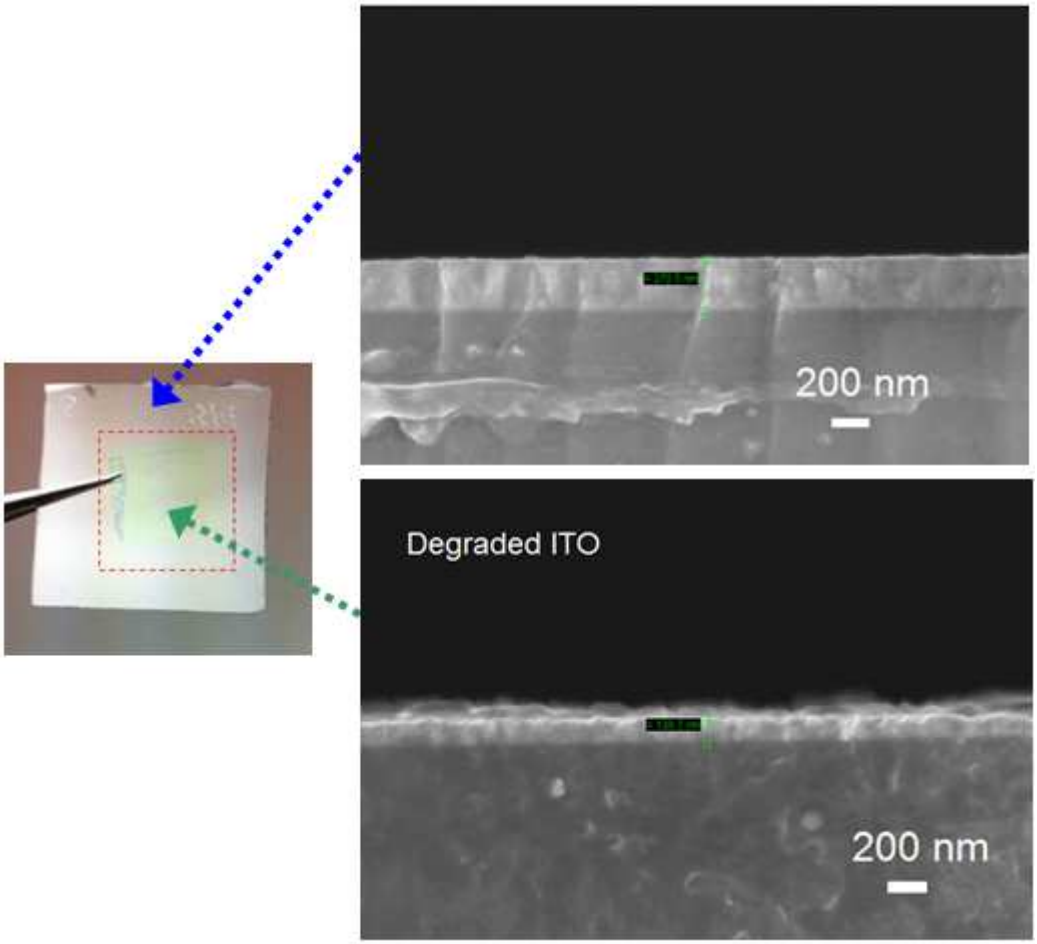
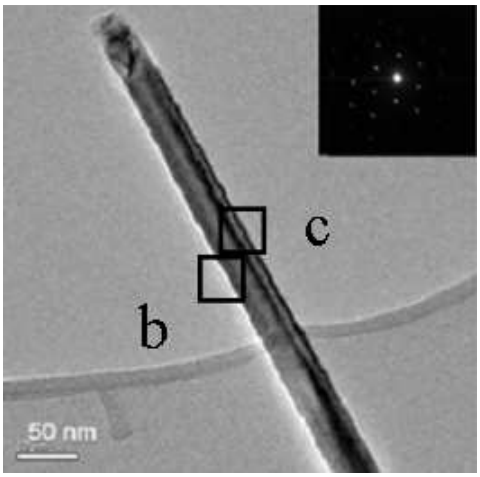


Figure 7.4 The mark (highlighted in the red square) was observed on the ITO detached from the device stored in 100%RH for 3 hours. By comparing the SEM images on the right hand side, it can be observed that the thickness of ITO is reduced at the mark region.

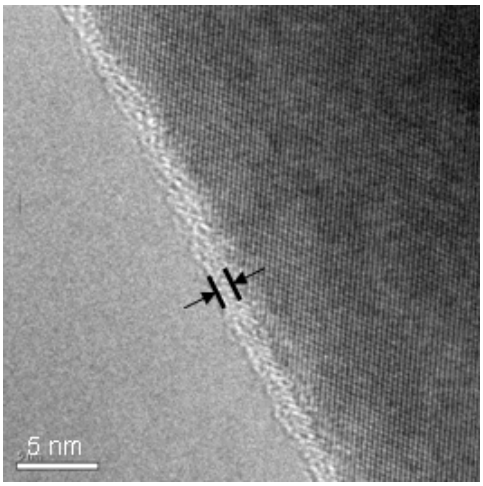
7.3.3. Degradation effect of the silicon nanostructures

We also examined if the change of oxide thickness on the surface of silicon nanostructures was related to device degradation. Tunneling electron microscopy (TEM) was used to study the oxide layer thickness prior (Figure 7.5) and after (Figure 7.6) keeping at the humid environment with 100% RH. The highlighted region on the left and right hand side of the silicon nanostructure were shown in Figure 7.5 (b), (c) and Figure 7.6 (b), (c), respectively. From HRTEM images, there was a thin amorphous native silicon dioxide layer on the sidewall of the highly crystallized silicon nanostructure. (Figure 7.5 (b) and (c)). From Figure 7.6 (b) and (c), there was not show a significant increase in the oxide thickness on the sidewall of the nanostructure after exposed the device to 100% RH for 3 h. The consistent silicon nanostructure before and after device degradation suggested the dominating effects were not contributed by the oxide on silicon nanostructures.

(a)



(b)



(c)

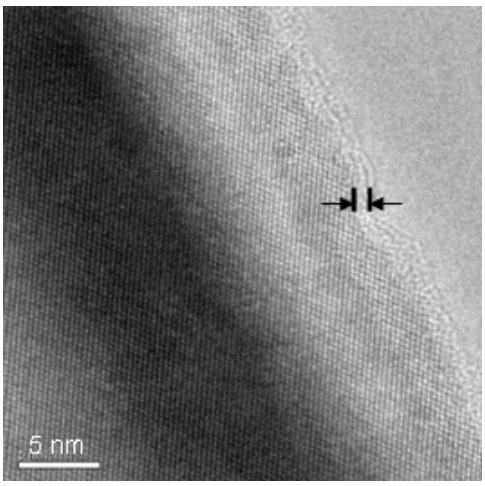
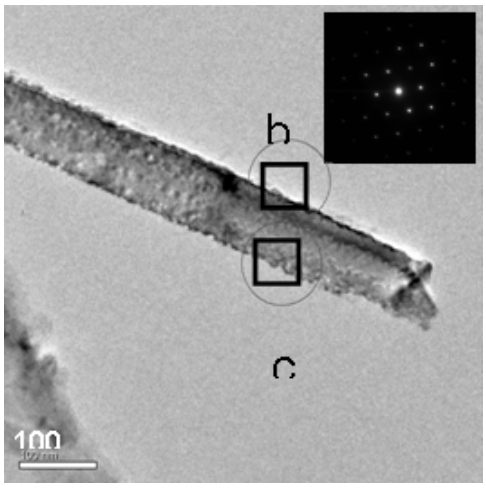
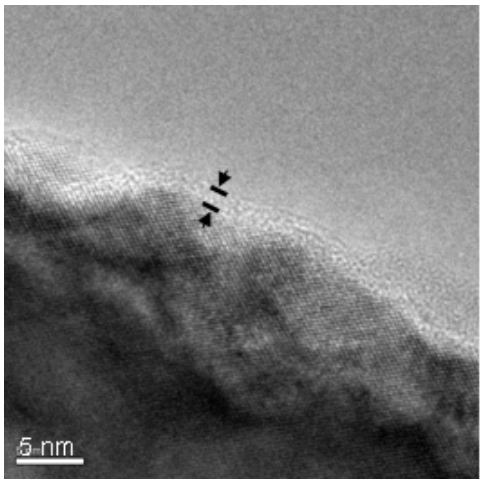


Figure 7.5 TEM images of a silicon nanostructure without storing in 100%RH chamber

(a)



(b)



(c)

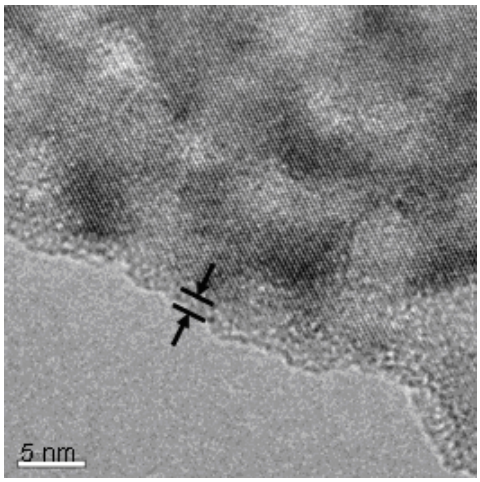


Figure 7.6 TEM images of a silicon nanostructure storing in 100%RH chamber for 3 hours

7.3.4. PCE recovery of the hybrid solar cells

From the previous results in this study, the PEDOT:PSS layer and the ITO glass were considered to involve in the PCE degradation of the current devices. We tried to test if the degraded devices could be recovered with a newly spin-coated PEDOT:PSS layer. To withstand the recovery processes, a more robust silicon nanostructure (Figure 7.7) instead of silicon nanowires was used in the recovery test and it was fabricated by changing the silver nitrate etchant concentration from 0.023 M to 0.16 M. Moreover, we did the annealing in glovebox and skipped the post UV ozone process to minimize the effect of induced oxide layer formed on the nanostructure that may influence the recovery of the devices.

The as-fabricated device had the original PCE value 4.9%, as shown by the black curve in Figure 7.8. After the degradation test, the PCE dropped to 0.01%. After that, we disassembled the device and separated ITO from the silicon wafer. The PEDOT:PSS residues on the surface of ITO and silicon were cleaned up. Then, a fresh layer of PEDOT:PSS was newly spin-coated onto the original ITO and then attached it to the hydrofluoric acid cleaned original silicon substrate. The J−V curve of the re-fabricated device was shown in blue color in Figure 7.8 with PCE of 2.32%. There was just a partial recovery in the PCE of devices.

Another device degradation factor was due to ITO. The reuse of degraded ITO could only get a partial recovery of PCE. With a fresh ITO, fresh PEDOT:PSS and then attached it to the hydrofluoric acid-cleaned original silicon substrate, the PCE

was around 4.5% that was nearly fully recovered the PCE of the original device. The difference in PCE of the original (4.9%) and recovered (4.5%) devices may be due to some damages in the silicon nanostructure or incomplete removal of the dried PEDOT:PSS film during the recovery process.

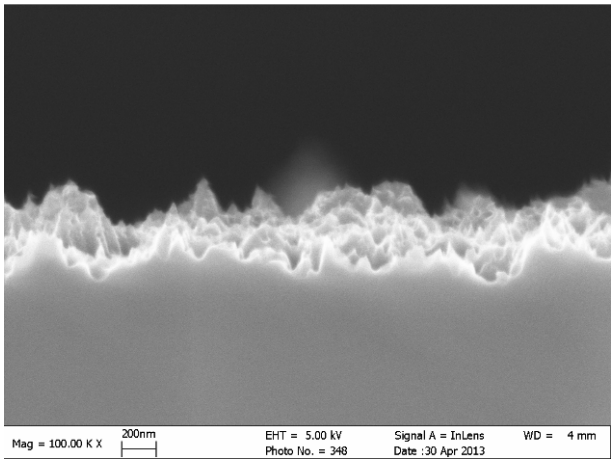


Figure 7.7 The SEM side view of the silicon nanostructures used in the recovery test

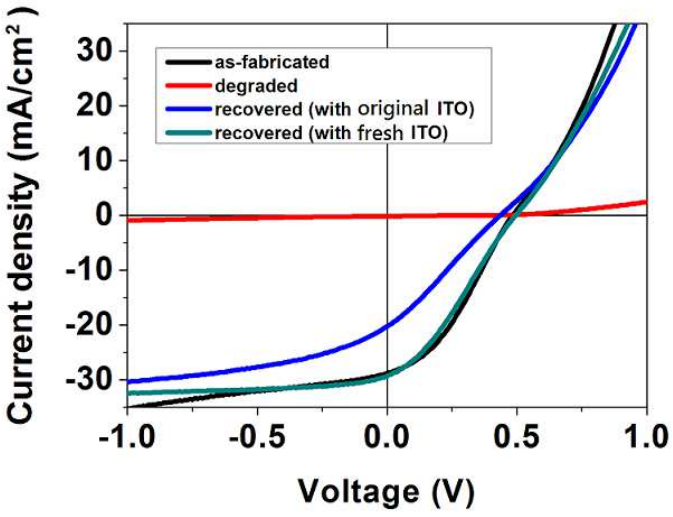


Figure 7.8 J-V characteristics curves of the as-fabricated (black), degraded (red), partially (blue) and almost (green) recovered device

7.4. Conclusions

The effect of humidity on the PCE of hybrid SiNW/PEDOT:PSS solar cells was studied. In the humidity test, the devices were stored under different relative humidity (RH) varied from 15% to 100% in an environmental chamber, accumulatively at 25 ºC for 3 hours. After individual studies of the ITO, silicon nanostructure and PEDOT:PSS layer, we confirmed that the major causes of the PCE drop in the current devices are stemmed from the increase of the PEDOT:PSS sheet resistances and the increase of the ITO interface resistances. The current work not only highlighted the importance of the humidity control in the SiNWs/PEDOT:PSS hybrid solar cells, but also identified the major causes of the device degradation. By re-depositing the fresh PEDOT:PSS layer onto a fresh ITO and recycling the silicon in the degraded device, we demonstrated that the efficiency of the device can be nearly fully recovered.

CHAPTER 8 CONCLUSIONS AND FUTURE WORK

The objective of this project was to improve the power conversion efficiency of the hybrid silicon/PEDOT:PSS solar cells. The efficiencies of the solar devices were enhanced by solving the problems: (i) strong light reflection of the planar silicon wafer and (ii) high resistance of PEDOT:PSS film. With the gradual progress, the hybrid silicon/PEDOT:PSS solar cells are approaching towards high efficiency devices. At this circumstance, the degree of important on the devices' stability increases. Hence, the second objective of this project was to study the influences of bending and humidity on the efficiencies of the hybrid silicon/PEDOT:PSS solar cells. The following sections summarized the major contributions of this research and some future work was suggested.

8.1. Major contributions

In this project, with just utilizing a few common apparatus such as an ultrasound cleaner, a UVO cleaner, a spin-coater, a magnetic stirrer, an oven and a screen-printer, the silicon/PEDOT:PSS hybrid solar cells were successfully fabricated in air environment. This simple and cost effective fabrication method for solar cells was easy to achieve. There are four major contributions in this study and they were summarized as follows:

8.1.1. Employing silicon nanowires for improving light absorption of silicon

- The obtained silicon nanowires (SiNWs) array on the surface of the silicon wafers was well-ordered and large area coverage.
- Surface texturization by silicon nanowires method was used to relieve the problem of high optical reflection from the planar silicon. For planar silicon surface, the reflectance was around 40-70% in the 300-500 nm region and around 30-40% in 500-800 nm region, whereas the reflectance of the 5.87 μm textured silicon nanowires surface can fall below 8% within the entire visible spectrum.
- The higher absorption ability of photons in the texturized cells than planar cells contributing to higher rates of hole-electrons collection and thus the short circuit current in the device improved from 8.5 to 24.13 $mAcm^{-2}$.
- The photovoltaic efficiency of the nanowires texturized cells was six times better than that of the silicon planar cells. The power conversion efficiency improved from 1.1 (planar) to 6.87% (390 nm nanowires textured).
- The optimal height for SiNWs was 390 nm, provided the best performance devices in our experiment.
- Two problems that restricted long SiNWs (e.g. 4-5 μm) to contribute in high efficiency devices were found. Firstly, the infiltration of PEDOT:PSS was difficult for long NWs. Secondly, the higher recombination rate in the long SiNWs solar device led to poor charges collection.

8.1.2. Applying acid treatment to increase the conductivity of PEDOT:PSS

- For the as-prepared 5% DMSO-added PEDOT:PSS films, the conductivity measured from the four-probes measurement was around 683 S/cm. There was a gradual increase in the conductivity of PEDOT:PSS film by using higher concentration formic acid in the treatment. The average conductivity of the PEDOT:PSS films after treatment by 9, 49 and 98 wt% formic acid were 962, 1456 and 1582 S/cm respectively.
- AFM phase images revealed the conductivity enhancement of the PEDOT:PSS films after film treatment by formic acid should be ascribed to the more orderly oriented and aggregated conductive PEDOT chains.
- This was observed a 16.4% PCE improvement in the SiNWs/PEDOT:PSS hybrid solar cells after 98 wt% formic acid treatment is employed on the 5 wt% DMSO-added PEDOT:PSS film. The PCE of the device, without formic acid treated, was 8.00%. The PCE reached 9.31% when 98 wt% formic acid solution was used.
- After formic acid treatment, the results showed an increase in both open circuit voltage (V_{oc}) and fill factor (*FF*). The formic acid treatment retained high transmittance of the untreated PEDOT:PSS film. Hence, the short circuit current (J_{sc}) of the hybrid solar cells after formic acid treatment was nearly unimpaired.

- Series resistance (R_s) decreases from 2.23 to 1.51 Ωcm^2 in the SiNWs/PEDOT:PSS hybrid solar cell after 98 wt% formic acid treatment. The decrease in R_s in the treated devices should probably relate to the increased conductivity of the PEDOT:PSS film. The significances of the high conductivity PEDOT:PSS film were enhancing charges transfer and lowering the series resistance loss. The higher fill factor (*FF*) was attributed to a smaller series resistance (*Rs*).
- The reverse saturation current J_0 in the solar cells was found decrease after the formic acid treatment. This implied that the charges recombination in the device decreased after formic acid treatment. Moreover, V_{bi} increased by 0.06 V after a 98 wt% formic acid treatment such that the electric field was stronger for carriers separation. This suppressed carriers recombination loss in the formic acid treated device.

8.1.3. Investigating the bending flexibility of thin film hybrid solar cells

- Flexible hybrid solar cells with thin crystalline silicon sheet/PEDOT:PSS schottky junction was fabricated.
- The 15 μm thin film silicon sheets were used to test the feasibility and performance of flexible polymer/silicon solar cells. The flexible solar cells achieved a power conversion efficiency of 5.56% with open circuit voltage and short circuit photocurrent of 0.51 V and 16.96 mA/cm^2 respectively. The fill

factor of the solar cell was around 64.4%.

- Bending cycle test showed a good recovery of the original efficiency after 5000 cycles under a bending radius of 7 mm that the estimate bending stress in silicon was around 217 MPa. The results showed that the devices were flexible and bendable.
- The ability of bending repeatedly without varying much in the power conversion efficiencies of the solar cells held a significant importance for the development in the lightweight and rollable applications.

8.1.4. Identifying the causes of devices degradation due to humidity

- The major causes of the PCE drop in the ITO/PEDOT:PSS/silicon/GaIn devices were due to the increase of the PEDOT:PSS sheet resistance and the increase of the ITO interface resistances.
- Experimental results given that the as-fabricate PEDOT:PSS film had a sheet resistance of 7 kΩ/sq. After keeping the film in a humidity level greater than 98%RH environment for 60 min, the reading value of the sheet resistance of the film fluctuated during the four point probe measurement and the maximum sheet resistance reading was 7.8 kΩ/sq. However, after a 10 seconds nitrogen gas blow on the PEDOT:PSS film, its sheet resistance returned to a stable reading of 7 kΩ/sq. The results reflected that probably some trapped moisture in the film led to the increase sheet resistance of PEDOT:PSS in the humidity environment.

- Regarding to ITO, the averaged sheet resistances of fresh ITO was around 5.83 Ω/sq. After the degradation study, the sheet resistances of a ITO glass went up to 6.6 Ω/sq in the four-probe measurement. This revealed that the ITO layer was degraded after storing in the high humidity condition. It might probably due to the film etching of ITO by the hygroscopic and acidic PEDOT:PSS in the humid environment. The ITO/PEDOT:PSS interface was unstable.
- By re-depositing the PEDOT:PSS layer onto the degraded device and recycling the Si (and fresh ITO), we demonstrated that the efficiency of the device can be partially recovered (to almost fully recovered).

To conclude, this thesis explored the efficiency enhancement methods, the mechanical flexibility of thin silicon sheets and the degradation causes due to humidity. This study was of important in development towards low cost silicon solar cells. The fabrication of silicon/PEDOT:PSS hybrid solar cells is simple, cost effective and low temperature processing. With the further developments and optimizations, they could have a great potential to be the solar cells for real application. To improve efficiency , it is recommended to maximize light absorption and enhance carrier separation/collection efficiency. Proper encapsulation of the hybrid solar cells is also a good method to slow down the residual oxygen and moisture diffusion process. The longer service time of the solar cell is also a key for energy cost reduction.

8.2. Future work

The following future work would be beneficial to the development of the silicon/PEDOT:PSS solar cells in two ways: lower material cost and higher lifetime stability.

8.2.1. Reduce the use of silicon material by a silicon nanowires array transfer method

In conventional p-n junction silicon solar cells, around 40% of the module cost is attributed to the silicon wafer cost. Hence, further research is needed to reduce the use of silicon material to cut down the price of silicon based solar cells.

It was realized that silicon nanowires array on silicon substrate, fabricated from the metal assisted electroless etching method, could be scraped off or transfer away from the silicon substrate [126,127]. Therefore, the nanowires could be embedded or coated on a flexible substrate to serve as the semiconducting element in any flexible electronics application. This is not only lower the cost by using less silicon material, but also improve the bending flexibility by taking the advantage of the thin silicon nanowires array embedded into a flexible and transparent substrate. However, the difficulties in this type of solar cells are the inefficient of charges collection and easy short circuit paths which need to be further studied in details.

8.2.2. Improve the lifetime stability by light stabilizers

Another suggested area to further study is on the environmental stable materials. Some literature have already studied on the degradation factors of PEDOT:PSS, such as light intensity. The light of wavelength smaller than 315 nm would increase the sheet resistance of the 5wt%-DMSO-added PEDOT:PSS film [128]. This conductivity loss of PEDOT:PSS would lead to degradation problem in the hybrid solar cells. However, the solution to tackle the degradation has yet been fully proposed. Further experiments could be studies on improving the stability of the organic polymeric materials. For instance, studies can be carried out on the effect of UV or light stabilizer on the degradation of PEDOT:PSS. This can benefit the development of the polymer/silicon hybrid solar cells for longer lifetime.

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