STUDY OF ELECTROLYTIC CAPACITOR-LESS DESIGNS FOR LIGHT-EMITTING-DIODE (LED) LIGHTING APPLICATIONS

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Study of Electrolytic Capacitor-less Designs for Light-Emitting-Diode (LED) Lighting Applications

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Abstract

In recent years, light emitting diodes (LEDs) have made good progress in general lighting applications, gradually replacing traditional incandescent, fluorescent and halogen lamps. Their main advantages are high luminous efficiency, long life span and being environmental friendly. However, many offline LED drivers are designed with electrolytic capacitors, leading to a short life span and limited range of operation temperature. Thus, electrolytic capacitor-less designs are expected for LED lighting applications, along with high power factor, constant output current and high power efficiency.

This thesis is devoted to the study and design of effective LED driving solutions with no necessity of electrolytic capacitors. The main contributions of this thesis are summarized as follows:

A single-output electrolytic capacitor-less LED driver is proposed, where a high efficiency is achieved by using a minimal power processing (MPP) configuration. Near perfect power factor correction (PFC) is achieved by a simple dual-output discontinuous-conduction-mode (DCM) pulse-width-modulation (PWM) front-end converter. One output of the front-end converter is connected to the LED load using a control switch. The other output is connected directly to a dc storage capacitor cascaded with a downstream DCM PWM converter driving the same LED load to achieve constant output current (COC) driving. The power flow is controlled to achieve the required MPP which can also reduce the storage capacitance by balancing only the ac input ripple power and the dc

output power without power recycling. Thus, the design requires no electrolytic capacitor, hence extending the system life span.

Furthermore, based on a single dual-winding coupled inductor, a single-inductor multiple-output (SIMO) LED driver with PFC function is proposed without the requirement of electrolytic capacitors, where a small storage capacitance is used to actively decouple the ac and dc input powers. Compared with previous works, the proposed PFC SIMO LED driver has some additional benefits, including a smaller line filter, multiple output currents without double line frequency ripple and a faster output regulation. With appropriate control strategy, an independent output regulation can be achieved for each output channel. Meanwhile, to improve the converter efficiency, the energy flow of the converter is optimized with an inductor current programming technique.

Finally, an attempt is made to establish a DC power distribution for LED lighting. A family of bidirectional single-phase AC-DC three-phase-leg sinusoidal pulse-width-modulation (SPWM) converters with an AC storage capacitor for use in a nanogrid system is designed with a general control structure and a modulation for minimizing the AC storage capacitance. The general control structure is built based on a decoupled system with a power factor correction converter cascaded with an active AC power load at the DC bus. The decoupled system is developed based on a transformation in terms of differential-mode and common-mode voltages. The modulation introduces an extra zero-sequence voltage injection derived from the three-phase-leg SPWM voltages without introducing higher order harmonic distortions. A significant reduction of the AC storage capacitance and an improvement of converter efficiency are achieved.

Publications

Journal papers

- **H. Wu**, S. C. Wong, C. K. Tse, and Q. Chen, "Control and modulation of bidirectional single-phase AC-DC three-phase-leg SPWM converters with active power decoupling and minimal storage capacitance," *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4226-4240, June 2016.

- **H. Wu**, S. C. Wong, C. K. Tse, S. Y. R. Hui, and Q. Chen, "Single-phase LED drivers with minimal power processing, constant output current, input power factor correction, and without electrolytic capacitor," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 6159-6170, July 2018.

- **H. Wu**, S. C. Wong, C. K. Tse, and Q. Chen, "A PFC single-inductor multiple-output LED driver without electrolytic capacitor," *IEEE Transactions on Power Electronics*, submitted.

Conference papers

- **H. Wu**, S. C. Wong, C. K. Tse, and Q. Chen, "Analysis, control and design of a long-lifetime AC-DC bus converter within a nanogrid," in *Proceedings, IEEE Applied Power Electronics Conference and Exposition (APEC)*, Char-

lotte, USA, March 2015.

- **H. Wu**, S. C. Wong, C. K. Tse, and Q. Chen, "Control and modulation of a family of bidirectional AC-DC converters with active power compensation," in *Proceedings, IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, Canada, September 2015..

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Abbreviations List

AM	amplitude modulation
BCM	boundary conduction modulation
COC	constant output current
DCM	discontinuous-conduction-mode
LED	light-emitting-diode
MPP	minimal power processing
MPPT	maximum-power-point-tracking
PCB	printed circuit board
PCCM	pseudo-continuous conduction mode
PCS	pulsating current source

SIMO	single-inductor multiple-output
SPWM	sinusoidal pulse-width-modulation
SVPWM	space-vector pulse-width-modulation
TRIAC	triode for alternating current
PFC	power factor correction
PLL	phase-locked loop
PS	power-stage
PV	photovoltaic
PWM	pulse-width-modulation
SIDO	single-inductor dual-output

Nomenclature List

Unless otherwise specified, some commonly-used symbols in the thesis are defined as follows.

Symbol	Description
L	Inductance
C	Capacitance
R	Resistance
P	Power
E	Energy
η	Efficiency
v_{in}	Input line voltage
V_{in}	Root mean square value of the input line voltage
V_m	Peak of the input line voltage
i_{in}	Input line current
I_{in}	Root mean square value of the input line current
I_m	Peak of the input line current
v_{rec}	Rectified line voltage
i_{rec}	Rectified line current
f_l	Line frequency
ω_l	Line angular frequency
I_o	Output current
V_o	Output voltage

Chapter 1

Introduction

1.1 Electric Lighting versus Fire

In the early stage of human civilization, fire could be the only controllable lighting source. A variety of fuels can be burned in an oil lamp, such as animal oil, vegetable oil and coal oil. Since these liquid fuels are uneasy to be stored or transported, the oil lamp is not a safe and reliable lighting source. Meanwhile, it requires to be refueled and cleaned manually, and generates black smoke and unpleasant smell as well. To have an improvement in convenience, lamps with burning solid or gaseous fuels were developed later, where disposable candles remove the requirement of manual cleaning and unattended gas lamps are suitable for a large-scale street lighting with a commercial gas distribution. However, the improvement in convenience is still limited, since all these lamps generate light with fire from heat as a by-product of chemical combustion.

Fortunately, Michael Faraday discovered the principle of electromagnetic induction in 1831. Then, after decades of effort, the modern dynamo for industrial applications, was invented independently by Sir Charles Wheatstone, Werner von Siemens and Samuel Alfred Varley. Based on the basic principles of electromagnetic induction, these invented modern dynamos can convert mechanical energy

to electric energy easily. Looking back at the history, these important discoveries and inventions launched the age of electricity, and also made electric lighting being feasible.

In the age of electricity, the carbon arc lamp, invented by Humphry Davy in the first decade of the 1800s, was the first practical electric light, but it was restricted only for the street and large building lighting. Indeed, it was the later incandescent lamp that detonated the revolutionary world-wide applications of general electric lighting. The basic idea is to heat a wire filament electrically instead of chemical combustion to such a high temperature that it glows with visible light. Although many earlier inventors had previously devised incandescent lamps, including Alessandro Volta, Henry Woodward and Mathew Evans, the incandescent lamp cannot be practically used for the extremely short lifespan and high production cost, until Thomas Alva Edison began to use "a carbon filament or strip coiled and connected to platina contact wires" in 1880.

Historically, the first generation of electric lighting, i.e., the carbon arc lamp and the incandescent lamp, separated the light from the fire for the first time, and it had already shown some attractive advantages over competitors. Since it produces no burning residue and requires no oxygen in the sealed lamp, a clean, safe and weatherproof lighting is obtained. Moreover, endless electric energy can be distributed economically, having a stable and continuous light through the electric lamp. Interestingly, it was the commercial profit of electric lighting that prompted Thomas Alva Edison to develop a public system of electric power generation and distribution, i.e., the earliest power system.

In the competition with DC power system, that developed by Thomas Alva Edison, Nikola Tesla insisted on promoting AC power system. Until Tesla invented an asynchronous motor, the advantages of AC high-voltage transmission were also demonstrated, and the problem that the machine was unable to use AC power was also solved.

1.2 Modern Electric Lamps

The modern incandescent lamp with a coiled filament of tungsten, was commercialized in the 1920s, and it has been used for nearly a hundred years. However, the incandescent lamp still shares a similar lighting principle of heating with that of fire. Particularly for the incandescent lamp, the electric current flow through the thin and fine filament to produce visible light. The current rises the temperature of the filament to such extent that it becomes luminous.

When the filament is made hot, the atoms inside the filament become thermally excited. If the filament is not melt, the outer orbit electrons of the atoms jump to higher energy level due to the supplied energy. The electrons on these higher energy levels are not stable they again fall back to lower energy levels. During falling from higher to lower energy levels, the electrons release their extra energy in a form of photons. These photons then emitted from the surface of the object in the form of electromagnetic radiation.

This radiation will have different wavelengths. A portion of the wavelengths is in the visible range of wavelengths, and a significant portion of wavelengths are in infrared range. The electromagnetic wave with wavelengths within the range of infrared is heat energy and the electromagnetic wave with wavelengths within visible range is light energy.

However, less than 3% of the electric energy can be converted into usable light, and other energy is wasted in a form of heat. Not only that, more electricity has to be consumed for air conditioning and exhaust systems, to dissipate the heat generated by incandescent lamps. Meanwhile, the lifespan of incandescent lamps is also limited.

Consequently, many countries have already planed to phase out incandescent lamps. Nowadays, the replacement of incandescent lamps could be halogen lamps, fluorescent lamps, and light-emitting-diode (LED) lamps. A brief comparison of

Table 1.1: Comparison of electric lamps

Types	Luminous efficacy [lm/W]	Lifespan [h]
Incandescent	14.3	1,000
Halogen	14.42	2,500
Fluorescent	57.14	8,000
LED	80∼96.94	25,000∼30,000

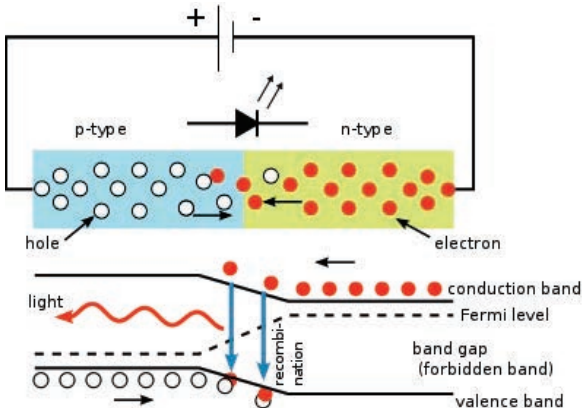


Figure 1.1: A representation of how LEDs create light.

electric lamps is given in Table 1.1.

It can be observed that LED lamps has the highest luminous efficacy and the longest lifespan, which has been applied widely. An LED is a type of semiconductor diode. It is a two-terminal electronic component that conducts electric current in only one direction. In an LED, a chip of semiconducting material is impregnated or doped, with impurities to create a structure called a p-n junction. These junctions are fundamental building blocks of many electronics, including transistors, integrated circuits, and solar cells. As in other diodes, current flows easily from the p side to the n side, but not in the reverse direction. Electrons and electron holes flow into the junction, and when an electron meets a hole, it drops to a lower energy level, thereby releasing a photon, as shown in Figure 1.1. This effect is called electroluminescence [1]. A fundamental change is that no heat is required to generate light. However, heat is generated as a by-product of electric conduction.

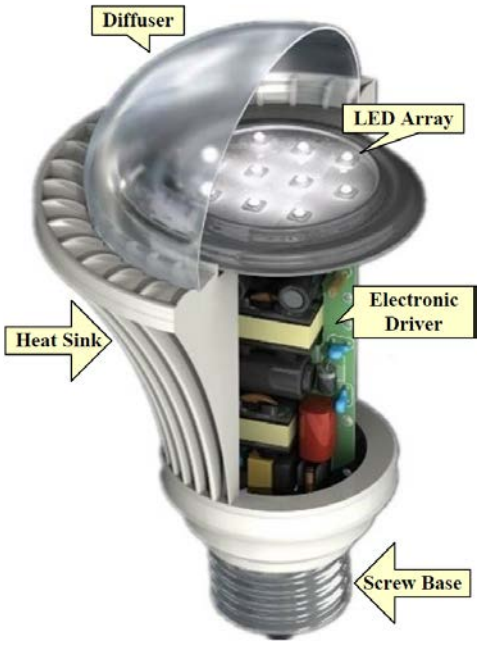


Figure 1.2: Breakdown of an LED lamp.

1.3 Requirements of LED Drivers

A breakdown of an LED replacement lamp is given in Figure 1.2. Multiple LEDs are intergraded to be a single electrical load, i.e., an LED array, and the light of LEDs is soften by the diffuser. While, a heat sink dissipates the generated heat of LEDs. On a purpose of power conversion, an electronic driver converts power from the power line to the LED array, which will be focused and investigated in this thesis.

1.3.1 LED's Circuit Model

The current and voltage of an LED can be approximated by

$$I_F = I_S \left(e^{qV_F/kT} - 1 \right), \tag{1.1}$$

where I_F is the current of LED, I_s is the reverse saturation current, q is the electron charge, k is the Boltzmann constant, and T is the absolute junction

temperature [2]. The V-I characteristic is similar to that of a diode.

In terms of temperature effects, the voltage of LED is inversely proportional to temperature, i.e., the voltage of LED decreases if temperature increases. If a voltage source powers LED, the LED current will raise rapidly with such a temperature characteristic. The LED will be burned if the heat cannot be released.

For a practical lighting application, multiple LEDs are normally connected in series and/or in parallel for a higher luminous output. With a sharp V-I characteristics, the overall LED load is normally modeled as a voltage source connected with a small resistor and an ideal diode. The output luminous can be simply changed by varying the current in LEDs.

Since the equivalent resistor is small, the LED current will be sensitive if using a voltage-source driver. However, voltage-source distribution has been popular for centuries. In this case, an LED driver, that bridges the power line and the LED array, should act as a current source for driving LEDs.

1.3.2 Current Balancing

For high-brightness lighting applications, several LED strings are normally connected in parallel to form a single LED load, where each LED string is formed by connecting some LEDs in series [3]. However, due to a statistical manufacturing spread and an effect of temperature gradient, unequal current in each LED string can be expected if a number of paralleled LED strings are connected to a common terminal as a single load. With a current balancing technology, the high current in some LED strings can be reduced, and a longer lifespan of LEDs can be achieved. In this case, various methods have been proposed to have a balanced current in LED strings.

As shown in Figure 1.3, in order to have identical V-I curves for each LED

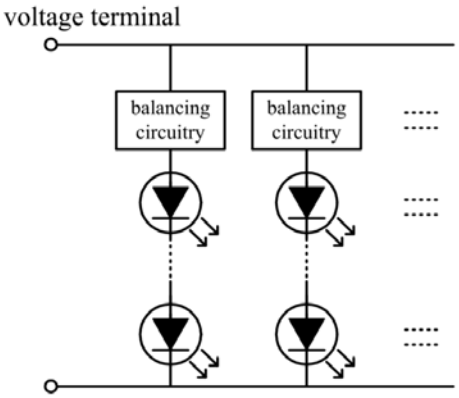


Figure 1.3: LED load with balancing circuitry for each LED string.

string, the voltage difference in each LED string should be compensated by the balancing circuitry. Present realizations of the balancing circuitry can be classified into active and passive approaches. The usual active balancing circuitry can be switched current regulators, linear current regulators and current mirrors and so on. The linear current regulator and current mirror are simple to be implemented, but the loss of the power transistor will be high due to the operation in linear region. While, the transistor in switched current regulator is operated on and off, a lower power loss accomplished with an increased control complexity are both expected.

In the passive balancing circuit, the inductor and capacitor are good candidates for minimizing loss. With the principles of magnetic flux and capacitive charge balance, currents in multiple LED strings can be balanced. However, a large number of coupled inductors or an even number of LED strings are required. Moreover, if using a reactance in series with the resistive LED string, balanced currents can also be achieved as long as the reactance is large enough.

1.3.3 Dimming and Color Mixing

In an LED driver, the output current can be sensed and controlled to be identical with a current reference. If a dimming function is required, an amplitude

modulation (AM) can be realized with simply modifying the LED current reference. While, for a pulse-width-modulation (PWM) dimming, the averaged LED current is also regulated, but the LED peak current is maintained at the desired value to have constant color coordinates. It should be noted that a multiple-stage design with a fast output regulation can provide a greater PWM dimming frequency. While, in the early stage of LED lighting, since the triode for alternating current (TRIAC) dimmers were widely used for incandescent lamps, an attempt was made that the LED current is adjusted depending on the TRIAC firing angle [4]. A flyback converter operated in discontinuous conduction mode (DCM) or boundary conduction mode (BCM) can satisfy such a requirement.

To further explore the advantage of LED dimming, the luminous that comes from different color LEDs, can be mixed easily [5]. The basic LED cells includes red, green, blue, warm white and cool white. If the color mixing is extended, multiple output function is also required.

1.3.4 Electrolytic Capacitor-less Design

To satisfy some industrial standards, such as Energy Star and IEC 61000-3-2, a power factor correction (PFC) function is required for LED drivers. On the other hand, the LED current is expected to have a minimal ripple current at the low-frequency range for flicker-free applications. The power difference between the input and output ends should be balanced by reactive components in the LED driver, where electrolytic capacitors are usually adopted for its high power density.

For some low-cost LED replacement lamps, electrolytic capacitors can be easily found on the printed circuit boards (PCBs), as shown in Figure 1.4(a). Various electrolytic capacitors are presented in Figure 1.4(b), where the electrolytic capacitor with a higher voltage rating or a higher capacitance usually has a larger

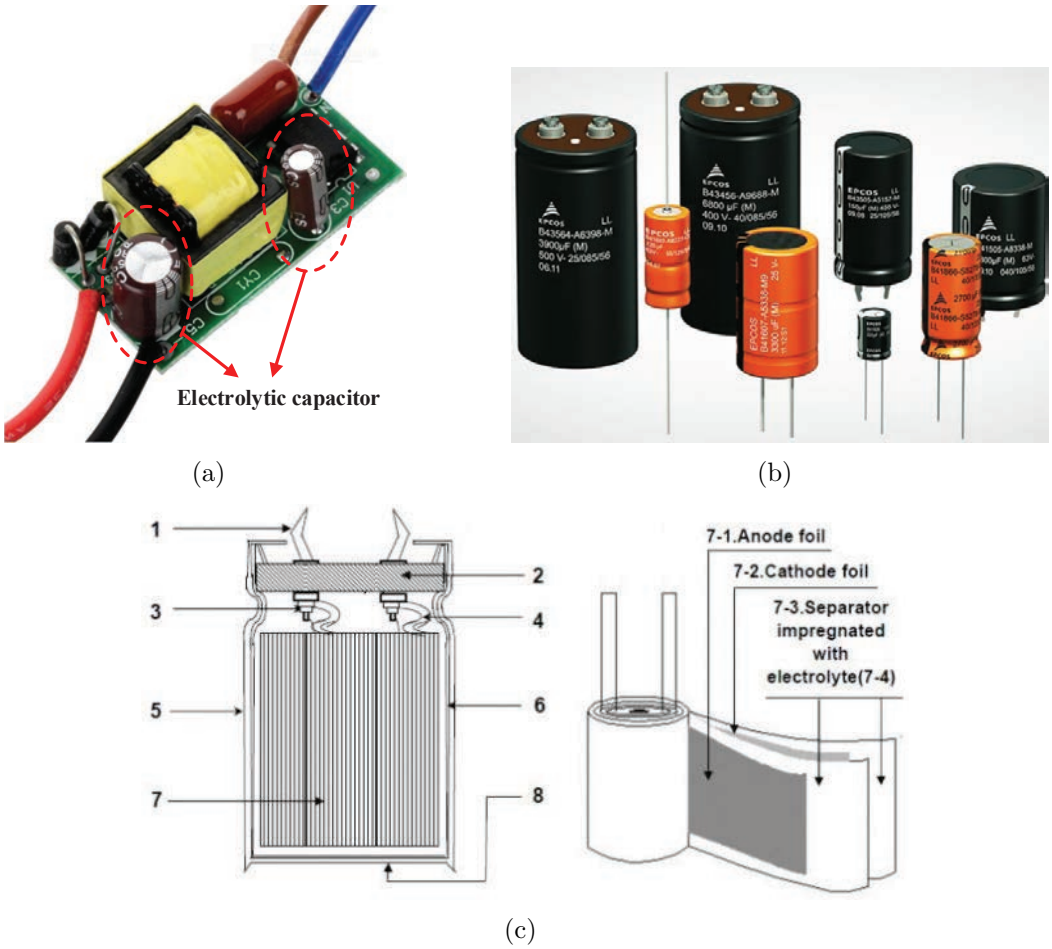


Figure 1.4: (a) An electronic driver for LED replacement lamps, (b) electrolytic capacitor and (c) its internal diagram.

size.

In an LED system, a normal operation of LED drivers is always expected before LEDs fail, i.e., the lifespan of LED drivers should be matched with that of LEDs. In the production process of electrolytic capacitors, the separator is impregnated with electrolyte, as shown in Figure 1.4(c). Unfortunately, the electrolytic capacitor greatly limit the lifetime of LED drivers. With an increase of 10 degrees in ambient temperature, the lifespan of electrolytic capacitors will be halved. Especially, for street lighting applications, the extreme high temperature may accelerate the evaporation of the electrolyte, and the extreme low temperature may also freeze the electrolyte. Therefore, electrolytic capacitor-less LED

drivers are intensely developed [6].

1.4 Objective of the Thesis

In the thesis, electrolytic capacitor-less designs will be investigated for LED lighting applications.

Focused on lower power applications, single-output and multiple-output LED drivers will be proposed without using electrolytic capacitors.

Furthermore, for higher power applications, bidirectional AC-DC PFC converters with active ripple power decoupling are investigated. With such kind of converters, a nanogrid system can be easily established. With the involvement of various sustainable sources, the energy utilization can be improved. Moreover, with a DC voltage input, electrolytic capacitor-less LED drivers can be easily designed.

1.5 Outline of the Thesis

This thesis is organized as follows.

Chapter 1 introduces the development of electric lighting and a general comparison for modern electric lamps. The requirements of LED drivers are introduced from three aspects, including current balancing, dimming technology and electrolytic capacitor-less design. The research objectives, as well as an outline of this thesis are presented.

Chapter 2 gives a literature review to pursue electrolytic capacitor-less designs for LED lighting. Existing single-output offline LED drivers are classified from the perspective power flow processing, and they are compared from three aspects, i.e., (1) capacitance reduction, (2) driver and control complexities and (3) losses due to parasitic elements. The electrical structures of LED drivers with multiple

outputs are also reviewed and discussed. Finally, bidirectional single-phase AC-DC converters with active ripple decoupling are reviewed.

Chapter 3 proposes a single-output LED driver, where the efficiency can be improved due to minimal power processing and its control is readily implemented.

Chapter 4 proposes a multiple-output LED driver with single inductor, where the number of inductors has been reduced greatly. Moreover, various benefits, including small line filter, multiple output currents without double line frequency ripple and a faster output regulation, are also achieved.

Chapter 5 presents a family of bidirectional single-phase AC-DC three-phase-leg converters. A general control is proposed, and a technology of zero-sequence voltage injection is adopted for sinusoidal pulse-width-modulation (SPWM) modulation to achieve a minimal AC capacitance.

Finally, Chapter 6 gives a conclusion to the thesis. The major work and contributions are reiterated. Some suggestions for future research are given.

Chapter 2

Literature Review

In this chapter, existing off-line LED drivers, where various circuit topologies can be operated without electrolytic capacitors, are first reviewed, including the single-output and multiple-output applications. On the other hand, since electrolytic capacitor-less LED drivers can be easily designed with a DC power line, it is an alternative solution to establish a hybrid nanogrid system, and thus bidirectional single-phase AC-DC bus converters with active ripple power decoupling are also reviewed.

2.1 Single-Output LED Drivers

2.1.1 Classification

For single-output LED drivers [6], the requirements of PFC and constant output current (COC) necessitate the use of an energy storage capacitor for handling the imbalance between the input ripple power at double line frequency and the output constant power, with minimal power processing (MPP) [7–9]. To make the life span of the LED driver comparable with the LEDs, the use of a high charge density but relatively shorter life span electrolytic capacitor should be

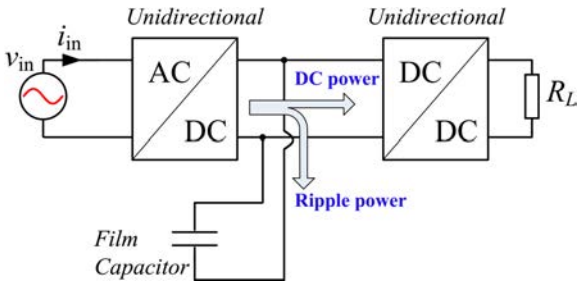
avoided.

An important design aspect of usual single-output LED drivers is the multiple design goals and their tradeoffs. Specifically, the charge storage capacitance can be reduced either by operating it at a higher voltage with the same power storage or relaxing the requirement of input power factor and/or the output current regulation with reduced power storage.

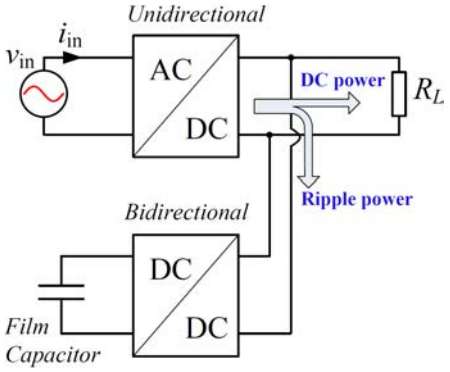
A single-stage design can hardly avoid the use of large storage capacitance [6,10] due to the low degree of freedom in optimizing input PFC, COC, MPP and the reduction of charge storage capacitor. An integrated multiple-stage design allows the storage capacitor to be isolated from the LED load and at the same time permits the use of smaller capacitance at the expense of a higher capacitor voltage ripple. However, an integrated multiple-stage converter may have low overall conversion efficiency [6]. By allowing the controls of MPP, PFC and COC to be less precise, other converter constraints can be optimized and the use of a shared switch can be achieved [11,12]. However, such implementation also incurs higher output current ripple which reduces the life span of the LEDs being driven. Given the importance of lighting applications and their huge power consumption, high power factor and efficiency are still the crucial design factors.

The two-independent-stage configuration shown in Figure 2.1(a) can achieve better input PFC, COC and efficiency, compared to other integrated configurations [6, 13–15]. In this design, a front-end PFC converter is cascaded with a DC-DC regulator, with a storage capacitor buffering the power imbalance. It is thus a 2-power-stage (2-PS) converter. The overall efficiency η_α is simply the product of the average efficiency η_1 of the PFC converter and that of the DC-DC converter η_2, i.e.,

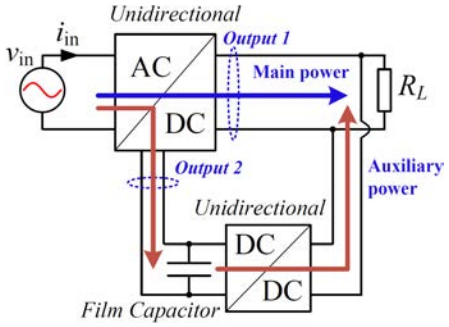
$$\eta_\alpha = \eta_1 \eta_2. \tag{2.1}$$



(a) two-stage design



(b) n_β-power-stage design



(c) n_χ-power-stage design

Figure 2.1: LED drivers and power processing stages.

The two-stage design can be optimized for MPP by directly forwarding power to the load, and the ripple power is compensated by connecting the output with a bidirectional converter and a capacitor storage [16–20], as shown in Figure 2.1(b). In this type of 2-PS with MPP design, the best overall efficiency is

$$\eta_\beta = k_1\eta_1 + (1-k_1)\eta_1\eta_{2_f}\eta_{2_b}, \tag{2.2}$$

where $k_1 = 1-\frac{1}{\pi}$ is the maximum portion of power directly delivered to the load by the PFC stage, η_{2_f} and η_{2_b} are the efficiencies of the forward and backward power conversions of the bidirectional converter, respectively. The number of effective power processing stages of the converter shown in Figure 2.1(b), denoted by n, can be determined from an energy-flow-path analysis [21]. Specifically, for the 2-PS configuration, if the efficiency of each stage is identically η_i, then $\eta_\alpha = \eta_i^{n_\alpha}$ and $n = n_\alpha = 2$. Similarly, for the 2-PS with MPP configuration, equation (2.2)

becomes

$$n = n_{\beta,\min} = k_1 + (1 - k_1)3 = 1.64. \tag{2.3}$$

Another power flow optimized 2-PS design with MPP is shown in Figure 2.1(c), which uses a PFC stage with dual outputs. One output directly delivers power to the load, and the other output delivers power to the charge storage capacitor. The charge stored in the capacitor is converted to the load via a power converter. The maximum overall efficiency is

$$\eta_\chi = k_1\eta_1 + (1 - k_1)\eta_1\eta_2. \tag{2.4}$$

Thus, we have $n = n_{\chi,\min} = 1.32$. In this way, based on the energy-flow-path analysis, a converter can generally be identified as an n-PS converter for a unified topological comparison. The parallel power-factor-correction converters described in [22–25] have been targeted for PFC regulator applications with no consideration of LED driving requirements. The basic concept, however, is applicable to LED drivers [26–29]. A specific example of an $n_{\chi,\min}$-PS converter was reported by Chen and Hui [26].

2.1.2 Comparison

The 2-PS off-line LED driver can be designed with the desired properties of absence of electrolytic capacitor, high input power factor, and constant current output [13–15]. However, in terms of efficiency, it is a 2-PS converter, and in terms of the number of active switches, it needs at least two. Improvement on efficiency has been proposed by adopting an n_β-PS design [18–20] and n_χ-PS design [26,27] with the number of active switches increased to three. On the other hand, the number of active switches can be reduced by integrating the stages at

the expense of compromising input power factor or output regulation. However, these integrated two-stage LED drivers [11, 12] are still 2-PS designs which have no topological advantage in improving efficiency. In this section, we will compare the off-line LED drivers in terms of (1) design without an electrolytic capacitor, (2) driver and control complexity, and (3) losses due to parasitic elements. A summary is given in Table 2.1.

Capacitance Reduction

The 2-PS LED driver can readily achieve a design without an electrolytic capacitor thanks to the storage capacitor being isolated from the input power factor and output current regulation. The storage capacitance can be further reduced if the input power factor can be compromised by allowing third-order current harmonics [14] or the constant output current is controlled with PWM dimming and/or bi-level dimming [15]. The n_β-PS and n_χ-PS off-line LED drivers can retain similar merits of the two-stage design for the reduction of the storage capacitance. Moreover, the output capacitance in parallel with the LED string can be used solely for removing converter switching ripples, and is therefore relatively small.

Due to the limited control freedom of a single switch in the integrated two-stage LED driver, double line-frequency ripple power cannot be completely eliminated at the output. Instead, the ripple power may be mitigated by designing the storage capacitor with a higher voltage or larger capacitance [11], making it harder to eliminate the electrolytic capacitor. Moreover, to achieve better output current regulation, the extra output current control in [12] may cause unstable converter operation. Also, without the extra control freedom provided by more active switches such as in 2-PS, n_β-PS design or n_χ-PS design, control techniques like third-order harmonics injection [14] and PWM dimming and/or bi-level dimming [15] are not applicable.

Table 2.1: Comparison of Electrolytic Capacitor-less LED Drivers

Classification		2-PS [13–15]	ISD [11, 12]	n_β-PS [18–20]	n_χ-PS [26, 27]
Topological number of processing stages		2	2	1.64	1.32
Minimum number of active switches		2	1	3	3
Control complexity		Medium	Low	High	High
Achieving both high PFC and COC		Easy	Difficult	Easy	Easy
Capacitance reduction	Narrow Input Range	Excellent	Good	Good	Good
	Wide Input Range	Excellent	Medium	Good	Good
Line current harmonics injection		Easy*	Difficult	Easy	Easy
Output PWM dimming		Easy#	Difficult	Difficult	Easy

Key: $*$ verified in [14]; # verified in [15]; ISD denotes integrated stage design

Driver and Control Complexities

The single-switch integrated two-stage off-line LED drivers have the lowest complexity in terms of active switch driving and control. For some specific applications, where the input voltage range is narrow and some double line-frequency ripple output currents are allowed, they have the lowest cost and size.

The control of two to three active switches in 2-PS, n_β-PS design and n_χ-PS design is more complicated. Efforts have been made to remove one active switch for the n_χ-PS design [28, 29]. However, either the input power factor or output current regulation must be significantly compromised.

Compared with 2-PS off-line LED drivers, the n_β-PS design described in [18–20] requires an extra sensor for its output current loop, and the n_χ-PS design described in [26, 27] requires an extra line voltage sensor for the timing control of charging and discharging of the storage capacitor.

Loss Due to Parasitic Elements

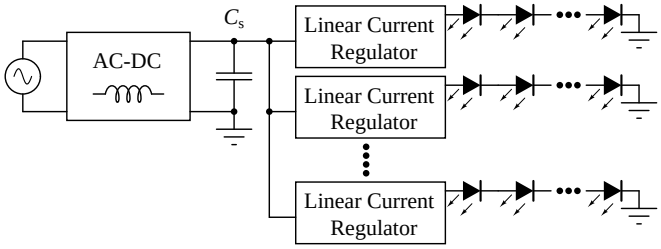
In general, the efficiency of various types of off-line LED drivers can be compared in terms of the value of n in an n-PS configuration by using the energy-flow-path analysis [21]. However, different configurations may involve different sets of parasitic elements which may incur extra power losses. Efforts have been made to minimize such losses. Specifically, the energy stored in the leakage inductance of the integrated configuration described in [11] has been recycled to the storage capacitor, the energy stored in the leakage inductance of the n_χ-PS design in [26] can be recycled via the one-stage power path and is dissipated in the two-stage power path, and the energy stored in the leakage inductance of the n_χ-PS design in [27] is completely dissipated.

2.2 Multiple-Output LED Drivers

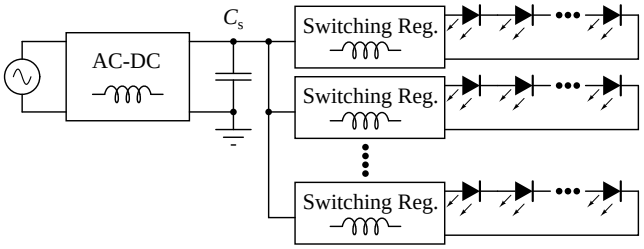
Due to the ease of dimming electronically, LEDs can support lighting applications with color mixing and color temperature adjustment [5]. The dimming control is generally an independent regulation of current for luminous brightness of different color LEDs, mixing color outputs chosen from red, green, blue, cool-white and warm-white LEDs. Therefore, an LED driver should be more desirably designed with multiple outputs for independent brightness control.

With an AC source input at a line frequency of f_l, the multiple-output LED driver can conveniently be designed using two-stage electrical structures as shown in Figures 2.2(a), 2.2(b) and 2.2(c). The front-stage PFC pre-regulator tightly controls the input current for near unity power factor which results in an output of equal magnitude DC and AC power components. The pre-regulator regulates a constant DC voltage across the capacitor C_s for the required DC output power. Therefore, the AC power component appearing as $2f_l$-ripple voltage is unregulated or otherwise the input unity power factor needs to be compromised. The capacitor C_s buffers the DC power component and filters the AC power component at $2f_l$. It is commonly denoted as a DC-link capacitor, and will also be denoted here as a $2f_l$-filtering capacitor. Load-stage converters acquire power from C_s and regulate LED powers independently.

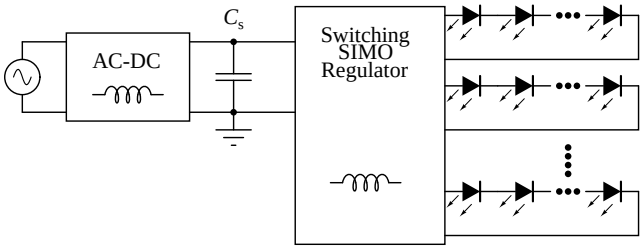
Multiple load-stage converters implemented with linear current regulators as shown in Figure 2.2(a) can provide accurate and rapid output current control independently for each LED string [34,35]. The linear regulators can be replaced by better efficiency switched-mode converters as shown in Figure 2.2(b), from which the design comes with more bulky power inductors whose number grows linearly with the number of LED strings. In Figure 2.2(c), a load-stage converter can be built to share a single inductor for multiple outputs (SIMO) with reduced size, cost and component count. Much research solely focuses on the second-



(a) A PFC pre-regulator cascaded with multiple linear current regulators



(b) A PFC pre-regulator cascaded with multiple switching DC-DC regulators



(c) A PFC pre-regulator cascaded with a switching SIMO DC-DC regulator

Figure 2.2: Two-stage electrical structures of AC-source input and multiple-output LED drivers.

stage topology which is a DC-DC SIMO converter derived from buck [36–38], boost [39–42] or buck-boost [43] converter. Although the topology in Figure 2.2(c) has been implemented in [44], no attempt has been made on the reduction of the electrolytic capacitor C_s. The regulations of outputs from the DC-DC SIMO converter have been extensively studied with different control strategies, such as DCM operation with time-multiplexing [40], digital-controlled continuous conduction mode (CCM) operation [36], and pseudo-continuous conduction mode (PCCM) operation with an extra switch paralleled with the inductor [42].

Among the two-stage structures shown in Figures 2.2(a), 2.2(b) and 2.2(c),

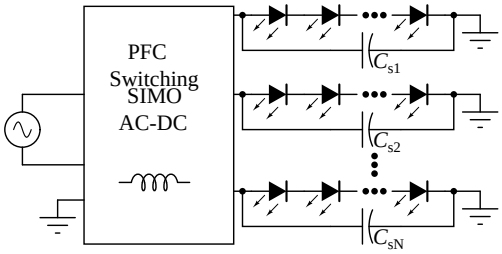


Figure 2.3: Single-stage SIMO converters with distributed C_s

only the structure shown in Figure 2.2(a) is a *true* SIMO LED driver, the other two structures use two or more independent inductors. However, in the structure shown in Figure 2.2(a), due to the low power efficiency of linear current regulators, heat sinks of larger size and weight are needed for heat dissipation, which may defeat the compact purpose of single inductor design. Moreover, all these two-stage structure has the drawback of two-power-processing stage.

Consequently, a single-stage PFC SIMO converter structure as shown in Figure 2.3 is reported to have a higher efficiency for some non-isolated LED applications [45–47]. However, due to single-stage design, C_s has to be distributed into multiple capacitors, and be connected in parallel with the N-LED strings for the filtering of individual $2f_l$-ripple current.

There are drawbacks in this current filtering configuration. Each filtering capacitor voltage has to be fixed at the LED driving voltage and thus, the voltage of each filtering capacitor cannot be a design parameter. A minor variation of the capacitor voltage would lead to a much larger variation of LED driving current. The utilization of capacitance for the purpose of current filtering is therefore low. The more than necessary capacitance values require high charge density electrolytic capacitors, making it impossible to replace electrolytic capacitors by small film capacitors for achieving longer life span and wider operating range of ambient temperature. The residue $2f_l$ ripple power makes constant current output or flicker-free lighting difficult and can be harmful to the LED life span.

Moreover, this passive capacitor $2f_l$-ripple power filtering is highly inefficient when it is compared with some active ripple power decoupling implementations [7], where the AC ripple power is actively buffered by C_s and the ripple-less DC power is decoupled and delivered to the LED load.

2.3 AC-DC Bus Converters and Nanogrids

Various green technologies have been investigated and developed to address the issues of energy shortage, poor sustainability and green-house gas production. However, a large portion of the green sources and loads, such as solar energy and LED load, are of DC type which cannot be fully utilized in the traditional AC distributed system. Thus, a DC bus is added to the traditional distribution system, forming a microgrid system [51] or a nanogrid system for residential power applications [52]. Most consumer electronics, electronic ballasts, LED lighting, and variable speed motor drives can be more conveniently powered by the DC bus. Specially, electrolytic capacitor-less LED drivers can be easily designed with a DC voltage-source input.

In the nanogrid system, a converter with functions of power factor correction at the AC port and second-order harmonic ripple power elimination at the DC bus is required for a bidirectional single-phase AC-DC power conversion [51–56]. The design of power-factor-correction converters has been well established. The second-order harmonic AC power will manifest as a second-order harmonic AC ripple voltage superimposed on the DC bus. The AC power ripple in the DC bus will cause visible flickers in LED lighting [57–60], deteriorate the maximum-power-point-tracking (MPPT) performance of module-integrated inverters [61–64] in photovoltaic (PV) systems, create thermal problems in fuel cell power conditioning systems [65], produce beat components in the motor current of AC-fed railway traction drives [66,67], complicate the operation of converters implement-

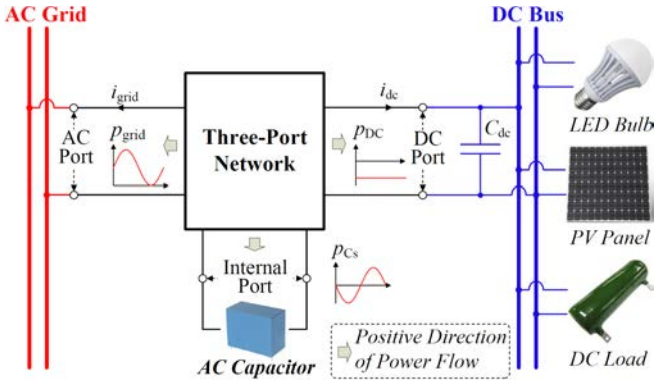


Figure 2.4: Nanogrid and single-phase AC-DC bus converter with active power decoupling.

ed with power sharing based on droop V-I characteristics, and cause overheating to battery storage [55, 56].

Techniques for eliminating second-order harmonic ripple power at the DC bus include bulky passive methods [68], as well as active methods [67,69–75], of which the active methods with AC capacitive storage provide solutions with smaller size and better second-order harmonic ripple power elimination.

Various topologies have been reviewed in [76]. Among these active methods, the three-phase-leg AC-DC pulse-width-modulation (PWM) converter is a natural evolution of the four-phase-leg AC-DC PWM converter [77], resulting in higher efficiency, smaller size, lower cost and longer lifetime. The space-vector PWM (SVPWM) three-phase-leg converter has been designed for optimized storage capacitance, but might suffer from higher order harmonic distortions [78]. Moreover, the two-phase-leg design might suffer from higher voltage stress than the DC bus voltage on main switches and with less room for optimizing storage capacitance [79].

Chapter 3

Single-Output LED Drivers With Minimal Power Processing

3.1 Introduction

To fully utilize the advantages of LED in lighting applications, the off-line power supply that drives the LED should possess the following features: high efficiency, long life span, high input power factor, and constant output current. In this chapter, high efficiency is achieved by using a minimal power processing (MPP) configuration. Near perfect PFC is achieved by a simple dual-output DCM PWM front-end converter. One output of the front-end converter is connected to the LED load using a control switch. The other output is connected directly to a dc storage capacitor cascaded with a downstream DCM PWM converter driving the same LED load to achieve constant output current (COC) driving. The power flow is controlled to achieve the required MPP which can also reduce the storage capacitance by balancing only the ac input ripple power and the dc output power without power recycling. Thus, the design requires no electrolytic capacitor, hence extending the system life span. The achievement of input PFC, MPP and COC requires design trade-off among design freedom, ease of control

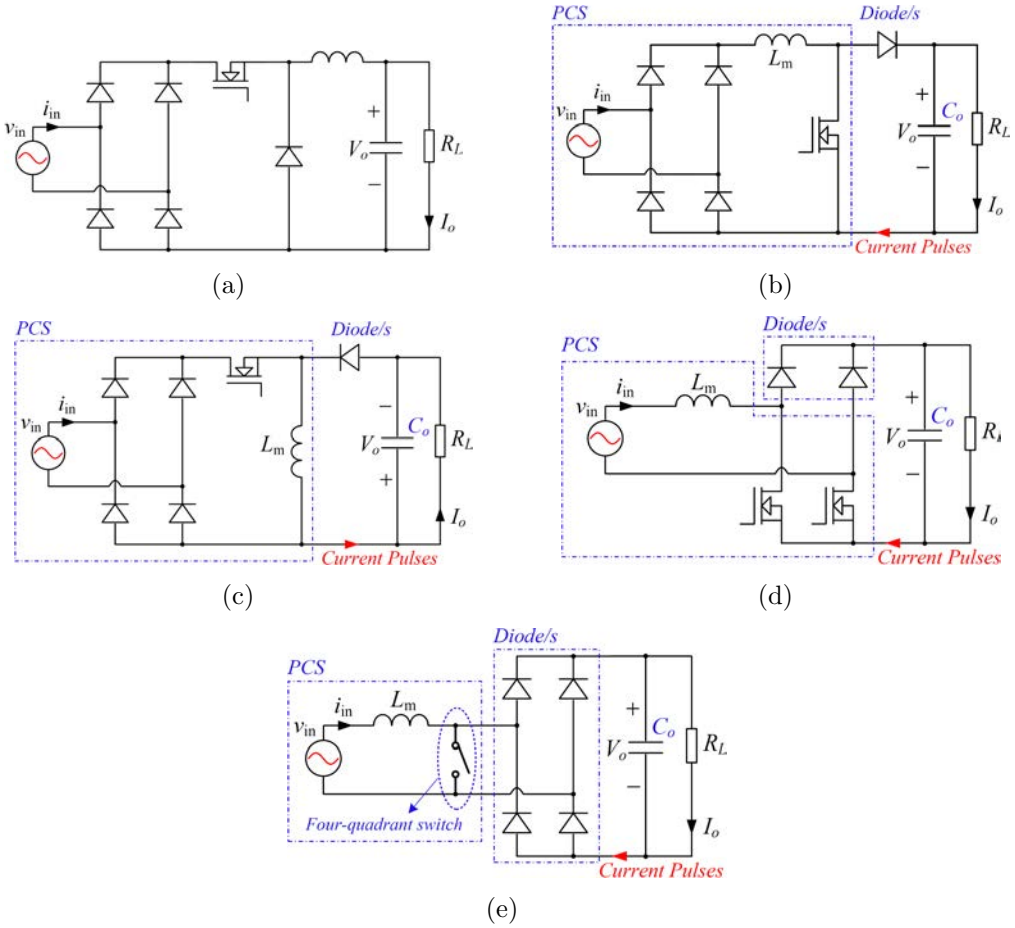


Figure 3.1: Active non-isolated PFC converters: (a) Buck PFC, (b) boost PFC, (c) buck-boost PFC, (d) bridgeless boost PFC, and (e) bridgeless PFC converters with a four-quadrant switch.

and component count. LED drivers having all these properties are developed, designed and tested.

3.2 LED Driver Architecture

In this section, a single-phase LED driver architecture with PFC and COC is developed using the $n_{\chi,\min}$-power-stage ($n_{\chi,\min}$-PS) design in Figure 2.1(c). The first stage PFC converter can be chosen from some simple non-isolated PWM converters shown in Figure 3.1, some of which have pulsating current source (PCS) outputs [31]. Among these topologies, the buck PFC converter shown in Fig-

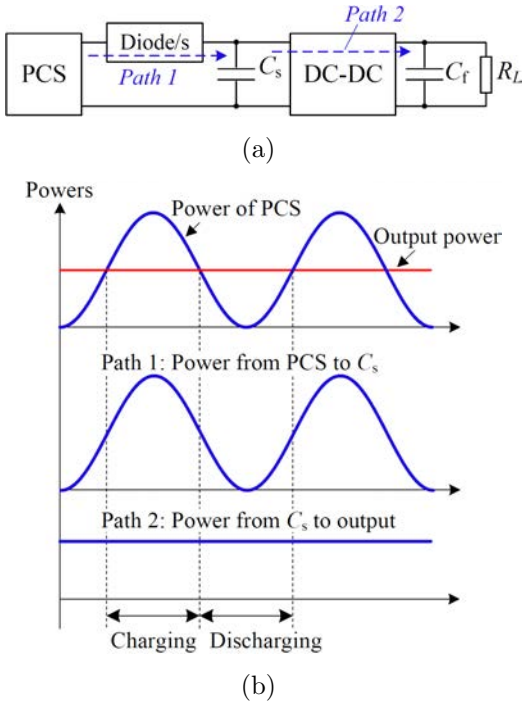


Figure 3.2: Power flow of a traditional two-stage LED driver: (a) Block diagram and (b) power waveforms.

ure 3.1(a) cannot sink input current when the rectified line voltage is lower than the output voltage, leading to a lower power factor. The boost PFC converter shown in Figure 3.1(b) and its bridgeless versions as shown in Figures 3.1(d) and 3.1(e) are widely implemented in high power applications, operating in continuous conduction mode (CCM). When operating in DCM, the average input current of the boost PFC converter, like the buck converter, depends on both the input and output voltages. Thus, the input resistance at constant duty cycle varies with the input-to-output voltage ratio, degrading the PFC performance. In contrast, the DCM operated buck-boost PFC converter shown in Figure 3.1(c) and its isolated version, i.e., flyback PFC converter, are suitable for low power applications with an automatic PFC function and a simple duty cycle control, eliminating the need for line current sensors.

The PFC converters shown in Figures 3.1(b), 3.1(c), 3.1(d) and 3.1(e) can be readily modified by adding an extra diode for each extra output to form multiple-

output converters. Specifically, the output of inductor L_m can be regarded as a PCS which is connected to each output using a diode as a passive switch. The proportion of power flowing to each output can be controlled with one or more active switch(es), as explained in Section 3.3.

At the input side, the line voltage v_{in} and power factor corrected current i_{in} with line angular frequency ω_l are

$$v_{\text{in}} = V_m \sin \omega_l t, \text{ and} \tag{3.1}$$

$$i_{\text{in}} = I_m \sin \omega_l t, \tag{3.2}$$

The output power of PCS is given by

$$\begin{aligned} p_{\text{PCS}} &= \eta_1 p_{\text{in}} \approx p_{\text{in}} = v_{\text{in}} i_{\text{in}} \\ &= \frac{1}{2} V_m I_m - \frac{1}{2} V_m I_m \cos 2\omega_l t, \end{aligned} \tag{3.3}$$

which is simply a summation of a DC power p_{dc} and a second-order AC power $p_{2\omega_l}$ given by

$$p_{\text{dc}} = \frac{1}{2} V_m I_m, \text{ and} \tag{3.4}$$

$$p_{2\omega_l} = -\frac{1}{2} V_m I_m \cos 2\omega_l t. \tag{3.5}$$

The 2-PS LED driver can be implemented with a single output PCS by using one of the topologies given in Figures 3.1(b), 3.1(c), 3.1(d) and 3.1(e), and its block diagram can be redrawn as shown in Figure 3.2(a). Here, the output power p_{PCS} from PCS flows to C_s via Path 1. The downstream DC-DC converter is controlled to deliver p_{dc} via Path 2. Capacitor C_s stores power when $p_{\text{PCS}} > p_{\text{dc}}$ and releases power when $p_{\text{PCS}} < p_{\text{dc}}$. The power waveforms are given in Figure 3.2(b). Obviously, the power is processed twice.

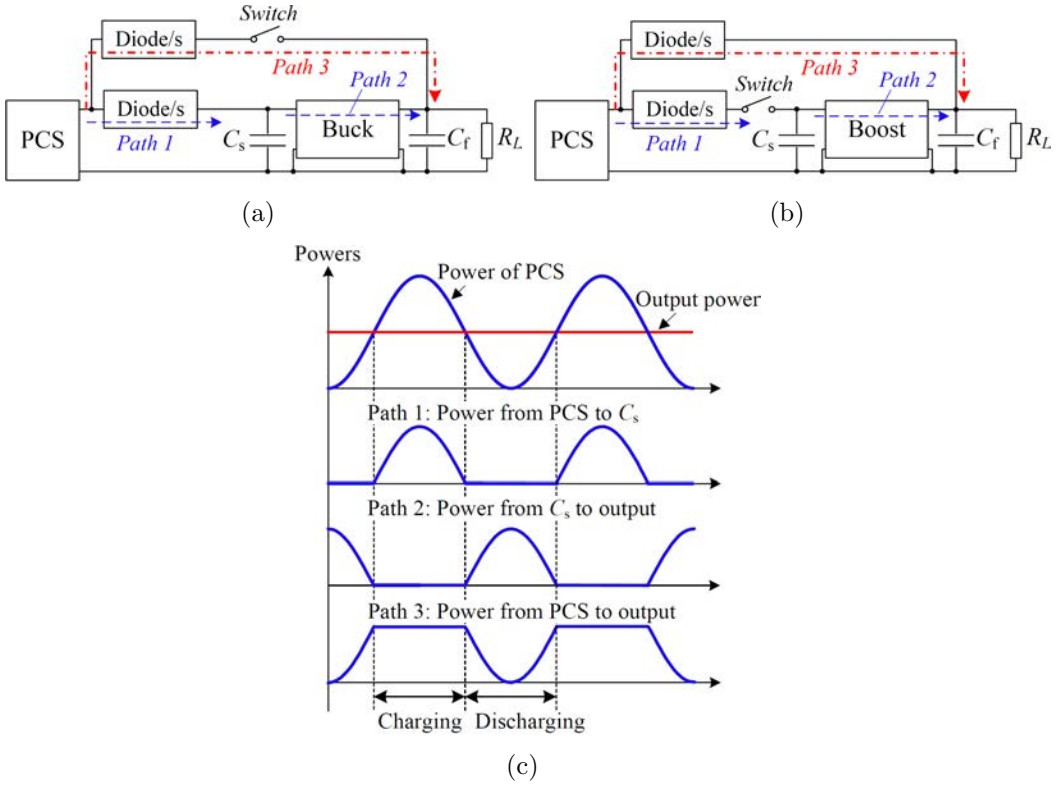


Figure 3.3: Configuration of the n_χ-PS LED driver: (a) low output voltage design, (b) high output voltage design, and (c) desired power flow waveforms within a line period.

To minimize repeated power processing, the n_χ-PS design is implemented using a two-output PCS. The additional output provides a direct power flow path from PCS to the LED load. Two typical designs are presented in Figures 3.3(a) and 3.3(b). For the design of Figure 3.3(a), a smaller capacitance C_s can be used due to its higher operating voltage. Furthermore, an extra power flow switch is connected between one output terminal of the PCS and the lower-voltage output terminal, i.e. C_f in Figure 3.3(a) and C_s in Figure 3.3(b). Figure 3.3(c) shows the desired power flows paths 1, 2 and 3. Comparing power flows shown in Figures 3.2(b) and 3.3(c), it can be observed that $k_1 = 1 - \frac{1}{\pi}$ and only $\frac{1}{\pi}$ of the total power is processed by the unidirectional DC-DC converter. This saves the cost of thermal management and reduces the power rating of devices.

Using the block diagrams shown in Figure 3.3, two families of the n_χ-PS design

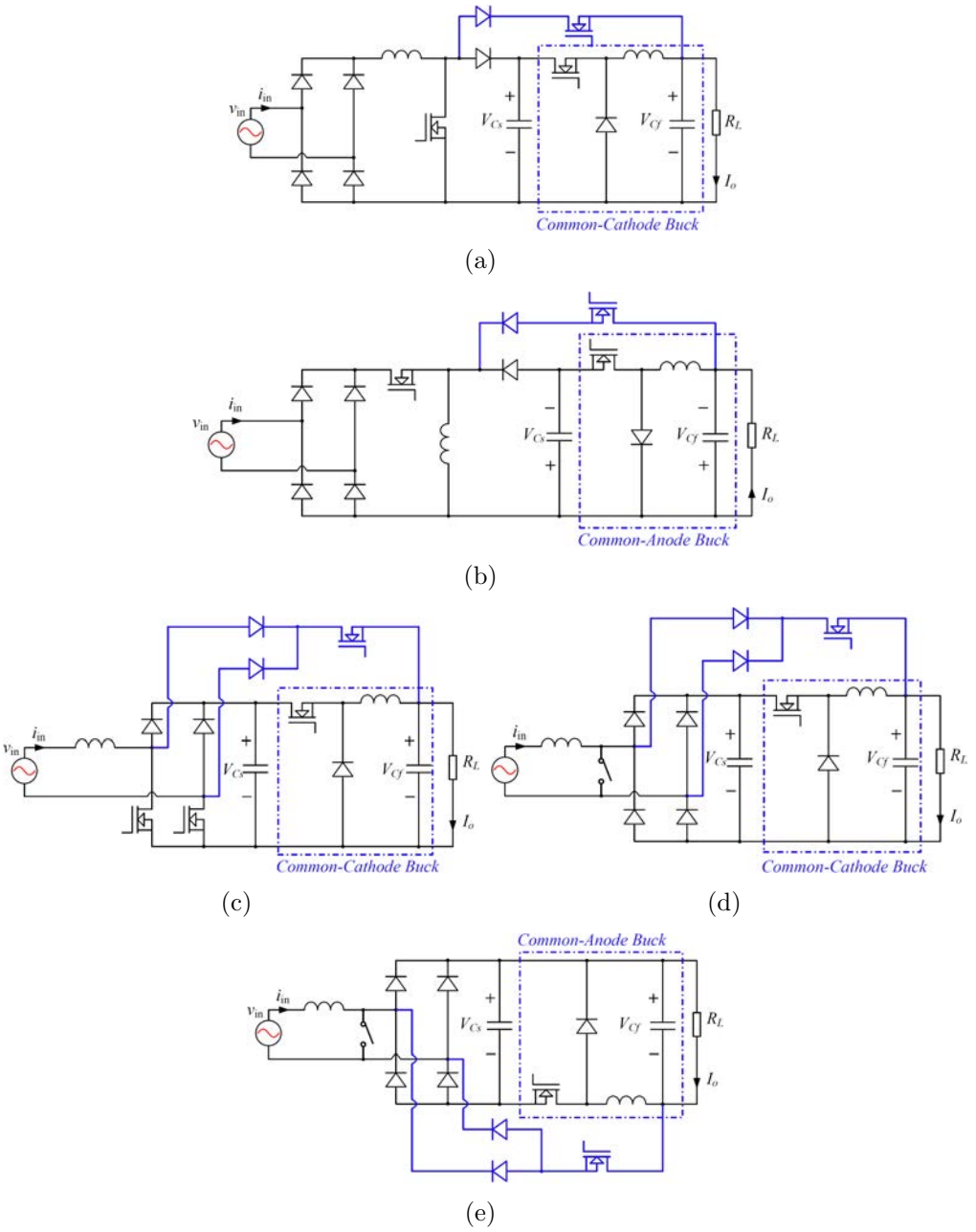


Figure 3.4: Family of low voltage output n_χ-PS converters. (a) Boost PFC and common-cathode buck cascaded converter. (b) Buck-boost PFC and common-anode buck cascaded converter. (c) Bridgeless boost PFC and common-cathode buck converter. (d) Bridgeless four-quadrant switch PFC and common-cathode buck converter. (e) Bridgeless four-quadrant switch PFC and common-anode buck converter.

can be synthesized as shown in Figure 3.4 for low output voltage applications and in Figure 3.5 for high output voltage applications. The structure shown in Figure 3.4(a) has been used in electric vehicle charging as a three-level quasi-two-

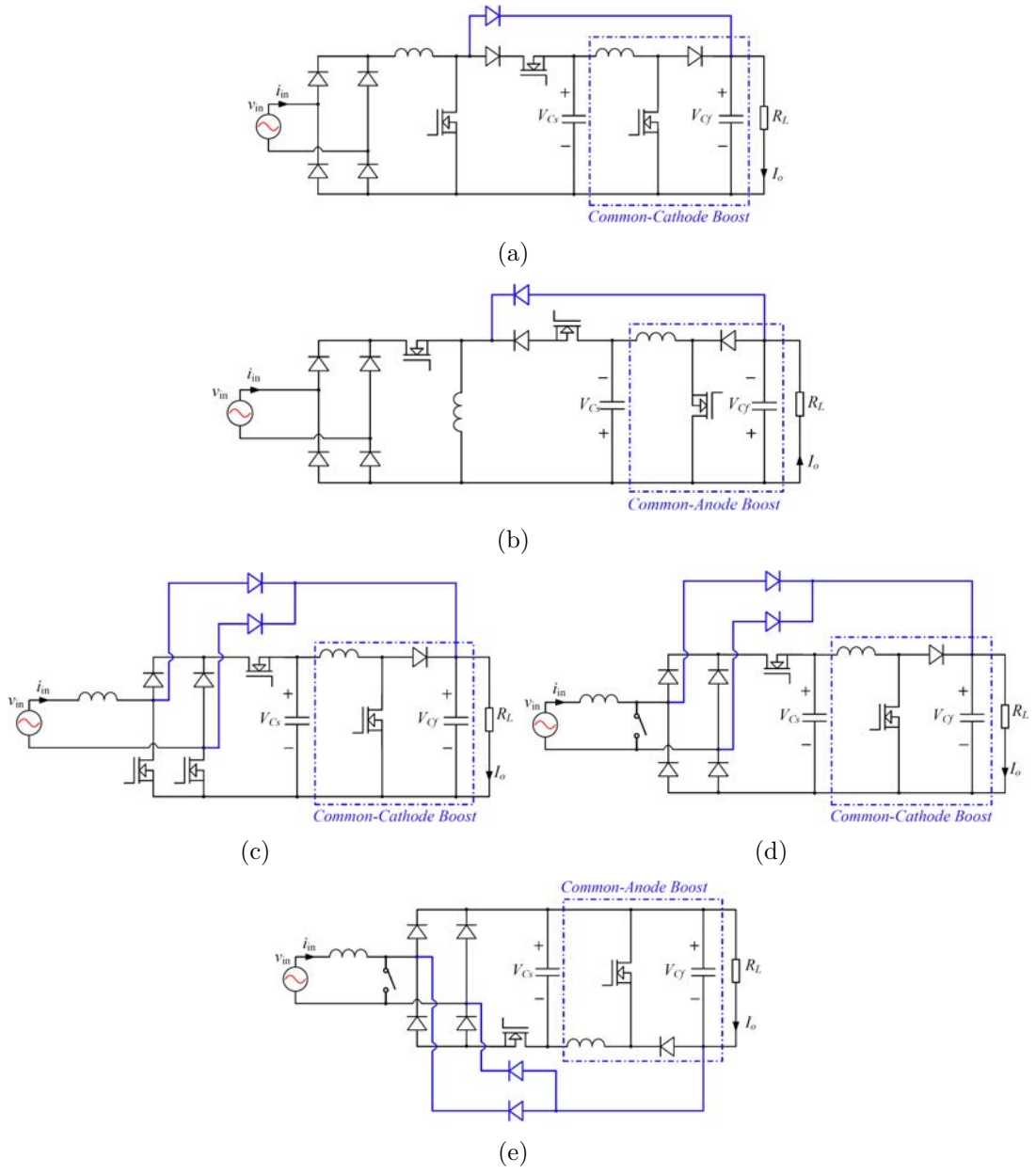


Figure 3.5: Family of high voltage output n_χ-PS converters. (a) Boost PFC and common-cathode buck cascaded converter. (b) Buck-boost PFC and common-anode buck cascaded converter. (c) Bridgeless boost PFC and common-cathode buck converter. (d) Bridgeless four-quadrant switch PFC and common-cathode buck converter. (e) Bridgeless four-quadrant switch PFC and common-anode buck converter.

stage single-phase PFC converter [32].

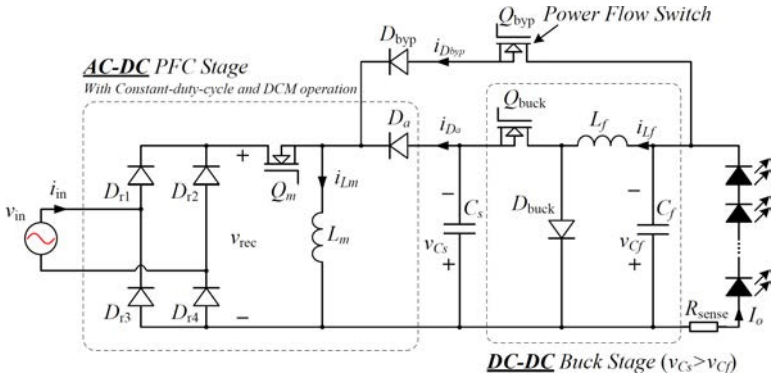


Figure 3.6: Proposed non-isolated n_χ-PS LED driver.

3.3 Implementation of n_χ-PS LED Driver

This section describes the implementation of a low-power and small-charge-storage-capacitance LED driver based on the circuit shown in Figure 3.4(b). The details of this non-isolated LED drivers are shown in Figure 3.6. The PFC stage is a buck-boost converter which provides two outputs. The averaged voltage of the storage capacitor C_s from one of its directly connected output is fed back for control [26]. Inductor L_m, operating in DCM, provides a native input unity power factor as long as the voltage loop is slow enough to keep the duty cycle of the main switch Q_m constant within a line period. The second stage is a common-anode buck converter with a small current filtering capacitor C_f. The inductor L_f of this buck converter also operates in DCM such that diode D_{buck} is zero-current turned off. The output current sensed by a small resistor R_{sense} will be regulated by the combined action of Q_{byp} and Q_{buck} to fullfil the desired COC requirement and the power flow condition to be described in the next subsection.

Comparing with a similar topological implementation reported in Valipour *et al.* [28], although one less switch is used, it has less design freedom and cannot be programmed to achieve the desired power flow. On the other hand, the design of Chen and Hui [26] has a higher power density thanks to the use of a single integrated transformer. However, the control of power flow is complicated due to

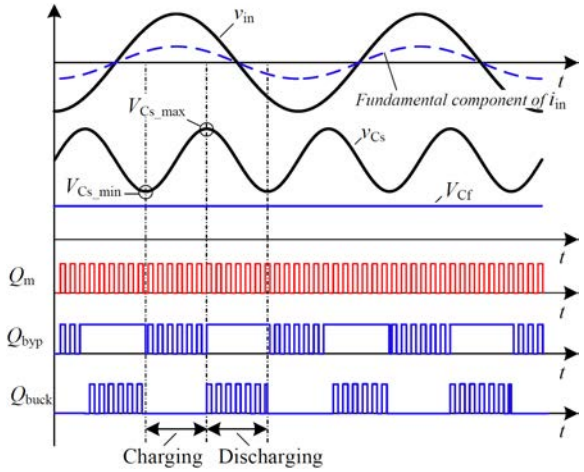
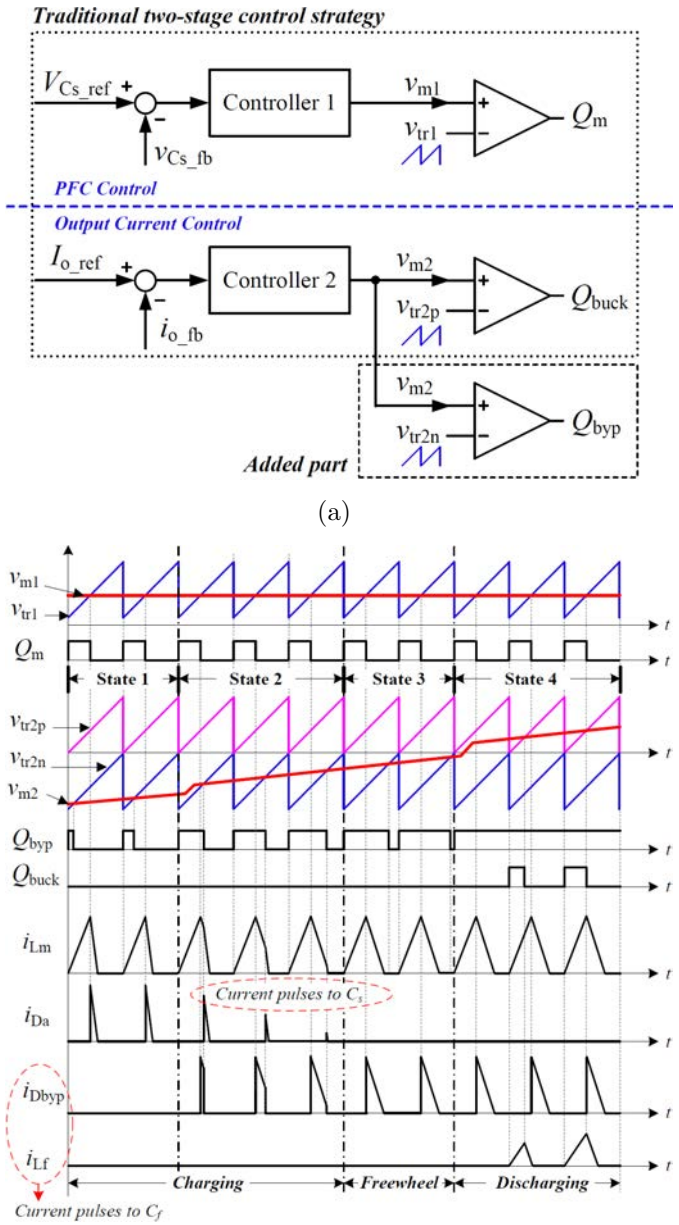


Figure 3.7: Operating waveforms of proposed n_χ-PS LED driver.

the time-multiplex control of two pairs of switches for charging and discharging of the mutual inductor of the flyback transformer and the need for maintaining DCM operation simultaneously. Furthermore, the control adopted in [26] for distinguishing the operating modes during charging and discharging of the charge storage capacitor as shown in Figures 3.3(c) or 3.7 is achieved by comparing the rectified input line voltage and its averaged value. The precision of this approach depends on the assumption of lossless power conversion and requires sensing the input line voltage.

3.3.1 Control Strategy With Carrier Disposition

A novel control strategy based on carrier disposition is proposed here as shown in Figure 3.8(a). Compared with the control strategy of the traditional two-stage LED driver, only one extra comparator for Q_{byp} is needed. In this modulation scheme, a single sawtooth carrier is added to three independent DC biased voltages to form three falling-edge synchronized sawtooth waveforms, i.e., v_{tr1}, v_{tr2p} and v_{tr2n}. The modulation signal v_{m1} shown in Figure 3.8(a) is compared with v_{tr1} to generate the driving signal for switch Q_m. Switches Q_{buck} and Q_{byp} are controlled in a coordinated manner. For simplicity, the lowest value of v_{tr2p} and



(a)

(b)

Figure 3.8: (a) Proposed control strategy based on carrier disposition; (b) waveforms.

the highest value of v_{tr2n} are fixed at 0 V. When v_{m2} is negative, it is compared with v_{tr2n} to generate the on-off driving signal for Q_{byp}, and at the same time Q_{buck} stays open. When v_{m2} is positive, it is compared with v_{tr2p} to generate the on-off driving signal for Q_{buck}, and at the same time Q_{byp} is kept closed.

Four possible operating states can be identified depending on the voltage level

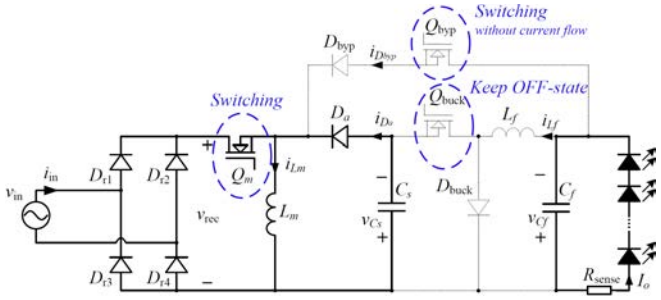


Figure 3.9: Operating states of LED driver within a line cycle: (a) State 1, (b) state 2, (c) state 3, and (d) state 4.

of v_{m2} as shown in Figure 3.8(b):

1) State 1, as shown in Figure 3.9(a): The duty cycle of Q_{byp} is lower than that of Q_m. The combined switch of D_{byp} and Q_{byp} is masked by D_{byp} which is

off. The energy from PCS is fully stored in C_s.

2) State 2, as shown in Figure 3.9(b): The duty cycle of Q_{byp} is larger than that of Q_m, and Q_{byp} is turned off before i_{Lm} falls to zero. The current from PCS first flows to the output load and later to the charge storage capacitor. The time duration of the current pulse from PCS to C_s decreases as v_{m2} increases.

3) State 3, as shown in Figure 3.9(c): The value of v_{m2} is still negative. Q_{byp} is turned off after i_{Lm} falls to zero. The time duration of the current pulse from PCS to C_s decreases to zero upon further increase in v_{m2}.

4) State 4, as shown in Figure 3.9(d): The value of v_{m2} becomes positive. Q_{byp} is kept closed to maximize the power transfer from PCS directly to the load. Meanwhile, any increase in v_{m2} will increase the duty cycle of Q_{buck}, which delivers more power from C_s to the output load.

As observed from Figure 3.8(b), the total output current ($i_{D_{byp}}$ and i_{L_f}) increases with increasing v_{m2} in states 2 and 4, and is kept unchanged in states 1 and 3. As a result, the output current can be controlled using the output v_{m2} of controller 2 and the error current ($I_{o\_\text{ref}} - i_{o\_\text{fb}}$). As the output current does not change in states 1 and 3, when a fast controller is used, the output transient response can be analyzed without consideration of states 1 and 3. Detailed analysis of states 2 and 4 will be performed in the following sub-sections.

3.3.2 Analysis of Charging Operation in State 2

In this subsection, we consider the charging operation of the buck-boost PFC converter. With a given input power P_{in}, the steady-state duty cycle of Q_m is given by

$$D_m = \frac{2}{V_m}\sqrt{P_{\text{in}} L_m f_s}, \tag{3.6}$$

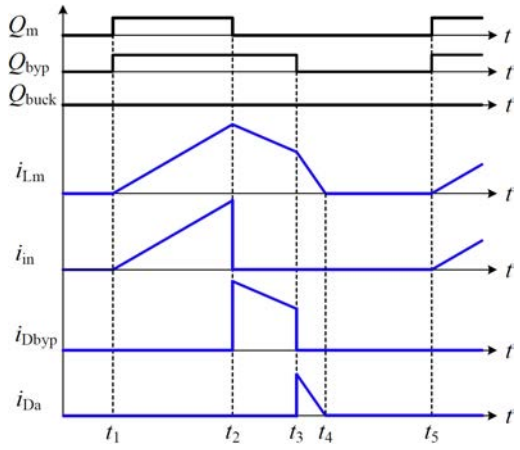


Figure 3.10: Switching waveforms within a switching period of State 2

where V_m is the amplitude of the line voltage in (3.1) and f_s is the switching frequency. The peak value of the PFC inductor current i_{L_m} is a function of time given by

$$i_{pk\_L_m} = \frac{D_m}{L_m f_s} |v_{\text{in}}| = \frac{V_m D_m}{L_m f_s} |\sin \omega_l t| \,. \tag{3.7}$$

The time-domain analysis of the charging operation is presented in Figure 3.11. The period between t_1 and t_5 in Figure 3.10 is divided into four sub-intervals.

1) $[t_1, t_2]$ *as shown in Figure 3.11(a):* Q_m and Q_{byp} are turned on at $t = t_1$. Inductor current i_{L_m} charges up linearly by the line voltage and attains a peak value $i_{pk\_L_m}$ at $t = t_2$ according to (3.7). The output paths are blocked by D_{byp} and D_a even though Q_{byp} is turned on.

2) $[t_2, t_3]$ *as shown in Figure 3.11(b):* Q_m is turned off at $t = t_2$. As $v_{C_f} < v_{C_s}$, D_{byp} is on and D_a is off. The current of i_{L_m} will flow to output capacitor C_f through D_{byp} and Q_{byp}. Current i_{L_m} decreases at a rate of $\frac{V_{C_f}}{L_m}$. The transferred

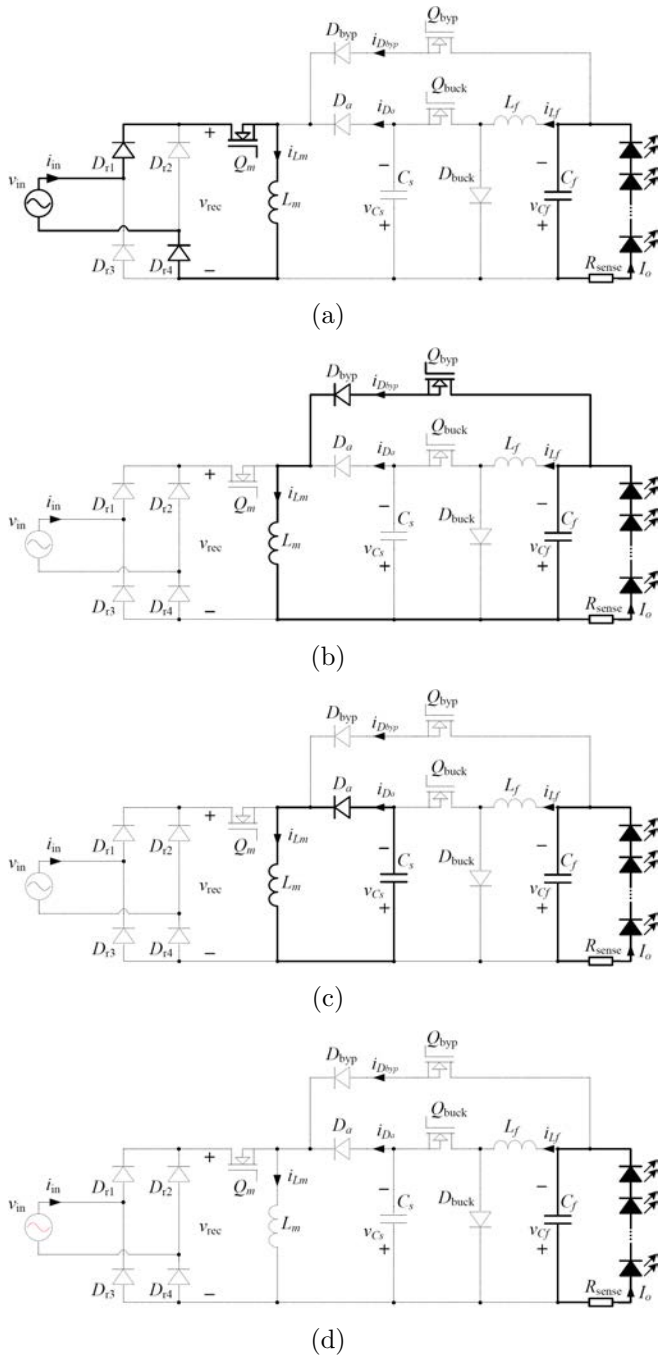


Figure 3.11: Current flow of State 2 in sub-intervals within (a) $[t_1, t_2]$, (b) $[t_2, t_3]$, (c) $[t_3, t_4]$, and (d) $[t_4, t_5]$.

energy to the output can be calculated as

$$\begin{aligned} e_{byp\_\text{charge}} &= \frac{1}{2} L_m \Delta i_{L_m}^2 \\ &= \frac{V_{C_f}}{f_s} \left(D_{byp} - D_m\right) i_{pk\_L_m} \\ &\quad - \frac{V_{C_f}^2}{2 L_m f_s^2} (D_{byp} - D_m)^2. \end{aligned} \tag{3.8}$$

3) $[t_3, t_4]$ *as shown in Figure 3.11(c):* Switch Q_{byp} is turned off at $t = t_3$. Current i_{L_m} flows to C_s through D_a and decreases at a rate of $\frac{V_{C_s}}{L_m}$. Only C_f provides energy for the load.

4) $[t_4, t_5]$ *as shown in Figure 3.11(d)*: Current i_{L_m} falls to zero at $t = t_4$ and stay there until t_5. Diodes D_a and D_{byp} are off during this interval.

Only during the interval of $[t_2, t_3]$, energy is transferred from inductor L_m to output. Within a switching period, the energy consumed by the load can be calculated as

$$e_{ld} = \frac{P_o}{f_s}, \tag{3.9}$$

and the peak energy of inductor L_m at $t = t_2$ can be calculated with (3.7) as

$$e_{pk\_L_m} = \frac{1}{2} L_m i_{pk\_L_m}^2 = \frac{V_m^2 D_m^2}{2 L_m f_s^2} \sin^2 \omega_l t. \tag{3.10}$$

Substituting (3.6) into (3.10), it has

$$e_{pk\_L_m} = \frac{2P_{\text{in}}}{f_s} \sin^2 \omega_l t = \frac{P_{\text{in}}}{f_s} - \frac{P_{\text{in}}}{f_s} \cos 2\omega_l t. \tag{3.11}$$

As long as

$$e_{pk\_L_m} \geq e_{ld}, \tag{3.12}$$

the inductor can provide sufficient energy for load consumption, and can charge the capacitor C_s with the excess energy in State 2. Condition (3.12) is also applicable during transient of load switching, i.e., $P_{\text{in}} \neq \frac{P_o}{\eta}$, where η is the measured efficiency at steady state.

3.3.3 Analysis of Discharging Operation in State 4

When $e_{pk\_L_m} < e_{ld}$, the circuit is in state 4, as shown in Figure 3.9(d), discharging the energy from capacitor C_s to the load. The buck-boost PFC converter and the DCM buck converter are delivering power to the load in parallel.

The energy provided by the buck-boost PFC converter, $e_{pk\_L_m}$, can be calculated from (3.10). Within a switching period, the energy difference can be calculated as

$$e_{\text{gap}} = e_{ld} - e_{pk\_L_m}, \tag{3.13}$$

and the energy provided by the DCM buck converter is given by

$$e_{\text{buck}} = \frac{V_{C_s} - V_{C_f}}{2L_f f_s^2} V_{C_s} D_{\text{buck}}^2. \tag{3.14}$$

Consequently, using the proposed control with D_{buck} as the control variable, the energy difference can be nullified , i.e., $e_{\text{buck}} = e_{\text{gap}}$.

3.3.4 Loss Analysis

As introduced in Section 3.2, the first stage buck-boost circuit is modeled as a pulsing current source (PCS). The PCS can be designed with one more output by using an extra switch Q_{byp} which can be turned on during the dead-time of the PCS. Thus, zero current turn-on can be achieved. The turn-on resistance of the switch Q_{byp} is small which incurs a penalty of a small conduction loss. However, the switch capacitive charge is completely dissipated during turn-on which should be the main loss during turn-on. The switch Q_{byp} could be turned off sharply to have zero voltage turn-off.

On the other hand, for the DC-DC buck converter, the switching loss can be reduced due to the reduced current stress and reduce switching operations.

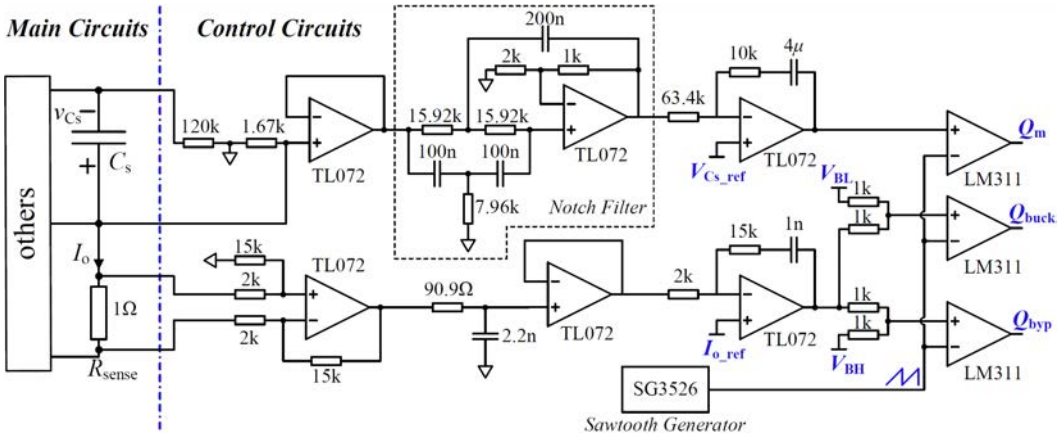


Figure 3.12: Detailed circuit diagram of the control circuit.

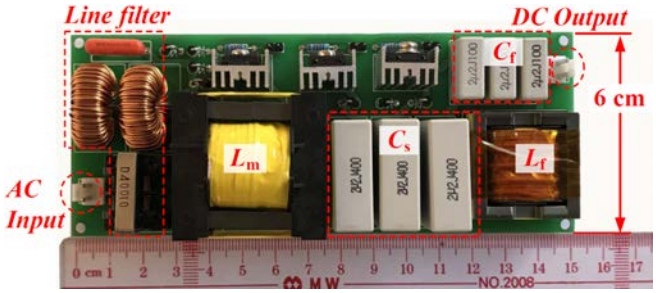


Figure 3.13: Photograph of main circuit board.

Meanwhile, the core loss of filtering inductor L_f can also be reduced.

3.4 Verification

An experimental prototype is constructed according to the control circuit given in Figure 3.12 and the parameter values given in Table 3.1. A photograph of the main circuit board is shown in Figure 3.13.

Figure 3.14(a) shows the measured input and output waveforms of the converter. High input power factor and constant output dc driving current are achieved. Figure 3.14(b) shows the measured control waveforms of the converter, demonstrating smooth transition of power splitting using the carrier disposition technique. Figures 3.14(c) and (d) show the enlarged waveforms during state 2 of charging and state 4 of discharging of C_f respectively. Figure 3.15 shows the

Table 3.1: Main parameters of the proposed LED driver

Parameters	Values
Grid Input Voltage v_{in}	110±20% VAC
Grid Frequency f	50 Hz
Input Inductor $L_{\text{in}}{}^{*}$	2×470 μH
Input Film Capacitor $C_{\text{in}}{}^{*}$	100 nF / 400V
Switching Frequency f_s	100 kHz
Inductor in PFC stage L_m	200 μH
Storage Capacitor C_s	3×2.2 μF / 400 V
Filtering Inductor in Buck stage L_f	50 μH
Filtering Film Capacitor in Buck stage C_f	3×2.2 μF / 100 V
Maximum Power Capacity $P_{o\,\max}$	16 W
Diodes $D_{r1} - D_{r4}$, D_{byp}, D_a, D_{buck}	MUR160G
MOSFETs Q_a, Q_{byp}, Q_{buck}	IPA60R385CP
Measured LED VI points	85.1 V @ 190 mA
	82.0 V @ 110 mA
	78.0 V @ 30 mA

Key: $*$ L_{in} and C_{in} constitute an input LC filter

portion of power directly delivered to the load that k_1 is close to the theoretical value of $1 - \frac{1}{\pi} \approx 0.682$.

Measured power factors at various output currents and input voltages are shown in Figure 3.16. At $V_{\text{in}} = 110$ V, harmonic contents of the grid current are shown in Figures 3.17(a) and 3.17(b) for $I_o = 50$ mA and $I_o = 160$ mA, respectively. The measured efficiencies of the proposed converter and a traditional two-stage implementation (by removing diode D_{byp} and switch Q_{byp} shown in Figure 3.6) are given in Figure 3.18. A loss breakdown of the proposed LED driver and its 2-stage counterpart is given in Table 3.2.

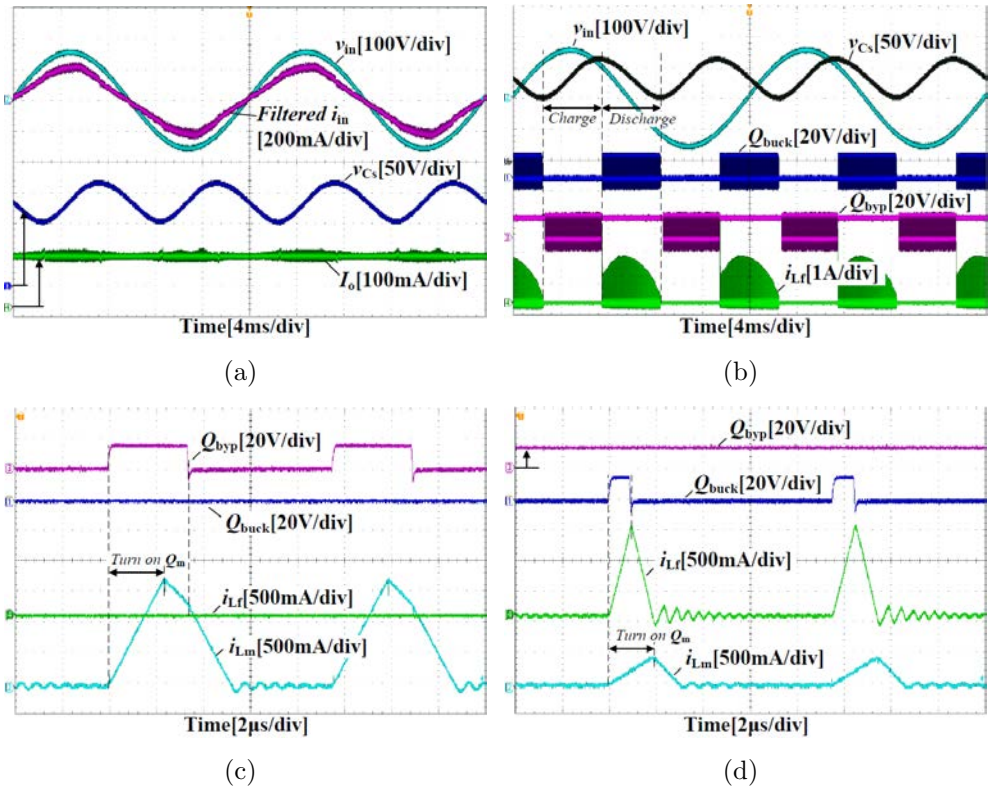


Figure 3.14: Key experimental waveforms of the LED driver.

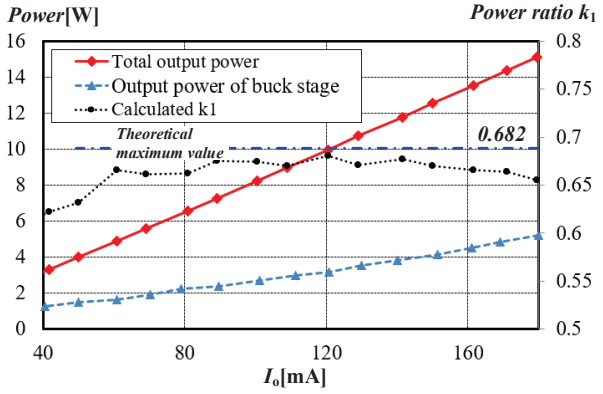


Figure 3.15: Experimental measurement of k_1, which is obtained from the ratio of power of the buck converter versus the total power outputting to the LED string.

3.5 Summary

In this chapter, an LED off-line driver is designed based on a minimum power processing structure. The LED driver is chosen from a family of converters having input power factor correction and output controlled dc constant current. The

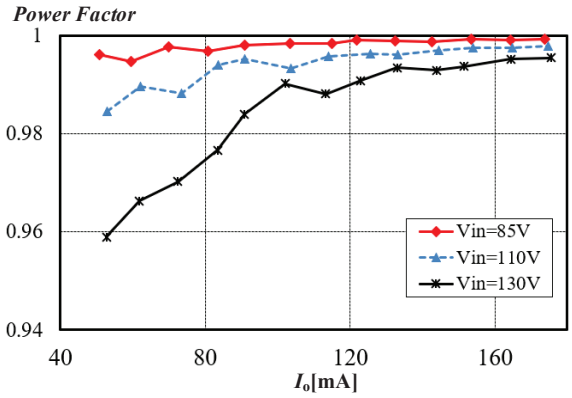


Figure 3.16: Measured power factor at various output currents.

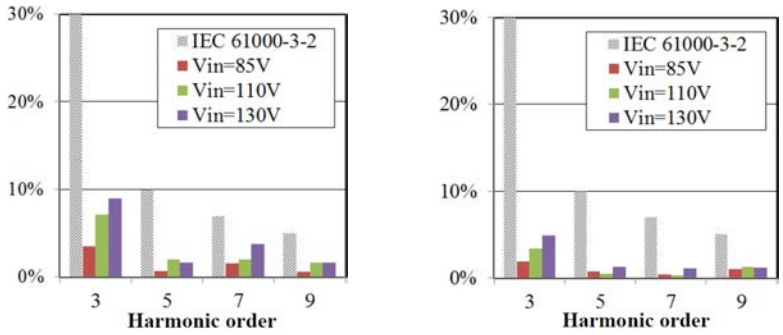


Figure 3.17: IEC 61000-3-2 Class C limits and input harmonic contents at (a) $I_o = 50$ mA and (b) at $I_o = 160$ mA .

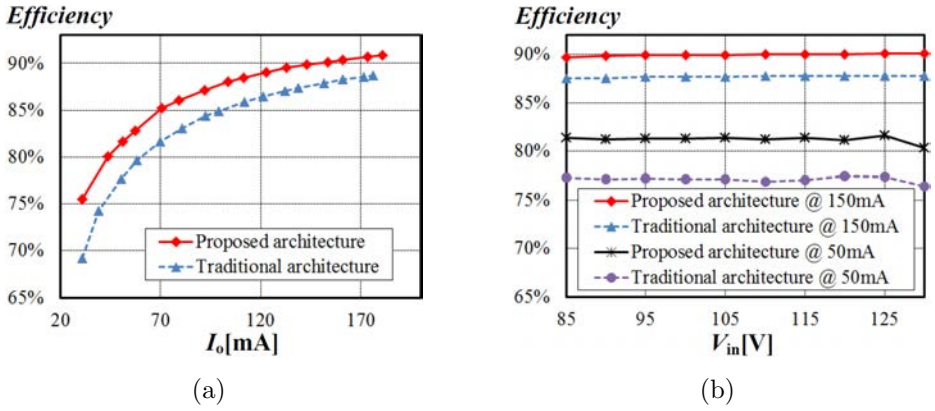


Figure 3.18: Comparison of efficiency of the LED driver and the traditional two-stage converter at (a) $V_{\text{in}} = 110$ V and (b) $I_o = 50$ mA and 150 mA

.

LED driver is designed with a control using the technique of carrier disposition for seamless splitting of the input power into two paths. An optimal portion of

Table 3.2: Loss Breakdown @ $V_{\text{in}} = 110$ V and $I_o = 150$ mA

Measured Prototype		Proposed driver	2-stage counterpart
Overall Efficiency		89.69%	87.34%
Overall Loss		1.46 W	1.83 W
AC-DC Stage	Efficiency	90.98%	90.10%
	Loss	1.27 W	1.43 W
	Loss weighting	86.99%	78.14%
DC-DC Buck Stage	Efficiency#	95.72%	96.93%
	Loss	0.19 W	0.40 W
	Loss weighting	13.01%	21.86%

Key: # defined as $\frac{P_{o\_\text{Buck}}}{P_{\text{in\_Buck}}}$.

the input power goes to the dc output and the rest to a storage buffering path connected to the dc output. Since the storage capacitor is operated at a much higher voltage than the output voltage, a small non-electrolytic capacitor can be used. The design of the LED driver has been verified experimentally.

Chapter 4

Multiple-Output LED Drivers With Single Inductor

4.1 Introduction

In order to lower the system cost and reduce the form factor, single-inductor multiple-output (SIMO) converters are intensely developed for on-chip DC-DC converters and off-line light emitting diode (LED) drivers. However, existing single-stage PFC SIMO LED drivers are usually designed with electrolytic capacitors, leading to a short life span and limited range of operation temperature. In this chapter, based on a single dual-winding coupled inductor, a SIMO LED driver with PFC function is proposed without the requirement of electrolytic capacitors, where a small storage capacitance is used to actively decouple the ac and dc input powers. Compared with previous works, the proposed PFC SIMO LED driver has some additional benefits, including a smaller line filter, multiple output currents without double line frequency ripple and a faster output regulation. With appropriate control strategy, an independent output regulation can be achieved for each output channel. Meanwhile, the energy flow of the converter is optimized with an inductor current programming technique to improve the

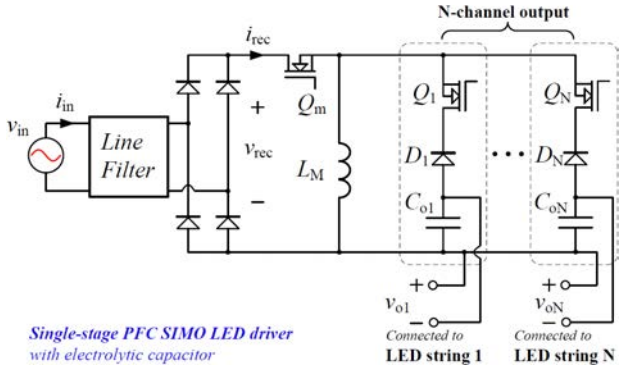


Figure 4.1: Single-stage PFC SIMO LED driver with electrolytic capacitor [45].

converter efficiency. Finally, the proposed electrolytic capacitor-less PFC SIMO LED driver is developed, designed, tested and compared with a single-stage SIMO design without active power decoupling.

4.2 Circuit Development

A single-stage PFC SIMO converter is derived from the buck-boost converter, as shown in Figure 4.1, where a special example of dual-output converter was investigated in [45]. In this section, an electrolytic capacitor-less PFC SIMO LED driver, which is also based on the buck-boost converter, will be derived as shown in Figure 4.2. The circuit development is explained as follows.

Step 1: We begin with a simple 2-stage structure of an LED driver which can be designed to achieve the PFC function and N-independent-current outputs. The front-stage buck-boost converter regulates i_{in} to achieve near unity power factor. N load-stage buck-boost converters acquire power from C_s and regulate the LED driving currents without low-frequency current ripples. Output capacitors C_{oi}, $i = 1 \cdots N$, are mainly designed for the filtering of switching frequency current ripples, and thus can normally be small. Electrolytic capacitors are usually adopted for C_s for a low cost design. However, for designs that require longer life span and wider ambient temperature operating range, film

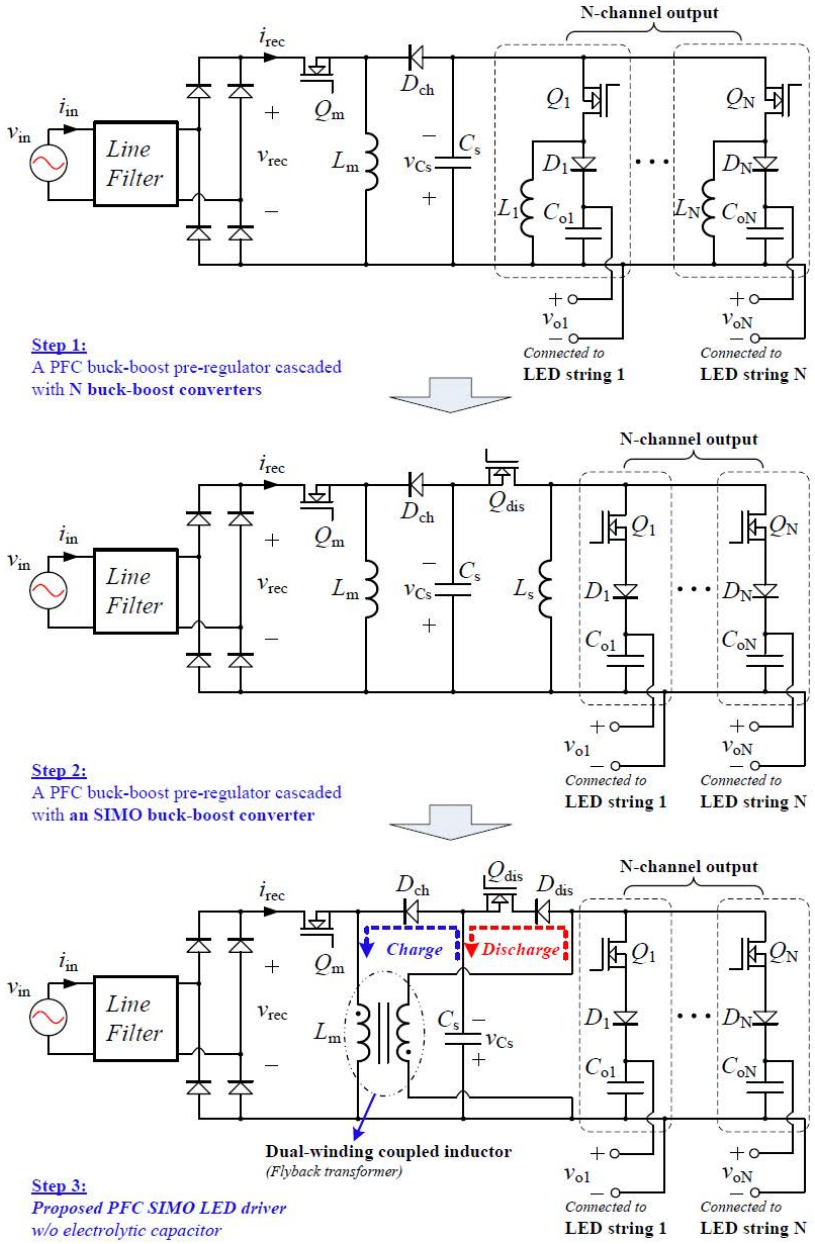


Figure 4.2: Topological derivation of the proposed PFC SIMO LED driver without electrolytic capacitor.

capacitors with small capacitance can be utilized and designed at a higher DC voltage level. The corresponding higher voltage ripple at $2f_l$ frequency is rejected by the regulation from the load-stage converters. In this structure, all buck-boost converters are operating independently. Thus, it provides the maximum freedom for design and control.

Step 2: In order to reduce the number of inductors, the N-load-stage converters can be replaced by a single SIMO buck-boost converter. Thus, $N-1$ inductors can be saved. Inductor L_s is shared among N-outputs with the help of an additional switch Q_{dis}. Time-multiplexing can be a control solution for the independent regulations of multiple outputs. Using inductor DCM operation, channel selection switches $Q_{1,\cdots,N}$ cooperating with Q_{dis}, transfer energy from C_s to L_s and distribute energy to each output channel in turn. Consequently, the two-stage converter comprises an input PFC pre-regulator cascaded with a SIMO LED driver and a DC-link capacitor for effective ripple power filtering. The system needs two independent inductors and power is processed twice.

Step 3: A PFC SIMO LED driver with active ripple power decoupling is derived. The two independent inductors L_m and L_s in the previous step are tightly coupled with a near unity coupling coefficient, forming a dual-winding coupled inductor or flyback-type transformer. In addition to a reduction of one magnetic core to save cost and space, the number of power-processing stage can be reduced to two or less [7, 50]. The implementation of active ripple power decoupling will enable designs without electrolytic capacitor. The dual-winding inductor L_m and the additional diode D_{dis} can be used to control the charging and discharging of capacitor C_s for a complete active ripple power decoupling, which will be explained in Section 4.4.

4.3 Design Guidelines

Time multiplexing can be applied to the proposed PFC SIMO LED driver introduced in Section 4.2 to accomplish the required functions of input power factor correction and output independent control. In the following subsections, the design considerations of PFC function, multiple outputs, ripple power balancing, and energy flow optimization will be discussed in Sections 4.3.1, 4.3.2, 4.3.3 and

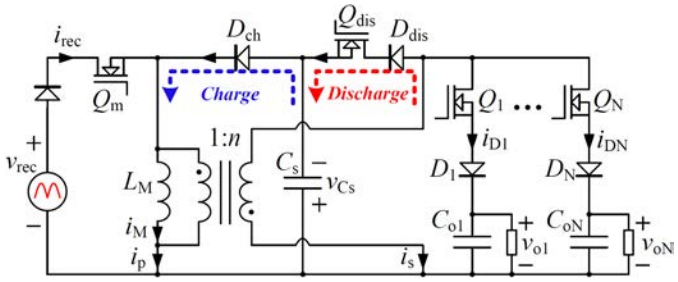


Figure 4.3: A simplified circuit model without leakage inductance.

4.3.4, respectively.

For simplicity, the dual-winding coupled inductor L_m in Figure 4.2 is represented by a transformer model which has a magnetizing inductor L_M and an ideal transformer with turns ratio $1 : n$, where the leakage inductance is ignored because of tight coupling. Besides, the grid input, line filter, and diode bridge are simplified to a rectified voltage source v_{rec} connected with a single diode in series. LED loads are all replaced by their equivalent load resistors. The simplified circuit model is given in Figure 4.3.

4.3.1 PFC Function Without Time-multiplexing

In the single-stage design shown in Figure 4.1, such as the single-inductor dual-output LED driver with electrolytic capacitor filtering [45], power factor correction and independent current output are implemented by time-multiplexing the inductor current at boundary conduction mode (BRM) operation with variable switching frequency. Such technique can be implemented for the design shown in Figure 4.3, but the power factor has to be sacrificed. Consequently, to have an unity power factor, the single inductor L_M operating at DCM with constant switching frequency can be shared by the N buck-boost LED drivers, each with an independent duty-cycle at a period of $\frac{N}{f_s}$, where f_s is the switching frequency of Q_m. Example waveforms for dual outputs are shown in Figure 4.4.

However, this implementation poses challenge to the design of the line filter.

Though the main switch Q_m is switched at f_s, due to time-multiplexing, the line filter has to remove the grid current harmonics at a much lower frequency of $\frac{f_s}{N}$. With time-multiplexing, the buck-type multiple-output PFC converter in [46] may have similar implementation issues.

An input LC line filter can designed with L_f and C_f. With reference to [48] and [49], given a tolerable phase shift angle of θ (normally, $\theta = 1^\circ$) of the filtered voltage, the maximum allowable C_f can be calculated as

$$C_{f\_\max} = \frac{I_{m\_\max} \tan\theta}{\omega_l V_m}, \tag{4.1}$$

where $\omega_l = 2\pi f_l$ is the grid angular frequency, V_m is the magnitude of v_{in} and $I_{m\_\max}$ is the maximum magnitude of i_{in}. The corresponding L_f is given by

$$L_f = \frac{1}{4\pi^2 f_c^2 C_f}, \tag{4.2}$$

where f_c is the cutoff frequency of the LC filter.

As discussed previously, for N-multiplexed outputs the cutoff frequency f_c in (4.2) should be reduced to $\frac{f_c}{N}$. Hence, L_f has to be increased by a factor of N^2, which increases the size and cost of the line filter.

In this thesis, due to an extra freedom brought by the intermediate storage, natural PFC function of the AC-DC conversion can be designed by using a constant duty cycle for the DCM operating L_M within a grid period without using time multiplexing, as shown in Figure 4.4. Time-domain analysis for the independent control of output current for individual LED channels will be given in Section 4.4.

For simplicity, the small phase shift brought by the line filter and losses are

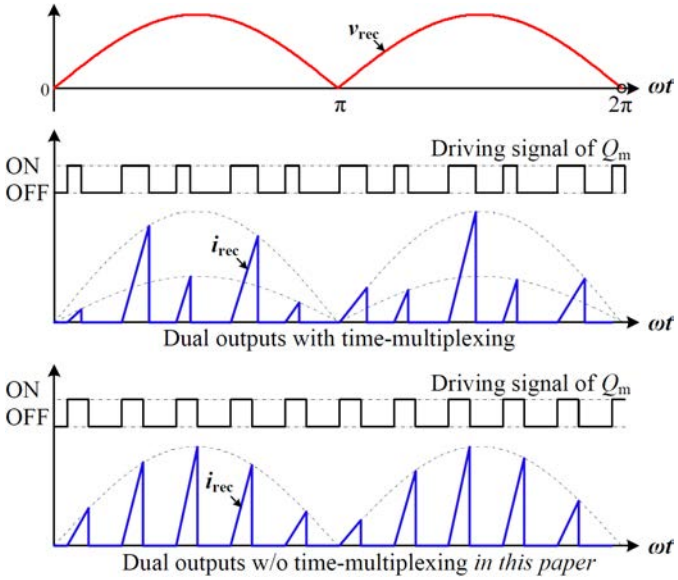


Figure 4.4: Comparison of PFC function with and without time-multiplexing in a dual-output LED driver.

ignored. The rectified input voltage v_{rec} shown in Figure 4.3 can be written as

$$v_{\text{rec}}(t) = \left|v_{C_f}(t)\right| = \left|v_{\text{in}}(t)\right| = V_m \left|\sin \omega_l t\right| . \tag{4.3}$$

Normally, we have $f_s \gg f_l$. Once Q_m is turned on, its current i_{rec} increases linearly from zero, and ends at a peak value of

$$i_{pk\_Q_m}(t) = \frac{D_m}{L_M f_s} \left|v_{\text{rec}}(t)\right| = \frac{V_m D_m}{L_M f_s} \left|\sin \omega_l t\right| , \tag{4.4}$$

where D_m is the duty cycle of driving signal. Within a switching period, the averaged current of i_{rec} can be readily calculated as

$$i_{avg\_Q_m} = \frac{1}{2} i_{pk\_Q_m} \cdot D_m = \frac{V_m D_m^2}{2 L_M f_s} \left|\sin \omega_l t\right|, \tag{4.5}$$

which is in phase with v_{rec}. From (4.5), the power factor correction can be achieved automatically as long as D_m is kept constant within a grid period. The input power of the LED driver will be regulated by D_m.

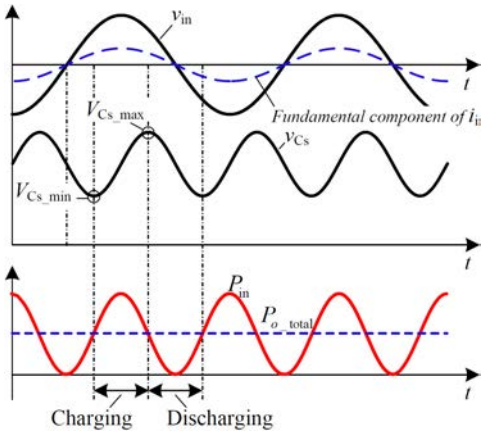


Figure 4.5: Typical waveforms for ripple power balancing.

4.3.2 Power Distribution With Time-multiplexing

In order to achieve an independent regulation, time-multiplexing of the discharging power from L_M shown in Figure 4.3 is adopted for multiple output channels. As a result, for each output channel $i \in \{1, \cdots, N\}$, output ripples at a much lower frequency $\frac{f_s}{N}$ should be filtered by capacitor C_{oi}. It should be noted that the simple output filtering capacitor circuit makes an upper limit for the number of output channels for the requirement of the LEDs.

4.3.3 Ripple Power Balancing

For the proposed LED driver, the ripple power is decoupled passively by C_s whose value has been chosen sufficiently large at the design phase.

To facilitate the analysis of the proposed PFC SIMO LED driver, i.e., the derived topology in Figure 4.2, the N-multiplexed outputs will be collectively regarded as a single output with a total power P_{o_total} averaged over a period of $\frac{N}{f_s}$, which is assumed to be much smaller than the grid period $\frac{1}{f_l}$. The power of the DCM operated L_M will be programmed for the required functions.

From (4.4) the energy E_s stored in L_M is given by

$$E_s(t) = \frac{1}{2} L_M i_{pk\_Q_m}^2(t) = \frac{V_m^2 D_m^2}{2 L_M f_s^2} \sin^2 \omega_l t. \tag{4.6}$$

Since the instantaneous input power $P_{\text{in}}(t)$ is simply $f_s E_s$, we have

$$P_{\text{in}}(t) = \frac{V_m^2 D_m^2}{2 L_M f_s} \sin^2 \omega_l t. \tag{4.7}$$

Since $\frac{N}{f_s} \ll \frac{1}{f_l}$, (4.7) is also valid for N switching periods of $\frac{N}{f_s}$. The averaged power input $\overline{P_{\text{in}}}$ is simply the average of $P_{\text{in}}(t)$ over half a grid period, i.e.,

$$\overline{P_{\text{in}}} = \frac{V_m^2 D_m^2}{4 L_M f_s}. \tag{4.8}$$

At steady state, the effective input power and output power are regulated by the PFC control, i.e.,

$$P_{o\_\text{total}} = \eta \overline{P_{\text{in}}} = \frac{V_m^2 D_m^2}{4 L_M f_s}, \tag{4.9}$$

where η is the efficiency of the LED driver. Comparing (4.7) and (4.9), the boundary of charging and discharging of C_s should occur at $\theta = \omega_l t$ when $\eta = 1$ and $P_{\text{in}}(\theta) = P_{o\_\text{total}}$, i.e.,

$$\theta = \sin^{-1}\left(\pm \frac{1}{\sqrt{2}}\right) = \frac{\pi}{4} + k\frac{\pi}{2} \tag{4.10}$$

for any integer k. Typical waveforms of ripple power balancing are given in Figure 4.5.

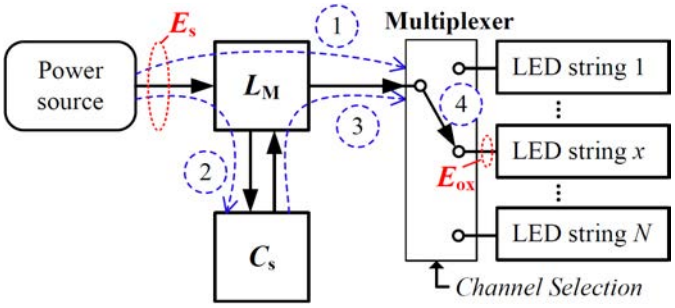


Figure 4.6: Energy flow paths.

4.3.4 Optimal Design via Energy-flow-path Analysis

For switching mode power converters, energy flows through passive components according to some preset switch configurations within a switching period. The principle of energy-flow-path analysis has been adopted to analyze the efficiency of PFC converters [7], single-output LED drivers [50] and switched-capacitor converters [21]. Similarly, for the proposed PFC SIMO LED driver, an energy-flow-path analysis will be applied to achieve minimal energy recycling.

An energy-flow-path map derived from Figure 4.3 is illustrated in Figure 4.6, where the energy E_s flows from the power source v_{rec}, through the two intermediate storage components L_M and C_s, and finally to an LED string selected by the multiplexer via Path 4. The multiplexer distributes a sequence of energy $\{E_{ox} : x = 1, 2, \cdots, N\}$ recurring at a period of $\frac{1}{f_s}$ to LED string x, and thus each LED string receives one period of energy within N switching periods $\frac{N}{f_s}$. The corresponding power P_{ox} distributed to LED string x satisfies

$$E_{ox} = \frac{N}{f_s} P_{ox}. \tag{4.11}$$

Since E_s varies slowly according to (4.6) for the PFC requirement and E_{ox} is mostly constant for flicker-free applications, their energy difference within $\frac{1}{f_s}$ should mostly be absorbed by the intermediate storage component C_s. An illustration of the energy difference using the input voltage v_{rec} within a line cycle

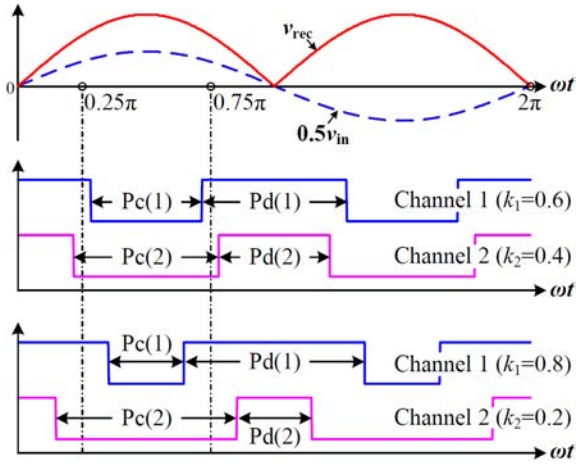


Figure 4.7: Energy-flow-path operations with respect to rectified voltage v_{rec} for $N = 2$.

is shown in Figure 4.7. At steady state with a single output of $N = 1$, the input and output energies are approximately equalized at phase angles $\theta = \frac{\pi}{4}$ and every $\frac{\pi}{2}$ apart, as given by (4.10). For $N = 2$, as illustrated in Figure 4.7, the averaged usable input energy $\eta f_l \int_{t-\frac{1}{f_l}}^{t} E_s(\tau)d\tau$ and the averaged output energy $\frac{1}{N}\sum_{x=1}^{N} E_{ox}$ are controlled to be equal at steady state. Three energy flow paths for a switching period, namely Paths 1, 2 and 3, can be identified. Path 2 charges up C_s while Path 3 discharges C_s. When designing the switching states, energy recycling should be minimized for an optimal design. Therefore, Paths 2 and 3 should not appear simultaneously within a period of $\frac{1}{f_s}$. The selection of energy flow path should be chosen depending on the sign of $\eta E_s - E_{ox}$ within a switching cycle. If $\eta E_s - E_{ox} > 0$, the energy flow $P_c(x)$, as shown in Figure 4.7, is allocated for Path 2 to charge up C_s and directed to LED string x. If $\eta E_s - E_{ox} < 0$, the energy flow $P_d(x)$ is allocated for Path 3 to discharge C_s and directed to LED string x. Finally, if $\eta E_s - E_{ox} = 0$, energy flows $P_c(x)$ and $P_d(x)$ are not selected.

Figure 4.7 gives two examples of energy-flow-path control for $N = 2$, where $k_x = \frac{E_{ox}}{\sum_{x=1}^{N} E_{ox}}$ is the portion of energy delivered to LED string x. A design of the control for the proposed PFC SIMO LED driver will be given in Section 4.4.

4.4 Output Current-mode Control

For the proposed PFC SIMO LED driver, the PFC function can be designed with a usual DCM operation of the inductor current controlled using the duty-cycle at a speed much slower than the line frequency. The input power is regulated by observing the averaged voltage of the storage capacitor C_s. In this section, an output current-mode control will be used to accomplish the multiple output function.

4.4.1 Driving Logic of Switches

In Figure 4.6, all energy paths go through L_M. The stored energy E_{L_M} can be measured by its magnetizing current i_M which gives $E_{L_M} = \frac{1}{2}L_M i_M^2$. The measured i_M can be used for the programing of the required driving signals based on the circuit shown in Figure 4.3 and the timing diagram shown in Figure 4.8. For each switching period, channel x, cycling from 1 to N, is defined as the outputting channel while other channels y, $y \neq x$ and $y = 1, \cdots, N$, have zero output. Hence, every switch Q_y is off within this period. The details of current programming for switches Q_m, Q_x and Q_{dis} are explained as follows.

Just before the start of a switching period, say $t = T_1$, all switches are off due to DCM operation. From $t = T_1$ to T_2, Q_m is turned on for the required input power. At $t = T_2$, Q_m is turned off. At this moment, i_M is compared with a reference current I_{Mx_ref} of channel x. If $i_M > I_{Mx\_\text{ref}}$ as shown in the waveforms on the left-hand side of Figure 4.8, switches Q_{dis} and Q_x are kept off forcing current i_M turning on diode D_{ch} charging up C_s. The converter is operating with power flow mode $P_c(x)$ for this switching period. When the decreasing i_M reaches I_{Mx_ref} at $t = T_3$, Q_x turns on until the end of this switching period. Within this time-interval C_s stops charging and i_M is delivering energy to channel x. Otherwise, switches Q_{dis} and Q_x turn on, as shown in the waveforms on the

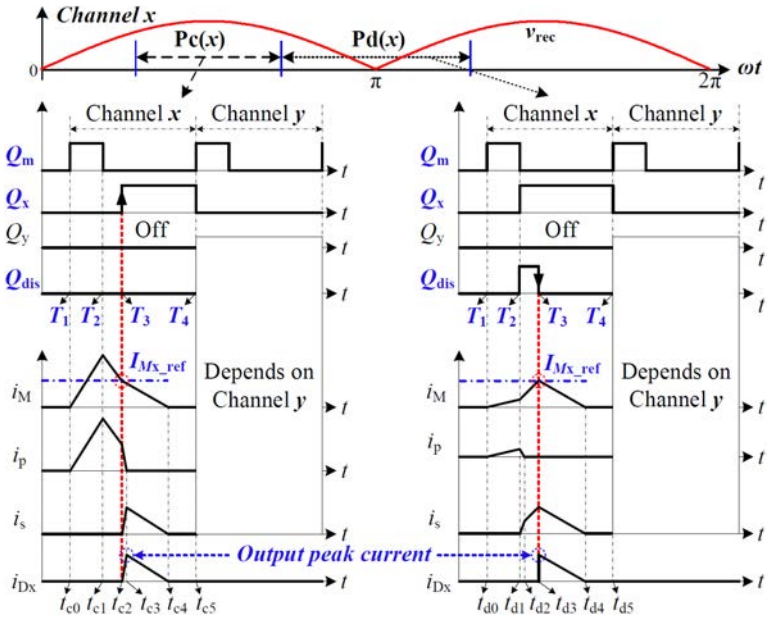


Figure 4.8: Typical time-domain waveforms for channel x.

right-hand side of Figure 4.8. The converter is operating with power flow mode $P_d(x)$. Storage capacitor C_s is charging up L_M until i_M reaches I_{Mx_ref} at $t = T_3$, where switch Q_{dis} is turned off. Switch Q_x is kept on until the end of this switching period. Within time-interval between T_3 and T_4, C_s stops discharging and i_M is delivering energy to channel x.

The current i_M can be programmed to discharge completely to the output starting from $t = T_3$ with respect to the current reference I_{Mx_ref}, where $x = 1 \cdots N$, for each output channel x. In this way, we have

$$P_{o\_\text{total}} = \frac{f_s}{N} \sum_{x=1}^{N} \frac{1}{2} L_M I_{Mx\_\text{ref}}^2. \tag{4.12}$$

These current programming can be fast to cope with the N output requirements. At steady state, $D_m = \frac{T_2 - T_1}{T_4 - T_1}$ will be regulated by the PFC control to have (4.8) and (4.12) satisfied.

With current programming, either of power flow modes $P_c(x)$ and $P_d(x)$ can be selected and operated automatically. The timings of energy flow paths in

Figure 4.6 are explained as follows. Energy flows to L_M via Paths 1 and 2 during $[T_1, T_2]$. Energy delivers to LED strings via Paths 1 and 3 during $[T_3, T_4]$. For power flow mode $P_c(x)$, energy flows via Path 2 during $[T_2, T_3]$. For power flow mode $P_d(x)$, energy flows via Path 3 during $[T_2, T_3]$.

4.4.2 Time-domain Analysis

A detailed time-domain analysis is conducted with consideration of a leakage inductor L_{lk}, verifying that extra lossy snubbers of switches are not required for the proposed PFC SIMO LED driver.

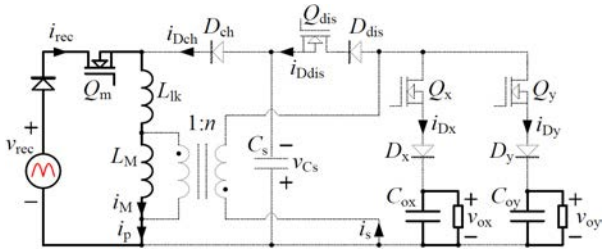
With power flow mode $P_c(x)$, there are five states of operation within a switching period as shown in Figure 4.9. The states are explained as follows.

C(1) $[t_{c0}, t_{c1}]$ as shown in Figure 4.9(a): Q_m turns on at $t = t_{c0}$. Switches Q_x and Q_{dis} are turned off. L_M, L_{lk}, v_{rec} and Q_m are connected in series to give $i_{\text{rec}} = i_p = i_M$. With the excitation of v_{rec}, i_M increases linearly from zero. At $t = t_{c1}$, the peak value of i_{rec} can be obtained by replacing L_M with $L_M + L_{lk}$ in (4.4).

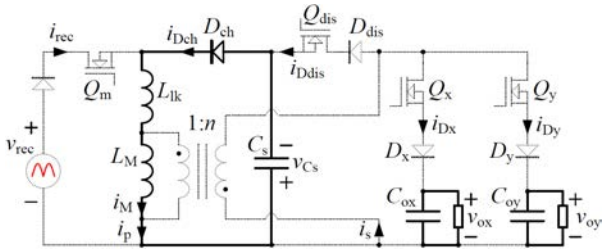
C(2) $[t_{c1}, t_{c2}]$ as shown in Figure 4.9(b): Q_m turns off at $t = t_{c1}$. Switches Q_x and Q_{dis} are off due to $i_M\,(t_{c1}) > I_{Mx\_\text{ref}}$. Current i_M flows into C_s through D_{ch}, decreasing at a rate of $\frac{V_{C_s}}{L_M+L_{lk}}$.

C(3) $[t_{c2}, t_{c3}]$ as shown in Figure 4.9(c): The falling i_M reaches I_{Mx_ref} and triggers Q_x to turn on at $t = t_{c2}$. Current i_p decreases at a rate of $\frac{nV_{C_s}-V_{ox}}{nL_{lk}}$, where the reflected voltage $\frac{V_{ox}}{n}$ should be lower than V_{C_s}. Current i_M decreases at a slower rate of $\frac{V_{ox}}{nL_M}$. Since $i_s = \frac{i_M - i_p}{n}$, i_{Dx} of channel x increases at the rate of $\frac{nV_{C_s}-V_{ox}}{n^2L_{lk}} - \frac{V_{ox}}{n^2L_M}$, reaching a peak value at $t = t_{c3}$.

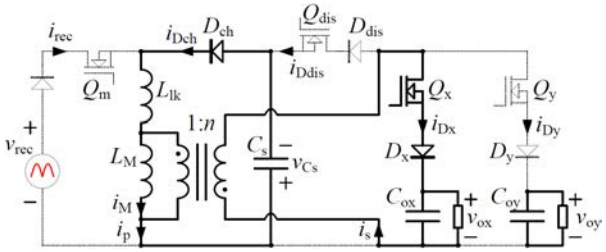
C(4) $[t_{c3}, t_{c4}]$ as shown in Figure 4.9(d): Diode D_{ch} turns off at $t = t_{c3}$. Current i_M discharges through the ideal transformer to channel x. Current i_{Dx}



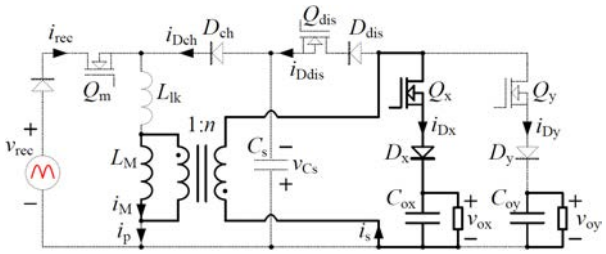
(a) C(1)



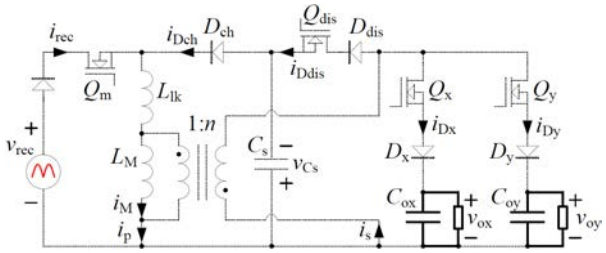
(b) C(2)



(c) C(3)



(d) C(4)



(e) C(5)

Figure 4.9: Time-domain analysis for channel x in power flow mode Pc(x).

decreases at a rate of $\frac{V_{ox}}{n^2 L_M}$.

C(5) $[t_{c4}, t_{c5}]$ as shown in Figure 4.9(e): Current i_M falls to zero at $t = t_{c4}$, waiting for the start of next period.

Similarly, with power flow mode $P_d(x)$, there are five states of operation as shown in Figure 4.9. The states are explained as follows.

D(1) $[t_{d0}, t_{d1}]$ as shown in Figure 4.10(a): Same situation as in C(1) of power flow mode Pc(x).

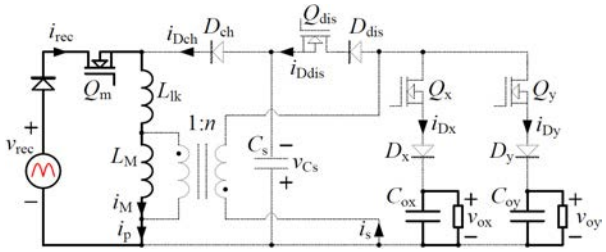
D(2) $[t_{d1}, t_{d2}]$ as shown in Figure 4.10(b): Q_m turns off at $t = t_{d1}$. Switches Q_x and Q_{dis} turn on synchronously due to $i_M\,(t_{d1}) < I_{Mx\_\text{ref}}$. Though Q_x is on, D_x is off since it is reverse biased by $v_{ox} + v_{Cs}$. There is no current flowing through Q_x. Voltage v_{C_s} can be reflected to the magnetizing inductor L_M through the transformer. Consequently, the inductor current i_M continues to increase at a higher rate of $\frac{V_{Cs}}{nL_M}$. The energy stored in L_{lk} recycles to C_s via D_{ch}, and its current i_p decreases at a rate of $\frac{n+1}{n}\frac{V_{Cs}}{L_{lk}}$.

D(3) $[t_{d2}, t_{d3}]$ as shown in Figure 4.10(c): Diode D_{ch} turns off at $t = t_{d2}$ when the energy of L_{lk} depletes. Current i_M continues to increase at the rate of $\frac{V_{Cs}}{nL_M}$.

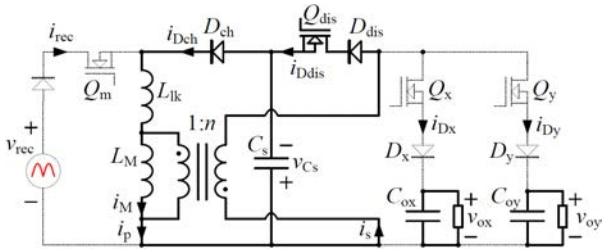
D(4) $[t_{d3}, t_{d4}]$ as shown in Figure 4.10(d): The rising current i_M reaches I_{Mx_ref} and triggers the turn-off signal of Q_{dis} at $t = t_{d3}$. Current i_M discharges as i_s which turns on D_x. Current i_s decreases at the rate of $\frac{V_{ox}}{n^2 L_M}$.

D(5) $[t_{d4}, t_{d5}]$ as shown in Figure 4.10(e): Same situation as in C(5) of power flow mode Pc(x).

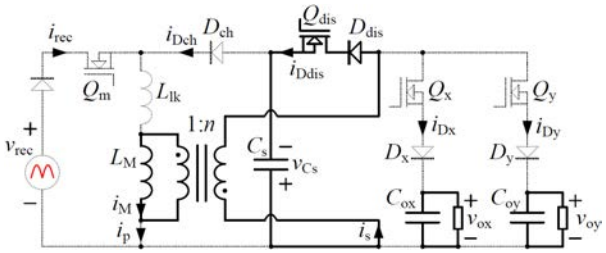
With power flow mode $P_c(x)$, the averaged current I_{Dx_charge} of i_{Dx} within a



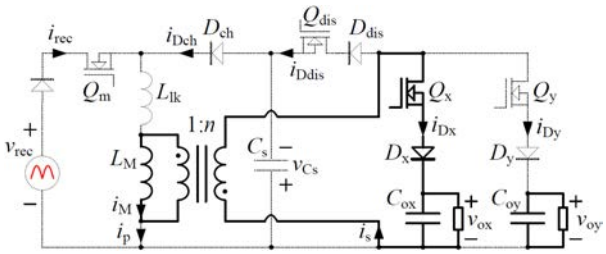
(a) D(1)



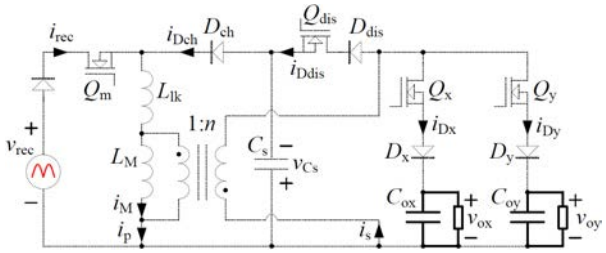
(b) D(2)



(c) D(3)



(d) D(4)



(e) D(5)

Figure 4.10: Time-domain analysis for channel x in power flow mode Pd(x).

period of $\frac{N}{f_s}$ can be calculated as

$$I_{Dx\_\text{charge}} = \frac{f_s}{2N}\left[\frac{L_M}{V_{ox}} - \frac{L_{lk}}{(nV_{C_s} - V_{ox})}\right] I^2_{Mx\_\text{ref}}. \tag{4.13}$$

With power flow mode $P_d(x)$, the current is

$$I_{Dx\_\text{dischage}} = \frac{f_s}{2N}\frac{L_M}{V_{ox}} I^2_{Mx\_\text{ref}}. \tag{4.14}$$

The output power of channel x is obtained by multiplying V_{ox} with equations (4.13) and (4.14). Hence, the current reference I_{Mx_ref} is effective for regulating the output power of channel x. A similar conclusion can be given for other channels.

4.4.3 Loss Analysis

Previously, the driving logic of switches and the according time-domain analysis have been introduced in Section 4.4.1 and 4.4.2 respectively. Then, a loss analysis can be conducted in this section, where the single-stage PFC SIMO LED driver with DCM and multiplexing is also involved for the purpose of comparison.

Common semiconductor devices

The proposed PFC SIMO LED driver shares some semiconductor devices with the traditional one, including the diode bridge, switch Q_m and output branches. Supposing the forward voltage of diodes is constant, the diode bridge and diodes in output branches, i.e., $D_i,\ i = 1 \cdots N$, could have a similar conduction loss. Furthermore, with power flow mode $P_c(x)$, switch Q_m has a higher turn-off loss due to the existence of the high-voltage DC-link capacitor C_s, and the active switches in output branches, i.e., $Q_i,\ i = 1 \cdots N$, endure a higher turn-on loss due to the lost of zero-current-switching (ZCS) turn-on. On the other hand, with

power flow mode $P_d(x)$, switch Q_m has a lower turn-off loss due to the turn-on operation of switch $Q_{\rm dis}$.

Additional semiconductor devices

Additional semiconductor devices, i.e., $D_{\rm ch}$, $Q_{\rm dis}$ and $D_{\rm dis}$, are necessary for the ripple power decoupling function, but additional losses are brought as well. Conduction loss is the main loss of diode $D_{\rm ch}$, as the leakage inductor L_{lk} could release the reverse recovery effort as shown in Figs. 4.9(b) and 4.10(c). Meanwhile, the switching loss of $Q_{\rm dis}$ and conduction loss of $D_{\rm dis}$ cannot be ignored.

Magnetic core

In the proposed LED driver, a single magnetic core is shared by the dual windings, and the the maximum value of magnetizing inductor current can be calculated with (4.4) and (4.9) to give

$$i_{L_M\text{-max}} = \frac{V_m D_m}{L_M f_s} = \sqrt{\frac{4}{L_M f_s} \cdot \sum_{i=1}^{N} P_{oi\_\max}} = \sqrt{\frac{4N}{L_M f_s} \cdot \text{avg}\left\{P_{o1\_\max}, \ldots, P_{oN\_\max}\right\}}, \tag{4.15}$$

where $P_{oi\_\max}$ is the maximum power capacity of channel i and η=1. While, for the single-stage design in [45], i.e., the converter in Fig. 4.1, the maximum value of inductor current should be given as

$$i_{L_M\text{-max}} = \sqrt{\frac{4N}{L_M f_s} \cdot \max\left\{P_{o1\_\max}, \ldots, P_{oN\_\max}\right\}}. \tag{4.16}$$

Observed from (4.15) and (4.16), when maximum power capacities of output channels are not identical, the proposed LED driver can achieve a lower maximum value of magnetizing inductor current, which could be helpful to reduce the maximum magnetic flux density in the magnetic core. However, with the ripple

power balancing function, energy flow Path 3 is required for the power flow mode $P_d(x)$ in Fig. 4.6. Thus, given identical output powers for each channel, the switching-on operation of Q_{dis} in Fig. 4.10(c) could increase the swing of magnetic flux density and lead to a higher core loss over a line period.

4.5 Verification

An experimental prototype of the PFC single-inductor dual-output (SIDO) LED driver is built according to the parameters shown in Table 4.1. The control circuitry is designed and experimentally verified in this section. The photograph of the main circuit board is given in Fig. 4.11.

4.5.1 Design of Control Circuitry

The control circuit for the required PFC function is shown in Figure 4.12(a). The DC component $\overline{v_{Cs}}$ of v_{Cs} is regulated at a fixed reference DC level of V_{Cs_ref} by this PFC controller to balance the required total output DC power. Voltage $\overline{v_{Cs}}$ is extracted by a notch filter to remove the $2f_l$ frequency component from the sensed v_{Cs}. The error voltage of $\overline{v_{Cs}}$ and V_{Cs_ref} is amplified by PI controller UC3526. The output of this PI controller is compared with an internal sawtooth voltage (at pin 10), generating the required duty cycle for driving Q_m.

Table 4.1: Main parameters of the proposed PFC SIDO LED driver without electrolytic capacitor

Parameters	Values	Parameters	Values
Grid Input Voltage v_{in}	110±20% VAC	Magnetizing Inductor L_M	271.4 μH
Grid Frequency f_l	50 Hz	Leakage Inductor L_{lk}	3.2 μH
Q_m Switching Frequency f_s	50 kHz	Turns Ratio n	1
Maximum Power Capacity	2×8 W	DC-link Film Capacitor C_s	4×2.2 μF / 400 V
Measured V-I Points of LED String 1	72.1 V @ 20 mA	Output Ceramic Capacitors C_{o1}, C_{o2}	3×2.2 μF / 100 V
	74.8 V @ 50 mA	Input Inductor L_f	2×470 μH
	77.5 V @ 100 mA	Input Capacitor C_f	220 nF / 400 V
Measured V-I Points of LED String 2	72.2 V @ 20 mA	MOSFETs Q_m, Q_{dis}, Q_1, Q_2	IPA60R385CP
	74.6 V @ 50 mA	Diodes $D_{r1} - D_{r4}$, D_{dis}, D_1, D_2	MUR160G
	77.7 V @ 100 mA	Diode D_{ch}	C3D02060A

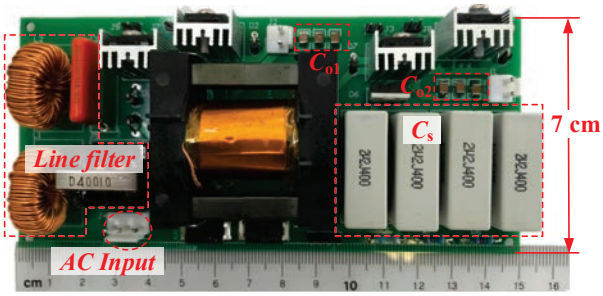


Figure 4.11: Main circuit board of the proposed PFC SIDO LED driver.

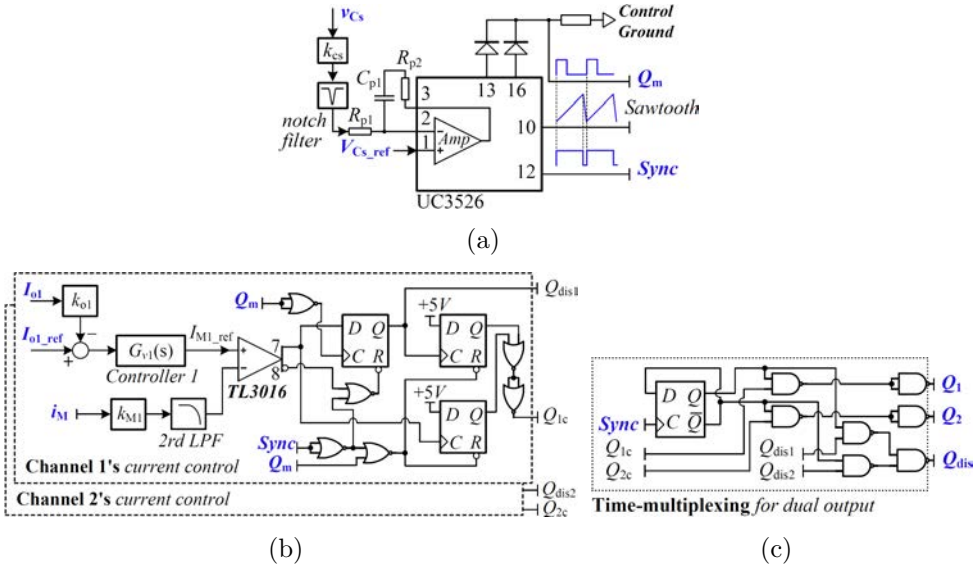


Figure 4.12: Control circuit block diagrams for (a) PFC function, (b) independent output current-mode control, and (c) time-multiplexing management.

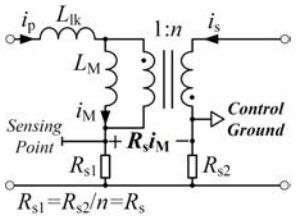


Figure 4.13: A sensing circuit for magnetizing inductor current.

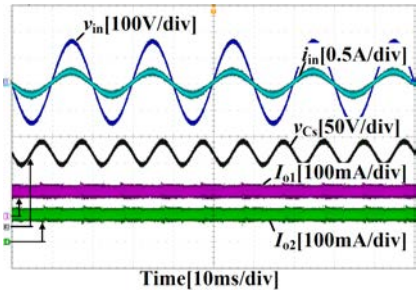
It should be noted that the PFC regulator should be slow enough to keep a constant duty cycle within a line period for a harmonic-free PFC. Meanwhile, the clock signal *Sync* generated at pin 12 and the driving signal of Q_m, as shown in Figure 4.12(a), will be used for the independent current-mode control of each output channel.

Circuit blocks for independent current-mode output control are shown in Figure 4.12(b), where the circuit for Channel 1 is given in detail and the circuit for Channel 2 has similar control structure. For Channel 1, controller 1 regulates the output current I_{o1} of LED string 1 with the reference current I_{o1_ref}. Its output I_{M1_ref} is used as a reference for the programming of i_M. The sensed magnetizing inductor current i_M, being filtered by a second-order low-pass filter to remove high-frequency noise, is compared with I_{M1_ref} by comparator TL3016. Furthermore, the differential outputs of the comparator, i.e., pin 7 and 8, are sent to a logical circuit built with IC 74AHCT. Two sets of signals can be generated from the logic channels, i.e., Q_{dis1}-Q_{1c} from channel 1 and Q_{dis2}-Q_{2c} from channel 2, which will be programmed by the time-multiplexing logic function as shown in Figure 4.12(c). Finally, the signals of Q_1, Q_2 and Q_{dis} are sent to the MOSFET transistor driving circuits.

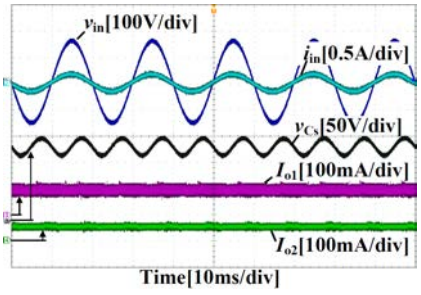
In the current-mode control, the magnetizing inductor current i_M should be carefully sensed without distortion by leakage inductances. A sensing circuit is shown in Figure 4.13, where the sensing point voltage v_s with respect to control ground has a voltage of $i_pR_{s1} - i_sR_{s2}$, and i_p (i_s) is the current of the primary (secondary) winding. From Kirchhoff's current law, $i_s = \frac{i_p - i_M}{n}$. R_{s2} can be designed as nR_{s1}. With an unity turns ratio, i.e., $n = 1$ as in Table 4.1, the two sensing resistors are selected as $R_{s1} = R_{s2} = R_s = 300$ mΩ in this thesis to give $v_s = R_s i_M$.

4.5.2 Experimental Results

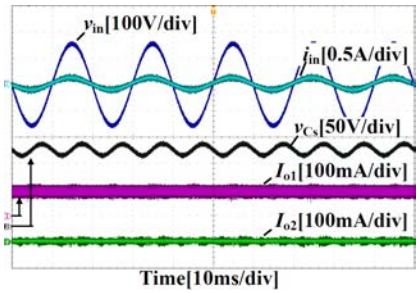
With a 110-VAC input, the steady-state waveforms of v_{in}, i_{in}, v_{Cs}, I_{o1} and I_{o2} are captured as shown in Figure 4.14. It can be observed that i_{in} is in phase with v_{in}, giving a near unity power factor. The voltage v_{Cs} swings at $2f_l$ (100 Hz) to balance the power difference between AC input and DC output. Output



(a) $I_{o1} = 100$ mA and $I_{o2} = 100$ mA



(b) $I_{o1} = 100$ mA and $I_{o2} = 50$ mA



(c) $I_{o1} = 100$ mA and $I_{o2} = 0$ mA

Figure 4.14: Waveforms of v_{in}, i_{in}, v_{Cs}, I_{o1} and I_{o2} of the proposed SIDO LED driver at steady state.

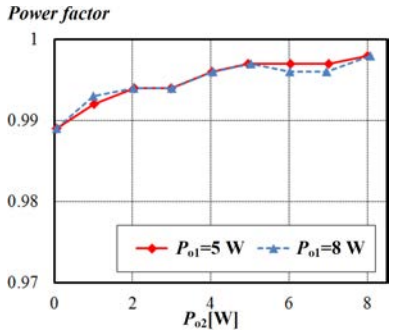
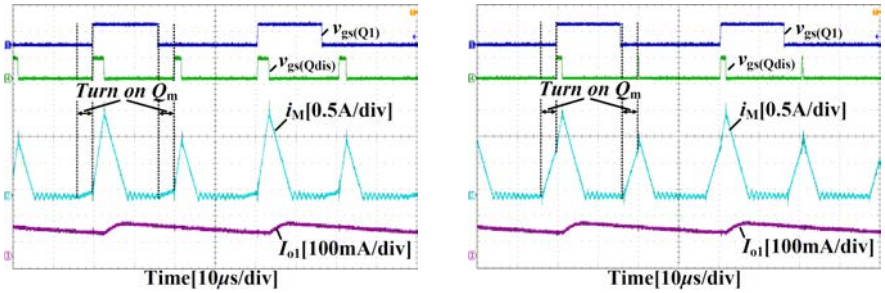


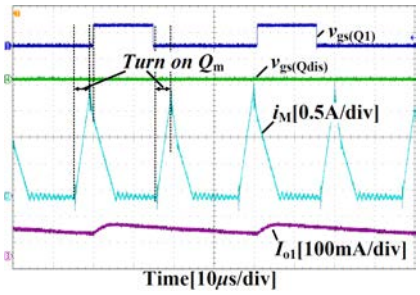
Figure 4.15: Measured power factor of the proposed SIDO LED driver at $v_{\text{in}} = 110$ VAC.

current I_{o1} is regulated at 100 mA. Output current I_{o2} is regulated at 100 mA, 50 mA and 0 mA, as shown in Figures 4.14(a), 4.14(b) and 4.14(c), respectively. Experimental values of power factor are shown in Figure 4.15. Two power values of channel 1 (P_{o1}) at 5 W and 8 W are plotted versus the power of channel 2 (P_{o2}). The power factor is kept at around 0.99.

In order to illustrate the practical current operation within a switching cycle, the waveforms of $v_{gs(Q1)}$, $v_{gs(Q\text{dis})}$, i_M and I_{o1} at switching frequency are illustrated



(a) Pd(x) mode for both channels (b) Pd(x) mode for both channels

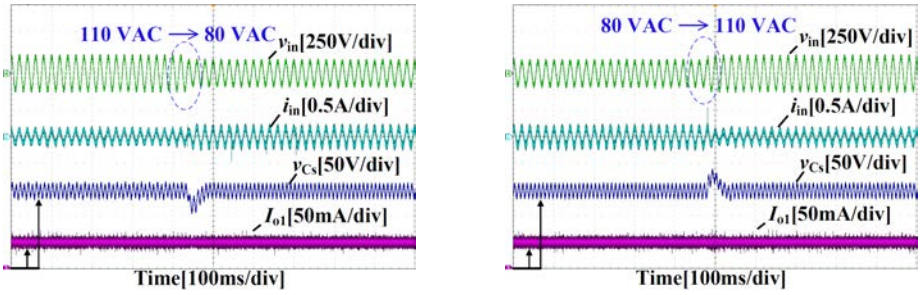


(c) Pc(x) mode for both channels

Figure 4.16: Enlarged waveforms of $v_{gs(Q1)}$, $v_{gs(Q\text{dis})}$, i_M and I_{o1} of the proposed SIDO LED driver at steady state. The waveforms are measured at $I_{o1} = 100$ mA and $I_{o2} = 50$ mA.

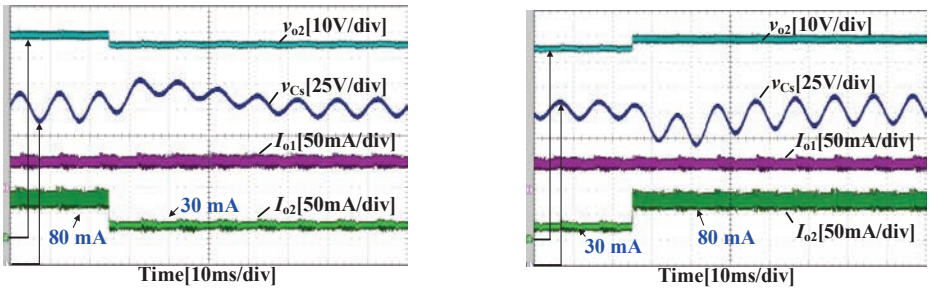
in Figure 4.16 at three grid voltage instances, for the regulated outputs of $I_{o1} =$ 100 mA and $I_{o2} = 50$ mA. The theoretical waveforms are given in detail, as shown in Figure 4.8. Due to time-multiplexing, Q_1 is switched at 25 kHz, which is half of Q_m (50 kHz). For power flow mode $P_d(x)$ as shown in Figures 4.16(a) and 4.16(b), since the energy provided by the grid is insufficient, Q_1 and Q_{dis} are turned on after Q_m is turned off. Current i_M absorbs energy from C_s and continues to increase. After it has reached the required value, Q_{dis} is turned off. Due to the rectified grid voltage in Figure 4.16(a) is lower than that in Figure 4.16(b), the corresponding duty cycle of Q_{dis} is larger to discharge more energy from capacitor C_s. In the $P_c(x)$ mode of Figure 4.16(a), since the energy provided by grid is excessive, Q_1 and Q_{dis} keeps off after Q_m is turned off. Energy of i_M is charging up C_s and decreasing until Q_1 is turned on.

The transient performance is given in Figure 4.17. Although transitions of v_{in} occur, the output current in the LED strings can be kept constant, with a



(a) A step-down transition of v_{in} (b) A step-up transition of v_{in}

Figure 4.17: Transient waveforms of v_{in}, i_{in}, v_{Cs} and I_{o1} of the proposed SIDO LED driver at $P_{o1} = P_{o2} = 4$ W.



(a) A step-down transition of I_{o2} (b) A step-up transition of I_{o2}

Figure 4.18: Transient waveforms of I_{o1}, I_{o2}, v_{o2} and v_{Cs} of the proposed SIDO LED driver at $I_{o1} = 50$ mA.

small overshoot or undershoot in the storage capacitor voltage v_{Cs}. Moreover, transitions of LED current is given for channel 2 between 30 mA and 80 mA as shown in Fig. 4.18, where the LED current of channel can keep constant.

For the purpose of comparison, another prototype is also built for the single-stage PFC SIDO LED driver in [45], i.e., the converter in Figure 4.1, where DCM control is adopted instead of the original one. Some key parameters are listed in Table 4.2. Experimental waveforms in Figure 4.19 are measured at the same set of conditions with that of the proposed LED driver. Comparisons of experimental results are summarized as follows.

(1) *Electrolytic capacitor-less design*: For the single-stage LED driver, although the output capacitance increases from 6.6 μF to 84.4 μF, current ripples in LED strings are even larger than that of the proposed converter. So, its elec-

Table 4.2: Key parameters of the traditional PFC SIDO LED driver with electrolytic capacitor

Key Parameters	Values
Inductor L_M	270.0 μH
Output Capacitors C_{o1}, C_{o2}	84.4 μF
Input Inductor L_f	2×470 μH
Input Capacitor C_f	220 nF / 400V
MOSFETs Q_m, Q_1, Q_2	IPA60R385CP
Diodes $D_{r1} - D_{r4}$, D_1, D_2	MUR160G

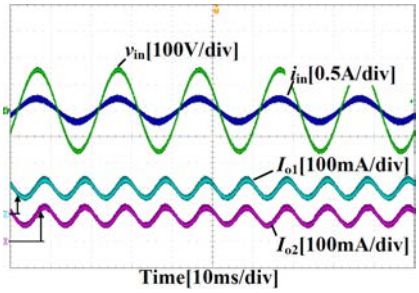
trolytic capacitor-less design, i.e., using film capacitors or ceramic capacitors for C_{o1} and C_{o2}, will come with at a higher cost.

(2) *Flicker*: The single-stage LED driver has a significant amount of ripple current at double line frequency, as shown in Figures 4.19(a), 4.19(b) and 4.19(c), which may cause flickers. In contrary, for the proposed LED driver, small output capacitors are used to remove current ripples at the switching frequency. Current ripple at 25 kHz is small and invisible.

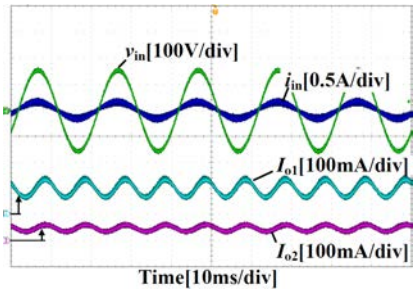
(3) *Line filter*: Line LC filters with the same set of parameters is used for the two prototypes. A smaller line current ripple can be observed for the proposed LED driver by comparing Figures 4.14(c) and 4.19(c).

(4) *Output dynamic performance*: With transitions of v_{in}, an undershot and overshoot of LED current can be observed in Figures 4.19(d) and 4.19(e) respectively. The overshoot may burn and reduce life span of LEDs. Moreover, with a fast output dynamic performance of the proposed LED driver, PWM dimming and bi-level dimming are applicable. Control technique in [15] can also be implemented to further reduce capacitance requirement.

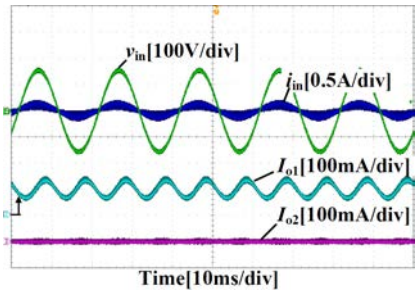
(5) *Efficiency*: In this proposed electrolytic capacitor-less design, the efficiency has been shown to be better than a corresponding two-stage design [50]. However, much lower efficiency as shown in Figure 4.20 is observed when compared with the



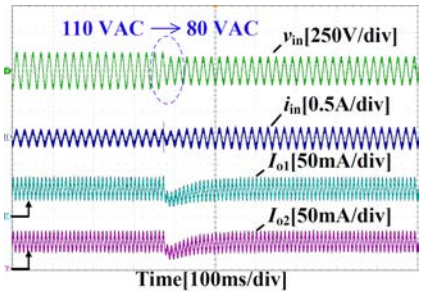
(a) $I_{o1} = 100$ mA and $I_{o2} = 100$ mA



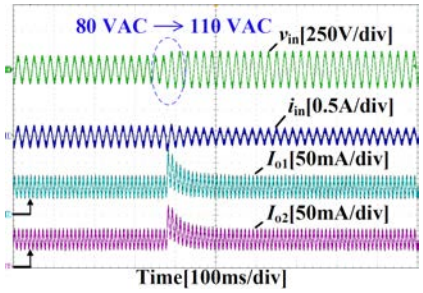
(b) $I_{o1} = 100$ mA and $I_{o2} = 50$ mA



(c) $I_{o1} = 100$ mA and $I_{o2} = 0$ mA



(d) A step-down transition of v_{in} at $P_{o1} = P_{o2} = 4$ W



(e) A step-up transition of v_{in} at $P_{o1} = P_{o2} = 4$ W

Figure 4.19: Waveforms of v_{in}, i_{in}, I_{o1} and I_{o2} of the single-stage SIDO LED driver.

corresponding single-stage design, where the overall efficiency is calculated using $\eta = \frac{P_{o1}+P_{o2}}{P_{\text{in}}}$. The lower efficiency performance may be due to the unavoidable extra switching instances within a switching cycle for the required controls of active power decoupling and output current regulations. The switching loss may be reduced if this driver is implemented in IC form.

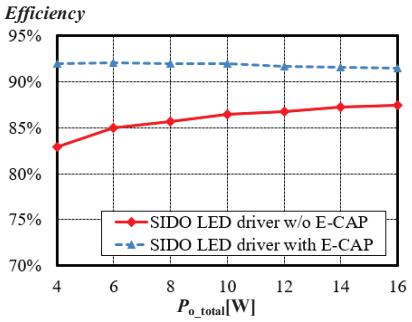


Figure 4.20: Efficiency comparison of the two SIDO LED drivers at $v_{\text{in}} = 110$ VAC and $P_{o1} = P_{o2}$.

4.6 Summary

In this chapter, an active power decoupling power-factor-corrected single-inductor-multiple-output LED driver is developed. The LED driver is optimized without the requirement of electrolytic capacitors for a better system life span and a wider operating temperature. Compared with an existing single-stage design without active power decoupling, the proposed LED driver has benefits of a design without electrolytic capacitor, a near zero low-frequency ripple current for each output channel, a much smaller line filter and a much faster output current regulation for each output channel. Prototype converters are built to show the effective control and various benefits of the proposed LED driver.

Chapter 5

Bidirectional Single-Phase AC-DC Three-Phase-Leg Converters

5.1 Introduction

In a single-phase grid-connected nanogrid system, a bidirectional AC-DC converter is usually required to transfer energy between the AC grid and a DC bus. Active AC power balancing is often implemented to prevent the AC grid ripple power from injecting into the DC bus. A four-phase-leg sinusoidal pulse-width-modulation (SPWM) converter can readily provide power factor correction and active AC power balancing. In this chapter, the use of three-phase-leg SPWM converters for achieving these functions is analyzed. A family of bidirectional single-phase AC-DC three-phase-leg SPWM converters with an AC storage capacitor for use in a nanogrid system is designed with a general control structure and a modulation scheme for minimizing the AC storage capacitance. The general control structure is designed to achieve a decoupled system of a power-factor-correction converter cascaded with an active AC power load at the DC

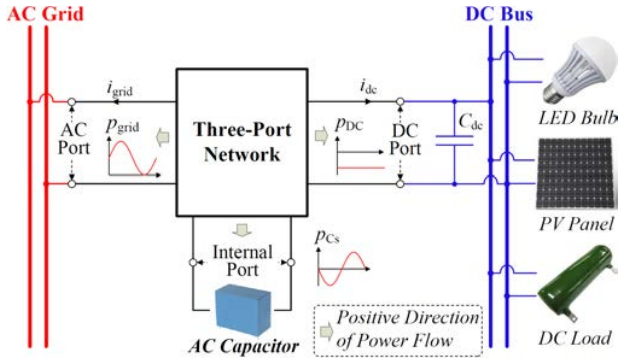


Figure 5.1: Nanogrid and single-phase AC-DC bus converter with active power decoupling.

bus. The decoupled system is developed based on decomposition to differential-mode and common-mode voltages. The modulation method involves an extra zero-sequence voltage injection derived from the three-phase-leg SPWM voltages without introducing higher order harmonic distortions. A significant reduction of the AC storage capacitance and an improvement of converter efficiency are achieved. The design and analysis are verified by simulations and experimental measurements. Table 5.1 has compared the work in this chapter with previous two chapters, i.e., Chapter 3 and 4.

5.2 Power Analysis and Converter Design

The single-phase AC-DC power converter with active ripple power decoupling can be considered as a three-port network, as shown in Figure 2.4 and repeated in Figure 5.1 for convenience. The instantaneous power measured at the AC port is composed of an averaged DC power and an AC ripple power. The averaged DC power is balanced by the DC power from the DC port, while the AC ripple power is buffered by an internal power storage device connected to the internal port of the power converter. An AC capacitor C_s is used as the internal storage of the power converter. In this section the decoupling of the averaged DC power and the AC ripple power will be described.

Table 5.1: Work in This Thesis

Chapter	5	3 and 4
Topology	AC-DC bus converter	Single/multiple-output LED driver
Power level	High	Low
Power flow	Bidirectional	Unidirectional
Control target	Minimize output voltage ripple	Minimize output current ripple
Storage capacitor	Instantaneous AC voltage is controlled	Averaged DC voltage is controlled

5.2.1 Power Decoupling

The AC grid voltage is assumed to be sinusoidal with an angular frequency ω. From Figure 5.1, the grid voltage v_{grid} and current i_{grid} can be written as

$$v_{\text{grid}} = V_{\text{grid}} \sin \omega t, \text{ and} \tag{5.1}$$

$$i_{\text{grid}} = I_m \sin \omega t, \tag{5.2}$$

where the value of I_m can be positive for inverter mode or negative for rectifier mode of operation.

Using (5.1) and (5.2), the instantaneous power delivered to the AC port is given by

$$p_{\text{grid}} = v_{\text{grid}} i_{\text{grid}} = \frac{1}{2} V_{\text{grid}} I_m - \frac{1}{2} V_{\text{grid}} I_m \cos 2\omega t, \tag{5.3}$$

which is simply a summation of an averaged DC power p_{avg} and a second-order harmonic AC power $p_{g\_2\omega}$ given by

$$p_{\text{avg}} = \frac{1}{2} V_{\text{grid}} I_m, \text{ and} \tag{5.4}$$

$$p_{g\_2\omega} = -\frac{1}{2} V_{\text{grid}} I_m \cos 2\omega t. \tag{5.5}$$

The AC power $p_{g\_2\omega}$ is sinusoidal, varying at twice the grid frequency. This AC power should be compensated internally by p_{C_s} of the converter. The three-port network is composed of active switches and some filtering inductors for removing the switching ripple. Assuming that the three-port network is lossless, the power balance condition can be written as

$$p_{C_s} = -p_{g\_2\omega} - \sum p_L = \frac{1}{2} V_{\text{grid}} I_m \cos 2\omega t - \sum p_L, \tag{5.6}$$

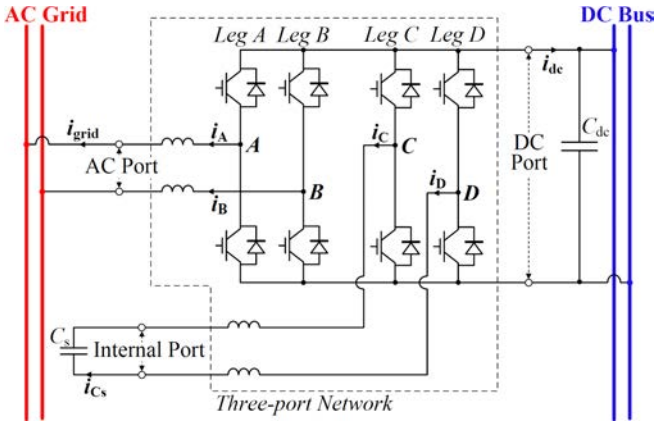


Figure 5.2: Four-leg AC-DC converters.

where $\sum p_L$ is the sum of power from every switching ripple filtering inductor within the three-port network.

5.2.2 Converter Design

Using the information of the decoupled power in (5.6), an initial design can be obtained as shown in Figure 5.2, where two H-bridge legs A and B of the converter are responsible for active power factor correction, and two other H-bridge legs C and D are responsible for the AC power balancing [77]. This four-H-bridge-leg converter can be considered as an integration of two independent converters connected at the common DC bus. The popular dual-loop control of the rectifier can be readily employed for active power factor correction. According to (5.6), the circuit with H-bridge legs C and D responsible for AC power balancing can be considered as an AC power load varying at double-line frequency connected at the DC bus. The two converters are stable as far as the first converter with active power factor correction has a response much slower than the double line frequency. Essentially, p_{C_s} can be assigned as either $i_{C_s}v_{C_s}$ or $(-i_{C_s})(-v_{C_s})$. Apparently, it is possible to combine two H-bridge legs into a common H-bridge leg as long as the original quantities v_{grid}, i_{grid}, v_{C_s} and i_{C_s} are maintained. The resulting converter is shown in Figure 5.3, where H-bridge leg D is removed and its function

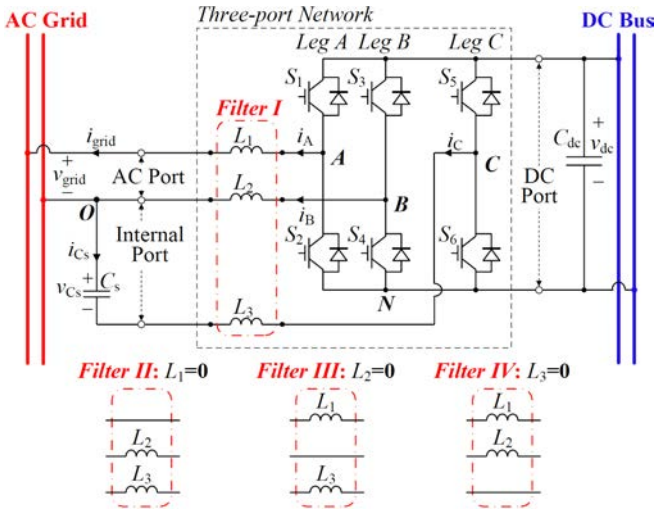


Figure 5.3: A family of three-leg AC-DC converters with (a) Filter I: three filtering inductors, (b) Filter II: $L_1 = 0$, (c) Filter III: $L_2 = 0$, and (d) Filter IV: $L_3 = 0$.

is shared by H-bridge leg B. The H-bridge leg B must satisfy $-i_B = i_{\text{grid}} - i_{C_s}$. Alternatively, the condition $-i_B = i_{\text{grid}} + i_{C_s}$ corresponds to the case where H-bridge leg C is removed and its function is shared by H-bridge leg B. For a given p_{C_s}, the same amount of compensated power can be achieved with two possible choices of v_{C_s}. It will be shown in Section 5.3.2 that one particular choice of v_{C_s} gives less loss.

Furthermore, since one of the three H-bridge legs can be assigned as a common terminal, its filtering inductor may appear to be redundant and may be removed from the converter. A family of converters can be derived as shown in Figure 5.3, of which the converter with Filter III has been thoroughly studied [67]. Among the converters in Figure 5.3, the converter with three filtering inductors is robust for some adaptive power applications by paralleling a number of converters [81]. Moreover, due to the sharing of an H-bridge leg, the control functions of active power correction and AC power balancing might be coupled. Hence, a general control structure applicable to the family of converters becomes necessary. In the following section, a general control structure will be developed for the converter with three filtering inductors. A general decoupled current control will be

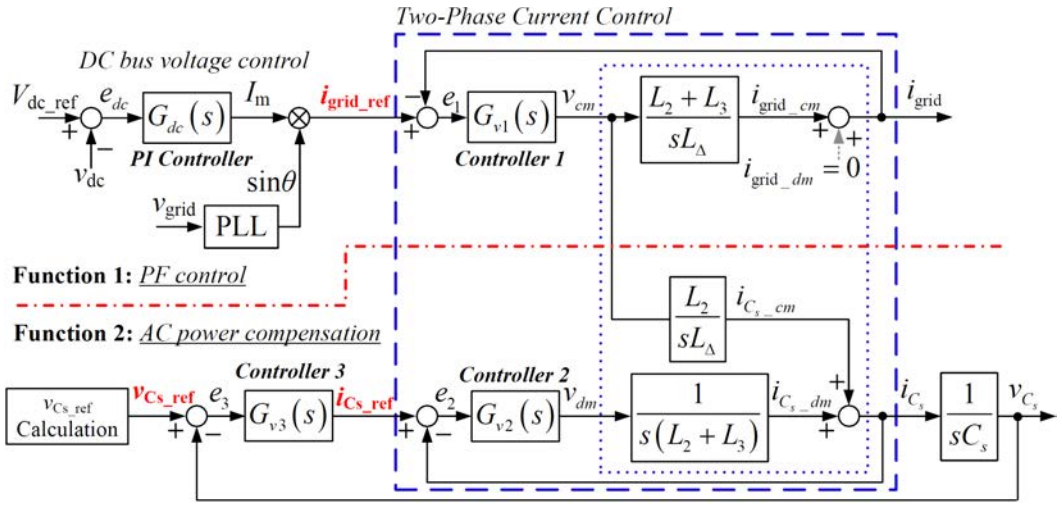


Figure 5.4: General control structure, where $\theta = \omega t$.

developed subsequently for the family of converters.

5.3 Converter Control

5.3.1 Control Structure

For the family of converters shown in Figure 5.3, a general control structure can be designed to realize two control functions, as given in Figure 5.4. The first function aims to control the averaged DC bus voltage and maintains unity power factor at the AC port. This control is readily designed with the usual dual-loop structure. For the outer DC bus voltage loop, I_m is the output of the controller, and $\sin\theta$ is generated by a phase-locked loop (PLL) module. The product $I_m \sin\theta$ is the reference of the grid current. The inverter or rectifier mode of operation is determined by the output of a PI controller with input error voltage $V_{\text{dc\_ref}} - V_{\text{dc}}$. As discussed in Section 5.2.2, this control should have a response much slower than the double line frequency.

The second control function is AC power balancing which minimizes the DC bus ripple voltage. As discussed in Section 5.2.2, this function should not inter-

fere with the control of the first function. The power of the AC capacitor C_s is regulated according to the power at the AC port calculated from I_m by (5.6). In [67], the DC bus voltage ripple is required by a closed-loop control to regulate the DC bus ripple voltage. However, the DC bus ripple voltage can be distorted by other converters, making tight control unreliable. Moreover, the control in [67] is not applicable to the converter with Filter I shown in Figure 5.3, where the second control function would interfere with the first control function of power factor correction through the three filtering inductors. We will explain this in Section 5.3.3. In this thesis, using a proper control voltage transformation, the coupling of the second control function with the first control function can be eliminated. Thus, the widely employed power-factor-correction control structure can be adopted. The power-factor-correction control structure is labeled as "Function 1" in Figure 5.4. Also, as shown in Figure 5.4, the AC power p_{C_s} is controlled by a real-time generated reference voltage $v_{C_s\_\mathrm{ref}}$. An inner current loop is used to reduce the order of the control system. As the inner current loop is much faster than the outer voltage loop, the capacitor voltage can be regarded as a voltage source for the inner current loop. The voltage at the AC port, the voltage at the internal port, and the modulated voltages of the H-bridges can be found from an unbalanced three-phase system.

In Figure 5.4, there might have cross couplings of the two-input two-output "two-phase current control" subsystem that may make the control difficult. A general decoupled current control method will be developed for the two-phase current control subsystem, as given in Section 5.3.3.

5.3.2 AC Storage Capacitor Reference Voltage

The amount of power p_{C_s} injected into C_s, as given in (5.6), can be determined from its voltage which is given as

$$v_{C_s} = a \cdot \sin \omega t + b \cdot \cos \omega t \tag{5.7}$$

where parameters a and b are to be determined. The corresponding capacitor current is calculated as

$$i_{C_s} = C_s \frac{dv_{C_s}}{dt} = X_{C_s}^{-1} b \cdot \sin \omega t - X_{C_s}^{-1} a \cdot \cos \omega t, \tag{5.8}$$

where $X_{C_s} = -\frac{1}{\omega C_s}$. Therefore,

$$p_{C_s} = v_{C_s} i_{C_s} = P_{C\_\sin 2\omega} \sin 2\omega t + P_{C\_\cos 2\omega} \cos 2\omega t, \tag{5.9}$$

where

$$P_{C\_\sin 2\omega} = -0.5 X_{C_s}^{-1} \left(a^2 - b^2\right), \text{ and} \tag{5.10}$$

$$P_{C\_\cos 2\omega} = -X_{C_s}^{-1} ab. \tag{5.11}$$

The AC power stored in all filtering inductors, i.e., $\sum p_L$ in (5.6), can be calculated as

$$\begin{aligned} \sum p_L &= p_{L1} + p_{L2} + p_{L3} \\ &= i_{\text{grid}} \cdot L_1 \frac{di_{\text{grid}}}{dt} + i_B L_2 \frac{di_B}{dt} + i_{C_s} L_3 \frac{di_{C_s}}{dt} \\ &= P_{L\_\sin 2\omega} \cdot \sin 2\omega t + P_{L\_\cos 2\omega} \cdot \cos 2\omega t, \end{aligned} \tag{5.12}$$

where

$$P_{L\_\sin 2\omega} = \frac{1}{2}\left(X_{L1} + X_{L2}\right) I_m^2 - \frac{\left(X_{L2} + X_{L3}\right)\left(a^2 - b^2\right)}{2X_{C_s}^2} - \frac{X_{L2}}{X_{C_s}} I_m b, \tag{5.13}$$

$$P_{L\_\cos 2\omega} = X_{L2} X_{C_s}^{-1} I_m a - X_{C_s}^{-2}\left(X_{L2} + X_{L3}\right) ab, \tag{5.14}$$

$$X_{Lx} = \omega L_x, \text{ for } x = 1, 2, 3, \text{ and} \tag{5.15}$$

$$i_{\text{grid}}(t) = I_m \sin \omega t. \tag{5.16}$$

Applying Kirchhoff's current law at node P of Figure 5.5(a), we get

$$i_B = i_{C_s} - i_{\text{grid}} = \left(X_{C_s}^{-1} b - I_m\right) \sin \omega t - X_{C_s}^{-1} a \cos \omega t. \tag{5.17}$$

Then, substituting (5.9) and (5.12) into (5.6), we have

$$\left(P_{L\_\sin 2\omega} + P_{C\_\sin 2\omega}\right) \cdot \sin 2\omega t + \left(P_{L\_\cos 2\omega} + P_{C\_\cos 2\omega} - \frac{1}{2} V_{\text{grid}} I_m\right) \cdot \cos 2\omega t = 0. \tag{5.18}$$

In order that (5.18) holds for all t, the coefficients of (5.18) must be zero. We have

$$P_{L\_\sin 2\omega} + P_{C\_\sin 2\omega} = 0, \text{ and} \tag{5.19}$$

$$P_{L\_\cos 2\omega} + P_{C\_\cos 2\omega} = \frac{1}{2} V_{\text{grid}} I_m. \tag{5.20}$$

Solving equations (5.19) and (5.20) for a and b, we have

$$a = \pm\sqrt{K_1 I_m^2 + \sqrt{K_2 I_m^4 + K_3 V_{\text{grid}}^2 I_m^2}}, \text{ and} \tag{5.21}$$

$$b = \frac{X_{L2} X_{C_s} I_m}{\lambda_X} - \frac{X_{C_s}^2 V_{\text{grid}} I_m}{2a\lambda_X}, \tag{5.22}$$

where

$$K_1 = \frac{(X_{L1} + X_{L2})\,\lambda_X - X_{L2}^2}{2\lambda_X^2} X_{C_s}^2, \tag{5.23}$$

$$K_2 = \left[(X_{L1} + X_{L2})\,\lambda_X - X_{L2}^2\right]^2 \frac{X_{C_s}^4}{4\lambda_X^4}, \tag{5.24}$$

$$K_3 = \frac{X_{C_s}^4}{4\lambda_X^2}, \text{ and} \tag{5.25}$$

$$\lambda_X = X_{L2} + X_{L3} + X_{C_s}. \tag{5.26}$$

Substituting (5.21) and (5.22) into (5.8), the amplitude I_{C_s} of i_{C_s} can be calculated as

$$I_{C_s} = \sqrt{X_{C_s}^{-2}\,(b^2 + a^2)} = \left|X_{C_s}^{-1}\right| \sqrt{m_{C_s} + n_{C_s} \cdot a^{-1}}, \tag{5.27}$$

where

$$m_{C_s} = \left(\frac{X_{L2} X_{C_s} I_m}{\lambda_X}\right)^2 + \left(\frac{X_{C_s}^2 V_{\text{grid}} I_m}{2a\lambda_X}\right)^2 + a^2 > 0, \text{ and} \tag{5.28}$$

$$n_{C_s} = -\frac{X_{L2} X_{C_s}^3 I_m^2 V_{\text{grid}}}{\lambda_X^2} > 0. \tag{5.29}$$

It is observed that the solution with $a < 0$ gives a smaller I_{C_s}. Similarly, substituting (5.21) and (5.22) into (5.17), the amplitude I_B of i_B is calculated as

$$I_B = \sqrt{\left(X_{C_s}^{-1} b - I_m\right)^2 + \left(X_{C_s}^{-1} a\right)^2} = \sqrt{m_{i_B} \cdot I_m^2 + n_{i_B} \cdot a^{-1}}, \tag{5.30}$$

where

$$\begin{aligned} m_{i_B} = {} & \left(\frac{X_{L2} - \lambda_X}{\lambda_X}\right)^2 I_m^2 + \left(\frac{0.5 X_{C_s} V_{\text{grid}}}{\lambda_X} a^{-1}\right)^2 I_m^2 \\ & + \left(X_{C_s}^{-1} a\right)^2 I_m^2 > 0, \text{ and} \end{aligned} \tag{5.31}$$

$$n_{i_B} = \frac{(X_{L3} + X_{C_s})\,X_{C_s}}{\lambda_X^2} V_{\text{grid}}. \tag{5.32}$$

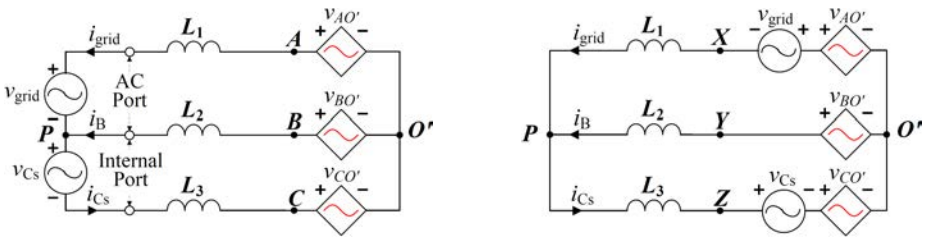


Figure 5.5: Three-phase unbalanced model for the development of a dual-loop current control.

In this family of converters, the energy stored in the AC capacitor C_s is much larger than that stored in L_3. Thus, $X_{L3} + X_{C_s} < 0$, and $n_{i_B} > 0$. Hence, we arrive at the same conclusion that a negative a gives a smaller I_B.

It is obvious that the zero-ripple power at DC port can be realized with the two different target capacitor reference voltages given by (5.7), (5.21) and (5.22). However, the v_{C_s} with a negative value in (5.21) is selected for lower RMS values of i_{C_s} and i_B, which will result in a smaller loss [79].

5.3.3 Decoupled Current Control

The circuit with Filter I in Figure 5.3 can be modeled as a three-phase unbalanced circuit, as shown in Figure 5.5(a), where O' is the mid-point voltage of the DC bus, and $v_{AO'}$, $v_{BO'}$ and $v_{CO'}$ are the averaged voltages modulated by the SPWM method. The model in Figure 5.5(a) can be replaced by the equivalent model of Figure 5.5(b) by re-locating the voltage sources v_{grid} and v_{C_s}.

The voltages v_{XY} and v_{ZY} shown in Figure 5.5(b) can be selected as control variables for controlling i_{grid} and i_{C_s}. Applying superposition, the circuit equations become

$$I_{\text{grid}}(s) = \frac{L_2 + L_3}{sL_\Delta} V_{XY}(s) - \frac{L_2}{sL_\Delta} V_{ZY}(s), \text{ and} \tag{5.33}$$

$$I_{C_s}(s) = \frac{L_2}{sL_\Delta} V_{XY}(s) - \frac{L_1 + L_2}{sL_\Delta} V_{ZY}(s), \tag{5.34}$$

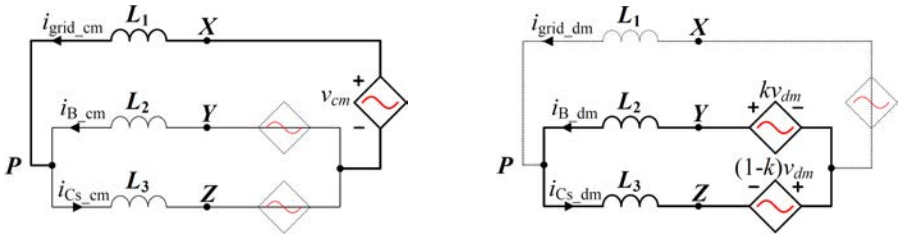


Figure 5.6: Model for decoupled control. (a) Common-mode operation, (b) differential-mode operation, where $k = L_2/(L_2 + L_3)$.

where

$$L_\Delta = L_1L_2 + L_1L_3 + L_2L_3. \tag{5.35}$$

Thus, equations (5.33) and (5.34) are coupled if $L_2 \neq 0$, making the control difficult.

In this thesis, a general decoupled current control is proposed based on decomposing v_{XY} and v_{ZY} to their common-mode voltage v_{cm} and differential-mode voltage v_{dm}, as shown in Figure 5.6. The decomposition is given by

$$v_{cm} - kv_{dm} = v_{XY} = v_{AO'} - v_{BO'} - v_{\text{grid}} \text{ and} \tag{5.36}$$

$$v_{dm} = v_{YZ} = v_{BO'} - v_{CO'} - v_{C_s}. \tag{5.37}$$

Likewise, the currents can be written with their common-mode and differential-mode components as

$$i_{\text{grid}} = i_{\text{grid\_}cm} + i_{\text{grid\_}dm} \text{ and} \tag{5.38}$$

$$i_{C_s} = i_{C_s\_cm} + i_{C_s\_dm}. \tag{5.39}$$

In Figure 5.6(b), if the coefficient k in (5.36) is defined as

$$k = \frac{L_2}{L_2 + L_3}, \tag{5.40}$$

then we always have

$$I_{\text{grid\_}dm}(s) = 0. \tag{5.41}$$

Hence, the control law in terms of v_{cm} and v_{dm} is

$$I_{\text{grid}}(s) = I_{\text{grid\_cm}}(s) = \frac{L_2 + L_3}{sL_\Delta} V_{cm}(s) \text{ and} \tag{5.42}$$

$$\begin{aligned} I_{C_s}(s) &= I_{C_s\_cm}(s) + I_{C_s\_dm}(s) \\ &= \frac{L_2}{sL_\Delta} V_{cm}(s) + \frac{1}{s(L_2 + L_3)} V_{dm}(s). \end{aligned} \tag{5.43}$$

The control structure is shown as the "two-phase current control" subsystem in Figure 5.4. Here, the active power factor control is decoupled from the AC power balancing. As a result, the two control functions can be considered as being connected in cascade, and the second control function block can be considered as an AC power load connected at the DC bus of a bidirectional rectifier with ordinary active power factor control. Thus, the design of the control parameters can be greatly simplified.

5.4 Modulation for Minimal AC Storage Capacitance

In the aforedescribed control, variables v_{cm} and v_{dm} are calculated and transformed to $v_{AO'}$, $v_{BO'}$ and $v_{CO'}$ for SPWM, which is linear when the modulated voltage is within $\pm\frac{1}{2}V_{\text{dc}}$. In this section, a novel linear modulation for maximizing

v_{C_s} leading to minimal AC storage capacitance will be developed.

5.4.1 Modulation with Optimized DC Utilization of v_{C_s}

The modulated voltages $v_{AO'}$ and $v_{BO'}$ are of equal magnitude and opposite phase [67], as shown in Figure 5.7, i.e.,

$$v_{AO'} = -v_{BO'}, \tag{5.44}$$

which is widely used in analyzing some single-phase full-bridge converters.

Applying this modulation method to the family of converters of Figure 5.3, and solving (5.36), (5.37) and (5.44), the three modulated voltages can be found as:

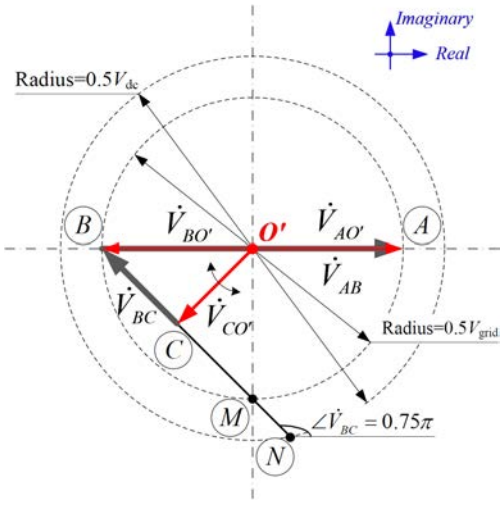
$$v_{AO'} = 0.5v_{cm} - 0.5kv_{dm} + 0.5v_{\text{grid}} = m_A \cdot \frac{1}{2}V_{\text{dc}} \sin(\omega t + \varphi_A), \tag{5.45}$$

$$v_{BO'} = -0.5v_{cm} + 0.5kv_{dm} - 0.5v_{\text{grid}} = m_B \cdot \frac{1}{2}V_{\text{dc}} \sin(\omega t + \varphi_B), \text{ and} \tag{5.46}$$

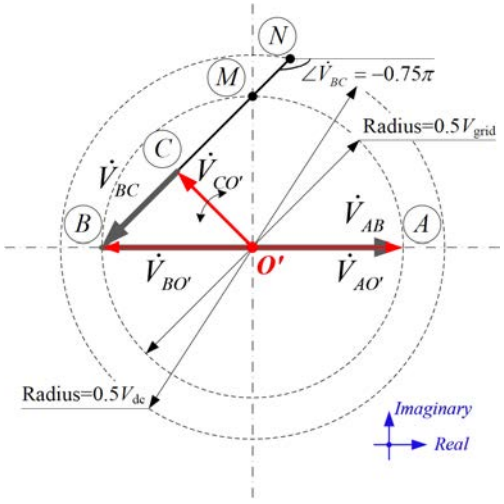
$$v_{CO'} = -0.5v_{cm} + (0.5k - 1)\, v_{dm} - 0.5v_{\text{grid}} - v_{C_s} = m_C \cdot \frac{1}{2}V_{\text{dc}} \sin(\omega t + \varphi_C), \tag{5.47}$$

where $m_x \leq 1$ ($x = A, B, \text{and } C$) is a modulation index for leg x. Voltage V_{dc} ($\geq V_{\text{grid}}$) is normally designed within a range ($V_{\text{dc\_min}}, V_{\text{dc\_max}}$) according to some specifications such as the voltage range for droop control of power within a nanogrid system.

According to the analysis presented in Section 5.3.2, v_{C_s} that gives less loss is chosen for the required power compensation. For simplicity, the ripple filtering inductors L_1, L_2 and L_3 are ignored in this analysis. Therefore, using (5.21) and



(a)



(b)

Figure 5.7: Vector diagrams of traditional modulation strategy. (a) Rectifier mode, (b) inverter mode.

(5.22), we have

$$v_{C_s} = -\sqrt{0.5\,|V_{\text{grid}} I_m X_{C_s}|}\sin\omega t - \text{sgn}\,(I_m)\sqrt{0.5\,|V_{\text{grid}} I_m X_{C_s}|}\cos\omega t \qquad (5.48)$$

It is noted that the time-domain quantity $a\sin\omega t + b\cos\omega t$ has a phasor equivalence. Using Euler's equation, i.e., $\sin\omega t = \Im(e^{j\omega t})$ and $\cos\omega t = \Im(je^{j\omega t})$, we

have

$$a\sin\omega t + b\cos\omega t = \Im[(a+jb)e^{j\omega t}], \tag{5.49}$$

which gives a one-to-one correspondence to phasor $a+jb$. Hence, v_{C_s} in (5.48) can be written in phasor form as

$$\dot{V}_{C_s} = a + jb = -\sqrt{0.5\,|V_{\text{grid}} I_m X_{C_s}|} - j\ \text{sgn}\,(I_m)\sqrt{0.5\,|V_{\text{grid}} I_m X_{C_s}|} \tag{5.50}$$

to facilitate the development of the vector diagram. Accordingly, $\dot{V}_{AB} = \dot{V}_{\text{grid}} = V_{\text{grid}} + j0$, $\dot{V}_{BC} = \dot{V}_{C_s}$ and $\angle\dot{V}_{BC} = +\frac{3}{4}\pi$ or $-\frac{3}{4}\pi$. The voltage relationships are shown in Figure 5.7, where O' is the center of circles having diameters V_{grid} and V_{dc}, as given in (5.45), (5.46) and (5.47). According to the vector directions shown in Figure 5.7, point C should be sliding along line BN making an angle of $\pm\frac{3}{4}\pi$ to line AB. Points A, B and C are confined within the circle centered at O' with radius $\frac{1}{2}V_{\text{dc}}$ due to $m_x \leq 1$. In the steady state, we have

$$|\dot{V}_{AB}| = V_{\text{grid}}, \text{ and} \tag{5.51}$$

$$V_{C_s} = |\dot{V}_{BC}| \leq |\dot{V}_{BN}| = \frac{\sqrt{2}}{4}V_{\text{grid}} + \frac{1}{2}\sqrt{V_{\text{dc}}^2 - \frac{1}{2}V_{\text{grid}}^2} \tag{5.52}$$

However, V_{C_s} has not been maximized, as will be shown later.

As increasing $|\dot{V}_{BC}|$ will give a smaller C_s, in this thesis, a modulation objective of maximizing v_{BC} will be adopted. With a maximized v_{C_s}, C_s can be minimized for the same amount of charge-storage capability. Specifically, a "zero-sequence" voltage $\dot{V}_{\text{zero}}$ will be added to separate the centers of the two circles of diameters V_{grid} and V_{dc}, as shown in Figures 5.8 and 5.9.

In Figure 5.8, we have $V_{\text{grid}} \leq V_{\text{dc}} \leq \sqrt{2}V_{\text{grid}}$. Voltages $\dot{V}_{AO'}$ and $\dot{V}_{BO'}$ are modulated with unity modulation index. Since $V_{\text{dc}} \geq V_{\text{grid}}$, point O' can be

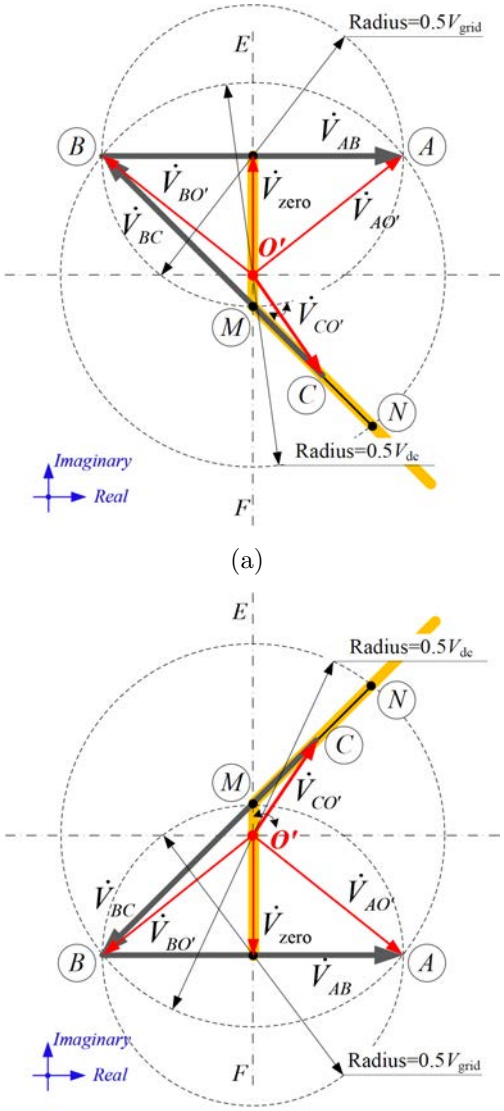


Figure 5.8: Vector diagrams of the proposed modulation strategy with $V_{\text{grid}} < V_{\text{dc}} \leq \sqrt{2}V_{\text{grid}}$ for (a) rectifier mode and (b) inverter mode.

assigned to move along the line of bisection EF perpendicular to line AB. The maximum value of $|v_{CO'}|$ can be designed equal to $|v_{AO'}| = |v_{BO'}|$, i.e., point C can be designed to overlap point N such that

$$\max\left(V_{C_s}\right) = |\dot{V}_{BN}| = V_{\text{dc}} \cos\left(\frac{\pi}{4} - \arccos\frac{V_{\text{grid}}}{V_{\text{dc}}}\right). \tag{5.53}$$

In Figure 5.9, we have $V_{\text{dc}} > \sqrt{2}V_{\text{grid}}$ and point O' deviates from line EF.

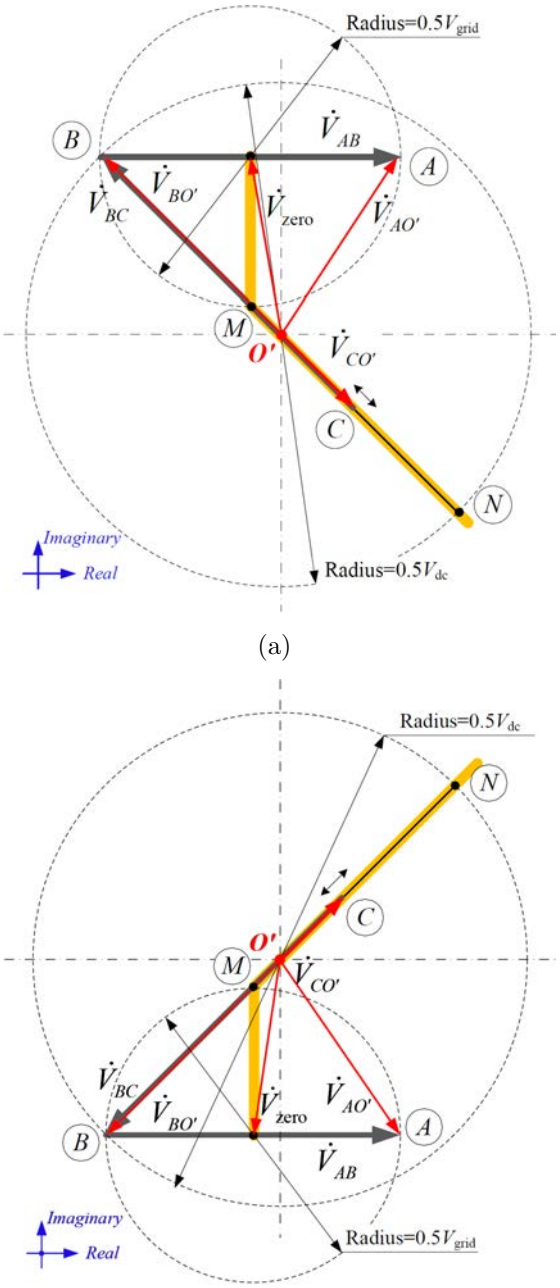


Figure 5.9: Vector diagrams of the proposed modulation strategy with $V_{\mathrm{dc}} > \sqrt{2}V_{\mathrm{grid}}$ for (a) rectifier mode and (b) inverter mode.

Only $\dot{V}_{BO'}$ can be modulated with unity modulation index. Point O' moves along MN. Although the modulation index of $\dot{V}_{AO'}$ is below one, the maximum value of $|v_{CO'}|$ can be designed equal to $|v_{BO'}|$, i.e., point C can be designed to overlap

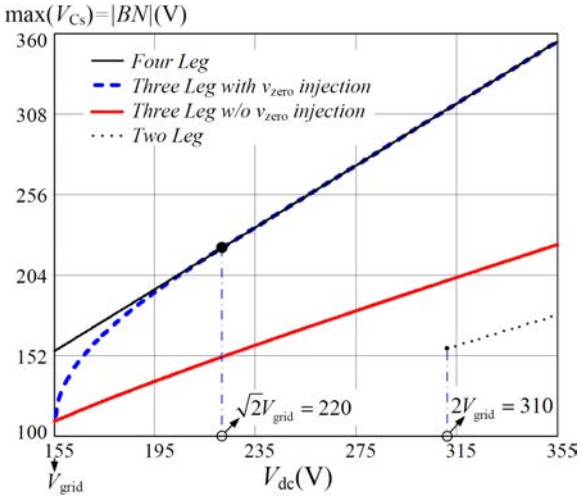


Figure 5.10: Comparison of achievable $\max(V_{C_s})$ using the four-phase-leg converter [77], the three-phase-leg converter without v_{zero} [67], the three-phase-leg converter with v_{zero} developed in this thesis and the two-phase-leg converter [79].

point N such that

$$\max(V_{C_s}) = |\dot{V}_{BN}| = V_{\text{dc}}. \tag{5.54}$$

A comparison of $\max(V_{C_s})$ using these two modulation techniques, i.e., equations (5.52), (5.53) and (5.54), is shown in Figure 5.10, where the converter is operated at $V_{\text{grid}} = 110\sqrt{2}$ V and $110\sqrt{2} \leq V_{\text{dc}} \leq 355$ V. In the proposed modulation, (5.53) is used for $V_{\text{dc}} \leq \sqrt{2}V_{\text{grid}} = 220$ V and (5.54) is used for $V_{\text{dc}} > \sqrt{2}V_{\text{grid}} = 220$ V. Also shown in Figure 5.10 are values of the modulated $\max(V_{C_s})$ for the four-phase-leg AC-DC SPWM converter shown in Figure 5.2 [77] and the two-phase-leg AC-DC SPWM converter [79], where the two-leg design must have $V_{\text{dc}} > 2V_{\text{grid}}$ as O' is restricted near point B at light load condition, as shown in Figures 5.8 and 5.9. With a much higher $\max(V_{C_s})$, the capacitance C_s will be designed smaller in Section 5.4.2.

In the time domain, voltage v_{zero} can be designed at minimum DC bus voltage

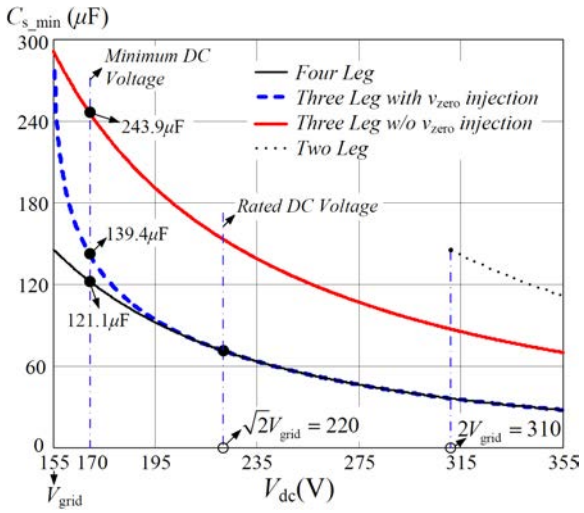


Figure 5.11: Comparison of achievable min (C_s) using the four-phase-leg converter [77], the three-phase-leg converter without v_{zero} [67], the three-phase-leg converter with v_{zero} developed in this thesis and the two-phase-leg converter [79].

$V_{\text{dc\_min}}$, i.e.,

$$v_{\text{zero}} = \frac{1}{2}V_{\text{dc\_min}} \sin(\omega t + \varphi_B) + \frac{1}{2}V_{\text{grid}} \sin \omega t, \tag{5.55}$$

where $\varphi_B = -\text{sgn}(I_m) \cdot \left[\frac{\pi}{2} + \arcsin\left(\frac{V_{\text{grid}}}{V_{\text{dc\_min}}}\right)\right]$ if $V_{\text{grid}} < V_{\text{dc\_min}} \leq \sqrt{2}V_{\text{grid}}$, or $\varphi_B = -\text{sgn}(I_m) \cdot \frac{3}{4}\pi$ if $V_{\text{dc\_min}} > \sqrt{2}V_{\text{grid}}$.

Eventually, the modulated voltages are modified by adding v_{zero} to equations (5.45), (5.46) and (5.47), i.e.,

$$v_{AO'} = (0.5v_{cm} - 0.5kv_{dm} + 0.5v_{\text{grid}}) + v_{\text{zero}}, \tag{5.56}$$

$$v_{BO'} = (-0.5v_{cm} + 0.5kv_{dm} - 0.5v_{\text{grid}}) + v_{\text{zero}}, \text{ and} \tag{5.57}$$

$$v_{CO'} = [-0.5v_{cm} + (0.5k - 1)\, v_{dm} - 0.5v_{\text{grid}} - v_{C_s}] + v_{\text{zero}}. \tag{5.58}$$

5.4.2 Comparison on AC Storage Capacitance

According to (5.48), we have

$$C_s = \frac{V_{\text{grid}}}{I_{\text{grid}}} \omega V_{C_s}^2 = \frac{2|p_{\text{grid}}|}{\omega V_{C_s}^2}. \tag{5.59}$$

The minimum AC storage capacitance should be designed at the maximum power point. For a given maximum power, if V_{C_s} can be higher, smaller capacitance can be employed. Thus,

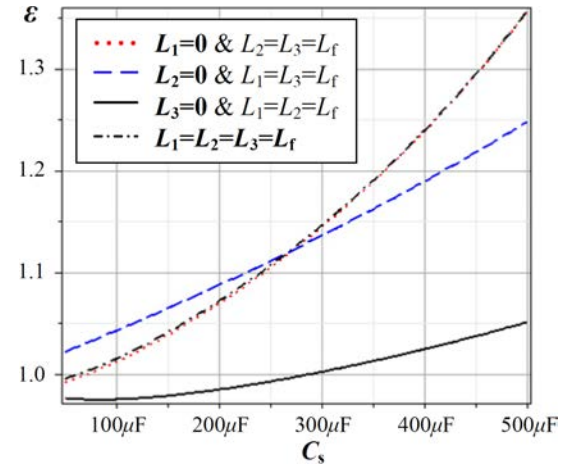
$$C_{s\_\min} = \frac{2|p_{\text{grid}\_\max}|}{\omega V_{C_s\_\max}^2}. \tag{5.60}$$

As an illustrative example, a converter is operating with the parameters shown in Table 5.2 and designed with $110\sqrt{2} \leq V_{\text{dc\_min}} \leq 355$ V, as described in Section 5.4 and equations (5.52) and (5.53). A comparison of the AC storage capacitance of the two modulation schemes is shown in Figure 5.11. A reduction of 42.8% capacitance value from 243.9 μF to 139.4 μF can be observed for the converter designed at $V_{\text{dc\_min}} = 170$ V. For this converter, a 144.7 μF AC film capacitor can be chosen for C_s. Also shown in Figure 5.11 for comparison are values of $C_{s\_\min}$ of the four-phase-leg converter [77] and the two-phase-leg converter [79].

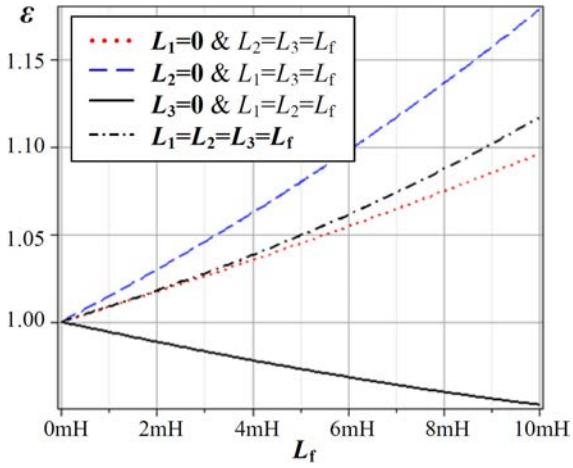
5.5 Verification

According to (5.6), the switching-frequency ripple-filtering inductors have contributions to the compensation of second-order harmonic AC power from the grid input. The amount of power compensated by the storage capacitor can be measured by a scalar ε defined as

$$\varepsilon = \frac{P_{C_s}}{P_{g\_2\omega}} = \frac{\sqrt{P_{C\_\sin 2\omega}^2 + P_{C\_\cos 2\omega}^2}}{|0.5 V_{\text{grid}} I_m|}, \tag{5.61}$$



(a)



(b)

Figure 5.12: Plots of ε for the family of converters at a grid power of 550 W (a) versus C_s with $L_f = 4$ mH and (b) versus L_f with $C_s = 144.7$ μF.

where P_{C_s} and $P_{g\_2\omega}$ are the amplitudes of powers stored in the capacitor and the second-order harmonic AC power from the grid input, respectively.

Using the analytical result developed in Section 5.3.2, ε is plotted in Figure 5.12 for the family of converters at a grid voltage of 110 V and power of 550 W. The results for the rectifier and inverter modes of operation are the same. Since L_3 and C_s are connected in series, p_{L3} is always in a reversed direction to p_{C_s}. Thus, part of p_{C_s} will be compensated by p_{L3}. As a result, the converter without L_3 always has the minimum value of ε and hence the smallest AC capacitor C_s.

We have performed simulations for each member converter of the family us-

ing the general control described in Section 5.3 and the modulation scheme in Section 5.4. The results show excellent performance. To achieve the smallest AC capacitor C_s, the converter without L_3 is chosen for verification of the analysis presented in this chapter. The main components are shown in Table 5.2. The AC capacitor has a value of 144.7 μF, as explained in Section 5.4.2. The DC capacitance can be determined from consideration of energy difference, i.e., $C_{\rm dc} = \frac{2\Delta P \cdot \Delta T_h}{V_{\rm dc\_ref}^2 - V_{\rm dc,min}^2}$, where ΔP is the output power change within ΔT_h, ΔT_h is the required holdup time and $V_{\rm dc,min}$ is the minimum DC bus voltage. Thus, substituting practical data of the prototype converter, the capacitance is found as $C_{\rm dc} = \frac{2 \cdot 250 \text{ W} \cdot 10 \text{ ms}}{(220 \text{ V})^2 - (170 \text{ V})^2} = 256$ μF. As $C_{\rm dc}$ also possesses AC-DC power balancing capability, we use $C_{\rm dc} = 200$ μF in order to have a better visualization of the residual voltage ripple resulting from the error due to power balancing of the AC capacitor C_s. The control algorithm is implemented using Table 5.2. The circuit shown in Figure 5.13 is also implemented using a MatLab model for verification purposes. The experimental prototype is implemented with a digital controller (MC56F84789) and an IPM module (FSBB30CH60C).

5.5.1 Hardware Realization

A converter without L_3 is constructed based on the block diagram shown in Figure 5.13 for experimental verification of the analysis developed in this thesis. A general description of the functional blocks has been given in Section 5.3. In this section, we will focus on the detailed hardware implementation. A practical implementation of the control described in Figure 5.13 is shown in Figure 5.14, where inductor parasitic resistors with $R_1 = R_2 = 0.1\,\Omega$ are included. The current controllers G_{v1} and G_{v2} for $i_{\rm grid}$ and i_{C_s} inside the functional block "Main Control Algorithm" of Figure 5.13 is redrawn in the s-domain, as shown in Figure 5.14(a). In Figure 5.13, output signals v_{cm} and v_{dm} are sent to the "Modulation" block to

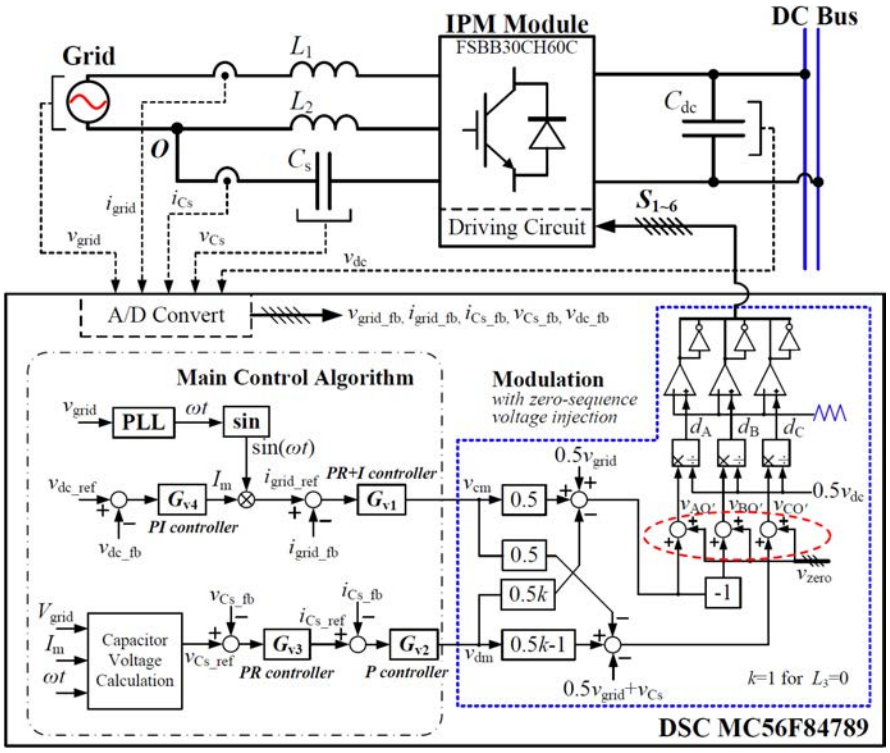
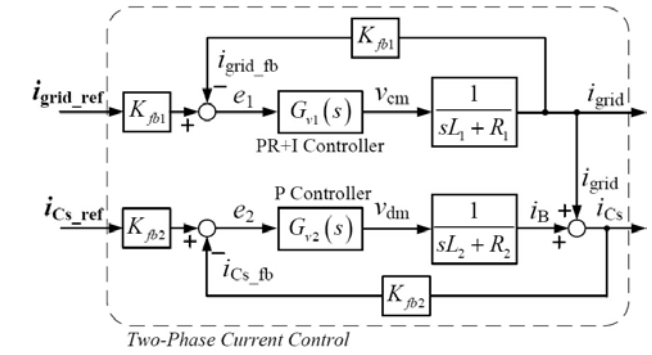


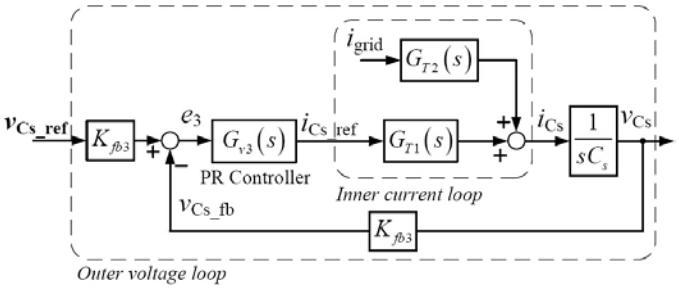
Figure 5.13: Block diagram of the bidirectional AC-DC bus power converter.

Table 5.2: Main parameters of an AC-DC bus converter

Grid Input Voltage v_{grid}	110 VAC
Grid Frequency f	50 Hz
DC Bus Voltage V_{dc}	220 V
DC Bus Capacitor C_{dc}	200 μF
Switching Frequency f_s	20 kHz
Maximum Power Capacity S_{max}	550 VA
Filter Inductor L_1	4 mH
Filter Inductor L_2	4 mH
Filter Inductor L_3	0 mH
AC capacitor C_s	144.7 μF
IPM Module	FSBB30CH60C
DSP Controller	MC56F84789



(a) Decoupled two-phase current control



(b) Dual loops for capacitor voltage control

Figure 5.14: Simplified models for control parameters design.

calculate the three-phase-leg reference voltages based on the model given in Figure 5.6. The reference voltages are compared with a common triangular carrier of frequency f_s which generates the corresponding PWM signals for driving switches S_1 to S_6. These SPWM modulated voltages at the three-phase legs are connected through the filtering inductors L_1 and L_2. The averaged three-phase-leg voltages can be regarded as the equivalent common-mode and differential-mode voltages v_{cm} and v_{dm}, as illustrated in Figure 5.6 with $L_3 = 0$. In Figure 5.6, v_{cm} is connected across L_1 to generate i_{grid}, and v_{dm} is connected across L_2 to generate i_B. Thus, in the s-domain, $i_{\text{grid}} = v_{cm}\frac{1}{sL_1+R_1}$ and $i_B = v_{dm}\frac{1}{sL_2+R_2}$, which are shown in Figure 5.14(a). As there is scaling of the sampled signals i_{grid} and i_{C_s} by 0.067 due to hardware and software implementation requirements, the reference signals $i_{\text{grid\_ref}}$ and $i_{C_s\text{\_ref}}$ are scaled down accordingly such that equivalent feedback factors $K_{fb1} = K_{fb2} = 0.067$ are incorporated as shown in Figure 5.14(a). The inner

current loop for power factor control uses a PIR controller given by

$$G_{v1}(s) = k_{p1} + k_{i1}s^{-1} + k_{r1}\frac{\cos\beta \cdot s + \sin\beta \cdot \omega_r}{s^2 + \omega_r^2}, \tag{5.62}$$

giving a loop gain of

$$G_{ol1}(s) = \frac{E_1(s)}{I_{\text{grid\_fb}}(s)} = \frac{K_{fb1}G_{v1}(s)}{sL_1 + R_1}. \tag{5.63}$$

Assigning $k_{p1} = 280$ and $k_{i1} = 10$, the cutoff frequency of the loop gain can be designed at 746 Hz with a phase margin of about 90°. With $k_{r1} = 650$, the loop gain of $G_{v1}(s)$ at $\omega_r = 100\pi$ is sufficiently large in order to reduce the steady-state error of the grid current. A β of $-\frac{\pi}{4}$ is used to acquire a sufficient phase margin at ω_r [19].

The function of power balancing is provided by $G_{v3}(s)$ of the outer voltage loop involving v_{C_s}, as shown in Figure 5.14(b). The inner current loop $G_{v2}(s)$ shown in Figure 5.14(a) is simplified to the following closed-loop transfer function:

$$I_{C_s}(s) = G_{T1}(s) \cdot I_{Cs\_\text{ref}}(s) + G_{T2}(s) \cdot I_{\text{grid}}(s), \tag{5.64}$$

where $G_{T1}(s) = \frac{K_{fb2}(sL_2+R_2)^{-1}G_{v2}(s)}{1+G_{ol2}(s)}$, $G_{T2}(s) = [1 + G_{ol2}(s)]^{-1}$ and $G_{ol2}(s) = \frac{E_2(s)}{I_{C_s\_\text{fb}}(s)} = \frac{K_{fb2}G_{v2}(s)}{sL_1+R_1}$ is the loop gain of $G_{v2}(s)$. The controller G_{v3} is a proportional-resonant (PR) controller given by $G_{v3}(s) = k_{p3} + k_{r3}\frac{\cos\beta\cdot s+\sin\beta\cdot\omega_r}{s^2+\omega_r^2}$.

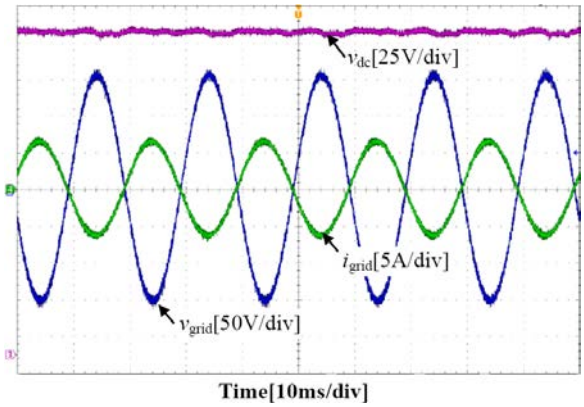
With scaling factor $K_{fb3} = 0.0023$, and the controller parameters $G_{v2}(s) = k_{p2} = 330$, $K_{p3} = 119.4$ and $K_{r3} = 955.2$, the cutoff frequency of $G_{ol2}(s) = \frac{E_2(s)}{I_{C_s\_\text{fb}}(s)} = \frac{K_{fb2}G_{v2}(s)}{sL_1+R_1}$ is 879 Hz with a phase margin of 90°, and the cutoff frequency of $G_{ol3}(s) = \frac{E_3(s)}{V_{C_s\_\text{fb}}(s)} = \frac{K_{fb3}G_{v3}(s)G_{T2}(s)}{sC_s}$ is 286 Hz with a phase margin of 72°. The closed-loop transfer function $G_{T2}(s)$ has a −24.9 dB attenuation at the grid frequency. Thus, i_{grid} has an insignificant effect on the steady-state error of i_{C_s}.

5.5.2 Performance of Control

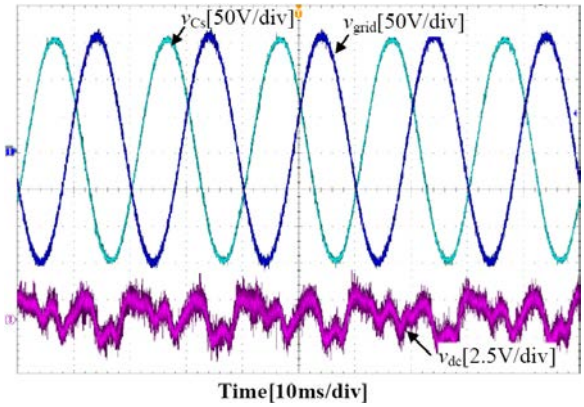
The experimental results measured from the prototype for stable operation in the rectifier mode are shown in Figure 5.15. As shown in Figure 5.15(a), the converter is operating as a rectifier, which maintains unity power factor and a constant DC bus voltage of 220 V. Figure 5.15(b) shows that the DC bus voltage ripple is about 2.5 V (peak to peak) due to the AC storage capacitor, whose voltage is leading the grid voltage by a phase angle of $\frac{3}{4}\pi$ approximately, and the voltage of the AC storage capacitor can approach that of the grid voltage at full load due to the use of the novel modulation method. The current waveforms of i_{grid}, i_B and i_{C_s} at steady state are shown in Figure 5.15(c). The transient responses to switching between half load and full load conditions are shown in Figure 5.16, which is realised by a series connection of a breaker and load resistance.

A DC power source, simulated by a DC voltage source having a value higher than the DC bus voltage connected in series with a power resistor, is connected to the DC bus with a DC breaker.

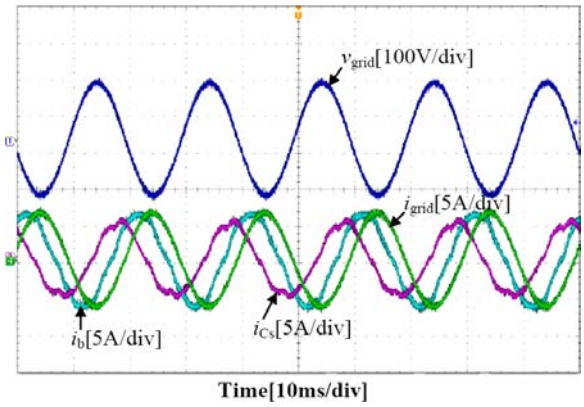
When the power source is connected, experimental results for the inverter operation are shown in Figure 5.17. The grid voltage and current are in phase and the DC bus voltage is kept at 220 V, as shown in Figure 5.17(a), indicating that power is being transferred from the DC source to the grid. Meanwhile, using the AC-DC power balancing scheme, the DC bus voltage ripple is kept below 2.5 V (peak to peak), as shown in Figure 5.17(b), where the AC storage capacitor voltage is lagging the grid voltage by a phase angle of $\frac{3}{4}\pi$ approximately. The phase relationships of the three currents are shown in Figure 5.17(c). The transient responses for the converter switching between rectifier and inverter modes are given in Figure 5.18. This verifies that the proposed control strategy is effective in the two modes of operation. We have also built a four-phase-leg prototype converter to measure the responses with conditions identical to Figures 5.15, 5.17 and 5.18.



(a)



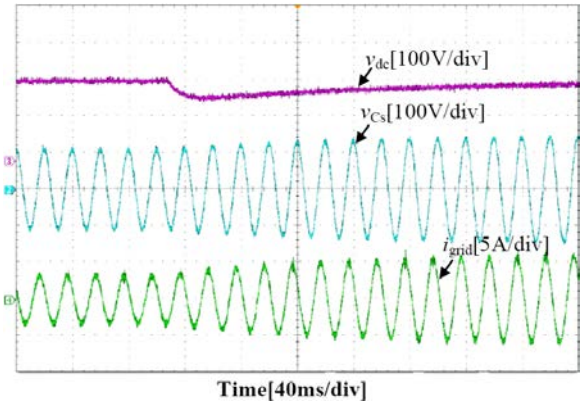
(b)



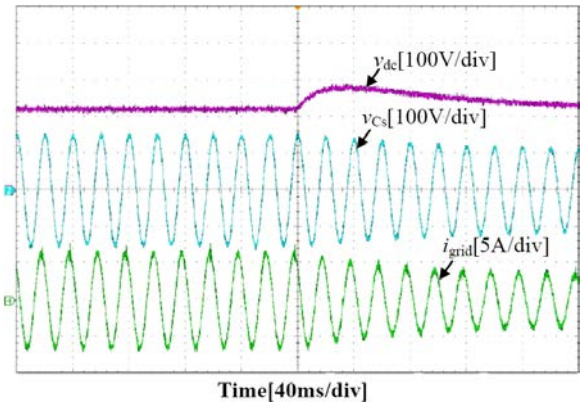
(c)

Figure 5.15: Experimental results for rectifier mode at stable operation. (a) DC bus voltage, grid input voltage and current; (b) DC bus voltage ripple and the phase relationship between grid voltage and AC storage capacitor voltage; (c) currents at steady state.

The results (omitted here for saving space) show no significant difference from those of Figures 5.15, 5.17 and 5.18, indicating that a three-phase-leg converter



(a)



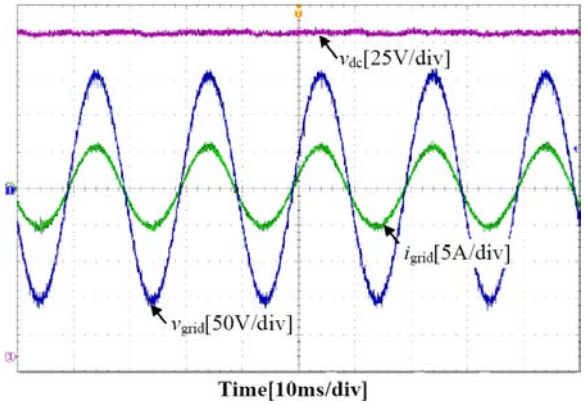
(b)

Figure 5.16: Transient process of stepping load for rectifier mode (a) from half load to full load; (b) from full load to half load.

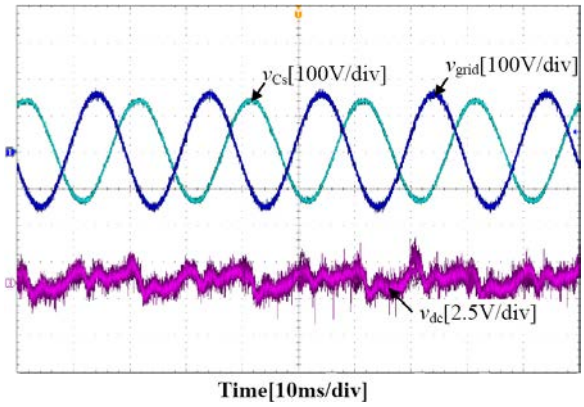
can perform as well as a four-phase-leg converter.

5.5.3 Performance of Modulation Methods

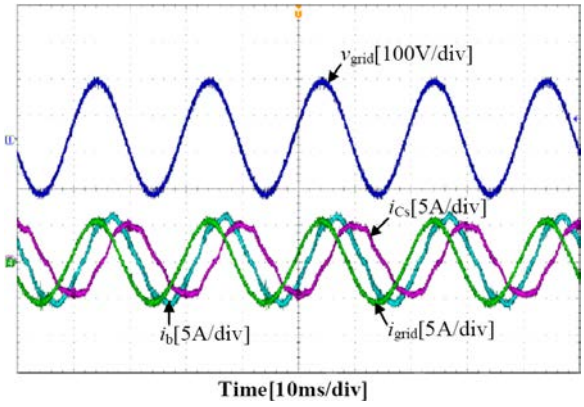
The performance of the proposed modulation technique for the three-phase-leg SPWM converter with v_{zero} is compared with the performance of the modulation presented in [67] at maximum power of 550 W in terms of real-time simulated waveforms at the three-phase legs A, B and C, as shown in Figure 5.19. The AC storage capacitor C_s is designed with a value of 144.7 μF at the minimum DC bus voltage $v_{\text{dc}} = 170$ V. Figure 5.19 shows the waveforms of modulation indexes $d_x = \frac{v_{xO'}}{0.5v_{\text{dc}}}$ for $x = A, B,$ and C, and the $d_{\text{zero}} = \frac{v_{\text{zero}}}{0.5v_{\text{dc}}}$ for the two modulation techniques. When the design with v_{zero} operates at maximum modulation indexes



(a)



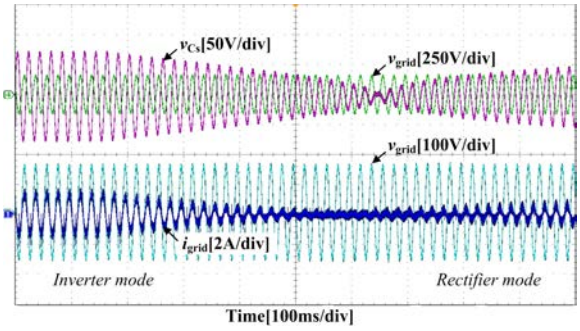
(b)



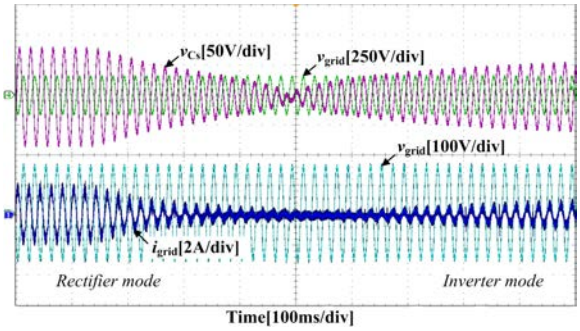
(c)

Figure 5.17: Experimental results for inverter mode operation. (a) DC bus voltage, grid input voltage and current; (b) DC bus voltage ripple and the phase relationship between grid voltage and capacitor voltage; (c) currents at steady state.

just confined within the peak values of carrier (±1 V), over modulation can be observed for the waveform of d'_C generated by the technique in [67]. For



(a)

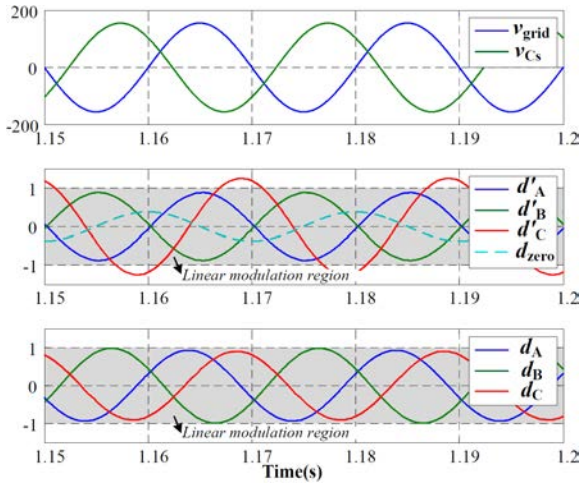


(b)

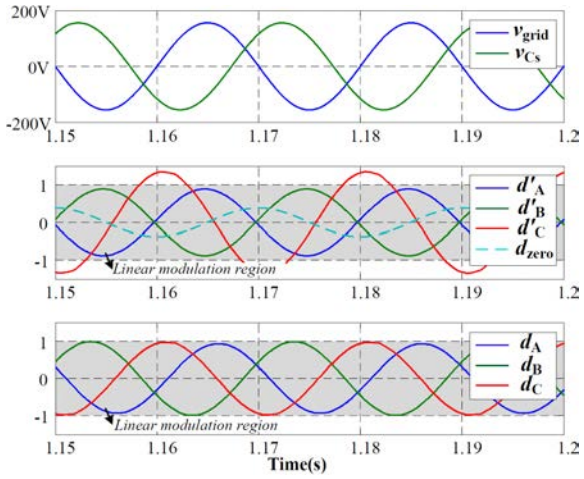
Figure 5.18: Transient waveforms of switching (a) from inverter mode to rectifier mode; (b) from rectifier mode to inverter mode.

comparison, the waveform of $d_{\text{zero}} = d_x - d'_x$ for $x = A, B,$ and C is also shown in the middle panel of Figure 5.19 to indicate how it corrects the over modulation of d'_C to d_C.

The efficiency improvement of operating the three-phase-leg converter at a power level with lower AC storage capacitance, higher capacitor voltage and lower capacitor current is given in Figure 5.20. The minimal AC storage capacitances used in the comparison at $v_{\text{dc,min}} = 170$ V are 144.7 μF for the three-phase-leg converter with v_{zero} injection, 244.7 μF for the three-phase-leg converter without v_{zero} injection and 120 μF for the four-phase-leg converter as given by Figure 5.11. Owing to the reduced conduction loss and switching loss at a lower current amplitude, the three-phase-leg converter with a smaller AC storage capacitance has a significantly higher efficiency. At the same power level, the four-phase-leg converter shows higher overall losses even though it has the smallest AC storage



(a)



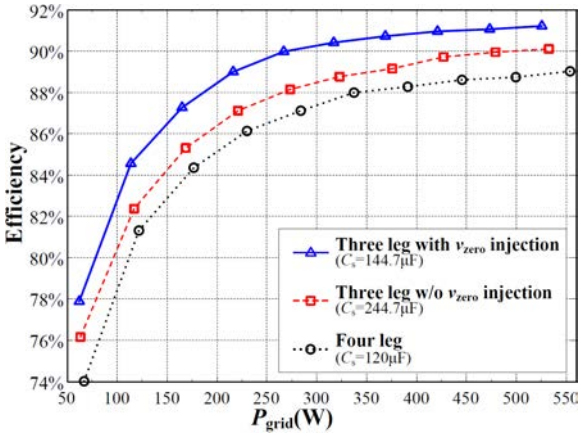
(b)

Figure 5.19: Comparison of simulated modulation waveforms at the three-phase legs A, B and C for the three-phase-leg SPWM converters without v_{zero} in the middle row (It is noted that the waveforms of d_{zero} belongs to the bottom row and is intentionally drawn here for comparison purpose.) and with v_{zero} in the bottom row operating at (a) rectifier mode and (b) inverter mode.

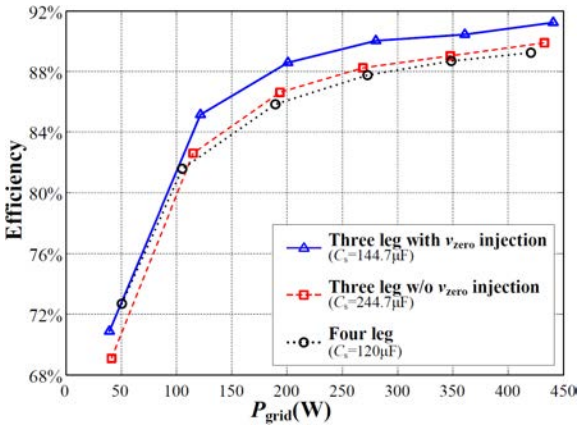
capacitance.

5.6 Summary

A family of single-phase AC-DC three-phase-leg sinusoidal pulse-width-modulation converters is designed with a general decoupled control structure and a modulation scheme sharing a common AC voltage in all phase legs of the converter,



(a)



(b)

Figure 5.20: Measured efficiency versus grid-side power for (a) rectifier mode and (b) inverter mode.

resulting in a minimized charge storage capacitance. The control is simple and effective. The modulation scheme has performance approaching that of a four-phase-leg converter. A comparison of the fundamental differences between two, three and four phase-leg converters are given. The control and modulation methods are verified with simulations and experimental measurements.

Chapter 6

Conclusion

This chapter summarizes the contributions which have been achieved in this project. Some possible future work and potential areas for further development are also presented.

6.1 Contributions of the Thesis

With the attractive luminous efficacy and long life span, LEDs are widely used in many commercial, domestic and industrial applications. In this thesis, electrolytic capacitor-less designs are investigated for LED applications. In terms of circuit topology, single-output LED drivers, multiple-output LED drivers and bidirectional single-phase AC-DC converters are studied in Chapter 3, 4 and 5, respectively. With these designs, electrolytic capacitors can be removed for a better system life span and a wider operating temperature. Specifically, the contributions of the thesis are stated as follows.

- Chapter 3 investigates the efficiency improvement for usual single-output LED drivers. From the perspective of power processing, since various cascaded LED drivers without electrolytic capacitors have not been optimized, a family of converters based on a minimum power processing structure are

proposed, having input power factor correction and output controlled dc constant current as well. One of these converters is selected for further verification, where a control uses the technique of carrier disposition for seamless splitting of the input power into two paths. An optimal portion of the input power goes directly to the dc output and the rest to a storage buffering path connected to the dc output. Since the storage capacitor is operated at a much higher voltage than the output voltage, a small non-electrolytic capacitor can be used.

- Chapter 4 investigates the single-inductor design for multiple-output LED drivers. An active power decoupling PFC SIMO LED driver is developed. In additional to the reduced inductor number, the proposed LED driver has benefits of a design without electrolytic capacitor, a near zero low-frequency ripple current for each output channel, a much smaller line filter and a much faster output current regulation for each output channel.

- Chapter 5 investigates the bidirectional AC-DC bus converters in a nanogrid system, where DC-DC LED drivers can be easily designed without electrolytic capacitors. A family of single-phase AC-DC three-phase-leg sinusoidal pulse-width-modulation converters is designed with a general decoupled control structure and a modulation scheme sharing a common AC voltage in all phase legs of the converter, resulting in a minimized charge storage capacitance. The control is simple and effective. The modulation scheme has performance approaching that of a four-phase-leg converter.

6.2 Suggestions for Future Work

Based on the previous works and experiences gathered in recent decades, and the work done in this project, suggestions for extensions and potential areas for

further studies are proposed here.

In Chapter 3, although a family of converters with a minimum power processing are proposed, only one of them has been verified and designed with a simple control strategy. It should be noted that other converters can also be designed to be low-power LED drivers or high-power PFC regulators, and thus their circuits characteristics and control design should be further investigated. Moreover, the minimum power processing structure considering control techniques, such as third-order harmonics injection [14] and PWM dimming and/or bi-level dimming [15] for a further reduced capacitance, could be analyzed. On the other hand, the simple control based on carrier disposition was inspired by the works of multi-level converters. Not limited to these, the carrier disposition technology could be explored and used for a seamless topology transition for other applications.

In Chapter 4, a PFC SIMO LED driver is derived from buck-boost converters. The use of time-multiplexing technology achieves independent output current regulation for multiple channels, but limits the number of channels. Efforts on topology or control should be made to remove the necessity of time multiplexing. Moreover, in terms of energy flow operation, more analysis and further optimization should be given. In terms of topology, more SIMO LED drivers without electrolytic capacitors could be developed and designed.

In Chapter 5, the voltage reference of AC capacitor is calculated with theoretical equations, which can be be considered as an open-loop approach. A general closed-loop approach could be further developed for the family of three-phase-leg converters. While, the zero-sequence voltage injection for SPWM modulation was only discussed for inverter mode and rectifier mode, and an analysis could be given for a general operation, where inductive and capacitive modes are involved as two specific cases.

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