ADVANCED SIC POWER DEVICES WITH ENHANCED SWITCHING PERFORMANCE BASED ON NUMERICAL SIMULATIONS

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CERTIFICATE OF ORIGINALITY

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Abstract

Power devices are essential and fundamental elements in power electronic circuits for controlling the current flows in switching operations. Traditionally, power devices are fabricated on silicon. Several representative power switches are thyristors, power bipolar junction transistors (BJTs), insulated gate bipolar transistors (IGBTs), power junction field effect transistors (JFETs), power metal oxide semiconductor field effect transistors (MOSFETs), etc. After development over several decades, silicon MOSFETs have become the dominant power switching devices in low-to-medium voltage range, while silicon IGBTs are the most popular power switch in medium-to-high voltage range. Apart from power switches, power rectifiers are also of significance in power electronics. The performance of these silicon based power devices is gradually reaching their theoretical limitation defined by the semiconductor material. The wide bandgap semiconductor silicon carbide (SiC) promises significant improvements in power device performance in terms of breakdown voltage, on-resistance, and thermal resistance, etc. At present, the most popular SiC power devices are SiC MOSFET as power switches and SiC junction barrier Schottky diode (JBS) as power rectifiers.

The development of SiC MOSFETs is challenged by the low electron mobility at the interface between the gate dielectric and SiC which results in a large channel resistance and thus boosts up the total ON-resistance (R_{ON}). The trench MOSFET structure is widely considered as a promising method, which allows a more compact cell design, and thus lowers the device R_{ON} by a higher channel density. When used in wide bandgap SiC devices, the trench MOSFET faces a critical issue for its commercial success: the high OFF-state oxide field at the trench bottom/corner.

An effective approach to reducing the maximum oxide field ($E_{ox\text{-}m}$) to a safe level (< 3 MV/cm) is to introduce a grounded p-shield region under the gate trench. However, the p-shield leads to the formation of a JFET region that presents a corresponding JFET resistance. Furthermore, the down-scaling of the unit cell is limited by the width of the current path in the JFET regions, hindering the effort to increase the channel density. In this thesis work, a SiC trench MOSFET solution is proposed for achieving a low R_{ON} in the SiC trench MOSFET by driving the MOS-gate and the JFET gate (the p-shield under the trench gate) simultaneously during device operation. The JFET portion is driven by the same gate-drive signal as the MOS-gate through a self-biasing network. This SiC trench MOSFET with a self-biased p-shield (SBS-MOS) boasts a widened current path in the JFET region at the ON-state, which lowers the JFET resistance and/or allows a further size reduction of the cell pitch.

For the SiC trench MOSFET with a p-shield, an appreciable chip area has to be sacrificed in order to contact the p-shield region. In this thesis work, a trench MOSFET structure with protruded p-bodies (PB-MOS), i.e. p-bodies deeper than the gate trench, is proposed. No additional p-shield regions are required. The lateral pinch-off effect of the protruded p-bodies in the PB-MOS protects the gate trench from the high OFF-state drain voltage, leading to a lower OFF-state oxide field. A low R_{ON} and a high breakdown voltage are maintained in the PB-MOS. The PB-MOS further boasts a much improved C_{rss} and better switching performance compared to the conventional SiC trench MOSFET.

The junction barrier Schottky diode (JBS) is the most popular rectifier among SiC based rectifiers since it features the merits of the fast switching and low turn-on voltage of a typical Schottky barrier diode as well as the merits of a high breakdown

voltage due to the integrated pn junction. Recently, some research studies suggest a Schottky contact to the p-grid in power devices, including the SiC JBS. For the SiC JBS, a rectifying Schottky contact to the p-grid suppresses the minority carrier injection from the p-grid, which avoids the possible bipolar degradation well known in SiC technology. In this thesis work, the role of the contact to the p-grid is comprehensively discussed. It is found whether a Schottky contact or an Ohmic contact do not impact on the static characteristics of the JBS. However, in the switching operation, the JBS with Schottky contact to p-grids would suffer a severe degradation in the *I-V* characteristics, including a larger turn-on voltage and a higher resistance. The mechanism behind this degradation is identified with the storage of negative charges in the p-grid. The rectifying Schottky contact allows charging the p-grids with a high reverse bias, but hinders the release of the negative charges in the p-grids. Therefore, a non-rectifying contact to the p-grid is essential for the switching operation of the SiC JBS.

List of Publications

[1] **M. Zhang**, J. Wei, H. Jiang, K. J. Chen, and C.-H. Cheng, "SiC trench MOSFET with self-biased p-shield for low R_{ON} and low OFF-state oxide field", *IET Power Electronics*, vol. 10, no. 10, pp. 1208-1213, 2017. DOI:10.1049/iet-pel.2016.0945. [Grade A, Impact factor = 3.547]

[2] **M. Zhang**, J. Wei, H. Jiang, K. J. Chen, and C.-H. Cheng, "A new SiC trench MOSFET structure with protruded p-base for low oxide field and enhanced switching performance", *IEEE Transactions on Device and Materials Reliability*, vol. 17, no. 2, pp. 432-437, 2017. DOI: 10.1109/TDMR.2017.2694220. [Grade B, Impact factor = 1.575]

[3] **M. Zhang**, P.-F. Chong, and C.-H. Cheng, "A MEMS switch with novel stopper structure and improved fabrication processes for power applications", in *Asia-Pacific Conference of Transducers and Micro-Nano Technology*, Kanazawa Japan, Jun. 2016.

[4] J. Wei, **M. Zhang**, H. Jiang, C.-H. Cheng, and K. J. Chen, "Low ON-resistance SiC trench/planar MOSFET with reduced OFF-state oxide field and low gate charges," *IEEE Electron Device Letters*, vol. 37, no. 11, pp. 1458 - 1461, 2016. [Grade A, Impact factor = 3.048]

[5] J. Wei, **M. Zhang**, H. Jiang, S. To, S. H. Kim, J.-Y. Kim, and K. J. Chen, "SiC trench IGBT with diode-clamped p-shield for oxide protection and enhanced conductivity modulation," in *ISPSD*, Chicago, USA, 2018. (Accepted)

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CHAPTER 1 Introduction

1.1 Background

The harnessing of electricity is one of the greatest achievements in the history of human beings. For a sustainable environment, electricity other than conventional energy such as oil, gas, and coal, is preferred. The demanding of electricity is increasing dramatically nowadays. From last century, the widespread use of semiconductor in power electronics has appreciably improved people's lives. Semiconductor devices are widely utilized as switches, rectifiers, amplifiers and so on, in integrated circuits. There are many parameters to define the electrical energy, such as voltage, current, frequency, etc. Power conversion technology is aimed as regulating the electrical energy, so as to modify the electricity to the desired form. Figure 1-1 shows a power converter, which converts the input voltage level to the desired value. The output voltage level is controlled with the time ratio the power switch Q is on. The power diode D is used as a freewheeling diode to continue the current through the inductor when Q is off, otherwise a high voltage spike would be created across the inductor L.

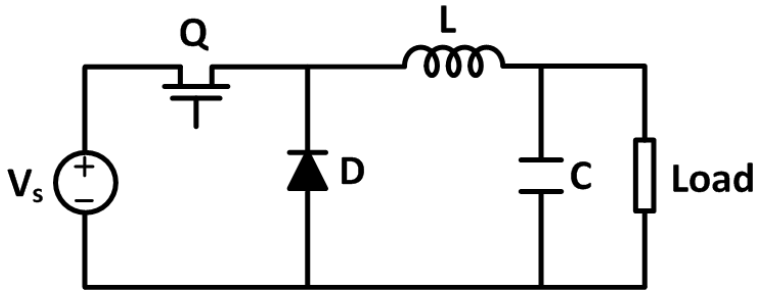


Figure 1-1 The circuit diagram of a buck converter.

Germanium (Ge) was chosen as a semiconductor in the beginning of semiconductor industry, but silicon (Si) now prevails because of its superior semiconductor-oxide interface, as well as its larger bandgap that leads to better stability at high temperature. With more and more mature processes, Si becomes the dominant semiconductor in digital integrated circuits. With mature processing technologies readily available, Si based devices have also gained remarkable success for power electronic applications. Actually, the most popular power devices in the market are Si MOSFETs and Si IGBTs nowadays. However, Si is not naturally a good material for power devices. For power devices, a high breakdown voltage is required, and Si based power devices need a long drift region to sustain this high voltage, which leads to a high on-state resistance. Wide bandgap semiconductors, such as gallium nitride (GaN) and silicon carbide (SiC), have a much larger critical breakdown electric field [1]. Therefore, to sustain the same breakdown voltage, SiC based power devices need a much shorter drift region than their silicon counterparts, which results in a much smaller on-state resistance. The lack of mature technology to prepare GaN substrates has hindered the development of GaN based power devices. Currently, the most popular GaN power device is the HEMT, typically fabricated on heterostructures grown on a hetero substrate, and is favorable for relatively low voltage high frequency applications [2].

This thesis will focus on SiC based power devices. The material and processing technologies for SiC are more mature compared to GaN. With the availability of native SiC substrates, vertical power devices are typically fabricated on SiC, which are more suitable for high voltage devices since the chip area does not scale with the requirement of breakdown voltage.

1.2 Research gaps

With the demand of higher and higher breakdown voltage, Si based power devices are approaching their limit, since the power loss in Si based power devices is more and more serious. SiC based power devices can provide a ten times higher critical field for avalanche breakdown and thus a shorter drift region is demanded. Thus, a smaller specific ON-resistance can be achieved in SiC based power devices than Si based power devices. Figure 1-2 shows the so-called material dependent limit [3]. Hence SiC based power devices are preferred in ultra-high voltage applications.

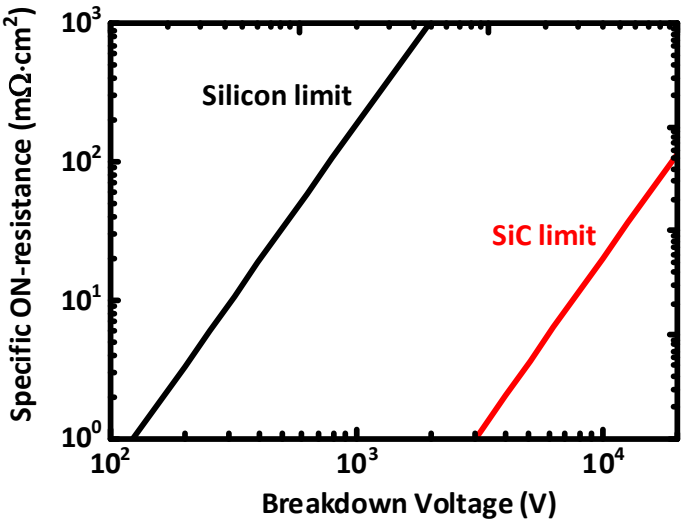


Figure 1-2 Material limits for unipolar power devices

The SiC planar MOSFETs suffer from a low channel mobility and thus a high channel resistance. The SiC trench MOSFET is an effective approach to reduce the device's channel resistance by increasing the channel density. But there are still several challenges to be addressed. Furthermore, the p-grids have been widely applied to form

PN junctions in SiC power devices as a voltage blocking structure. For certain devices, the impact of the contact to p-grid is not fully clear.

1. High OFF-state electric field in gate oxide

Because the high critical field in SiC, the OFF-state oxide electric field in SiC trench MOSFET can be much higher than 3 MV/cm which is commonly regarded as the maximum gate oxide electric field for long term safety applications

2. JFET effect between p-shields

SiC trench MOSFET with a grounded p-shield located under the trench gate has been demonstrated to screen the gate oxide from the high OFF-state electric field. However, it brings another issue that the JFET effect between neighboring p-shields leads to more power loss.

3. Low area efficiency

The grounded p-shield in SiC trench MOSFET has to be connected out to source. Therefore, another issue caused by the SiC trench MOSFET with a grounded p-shield is the surface contact area of the grounded p-shield.

4. The difference between Ohmic or Schottky contact to p-grids in SiC JBS

For a SiC JBS, the p-grid could help the device to block a high reverse voltage while at the same time reduce the electric field at the anode electrode, no matter the contact to p-grid is a Schottky contact or an Ohmic contact. However, detailed study of the role of the contacts to the p-grid is still missing, and the influence of contact to

p-grid upon the switching performance is not well understood leading to working on less good devices.

1.3 Objectives

Given the above issues, the research in this thesis aims to improve the performance of SiC power devices. SiC trench MOSFET with a grounded p-shield is the state-of-the-art SiC trench MOSFET. Based on it, some improvements are proposed and studied in this thesis. In SiC power devices, normally there are Ohmic contact and Schottky contact to p-grid between metal and semiconductor. Apart from electrical conduction, other functions of the contacts to p-grids are needed to be studied. The specified objectives of the research are:

1. To lower the maximum OFF-state oxide electric field in SiC trench MOSFET, and at the same time to ensure a weaker JFET effect in order to achieve a smaller resistance at on-state in power applications.
2. To achieve a higher chip surface area efficiency in SiC trench MOSFET than the state-of-the-art SiC trench MOSFET with a grounded p-shield and at the same time keep the device characteristics as well as or better than the state-of-the-art SiC trench MOSFET with a grounded p-shield.
3. To explore the suitability of an Ohmic contact and a Schottky contact to p-grid in SiC power devices in both static and dynamic characteristics.

1.4 Organization of this thesis

The work presented in this thesis is based on SiC power devices.

In chapter 1, the background, research gaps and objectives are included.

In chapter 2, the advantages of the SiC semiconductor, the reason for the choice of 4H-SiC based power devices, the bulk growth of a single SiC crystal, device processing method, as well as several popular SiC based power devices are introduced.

In chapter 3, the flow of research method is introduced and the software used is introduced. Based on the software, the meshing method as well as the evaluation criteria used in this study are also illustrated.

In chapter 4, considering the current improvement of the trade-off between the gate oxide electric field and R_{ON} by alternating the structures of the SiC trench MOSFET, a biasing circuit is harnessed to provide a novel way to arrive the same aim as in the proposed SiC trench MOSFET with a self-biased p-shield (SBS-MOS). The detailed considerations in the design of SBS-MOS are presented. Comparison is made with conventional trench MOSFET without the p-shield (C-MOS) and that with a grounded p-shield (GS-MOS), which suggests the proposed SBS-MOS better performances.

In chapter 5, a SiC trench MOSFET with protruded p-bodies (PB-MOS) is proposed, which features protruded p-bodies to shield the gate oxide at the trench bottom against the high OFF-state drain voltage. Its working mechanism is illustrated with a feasible fabrication process. Both the static and switching performance are compared with C-MOS.

In chapter 6, a case study with the SiC junction barrier Schottky diode (JBS) is carried out to study the differences between the Schottky contact and Ohmic contact to p-grid. It is found that the static characteristics of the SiC JBSs, whether with Schottky contact or Ohmic contact to the p-grids, are almost the same. However, the switching performance of the SiC JBS with a Schottky contact to the p-grid is severely

degraded. The reasons for this phenomenon are deeply illustrated with the simulation results for verification.

Chapter 7 makes overall conclusions for this thesis and the relevant study is suggested for future work.

CHAPTER 2 Literature Review

2.1 Crystal structures of SiC material

SiC is a well-known example of polytypism, i.e. the material has different crystal structures. The stacking sequence decides the polytype of SiC. Three popular SiC polytypes are 3C-SiC, 4H-SiC and 6H-SiC, as shown in Figure 2-1 [4]. Here A, B, and C stand for different stacking positions of the lattice points. The repeating stacking sequences of 3C-SiC, 4H-SiC and 6H-SiC are ABCABC…., ABAC… (or ACAB…), and ABCACB…, respectively.

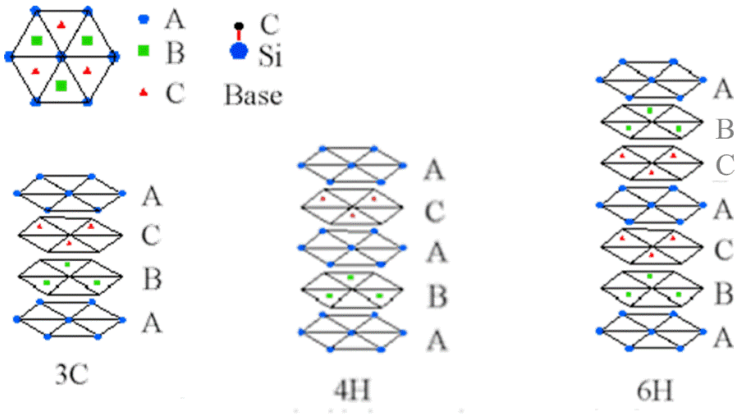


Figure 2-1 The stacking sequence of 3C, 4H and 6H polytypes of SiC.

3C-SiC is formed in cubic crystal lattice structure, while the crystal structures of 4H- and 6H-SiC are hexagonal. Cubic crystals can be illustrated in a three-dimensional Cartesian coordinate system. For hexagonal crystals, four-parameter Miller-Bravais lattice coordinates x, y, z and c, can be used. The crystal direction of SiC can be distinguished with Miller indices. For example, in Figure 2-2, the c-axis is denoted by <0001> Miller indices in 4H-SiC. The Si atom on Si face (also called (0001) face) is bonded along <0001>. The other face where the C atom is on and bonded along

<000-1> is called C face. Apart from the Si face and the C face, other two major faces in a hexagonal structure are the (1-100) and (11-20) faces, as shown in Figure 2-3 [5]. The chemical and electrical characteristics are quite different on different crystal faces.

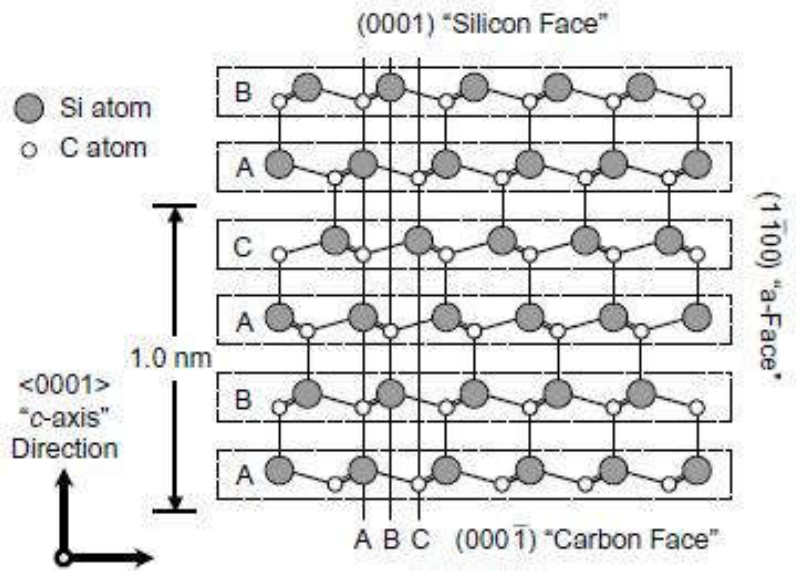


Figure 2-2 Schematic illustration of Si-C bond in a hexagonal SiC polytype.

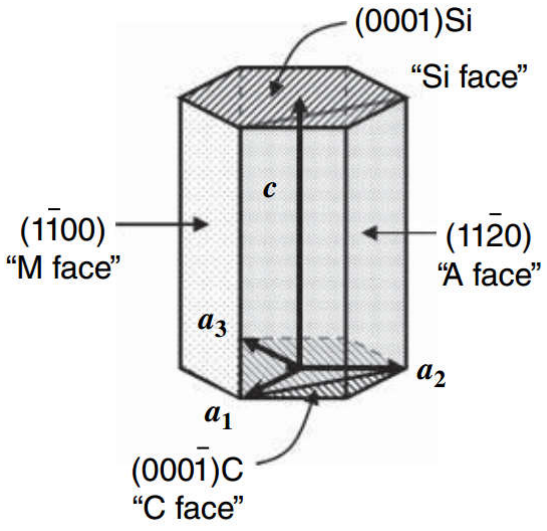


Figure 2-3 Definition of several major faces in the hexagonal crystallographic notation of SiC crystal.

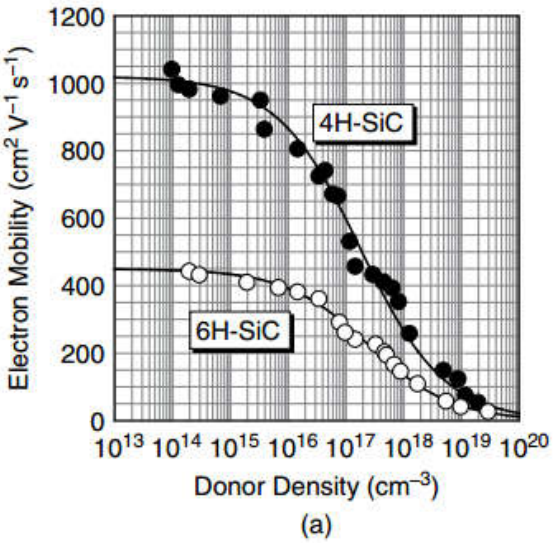
Table 2-1 Physical properties of 3C-SiC, 4H-SiC and 6H-SiC[a]

	Unit	3C-SiC	4H-SiC	6H-SiC
Bandgap, E_g	eV	2.4	3.2	3.0
Critical field, E_c	V/cm	2e6	2.2e6	2.5e6
Saturated electron drift velocity	cm/s	2.5e7	2e7	2e7
Electron mobility[b]	$cm^2/V\text{-}s$	1000	950	500
perpendicular to c-axis				
Electron mobility[b]	$cm^2/V\text{-}s$	1000	1200	100
parallel to c-axis				
Hole mobility[b]	$cm^2/V\text{-}s$	40	120	80
Dielectric constant	nC·mΩ	9.7	10	10

[a]At room temperature

[b]At low doping

Due to the different stacking sequences, 3C-SiC, 4H-SiC and 6H-SiC have different physical characteristics, as shown in Table 2-1 [6-9]. If the temperature, doping density, and other factors are same, 4H-SiC and 6H-SiC have much larger bandgaps than 3C-SiC. The mobility of materials is mainly influenced by the doping density and temperature. Figure 2-4 shows the mobility of 4H-SiC and 6H-SiC in the direction perpendicular to the c-axis. The 4H-SiC features higher electron and hole mobility than 6H-SiC at room temperature [5]. Mobility decreases when the doping density goes higher and higher, because the impurity scattering is enhanced. When the temperature is increased, crystal scattering can be a remarkable factor in decreasing the mobility.



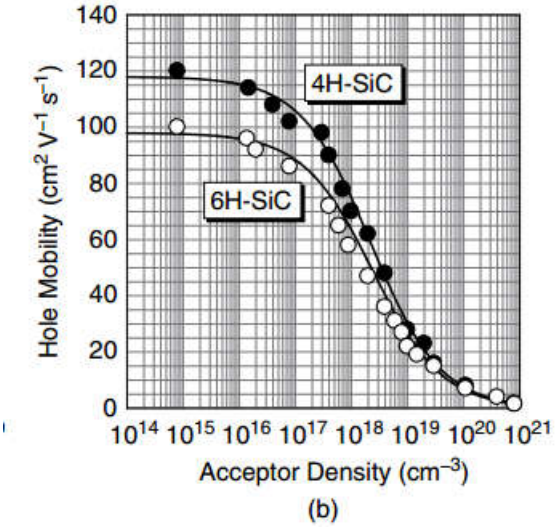


Figure 2-4 (a) Influence of donor density on low field electron mobility, (b) influence of acceptor density on low field hole mobility.

Mobility anisotropy is well known in 6H-SiC. The electron mobility along the c-axis is much smaller than the mobility perpendicular to the c-axis (at room temperature, maximum electron mobility along c-axis is about 100 $cm^2/V\text{-}s$) [10, 11]. However, the mobility anisotropy is much smaller in 4H-SiC. Mobility along the c-axis is only about twenty percent higher than that perpendicular to the c-axis.

The critical field is one of the significant parameters in semiconductors. It is short for the critical breakdown electric field. When the electric field in a semiconductor junction reaches this critical field, the junction will suffer from a breakdown. Due to the wide bandgap in 4H-SiC and 6H-SiC, their critical fields are larger than 3C-SiC.

2.2 Single crystal growth of SiC

2.2.1 Bulk growth of SiC

As an old natural material, SiC exists mainly in its polycrystalline form. The growth of a single crystal was first invented by Lely [12]. A schematic illustration of this method is shown in Figure 2-5. A SiC source is put in a graphite crucible which is circumscribed with a thermal insulator. The radio frequency (rf) coil outside is applied as a heat source for this set up. Inside the SiC source is porous graphite and a growth cavity. When the SiC source is heated to about 2500°, SiC sublimes, goes through the porous graphite and then sets on the graphite. However, SiC platelets grown in this way are small and the large ones are mainly in the range of 1~2 cm^2. For power device substrates which are usually required to be larger than tens of cm^2, this growth method is not suitable for substrate preparation. The shapes are also not unified. The polytype is mainly 6H-SiC mixed with other polytypes.

Tairov and Tsvetkov invented another SiC growth method with a seed crystal [13, 14] which is also called “modified Lely method”. The schematic illustration of the growth method is shown in Figure 2-6. The crucible is evacuated, filled with inert gas in a certain required pressure and heated to a certain temperature. The seed crystal with a single crystal polytype helps to decide the polytype of the grown SiC crystal.

The temperature of the seed is much smaller than the SiC source. So, similar to the principle of the Lely method, when a SiC source is heated to sublimation, the SiC gas is led to bond with the seed crystal. As silicon is consumed in a faster speed than carbon, the source material gradually becomes carbonized as the growth continues. The growth has to be stopped to renew the source material. Therefore, the volume of the SiC bulk is limited, which makes the cost of the SiC wafers very high compared to silicon wafers.

The temperature and pressure in the modified Lely method have to be controlled for single polytype substrate growth. It is found 6H-SiC is preferably grown on the SiC (0001) face at high temperature and pressure, while 4H-SiC is easily obtained at lower temperature and pressure [15]. 3C-SiC, as a metastable polytype, is unstable at high temperature and so is difficult to be grown by the sublimation method. In order to obtain a single crystal with good quality, the modified Lely method has now been refined. After the step controlled method used in SiC epitaxial growth, it was also applied in SiC sublimation growth. The step controlled method is illustrated in the next epitaxial growth part.

Nitrogen is a well known n-type dopant in SiC. Adding small amounts of gaseous nitrogen in the crucible in Figure 2-6 can make n-type SiC crystals [16]. Nitrogen doping is an exception, as doping SiC with other dopants in the sublimation method is much more difficult. Vanadium and aluminum are important dopants used for high-resistivity semi-insulating SiC crystals and conductive p-type SiC crystals, respectively. As solid dopants, they are admixed in SiC source for doping [17].

The commercialization of the SiC semiconductor owes much to the modified Lely method. In the 1990s, the SiC wafers were commercialized by Cree Inc. in USA. The availability of the commercial SiC wafers dramatically accelerated research on SiC based devices since then.

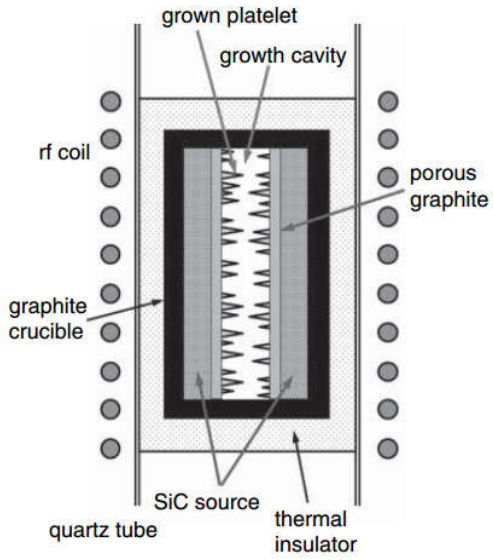


Figure 2-5 A schematic illustration of SiC bulk growth with Lely method.

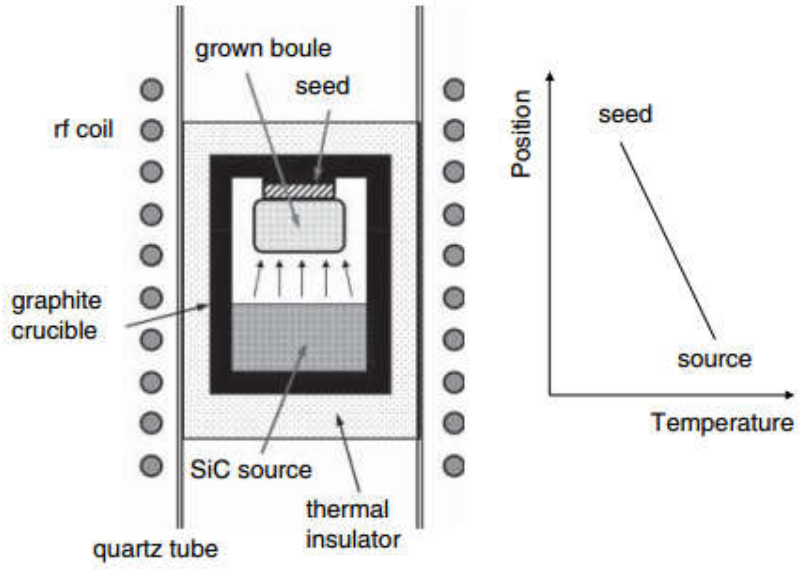


Figure 2-6 Schematic illustration of SiC bulk growth with the modified Lely method and approximate temperature profile.

2.2.2 Epitaxial growth of SiC

To develop SiC based power devices, epitaxial layers on substrate with a precisely controlled thickness and doping concentration are critically important, and determines the device breakdown voltage. High temperature chemical vapor deposition (HTCVD) [18, 19] has been currently widespread as an epitaxial technique for SiC growth. Figure 2-7 shows the set up. The growth is carried out in a crucible made of graphite. The precursor gas flows upward under a typical temperature of 2100~2300 °C. SiH_4 and hydrocarbon are included as the precursor gases. The precursor gas is flowing under a carrier gas environment. Hydrogen is generally used as the carrier gas.

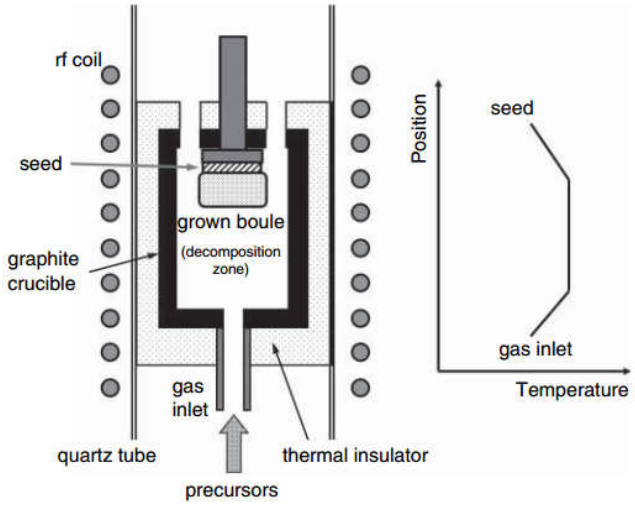


Figure 2-7 Schematic illustration of HTCVD and approximate temperature profile.

As discussed previously, multiple polytypes exist for SiC due to the difference in the stacking sequence. This adds to the complication of the epitaxial growth of SiC. Imagining that a SiC substrate with the surface terminated with a layer of position A in Figure 2-1, then the atoms on the surface could adopt either position B or position

C. Therefore, the polytype of the epitaxial layer is unable to be effectively controlled, as shown in Figure 2-8. A step controlled epitaxial technique has been found as an efficient way to control the polytype of the SiC epitaxial layer. With the substrate cut with a certain off-axis angle, the SiC surface exhibits the stacking steps, as shown in Figure 2-9 [20]. It can be seen, at the step, that the position is determined by the step edge, and only one of A, B, and C occupations is possible for each step, which ensures the total polytype of this crystal [21]. Currently, off-axis 4H-SiC wafers with 4-degree off-axis towards the (11-20) direction are typically used in the industry, and could be considered as a standard technology.

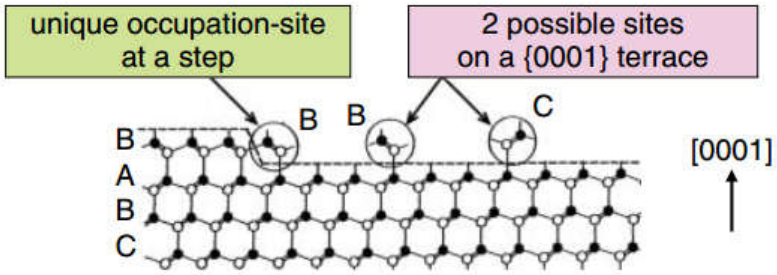


Figure 2-8 Schematic illustration of bond configuration on-axis and at a step in SiC growth.

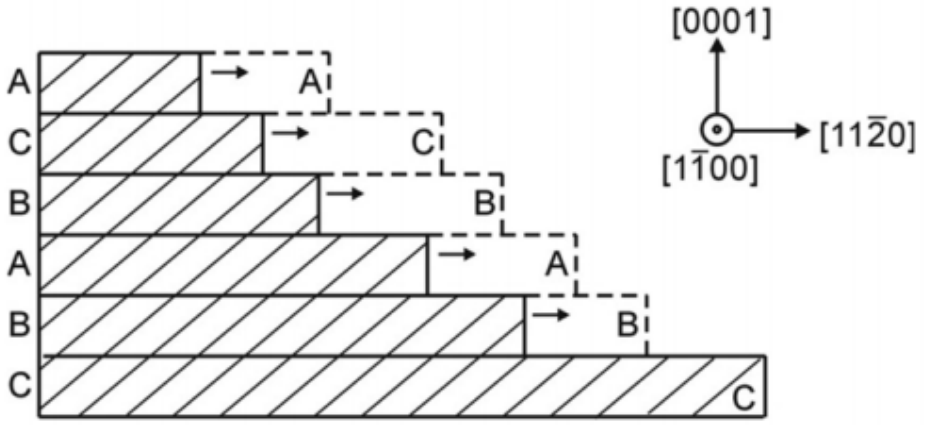


Figure 2-9 Schematic illustration of single crystal type growth of step-controlled epitaxy.

Precise control of doping in the epitaxial layer is critical in determining the characteristics of a power device, such as the ON-state resistance (R_{ON}), breakdown voltage, etc. Nitrogen is typically used for n-type doping in the SiC epitaxial layer, while aluminum is usually used for p-type doping. Nitrogen doping is performed by introducing some nitrogen gas into an inert gas environment (argon gas, for example). For p-type doping in SiC CVD growth, adding some TMA: $Al(CH_3)_3$ can be helpful [22].

2.3 Details in choosing SiC material for power MOSFET

The 4H-SiC wafer with 4 degrees off-axis angle towards the (11-20) direction is a standard solution for SiC power devices. The following illustrates in detail the reasons for this standard solution.

There are three popular SiC polytypes, 3C-SiC, 4H-SiC and 6H-SiC. The detailed physical characteristics of them are shown in Table 2-1.

Among them, 3C-SiC has a much smaller energy bandgap and so is not favorable for power devices. What's more, the 3C-SiC crystal is also not thermally stable and is easy to be transformed to other polytypes when the temperature is changed [23, 24]. 6H-SiC drew a lot of attention at the early stage of SiC devices. 6H-SiC features comparable bandgap to 4H-SiC, and the material growth of 6H-SiC is easier than 4H-SiC. One advantage of 6H-SiC is that the electron mobility in the 6H-SiC MOS-channel is found to be higher than that in the 4H-SiC MOS-channel. However, the bulk electron mobility in 6H-SiC is much lower than 4H-SiC, and manifest mobility anisotropy exists in 6H-SiC. In 6H-SiC, electron mobility perpendicular to the c-axis is about 500 cm^2/V-s, while the mobility along c-axis is only about 100 cm^2/V-s [10]. The electron mobility anisotropy is much smaller in 4H-SiC, with a mobility of about 1200 cm^2/V-s along the c-axis and about 900 cm^2/V-s perpendicular to the c-axis. Besides, the anisotropy of critical field exists in 6H-SiC. The critical field in the direction <11-20> is fifty percent smaller than that in the direction <0001> [25]. 4H-SiC has a much smaller anisotropy with the critical field in the direction <11-20> twenty percent smaller than that in the direction <0001> [26, 27]. The higher electron mobility and the higher critical breakdown field along the c-axis make 4H-SiC the most desired SiC polytype for fabricating power devices.

In the part of SiC epitaxial growth, the step control method is described and an off-axis direction of <11-20> is preferred. The choice of the off-axis direction is <11-20> rather than <1100> due to the induced stripe-like morphology and also pronounced step bunching on SiC grown on Si (0001) substrates inclined to <1100> [28, 29].

Besides, the choice of the 4 degrees off-axis angle has been carefully designed. Figure 2-10 shows the influence of the off-axis angles on the growth rate at different

temperatures [30]. With small off-axis angles, the growth rate is also very small. Rough surfaces also appear in crystals with small off-axis angles [31]. With a larger off-angle, the growth rate is enhanced and the surface of the crystal is smoother. However, crystal waste is increased when slicing large off-angle wafers [32], which increases the cost.

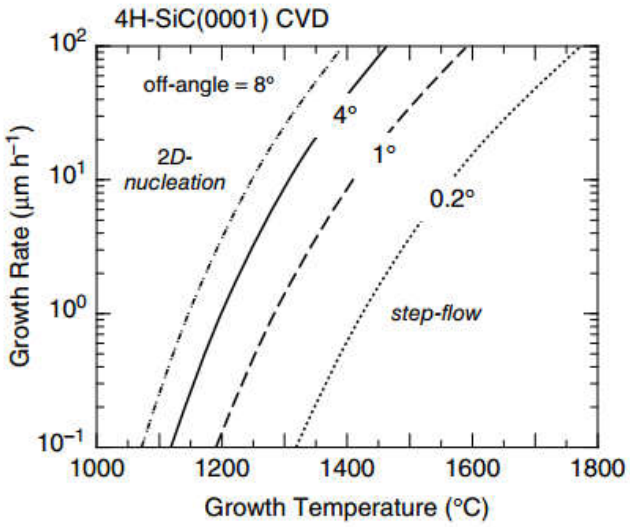


Figure 2-10 The influence of off-axis angles on HTCVD growth of 4H-SiC (0001) at different temperatures.

2.4 Device processing of SiC

SiC power devices are fabricated on an epitaxial layer with well controlled doping and thickness. Taking the SiC MOSFET as an example, there are several critical processing steps, such as ion implantation, thermal activation, etching, thermal oxidation, dielectric deposition, metallization, etc.

2.4.1 Ion implantation

In silicon based power devices, thermal diffusion is a popular way to introduce dopants or to drive the frontier of the doped region. For example, in a silicon power MOSFET, the channel could be defined by the difference between the diffused distance of the p-body region and the n+ source region. SiC features very strong chemical bonds, which makes the diffusion constant very small even if the temperature is above 1600 °C. A comparison of diffusion constants of several major dopants between Si and SiC are presented in Figure 2-11 [33, 34]. From this figure, it can be seen, to achieve the same diffusion constants, the temperature for SiC has to be doubled that of Si. For a deep doping, the temperature has to be above 2000 °C. But at such a high temperature, a high density of traps [34] and plane dislocations [35] are induced in SiC. What's more, applying an equipment which can bear a high temperature could add significantly to the processing cost.

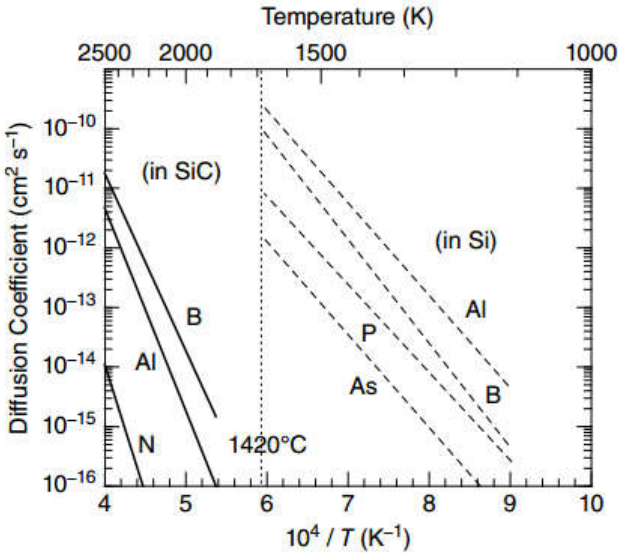


Figure 2-11 Diffusion constants for several major dopants in Si and SiC.

Ion implantation is a common approach to achieve area-selective doping in SiC. For thin and/or light doping, implantation at room temperature can reach this destination. The mask for the selective doping can be a photoresist or SiO_2. For deep and/or heavy doping, high temperature (300~800℃) implantation is desired. In heavy doping, the lattice damage caused by high temperature implantation is not as serious as room temperature implantation. At room temperature, a high density of stacking faults and 3C-SiC grains is contained in the implanted region after activation annealing [36-40]; while in high temperature implantation, the implanted region can easily recover to the initial polytype structure. Figure 2-12 shows the sheet resistance of n+ and p+ implantation in SiC under room temperature and 500 °C [41]. The sheet resistance is similar after implantation at the two temperatures at light doping. For heavier doping, the sheet resistance at room temperature is larger because of the severe lattice damage. It should be noted that a photoresist is not suitable as a mask for high temperature implantation.

Nitrogen is commonly adopted as an n-type dopant in SiC and aluminum as a p-type dopant when performing ion implantation. Boron is well known as a p-type dopant in silicon technology, but when implemented in SiC, the implanted boron atoms feature serous out-diffusion and in-diffusion at high temperature [42, 43]. The out-diffusion results in a loss of implanted boron atoms, while in-diffusion leads to a remarkably larger junction depth than the designed depth. Another two dopants, gallium and beryllium, have been studied as acceptors in SiC, but the resulting sheet resistance is very high because of their high ionization energy [44, 45].

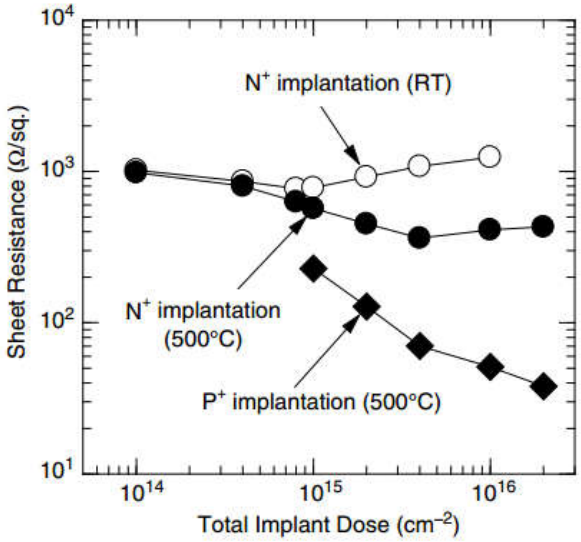


Figure 2-12 Sheet resistance vs. total implant dose for N+ and P+-implanted 4H-SiC under room temperature and 500 °C.

The implanted dopants usually occupy interstitial lattice sites where they cannot work as a donor or an acceptor [46]. After implantation, annealing at temperatures larger than 1600 °C should be done to activate the dopants as well as to attain lattice recovery. However, thermal annealing at such high temperature induces sublimation of the silicon atoms, surface atom migration, and so on, leading to roughness of the surface. A carbon cap was found to be effective to solve this problem. Figure 2-13 presents atomic force microscopy (AFM) images of SiC surfaces annealed at 1800 °C, with or without a carbon cap [43]. It is clear that the carbon cap maintains the smoothness of the SiC surface during high temperature annealing, while annealing with a bare SiC results in unacceptable roughness. After thermal annealing, the carbon cap can be removed easily with O_2 plasma.

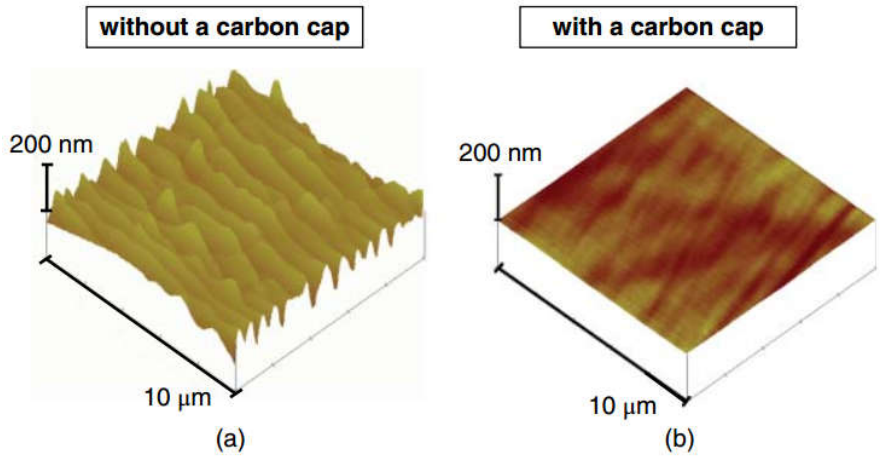


Figure 2-13 AFM images of SiC surfaces after annealing at 1800 °C (a) without a carbon cap, (b) with a carbon cap.

2.4.2 Oxidation

Compared to other wide bandgap semiconductors, SiC has a unique advantage that thermal oxidation can be conducted on SiC to form a SiO_2 layer, which is of great benefit in making a metal-oxide-semiconductor structure.

The oxidation process of SiC is similar to that of Si, but the oxidation temperature for SiC is much higher than that of Si. Under high temperature (about 1200 °C), oxygen gas is supplied and goes through SiC substrates. Oxygen reacts with the SiC surface to form SiO_2 while the byproduct CO/CO_2 is quickly carried away. To decrease contamination and grow a good quality of SiO_2, HCl can be introduced during oxidation to remove mobile ions. The oxidation process with oxygen as an oxidant is called dry oxidation. Apart from oxygen, water vapor (H_2O) has also been extensively studied as an oxidant for SiC. This is called wet oxidation. It has been reported that a higher MOS-channel electron mobility is achieved with wet oxidation due to much lower charge densities and interface state densities [47-49]. The oxidation rate of wet

oxidation is typically much faster than that of dry oxidation, but the oxide layer formed with wet oxidation is commonly considered to be inferior to that achieved by dry oxidation. In long wet oxidation, surface pits at the place of dislocations can be created due to enhanced oxidation near the dislocation cores [50, 51]. The pits can cause electric field crowding resulting in degraded oxide reliability. Therefore, dry oxidation is commonly adopted for reliability consideration. The electron mobility in the SiC MOS-channel is extremely low compared to the bulk mobility or the silicon MOS-channel mobility. The SiC MOS-structure formed by dry oxidation results in an electron mobility of less than 5 cm^2/V-s. The poor performance is considered due to a large interface state density located at approximately 2.9 eV above the valence band edge [52]. These states decrease the channel mobility through field termination, carrier trapping and Coulomb scattering. These states are attributed to the carbon clusters at the interface and the defects in near-interface sub-oxide which are produced in oxidation process [53].

The low channel mobility renders the SiC MOSFET unsuitable as a power device due to its extremely large channel resistance. A breakthrough in SiC technology was the discovery in the late 1990s that post-oxidation annealing (POA) in nitric oxide could significantly improve the channel mobility in SiC to ~ 20 cm^2/V-s [54, 55]. After that, tremendous efforts have been made in the hope of further improving the MOS-property in SiC. Wet re-oxidation annealing after gate oxidation has effectively improved the interface quality and mobility [48, 56]. The water vapor content as well as the re-oxidation temperature is significant in the process. Some other methods have also been identified to improve SiC channel mobility, such as annealing in phosphorus containing gas or in aluminum contaminated environment [57, 58], but these methods inevitably lead to instability in the threshold voltage of the MOSFET and therefore are

not adopted for practical use. After the publication of the nitric annealing approach, no significant progress has been made in terms of SiC MOS-interface in around the following twenty years.

2.4.3 Etching

SiC can be etched in a molten base solution at about 450~600 °C [59], but this process introduces interface states on SiC surface and dislocations. Besides, contamination of Na^+, K^+ and so on, should be also considered.

Plasma based dry etching is a convenient way to etch SiC. Compared to silicon, the dry etch of SiC does not require special etching gases or high temperatures. Fluorine-based gases such as SF_6, CF_4, and BF_3 are popular in etching SiC. Carbon atoms need to be removed during a dry etch by O_2 or Ar gases. The byproducts, SiF_4 and CO/CO_2, are gases that would be easily carried away from the SiC wafer.

For dry etching of SiC, photoresist can be adopted as the etching mask. However, the photoresist is consumed at a high rate during SiC etching, therefore, a hard mask is typically used when a relatively deep trench is required. SiO_2 is the most popular etching mask for SiC, and the selective etching between SiC and SiO_2 can be adjusted to favor the SiC etch. Metal layers boast a very high etching selectivity versus SiC, and are popular in laboratory use. In industry, the concern of metal contamination hinders the adoption of metal as an etching mask.

2.4.4 Metal contact

Metallization is an essential step to make a functional semiconductor device. In a semiconductor device, Ohmic contacts are required for the electrical connection to

the intrinsic device from the outside world. Another important contact is the Schottky contact, which forms a junction between the metal and the semiconductor, leading to a rectifying property.

In SiC technology, the typical Ohmic contact to an n-type region is nickel (Ni), and the annealing temperature is about 700~800 °C. Al/Ti is a standard Ohmic contact for p-type SiC [60-64] , and is annealed with a temperature of about 900~1000 °C. After this step, sintering is performed by a rapid thermal process (RTP) of 2 minutes at 1000 °C [65].

Both Ni and Ti have been adopted on lightly doped 6H-SiC [66] and 4H-SiC [67, 68] to form Schottky contacts on n-type SiC. Schottky metal deposition can be achieved by sputtering at room temperature. After metal deposition, a low temperature of 200~500 °C annealing in inert gas ambient is beneficial for decreasing the leakage current of devices.

In some types of devices, the junction barrier Schottky diode (JBS), for example, is desired to have a Schottky contact to both the n-type and p-type SiC. Bilayer metallization of Ti/Ag and Ni/Al has been reported for fabrication of a JBS [69, 70].

2.5 SiC based power devices

As shown in Figure 1-1, both power diodes and power switching devices are required for power converters. The energy loss of a power converter mainly occurs in power devices. To reduce the energy loss of a power converter, the power devices should be as close as possible to the ideal power device. In the on-state, the voltage drop on the power devices should be as low as possible, while in the off-state, the leakage current through the power devices should be as small as possible. The breakdown voltage should be as high as possible. The devices should be switched

between off-state and on-state as fast as possible. SiC power devices present characteristics closer to ideal power devices compared to their Si counterparts owing to the high critical breakdown field in SiC.

2.5.1 PiN diode

PiN junction diode is one of the most common diodes in semiconductor technology. For power applications, a lightly doped n-type with a certain thickness is sandwiched between a p+ layer and an n+ layer to block the reverse voltage. The schematic cross-sectional structure of a typical PiN diode is shown in Figure 2-14.

A depletion region is formed inside the PiN diode due to the difference in work functions of the n-type SiC and p-type SiC, which bends the energy bands in semiconductor, creating a barrier for electrons from the n-side to p-side and a barrier for holes from the p-side to n-side. When the PiN diode is under a forward bias V_F between the p-side and the n-side, the energy barrier is reduced by $q \cdot V_F$, which facilitates electrons moving from the n-side to the p-side and holes moving from p-side to n-side. If the V_F is large enough, a high current could flow through the PiN diode. At this condition, the PiN diode is in a forward conduction state. When the PiN is under a reverse bias V_R, the energy barrier in the semiconductor side is increased by $q \cdot V_R$, so the number of electrons moving from n-side to p-side and that of holes from p-side to n-side quickly drop to a negligible level. But it should be noted, there is a tiny number of electrons in the p-side and a tiny number of holes in the n-side. These carriers are termed minority carriers. With a reverse bias V_R across the PiN diode, the minority carriers move to the opposite sides, resulting in a tiny leakage current. This is the reverse blocking state of the PiN diode.

In the forward conduction state, the holes injected from the p-side into the lightly doped drift layer and the electrons from the n-side into the lightly doped drift layer may exceed the background doping level in the drift layer. Therefore, the conductivity in the drift layer is enhanced. This effect is called conductivity modulation. Thanks to this effect, the PiN diode could be designed to block a very high reverse voltage with a thick and very lightly doped drift layer, while maintain superior conduction by conductivity modulation.

With the high critical breakdown field in SiC, SiC PiN diodes could achieve 10-kV level voltage ratings [71]. However, the development of SiC PiN diodes is hindered by several factors. Firstly, the turn-on voltage of a SiC PiN diode is ~2.8 V, which is much larger than that of a Si PiN diode (~0.7 V). This makes the SiC PiN only justified in very high voltage applications. Secondly, the minority carrier lifetime in SiC is typically very low (< 1 μs), which makes the conductivity modulation effect less pronounced since the injected carriers quickly vanish. The low lifetime for minority carriers is found to be related to defects originating from the carbon deficiency inside the SiC. Some approaches are proposed to improve the minority carrier lifetime in SiC, such as carbon atom implantation and long-time thermal oxidation [72-76]. Thirdly, SiC PiN diodes suffer from bipolar degradation [77-79]. As shown in Figure 2-15, the forward voltage drop gradually increases with continuous forward conduction [80]. This phenomenon comes from the formation of stacking faults. These faults act as a recombination center, reducing the carrier lifetime in SiC material [81]. The bipolar degradation is addressed in the material level. With optimization in material growth, the bipolar degradation can be suppressed in state-of-the-art PiN diodes.

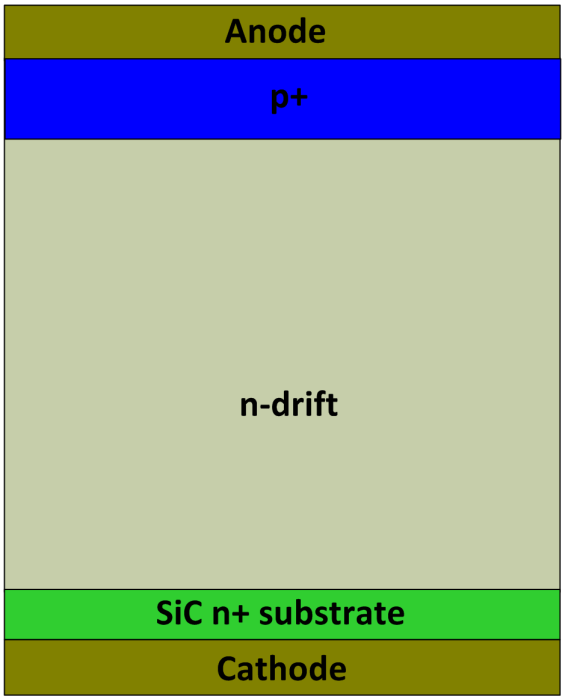


Figure 2-14 Schematic cross-sectional structure of a typical PiN diode.

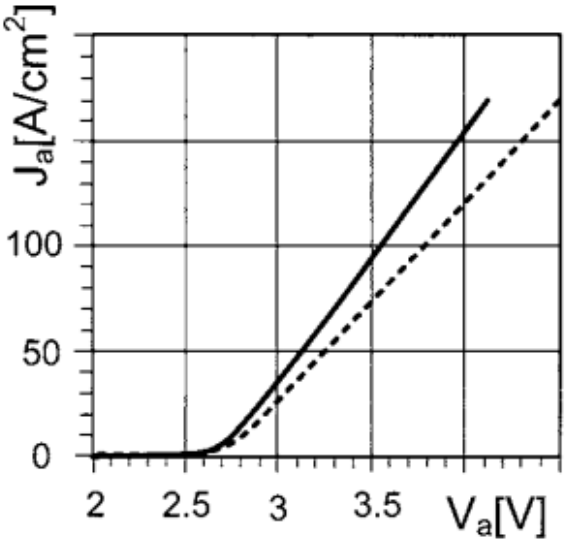


Figure 2-15 Forward *I-V* characteristic before (solid) and after (dashed) continuous converter operation [80].

2.5.2 SBD diode

The SiC Schottky barrier diode (SBD) is a unipolar device, which eliminates the minority carrier storage effect. Therefore, the SBD is suitable for high frequency operation. Figure 2-16 shows a schematic cross-sectional structure of a SiC SBD. The anode metal forms a Schottky junction to the underlying n-region. The energy band diagram of an n-type Schottky junction is shown in Figure 2-17 [33]. An energy barrier for electrons from metal to semiconductor is created by the difference between the work function in the metal and electron affinity in the semiconductor. A depletion region is formed inside the semiconductor, which bends the energy bands in the semiconductor, creating a barrier for electrons from semiconductor to metal. With zero bias on the SBD, a tiny portion of electrons thermally overcoming the barrier from metal to semiconductor results in a low leakage current, while those electrons from the semiconductor to the metal counteract result in another leakage current with opposite sign. The two leakage currents counteract each other, leading to zero current. When the SBD is under a forward bias V_F between the metal and n-type semiconductor, the energy barrier in the semiconductor side is reduced by $q \cdot V_F$, which facilitates electrons moving from the semiconductor to the metal. If V_F is large enough, a high current could flow through the SBD. At this condition, the SBD is in the forward conduction state. When the SBD is under a reverse bias V_R, the energy barrier in the semiconductor side is increased by $q \cdot V_R$, so the number of electrons moving from semiconductor to metal quickly drops to a negligible level. At this reverse biased condition, only a small leakage current exists due to the electrons moving from the metal to the semiconductor. This is the reverse blocking state of the SBD.

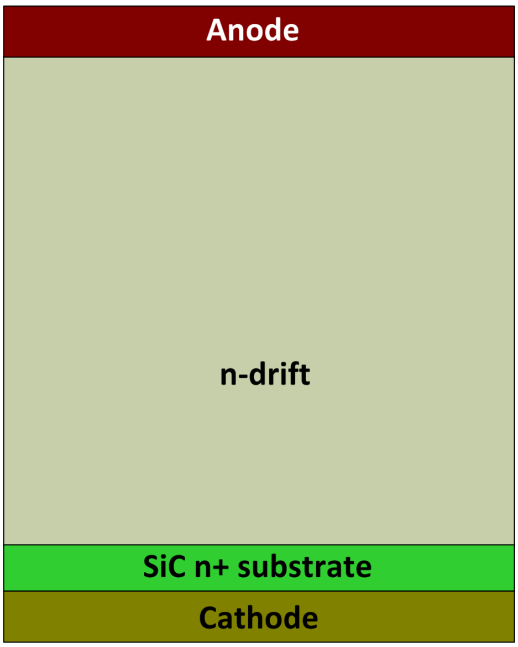


Figure 2-16 Schematic cross-sectional structure of a typical SBD.

To achieve the same forward current density, the forward voltage V_F in the SiC SBD is smaller than its silicon counterpart since the doping level in the SiC could be raised to lower the parasitic resistance. Therefore, the SiC SBD could easily achieve the kV-level, while the Si based SBD typically operates at much lower voltage levels (<100 V).

As the electric field inside a SiC SBD is much higher than its Si counterpart due to the high critical breakdown field in SiC, the barrier lowering effect in the SiC Schottky junction is more severe for SBD. For this reason, the SiC SBD suffers from a high leakage current, especially at elevated temperatures.

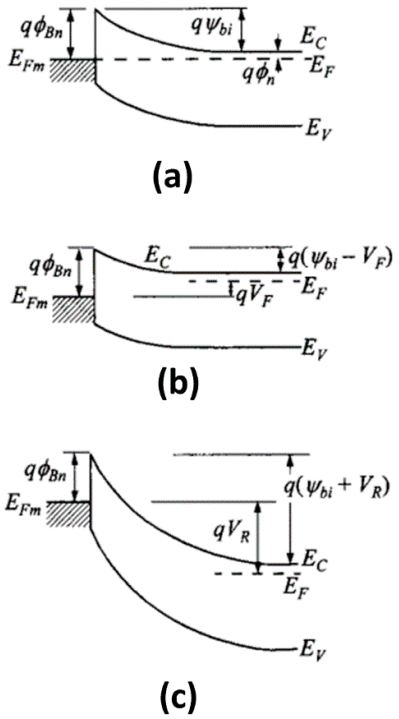


Figure 2-17 Energy band diagrams of metal on n-type under (a) zero bias, (b) forward bias, and (c) reverse bias.

2.5.3 Junction barrier Schottky diode (JBS)

The SiC PiN features a lower leakage current and a better thermal stability compared to SiC SBD, while the SiC SBD boasts a much better switching performance and a lower turn-on voltage. The SiC junction barrier Schottky diode features periodically varied PN junctions and Schottky junctions, as shown in Figure 2-18. In the forward conduction state, the Schottky junction is turned on, contributing to the forward current. As the conduction is unipolar in nature, the switching performance of the JBS is superior. In the reverse bias state, the depletion region around the PN junction screens the high electric field away from the Schottky junction, leading to a lower leakage current and improved high temperature performance.

The critical point in the design of a SiC JBS is the trade-off between the Schottky junction field and the forward voltage drop. With a small space between the adjacent p-grids, a lower Schottky junction field is achievable which reduces the leakage current under reverse bias. However, the smaller space between the p-grids increases the resistance and reduces the effective Schottky contact area, leading to an increased forward conduction voltage V_F.

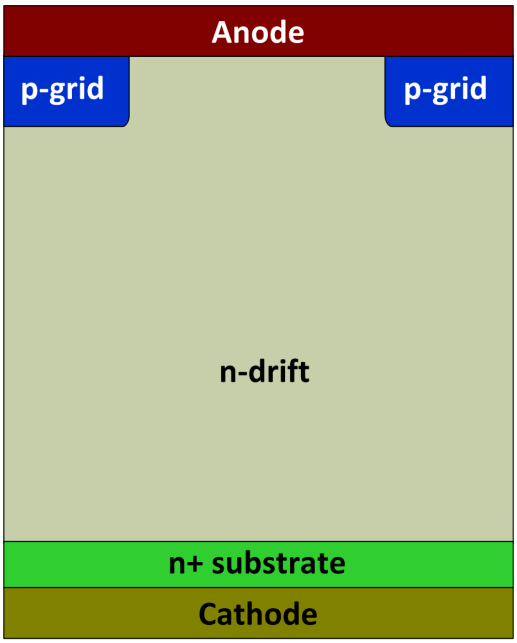


Figure 2-18 Schematic cross-sectional structure of a typical JBS.

The junction barrier Schottky diode (JBS) takes advantage of both diodes. A schematic cross-sectional structure of JBS is shown in Figure 2-18. It includes the parallel interdigitated PiN and Schottky diodes. Under a forward bias which is smaller than the turn-on voltage of pn junction in the JBS but larger than the turn-on voltage of Schottky junction in the JBS, the JBS works with the Schottky style. When under a reverse bias, the JBS bears the V_R by the pn junction. The SiC JBS holds the same

advantage over Si JBS as that of the SiC Schottky diode and SiC PiN diode in high voltage applications.

2.5.4 Bipolar junction transistor (BJT)

The SiC bipolar junction transistor (BJT), as shown in Figure 2-19, has the same structure with the Si BJT. In the early stage of SiC power devices, BJT was expected to be the final solution to utilize the superior material properties of SiC, since the SiC BJT avoids the notorious SiC MOS-interface issues. With base current to turn-on the base-emitter junction, electrons emitted from the emitter reach the collector. The BJT is turned off by applying a zero or negative base current. However, the SiC BJT faces similar issues to the silicon power BJTs. To drive the SiC BJT, a continuous base current is required. A high current amplification ratio ($\beta = I_C/I_B$) in the SiC BJT is difficult to achieve, which means a large driving circuit is required for SiC BJT, and a high driving loss is expected [82, 83]. Special attention should be given to the base-emitter junction inside the SiC BJT. Since it is a PN junction in nature, it may also suffer from the bipolar degradation. Therefore, the long-term application and stability of the SiC BJT is an important issue.

With the progresses made in SiC MOS-interface engineering, the SiC MOSFET gradually drew the attention of researchers. Therefore, research activities in the SiC BJT has been reduced in recent years.

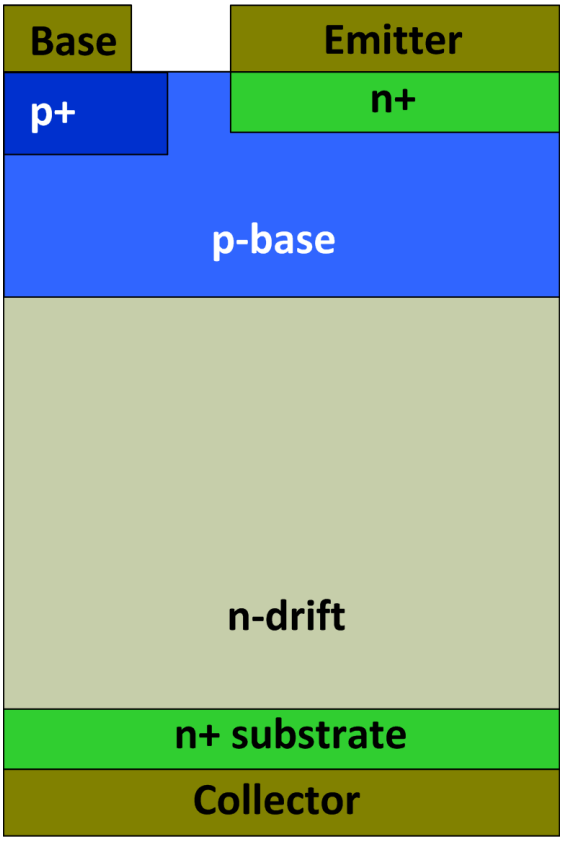


Figure 2-19 Schematic cross-sectional structure of a typical structure of SiC BJT.

2.5.5 Junction field effect transistor (JFET)

The SiC junction field effect transistor (JFET) is a strong competitor with the SiC MOSFET in the early stage of SiC technology. The SiC JFET avoids the notorious MOS-interface problem, and is a voltage-controlled device. The SiC JFET is simply controlled by the gate voltage to modulate the depletion region width of the PN junction gate. With a negative gate voltage to pinch off the region between the gates, the SiC JFET is turned off. A schematic cross-sectional structure of an n-type JFET is shown in Figure 2-20. The JFET is fabricated on a thick lightly-doped n-type drift region located between the p-gate and the n+ substrate. The n-drift region is designed to withstand the blocking voltage. The two p-gates and the channel between them form

two pn junctions. The width of the depletion region of the pn junctions decreases linearly according to the square root of the gate to the channel voltage. Hence a negative voltage from the gate to the channel is required to turn off the SiC JFET.

Carriers can tunnel through a short depletion region, so current can flow between the drain and source, even if a negative voltage from the gate to a short channel is applied. Therefore, this prototype SiC JFET needs a long channel in order to be turned off, however it is not easy to make very deep p-regions. The difficulty has been illustrated in the above "Ion implantation" section. Besides, the capacitance between gate and drain (C_{GD}) is large.

Therefore, an improved JFET structure, as shown in Figure 2-21, was proposed with a lateral channel [84-86]. It's easier to obtain a long channel in a lateral channel than in a vertical channel, because a deep ion implantation can be avoided. The problem is that a large C_{GD} still exists.

Simens Co. proposed another improved JFET structure, as shown in Figure 2-22 [87]. With only the upper p-region connected to the gate electrode to control the channels and the other two p-regions connected to source electrode, C_{GD} can be effectively shortened. To solve the obstacle of the fabrication of the deep p-region, a second epitaxial on SiC was invented in this structure.

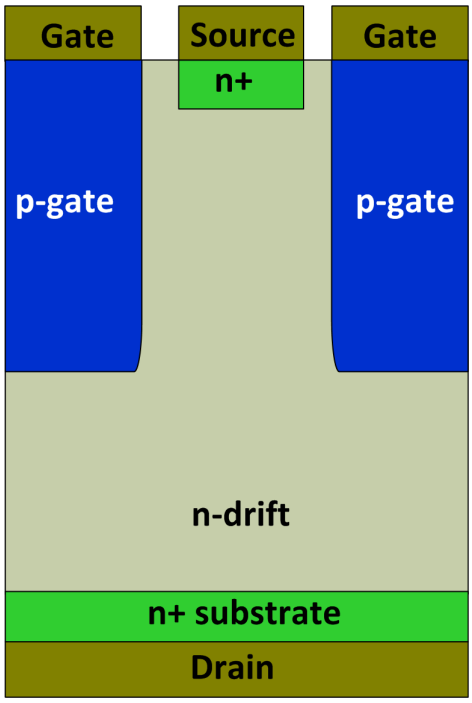


Figure 2-20 Schematic cross-sectional structure of a typical JFET.

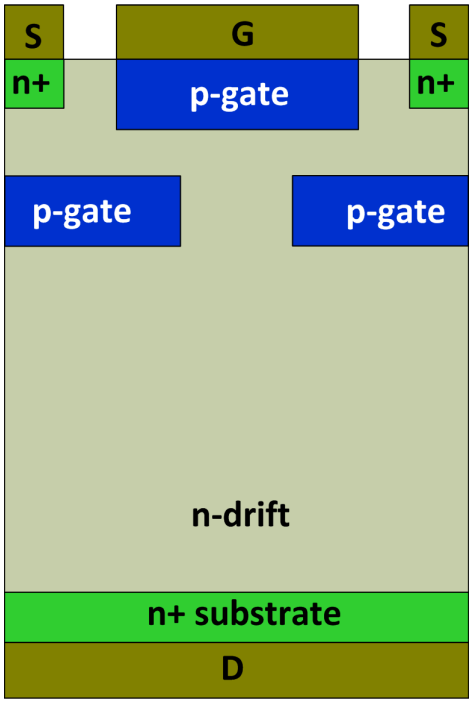


Figure 2-21 Schematic cross-sectional structure of an improved JFET structure.

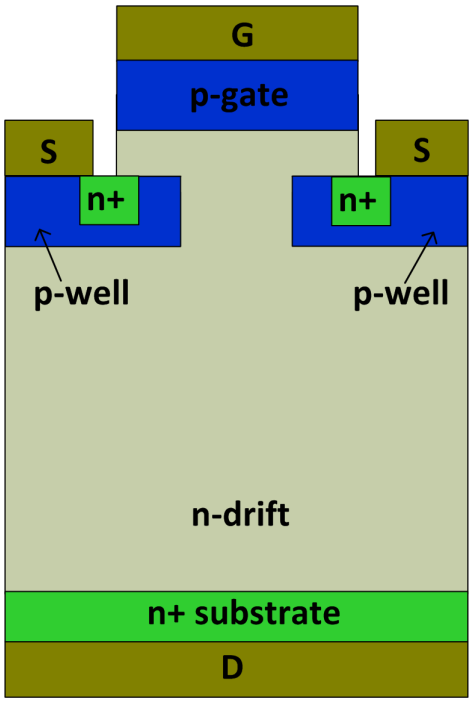


Figure 2-22 Schematic cross-sectional structure of another novel JFET structure.

The above three SiC based JFET structures are usually designed and applied as normally-on power switches. However, the control of a normally-on device is much more complex than the control of a normally-off device. Therefore, a vertical channel is designed as normally-off power switches with p-regions very close to each other, as shown in Figure 2-23 [88-93]. The p regions connected to the gate electrode in this device are fabricated on the surface, so they can be more easily connected to the gate electrode than the buried p-gates. Besides, in the buried p-gates, the gate voltage far from gate electrode is lower which goes against the unity of currents. Another advantage of this device is a high channel density allowed with vertical channels. The channel area in the vertical direction is only the channel width for this kind of JFET, while for the JFET with lateral channels, the area in the vertical direction is channel length which is several micro-meters long. The application of this device involves the

intrinsic limitation of the large R_{ON} of JFET that still exists. Besides, C_{GD} is still too large.

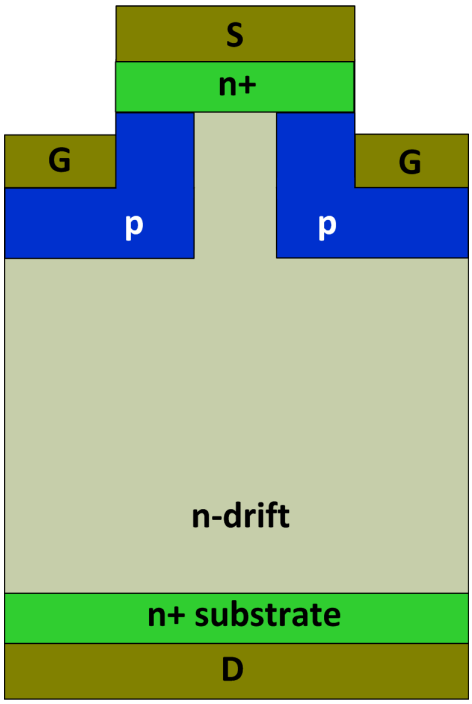


Figure 2-23 JFET with trench p-regions.

Given the above limitation in the SiC JFET, a cascode configuration, as shown in Figure 2-24, includes a normally-off Si MOSFET with a low BV and a normally-on SiC JFET with a high BV, which seems a promising solution [94]. In this scheme, because the SiC JFET is normally-on, the working state is decided by the Si MOSFET so that a much smaller R_{ON} can be arrived at. At the same time, BV is borne by the SiC JFET. But this cascode still suffers from parasitic effect, high cost, and so on.

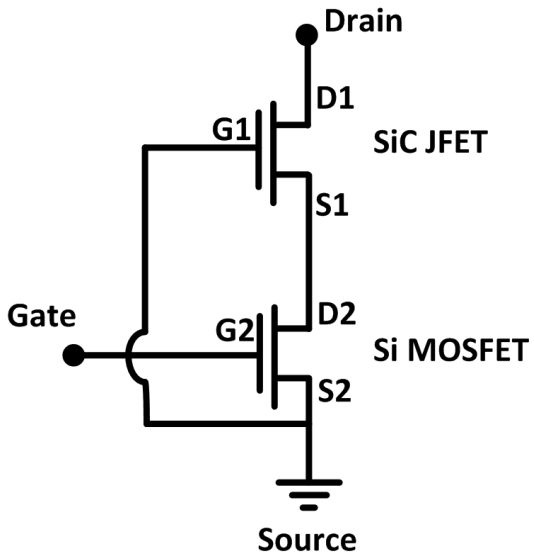


Figure 2-24 A cascode configuration of SiC JFET and Si MOSFET for power applications.

2.5.6 Metal-oxide-semiconductor field effect transistor

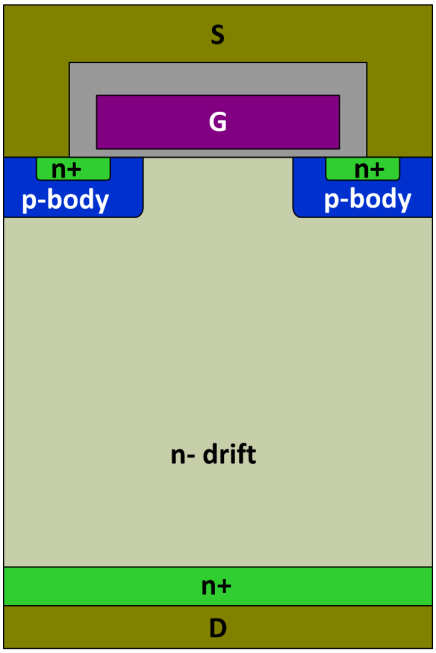
MOSFET is the most popular power transistor because of its fast switching speed as well as its high input impedance. In lower voltage applications, the Si MOSFET is preferred to the SiC MOSFET. While in higher voltage applications, the SiC MOSFET tends to replace the Si MOSFET.

MOSFET can be mainly classified into two types: the double-diffused planar MOSFET (D-MOS) and the conventional trench MOSFET (C-MOS), which are shown in Figure 2-25. In D-MOS, the neighboring p-bodies and n-drift region constitute a JFET structure. The depletion region in this JFET structure hinders the current flowing capability when the cell pitch of D-MOS is not large enough and is in the ON-state, which increases the ON-resistance (R_{ON}) of the device [95, 96]. Besides, the channel of D-MOS is fabricated horizontally, and this channel has to be large

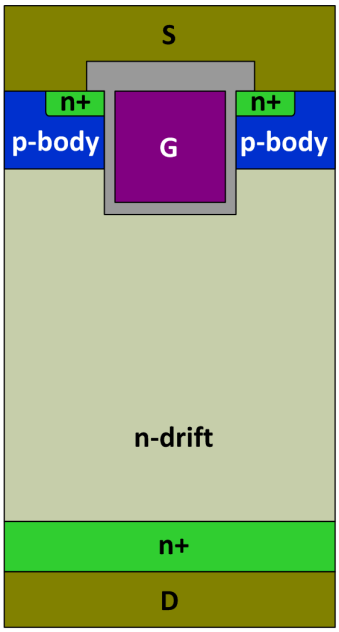
enough to ensure an acceptable leakage current when the device is at the OFF-state. Hence, the D-MOS is not a good choice if a small area is preferred in applications. But C-MOS with a trench gate structure helps to decrease R_{ON}, because it doesn't contain a JFET region. A small cell pitch can be obtained because the C-MOS channel is fabricated vertically. With a smaller cell pitch, the density of channels in C-MOS is higher, which contributes to decrease R_{ON}. A C-MOS with a small cell pitch is remarkably favorable for the requirement of portability, flexibility, and convenience of electric devices nowadays.

However, C-MOS faces a critical issue for its commercial success: the high OFF-state oxide field at the trench bottom/corner. This high oxide field is a byproduct when SiC utilizes its significantly higher critical breakdown field. This high peak electric field in the gate oxide could accelerate the gate oxide failure, resulting in degraded device reliability [97].

A p-shield under the trench gate is proposed as an oxide protection, as shown in Figure 2-26. However, the p-shield is required to be well grounded to the source contact, otherwise the safe operation area of the device is compromised and the switching performance of the device is degraded. Therefore, a large portion of the chip area is sacrificed for contact vias. The double trench structure [98-100] reduces the oxide field with an additional source trench, which, however, adds to the difficulty in minimizing the device cell size (thus is difficult to exert the full potential of the trench MOSFET in terms of increasing high channel density).



(a) D-MOS



(b) C-MOS

Figure 2-25 Schematic cross-sectional structures of (a) D-MOS and (b) C-MOS.

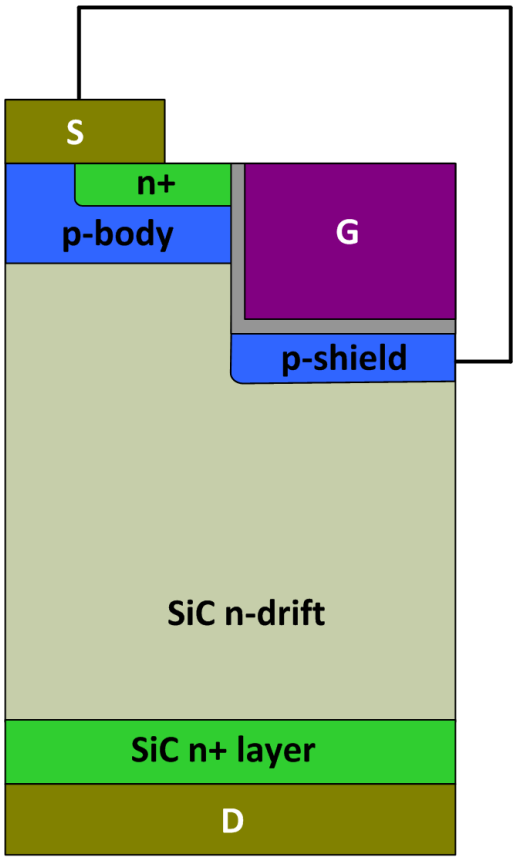


Figure 2-26 Trench SiC MOS with grounded p-shied (GS-MOS).

Chapter 3 Research Methodology

3.1 Introduction

The research begins with the issues met in the study of current SiC power devices. Creative ideas are needed to design novel power structures. At the same time, some potential issues in the current structures are needed to be analyzed for future study.

The proposed device structures and the operation mechanisms of the devices are studied by numerical simulations. The simulations help to reveal the internal device physics during the device operation, and give hints to further optimize the device structure and geometry.

Figure 3-1 shows a flowchart of a simulation work in a project. Device structure is firstly created in the SDE tool by defining different regions with specific material, doping, size, etc. Then meshing is set up to create points for calculation of electric field, electric potential, mobility, etc. in the structure. The final step in the SDE tool is exporting the structure with meshing to a TDR file format for the following SDevice tool.

The SDevice tool is favorable to simulate electrical, thermal and optical characteristics of semiconductor devices. The structure generated by the SDE tool is imported and then analyzed under specific physical models as well as math iteration. For numerical simulations, boundary conditions are required. In device simulation, the boundaries conditions are defined by setting the voltage and/or current at each electrode of the device. After SDevice simulation, all the characteristics achieved will be saved in a TDR or PLT file format for plotting.

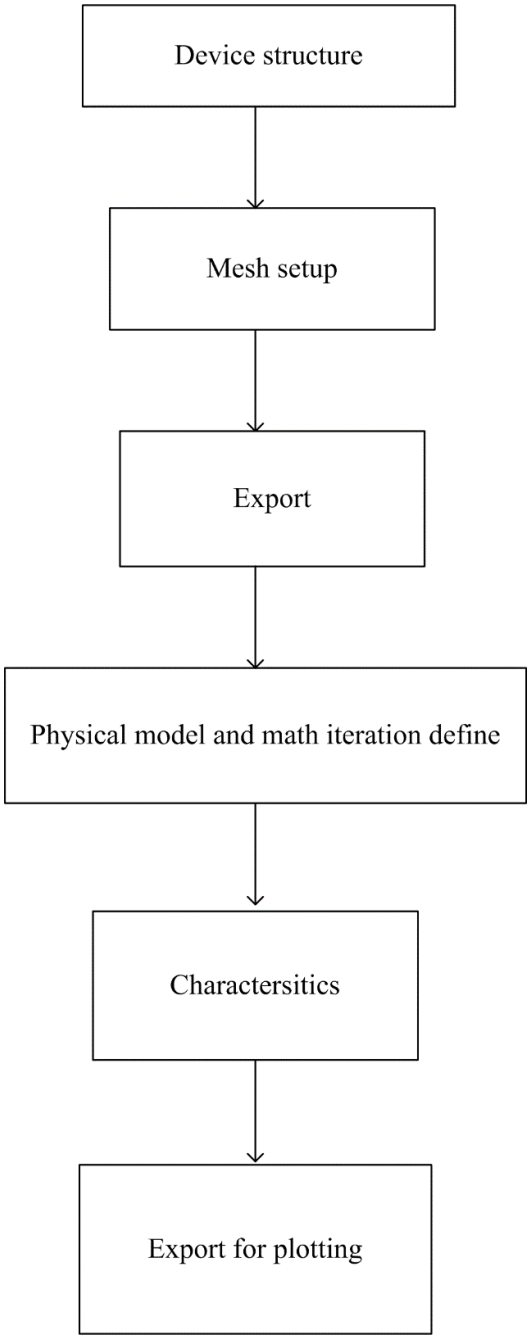


Figure 3-1 Simplified simulation flowchart in a complete project.

3.2 Mesh setup and initialization

In the meshing of the structures, a denser mesh at some important regions or interfaces is a method in order to increase accuracy and efficiency. Figure 3-2 displays

the meshing of a SiC MOSFET (the PB-MOS, the details of which will be presented in chapter 5). At the top side of the PBMOS, more mesh lines are designed than the lower drift region, because there is material variation between oxide and SiC, gradient of doping density, more pn junctions, and contacts. A default setting in SDE tool is adding mesh lines at the place of junctions. Much more mesh lines at the interface of oxide and SiC is also deliberately designed, because the material parameters and electrical parameters (such as doping concentration, electric field strength, etc.) vary significantly and a denser mesh lines can reflect the variation accurately. However, a coarse grid is sufficient for constant doping at the lower drift region, as shown in Figure 3-2.

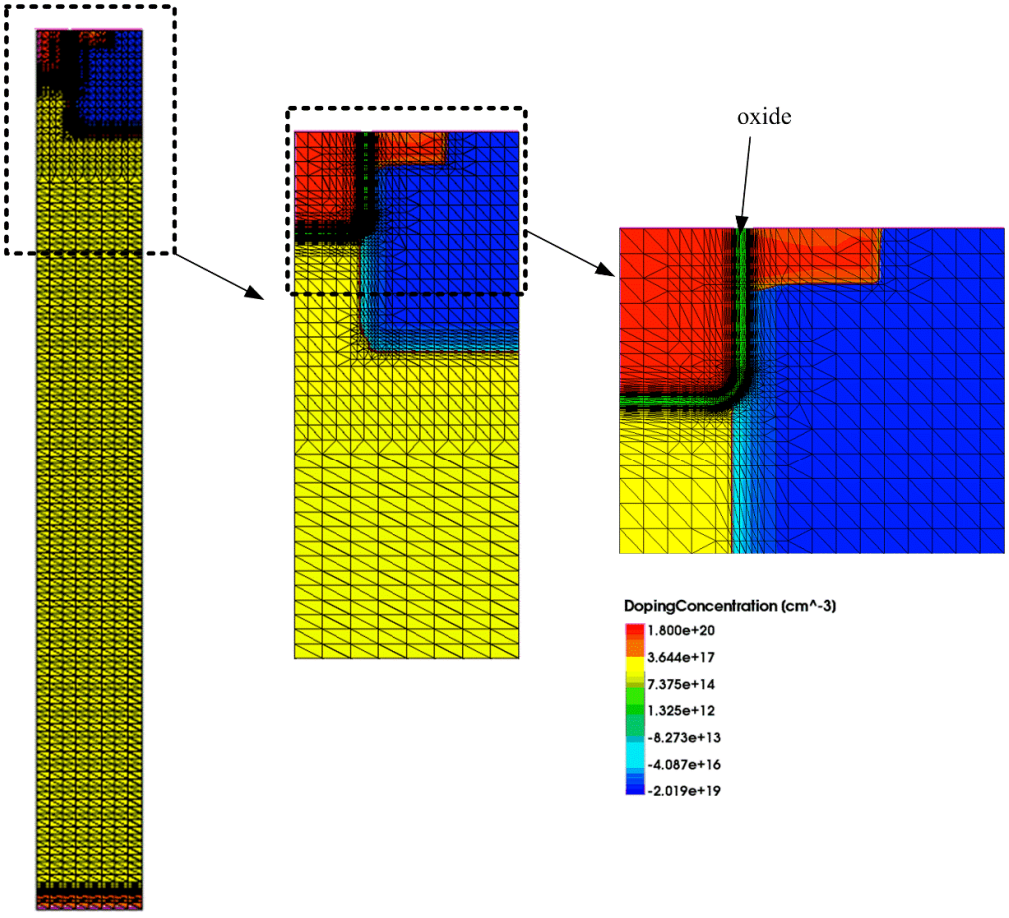


Figure 3-2 Mesh design in a SiC MOSFET.

3.3 Plotting tools

Tecplot and Inspect are two plotting tools integrated in the simulation software workbench. TDR files from SDE tool can be loaded into Tecplot for viewing the contours. Figure 3-3 shows the main Tecplot window. By selecting parameters in the Sidebar, different characteristics (such as ElectricField, Lattice Temperature and eDensity) of devices can be displayed. Menu bar is helpful to process the figures in the frame.

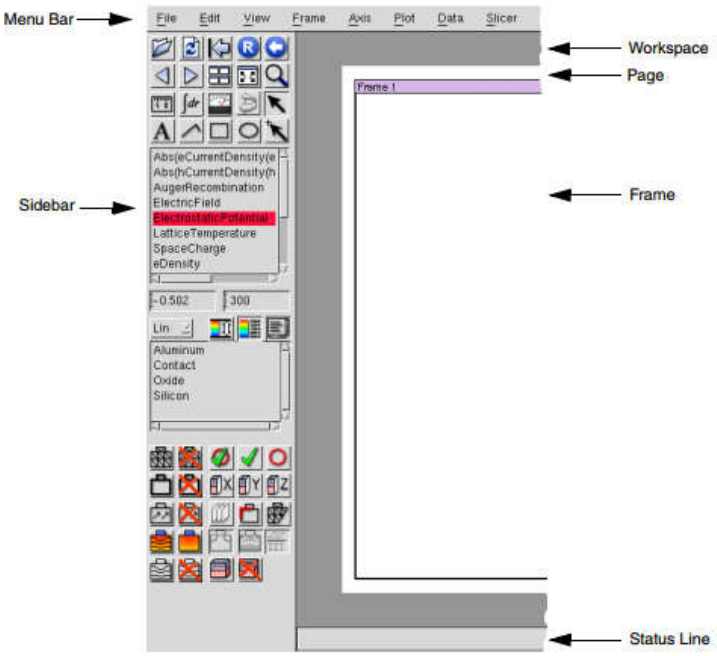


Figure 3-3 The main window of Tecplot.

Inspect can be exploited to show and analyze curves. An Inspect curve is a group of points (defined by x-axis and y-axis) as well as lines between neighboring points. Inspect curve can be exported to CSV format for plotting in Windows system. The main window of Inspect is shown in Figure 3-4. From the datasets group box in the left side, the variables of x-axis and y-axis can be selected.

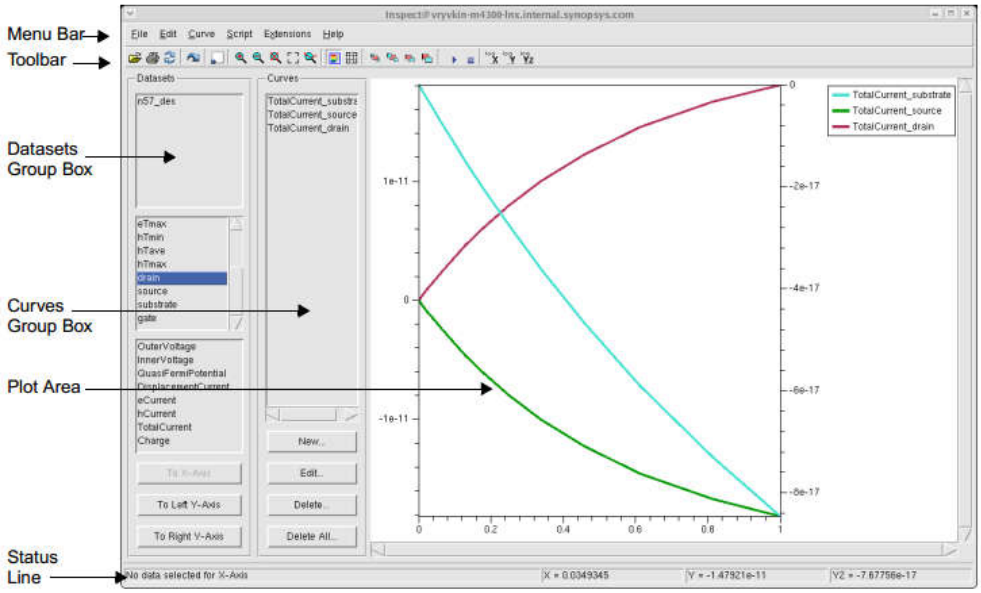


Figure 3-4 The main window of Inspect.

3.4 Static characteristics

After device structures are built, the following crucial characteristics of power MOSFET are mainly employed in order to evaluate the performances of the devices in this thesis.

3.4.1 Transfer characteristics

Transfer characteristics is one of the fundamental performances of MOSFET. Figure 3-5 exhibits the transfer characteristics of a typical N-channel MOSFET. The drain current I_d is influenced by gate to source voltage V_{GS} when drain to source voltage V_{DS} is kept constant. The threshold voltage V_T is defined as the minimum V_{GS} which can form a conducting channel between the source and the drain. V_T should neither be too large nor too small, because MOSFET with a small V_T is easily to be turned on by noise while a large V_T causes more energy loss in the gate driver. V_T can

be negative or positive physically. But a positive one is required in power applications since there is no energy loss at 0-V V_{GS}.

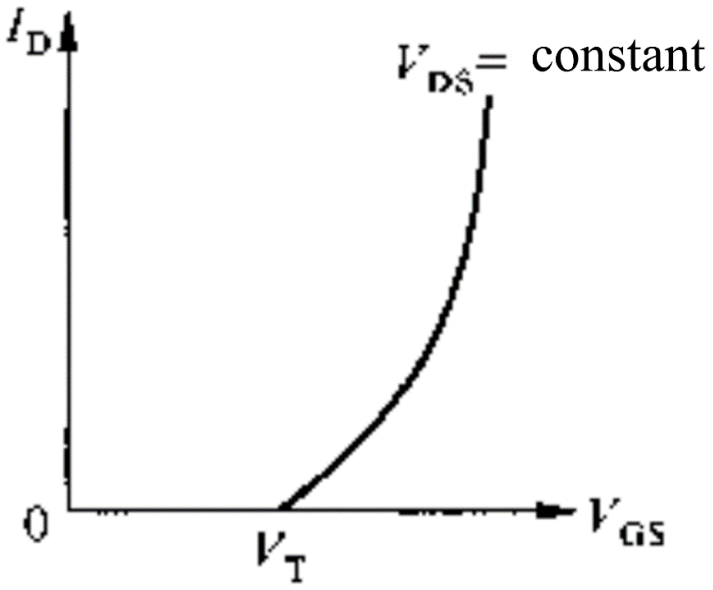


Figure 3-5 Transfer characteristics of an N-channel MOSFET.

3.4.2 Output characteristics

If the gate voltage V_{GS} is kept constant, the relation between the drain current I_D and drain to source voltage V_{DS} is the output characteristics, as shown in Figure 3-6. When V_{DS} is still small, I_D increases with V_{DS}. Eventually, I_D will saturate due to the pinch-off of the channel at the drain side or due to the velocity saturation. For a power transistor, the on-resistance in the linear region is the key focus of study since it determines the conduction loss. The saturation current in the output characteristics should also be considered. In a power transistor, too large a saturation current is unfavorable for short-circuit capability.

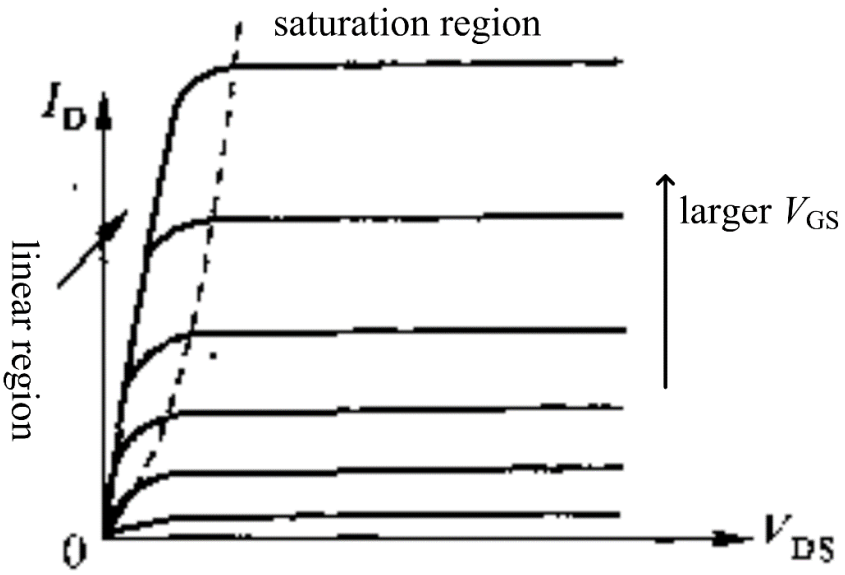


Figure 3-6 Output characteristics of a typical N-channel MOSFET

3.4.3 Breakdown voltage (*BV*)

When a gate voltage lower than the threshold voltage V_T is applied, the V_{DS} can be increased to a value with a limited leakage current in the MOSFET. The drain current I_d increases to a certain criterion at a certain V_{DS} which is the breakdown voltage (*BV*), shown in Figure 3-7. For a power transistor, the breakdown typically occurs when avalanche breakdown is reached, which marks a sudden increase of drain current. It is important for power devices since only MOSFETs with a higher *BV* than required can only be chosen for the power electronics.

In most devices, the breakdown voltage is beard by a light doped region since electric field in a lightly doped region decreases much slowly than a heavily doped region. Devices with a high breakdown voltage features a long light doped region whose resistivity is high. Hence, power semiconductor devices with a higher *BV* encounter a problem of larger resistance.

Therefore, power devices with a high *BV* and a small resistance are preferred.

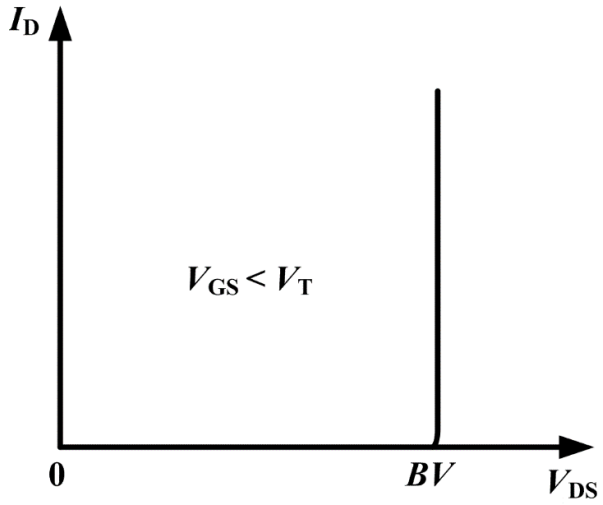


Figure 3-7 *BV* characteristics of power devices

3.4.4 OFF-state electric field in gate oxide

As said in chapter 2, the critical electric field in SiC is much higher than that in Si. This means the corresponding gate oxide field in SiC MOSFET may be much higher than that in Si MOSFET. Besides, the poorer interface properties of SiC/SiO_2 than that of Si/SiO_2 also easily leads large electric field enhancement. A higher gate oxide field leads to a shorter lifetime of the device which is a barrier for the commercialization of SiC MOSFET. Therefore, OFF-state gate oxide field is a vital factor to evaluate the reliability of SiC MOSFET.

3.4.5 ON-state resistance R_{ON}

When a MOSFET is switched on, the device behaves as a resistor in the linear region. The on-resistance of the device is simply determined by V_D/I_D in the linear region.

Figure 3-8 shows the components concluded in a R_{ON} of a trench MOSFET. R_S represents heavily doped n+ region; R_{CH} represents the channel resistance; R_{ACC} represents the resistance of the accumulation region; R_{epi} represents the resistance of the epitaxial n- drift layer; R_{subs} represents the resistance of the substrate.

In SiC trench MOSFET, the R_{CH} occupies a lot due to carrier mobility at the interface of oxide and SiC is much lower than that of Si and oxide.

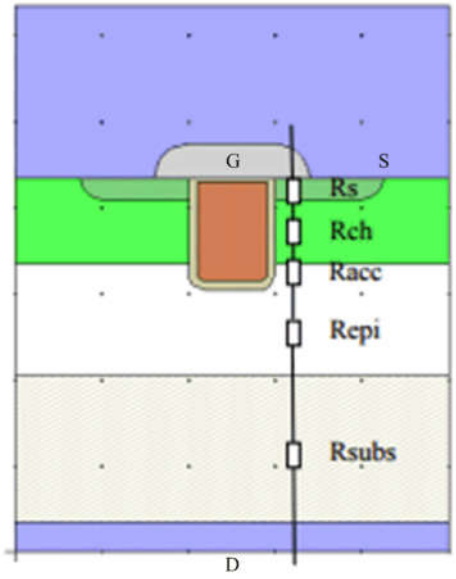


Figure 3-8 Detailed components in R_{ON} of a trench MOSFET.

3.5 Dynamic characteristics

3.5.1 Switching energy loss

In an ideal MOSFET switch, the drain voltage is zero at on-state, while the drain current is zero at off-state. Thus, the power loss P, as a product of the voltage and current, is always zero. However, in real power electronics, there is an overlap between non-zero voltage and current, as shown in Figure 3-9.

When designing power MOSFET, this energy loss is a criterion for judgment and must be considered. For SiC MOSFET, since the power supply voltage is much higher than Si MOSFET, the switching energy loss is deteriorated. A faster switching speed is helpful to decrease the loss.

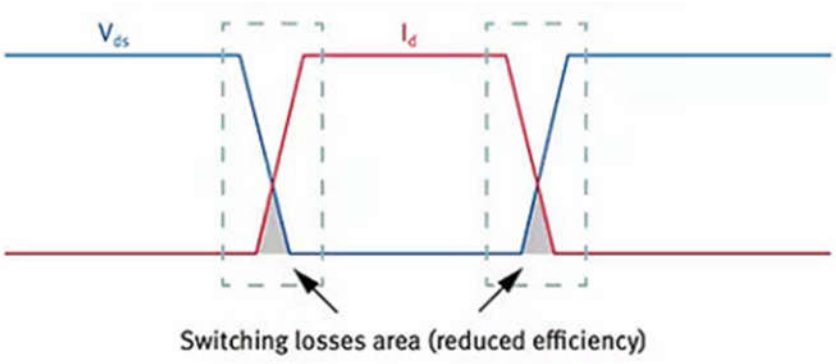


Figure 3-9 Drain current and drain-to-source voltage waveforms of the switching of a MOSFET.

But too fast a switching speed may lead to a large current or voltage overshoot. These overshoots may result in the failure of devices, for example, the device is turned on again after a large voltage overshoot after the device is turned off. Hence, there

should be a trade-off of switching loss and overshoot, and this trade-off is a significant evaluation of power devices.

The switching speed can be controlled by the switching circuit design, especially the value of gate resistance R_G in the circuit. A larger R_G brings a smaller current in the gate drive circuit, hence the charging and discharging speed of gate is decreased.

3.5.2 Reverse transfer capacitance C_{rss}

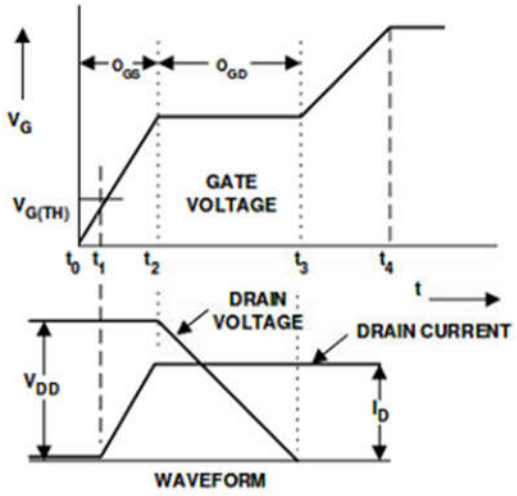


Figure 3-10 Waveforms of V_G, I_D, and V_{DD} at turn-on process of MOSFET

C_{rss} is the capacitance between gate and drain, and also is one of the main factor affecting the increasing or decreasing time of V_{DS}. From Figure 3-10, it can be seen the decreasing time of drain voltage is t_2~t_3. A majority of the switching loss is generated during this period. The V_G at this time is stagnated which means the gate current is used to discharging V_{GD}. The time depends on C_{GD} (C_{rss}). Therefore, a good design of MOSFET should have a smaller C_{rss}, or other aspects of the MOSFET have to be much better.

C_{rss} is also an important factor influencing the false turn-on of a power transistor. With a large C_{rss}, the rising V_{DS} during turn-off transient easily couples to the gate contact, which boosts up V_{GS} and turns on the transistor unintentionally. Such false turn-on events of a power transistor may result in large switching loss, and may even leads to system failure.

3.5.3 Gate resistance R_G

Apart from C_{rss}, the gate resistance R_G can also change the switching loss, although one significance of R_G is to protect the gate driving circuit. R_G is tunable in power electronics to make a trade-off of switching energy loss and overshoot. A larger R_G will lower I_G and slow down the charging or discharging of gate, which will increase the rise or fall time (t_2~t_3 in Figure 3-10) of drain voltage. A smaller R_G will result in an opposite effect. However, too small R_G will bring another issue of fast switching speed leading to electromagnetic effect. Therefore, R_G should be designed with a suitable value.

Chapter 4 SiC Trench MOSFET with Self-Biased p-Shield (SBS-MOS)

4.1 Motivation for a SBS-MOS

The SiC is an attractive wide-bandgap semiconductor material for building power devices owing to its high critical breakdown field (~3 MV/cm) when compared to silicon (~0.3 MV/cm) [5]. The performance of the SiC power MOSFETs is compromised by the low channel mobility which leads to a high channel resistance and a resultant high overall ON-resistance [5, 54, 101, 102]. Various approaches have been proposed to reduce the channel resistance [103-107], among which, trench gate MOSFETs are a promising solution that allows smaller cell size and increased channel density [102, 108]. However, a high electric field (*E*-field) in the gate oxide can be easily created at the bottom or corners of the trench when the device is biased at the high-voltage OFF-state. The *E*-field is much higher in the gate oxide of SiC based trench MOSFET than Si based trench MOSFET, because at the interface of the semiconductor and oxide, the following equation can be obtained from the Gauss' law.

$$\varepsilon_s \cdot E_s = \varepsilon_{ox} \cdot E_{ox}$$

where ε_s is the dielectric constant of the semiconductor, E_s is the vertical electric field of the semiconductor at the surface, ε_{ox} is the dielectric constant of gate oxide, E_{ox} is the vertical electric field of gate oxide at the surface.

So

$$E_{ox} = \frac{\varepsilon_s}{\varepsilon_{ox}} \cdot E_s$$

The dielectric constants of Si and SiC are 11.9 and 10 respectively, but the critical electric field of SiC is about 2.5 MV/cm which is more than three times that of about 0.7 MV/cm in silicon. Therefore, E_{ox} at breakdown in the SiC trench MOSFET is much larger than that in the Si trench MOSFET.

This high peak *E*-field in the gate oxide could accelerate gate oxide failure, resulting in degraded device reliability [98, 109, 110]. An effective approach to reducing the maximum oxide field ($E_{ox\text{-}m}$) to a safe level (< 3 MV/cm) is to introduce a grounded p-shield region under the gate trench [100, 110, 111]. A floating p-shield has also been studied for power MOSFETs [112, 113], but it is found to worsen the device switching performance and increase the ON-resistance during switching [114-116]. The p-shield leads to the formation of a JFET region that presents a corresponding JFET resistance [97, 117]. Furthermore, the down-scaling of the unit cell is limited by the width of the current path in the JFET regions, hindering the effort to increase the channel density. Several methods have been proposed to relieve the adverse JFET effects, such as adopting a stepped trench gate with the p-shield narrower than the gate [97], or by introducing additional n type doping in the JFET region [117, 118]. These approaches require more complicated processes and/or tighter process controls in order not to compromise the breakdown voltage.

In this chapter, an alternative solution, without structural and process modifications, is proposed for achieving low specific ON-resistance (R_{ON}) in the SiC trench MOSFET by driving the MOS-gate and the JFET gate (p-shields under the trench gate) simultaneously during device operation. Numerical simulations based on Sentaurus TCAD are carried out for this study. The JFET portion is driven by the same gate-drive signal as the MOS-gate through a self-biasing network. The SiC trench MOSFET with a self-biased p-shield (SBS-MOS) boasts a widened current path in the

JFET region at the ON-state, which lowers the JFET resistance and/or allows further size reduction of the cell pitch. Consequently, a low R_{ON} is obtained. The device is comprehensively studied with device simulations. Comparisons are made with conventional trench MOSFET without p-shield (C-MOS) and that with a grounded p-shield (GS-MOS). The SBS-MOS can simultaneously achieve a low R_{ON}, low $E_{ox\text{-}m}$, and a superior figure-of-merit ($Q_{GD} \cdot R_{ON}$).

4.2 Device structure and operating mechanism

The cross-sectional structures of the conventional SiC trench MOSFET (C-MOS), the SiC trench MOSFET with grounded p-shield (GS-MOS) are given in Figure 4-1 (a) and (b) respectively. The proposed SiC trench MOSFET with a self-biased p-shield (SBS-MOS) is shown in Figure 4-2.

The SBS-MOS consists of a main body, which is the same as the GS-MOS, except that the p-shield is not connected to the source. The self-biasing network of the SBS-MOS consists of a series of diodes and a capacitor. D_1, D_2, D_3 as well as D_6 connected to p-shield in the circuit are pn diodes, while D_4 and D_5 are Schottky diodes. The self-biasing network can be integrated monolithically with the main body of the SBS-MOS, which, however, requires a complicated isolation process. An external self-bias network is suggested as a simpler approach, which leaves large flexibility in design. The mechanism and design rules of the SBS-MOS are revealed later. The devices are designed for 1200-V voltage ratings. The drift region (between the n+ substrate and p-body) has a thickness of 12 μm and an n-type doping of 8×10^{15} cm^{-3}. The channel length in all the studied devices is set to be 0.7 μm, while the electron mobility in the channel is set to be 15 $cm^2/V\text{-}s$ [98, 119].

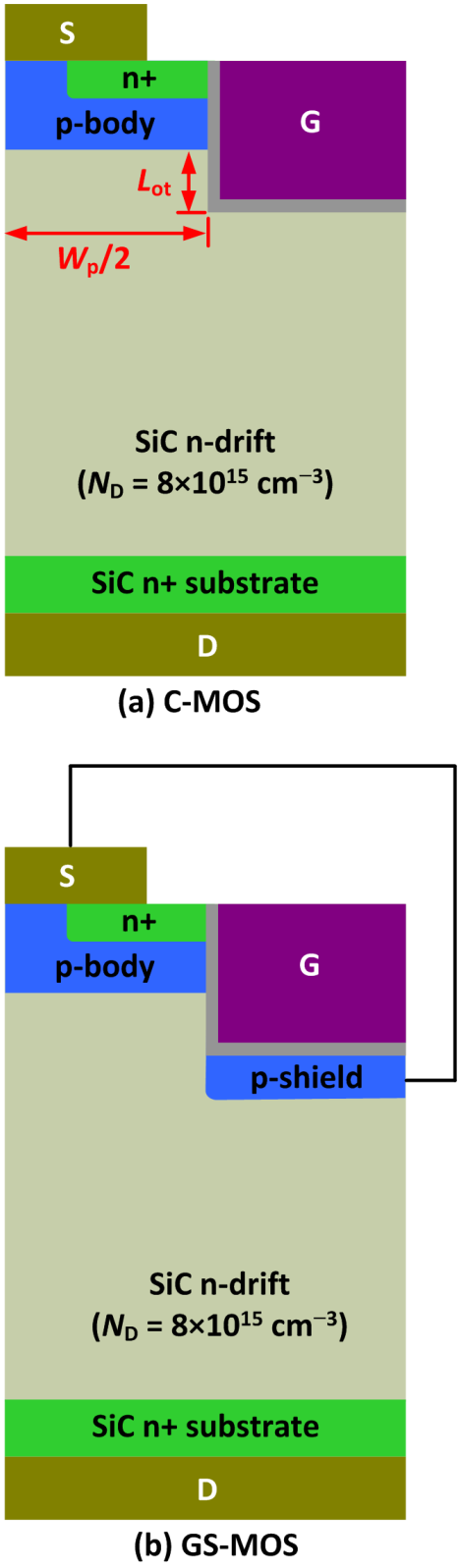


Figure 4-1 Schematic structures of (a) C-MOS, and (b) GS-MOS.

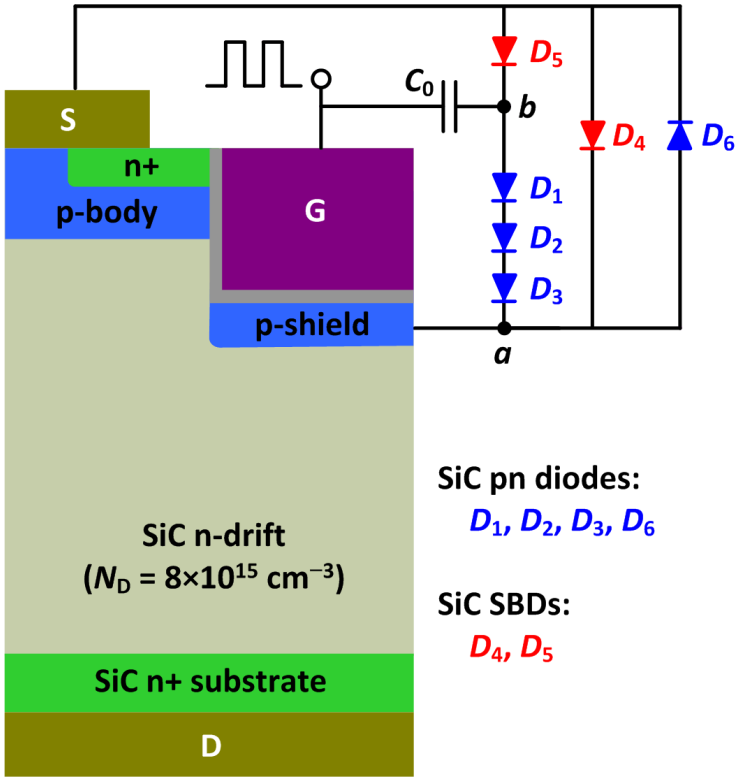


Figure 4-2 Schematic structure of the proposed SBS-MOS. In this study, SiC pn junction diodes are used for D_1, D_2, D_3, and D_6, while SiC SBDs are used for D_4 and D_5. C_0 is 100 nF, except when other values are specified.

At the OFF-state, the trench bottom of the C-MOS suffers from a high oxide *E*-field that can easily exceed the safe operating level in long-term application. The GS-MOS features a buried p-shield under the gate oxide to screen the high drain voltage, since the electric field line emitted from the Drain electrode is firstly terminated at the p-shield. Due to the zero-biased p-shield, the voltage difference between the gate and p-shield is zero at the OFF-state. However, the existence of the p-shields prevents further down-scaling of the cell pitch and limits the overall specific channel resistance. The p-shield region also introduces an additional JFET section with a non-negligible resistance when the p-shield is tied up with the source.

If the p-shield can be independently biased, the R_{ON} of the trench MOSFET with a p-shield could be reduced by modulating the JFET resistance. Figure 4-3 shows the R_{ON} of a trench MOSFET with a p-shield (with a mesa width W_p set to 1 μm) as a function of the voltage applied to the p-shield region (V_{sh}). When the p-shield is grounded (V_{sh} = 0 V), R_{ON} is unacceptably large due to the JFET effect, i.e. the formation of a depletion region around the p-shield. When the p-shield is biased with a positive voltage, e.g. V_{sh} > 2 V, the depletion region is significantly narrowed and the current conduction path is widened. As a result, R_{ON} is dramatically reduced.

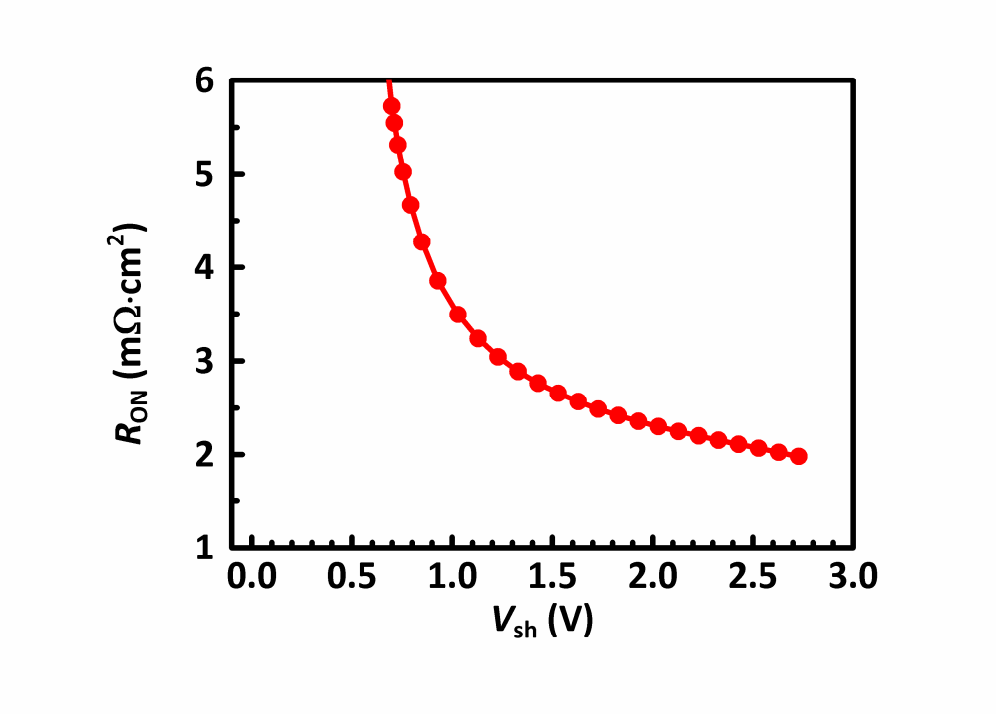


Figure 4-3 Influences of the voltage of the p-shield V_{sh} upon R_{ON} of a SiC trench MOSFET with a p-shield.

The proposed SBS-MOS utilizes a self-biasing network to automatically drive the p-shield with a positive voltage during the switching operation. Therefore, the current path in the JFET regions is widened, resulting in a reduction of the JFET

resistance. Furthermore, as the depletion region of the JFET portion is suppressed by the self-bias on the p-shield, the cell size can be further reduced to achieve a higher channel density and a consequent lower channel resistance.

The switching process of the SBS-MOS is analyzed to reveal the self-biasing mechanism. The switching process is studied with the test circuit shown in Figure 4-4. The supply voltage is 800 V. The device under test (DUT) contains the main body of the SBS-MOS as well as the self-biasing network. The area of the main body of the SBS-MOS is 1 cm^2. A SiC JBS is adopted as a freewheeling diode for continuation of the load current. A current source of 100 A is used to represent the inductance load. A parasitic inductance of 20 nH is assumed in the study. The gate resistance R_G of 5 Ω is used. The gate driving signal is switched between 0 V and 18 V to set the device to the OFF-state and ON-state, respectively.

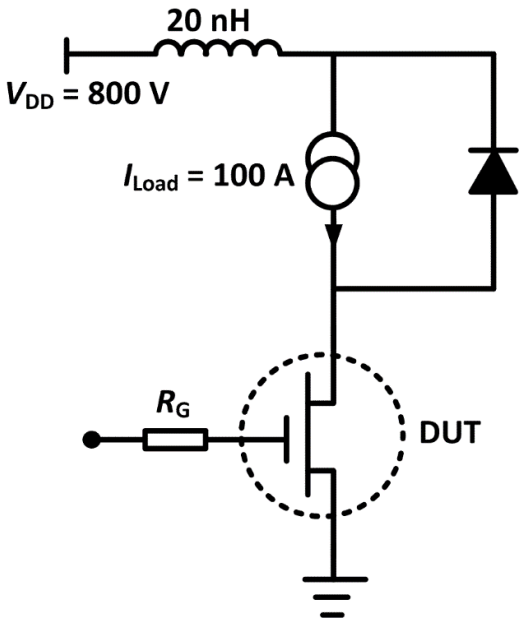
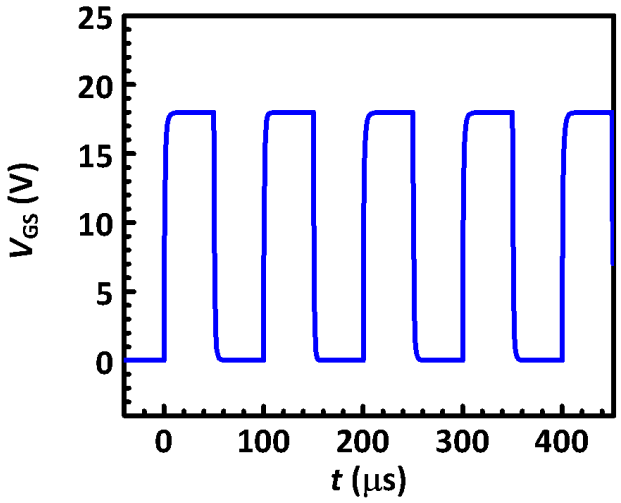
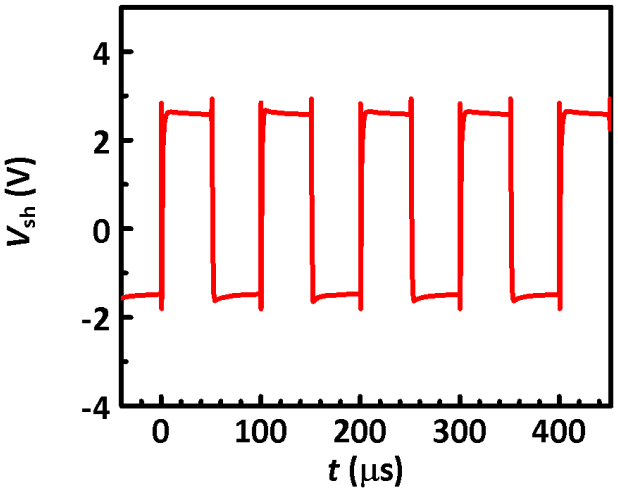


Figure 4-4 Test circuit for switching characteristics of the devices under study. A supply voltage of 800 V and a load current of 100 A are used. The area for the device under test is 1 cm^2. A SiC junction barrier Schottky diode is used to provide a freewheeling path.

Figure 4-5(a) and (b) plot the switching waveforms of the gate voltage V_G and the voltage of the p-shield V_{sh} respectively. The device is initially at the OFF-state. The rising edge of the first driving pulse is set to be t = 0 μs. During each turn-on operation, the V_{sh} is driven to around 2.7 V, which is near the turn-on voltage of the pn junction around the p-shield.



(a)



(b)

Figure 4-5 Switching curves (a) V_{GS} and (b) V_{sh} of the proposed SBS-MOS.

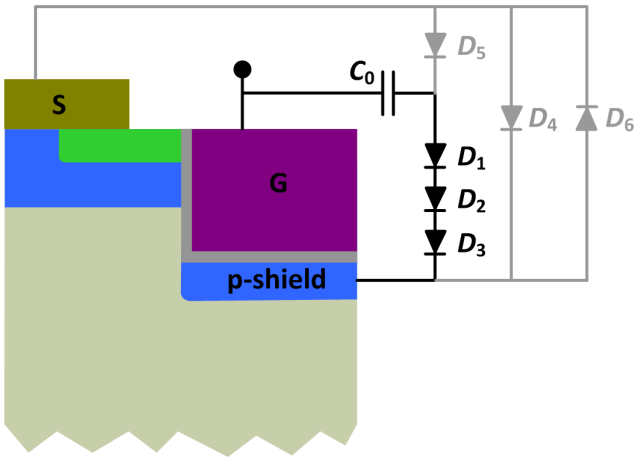
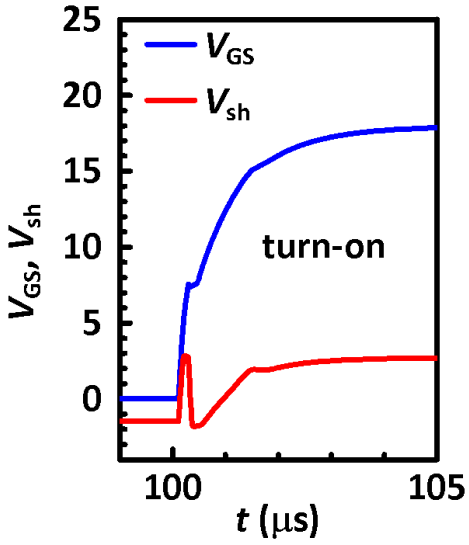


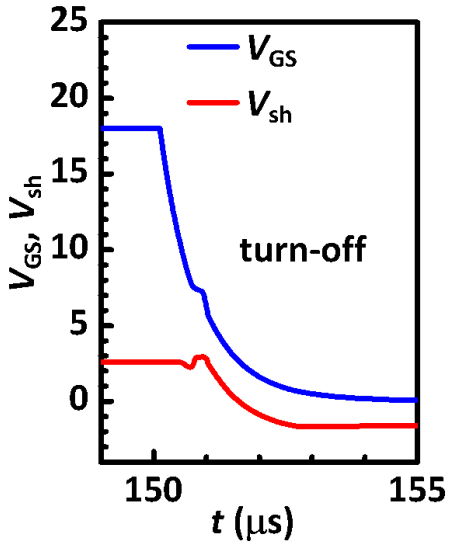
Figure 4-6 Illustration of the charging current path in the first stage of turn-on transient for the SBS-MOS.

The detailed waveforms during turn-on and turn-off transients are shown in Figure 4-7(a) and (b), respectively. At the start of the turn-on transient, the gate-to-source capacitance (C_{GS}) of the main body of SBS-MOS is being charged, leading to an increase of V_{GS}. The p-shield is also being charged during this phase by the gate voltage via the capacitive coupling of C_0. The displacement current flows through D_1-D_3 as shown in Figure 4-6. When V_{GS} reaches the Miller plateau [108], V_{sh} drops due to discharging through the drain-to-shield capacitance (the capacitance between the p-shield and the drain). When V_{sh} reaches −1.8 V, the SBD D_4 is turned on and clamps V_{sh}. The presence of D_4 prevents V_{sh} from becoming too negative; otherwise, a large amount of charge is required to drive V_{sh} to the desired positive value in the following stage. After the Miller plateau, V_{DS} has already dropped to a low value, and its influence upon V_{sh} is negligible. V_{GS} continues to rise and V_{sh} is again charged through the capacitive coupling of C_0. For a short transient before V_{GS} reaches the targeted value, the pn junction around the p-shield enters the forward condition and clamps V_{sh}

around its turn-on voltage. The bipolar conduction of the pn junction ceases once V_{GS} reaches the targeted value, and the injected holes quickly vanish as they are collected by the p-body or recombine with the electrons.



(a)



(b)

Figure 4-7 (a) Detailed switching transient of the turn-on process, (b) detailed switching transient of the turn-off process.

At the start of the turn-off transient, C_{GS} is being discharged, and V_{GS} begins to drop. During the Miller plateau, V_{DS} increases rapidly to the supply voltage. The rising V_{DS} is coupled to V_{sh} via the drain-to-shield capacitance, and to push V_{sh} to a higher value. But due to the presence of the pn junction diode D_6, V_{sh} is clamped by the turn-on voltage of D_6. After the Miller plateau, the drain current quickly drops to 0 when V_{GS} drops below V_{th}. The C_{GS} continues to be discharged until V_{GS} drops to 0. The displacement current for C_{GS} is not effectively provided by the n+ source after V_{GS} becomes lower than V_{th}, since the channel is already turned off. The pn junction at the p-body and/or the p-shield would be contributing to the displacement current, as depicted in Figure 4-8. Close to the p-body, V_A would drop and become clamped by the turn-on voltage of the pn junction. However, as the JFET region is fully depleted at this stage, the region close to the p-shield could have a lower voltage than V_A. Eventually, V_B is clamped by the turn-on voltage of the pn junction plus that of D_4. Consequently, V_{sh} drops and is clamped by the turn-on voltage of D_4.

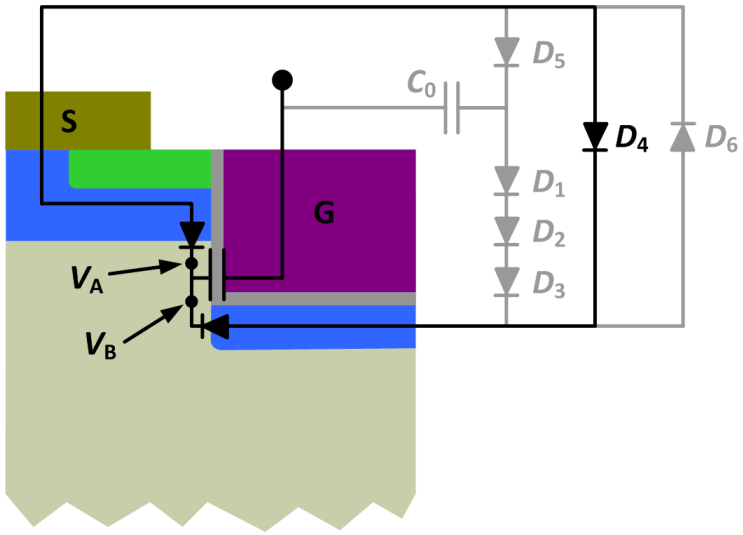


Figure 4-8 Illustration of the discharging current path in the last stage of turn-off transient for the SBS-MOS.

The main component of the self-biasing network is C_0. The diodes are adopted mainly for voltage clamping. The Schottky barrier diodes D_4 and D_5 are used to prevent the voltages at nodes *a* and *b* [as labelled in Figure 4-2] from becoming too negative. The pn diode D_6 is used to prevent the voltage at node *b* from becoming too positive under the influence of a high OFF-state V_{DS}. Besides, D_6 also provides a conduction path for the breakdown current. The pn diodes D_1-D_3 are mainly used to adjust the voltage across C_0, and their impact on the device performance is discussed in the next section.

4.3 Design considerations of self-biasing network

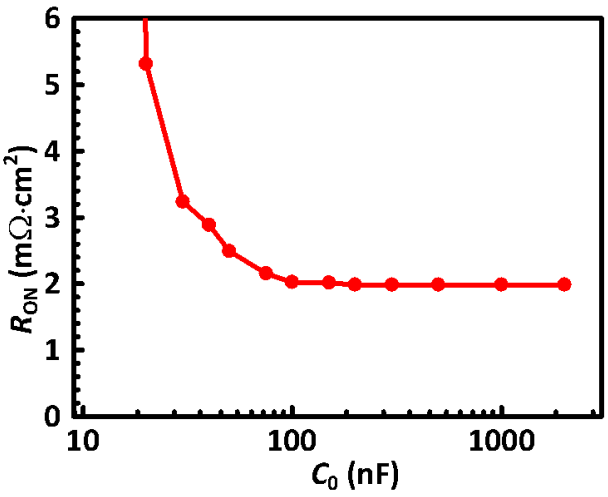


Figure 4-9 The influences of C_0 upon (a) R_{ON}, (b) Q_G and $Q_G \cdot R_{ON}$, and (c) Q_{GD} and $Q_{GD} \cdot R_{ON}$.

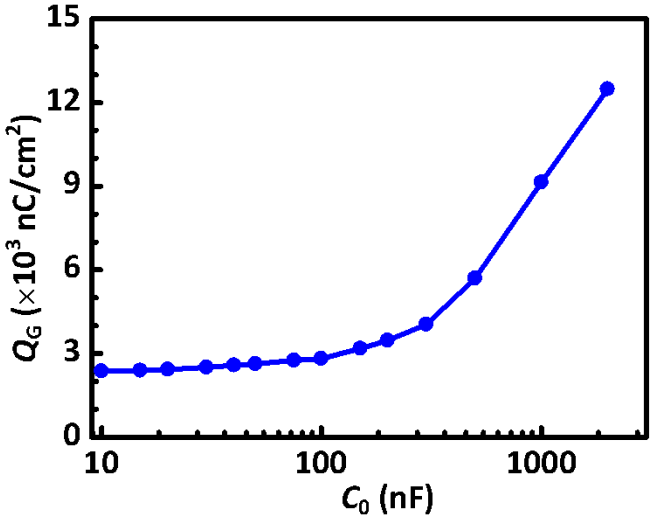


Figure 4-10 The influence of C_0 upon Q_G.

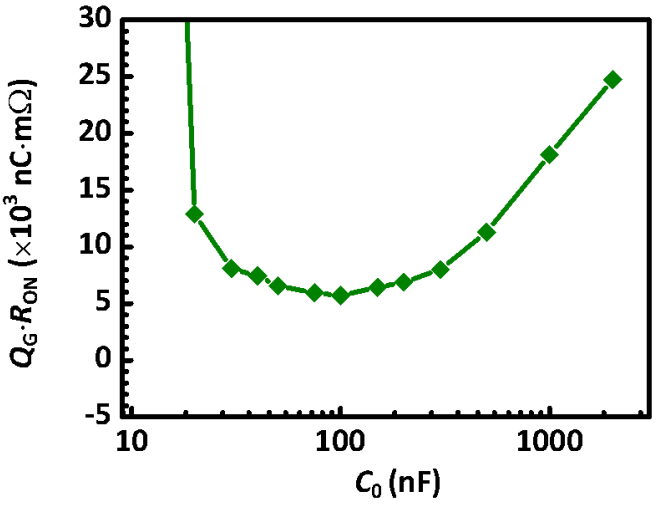


Figure 4-11 The influence of C_0 upon $Q_G \cdot R_{ON}$.

According to the mechanism of the SBS-MOS, the capacitor C_0 is charged and discharged during the switching transients. The value of C_0 is of importance for the operation of SBS-MOS. In the early part of this chapter, the default value of C_0 =

100 nF is adopted for the SBS-MOS with an area of 1 cm^2. Figure 4-9 plots the influence of C_0 upon R_{ON}; if the value of C_0 is too small, the p-shield cannot be charged to the desired positive voltage, resulting in a large R_{ON} for the SBS-MOS. A large C_0 guarantees a low R_{ON}, but from Figure 4-10, too large a C_0 would significantly increase Q_G. Therefore, C_0 allows a trade-off between Q_G and R_{ON}, and $Q_G \cdot R_{ON}$ reaches a minimum when C_0 is ~100 nF, as shown in Figure 4-11. The Q_{GD} is not a strong function of C_0, as shown in Figure 4-12, so the figure of merit $Q_{GD} \cdot R_{ON}$ mainly depends on R_{ON}. As shown in Figure 4-13, when C_0 is ~100 nF, $Q_{GD} \cdot R_{ON}$ almost reaches a minimum.

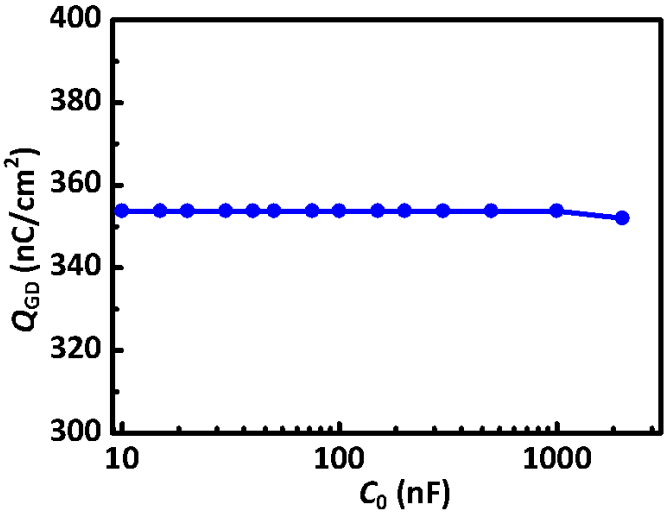


Figure 4-12 The influence of C_0 upon Q_{GD}.

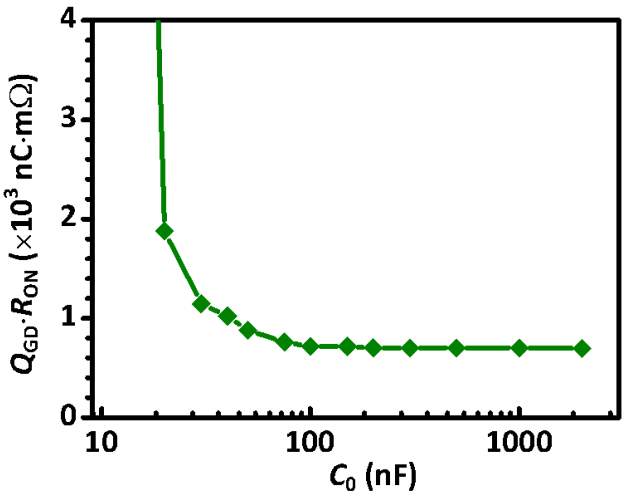


Figure 4-13 The influence of C_0 upon Q_{GD}·R_{ON}.

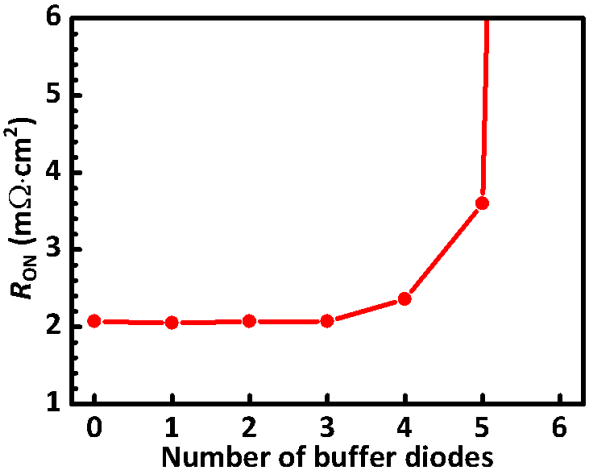


Figure 4-14 The influence of the number of buffer diodes upon R_{ON}.

The pn diodes D_1, D_2 and D_3 are used as voltage buffers for the capacitor C_0. From Figure 4-14, too many diodes will make the self-biasing network less efficient, resulting in a larger R_{ON}. Without these diodes, more charges are required for C_0 during

the switching transients. Figure 4-15(a) and (b) plot Q_G and Q_{GD} of the SBS-MOS with various numbers of pn diodes between the C_0 and p-shield. With more diodes, C_0 would undergo a smaller voltage change during switching, and therefore, less charges are required. From Figure 4-15(a) and (b), both Q_G and Q_{GD} will be decreased with more buffer diodes. The best figures of merit $Q_G \cdot R_{ON}$ and $Q_{GD} \cdot R_{ON}$ are achieved when three buffer diodes are used.

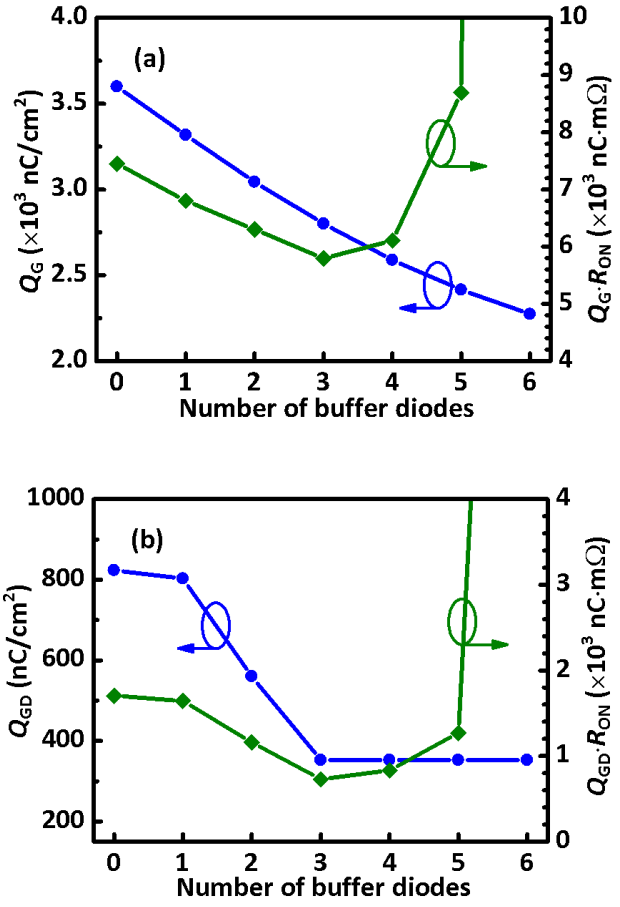


Figure 4-15 The influence of the number of buffer diodes upon (a) Q_G and $Q_G \cdot R_{ON}$, and (b) Q_{GD} and $Q_{GD} \cdot R_{ON}$. The buffer diodes are those between node a and b. As in Figure 4-1(c), three buffer didoes D_1-D_3 are illustrated.

4.4 Device performance

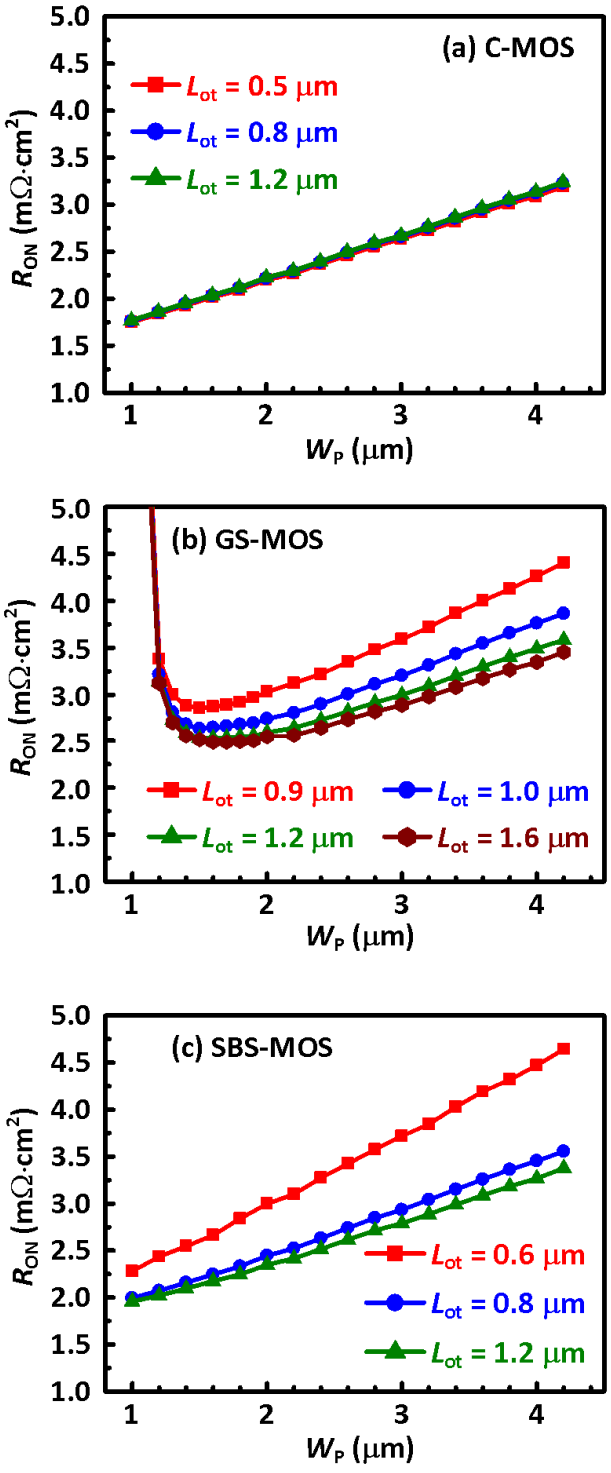


Figure 4-16 Influences of W_P on R_{ON} of (a) C-MOS, (b) GS-MOS and (c) SBS-MOS.

Figure 4-16 plots the R_{ON} of the devices under study. For all the devices, R_{ON} shows a dependence on the distance between adjacent gate trenches, W_p. With a smaller W_p, the cell size is reduced, and the channel resistance per unit area is lowered, leading to a reduction of overall specific R_{ON} in C-MOS. In GS-MOS, however, R_{ON} first decreases with shrinking W_p until W_p is ~1.6 μm, but then begins to increase when W_p is further reduced, showing the limitation in cell size reduction. Such a limitation originates from the JFET region associated with the p-shield. When W_p is smaller than a certain value (e.g. 1.6 μm), the JFET resistance becomes the dominant limiting factor of R_{ON}, and R_{ON} increases. The SBS-MOS, although with p-shields under the trench gate, shows a monotonous decrease of R_{ON} with W_p down-scaled to 1 μm. The JFET resistance between the p-shields is effectively suppressed when the p-shields are self-biased with a positive voltage; it is no longer a limiting factor for R_{ON}. The SBS-MOS and the C-MOS have a larger room for down-scaling the cell size than the GS-MOS.

The over trenched depth L_{ot} (the vertical distance between the gate trench bottom and the p-well bottom, as shown in Figure 4-1(a)) also affects the R_{ON} of the GS-MOS and SBS-MOS, since the JFET effect also exists between the p-well and the p-shield. Figure 4-17 shows the influence of L_{ot} (with the thickness of the n-drift region kept unchanged) on R_{ON}. For the C-MOS and SBS-MOS, W_p is kept at 1 μm, while for the GS-MOS, W_p is 1.6 μm for a minimum R_{ON}. R_{ON} of the C-MOS exhibits a weak dependence on L_{ot}, as the above mentioned JFET effect is not expected in this device. For the GS-MOS and SBS-MOS, R_{ON} is unacceptably large when L_{ot} is very small. It is noted that the GS-MOS requires a much larger L_{ot} than the SBS-MOS to achieve a low R_{ON}. As discussed later, a smaller L_{ot} is preferred since it is less demanding

process-wise, and also leaves a thicker n-drift region to block a larger drain voltage at the OFF-state.

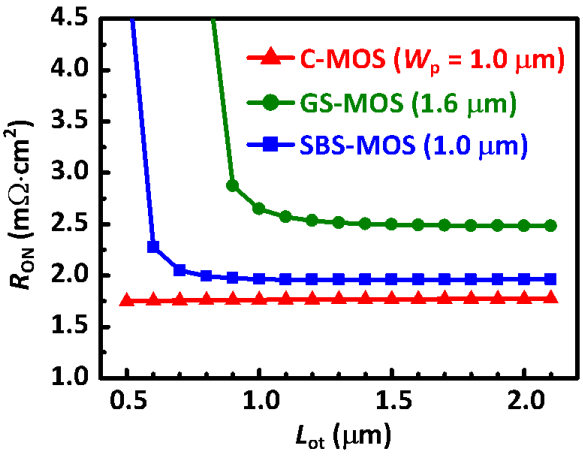


Figure 4-17 Influence of L_{ot} on R_{ON} of the studied devices.

In the following sections, the C-MOS with W_p = 1 μm and L_{ot} = 0.5 μm, the GS-MOS with W_p = 1.6 μm and L_{ot} = 1.1 μm, and the SBS-MOS with W_p = 1 μm and L_{ot} = 0.8 μm, are chosen for further study. The C-MOS, GS-MOS and SBS-MOS with the chosen parameters exhibit R_{ON} values of 1.8 mΩ·cm^2, 2.6 mΩ·cm^2, and 2.0 mΩ·cm^2, respectively.

The OFF-state breakdown characteristics of the devices are shown in Figure 4-18. The C-MOS exhibits the highest OFF-state breakdown voltage (*BV*) of 2046 V, because it doesn't adopt a p-shield to screen the gate oxide. The GS-MOS, however, has a *BV* of 1583 V. This reduced *BV* is caused by the reduced drift region thickness, as well as the larger cell pitch that leads to less uniform electric field distribution. The SBS-MOS has a *BV* of 1800 V, which lies between the C-MOS and the GS-MOS.

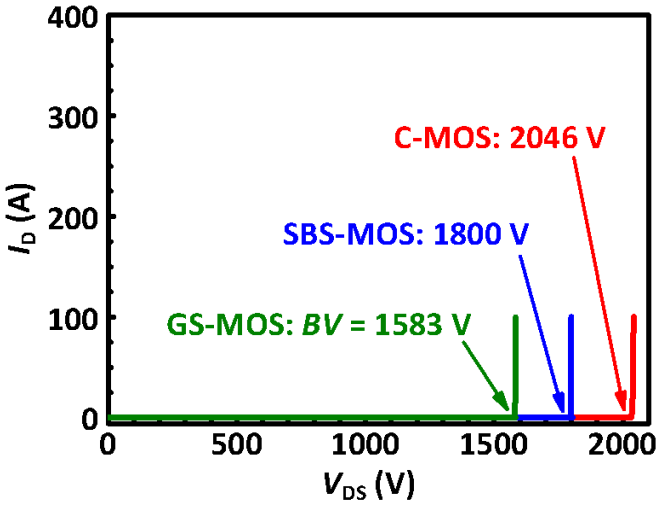


Figure 4-18 OFF-state breakdown characteristics of the studied devices.

Table 4-1 Comparison of the device characteristics

	UNIT	C-MOS	GS-MOS	SBS-MOS
R_{ON}	mΩ·cm^2	1.8	2.6	2.0
BV	V	2046	1583	1800
$E_{ox\text{-}m}$ [a]	MV/cm	6.98	1.22	0.53
Q_G	nC/cm^2	2972	2092	2788
Q_{GD}	nC/cm^2	1269	345	353
$Q_G \cdot R_{ON}$	nC·mΩ	5350	5439	5576
$Q_{GD} \cdot R_{ON}$	nC·mΩ	2284	897	706

[a] $E_{ox\text{-}m}$ at V_{DS} = 1200 V.

Although dielectric breakdown in the gate oxide does not occur in the studied SiC MOSFETs since the breakdown field of an oxide (typically 10~15 MV/cm [120,

121]) is much higher than that of SiC, the high field in the oxide may have already exceeded the safety level for oxide reliability (~ 3 MV/cm). The C-MOS, although with a high *BV*, suffers from the high oxide field at the trench bottom. As shown from Figure 4-19, the $E_{ox\text{-}m}$ of 6.98 MV/cm (at V_{DS} = 1200 V) in the C-MOS far exceeds the safety level (~ 3 MV/cm) for long-term reliability. Therefore, the C-MOS could not satisfy the reliability qualification for commercial applications.

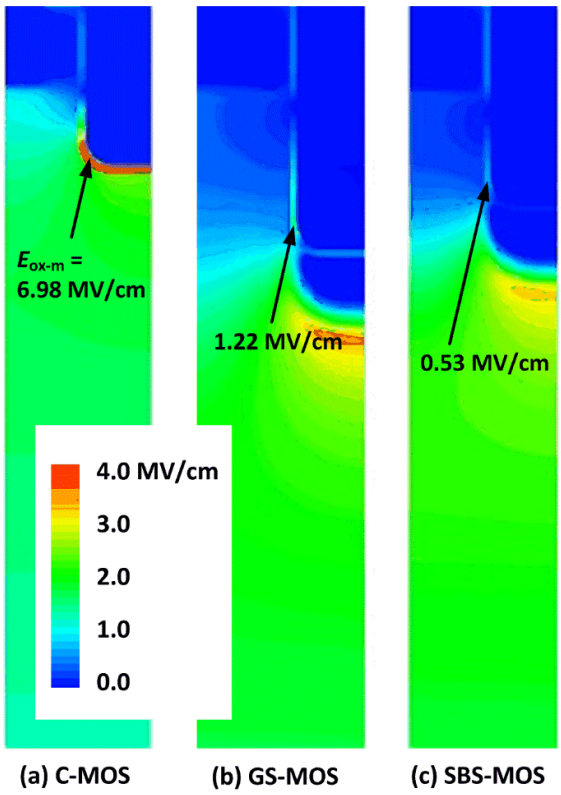


Figure 4-19 Electric field contours at V_{DS}=1200V in the half cell of (a) C-MOS, (b) GS-MOS and (c) SBS-MOS.

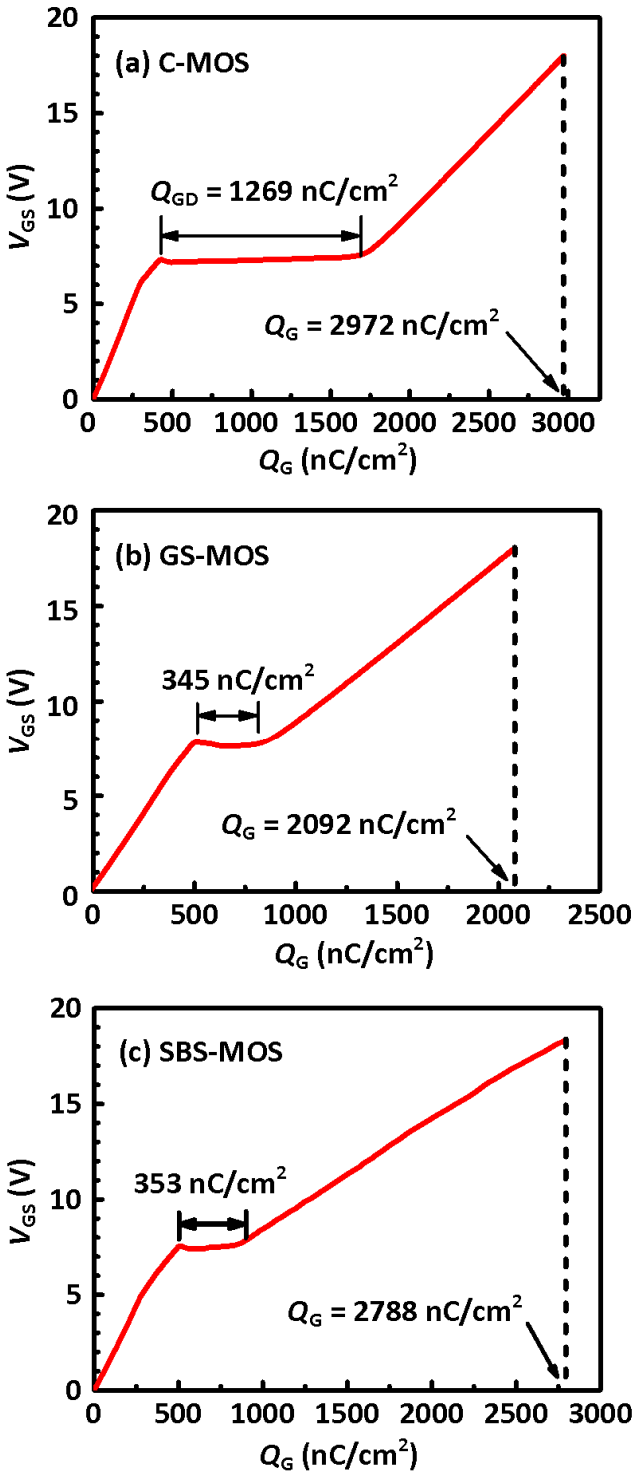


Figure 4-20 Gate charges of (a) C-MOS, (b) GS-MOS and (c) SBS-MOS.

The p-shield region in both the GS-MOS and the SBS-MOS screens the high drain voltage, to result in much reduced $E_{ox\text{-}m}$ values of 1.22 MV/cm and 0.53 MV/cm, which are below the criterion of gate oxide reliability. The lower $E_{ox\text{-}m}$ of the SBS-MOS compared to GS-MOS is due to the closer distance between the adjacent p-shields, which results in a stronger screening effect.

For the SBS-MOS, the self-biasing network is utilized to charge the p-shield region during each switching cycle. Figure 4-20 shows the V_{GS}-Q_G curves of the devices. The C-MOS presents the largest Q_G of 2972 nC/cm^2 and Q_{GD} of 1269 nC/cm^2. The GS-MOS and SBS-MOS both exhibit reduced Q_G and Q_{GD} owing to the presence of the p-shield region. Q_G of the SBS-MOS is 2788 nC/cm^2 which is larger than that of the GS-MOS (2092 nC/cm^2). The Q_{GD} of the SBS-MOS is 353 nC/cm^2, close to that of the GS-MOS (345 nC/cm^2). The higher channel density of the SBS-MOS is one of the reasons for the higher Q_G, when compared to GS-MOS. A test SBS-MOS with the same dimensions as the GS-MOS (W_p = 1.6 μm and L_{ot} = 1.1 μm) is also simulated, and renders a Q_G of 2610 nC/cm^2. It is noted even when the test SBS-MOS features the same device dimensions as the GS-MOS, its Q_G is still higher than the GS-MOS. Thus, additional charges are required for the self-biasing network in the SBS-MOS, which is in agreement with the analysis in last section.

The characteristics of the devices are summarized in Table 4-1. The SBS-MOS exhibits superior performance to the C-MOS and GS-MOS. The high $E_{ox\text{-}m}$ makes the C-MOS unacceptable from the gate oxide reliability point of view, even though it has a low R_{ON}. Besides, the C-MOS also suffers from a high Q_{GD}. The SBS-MOS exhibits a smaller R_{ON} than the GS-MOS at a cost of a slightly increased Q_G. Q_G is related to the driving loss required for a power switch. For high voltage power conversion applications, the driving loss is typically not a significant part when compared to the

switching loss and on-state conduction loss. Therefore, the cost of a higher Q_G in the SBS-MOS is justified. Q_{GD} is critical in determining the switching loss of a power switch, which is one of the major parts of the total power loss for a power switch, especially in high frequency power switching applications. The SBS-MOS presents a similar Q_{GD} compared to the GS-MOS. The commonly used figure of merit $Q_{GD} \cdot R_{ON}$ is 706 nC·mΩ for the SBS-MOS, which is superior to the GS-MOS (897 nC·mΩ) and the C-MOS (2284 nC·mΩ).

4.5 Summary

A SiC trench MOSFET with a self-biased p-shield region is discussed in this chapter. The SBS-MOS utilizes a self-biased p-shield under the gate trench to screen the high drain voltage and thus reduces the oxide field to a safe level. Instead of shorting the p-shield region with the source terminal as in grounded p-shield trench MOSFET, a self-biasing network is utilized to drive the p-shield to a positive voltage, so that the JFET resistance between adjacent p-shields is reduced and further down-scaling of the cell size is allowed. The influences of the self-biasing network upon gate charges are comprehensively studied. Although additional charges are required to drive the self-biasing network, the amount of the additional charges could be minimized with proper design. The optimized SBS-MOS exhibits a low R_{ON}, a low oxide field and a low Q_{GD} simultaneously. The figure of merit $Q_{GD} \cdot R_{ON}$ of the SBS-MOS is better than that of the C-MOS and GS-MOS. Therefore, the proposed SiC SBS-MOS is a promising candidate for power switching applications.

Chapter 5 SiC Trench MOSFET with Protruded p-Body (PB-MOS)

5.1 Motivation for the PB-MOS

The SiC MOSFET is considered as a promising solution for the next generation of power conversion systems, due to the superior material properties of SiC, such as high critical breakdown field, high thermal conductance, capability to work at high temperature [122]. The development of SiC MOSFETs is challenged by the low electron mobility in the MOS-channel which results in a large channel resistance and thus boosts up the total ON-resistance (R_{ON}) [5, 101]. Many approaches have been proposed in the past decade to reduce the channel resistance of SiC MOSFET, such as reduction of the channel length, improvement of the channel mobility via process optimization or structure design [54, 57, 103, 105, 106, 123]. Among these efforts, the trench MOSFET structure is widely considered as a promising method, and allows a more compact cell design, and thus lowers the device R_{ON} by a higher channel density [98, 108, 124].

The trench MOSFET is a commercially mature technology for silicon based power devices. When used in wide bandgap SiC devices, the trench MOSFET faces a critical issue for its commercial success: the high OFF-state oxide field at the trench bottom/corner. This high oxide field is a byproduct when SiC utilizes its significantly higher critical breakdown field. For long term application, it is commonly desired to keep the maximum oxide electric field below 3 MV/cm [99, 125]. A p-shield under the trench gate is proposed as an oxide protection. However, the p-shield is required to be well grounded to the source contact, otherwise the safe operation area of the device is compromised [126] and the switching performance of the device is degraded

[115, 116]. Therefore, a large position of the chip area is sacrificed for contact vias, which surely increases the cost. The double trench structure reduces the oxide field with an additional source trench, which is shown in Figure 5-1, however, adds to difficulty in minimizing the device cell size (thus is difficult to exert the full potential of the SiC trench MOSFET in terms of the increasing high channel density) [98, 99, 127].

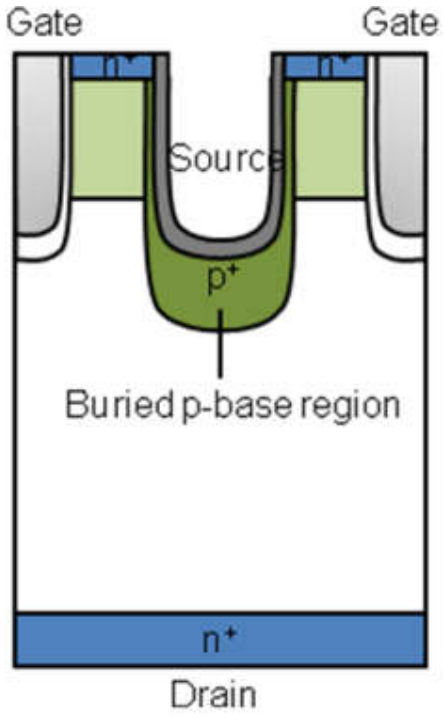


Figure 5-1 The cross-sectional structure of double trench SiC MOSFET.

The conventional trench MOSFET (C-MOS) features a gate trench deeper than the p-bodies. In this study, we propose that a trench MOSFET structure with protruded p-body (PB-MOS), i.e. p-body deeper than the gate trench, is better suited for SiC technology. Comprehensive device simulations based on Sentaurus TCAD have been implemented to reveal the benefits of the proposed structure. The lateral pinch-off effect of the protruded p-body in the PB-MOS protects the gate trench from the high

OFF-state drain voltage, leading to a lower OFF-state oxide field. A low R_{ON} is maintained in the PB-MOS by additional JFET doping to ameliorate the newly introduced JFET resistance. The switching performance of the PB-MOS is also significantly improved owing to the reduction in C_{rss}.

5.2 Simulation models

The simulation study in this chapter is based on the 4H-SiC. The electron/hole continuity equations and Poisson equation are solved self-consistently, with SRH recombination, Auger recombination, incomplete dopant ionization, band narrowing, doping dependent transport, anisotropic material properties and impact ionization taken into account [128]. The electron and hole impact ionization coefficients from Ref. [129] are adopted in this study.

5.3 Device mechanism and proposed process flow of the PB-MOS

Figure 5-2 and Figure 5-3 show the schematic cross-sectional structures of the C-MOS and the proposed PB-MOS, respectively. For the C-MOS, the gate trench is etched through the p-body region, and extends into the drift region. The channels are located at the sidewall of the p-body. With a positive gate voltage to turn on the channel, electrons could flow from the n+ source region to cross the channel, and finally reach the drain.

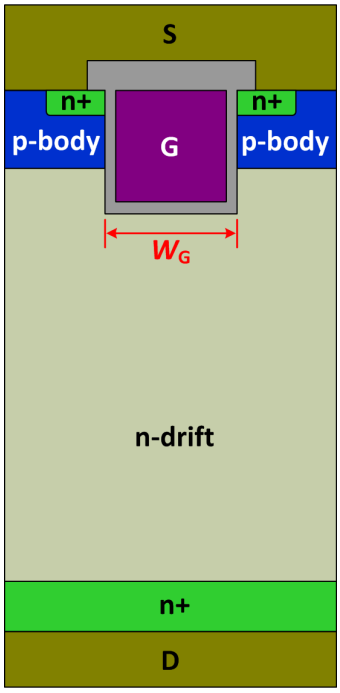


Figure 5-2 Schematic cross-sectional structure of the conventional trench MOSFET (C-MOS). The width of the gate trench is W_G.

The PB-MOS features protruded p-bodies, and is deeper than its gate trench by L_{ot}. The channels are located at the sidewall of the etched p-body. With a positive gate voltage to turn on the channel, electrons could flow from the n+ source region to the region between the protruded p-bodies, and finally reach the drain. In this work, the devices are designed for a 1200-V voltage rating. For both devices, the doping concentration of the drift region is 8×10^{15} cm^{-3}, while the thickness of the epi-layer (from n+ substrate to the semiconductor surface) is 13 µm. The channel length is 0.5 µm, and the MOS-channel mobility is assumed to be 20 cm^2/V-s. The p-bodies are doped with $N_A = 2 \times 10^{17}$ cm^{-3}. For the C-MOS, the width of the gate trench is W_G = 1 µm, and the cell pitch is W_{cell} = 3 µm. For the PB-MOS, L_{ot} and W_G are the parameters to be optimized, and the cell pitch is $W_{cell} = W_G + 2$ µm.

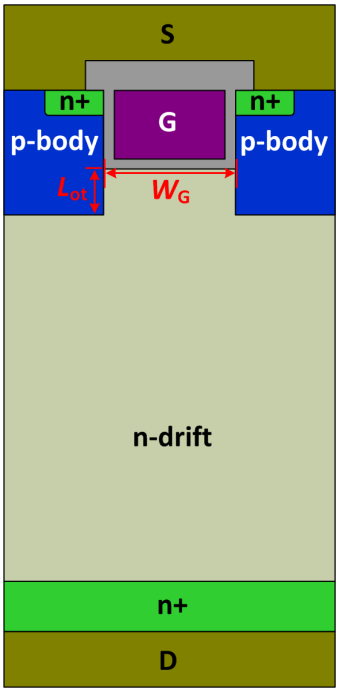
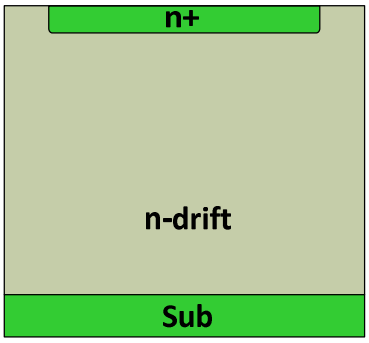


Figure 5-3 Schematic cross-sectional structure of the proposed protruded p-bodies trench MOSFET (PB-MOS). The width of the gate trench is W_G, and the p-bodies protrude beyond the gate trench by L_{ot}.

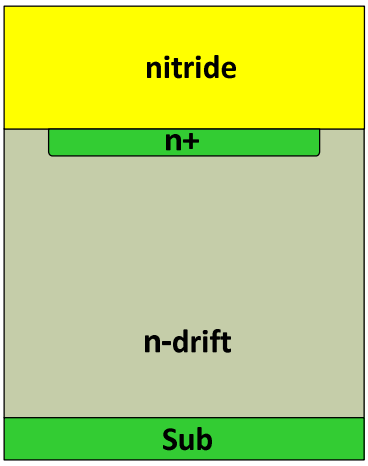
5.4 Proposed process flow of the PB-MOS

The proposed fabrication method for the PB-MOS is illustrated in Figure 5-4, which is designed according to a typical fabrication process of C-MOS (shown in Appendix). A dummy gate technology, which was developed for silicon CMOS, is suggested to form the protruded p-bodies [130, 131]. An n+ Si-face SiC substrate with 4° off-axis angle is suggested as the starting wafer. A n-drift layer is grown on the n+ substrate. The doping and thickness of the drift layer is designed for the required blocking voltage. An ion implantation is performed on the patterned SiC surface to serve as the n+ source regions for the MOSFET. A dielectric (e.g. SiN) is deposited and patterned to serve as a hard mask. An etching step is carried out to form a gate

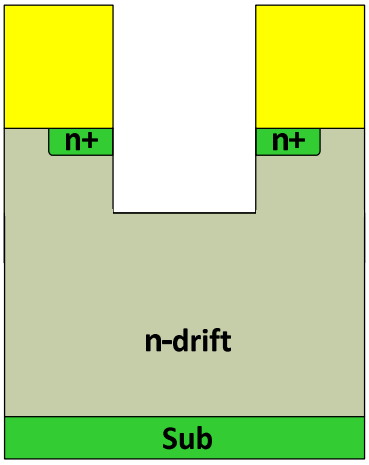
trench. The channel length of the SiC MOSFET is determined by the difference of the trench depth and the n+ source region thickness. A second hard mask layer is deposited all over the wafer, and then is etched back to expose the first hard mask. The first hard mask is removed with a wet etch to leave the second hard mask as a dummy gate self-aligned to the gate trench. The dummy gate serves as a hard mask for the implantation to form p-body regions. In SiC technology, an oxide is a popular implantation mask for energy up to several MeV [6, 100], and therefore is a material of choice for the dummy gate. A metal mask could also be considered, which providing a high blocking capability for the implanted ions [6]. After formation of the p-bodies, the dummy gate is removed with a wet etch. The wafer is capped with a carbon layer and a high temperature annealing is conducted to activate the dopants. With the carbon layer removed by oxygen plasma, the gate dielectric is formed by thermal oxidation or deposition, followed by polysilicon deposition. The polysilicon layer is etched back. An insulating layer is then deposited to serve as isolation. Contact holes through the isolation are then formed and metal contacts are formed and sintered. It is noted that the fabrication flow of the proposed PB-MOS is similar to the C-MOS, except a small modification in the p-body region is formed.



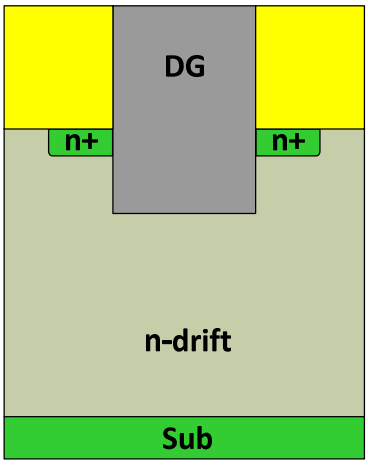
(a) n+ doping



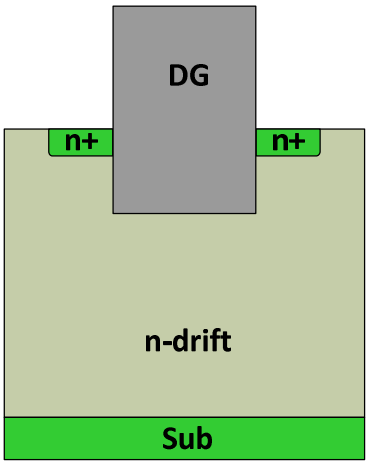
(b) nitride deposition



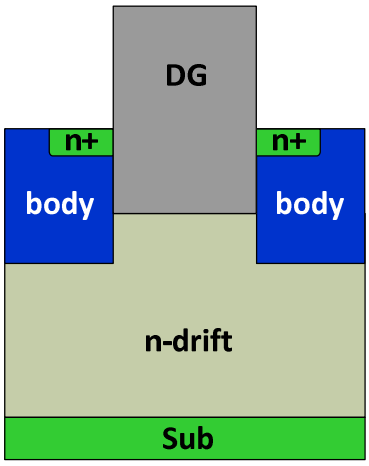
(c) trench formation



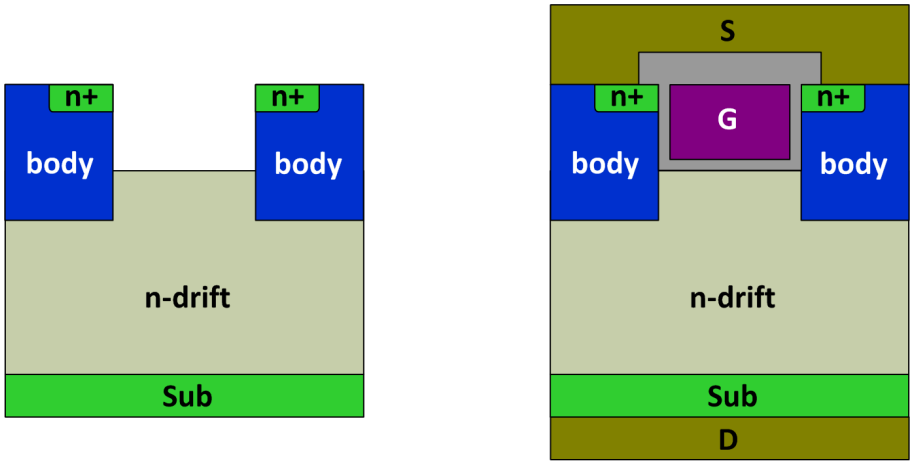
(d) dummy gate by deposition and etch back



(e) nitride strip



(f) p-body implantation



(g) dummy gate removal (h) gate and contact

Figure 5-4 The proposed process flow for the PB-MOS. A dummy gate is used in this flow as an implantation mask.

5.5 Static performance of the PB-MOS

The extent that the p-bodies protrude beyond the gate trench (L_{ot}) and the width of aperture between the protruded p-bodies (W_G) are critical for the performance of the PB-MOS. The protruded p-bodies shield the gate oxide by terminating most of the electric field lines originating from the positive space charges in the drift region, which would otherwise pass through the gate oxide to elevate the oxide field. As shown in Figure 5-5, a larger L_{ot} or a smaller W_G enhances the shielding effect from the protruded p-bodies, thus helping reduce the maximum oxide field ($E_{ox\text{-}m}$). A large L_{ot} results in a strong JFET effect, but sacrifices the R_{ON} to some extent. A smaller W_G also leads to a larger JFET resistance, but the smaller W_G results in higher channel density, which reduces the channel resistance, so the two trends compensate each other, resulting in a smaller R_{ON} dependence on W_G. Therefore, a smaller W_G is preferred

since it presents a better trade-off between the R_{ON} and oxide field than in elongating L_{ot}.

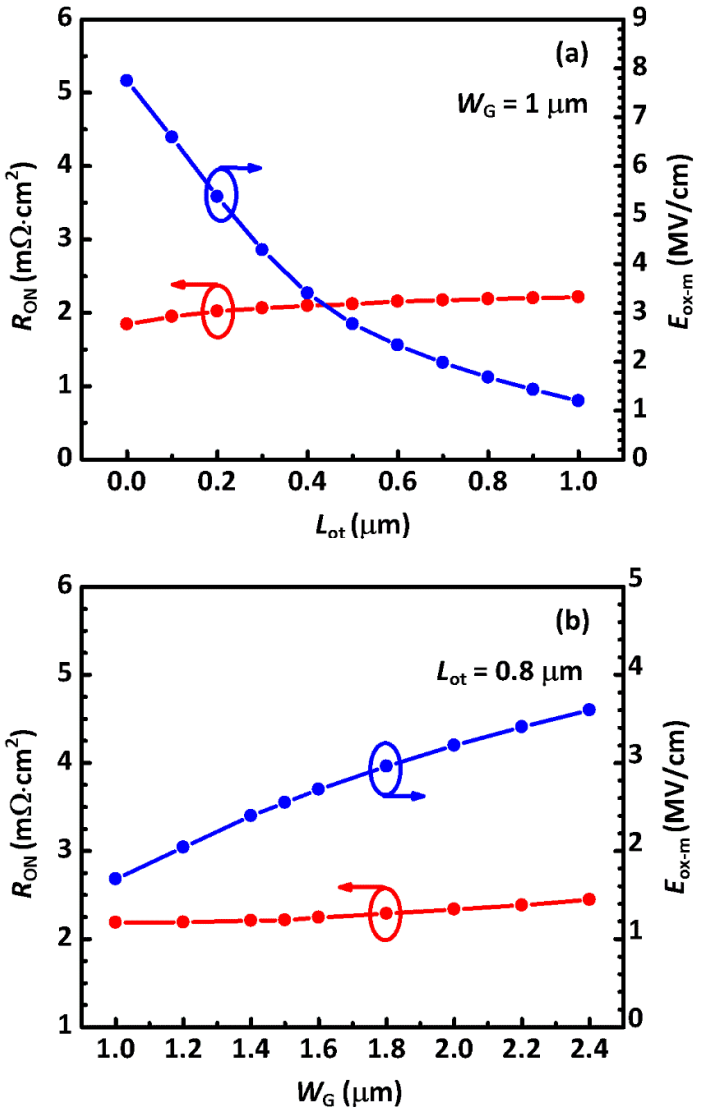


Figure 5-5 The influence of (a) L_{ot} and (b) W_G upon R_{ON} and E_{ox-m} in the PB-MOS. E_{ox-m} is defined as the maximum oxide field at V_{GS} = −5 V and V_{DS} = 1200 V. W_G = 1 μm and L_{ot} = 0.8 μm are chosen for the PB-MOS for comparisons with the C-MOS in the rest part of the study.

With the above analysis and also the ease in fabrication taken into consideration, L_{ot} = 0.8 μm and W_G = 1.0 μm are reasonable parameters for the PB-MOS, which renders an R_{ON} of 2.2 mΩ·cm^2 and an $E_{ox\text{-}m}$ of 1.7 MV/cm. In the following part of this study, the PB-MOS with the chosen parameters is used for comparisons with the C-MOS, unless otherwise specified.

The *I-V* characteristics of the devices are plotted in Figure 5-6. The PB-MOS presents a very similar R_{ON} (2.2 mΩ·cm^2) to that of the C-MOS (2.1 mΩ·cm^2). The saturation current of the PB-MOS is much lower than that of the C-MOS, which is due to the pinch-off by the protruded p-bodies at high V_{DS} [132]. A low saturation current is beneficial for the short-circuit capability of a power transistor. The breakdown voltage of the PB-MOS is 1796 V, which is close to that of the C-MOS (1865 V). This slight degradation of the breakdown voltage in the PB-MOS is well justified by the benefits from other aspects.

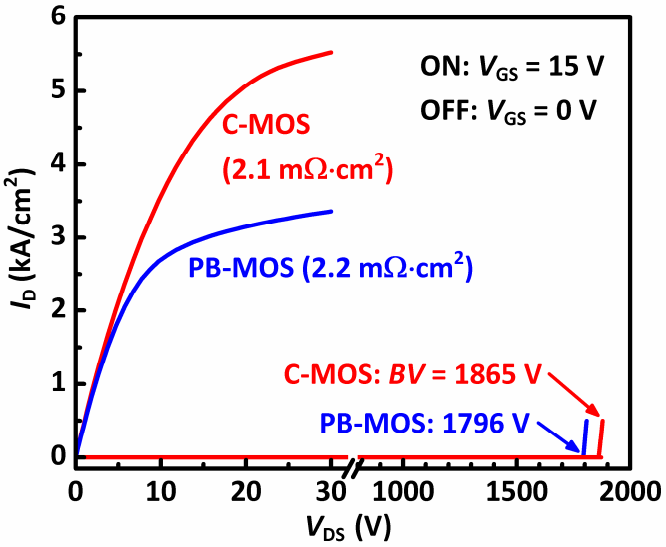


Figure 5-6 The *I-V* characteristics of the C-MOS and the PB-MOS.

The OFF-state electric field distributions (at V_{GS} = −5 V and V_{DS} = 1200 V) of the C-MOS and the PB-MOS are shown in Figure 5-7. The C-MOS suffers from a high maximum oxide field ($E_{ox\text{-}m}$) of 8.6 MV/cm located at the trench corner, and an oxide field of 6.2 MV/cm at the trench bottom, both of which far exceed the acceptable level of 3 MV/cm. The profile of the trench corner is process dependent. A rounded corner with a large radius of curvature is expected to result in a lower local oxide field, but it is likely to be no less than that at the trench bottom [102]. With the shielding effect by the protruded p-bodies, the $E_{ox\text{-}m}$ in the PB-MOS is lowered to 1.7 MV/cm, and is located at the middle of trench bottom.

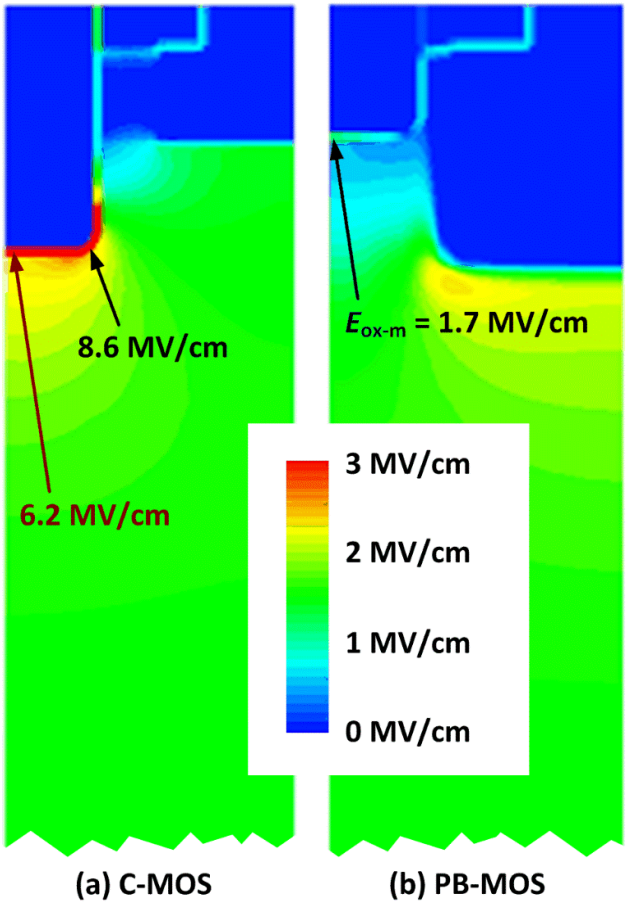


Figure 5-7 OFF-state electric field contours of (a) the C-MOS and (b) the PB-MOS at V_{GS} = −5 V and V_{DS} = 1200 V.

A low reverse transfer capacitance (C_{rss} = C_{GD}) is of great importance for reducing the switching loss and preventing false turn-on. Figure 5-8 presents the C_{rss} of the C-MOS and that of PB-MOS as a function of V_{DS}. Owing to the capacitive screening effect of the protruded p-bodies, the PB-MOS exhibits a remarkably lower C_{rss} than C-MOS.

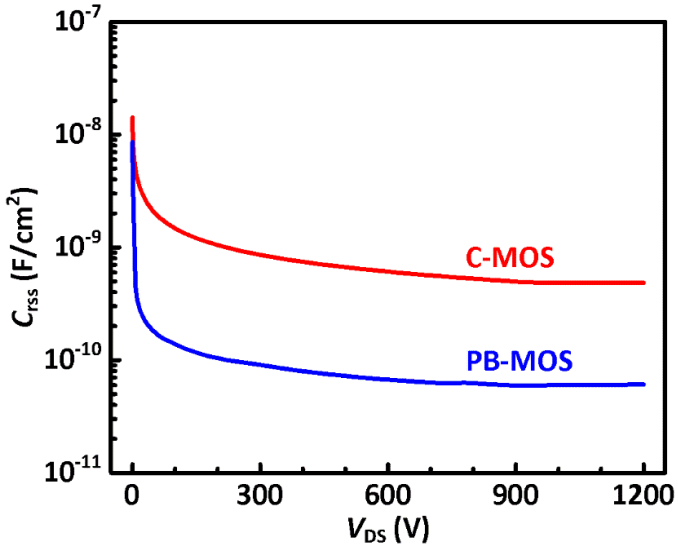


Figure 5-8 Reverse transfer capacitance (C_{rss}) of the C-MOS and the PB-MOS with V_{GS} = 0 V.

The gate charges of the devices are tested with the circuit in Figure 5-9(b). A SiC Schottky barrier diode is used to provide a freewheeling path. The MOSFET and the SBD both have an area of 1 cm^2. The supply voltage is 800 V. The load current is set to be 200 A. V_{GS} is switched from −5 V to +15 V. With a gate current to charge the input capacitance (C_{iss} = C_{GD} + C_{GS}), V_{GS} is increased to above V_{th} until the Miller plateau is reached when all the load current is diverted from the freewheeling diode

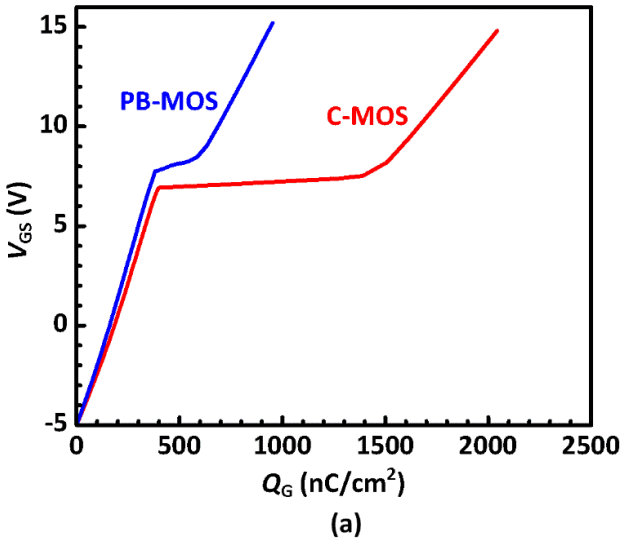
into the MOSFET. At the Miller plateau, V_{DS} drops (and so does the V_{DG}) at a high speed. Therefore, most of the gate current is used to charge C_{rss} (= C_{GD}) during Miller plateau, leaving V_{GS} nearly unchanged. At the Miller plateau, high I_D and high V_{DS} exist simultaneously, and the duration at this plateau (Q_{GD}) plays a significant role in determining the switching loss of the power MOSFET [108]. For the C-MOS, Q_G = 2043 nC/cm^2 and Q_{GD} = 988 nC/cm^2, while for the PB-MOS, Q_G = 952 nC/cm^2 and Q_{GD} = 204 nC/cm^2. Therefore, both Q_G and Q_{GD} are dramatically reduced in the PB-MOS. The reduction in the gate charges in the PB-MOS is mainly due to the smaller C_{rss}, which requires much less charge from the gate terminal to sustain the same drain voltage. A lower Q_G is beneficial for reduction of the driving loss, while a lower Q_{GD} is critical for reduction of the switching loss.

Table 5-1 Comparison of the device characteristics

	Unit	C-MOS	PB-MOS
R_{ON}	mΩ·cm^2	2.1	2.2
BV	V	1865	1796
$E_{ox\text{-}m}$ [a]	MV/cm	8.6	1.7
C_{rss} [b]	pF/cm^2	529	62.5
Q_G	nC/cm^2	2043	952
Q_{GD}	nC/cm^2	988	204
$Q_G \cdot R_{ON}$	nC·mΩ	4290	2094
$Q_{GD} \cdot R_{ON}$	nC·mΩ	2075	449

[a] $E_{ox\text{-}m}$ at V_{GS} = −5 V and V_{DS} = 1200 V.

[b] C_{rss} at V_{GS} = 0 V and V_{DS} = 800 V.



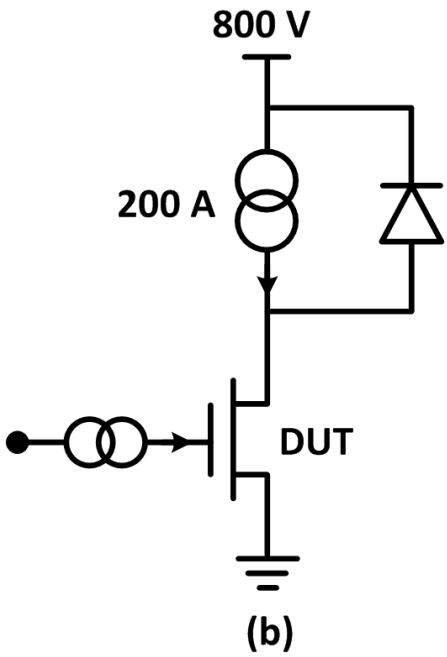


Figure 5-9 (a) V_{GS}-Q_G characteristics of the C-MOS and the PB-MOS. V_{GS} is switched from −5 V to +15 V. For the C-MOS, Q_G = 2043 nC/cm^2 and Q_{GD} = 988 nC/cm^2, while for the PB-MOS, Q_G = 952 nC/cm^2 and Q_{GD} = 204 nC/cm^2. (b) The circuit used for the gate charge test.

Considering that the two devices have similar R_{ON} values, the PB-MOS boasts much better figures of merit, $Q_G \cdot R_{ON}$ = 2094 nC·mΩ and $Q_{GD} \cdot R_{ON}$ = 449 nC·mΩ,

compared to $Q_G \cdot R_{ON}$ = 4290 nC·mΩ and $Q_{GD} \cdot R_{ON}$ = 2075 nC·mΩ for the C-MOS. For a better comparison, the key characteristics of the C-MOS and the PB-MOS are summarized in Table 5-1.

5.6 Dynamic performance of PB-MOS

The switching performance of the studied SiC MOSFETs is simulated using the test circuit in Figure 5-10. Similar to the gate charge test, a SiC Schottky barrier diode is used to provide a freewheeling path. The MOSFET and the SBD both have an area of 1 cm^2. The supply voltage is 800 V. The load inductance is 200 µH. The stray inductance is assumed to be 10 nH. V_{GS} is switched between −5 V and +15 V to set the device to the OFF- and ON-state, respectively.

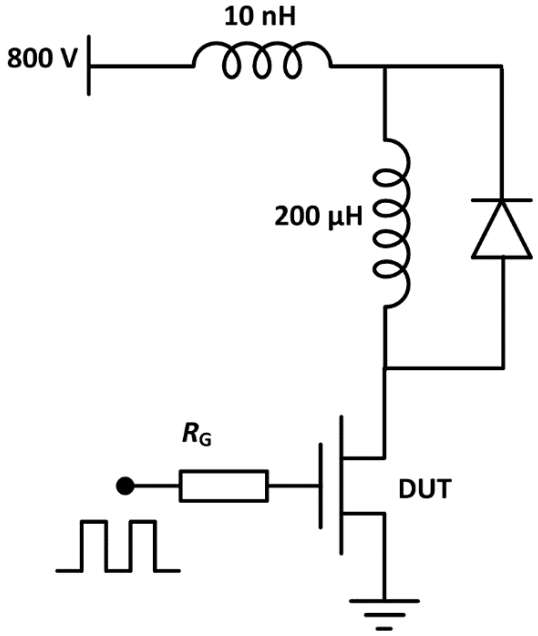


Figure 5-10 Circuit used for the switching tests.

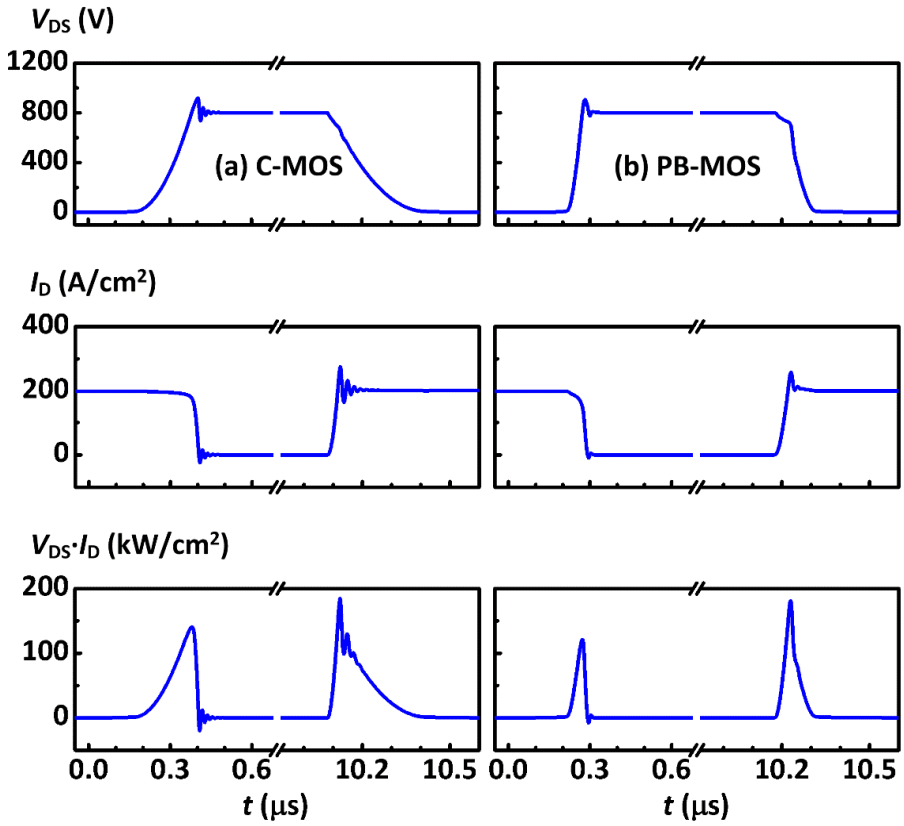


Figure 5-11 Switching waveforms of (a) the C-MOS and (b) the PB-MOS. The circuit in Figure 5-10 is used for the switching test, with R_G = 3 Ω for the C-MOS and 7 Ω for the PB-MOS.

Figure 5-10 Figure 5-11 shows the switching waveforms of (a) the C-MOS and (b) PB-MOS. The circuit in Figure 5-10 is used for switching test, with R_G = 3 Ω for the C-MOS and 7 Ω for the PB-MOS. The MOSFET is switched off at t = 0 μs and then switched on at t = 10 μs. The switching speed of the PB-MOS is appreciably faster than that of the C-MOS during both the turn-off and turn-on transients. By integrating the power (V_{DS}·I_D) waveform against time, the energy loss for the turn-off transient and turn-on transient are calculated. The PB-MOS boasts a turn-off energy loss (E_{OFF}) of 4.4 mJ/cm^2 and a turn-on energy loss (E_{ON}) of 8.6 mJ/cm^2, while the C-MOS suffers from a much higher turn-off energy loss, (E_{OFF}) of 13.6 mJ/cm^2 and a turn-on energy

loss (E_{ON}) of 16.7 mJ/cm^2. Current and voltage overshoots during switching transients are undesirable for a power conversion system. From Figure 5-12, the PB-MOS exhibits a voltage overshoot of 105 V during turn-off transients, and a current overshoot of 57 A/cm^2 during turn-on transients. As a comparison, the C-MOS suffers from a larger voltage overshoot of 119 V and a larger current overshoot of 75 A/cm^2.

Both the electrical overshoots and switching energy are tunable with R_G in real applications of power devices. A smaller R_G is favorable for faster switching, but results in a more severe overshoot. Figure 5-12 presents the trade-off between electrical overshoots and the switching loss. The PB-MOS exhibits much improved trade-off curves, which provide the PB-MOS with particular advantages over the C-MOS for high frequency switching applications.

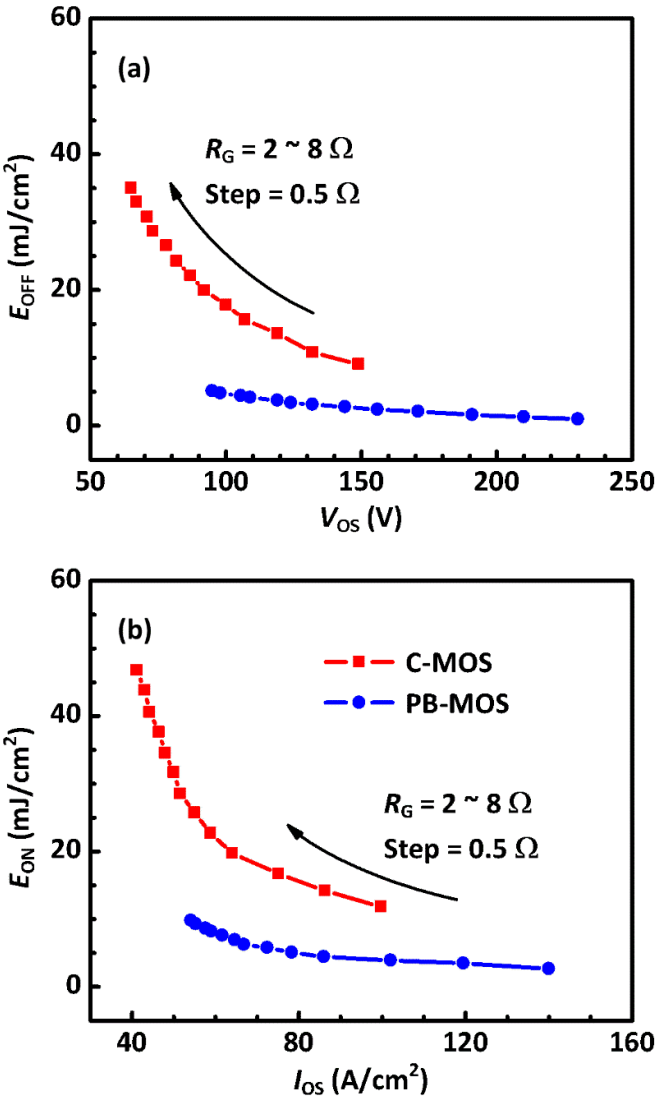


Figure 5-12 (a) The trade-off curve between the voltage overshoot (V_{OS}) and the turn-off energy loss (E_{OFF}) of the studied MOSFETs, and (b) the trade-off curve between the current overshoot (I_{OS}) and the turn-on energy loss (E_{ON}), as R_G is varied.

5.7 Summary

A SiC trench MOSFET with protruded p-bodies (PB-MOS) is described in this chapter as a promising structure for a SiC power transistor. Compared to the

conventional trench MOSFET (C-MOS), the PB-MOS achieves a dramatically lower OFF-state oxide field, due to the shielding effect provided by the protruded p-bodies. The proposed structure also helps reduce C_{rss}, which further leads to a reduction in the gate charges. The switching characteristics are also present, with the PB-MOS exhibiting a much lower switching energy loss during both the turn-on and the turn-off transients. All the benefits in the PB-MOS are achieved with inconsiderable sacrifice of other performances, such as R_{ON} and BV. Much better figures of merit $Q_G \cdot R_{ON}$ and $Q_{GD} \cdot R_{ON}$ are obtained with the proposed PB-MOS. Therefore, the PB-MOS is a promising approach for utilizing SiC in next generation of power conversion systems.

CHAPTER 6 SiC JBS with Ohmic or Schottky Contact to the p-Grid

6.1 Motivation for the study of contact types to p-grid in SiC JBS

Power devices typically feature a junction to block the high OFF-state voltage [33]. For an n-type device, a localized p-region is usually created to form a pn junction. In power transistors, such p-regions are typically termed p-bodies, since they also serve to provide a gate-controlled channel to the transistor. For JBS diodes, such p-regions are routinely named p-grids [133, 134]. In this part, the term p-grid is adopted in discussion of any type of power device with a p-region for voltage blocking. Since in the blocking state, the pn junction is reversely biased to withstand the high voltage, the p-grids are typically connected to the low voltage level. In power transistors, such as the power MOSFET, the p-grid is grounded to the source electrode, while in the JBS, the p-grid is connected to the Schottky anode. From this aspect, the electrical contact to the p-grids only serves to fix the potential of the p-grid in the blocking state [135]. Recently, it was proposed to have a rectifying contact to the p-grid in the IGBT so that the minority carrier concentration near the emitter side is enhanced [136]. The blocking capability of the proposed IGBT configuration is maintained, since in the off-state the contact to the p-grid is in forward conducting condition, therefore clamping the potential of the p-grid at the turn-on voltage of the rectifying contact. A rectifying contact to the p-grid is also proposed/discussed for the SiC JBS to suppress the minority injection from the p-grid, while maintaining the blocking capability of the device [69, 137], as shown in Figure 6-1.

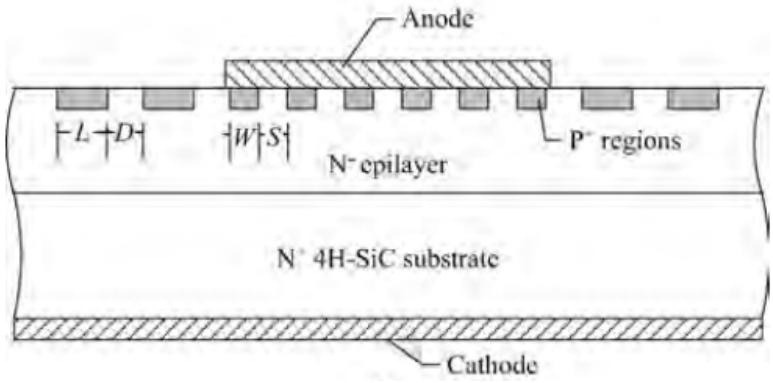
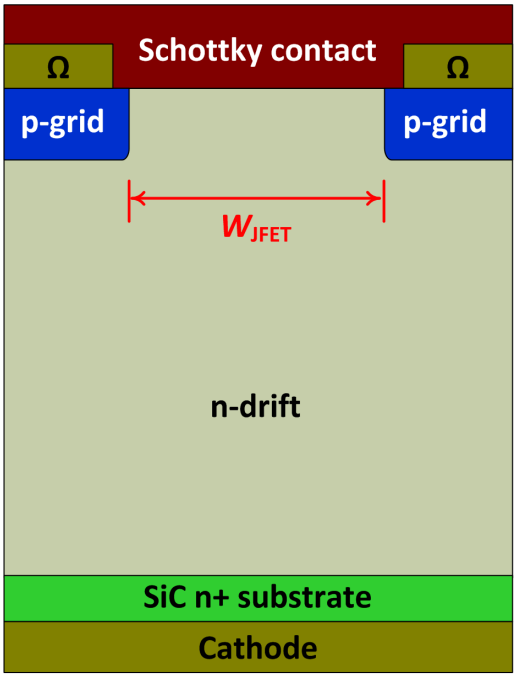


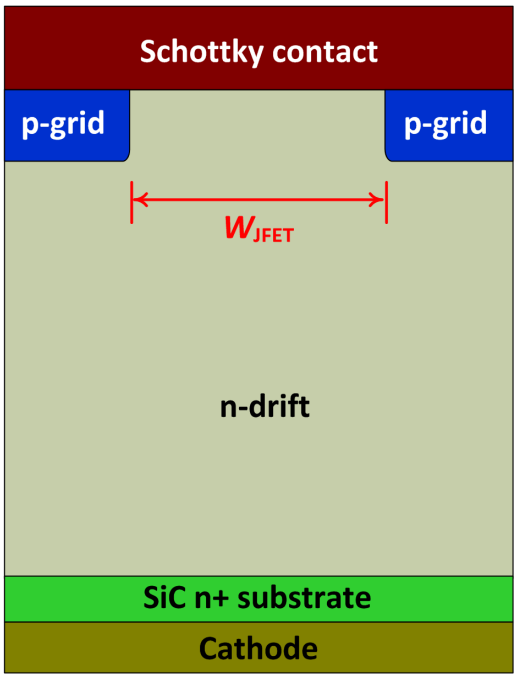
Figure 6-1 SiC Schottky diode with a Schottky electrode instead of Ohmic electrode as the Anode electrode [69].

This chapter aims to discuss the role of the contact to p-grids in power devices. In most studies, an Ohmic contact is designed to the p-grid. However, in some studies, a Schottky contact is devised. The feasibility of the two different contacts is expected to be clear. In this work, a case study with a SiC JBS is carried out with numerical simulation for a comprehensive study. It is found that the static characteristics of the SiC JBS with either the Schottky contact or Ohmic contact to the p-grids are almost the same. The switching performance of the SiC JBS with an Ohmic contact to the p-grid is same for several cycles. However, the switching performance of the SiC JBS with a Schottky contact to the p-grid is severely degraded. The dynamic on-state resistance is not stable and increases. The rectifying contact that hinders the discharging of the stored negatively charges in the p-grid is the cause for the degraded switching performance. With the stored negative charges in the p-grids, a wider depletion region is formed between the p-grids, resulting a larger forward voltage in the SiC JBS. An Ohmic contact to the p-grid is essential in terms of effectively discharging the p-grids.

6.2 Device structure of the SiC JBS with different contacts to p-grid.



(a)



(b)

Figure 6-2 Schematic structures of (a) the SiC JBS with Ohmic contacts to p-grids and (b) the SiC JBS with Schottky contacts to the p-grids.

Figure 6-2 shows the schematic cross-sectional structures of the SiC JBS with either Ohmic contacts to the p-grids or Schottky contacts to the p-grids. The Schottky contact is with a work function of 4.33 eV. The n-drift region has a thickness of 12 μm, and a doping concentration of 8×10^{15} cm^{-3}. The width of the p-grid in one cell is 2 μm (in the figures, two half p-grids are drawn at opposite sides of the schematic structure).

6.3 Device performances and analysis.

The static *I-V* characteristics of the SiC JBSs are plotted in Figure 6-3. The two *I-V* curves are coincided, so whether an Ohmic contact or a Schottky contact to the p-grid adopted in the SiC JBS does not affect the static *I-V* characteristics of the SiC JBS for low current levels. In the forward state, the current flows through the Schottky contact to the n-region. At high forward bias, the voltage bias is large enough so that the pn junction of the JBS with an Ohmic contact to the p-grid is also turned on. The device enters the bipolar mode, providing a better capability of conducting surge current (not shown). For the JBS with a Schottky contact to the p-grid, the bipolar conduction through the pn junction is suppressed by the reversely biased Schottky contact.

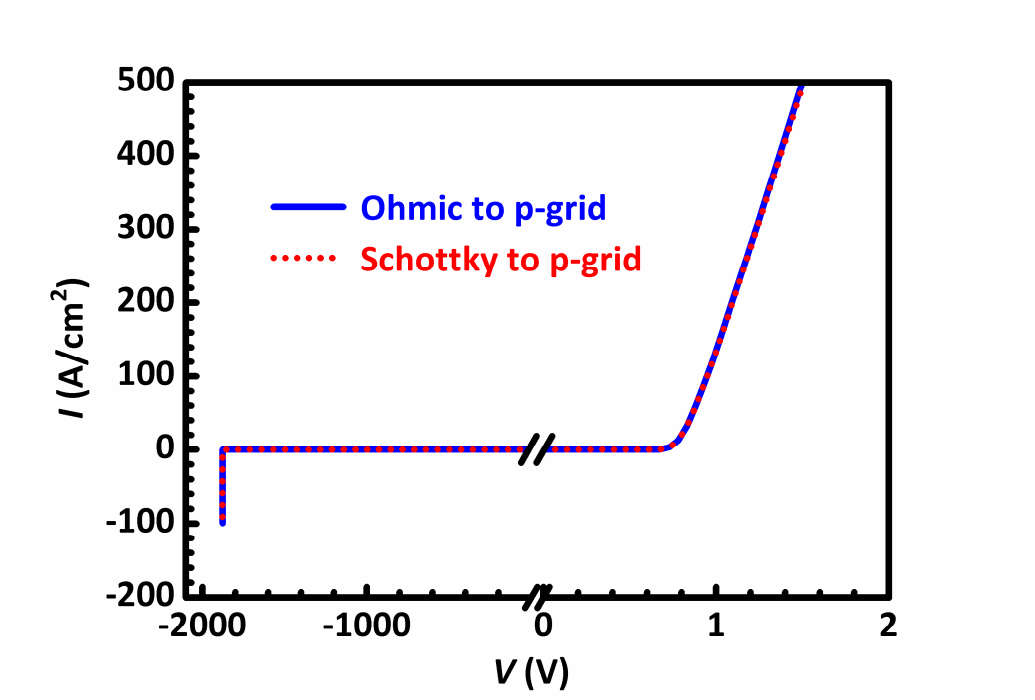


Figure 6-3 Static *I-V* characteristics of the SiC JBSs.

The reverse blocking capability of the JBS is independent of the type of contacts to the p-grid, because the anode is screened by the pn junction. With an Ohmic contact or Schottky contact to the p-grid, the pn junction is reversely biased to bear the high reverse voltage. The contours and the doping density of the p side and n side of the pn junction in the two SiC JBSs are same. The high electric field exists at around the interface of p side and n side, as shown in Figure 6-4. With the reverse voltage is larger and larger, the highest electric field is larger and larger. At about 1995 V, the electric field is large enough so that avalanche breakdown happens and the current increases fast.

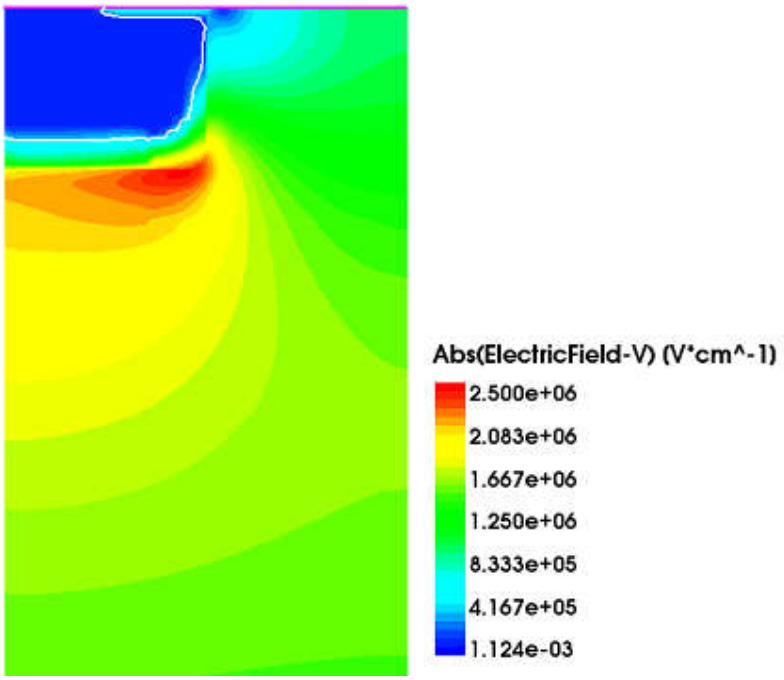


Figure 6-4 Electric field at 1200 V of the studied SiC JBS.

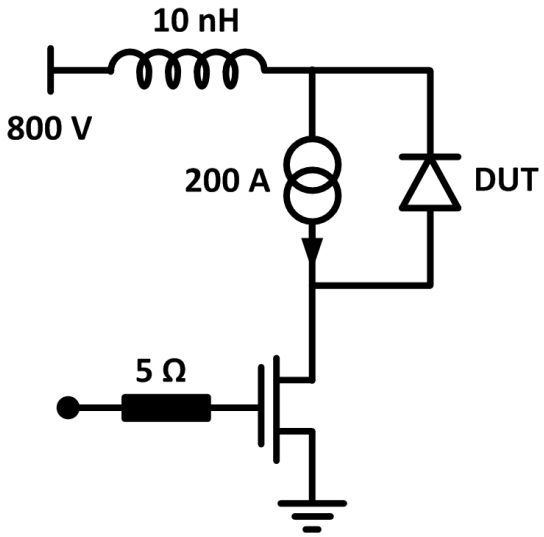


Figure 6-5 The test circuit to test the switching characteristics of the SiC JBS. A SiC MOSFET is used as the switch. The driving signal is switched between −5 V and 15 V to set the MOSFET to OFF- and ON-state, respectively.

The circuit used to test the switching characteristics of the SiC JBS is shown in Figure 6-5. When the MOSFET is in OFF state, the load current flows through the SiC JBS which is the device under test (DUT). But if the MOSFET is in ON state again, the load current will flow through the SiC JBS instead of flowing through the MOSFET. The MOSFET used in the test circuit can be Si MOSFET as well as SiC MOSFET. The requirement for the MOSFET is mainly that its *BV* should be larger than about 1200 V. The supply voltage is 800 V and the load current is 200 A supplied by a current source. A stray inductance of 10 nH is assumed in the loop. A gate resistor of 5 Ω is applied. The area of the JBS in the test is 1 cm^2. Figure 6-6 (a) and (b) show the current at the turn-off and turn-on transient of the SiC JBS respectively. Current flows through the SiC JBS before t = 0 ns and a drive signal of SiC MOSFET is switched on to 15 V at t = 0 ns. After the MOSFET is switched on at t = 0 ns, the current flowing in JBS begins to decrease and begins to flow through the MOSFET. Holes in the SiC JBS move towards the anode of the JBS while electrons move to the other way. The depletion region between the p-grid and n-drift expands to bear the 800-V supply voltage. In this turn-off process, the type of contacts to the p-grid does not affect their switching characteristics. The SiC JBS is turned on again after t = 0 ns, as shown in Figure 6-6(b), so current again flows through the SiC JBS.

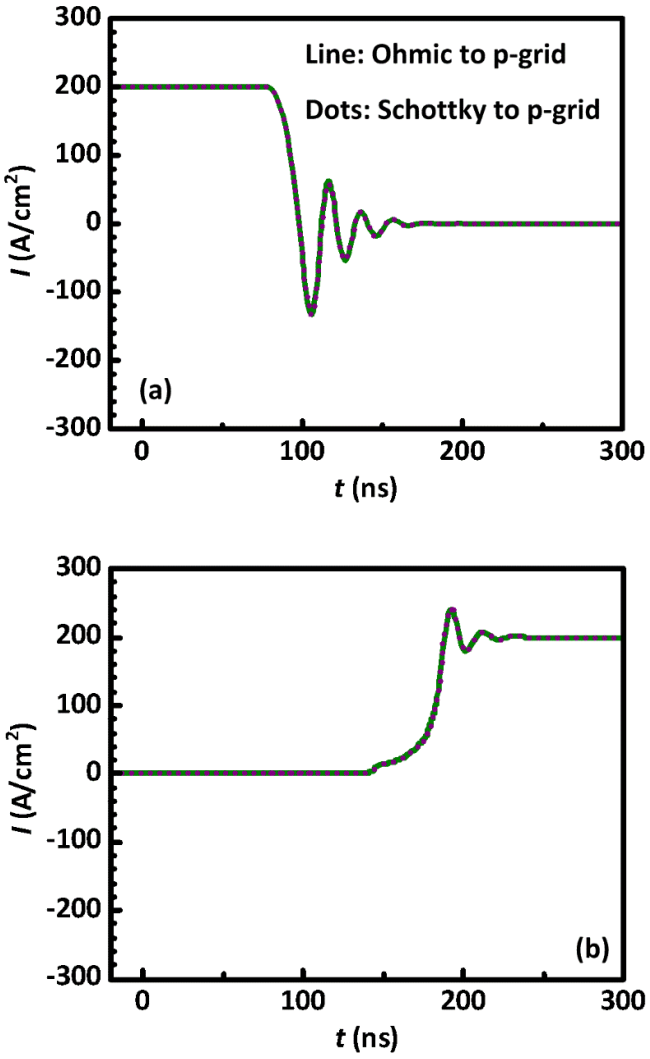


Figure 6-6 The current of JBS at (a) the turn-off transient of the SiC JBS by switching on the MOSFET, (b) the turn-on transient of the SiC JBS by switching off the MOSFET.

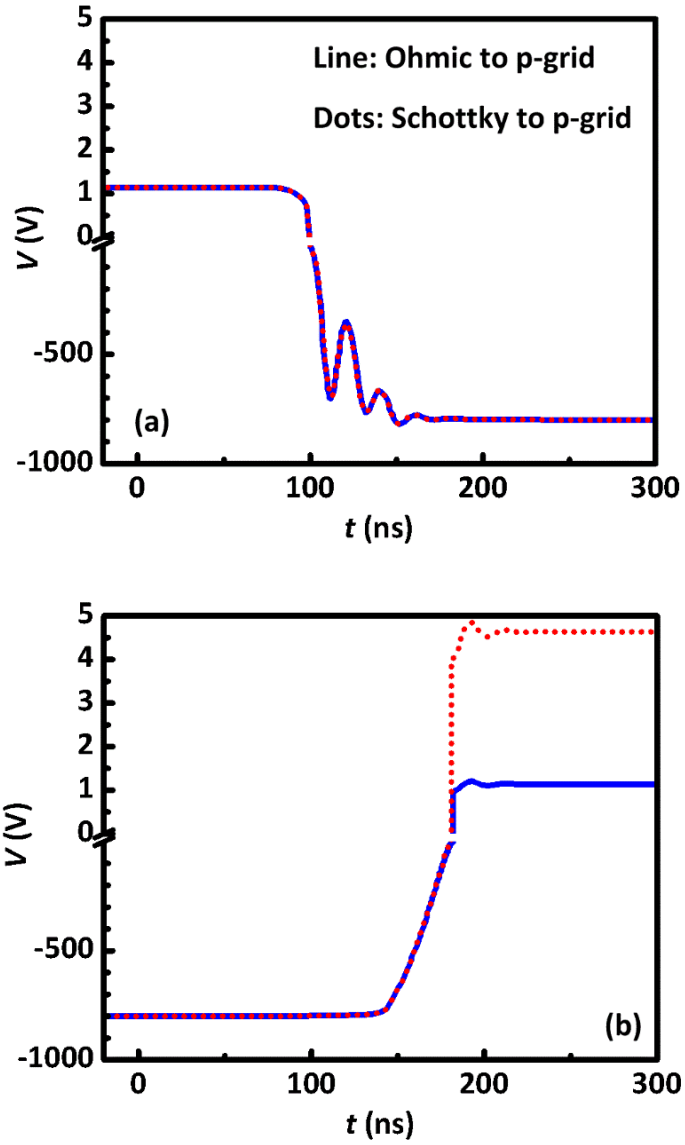


Figure 6-7 The voltage of JBS at (a) the turn-off transient of the SiC JBS by switching on the MOSFET, (b) the turn-on transient of the SiC JBS by switching off the MOSFET.

Figure 6-7 shows the voltage of the JBS at the turn-on and turn-off transients. At the turn-off transient, the voltage is the same because the pn junction bears the reverse voltage. In the OFF-state, electrons in n-drift move to the cathode, while holes in the p-grid go to the anode. So at the turn-on transient, the barrier height with Ohmic

contact is low so that holes can flow more freely and the forward voltage of the JBS with Ohmic to the p-grid contact is same to the forward voltage in the last ON-state cycle. However, the forward voltage of the JBS with the Schottky to the p-grid is much higher in order to undertake the same 200-A load current. This means a higher dynamic R_{ON} in the JBS with the Schottky to the p-grid. The reason for the higher dynamic R_{ON} is due to the fact that holes cannot flow back in the direction of the anode to the p-grid in the device with the reverse biased Schottky contact. Therefore, the p-grid is negatively charged, and the depletion region between the p-girds is larger. This narrows the current path at the ON-state, which leads to a higher dynamic R_{ON}. This can be demonstrated with the carrier distribution in Figure 6-8.

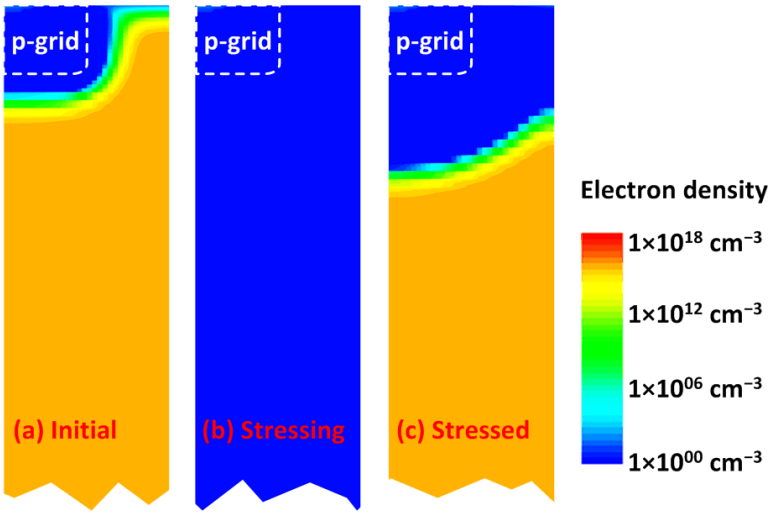


Figure 6-8 The electron distribution in the SiC JBS with a Schottky contact to the p-grid. (a) The initial state with the device zero biased. (b) The state with an 800-V reverse bias stress. (c) The state immediately following the stressing period, with the device zero biased. The time used to turn the device from the stressing state in (b) to the zero-biasing state in (c) is 1 μs.

Figure 6-8 (a), (b) and (c) show the carrier distribution in the SiC JBS with the Schottky to the p-grid contact before, in and after an 800-V reverse bias stress, respectively. After the stress, the carrier density between the p-grids is much smaller than that of the initial state. This hinders the current flowing capability.

The corresponding energy band in the simulation for these three states is shown in Figure 6-9. The energy band is along the line AA' in the inset of Figure 6-9(b) and the interface between the Schottky contact and the semiconductor is set as 0 μm. Compared to that in initial state, the voltage of p-grid increases when stressing, because an 800-V bias stress is applied between Cathode and Anode. The barrier height between p-grid and Anode is lowered, so it's easier for holes to flow from p-grid to Anode. After holes flow out, negative charges are left in p-grid. In Figure 6-9(c), even if the stress is removed, the bandgap cannot go back to initial state. This is because the holes cannot flow back into p-grid again to balance the negative charges after stressing due to the reversely biased Schottky contact. Since the electric potential of the p-grid is negative, the depletion region of p- to n-drift is longer which can be verified from the energy band in Figure 6-9(c).

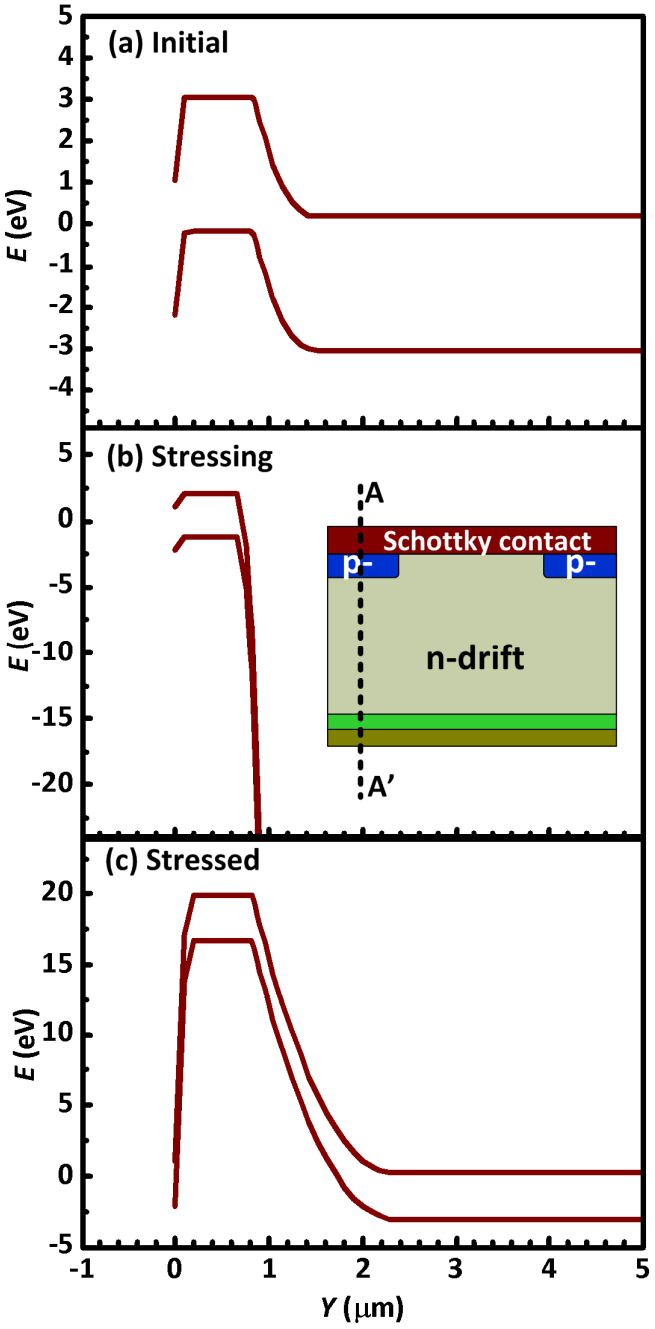


Figure 6-9 Simulated energy band along AA' in the inset in (b) under the three states of Figure 6-8 in the SiC JBS with Schottky contact to p-grid. The interface between the Schottky contact and the semiconductor is set as 0 μm.

This mechanism of the negative charge stored in the p-grid is illustrated in Figure 6-10. When the SiC JBS is turned off, holes flow from the p-grid to the anode. There is a route for the charging of the p-grid. After holes go out, negatively charged ions are induced in the p-grid. However, because the Schottky contact works as a rectifier diode, the holes can go from the direction of p-grid to the anode but cannot go from the other direction of anode to p-grid. The discharging route is blocked when the device is turned on again. Therefore, negatively charged ions are kept in the p-grid, and the negatively charged p-grid influences the *I-V* characteristics of the device, as can be seen in Figure 6-11.

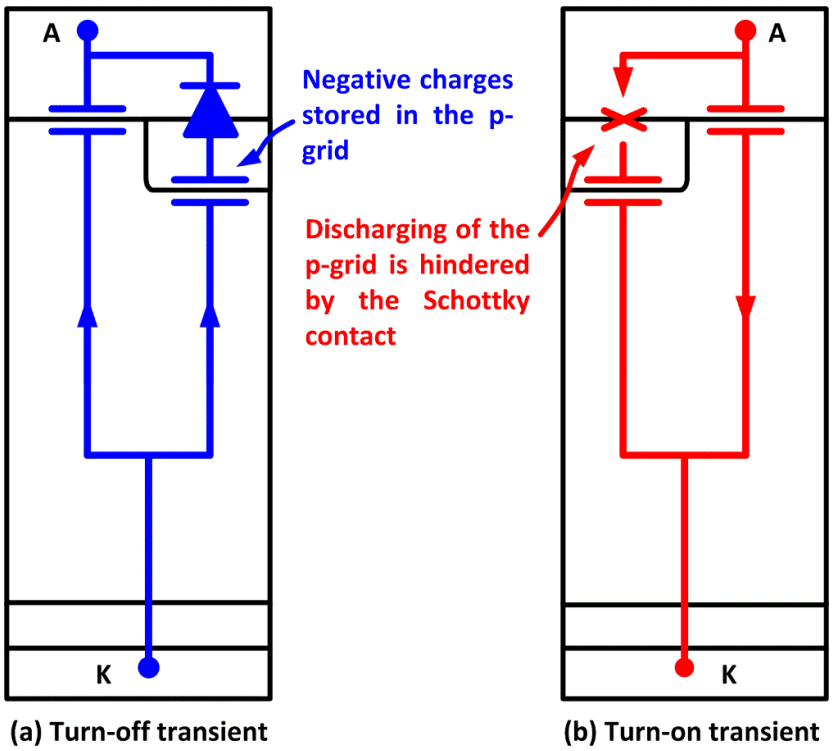


Figure 6-10 Illustration of the charge storing mechanism of the SiC JBS with Schottky contact to p-grid.

With the Ohmic contact to p-grid in the SiC JBS, the charging and discharging of the p-grid can be finished normally. The stressing process does not have an impact on the JBS's characteristics. As can be seen in Figure 6-11(a), the *I-V* characteristics in Fresh and after stress are nearly same, which corresponds with that in Figure 6-6. However, in Figure 6-11(b), the forward voltage of the SiC JBS with a Schottky contact to the p-grid is larger in the Stressed than that in the Fresh because of the stored negative charges in the p-grid.

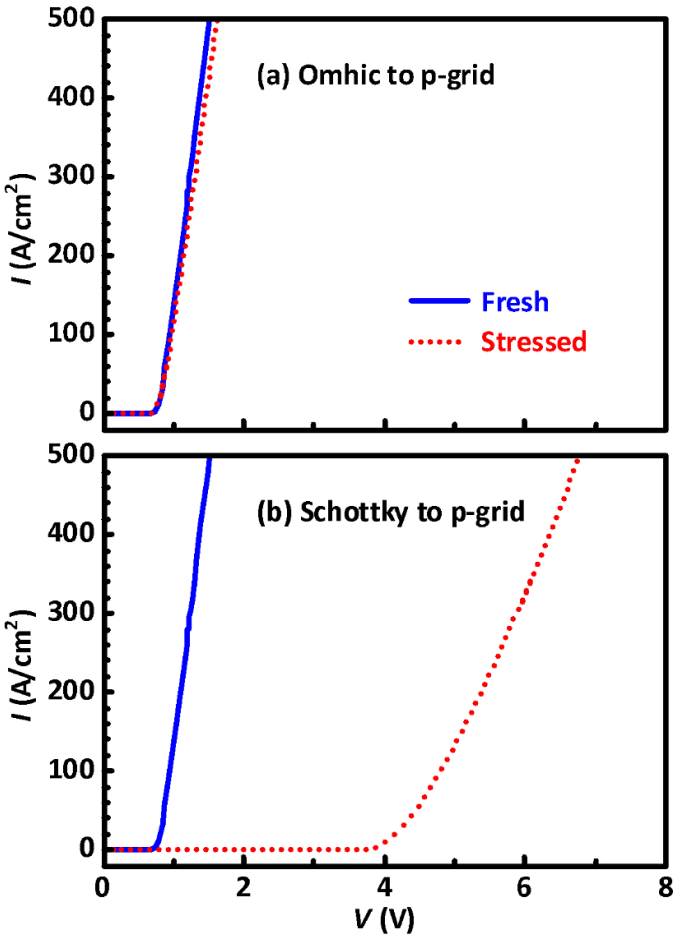


Figure 6-11 The static *I-V* characteristics of (a) the SiC JBS with an Ohmic contact to the p-grid, and (b) that with a Schottky contact to the p-grid.

The forward voltage drop (V_F) difference between the Fresh and the Stressed in SiC JBS with Schottky contact to the p-grid has relationship with the distance between p-grids (W_{JFET}). It can be seen in Figure 6-12, when W_{JFET} is larger, the difference is smaller. This is because the depletion region between neighboring negatively charged p-grid after stress only occupies a smaller part of W_{JFET}. But a larger W_{JFET} sacrifices a higher electric filed in the Schottky contact above n-drift at OFF-state. W_{JFET} is a critical parameter for the performance of JBS. P-grids shield the Schottky contact above n-drift by terminating most of electric field lines from Cathode which would otherwise terminate at Schottky contact and increase Schottky junction field. The trade-off between Schottky junction field E_J (at the middle of Schottky contact between p-grids) and forward voltage drop V_F in SiC JBS with Schottky contact to p-grid is shown in Figure 6-12. Thus increasing the W_{JFET} cannot eliminate the difference between V_F of Fresh and Stressed under the condition of a smaller E_J in SiC JBS with a Schottky contact to p-grid. An Ohmic contact to the p-grid is required in SiC JBS.

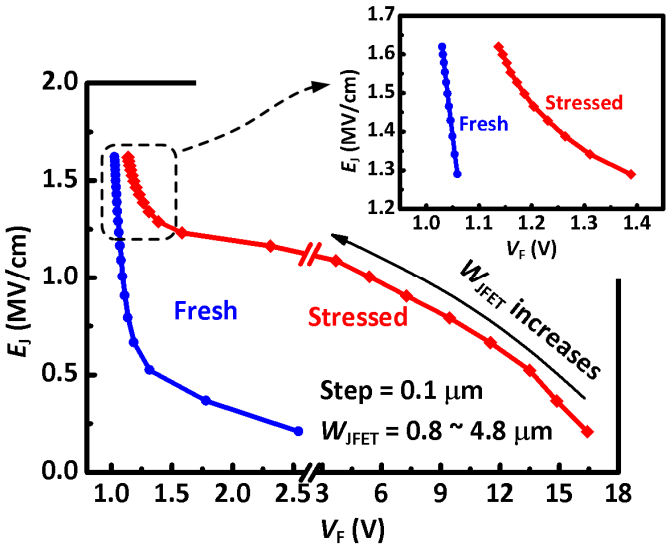


Figure 6-12 The trade-off between junction field E_J and the forward voltage V_F. The distance between p-grids W_{JFET} is varied.

6.4 Summary

This work reveals the significance of the electrical contact type to the p-grid in the SiC JBS. The selection of a Schottky contact and an Ohmic contact does not have influences on the static characteristics of the JBS. However, in the dynamic process, the *I-V* characteristics of the JBS with a Schottky contact to the p-grids after a reversely biased stress is different from that before the stress. This is caused by the stored charge mechanism. Holes can go across the Schottky contact to p-grid at OFF-state, but cannot go back because of the rectifying characteristics of Schottky contact. The rectifying Schottky contact supports the charging of the p-grids but hinders the discharging of the p-grids, leading to negative charges being left in the p-grids. A larger W_{JFET} can help to narrow the difference of the forward voltage difference between Fresh and Stressed, but will cause the sacrifice of the junction electric field. Therefore, for switching performance consideration, an Ohmic contact to the p-grids in SiC JBS as well as other SiC power devices should be adopted.

CHAPTER 7 Conclusions and Suggestions for Future Work

7.1 Overall conclusions

In conclusion, with the requirement for an efficient power system, SiC, as a wide bandgap semiconductor, has received a large attention. SiC allows devices to work at higher voltage ratings and higher temperatures than Si based devices. With a Si-face in SiC, this compound semiconductor also achieves the advantage of gate oxide growth. However, several critical problems are waiting for solutions. Therefore, in this thesis, a SiC based power trench MOSFET and a Schottky contact to the p-grids are studied for power switching applications.

Firstly, the SiC trench MOSFET with a self-biased p-shield region (SBS-MOS) is proposed. The SBS-MOS utilizes a self-biased p-shield under the gate trench to screen the high drain voltage and thus reduces the oxide field to a safe level. A self-biasing network is utilized to drive the p-shield to a positive voltage, so that the JFET resistance between adjacent p-shields is reduced, and further down-scaling of the cell size is allowed. The influences of the self-biasing network upon the gate charges are comprehensively studied. Although additional charges are required to drive the self-biasing network, the amount of additional charges can be minimized with proper design. The optimized SBS-MOS exhibits a low R_{ON}, a low oxide field and a low Q_{GD} simultaneously. The figure of merit $Q_{GD} \cdot R_{ON}$ of the SBS-MOS is better than that of the C-MOS and GS-MOS. Therefore, the proposed SiC SBS-MOS is a promising candidate for power switching.

Secondly, a trench MOSFET structure with protruded p-bodies (PB-MOS) is proposed to address the challenges in SiC trench MOSFETs. No additional

components are required for this solution. Compared to the conventional MOSFET (C-MOS), the PB-MOS achieves a dramatically lower OFF-state oxide field, owing to the shielding effect provided by the protruded p-bodies. The SiC trench MOSFET with a p-shield under the trench gate to screen the high electric field at the OFF-state needs extra contact vias for the p-shield. The protruded p-bodies are connected to the Source electrode, so no extra contact area is required, especially for the p-bodies. This helps to decrease the cost remarkably. The protruded p-bodies also help to reduce C_{rss}, which further leads to a reduction in the gate charges. The switching characteristics are also presented, with the PB-MOS exhibiting a much lower switching energy loss during both turn-on and the turn-off transients. A low R_{ON} and a high BV are maintained in the proposed PB-MOS. Much better figures of merit $Q_G \cdot R_{ON}$ and $Q_{GD} \cdot R_{ON}$ are obtained with the proposed PB-MOS. A feasible process flow for PB-MOS is also proposed, which is based on the process flow of the conventional trench MOSFET. Therefore, the PB-MOS is a promising approach for utilizing SiC in the next generation of power conversion systems.

Thirdly, a case study is conducted for the SiC junction barrier Schottky (JBS). The focus of the study is to investigate the influence of contact on the p-grid, i. e. Schottky contact or Ohmic contact to p-grid, since several studies have proposed to use a rectifying Schottky contact connected to the p-grid. It is found that the SiC JBS with a Schottky contact to the p-grid and that with an Ohmic contact to the p-grid exhibit similar static characteristics, but their switching performances are different. With a Schottky contact to the p-grid, the JBS suffers from an increase of the dynamic V_F. The finding is explained by the charge storage effect. The p-grid in the JBS is charged with negative charges in the reverse biased state. When the device is switched to the forward stage, the rectifying Schottky contact to the p-gird hinders the

discharging of the stored negative charges in the p-grid. With the stored negative charges in the p-grid, a wider depletion region is formed between the p-grids, resulting in a larger forward voltage in the SiC JBS. Therefore, an Ohmic contact to the p-grid is essential in terms of effectively discharging the p-grids.

7.2 Suggestions for future work

(1) The physical mechanism of the proposed SiC power devices is deeply analyzed in both static and dynamic parts in this thesis.

To verify the illustrated advantage of SBS-MOS and PB-MOS, the demonstration of them is suggested for future work. Since the demonstration of SiC MOSFET is very complicated and advanced micro-fabrication equipments are demanded, the cooperation with factories is preferred. Some basic processes for conventional SiC trench MOSFET might be referred, while the pressure, temperature, energy, processing time, etc. of some specific processes (for example, the dummy gate deposition and etching in the PBMOS process flow) have to be designed after a series of dummy processes. In the SBS-MOS, the integrated diodes in SBS-MOS can be fabricated in a same chip or packaged together with the SBS-MOS. While in the PB-MOS, since a deeper p-region is needed in PB-MOS than traditional ones, the implantation energy is pretty large. The details in the following annealing process have to be found to achieve a better crystal state.

(2) There are several diodes proposed in the self-driving network of the SBS-MOS. The diodes can be designed in one chip with the main MOSFET part, and also can be integrated with the main MOSFET part by packaging. Thus, that whether these two different methods will have different influences on the characteristics is necessary

to be studied in future work. If the diodes are designed in one chip, the parasitic effect of the wires which exists in the package method may be avoided. Besides, the parasitic capacitance effect of the neighboring devices in the package method is also a consideration.

APPENDIX

The fabrication process of conventional MOSFET.

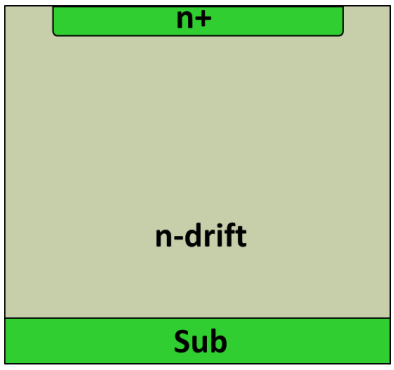
(a) After n-drift layer is grown on the n+ substrate, a heavy N-type doped region is performed on a patterned SiC surface.

(b) A p-body region is implanted on the topside.

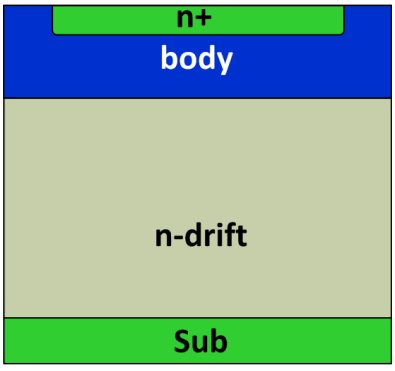
(c) After the formation of the p-body, a gate trench is formed by etching.

(d) After cleaning of the surface, the gate dielectric is deposited or oxidized. Then polysilicon part is etched in the gate dielectric and polysilicon is deposited. To isolate the gate electrode and source electrode, an insulating layer is deposited as isolation.

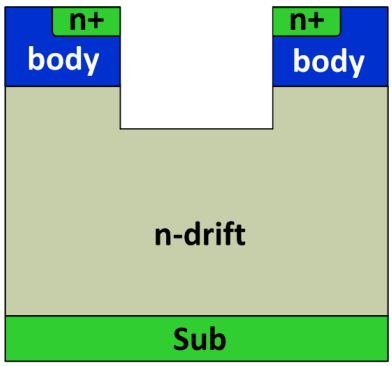
(e) Source electrode metal is deposited.



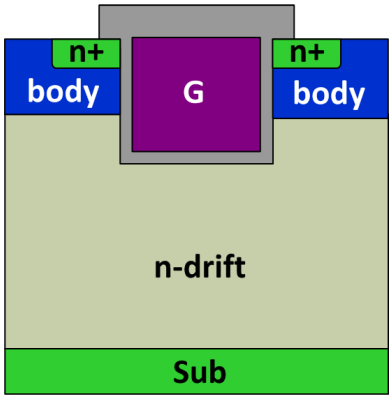
(a) n+ implantation



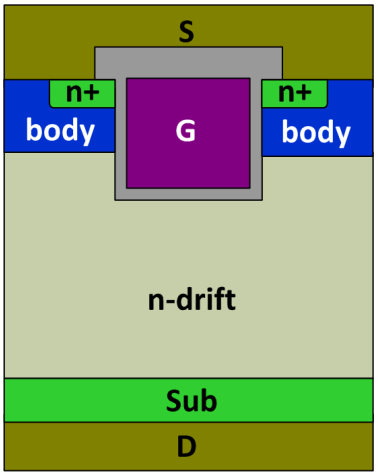
(b) pbody implantation



(c) gate trench removal



(d) gate deposition



(e) contact formation

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