TOPOLOGIES AND CONTROL OF SINGLE-STAGE AC-DC WIRELESS-POWER-TRANSFER RESONANT CONVERTERS WITH POWER-FACTOR-CORRECTION

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Topologies and Control of Single-Stage AC-DC Wireless-Power-Transfer Resonant Converters with Power-Factor-Correction

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CERTIFICATE OF ORIGINALITY

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_____LIU Junwei_____(Name of Student)

Abstract

High power wireless power transfer (WPT) technologies have drawn much attention in industrial and academic areas in recent years due to their obvious advantages: convenience and safety (avoidance of electric shock). For applications of high power WPT, such as wireless electric vehicle (EV) charging, power is usually drawn from the power grid and a separate power factor correction (PFC) stage is typically needed to ensure the power quality of the grid. Therefore, a two-stage topology with an AC-DC converter with PFC stage and a DC-DC WPT converter stage is often adopted. Generally, such two-stage topology cannot achieve the highest efficiency because of more power losses in the two-stage conversion while it is also not the most economical as more components are required. Also its control is more complicated because two separate controllers for two stages are required.

Recently there has been a lot of research on single-stage AC-DC converters with PFC aimed to reduce power losses, power switch counts, and control complexity. Much of existing research focuses mainly on applying single-stage topologies in transformer-based-isolated converter. There are very few studies on applying single-stage topologies in WPT systems, and it is therefore the aim of this thesis to explore and develop the topologies and control methods of AC-DC WPT resonant converters with single-stage PFC topologies.

A new single-phase single-stage AC-DC WPT converter with PFC is proposed, which utilizes the lowest count of power semiconductor devices (6 diodes and 4 switches), compared with conventional two-stage AC-DC WPT converters (9 diodes and 5 switches) and other existing AC-DC WPT converters. Due to the reduced count of power semiconductor devices, the power loss is significantly reduced and a remarkably high efficiency of 90.1% was measured in experiments

with power factor and input current THD achieved 0.99 and 15.4%, respectively. A new control method for the topology is also proposed to further improve the power quality, reduce bus voltage, and extend load range of operation. Though it is slightly more complicated due to the introduction of two control parameters, the proposed control method can largely improve the power quality with the measured input current THD below 1% and power factor over 0.99. Furthermore, the bus voltage is largely reduced and controlled to 500V as compared to the original of 723.5V so as to significantly alleviate the voltage stresses of all the power switches and bus capacitor.

A new three-phase single-stage AC-DC WPT converter with PFC is proposed, which also has the lowest count of power semiconductor devices (10 diodes and 4 switches) and reduced power loss compared with other existing three-phase AC-DC WPT converters with PFC. It achieved the maximum efficiency of 91.7% in experiments. Compared to the proposed single-phase topology, this three-phase topology possesses additional advantages of better power quality with power factor and input current THD reached 1.0 and 3.5%, respectively, due to the elimination of the zero-sequence components in input current; and higher power capacity due to the inherent superiority of three-phase power source.

As the backend of single-stage AC-DC WPT converters, DC-DC WPT converters are also studied, and a new parameter estimation algorithm requiring only primary-side information under unknown varying misalignment and load conditions, is newly proposed. The proposed algorithm mainly utilizes both the existing fundamental and higher-order harmonics (third-order) in the WPT resonant converter. In experiments, the measured errors of estimations are below 3% and better than other existing methods (maximum errors larger than 8.3%). Such algorithm could be applied in primary-side feedback and control system of DC-DC or AC-DC WPT resonant converters without any additional wireless communication device or secondary-side measurement units and controller, so as to greatly simplify the hardware and reduce the total cost.

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List of Abbreviations

WPT	Wireless-power-transfer
EV	Electric vehicle
RF	Radio frequency
MRC	Magnetic resonant coupling
SS	Series-series
SP	Series-parallel
PS	Parallel-series
PP	Parallel-parallel
PFC	Power-factor-correction
SMPS	Switched mode power supply
DCM	Discontinuous current mode
ADCM	Average discontinuous current mode control
ZVS	Zero voltage switching
EDF	Extended describing function
FHA	Fundamental harmonic approximation
ADCM	Average discontinuous current mode
KVL	Kirchhoff voltage law
PF	Power factor
THD	Total harmonic distortion
RMS	Root-mean-square
EMI	Electro-magnetic interference
ESR	Equivalent series resistance
SAE	Society of Automotive Engineers
DSP	Digital signal process
AD	Analogue-to-digital
PWM	Pulse width modulation
V2G	Vehicle-to-grid power delivery

G2V	Grid-to-vehicle power delivery
DAB	Dual active bridge
ABS	Absolute value
DIV	Divider
SUB	Subtractor
MUL	Multiplier
SQRT	Square root value
SAT	Saturation
COMP	Comparator
SIN	Sine function
ASIN	Arcsine function

List of Symbols

$\alpha, \beta, \theta, \delta$	Phase angles of fundamental components of v_{AB}, v_{CD}, i_r, and i_{rs}
$\alpha_1 - \alpha_4$	Phase angles defined in Fig. VI-1 and (6.1)
θ_{cd}	Phase angle defined in Fig. VI-1
$\theta_{Vd.n}$	n-order component's phase delay of v_{AB}'s sampled signal
$\theta_{Id.n}$	n-order component's phase delay of i_r's sampled signal
φ_a	Initial phase angle of v_a
φ_b	Initial phase angle of v_b
φ_c	Initial phase angle of v_c
φ	Phase difference of fundamental components of v_{AB} and i_r
η	System efficiency
η_{ss}	Efficiency of SS resonant tank
η_{sp}	Efficiency of SP resonant tank
ρ	Resistivity of copper
μ	Permeability of copper
C_{bus}	Bus capacitor
C_{b1}	Upper bus capacitor
C_{b2}	Under bus capacitor
C_f	Output filtering capacitor of secondary-side circuit
C_{if}	Capacitor (capacitance) of input filter
$C_{s1} - C_{s4}$	Snubber capacitors of switches $Q_1 - Q_4$
C_1	Capacitor (capacitance) of primary side
C_2	Capacitor (capacitance) of secondary side
c	Thickness of primary-side and secondary-side coils
c_w	Diameter of litz wire
D_a	Duty cycle defined in Fig. IV-1 and Fig. IV-2
D_{ab}	Duty cycle of v_{AB} (ratio of non-zero voltage in a switching period T_s)

$D_{ab.100\%}$	D_{ab} value at 100% load condition
$D_{ab.20\%}$	D_{ab} value at 20% load condition
D_b	Duty cycle defined in Fig. IV-1 and Fig. IV-2
D_g	Duty cycle of the switch in the boost PFC converter/rectifier ot duty cycle defined in Fig. IV-1 and Fig. IV-2
D_g’	Duty cycle considering dead time of the switch in the boost PFC converter/rectifier
$D_{g.\min}$	Maximum value of D_g
$D_{g.\max}$	Minimum value of D_g
D_{g1}	Duty cycle of switch Q_1
D_{g2}	Duty cycle of switch Q_2
D_h	Duty cycle defined in Fig. IV-1 and Fig. IV-2
D_{R1}, D_{R2}	Diodes of front-end bridgeless rectifier
$D_{r1} – D_{r6}$	Diodes of three front-end diode-legs of proposed three-phase single-stage AC-DC WPT resonant converter with PFC
$D_{s1} – D_{s4}$	Diodes of secondary-side high-frequency full-bridge rectifier
D_0	Output diode of boost PFC converter
$D_1 – D_4$	Body diodes of switches $Q_1 – Q_4$
d	Average diameter of primary-side and secondary-side coils
d_{aq}	Distance between primary-side and secondary-side coils
d_m	Horizontal misalignment distance of resonant coils
d_{sk}	Skin depth of skin effect
d_{st}	Diameter of each strand of litz wire
F_f	Transfer function of input filter
f_s (ω_s)	Operation/switching frequency (in radian)
$f_{s.\min}$	Minimum operation frequency f_s
f_l (ω_l)	Line frequency (in radian) of AC input voltage
f_1 (ω_1)	Lower resonant frequency (in radian) of SS resonant tank
f_2 (ω_2)	Higher resonant frequency (in radian) of SS resonant tank

f_3 (ω_3)	Middle resonant frequency (in radian) of SS resonant tank
$I_{m.ns}$	Fourier series coefficient of i_r's sampled signal (n-order sinusoidal component)
$I_{m.nc}$	Fourier series coefficient of i_r's sampled signal (n-order cosine component)
I_n	Matrix defined in (6.19)
$I_{o.\max}$	Maximum output current
I_{rp}	Peak value of fundamental component of i_r
I_{rsp}	Peak value of fundamental component of i_{rs}
$I_{r.ns}$	Sinusoidal component of $i_{r.n}$
$I_{r.nc}$	Cosine component of $i_{r.n}$
$I_{rs.ns}$	Sinusoidal component of $i_{rs.n}$
$I_{rs.nc}$	Cosine component of $i_{rs.n}$
i_a, i_b, i_c	Three-phase input currents
i_{abc}	Sum of $i_{in.a}$, $i_{in.b}$, and $i_{in.c}$
$i_{\text{avg}.x}$	Average value of $i_{in.x}$ within a switching period T_s
i_{bus}	Current flowing through C_{bus}
$i_{D1} - i_{D4}$	Currents flowing through diodes $D_1 - D_4$
i_{in}	Currents flowing through L_{in} (input inductor current)
$i_{in.\text{avg}}$	Average value of i_{in} during a switching period T_s
$i_{in.a}$, $i_{in.b}$, $i_{in.c}$	Currents flowing through $L_{in.a}$, $L_{in.b}$, and $L_{in.c}$ respectively
$i_{in.\text{rms}}$	RMS value of i_{in} within a line period T_l
$i_{in.x}$	$i_{in.a}$, $i_{in.b}$, or $i_{in.c}$
$i_{Q1} - i_{Q4}$	Currents flowing through switches $Q_1 - Q_4$
i_r	Current flowing through primary-side coil
i_{rs}	Current flowing through secondary-side coil
$i_{r.n}$	n-order harmonic of i_r
$i_{rs.n}$	n-order harmonic of i_{rs}
i_1	Total currents of Q_1, D_1, and C_{s1}

i_2	Total currents of Q_2, D_2, and C_{s2}
i_3	Total currents of Q_3, D_3, and C_{s3}
i_4	Total currents of Q_4, D_4, and C_{s4}
k_I	Control parameter defined as (4.9)
$k_{I.\max}$	Maximum value of k_I
k_{II}	Control parameter defined as (4.18)
$k_{Im.n}$	n-order component's amplitude attenuation factor of i_r's sampled signal
k_{iv}	Ratio of $i_{in.\text{avg}}$ and v_s
k_L	Self-inductance coefficient
k_{ps}	Coupling coefficient of primary-side and secondary coils
$k_{Vm.n}$	n-order component's amplitude attenuation factor of v_{AB}'s sampled signal
L_{if}	Inductor (inductance) of input filter
L_{in}	Input inductor of boost PFC converter
$L_{in.a}$, $L_{in.b}$, $L_{in.c}$	Input inductor (inductance) of proposed three-phase single-stage AC-DC WPT resonant converter with PFC
L_m	Magnetic inductance of equivalent transformer of coupled coils
L_p	Inductor (inductance) of primary-side coil
L_s	Inductor (inductance) of secondary-side coil
L_t	Sampling inductor (inductance)
L_1	Primary leakage inductor (inductance) of equivalent transformer of coupled coils
L_2	Secondary leakage inductor (inductance) of equivalent transformer of coupled coils
M	Mutual inductance of primary-side and secondary-side coils
M_e	Mutual-inductance coefficient
m	Ratio of V_{sp} and V_{bus}

N	Number of primary-side and secondary-side coils
n_e	Ratio of equivalent transformer of coupled coils
n	Harmonic's order
$P_{e.ss}$	Transferred power of SS resonant tank
$P_{e.sp}$	Transferred power of SP resonant tank
$P_{f.loss}$	Loss of input filter
PF	Power factor
PF_{dp}	Displacement power factor
PF_{dt}	Distortion power factor
P_{in}	Average input power in a line period T_l
$P_{in.\max}$	Maximum input power
P_o	Output power
$P_{o.\max}$	Maximum output power
P_T	Average input power in a switching period T_s
Q_0	Power switch of boost PFC converter
$Q_1 - Q_4$	Switches of primary-side high-frequency full-bridge (or T-type) inverter
R	Load resistance
R_{c1}	ESR of C_1
R_{c2}	ESR of C_2
R_e	Equivalent load resistance
R_i	Input resistance of proposed three-phase single-stage AC-DC WPT resonant converter with PFC
$R_{i.\min}$	Minimum value of R_i
R_{in}	Input resistance of proposed single-phase single-stage AC-DC WPT resonant converter with PFC
$R_{in.\min}$	Minimum value of R_{in}
$R_{in.\max}$	Maximum value of R_{in}
R_{lf}	ESR of L_{if}

R_{lp}	ESR of L_p
R_{ls}	ESR of L_s
$R_{\min}$	Minimum load resistance
R_{on}	On resistance of switches $Q_1 - Q_4$
R_p	Sum of $2R_{on}$, R_{lp}, and R_{c1}, ESR of primary-side circuit
R_s	Sum of R_{ls} and R_{c2}, ESR of secondary-side circuit
s_w	Effective cross section area of liz wire
$\mathrm{THD_i}$	THD of input current (average value in a switching period)
T_l	Line period of AC input voltage
T_s	Operation/switching period
$V_{AB.ns}$	Sinusoidal component of $v_{AB.n}$
$V_{AB.nc}$	Cosine component of $v_{AB.n}$
$V_{AB.1.\mathrm{pk}}$	Peak value of v_{AB}'s fundamental component
V_{bus}	Voltage of bus capacitor (Bus voltage)
$V_{bus.\max}$	Maximum value of V_{bus}
$V_{bus.100\%}$	V_{bus} value at 100% load condition
$V_{bus.20\%}$	V_{bus} value at 20% load condition
V_b	Voltage of C_{b1} and C_{b2} (when V_{b1} is equal to V_{b2})
V_{b1}	Voltage of C_{b1}
V_{b2}	Voltage of C_{b2}
$V_{CD.ns}$	Sinusoidal component of $v_{CD.n}$
$V_{CD.nc}$	Cosine component of $v_{CD.n}$
$V_{c1.ns}$	Sinusoidal component of $v_{c1.n}$
$V_{c1.nc}$	Cosine component of $v_{c1.n}$
$V_{c2.ns}$	Sinusoidal component of $v_{c2.n}$
$V_{c2.nc}$	Cosine component of $v_{c2.n}$
V_d	Forward voltage of diodes of secondary-side high-frequency full-bridge rectifier
V_{ep}	Peak value of v_e

V_{in}	Input voltage of DC-DC WPT resonant converter
V_{ip}	Peak value of v_i
$V_{Lt.ns}$	n-order sinusoidal component of L_t's voltage
$V_{Lt.nc}$	n-order cosine component of L_t's voltage
$V_{m.ns}$	Fourier series coefficient of v_{AB}'s sampled signal (n-order sinusoidal component)
$V_{m.nc}$	Fourier series coefficient of v_{AB}'s sampled signal (n-order cosine component)
V_n	Matrix defined in (6.19)
V_o	Output voltage of AC-DC or DC-DC WPT resonant converter
v_a, v_b, v_c	Three-phase input voltages
v_{a1}, v_{b1}, v_{c1}	Equivalent three-phase input voltages after input filter
v_{AB}	Output voltage of primary-side high-frequency full-bridge (or T-type) inverter
$v_{AB.1}$	Fundamental component of v_{AB}
$v_{AB.n}$	n-order harmonic of v_{AB}
v_{CD}	Input voltage of secondary-side high-frequency full-bridge rectifier
$v_{CD.1}$	Fundamental component of v_{CD}
$v_{CD.n}$	n-order harmonic of v_{CD}
v_{c1}	Voltage across C_1
v_{c2}	Voltage across C_2
$v_{c1.n}$	n-order harmonic of v_{c1}
$v_{c2.n}$	n-order harmonic of v_{c2}
v_e	Output voltage of secondary-side resonant tank
$v_{q1} - v_{q4}$	Driving voltage of switches $Q_1 - Q_4$
v_i	Input voltage of primary-side resonant tank
$v_{Q1} - v_{Q4}$	Voltages across switches $Q_1 - Q_4$
v_s	Single-phase AC input voltage

v_x	v_a, v_b, or v_c
v_{x1}	v_{a1}, v_{b1}, or v_{c1}
Z_{An}	Matrix defined in (6.20)
Z_{Bn}	Inverse matrix of Z_{An}
Z_{ic}	Input impedance of proposed single-phase single-stage AC-DC WPT resonant converter with PFC
Z_{mn}	Value defined in (6.21)
Z_{of}	Output impedance of input filter
Z_{pn}	Value defined in (6.21)
Z_r	Equivalent impedance of secondary-side circuit (at fundamental frequency)
$Z_{r.ss}$	Input impedance of SS resonant tank
$Z_{r.sp}$	Input impedance of SP resonant tank
Z_{sn}	Value defined in (6.21)

Chapter I
Introduction

I.1 Background and Incentives of Research

I.1.1 Wireless power transfer

Nowadays electric power is more and more essential because most human's activities and comfort rely on it, such as lighting, air-conditioning, heating, electric vehicle charging, and so on. Traditionally electric power is transferred and utilized with power cables. It has to be admitted that transmission of electric power in such a way exhibits dominant advantages: high-efficient, stable, directed, long-distant, and so on. However, in recent years, transferring electric power in a wireless way, also known as wireless power transfer (WPT), is taking up more and more roles in people's daily life and industrial cycles due to its unique advantages that traditional wired way does not possess: convenience and safety (avoidance of electric shock). Although transmission efficiency and reliability of WPT still cannot exceed those in wired way, they are high enough and acceptable. In addition, such technology is still in a highway of development, meaning that it still has large space of improvements in many aspects. WPT technology has a variety of applications with power levels ranged from several milliwatts to tens of kilowatts, including charging portable telephone [1], supplying power for biomedical implants or instruments [2] – [6], electric vehicle (EV) battery charging [7], [8], roadway powering moving EVs [9] – [14] and moving train [15], and undersea application [16]. For biomedical applications, such as charging or powering artificial organs inside the body, WPT technology exhibits its huge advantages compared to traditional wired way (surgery needed). For EV charging and moving EV powering, traditional wired way is limited by location, weather,

and safety issues (unexpected electric shocks). However, those problems and limitations can be resolved by applying WPT technology. Moreover, it is much more convenient than the traditional wired way for EV charging. When an EV is parked, the driver does not have to operate the charging station and manually connect the power cable to the charging socket. Instead, he/she can just leave and the wireless EV charging system would automatically start charging the EV. In general, WPT technology is more and more popular and will be applied in a wide range of home living and industrial communities in the future.

WPT technologies can be categorized in terms of their power-transfer mechanisms and principles. Firstly, inductive coupling method [1], [2], [8] – [10], [17] – [22], as a traditional and the most common WPT technology, has been researched for a long time and is a very efficient way to deliver power wirelessly within a short distance in millimeters. However, power and efficiency drop severely if transfer distance extends or there is a misalignment between transmitter and receiver. Such inductive technology has many limitations, such as inability to power and charge moving EVs. Secondly, for far-field or long-distant WPT, propagating electromagnetic waves (the same way radios transmit signals) or RF broadcast method are used to transfer energy. Such far-field WPT methods allow for transferring power to any directions in the coverage area. However, low efficiency and low power capacity are the disadvantages which limit the development. Thirdly, capacitive WPT technology, which utilizes electric filed coupling to transfer power wirelessly, has been studies and explored in recent years [23] – [33]. Generally, capacitive WPT technology is more suitable for small gap distance application, compared with inductive WPT technology [34]. Combined inductive and capacitive WPT technology [35], [36], which takes advantages of both magnetic and electric field couplings simultaneously, have also drawn some interest recently. Lastly, there is an efficient WPT technology for mid-range transfer, magnetic resonant coupling (MRC) approach [37] – [43], proposed and demonstrated by MIT in 2007 [44], attracts much interest from

researchers in recent years, due to its high efficiency and relatively longer transfer distance. This approach utilizes resonance characteristic of coupled primary and secondary resonant tanks under a specific frequency to achieve WPT efficiently. In this thesis, the discussions are based on MRC WPT technology.

State-of-the-art studies and researches on the MRC WPT technology cover many different aspects from theoretical analysis to practical applications. Firstly, modeling and theoretical analysis of varies WPT systems are studied in [45] – [49]. In addition, control methods [50] – [54], circuit topologies [54] – [57], efficiency analysis and improvement [58], optimal design methods [59], [60], and maximum efficiency point tracking [16], [53] of WPT systems are research hot spots in recently years. Thirdly, a lot of research efforts have also been devoted to multiple-coil topology WPT systems [61], [62], including three-coil topology [63] – [66] and four-coil topology systems [67] – [69]. Fourthly, for vehicle-to-grid (V2G) and grid-to-vehicle (G2V) applications in modern smart grid, bi-directional WPT systems are becoming popular in academic research field [21], [70] – [76]. Fifthly, research on WPT systems with multiple transmitters or/and multiple receivers [62], [77] – [83], has been reported. Furthermore, there are still many other research directions on WPT including but not limited to: multi-dimensional omnidirectional WPT systems [84], WPT systems with class E power amplifier and rectifier: [85] – [87], multi-frequency WPT systems [88] – [90], and harmonic-frequency WPT systems [91], [92].

Basically, a typical MRC WPT system consists of a high frequency voltage/current source, coupled primary and secondary resonant tanks, and a load. For the high frequency source, wide-bandwidth power amplifier, class-E amplifier, full-bridge inverter, and half-bridge inverter are alternatives. Usually for practical applications, DC-AC full-bridge inverter is the most common and economical source of the WPT system, especially for high power applications. For resonant tanks, generally there are four basic topologies regarding to the configurations of resonant coils and capacitors: series-series (SS), series-parallel (SP), parallel-

series (PS), parallel-parallel (PP). If a voltage source is used, SS and SP topologies are suitable while PS and PP topologies are more suitable for current source. For SS and PS topologies, the load is connected in series with the secondary resonant tank, while for SP and PP topologies, it is connected in parallel with the secondary resonant tank. If the load requires a specific DC voltage, then an AC-DC rectifier or multi-stage AC-DC converter would be used to convert the high frequency AC voltage to a specific DC voltage. Power source of the WPT system is usually taken from the electric grid (220 V_{rms}, 50 Hz) or DC voltage source (battery packs). If power is taken from the electric grid, AC-DC power factor correction stage (PFC) is usually needed to guarantee the power quality of the electric grid. Therefore, it is very common that a WPT system consists of an AC-DC PFC stage, a DC-AC high frequency inverter, coupled primary and secondary resonant tanks, an AC-DC rectifier, a DC-DC converter, and a load, as shown in Fig. I-1.

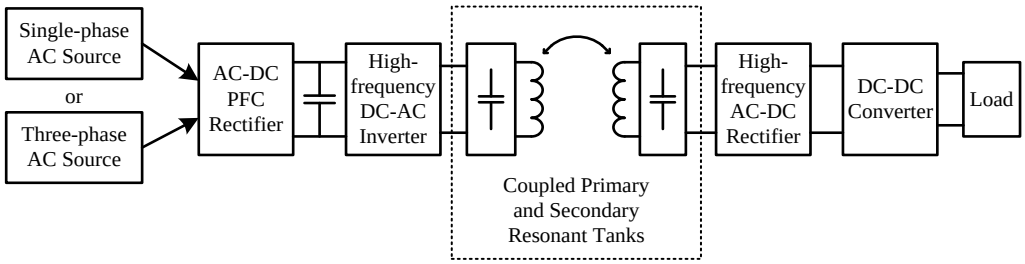


Fig. I-1. Typical WPT system

I.1.2 Single-phase single-stage AC-DC converters with power factor correction

Harmonic pollutions are essential concerns for designing power electronics converters when drawing power from the electric grid. Due to more and more use of switching mode power supplies (SMPS), the power quality of the electric grid has become an important issue. It is now indispensable to embed functions of PFC and input current shaping into an AC-DC converter. A traditional isolated AC-DC

converter with PFC usually employs a two-stage topology: the first stage is an AC-DC boost PFC converter and the second is a DC-DC isolated conversion stage. Generally, such two-stage topology cannot achieve the highest efficiency due to more power losses in the two-stage conversion while it is also not the most economical as more components would be required. Moreover, the complexity of control circuits and algorithms is also increased too.

In recent years, single-stage topologies [93], [94] that integrate both the PFC and isolated DC-DC conversion into one power conversion stage have been proposed to overcome the aforementioned drawbacks. Most existing researches are mainly focused on applying single-stage topologies in full-bridge converter [95], half-bridge converter [96], LLC converter [97] – [99], forward converter [100], flyback converter [101] – [103], and so on, with most of them designed for small power applications, as shown in Fig. I-2 – Fig. I-6.

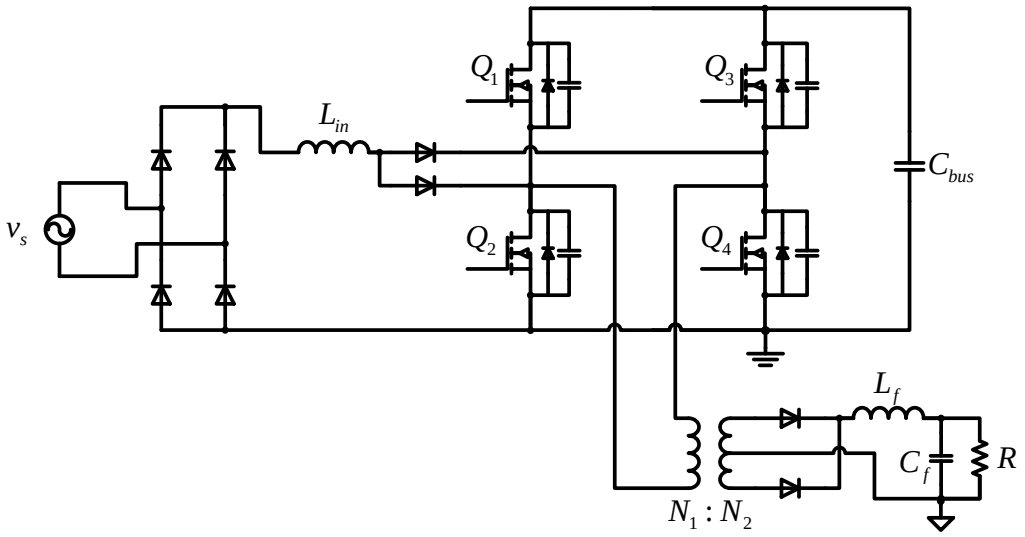


Fig. I-2. Single-stage full-bridge converter [95]

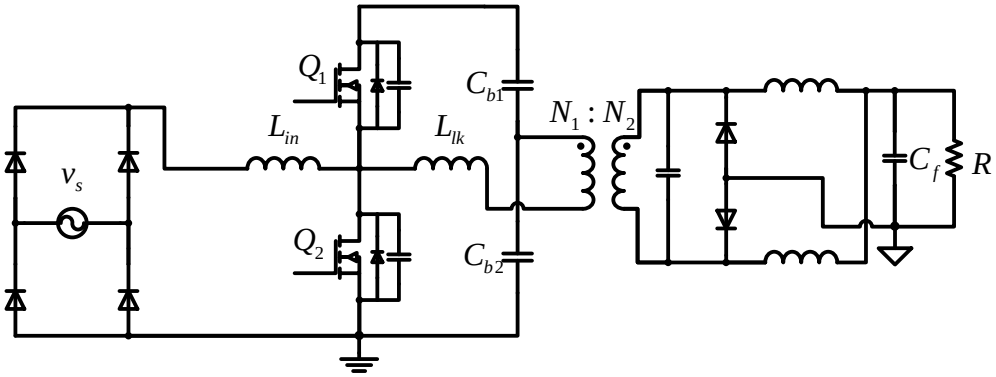


Fig. I-3. Single-stage half-bridge converter [96]

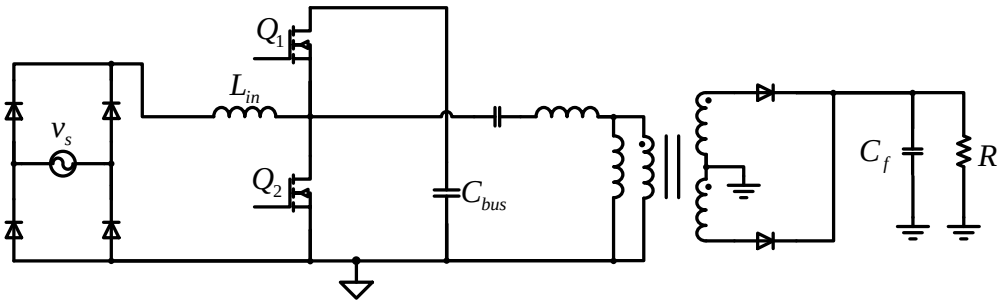


Fig. I-4. Single-stage LLC converter [97]

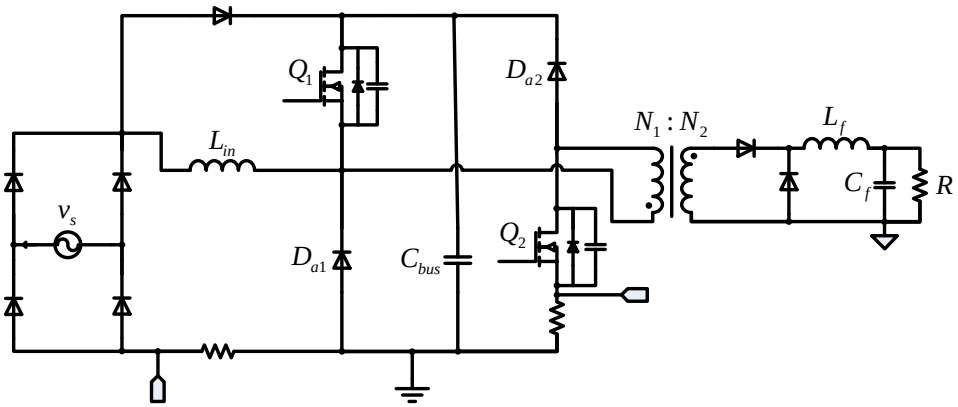


Fig. I-5. Single-stage boost-forward converter [100]

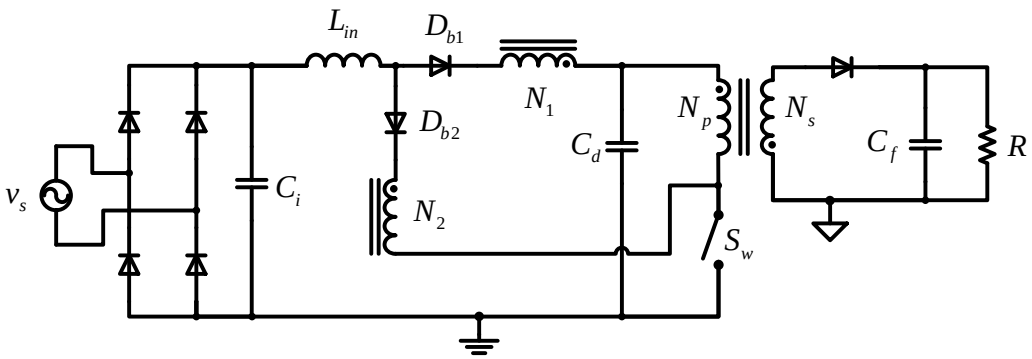


Fig. I-6. Single-stage flyback converter introduced in [101] and [102]

From Fig. I-2 – Fig. I-6, it can be seen that there is no separate PFC stage in those topologies. After the full-bridge diode rectifier is the integrated PFC and DC-DC isolated topology. Because the functions of PFC and DC-DC isolated conversion are realized simultaneously in a stage with a set of switching devices, they are called as single-stage topologies.

To reduce conduction losses of the front-end full-bridge diode-rectifier bridge, bridgeless boost PFC rectifiers [104] – [107] have been studied by many researchers, as shown in Fig. I-7 – Fig. I-9. Conduction losses caused by rectifier diodes can be reduced by eliminating a diode in line current path. As shown in Fig. I-7 and Fig. I-8, number of low-frequency rectifier diodes can be reduced from 4 to 2, and hence lower the circuit cost. Generally, bridgeless boost PFC rectifiers have two main advantages than conventional full-bridge diode boost PFC rectifier: less conduction losses and lower diode count. Due to those merits, bridgeless boost PFC rectifier is applied in single-stage AC-DC isolated half-bridge converter with soft switching [108] to further improve the system efficiency and lower the production cost, as shown in Fig. I-10. This topology uses only 2 power switches, 2 low frequency diodes, and 2 high frequency diodes to realize PFC and isolated DC-DC conversion with high efficiency, low cost, and low control complexity.

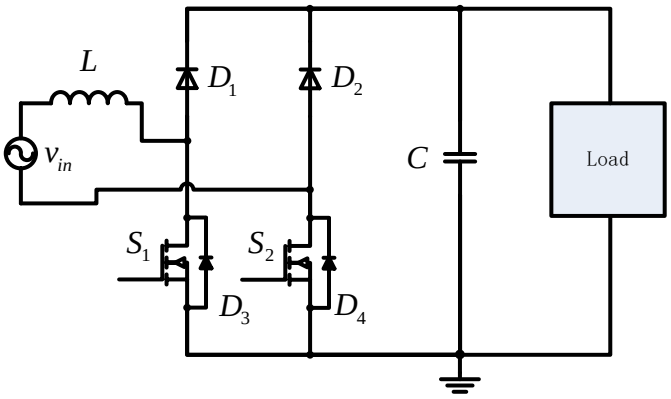


Fig. I-7. Single-phase rectifier with input power factor correction [104]

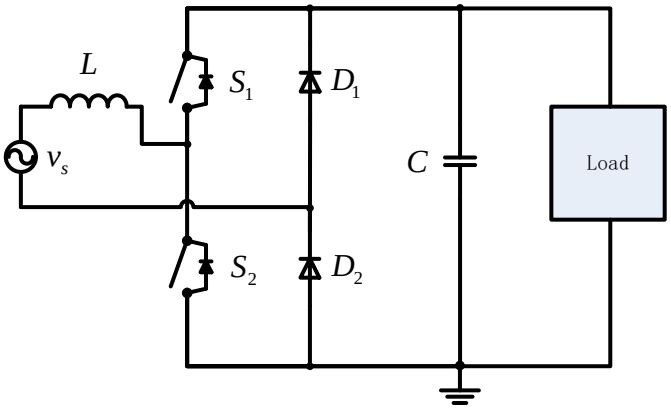


Fig. I-8. Single-phase PWM rectifier with input power factor correction [105]

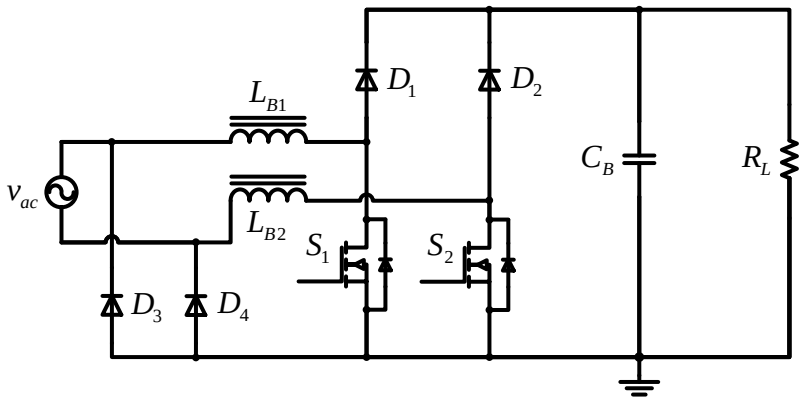


Fig. I-9. Bridgeless PFC boost rectifier with two dc/dc boost circuits introduced in [107]

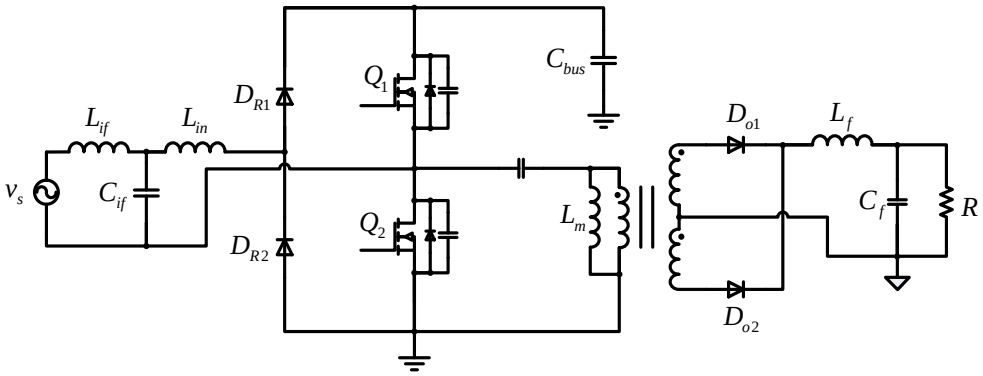


Fig. I-10. Single-stage half-bridge AC-DC converter with bridgeless boost PFC rectifier proposed in [108]

I.1.3 Three-phase single-stage AC-DC converters with power factor correction

For high power isolated AC-DC conversions, power is usually drawn from a three-phase 50/60 Hz AC source. Like single-phase isolated AC-DC converters, the function of PFC needs to be considered in three-phase topologies as well so as to avoid inserting too much harmonics pollutions into the power grid and guarantee its power quality. PFC functionality for three-phase AC-DC topologies is of greater significance than single-phase AC-DC topologies because the power of three-phase topologies is usually much larger, meaning that they may insert much more unwanted harmonics into the power grid if their PFC performances are unsatisfactory. The most common three-phase isolated AC-DC converters also apply two-stage conversion: the first is a three-phase AC-DC PFC rectifier and the second is DC-DC conversion. For three-phase AC-DC PFC rectifier, there exist various kinds of topologies: three separate single-phase boost PFC rectifiers, three-phase single-switch DCM boost PFC converter [109], TAIPEI rectifier (a three-phase two-switch ZVS PFC DCM boost rectifier) [110], three-phase buck-boost type six-switch PFC converter [111], etc. To improve system efficiency, reduce circuit complexity and cost, a number of three-phase single-stage isolated AC-DC topologies are proposed and studied by scholars and researchers: modular

type topology [112], interleaved type topologies [113], [114], three-level type topology [115], buck-type full-bridge topology [116], and others [117] – [119], as shown in Fig. I-11 – Fig. I-15.

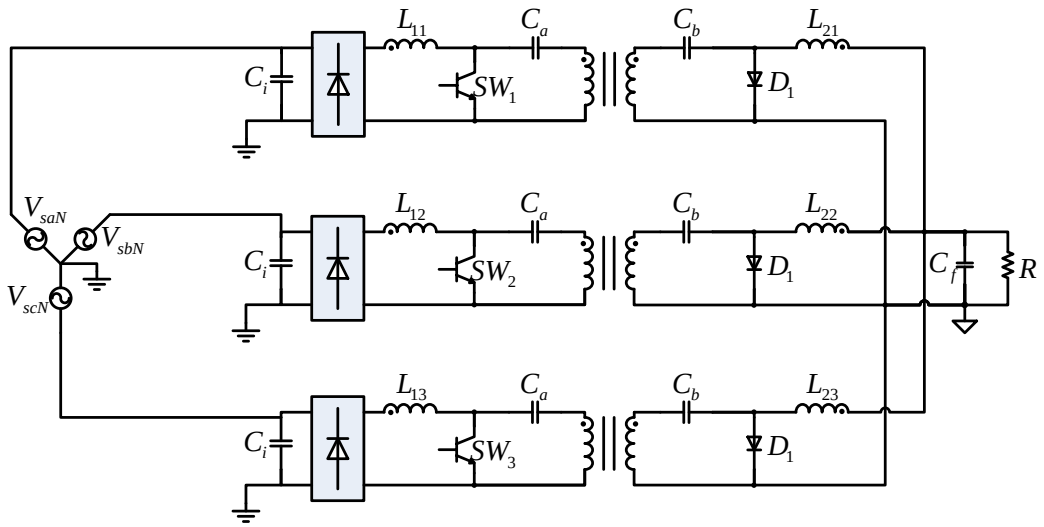


Fig. I-11. Modular type three-phase single-stage isolated AC-DC topology [112]

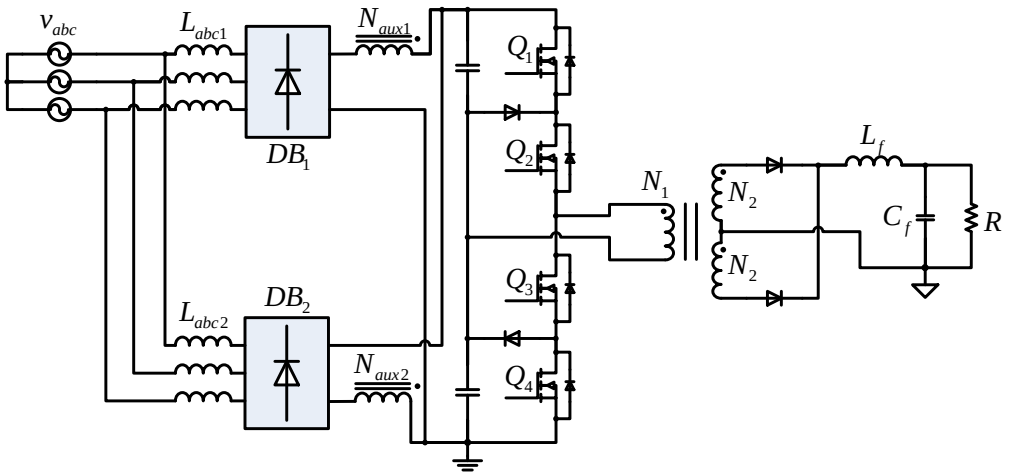


Fig. I-12. Interleaved type three-phase single-stage isolated AC-DC topology [113]

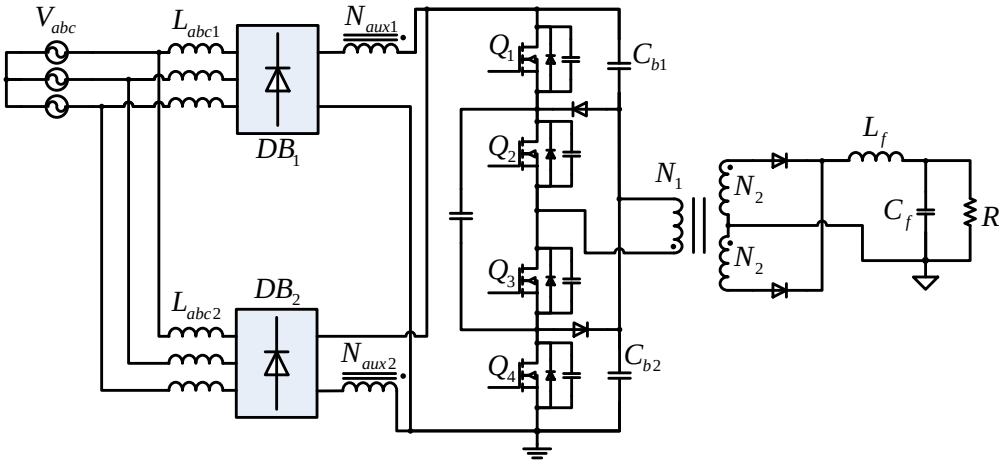


Fig. I-13. Interleaved type three-phase single-stage isolated AC-DC topology [114]

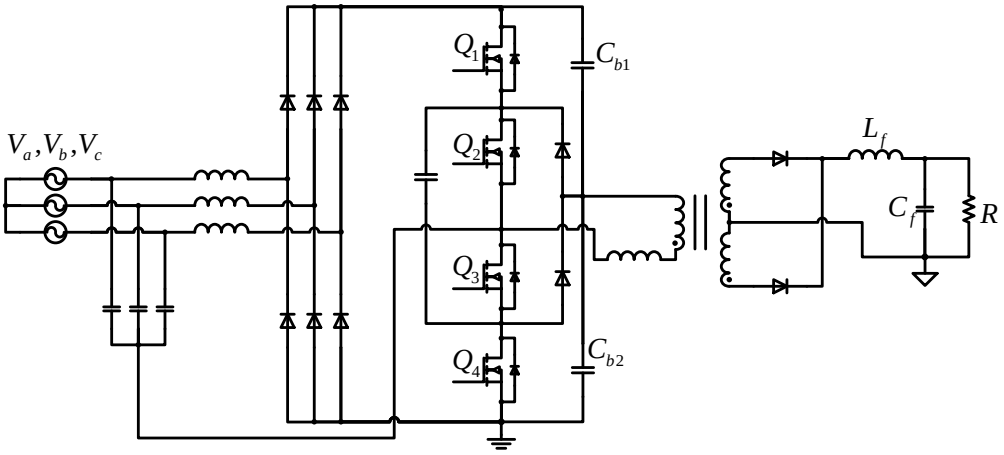


Fig. I-14. Three-level type three-phase single-stage isolated AC-DC topology [115]

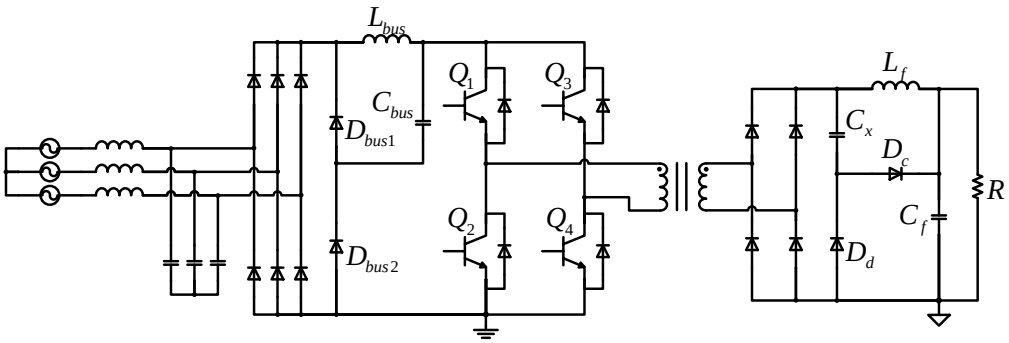


Fig. I-15. Buck type full-bridge three-phase single-stage isolated AC-DC topology [116]

I.1.4 Incentives of Research

Wireless power transfer is more and more important in home appliances and industrial applications, and the power quality of the electric grid will be affected if WPT applications are directly drawing power from the electric grid. Hence, PFC or THD reduction function is necessary for any grid-connected WPT applications. Moreover, loads of WPT applications are often DC loads with controlled voltages. Therefore, most WPT applications drawing power from AC electric grid and supplying DC loads adopt a two-stage conversion approach, the same as many transformer-based AC-DC converters with PFC. As single-stage topologies are widely used in transformer-based AC-DC converters, it was considered to apply single-stage topologies with PFC into WPT applications in order to improve the system efficiency, reduce production cost, and reduce control complexity while providing good PFC functionality.

A DC-DC WPT converter consists of a primary-side DC-AC high frequency inverter, coupled primary and secondary WPT resonant tanks, a secondary-side AC-DC high frequency rectifier, a DC filtering capacitor, and a DC load, similar to other transformer-based DC-DC converters except for the difference of the WPT resonant tanks and transformer-based tanks. There have been many researches and studies of single-stage isolated AC-DC converters, which combine an AC-DC PFC rectifier and a transformer-based DC-DC converter into one conversion stage. Therefore, it is also feasible to combine an AC-DC PFC rectifier and a DC-DC WPT converter into one conversion stage, which can be called as single-stage AC-DC WPT converter. The topologies and control methods of this idea for single-phase and three-phase AC sources are main research focuses of this work.

I.2 Primary Contribution

In this thesis, topologies and control of single-stage AC-DC WPT converters with PFC and the characteristics of the DC-DC WPT converter with SS topology are explored and developed, and the primary contributions of this work are

summarized as follows:

Firstly, a new single-phase single-stage AC-DC WPT converter with PFC is proposed to not only reduce the system cost and complexity but also improve the system efficiency. Compared with other single-phase AC-DC WPT converters with PFC, the proposed converter has lowest count of power semiconductor devices and high system efficiency with constant operation frequency, three-level adjustable duty cycle control with soft-switching. A laboratory prototype has been built to verify the proposed topology and control method with impressive measured performance of 90.1% efficiency at 2.56 kW output power, with 0.99 power factor and 15.4% input current THD.

Secondly, a new control method for the above single-phase single-stage AC-DC WPT resonant converter with PFC is proposed to further improve the power quality of the input source and lower the DC bus voltage in order to reduce the voltage ratings of the primary-side components. Though soft-switching cannot be realized in this control method, simulation results show that the power factor can be improved to higher than 0.99 and that input current THD can be reduced to lower than 1% with the DC bus voltage reduced to 500 V from the original 723.5 V (with original constant frequency variable duty cycle control method).

Thirdly, a new three-phase single-stage AC-DC WPT converter with PFC is proposed for high power applications. Compared with the proposed single-phase single-stage topology, the proposed three-phase topology exhibits remarkably better PFC function with power factor 1.0 and input current THD 3.5% due to the elimination of zero-sequence components in input current, and utilizes lower count of power semiconductor devices compared with other three-phase AC-DC WPT converters with PFC. A maximum efficiency of 91.7% is archived from a laboratory prototype with 1.25 kW output power. Furthermore, a new control strategy is proposed to simultaneously regulate the operation frequency and duty cycle according to the characteristics of the proposed topology so as to largely reduce and constantly control the bus voltage for varying load power.

Last but not least, an accurate steady-state analysis method of DC-DC SS WPT converter is proposed for the first time. Unlike common analysis method of DC-DC resonant converters with fundamental harmonic approximation (FHA), the proposed accurate analysis method considers both fundamental and higher-order components in the circuit, and is further applied to develop a novel parameters estimation algorithm for the DC-DC WPT converter with SS topology to estimate the mutual inductance, output voltage, output power, and system efficiency with only the primary-side information of the WPT converter without requiring any sensing of voltage and current as well as wireless communication module for information feedback from the secondary side. Compared with other existing parameter estimation methods of WPT systems with at least 8.3% error, the proposed algorithm exhibits higher accuracy with maximum measured error below 3%.

I.3 Thesis Layout

Chapter I introduces background, incentives of research, contributions, and layout of the thesis. Chapter II presents the analysis of a DC-DC WPT converter, including steady-state analysis and small-signal analysis. Chapter III proposes a new single-phase single-stage AC-DC WPT converter with PFC. Steady-state analysis, operation principle, general control method, and design procedure of the converter are presented in detail. A 2.56 kW experimental prototype is developed and tested. In Chapter IV, a new control method for the proposed single-phase single-stage AC-DC WPT converter named Average Discontinuous Current Mode (ADCM) Control is proposed and illustrated in details, with simulation results validating its advantages and feasibility. Chapter V proposes the design of a new three-phase single-stage AC-DC WPT converter with PFC and presents its detailed theoretical analysis and corresponding control method. An example with detailed design procedure is implemented to verify its functions and feasibility

with a 1.25kW laboratory prototype. The proposed accurate analysis method of DC-DC WPT converter is introduced and studied in Chapter VI. Based on the accurate analysis method, a new parameters estimations algorithm is proposed and verified in this chapter. Finally, Chapter VII gives a conclusion of the thesis and plans for the future work. The thesis layout is also shown in Fig. I-16.

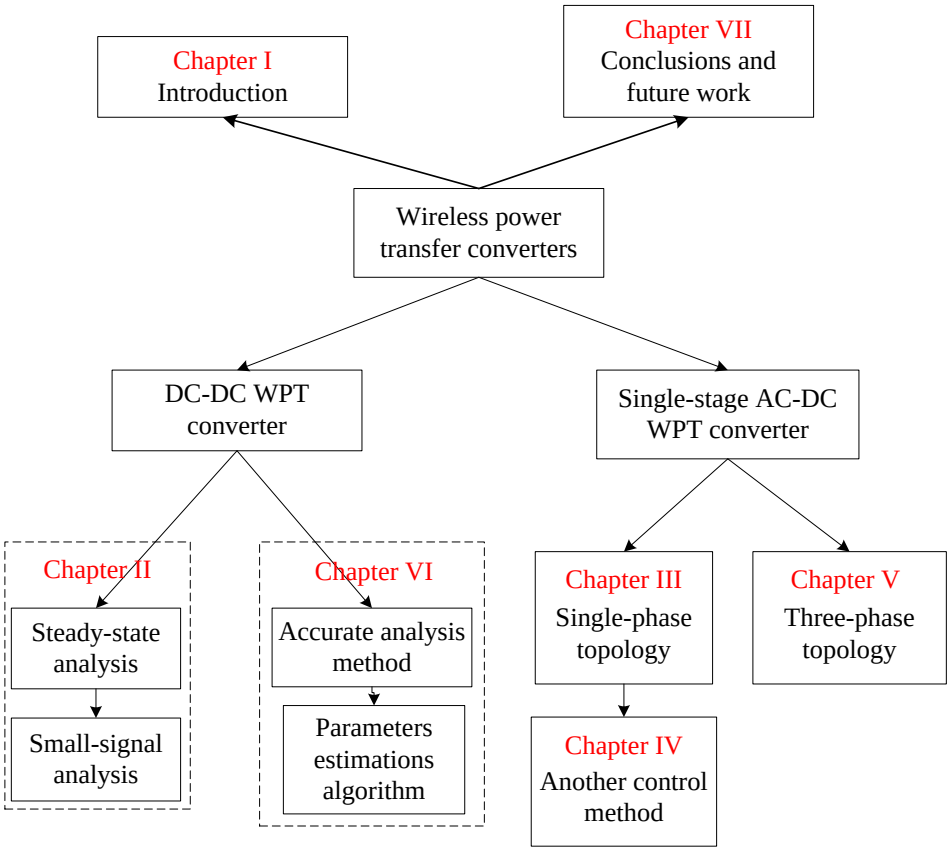


Fig. I-16. Schematic of thesis layout

I.4 List of Publications

Journal papers:

1. **J. Liu**, K. W. Chan, C. Y. Chung, N. H. L. Chan, M. Liu and W. Xu, "Single-stage wireless-power-transfer resonant converter with boost bridgeless power-factor-correction rectifier," in *IEEE Transactions on Industrial Electronics,* vol. 65, no. 3, pp. 2145-2155, March 2018.

2. **J. Liu**, W. Xu, K. W. Chan, N. H. L. Chan, M. Liu, "A three-phase single-stage AC-DC wireless-power-transfer converter with power factor correction and bus voltage control," submitted to *IEEE Journal of Emerging and Selected Topics in Power Electronics*, JESTPE-2018-08-0628.
3. **J. Liu**, K. W. Chan, N. H. L. Chan, C. Y. Chung, "A new parameter estimation algorithm requiring only primary-side information of DC-DC wireless-power-transfer resonant converter under unknown varying misalignment and load conditions," under revision for resubmission to *IEEE Transactions on Industrial Electronics*, 17-TIE-3426.R1.
4. **J. Liu**, K. W. Chan, N. H. L. Chan, W. Xu, M. Liu, “A modulation and control method of single-stage AC-DC wireless-power-transfer resonant converter with improved input power quality, reduced bus voltage, and wide load range operation, and without bulky bus capacitor,” under preparation for submission to *IEEE Transactions on Industrial Electronics*.

Conference papers:

1. **J. Liu**, C. Y. Chung and H. L. Chan, "Design and implementation of high power closed-loop AC-DC resonant converter for wireless power transfer," *2014 IEEE 15th Workshop on Control and Modeling for Power Electronics (COMPEL),* Santander, 2014, pp. 1-8.

2. T. Wu, W. Mai, M. Qin, C. Zhang, J. Li, Y. Nie, **J. Liu**, C. Y. Chung, "Optimal

operation of combined cooling heat and power microgrid with PEVs," *2015 IEEE Eindhoven PowerTech*, Eindhoven, 2015, pp. 1-6.

3. W. Xu, K. W. Chan, N. H. L. Chan and **J. Liu**, "A modified control method for bi-directional Z-source converters," *2016 IEEE Transportation Electrification Conference and Expo (ITEC)*, Dearborn, MI, 2016, pp. 1-7.

Chapter II

DC-DC Wireless-Power-Transfer Resonant Converter

II.1 WPT Resonant Tanks

Basically there are four types of topologies of WPT resonant tank [8]: series-series (SS), series-parallel (SP), parallel-series (PS), and parallel-parallel (PP), as shown in Fig. II-1. Such topologies depend on how resonant capacitors and coils (inductors) are configured. As shown in Fig. II-1, series connected primary sides (SS and SP) are commonly used with voltage source while parallel connected primary sides (PS and PP) are used with current source. In this thesis, voltage source driving converters are the research focus, and therefore, characteristics of SS and SP topologies are studied in details.

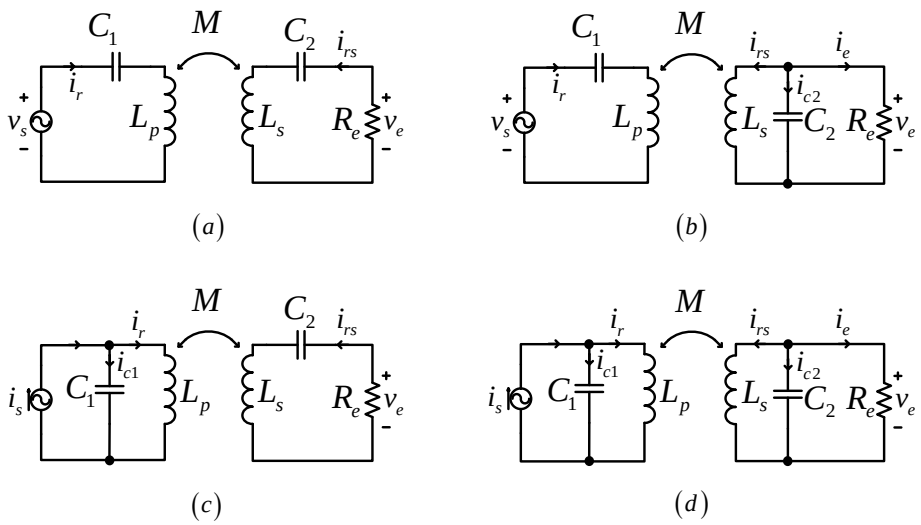


Fig. II-1. Topologies of WPT resonant tank: (a) SS; (b) SP; (c) PS; (d) PP

II.1.1 SS topology

Applying Kirchhoff's voltage law (KVL) to the circuit of Fig. II-1 (a), the following equations can be obtained:

$$v_i = \left(\frac{1}{j\omega_s C_1} + j\omega_s L_p \right) \cdot i_r + j\omega_s M \cdot i_{rs}, \tag{2.1}$$

$$0 = j\omega_s M \cdot i_r + \left(\frac{1}{j\omega_s C_2} + j\omega_s L_s \right) \cdot i_{rs} + R_e \cdot i_{rs}, \tag{2.2}$$

$$v_e = -i_{rs} \cdot R_e. \tag{2.3}$$

Therefore, the voltage gain, input impedance, and transferred power are obtained as:

$$\left(\frac{V_{ep}}{V_{ip}} \right)_{ss} = \left(\frac{|v_e|}{|v_i|} \right)_{ss} = \frac{1}{\sqrt{\frac{1}{R_e^2}\left[\frac{\left(\omega_s L_p - \frac{1}{\omega_s C_1} \right)\left(\omega_s L_s - \frac{1}{\omega_s C_2} \right)}{\omega_s M} - \omega_s M \right]^2 + \left[\frac{\omega_s L_p - \frac{1}{\omega_s C_1}}{\omega_s M} \right]^2}}, \tag{2.4}$$

$$Z_{r.ss} = \frac{v_i}{i_r} = \frac{\omega_s^2 M^2 R_e}{R_e^2 + \left(\omega_s L_s - \frac{1}{\omega_s C_2} \right)^2} + j\left[\left(\omega_s L_p - \frac{1}{\omega_s C_1} \right) - \frac{\omega_s^2 M^2 \left(\omega_s L_s - \frac{1}{\omega_s C_2} \right)}{R_e^2 + \left(\omega_s L_s - \frac{1}{\omega_s C_2} \right)^2} \right], \tag{2.5}$$

$$P_{e.ss} = \frac{V_{ip}^2 / (2R_e)}{\frac{1}{R_e^2}\left(\frac{\left(\omega_s L_p - \frac{1}{\omega_s C_1} \right)\left(\omega_s L_s - \frac{1}{\omega_s C_2} \right)}{\omega_s M} - \omega_s M \right)^2 + \left(\frac{\omega_s L_p - \frac{1}{\omega_s C_1}}{\omega_s M} \right)^2}. \tag{2.6}$$

The circuit of resonant tank can also be transformed to an equivalent circuit with an ideal transformer as shown in Fig. II-2 (a). L_1, L_2, L_m, and n_e are defined as:

$$\begin{aligned} n_e &= \sqrt{L_s / L_p}, \\ L_1 &= L_p - M / n_e, \\ L_2 &= L_s - M \cdot n_e, \\ L_m &= M / n_e. \end{aligned} \tag{2.7}$$

If the ESRs of the coils are considered, noted as R_{lp} and R_{ls}, as shown in Fig. II-2 (b), then the efficiency can be obtained as:

$$\eta_{ss} = \frac{\mathrm{Re}(Z_{m2})}{\mathrm{Re}(Z_{m2}) + R_{lp}} \cdot \frac{R_e}{R_e + R_{ls}}, \tag{2.8}$$

where

$$Z_{m2} = \frac{\frac{1}{n^2}\left(j\omega_s L_2 + \frac{1}{j\omega_s C_2} + r_2 + R_e \right) \cdot j\omega_s L_m}{\frac{1}{n^2}\left(j\omega_s L_2 + \frac{1}{j\omega_s C_2} + r_2 + R_e \right) + j\omega_s L_m}. \tag{2.9}$$

For SS topology, the curves of different kinds of characteristics varying with frequency and load resistance are shown in Fig. II-4, where the corresponding parameters are: L_p=100 μH; L_s=100 μH; M=10 μH; C_1=10 nF; C_2=10 nF; R_{lp}=0.5 Ω; R_{ls}=0.5 Ω.

For SS topology WPT resonant tank, there are three resonant frequencies: lower resonant frequency f_1 (ω_1), higher resonant frequency f_2 (ω_2), and middle resonant frequency f_3 (ω_3), which are defined as:

$$f_1 = \frac{1}{2\pi\sqrt{(L_p + M/n_e)C_1}} = \frac{1}{2\pi\sqrt{(L_s + M \cdot n_e)C_2}}, \quad \omega_1 = 2\pi f_1, \tag{2.10}$$

$$f_2 = \frac{1}{2\pi\sqrt{(L_p - M/n_e)C_1}} = \frac{1}{2\pi\sqrt{(L_s - M \cdot n_e)C_2}}, \quad \omega_2 = 2\pi f_2, \tag{2.11}$$

$$f_3 = \frac{1}{2\pi\sqrt{L_p C_1}} = \frac{1}{2\pi\sqrt{L_s C_2}}, \quad \omega_3 = 2\pi f_3, \tag{2.12}$$

It can be analyzed theoretically that at lower resonant frequency f_1 or higher resonant frequency f_2, voltage transfer gain is constant and load-independent. At middle resonant frequency f_3, efficiency reaches the maximum value.

II.1.2 SP topology

Applying Kirchhoff's voltage law (KVL) to the circuit of Fig. II-1 (b), the following equations can be obtained:

$$v_i = \left(\frac{1}{j\omega_s C_1} + j\omega_s L_p \right) \cdot i_r + j\omega_s M \cdot i_{rs}, \tag{2.13}$$

$$v_e = j\omega_s L_s \cdot i_{rs} + j\omega_s M \cdot i_r, \tag{2.14}$$

$$i_{rs} + v_e \cdot j\omega_s C_2 + \frac{v_e}{R_e} = 0. \tag{2.15}$$

Therefore, the voltage gain, input impedance, and transferred power are obtained as:

$$\left(\frac{V_{ep}}{V_{ip}} \right)_{sp} = \left(\frac{|v_e|}{|v_i|} \right)_{sp} = \frac{1}{\sqrt{\left[\omega_s^2 C_2 M - \frac{\left(1-\omega_s^2 L_p C_1\right)\left(1-\omega_s^2 L_s C_2\right)}{\omega_s^2 C_1 M} \right]^2 + \frac{1}{R_e^2}\left[\frac{L_s\left(\omega_s^2 L_p C_1 - 1\right)}{\omega_s C_1 M} + \omega_s M \right]^2}}, \tag{2.16}$$

$$Z_{r.sp} = \frac{v_i}{i_r} =$$

$$\frac{\omega_s{}^2 M^2 R_e}{R_e{}^2\left(1-\omega_s{}^2 L_s C_2\right)^2 + \omega_s{}^2 L_s{}^2} + \tag{2.17}$$

$$j\left[\left(\omega_s L_p - \frac{1}{\omega_s C_1}\right) + \frac{\omega_s{}^2 M^2\left(\omega_s C_2\left(1-\omega_s{}^2 L_s C_2\right) R_e{}^2 - \omega_s L_s\right)}{R_e{}^2\left(1-\omega_s{}^2 L_s C_2\right)^2 + \omega_s{}^2 L_s{}^2}\right],$$

$$P_{e.sp} =$$

$$\frac{V_{ip}{}^2}{2R_e\left[\left(\omega_s{}^2 C_2 M - \frac{\left(1-\omega_s{}^2 L_p C_1\right)\left(1-\omega_s{}^2 L_s C_2\right)}{\omega_s{}^2 C_1 M}\right)^2 + \frac{1}{R_e{}^2}\left(\frac{L_s\left(\omega_s{}^2 L_p C_1 - 1\right)}{\omega_s C_1 M} + \omega_s M\right)^2\right]}. \tag{2.18}$$

If the internal resistances of the two coils are considered, then the efficiency can be obtained as:

$$\eta_{sp} = \frac{\mathrm{Re}\left(Z_{m2}\right)}{\mathrm{Re}\left(Z_{m2}\right) + R_{lp}} \cdot \frac{\mathrm{Re}\left(Z_{a1}\right)}{\mathrm{Re}\left(Z_{a1}\right) + R_{ls}}, \tag{2.19}$$

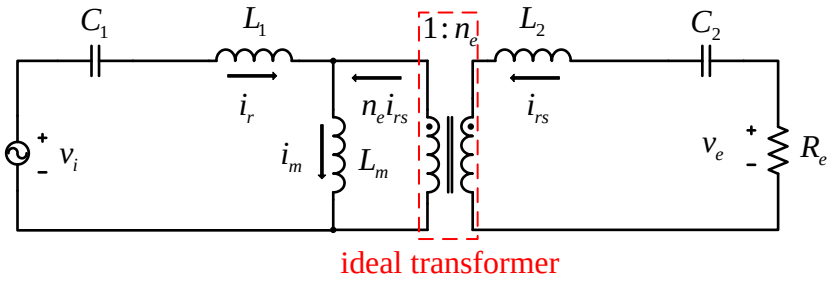
where

$$Z_{a1} = \frac{\frac{1}{j\omega_s C_2} \cdot R_e}{\frac{1}{j\omega_s C_2} + R_e} = \frac{R_e}{1 + j\omega_s C_2 R_e}, \tag{2.20}$$

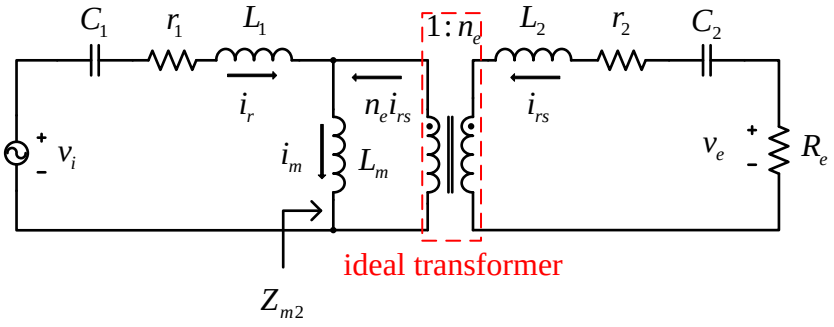
$$Z_{m2} = \frac{\frac{1}{n^2}\left(j\omega_s L_2 + r_2 + \frac{R_e}{1 + j\omega_s C_2 R_e}\right) \cdot j\omega_s L_m}{\frac{1}{n^2}\left(j\omega_s L_2 + r_2 + \frac{R_e}{1 + j\omega_s C_2 R_e}\right) + j\omega_s L_m}. \tag{2.21}$$

For SP topology, the circuit can also be transformed to the equivalent circuits with ideal transformer as shown in Fig. II-3 and the curves of different kinds of characteristics varying with frequency and load resistance are shown in Fig. II-5,

where the corresponding parameters are: L_p = 100 μH; L_s = 100 μH; M = 10 μH; C_1 = 10 nF; C_2 = 10 nF; R_{lp} = 0.5 Ω; R_{ls} = 0.5 Ω.

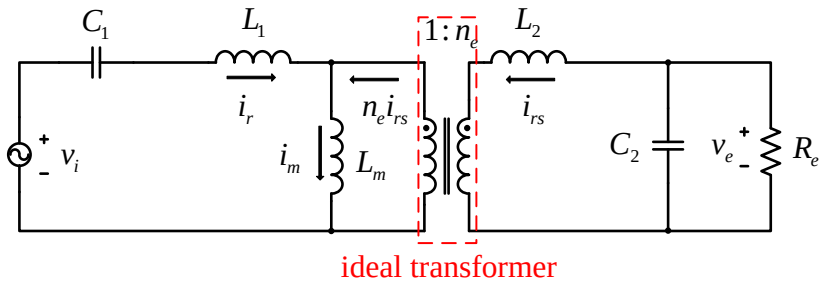


(a)

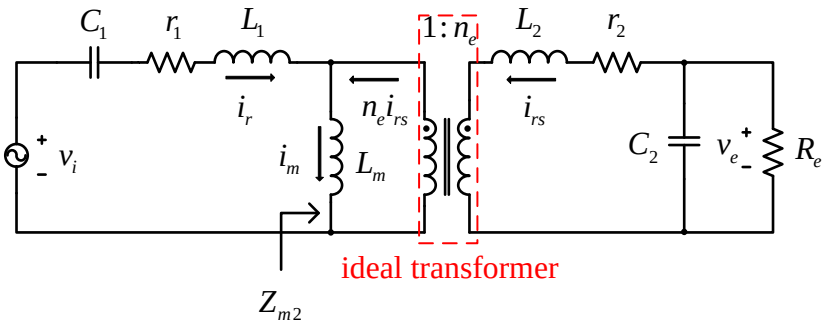


(b)

Fig. II-2. Equivalent circuits for SS topology



(a)



(b)

Fig. II-3. Equivalent circuits for SP topology

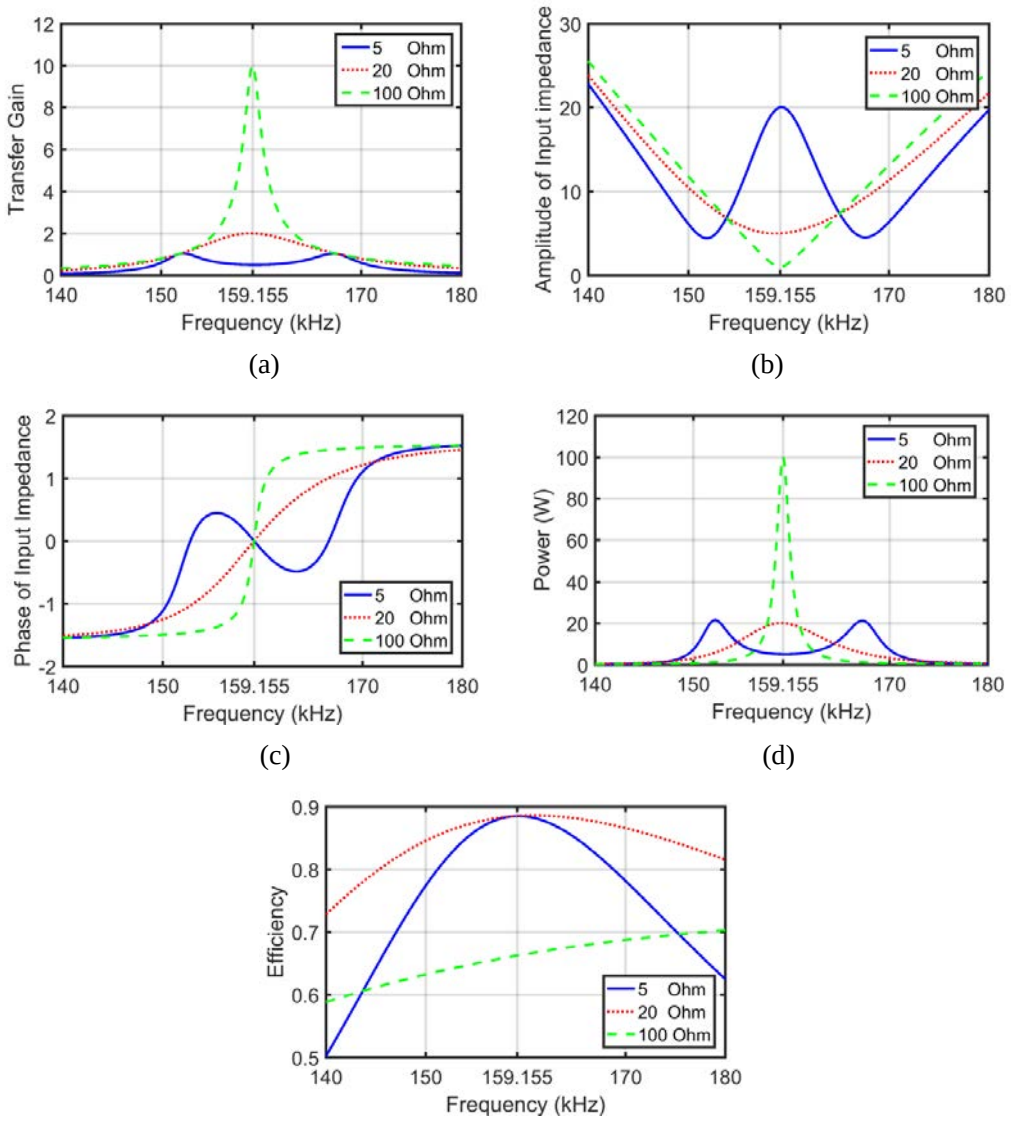


Fig. II-4. Characteristics for SS topology: (a) Transfer gain; (b) Amplitude of input impedance; (c) Phase of input impedance; (d) Power; (e) Efficiency

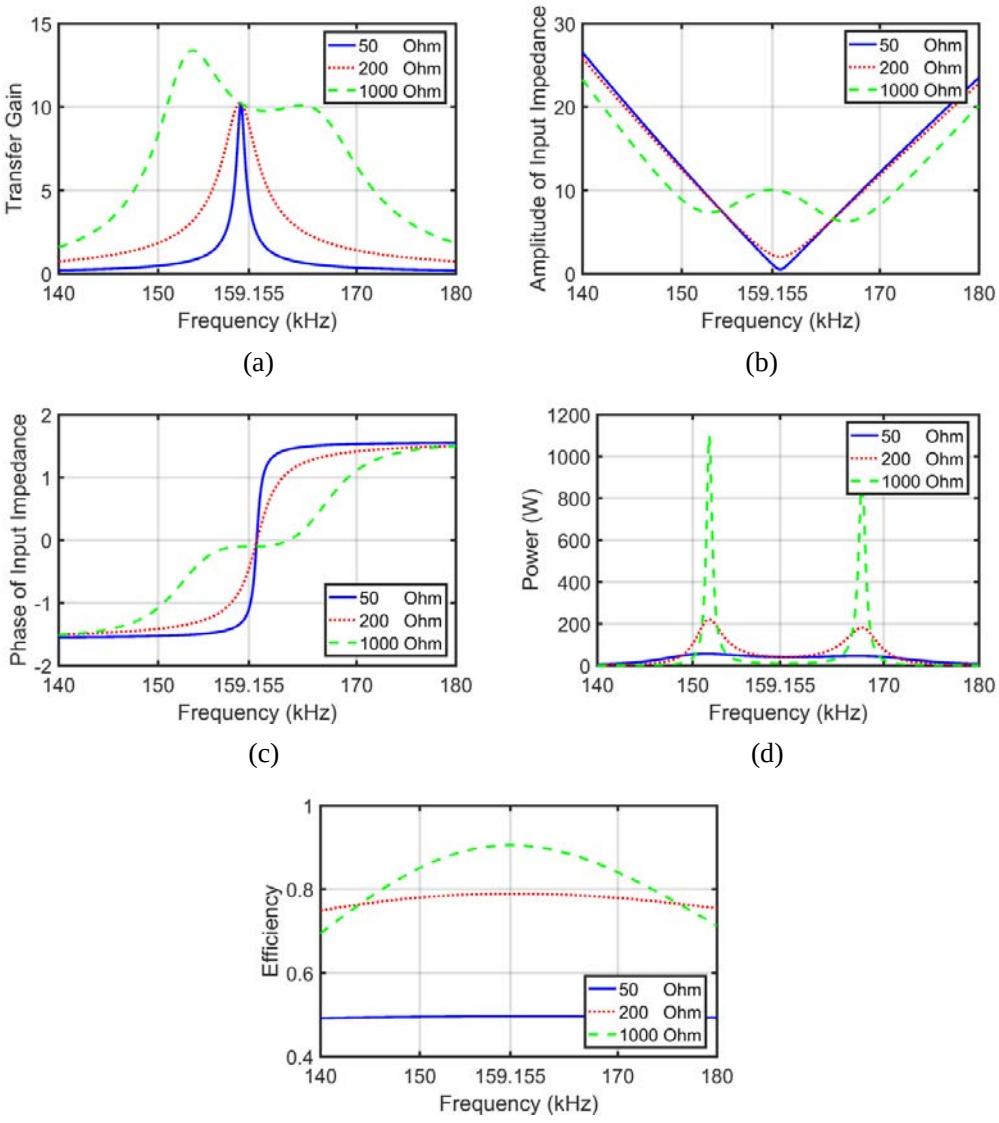


Fig. II-5. Characteristics for SP topology (a) Transfer gain; (b) Amplitude of input impedance; (c) Phase of input impedance; (d) Power; (e) Efficiency

II.2 Steady-State Analysis of DC-DC WPT Resonant Converter

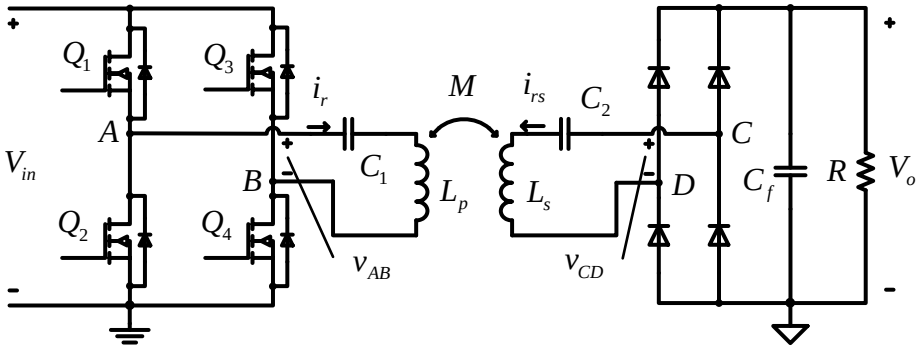


Fig. II-6. DC-DC WPT resonant converter with SS topology

A typical DC-DC WPT resonant converter consists of a primary-side high frequency full-bridge inverter, coupled primary and secondary resonant tanks (SS), a secondary-side rectifier bridge, an output filtering capacitor, and a load resistor, as shown in Fig. II-6. It can be analyzed that voltages of the resonant tanks (v_{AB} and v_{CD}) are square wave, not sine wave. However, due to the filtering characteristic of the resonant tank at resonant frequencies, fundamental component of currents and voltages are dominant in the converter. Therefore, fundamental harmonic approximation (FHA) method [120], assuming that all currents and voltages are fundamental frequency sine wave, is applied to analyze the steady state of the converter. Applying Fourier series method, v_{AB} and v_{CD} are assumed to be their fundamental components, expressed as follows:

$$v_{AB} \approx v_{AB.1} = \frac{4}{\pi} \cdot V_{in} \sin\left(\omega_s t + \alpha\right) \tag{2.22}$$

$$v_{CD} \approx v_{CD.1} = \frac{4}{\pi} \cdot V_o \sin\left(\omega_s t + \beta\right) \tag{2.23}$$

The currents flowing through primary and secondary resonant tanks are nearly sinusoidal, and they can also be expressed as follows:

$$i_r = I_{rp} \sin\left(\omega_s t + \theta\right) \tag{2.24}$$

$$i_{rs} = I_{rsp} \sin\left(\omega_s t + \delta\right) \tag{2.25}$$

Here I_{rp} and I_{rsp} are peak values of currents through primary and secondary resonant tanks, respectively. α, β, θ, and δ are phase angles. ω_s is operating frequency in radian.

The DC-DC WPT resonant converter (with SS topology) can be equivalent to the simplified circuit of Fig. II-1 (a), with the following relations:

$$V_{ip} = \frac{4}{\pi} V_{in}, \tag{2.26}$$

$$V_{ep} = \frac{4}{\pi} V_o, \tag{2.27}$$

$$R_e = \frac{8}{\pi^2} R. \tag{2.28}$$

Hence, the steady-state analysis of the DC-DC WPT resonant converter can be done with reference to the characteristics analysis of WPT resonant tanks in Section II.1.

II.3 Small-Signal Analysis of DC-DC WPT Resonant Converter

To design a closed-loop control system for the resonant converter, the small signal model of the converter has to be derived. In this thesis, the extended describing function (EDF) [121] method is adopted to proceed the small signal analysis.

II.3.1 Nonlinear State Equations

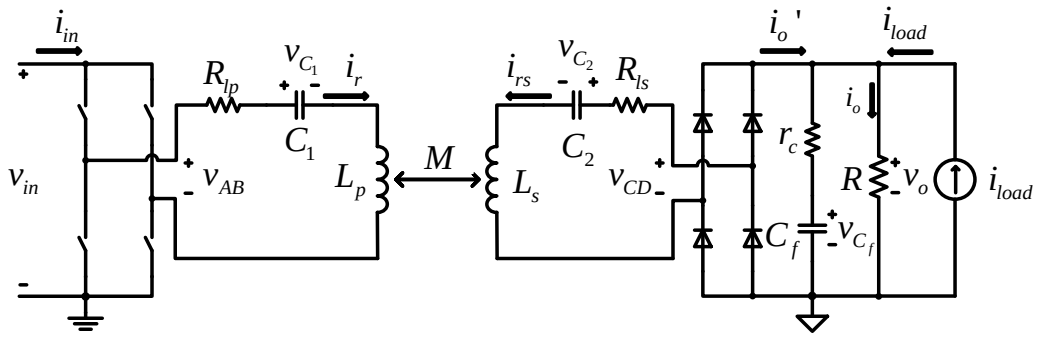


Fig. II-7. Equivalent circuit for small signal analysis

In Fig. II-7, an equivalent circuit for small signal analysis is given. Here, i_r, i_{rs}, v_{c1}, v_{c2}, v_{cf} are state variables and v_o is output variable. Applying Kirchhoff's Law, the following equations can be obtained:

$$v_{AB} = L_p \frac{di_1}{dt} + i_r R_{lp} + v_{C1} + M \frac{di_{rs}}{dt}, \tag{2.29}$$

$$i_r = C_1 \frac{dv_{C1}}{dt}, \tag{2.30}$$

$$v_{CD} = L_s \frac{di_{rs}}{dt} + i_{rs} R_{ls} + v_{C2} + M \frac{di_r}{dt}, \tag{2.31}$$

$$i_{rs} = C_2 \frac{dv_{C2}}{dt}, \tag{2.32}$$

$$v_{CD} = -\mathrm{sgn}\left(i_{rs}\right)\cdot v_o, \tag{2.33}$$

$$i_o\,' = \left|i_{rs}\right|, \tag{2.34}$$

$$i_o\,' + i_{load} = \left(1+\frac{r_C}{R}\right)C_f\,\frac{dv_{Cf}}{dt} + \frac{1}{R}v_{Cf}, \tag{2.35}$$

$$v_o = r_C\,'\cdot\left(i_o\,' + i_{load}\right) + \frac{r_C\,'}{r_C}\cdot v_{Cf}, \tag{2.36}$$

$$i_{in} = \frac{1}{T_s}\int_0^{T_s}\left(i_r\cdot\frac{v_{AB}\left(t\right)}{v_{in}}\right)dt, \tag{2.37}$$

where

$$r_C\,' = r_C \parallel R. \tag{2.38}$$

II.3.2 Fundamental harmonic approximation

In small signal analysis, state parameters i_1, i_2, v_{c1}, v_{c2} are approximated to their fundamental components.

$$i_r = i_{r.1s}\sin\omega_s t + i_{r.1c}\cos\omega_s t, \tag{2.39}$$

$$i_{rs} = i_{rs.1s}\sin\omega_s t + i_{rs.1c}\cos\omega_s t, \tag{2.40}$$

$$v_{C1} = v_{C1.1s}\sin\omega_s t + v_{C1.1c}\cos\omega_s t, \tag{2.41}$$

$$v_{C2} = v_{C2.1s}\sin\omega_s t + v_{C2.1c}\cos\omega_s t, \tag{2.42}$$

$$\frac{di_r}{dt} = \left(\frac{di_{r.1s}}{dt} - \omega_s i_{r.1c}\right)\sin\omega_s t + \left(\frac{di_{r.1c}}{dt} + \omega_s i_{r.1s}\right)\cos\omega_s t, \tag{2.43}$$

$$\frac{di_{rs}}{dt}=\left(\frac{di_{rs.1s}}{dt}-\omega_s i_{rs.1c}\right)\sin\omega_s t+\left(\frac{di_{rs.1c}}{dt}+\omega_s i_{rs.1s}\right)\cos\omega_s t, \tag{2.44}$$

$$\frac{dv_{C1}}{dt}=\left(\frac{dv_{C1.1s}}{dt}-\omega_s v_{C1.1c}\right)\sin\omega_s t+\left(\frac{dv_{C1.1c}}{dt}+\omega_s v_{C1.1s}\right)\cos\omega_s t, \tag{2.45}$$

$$\frac{dv_{C2}}{dt}=\left(\frac{dv_{C2.1s}}{dt}-\omega_s v_{C2.1c}\right)\sin\omega_s t+\left(\frac{dv_{C2.1c}}{dt}+\omega_s v_{C2.1s}\right)\cos\omega_s t. \tag{2.46}$$

II.3.3 Applying extended describing function (EDF) method

Extended describing function (EDF) method is often applied in nonlinear system analysis. Using this approach, nonlinear state term is approximately to be equal to their fundamental or DC components, neglecting their higher harmonic components.

$$v_{AB}=f_0\left(v_{in},d\right)\sin\left(\omega_s t\right)+f_1\left(v_{in},d\right)\cos\left(\omega_s t\right), \tag{2.47}$$

$$\begin{aligned} v_{CD}&=-\operatorname{sgn}\left(i_{rs}\right)\cdot v_o \\ &=f_2\left(i_{rs.1s},i_{rs.1c},v_{Cf}\right)\sin\left(\omega_s t\right)+f_3\left(i_{rs.1s},i_{rs.1c},v_{Cf}\right)\cos\left(\omega_s t\right), \end{aligned} \tag{2.48}$$

$$i_o'=\left|i_{rs}\right|=f_4\left(i_{rs.1s},i_{rs.1c}\right), \tag{2.49}$$

$$i_{in}=f_5\left(d,i_{r.1s}\right). \tag{2.50}$$

Those nonlinear terms can be expanded to Fourier series and then the EDFs can be obtained as follows:

$$f_0\left(v_{in},d\right)=v_{AB.1s}=\frac{4}{\pi}v_{in}\sin\left(\frac{\pi}{2}d\right), \tag{2.51}$$

$$f_1\left(v_{in},d\right)=v_{AB.1c}=0, \tag{2.52}$$

$$f_2\left(i_{rs.1s}, i_{rs.1c}, v_{Cf}\right) = v_{CD.1s} = -\frac{4}{\pi}\frac{i_{rs.1s}}{\sqrt{{i_{rs.1s}}^2 + {i_{rs.1c}}^2}} v_{Cf}, \tag{2.53}$$

$$f_3\left(i_{rs.1s}, i_{rs.1c}, v_{Cf}\right) = v_{CD.1c} = -\frac{4}{\pi}\frac{i_{rs.1c}}{\sqrt{{i_{rs.1s}}^2 + {i_{rs.1c}}^2}} v_{Cf}, \tag{2.54}$$

$$f_4\left(i_{rs.1s}, i_{rs.1c}\right) = \frac{2}{\pi}\sqrt{{i_{rs.1s}}^2 + {i_{rs.1c}}^2}, \tag{2.55}$$

$$f_5\left(d, i_{r.1s}\right) = \frac{2}{\pi}\sin\left(\frac{\pi}{2}d\right)\cdot i_{r.1s}. \tag{2.56}$$

II.3.4 Harmonic balance

The coefficients of sine and cosine components can be separately obtained by substituting equation (2.39) – (2.46) into equation (2.29) – (2.32). The harmonic balance equations are as follows:

$$v_{AB.1s} = L_p\left(\frac{di_{r.1s}}{dt} - \omega_s i_{r.1c}\right) + i_{r.1s}R_{lp} + v_{C1.1s} + M\left(\frac{di_{rs.1s}}{dt} - \omega_s i_{rs.1c}\right), \tag{2.57}$$

$$v_{AB.1c} = L_p\left(\frac{di_{r.1c}}{dt} + \omega_s i_{r.1s}\right) + i_{r.1c}R_{lp} + v_{C1.1c} + M\left(\frac{di_{rs.1c}}{dt} + \omega_s i_{rs.1s}\right), \tag{2.58}$$

$$i_{r.1s} = C_1\left(\frac{dv_{C1.1s}}{dt} - \omega_s v_{C1.1c}\right), \tag{2.59}$$

$$i_{r.1c} = C_1\left(\frac{dv_{C1.1c}}{dt} + \omega_s v_{C1.1s}\right), \tag{2.60}$$

$$v_{CD.1s} = L_s\left(\frac{di_{rs.1s}}{dt} - \omega_s i_{rs.1c}\right) + i_{rs.1s}R_{ls} + v_{C2.1s} + M\left(\frac{di_{r.1s}}{dt} - \omega_s i_{r.1c}\right), \tag{2.61}$$

$$v_{CD.1c} = L_s\left(\frac{di_{rs.1c}}{dt} + \omega_s i_{rs.1s}\right) + i_{rs.1c}R_{ls} + v_{C2.1c} + M\left(\frac{di_{r.1c}}{dt} + \omega_s i_{r.1s}\right), \tag{2.62}$$

$$i_{rs.1s} = C_2\left(\frac{dv_{C2.1s}}{dt} - \omega_s v_{C2.1c}\right), \tag{2.63}$$

$$i_{rs.1c} = C_2\left(\frac{dv_{C2.1c}}{dt} + \omega_s v_{C2.1s}\right). \tag{2.64}$$

II.3.5 Steady state operation point

When the system is operating in steady state, the derivatives of the state variables will be zero. Therefore, the steady state point solution can be obtained by steady state matrix calculation.

$$V_{AB.1s} = -L_p\Omega_s I_{r.1c} + I_{r.1s}R_{lp} + V_{C1.1s} - M_0\Omega_s I_{rs.1c}, \tag{2.65}$$

$$V_{AB.1c} = L_p\Omega_s I_{r.1s} + I_{r.1c}R_{lp} + V_{C1.1c} + M_0\Omega_s I_{rs.1s}, \tag{2.66}$$

$$I_{r.1s} = -C_1\Omega_s V_{C1.1c}, \tag{2.67}$$

$$I_{r.1c} = C_1\Omega_s V_{C1.1s}, \tag{2.68}$$

$$V_{CD.1s} = -L_s\Omega_s I_{rs.1c} + I_{rs.1s}R_{ls} + V_{C2.1s} - M_0\Omega_s I_{r.1c}, \tag{2.69}$$

$$V_{CD.1c} = L_s\Omega_s I_{rs.1s} + I_{rs.1c}R_{ls} + V_{C2.1c} + M_0\Omega_s I_{r.1s}, \tag{2.70}$$

$$I_{rs.1s} = -C_2\Omega_s V_{C2.1c}, \tag{2.71}$$

$$I_{rs.1c} = C_2\Omega_s V_{C2.1s}, \tag{2.72}$$

$$\frac{1}{R}V_{Cf} = \frac{2}{\pi}\sqrt{I_{rs.1s}{}^2 + I_{rs.1c}{}^2}, \tag{2.73}$$

$$V_o = r_C{}' \cdot \frac{2}{\pi}\sqrt{I_{rs.1s}{}^2 + I_{rs.1c}{}^2} + \frac{r_C{}'}{r_C}\cdot V_{Cf}, \tag{2.74}$$

$$I_{in} = \frac{2}{\pi} I_{r.1s} \sin\left(\frac{\pi}{2} D\right), \tag{2.75}$$

where

$$V_{AB.1s} = \frac{4}{\pi} V_{in} \sin\left(\frac{\pi}{2} D\right), \tag{2.76}$$

$$V_{AB.1c} = 0, \tag{2.77}$$

$$V_{CD.1s} = -I_{rs.1s} R_e, \tag{2.78}$$

$$V_{CD.1c} = -I_{rs.1c} R_e. \tag{2.79}$$

By rearranging the above equations, the steady state matrix can be obtained as follows:

$$X \cdot Y = U_0, \tag{2.80}$$

where

$$Y = \begin{bmatrix} I_{r.1s} & I_{r.1c} & I_{rs.1s} & I_{rs.1c} & V_{C1.1s} & V_{C1.1c} & V_{C2.1s} & V_{C2.1c} \end{bmatrix}^T, \tag{2.81}$$

$$U_0 = \begin{bmatrix} V_{AB.1s} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}^T, \tag{2.82}$$

$$X = \begin{bmatrix} R_{lp} & -L_p\Omega_s & 0 & -M_0\Omega_s & 1 & 0 & 0 & 0 \\ L_p\Omega_s & R_{lp} & M_0\Omega_s & 0 & 0 & 1 & 0 & 0 \\ 0 & -M_0\Omega_s & (R_e + R_{ls}) & -L_s\Omega_s & 0 & 0 & 1 & 0 \\ M_0\Omega_s & 0 & L_s\Omega_s & (R_e + R_{ls}) & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & C_1\Omega_s & 0 & 0 \\ 0 & 1 & 0 & 0 & -C_1\Omega_s & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & C_2\Omega_s \\ 0 & 0 & 0 & 1 & 0 & 0 & -C_2\Omega_s & 0 \end{bmatrix}. \tag{2.83}$$

By matrix calculation, steady state variables $I_{r.1s}$, $I_{r.1c}$, $I_{rs.1s}$, $I_{rs.1c}$, $V_{c1.1s}$, $V_{c1.1c}$, $V_{c2.1s}$, $V_{c2.1c}$ can be obtained by given operation point (V_{in}, D, M_0, Ω_s, R).

II.3.6 Small signal perturbation

Each variable can be separated into a large signal and a small perturbed signal (refer to Appendices). By substituting the above separated signals into harmonic balance equations and eliminating large signals, the following small signal equations can be obtained:

$$\hat{v}_{AB.1s} = \left(L_p - M_0\right)\frac{d\hat{i}_{r.1s}}{dt} + M_0\frac{d\left(\hat{i}_{r.1s} + \hat{i}_{rs.1s}\right)}{dt} + R_{lp}\hat{i}_{r.1s} - L_p\Omega_s\hat{i}_{r.1c} \\ -M_0\Omega_s\hat{i}_{rs.1c} - \left(L_pI_{r.1c} + M_0I_{rs.1c}\right)\hat{\omega}_s - \Omega_sI_{rs.1c}\hat{m} + \hat{v}_{C1.1s}, \tag{2.84}$$

$$\hat{v}_{AB.1c} = \left(L_p - M_0\right)\frac{d\hat{i}_{r.1c}}{dt} + M_0\frac{d\left(\hat{i}_{r.1c} + \hat{i}_{rs.1c}\right)}{dt} + R_{lp}\hat{i}_{r.1c} + L_p\Omega_s\hat{i}_{r.1s} \\ +M_0\Omega_s\hat{i}_{rs.1s} + \left(L_pI_{r.1s} + M_0I_{rs.1s}\right)\hat{\omega}_s + \Omega_sI_{rs.1s}\hat{m} + \hat{v}_{C1.1c}, \tag{2.85}$$

$$\hat{v}_{CD.1s} = \left(L_s - M_0\right)\frac{d\hat{i}_{rs.1s}}{dt} + M_0\frac{d\left(\hat{i}_{r.1s} + \hat{i}_{rs.1s}\right)}{dt} + R_{ls}\hat{i}_{rs.1s} - L_s\Omega_s\hat{i}_{rs.1c} \\ -M_0\Omega_s\hat{i}_{r.1c} - \left(L_sI_{rs.1c} + M_0I_{r.1c}\right)\hat{\omega}_s - \Omega_sI_{r.1c}\hat{m} + \hat{v}_{C2.1s}, \tag{2.86}$$

$$\hat{v}_{CD.1c} = \left(L_s - M_0\right)\frac{d\hat{i}_{rs.1c}}{dt} + M_0\frac{d\left(\hat{i}_{r.1c} + \hat{i}_{rs.1c}\right)}{dt} + R_{ls}\hat{i}_{rs.1c} + L_s\Omega_s\hat{i}_{rs.1s} \\ +M_0\Omega_s\hat{i}_{r.1s} + \left(L_sI_{rs.1s} + M_0I_{r.1s}\right)\hat{\omega}_s + \Omega_sI_{r.1s}\hat{m} + \hat{v}_{C2.1c}, \tag{2.87}$$

$$\hat{i}_{r.1s} = C_1\frac{d\hat{v}_{C1.1s}}{dt} - C_1\Omega_s\hat{v}_{C1.1c} - C_1V_{C1.1c}\hat{\omega}_s, \tag{2.88}$$

$$\hat{i}_{r.1c} = C_1\frac{d\hat{v}_{C1.1c}}{dt} + C_1\Omega_s\hat{v}_{C1.1s} + C_1V_{C1.1s}\hat{\omega}_s, \tag{2.89}$$

$$\hat{i}_{rs.1s} = C_2\frac{d\hat{v}_{C2.1s}}{dt} - C_2\Omega_s\hat{v}_{C2.1c} - C_2V_{C2.1c}\hat{\omega}_s, \tag{2.90}$$

$$\hat{i}_{rs.1c} = C_2\frac{d\hat{v}_{C2.1c}}{dt} + C_2\Omega_s\hat{v}_{C2.1s} + C_2V_{C2.1s}\hat{\omega}_s, \tag{2.91}$$

$$\hat{v}_o = K_1 r_C' \cdot \hat{i}_{rs.1s} + K_2 r_C' \cdot \hat{i}_{rs.1c} + \frac{r_C'}{r_C} \cdot \hat{v}_{Cf} + r_C' \hat{i}_{load}, \tag{2.92}$$

$$\hat{i}_{in} = J_2 \cdot \hat{i}_{r.1s} + J_1 \cdot \hat{d}, \tag{2.93}$$

where

$$\hat{v}_{AB.1s} = P_1 \cdot \hat{v}_{in} + P_2 \cdot \hat{d}, \tag{2.94}$$

$$\hat{v}_{AB.1c} = 0, \tag{2.95}$$

$$\hat{v}_{CD.1s} = H_1 \cdot \hat{i}_{rs.1s} + H_2 \cdot \hat{i}_{rs.1c} + H_3 \cdot \hat{v}_{Cf}, \tag{2.96}$$

$$\hat{v}_{CD.1c} = G_1 \cdot \hat{i}_{rs.1s} + G_2 \cdot \hat{i}_{rs.1c} + G_3 \cdot \hat{v}_{Cf}, \tag{2.97}$$

and K_1, K_2, J_1, J_2, P_1, P_2, H_1, H_2, H_3, G_1, G_2, G_3 are defined in Appendices.

II.3.7 Small-signal equivalent circuit

By analyzing (2.84) – (2.97), equivalent circuit of the small signal model can be obtained as shown in Fig. II-8. Also, by rearranging (2.84) – (2.97), state-space model of the DC-DC WPT resonant converter can be calculated in matrix form:

$$\frac{d\hat{x}}{dt} = A\hat{x} + B\hat{u},\ \hat{y} = C\hat{x} + D\hat{u}, \tag{2.98}$$

where state variables, control and disturbance inputs, and outputs are:

$$\hat{x} = \begin{bmatrix} \hat{i}_{r.1s} & \hat{i}_{r.1c} & \hat{i}_{rs.1s} & \hat{i}_{rs.1c} & \hat{v}_{C1.1s} & \hat{v}_{C1.1c} & \hat{v}_{C2.1s} & \hat{v}_{C2.1c} & \hat{v}_{Cf} \end{bmatrix}^T, \tag{2.99}$$

$$\hat{u} = \begin{bmatrix} \hat{\omega}_s & \hat{v}_{in} & \hat{d} & \hat{m} & \hat{i}_{load} \end{bmatrix}^T, \tag{2.100}$$

$$\hat{y} = \begin{bmatrix} \hat{v}_o & \hat{i}_{in} \end{bmatrix}^T. \tag{2.101}$$

And matrix *A*, *B*, *C*, and *D* are defined as the coefficients of the state-space model and obtained as shown in Appendices.

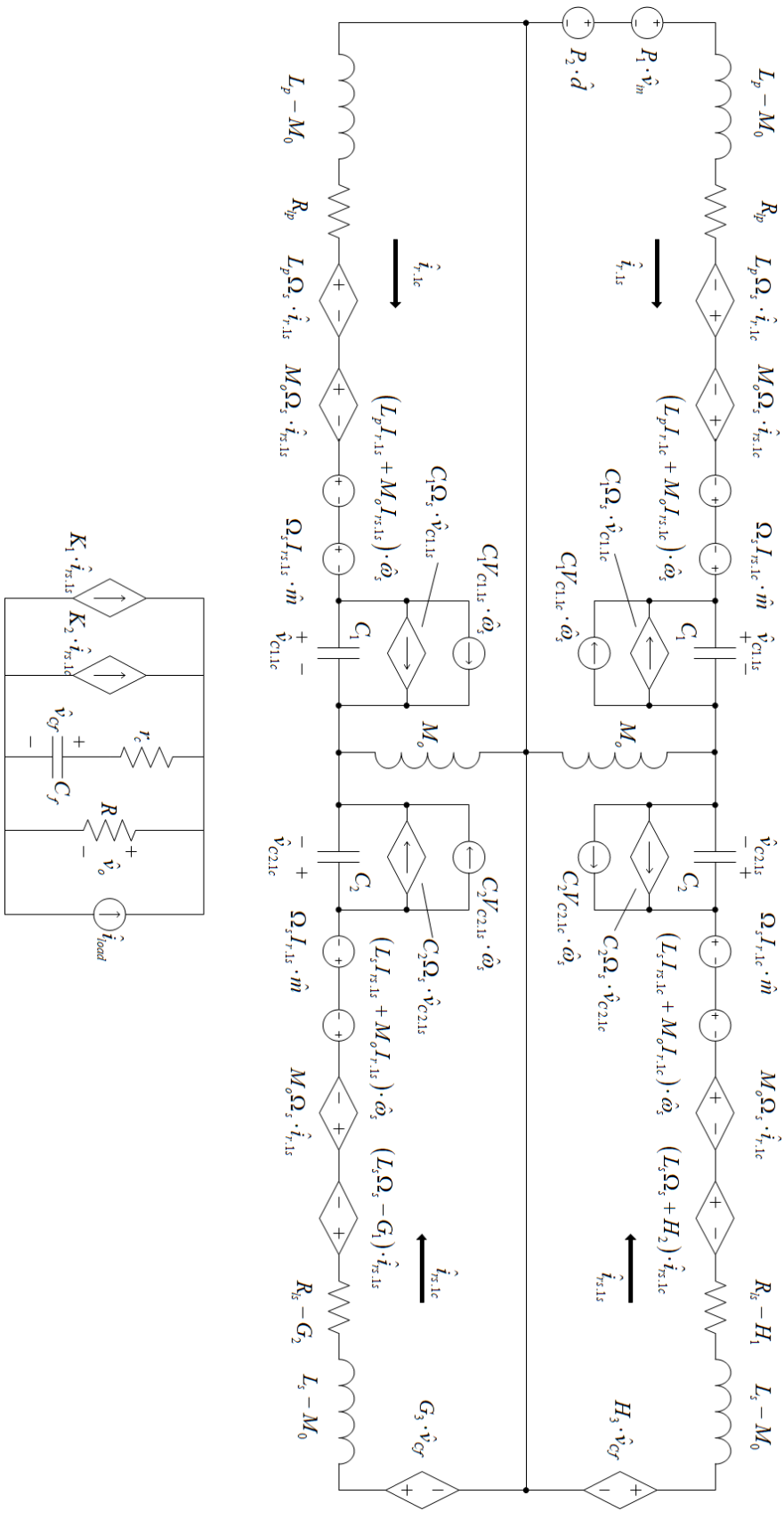


Fig. II-8. Equivalent circuit of small signal model

II.4 Design Example

II.4.1 System requirement

A high power closed-loop DC-DC resonant converter for wireless power transfer is designed and implemented. DC input voltage ranges from 265 V to 335 V. The output voltage is designed to be 350 V with rated output power 3.5 kW. This system is designed to verify the steady-state analysis and small-signal analysis of DC-DC WPT resonant converter.

II.4.2 Parameters design

In order to make the converter more load-independent, operating frequency is designed to be near and larger than the load-independent frequency. In the operating area, the DC-DC voltage gain decreases with frequency increasing. Therefore, at the load-independent frequency, the DC-DC voltage gain, also the ideal transformer ratio n_e in Fig. II-2, is designed to be:

$$n_e \geq 350/265=1.32. \tag{2.102}$$

For the design of the coils, the relationship between them is

$$L_s = n_e^{\,2} \cdot L_p. \tag{2.103}$$

Therefore, the parameters of the coils and capacitors are designed as follows:

$$\begin{aligned} &L_p = 70.5\mu H, L_s = 125.5\mu H, M = 19\mu H, C_1 = 14.6nF, C_2 = 8.2nF, \\ &n_e^{\,2} = \frac{125.5}{70.5} = 1.78 \Rightarrow n_e = 1.334, \\ &L_1 = L_p - M/n_e = 56.26\mu H, L_2 = L_s - M \cdot n_e = 100.15\mu H. \end{aligned} \tag{2.104}$$

Therefore, the load-independent frequency is obtained:

$$f_2 = \frac{1}{2\pi\sqrt{L_1 C_1}} = \frac{1}{2\pi\sqrt{L_2 C_2}} = 175.6kHz. \tag{2.105}$$

In the converter, the aligning distance between primary coil and secondary coil is set to be 200mm and then their mutual inductance is 19 μH. However, because of coils misalignment and distance variation, the mutual inductance will vary, assuming that the mutual inductance varies from 17 μH to 21 μH. The designed output voltage is 350 V with rated output power 3.5 kW, so the rated load resistance is 35 Ω. Here the minimum output power is limited to be 1.75 kW, so the maximum load resistance is 70 Ω.

II.4.3 DC operating point

With the above parameters, curves of relationship between voltage and frequency can be obtained. In Fig. II-9, there are 6 relation curves, referring to 6 different conditions. When the input voltage is 265 V, the needed normalized voltage gain is 0.99. When the input voltage is 335 V, the needed normalized voltage gain is 0.783. Therefore, the range of normalized voltage needed for operation is set to be 0.78 ~ 1. Hence, the normalized operation frequency ranges from 0.987 to 1.05.

II.4.4 Close loop compensation design

Using extended describing function method (EDF) [121], small signal model of the converter can be derived. Fig. II-10 shows the bode plot of calculated control to output transfer function by MATLAB and Fig. II-11 shows the simulated bode plot by PSIM. Here, the DC operation condition is:

$$M = 19\mu H, V_{in} = 265V, R = 35\Omega, f_s = 175.6kHz. \quad (2.106)$$

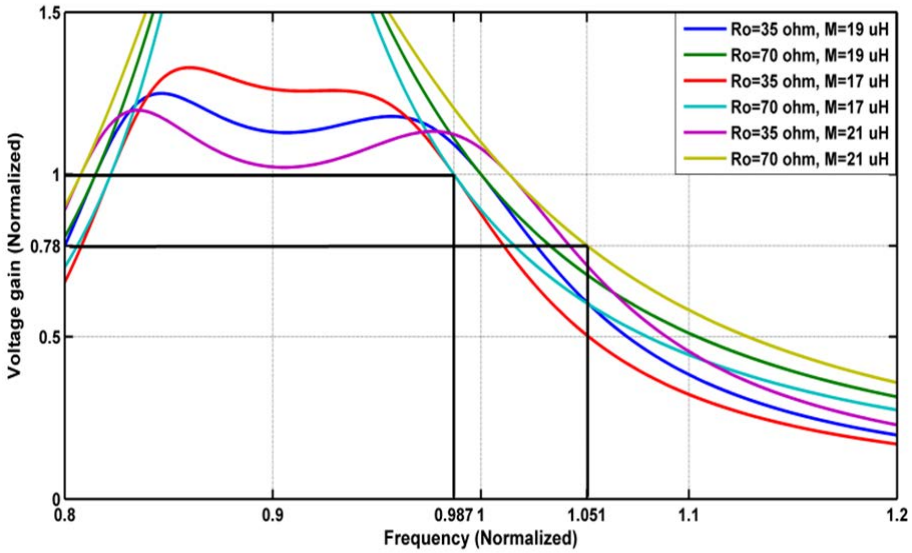


Fig. II-9. DC voltage gain in different conditions

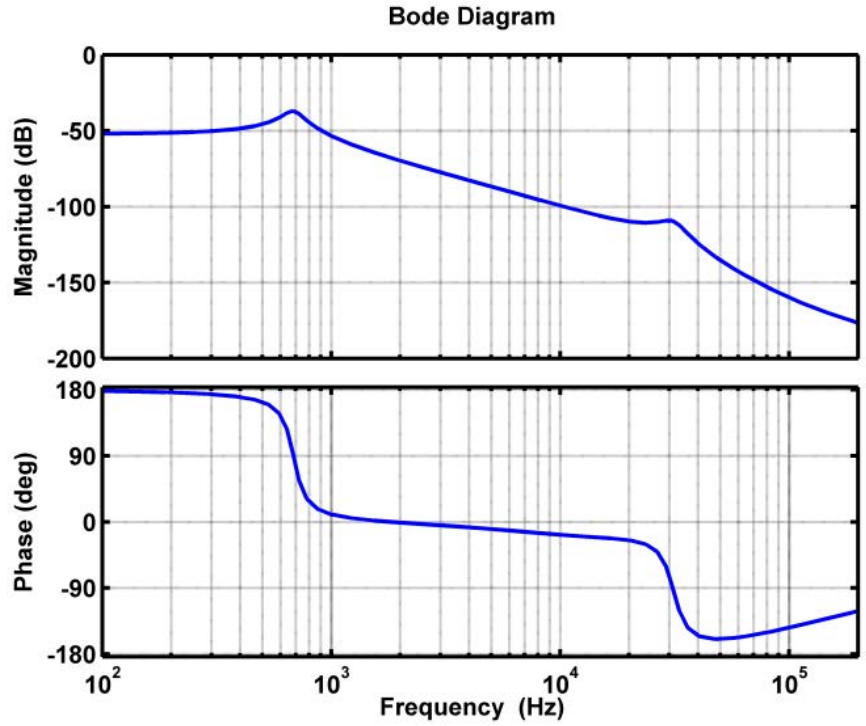


Fig. II-10. Bode plot of calculated control to output transfer function by Matlab

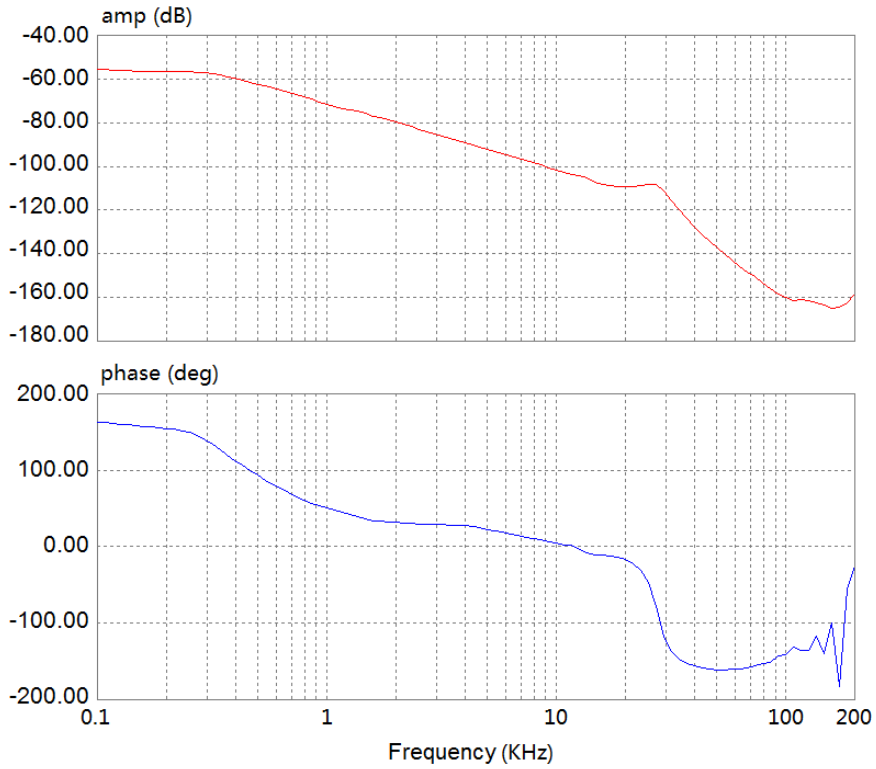


Fig. II-11. Simulated bode plot from control to output by PSIM

Fig. II-12 shows the close loop control system of the DC-DC resonant converter with a type III compensation network [122]. In this system, controller IC L6599 is adopted to adjust the frequency in order to control the output voltage. Applying type III compensation network, the new transfer function of the system in open loop is shown in (2.134). Here, $G_{\omega\text{-}v}$ is the control to output transfer function obtained in section II.3. $G_{c\text{-}\omega}$ is the transfer function of controller IC L6599 and Mosfets Driver. G_o is the transfer function of the original system without compensation in open loop. G_c is the transfer function of the compensation circuit.

$$G_o \cdot G_c = G_{\omega-v} \cdot \frac{R_{d2}}{R_{d1}+R_{d2}} \cdot \frac{R_{d3}}{R_{d3}+R_{d4}} \cdot G_{c-\omega} \cdot \frac{\left(1+sR_{c2}C_{c1}\right)\left[1+s\left(R_{c1}+R_{c3}\right)C_{c3}\right]}{\left[sR_{c1}\left(C_{c1}+C_{c2}\right)\right]\left(1+s\frac{R_{c2}C_{c1}C_{c2}}{C_{c1}+C_{c2}}\right)\left(1+sR_{c3}C_{c3}\right)}. \quad (2.107)$$

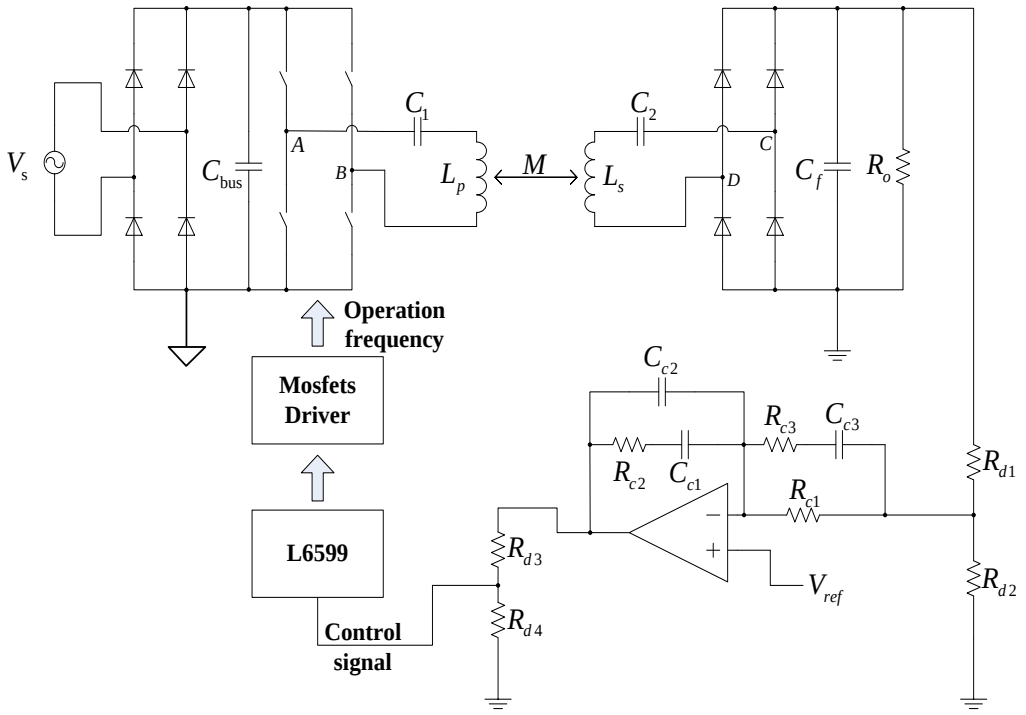


Fig. II-12. Proposed DC-DC converter with type III compensation network

By calculation, the values of the compensator and voltage divider are given in Table II-I.

TABLE II-1 Values of the compensator and voltage divider

Parameter	Values	Parameter	Values
R_{d1}	80 kΩ	R_{c2}	63.4 kΩ
R_{d2}	20 kΩ	R_{c3}	10 Ω
R_{d3}	91 kΩ	C_{c1}	5.6 nF
R_{d4}	10 kΩ	C_{c2}	5 pF
R_{c1}	10 kΩ	C_{c3}	33 nF

In Fig. II-13, the bode plot of the new transfer function of the system in open loop is presented. The gain margin and phase margin are 9.74 dB and 68.1 deg, respectively. The system with compensation is stable with good dynamic response.

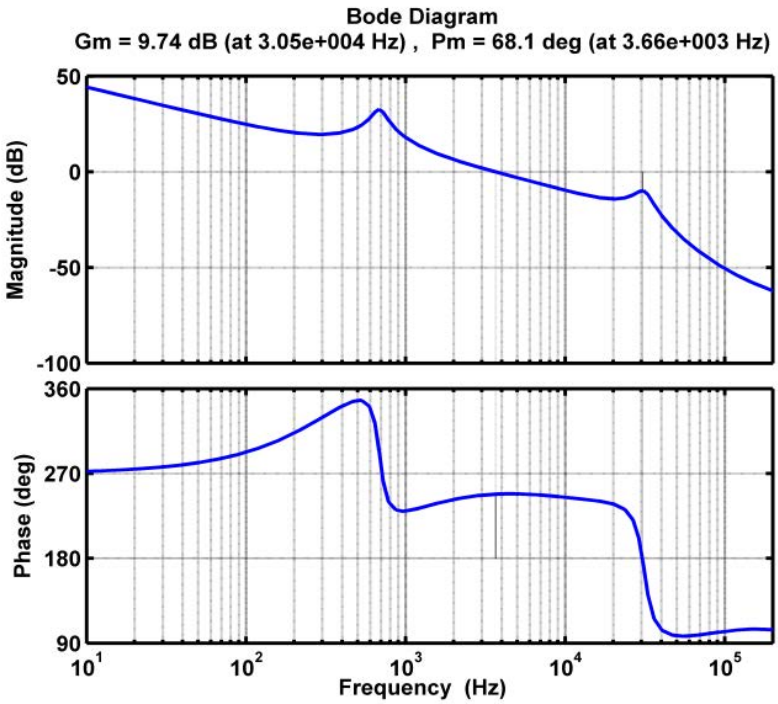


Fig. II-13. Bode plot of the system in open loop with compensation

II.5 Conclusion

In this chapter, DC-DC WPT resonant converters are introduced and studied. Firstly, topologies of WPT resonant tank are introduced, specifically for SS and SP topologies. Secondly, steady-state analysis of DC-DC WPT resonant converters is given and small-signal analysis of DC-DC WPT resonant converter with SS topology is presented in detail. Finally, a design example of the converter with closed-loop control is given and verified by simulation results.

Chapter III

Single-phase Single-stage AC-DC Wireless-Power-Transfer Resonant Converter with Front-end Bridgeless Boost Power-Factor-Correction Rectifier

III.1 Introduction

A conventional WPT system consists of a single-phase electric power supply, a full-bridge rectifier, a boost power factor corrector (PFC), a dc bus capacitor, a high-frequency inverter, coupled primary and secondary resonant tanks, a secondary high-frequency rectifier-bridge, a filter capacitor and a load resistor, as shown in Fig. III-1. A traditional AC-DC converter with power factor correction usually employs a two-stage topology. The first stage is a boost PFC converter and the second is a DC-DC conversion stage. Like the WPT system in Fig. III-1, the first stage includes a full-bridge rectifier and a boost PFC, and the second stage is a DC-DC WPT resonant converter. Generally such two-stage topology cannot achieve the highest efficiency due to more power losses in two-stage conversion while it is also not the most economical as more components would be required too. In recent years, single-stage topologies [93], [94] that integrate both PFC and DC-DC conversion into one power conversion stage have been proposed to overcome the aforementioned drawbacks. Most existing researches are mainly focused on applying single-stage topologies in full -bridge converter [95], half-bridge converter [96], LLC converter [97] – [99], forward converter [100], flyback converter [101], [103], and so on, with most of them designed for low power applications. In this thesis, a novel single-stage topology is proposed and

applied to high power WPT systems with improved efficiency and lower cost. Furthermore, based on this single-stage technique, bridgeless boost PFC rectifiers [104] – [107] are introduced and integrated in the WPT system. Bridgeless boost PFC rectifiers would have less conduction loss due to less number of semiconductor devices being involved. Therefore, the newly proposed converter can further reduce losses and cost while the high performance of the PFC function can be maintained. Compared to the single-stage Z-source resonant converter proposed in [123] for WPT application, the newly proposed converter is advantageous in terms of efficiency and number of semiconductor devices and passive components.

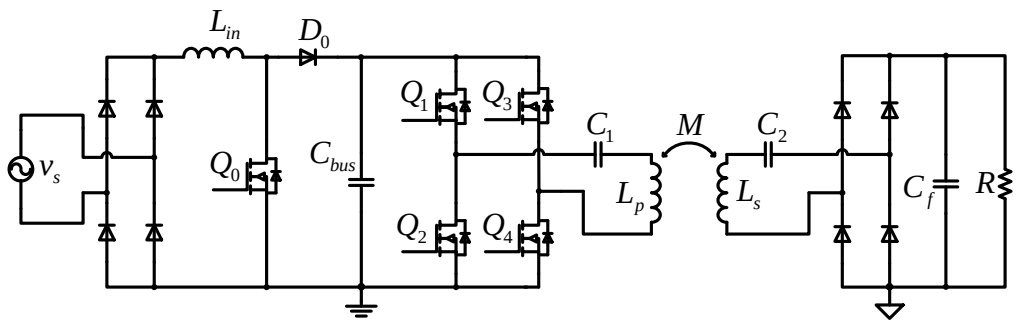


Fig. III-1. Conventional AC-DC WPT resonant converter with boost PFC

In this chapter, the topology description and analysis, power factor (PF) and total harmonics distortion (THD) analysis, modulation method and circuit operation of the proposed converter with a new control approach are first presented, and then, the design procedure with an example is proposed. Finally, an experimental prototype is implemented to verify the analysis and design.

III.2 Proposed Single-Stage Topology

III.2.1 Circuit Description

Fig. III-2 shows the proposed novel topology – single-stage WPT resonant

converter with bridgeless boost PFC rectifier, which ultimately integrates the front-end full-bridge rectifier, boost PFC, and full-bridge inverter in the primary side together. v_s is ac input voltage, D_{R1} and D_{R2} are front-end bridgeless rectifier diodes, L_{in} is input inductor, C_{bus} is bus capacitor, Q_1 – Q_4 are four MOSFET switches (with body diodes D_1 – D_4), C_{s1} – C_{s4} are snubber capacitors of the switches, C_1 and C_2 are capacitors of primary and secondary resonant tanks, L_p and L_s are inductors of primary and secondary resonant tanks, M is mutual inductance of L_p and L_s, D_{s1} – D_{s4} are secondary-side rectifier diodes, C_f is output filtering capacitor, and R is load resistor. Compared with the conventional topology in Fig. III-1, a half bridge of the full-bridge rectifier, the switch Q_0, and the diode D_0 (totally four semiconductor devices) are eliminated. In the proposed topology, Q_1 and Q_2 perform two functions: (a) realization of PFC: they act as D_0 and Q_0 for PFC as shown in Fig. III-1; and (b) combination with Q_3 and Q_4 to form the full-bridge inverter of the DC-DC WPT resonant converter.

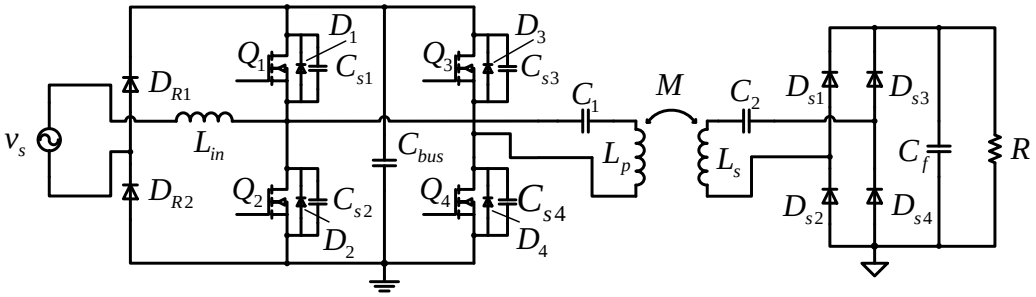


Fig. III-2. Proposed novel topology – Single-stage WPT resonant converter with front-end bridgeless boost PFC rectifier

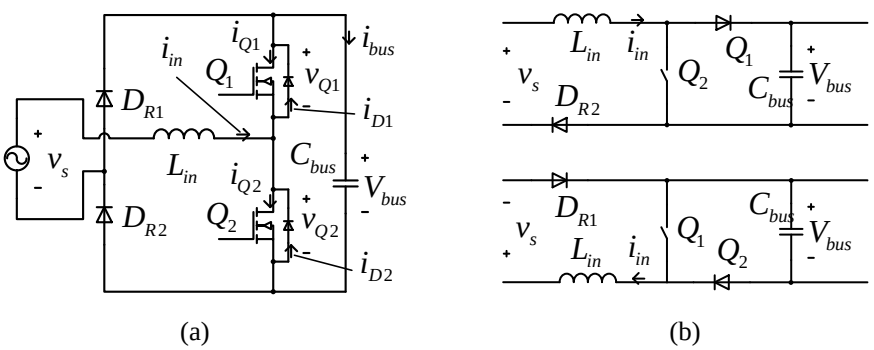


Fig. III-3. Bridgeless boost PFC rectifier

III.2.2 Bridgeless Boost Power-Factor-Correction rectifier

Fig. III-3 (a) shows the bridgeless boost PFC rectifier of the proposed topology, which consists of rectifier diodes D_{R1} and D_{R2}, input inductor L_{in}, half bridge switches Q_1 and Q_2, and bus capacitor C_{bus}. Fig. III-3 (b) shows the operations in positive and negative line cycle. In fact, whenever in positive or negative line cycle, the bridgeless boost PFC rectifier can act as a boost converter to fulfill PFC function. Here upper equivalent circuit in Fig. III-3 (b) is taken as an example to analyze its characteristics.

A. Working Principle and Analysis

As shown in Fig. III-4, the input inductor must work in discontinuous conduction mode (DCM) in order to reduce the higher-order harmonics in the line current [96], [97], [101], and [108]. When switch Q_2 is on, voltage across L_{in} is v_s, and the input current i_{in} flowing through L_{in} is given by:

$$\frac{di_{in}}{dt} = \frac{v_s}{L_{in}}. \tag{3.1}$$

When Q_2 is off, v_{Q2} is equal to V_{bus} (bus voltage) and the voltage across L_{in} is v_s-V_{bus}, then i_{in} is given by:

$$\frac{di_{in}}{dt} = \frac{(v_s - V_{bus})}{L_{in}}. \tag{3.2}$$

For a complete cycle of switching period T_s, i_{in} is expressed as:

$$i_{in} = \begin{cases} \dfrac{v_s}{L_{in}} \cdot t & t \in [t_0, t_1) \\ \dfrac{V_{bus}}{L_{in}} \cdot (t_1 - t_0) - \dfrac{V_{bus} - v_s}{L_{in}} \cdot t & t \in [t_1, t_2), \\ 0 & t \in [t_2, t_3] \end{cases} \tag{3.3}$$

where t_0-t_3 are defined as (D_g is duty cycle of the switch):

$$t_0 = 0, t_1 = D_g T_s, t_2 = D_g T_s \left(V_{bus} / \left(V_{bus} - v_s \right) \right), t_3 = T_s. \tag{3.4}$$

To make input inductor work in DCM, t_2 must be smaller than or equal to t_3, which means (peak value of v_s noted as V_{sp}):

$$D_g T_s \left(V_{bus} / \left(V_{bus} - v_s \right) \right) \le T_s \Rightarrow V_{sp} / V_{bus} \le 1 - D_g. \tag{3.5}$$

Therefore, the average input power in a switching period T_s is:

$$P_T(t) = \left(\int_{t_0}^{t_3} v_s(t) i_{in} dt \right) / T_s = \frac{D_g{}^2 v_s(t)^2 T_s V_{bus}}{2 L_{in} \left(V_{bus} - v_s(t) \right)}. \tag{3.6}$$

For a line cycle, the average input power is:

$$P_{in} = \left[\int_0^{T_l} P_T(t) dt \right] / T_l = \frac{D_g{}^2 V_{sp}{}^2}{2\pi L_{in} f_s} \int_0^{\pi} \frac{(\sin\alpha)^2}{1 - m\sin\alpha} d\alpha, \tag{3.7}$$

where T_l is line period, and m is V_{sp}/V_{bus}.

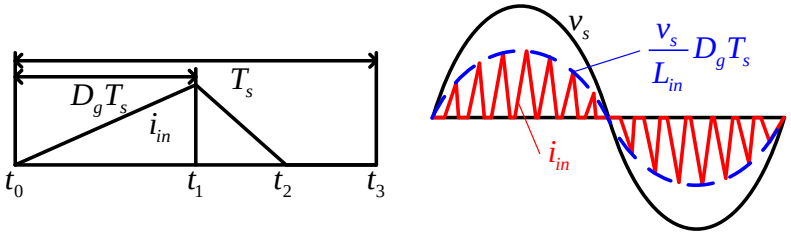


Fig. III-4. Waveforms of input current

B. Analysis of PF and THD_i

The average value of i_{in} during a switching period is given as:

$$i_{in.avg} = \frac{1}{T_s} \int_0^{T_s} i_{in} dt = D_g{}^2 \cdot \frac{V_{sp}}{2 L_{in} f_s} \cdot \frac{\sin(\omega_l t)}{1 - m\left|\sin(\omega_l t)\right|}, \tag{3.8}$$

where ω_l is line frequency in radian. Because of the symmetric characteristics for both positive and negative half cycles of v_s, the root-mean-square (RMS) values of input current i_{in} for positive and negative half cycles of v_s are equal. Therefore, the

RMS value of input current i_{in} for T_l is as follows:

$$i_{in.\mathrm{rms}} = \frac{D_g{}^2 V_{sp}}{2\sqrt{\pi} L_{in} f_s} \sqrt{\int_0^{\pi} \frac{(\sin\alpha)^2}{(1-m|\sin\alpha|)^2} d\alpha}. \tag{3.9}$$

Therefore, the PF of the proposed converter is obtained:

$$\mathrm{PF} = \left(\sqrt{2} \int_0^{\pi} \frac{(\sin\alpha)^2}{1-m\sin\alpha} d\alpha \right) \Bigg/ \left(\sqrt{\pi} \sqrt{\int_0^{\pi} \frac{(\sin\alpha)^2}{(1-m\sin\alpha)^2} d\alpha} \right). \tag{3.10}$$

From (3.10), the PF of the proposed converter is only related to m (equal to V_{sp}/V_{bus}), as shown in Fig. III-5 (curve in blue). For $\mathrm{THD_i}$ (THD of input current i_{in}) analysis, $i_{in.\mathrm{avg}}$ can be expressed as Fourier series:

$$i_{in.\mathrm{avg}}(t) = b_1 \sin(\omega_l t) + b_3 \sin(3\omega_l t) + b_5 \sin(5\omega_l t) + \cdots, \tag{3.11}$$

$$b_n = (2/T_l) \int_0^{T_l} i_{in.avg}(t) \sin(n\omega_l t)\, dt \quad n = 1,3,5,..., \tag{3.12}$$

and $\mathrm{THD_i}$ can be obtained:

$$\mathrm{THD_i} = \sqrt{b_3{}^2 + b_5{}^2 + b_7{}^2 + \cdots} / b_1. \tag{3.13}$$

By analysis and calculation, $\mathrm{THD_i}$ is also only related to m value, as shown in Fig. III-5 (curve in green).

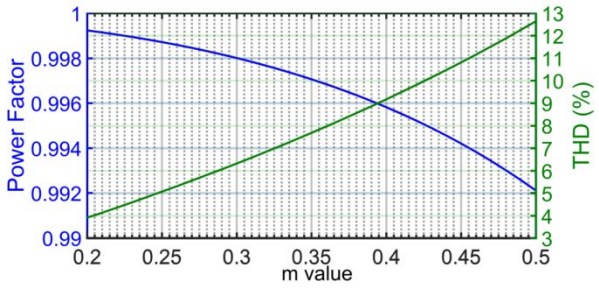


Fig. III-5. Relations of m value vs PF and $\mathrm{THD_i}$

III.2.3 Circuit Operation

The proposed modulation and operation waveforms are shown in Fig. III-6. Duty cycles of v_{g1} and v_{g2} are noted as D_{g1} and D_{g2}, respectively. Duty cycles of v_{g1} and v_{g2} are complementary, so are those of v_{g3} and v_{g4}. When v_s is in its positive cycle, D_{g2} is equal to D_g' and v_{g4} leads v_{g2} half a switching period; when v_s is in its negative cycle, D_{g1} is equal to D_g' and v_{g3} lags v_{g1} half a switching period. In an ideal condition, D_g' is equal to D_g. However, in practical implementation considering dead time, D_g' is smaller than D_g. Such modulation method generates a three-level voltage with an adjustable duty cycle. For operation analysis, the proposed topology is simplified to an equivalent circuit shown in Fig. III-7.

Stage 1 (t_0 – t_{a1}): From t_0 to t_{a1}, Q_1 and Q_3 are on while Q_2 and Q_4 are off. Current flows through v_s, L_{in}, Q_1, C_{bus}, D_{R2}, Q_3, and Z_r, as shown in Fig. III-8 (a).

Stage 2 (t_{a1} – t_{a4}): At t_{a1}, Q_3 is turned off; C_{s3} starts to be charged and C_{s4} starts to be discharged. From t_{a1} to t_{a3}, current flows through v_s, L_{in}, Q_1, C_{bus}, D_{R2}, C_{s3}, C_{s4}, and Z_r, as shown in Fig. III-8 (b). At t_{a3}, C_{s3} is charged to V_{bus} and C_{s4} is discharged to zero. From t_{a3} to t_{a4}, current flows through v_s, L_{in}, Q_1, C_{bus}, D_{R2}, D_4, and Z_r, as shown in Fig. III-8 (c).

Stage 3 (t_{a4} – t_{b1}): At t_{a4}, Q_4 is turned on. From t_{a4} to t_{b1}, Q_1 and Q_4 are on while Q_2 and Q_3 are off. At t_1, input current i_{in} reaches zero. From t_{a4} to t_1, current flows through v_s, L_{in}, Q_1, C_{bus}, D_{R2}, Q_4, and Z_r, as shown in Fig. III-8 (d). At t_2, i_r changes polarity from negative to positive. From t_1 to t_{b1}, current flows through Q_1, C_{bus}, Q_4, and Z_r, as shown in Fig. III-8 (e) and (f).

Stage 4 (t_{b1} – t_{b4}): At t_{b1}, Q_4 is turned off; C_{s3} and C_{s4} start to be discharged and charged respectively. From t_{b1} to t_{b3}, current flows through Q_1, Z_r, C_{s3}, C_{s4}, and C_{bus}, as shown in Fig. III-8 (g). At t_{b3}, voltages of C_{s3} and C_{s4} reach zero and V_{bus}. From t_{b3} to t_{b4}, current flows through Q_1, Z_r, and D_3, as shown in Fig. III-8 (h).

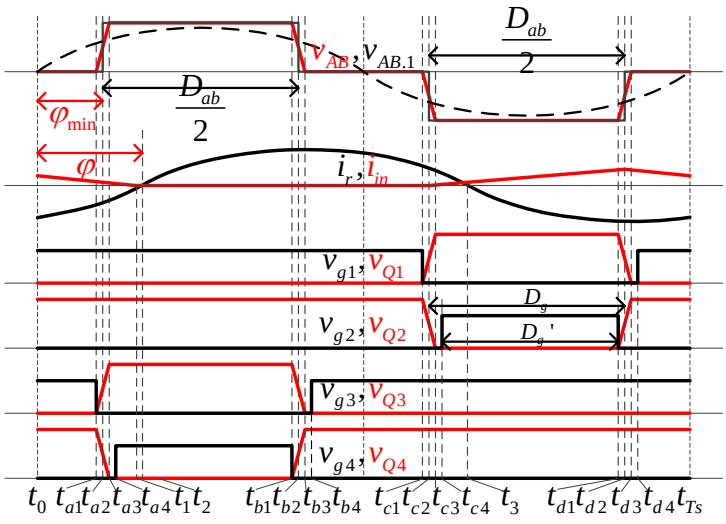
Stage 5 (t_{b4} – t_{c1}): At t_{b4}, Q_3 is turned on. From t_{b4} to t_{c1}, Q_1 and Q_3 are on while Q_2 and Q_4 are off. Current flows through Q_1, Z_r, and Q_3, as shown in Fig. III-8 (i).

Stage 6 (t_{c1} – t_{c4}): At t_{c1}, Q_1 is turned off; C_{s1} and C_{s2} start to be charged and discharged respectively. From t_{c1} to t_{c3}, current flows through C_{s1}, C_{s2}, Z_r, Q_3, and C_{bus}, as shown in Fig. III-8 (j). At t_{c2}, i_{in} starts to increase from zero. From t_{c2} to t_{c3}, current flows through v_s, L_{in}, C_{s1}, C_{s2}, Z_r, Q_3, C_{bus}, and D_{R2}, as shown in Fig. III-8 (k). At t_{c3}, C_{s1} is charged to V_{bus} and C_{s2} is discharged to zero. From t_{c3} to t_{c4}, current flows through v_s, L_{in}, D_2, Z_r, Q_3, C_{bus}, and D_{R2}, as shown in Fig. III-8 (l).

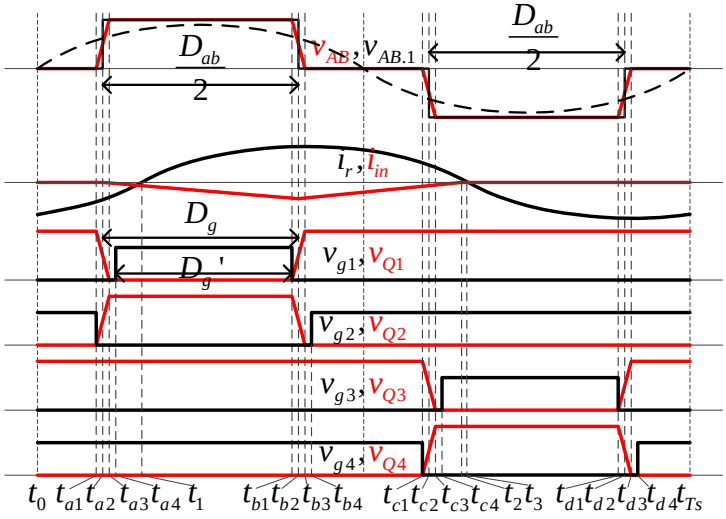
Stage 7 (t_{c4} – t_{d1}): At t_{c4}, Q_2 is turned on. From t_{c4} to t_{d1}, Q_2 and Q_3 are on while Q_1 and Q_4 are off. Current flows through v_s, L_{in}, Q_2, Z_r, Q_3, C_{bus}, and D_{R2}, as shown in Fig. III-8 (m) and (n). At t_3, i_r changes polarity from positive to negative.

Stage 8 (t_{d1} – t_{d4}): At t_{d1}, Q_2 is turned off; C_{s1} starts to be discharged and C_{s2} starts to be charged. From t_{d1} to t_{d3}, current flows through v_s, L_{in}, C_{s1}, C_{s2}, C_{bus}, Q_3, Z_r, and D_{R2}, as shown in Fig. III-8 (o). At t_{d3}, C_{s1} is discharged to zero and C_{s2} is charged to V_{bus}. From t_{d3} to t_{d4}, current flows through v_s, L_{in}, D_1, V_{bus}, D_{R2}, Q_3, and Z_r, as shown in Fig. III-8 (p).

Stage 9 (t_{d4} – t_{Ts}): At t_{d4}, Q_1 is turned on, and this stage is the same with Stage 1, as shown in Fig. III-8 (q).



(a)



(b)

Fig. III-6. Operation waveforms of the proposed modulation method: (a) when v_s is in its positive cycle; (b) when v_s is in its negative cycle

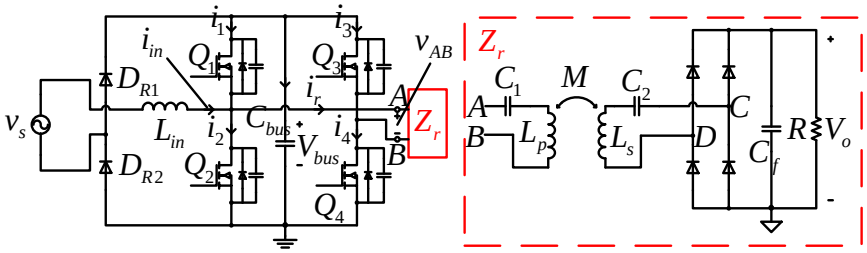


Fig. III-7. Equivalent circuit of the proposed topology with resonant tank and secondary side equivalent to impedance Z_r

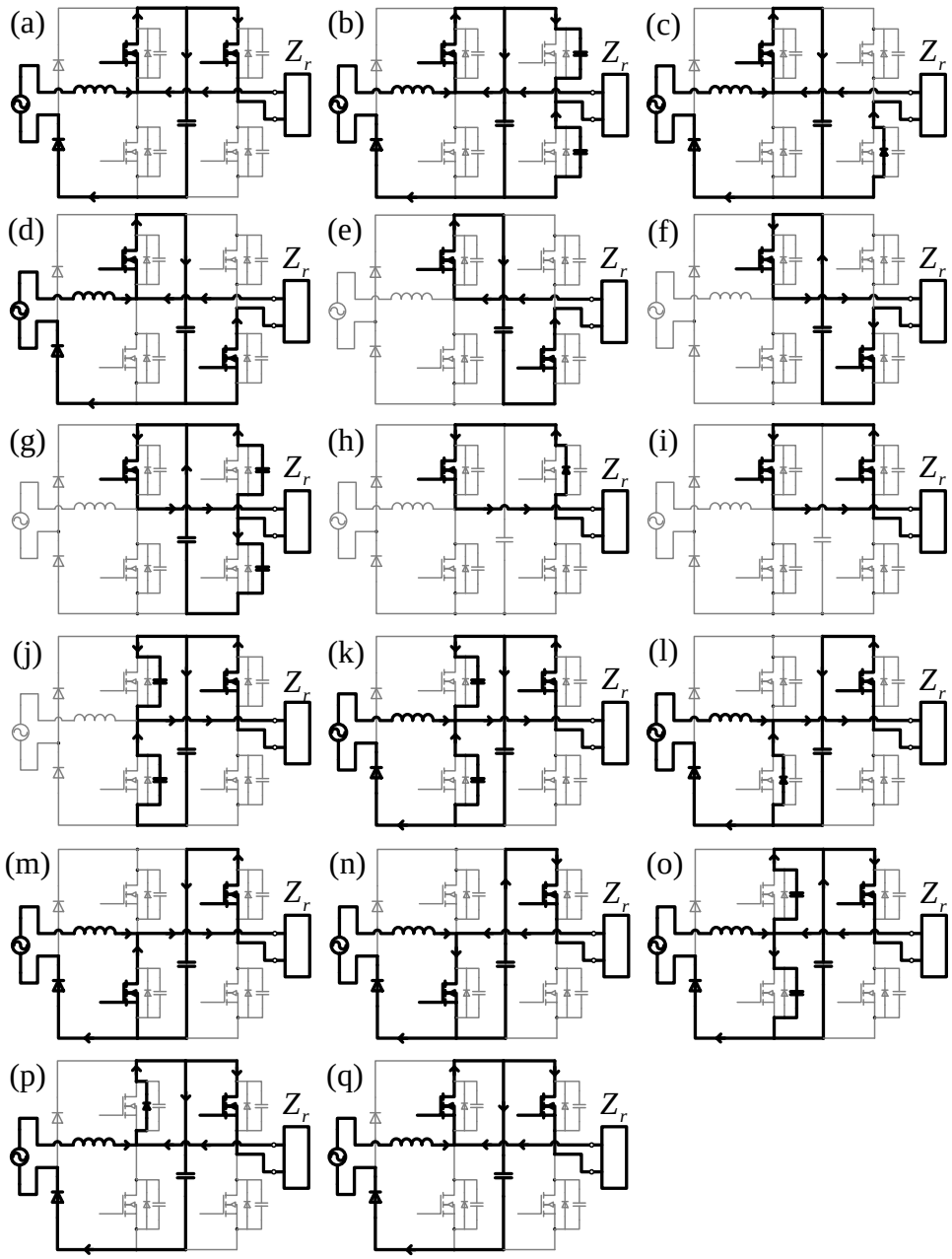


Fig. III-8. Operation modes during a switching period for positive half cycle of input line voltage v_s

III.3 Control method for the proposed topology

Usually frequency control methods are applied in variable kinds of resonant converters. However, frequency control method is not suitable for the proposed topology. By analysis, if D_{ab} is set constantly at 1, by increasing operation

frequency f_s, P_{in} and P_o will be regulated to low level. However, such regulation will lead to very large V_{bus}, usually larger than 1 kV, which requires bus capacitor and all primary-side semiconductor devices with high voltage rating and causes severe EMI problem because of high dv/dt.

Here a control approach for constant output voltage with soft-switching is proposed and can allow the proposed converter to work in a wide-range load condition with high performances (high efficiency, low THD, and high PF). In the proposed control method, D_{ab} is the control parameter to regulate output power with constant V_o when load varies, with f_s kept constant within the optimal range of the resonant tank. Make $D_g = D_{ab}/2$, then P_{in} and P_o are amended as:

$$P_{in} = \frac{{D_{ab}}^2 {V_{sp}}^2}{8\pi f_s L_{in}} \int_0^{\pi} \frac{(\sin\theta)^2}{1 - m\sin\theta} d\theta. \tag{3.14}$$

$$P_o = \frac{8{V_o}^2}{\pi^2} \cdot \frac{\sqrt{\left(\frac{V_{bus}}{V_o}\sin\left(\frac{D_{ab}\pi}{2}\right)\right)^2 - \left(\frac{\omega_s L_p - 1/(\omega_s C_1)}{\omega_s M}\right)^2}}{\left|\frac{(\omega_s L_p - 1/(\omega_s C_1))(\omega_s L_s - 1/(\omega_s C_2))}{\omega_s M} - \omega_s M\right|} \tag{3.15}$$

P_{in} and P_o can be easily regulated to low level by adjusting D_{ab} and will not cause very high bus voltage. Therefore, such control method is applied to give a wide-range load regulation.

In order to realize soft-switching of all the four switches in the proposed converter with the proposed modulation method, operation frequency f_s should be selected properly. Firstly, by analyzing the operation of the converter, $i_1 - i_4$, as defined and shown in Fig. III-7, should be positive at the instances of $Q_1 - Q_4$ turning-off, respectively, so as to achieve soft-switching in all four switches. Therefore, phase difference of $v_{AB.1}$ and i_r (defined as φ) must satisfy the following:

$$\varphi > \left[(1 - D_{ab})/2\right]\pi. \tag{3.16}$$

From (2.1) – (2.3), φ only varies with equivalent load resistance R_e (if operation frequency f_s is confirmed):

$$\varphi = \angle\frac{v_{AB}}{i_r} = \angle\frac{v_i}{i_r} = \angle\left(j\omega_s L_p - \frac{j}{\omega_s C_1} + \frac{\omega_s^2 M^2}{j\omega_s L_s - j/(\omega_s C_2) + R_e} \right). \quad (3.17)$$

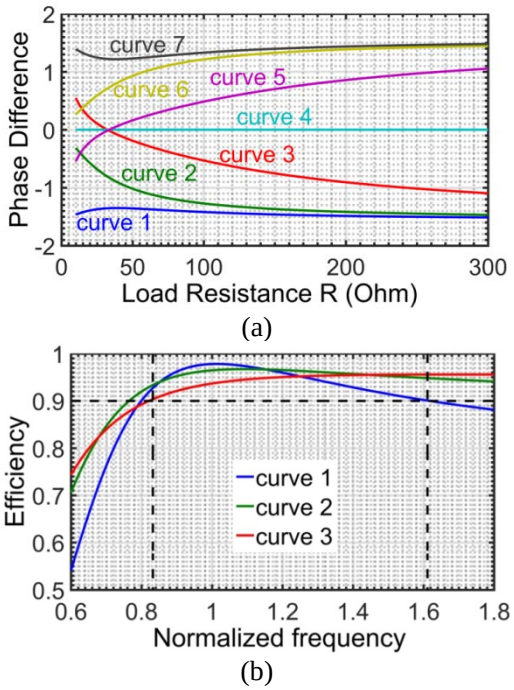


Fig. III-9. (a) Phase difference vs R at different operation frequencies; (b) Efficiency vs normalized frequency at different load conditions

Fig. III-9 (a) shows the curves of phase difference vs load resistance at different operation frequencies (curve 1: $\omega_s < \omega_1$; curve 2: $\omega_s = \omega_1$; curve 3: $\omega_1 < \omega_s < \omega_3$; curve 4: $\omega_s = \omega_3$; curve 5: $\omega_3 < \omega_s < \omega_2$; curve 6: $\omega_s = \omega_2$; curve 7: $\omega_s > \omega_2$). To obtain enough large φ, curve 6 and 7 should be selected. However, from (3.15), P_o will be infinitely large if ω_s is equal to ω_2. Therefore, ω_s should be larger than ω_2. Considering total equivalent series resistance (ESR) of the resonant tank, transmission efficiency characteristics of the resonant tank can be obtained at base frequency ω_3, assuming ESR of primary and secondary sides to be 0.3Ω, as shown in Fig. III-9 (b) (curve 1: R=40Ω; curve 2: R=100Ω; curve 3: R=200Ω). To maintain high efficiency, ω_s is suggested to be smaller than $1.6\omega_3$.

III.4 Design Procedure and Considerations

III.4.1 Design Procedure

To facilitate production design of the proposed converter, a 2.56kW laboratory prototype was designed to verify the proposed idea. The design procedures are described as follows.

1) Requirements of input and output:

The input line voltage v_s is designed to be $220V_{rms}$, 50Hz. Maximum output power $P_{o.max}$ is 2.56kW, with constant output voltage V_o = 320V. Thus, maximum output current $I_{o.max}$ is 8A.

2) Requirements and design of resonant coils:

Firstly, the parameters of resonant coils need to be fixed. To simplify the design and calculations, the two coils (air-core) are designed to be identical in spiral shape with the same wire type, mean coil diameter d, winding thickness c, and coils number N, as shown in Fig. III-10. The operation frequency is set around 110kHz. Skin effect is considered and then skin depth d_{sk} is obtained as:

$$d_{sk} = \sqrt{\frac{\rho}{\pi f_s \mu}} \approx 0.2mm, \tag{3.18}$$

where ρ and μ are resistivity and permeability of copper. Therefore, copper litz wire is used to reduce the skin effect. The diameter of each thin wire strand should be smaller than twice of d_{sk}, 0.4mm. Hence, the litz wire with the following parameters was chosen: diameter of each strand d_{st} is 0.2mm; number of strands is 100; effective cross section area of the wire s_w is $3.14mm^2$; diameter of the wire c_w is 3.0mm.

From [124], self-inductances of primary and secondary coils can be expressed as:

$$L_p = L_s = \frac{0.3937\left(\left(d/2\right)\times 100\right)^2 \cdot N^2 \cdot 10^{-6}}{8\left(\left(d/2\right)\times 100\right)+11\left(c\times 100\right)} = k_L N^2. \tag{3.19}$$

In practical implementation, c is determined by c_w, N, and air gap of loops c_{ag} (usually c_{ag} is 1.0mm):

$$c = N\left(c_w + c_{ag}\right). \tag{3.20}$$

For mutual inductance calculation, primary coil is represented by two equivalent filaments 1, 1' and 2, 2', and secondary coil by 3, 3' and 4, 4', as shown in Fig. III-10. Mutual inductance of the two coils can be calculated by:

$$M = N^2 M_e, \tag{3.21}$$

$$M_e = \left(M_{13} + M_{14} + M_{23} + M_{24}\right)/4, \tag{3.22}$$

$$M_{ij} = f_k\left(r_i, r_j, d_{ag}\right) \cdot \sqrt{r_i \cdot r_j} \times 10^{-4}, \tag{3.23}$$

where f_k is the function of k'^2, obtained from tables in [125] and:

$$k'^2 = \frac{\left(r_i - r_j\right)^2 + {d_{ag}}^2}{\left(r_i + r_j\right)^2 + {d_{ag}}^2}, \tag{3.24}$$

where d_{ag} is air gap distance of two coils and

$$r_1 = r_3 = \frac{d}{2}\left(1 + \frac{{c_w}^2}{6d^2}\right) + \sqrt{\frac{c^2 - {c_w}^2}{12}}, \tag{3.25}$$

$$r_2 = r_4 = \frac{d}{2}\left(1 + \frac{{c_w}^2}{6d^2}\right) - \sqrt{\frac{c^2 - {c_w}^2}{12}}. \tag{3.26}$$

For the application of wireless EV charging with typical automobile chassis size and height, d and d_{ag} are designed to be 500mm and 200mm, respectively. Considering in a loosely coupled WPT system the coupling coefficient of two coils is around 0.1 – 0.3 [19], [126], the coupling coefficient k_{ps} is assumed to be 0.18, which also satisfies

$$k_{ps} = \frac{M}{\sqrt{L_p L_s}} = \frac{M_0}{k_L}. \tag{3.27}$$

With above known parameters and from (3.19) – (3.27), N is calculated to be 16. L_p and L_s are calculated to be 249.2μH and M is 44.8μH. In practical implementation, the measured values of L_p, L_s, and M are 241μH, 241μH, and 46μH, respectively.

Because of high core loss and low power density of coils with magnetic cores operating at high frequency (>100kHz), the resonant coils are designed without magnetic cores [17], [19]. In practical applications, shielding should be designed for WPT system, however in the laboratory environment without strict EMI requirements, shielding is not designed for the prototype. There are existing researches on shielding design for WPT system [127] – [129], among which [128] using resonant reactive shielding coil is suitable for air-core coils.

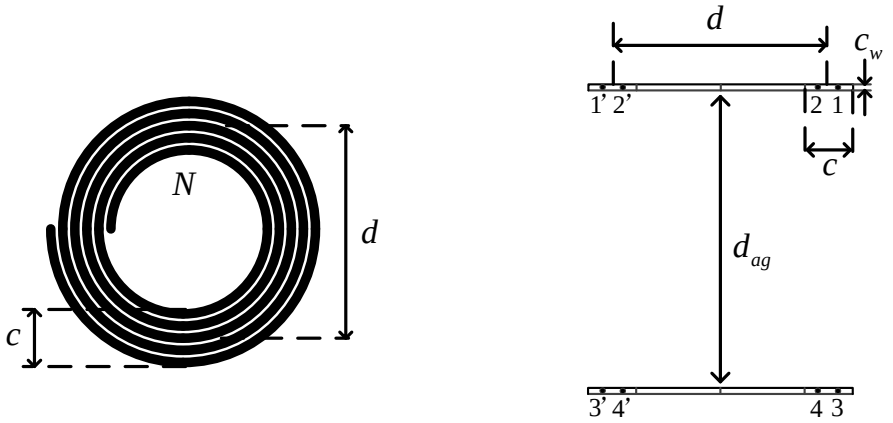


Fig. III-10. Schematic of the resonant coils: (a) top view of one coil; (b) side view of two coils. (N: coils number; c: winding thickness; d: mean coil diameter; d_{ag}: air gap distance of two coils; c_w: diameter of litz wire; primary coil is represented by two equivalent filaments 1, 1' and 2, 2', and secondary coil by 3, 3' and 4, 4')

3) Resonant capacitors and operation frequency:

The operation frequency f_s is chosen to be around 110kHz. Make the higher resonant frequency f_2 [19] equal to 110kHz and resonant capacitors are obtained by:

$$f_2 = \frac{1}{2\pi\sqrt{\left(L_p - M\right)C_1}} = \frac{1}{2\pi\sqrt{\left(L_s - M\right)C_2}}. \tag{3.28}$$

In practical implementation, two 5nF capacitors and two 1nF capacitors are connected in parallel to form the resonant capacitors, which are measured to be 11.83nF. Then the accurate higher resonant frequency is revised to be 104.8 kHz. Applying the proposed modulation method, D_{ab} is used to regulate the output voltage as load varies to maintain constant output voltage. When D_{ab} is equal to 1, output power should reach maximum 2.56 kW. In such condition, with the known parameters (L_p, L_s, M, C_1, C_2, V_{sp}, and V_o), assuming f_s to be 106kHz (a little higher than 104.8 kHz), from (3.14) and (3.15), m is calculated to be 0.97 which cannot satisfy (3.5). Therefore, f_s needs to be revised. By calculation, f_s is chosen to be 111.6 kHz, at which m is equal to 0.49 satisfying (3.5).

4) Input inductance L_{in}:

From above, when in maximum output condition, operation parameters are obtained: D_{ab}=1; P_{in}=2.56 kW; f_s=111.6 kHz; m=0.49. Therefore, from (3.14), L_{in} is calculated to be 36.9 μH. In practical implementation, L_{in} is measured to be 37.0 μH. Here, L_{in} is designed to be air-core inductor because of high core loss and low power density if using a magnetic-core inductor. In the experimental prototype, appropriate measures are implemented to avoid the EMI problem due to the air-core inductor.

5) Load range and maximum bus voltage:

From (3.14) and (3.15), two three-dimensional graphs of P_{in} and P_o (both vary with D_{ab} and m) can be obtained as shown in Fig. III-11. The intersecting curve of the two surfaces is the real operation curve at different load conditions (the black

curve with black circular dot markers). From the curve, at low load conditions, *m* value decreases with output power decreasing. Therefore, the minimum output power is limited by minimum *m* value (maximum V_{bus}). Here the minimum output power is set as 20% of rated output power, which is 512W, and the corresponding *m* value is 0.43. Therefore, maximum bus voltage is 723.5V.

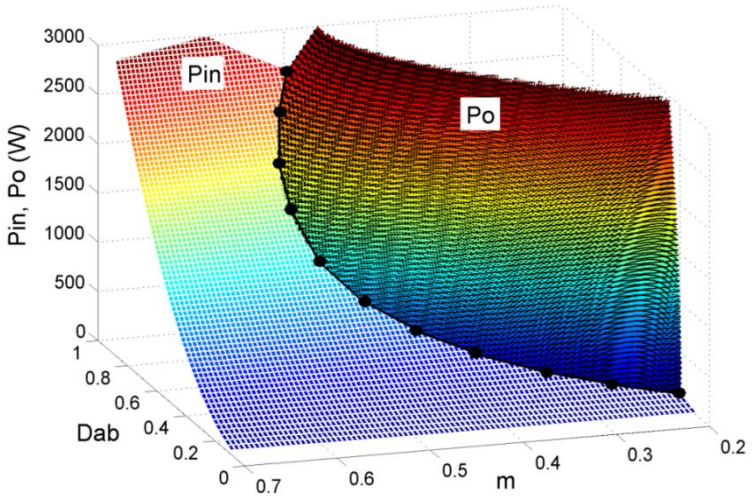


Fig. III-11. Relations of P_{in} and P_o varying with D_{ab} and *m*

6) Design of input EMI filter:

To design the input EMI filter of the proposed converter, the input impedance of the proposed converter needs to be obtained. Because input part of the proposed converter acts as a DCM boost PFC converter, input impedance characteristics can be analyzed like that of a DCM boost PFC converter. From [130], input impedance of the proposed converter Z_{ic} is given as:

$$Z_{ic} = \frac{8L_{in} f_s \left(V_{bus} - v_s\right)}{{D_{ab}}^2 V_{bus}} \frac{1 + s \Big/ \left(\dfrac{{D_{ab}}^2}{8L_{in} C_{bus} f_s} \dfrac{{v_s}^2 \left(2V_{bus} - v_s\right)}{V_{bus} \left(V_{bus} - v_s\right)^2} \right)}{1 + s \Big/ \left(\dfrac{{D_{ab}}^2}{8L_{in} C_{bus} f_s} \dfrac{{v_s}^2 \left(2V_{bus} - v_s\right)}{{V_{bus}}^2 \left(V_{bus} - v_s\right)} \right)}. \tag{3.29}$$

Fig. III-12 gives the input impedance characteristics of the proposed converter at different load condition. (Red curves: 100% load; Green curves: 60% load; Blue

curves: 20% load and solid lines are those with instant line voltage 311V; dotted lines are those with instant line voltage 50V.). At line frequency 50Hz, input impedance of the proposed converter is almost resistive at all load conditions, which can be noted as the input resistance R_{in}. Minimum R_{in} occurs in 100% load condition with v_s to be V_{sp} (311V) and maximum R_{in} occurs in 20% load condition with v_s to be zero:

$$R_{in.\min} \approx \frac{8L_{in} f_s}{D_{ab.100\%}^{\ 2}} \left(1 - \frac{V_{sp}}{V_{bus.100\%}}\right)^2 = 8.7\Omega, \tag{3.30}$$

$$R_{in.\max} \approx \frac{8L_{in} f_s}{D_{ab.20\%}^{\ 2}} = 149.5\Omega. \tag{3.31}$$

A LC low-pass filter is implemented with inductor and capacitor noted as L_{if} and C_{if}. Assuming voltage out from input EMI filter is ideally the same as input voltage, in order to avoid phase-shift of input current, impedance of C_{if} at 50Hz is required to be much larger than $R_{in.\max}$:

$$\frac{1}{\omega_l C_{if}} \gg R_{in.\max} \Rightarrow C_{if} \ll 21.3\mu F. \tag{3.32}$$

Therefore, C_{if} is designed to be 1.0μF. And, in order to make voltage out from input EMI filter close to input voltage as much as possible, impedance of L_{if} at 50Hz is required to be much smaller than $R_{in.\min}$:

$$\omega_l L_{if} \ll R_{in.\min} \Rightarrow L_{if} \ll 27.5mH. \tag{3.33}$$

Hence, L_{if} is designed to be 1.0mH with measured equivalent series resistance (ESR) R_{lf} to be 0.1Ω. With the parameters, output impedance of the input EMI filter is:

$$Z_{of} = \frac{\left(1/\left(sC_{if}\right)\right)\left(sL_{if} + R_{lf}\right)}{1/\left(sC_{if}\right) + sL_{if} + R_{lf}} = \frac{sL_{if} + R_{lf}}{s^2 L_{if} C_{if} + sR_{lf} C_{if} + 1}. \tag{3.34}$$

And therefore transfer function of the input EMI filter is:

$$F_f = \frac{Z_{ic}}{Z_{ic} + Z_{of}} = \frac{1}{1 + Z_{of} / Z_{ic}}. \tag{3.35}$$

By calculation and analysis, Z_{of}/Z_{ic}, regarded as the open loop gain, fulfilled the Nyquist stability criterion at different load conditions. Hence, there is no possible instability problem due to interaction with the input EMI filter.

Because current flowing through L_{if} is 50Hz, core loss is very small and can be ignored compared to copper loss. Hence, the loss of the input EMI filter can be calculated by:

$$P_{f.loss} = i_{in.\mathrm{rms}}{}^2 \cdot R_{lf}, \tag{3.36}$$

where $i_{in.\mathrm{rms}}$ can be calculated with (3.9). Therefore, at 100% load condition, loss of input EMI filter is calculated to be 13.6W, about 0.5% of the load power, which is acceptable.

III.4.2 Design summary and laboratory prototype

Table III-1 shows the design summary and component selection of the laboratory prototype. For Q_1 – Q_4, 2 SiC half-bridge Mosfet modules with 1.2 kV voltage rating are used. Fig. III-13 shows the setup of the laboratory prototype.

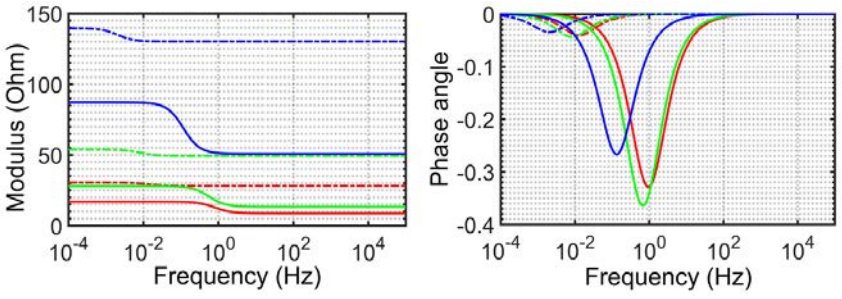


Fig. III-12. Input impedance characteristics of the proposed converter at different load condition

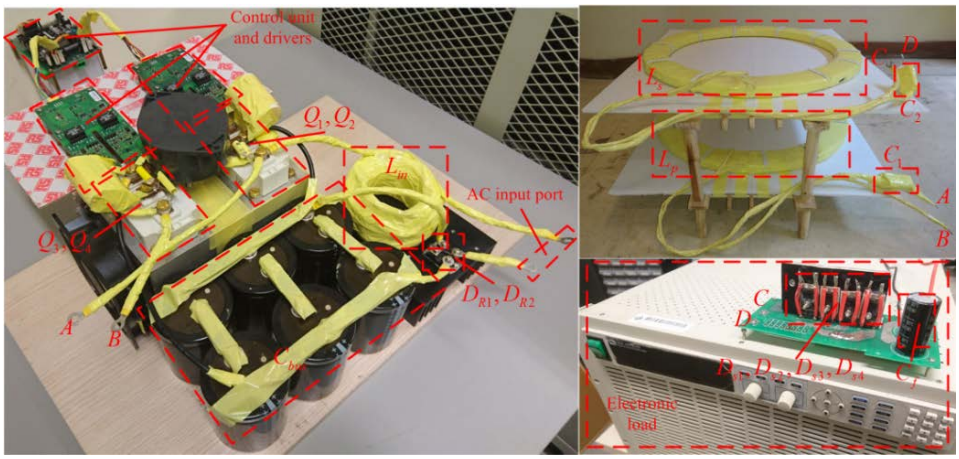


Fig. III-13. Setup of the laboratory prototype

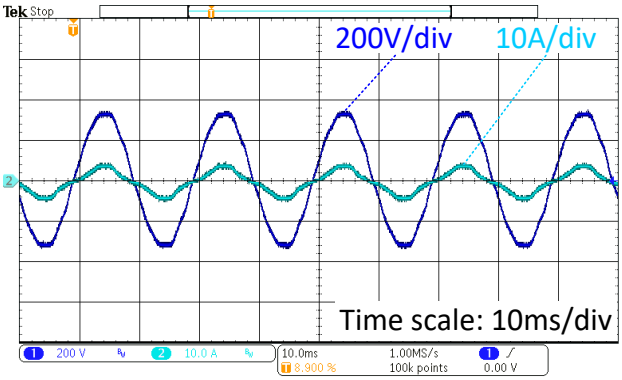
TABLE III-1 Parameters of the laboratory prototype

Components	Details
L_{in}	37.0μH (air core inductor)
D_{R1}, D_{R2}	IXYS DSEI 2x31-10B
Q_1, Q_2, Q_3, Q_4	CREE CAS120M12BM2
C_{bus}	4950μH, 900V (electrolytic capacitors bank)
C_{s1}, C_{s2}	5nF, 1kV (polypropylene capacitors)
C_{s3}, C_{s4}	1nF, 1kV (polypropylene capacitors)
L_p, L_s, M	241μH; 241μH; 46μH
C_1, C_2	11.83nF; 11.83nF (5kV polypropylene capacitors)
D_{s1}, D_{s2}, D_{s3}, D_{s4}	Vishay VS-30EPH06PbF
C_f	220μF, 450V (electrolytic capacitor)
L_{if}, C_{if}	1.0mH, 1.0μF

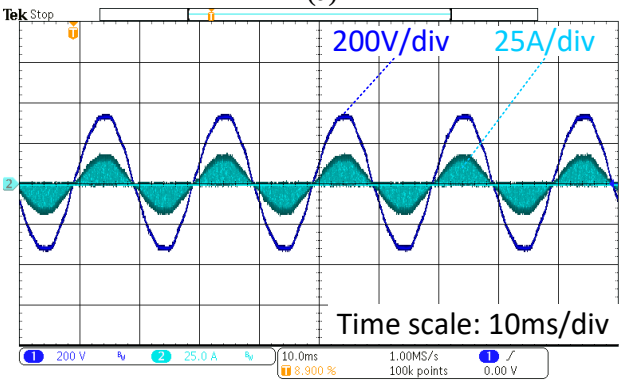
III.5 Experimental Results

Referring to the proposed design procedure, the laboratory prototype with rated (100% load) 2.56kW output is built and tested at different load conditions. Fig. III-14 and Fig. III-15 show the waveforms of AC line input voltage and current and Fig. III-16 (b) shows the PF of AC line input and THD of AC line current (THD_i). At rated load condition, the PF and THD_i reach 0.99 and 15.4%, respectively. Overall, from 20% to 100% load range, the PF is over 0.97 and THD_i

is below 22%. The AC line input voltage is not completely a pure sinewave (with measured THD 3%). If AC line input voltage's THD is close to zero, then THD_i can be 3% – 4% further lower than present measured values. Fig. III-16 (a) shows the total efficiency and partial efficiencies at different stages (Stage 1: from AC line input to input port (AB) of resonant tank; stage 2: from input port (AB) to output port (CD) of resonant tank; stage 3: from output port (CD) of resonant tank to load). At rated load condition, total efficiency reaches 90.1% and efficiency of resonant tank (stage 2) reaches 98.3%. From 40% to 100% load range, total efficiency maintains as high as 90%. However, at 20% load condition, total efficiency drops to 81.7% because switching loss of Q_1 and Q_2 increases as soft-switching cannot be realized completely due to insufficient resonant current. Fig. III-17 shows the switching waveforms of Q_1 and Q_2 at 20% load condition. Fig. III-18 shows the soft-switching waveforms of Q_1 and Q_2 at 100% load condition. Fig. III-19 shows the soft-switching waveforms of Q_3 and Q_4 at both 20% and 100% load conditions. Fig. III-20 – Fig. III-23 show the voltage and current waveforms of primary- and secondary-side resonant tanks at 20% and 100% load condition respectively. For comparison, a traditional two-stage topology for WPT with separate boost DCM PFC and a traditional topology for WPT without PFC are built up and tested. Table III-2 shows the comparisons results at 100% load condition in terms of efficiency, PF, THD_i, and number of semiconductor devices. The Z-source resonant converter with PFC for WPT proposed in [123] is also compared in Table III-2. Generally, the proposed topology exhibits its advantages compared to the other three topologies.

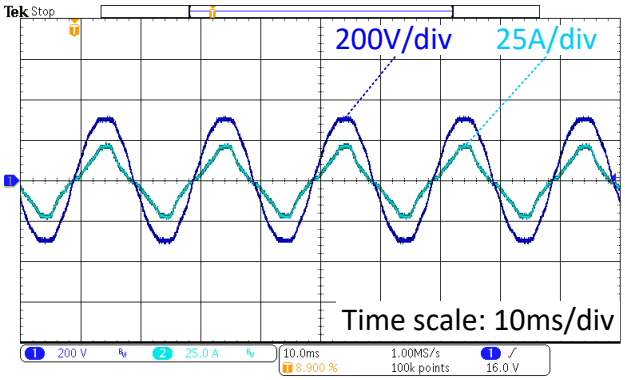


(a)

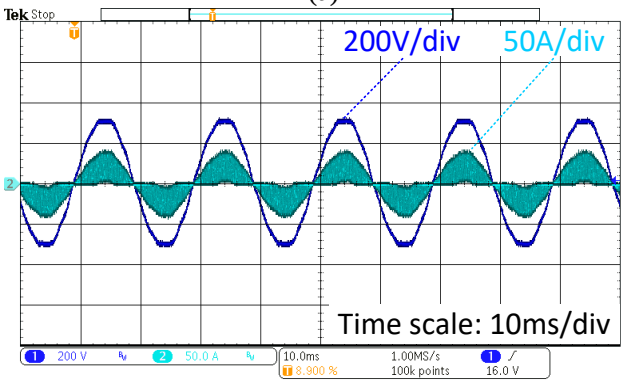


(b)

Fig. III-14. Input voltage (in dark blue) and current (in light blue): (a) with EMI filter, 20% load; (b) without EMI filter, 20% load;

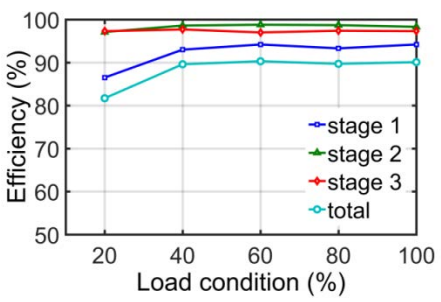


(a)

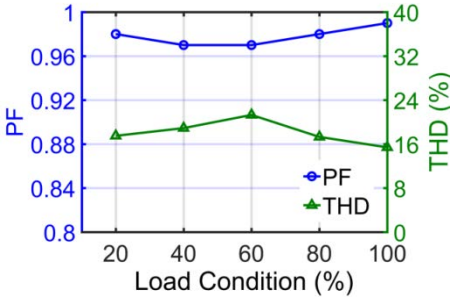


(b)

Fig. III-15. Input voltage (in dark blue) and current (in light blue): (a) with EMI filter, 100% load; (b) without EMI filter, 100% load

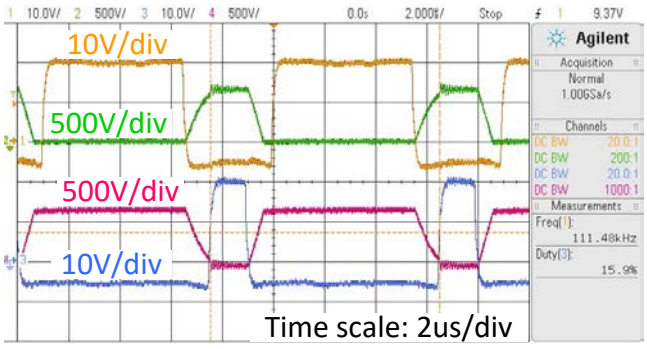


(a)

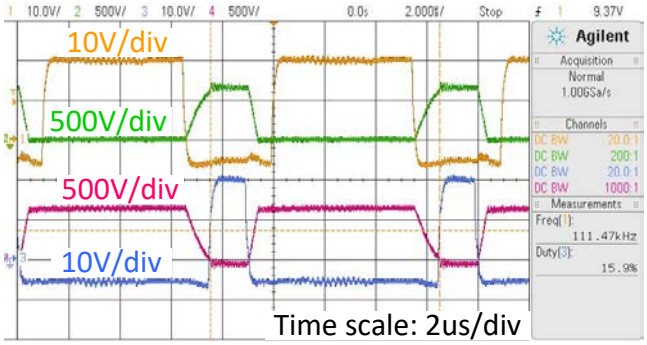


(b)

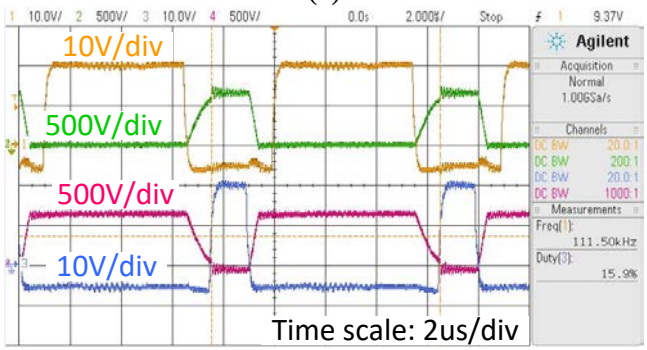
Fig. III-16. (a) Efficiencies under different load conditions at different stages; (b) PF and THD_i under different load conditions



(a)



(b)



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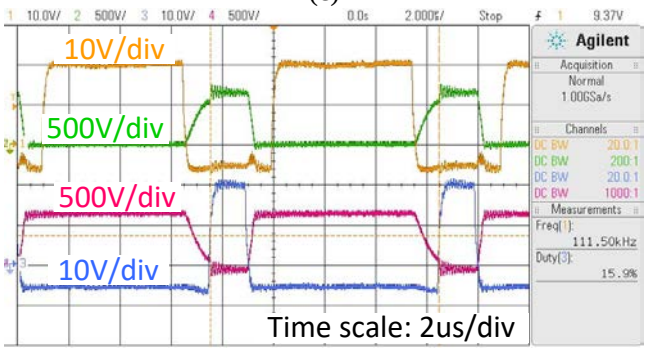
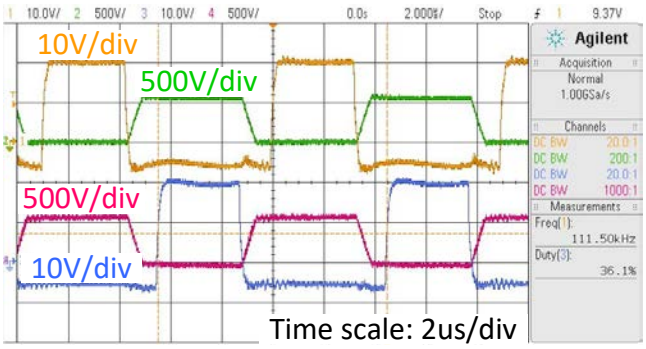
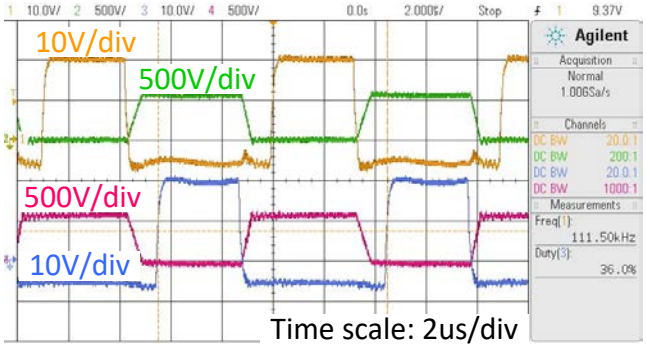


(d)

Fig. III-17. Switching waveforms of Q_1 and Q_2 with 20% load under different phase of input line voltage: (a) 0; (b) π/6; (c) π/3; (d) π/2. (v_{g1} and v_{Q1} in yellow and green; v_{g2} and v_{Q2} in blue and violet)



(a)



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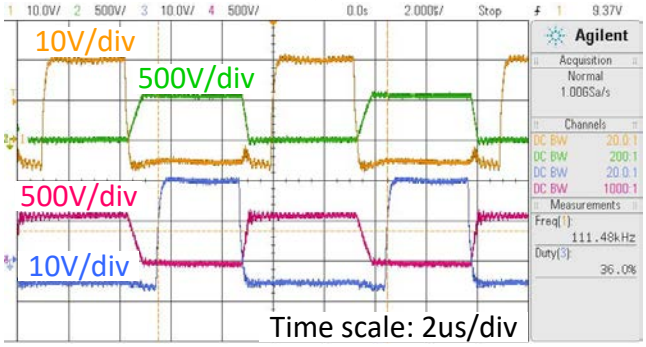

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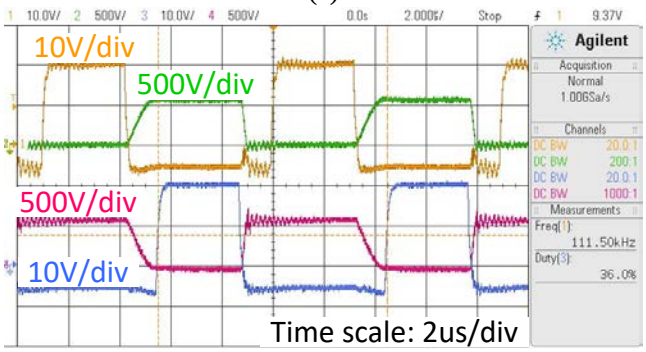
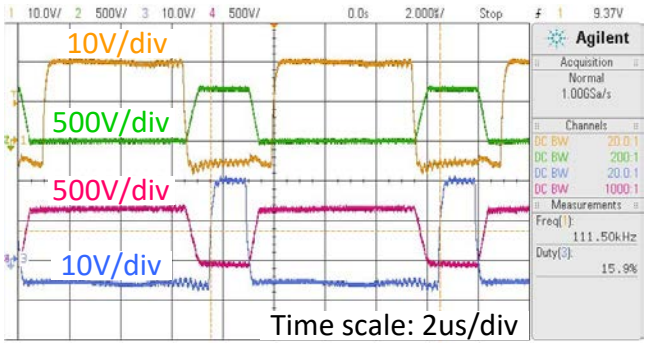
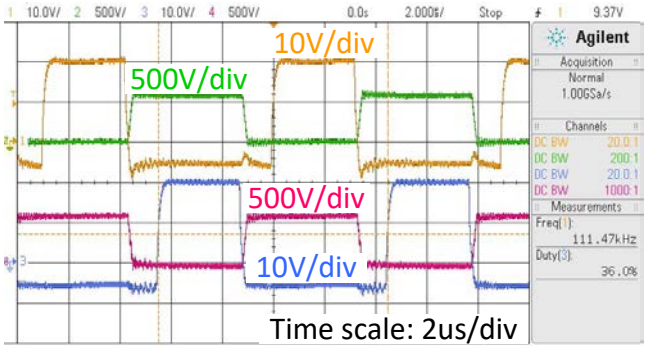


(d)

Fig. III-18. Soft switching waveforms of Q_1 and Q_2 with 100% load under different phase of input line voltage: (a) 0; (b) π/6; (c) π/3; (d) π/2. (v_{g1} and v_{Q1} in yellow and green; v_{g2} and v_{Q2} in blue and violet)

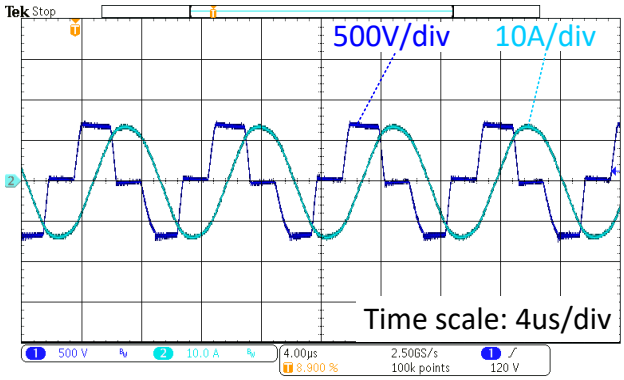


(a)

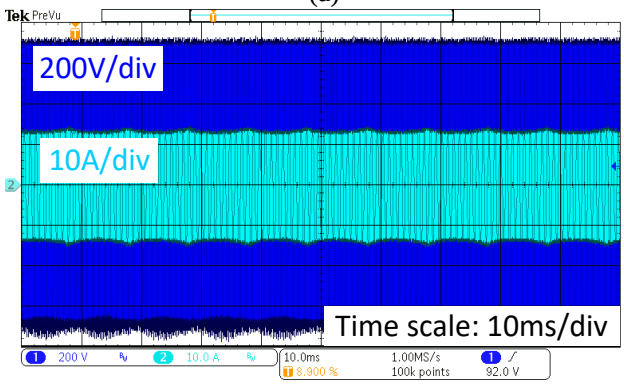


(b)

Fig. III-19. Soft switching waveforms of Q_3 and Q_4: (a) 20% load; (b) 100% load. (v_{g3} and v_{Q3} in yellow and green; v_{g4} and v_{Q4} in blue and violet)

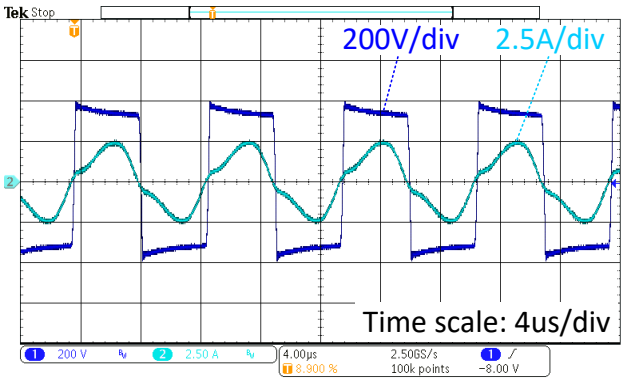


(a)

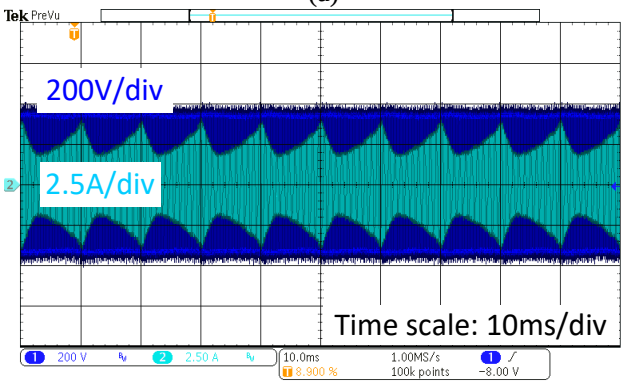


(b)

Fig. III-20. Voltage (in dark blue) and current (in light blue) of primary-side resonant tank at 20% load condition: (a) high frequency profile; (b) low frequency profile

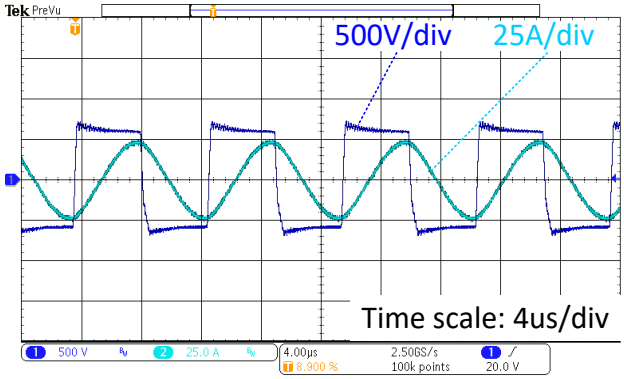


(a)

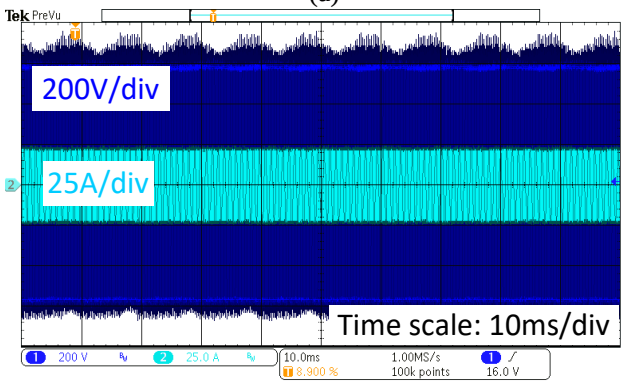


(b)

Fig. III-21. Voltage (in dark blue) and current (in light blue) of secondary-side resonant tank at 20% load condition: (a) high frequency profile; (b) low frequency profile

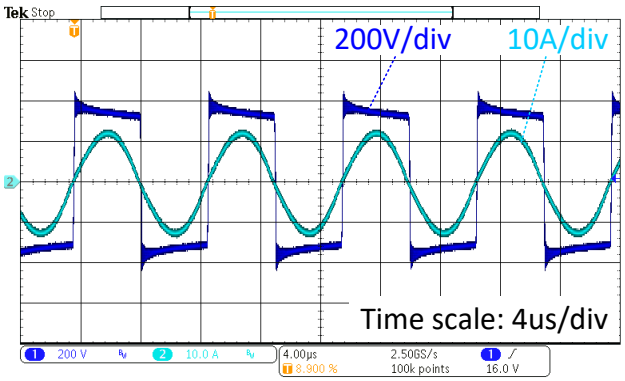


(a)

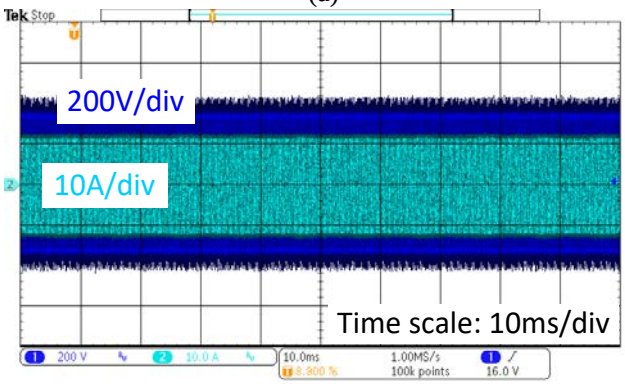


(b)

Fig. III-22. Voltage (in dark blue) and current (in light blue) of primary-side resonant tank at 100% load condition: (a) high frequency profile; (b) low frequency profile



(a)



(b)

Fig. III-23. Voltage (in dark blue) and current (in light blue) of secondary-side resonant tank at 100% load condition: (a) high frequency profile; (b) low frequency profile

TABLE III-2 Comparison of WPT system topologies

Topologies	Efficiency (%)	Power Factor	THD_i (%)	Number of switching devices
Proposed single-stage WPT converter	90.1	0.99	15.4	6 diodes + 4 switches
Traditional two-stage converter for WPT	86.8	0.99	15.7	9 diodes + 5 switches
Traditional converter without PFC for WPT	92.2	0.69	96.5	8 diodes + 4 switches
Z-source converter with PFC for WPT	72.1	0.99	15.7	8 diodes + 4 switches

III.6 Conclusion

In this chapter, a single-stage topology with bridgeless boost PFC rectifier is proposed to apply in high power WPT system, for the first time. Compared to traditional WPT system with a separate boost PFC converter, the proposed topology is more efficient and economical because of less number of semiconductor components. Detailed analysis of the proposed topology, design procedure and example are presented. Finally, a 2.56kW experimental prototype is implemented and tested to prove its high efficiency, PFC functionality, and economy. Future research will focus on improving its efficiency and reducing bus voltage of the proposed topology at light load conditions as well as issues in EMI and shielding.

Chapter IV

A New Control Method for Single-Stage AC-DC Wireless-Power-Transfer Resonant Converter with Improved Input Power Quality, Reduced Bus Voltage and Wide Load Range Operation

IV.1 Introduction

Single-phase single-stage AC-DC transformer-based-isolated converters with PFC have many advantages including higher efficiency, lower count of power semiconductor devices, lower control complexity, and lower cost, compared with traditional single-phase two-stage AC-DC converters. However, they do have pitfalls including varying and excessive bus voltage and imperfect power quality due to not actively shaped input current. The proposed single-phase single-stage AC-DC WPT resonant converter in Chapter III also suffers from those issues. Recently, there have been many researches [131] – [136] proposed to overcome those drawbacks for various single-phase single-stage AC-DC transformer-based-isolated converters. However, there is no existing solution to fix the problems of the proposed single-phase single-stage AC-DC WPT resonant converter in Chapter III.

In this chapter, a new control method for the proposed single-phase single-stage WPT resonant topology is proposed and discussed. Such approach can effectively overcome the mentioned drawbacks. Theoretical analysis, design procedure and example, and simulation results are given with discussions and comparisons between the proposed control method and the original control method in Chapter III. The experiments have not yet been done due to limitation of time and hence

experimental results cannot be given in the thesis. In the coming future, they will be implemented with a laboratory prototype to validate the theory and analysis, as well as the simulation results.

IV.2 Description of Proposed Control Method – Average Discontinuous Current Mode (ADCM) Control

As mentioned in Chapter III, D_g is used to regulate input power or input current and D_{ab} is used to regulate output power or output voltage when operation frequency f_s is confirmed to be constant. In the control method of Chapter III, D_g is set to be equal to half of D_{ab} in order to control the topology simply. In this chapter, an average discontinuous current mode (ADCM) Control is newly proposed to reduce bus voltage and improve power quality furtherly, as well as to realize full load range operation. In this proposed approach, average input inductor current $i_{in.\mathrm{avg}}$, working in discontinuous current mode (DCM), is controlled to follow the input voltage v_s so as to improve the power quality. Therefore, D_g would vary with input voltage v_s in steady state. There are two control parameters, noted as k_I and k_{II}, which are used to control input power and output power respectively.

IV.3 Theoretical Analysis

IV.3.1 Definitions of k_I and k_{II}

In Fig. IV-1, GS and DS waveforms of Q_2 and Q_4 are given. Ideally GS waveforms of Q_1 and Q_3 are complementary with those of Q_2 and Q_4 respectively, and hence are not included in this figure. Because of the symmetry characteristic of v_s in positive and negative cycle, condition of v_s in negative cycle is taken for theoretical analysis. Therefore, D_g refers to duty cycle of Q_2 GS voltage and controls input inductor current i_{in}. Waveforms of Q_4 are also given for reference because v_{AB} is the difference of v_{Q2} and v_{Q4}. In steady state, duty cycle of Q_2 (D_g)

would vary following any change of $v_{s,}$ and duty cycle of Q_4 is controlled as a function of D_g in order to make fundamental component of v_{AB} constant. Therefore, waveform of v_{AB} is varying at different switching period, however, its fundamental component's amplitude and phase are controlled to remain constant at steady-state condition. Fig. IV-1 shows the modulation method of increasing fundamental component's amplitude, while Fig IV-2 shows that of reducing effect, with help of Q_3 and Q_4 half-bridge leg.

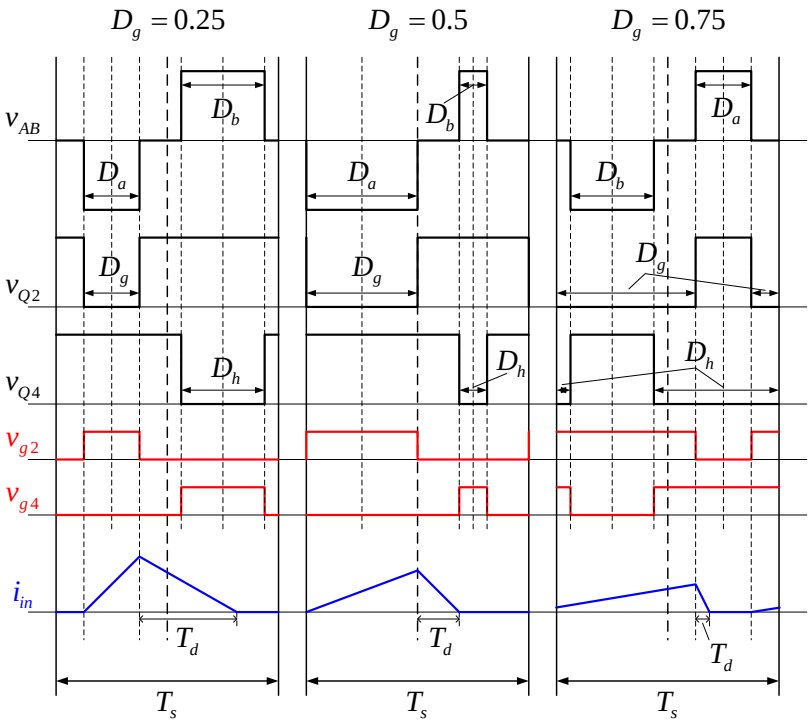


Fig. IV-1. Modulation waveforms of different conditions when v_s is in its positive cycle

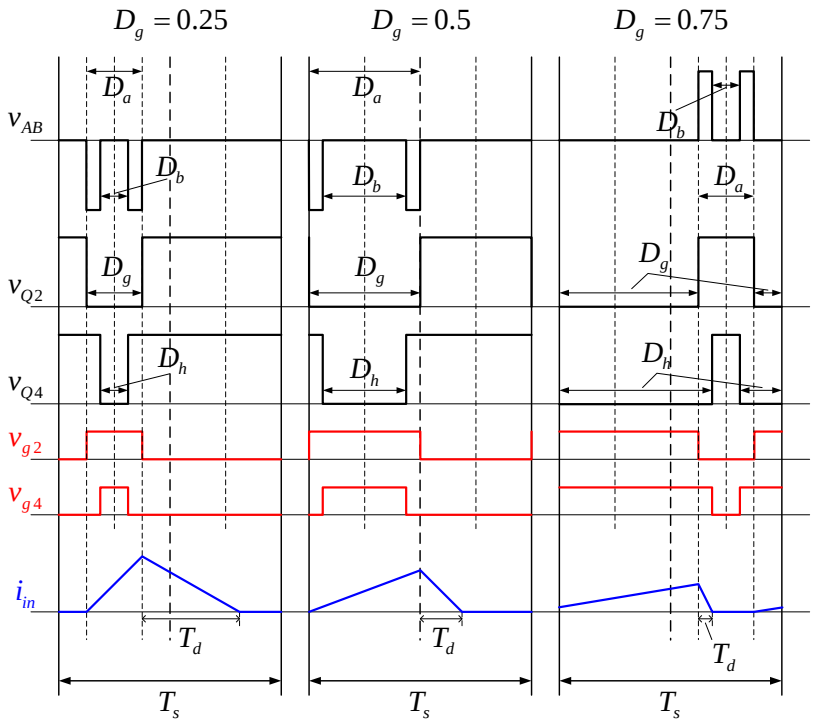


Fig. IV-2. Modulation waveforms of different conditions when v_s is in its positive cycle

Next is to calculate the average of input inductance current i_{in} in a switching period. Firstly, i_{in} is designed to work in DCM and therefore has the following limitation:

$$\frac{v_s}{L_{in}} \cdot D_g T_s + \frac{v_s - V_{bus}}{L_{in}} \cdot \left(1 - D_g\right) T_s \le 0, \tag{4.1}$$

which means:

$$D_g \le \frac{V_{bus} - v_s}{V_{bus}}. \tag{4.2}$$

The average of i_{in} in a switching period T_s is:

$$\begin{aligned} i_{in.\text{avg}} &= \frac{1}{2} \cdot \frac{v_s}{L_{in}} \cdot D_g T_s \cdot D_g + \frac{1}{2} \cdot \frac{v_s}{L_{in}} \cdot D_g T_s \cdot \frac{T_d}{T_s} \\ &= \frac{1}{2} \cdot \frac{v_s}{L_{in}} \cdot D_g T_s \cdot \left(D_g + \frac{T_d}{T_s} \right), \end{aligned} \tag{4.3}$$

where T_d is obtained by:

$$\frac{v_s}{L_{in}} \cdot D_g T_s + \frac{v_s - V_{bus}}{L_{in}} \cdot T_d = 0$$
$$\Rightarrow T_d = \frac{v_s D_g T_s}{V_{bus} - v_s}. \tag{4.4}$$

Therefore, average i_{in} is given by:

$$i_{in.\text{avg}} = \frac{v_s V_{bus} D_g{}^2 T_s}{2L_{in}\left(V_{bus} - v_s\right)}. \tag{4.5}$$

To improve the power factor and reduce the total harmonics distortion (THD), the average i_{in} would be controlled to follow the variation of v_s, and the following expression is given:

$$i_{in.\text{avg}} = k_{iv} \cdot v_s, \tag{4.6}$$

where k_{iv} is ratio of $i_{in.\text{avg}}$ and v_s.

Therefore,

$$\frac{v_s V_{bus} D_g{}^2 T_s}{2L_{in}\left(V_{bus} - v_s\right)} = k_{iv} \cdot v_s$$
$$\Rightarrow D_g = \sqrt{\frac{2L_{in}\left(V_{bus} - v_s\right) \cdot k_{iv}}{V_{bus} T_s}}. \tag{4.7}$$

From (4.2) and (4.7), meaningful range of k_{iv} can be obtained as:

$$0 \le k_{iv} \le \frac{1}{2L_{in} f_s} \cdot \frac{V_{bus} - V_{sp}}{V_{bus}}. \tag{4.8}$$

The first control parameter k_I is defined to replace k_{iv}:

$$k_I = k_{iv} \cdot 2L_{in} f_s. \tag{4.9}$$

Also a parameter m is defined to be the ratio of V_{sp} and V_{bus}:

$$m = \frac{V_{sp}}{V_{bus}}. \tag{4.10}$$

From (4.8), k_I is limited as:

$$0 \le k_I \le 1-m. \tag{4.11}$$

From (4.7), D_g is obtained as:

$$D_g = \sqrt{\left(1-m\sin\left(\omega_l t\right)\right)\cdot k_I}\,. \tag{4.12}$$

For a given k_I, maximum and minimum values of D_g are:

$$D_{g.\min} = \sqrt{(1-m)\cdot k_I}\,,\quad D_{g.\max} = \sqrt{k_I}\,. \tag{4.13}$$

For the WPT conversion function, FHA method is applied to analyze the output power and output voltage. There are two kinds of v_{AB} waveforms: the first one is to increase v_{AB}'s fundamental component's amplitude; and the second one is to decrease it, as shown in Fig. IV-1 and Fig. IV-2. And from Fig. IV-1, it can be observed that duty cycle of one half of the v_{AB} waveform is D_a and the other half is D_b. Therefore, amplitude of fundamental component of v_{AB} is obtained as:

$$V_{AB.1.\mathrm{pk}} = \frac{2V_{bus}}{\pi}\left[\sin\left(D_a\pi\right)+\sin\left(D_b\pi\right)\right]. \tag{4.14}$$

From Fig. IV-2, amplitude of fundamental component of v_{AB} is obtained as:

$$V_{AB.1.\mathrm{pk}} = \frac{2V_{bus}}{\pi}\left[\sin\left(D_a\pi\right)-\sin\left(D_b\pi\right)\right]. \tag{4.15}$$

From Fig. IV-1 and Fig. IV-2, it can be observed that D_a and D_b are directly related to duty cycles of Q_2 and Q_4, which are D_g and D_h respectively. D_g is varying with time periodically as (4.12). D_h also needs to be controlled to coordinate with D_g in order to make $V_{AB.1.\mathrm{pk}}$ constant at steady-state condition. Here, the second control parameter k_{II} is defined as:

$$k_{II} = \sin\left(D_a\pi\right)\pm\sin\left(D_b\pi\right). \tag{4.16}$$

Therefore, (4.14) and (4.15) can be expressed as:

$$V_{AB.1.\mathrm{pk}} = \frac{k_{II}}{m} \cdot \frac{2V_{sp}}{\pi}. \tag{4.17}$$

From Fig. IV-1 and Fig. IV-2, D_a and D_b are both with the range of [0, 0.5], and hence, when D_g is smaller than or equal to 0.5, D_h is also smaller than or equal to 0.5 (condition 1); when D_g is larger than 0.5, D_h is larger than or equal to 0.5 (condition 2). For condition 1, D_a is equal to D_g and D_b is equal to D_h, while for condition 2, D_a is equal to 1-D_g and D_b is equal to 1-D_h. Therefore, (4.16) can be also expressed as:

$$k_{II} = \sin\left(D_g \pi\right) \pm \sin\left(D_h \pi\right). \tag{4.18}$$

At steady state, D_g is varying in a range [$D_{g\min}$, $D_{g\max}$], and the maximum and minimum values of sin ($D_g\pi$) are bounded as follows.

If $D_{g.\max} > 0.5$ and $D_{g.\min} < 0.5$,

$$\begin{aligned} \left[\sin\left(D_g \pi\right)\right]_{\max} &= 1, \\ \left[\sin\left(D_g \pi\right)\right]_{\min} &= \min\left[\sin\left(D_{g\max} \pi\right), \sin\left(D_{g\min} \pi\right)\right]. \end{aligned} \tag{4.19}$$

If $D_{g.\max} \leq 0.5$,

$$\begin{aligned} \left[\sin\left(D_g \pi\right)\right]_{\max} &= \sin\left(D_{g\max} \pi\right), \\ \left[\sin\left(D_g \pi\right)\right]_{\min} &= \sin\left(D_{g\min} \pi\right). \end{aligned} \tag{4.20}$$

If $D_{g.\min} \geq 0.5$,

$$\begin{aligned} \left[\sin\left(D_g \pi\right)\right]_{\max} &= \sin\left(D_{g\min} \pi\right), \\ \left[\sin\left(D_g \pi\right)\right]_{\min} &= \sin\left(D_{g\max} \pi\right). \end{aligned} \tag{4.21}$$

By analysis, k_{II} is limited in a meaningful range of:

$$0 \leq k_{II} \leq 1 + \left[\sin\left(D_g \pi\right)\right]_{\min}. \tag{4.22}$$

For a given D_g value, if k_{II} is larger than or equal to sin ($D_g\pi$), modulation method of Fig. IV-1 will be applied; otherwise, modulation of Fig. IV-2 will be applied.

By analyzing the two modulation methods, D_h can be obtained as:

$$D_{h1}, D_{h2} = \frac{1}{\pi} \arcsin \left| k_{II} - \sin\left(D_g \pi\right) \right|, \tag{4.23}$$

$$\begin{aligned} 0 \le D_{h1} \le 0.5; \\ 0.5 \le D_{h2} \le 1. \end{aligned} \tag{4.24}$$

$$D_h = \begin{cases} D_{h1} & \text{when } D_g \le 0.5 \\ D_{h2} & \text{when } D_g > 0.5 \end{cases}. \tag{4.25}$$

IV.3.2 Power balance analysis

From (2.6), at middle resonant frequency, assuming that the single-stage WPT resonant converter is ideal and therefore there is no power loss, then output power in a switching period $P_{o.sw}$ is:

$$P_{o.sw} = \frac{{V_{AB.1.pk}}^2 R_e}{2{\omega_s}^2 M^2}, \tag{4.26}$$

where R_e is equivalent resistance of FHA model and defined as:

$$R_e = \frac{8}{\pi^2} R. \tag{4.27}$$

And therefore the output power is calculated as:

$$P_o = \frac{2}{T_l} \int_0^{T_l/2} P_{o.sw} dt. \tag{4.28}$$

For the power factor correction function, because D_g is controlled to make $i_{in.\text{avg}}$ follow varying v_s, the input power is calculated as:

$$P_{in} = \frac{k_I}{4 L_{in} f_s} {V_{sp}}^2, \tag{4.29}$$

where V_{sp} is amplitude of input voltage v_s.

Load resistance R can be expressed as:

$$R = \frac{V_o^{\,2}}{P_o}. \tag{4.30}$$

From (4.14) – (4.28), then output power is obtained as:

$$P_o = \frac{16 V_{sp}^{\,2} R k_{II}^{\,2}}{\pi^4 \omega_s^{\,2} M^2 m^2}. \tag{4.31}$$

For constant output voltage application, P_o is expressed as:

$$P_o = \frac{4 V_{sp} V_o k_{II}}{\pi^2 \omega_s M m}. \tag{4.32}$$

From (4.29) and (4.32), both P_{in} and P_o can be regulated from maximum power level to zero by adjusting values of k_I and k_{II}, without causing V_{bus} too high. Ideally, there is no power loss in the single-stage power conversion and therefore input power is equal to output power and the following expression can be obtained:

$$\left(k_I / k_{II}\right) \cdot M = \left(16 V_o L_{in} f_s\right) \Big/ \left(V_{sp} \pi^2 \omega_s m\right). \tag{4.33}$$

IV.3.3 Modulation method and driving signals generation circuit

Fig. IV-3 shows the driving signals generation circuit of the proposed control method without considering dead-time operation. Such circuit can be realized by DSP programming and some logic gates operation. In practical experiment, dead-time generator (delay modules) will be added. In the circuit there is a triangular-wave signal generator (from 0 to 1, and to 0) with fixed operation frequency f_s. Such circuit is can be easily implemented using a FPGA IC with embedded soft-core processor (such as ALTERA FPGAs with NIOS II processor).

IV.4 Design Procedure and Example

An example of the proposed control method is presented here with detailed design procedures. This example is based on the hardware setup of Chapter V.

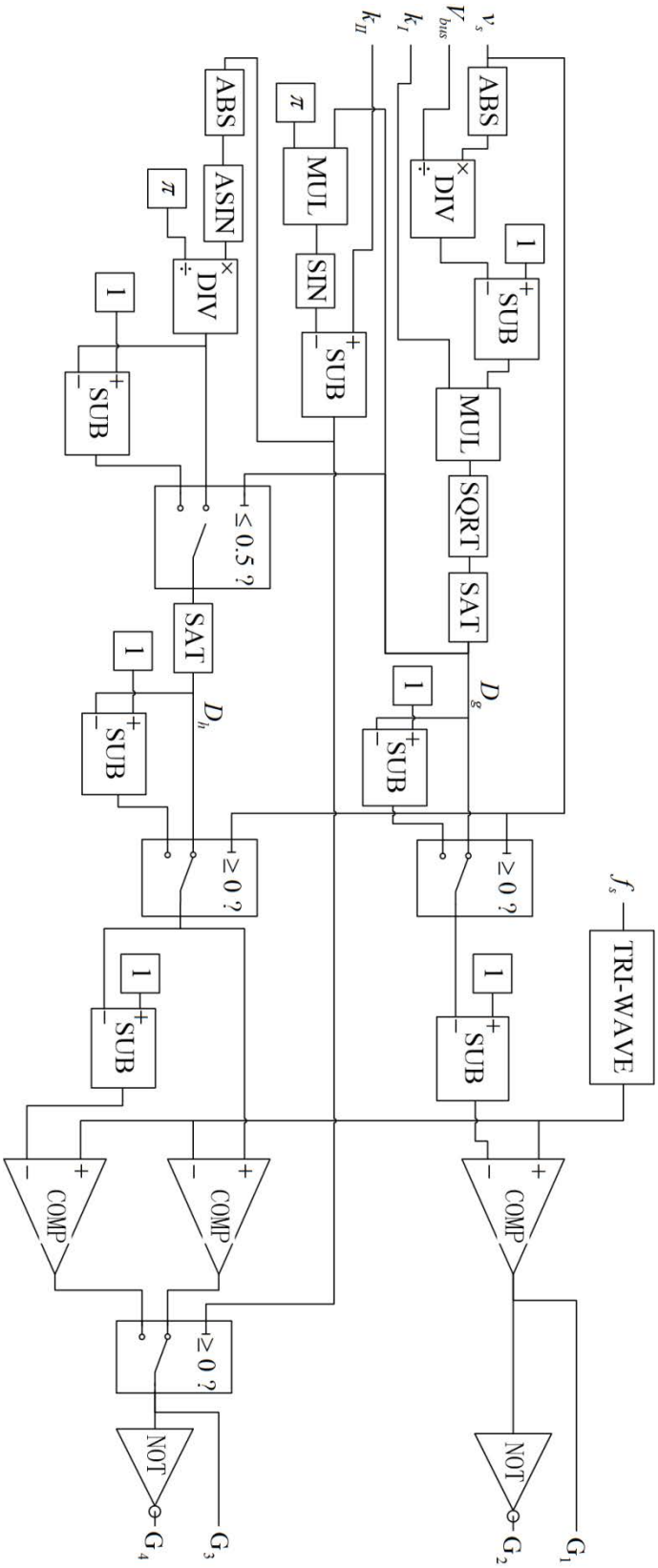


Fig. IV-3. Driving signals generation circuit of the proposed control method (without considering dead-time operation)

1) Input, output and bus voltage requirements:

Input voltage v_s is confirmed to be 50 Hz, 220 V_{rms} AC from the power grid. Output voltage V_o is designed to be 200 V and maximum (rated) output power $P_{o.\max}$ is 1.6 kW. Therefore, maximum output current $I_{o.\max}$ is 8 A and the corresponding load resistance is 25 Ω. Maximum bus voltage V_{bus} is designed to be 500 V, during full load range conditions. From (6-11), k_I is limited and the maximum value of k_I is obtained when m is minimum (maximum bus voltage), therefore, maximum output power condition occurs when k_I and V_{bus} reach maximum values. Maximum value of k_I, noted as $k_{I.\max}$, should fulfill the limitation of (4.34) and therefore $k_{I.\max}$ is chosen to be 0.36.

$$k_{I.max} \le 1 - \frac{220\sqrt{2}}{500} = 0.378. \tag{4.34}$$

2) Confirm operation frequency f_s and design resonant tanks:

According to hardware setup in Chapter V, resonant tanks were designed and implemented with:

$$L_p = 245.8\mu H, L_s = 245.3\mu H. \tag{4.35}$$

Operation frequency f_s should be designed to be around 85 kHz (81.39 – 90 kHz) to comply with the industrial wireless charging standard (SAE J2954). Here the operation frequency is chosen to be the middle resonant frequency and is set to be 85 kHz first. C_1 and C_2 are calculated as 14.26 nF and 14.29 nF respectively according to (4.36). Practically, C_1 and C_2 are measured to be 14.46 nF and 14.39 nF. To make the secondary-side resonant tank at a pure resonant condition, f_s is revised to be 84.7 kHz. The mutual inductance M can be regulated by changing misalignment distance of the two coils. Here M value is limited and varying in a range from 40 μH to 55 μH.

$$f_s = \frac{1}{2\pi\sqrt{L_p C_1}} = \frac{1}{2\pi\sqrt{L_s C_2}}. \tag{4.36}$$

3) Calculation of input inductor L_{in}:

Practically there are losses existing in the converter, therefore, when determining the value of L_{in}, approximate value of $P_{in.\max}$ needs to be confirmed firstly. Assuming the total efficiency of the converter is 90% at full load condition, $P_{in.\max}$ is estimated to be 1.6/0.9 kW.

At full load condition (100% load), the control parameter k_I is chosen to be $k_{I..\max}$, 0.36, and therefore from (6-29):

$$\begin{aligned} L_{in} &= \frac{k_{I.max}}{4P_{in.\max} f_s} V_{sp}^{\ 2} \\ &= \frac{0.36}{4\times\left(1.6\times10^3/90\%\right)\times84.7\times10^3}\times\left(220\sqrt{2}\right)^2 \ \mu\text{H} = 57.9\ \mu\text{H}. \end{aligned} \tag{4.37}$$

4) Determination of k_{II} at full load condition

At full load condition (100% load), the control parameter k_I and m are as follows:

$$k_I = 0.36, \quad m = 220\sqrt{2}/500 = 0.622. \tag{4.38}$$

Therefore, from (4.13) and (4.22),

$$D_{g.\min} = 0.369, \quad D_{g.\max} = 0.6. \tag{4.39}$$

$$0 \le k_{II} \le 1.916. \tag{4.40}$$

From (4.32), k_{II} is obtained as follows with different M conditions:

$$k_{II} = \frac{P_{o.\max}\pi^2\omega_s m}{4V_{sp}V_o}\cdot M \in [0.840, 1.155], \tag{4.41}$$

which fulfills the limitation of (4.40).

5) Calculation of control parameters (k_I and k_{II}) under different load conditions:

A half load, i.e. 0.8 kW, is taken as an example to illustrate the calculation of k_I and k_{II}. From (4.29), at 50% load condition, k_I is also 50% of $k_{I.\max}$, hence, it is 0.18.

And V_{bus} is kept constantly equal to 500V and hence m is kept constantly 0.622. From (4.13) and (4.22),

$$D_{g.\min} = 0.261, \quad D_{g.\max} = 0.424. \tag{4.42}$$

$$0 \le k_{II} \le 1.731. \tag{4.43}$$

From (4.32), k_{II} is obtained as follows with different M conditions:

$$k_{II} = \frac{P_{o.50\%}\pi^2\omega_s m}{4V_{sp}V_o} \cdot M \in [0.420, 0.578], \tag{4.44}$$

which fulfills the limitation of (4.43).

Table IV-1 gives the values of k_I and k_{II}, as well as THD of input current (THD_i) at different load conditions. Waveforms of $i_{in.\text{avg}}$ at different load conditions are calculated and simulated and the THD is very small. Theoretically, $i_{in.\text{avg}}$ is pure sine wave in phase with input voltage v_s.

6) Design summary:

Table IV-2 gives the design summary of the example.

TABLE IV-1 Control parameters and THD at different load conditions

Load condition	k_I	k_{II}	THD_i (%)
100% (1600 W)	0.360	0.840 – 1.155	0.10
80% (1280 W)	0.288	0.672 – 0.924	0.10
60% (960 W)	0.216	0.504 – 0.693	0.10
50% (800 W)	0.180	0.420 – 0.578	0.10
40% (640 W)	0.144	0.336 – 0.462	0.10
20% (320 W)	0.072	0.168 – 0.231	0.10
10% (160 W)	0.036	0.084 – 0.116	0.10

TABLE IV-2 Parameters of the laboratory prototype

Parameter	Values	Parameter	Values
$P_{o.\max}$	1600 W	L_{in}	57.9 μH
V_o	200 V	L_p, L_s, M	245.8 μH; 245.3 μH; 40 – 55 μH
v_s	220 Vrms, 50 Hz	C_1, C_2	14.46 nF; 14.39 nF
V_{bus}	500 V	$k_{I.\max}$	0.36
f_s	84.7 kHz	$k_{II.\max}$	0.840 – 1.155

IV.5 Simulation Results

Simulation results are given with the designed parameters detailed in Section IV.4. Fig. IV-4 – IV-17 give the waveforms of v_s, i_s, i_{in}, v_{AB}, i_r, v_{CD}, i_{rs}, V_{bus}, and V_o under 100% load condition in details respectively, while Fig. IV-18 – IV-31 give those under 10% load condition. It can be shown that the power quality under both full load and low load conditions are at very good level, with THD and power factor measured to be smaller than 1% and larger than 0.99 respectively. Also output voltage ripples are very small, and measured below 0.8 V. In addition, bus voltage is controlled to be constantly 500 V at different load conditions.

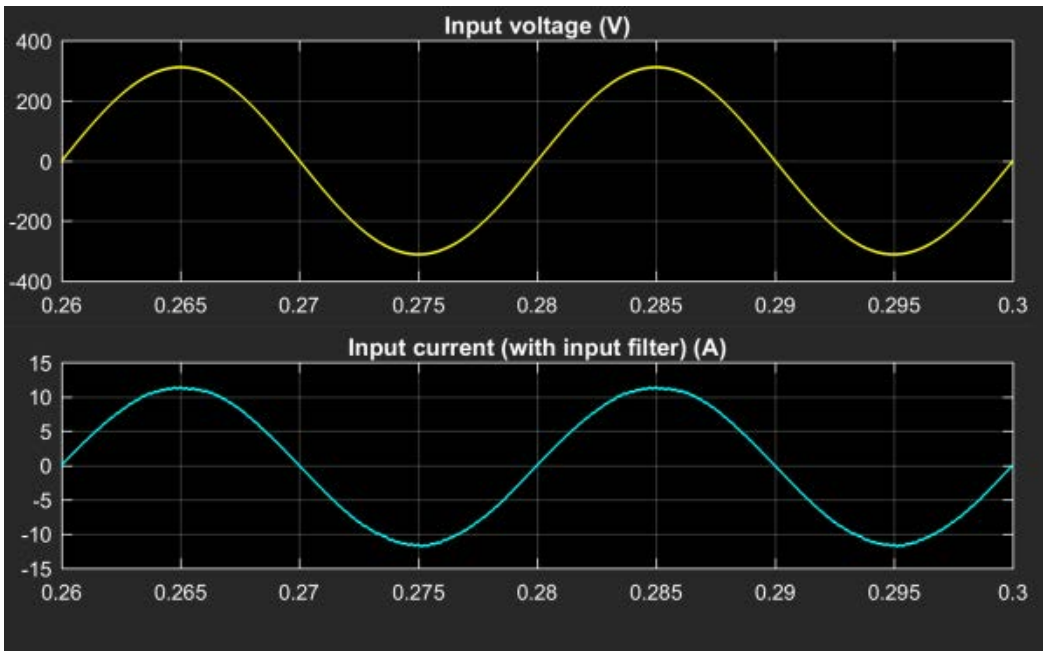


Fig. IV-4. Input voltage and current with input filter (v_s and i_s) at 100% load condition (low frequency profile)

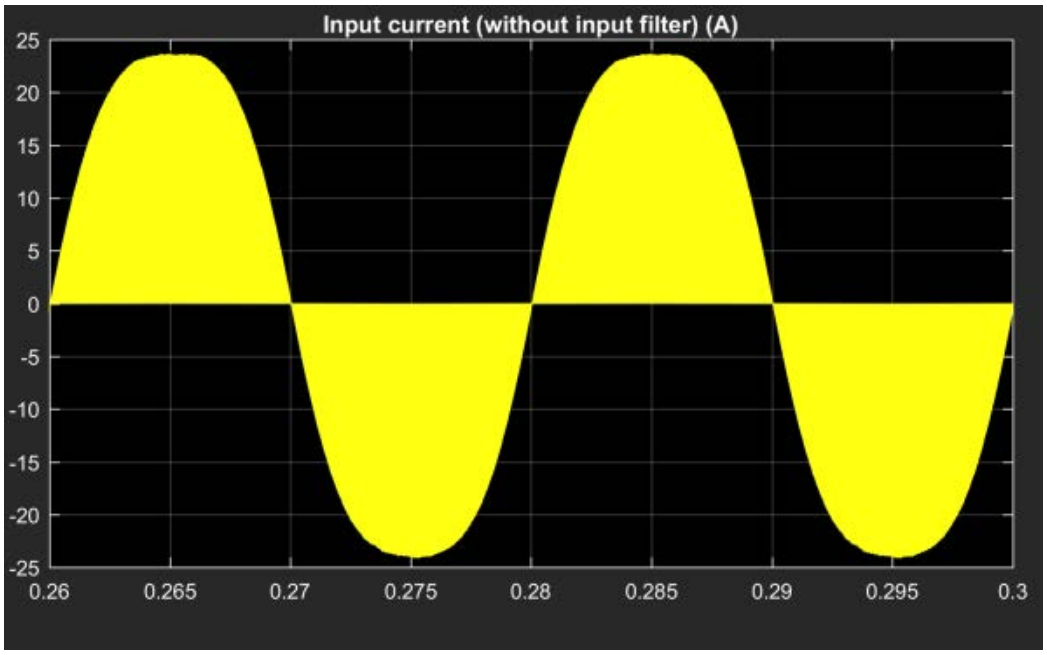


Fig. IV-5. Input current without input filter (i_{in}) at 100% load condition (low frequency profile)

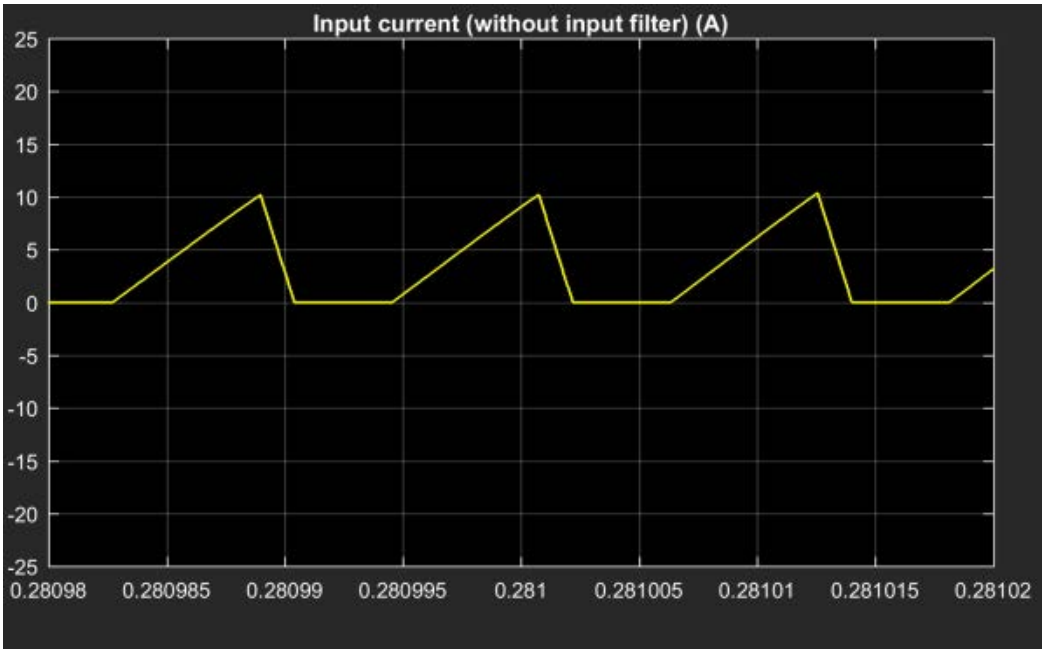


Fig. IV-6. Input current without input filter (i_{in}) at 100% load condition (high frequency profile at 0.281 s)

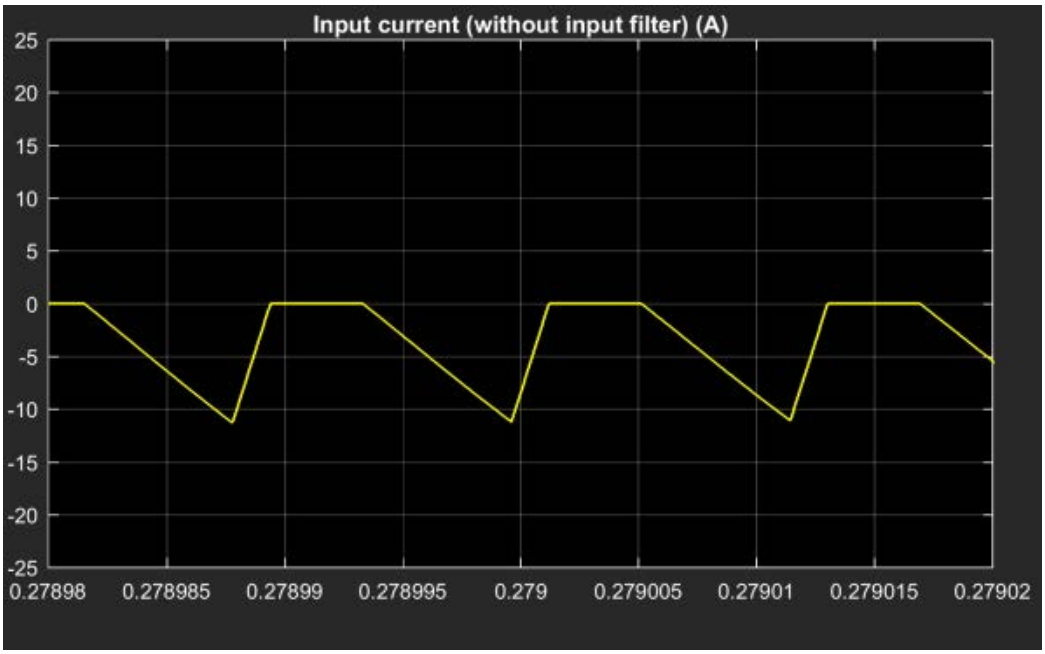


Fig. IV-7. Input current without input filter (i_{in}) at 100% load condition (high frequency profile at 0.279 s)

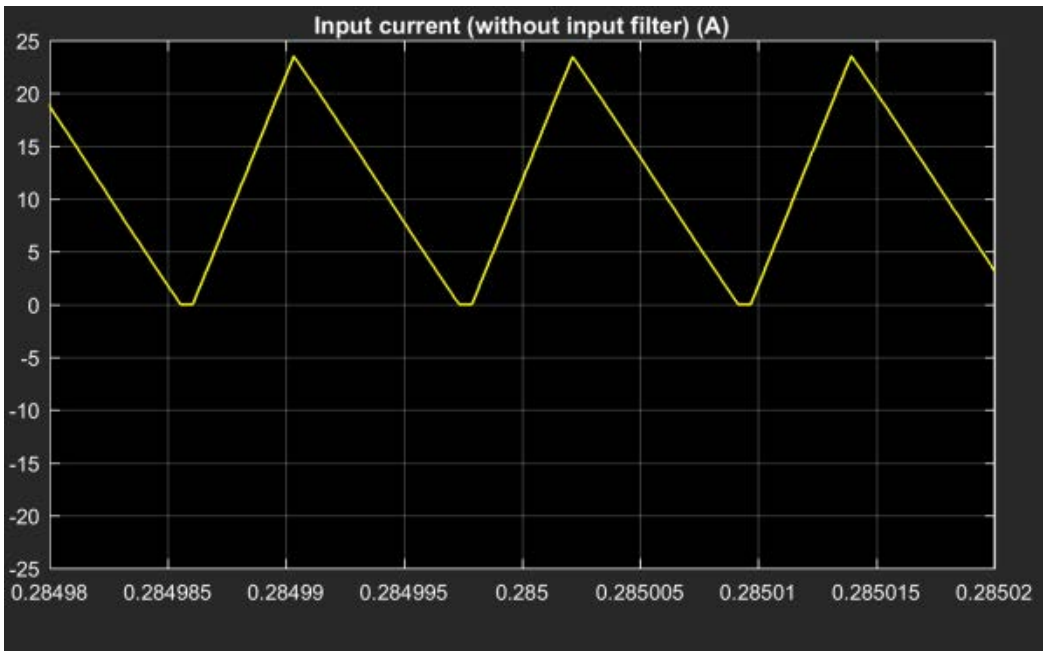


Fig. IV-8. Input current without input filter (i_{in}) at 100% load condition (high frequency profile at 0.285 s)

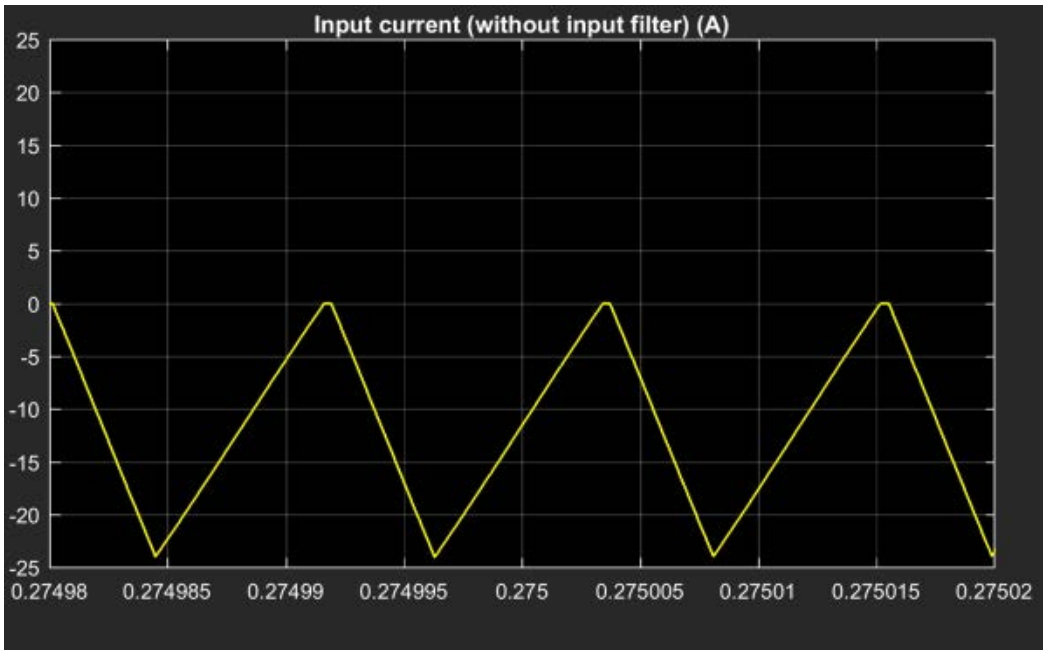


Fig. IV-9. Input current without input filter (i_{in}) at 100% load condition (high frequency profile at 0.275 s)

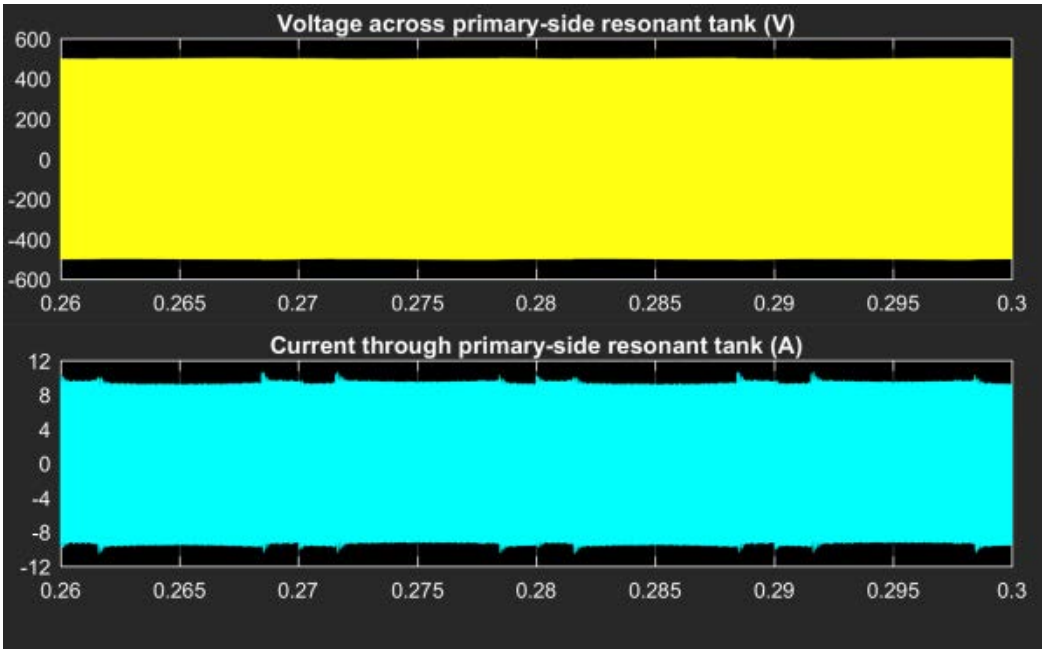


Fig. IV-10. Voltage and current of primary-side resonant tank (v_{AB} and i_r) at 100% load condition (low frequency profile)

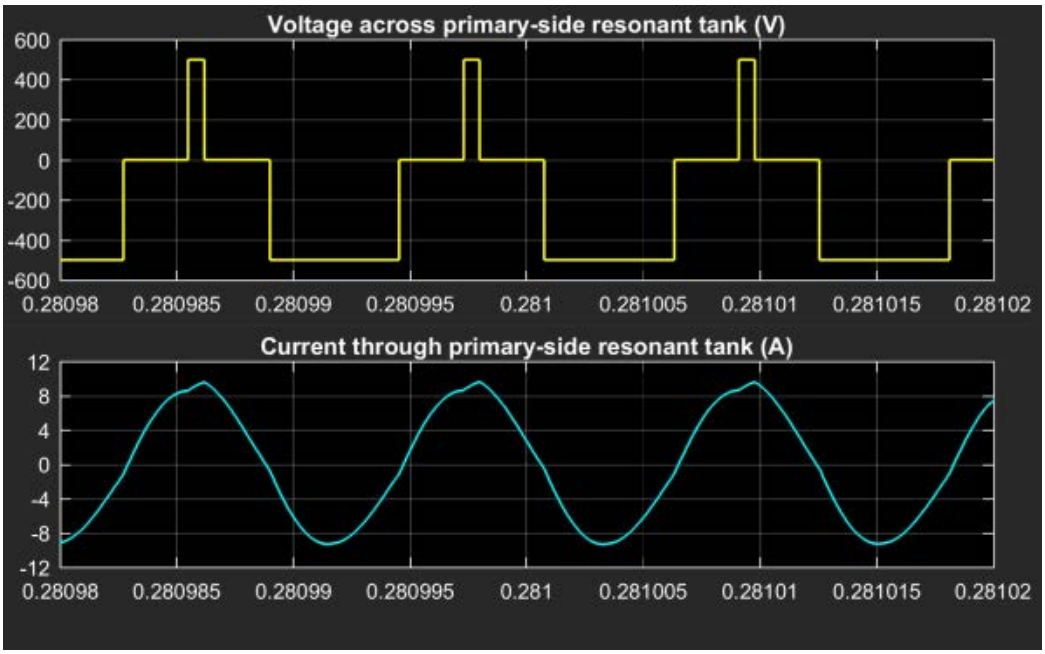


Fig. IV-11. Voltage and current of primary-side resonant tank (v_{AB} and i_r) at 100% load condition (high frequency profile at 0.281 s)

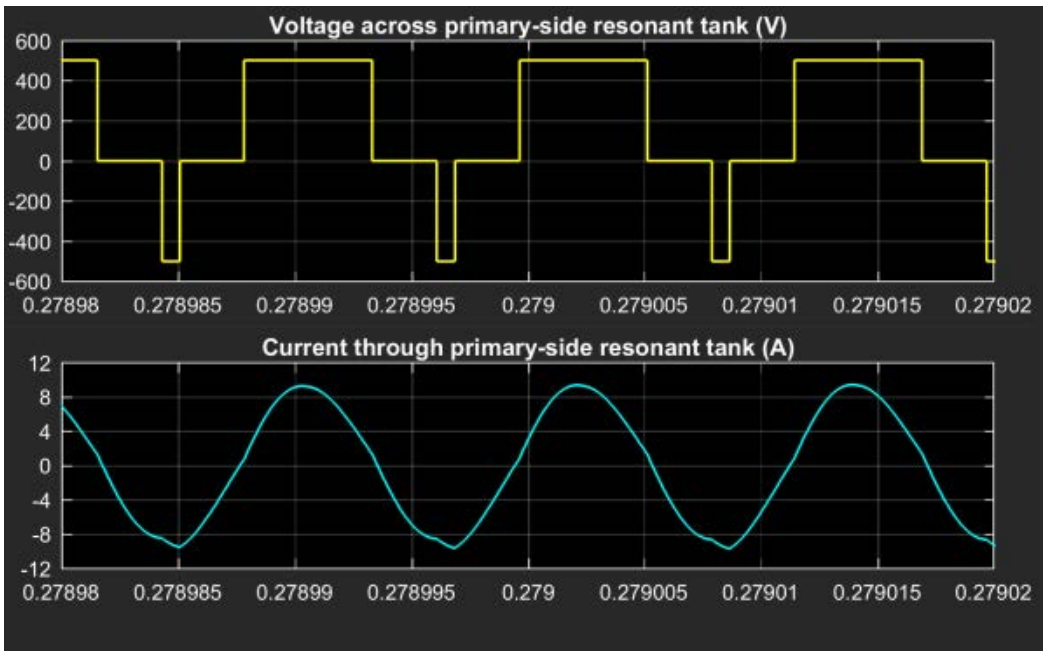


Fig. IV-12. Voltage and current of primary-side resonant tank (v_{AB} and i_r) at 100% load condition (high frequency profile at 0.279 s)

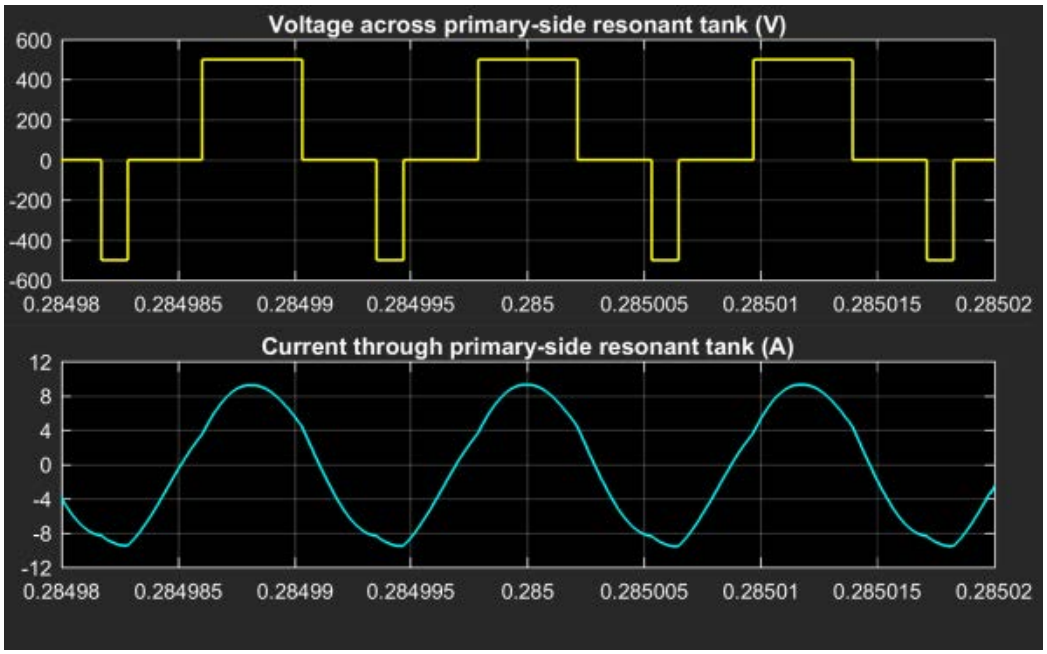


Fig. IV-13. Voltage and current of primary-side resonant tank (v_{AB} and i_r) at 100% load condition (high frequency profile at 0.285 s)

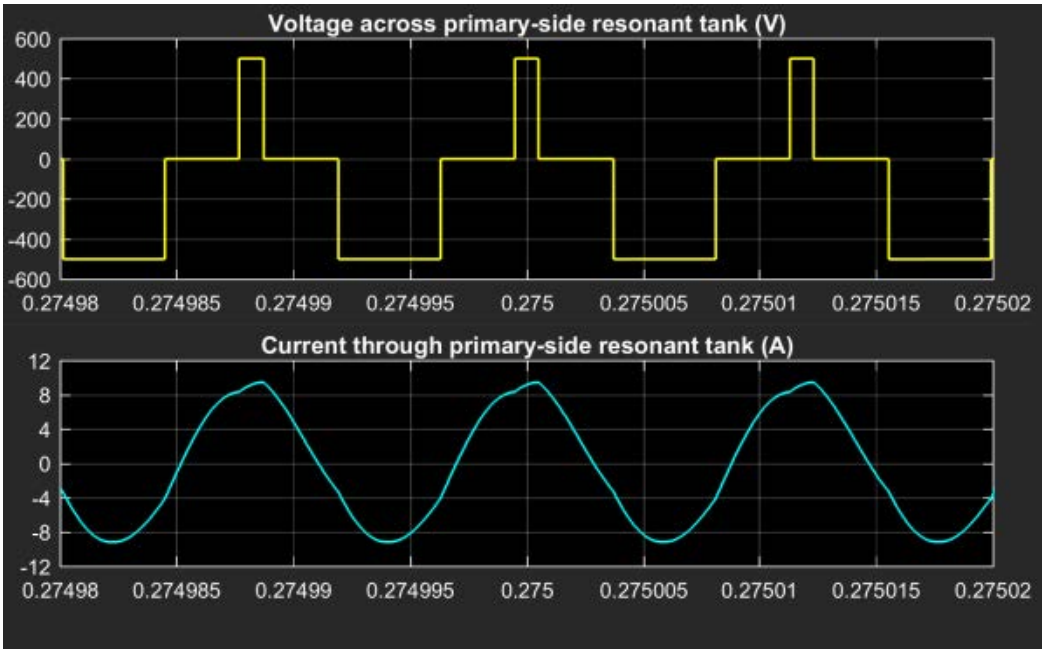


Fig. IV-14. Voltage and current of primary-side resonant tank (v_{AB} and i_r) at 100% load condition (high frequency profile at 0.275 s)

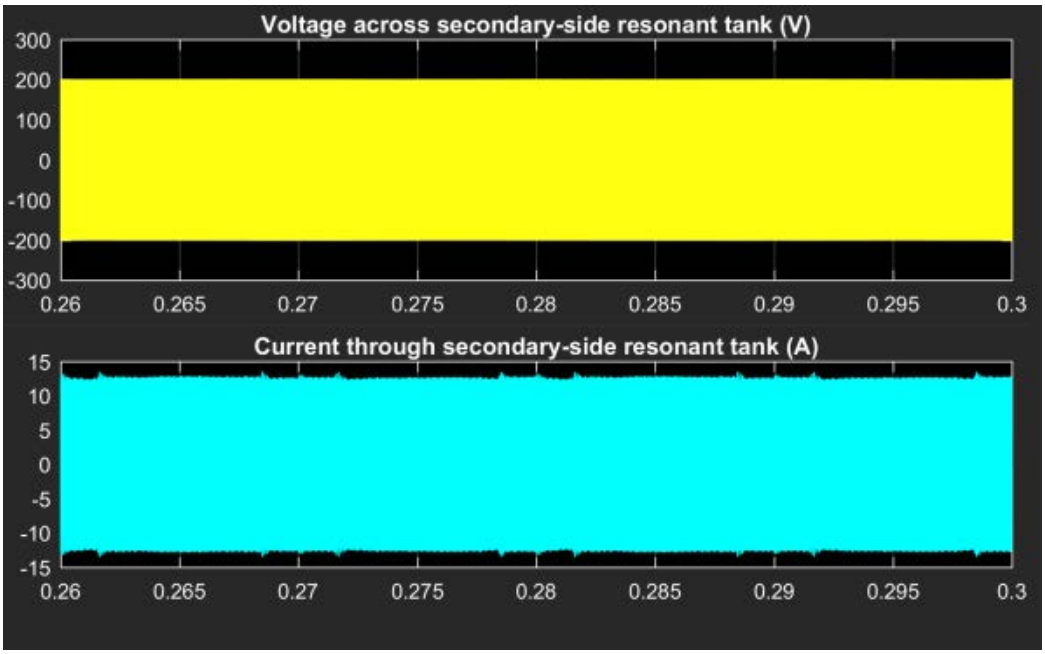


Fig. IV-15. Voltage and current of secondary-side resonant tank (v_{CD} and i_{rs}) at 100% load condition (low frequency profile)

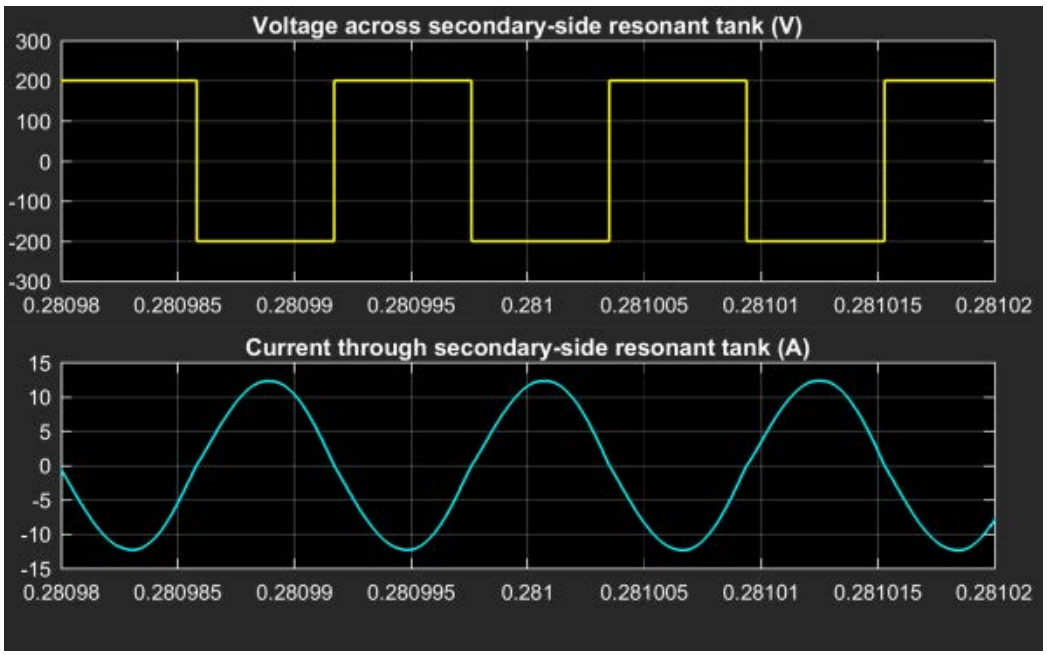


Fig. IV-16. Voltage and current of secondary-side resonant tank (v_{CD} and i_{rs}) at 100% load condition (high frequency profile at 0.281 s)

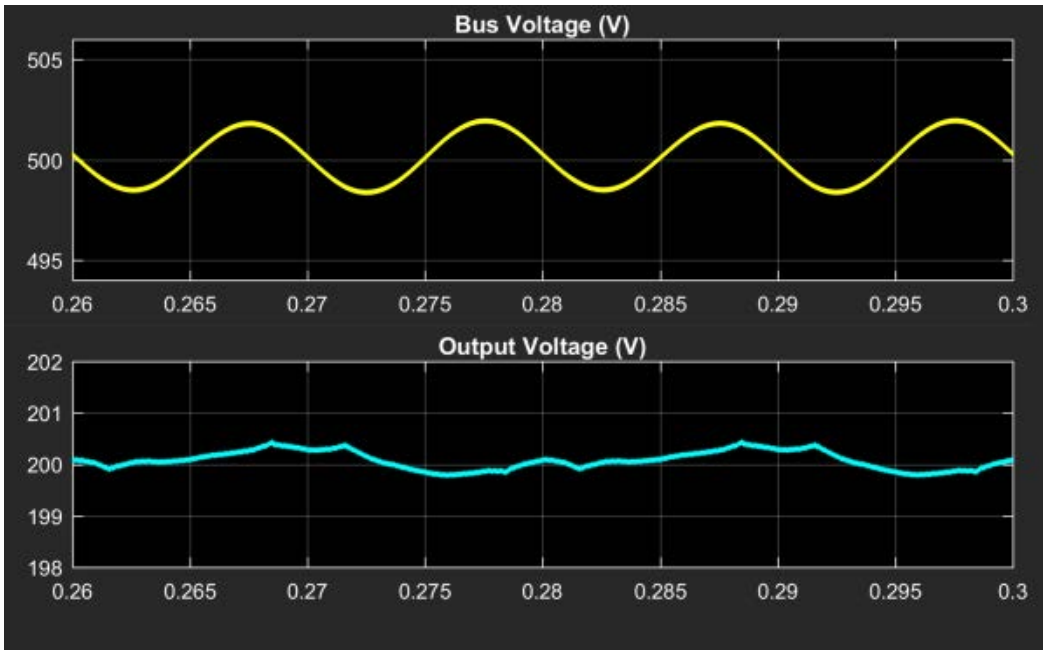


Fig. IV-17. Bus voltage and output voltage at 100% load condition (low frequency profile)

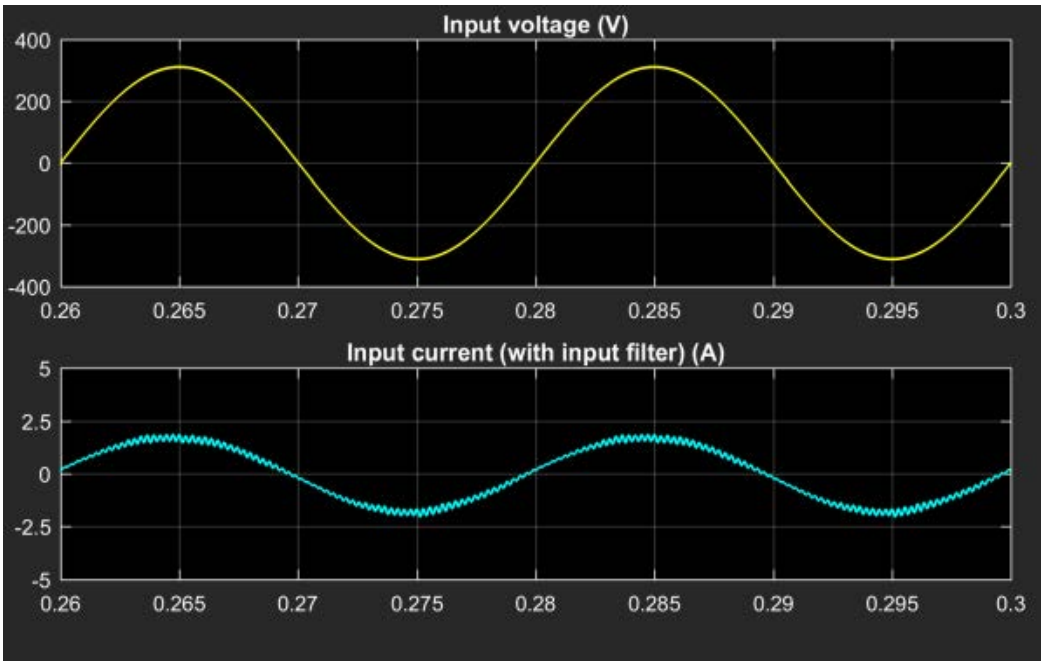


Fig. IV-18. Input voltage and current with input filter (v_s and i_s) at 10% load condition (low frequency profile)

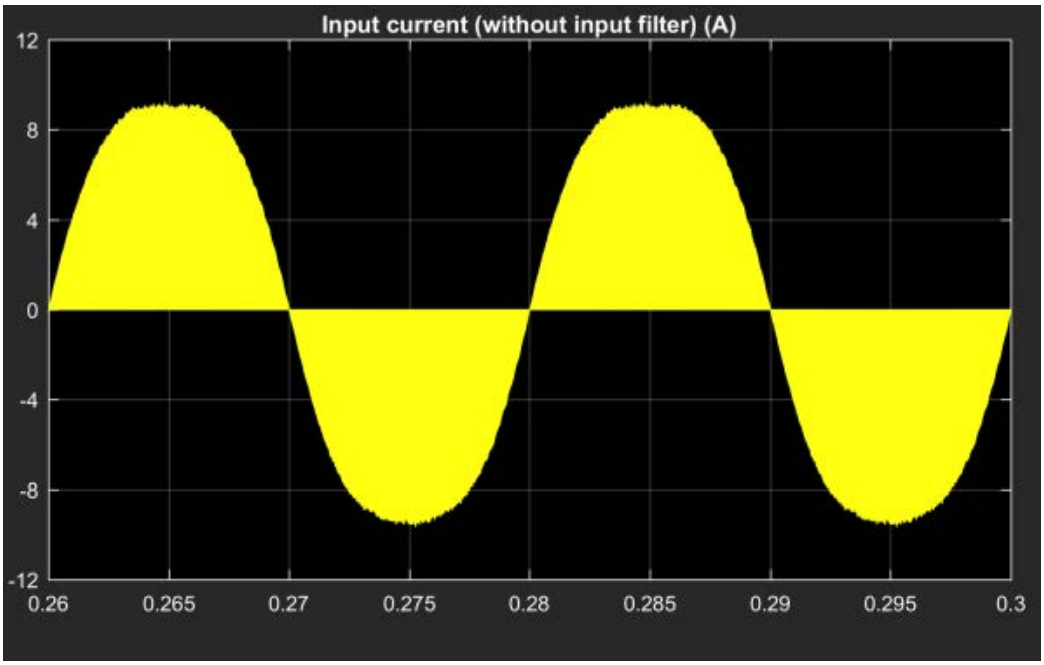


Fig. IV-19. Input current without input filter (i_{in}) at 10% load condition (low frequency profile)

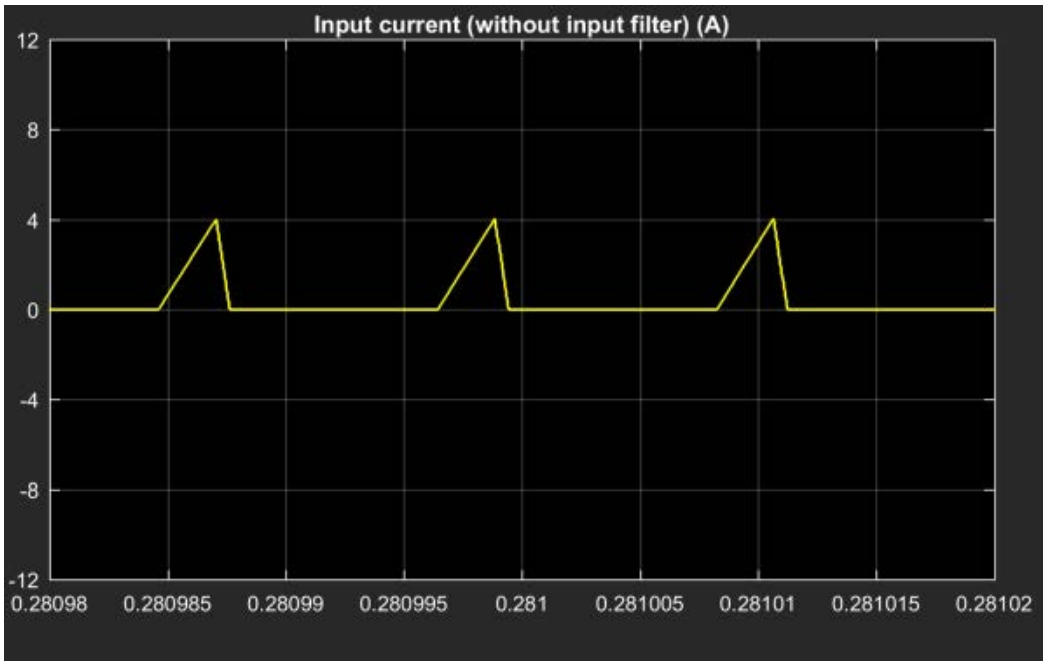


Fig. IV-20. Input current without input filter (i_{in}) at 10% load condition (high frequency profile at 0.281 s)

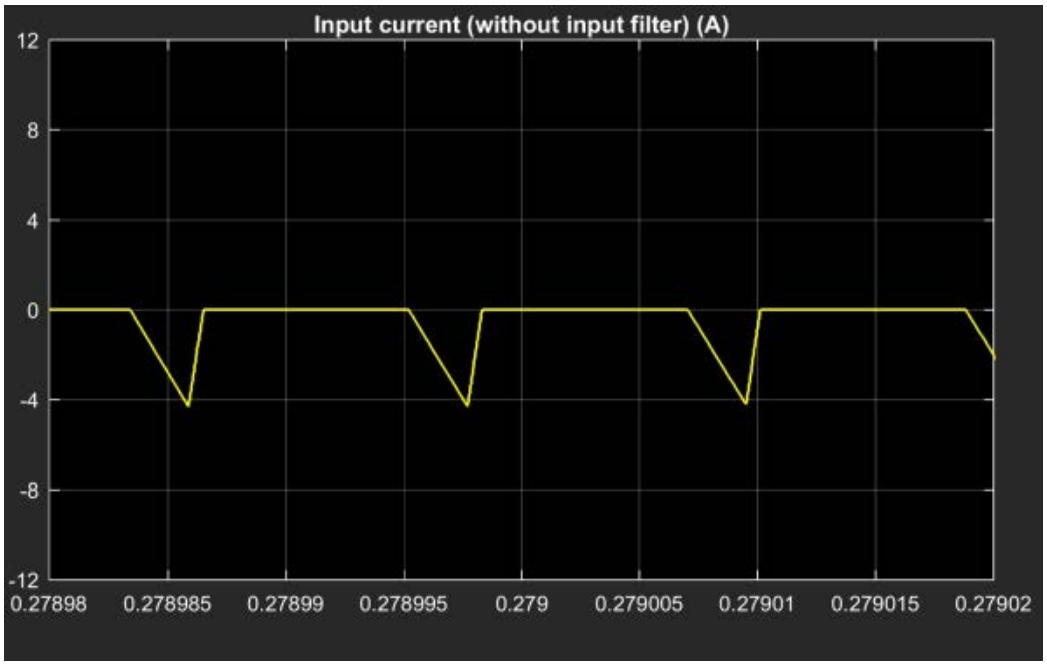


Fig. IV-21. Input current without input filter (i_{in}) at 10% load condition (high frequency profile at 0.279 s)

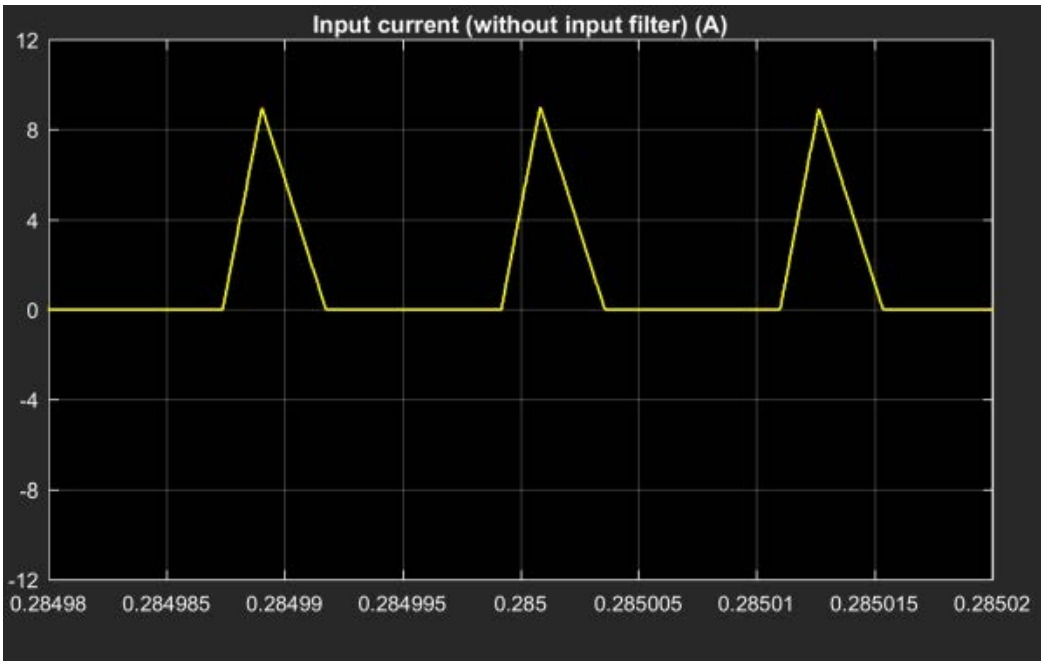


Fig. IV-22. Input current without input filter (i_{in}) at 10% load condition (high frequency profile at 0.285 s)

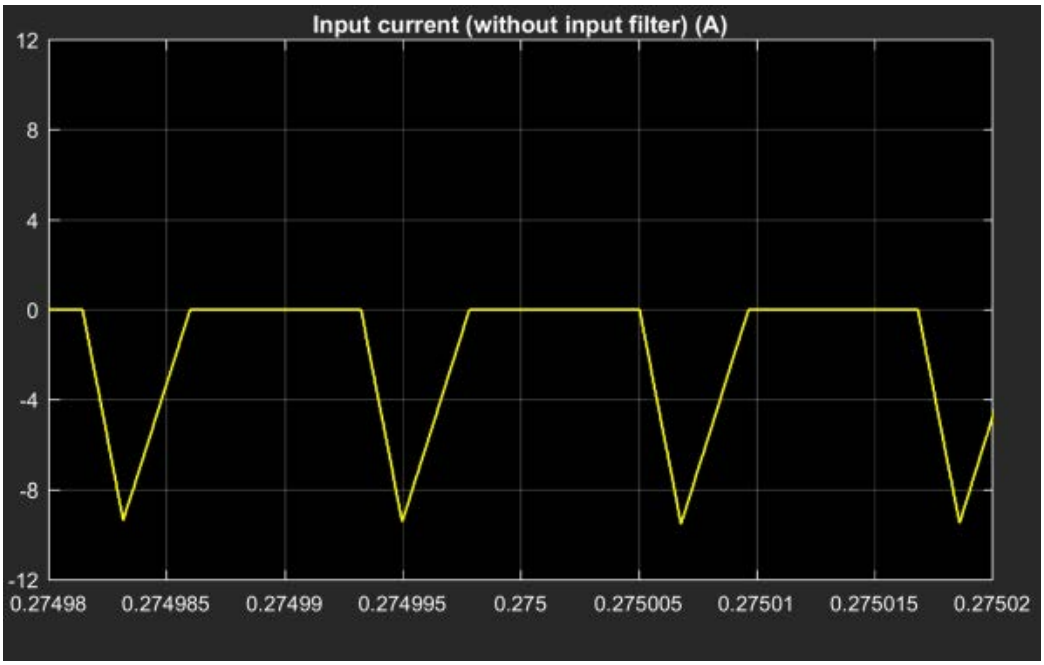


Fig. IV-23. Input current without input filter (i_{in}) at 10% load condition (high frequency profile at 0.275 s)

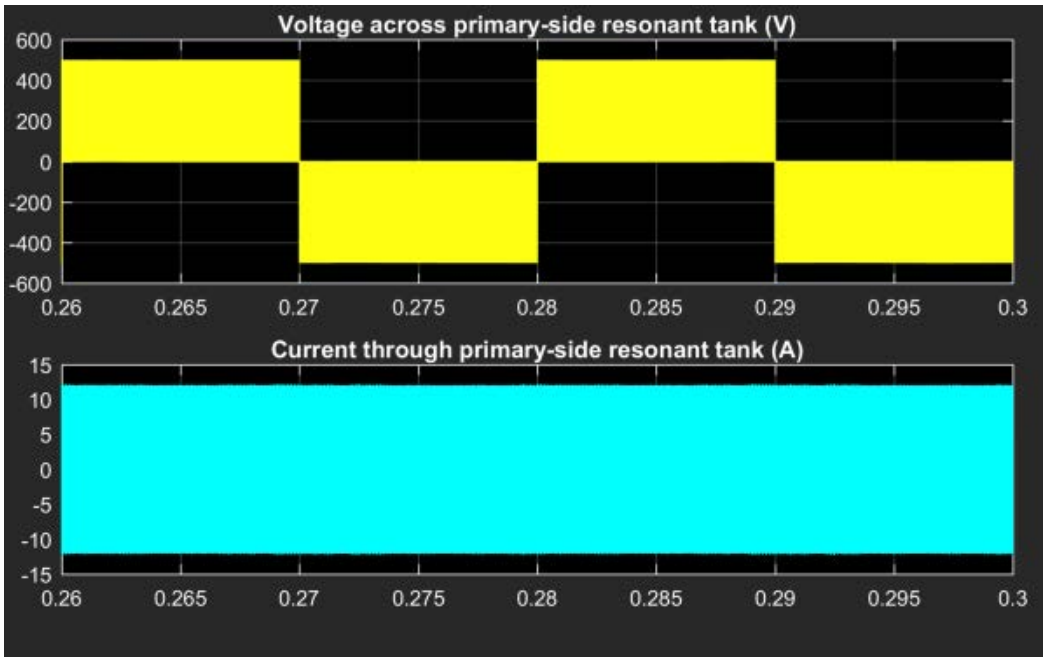


Fig. IV-24. Voltage and current of primary-side resonant tank (v_{AB} and i_r) at 10% load condition (low frequency profile)

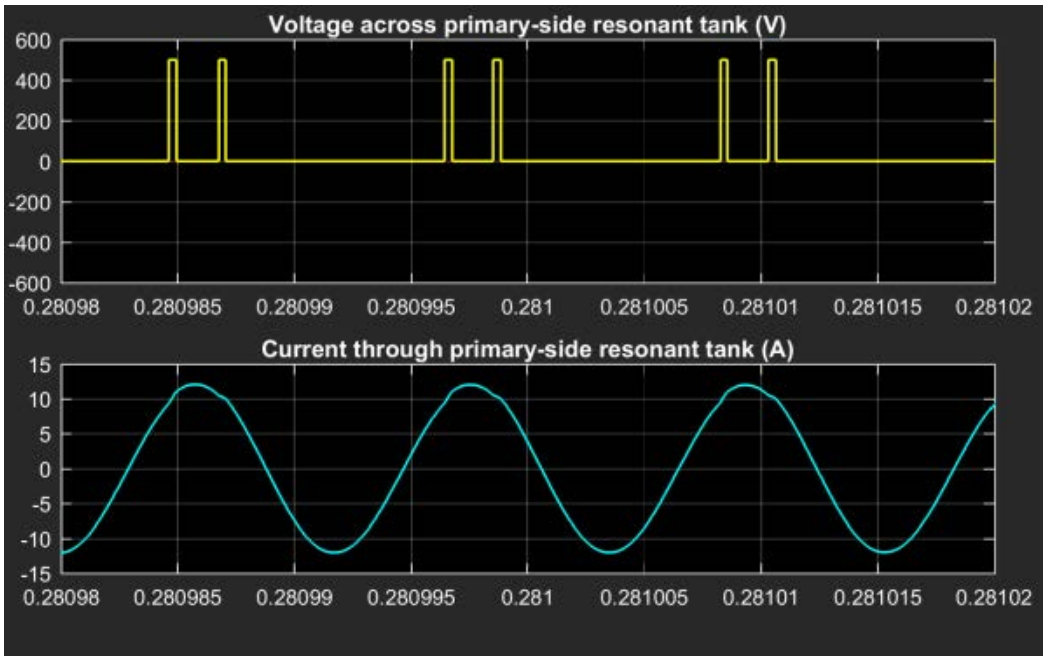


Fig. IV-25. Voltage and current of primary-side resonant tank (v_{AB} and i_r) at 10% load condition (high frequency profile at 0.281 s)

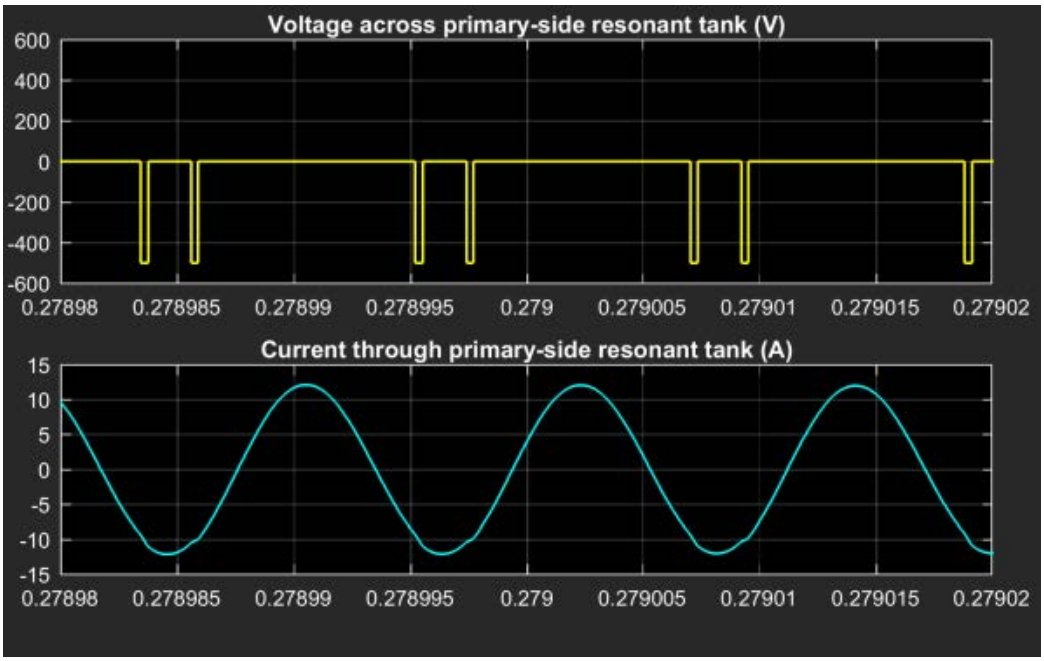


Fig. IV-26. Voltage and current of primary-side resonant tank (v_{AB} and i_r) at 10% load condition (high frequency profile at 0.279 s)

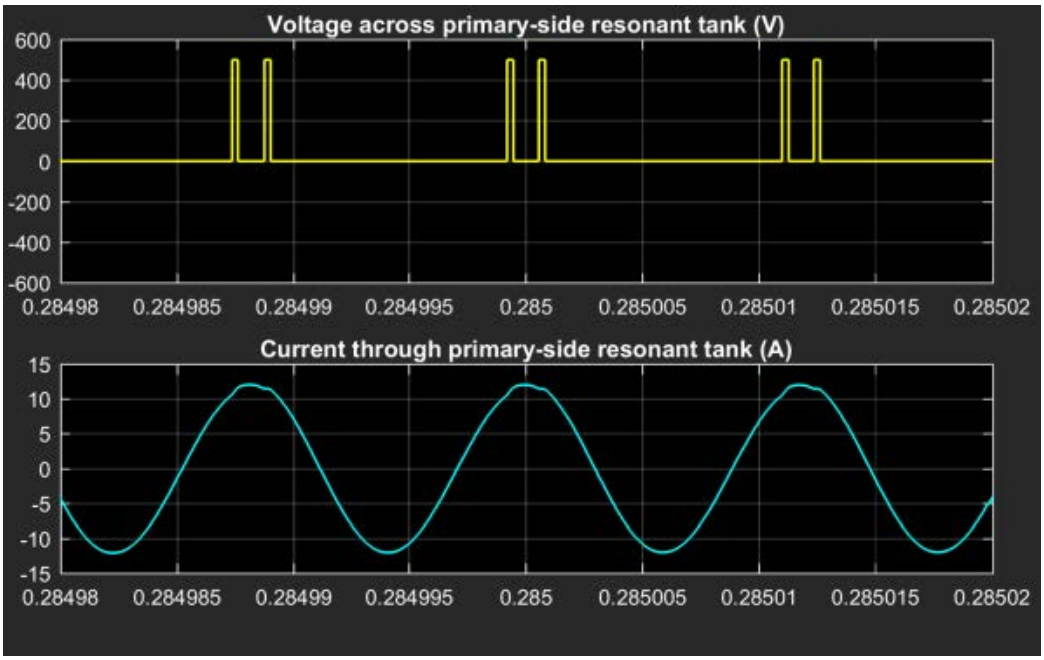


Fig. IV-27. Voltage and current of primary-side resonant tank (v_{AB} and i_r) at 10% load condition (high frequency profile at 0.285 s)

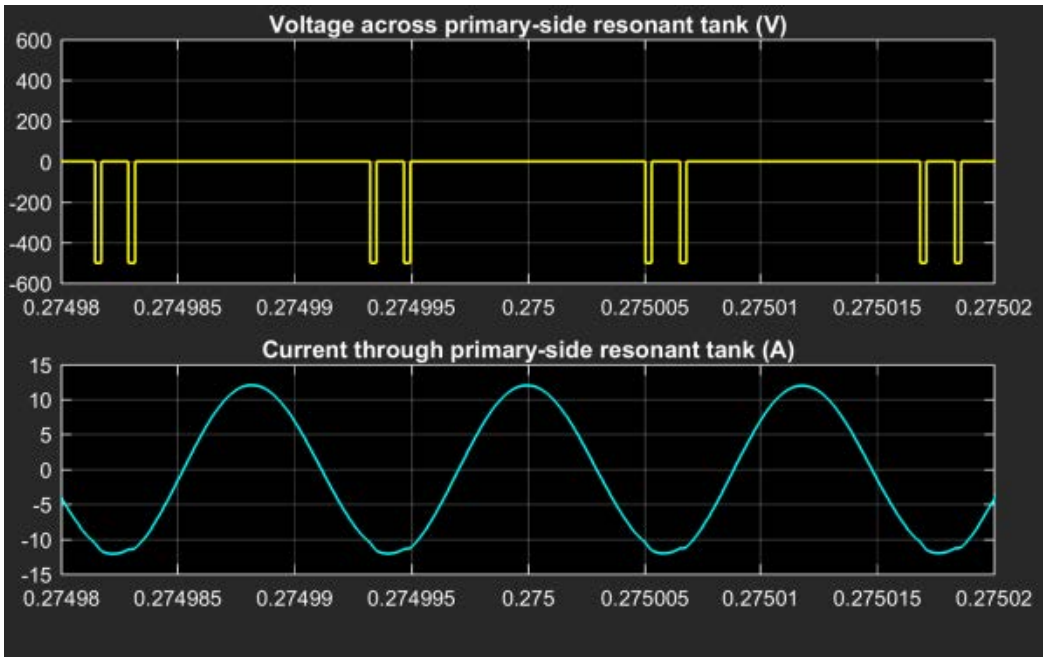


Fig. IV-28. Voltage and current of primary-side resonant tank (v_{AB} and i_r) at 10% load condition (high frequency profile at 0.275 s)

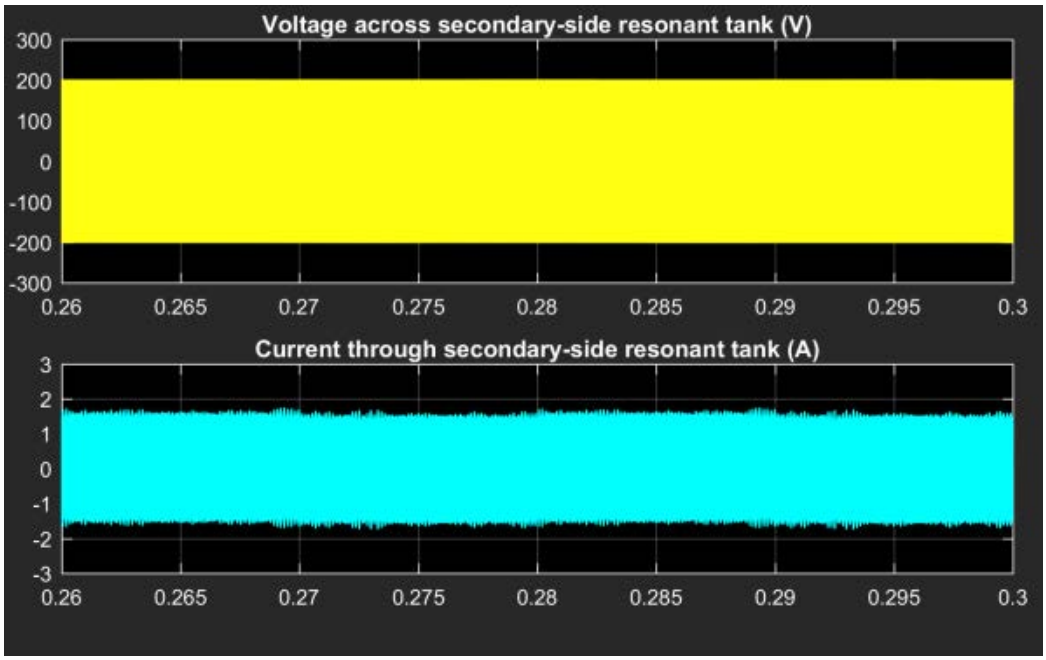


Fig. IV-29. Voltage and current of secondary-side resonant tank at 10% load condition (low frequency profile)

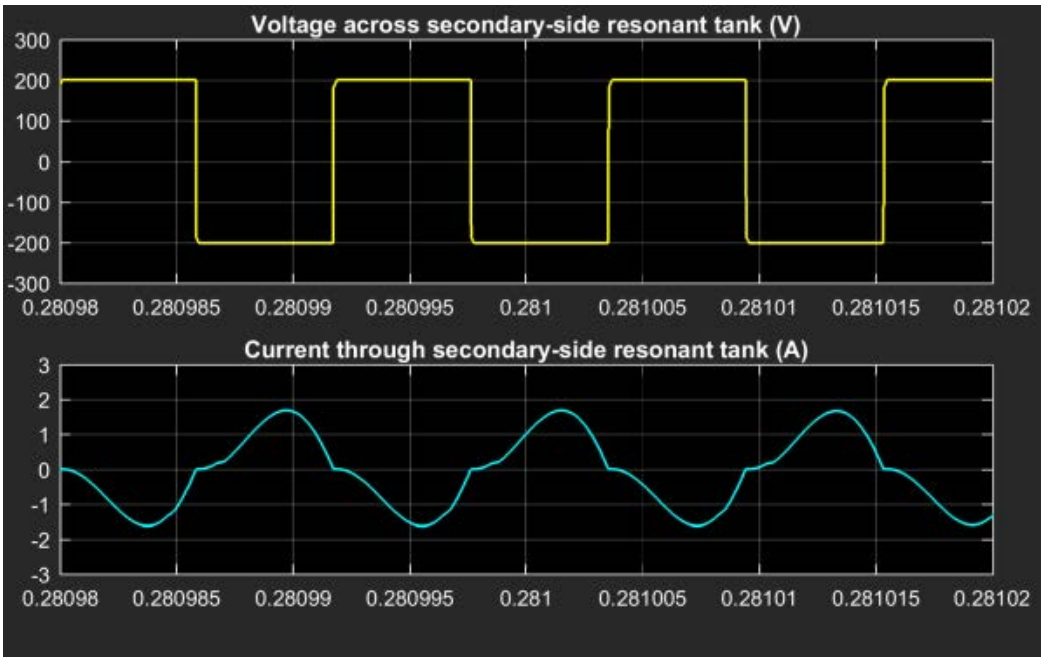


Fig. IV-30. Voltage and current of secondary-side resonant tank at 10% load condition (high frequency profile at 0.281 s)

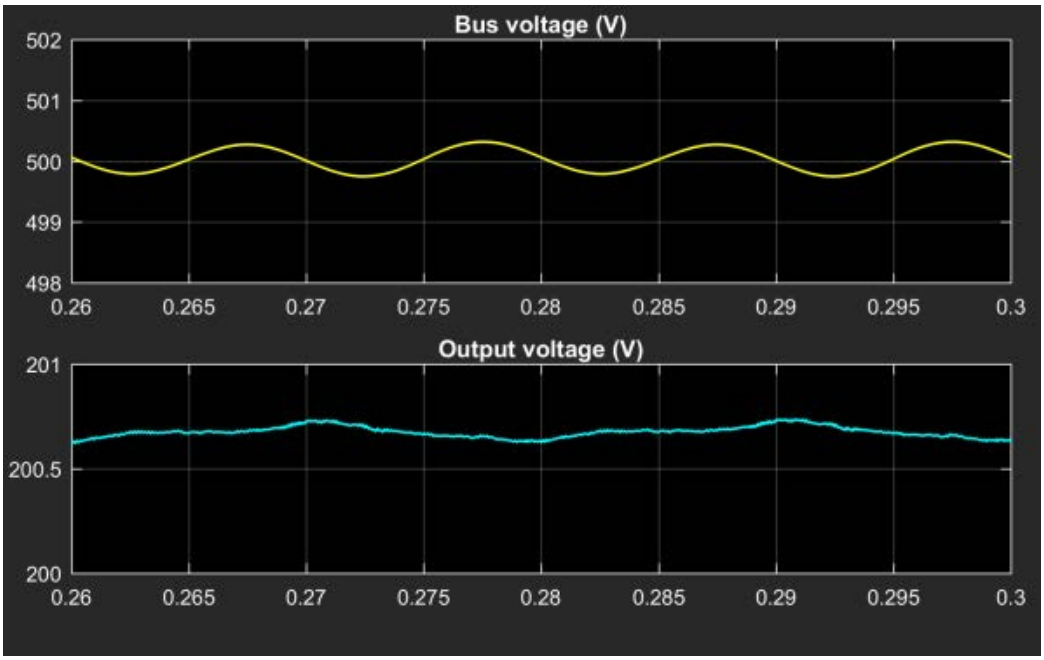


Fig. IV-31. Bus voltage and output voltage at 10% load condition (low frequency profile)

IV.6 Discussion and Conclusion

This chapter proposed a new control method of single-phase single-stage WPT resonant converter, which exhibits much better power quality with PF higher than 0.99 and THD_i lower than 1% and significant reduced bus voltage of 500V, compared with the original method with PF lower than 0.99 and THD_i higher than 15.4% and bus voltage of 723.5 V in Chapter III. Also making the resonant tank working at middle resonant frequency contributes good WPT efficiency. Therefore, the performance of the proposed control method is better than that proposed in Chapter III except for the control and modulation method using two control parameters, which is a little more complicated than that of Chapter III. However, it can be realized with assistance of MCU and FPGA or CPLD easily. This control method is generally suitable for the environment with very high requirement on maintaining power quality. Due to reduction of bus voltage, voltage rating of power switches can also be reduced, and so as the cost of power switches.

Chapter V
Three-phase Single-Stage AC-DC Wireless-Power-Transfer Resonant Converter with Power-Factor-Correction

V.1 Introduction

Power of WPT system is usually drawn from 50/60 Hz single-phase or three-phase AC source. The latter is commonly used for high power applications. Conventionally a high power WPT system consists of two stages: the first stage is a three-phase AC-DC rectifier with PFC; and the second stage is DC-DC WPT resonant converter. There have been many researches on three-phase AC-DC rectifier, including boost type [109], [110], [137], buck-boost type [111], and others. Those topologies have at least one active switch. A DC-DC WPT resonant converter consists of a high-frequency inverter, coupled primary and secondary resonant tanks, a secondary high-frequency rectifier-bridge, a filter capacitor and a load. Generally two-stage topology for WPT system needs two control strategies for both stages, which obviously increases the control complexity of the system. In addition, such two-stage topology cannot achieve a highest efficiency due to more power losses in the two-stage conversion. Moreover, it is also not the most economical because two-stage conversion means more components.

In recent years, three-phase single-stage AC-DC topologies [112] – [119] that integrate both AC-DC rectifier with PFC and DC-DC conversion into only one power conversion stage have been proposed to overcome the aforementioned drawbacks. However, most of them are focused on transformer-based isolated power conversion, not WPT systems. Some researchers proposed single-phase and

three-phase single-stage AC-AC matrix converters for WPT system [138], [139]. However, they are not suitable for WPT system with a constant DC voltage output. Chapter III proposes a single-phase single-stage AC-DC topology for WPT system, which provides a constant DC output voltage. However, since its single-phase topology, its power quality is not as good as that of three-phase single-stage topology and its bus voltage is too high at low load condition.

Here, a new concept of three-phase single-stage AC-DC topologies is proposed to apply in WPT system: a three-phase, single-stage, T-type, WPT resonant converter. It is capable of improving the efficiency and power quality, lowering the cost, and minimizing count of power semiconductor devices. Many single-stage AC-DC topologies suffer the problem of too high bus voltage [115], [140]. This problem can be mitigated in the proposed converter because bus voltage control method is proposed. It is realized through regulating frequency and duty cycle, by utilizing and integrating the characteristics of three-phase AC-DC rectifier and DC-DC WPT converter. Such method can optimize performance of power quality of three-phase voltage source as well as fulfill the requirement of bus voltage.

In this chapter, topology description and analysis, power factor (PF) and total harmonics distortion (THD) analysis, control method and circuit operation of the proposed converter are presented. Then, design procedure and example are proposed. Finally, an experimental prototype is implemented to verify the analysis and design.

V.2 Proposed Topology

V.2.1 Topology description

Fig. V-1 shows the proposed novel topology. Firstly a three-wire three-phase voltage source connects with an input filter for filtering the high frequency components and zero-sequence components of three phase currents. Followed by the input filter are three input inductors (with the same values), three diode-legs (6

diodes), and a T-type inverter (four switches and two bus capacitors), which are formed together to perform the three-phase PFC functionality. The T-type inverter also connects a resonant tank (resonant capacitors and inductors of primary and secondary side), a secondary-side diode rectifier bridge, an output filtering capacitor, and a load resister, to perform DC-DC WPT conversion functionality.

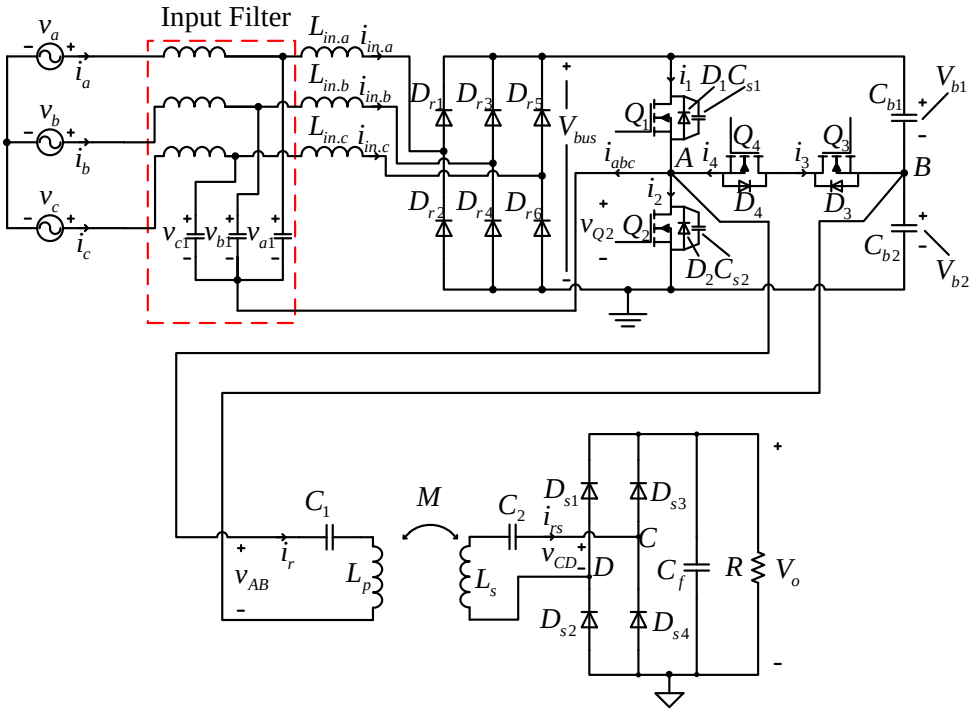


Fig. V-1. Topology of proposed three-phase, single-stage, T-type, WPT converter

V.2.2 T-type three-level high frequency inverter

Fig. V-2 (a) shows the T-type three-level high frequency inverter, with high-side mosfet Q_1, low-side mosfet Q_2, middle-side mosfets Q_3 and Q_4. Output voltage of this converter, v_{AB}, can be configured to be a three-level waveform. With the modulation method shown in Fig. V-2 (b), duty cycle of v_{AB}, D_{ab} (ratio of non-zero voltage in a switching period T_s) is adjustable and output current i_o commutates naturally in spite of its direction [141]. Compared to full bridge inverter, voltage stress of Q_3 and Q_4 reduces to half of the bus voltage while conduction loss when v_{AB} is positive or negative also reduces significantly.

Compared to three-level NPC inverter, simpler modulation method, less semiconductor number, less conduction loss, and less isolated driver power supplies are the significant advantages of the T-type inverter [141].

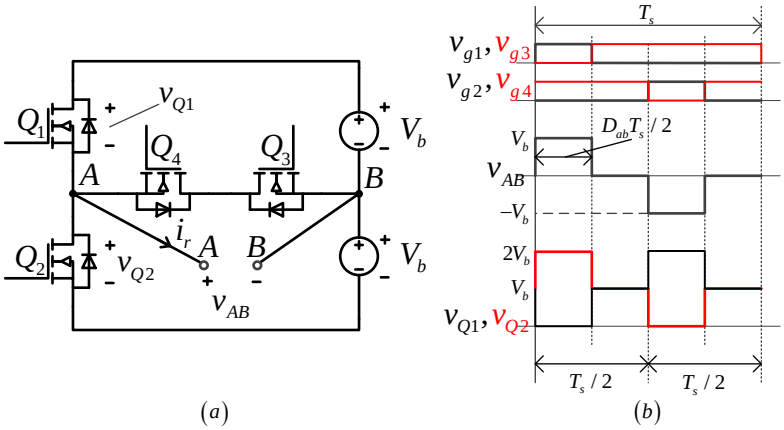


Fig. V-2. (a) T-type three-level high frequency inverter; (b) Modulation waveforms of the T-type inverter, where V_b is equivalent DC voltage source.

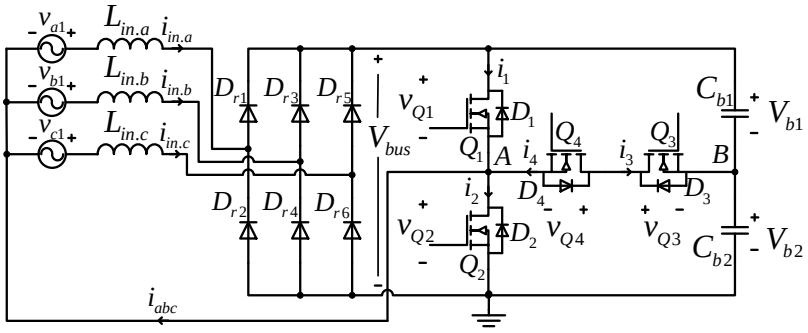


Fig. V-3. Proposed three-phase PFC converter stage with equivalent three-phase voltage sources v_{a1}, v_{b1}, and v_{c1}

V.2.3 Three-Phase power-factor-correction stage

A. Working principle and analysis

Fig. V-3 shows the three-phase PFC converter stage with equivalent three-phase voltage source (voltage after input filter). The three-phase PFC converter stage consists of 3 input inductors, 6 low frequency diodes, 2 series-connected bus capacitors, and a T-type converter. $L_{in.a}$, $L_{in.b}$, $L_{in.c}$ are three

phase input inductors with the same inductance L_{in}, $i_{in.a}$, $i_{in.b}$, $i_{in.c}$ are currents flowing through $L_{in.a}$, $L_{in.b}$, and $L_{in.c}$, respectively. i_{abc}, is the sum of $i_{in.a}$, $i_{in.b}$, and $i_{in.c}$. D_{r1}, D_{r2}, D_{r3}, D_{r4}, D_{r5}, and D_{r6} are low frequency diodes. V_{bus} is bus voltage of two bus capacitors C_{b1} and C_{b2} in series together. V_{b1} and V_{b2} are voltages of C_{b1} and C_{b2} respectively and $V_{b1} = V_{b2} = V_{bus}/2 = V_b$. Fig. V-4 (b) gives the operation waveforms of three phase currents $i_{in.a}$, $i_{in.b}$, and $i_{in.c}$. Their operation principle is the same. In the following analysis, v_{x1} refers to v_{a1}, v_{b1}, or v_{c1} and $i_{in.x}$ refers to $i_{in.a}$, $i_{in.b}$ or $i_{in.c}$.

When v_{x1} is at its positive cycle, $i_{in.x}$ can behave as condition 1 or 2, where voltage across $L_{in.x}$ is $v_{x1} - v_{Q1}$; when v_{x1} is at its negative cycle, $i_{in.x}$ can behave as condition 3 or 4, where voltage across $L_{in.x}$ is $v_{x1} + v_{Q2}$, as shown in Fig. V-4 (b). $i_{in.x}$ as conditions 1, 2, 3, and 4 are all working in discontinuous current mode (DCM), which is capable of reducing higher harmonics and performing PFC functionality. Firstly, v_{x1} is expressed as:

$$v_{x1} = v_x = V_{sp} \sin\left(\omega_l t - \varphi_x\right), x = a, b, c, \tag{5.1}$$

where V_{sp} is peak value, ω_l is line frequency in radian, and φ_x is initial phase (φ_a=0, φ_b=2π/3, φ_c=4π/3). The limitation of $i_{in.x}$ working in DCM is:

$$V_{sp} \le V_{bus}/2. \tag{5.2}$$

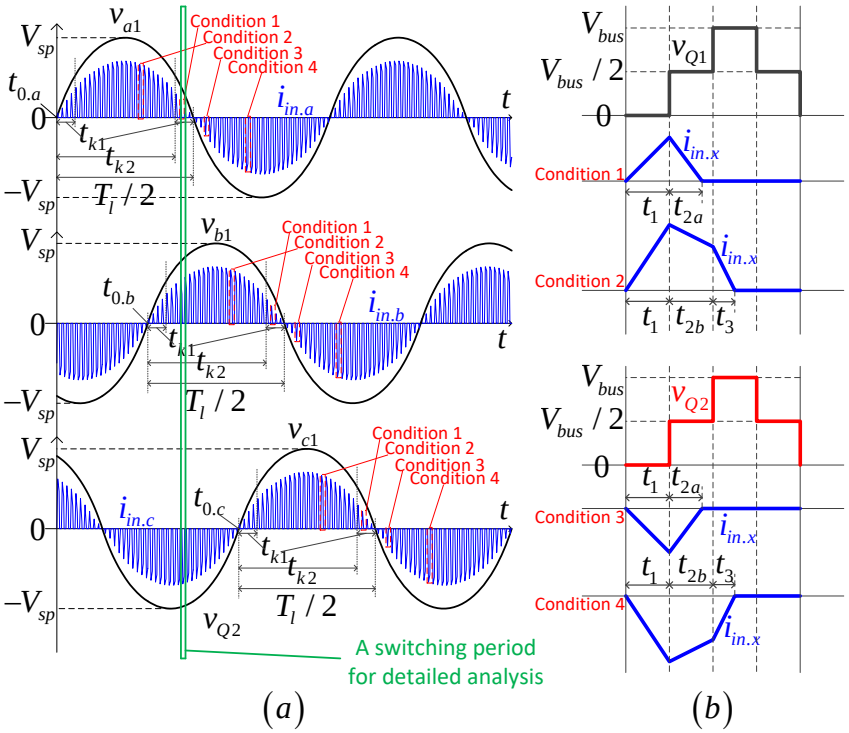


Fig. V-4. Waveforms of v_{x1} and $i_{in.x}$ (x=a, b, and c): (a) low frequency profile; (b) high frequency profile

Note V_{sp}/V_{bus} as m, and the limitation is:

$$m \le 0.5. \tag{5.3}$$

When $i_{in.x}$ working in condition 1, current increases from zero to peak value during t_1 and then decreases from peak value to zero during t_{2a}. Therefore,

$$\frac{v_{x1}}{L_{in}} \cdot t_1 + \frac{v_{x1} - V_{bus}/2}{L_{in}} \cdot t_{2a} = 0. \tag{5.4}$$

When in condition 2, current increases from zero to peak value during t_1 and then decreases from peak value to zero during t_{2b} and t_3 with two different slopes. Therefore,

$$\frac{v_{x1}}{L_{in}} \cdot t_1 + \frac{v_{x1} - V_{bus}/2}{L_{in}} \cdot t_{2b} + \frac{v_{x1} - V_{bus}}{L_{in}} \cdot t_3 = 0. \tag{5.5}$$

When in condition 3, current decreases from zero to negative peak value during t_1 and then increases from negative peak value to zero during t_{2a}. Therefore,

$$\frac{v_{x1}}{L_{in}} \cdot t_1 + \frac{v_{x1} + V_{bus}/2}{L_{in}} \cdot t_{2a} = 0. \tag{5.6}$$

When in condition 4, current decreases from zero to negative peak value during t_1 and then increases from negative peak value to zero during t_{2b} and t_3 with two different slopes. Therefore,

$$\frac{v_{x1}}{L_{in}} \cdot t_1 + \frac{v_{x1} + V_{bus}/2}{L_{in}} \cdot t_{2b} + \frac{v_{x1} + V_{bus}}{L_{in}} \cdot t_3 = 0, \tag{5.7}$$

where t_1 and t_{2b} are determined by D_{ab}:

$$t_1 = D_{ab}\, T_s/2, \;\; t_{2b} = (1 - D_{ab})\, T_s/2. \tag{5.8}$$

The boundary of condition 1 and 2 is $v_{x1}=V_{bus}(1-D_{ab})/2$ and the boundary of condition 3 and 4 is $v_{x1}=-V_{bus}(1-D_{ab})/2$. From (5.1) – (5.8), average value of $i_{in.x}$, $i_{\text{avg}.x}$ is expressed as:

When $0 \le \sin(\omega_l t - \varphi_x) \le \dfrac{(1 - D_{ab})}{2m}$,

$$i_{\text{avg}.x} = \frac{V_{sp} T_s}{L_{in}} \cdot \frac{D_{ab}{}^2 \sin(\omega_l t - \varphi_x)}{8(1 - 2m \sin(\omega_l t - \varphi_x))}; \tag{5.9}$$

When $\sin(\omega_l t - \varphi_x) > \dfrac{(1 - D_{ab})}{2m}$,

$$i_{\text{avg}.x} = \frac{V_{sp} T_s}{L_{in}} \cdot \frac{-(1/m)(1 - D_{ab})^2 + 2(1 + D_{ab}{}^2)\sin(\omega_l t - \varphi_x)}{32(1 - m \sin(\omega_l t - \varphi_x))}; \tag{5.10}$$

When $0 > \sin(\omega_l t - \varphi_x) \ge -\dfrac{(1 - D_{ab})}{2m}$,

$$i_{\text{avg}.x} = \frac{V_{sp} T_s}{L_{in}} \cdot \frac{D_{ab}{}^2 \sin(\omega_l t - \varphi_x)}{8(1 + 2m \sin(\omega_l t - \varphi_x))}; \tag{5.11}$$

When $\sin(\omega_l t - \varphi_x) < -\dfrac{(1 - D_{ab})}{2m}$,

$$\frac{V_{sp} T_s}{L_{in}} \cdot \frac{(1/m)(1 - D_{ab})^2 + 2(1 + D_{ab}{}^2)\sin(\omega_l t - \varphi_x)}{32(1 + m \sin(\omega_l t - \varphi_x))}. \tag{5.12}$$

If $m \leq (1-D_{ab})/2$, $i_{in.x}$ always works in condition 1 or 3. Because of the symmetrical characteristic of $i_{in.x}$ when v_{x1} in positive or negative cycle, input power of a phase can be calculated by average power in half a line period ($T_l/2$):

$$P_{in.x} = \frac{2}{T_l} \int_{t_{0.x}}^{t_{0.x}+T_l/2} i_{\text{avg1.}x} \cdot v_{x1} dt. \tag{5.13}$$

If $m > (1-D_{ab})/2$, $i_{in.x}$ works in all condition 1, 2, 3, and 4. Because of the symmetrical characteristic of $i_{in.x}$ when v_{x1} in positive or negative cycle, input power of a phase can be calculated by average power in half a line period ($T_l/2$):

$$P_{in.x} = \frac{2}{T_l}\left[\int_{t_{0.x}}^{t_{0.x}+t_{k1}} i_{\text{avg1.}x} v_{x1} dt + \int_{t_{0.x}+t_{k1}}^{t_{0.x}+t_{k2}} i_{\text{avg2.}x} v_{x1} dt + \int_{t_{0.x}+t_{k2}}^{t_{0.x}+T_l/2} i_{\text{avg1.}x} v_{x1} dt \right], \tag{5.14}$$

where $t_{0.x}=\varphi_x/\omega_l$ ($x=a$, b, or c) and

$$t_{k1} = \frac{1}{\omega_l} \arcsin\left(\frac{V_{bus}}{2V_{sp}} (1-D_{ab}) \right), \tag{5.15}$$

$$t_{k2} = \frac{1}{\omega_l}\left[\pi - \arcsin\left(\frac{V_{bus}}{2V_{sp}} (1-D_{ab}) \right) \right]. \tag{5.16}$$

Therefore, total input power is

$$P_{in} = P_{in.a} + P_{in.b} + P_{in.c}. \tag{5.17}$$

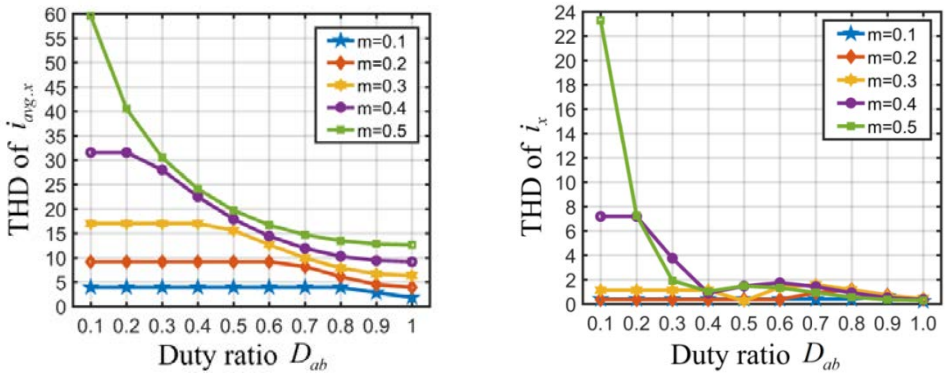
B. Analysis of THD and PF

From Fig. V-1, before the three-phase PFC converter stage is the input filter. The input filter eliminates high frequency components of $i_{in.x}$, as well as the zero-sequence components because of using artificial neutral point of the input filter [115]. Note the average current of $i_{in.x}$ as $i_{\text{avg.}x}$, which can be transformed to Fourier series and then its THD (only related to D_{ab} and m value) is obtained by calculation. Because zero-sequence components are eliminated, THD of i_x is much smaller than that of $i_{\text{avg.}x}$.

True PF is the result that displacement PF (PF_{dp}) multiplied with distortion PF (PF_{dt}). It can be analyzed that displacement PF is 1 theoretically and then true PF can be calculated by:

$$PF = PF_{dp} \cdot PF_{dt} = PF_{dt} = \frac{1}{\sqrt{1+THD_i^2}}. \tag{5.18}$$

Fig. V-5 shows the THD of $i_{avg.x}$ and i_x at different m conditions. It is obvious that THD of i_x is much lower than that of $i_{avg.x}$



(a) (b)

Fig. V-5. THD under different m conditions: (a) THD of $i_{avg.x}$; (b) THD of i_x

V.2.4 Single-stage operation and analysis

Input power can be obtained from (5.9) – (5.17) and output power P_o can be derived from (2.1) – (2.3). If the converter is designed with constant output voltage V_o, then P_o is:

$$P_o = \frac{V_o^2}{R} = \frac{8V_o^2}{\pi^2} \sqrt{\frac{\left(\frac{V_{sp} \cdot \sin\left(D_{ab}\,\pi/2\right)}{2mV_o}\right)^2 - \left(\frac{L_p}{M} - \frac{1}{\omega_s^2 C_1 M}\right)^2}{\left(\frac{\omega_s^2 L_p L_s - \frac{L_s}{C_1} - \frac{L_p}{C_2} + \frac{1}{\omega_s^2 C_1 C_2}}{\omega_s M} - \omega_s M\right)^2}}. \tag{5.19}$$

For single-stage operation, ideally P_{in} is equal to P_o at all times. Once P_{in} is not equal to P_o, V_{bus} will change in order to make them equal to realize steady-state

condition. By FHA method, the resonant tank and secondary side can be equivalent to an impedance Z_r, then the detailed operation analysis is given out with Fig. V-6 and Fig. V-7 – Fig. V-17. The waveforms of Fig. V-6 are taken from a switching period of Fig. V-4 (a).

Stage 1 ($t_0 - t_2$): From t_0 to t_2, Q_3 and Q_4 are ON, whereas Q_1 and Q_2 are OFF. At t_1, $i_{in.a}$ decreased to zero. Current paths of $t_0 - t_1$ and $t_1 - t_2$ are shown in Fig. V-7 and Fig. V-8 respectively.

Stage 2 ($t_2 - t_4$): At t_2, Q_4 is turned OFF and Q_2 is turned ON. At this instant, i_4 is negative because i_r is negative and its magnitude is larger than that of $i_{in.b}$. Hence, Q_4's turning OFF and Q_2's turning ON are hard switching. At t_3, $i_{in.b}$ decreased to zero. Current paths of $t_2 - t_3$ and $t_3 - t_4$ are shown in Fig. V-9 and Fig. V-10 respectively.

Stage 3 ($t_4 - t_6$): At t_4, Q_2 is turned OFF and C_{s2} starts to be charged by i_r and $i_{in.c}$. At t_5, C_{s2} is charged to $V_{bus}/2$ and D_4 starts to conduct. At t_6, v_{Q4} has been zero and Q_4 is turned ON. Q_2's turning OFF and Q_4's turning ON realize zero voltage switching (ZVS). Current paths of $t_4 - t_5$ and $t_5 - t_6$ are shown in Fig. V-11 and Fig. V-12 respectively.

Stage 4 ($t_6 - t_7$): From t_6 to t_7, Q_3 and Q_4 are ON, whereas Q_1 and Q_2 are OFF. Current path of this stage is shown in Fig. V-13.

Stage 5 ($t_7 - t_9$): At t_7, Q_3 is turned OFF and Q_1 is turned ON. At this instant, i_3 is negative because i_r is positive and its magnitude is larger than that of $i_{in.c}$. Hence, Q_3's turning OFF and Q_1's turning ON are hard switching. At t_8, $i_{in.c}$ increased to zero. Current paths of $t_7 - t_8$ and $t_8 - t_9$ are shown in Fig. V-14 and Fig. V-15 respectively.

Stage 6 ($t_9 - t_{11}$): At t_9, Q_1 is turned OFF and C_{s1} starts to be charged by i_r, $i_{in.a}$, and $i_{in.b}$. At t_{10}, C_{s1} is charged to $V_{bus}/2$ and D_3 starts to conduct. At t_{11}, v_{Q3} has been zero and Q_3 is turned ON. Q_1's turning OFF and Q_3's turning ON realize zero voltage switching (ZVS). Current paths of $t_9 - t_{10}$ and $t_{10} - t_{11}$ are shown in Fig. V-16 and Fig. V-17 respectively.

Stage 7 ($t_{11} - t_{12}$): This stage is the same with stage 1.

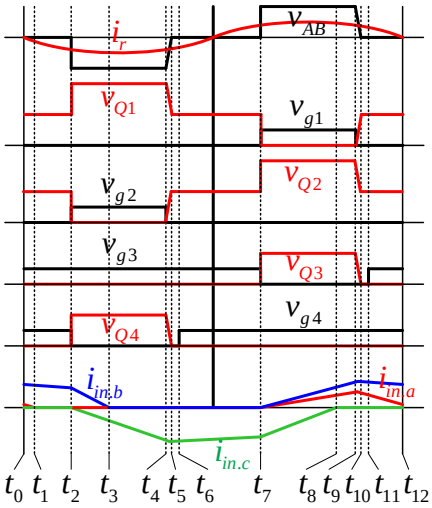


Fig. V-6. Operation waveforms during a switching period

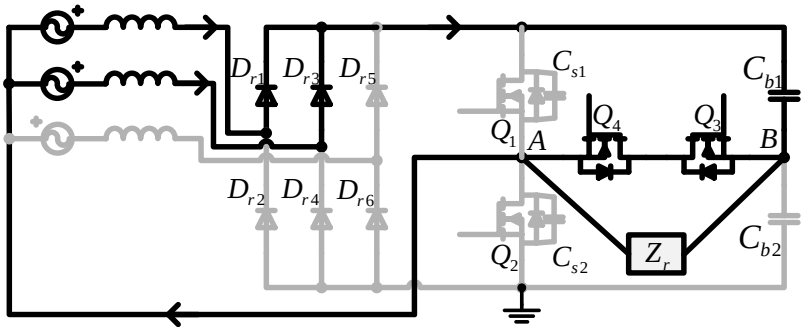


Fig. V-7. Operation modes during a switching period: $t_0 - t_1$

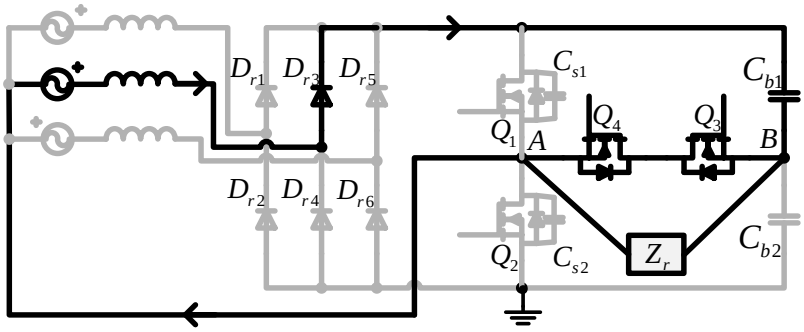


Fig. V-8. Operation modes during a switching period: $t_1 - t_2$

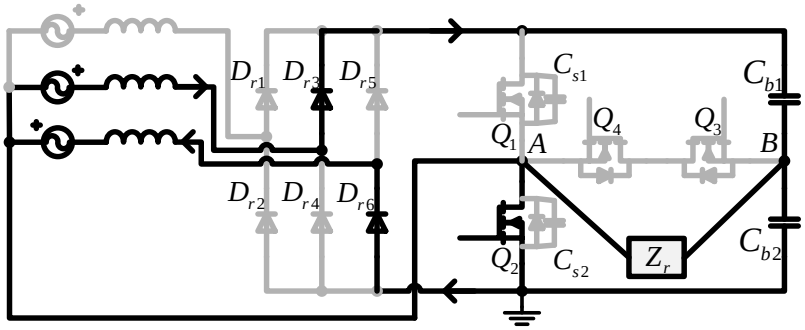


Fig. V-9. Operation modes during a switching period: $t_2 - t_3$

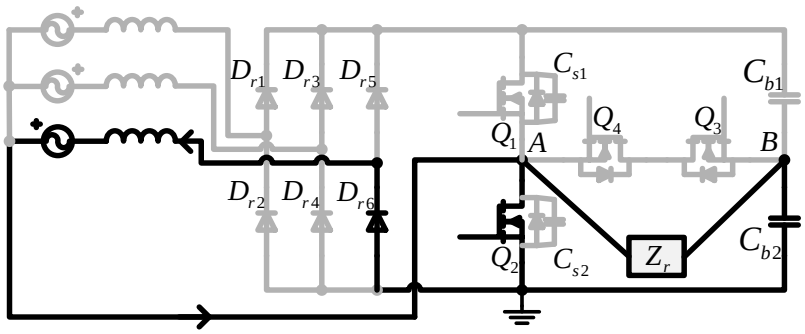


Fig. V-10. Operation modes during a switching period: $t_3 - t_4$

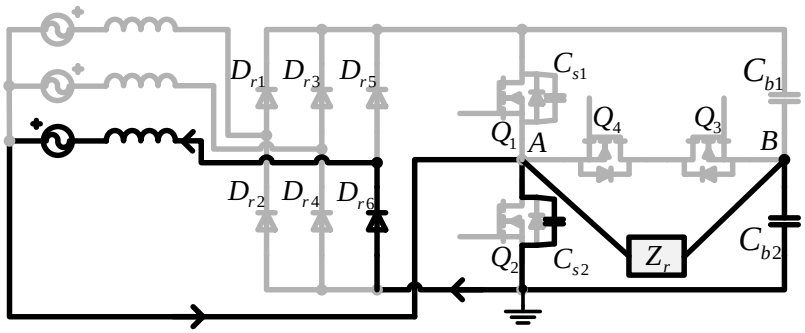


Fig. V-11. Operation modes during a switching period: $t_4 - t_5$

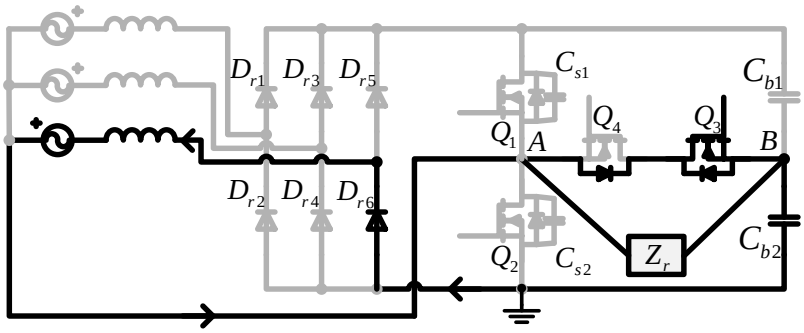


Fig. V-12. Operation modes during a switching period: $t_5 - t_6$

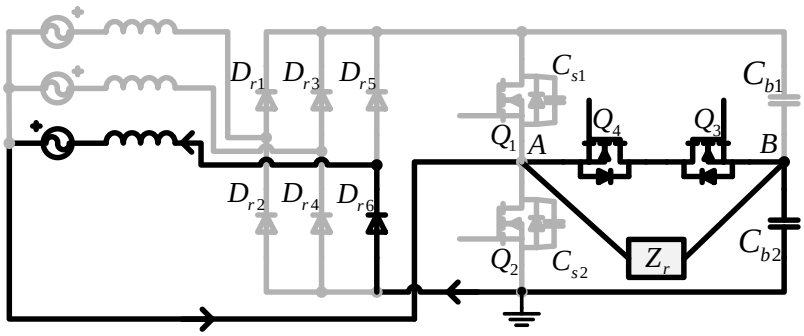


Fig. V-13. Operation modes during a switching period: $t_6 - t_7$

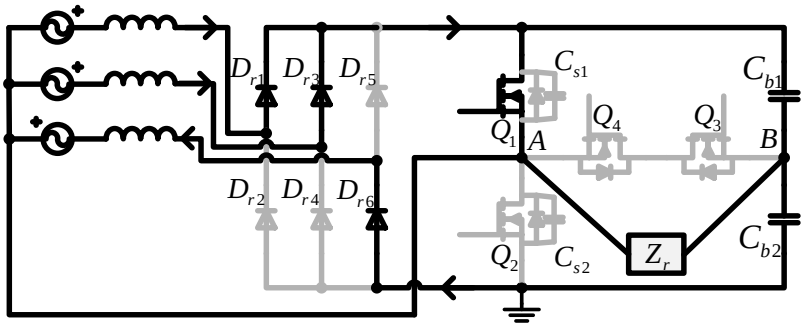


Fig. V-14. Operation modes during a switching period: $t_7 - t_8$

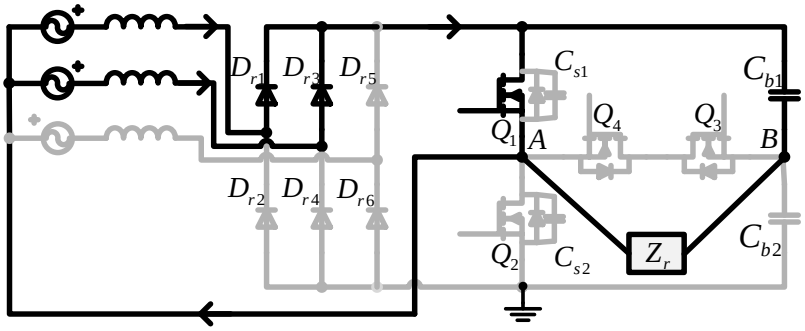


Fig. V-15. Operation modes during a switching period: $t_8 - t_9$

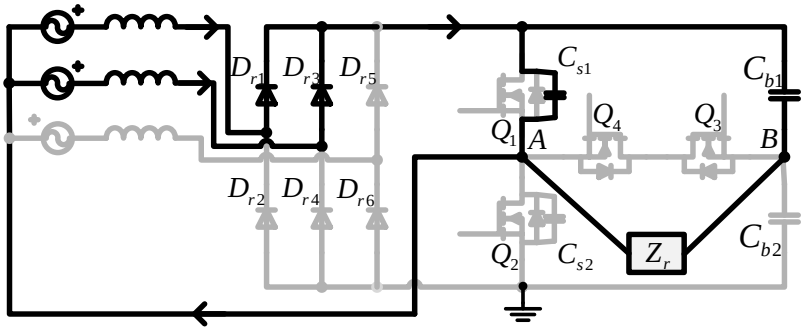


Fig. V-16. Operation modes during a switching period: $t_9 - t_{10}$

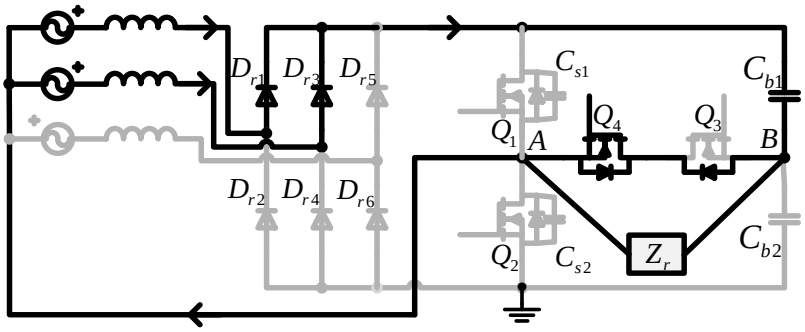


Fig. V-17. Operation modes during a switching period: $t_{10} - t_{11}$

V.2.5 Bus voltage control and operation

The bus voltage (V_{bus}) of the topology is very important as it decides the maximum voltage ratings of diodes $D_{r1} - D_{r6}$, switching devices $Q_1 - Q_4$, and bus capacitors C_{b1} and C_{b2}. Usually for single-stage topologies, bus voltage fluctuates

with load variations and could be very high at light load condition [140], [115]. Too high the bus voltage is unacceptable and therefore many single-stage topologies cannot work at light load condition or stand-by (zero-load) condition. In this chapter, a bus voltage control method is proposed to control V_{bus} stably within a full load range. In this analysis, input voltage is assumed to be constant (constant V_{sp}). If allowable maximum bus voltage $V_{bus.\max}$ is confirmed, then minimum m value ($m_{\min}$) will be obtained. From Fig. V-5, generally THD of i_x decreases with m value decreases (V_{bus} increases). Therefore, V_{bus} is controlled to be $V_{bus.\max}$ stably to obtain the best THD performance.

D_{ab} and f_s are two control parameters used for regulating output voltage V_o and bus voltage V_{bus}. Fig. V-18 shows the curves of P_{in} (dotted lines) and P_o (solid lines) under different D_{ab} and f_s conditions, with constant m value and V_o. The specific parameters are: L_{in} = 73.5 μH; L_p = L_s = 246 μH; C_1 = C_2 = 10.3 nF; M = 46 μH; m = 0.5; V_{sp} = 110$\sqrt{2}$ V; V_o = 250 V. There are six sets of curves with operation frequency: a1 and a2 (ω_s = ω_3); b1 and b2 (ω_s = 1.01*ω_3); c1 and c2 (ω_s = 1.02*ω_3); d1 and d2 (ω_s = 1.03*ω_3); e1 and e2 (ω_s = 1.04*ω_3); f1 and f2 (ω_s = 1.05*ω_3). At specific D_{ab} and f_s condition, when P_{in} is equal to P_o, V_o and V_{bus} will be stable. However, when P_{in} is larger than P_o, V_{bus} will increase and therefore V_o will increase and vice versa. Increasing f_s will decrease both P_{in} and P_o, however, the decrement of P_o is much larger than that of P_{in}, which means that increasing f_s can increase V_{bus}.

D_{ab} is mainly for V_o control and f_s is mainly for V_{bus} control. When V_o is detected to be higher, D_{ab} will be decreased; simultaneously, when V_{bus} is detected to be higher, f_s will be decreased, and vice versa. Black dots of Fig. V-18 are the real operation points at different load conditions. Such control method is capable to realize full load range operation and bus voltage control. From Fig. V-18, operation range of f_s within full load range is very small (smaller than 5% of f_3), so it is easy to design input EMI filter.

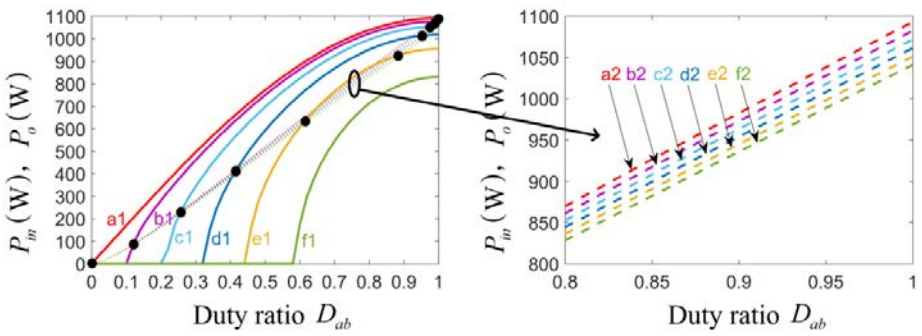


Fig. V-18. An example of P_{in} and P_o vs D_{ab} under different operation frequency. Curves a1 – f1: P_o vs. D_{ab} under ω_3, $1.01\omega_3$, $1.02\omega_3$, $1.03\omega_3$, $1.04\omega_3$, and $1.05\omega_3$ operation frequencies respectively. Curves a2 – f2: P_{in} vs. D_{ab} under ω_3, $1.01\omega_3$, $1.02\omega_3$, $1.03\omega_3$, $1.04\omega_3$, and $1.05\omega_3$ operation frequencies respectively. ω_3 refers to middle resonant frequency in radian.

V.3 Design Procedure and Considerations

V.3.1 Design procedure

To verify the design and control of the proposed topology, a 1.25-kW laboratory prototype with constant V_o is designed and implemented. The design procedures are given as follows:

1) Requirements of input and output:

Phase voltage v_x of the three phase voltage source is designed to be 110 V_{rms}, 50 Hz. Maximum output power $P_{o.max}$ is 1.25 kW, with constant output voltage V_o to be 250 V and hence maximum output current $I_{o.max}$ is 5 A (minimum load resistance R_{min} being 50 Ω).

2) Requirements of bus voltage:

$V_{bus.max}$ is designed to be 320 V and hence V_{bus} is kept to be $V_{bus.max}$ during full load range operation. Then, m value is obtained as $110\sqrt{2}/320 = 0.486$.

3) Minimum operation frequency $f_{s.min}$ and mutual inductance M:

From Fig. V-18, maximum output power condition occurs at the condition with D_{ab} being 1 and f_s being middle resonant frequency f_3, and $P_{o.max}$ is expressed as:

$$P_{o.\max} = \frac{2V_o V_{sp}}{\pi^3 m f_3 M}. \tag{5.20}$$

$f_{s.\min}$ is selected to be around 100 kHz in order to comply with the industrial wireless charging standard (SAE J1773). f_3 ($f_{s.\min}$) is set as 100 kHz and then mutual inductance M is calculated to be 41.3 μH.

4) Design of resonant tank:

For mid-range wireless power transfer, the coupling coefficient k of two resonant coils ranges from 0.1 to 0.2 [19], [126]. And considering for EV charging application, air gap distance d_{ag} of two coils is designed to be 200 mm. Therefore, integrating the known parameters of k, M, and d_{ag}, the two resonant coils are designed identically in spiral shape with average diameter d to be 500 mm and coils number N to be 16. To reduce AC resistance of resonant coils, litz wire with 100 strands (each strand's diameter is 0.2 mm) are used. The strand's diameter is smaller than two times of skin depth d_{sk}, which is obtained as:

$$d_{sk} = \sqrt{\frac{\rho}{\pi f_s \mu}} \approx 0.2\text{mm}, \tag{5.21}$$

where ρ and μ are resistivity and permeability of copper litz wire. Therefore, skin effect can be significantly reduced. Finally, measured values of the L_p, L_s, and M are 245.8 μH, 245.3 μH, and 41.2 μH, respectively. According to:

$$f_3 = \frac{1}{2\pi\sqrt{L_p C_1}} = \frac{1}{2\pi\sqrt{L_s C_2}}. \tag{5.22}$$

assuming f_3 to be 100 kHz, then C_1 and C_2 are calculated as 10.31 nF and 10.33 nF respectively. Practically, measured values of C_1 and C_2 are 10.30 nF and 10.31 nF.

5) Inductance of input inductors L_{in}:

Ideally, maximum input power ($P_{in.\max}$) is equal to $P_{o.\max}$, and also occurs when $D_{ab} = 1$ and $f_s = f_3$. With known m value (0.486) and V_{sp} ($110\sqrt{2}$ V), L_{in} can be calculated from (5.8) – (5.17), which is 62.75 μH.

6) Maximum operation frequency $f_{s.max}$:

By analysis and calculation, at operation frequency f_s equal to $1.041f_3$, P_{in} and P_o curves have only one intersection point. Hence, $f_{s.\max}$ is confirmed to be $1.041f_3$, which is 104.1 kHz.

7) Input filter design:

To design the input filter, input resistance of the proposed converter need to be confirmed. Because the input filter configuration of each phase is the same, input resistance of one phase (v_x) is calculated. Here only half positive cycle of v_x are considered. When $0 \le v_x \le (1 - D_{ab})V_{bus}/2$, input resistance R_i is:

$$R_i = \frac{8L_{in} f_s \left(V_{bus} - 2v_x\right)}{D_{ab}{}^2 V_{bus}}, \tag{5.23}$$

and when $v_x > (1 - D_{ab})V_{bus}/2$, R_i is:

$$R_i = \frac{32L_{in} f_s v_x \left(V_{bus} - v_x\right)}{2v_x V_{bus}\left(1 + D_{ab}{}^2\right) - V_{bus}{}^2\left(1 - D_{ab}\right)^2}. \tag{5.24}$$

It can be analyzed that minimum input resistance $R_{i.\min}$ occurs when $D_{ab} = 1$ (100% load) and $v_x = 110\sqrt{2}\,V$. And $R_{i.\min}$ is calculated to be 25.8Ω. Note inductance and capacitance of the input filter of each phase as L_{if} and C_{if}, then $\omega_l L_{if} \ll R_{i.\min}$ should be fulfilled. Therefore, L_{if} is designed to be 500 μH first. Because f_s is around 100 kHz, the cutoff frequency is designed to be 10 kHz. Therefore, C_{if} is designed to be 506.6 nF. In practice, L_{if} is measured to be 633.9 μH, 635.9 μH, 631.5 μH (three input filter inductors) and C_{if} is measured to be 1.0 μF.

V.3.2 Design summary and laboratory prototype

Table V-1 gives the detailed design parameters of the laboratory prototype. Input inductor $L_{in.a}$, $L_{in.b}$, and $L_{in.c}$ are designed to be the same, however, they are a little different due to practical manufacture errors and their values are measured to be 62.30 μH, 62.20 μH, and 62.15 μH respectively.

TABLE V-1 Parameters of the laboratory prototype

Components	Details
$L_{in.a}$, $L_{in.b}$, $L_{in.c}$	62.30 μH, 62.20 μH, and 62.15 μH
D_{r1} - D_{r6}	IXYS DSEI 2x31-10B
Q_1, Q_2, Q_3, Q_4	CREE C2M0080120D
C_{b1}, C_{b2}	3300 μH, 450 V (electrolytic capacitors bank)
C_{s1}, C_{s2}	1 nF, 1 kV (polypropylene capacitors)
L_p, L_s, M	245.8 μH; 245.3 μH; 41.2 μH
C_1, C_2	10.30 nF; 10.31 nF (5 kV polypropylene capacitors)
D_{s1}, D_{s2}, D_{s3}, D_{s4}	Vishay VS-30EPH06PbF
C_f	220 μF, 450 V (electrolytic capacitor)
L_{if}, C_{if}	(633.9 μH, 635.9 μH, 631.5 μH), 1.0 μF
f_s	Min: 100 kHz; Max: 104.1 kHz
D_{ab}	0 – 1

TABLE V-2 Operation parameters at different load conditions

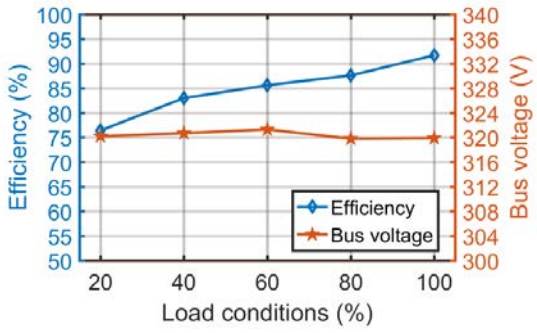
Load conditions	Load resistance R	Duty cycle D_{ab}	Operation frequency f_s
100% load (1.25 kW)	50 Ω	1.0	99.6 kHz
80% load (1.00 kW)	62.4 Ω	0.92	103.5 kHz
60% load (0.75 kW)	83.33 Ω	0.70	103.9 kHz
40% load (0.50 kW)	125 Ω	0.52	103.3 kHz
20% load (0.25 kW)	250 Ω	0.34	102.4 kHz

V.4 Experimental Results

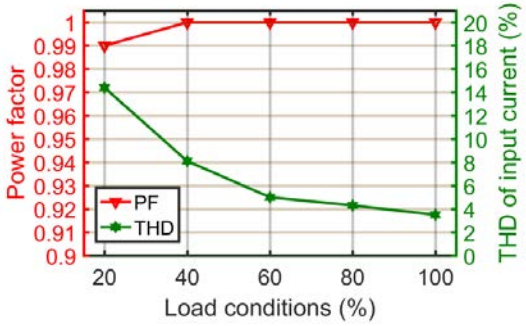
Following the proposed design procedure, a laboratory prototype is implemented with rated output power of 1.25 kW. In the experiments, operations at 20% – 100% load conditions (0.25 – 1.25 kW) are tested to verify the functionalities and advantages of the proposed topology with different operation

parameters shown in Table V-2.

Fig. V-19 shows the performances of the proposed topology at different load conditions. At full load condition, efficiency, power factor, and THD of input current reach the best performances (91.7%, 1.00, and 3.5%, respectively). From Fig. V-19 (a), efficiency drops as load power decreases because load resistance deviates from the optimum load resistance of the WPT resonant tank. And throughout the wide load varying range, bus voltage is maintained to be stable (320 V) as designed previously. Compared to single-phase single-stage WPT topology proposed in Chapter III, the power quality of the proposed topology is much better and bus voltage is maintained at a relative low level within a wide load range. Fig. V-20 and Fig. V-21 show the input current, phase input voltage, and input inductor current at 100% and 20% load conditions respectively. Fig. V-22 and Fig. V-23 show the voltages and currents of resonant tank at 100% and 20% load conditions respectively.

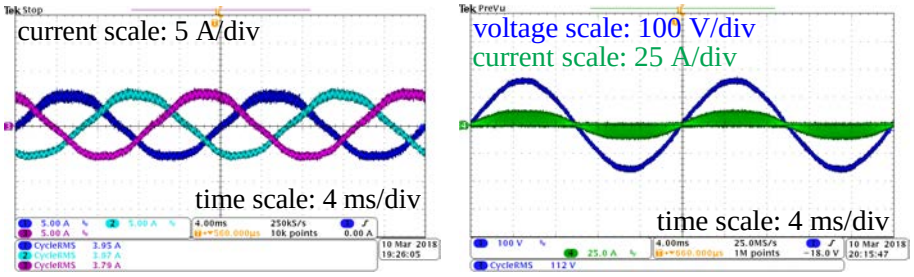


(a)



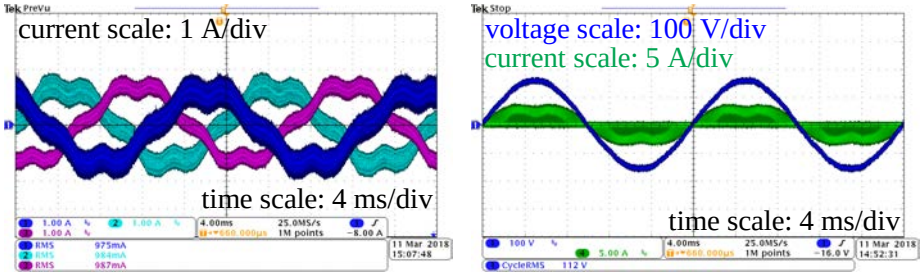
(b)

Fig. V-19. Performances at different load conditions: (a) Efficiency and bus voltage; (b) Power factor and THD of three-phase input current



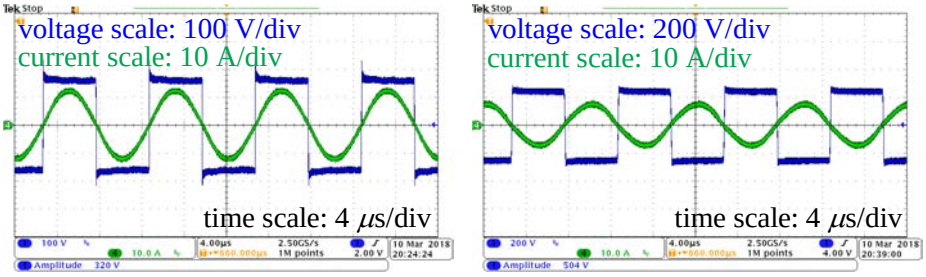
(a) (b)

Fig. V-20. (a) Three-phase input current at 100% load condition; (b) Phase voltage and input inductor current of one phase of 100% load condition



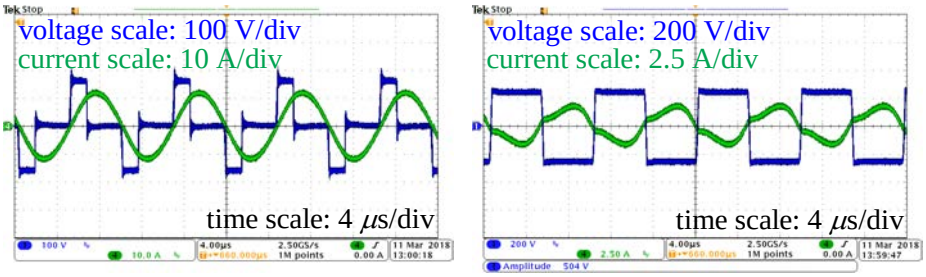
(a) (b)

Fig. V-21. (a) Three-phase input current at 20% load condition; (b) Phase voltage and input inductor current of one phase of 20% load condition



(a) (b)

Fig. V-22. Waveforms of resonant tank at 100% load condition. (a) v_{AB} (in blue) and i_r (in green); (b) v_{CD} (in blue) and i_{rs} (in green)



(a) (b)

Fig. V-23. Waveforms of resonant tank at 20% load condition. (a) v_{AB} (in blue) and i_r (in green); (b) v_{CD} (in blue) and i_{rs} (in green)

V.5 Conclusion

A three-phase single-stage AC-DC WPT resonant converter with PFC is firstly proposed, studied, and developed in this chapter. The proposed topology combines a three-phase rectifier bridge and a T-type three-level inverter together to realize the functionalities of AC-DC power factor correction and DC-DC WPT simultaneously. The proposed three-phase topology exhibits much better performance of PFC than the proposed single-phase topology because it can naturally eliminate zero-sequence harmonics of input current, especially for third-order harmonic. Doubtlessly, three-phase topologies are capable of handling higher power than single-phase topologies, therefore, in high power WPT applications, such as 7.7 kW, 11.1 kW, and 22 kW wireless EV charging system, the proposed three-phase single-stage AC-DC WPT resonant converter holds advantage. As the bus voltage is maintained constant at different load conditions by regulating operation frequency and duty cycle simultaneously, it will not rasie too high when load condition varies.

Chapter VI

A New Parameter Estimation Algorithm requiring only Primary-side Information of DC-DC Wireless-Power-Transfer Resonant Converter under Unknown Varying Misalignment and Load Conditions

VI.1 Introduction

Wireless power transfer (WPT) technology has drawn more and more attention in research fields, industrial circles, and people's daily life. It is now commonly applied in wireless electric vehicle (EV) charging, artificial organs powering, portable devices (mobile phones, tablet PCs, and laptops) charging, powering moving EVs, and so on [1], [2], [4], [8], [9], [142], [143]. There are basically four topologies of WPT resonant tank: series-series (SS), series-parallel (SP), parallel-parallel (PP), and parallel-series (PS) [8]. For the whole WPT system, some use class-E amplifier as the source [144]; some use multi-stage converter [145] – [148]; and some use one-stage DC-DC resonant converter [19], [149], [150]. In addition to various topologies, control methods and algorithms are also diversified, including maximum efficiency tracking [42], [126], [148], [149], load modulation [151], converter parameters estimating [146], [148], [152], and so on.

For WPT systems, such as wireless EV chargers, coils misalignment and load conditions are usually unknown because they are neither constant nor static. For example, for wireless EV charging, the secondary-side coil on the EV may misalign with the primary-side coil of the wireless EV charger when the EV is casually parked, and the misalignment is likely different every time even for the

same EV model. Moreover, the load conditions would vary as the charging progress with varying state-of-charge of the EV battery. Therefore, mutual inductance and load conditions are unknown parameters for a WPT system. However, they are essential to regulate output voltage and power or track maximum efficiency, and are often estimated using feedback information from secondary (load) side [148], [149], [153]. Though load modulation methods [151], which utilize WPT resonant tank to transmit signals from secondary-side back to primary-side, can be used to eliminate any additional wireless communication device, secondary-side controller and measurement units are always required in this approach.

Many algorithms have recently been proposed to estimate the mutual inductance and load conditions only from primary- side information for regulation of output voltage and power as well as system efficient [146], [147], [152], [154]. Such parameter estimation techniques are of great significance as the physical system can be largely simplified without the need for any additional wireless communication device and secondary-side measurement units and controller. Also, the estimated mutual inductance and load conditions can be used for control to ensure the WPT system with high efficiency and desired output power and voltage. However, those existing approaches do have various limitations. The method proposed in [154] applied a simplified circuit model with the assumptions of linear load and no coil parasitic resistances, and therefore is not so accurate. The technique proposed in [147] requires topology with linear resistive load and without secondary-side rectifiers; whereas, the method proposed in [146] requires complicated and multiple-iteration calculations, which slows down the system response. In addition, methods in [146] and [147] are only applicable for two-stage regulation with 50% duty-ratio two-level square wave voltage source for the WPT resonant tank. The approach in [152] is restrictedly applicable for linear AC-AC topology without any non-linear semi-conductor devices, and requires the operation frequency not operated at the middle resonant frequency; therefore, its

application is limited.

Fundamental harmonic approximation (FHA) method [120] is commonly applied to analyze resonant converters with non-linear semi-conductor devices, such as DC-DC WPT resonant converter [149], [150], [155], and other types of resonant converters [156] – [158], but often such method is not accurate enough as the high-order harmonics existing in the converters are neglected. In this chapter, an accurate analysis method would first be introduced and applied to analyze a DC-DC WPT resonant converter with SS topology, and then, a new parameter estimation algorithm is proposed and developed based on this accurate steady-state analysis method, which requires only the primary-side voltage and current waveforms to calculate the mutual inductance, output voltage, output power and efficiency under unknown varying coupling and load conditions. The proposed algorithm is suitable for not only one-stage DC-DC WPT resonant converters with multi-level voltage source for the WPT resonant tank and no restriction on the operation frequency, but also soft-switching operation with non-pure square-wave or three-level voltage waveform into the resonant tank, which is not previously considered in [146], [147], [154].

In this chapter, the accurate steady-state analysis method of DC-DC WPT resonant converter is firstly given in Section V.2 while the parameter estimation algorithm is presented in details in Section V.3. Hardware design and laboratory prototype for the evaluation of the proposed parameter estimation algorithm are introduced in Section V.4 with experimental results presented and discussed in Section V.5 for validating the correctness and accuracy of the proposed algorithm.

VI.2 Accurate Analysis of DC-DC WPT Resonant Converter

VI.2.1 Basic Definitions

Fig. VI-1 shows a typical DC-DC WPT resonant converter, which consists of a full-bridge inverter ($Q_1 - Q_4$), a WPT resonant tank, a full-bridge diode rectifier

($D_{s1} - D_{s4}$), an output filter C_f, and a load resistor R. V_{in} is DC input voltage and V_o is output DC voltage. The WPT resonant tank includes primary-side resonant inductor and capacitor L_p and C_1, and secondary-side resonant inductor and capacitor L_s and C_2 while M is the mutual inductance of L_p and L_s. v_{AB} and i_r are the primary–side voltage and current of the resonant tank while v_{CD} and i_{rs} are those of the secondary side. By modulating the duty cycles and the switching sequences of $Q_1 - Q_4$, v_{AB} can be configured as a three-level voltage with duty cycle D_{ab}, which is defined as the ratio of v_{AB}'s non-zero duration and switching period T_s. As i_{rs} would work at continuous current mode (CCM) at most load conditions except for very low load power condition, v_{CD} should be a two-level square wave voltage with 50% duty cycle, as shown in Fig. VI-1, and the switching frequency is defined as f_s or ω_s (in radian).

Steady-state analysis of a DC-DC WPT resonant converter usually refers to determining the DC transfer gains under different duty cycles and operation frequencies. The known parameters include L_p, L_s, C_1, C_2, M, R, D_{ab}, and f_s. If parasitic resistances of primary and secondary sides (R_p and R_s) and forward voltage drop (V_d) of secondary-side diodes are known, then efficiency can be calculated and analyzed.

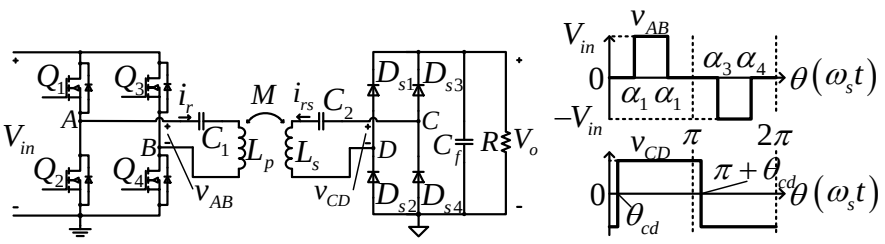


Fig. VI-1. DC-DC WPT resonant converter and waveforms of v_{AB} and v_{CD} for theoretical analysis

VI.2.2 Proposed Accurate Analysis and Calculation Method

Because of the existence of the switching devices $Q_1 - Q_4$ and $D_{s1} - D_{s4}$, v_{AB}

and v_{CD} cannot be regulated as pure sinusoid wave and there are higher-order harmonics existed in v_{AB} and v_{CD}. From Fig. VI-1, v_{AB} and v_{CD} consist of 1st, 3rd, 5th, and more higher-order components. Although the resonant tank can be regarded as a band-pass filter, it cannot eliminate all the higher-order harmonics, especially those close to the 1st frequency, i.e. 3rd and 5th harmonics. Therefore, except for the fundamental component, there still are higher-order harmonics existed in the converter, especially for the conditions of v_{AB} with small D_{ab}. Hence, FHA often cannot be used to accurately analyze the DC characteristics of the converter.

A more accurate method considering both fundamental component and higher-order harmonics to analyze the DC/DC WPT resonant converter was introduced in [140] without considering the ESRs of the converter. Here in this chapter, a more detailed analysis procedure with considering both parasitic resistances and forward voltage drop of rectifier diode is presented.

In Fig. VI-1, θ is equal to $\omega_s t$, θ_{cd} is the phase angle of v_{CD}, and α_1, α_2, α_3, and α_4 are defined as:

$$\alpha_{1,2} = \left(1 \mp D_{ab}\right)\pi/2, \quad \alpha_{3,4} = \left(3 \mp D_{ab}\right)\pi/2. \tag{6.1}$$

Hence, v_{AB} and v_{CD} can be expressed as Fourier series:

$$v_{AB} = \sum_{n=1}^{+\infty} v_{AB.n}, \quad v_{CD} = \sum_{n=1}^{+\infty} v_{CD.n}, \tag{6.2}$$

where n is the harmonic's order (n=1,3,5,7, …) and:

$$v_{AB.n} = V_{AB.ns}\sin\left(n\omega_s t\right) + V_{AB.nc}\cos\left(n\omega_s t\right), \tag{6.3}$$

$$v_{CD.n} = V_{CD.ns}\sin\left(n\omega_s t\right) + V_{CD.nc}\cos\left(n\omega_s t\right), \tag{6.4}$$

and $V_{AB.ns}$, $V_{AB.nc}$, $V_{CD.ns}$, and $V_{CD.nc}$ are calculated:

$$V_{AB.ns} = \left(-1\right)^{(n-1)/2} \cdot 4V_{in}\sin\left(nD_{ab}\pi/2\right)/\left(n\pi\right), \tag{6.5}$$

$$V_{AB.nc} = 0, \tag{6.6}$$

$$V_{CD.ns} = 4\left(V_o + 2V_d\right)\cos\left(n\theta_{cd}\right)/\left(n\pi\right), \tag{6.7}$$

$$V_{CD.nc} = -4\left(V_o + 2V_d\right)\sin\left(n\theta_{cd}\right)/\left(n\pi\right), \tag{6.8}$$

where V_d is forward voltage drop of secondary-side rectifier diode. i_r and i_{rs} are currents through L_p and L_s, v_{c1} and v_{c2} are voltages across C_1 and C_2, also shown in Fourier Series:

$$i_r = \sum_{n=1}^{+\infty} i_{r.n},\ \ i_{rs} = \sum_{n=1}^{+\infty} i_{rs.n},\ \ v_{c1} = \sum_{n=1}^{+\infty} v_{c1.n},\ \ v_{c2} = \sum_{n=1}^{+\infty} v_{c2.n}, \tag{6.9}$$

where

$$i_{r.n} = I_{r.ns}\sin\left(n\omega_s t\right) + I_{r.nc}\cos\left(n\omega_s t\right), \tag{6.10}$$

$$i_{rs.n} = I_{rs.ns}\sin\left(n\omega_s t\right) + I_{rs.nc}\cos\left(n\omega_s t\right), \tag{6.11}$$

$$v_{c1.n} = V_{c1.ns}\sin\left(n\omega_s t\right) + V_{c1.nc}\cos\left(n\omega_s t\right), \tag{6.12}$$

$$v_{c2.n} = V_{c2.ns}\sin\left(n\omega_s t\right) + V_{c2.nc}\cos\left(n\omega_s t\right). \tag{6.13}$$

Applying KVL, (6.14) – (6.17) are obtained:

$$v_{AB} = R_p i_r + L_p\left(di_r/dt\right) + v_{c1} + M\left(di_{rs}/dt\right), \tag{6.14}$$

$$i_r = C_1\left(dv_{c1}/dt\right), \tag{6.15}$$

$$v_{CD} = R_s i_{rs} + L_s\left(di_{rs}/dt\right) + v_{c2} + M\left(di_r/dt\right), \tag{6.16}$$

$$i_{rs} = C_2\left(dv_{c2}/dt\right). \tag{6.17}$$

From (6.9) – (6.17), we have:

$$V_n = Z_{An} \times I_n, \tag{6.18}$$

where V_n, Z_{An}, and I_n are defined as:

$$V_n = \begin{bmatrix} V_{AB.ns} \\ V_{AB.nc} \\ V_{CD.ns} \\ V_{CD.nc} \end{bmatrix}, I_n = \begin{bmatrix} I_{r.ns} \\ I_{r.nc} \\ I_{rs.ns} \\ I_{rs.nc} \end{bmatrix}, \tag{6.19}$$

$$Z_{An} = \begin{bmatrix} R_p & -Z_{pn} & 0 & -Z_{mn} \\ Z_{pn} & R_p & Z_{mn} & 0 \\ 0 & -Z_{mn} & R_s & -Z_{sn} \\ Z_{mn} & 0 & Z_{sn} & R_s \end{bmatrix}, \tag{6.20}$$

where R_p and R_s are equivalent series resistances (ESRs) of primary and secondary sides respectively, and Z_{pn}, Z_{mn}, and Z_{sn} (n=1, 3, 5, …) are defined as real values:

$$Z_{pn} = n\omega_s L_p - \frac{1}{n\omega_s C_1}, \quad Z_{mn} = n\omega_s M, \quad Z_{sn} = n\omega_s L_s - \frac{1}{n\omega_s C_2}. \tag{6.21}$$

By analysis, P_o can be expressed as:

$$\begin{aligned} P_o &= \frac{1}{\pi} \int_{\theta_{cd}}^{\pi+\theta_{cd}} V_o \left(-i_{rs}\right) d\theta \\ &= \frac{2V_o}{\pi} \sum_{n=1}^{+\infty} \left[\frac{I_{rs.nc} \sin\left(n\theta_{cd}\right) - I_{rs.ns} \cos\left(n\theta_{cd}\right)}{n} \right] = \frac{V_o^{\,2}}{R}. \end{aligned} \tag{6.22}$$

From the characteristic of the secondary-side rectifier-bridge, at $\omega_s t=\theta_{cd}$, i_{rs} is equal to zero, therefore,

$$\begin{aligned} i_{rs}\left(\theta_{cd}\right) &= \sum_{n=1}^{+\infty} i_{rs.n}\left(\theta_{cd}\right) \\ &= \sum_{n=1}^{+\infty} \left[I_{rs.ns} \sin\left(n\theta_{cd}\right) + I_{rs.nc} \cos\left(n\theta_{cd}\right) \right] = 0. \end{aligned} \tag{6.23}$$

To calculate V_o and θ_{cd}, inverse matrix of Z_{An} can be calculated and noted as (n=1, 3, 5, …):

$$Z_{Bn} = Z_{An}^{-1} = \begin{bmatrix} b_{n.11} & b_{n.12} & b_{n.13} & b_{n.14} \\ b_{n.21} & b_{n.22} & b_{n.23} & b_{n.24} \\ b_{n.31} & b_{n.32} & b_{n.33} & b_{n.34} \\ b_{n.41} & b_{n.42} & b_{n.43} & b_{n.44} \end{bmatrix}. \tag{6.24}$$

Therefore, $I_{rs.ns}$ and $I_{rs.nc}$ are obtained:

$$I_{rs.ns} = b_{n.31}V_{AB.ns} + b_{n.32}V_{AB.nc} + b_{n.33}V_{CD.ns} + b_{n.34}V_{CD.nc}, \tag{6.25}$$

$$I_{rs.nc} = b_{n.41}V_{AB.ns} + b_{n.42}V_{AB.nc} + b_{n.43}V_{CD.ns} + b_{n.44}V_{CD.nc}, \tag{6.26}$$

Practically, the accuracy and calculation complexity can be balanced with consideration of 1st, 3rd, and 5th order harmonics (n=1, 3, and 5) only to calculate V_o and θ_{cd} using the nonlinear equation set (6.22) and (6.23), by substituting (6.25) and (6.26) into them. The nonlinear equation set is solved using Newton iteration method in Matlab and the initial values of Newton iteration calculation are obtained through FHA method.

Assuming that there is no switching loss of $Q_1 - Q_4$, only on-resistance R_{on} of $Q_1 - Q_4$, ESRs (R_{lp}, R_{c1}, R_{ls}, R_{c2}) of resonant inductors and capacitors, and forward voltage drop V_d of rectifier diode are considered to analyze the efficiency of the converter. Then (6.27) is obtained:

$$R_p = 2R_{on} + R_{lp} + R_{c1}, \quad R_s = R_{ls} + R_{c2}. \tag{6.27}$$

And input power P_{in} is expressed as:

$$P_{in} = \frac{1}{\pi}\int_{\alpha_1}^{\alpha_2} V_{in} i_r \, d\theta = \frac{2V_{in}}{\pi}\sum_{n=1}^{+\infty} \frac{I_{r.ns}\sin\left(nD_{ab}\pi/2\right)}{\left(-1\right)^{(n-1)/2} n}. \tag{6.28}$$

where $I_{r.ns}$ can be calculated by:

$$I_{r.ns} = b_{n.11}V_{AB.ns} + b_{n.12}V_{AB.nc} + b_{n.13}V_{CD.ns} + b_{n.14}V_{CD.nc}. \tag{6.29}$$

Hence, efficiency of the converter is:

$$\eta = P_o / P_{in}. \tag{6.30}$$

VI.2.3 Comparisons between the Proposed Analysis Method and FHA Method

Table VI-1 shows the comparisons of output voltage V_o and efficiency η under different operation frequency conditions, with duty cycle D_{ab} set to 1 while Table VI-2 shows the results under various duty cycle conditions with operation frequency f_s set to the middle resonant frequency 94.26 kHz. The other parameters are: L_p = 241 μH; C_1 = 11.83 nF; R_p = 0.2 Ω; L_s = 241 μH; C_2 = 11.83 nF; R_s = 0.2 Ω; M = 46 μH; R = 50 Ω; V_d = 0.5 V; V_{in} = 100 V. It can be shown from the two tables that calculated V_o using proposed analysis method are more accurate than that using FHA method. Also calculated V_o and η using proposed analysis method are very close to the simulation results, which validates the high accuracy of the proposed analysis method. In Table VI-1, 86.37 kHz, 94.26 kHz, and 104.79 kHz are three resonant frequencies.

TABLE VI-1 Comparisons of output voltage and efficiency under different operation frequency conditions (duty cycle D_{ab}=1)

Frequency (kHz)	70	86.37	94.26	104.79	150
Calculated V_o using proposed method (V)	10.04	98.03	147.2	98.01	9.45
Calculated V_o using FHA method (V)	10.46	100.0	148.8	100.0	9.82
V_o by simulation (V)	10.22	98.10	147.0	97.92	9.41
Calculated η using proposed method	0.817	0.969	0.978	0.971	0.856
η by simulation	0.821	0.969	0.978	0.971	0.855

TABLE VI-2 Comparisons of output voltage and efficiency under different duty cycle conditions (operation frequency f_s=94.26 kHz)

Duty cycle D_{ab}	0.2	0.4	0.6	0.8	1
Calculated V_o using proposed method (V)	45.14	86.12	118.9	139.9	147.2
Calculated V_o using FHA method (V)	45.97	87.44	120.4	141.5	148.8
V_o by simulation (V)	45.08	86.06	118.7	139.8	147.0
Calculated η using proposed method	0.963	0.973	0.976	0.977	0.978
η by simulation	0.962	0.973	0.976	0.977	0.978

VI.3 Proposed Parameters Estimation Algorithm

A novel algorithm for parameter estimation of a DC-DC WPT resonant converter is proposed and developed here based on the above accurate steady-state analysis method. The proposed algorithm does not require any signal acquisition from the secondary side of the converter and is able to estimate the mutual inductance, output voltage, output power and efficiency online, without knowing the exact misalignment and load resistance conditions. The proposed algorithm only requires the inherent parameters (L_p, L_s, C_1, C_2, f_s, R_p, R_s, and V_d) in advance and then samples primary-side voltage and current waveforms in real time.

VI.3.1 Calculations of M and V_o

A. Neglecting parasitic resistances R_p and R_s

For high transmission efficiency, litz wire with large number of strands will usually be used in the WPT resonant tank to make the ESRs of the resonant coils

very small. Polypropylene capacitors are commonly adopted as the resonant capacitors in WPT resonant tank as their ESRs are also very small. If mosfets with very small on-resistances are used in the converter too, R_p and R_s can also be neglected. Therefore, in these conditions, from (6.19) and (6.20), we have:

$$I_{r.ns} = \left(Z_{sn}V_{AB.nc} - Z_{mn}V_{CD.nc}\right) \Big/ \left(Z_{pn}Z_{sn} - {Z_{mn}}^2\right), \tag{6.31}$$

$$I_{r.nc} = \left(-Z_{sn}V_{AB.ns} + Z_{mn}V_{CD.ns}\right) \Big/ \left(Z_{pn}Z_{sn} - {Z_{mn}}^2\right). \tag{6.32}$$

Make n=1 and 3, then (6.33) – (6.36) are obtained:

$$I_{r.1s}{Z_{m1}}^2 + Z_{m1}\frac{4\left(V_o + 2V_d\right)}{\pi}\sin\theta_{cd} = I_{r.1s}Z_{p1}Z_{s1} - Z_{s1}V_{AB.1c}, \tag{6.33}$$

$$I_{r.1c}{Z_{m1}}^2 + Z_{m1}\frac{4\left(V_o + 2V_d\right)}{\pi}\cos\theta_{cd} = I_{r.1c}Z_{p1}Z_{s1} + Z_{s1}V_{AB.1s}, \tag{6.34}$$

$$I_{r.3s}{Z_{m3}}^2 + Z_{m3}\frac{4\left(V_o + 2V_d\right)}{3\pi}\sin\left(3\theta_{cd}\right) = I_{r.3s}Z_{p3}Z_{s3} - Z_{s3}V_{AB.3c}, \tag{6.35}$$

$$I_{r.3c}{Z_{m3}}^2 + Z_{m3}\frac{4\left(V_o + 2V_d\right)}{3\pi}\cos\left(3\theta_{cd}\right) = I_{r.3c}Z_{p3}Z_{s3} + Z_{s3}V_{AB.3s}. \tag{6.36}$$

Then, (6.37) and (6.38) are obtained:

$$\begin{aligned}
&\left[16\left(V_o + 2V_d\right)^2 {Z_{m1}}^2\right] \Big/ \left(\pi^2\right) \\
&= \left[\left(Z_{p1}Z_{s1} - {Z_{m1}}^2\right)I_{r.1s} - Z_{s1}V_{AB.1c}\right]^2 \\
&+ \left[\left(Z_{p1}Z_{s1} - {Z_{m1}}^2\right)I_{r.1c} + Z_{s1}V_{AB.1s}\right]^2,
\end{aligned} \tag{6.37}$$

$$\begin{aligned}
&\left[16\left(V_o + 2V_d\right)^2 {Z_{m3}}^2\right] \Big/ \left(9\pi^2\right) \\
&= \left[\left(Z_{p3}Z_{s3} - {Z_{m3}}^2\right)I_{r.3s} - Z_{s3}V_{AB.3c}\right]^2 \\
&+ \left[\left(Z_{p3}Z_{s3} - {Z_{m3}}^2\right)I_{r.3c} + Z_{s3}V_{AB.3s}\right]^2.
\end{aligned} \tag{6.38}$$

Let A_{g1}, B_{g1}, A_{g3}, and B_{g3} be as follows:

$$A_{g1} = I_{r.1s} Z_{p1} Z_{s1} - V_{AB.1c} Z_{s1}, \tag{6.39}$$

$$B_{g1} = I_{r.1c} Z_{p1} Z_{s1} + V_{AB.1s} Z_{s1}, \tag{6.40}$$

$$A_{g3} = I_{r.3s} Z_{p3} Z_{s3} - V_{AB.3c} Z_{s3}, \tag{6.41}$$

$$B_{g3} = I_{r.3c} Z_{p3} Z_{s3} + V_{AB.3s} Z_{s3}. \tag{6.42}$$

Then (6.43) is obtained:

$$A_M {Z_{m1}}^4 + B_M {Z_{m1}}^2 + C_M = 0. \tag{6.43}$$

And ${Z_{m1}}^2$ is calculated as:

$${Z_{m1}}^2 = \frac{-B_M \pm \sqrt{{B_M}^2 - 4A_M C_M}}{2A_M} > 0, \tag{6.44}$$

where A_M, B_M, and C_M are denoted as:

$$A_M = {I_{r.1s}}^2 + {I_{r.1c}}^2 - 81\left({I_{r.3s}}^2 + {I_{r.3c}}^2\right), \tag{6.45}$$

$$B_M = -2A_{g1} I_{r.1s} - 2B_{g1} I_{r.1c} + 18A_{g3} I_{r.3s} + 18B_{g3} I_{r.3c}, \tag{6.46}$$

$$C_M = {A_{g1}}^2 + {B_{g1}}^2 - {A_{g3}}^2 - {B_{g3}}^2. \tag{6.47}$$

Hence, the mutual inductance M can be calculated from (6.44) and then the output voltage V_o can be calculated from (6.37) using the primary-side signals $V_{AB.1s}$, $V_{AB.1c}$, $V_{AB.3s}$, $V_{AB.3c}$, $I_{r.1s}$, $I_{r.1c}$, $I_{r.3s}$, $I_{r.3c}$, and the inherent parameters (L_p, C_1, L_s, C_2, V_d, ω_s) of the converter measured and confirmed in advance. In practical applications, misalignment of coils is designed and limited within a range, and therefore M value is within a reasonable range. When real solutions of ${Z_{m1}}^2$ are obtained, M values are also obtained and the one within the reasonable range would be the final solution.

B. Considering parasitic resistances R_p and R_s

For more accurate estimations of M and V_o, R_p and R_s need to be considered too. Newton iteration method is applied with the initial values of M and V_o obtained without considering R_p and R_s (V.3.1.A), and the initial value of θ_{cd} obtained from (6.33) and (6.34). In other words, M, V_o and θ_{cd} are the three unknown variables to be determined. Therefore, a function set containing three non-linear functions is derived from (6.18) – (6.20), and (6.24):

$$\begin{aligned} f_1(x) &= I_{r.1s} - b_{1.11}(x_1)V_{AB.1s} - b_{1.12}(x_1)V_{AB.1c} \\ &-b_{1.13}(x_1)V_{CD.1s}(x_2,x_3) - b_{1.14}(x_1)V_{CD.1c}(x_2,x_3), \end{aligned} \tag{6.48}$$

$$\begin{aligned} f_2(x) &= I_{r.1c} - b_{1.21}(x_1)V_{AB.1s} - b_{1.22}(x_1)V_{AB.1c} \\ &-b_{1.23}(x_1)V_{CD.1s}(x_2,x_3) - b_{1.24}(x_1)V_{CD.1c}(x_2,x_3), \end{aligned} \tag{6.49}$$

$$\begin{aligned} f_3(x) &= I_{r.3s} - b_{3.11}(x_1)V_{AB.3s} - b_{3.12}(x_1)V_{AB.3c} \\ &-b_{3.13}(x_1)V_{CD.3s}(x_2,x_3) - b_{3.14}(x_1)V_{CD.3c}(x_2,x_3). \end{aligned} \tag{6.50}$$

And we have the following definitions:

$$F(x) = \begin{bmatrix} f_1(x) \\ f_2(x) \\ f_3(x) \end{bmatrix}, x = \begin{bmatrix} x_1 \\ x_2 \\ x_3 \end{bmatrix} = \begin{bmatrix} M \\ V_o \\ \theta_{CD} \end{bmatrix}. \tag{6.51}$$

The Jacobi matrix of $F(x)$ is obtained as:

$$F'(x) = \begin{bmatrix} \partial f_1/\partial x_1 & \partial f_1/\partial x_2 & \partial f_1/\partial x_3 \\ \partial f_2/\partial x_1 & \partial f_2/\partial x_2 & \partial f_2/\partial x_3 \\ \partial f_3/\partial x_1 & \partial f_3/\partial x_2 & \partial f_3/\partial x_3 \end{bmatrix}. \tag{6.52}$$

Therefore, accurate solutions can be obtained by iteration calculations of (6.53):

$$x^{(p+1)} = x^{(p)} - F'\left(x^{(p)}\right)^{-1} F\left(x^{(p)}\right), p = 0,1,2,\cdots. \tag{6.53}$$

After a few iterations, if the iterative errors are within the set error limits, values of M, V_o and θ_{cd} are confirmed. Here, M and V_o iterative error limits are noted as E_M and E_{Vo}, respectively.

VI.3.2 Power and efficiency calculations (P_{in}, P_o, and η)

From (6.20) and (6.24), matrix Z_{Bn} can be obtained. Afterwards, $I_{rs.ns}$ and $I_{rs.nc}$ can be calculated from (6.25) and (6.26). Make n = 1, 3, and 5, then output power P_o can be obtained from (6.22). However, to calculate input power P_{in}, (6.28) cannot be used because v_{AB} may not be in phase with the waveform of Fig. VI-1 when it was sampled.

Assuming that v_{AB}'s phase angle is θ_{ab}, $V_{AB.ns}$ and $V_{AB.nc}$ are revised as:

$$V_{AB.ns} = \frac{4V_{in}\sin\left(\frac{n\pi D_{ab}}{2}\right)\cos\left(n\theta_{ab}\right)}{n\pi}, \tag{6.54}$$

$$V_{AB.nc} = \frac{-4V_{in}\sin\left(\frac{n\pi D_{ab}}{2}\right)\sin\left(n\theta_{ab}\right)}{n\pi}. \tag{6.55}$$

And P_{in} can be calculated by:

$$P_{in} = \frac{1}{\pi}\int_{\theta_{ab}+\alpha_1}^{\theta_{ab}+\alpha_2} V_{in} i_r \, d\theta = \sum_{n=1}^{+\infty} \frac{I_{r.ns}V_{AB.ns} + I_{r.nc}V_{AB.nc}}{2\cdot(-1)^{\frac{n-1}{2}}}. \tag{6.56}$$

Hence, efficiency is obtained from (6.30).

VI.3.3 Discrete Fourier series (DFS)

For one switching period, N points of v_{AB} and i_r are sampled, and therefore, we will have $v_{AB}(0)$, $v_{AB}(1)$, ……, $v_{AB}(N\text{-}1)$, and $i_r(0)$, $i_r(1)$, ……, $i_r(N\text{-}1)$. Discrete Fourier series (DFS) calculations are applied to calculate $V_{AB.ns}$, $V_{AB.nc}$, $I_{r.ns}$, and $I_{r.nc}$ as (6.57) – (6.60), where n = 1, 3 and 5:

$$V_{AB.ns} = \frac{2}{N}\sum_{j=0}^{N-1}\left[v_{AB}\left(j\right)\sin\left(\frac{2\pi nj}{N}\right)\right], \tag{6.57}$$

$$V_{AB.nc} = \frac{2}{N}\sum_{j=0}^{N-1}\left[v_{AB}\left(j\right)\cos\left(\frac{2\pi nj}{N}\right)\right], \tag{6.58}$$

$$I_{r.ns} = \frac{2}{N}\sum_{j=0}^{N-1}\left[i_r(j)\sin\left(\frac{2\pi nj}{N}\right)\right], \tag{6.59}$$

$$I_{r.nc} = \frac{2}{N}\sum_{j=0}^{N-1}\left[i_r(j)\cos\left(\frac{2\pi nj}{N}\right)\right]. \tag{6.60}$$

VI.3.4 Summary of proposed algorithm

Fig. VI-2 shows the flowchart of the proposed primary-side calculation algorithm. If parasitic resistances R_p and R_s of the converter are small enough to be neglected, Newton iteration will not be required and Path 2 of the flowchart can be followed. However, if R_p and R_s cannot be neglected, the more time consumed Path 1 with Newton iteration will be selected instead, and the system response will be relatively slower compared to Path 2.

VI.4 Design, Implementation and Laboratory Prototype

A laboratory prototype of the DC-DC WPT resonant converter is designed and implemented in order to validate the proposed parameters estimation algorithm. Fig. VI-3 shows the schematic of hardware setup in which the proposed algorithm is embedded in the DSP controller without knowing the values of load resistance and mutual inductance. The DSP samples the primary-side waveforms, calculates the parameters and then displays them in a LCD screen in real time. When load resistance or mutual inductance (coils misalignment) is changed manually, the estimated parameters shown on the LCD screen are recorded while the corresponding parameters are also measured manually using laboratory instruments. The estimated and measured values are recorded and compared to validate the correctness and accuracy of the proposed algorithm.

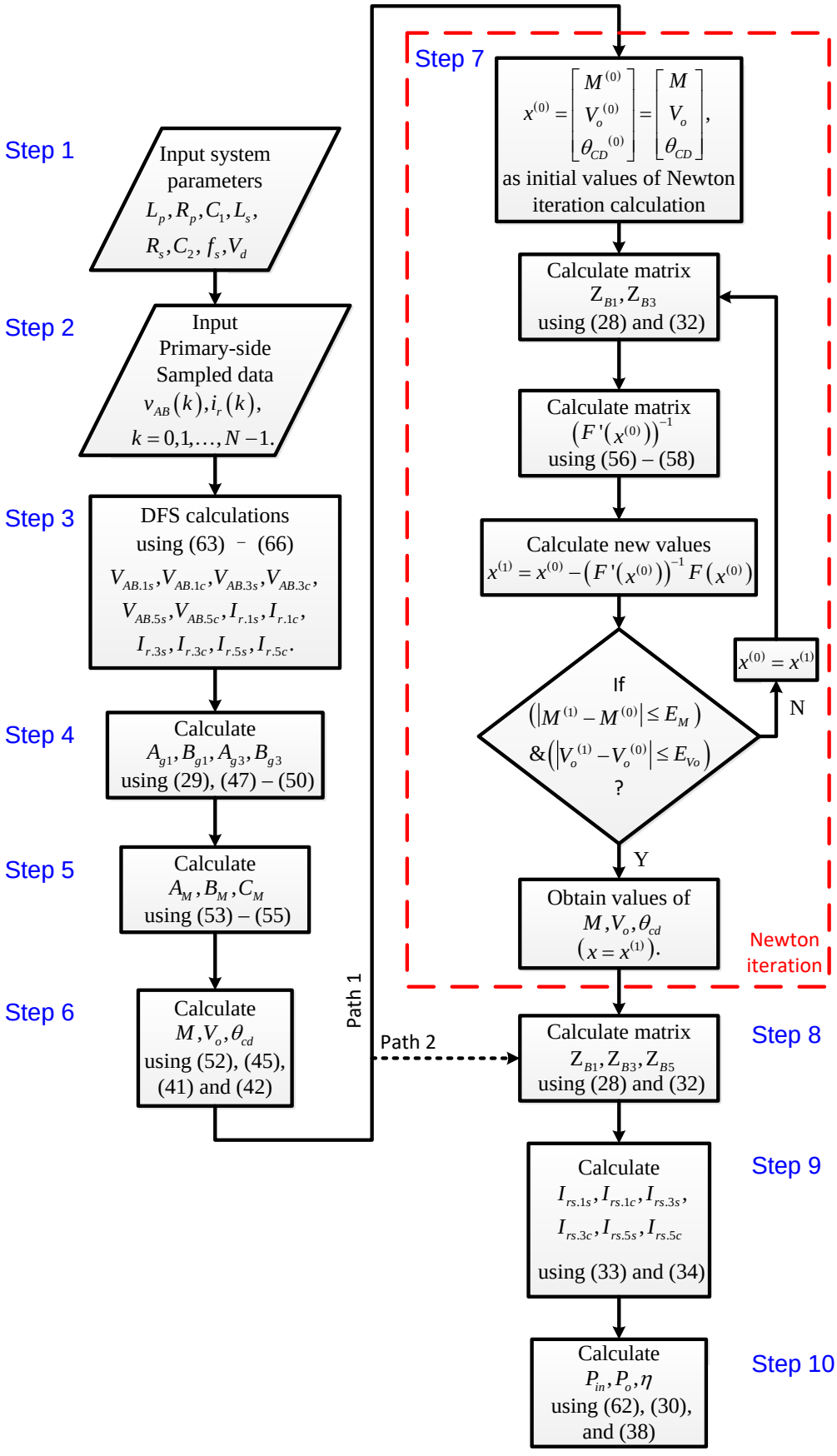


Fig. VI-2. Flowchart of proposed parameter estimation algorithm

VI.4.1 Hardware Design

Firstly, the operation frequency f_s should be set according to the sample rate of the analogue-to-digital (AD) module, that is, sample and hold module. In this laboratory prototype, DSP28335 with on-chip AD module is used for both the calculation and PWM generation. Its highest sample rate is 12.5 MSPS (80 ns per sampling). As both v_{AB} and i_r need to be sampled, the total sampling time is 160 ns. Hence, the operation period T_s should be integer multiples of 160 ns. Meanwhile, f_s should be designed to be around 85 kHz (81.39 – 90 kHz) to comply with the industrial wireless charging standard (SAE J2954). Therefore, two operation frequencies are selected here to be 84.46 kHz (f_{s1}) and 89.29 kHz (f_{s2}) for validating the proposed estimation algorithm being suitable for various operation frequencies.

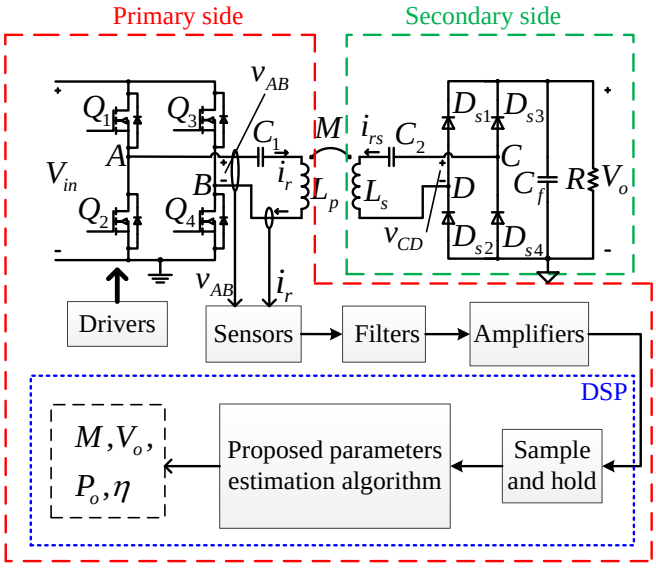


Fig. VI-3. Schematic of hardware setup for the proposed parameters estimation algorithm implementation

In practical implementation, the two resonant coils are designed in spiral shape (coils number: 16; diameter: 50 cm) using litz wire with strands number 100, strand's diameter 0.2 mm, effective cross area of the wire 3.14 mm^2 and diameter of the wire 3.0 mm. The measured parameters (inductances and ESRs) of the two

coils are: L_p = 245.8 μH, L_s = 245.3 μH, R_{lp} = 0.40 Ω, R_{ls} = 0.38 Ω. If f_{s1} is designed as the middle resonant frequency, the resonant capacitors C_1 and C_2 are calculated to be 14.45 nF and 14.48 nF, respectively. To realize soft switching, middle resonant frequency of primary side is designed to be a little lower than f_{s1} and therefore C_1 is revised to be 15.45 nF. Practically, C_1 and C_2 are measured to be 15.36 nF and 14.46 nF, respectively. Their ESRs R_{c1} and R_{c2} are very small and therefore can be neglected.

In this laboratory converter, the primary-side full-bridge inverter consists of two half-bridge modules (CREE CAS120M12BM2) with on-resistance R_{on} 0.013 Ω, and the secondary-side full-bridge rectifier is built using four discrete diodes (Vishay VS-30EPH06PbF) with voltage drop V_d 1.34 V. R_p and R_s are therefore 0.426 Ω and 0.38 Ω, respectively according to (6.27).

Vertical distance d_{ag} of the two coils is designed to be 20 cm and their mutual inductance is measured to be 45.3 μH when they are coaxially aligned. Horizontal misalignment distance d_m of the two coils is allowable from 0 to 21 cm with M measured to vary in the range of 45.3 – 22.7 μH. Fig. VI-4 shows the structure of primary-side and secondary-side coils.

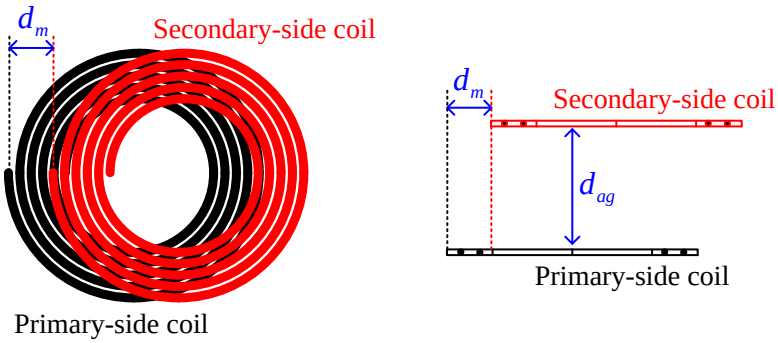


Fig. VI-4. Structure of primary-side and secondary-side coils: (a) top view; (b) side view

VI.4.2 Delay and Attenuation of Primary-Side Signals

From previous analysis, primary-side signals v_{AB} and i_r are assumed to be sampled simultaneously. However, in practices, DSP28335 cannot sample two signals simultaneously, and they are alternately sampled instead. This means that one of the two signals would have one sampling time delay (80 ns) compared to the other. Meanwhile, signals are inevitably delayed and attenuated as they go through sensors, filters and amplifiers modules from main power converter to DSP controller, as shown in Fig. 3. Furthermore, different frequency components of the signals are delayed and attenuated differently. Therefore, delay times and attenuation factors of the two signal paths of different frequency components need to be measured in order to correct the signal amplitudes and phases accordingly. Let the signals sampled by DSP be $v_m(0)$, $v_m(1)$, ……, $v_m(N-1)$, and $i_m(0)$, $i_m(1)$, ……, $i_m(N-1)$, and the Fourier series coefficients of them be $V_{m.ns}$, $V_{m.nc}$, $I_{m.ns}$, and $I_{m.nc}$, where n = 1, 3, and 5. The real signals $V_{AB.ns}$, $V_{AB.nc}$, $I_{r.ns}$, and $I_{r.nc}$ are corrected as follows:

$$V_{AB.ns} = \frac{V_{m.ns}}{k_{Vm.n}} \cos\theta_{Vd.n} - \frac{V_{m.nc}}{k_{Vm.n}} \sin\theta_{Vd.n}, \tag{6.61}$$

$$V_{AB.nc} = \frac{V_{m.ns}}{k_{Vm.n}} \sin\theta_{Vd.n} + \frac{V_{m.nc}}{k_{Vm.n}} \cos\theta_{Vd.n}, \tag{6.62}$$

$$I_{r.ns} = \frac{I_{m.ns}}{k_{Im.n}} \cos\theta_{Id.n} - \frac{I_{m.nc}}{k_{Im.n}} \sin\theta_{Id.n}, \tag{6.63}$$

$$I_{r.nc} = \frac{I_{m.ns}}{k_{Im.n}} \sin\theta_{Id.n} + \frac{V_{m.nc}}{k_{Im.n}} \cos\theta_{Id.n}. \tag{6.64}$$

where $k_{Vm.n}$ and $k_{Im.n}$ are amplitude attenuation factors and $\theta_{Vd.n}$ and $\theta_{Id.n}$ are phase delays, of n-order frequency components.

VI.4.3 Alternative Current Sensor – Sampling Inductor

To accurately sample the current information of the primary side, usually high bandwidth and high speed current sensor, such as SENSITEC CMS3000 series, is used. However, if the sampling rate of the AD module is not so high enough, the information of higher-order components (3^{rd}, 5^{th} …) cannot be sampled accurately because higher-order components of primary-side current are very small compared to fundamental component (The ratio of 3^{rd} and 1^{st} components' magnitudes is usually small than 5%). And often such high bandwidth and high speed current sensor is expensive and auxiliary isolated power supply is needed.

Here an alternative current sensor is proposed to obtain current information. A small inductor L_t, called as sampling inductor, is connected in series with the primary-side resonant tank. Voltage across L_t is noted as v_{Lt}, which is transformed to a signal (noted as $v_{Lt.s}$) for AD sampling after sensor, filter, and amplifier modules. When L_t's voltage (v_{Lt}) is sampled, its Fourier series coefficients ($V_{Lt.ns}$ and $V_{Lt.nc}$) can be obtained, and the primary- side current information can be calculated as:

$$I_{r.ns} = \frac{V_{Lt.nc}}{n\omega_s L_t}, \quad I_{r.nc} = -\frac{V_{Lt.ns}}{n\omega_s L_t}. \tag{6.65}$$

As the ratios of higher-order and fundamental components' magnitudes of v_{Lt} are higher than those of I_r, for example, the ratio of 3^{rd} and 1^{st} components' magnitudes of v_{Lt} is 2 times larger than that of I_r, this alternative approach would be able to produce more accurate measurements and samplings.

VI.4.4 Design Summary and Laboratory Prototype

Table VI-3 gives the detailed summary of the design and laboratory prototype. It should be noted that C_{s1} – C_{s4} are snubber capacitors of Q_1 – Q_4 for soft-switching realization. Fig. VI-5 shows the setup of the laboratory prototype. Sampling inductor L_t is applied in this experimental prototype and a 16:4 voltage

transformer is used to sense its voltage. For v_{AB} sensor, two cascaded voltage transformers (20:1 and 10:1) are used.

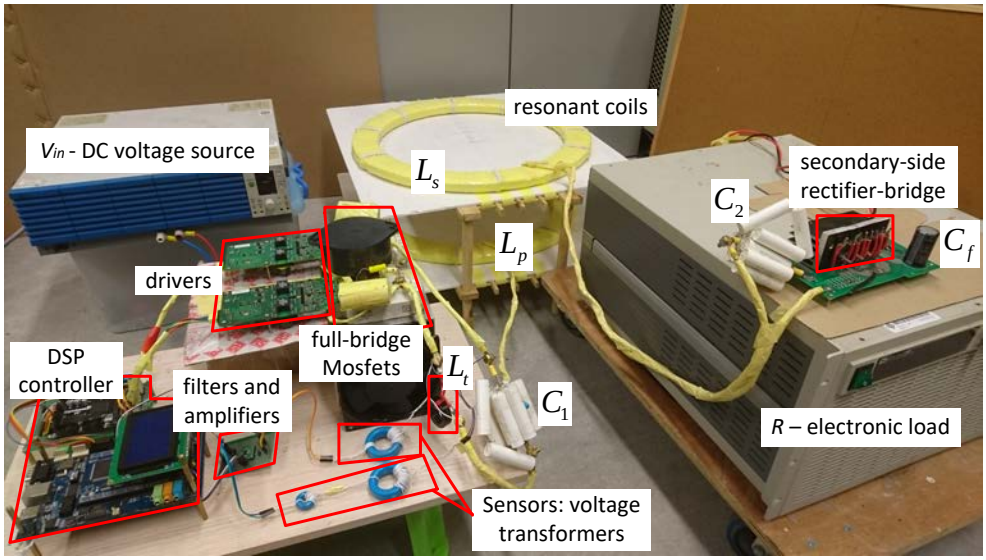


Fig. VI-5. Setup of the laboratory prototype

TABLE VI-3 Details of the laboratory prototype

Components	Details
f_s	84.46 kHz, 89.29 kHz;
D_{ab}	1.0, 0.8;
Q_1, Q_2, Q_3, Q_4	CREE CAS120M12BM2;
C_{s1}, C_{s2}, C_{s3}, C_{s4}	2.2 nF, 1 kV (polypropylene capacitors);
L_p, L_s	245.8 μH, 245.3 μH;
M	22.7 – 45.3 μH;
C_1, C_2	15.36 nF; 14.46 nF (5 kV polypropylene capacitors);
D_{s1}, D_{s2}, D_{s3}, D_{s4}	Vishay VS-30EPH06PbF;
C_f	220 μF, 450 V (electrolytic capacitor);
Controller	TI DSP28335;
v_{Lt} sensor	L_t=0.48 μH, 16:4 voltage transformer;
v_{AB} sensor	20:1 and 10:1 voltage transformers;
Drivers	CREE PT62SCMD17;
Filters	RC low-pass filter: R_{sf}=4.7 Ω; C_{sf}=2.2 nF;
Amplifiers	STMicroelectronics TSH114IPT.

VI.5 Experimental Results

Three experiments with different settings have been carried out to verify the proposed parameter estimation algorithm's wide applicability: one-stage DC-DC WPT resonant converter with adjustable duty cycle multi-level voltage source; no restriction on operation frequency; soft-switching operation; and unknown varying load resistance and mutual inductance. Fig. VI-6 – Fig. VI-9 shows the comparisons of estimated values and measured values of mutual inductance (M), output voltage (V_o), output power (P_o) and total efficiency (η) with load resistance R (20 – 50 Ω) varying (set by electronic load) in setting 1: D_{ab} = 1, d_m = 0, V_{in} = 100 V, f_s = 84.46 kHz. Fig. VI-10 – Fig. VI-13 plots the results with misalignment d_m (0 – 21 cm) varying in setting 2: D_{ab} = 1, R = 20 Ω, V_{in} = 100 V, f_s = 84.46 kHz. Fig. VI-14 – Fig. VI-17 shows the results with R (40 – 70Ω) varying in setting 3: D_{ab} = 0.8, d_m = 0, V_{in} = 150 V, f_s = 89.29 kHz. All the information of load resistance and mutual inductance (misalignment) is unknown to the DSP controller (the proposed algorithm).

Table VI-4 gives the errors statistics of the estimations in the above 3 settings. In all cases, the maximum error is within 3% with most average errors lower 2%. Compared to the method in [146], in which the average and maximum errors between measured and estimated values of coupling coefficient are 8.2% and 22.6% respectively, the errors of the proposed algorithm in this chapter are much smaller. Compared to the method in [154], in which the average and maximum errors between measured and estimated values of output voltage are 3.5% and 8.3% respectively, the errors of the proposed algorithm in this chapter are also much smaller.

Estimations of efficiencies are the most accurate compared to other parameters. Experimental results of setting 3 are not as accurate as those of setting 1 and 2 because operation frequency of setting 3 is higher, meaning sample points for a switching period are fewer. The results verify the proposed

algorithm's applicability and accuracy. Estimations can be more accurate if AD module with faster sampling rate is used.

Fig. VI-18 – Fig. VI-21 show the waveforms of resonant tank and soft-switching in setting 1 when R is 50 Ω while Fig. VI-22 – Fig. VI-25 shows the waveforms in setting 2 when d_m is 21 cm, where $v_{g1} - v_{g4}$ are GS voltages of $Q_1 - Q_4$ and $v_{Q1} - v_{Q4}$ are DS voltage of $Q_1 - Q_4$. And Fig. VI-26 – Fig. VI-29 shows those waveforms in setting 3 when R is 40 Ω. From the figures, there are obvious switching noises and spikes existing in v_{Lt}'s voltage waveforms. However, after filter and amplifier modules, the transformed signal $v_{Lt.s}$ is much smoother and suitable for AD sampling.

In the experiments, TI's DSP's integrated development environment tool CCS3.3 was used with DSP28335's operation frequency 150 MHz. The proposed algorithm totally requires 389,347 DSP clock cycles, and hence the total computation time is 2.6 ms. For application of wireless EV charging, change of M (mutual inductance) is usually due to mechanical motion of coils misalignment and change of R is usually resulted from the variation of battery's state-of-charge. In both cases, the changes are slow, and the computation time is fast enough to estimate the parameters online and response to any changes.

TABLE VI-4 Estimation errors (Maximum and average)

Setting	M errors (%)		V_o errors (%)		P_o errors (%)		η errors (%)	
	max	avg	max	avg	max	avg	max	avg
1	1.32	0.73	1.79	0.85	1.89	1.75	0.64	0.41
2	1.92	1.04	1.77	1.00	2.43	1.49	0.65	0.42
3	2.65	2.08	1.06	0.65	2.24	1.98	0.32	0.23

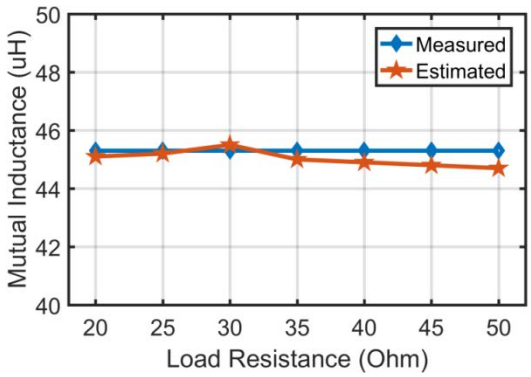


Fig. VI-6. Measured and estimated values of mutual inductance under varying load conditions with setting 1: D_{ab} = 1, d_m = 0, V_{in} = 100 V, f_s = 84.46 kHz

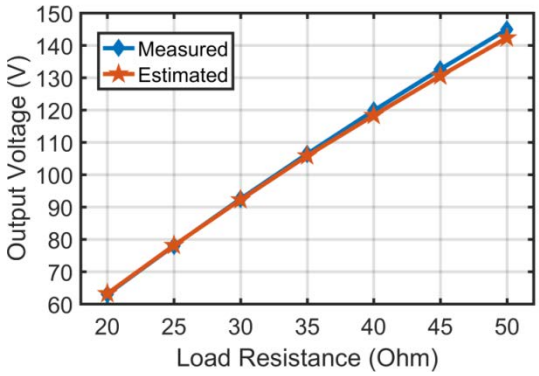


Fig. VI-7. Measured and estimated values of output voltage under varying load conditions with setting 1: D_{ab} = 1, d_m = 0, V_{in} = 100 V, f_s = 84.46 kHz

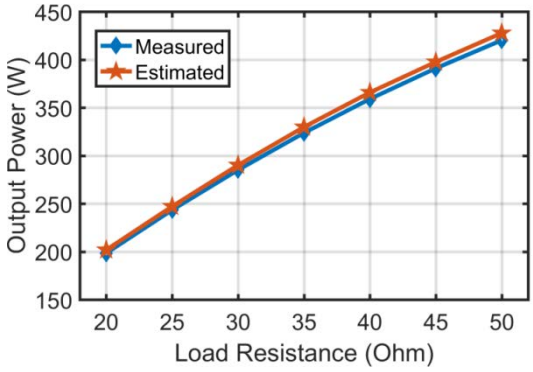


Fig. VI-8. Measured and estimated values of output power under varying load conditions with setting 1: D_{ab} = 1, d_m = 0, V_{in} = 100 V, f_s = 84.46 kHz

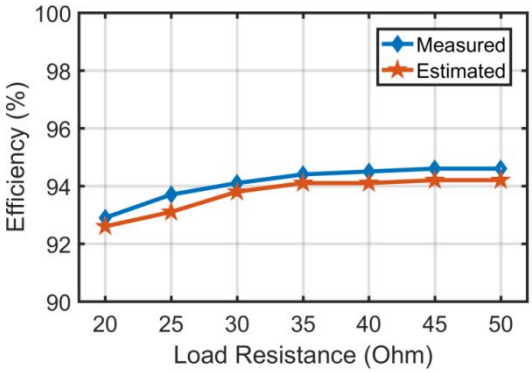


Fig. VI-9. Measured and estimated values of efficiency under varying load conditions with setting 1: D_{ab} = 1, d_m = 0, V_{in} = 100 V, f_s = 84.46 kHz

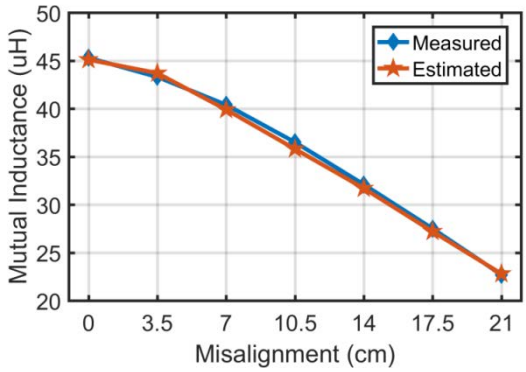


Fig. VI-10. Measured and estimated values of mutual inductance under varying misalignment conditions with setting 2: D_{ab} = 1, R = 20 Ω, V_{in} = 100 V, f_s = 84.46 kHz

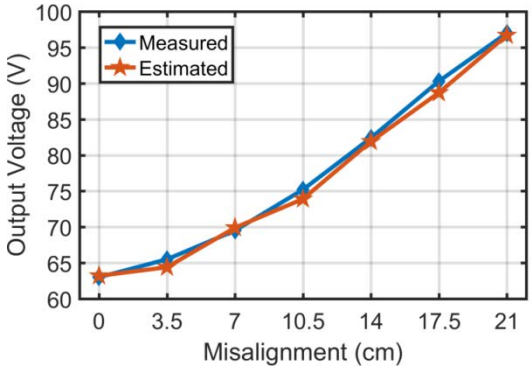


Fig. VI-11. Measured and estimated values of output voltage under varying misalignment conditions with setting 2: D_{ab} = 1, R = 20 Ω, V_{in} = 100 V, f_s = 84.46 kHz

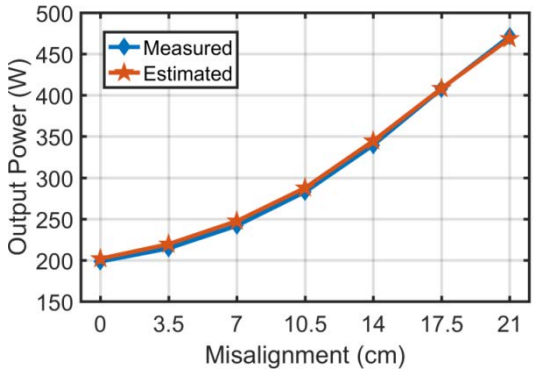


Fig. VI-12. Measured and estimated values of output power under varying misalignment conditions with setting 2: D_{ab} = 1, R = 20 Ω, V_{in} = 100 V, f_s = 84.46 kHz

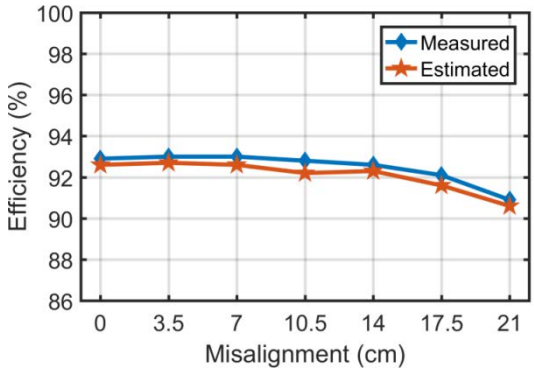


Fig. VI-13. Measured and estimated values of efficiency under varying misalignment conditions with setting 2: D_{ab} = 1, R = 20 Ω, V_{in} = 100 V, f_s = 84.46 kHz

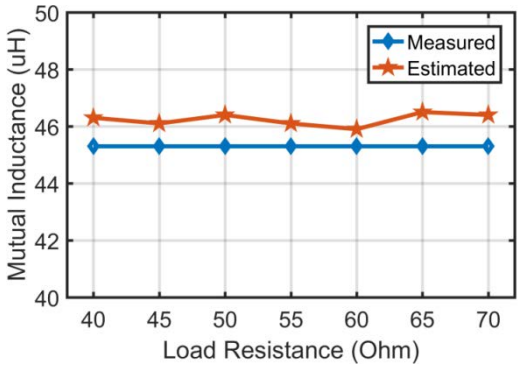


Fig. VI-14. Measured and estimated values of mutual inductance under varying load conditions with setting 3: D_{ab} = 0.8, d_m = 0, V_{in} = 150 V, f_s = 89.29 kHz

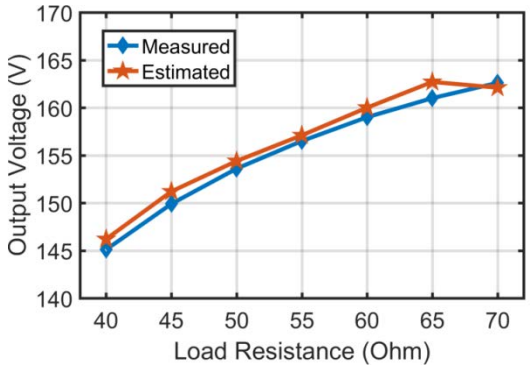


Fig. VI-15. Measured and estimated values of output voltage under varying load conditions with setting 3: D_{ab} = 0.8, d_m = 0, V_{in} = 150 V, f_s = 89.29 kHz

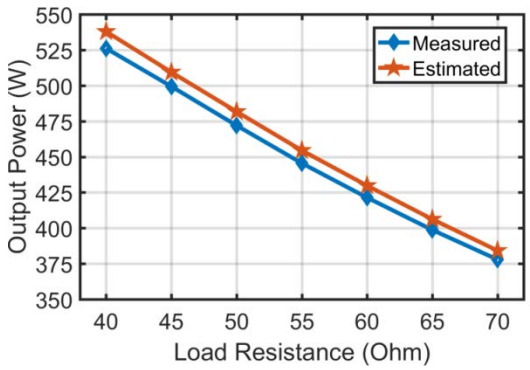


Fig. VI-16. Measured and estimated values of output power under varying load conditions with setting 3: D_{ab} = 0.8, d_m = 0, V_{in} = 150 V, f_s = 89.29 kHz

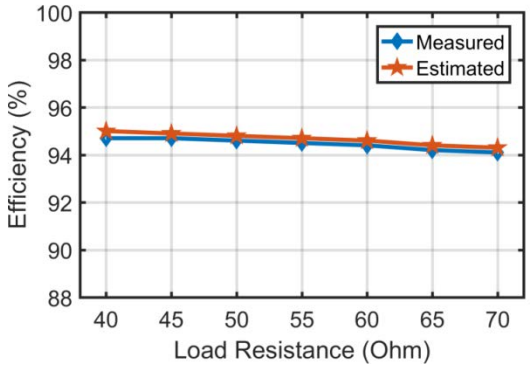


Fig. VI-17. Measured and estimated values of efficiency under varying load conditions with setting 3: D_{ab} = 0.8, d_m = 0, V_{in} = 150 V, f_s = 89.29 kHz

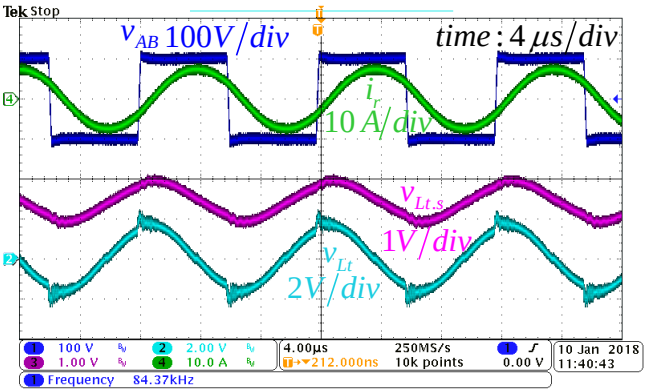


Fig. VI-18. Waveforms of primary-side v_{AB}, v_{Lt}, $v_{Lt.s}$, and i_r with setting 1 when R=50 Ω

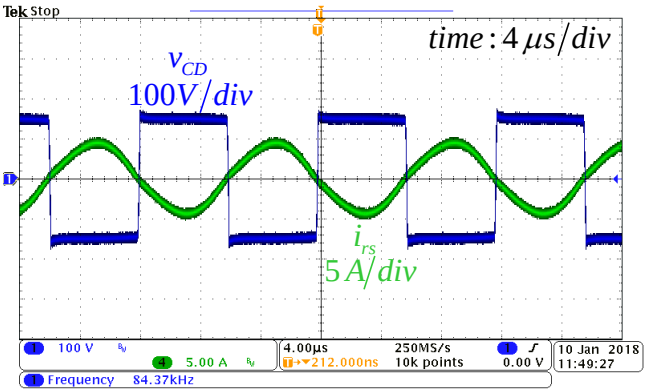


Fig. VI-19. Waveforms of secondary-side v_{CD} and i_{rs} with setting 1 when R=50 Ω

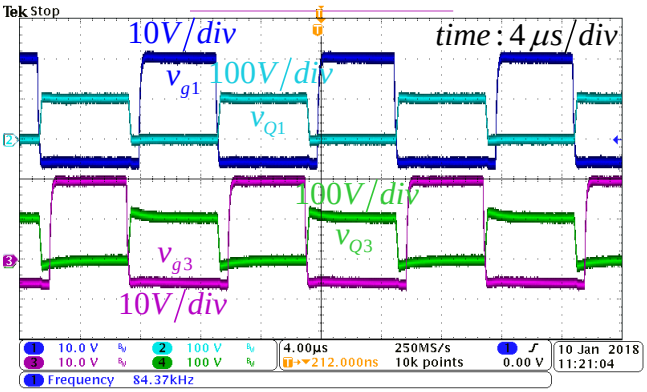


Fig. VI-20. Soft-switching waveforms of Q_1 and Q_3 with setting 1 when R=50 Ω

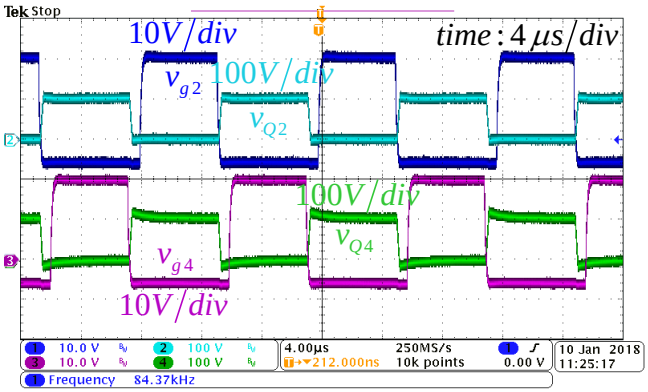


Fig. VI-21. Soft-switching waveforms of Q_2 and Q_4 with setting 1 when R=50 Ω

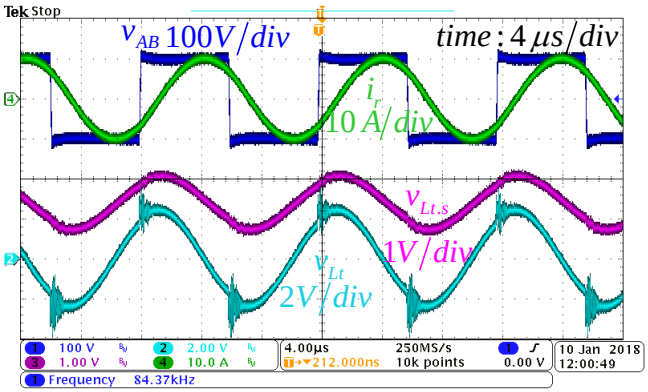


Fig. VI-22. Waveforms of primary-side v_{AB}, v_{Lt}, $v_{Lt.s}$, and i_r;with setting 2 when d_m=21 cm

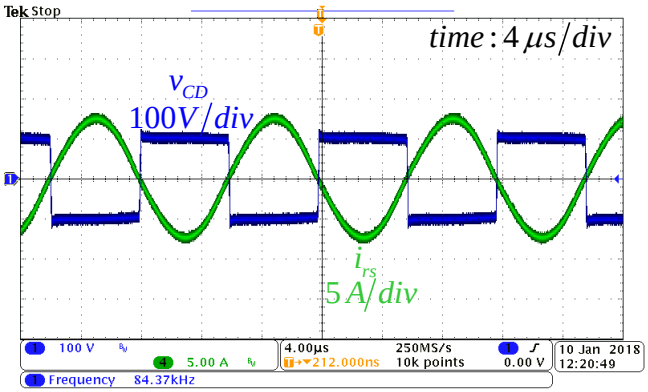


Fig. VI-23. Waveforms of secondary-side v_{CD} and i_{rs} with setting 2 when d_m=21 cm

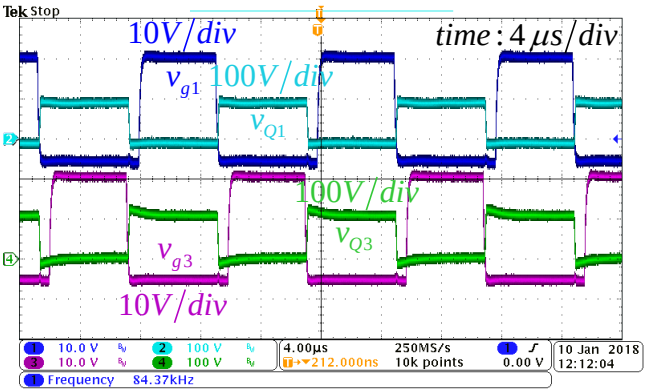


Fig. VI-24. Soft-switching waveforms of Q_1 and Q_3 with setting 2 when d_m=21 cm

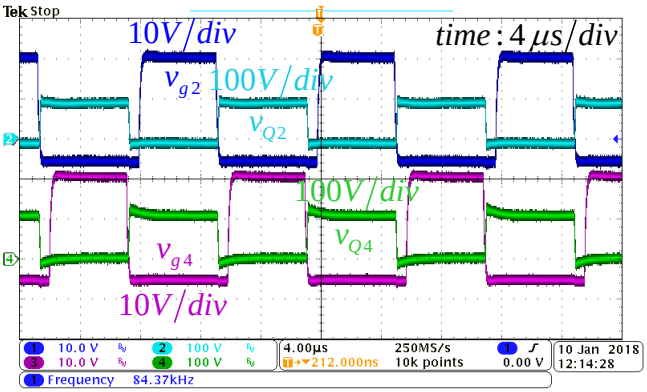


Fig. VI-25. Soft-switching waveforms of Q_2 and Q_4 with setting 2 when d_m=21 cm

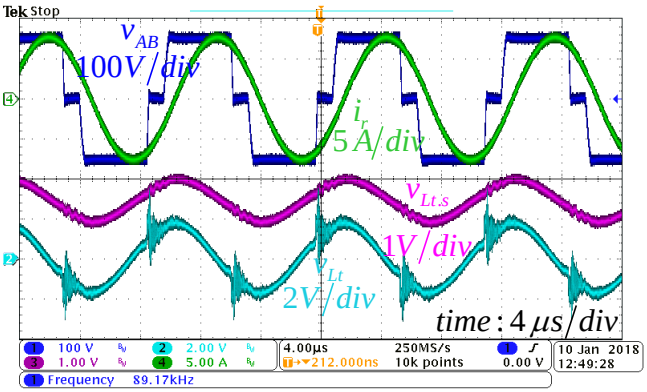


Fig. VI-26. Waveforms of primary-side v_{AB}, v_{Lt}, $v_{Lt.s}$, and i_r with setting 3 when R=40 Ω

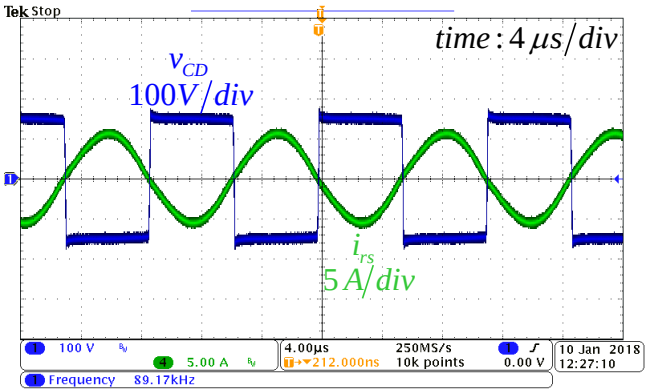


Fig. VI-27. Waveforms of secondary-side v_{CD} and i_{rs} with setting 3 when R=40 Ω

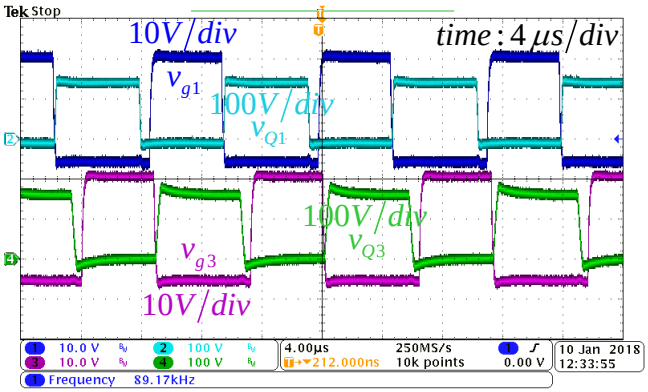


Fig. VI-28. Soft-switching waveforms of Q_1 and Q_3 with setting 3 when R=40 Ω

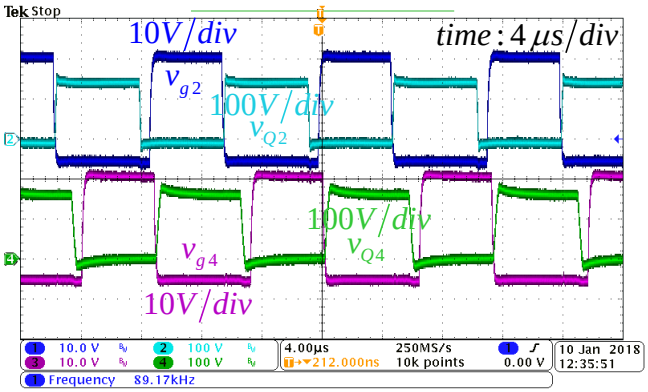


Fig. VI-29. Soft-switching waveforms of Q_2 and Q_4 with setting 3 when R=40 Ω

VI.6 Conclusion

This chapter firstly proposes an accurate steady-state analysis method of DC-DC WPT resonant converter, based on which a new parameter estimation algorithm is further developed and proposed. Such parameter estimation algorithm only samples primary-side voltage and current information and has a wider applicability and a higher accuracy compared to other existing estimation algorithms. Such algorithm can be applied in primary-side feedback and control system of DC-DC WPT resonant converter, which makes the physical implementation simpler and lower cost. Analysis and implementation of the algorithm are given out in details, and its applicability and accuracy have been proven by experimental results.

Chapter VII

Conclusions and Future Work

VII.1 Conclusions

Wireless power transfer has come more and more popular in people's daily life and industrial applications. Especially with EVs emerging in recent years, high power wireless EV charging draws much attention due to its dominant advantages: safety and convenience. For high power applications, in most cases, power is drawn from grid to loads by means of WPT in several conversion stages, among which the AC-DC PFC stage is essential to guarantee the power quality of grid. Therefore, typical WPT systems are commonly consist of two stages including an AC-DC PFC stage and a DC-DC WPT resonant converter stage. As improving efficiency, reducing production cost and control complexity of power converter systems are always the targets of research and development, the main efforts in this thesis are focused on improving the overall performances of WPT systems with the main contributions summarized as follows:

a) *A single-phase single-stage AC-DC WPT resonant converter with PFC is newly proposed*

The proposed converter combines a bridgeless PFC rectifier and a full-bridge inverter together to realize single-stage operation for PFC and DC-DC WPT conversion, which utilizes only 4 switches and 6 diodes, as the lowest count of power semiconductor devices compared with other existing single-phase AC-DC WPT resonant converters with PFC. Generally, less power switches means less production cost. Also because of the reduction in power semiconductor devices count, overall power loss decreases and therefore efficiency of the whole WPT system increases. The maximum efficiency in experiments of laboratory

prototype with 2.56 kW output power achieves 90.1%, remarkably larger than other existing single-phase AC-DC WPT resonant converters with PFC. In terms of PFC functionality, THD of input current and power factor achieve 15.4% and 0.99 respectively. Compared with two-stage AC-DC WPT converters with PFC, which use two separate controllers to control two stages, the control complexity of the proposed converter is reduced significantly due to utilizing only one controller with one control parameter.

b) *A new control method of the proposed single-phase single-stage AC-DC WPT resonant converter with PFC is proposed*

Though the proposed single-phase single-stage AC-DC WPT resonant converter exhibits many advantages over the existing single-phase AC-DC WPT converters with PFC, there is room for further improvement and a new control method is hence proposed to further reduce the bus voltage and improve the power quality. In this proposed approach, average input current, working in DCM, is controlled to follow the input voltage v_s so as to improve the power quality. Simulation results show that THD of input current and power factor are smaller than 1% and larger than 0.99 respectively while the bus voltage is reduced and maintained at 500 V within wide load range as compared to 723.5 V at 20% load condition under the original control method.

c) *A three-phase single-stage AC-DC WPT resonant converter with PFC is newly proposed*

The proposed converter combines a three-phase diode rectifier and a T-type three-level inverter to realize single-stage operation for three-phase PFC and DC-DC WPT conversion, which utilizes only 4 switches and 10 diodes. The count of power semiconductor devices is also the lowest compared with those of other existing three-phase AC-DC WPT resonant converters with PFC. Hence, production cost and power loss are also reduced. The maximum efficiency of the proposed converter under 100% load condition with 1.25 kW output power achieves 91.7%. Compared with the proposed single-phase single-stage AC-DC

WPT resonant converter with PFC, bus voltage is reduced and power quality is improved significantly. The bus voltage is maintained at 320 V when input voltage is 110 V_{rms} at different load conditions. The THD of input current and power factor achieve 3.5% and 1.0 respectively. Because of inherent superiority of three-phase topology, the proposed converter possesses larger power capacity and hence more suitable for high power applications.

d) A new parameter estimation algorithm of DC-DC WPT resonant converter is newly proposed

An accurate steady-state analysis method of DC-DC WPT resonant converter with series-series topology is proposed for the first time. Unlike common analysis method of DC-DC resonant converters with fundamental harmonic approximation (FHA), the proposed accurate analysis method considers both fundamental and higher-order components in the circuit. The proposed analysis method exhibits more accurate results, though computation process is more complicated. Further to the analysis method, a new parameter estimation algorithm is newly proposed, which is capable of estimating mutual inductance, output voltage, output power, and efficiency only with primary-side voltage and current information, under unknown misalignment and load conditions. It is suitable for many circumstances which are not previously considered in other existing primary-side parameter estimation methods. Furthermore, errors of estimations in the experiments (not exceed 3%) are smaller than those of other existing parameter estimation methods. Such algorithm is aimed to be applied in primary-side feedback and control of DC-DC or AC-DC WPT resonant converters so that neither additional wireless communication device nor secondary-side measurement units and controller is needed, which makes the physical implementation simpler and with lower cost.

VII.2 Future Work

The research in the near future will focus on the control and optimization of single-stage AC-DC WPT resonant converters for their practical use in industrial applications.

Firstly, the parameter estimation algorithm will be applied in the closed-loop control system of the proposed converters: single-phase and three-phase single-stage AC-DC WPT resonant converters with primary-side feedback and control. Such primary-side feedback and control method will make the WPT system with lower cost and simpler physical implementation because neither the measurement units nor controller for the secondary side are required, and so as wireless communication devices can be eliminated too.

Secondly, while multi-frequency wireless power transfer topologies have been studied on their steady-state characteristics [88] [89] [159] – [161], the proposed primary-side feedback and control algorithm could be further extended and enhanced for specific output requirements and maximum energy efficiency tracking of multi-frequency WPT topologies. Furthermore, the proposed single-phase and three-phase single-stage AC-DC topologies will be further applied and studied in multi-frequency WPT converters.

Thirdly, performances improvements (reducing bus voltage, furtherly improving power quality, wider load range operation with high efficiency) of the two proposed single-phase and three-phase topologies will be studied and researched. The main research direction would focus on modulation methods and control algorithm of the two topologies by investigating characteristics of SS WPT resonant tank deeply. In addition, other topologies of WPT resonant tank, including SP, PS and PP will be studied and integrated in the single-stage AC-DC topologies with performance evaluation in various aspects. Soft-switching technique is important for switching mode power converters because of it guarantees high efficiency. Currently, soft switching cannot be realized in the

proposed three-phase topology. Therefore, one of the coming tasks will focus on the realization of soft-switching in the proposed three-phase topology so as to further improve its efficiency. Moreover, soft-switching realization at light load conditions of the proposed single-phase topology will also be studied and developed.

Last but not least, bi-directional topologies and operations of single-stage AC-DC WPT resonant converters will be researched and developed, in order to meet the EV wireless charging requirements of modern smart grid: vehicle-to-grid power delivery (V2G) and grid-to-vehicle power delivery (G2V). Topologies and corresponding control methods of bi-directional single-stage AC-DC WPT resonant converters will be of great significance in smart grid applications. Bi-directional AC-DC WPT resonant converters are capable of delivering power wirelessly in two directions: from AC power gird (three-phase or single-phase) to DC battery load; and from DC battery load to AC power grid. The largest advantage of bi-directional single-stage AC-DC WPT resonant converters is the greatly reduced amount of power devices. The power density and utilization rate of power devices are also huge advantages. Bi-directional DC-DC transformer-based-isolated converters or WPT resonant converters have been studied and developed widely and deeply with the use of dual active bridge (DAB). However, there are few researches and studies on bi-directional single-stage AC-DC WPT resonant converters and it is believed that they will be popular and useful due to their unique superiorities in the coming future.

Appendices

A. Variables defined in the small signal analysis process

In Chapter II, when doing small signal analysis, each variable can be separated into a large signal and a small perturbed signal, as shown in (A.1) – (A.15).

$$v_{in} = V_{in} + \hat{v}_{in}, \tag{A.1}$$

$$d = D + \hat{d}, \tag{A.2}$$

$$\omega_s = \Omega_s + \hat{\omega}_s, \tag{A.3}$$

$$i_{load} = 0 + \hat{i}_{load}, \tag{A.4}$$

$$M = M_0 + \hat{m}, \tag{A.5}$$

$$v_{AB.1s} = V_{AB.1s} + \hat{v}_{AB.1s}, \tag{A.6}$$

$$i_{r.1s} = I_{r.1s} + \hat{i}_{r.1s}, \tag{A.7}$$

$$i_{r.1c} = I_{r.1c} + \hat{i}_{r.1c}, \tag{A.8}$$

$$i_{rs.1s} = I_{rs.1s} + \hat{i}_{rs.1s}, \tag{A.9}$$

$$i_{rs.1c} = I_{rs.1c} + \hat{i}_{rs.1c}, \tag{A.10}$$

$$v_{C1.1s} = V_{C1.1s} + \hat{v}_{C1.1s}, \tag{A.11}$$

$$v_{C1.1c} = V_{C1.1c} + \hat{v}_{C1.1c}, \tag{A.12}$$

$$v_{Cf} = V_{Cf} + \hat{v}_{Cf}, \tag{A.13}$$

$$v_{CD.1s} = V_{CD.1s} + \hat{v}_{CD.1s}, \tag{A.14}$$

$$v_{CD.1c} = V_{CD.1c} + \hat{v}_{CD.1c}. \tag{A.15}$$

In Chapter II, parameters K_1, K_2, J_1, J_2, P_1, P_2, H_1, H_2, H_3, G_1, G_2, G_3 are defined as (A.16) – (A.27).

$$K_1 = \frac{2}{\pi} \cdot \frac{I_{rs.1s}}{\sqrt{{I_{rs.1s}}^2 + {I_{rs.1c}}^2}}, \tag{A.16}$$

$$K_2 = \frac{2}{\pi} \cdot \frac{I_{rs.1c}}{\sqrt{{I_{rs.1s}}^2 + {I_{rs.1c}}^2}}, \tag{A.17}$$

$$J_1 = I_{r.1s} \cos\left(\frac{\pi}{2} D\right), \tag{A.18}$$

$$J_2 = \frac{2}{\pi} \sin\left(\frac{\pi}{2} D\right), \tag{A.19}$$

$$P_1 = \frac{4}{\pi} \sin\left(\frac{\pi}{2} D\right), \tag{A.20}$$

$$P_2 = 2V_{in} \cos\left(\frac{\pi}{2} D\right), \tag{A.21}$$

$$H_1 = -\frac{4V_{Cf}}{\pi} \cdot \frac{{I_{rs.1c}}^2}{\left({I_{rs.1s}}^2 + {I_{rs.1c}}^2\right)^{3/2}}, \tag{A.22}$$

$$H_2 = \frac{4V_{Cf}}{\pi} \cdot \frac{I_{rs.1s} I_{rs.1c}}{\left({I_{rs.1s}}^2 + {I_{rs.1c}}^2 \right)^{3/2}}, \tag{A.23}$$

$$H_3 = -\frac{4}{\pi} \cdot \frac{I_{rs.1s}}{\left({I_{rs.1s}}^2 + {I_{rs.1c}}^2 \right)^{1/2}}, \tag{A.24}$$

$$G_1 = \frac{4V_{Cf}}{\pi} \cdot \frac{I_{rs.1s} I_{rs.1c}}{\left({I_{rs.1s}}^2 + {I_{rs.1c}}^2 \right)^{3/2}}, \tag{A.25}$$

$$G_2 = -\frac{4V_{Cf}}{\pi} \cdot \frac{{I_{rs.1s}}^2}{\left({I_{rs.1s}}^2 + {I_{rs.1c}}^2 \right)^{3/2}}, \tag{A.26}$$

$$G_3 = -\frac{4}{\pi} \cdot \frac{I_{rs.1c}}{\left({I_{rs.1s}}^2 + {I_{rs.1c}}^2 \right)^{1/2}}. \tag{A.27}$$

B. Coefficients of state-space model of the DC-DC WPT resonant converter

In Chapter II, Matrix *A*, *B*, *C*, and *D* are defined as the coefficients of state-space model of the DC-DC WPT resonant converter, which are obtained as (B.1) – (B.4).

$$A=\begin{bmatrix}
-\frac{L_s R_{lp}}{L_p L_s - M_0^2} & \Omega_s & \frac{M_0\left(R_{ls}-H_1\right)}{L_p L_s - M_0^2} & -\frac{M_0 H_2}{L_p L_s - M_0^2} & -\frac{L_s}{L_p L_s - M_0^2} & 0 & \frac{M_0}{L_p L_s - M_0^2} & 0 & -\frac{M_0 H_3}{L_p L_s - M_0^2} \\
-\Omega_s & -\frac{L_s R_{lp}}{L_p L_s - M_0^2} & -\frac{M_0 G_1}{L_p L_s - M_0^2} & \frac{M_0\left(R_{ls}-G_2\right)}{L_p L_s - M_0^2} & 0 & -\frac{L_s}{L_p L_s - M_0^2} & 0 & \frac{M_0}{L_p L_s - M_0^2} & -\frac{M_0 G_3}{L_p L_s - M_0^2} \\
\frac{M_0 R_{lp}}{L_p L_s - M_0^2} & 0 & -\frac{L_p\left(R_{ls}-H_1\right)}{L_p L_s - M_0^2} & \Omega_s + \frac{L_p H_2}{L_p L_s - M_0^2} & \frac{M_0}{L_p L_s - M_0^2} & 0 & -\frac{L_p}{L_p L_s - M_0^2} & 0 & \frac{L_p H_3}{L_p L_s - M_0^2} \\
0 & \frac{M_0 R_{lp}}{L_p L_s - M_0^2} & \frac{L_p G_1}{L_p L_s - M_0^2} - \Omega_s & -\frac{L_p\left(R_{ls}-G_2\right)}{L_p L_s - M_0^2} & 0 & \frac{M_0}{L_p L_s - M_0^2} & 0 & -\frac{L_p}{L_p L_s - M_0^2} & \frac{L_p G_3}{L_p L_s - M_0^2} \\
\frac{1}{C_1} & 0 & 0 & 0 & 0 & \Omega_s & 0 & 0 & 0 \\
0 & \frac{1}{C_1} & 0 & 0 & -\Omega_s & 0 & 0 & 0 & 0 \\
0 & 0 & \frac{1}{C_2} & 0 & 0 & 0 & 0 & \Omega_s & 0 \\
0 & 0 & 0 & \frac{1}{C_2} & 0 & 0 & -\Omega_s & 0 & 0 \\
0 & 0 & \frac{K_1}{\left(1+\frac{r_C}{R}\right)C_f} & \frac{K_2}{\left(1+\frac{r_C}{R}\right)C_f} & 0 & 0 & 0 & 0 & -\frac{1}{R\left(1+\frac{r_C}{R}\right)C_f}
\end{bmatrix} \tag{B.1}$$

$$B=\begin{bmatrix}
I_{r.1c} & \frac{L_s P_1}{L_p L_s - M_0^2} & \frac{L_s P_2}{L_p L_s - M_0^2} & \frac{\left(I_{rs.1c} L_s - I_{r.1c} M_0\right)\Omega_s}{L_p L_s - M_0^2} & 0 \\
-I_{r.1s} & 0 & 0 & \frac{\left(I_{r.1s} M_0 - I_{rs.1s} L_s\right)\Omega_s}{L_p L_s - M_0^2} & 0 \\
I_{rs.1c} & -\frac{M_0 P_1}{L_p L_s - M_0^2} & -\frac{M_0 P_2}{L_p L_s - M_0^2} & \frac{\left(I_{r.1c} L_p - I_{rs.1c} M_0\right)\Omega_s}{L_p L_s - M_0^2} & 0 \\
-I_{rs.1s} & 0 & 0 & \frac{\left(I_{rs.1s} M_0 - I_{r.1s} L_p\right)\Omega_s}{L_p L_s - M_0^2} & 0 \\
V_{C1.1c} & 0 & 0 & 0 & 0 \\
-V_{C1.1s} & 0 & 0 & 0 & 0 \\
V_{C2.1c} & 0 & 0 & 0 & 0 \\
-V_{C2.1s} & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & \frac{1}{\left(1+\frac{r_C}{R}\right)C_f}
\end{bmatrix} \tag{B.2}$$

$$C=\begin{bmatrix}
0 & 0 & K_1 r_C' & K_2 r_C' & 0 & 0 & 0 & 0 & \frac{r_C'}{r_C} \\
J_2 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix} \tag{B.3}$$

$$D = \begin{bmatrix} 0 & 0 & 0 & 0 & r_C' \\ 0 & 0 & J_1 & 0 & 0 \end{bmatrix} \tag{B.4}$$

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