VERTICAL GRAPHENE TUNNELLING HETEROSTRUCTURES WITH ULTRATHIN FERROELECTRIC FILM AS A TUNNEL BARRIER

CHAN Hung Lit

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The Hong Kong Polytechnic University

Department of Applied Physics

Vertical Graphene Tunnelling Heterostructures with Ultrathin Ferroelectric Film as a Tunnel Barrier

CHAN Hung Lit

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Philosophy

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CERTIFICATE OF ORIGINALITY

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Abstract

Two-dimensional (2D) layered materials have attracted enormous interests in both fundamental research and industrial applications. When one dimension is restricted in size, 2D materials exhibit distinct properties, which are different from their bulk materials. With its unique 2D structure, graphene, a single layer of carbon atoms in a hexagonal lattice, reveals remarkable electronic, thermal, optical and mechanical properties. Recently, graphene can be coupled with ferroelectric materials to form functional graphene/ferroelectric hybrid structure. Ferroelectric materials show a spontaneous ferroelectric polarization, which can be switched via an external electric field. The novel graphene/ferroelectric heterostructure can yield fascinating behaviors and reveal great potential for various functional devices.

In this thesis, firstly, a ferroelectric tunnel junction (FTJ) based on graphene/$BaTiO_3$/Nb:$SrTiO_3$ heterostructure can be fabricated. The crystal quality and layer number of the graphene nanosheets are studied by Raman spectroscopy. The crystal structure of the $BaTiO_3$/Nb:$SrTiO_3$ is revealed by X-ray diffraction (XRD) characterization. The chemical composition of the $BaTiO_3$ films is investigated by X-ray photoelectron spectroscopy (XPS). The morphology and ferroelectricity of the $BaTiO_3$ thin films are determined with piezoresponse force microscopy (PFM). The

electrical resistance switching is studied in the graphene/$BaTiO_3$/Nb:$SrTiO_3$ heterostructure. The ON/OFF conductance ratio is found to increase with decreasing Nb concentration from 1.0 wt% to 0.1 wt% on the Nb:$SrTiO_3$ semiconductor substrates, due to ferroelectric modulation of barrier height and width. A remarkable ON/OFF ratio up to 10^3 is obtained in the devices when introducing Nb concentration of 0.1 wt% at room temperature. Furthermore, good retention property and switching reproducibility can be achieved in the devices, which are suitable for non-volatile memory applications. Secondly, vertical graphene heterostructure FET (VGHFET) employing ultrathin ferroelectric film as a tunnel barrier can be fabricated. The ferroelectric switching may add tunability to the VGHFET. The multilayer devices are based on Au/Sm:$BiFeO_3$/graphene/SiO_2/Si, Au/Al_2O_3/graphene/$BaTiO_3$/Nb:$SrTiO_3$ as well as Au/Al_2O_3/graphene/$BaTiO_3$/$La_{0.7}Sr_{0.3}MnO_3$/$SrTiO_3$ heterostructure. The output and transfer electrical characteristics of the devices can be observed, which are beneficial for logic electronic applications.

In conclusion, vertical graphene tunneling heterostructure with ultrathin ferroelectric barrier has been studied. The electronic properties and device demonstrations of FTJs and VGHFETs have been investigated. These fundamental studies provide a platform for further research of 2D/ferroelectric hybrid structure and show promise for future applications on the nanoscale.

List of Publications

Journal Papers

1. **Hung-Lit Chan**, Shuoguo Yuan, Jianhua Hao*, "Vertical graphene tunneling heterostructure with ultrathin ferroelectric $BaTiO_3$ film as a tunnel barrier", ***Phys. Status Solidi RRL*** 12, 1800205 (2018).

2. Shuoguo Yuan, Xin Luo, **Hung-Lit Chan**, Yawei Dai, Maohai Xie, Jianhua Hao*, "Room-temperature ferroelectricity in $MoTe_2$ down to the atomic monolayer limit", submitted.

Presentations in International Conferences

1. **Hung-Lit Chan**, Shuoguo Yuan, Zhibin Yang, Jianhua Hao*, "Graphene-based tunneling heterostructure with ferroelectric thin film", conference poster presentation, E-MRS 2018 Spring Meeting, 18-22 June 2018, France.

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List of Acronyms

Acronyms	Description
BTO	Barium titanate, $BaTiO_3$
SBFO	Sm-doped bismuth ferrite, $Sm:BiFeO_3$
NSTO	Nb-doped strontium titanate, $Nb:SrTiO_3$
LSMO	Lanthanum strontium manganite, $La_{1-x}Sr_xMnO_3$
VGHFET	Vertical graphene heterostructure field-effect transistor
VGFTH	Vertical graphene-ferroelectric tunneling heterostructure
FTJ	Ferroelectric tunnel junction
TER	Tunneling electroresistance
CVD	Chemical vapor deposition
PLD	Pulsed laser deposition
XRD	X-ray diffraction
XPS	X-ray photoemission spectroscopy
PFM	Piezoresponse force microscopy

Chapter 1 Introduction

1.1 Background of 2D graphene sheets

The requirement of more compact and powerful devices in electronic and optoelectronic applications has been growing since the silicon has achieved its limit. In the recent decade, two-dimensional (2D) materials have drawn considerable attention for both scientific research and device fabrication. When a dimension approaches atomic scale, 2D materials reveal fascinating characteristics which are dissimilar to their bulk parents [1, 2]. Graphene nanosheets were discovered via a mechanical exfoliation method by Novoselov and Geim in 2004 [3]. Graphene is a single carbon layer with sp^2 hybridization in a honeycomb lattice structure. The layered graphene is suspended in some organic solutions or adhered on a flat substrate surface rather than being an integral component of a carbon material. Figure 1.1(a) shows the schematic graphene lattice. There are two interpenetrating carbon atoms per unit cell in the lattice. The bond length between two nearest neighbor carbon atoms is 1.42 Å and the lattice parameter is around 2.46 Å [4]. As shown in Figure 1.1(b), the conduction bands and valence bands of graphene intersect at the Dirac point in the low-energy band structure. The charge-neutrality point, which refers to the Fermi level in the undoped graphene, locates at the Dirac point [5]. Therefore, graphene has nearly zero bandgap, which

makes it behave like a semimetal.

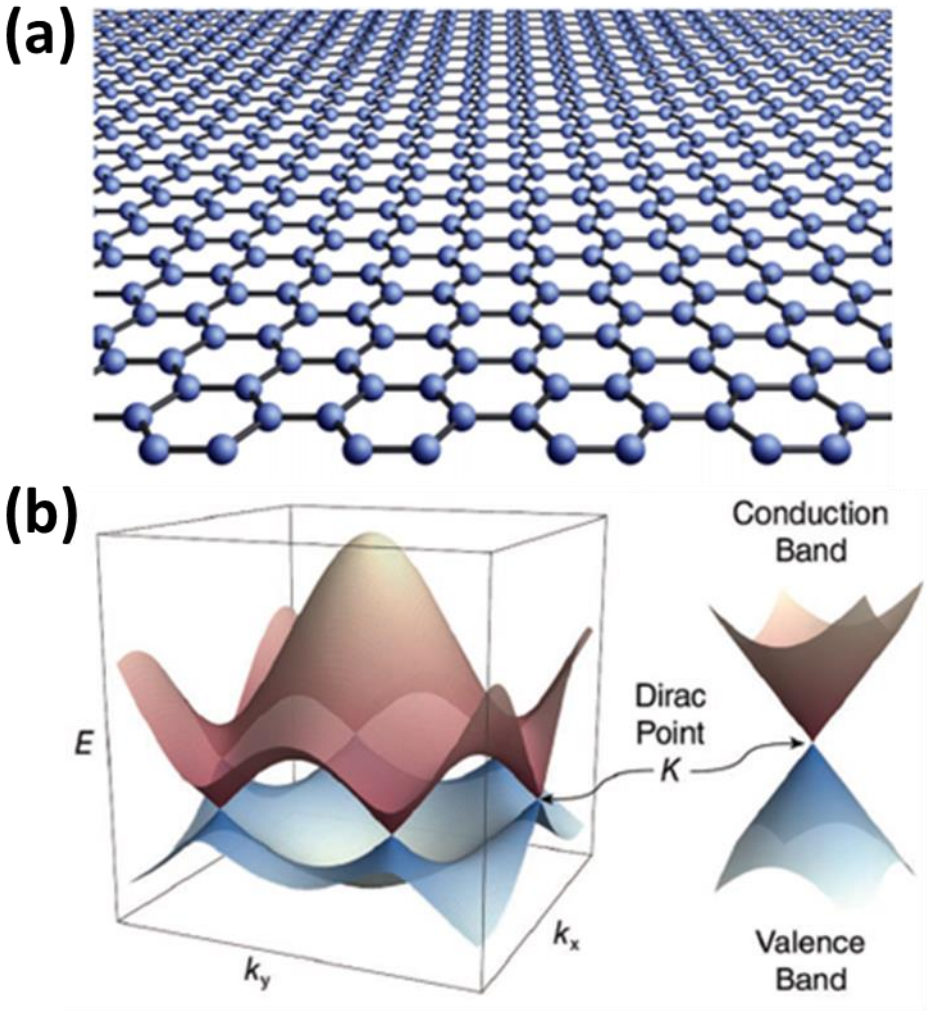


Figure 1. 1 (a) Schematic illustration of graphene lattice [4]. (b) The low-energy electronic band structure of graphene [5].

With its unique 2D layered structure and zero-bandgap nature, graphene has revealed many outstanding properties. As electrons in graphene behave like massless Dirac fermions, the electrons can transport a long distance without significant scattering, leading to ultrahigh electron mobility at room temperature. The reported electron mobility of graphene can exceed 10^4 cm^2/Vs, which is approximately 10 times higher

than silicon [6]. The room-temperature ballistic transport for an electron mean free path has also been demonstrated on a micrometer scale [7]. With remarkable ambipolar electric field effect, graphene can change the charge carriers between electrons and holes in concentration in the order of 10^{11} cm^{-2} [8]. Interestingly, a pronounced quantum Hall effect can be observed in graphene at room temperature [9]. In addition, graphene also exhibits a wide range of excellent electrical, optical, thermal and mechanical properties. Graphene reveals high conductivity [10-12], excellent optical transparency (~97.7 %) [13-15], good mechanical flexibility (~1.0 TPa Young's modulus and 130 GPa fracture strength) [16-18], remarkable thermal conductivity (3000-5000 W/mK) [19], high specific area (~2630 m^2/g) [20, 21], high chemical stability and good impermeability with gas and liquid [22, 23]. These unique properties make graphene a potential candidate for a series of electronic and optoelectronic applications, such as touch screens [24], liquid crystal displays [25], field effect transistors [26], memories [27, 28], biosensors [29, 30], light-emitting diodes [31, 32], solar cells [33, 34] and photodetectors [35, 36].

1.2 Vertical graphene heterostructure field-effect transistor

The first prototype of graphene-based field-effect transistor (GFET) made by coupling graphene with oxidized silicon was reported by Novoselov *et al*. [6]. Due to absence of a finite bandgap between its conduction and valence bands in graphene,

GFET remains conducting even when switched off. Hence, a fundamental problem of the planar graphene-based transistors is their limited current ON/OFF ratio [37-41]. Other methods have been employed to induce a bandgap in the graphene, such as using bilayer graphene, nanoribbons and chemical derivatives, but it has proven to degrade the graphene's electronic quality [42-44]. To improve the performance of graphene-based devices, Georgiou *et al*. proposed a novel vertical graphene heterostructure field-effect transistor (VGHFET) in 2012 [45]. As shown in Figure 1.2(a), the device is based on vertically stack graphene/tungsten disulphide (WS_2)/graphene heterostructure on an SiO_2/Si substrate. The WS_2 thin film serves as an atomically thin tunnel barrier. The electrons can tunnel from a graphene layer to another layer through the ultrathin barrier. The operation of the VGHFET depends on the changes of Fermi level of the graphene and the effective barrier height of the tunnel barrier adjacent to the graphene. Figure 1.2(b) shows the band diagram without external gate voltage V_g and bias voltage V_b applied. When a V_g is applied between the silicon substrate and the graphene layer, the charge carrier concentration and the Fermi level in the graphene is changed. By taking the advantage of the low density of states of graphene, large variation in Fermi level can be achieved in a given V_g. The sign of the Fermi level shift relies on the polarity of the V_g applied. Figure 1.2(c) reveals that a negative V_g shifts the Fermi level of the graphene downwards from the neutrality point, which increases the tunneling barrier

height. Fewer charge carriers can tunnel through the barrier. The device is set to the OFF state. Figure 1.2(d) shows that a positive V_g shifts the Fermi level of the graphene upwards, which decreases the tunneling barrier height. More carriers can pass through the barrier. The device is driven into the ON state. Based on the operation principle, ON/OFF ratio enhancement is expected in the vertical graphene-based transistor. The results pave the way to develop two-dimensional multilayer structure with fascinating characteristics and enhanced performance.

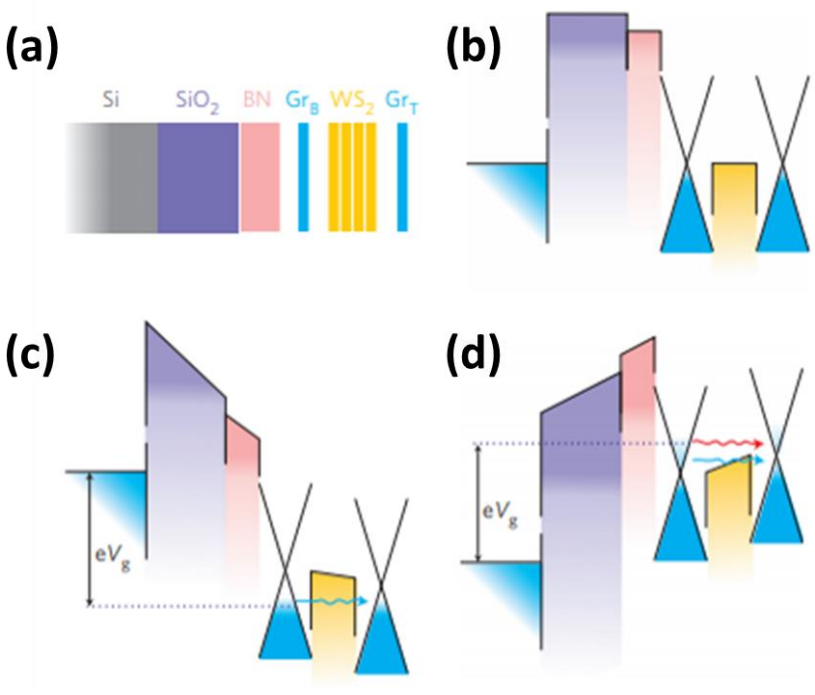


Figure 1. 2 (a) Schematic vertical architecture of graphene-based heterostructure. Band diagrams of the device at no external V_g and V_b applied (b), at negative V_g (c) and at positive V_g (d) [45].

It is interesting to note that using barrier materials with a relatively small bandgap such as tungsten disulphide (WS_2) [45] and molybdenum disulphide (MoS_2) semiconductor [46, 47] can increase the ON/OFF ratio of the vertical graphene-based transistor. With the low density of states of graphene, the significant changes in the Fermi level of the graphene can exceed the tunneling barrier height, leading to dramatic ON/OFF enhancement. However, barrier materials with a relatively large bandgap such as hexagonal-boron nitride (hBN) insulator [48, 49] form a high tunneling barrier, so changes in the Fermi level of the graphene are small compared to the barrier height. Hence, ON/OFF enhancement is insignificant using large-bandgap materials. There is a wide range of available materials that could be integrated into the graphene-based vertical stacks. In addition to the flakes of 2D layered materials, other possible materials also involve inorganic semiconductor including silicon [50] and indium gallium zinc oxide (IGZO) [51, 52], as well as organic semiconductor such as fullerene (C_{60}) [53] and pentacene thin films [54, 55]. The employment of different materials as the tunneling barrier could bring new functionality to the multilayer graphene-based heterostructure to modify the device characteristics.

In the view of device architecture, there are three types of VGHFETs: back-gated, top-gated and dual-gated FETs. A back-gated FET can be fabricated by depositing the vertically stacked graphene-based heterostructure on an oxidized Si substrate [53]

(Figures 1.3(a) and (b)). The top-gated FET can be prepared by forming an insulator layer such as aluminum oxide (Al_2O_3) and hafnium oxide (HfO_2) on top of the graphene-based vertical stacks to serve as a gate dielectric [51] (Figures 1.3(c) and (d)). As shown in Figures 1.3(e) and (f), the dual-gated architecture can be implemented with both the back- and top- gate dielectric layers [56]. The charge carrier concentration and Fermi level of the graphene layers can be tuned by both gate dielectrics simultaneously to further control the carrier transport in the vertical graphene-based devices.

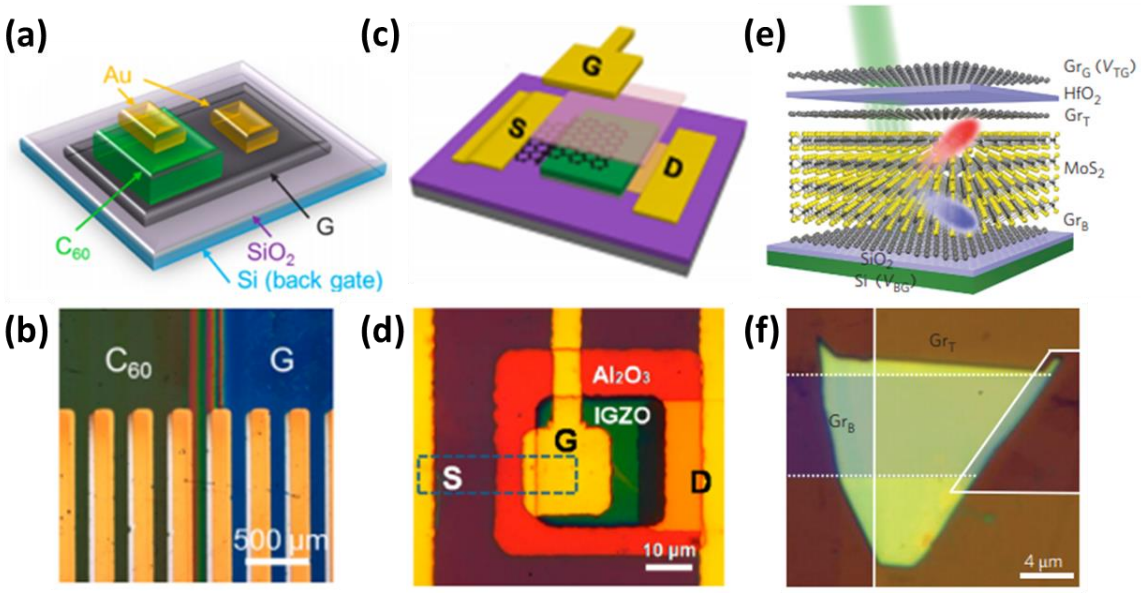


Figure 1. 3 Schematic diagrams of the back-gated (a), top-gated (c) and dual-gated (e) architectures of VGHFETs respectively. (b, d, f) Corresponding optical images of the device architectures in (a, c, e) [51, 53, 56].

1.3 Introduction to perovskite oxide-based ferroelectrics

1.3.1 Crystal structure of ferroelectric perovskite oxide

The perovskite oxide family has drawn tremendous interests for studying physics and fabricating devices with better performance. The perovskite materials have the general lattice structure with chemical formula ABO_3, in which A-site cations (usually an alkaline earth or rare earth element) are placed at the corner of the unit cell, a B-site cation (usually a transition metal) is situated at the center of the unit cell and anions (an oxygen element) locate in the face centers [57]. The typical ferroelectric perovskite oxide such as barium titanate ($BaTiO_3$), bismuth ferrite ($BiFeO_3$) and lead titanate ($PbTiO_3$) demonstrate ferroelectric properties, which depend on its perovskite lattice structure. Figure 1.4 presents the tetragonal crystal structure of $BaTiO_3$ at room temperature. The A-site cations are the Ba^{2+} barium ions, and the B-site cation is the Ti^{4+} titanium ion, while the anions are the O^{2-} oxygen ions. Without application of external electric field, as the center of Ti^{4+} cation and O^{2-} anions does not overlap in the unit cell, the spontaneous ferroelectric polarization would occur. With the presence of electric field, the spontaneous electric dipole moments as a result of the Ti-O displacement can be changed from one crystallographic orientation to another, leading to different ferroelectric polarization orientations.

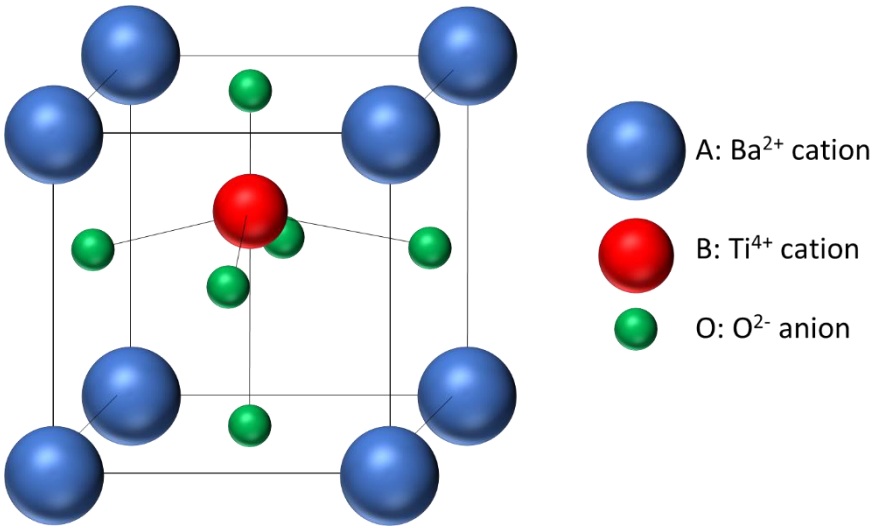


Figure 1. 4 Schematic tetragonal crystal structure of $BaTiO_3$ at room temperature.

1.3.2 Ferroelectricity of perovskite oxide

Ferroelectric materials exhibit ferroelectricity properties as shown in Figure 1.5. With the presence of external electric field, ferroelectric domains start to change the polarization orientations in parallel to that of the electric field. The ferroelectric polarization increases with the increasing electric field. When the electric field is strong enough, all the ferroelectric domains will have the same orientations at the state of saturated polarization (P_s). If an opposite external electric field is applied, the ferroelectric domains will reverse its orientations. In case that the electric field is equal to the coercive field (E_c), the polarization becomes zero. When the electric field increases further, the polarization achieves another maximum with opposite sign. It is noted that unlike dielectric materials, ferroelectric materials can retain nonzero spontaneous polarization, which is defined as remnant polarization (P_r), even in the absence of electric field, making it suitable for memory applications.

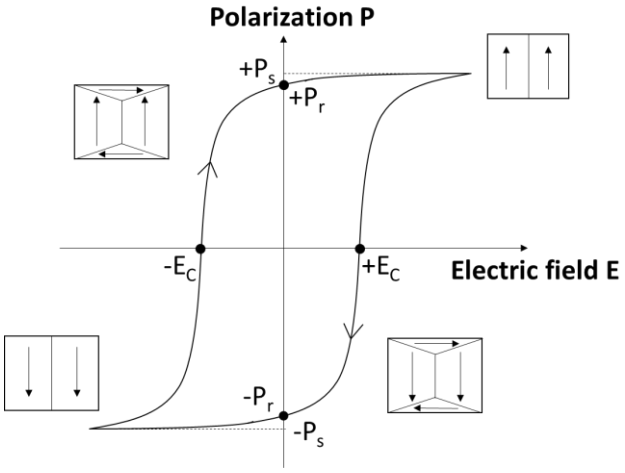


Figure 1. 5 Hysteresis polarization (P)-electric field (E) loop of ferroelectric materials.

It is worth mentioning that ferroelectric materials exhibit temperature-dependent ferroelectricity. Similar to the bulk ferroelectrics, ferroelectric thin films exhibit different phase transition at different temperature. The ferroelectric films show domain structure and spontaneous polarization below the critical temperature, which is termed as Curie temperature (T_c). At this point, the B-site cation has equilibrium state at the center of its octahedral in the unit cell. Below this temperature, cations and anions will move relative to each other, resulting in structure distortion and phase transition. When the temperature is higher than the Curie temperature, the ferroelectric films will easily lose their ferroelectric behavior and transform to a paraelectric (non-ferroelectric) phase. The phase transformation of $BaTiO_3$ is illustrated in Figure 1.6. At higher temperature, $BaTiO_3$ is in cubic lattice structure and transforms to the paraelectric phase with the absence of spontaneous polarization. When temperature is reduced, $BaTiO_3$ changes from tetragonal lattice structure at room temperature to orthorhombic structure and

finally to rhombohedral structure at temperature below 183 K [58]. Hence, the ferroelectricity depends on the crystal structure of ferroelectric materials at different temperature.

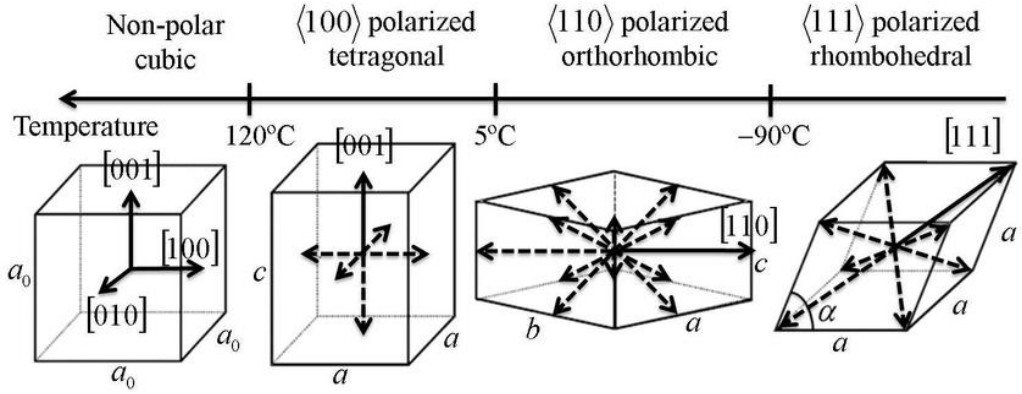


Figure 1. 6 Phase transformation from cubic to rhombohedral lattice in $BaTiO_3$ [58].

In addition to temperature-dependent ferroelectricity, ferroelectric thin films also demonstrate thickness-dependent ferroelectric behaviors. The effect of film thickness on ferroelectricity is directly corelated with induced lattice strain. When a ferroelectric film is thin enough and epitaxially grows on the substrate, the unit cell of the ferroelectric can be distorted tetragonally on the lattice of the substrate, due to the strain generated by the lattice mismatch between the thin film and substrate [59, 60]. Above a certain thickness, the ferroelectric film would not suffer from lattice mismatch as a result of strain gradient, and eventually change to the lattice structure similar to the bulk one. As shown in Figure 1.7, the thickness-dependent ferroelectricity can be observed in multiferroic $BiFeO_3$ thin films grown on (001)-oriented $SrTiO_3$ substrates with $SrRuO_3$ buffer layers [61]. When the thickness of $BiFeO_3$ films increases, both the c/a

ratio of the out-of-plane lattice constant (c) to the in-plane lattice constant (a), and the remnant polarization (P_r) decrease. The experimental results suggest the strain relaxation on the ferroelectric film when the film tends to be bulk at increasing thickness. Therefore, ferroelectricity is related to the lattice strain induced between the substrate and ferroelectric film with different thickness.

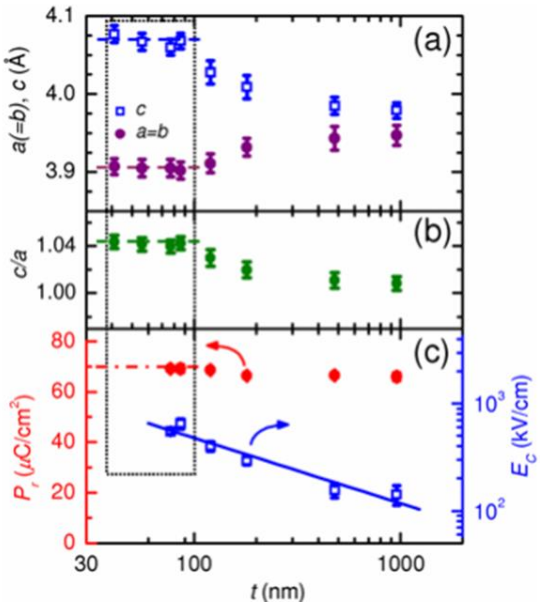


Figure 1. 7 (a) In-plane and out-of-plane lattice parameters, (b) c/a ratio, and (c) P_r and E_c of the $BiFeO_3$ films as a function of thickness [61].

On the other hand, it is interesting to find that ferroelectric thin films exhibit ferroelectricity above a critical thickness. With the use of piezoresponse force microscopy, ferroelectric properties are reported for the $BaTiO_3$ thin films with thickness ranging from 1 to 3 nm grown on (001)-oriented $NdGaO_3$ substrates with $La_{0.67}Sr_{0.33}MnO_3$ (LSMO) buffer layers [62]. It is noted that ferroelectricity can still exist in the highly strained $BaTiO_3$ film down to a thickness of 1 nm. However, the

ferroelectricity of the 1 nm-thick $BaTiO_3$ film is weaker than that of the 3 nm-thick one. The preserved ferroelectricity of nanometer-thick ferroelectric films is important to fabrication of memory devices at nanoscale.

1.4 Ferroelectric tunnel junction

1.4.1 Basic principle of tunnel electroresistance

In recent years, ferroelectric films have been studied extensively for various technological applications. Ferroelectric random-access memories (FeRAM) have already been commercialized in mass production. With the ferroelectric characteristics, FeRAM possess several advantages such as non-volatility [63], high density due to simple device architecture [64], high speed [65] and low power consumption [66]. However, the reading process of information is destructive and a re-write process is also needed after the reading [67, 68]. Hence, there are still restrictions for FeRAM to dominate in the industrial applications.

In 1970s, Esaki *et al.* proposed the idea of ferroelectric tunnel junction (FTJ) [69]. The introduced device relies on the switchable spontaneous polarization in the ferroelectric thin film by external electric field, which adds a new tunability and functionality to memory application. However, the requirement of nanometer-thick ferroelectric films poses a great challenge to fabricating the tunnel junction at that time. With improved thin film deposition and characterization techniques in 2000s,

ferroelectricity is found at ferroelectric films with nanometer thickness [70-72]. The idea of FTJ has again aroused considerable interests for investigating the relation between ferroelectric polarization and resistance switching.

A basic FTJ is composed of two metal electrodes separated by an ultrathin ferroelectric film. According to basic quantum mechanics, a charge carrier can pass through a barrier if the barrier is low and thin enough. It means that the carrier has a finite probability to appear on another side of the barrier [73]. More specifically, the charge carrier can tunnel through the ferroelectric thin film, depending on the ferroelectric barrier height and width in the FTJ.

The tunnel electroresistance of the FTJ is related with the ferroelectric polarization. In 2005, Zhuravlev *et al.* introduced the basic principle of ferroelectric-driven resistance switching behavior [74]. The energy barrier diagrams of the simple metal/ferroelectric/metal FTJ are shown in Figure 1.8. When the ferroelectric polarization happens, polarization charges on the ferroelectric surface will repel or attract electrons near the electrode. Based on Thomas-Fermi theory, the screening length that the electrons screen the polarization charges is a function of the electron density of states at the Fermi level. Therefore, different materials have different screening lengths. The incomplete screening results in additional electrostatic potential at the ferroelectric interface. The larger screening length over the dielectric constant of

the electrode means larger modulation of the electrostatic potential of the ferroelectric barrier.

By ferroelectric polarization reversal, the asymmetry of the electronic potential is changed. The asymmetry between the two ferroelectric/electrode interfaces is important to the current transmittance modulation. For a certain ferroelectric polarization direction after applying an external voltage to the tunnel junction, the barrier height decreases. More charge carriers can pass through the ferroelectric barrier. The junction is set to the ON state with low resistance. The tunnel transmission has exponential dependence on the square root of the average barrier height. At opposite polarization direction, the barrier height increases such that fewer carriers can tunnel through the barrier. The junction is driven into the OFF state with high resistance. Through applying external voltage to the tunnel junction, two spontaneous polarization orientations can be achieved, leading to two distinct resistance states. The tunnel electroresistance (TER) ratio quantifies the efficiency of tunneling electrical resistance in the ON state and the OFF state. The TER formula is shown as follows:

$$\mathrm{TER} = (R_{OFF} - R_{ON})/R_{ON} \tag{1.1}$$

where R_{OFF} and R_{ON} represent resistances in the OFF state and ON state respectively.

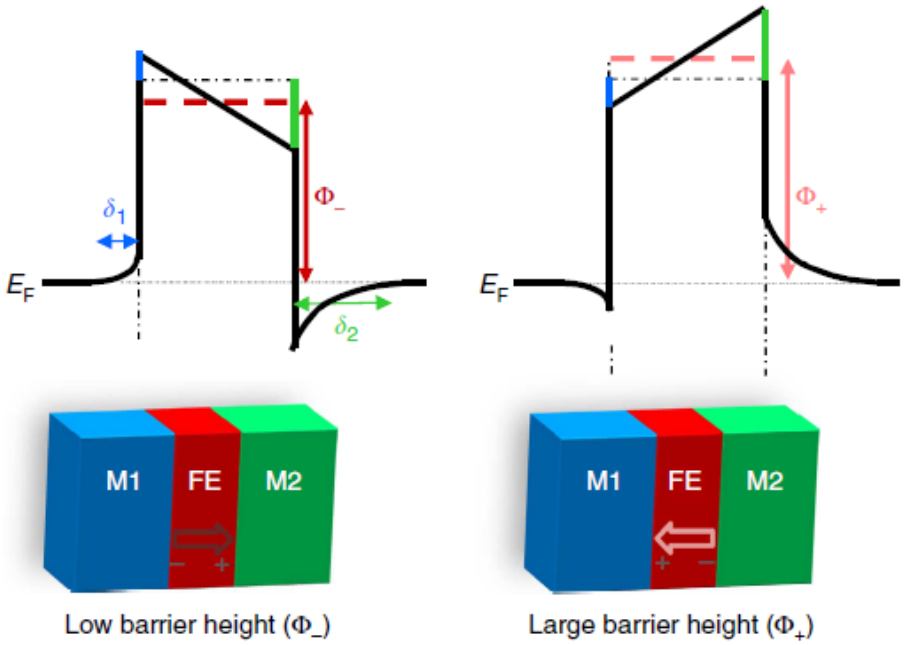


Figure 1. 8 The energy barrier diagrams of the metal 1(M1)/ferroelectric/metal 2(M2) FTJ for two different ferroelectric polarization directions [75].

1.4.2 Transport through ferroelectric barrier

In the simple metal/ferroelectric/metal FTJ, charge carriers can transport across the ultrathin ferroelectric barrier in several possible ways. Direct tunneling is not the only transport mechanism. Pantel and Alexe [76] calculated the influence of polarization charges on the current flowing density and electroresistance effect through ferroelectric barrier for three possible transport mechanisms, including direct tunneling (DT), Fowler-Nordheim tunneling (FNT) and thermionic emission (TE). As indicated in Figure 1.9(a), DT is a quantum-mechanical behavior. By Wentzel–Kramers–Brillouin (WKB) approximation, the carrier flow is assumed in a trapezoidal potential barrier [77]. For FNT, the carriers pass through a triangular potential barrier [78]. FNT

has the same physical behavior as DT, but in different voltage regimes. TE illustrates the carrier flow overcomes the potential barrier by thermal energy [79]. Figure 1.9(b) shows the current density versus voltage curve through a 3.2 nm-thick ferroelectric film for two opposite polarization states. It can be observed that the DT mechanism dominates at low voltage region and FNT is prominent at high voltage region. DT gives parallel current branches for the two opposite polarization states, so the electroresistance effect is rather independent of the applied voltage. In contrast, FNT current increases rapidly as the voltage increases. There is absence of FNT in the low voltage region. For TE, the electroresistacne effect is quite significant with its value defined by the barrier height change upon polarization reversal. TE mechanism is prominent for thicker ferroelectric barrier with reduced current density (Figure 1.9(c)). Figure 1.9(d) summarizes the dependence of electroresistance on voltage bias and ferroelectric barrier thickness in the FTJ. At low voltage, DT can be obtained with a transition to TE when barrier thickness increases. At high voltage, FNT dominants the transport mechanism. Therefore, the transport behavior is affected by the voltage, barrier thickness, polarization direction and the materials used in the simple metal/ferroelectric/metal heterostructure.

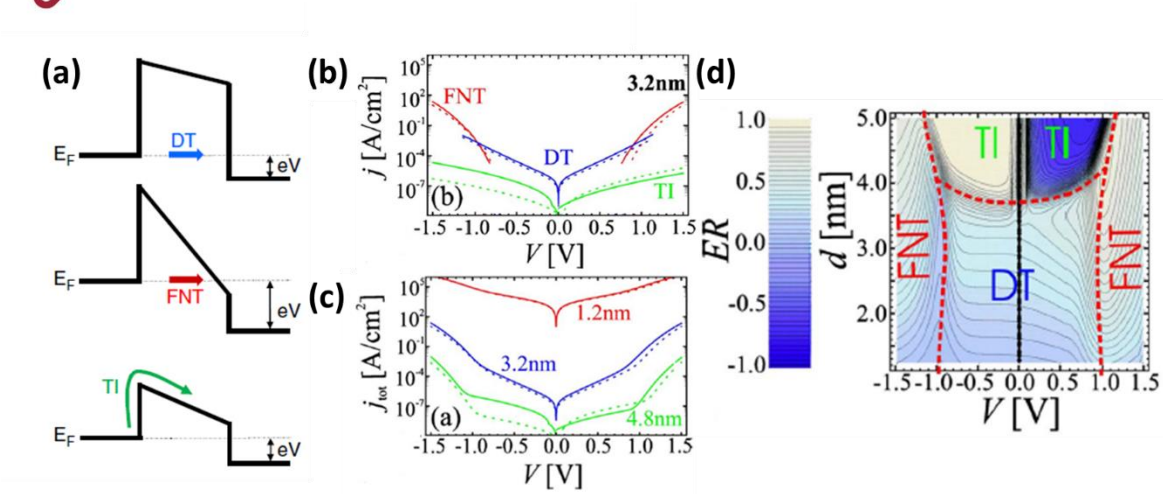


Figure 1. 9 (a) Schematic illustration of DT, FNT and TE transport mechanisms through ultrathin ferroelectric barrier [75]. Current densities versus voltage with different transport mechanisms (b) and ferroelectric barrier thickness (c). The solid and dashed lines represent two different polarization states. (d) Electroresistance as a function of voltage and barrier thickness [76].

1.4.3 Ferroelectric polarization control of resistive switching

Recently, the correlation between resistance switching and ferroelectric polarization has been demonstrated in FTJs [80-85]. By using resistance maps of conductive atomic force microscopy (C-AFM) and ferroelectric domain images of piezoresponse force microscopy (PFM), Garcia *et al*. found that the resistance variation corresponds to different ferroelectric polarization orientations in the positively and negatively poled domains in the highly strained 1 nm-thick $BaTiO_3$ films [62]. By employing the similar methods, Gruverman *et al*. reported ferroelectric-induced resistance switching in the 2 nm-thick $BaTiO_3$ films grown on (001)-oriented $SrTiO_3$

substrates with $SrRuO_3$ buffer layers [81]. The typical current-voltage (*I-V*) characteristics exhibit two distinct and stable resistance states, indicating the occurrence of ferroelectric polarization reversal. In addition to using conductive probe as top electrode in C-AFM, Chanthbouala *et al*. demonstrated the resistive switching in the Au/Co/(2 nm) $BaTiO_3$/LSMO/$NdGaO_3$ heterostructure [85]. Figures 1.10(a) and (b) show the local PFM phase and amplitude versus voltage hysteresis loops, suggesting the stable and switchable polarization in the ultrathin $BaTiO_3$ films. The remnant resistance versus voltage (Figure 1.10(c)) is varied hysteretically with the coercivity of the PFM signals, further confirming the correlation between resistive switching and ferroelectricity of the $BaTiO_3$ films. A giant TER effect of 10,000% can be achieved in the FTJ. Different techniques can be employed to characterize the ferroelectric control of resistance switching.

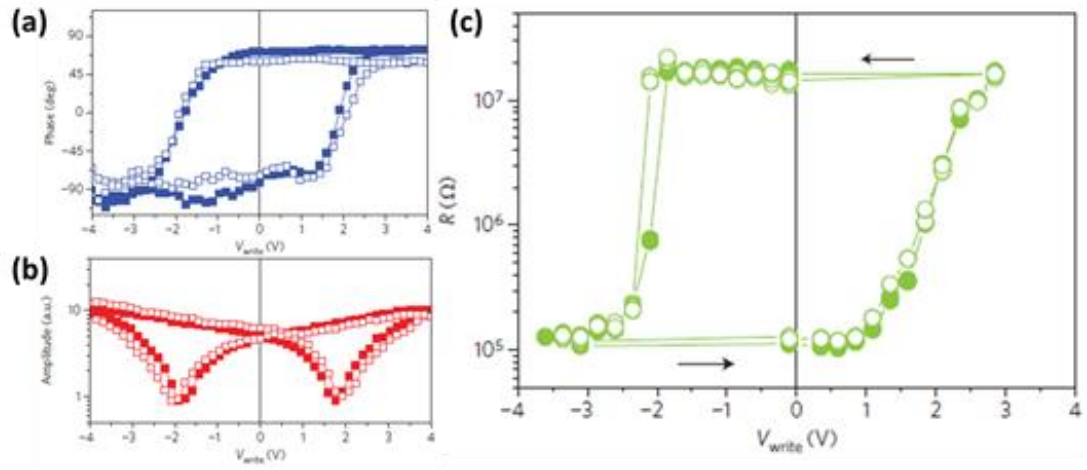


Figure 1. 10 Out-of-plane PFM phase (a) and amplitude (b) loops of the Au/Co/$BaTiO_3$/LSMO/$NdGaO_3$. (c) Resistance versus voltage of the device [85].

1.4.4 Polarization modulation of the electronic states of the electrode

Since the tunneling current is highly sensitive to the electronic properties of the ferroelectric/electrode interface in the FTJs, the electrode materials can be particularly selected to modulate the electronic properties by ferroelectric field effect. It is predicted that an extra barrier placed at the interface between the ferroelectric and electrode can enhance the electroresistance effect with modulating the electrostatic potential induced by polarization reversal [86, 87]. Based on this idea, Wen *et al*. proposed a novel tunneling heterostructure by replacing one of the metal electrodes in the conventional FTJ with a heavily doped semiconductor [88]. In the conventional metal/ferroelectric/metal FTJ, the electroresistance is mainly attributed to the ferroelectric modulation of barrier height. In the metal/ferroelectric/semiconductor FTJ, a greatly enhanced electroresistance is expected when the barrier width can be modulated along with the barrier height. The resistance switching principle of the metal/ferroelectric/semiconductor heterostructure is schematically illustrated in Figures 1.11(a) and (b). When the ferroelectric polarization points towards the semiconductor, positive bound charges in the ferroelectric/semiconductor interface will attract electrons and drive the n-type semiconductor surface into accumulation state [89, 90]. The accumulated semiconductor behaves like a metal. Due to incomplete screening, a depolarization field develops in the ferroelectric barrier to oppose the polarization

[74]. This depolarization field reduces the barrier height and increases the charge tunneling transmittance [91]. More charges can tunnel through the ferroelectric barrier. The device is set to the ON state with low resistance. When the ferroelectric polarization points away from the semiconductor, negative ferroelectric bound charges will repel the electrons and set the semiconductor into depletion state. The incomplete screening generates a depolarization field to increase the barrier height. Also, the immobile screening charges form a space charge region in the depleted semiconductor. The charges need to pass through an additional barrier in the space charge region. The tunneling transmittance is significantly decreased and fewer charges can tunnel through the ferroelectric barrier. The device is set to the OFF state with high resistance. As revealed in Figure 1.11(c), the resistance switching of the metal/ferroelectric/semiconductor heterostructure according to above mechanism exhibits two distinct resistance states. Moreover, the electroresistance effect can be further optimized by tuning the doping concentration in the semiconductor due to widening of space charge region in the ferroelectric/semiconductor interface, as shown in Figure 1.11(d). Therefore, the use of semiconductor as one of the electrodes can give rise to enhanced electroresistance effect in the FTJs.

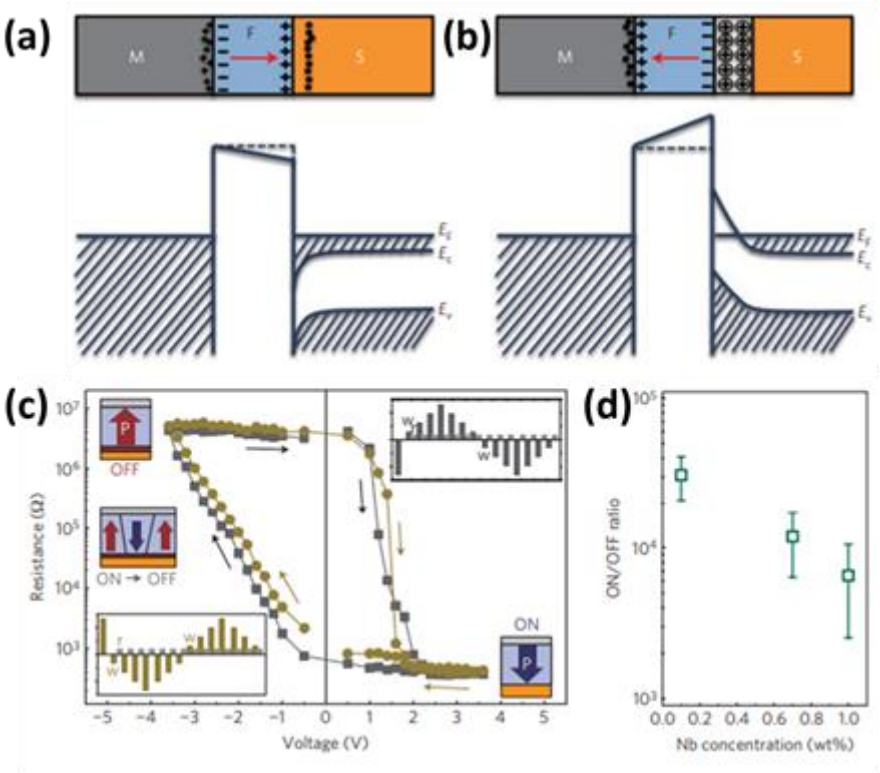


Figure 1. 11 Schematic illustration of resistive switching mechanism of the metal/ferroelectric/semiconductor heterostructure and corresponding potential energy profiles for the low resistance state (a) and high resistance state (b). (c) Room-temperature resistance hysteresis loops. (d) ON/OFF ratio as a function of Nb doping in the semiconductor electrode [88].

Later, Yin *et al*. reported a metal/insulator phase transition at the interface between the ferroelectric and electrode to improve the electroresistance effect of FTJs [92]. It is predicted that the manganite material $La_xCa_{1-x}MnO_3$ (LCMO) can undergo a phase transition between a metallic phase and an insulator phase in response to ferroelectric polarization [93]. In the experiment, an ultrathin magnetic complex oxide $La_{0.5}Ca_{0.5}MnO_3$ layer was inserted into the LSMO/(0.8 nm) LCMO/(3 nm)

$BaTiO_3$/LSMO tunnel junctions. As shown in Figure 1.12(a), when the polarization points towards the LCMO layer, electron accumulation induced to screen the polarization charges pushes the doping level of LCMO towards ferromagnetic metallic phase (for $x < 0.5$). When the polarization points away from the LCMO layer, hole accumulation of LCMO results in anti-ferromagnetic insulating phase (for $x > 0.5$). The resistance switching characteristics of the LSMO/LCMO/$BaTiO_3$/LSMO heterostructure shows an enhanced TER ratio of 5000 % (Figure 1.12(b)), which is two orders of magnitude larger than the LSMO/$BaTiO_3$/LSMO heterostructure (Figure 1.12(c)). Therefore, the ferroelectric-driven metal/insulator phase transition in the interfacial layer can increase the resistance switching effect.

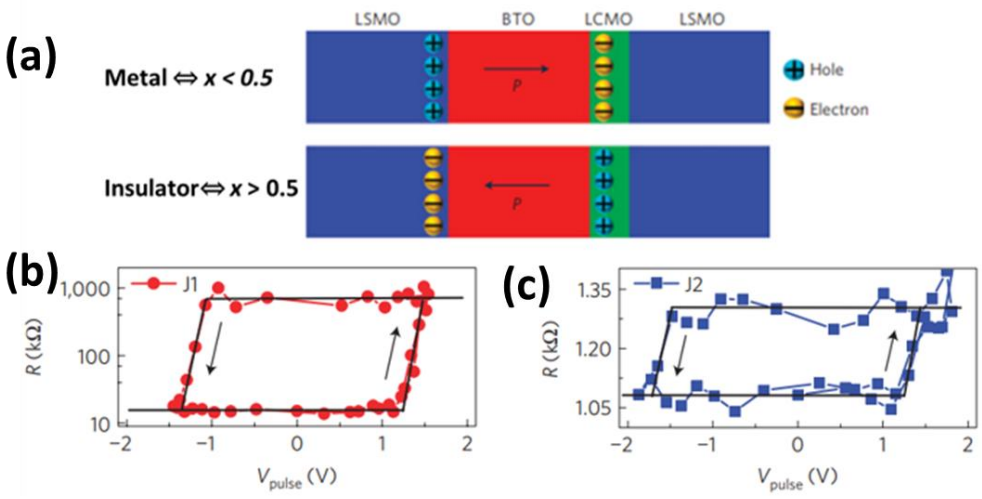


Figure 1. 12 (a) Schematic demonstration of the screening charge accumulation in the LSMO and LCMO electrodes for opposite ferroelectric polarization orientations in the $BaTiO_3$ layer. Resistance hysteresis loops of LSMO/LCMO/$BaTiO_3$/LSMO (b) and LSMO/$BaTiO_3$/LSMO heterostructure (c) [92].

On the other hand, Lu *et al*. demonstrated the use of graphene, a two-dimensional material, as one of the electrodes in FTJs to modulate the interface properties for enhanced device performance [94]. In the experiment, the introduction of ammonia species (NH_3) into the graphene/ferroelectric interface could enhance the polarization stability and electroresistance effect in the $BaTiO_3$-based tunnel junction. Due to good impermeability with gas or liquid, graphene could be used to trap and stabilize molecular layers on the interface [95-97]. There is a considerable number of available molecules possessing a wide range of parameters including size, shape, dipole moment and so on. Hence, interface engineering can be realized by introducing molecules with certain characteristics at the interface between the ferroelectric and electrode. The ease of graphene transfer on any surface opens a possibility of using it as ultrathin electrodes in FTJs.

1.5 Significance of research

Due to its unique 2D structure and remarkable properties, graphene has been considered as a promising candidate for potential applications in many aspects. Graphene can be integrated with different functional materials to form novel heterostructure with unique characteristics [98, 99]. In particular, the coupling of graphene with ferroelectric materials has attracted enormous interests in novel electronic devices. Ferroelectric materials exhibit an electrically switchable

spontaneous polarization, allowing a possibility of electrical modulation of the functional properties of the graphene/ferroelectric hybrid structure, which are attractive for memory and logic applications. However, many previous studies were focused on modulation of the in-plane transport of graphene in the ferroelectric field-effect transistors [100-104]. There is limited research on the perpendicular-to-plane transport of graphene in the devices [94]. Therefore, it is significant to study the interesting characteristics of the vertical graphene/ferroelectric hybrid structure.

2D graphene has been widely used as electrodes in electronic and optoelectronic applications. Graphene nanosheets exhibit the great advantages of atomic level thickness and optical transparency properties, and also reveal the merits of high carrier mobility, high thermal conductivity, and high mechanical strength [20]. 2D graphene can be used as a top electrode in the $BaTiO_3$ tunnel junction to study the effect of ferroelectric polarization on its electronic and transport properties. With the semiconducting $Nb:SrTiO_3$ electrode, the polarization-induced modulation of the Schottky barrier at the $BaTiO_3/Nb:SrTiO_3$ interface could further enhance the electroresistance effect of the graphene-based FTJ.

On the other hand, VGHFET using ferroelectric thin film as a tunnel barrier can be developed. Unlike conventional tunnel junctions, the tunneling barrier profile of ferroelectric thin film in the FTJ can be altered by spontaneous polarization [105]. By

replacing the conventional tunnel barrier of insulator or semiconductor with ultrathin ferroelectric film, the novel vertical graphene-based FET can be implemented with the characteristics of both FTJ and VGHFET. The coupling of VGHFET with FTJ could bring additional functionality and tunability to the vertical graphene-based heterostructure, which provides a pathway to develop electronic devices with interesting behaviors.

1.6 Structure of thesis

The chapters of this thesis are organized as follows:

Chapter 1: Introduction. In this chapter, the unique structure and fascinating properties of graphene are first introduced. Then, the device structure and research status of VGHFETs are described. Following that, the crystal structure and ferroelectric behavior of perovskite oxides are illustrated. The device geometry, basic principle and recent progress of perovskite-based FTJs are discussed. Then, the motivation and objectives of this thesis are presented.

Chapter 2: Experimental techniques. This chapter introduces the important experimental techniques, which are employed in this research, including the preparation and transfer methods of graphene nanosheets, the pulsed-laser deposition of perovskite oxides, the structural characterization techniques, as well as the electrical measurement systems.

Chapter 3: Structural and electrical characterization of graphene-based ferroelectric tunnel junction. This chapter demonstrates the fabrication method, the structure characterization, as well as the electrical measurement of the graphene/$BaTiO_3$/Nb:$SrTiO_3$ heterostructure. The effects of Nb doping concentration in the Nb:$SrTiO_3$ substrates on the electrical properties of the devices are studied.

Chapter 4: Fabrication and characterization of vertical graphene-based tunneling transistor. This chapter explores the fabrication process, and the structural and electrical measurement of the Au/Sm:$BiFeO_3$/graphene/SiO_2/Si, Au/Al_2O_3/graphene/$BaTiO_3$/Nb:$SrTiO_3$, as well as Au/Al_2O_3/graphene/$BaTiO_3$/ $La_{0.7}Sr_{0.3}MnO_3$/$SrTiO_3$ heterostructure.

Chapter 5: Conclusion and future prospect. In this chapter, the results in this thesis are summarized. Meanwhile, future prospect of vertical graphene-based tunneling heterostructure with ultrathin ferroelectric tunnel barrier is presented.

Chapter 2 Experimental Techniques

This chapter will introduce the important experimental techniques employed in the research. Graphene nanosheets were prepared and transferred. Perovskite oxide ferroelectric films were deposited by pulsed laser deposition (PLD). The crystal structure was characterized by X-ray diffraction (XRD) and Raman spectroscopy. The chemical composition was studied by X-ray photoelectron spectroscopy (XPS). The surface morphology and ferroelectricity property were characterized by piezoresponse force microscopy (PFM). The electrical properties were measured by semiconductor analyzer equipped with probe station.

2.1 Sample preparation

2.1.1 Preparation and transfer process of CVD-grown graphene

There are several widely-used methods to produce graphene sheets, such as mechanical exfoliation [6], Si desorption from SiC single crystal [106], chemical exfoliation [107, 108], chemical reduction of graphene oxide to functionalized graphene single layer [109] and so on. The first graphene sheet was obtained from pyrolytic graphite by mechanical exfoliation with the use of a Scotch tape. The exfoliated graphene exhibits superior properties but the size of the exfoliated graphene is on microscale. Hence, it is difficult to obtain wafer-scale graphene sheets by

mechanical exfoliation. Several alternative ways have been adopted to grow large-area graphene, including epitaxial growth and chemical vapor deposition (CVD). Large-area graphene sheets can be grown on metal surfaces such as Ni and Cu by CVD method [110, 111]. CVD-grown graphene typically has the polycrystalline structure with domain boundaries and surface wrinkles. Yet, CVD-grown graphene can be easily transferred onto any target substrate after removing the underlying metal foils. The ease of graphene transfer allows the CVD-grown graphene to be used extensively in integrated devices.

In our experiment, a general technique is to transfer CVD-grown graphene sheets onto desired substrates. As shown in Figure 2.1, the process of graphene transfer includes the following steps: (1) Spin coating. A thin layer of poly(methyl methacrylate) (PMMA) is spin-coated on top of the graphene grown on copper foil surface. As graphene grows on both sides of the copper, graphene will be used on one side where PMMA layer is spin-coated. The PMMA layer can provide mechanical support to the graphene during transfer. (2) Copper etching. The PMMA/graphene/copper sheet is baked for 10 mins at 110 °C to enhance the adhesion between the PMMA and graphene. The sample is then placed into ammonium persulfate (APS) to etch away the underlying copper. It takes around 12 hours to completely dissolve the copper foil. After that, the floating membrane of PMMA/graphene is rinsed on the deionized water (DI) surface.

(3) Graphene transferring. The PMMA/graphene membrane is transferred onto the target substrate. (4) PMMA removal. After drying for better adhesion between the graphene and substrate, the PMMA coating can be removed with acetone. Finally, a graphene layer is left on the substrate sample.

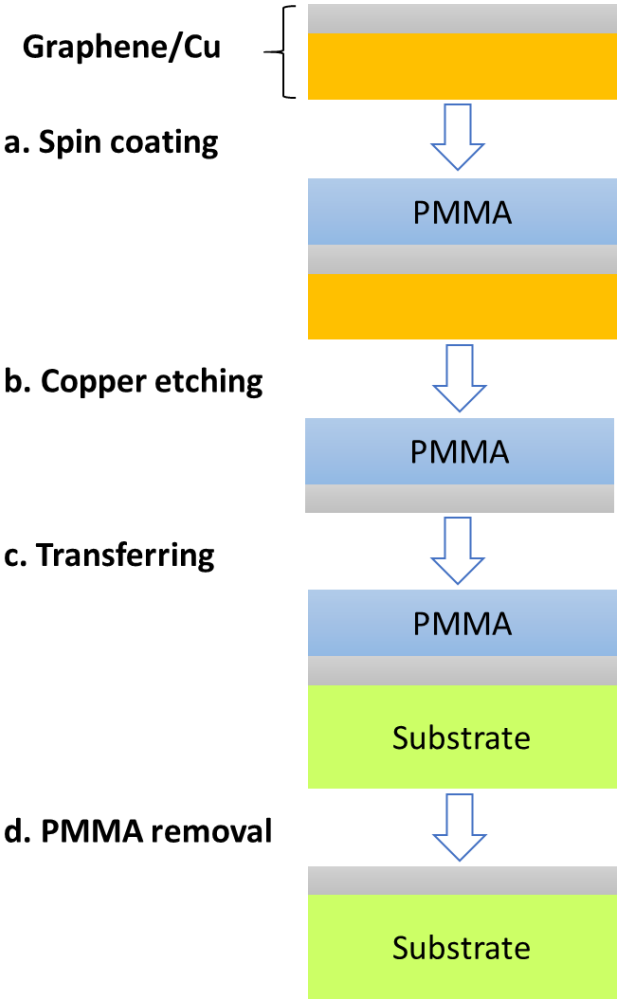


Figure 2. 1 A typical method to transfer graphene onto target substrate. (a) PMMA-coated graphene on copper foils. (b) Floating PMMA/graphene membrane after etching copper. (c) Transfer of PMMA/graphene onto substrate. (d) Graphene left on the substrate after removing PMMA layer.

2.1.2 Fabrication of perovskite oxide by pulsed-laser deposition

Pulsed laser deposition (PLD) is widely used as an efficient and reproductive thin film deposition technique [112, 113]. PLD is a kind of physical vapor technique for fabricating high-quality thin films. As shown in Figure 2.2, the typical PLD system consists of three main components: vacuum system, deposition chamber and laser system. The basic working principle of the PLD involves the interaction of the laser and the target material in high vacuum environment. During the deposition process, a pulsed laser beam is focused on the surface of the target material. When the laser energy is high enough, the material will create a plasma plume, which includes atoms, molecules, ions and clusters. The substrate is placed in front of the target material. The released particles will re-crystalline on the substrate surface as a thin film. The quality of the PLD-growth thin film is controlled by a series of parameters such as laser energy, base vacuum pressure of the chamber, substrate temperature, oxygen growth pressure and the distance between the target and substrate. The film thickness can be controlled accurately by the total numbers of laser pulses during deposition. In our experiment, a KrF excimer laser is employed with a wavelength of 248 nm and pulse duration of 25 ns. In order to guide the laser light into the chamber, light path should be adjusted precisely. The chamber is pumped with a turbo pump and rotary pump to achieve high vacuum environment (~10^{-4} Pa). The substrate holder can be heated to an elevated

temperature (~750 ºC) for thin film deposition.

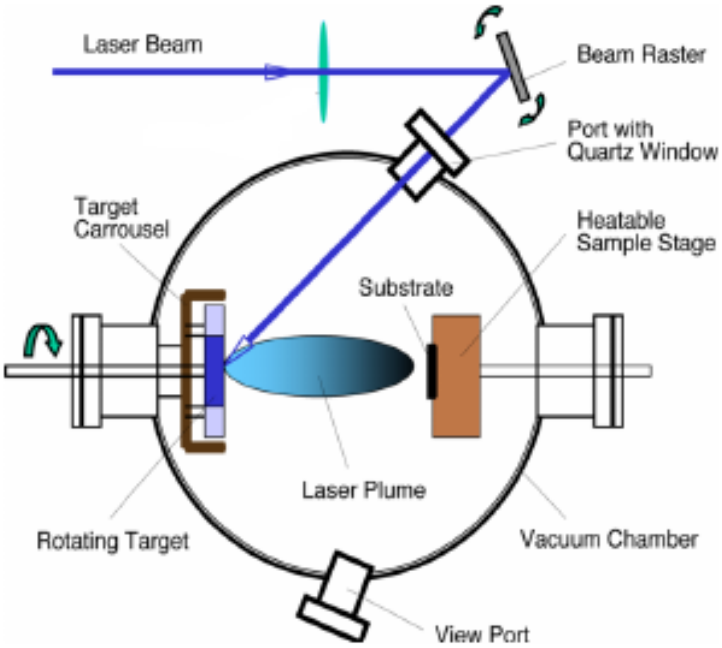


Figure 2. 2 Schematic illustration of the PLD system.

2.2 Structural characterization

2.2.1 X-ray diffraction

X-ray diffraction (XRD) is a non-destructive method to study the crystal structure of materials. Figure 2.3 shows the basic geometry of XRD. When a parallel monochromatic X-ray beam is incident on the sample surface, part of the beams will be scattered by the crystalline lattice planes of the sample, which will interfere with each other and produce a diffraction maximum. This may happen in the condition that the path difference between the scattered beams is equal to an integral number (n) of the wavelength. The relationship can be expressed in Bragg's law:

$$2d_{hkl}sin\theta = n\lambda \quad (2.1)$$

where h, k, l are the Miller indices, d_{hkl} the distance between the parallel lattice planes ($h\,k\,l$), θ the incident angle, and λ the wavelength of X-ray beam. Based on the measured diffraction pattern, the crystal structure of the sample can be analyzed by comparing with standard diffraction pattern. The distance between the lattice planes and the crystal orientation can also be determined. In our experiment, high resolution X-ray diffractometer (Rigaku, SmartLab) is employed to investigate the lattice structure of different materials.

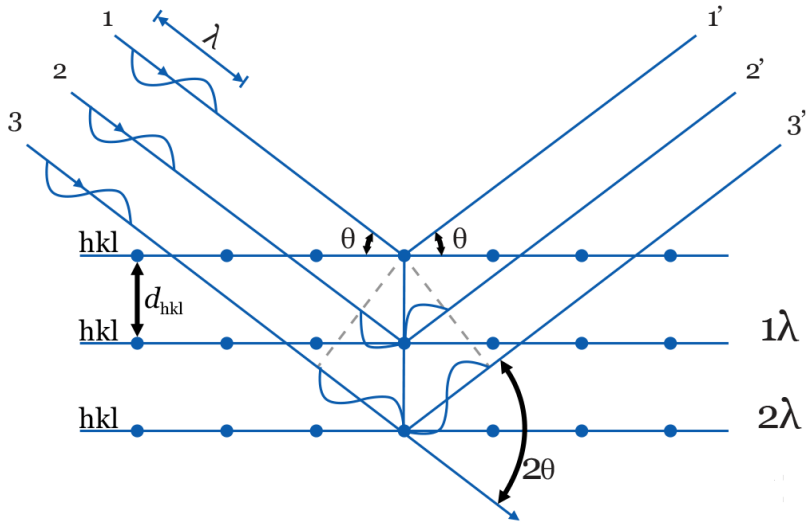


Figure 2. 3 Schematic of the working principle of XRD.

2.2.2 Raman spectroscopy

Raman spectroscopy is a powerful tool for chemical identification and molecular structure analysis. The basic principle of the Raman spectroscopy is shown in Figure 2.4. When light illuminates the target material, both Rayleigh scattering and Raman scattering can be observed. Rayleigh scattering is a kind of elastic scattering. After

absorbing the energy of the incident photon, the molecules of the material can jump from the energy ground states to the virtual energy states, and then return to its ground states. During the transition, another photon is released with the same energy as the incident photon. On the other hand, Raman scattering belongs to inelastic scattering. After absorbing the incident photon, the molecules can jump to the virtual energy states but drop to the energy states lower than or higher than the initial ground states. The energy of the released photon is different from the incident photon. For Stokes Raman scattering, the released photon has lower energy than the incident photon. For anti-Stokes Raman scattering, the released photon has higher energy than the incident photon. Among these scattering modes, Rayleigh scattering has the highest probability to take place. Stokes Raman scattering has a higher occurrence chance than anti-Stokes Raman scattering. Therefore, Raman measurement is usually accorded to the Stokes Raman scattering. As the energy transferring to or from the photons is associated with specific phonon vibration, different materials have distinct frequency shifts of the scattering light, which can be measured to identify the materials. In our experiment, the Raman spectra are acquired by high resolution Raman system (Horiba, LabRAM HR 800). A blue laser beam with 488 nm wavelength is employed as the source of incident photons for Raman measurement.

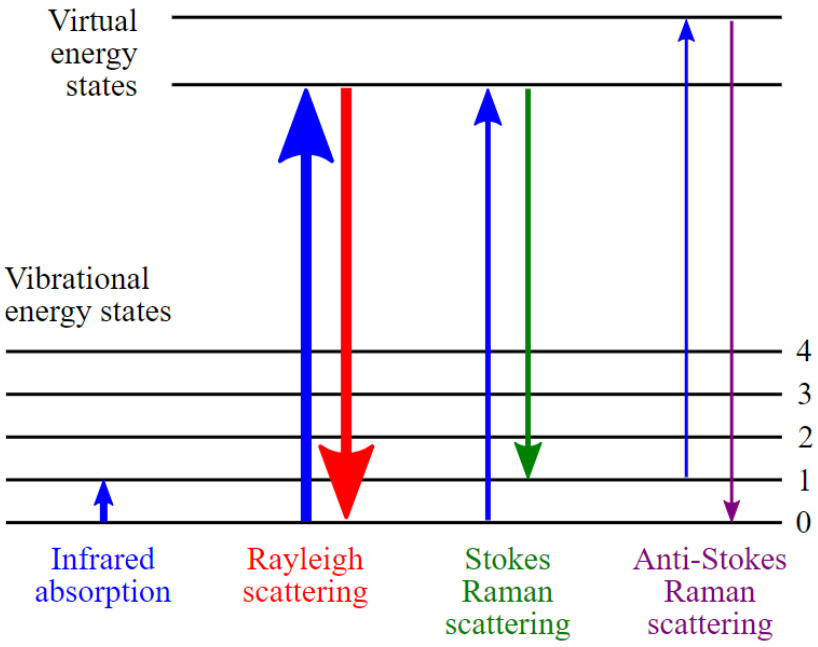


Figure 2. 4 Basic mechanism of Rayleigh scattering, Stokes Raman scattering and anti-Stokes Raman scattering.

2.2.3 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) can be used to characterize the chemical compositions and the valence states of elements in the sample. As shown in Figure 2.5, when a sample surface is irradiated with X-ray beam, the interaction between an X-ray photon and a core level electron of an atom can transfer the energy of the photon to the electron. If the photon energy is large enough, the electron can escape from the surface of the sample. This is called photoemission process. The binding energy (E_b) of an electron at an electronic level is given by:

$$E_b = h\nu - E_k - \varphi \qquad (2.2)$$

where $h\nu$ is the incident photon energy, E_k the kinetic energy of the emitted electron and

φ the work function of the sample. As each element possesses a unique binding energy, XPS spectrum can be used to identify the elemental compositions and the chemical states of the sample.

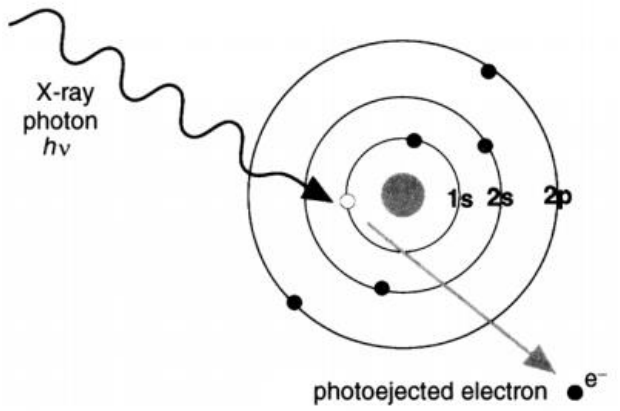


Figure 2. 5 Working principle of photoemission process.

2.2.4 Piezoresponse force microscopy

Piezoresponse force microscopy (PFM) is a powerful analytical technique to characterize the ferroelectric domain configuration and local switching property of ferroelectric thin films. The PFM imaging setup is shown in Figure 2.6. A conductive probe is in contact with and is moveable to scan over the sample surface. An ac voltage, $V_{ac}cos\omega t$, can be applied either through the conductive probe or the bottom electrode to provide an electric field on the sample. As a result of the converse piezoelectric effect, the sample will oscillate and deform locally with the same frequency ω as the ac field applied.

By converting the optical signal measured from the probe deflection into the electrical signal via the photodiode, the deformation signal which is proportional to

local polarization can be obtained. The local deformation signal, $Acos(\omega t+\varphi)$, and the reference signal, $V_{ac}cos\omega t$, will be mixed in the lock-in amplifier. After processing in the low-pass filters, the output signal becomes a dc component $(V_{ac}Acos\varphi)/2$, where φ is the phase angle of electromechanical response or polarization direction, and A is the local electromechanical response of the sample. By imaging φ and A over an area, the domain images of the sample can be acquired.

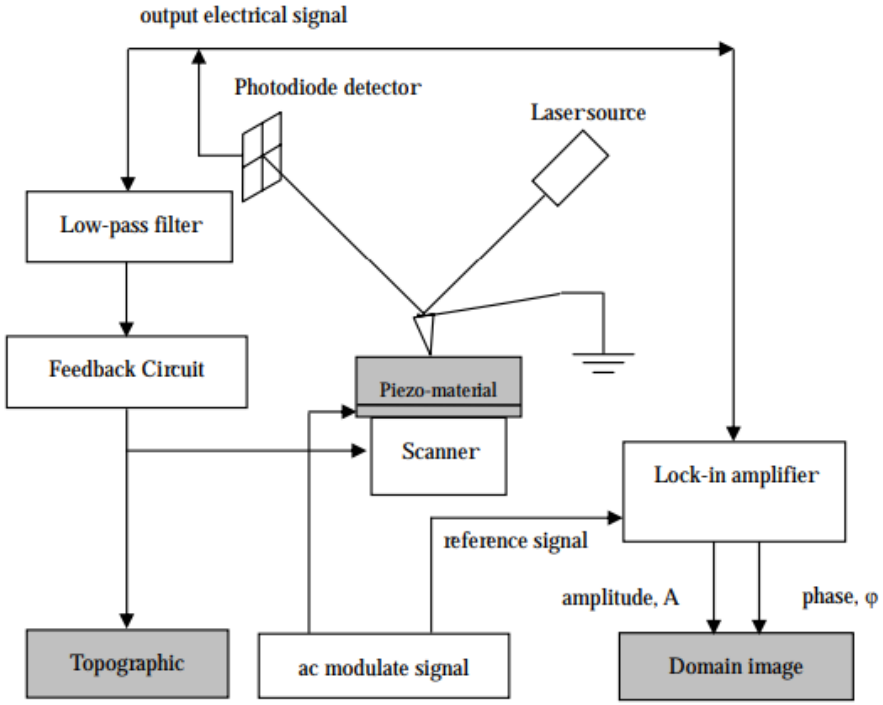


Figure 2. 6 Schematic of the setup of piezoresponse force microscopy.

With the use of the imaging system, the out-of-plane and in-plane polarization features of the sample can be measured. When an electric field perpendicular to the sample is applied, the out-of-plane domains will deform along the field direction. However, the in-plane domains will cause tilted surface. Since the PFM probe moves in contact with the sample surface, the vertical deformation of the out-of-plane domains

is detected by the deflection of the cantilever and the shear deformation of the in-plane domains is measured by the twisting of the cantilever. The detected signals will be collected for PFM measurement.

2.2.5 Electrical property measurement of devices

In our experiment, measurement of electrical properties of devices is performed with the probe station system. As shown in Figure 2.7, the main electrical characterization system includes the probe station, semiconductor parameter analyzer, CCTV camera and LCD monitor. In the probe station, tungsten tips are used to contact device electrodes for connecting the measurement system. The probe configurations are determined by the device geometry. For ferroelectric tunnel junctions, there are two electrodes needed for the top and bottom electrodes. For field-effect transistors, there are three electrodes for the drain, source and gate electrodes connected to the measurement system. In addition, the semiconductor parameter analyzer (Keithley 4200-SCS) is designed for providing voltage source and measuring current response in the devices. The current resolution of the parameter analyzer is in the order of femto ampere, which can give high accuracy and sensitivity of electrical measurement. Moreover, the CCTV camera and LCD monitor are installed in the probe station system. With the CCTV camera used for microscopy function, micro-scale patterns of the devices can be clearly identified through the LCD display. In the experiment, all the

electrical characterization of the devices is performed in air ambient at room temperature.

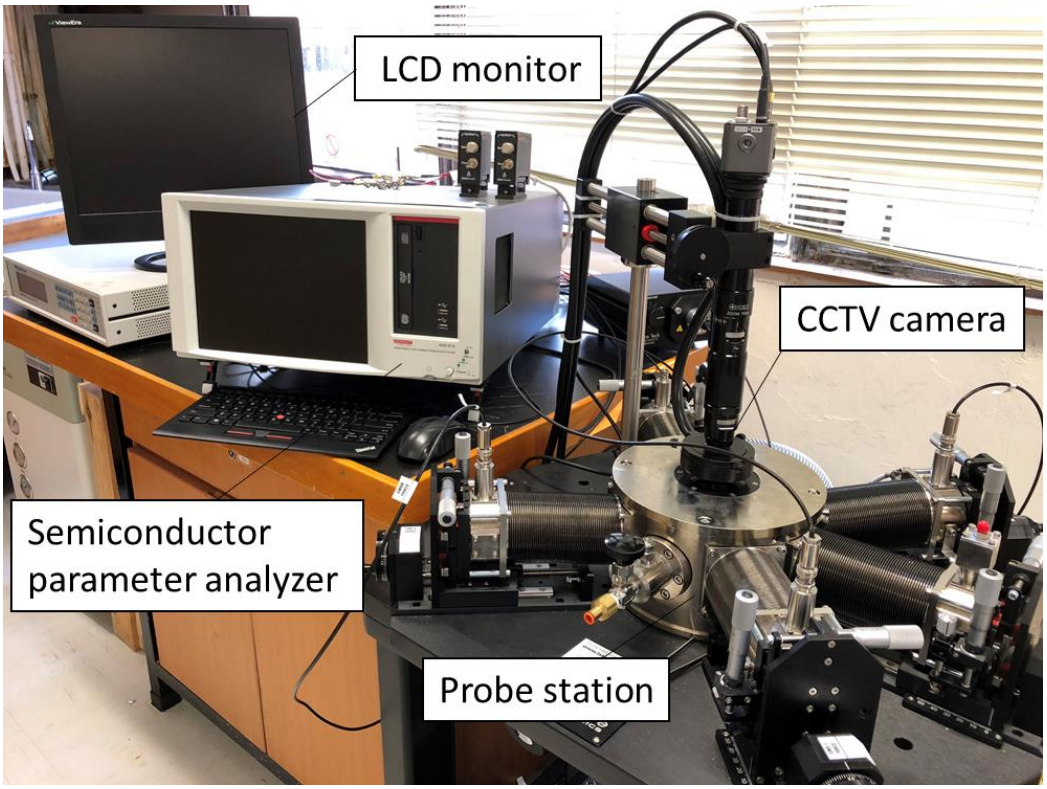


Figure 2. 7 Photograph of the electrical measurement setup in our laboratory.

Chapter 3 Structural and Electrical Characterization of Graphene-Based Ferroelectric Tunnel Junction

3.1 Introduction

Ferroelectric tunnel junctions (FTJs) have received extensive attention for non-volatile memory application with non-destructive resistive readout, high data storage density and simple device architecture [114, 115]. FTJs are composed of an ultrathin ferroelectric film sandwiched between two electrodes [92, 116]. The concept of FTJs was formulated by Esaki *et al*. in 1970s [69]. With rapid technological development in the epitaxial growth of perovskite oxide films, ferroelectricity is observed to exist in films with a few nanometers in thickness [70, 117, 118]. This result makes it possible to realize FTJs by using ultrathin ferroelectrics as tunnel barrier. The overall effective barrier of an FTJ can be modulated by polarization reversal in the ferroelectric barrier, which gives rise to the switching of the resistance between a high (OFF state) value and a low (ON state) value. The effect is known as tunneling electroresistace (TER) [62, 119]. The TER effect has been demonstrated in various FTJs employing metal electrodes, such as Pt/$BaTiO_3$(BTO)/$SrRuO_3$ [120], Cr/BTO/Pt [121], Co/Pb(Zr,Ti)O_3/($La_{0.70}Sr_{0.30}$)MnO_3 [122], as well as ($La_{0.67}Sr_{0.33}$)MnO_3/$BiFeO_3$/

$(La_{0.67}Sr_{0.33})MnO_3$ [123], where the ON/OFF conductance ratio is attributed to the ferroelectric modulation of barrier height. According to basic quantum mechanics, the tunneling transmission of electrons passing through the ferroelectric barrier is exponentially dependent on the barrier width, in addition to the barrier height. The TER is expected to be increased when the barrier width can be further modulated [74, 86]. Recently, FTJs using the semiconductor electrode, $Nb:SrTiO_3$ (NSTO), have been reported in Pt/BTO/NSTO [88]. A giant TER has been observed due to the barrier width modulation. In response to polarization reversal in the ferroelectric film, enhancement or suppression of an extra tunnel barrier in the depleted region occurs as a result of the depletion or accumulation state of the semiconducting electrode. Therefore, the use of a semiconductor electrode is an efficient approach to tune the transport properties of the junction device.

On the other hand, it is well known that graphene, a zero-bandgap two-dimensional material, exhibits various outstanding properties, such as high carrier mobility, thermal conductivity, mechanical strength and impermeability with gas and liquid [23, 124]. Graphene is widely used as single-atom-thick and transparent electrodes for electronic and optoelectronic devices [125]. However, there has been limited study on the device design using both graphene electrode and semiconductor electrode. Our recent study implies that high performance can be achieved in a

graphene-based field-effect transistor based on Au/$BiFeO_3$/graphene on an oxidized Si by tuning transport properties of the multilayer structure [126]. Therefore, it is expected that employment of semiconducting electrodes may further manipulate the resistance switching of the graphene-based FTJs.

In this chapter, we report a novel FTJ employing both two-dimensional material and semiconductor electrode in graphene/BTO/NSTO heterostructure. The TER behavior of the graphene-based heterostructure is studied. The ON/OFF conductance ratio is found to increase with decreasing Nb doping concentration from 1.0 wt% to 0.1 wt% on the semiconductor electrode. An optimized ON/OFF ratio up to 10^3 is obtained in the device when introducing Nb concentration of 0.1 wt% at room temperature. The observations show the ferroelectric-driven barrier tunability in terms of both height and width on the semiconductor interface for TER enhancement. Furthermore, good retention property and switching reproducibility can be observed in the device, which is helpful for developing non-volatile graphene-based memory at nanoscale.

3.2 Experimental

3.2.1 Thin film deposition by PLD

PLD has proved to be a conventional technique in depositing high-quality titanate thin films. Here, 3 nm-thick BTO thin films were grown on (001)-oriented NSTO single crystal substrates by PLD method. The PLD growth conditions of BTO thin films are

summarized in Table 3.1. The NSTO substrates with different Nb doping concentration of 0.1 wt%, 0.7 wt% and 1.0 wt% were used. The NSTO substrates were sonicated sequentially with acetone, ethanol and DI water for 20 minutes each to remove the impurities on the substrate surface. High-purity stoichiometric BTO ceramic (99.99%) was employed as target materials. Prior to the deposition, the chamber was evacuated to a base pressure of 10^{-4} Pa. The substrates were placed in parallel to the target at a distance of 5 cm. During deposition, a KrF excimer laser was focused on the target with the wavelength of 248 nm, fluence of 250 mJ and repetition rate of 1 Hz. The target was rotated to reduce non-uniform erosion. The BTO films were grown at deposition temperature of 700 °C under oxygen pressure of 10 Pa. The estimated growth rate is around 0.1 Å/pulse, which depends on the crystalline of the target materials, distance between the target and substrates, substrate temperature, oxygen pressure, laser energy and so on. The film thickness can be accurately controlled by the laser pulse repetition rate and the total growth time. After deposition, the thin films were cooled down naturally to room temperature.

Table 3. 1 PLD deposition conditions for BTO thin film on NSTO substrate.

Target	BTO ceramic
Laser wavelength	248 nm
Laser energy	250 mJ
Deposition frequency	1 Hz
Target-substrate distance	5 cm
Base pressure	10^{-4} Pa
Substrate temperature	700 °C
Growth pressure	10 Pa
Growth rate	0.1 Å/pulse

3.2.2 Fabrication of graphene/$BaTiO_3$/Nb:$SrTiO_3$ heterostructure

The device geometry of the graphene/BTO/NSTO heterostructure and the fabrication process are illustrated schematically in Figure 3.1. The BTO thin films were grown on (001)-oriented NSTO single crystal substrates by PLD technique. The commercially obtained NSTO substrates have the Nb doping concentration ranging from 0.1 to 1.0 wt%. The purchased CVD-grown graphene/copper sheets were spin-coated with poly (methyl methacrylate) (PMMA), cut into small pieces and put into ammonium persulfate solution (APS) for 12 hours to completely dissolve the underlying copper foils. The PMMA-coated graphene layers were transferred onto

BTO/NSTO heterostructure by standard wet transfer method. After removing the PMMA with acetone, Au dots with 100 μm diameter and 100 nm thickness were prepared on the graphene surface by thermal evaporation through a shadow mask. Indium (In) metal was soldered on the NSTO surface to form good Ohmic contacts. After that, the samples were heated on a hot plate to improve the adhesion between the In metal and NSTO substrates for electrical measurement.

Figure 3. 1 Schematic fabrication process of graphene/BTO/NSTO heterostructure.

3.2.3 Crystalline characterization

High resolution X-ray diffractometer (Rigaku, SmartLab) was employed to study the epitaxial characteristic of the as-grown BTO films. During PLD growth condition optimization, thicker BTO films were grown on (001)-oriented STO single crystal substrates, which are supposed to have similar lattice structure with NSTO single crystal substrates. Figure 3.2(a) shows a typical XRD pattern of the BTO film deposited on (001)-oriented STO substrate. It can be observed that only (00l) peaks of BTO exist in the diffraction pattern besides the peaks of STO wafer, which confirms the single perovskite phase of BTO film grown on STO substrate. The crystallographic planes of BTO are parallel with the (00l) planes of STO, indicating the c-axis of the BTO film is

perpendicular to the substrate surface. The result shows the high quality of the as-grown BTO film by PLD approach. As shown in Figure 3.2(b), the X-ray reflectivity (XRR) profile exhibits that the reflectivity measurement matches well with the fitting result, suggesting the BTO film has a thickness around 50 nm. Reasonable parameters (density: BTO: 6.02 g/cm^3, STO: 5.18 g/cm^3) were used during fitting. Using the optimized PLD growth conditions, thinner BTO films at a thickness down to few nanometers can be grown by controlling the numbers of laser pulses during PLD process.

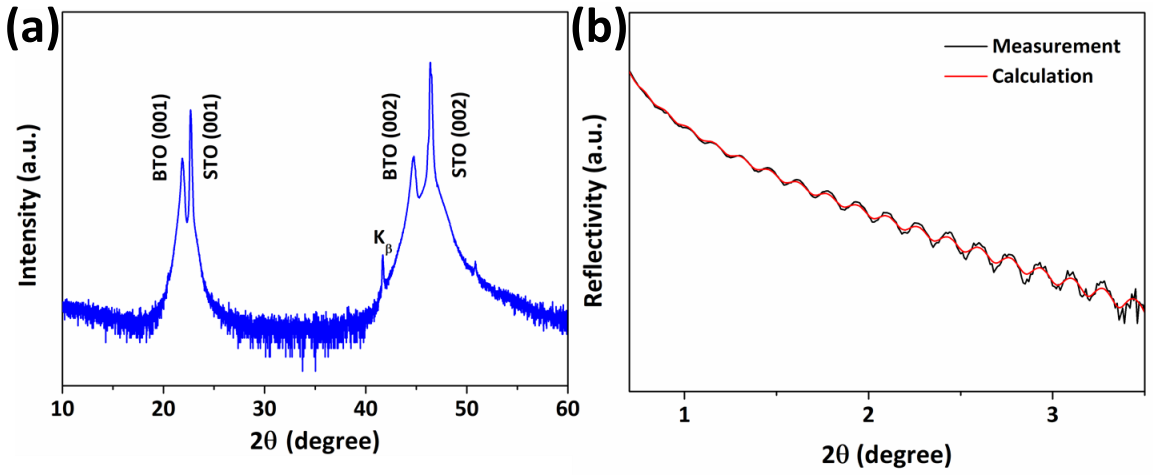


Figure 3. 2 Typical XRD (a) and XRR (b) patterns of BTO films grown on STO substrates.

3.2.4 Structural characterization

The chemical compositions and the bonding energies of the BTO films grown on NSTO substrates were characterized by X-ray photoelectron spectrometer (Thermo Scientific, ESCALAB 250Xi). Figure 3.3 shows the XPS measurement of Ti 2p and Ba 3d core levels in the BTO films. Two strong binding energy peaks of Ti element can be

observed at 458.3 eV (Ti $2p_{3/2}$) and 464.0 eV (Ti $2p_{1/2}$), which indicates the chemical valence state of Ti is fixed to be +4. Two binding energy peaks of Ba element can be seen at 778.5 eV (Ba $3d_{5/2}$) and 793.8 eV (Ba $3d_{3/2}$), which represents the chemical valence state of Ba is fixed to be +2. The content ratio of Ba/Ti of around 1:1 is revealed. These results are in good agreement with the typical pure BTO XPS observations [127, 128], which suggests the high quality of the BTO thin films grown by PLD method.

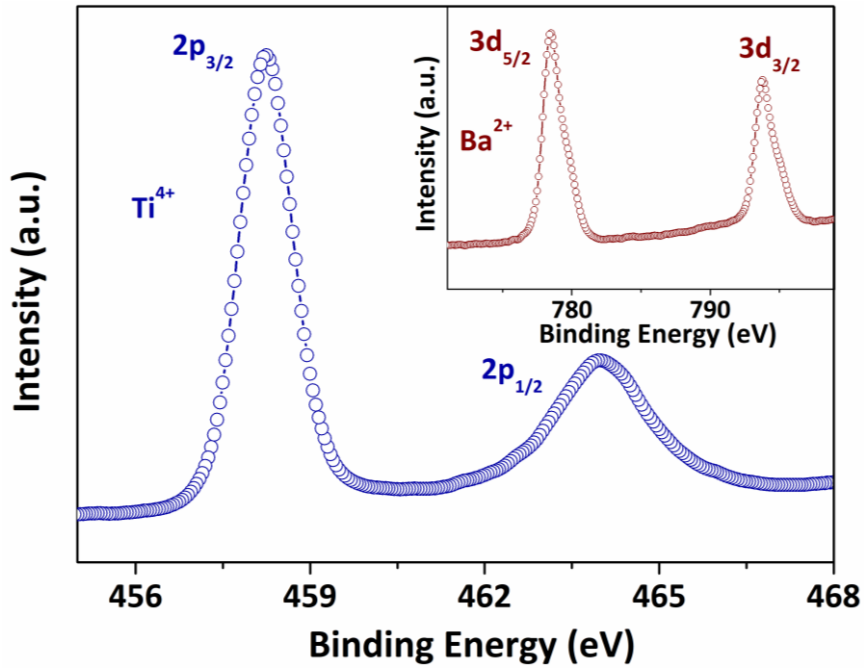


Figure 3. 3 XPS spectra of the BTO films.

3.2.5 Surface morphology and ferroelectric property characterization

PFM measurement was performed to characterize the domain structure and the ferroelectricity of BTO thin films grown on NSTO single crystal substrates. PFM was conducted on a commercial atomic force microscope (Asylum Research, MFP-3D infinity) using Pt/Ti-coated tip. The PFM signal was collected when the conductive tip

was in contact with the BTO film surface and the NSTO bottom electrode was grounded. Figure 3.4 shows the topography of BTO thin film with thickness of 3 nm grown on NSTO substrate (Nb: 0.7 wt%). The BTO/NSTO heterostructure reveals atomically flat surface with a root-mean-square (r.m.s) roughness of approximately 0.27 nm over an area of 1 x 1 μm^2.

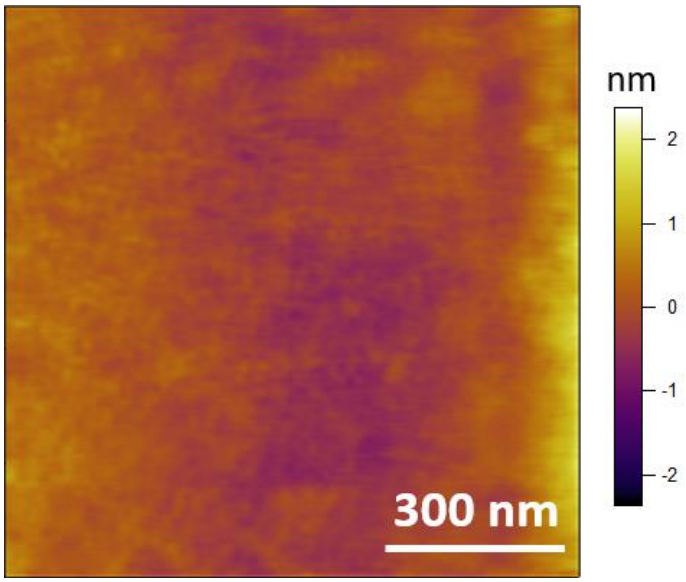


Figure 3. 4 Morphology of the BTO surface on NSTO substrate.

Ferroelectric polarization patterns can be acquired by changing the voltages applied to the film surface through the conductive tip during PFM scanning process. It is known that BTO has larger lattice constants than the NSTO, so the lattice mismatch induces compressive strain with the c-axis along the BTO film normal direction. The ferroelectric polarization is enhanced in the BTO thin film under the effect of compressive strain [85, 129, 130]. Based on the pre-defined protocol as shown in Figure 3.5(a), the ferroelectric domains are written by applying positive and negative DC

voltages of 3 V on the surface of BTO thin film through the conductive tip. Figures 3.5(b) and (c) reveal the out-of-plane PFM amplitude and phase images of the BTO film respectively. After applying a positive DC poling voltage of +3 V to a selected area, BTO is switched to a downward direction (polarization points towards the NSTO substrate), and its PFM phase image exhibits a uniform yellow contrast. When a negative DC poling voltage of -3V is applied to the remaining areas, BTO is switched to an upward direction (polarization points away from the NSTO substrate), and its PFM phase image shows a uniform purple contrast. The 180° phase contrast reveals the antiparallel polarization in the two domains of the BTO thin film. The minimum amplitude in the PFM amplitude image also indicates the domain structure boundary with antiparallel polarization. The local PFM hysteresis loops further confirm the ferroelectric nature with switchable polarization of the BTO thin film on NSTO substrate, as shown in Figure 3.5(d).

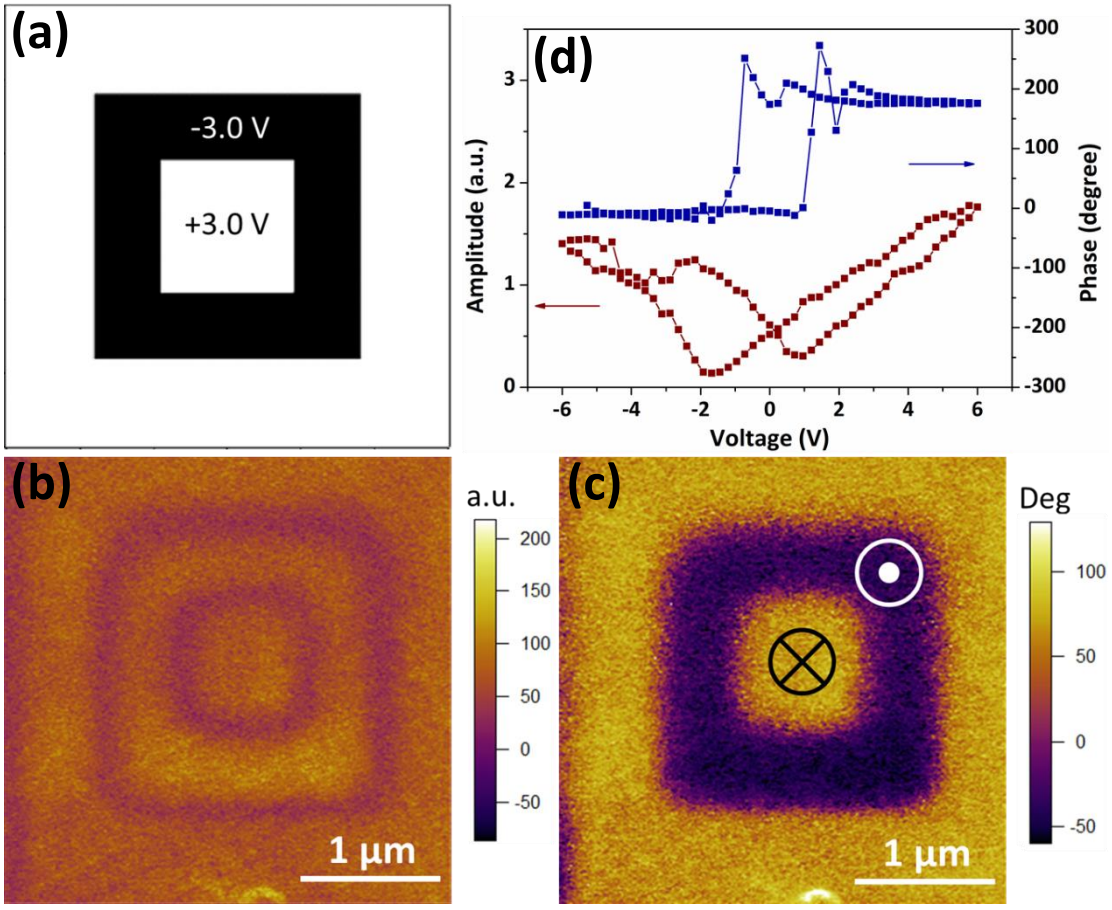


Figure 3. 5 (a) Protocol for PFM domain pattering. PFM out-of-plane amplitude (b) and phase (c) images of square domains with opposite polarization orientations written on BTO/NSTO surface. (d) Local PFM hysteresis loops: phase signal (top) and amplitude signal (bottom).

3.2.6 Raman characterization

Raman spectroscopy is useful for quick and effective inspection of the crystal quality and the layer number of the synthesized graphene. The CVD-grown graphene was characterized by high resolution Raman spectrometer (Horiba, LabRAM HR 800) with the excitation wavelength of 488 nm. An 100x objective lens was employed in the

measurement. Figure 3.6 shows the Raman spectrum of the CVD-grown graphene after transferring onto BTO/NSTO heterostructure. Two active features of G peak and 2D peak can be identified. A symmetric 2D peak centers at about 2690 cm^{-1} with a full-width-at-half-maximum (FWHM) of around 30 cm^{-1}. The intensity of the 2D peak is found to be approximately two times higher than that of the G peak, which confirms the graphene is a single layer. No significant defect-related D peak can be observed. The result suggests the high quality of the transferred graphene and the insignificant defect in the graphene layer.

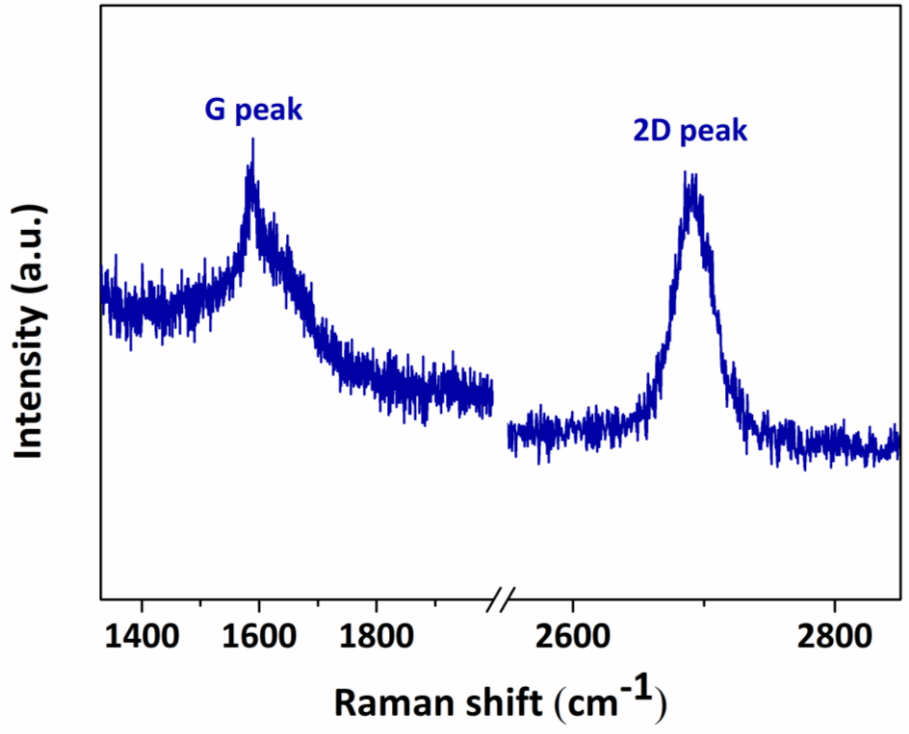


Figure 3. 6 Raman spectrum of the CVD-grown monolayer graphene on BTO/NSTO heterostructure.

3.3 Electrical measurement

In the work, we have fabricated the asymmetrical FTJ which employs both 2D material and semiconductor as the electrodes in conjunction with the ferroelectric thin film as the tunnel barrier. The device geometry of the graphene/BTO/NSTO heterostructure is schematically illustrated in Figure 3.7(a). The device exhibits a smooth surface with a r.m.s roughness of around 0.19 nm over a region of 5 x 5 μm^2 as shown in Figure 3.7(b). The schematic resistance switching principle of the graphene/BTO/NSTO tunnel junction is revealed in Figure 3.7(c). When a positive voltage is applied to the graphene surface, the ferroelectric polarization in BTO film points downward (polarization pointing towards the NSTO substrate). The positive bound charges in the BTO film will attract electrons on the NSTO surface. The NSTO n-type semiconductor is driven into accumulation state. Because of incomplete screening, a depolarization field emerges to oppose the polarization in the ferroelectric barrier. This depolarization field decreases the barrier height and enhances the charge tunneling transmittance. More charges can pass through the ferroelectric barrier. The device is set to the ON state with low resistance. After applying a negative voltage to the graphene surface, the ferroelectric polarization in BTO film is switched upward (polarization pointing away from the NSTO substrate). The negative bound charges in the BTO film will repel the electrons and drive the NSTO surface into depletion state.

The incomplete screening produces a depolarization field to increase the barrier height. Meanwhile, the immobile screening charges develop a space charge region in the depleted semiconductor. The electrons are required to tunnel through an extra barrier in the space charge region. The tunneling transmittance is reduced drastically by this additional barrier. Fewer charges can pass through the ferroelectric barrier. The device is set to the OFF state with high resistance.

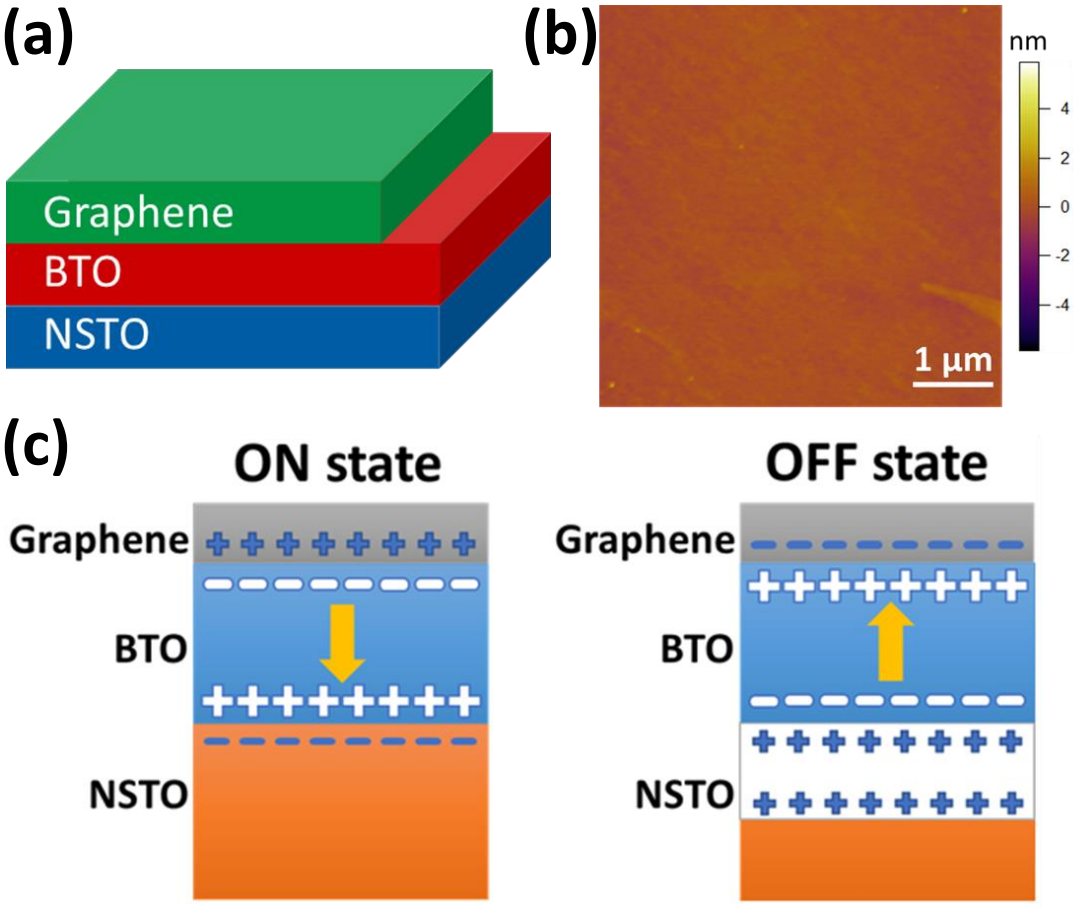


Figure 3. 7 (a) Schematic illustration of the graphene/BTO/NSTO heterostructure. (b) Surface morphology of the corresponding device. (c) Resistance switching principle of the graphene/BTO/NSTO tunnel junction for the ON state and the OFF state. The solid plus and minus symbols represent holes and electrons respectively. The empty plus and

minus symbols denote positive and negative ferroelectric bound charges respectively. The yellow arrows mean the ferroelectric polarization directions in the BTO film.

In the experiment, the electrical resistance switching of the graphene/BTO/NSTO heterostructure was characterized using a probe station connected to a Keithley 4200-SCS semiconductor parameter analyzer. To study the TER effect of the graphene/BTO/NSTO tunnel junction, two-terminal geometry was employed for current-voltage (*I*-*V*) characterization at room temperature. The applied voltage is termed as positive direction when a positive bias is applied to the graphene electrode. The NSTO electrode was grounded for all electrical measurement. Figures 3.8(a) and (b) show the *I*-*V* curves for the ON state and the OFF state of the graphene/BTO/NSTO heterostructure as a function of Nb doping concentration in the semiconductor electrode respectively. After applying a positive or negative write voltage pulse V_{write} with pulse width of 0.5 s to the graphene electrode, the *I*-*V* curve was measured in a low-bias regime (-0.2 V to 0.2 V). The applied voltages are +2.5/-2.5 V, +3.0/-3.0 V and +4.5/-5.0 V for the devices with 1.0 wt%, 0.7 wt% and 0.1 wt% Nb doping concentration respectively. When a positive voltage is larger than that of ferroelectric coercivity, downward polarization is developed in the BTO film. The device is set to low resistance ON state. Similarly, a larger negative voltage drives the device into high resistance OFF state with upward polarization. It is seen from the *I*-*V* curves that the ON state current

is much larger than the OFF state current for all the devices with 1.0 wt%, 0.7 wt% and 0.1 wt% Nb doping concentration. The clear conductance contrast confirms that the ferroelectric polarization reversal happens. When the Nb concentration changes from 1.0 wt% to 0.1 wt% in the semiconductor electrode, the magnitude of the OFF state current decreases sharply from around 10^{-6} to 10^{-8} A, but the ON state current magnitude reduces slightly from 10^{-4} to 10^{-5} A. Consequently, the ON/OFF conductance ratio taken at 0.2 V increases with decreasing Nb concentration, as shown in Figure 3.9. Our results are in good agreement with the observations in Pt/BTO/NSTO heterostructure where more significant variation of the OFF state *I-V* characteristic compared with the ON state *I-V* behavior leads to an increased ON/OFF ratio with decreasing Nb doping concentration [88, 131], showing the barrier tunability in both height and width as a function of Nb concentration on the semiconductor electrode. A remarkable ON/OFF ratio about 10^3 can be observed at 0.1 wt% Nb doping concentration of the graphene/BTO/NSTO FTJ, which is about one to two orders higher than that in typical BTO-based FTJs with metal electrodes [120, 121, 132, 133].

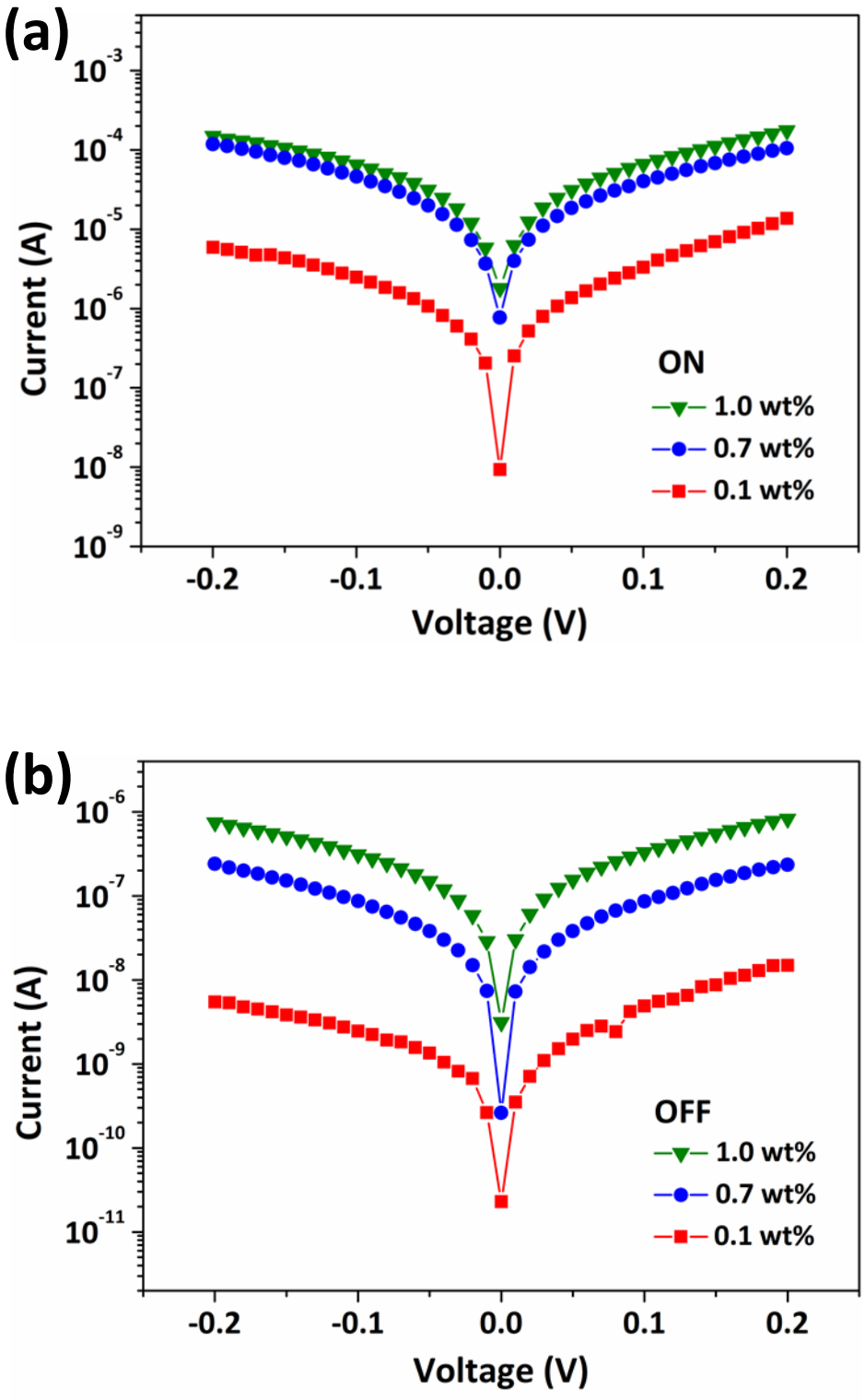


Figure 3. 8 The *I-V* curves of the graphene/BTO/NSTO heterostructure with various Nb doping concentration of semiconductor substrates in (a) the ON and (b) the OFF states at room temperature.

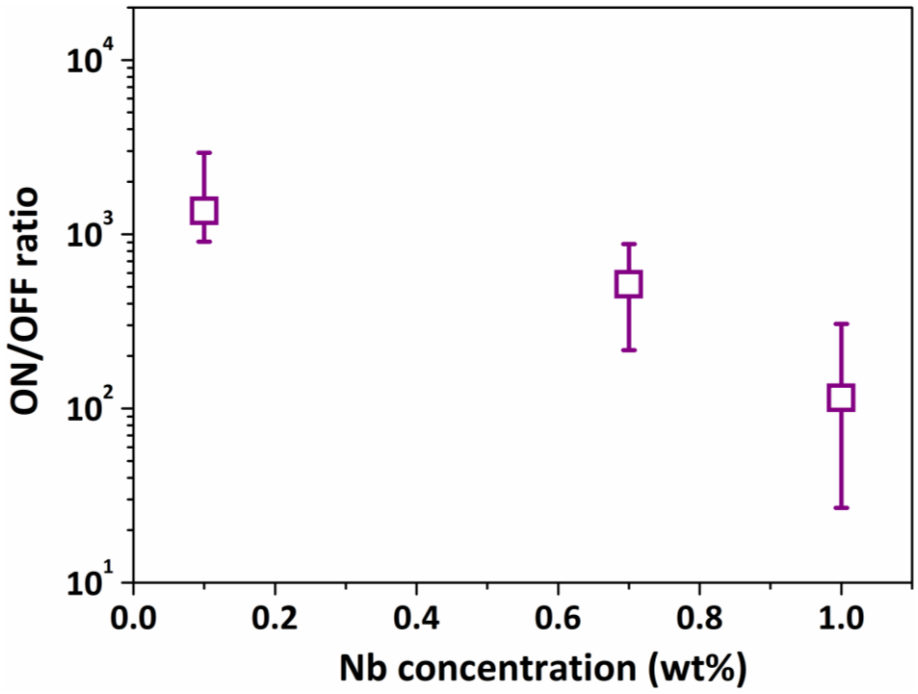


Figure 3. 9 The ON/OFF ratio of the graphene/BTO/NSTO heterostructure as a function of Nb doping concentration. The error bars present the average measured in 10 different device points for each Nb concentration.

To explain the TER dependence on Nb doping concentration, the schematic band structure of the graphene/BTO/NSTO heterostructure is revealed in Figure 3.10. When a positive voltage pulse drives the polarization pointing towards the NSTO electrode, the depleted region is decreased or even eliminated by electron accumulation on the semiconductor surface. The tunneling barrier height is decreased. The ON state transport is mainly governed by direct tunneling mechanism in the trapezoidal potential barrier of the ferroelectric thin film. When a negative voltage pulse is applied, ferroelectric polarization points away from the NSTO electrode. The depleted region is enhanced by electron depletion on the NSTO surface. The depletion region represents

an extra tunneling barrier, which increases in both barrier height and barrier width. In the OFF state, thermionic emission dominates the transport mechanism, which can be described by:

$$J_F = A^* T^2 \exp(-\phi_B/k_B T)\exp(qV/nk_B T) \quad (3.1)$$

where J_F is the forward bias current density, A^* the Richardson constant, T the absolute temperature, ϕ_B the barrier height, q the electron charge, k_B the Boltzmann constant and n the ideal factor. The barrier height increases with decreasing Nb doping concentration in the NSTO semiconductor. The corresponding width (W_D) of the depletion region can be expressed as the following equation:

$$W_D = (2\varepsilon_s V_{bi}/qN_D)^{1/2} \quad (3.2)$$

where ε_s is the dielectric constant of NSTO, N_D the Nb doping concentration, V_{bi} the build-in potential, $V_{bi} = (\phi_B + E_F - E_C)/q$, E_F and E_C the Fermi level and conduction-band minimum of NSTO respectively. As wider depletion regions are formed on lower Nb doping semiconductor in the OFF state, both the barrier height and barrier width are increased greatly [131]. From this, more significant reduction of the OFF state current is expected at the lower Nb concentration, which in turns increases the ON/OFF ratio with decreasing Nb concentration in the graphene/BTO/NSTO heterostructure.

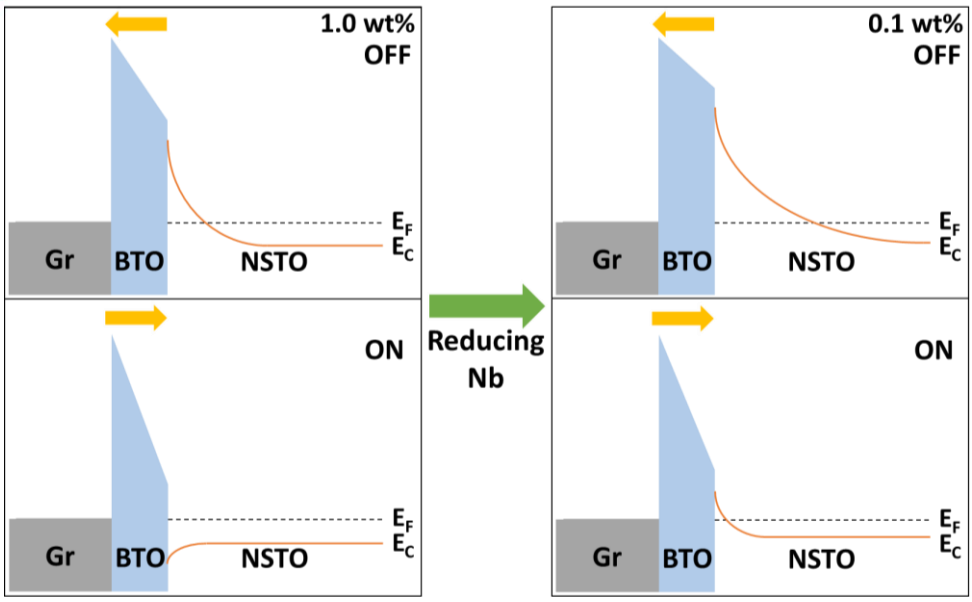
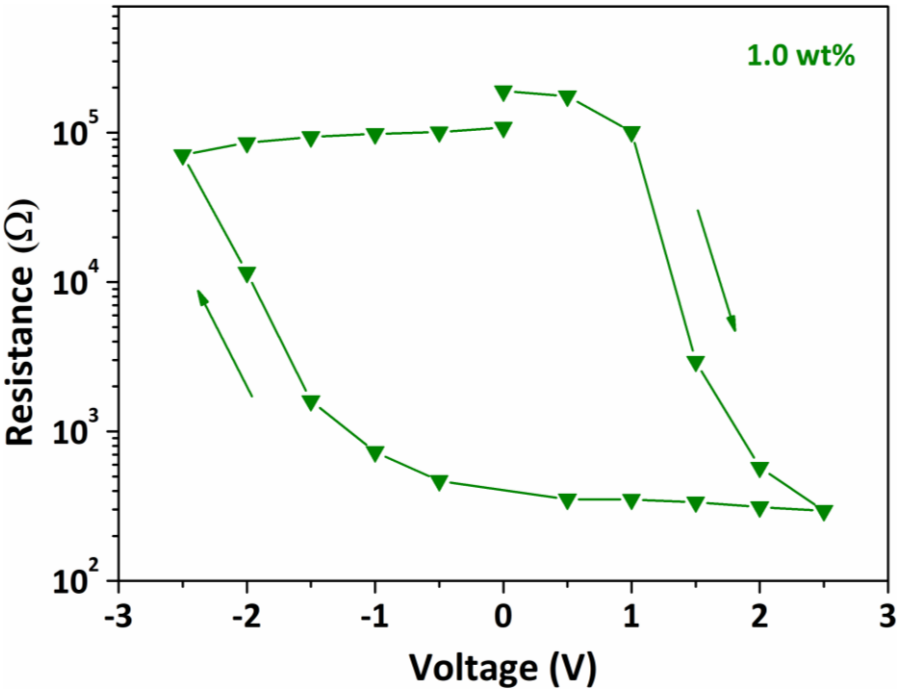


Figure 3. 10 Schematic energy barrier diagram of the graphene/BTO/NSTO heterostructure for the ON and OFF states with different Nb doping concentration. The Gr symbol represents graphene layer. The yellow arrows denote the polarization directions in the BTO barrier.

Figure 3.11 shows the non-volatile resistance-voltage (*R*-*V*) hysteresis loops of the graphene/BTO/NSTO heterostructure at room temperature. After applying different write pulses V_{write} with a step of 0.5 V, the resistance was recorded at a fixed read pulse V_{read} of 0.2 V. The obtained *R*-*V* loops exhibit resistive switching behaviors near the coercivity of PFM hysteresis loops in Figure 3.5(d). The observation indicates that the FTJ resistance switching is a direct result of the ferroelectric polarization switching of the BTO film. The positive pulse switches the polarization of BTO to a downward direction, while the negative pulse switches the polarization to an upward direction. It is shown that a positive or negative V_{write} drives the devices into the low resistance state

or high resistance state respectively. When the Nb concentration decreases from 1.0 wt% to 0.1 wt% in the semiconductor electrode, it can be seen from the *R*-*V* loops that the magnitude of the OFF state resistance increases significantly, but the resistance magnitude of the ON state changes slightly. As a result, the ON/OFF ratio increases with decreasing Nb concentration. For the 0.1 wt% device, a remarkable ON/OFF ratio above 10^3 can be obtained. The ON/OFF ratio enhancement in the *R*-*V* loops is similar to the estimation of the *I*-*V* curves as described before.



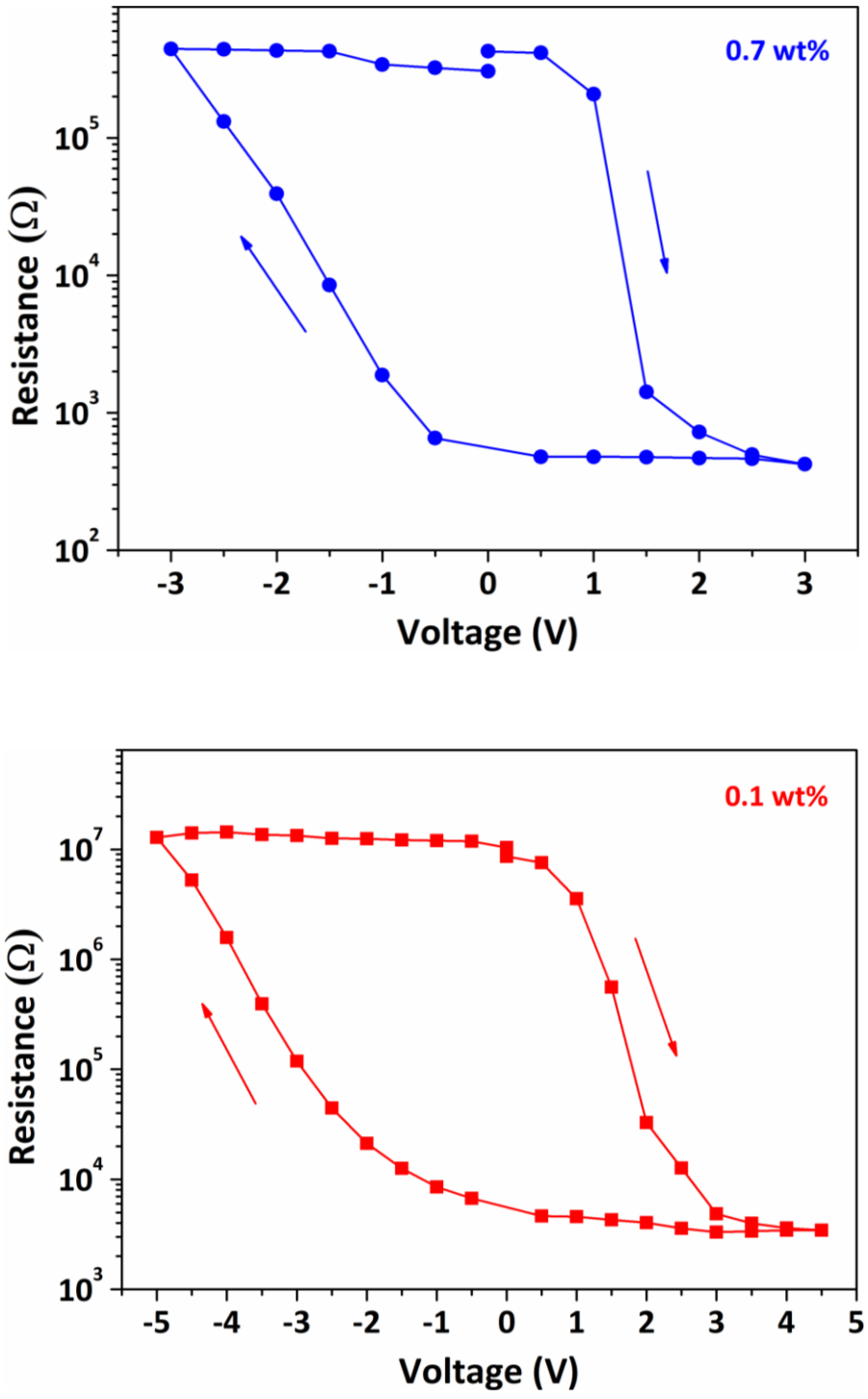


Figure 3. 11 The room-temperature *R-V* hysteresis loops of the graphene/BTO/NSTO heterostructure as a function of Nb doping concentration in NSTO substrates: 1.0 wt% (top), 0.7 wt% (middle), and 0.1 wt% (bottom).

Furthermore, retention property and switching reproducibility are important parameters in non-volatile memory applications. Figure 3.12(a) reveals the resistance retention of the graphene/BTO/NSTO heterostructure as a function of Nb concentration. There is no obvious degradation of resistance in both ON state and OFF state within 10^2 s. Figure 3.12(b) exhibits the bipolar resistance switching of the devices with different Nb concentration. The switching characteristics were tested via the application of repeated bipolar electrical pulses to the devices. The V_{write} heights were determined from the *R-V* hysteresis loops for each Nb wt% and V_{read} of 0.2 V remained unchanged. For the 0.1 wt% device, a high ON/OFF ratio about 10^3 could still be preserved after more than 40 write/read cycles. The 0.7 wt% and 1.0 wt% devices with lower ON/OFF ratios also show good switching endurance after several cycles. Therefore, good resistance stability and switching reproducibility of the graphene/BTO/NSTO heterostructure can be achieved. As reported previously, encapsulating functional molecules at the graphene/ferroelectric interface could further enhance the resistance switching effect [94]. The way of graphene interface engineering makes our graphene/BTO/NSTO device design useful.

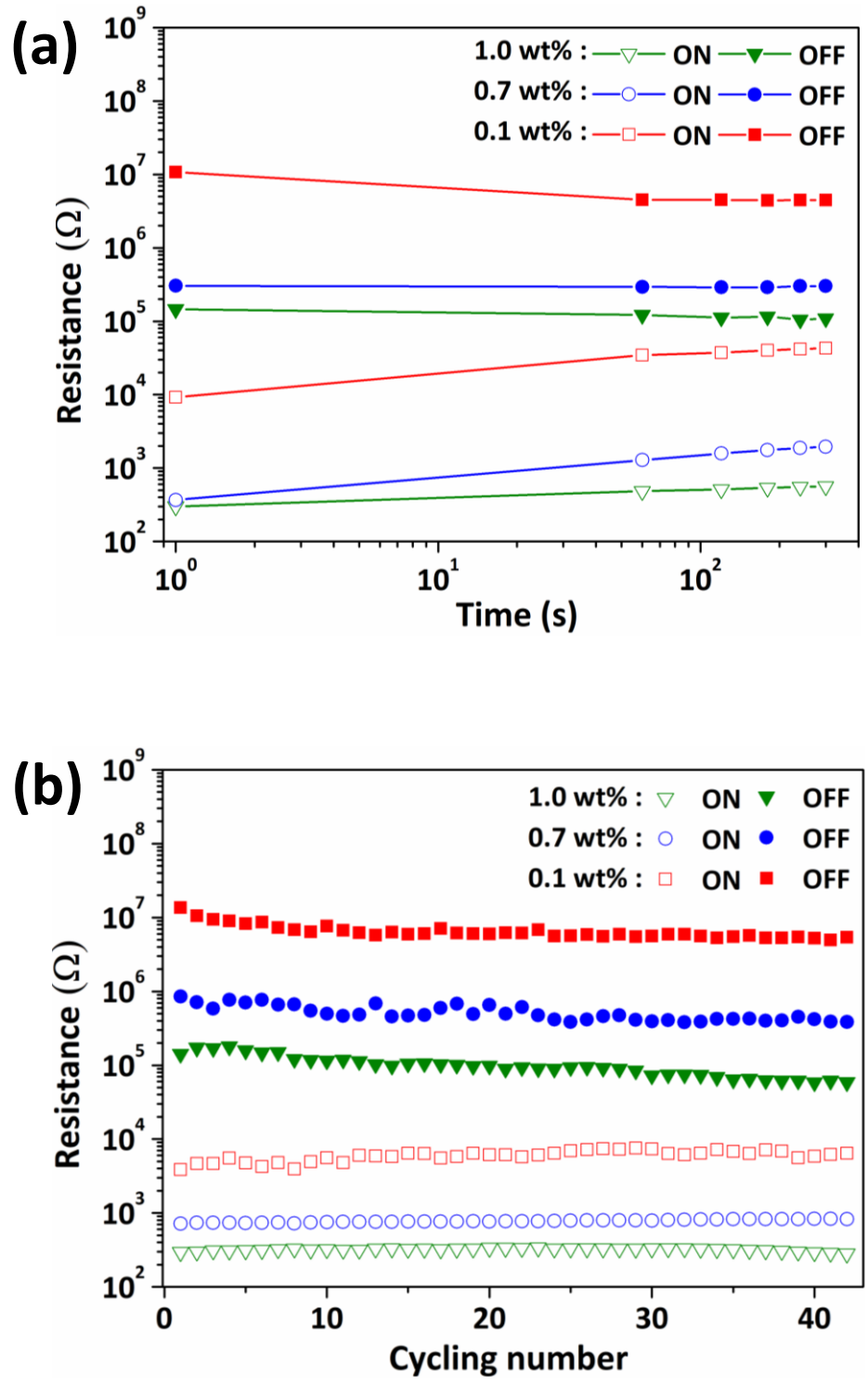


Figure 3. 12 (a) Data retention and (b) bipolar resistance switching of the graphene/BTO/NSTO heterostructure with different Nb doping concentration in semiconducting NSTO substrates at room temperature.

3.4 Summary

In summary, we present an asymmetrical FTJ employing both two-dimensional material and semiconductor electrode in the graphene/BTO/NSTO heterostructure. Compared with traditional metal electrodes, graphene electrodes possess the great advantages of atomic level thickness and optical transparency, which may facilitate the design of future ultra-broadband and high-speed optoelectronic devices. By utilizing various characterization techniques including Raman spectroscopy, XRD, XPS and PFM, we find that the graphene nanosheets and BTO thin films are of high quality. The TER dependence of the graphene/BTO/NSTO heterostructure is revealed on Nb doping concentration from 0.1 wt% to 1.0 wt% in the semiconductor electrode. In addition to modulating barrier height by ferroelectric polarization reversal, the ON/OFF resistance ratio can be tuned by adjusting Nb doping concentration due to further modulation of barrier width. An optimized ON/OFF ratio up to 10^3 is observed at room temperature when introducing 0.1 wt% Nb concentration of the device. Furthermore, good retention property and switching reproducibility can be achieved in the devices. The results pave the way to design the graphene-based FTJs at nanoscale, which is useful for developing non-volatile memory with enhanced performance.

Chapter 4 Fabrication and Characterization of Vertical Graphene-Based Tunneling Transistor

4.1 Introduction

The requirement of more compact and powerful devices in electronic and optoelectronic applications has been growing since the silicon has reached its limit. The first prototype of graphene-based field-effect transistor (GFET) was demonstrated by Novoselov *et al*. in the last decade [6]. Without a finite energy bandgap between the conduction and valence bands of graphene, the GFET is still conducting even when switched off. Therefore, a fundamental problem of the planar graphene-based transistors is their limited current ON/OFF ratio [37-41]. Other alternatives including using bilayer graphene, nanoribbons and chemical derivatives would degrade the graphene's electronic quality although a finite bandgap could be introduced to the graphene layer [42-44]. To improve the GFET performance, Georgiou *et al*. proposed a novel idea of vertical graphene heterostructure FET (VGHFET) [45]. In the device architecture, the electrons can tunnel from a graphene layer to another layer through an ultrathin tunnel barrier. The noticeable ON/OFF ratio enhancement has been achieved by using 2D hBN or MoS_2 as the tunnel barrier in the VGHFETs.

In general, a tunnel junction consists of a thin tunnel barrier sandwiched between

two electrodes. In contrast to conventional tunnel junction, the ferroelectric barrier profile in FTJs can be modulated in response to polarization reversal [105]. Theoretical and experimental works have given evidence to the local modulation of electron transport in the ferroelectric barrier [62, 74]. The phenomenon can give rise to tunneling resistance switching effect and tunneling current amplification when ferroelectric switching takes places. However, there is limited study on the integration of FTJ and VGHFET to design the novel device architecture. Therefore, it is an interesting topic to investigate the coupling of FTJ and VGHFET in the multilayer heterostructure.

In this chapter, we report a vertical graphene-ferroelectric tunneling heterostructure (VGFTH)-based field-effect transistor (FET). The device is based on VGHFET where conventional tunnel barrier of insulator or semiconductor is replaced with ultrathin ferroelectric film. The combination of VGHFET and FTJ could add new functionality and tunability to the multilayer graphene-based heterostructure. The VGFTH-based FETs are designed and fabricated, including the back-gated and top-gated architectures. The output and transfer electronic properties of the devices are characterized in the study.

4.2 Experimental

4.2.1 Fabrication of back-gated VGFTH-based FETs

In the experiment, we have fabricated the back-gated VGFTH-based FETs. The device geometry is based on Au/Sm:$BiFeO_3$ (SBFO)/graphene on an oxidized Si substrate. The SBFO film has the merits of good ferroelectricity and low energy bandgap [134]. Due to chemical doping, the SBFO is supposed to have lower current leakage than the pure BFO, which is desirable for the ferroelectric tunnel barrier [135]. During the fabrication process, SiO_2 (300 nm)/Si substrates were sonicated with acetone, ethanol and DI water for 20 minutes each to ensure clean substrate surface. The CVD-grown graphene sheets were transferred onto the SiO_2 (300 nm)/Si substrates by standard wet transfer approach. The SBFO thin films were deposited on the graphene surface through PLD method. The PLD conditions of SBFO thin films are summarized in Table 4.1. Before deposition, the base pressure of the chamber was evacuated to 10^{-4} Pa. During deposition, a KrF excimer laser was focused on the high-purity SBFO ceramic target (99.99%) with the wavelength of 248 nm, fluence of 250 mJ and repetition rate of 5 Hz. The substrates-target distance was 5 cm. The SBFO thin films were grown at deposition temperature of 700 °C under oxygen pressure of 10 Pa. The estimated growth rate is around 0.06 Å/pulse. The film thickness can be controlled by the total laser pulse numbers. After deposition, the thin films were cooled down

naturally to room temperature. Au electrodes with the thickness of 100 nm and diameter of 100 μm were prepared on the sample through a defined shadow mask by thermal evaporation.

Table 4. 1 PLD deposition conditions for SBFO thin film.

Target	SBFO ceramic
Laser wavelength	248 nm
Laser energy	250 mJ
Deposition frequency	5 Hz
Target-substrate distance	5 cm
Base pressure	10^{-4} Pa
Substrate temperature	700 °C
Growth pressure	10 Pa
Growth rate	0.06 Å/pulse

4.2.2 Device structural characterization

The device geometry of the back-gated VGFTH-based FETs is schematically shown in Figure 4.1(a). The optical image taken by optical microscopy reveals the multilayer device structure as shown in Figure 4.1(b). The epitaxial features of the PLD-grown SBFO films were characterized by high resolution X-ray diffractometer (Rigaku, SmartLab). As indicated in Figure 4.1(c), the XRD pattern shows that only (00l) peaks

of SBFO exist in the diffraction pattern apart from the STO peaks, indicating the single perovskite phase and high quality of the SBFO films. After optimization, we employed the same PLD conditions to grow ultrathin SBFO films with the thickness of around 3 nm on the graphene surface for device fabrication. The CVD-grown graphene sheets were characterized by Raman spectrometer (Horiba, LabRAM HR 800) with the 488 nm excitation wavelength. Figure 4.1(d) shows the typical Raman spectrum of the graphene layer on the SiO_2 (300 nm)/Si substrate before PLD process. There are two active Raman features of the G peak and 2D peak observed. A symmetric 2D peak centers at around 2695 cm^{-1} with a FWHM of 30 cm^{-1}. The intensity of the 2D peak is about two times higher than that of the G peak, indicating the graphene single layer. The absence of the significant defect-related D peak suggests the insignificant defect and high quality of the transferred graphene on the oxidized silicon substrate. Figure 4.1(e) shows the Raman spectrum of the graphene layer without SBFO film on the graphene surface after PLD process. A defect D peak can be found in the graphene layer, which may be explained by the critical PLD conditions such as high temperature and oxygen pressure for thin film deposition. Figure 4.1(f) exhibits the Raman spectrum of the graphene layer with SBFO film on the graphene surface after PLD. The absence of the two active Raman characteristics of the G peak and 2D peak suggests that the graphene is damaged, which may be ascribed to the highly energetic PLD process.

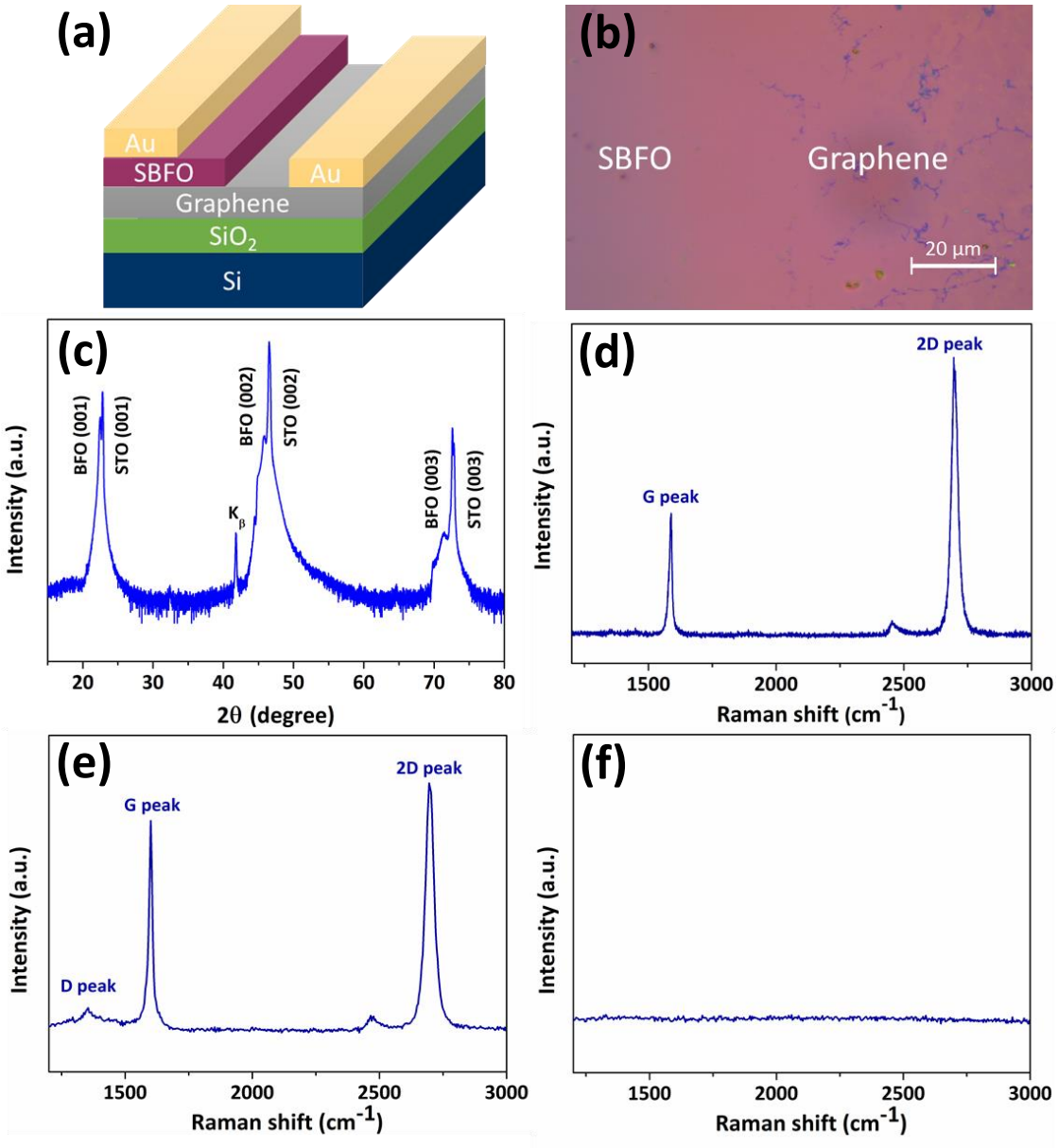


Figure 4. 1 (a) Schematic device architecture of the VGFTH-based FET with Au/SBFO/graphene/SiO_2/Si heterostructure. (b) Optical micrograph of the device. (c) XRD pattern of SBFO film on STO substrate. Raman spectrum of single layer graphene on SiO_2/Si wafer before PLD (d), after PLD without direct exposure to SBFO film deposition (e), and after PLD with direct exposure to film deposition (f).

4.2.3 Fabrication of top-gated VGFTH-based FETs

In the experiment, we have demonstrated the top-gated VGFTH-based FETs in the Au/Al_2O_3/graphene/BTO/NSTO heterostructure. The fabrication procedures of the device are schematically illustrated in Figure 4.2. During the fabrication process, (001)-oriented NSTO single crystal substrates were sequentially sonicated with acetone, ethanol and DI water for 20 minutes each to remove the surface impurities. The BTO thin films were grown on the NSTO substrates by PLD method. Following standard wet transfer technique, the PMMA/graphene sheets were transferred onto the BTO/NSTO heterostructure. Part of the PMMA coating was removed after soaking in acetone solution to pattern the exposed areas of the underlying graphene. The aluminum oxide (Al_2O_3) dielectric layers with the thickness of 50 nm were grown on the samples through atomic layer deposition (ALD). The ALD conditions of Al_2O_3 films are presented in Table 4.2. After that, the samples were immersed again in the acetone solution to lift-off the Al_2O_3 dielectric layers on top of the PMMA coating. Au electrodes with the thickness of 100 nm and diameter of 200 μm were prepared on the samples through thermal evaporation with a defined shadow mask. In metal was soldered on the NSTO surface to form good Ohmic contacts for electrical measurement.

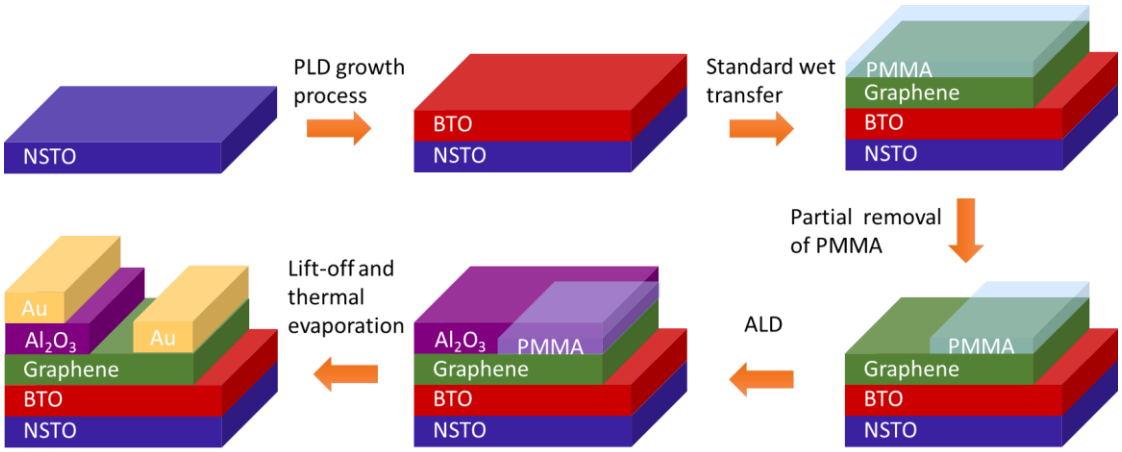


Figure 4. 2 Schematic illustration of the fabrication process of the Au/Al_2O_3/graphene/BTO/NSTO heterostructure.

Table 4. 2 ALD deposition conditions for Al_2O_3 dielectric film.

Dielectric	Al_2O_3
Precursor 1	Trimethylaluminum (TMA)
Precursor 2	H_2O
Growth temperature	80 °C
Growth rate	0.375 Å/s

In addition, we have demonstrated alternative top-gated VGFTH-based FETs in the Au/Al_2O_3/graphene/BTO/$La_{0.7}Sr_{0.3}MnO_3$ (LSMO)/STO heterostructure. The schematic fabrication process of the heterostructure is shown in Figure 4.3. The (001)-oriented STO single crystal substrates were sequentially washed with acetone, ethanol and DI water to clean the substrate surface. PLD method was employed to grow LSMO thin films on the STO substrates. The PLD growth conditions of LSMO films are

summarized in Table 4.3. Prior to deposition, the chamber was evacuated to a base pressure of 10^{-4} Pa. High-purity stoichiometric LSMO ceramic was used as the target material. During deposition, a KrF excimer laser was focused on the LSMO target with 248 nm wavelength, 250 mJ fluence and 5 Hz pulse frequency. The target was placed parallel to the substrate at a distance of 5 cm. The LSMO films were grown at deposition temperature of 700 °C under oxygen pressure of 25 Pa. The estimated growth rate is around 0.08 Å/pulse. The film thickness can be adjusted by controlling the total growth time and laser pulse frequency. After deposition, the LSMO films were cooled down to room temperature. Then, BTO thin films were grown on the LSMO/STO hybrid structure by PLD method employing the high-quality BTO ceramic target. Graphene sheets were transferred onto the BTO/LSMO/STO heterostructure by wet transfer technique. Following ALD approach, (50 nm) Al_2O_3 layers were deposited on the samples to serve as gate dielectrics. Au electrodes were patterned on the sample surface via thermal evaporation using a pre-defined shadow mask.

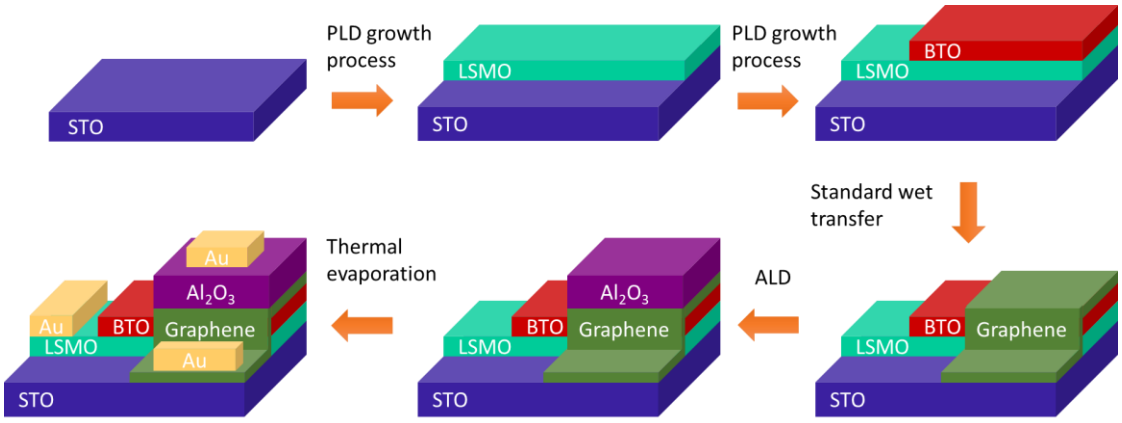


Figure 4. 3 Schematic fabrication flow of the Au/Al_2O_3/graphene/BTO/LSMO/STO heterostructure.

Table 4. 3 PLD deposition conditions for LSMO film on STO substrate.

Target	LSMO ceramic
Laser wavelength	248 nm
Laser energy	250 mJ
Deposition frequency	5 Hz
Target-substrate distance	5 cm
Base pressure	10^{-4} Pa
Substrate temperature	700 °C
Growth pressure	25 Pa
Growth rate	0.08 Å/pulse

4.3 Electrical measurement

4.3.1 Electrical characterization of Au/Al_2O_3/graphene/$BaTiO_3$/Nb:$SrTiO_3$ heterostructure

In the work, we have fabricated the top-gated VGFTH-based FETs. The device is based on Au/Al_2O_3/graphene/(5 nm) BTO/(0.7 wt%) NSTO multilayer heterostructure. To characterize the electrical properties of the device, three-terminal geometry was employed for the *I-V* characterization at room temperature. There are three electrodes for gate, drain and source. In this system, a gate voltage (V_g) is applied to the Al_2O_3 gate electrode and a drain voltage (V_d) is applied between the graphene drain electrode and NSTO source electrode. The schematic structure of the VGFTH-based FET is shown in Figure 4.4(a). For simplicity, the initial electronic potential barrier is assumed to have rectangular shape without voltage applied. The operation principle of the device relies on the changes in the density of states (DoS) and Fermi level (E_F) of the graphene, as well as the effective barrier height of the ferroelectric tunnel barrier adjacent to the graphene when V_g is varied between Au and graphene across Al_2O_3 dielectrics. Graphene can exhibit large variation of E_F in a given V_g due to its low DoS characteristics. Figure 4.4(b) reveals the band diagram of the device in the absence of V_g and V_d across ferroelectric barrier between graphene and NSTO. As shown in Figure 4.4(c), a negative V_g shifts E_F in the graphene downward, leading to an increase in the

barrier height from Φ_0 to Φ_{1+}. The device is set to the OFF state and the current in this state is denoted as I_{off}. When the applied V_d exceeds the coercive voltage (V_c) of the ferroelectric barrier, the asymmetry of the electronic potential profile of the ferroelectric barrier will be reversed by polarization reversal, which may alter the potential barrier height. When increasing positive V_d is applied, the NSTO semiconductor is switched to an accumulation state on the NSTO surface by ferroelectric field effect, resulting in a reduction in the barrier height (Figure 4.4(d)). In this case, the overall barrier height can be decreased by $\Delta\Phi_B$, which is termed as the difference in the barrier height before and after polarization reversal. Since the original barrier height Φ_{1+} is large, such a reduction of $\Delta\Phi_B$ will make an insignificant effect on the overall barrier height. The I_{off} has little change with polarization reversal. The sign of the Fermi level shift of graphene depends on the polarity of the V_g applied. As shown in Figure 4.4(e), a positive V_g shifts E_F in the graphene upward, leading to a decrease in the barrier height from Φ_0 to Φ_{2+}. The device is set to the ON state and the current in this state is denoted as I_{on}. With increasing positive V_d applied, ferroelectric polarization reversal will take place and barrier height can be further decreased by extra $\Delta\Phi_B$ (Figure 4.4(f)), which can be ascribed to the ferroelectric domain switching (Figure 4.4(g)). In this case, the reduction of $\Delta\Phi_B$ in the barrier height is more significant as the original barrier height Φ_{2+} is quite low and the I_{on} has more obvious change with polarization reversal. Therefore, the VGFTH-based

FETs coupling conventional VGHFET with FTJ could enhance the I_{on}/I_{off} ratio in principle.

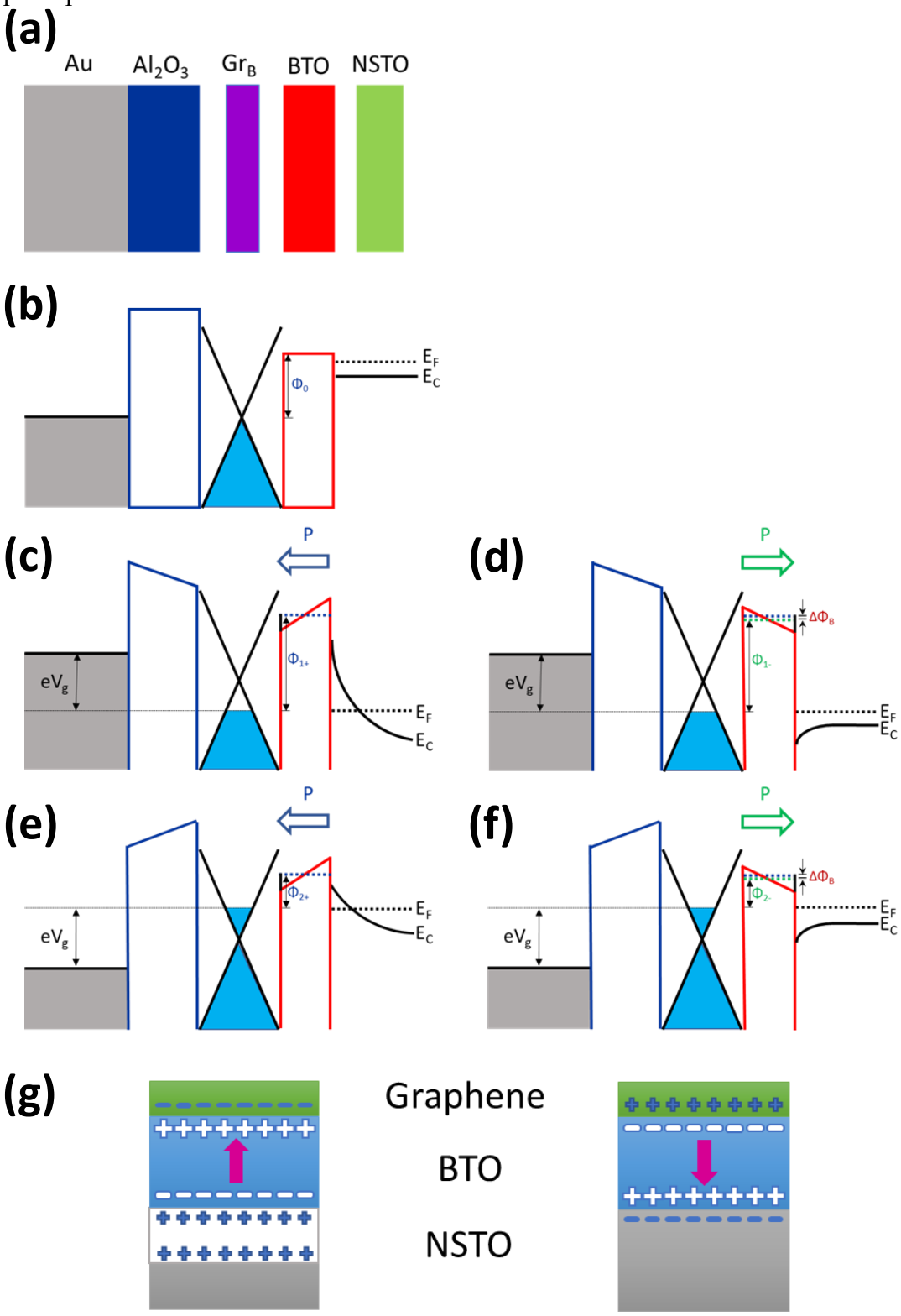


Figure 4. 4 (a) Schematic illustration of device structure. (b) Energy band diagram when

$V_g = 0$ and $V_d = 0$. (c) When $V_g < 0$ and $V_d < V_c$, V_g shifts E_F downward in the OFF state. (d) When $V_g < 0$ and $V_d > V_c$, the overall potential barrier is slightly shifted, resulting in little change of I_{off} due to large Φ_{1+}. (e) When $V_g > 0$ and $V_d < V_c$, V_g shifts E_F upward in the ON state. (f) When $V_g > 0$ and $V_d > V_c$, the overall barrier is reduced by $\Delta\Phi_B$ (blue line: before ferroelectric switching; green line: after ferroelectric switching), resulting in enhanced I_{on} due to small Φ_{2+}. (g) Schematic ferroelectric domain switching.

In the experiment, the VGFTH-based FET was characterized using a probe station connected to a Keithley 4200-SCS semiconductor parameter analyzer. The *I-V* electrical measurement of the device was conducted in air ambient at room temperature. Figure 4.5(a) shows the output characteristics of the VGFTH-based FET with Au/Al_2O_3/graphene/BTO/NSTO heterostructure. The inset presents the corresponding device geometry. In the top-gated device architecture, the graphene layers may expose less damages from fabrication process such as highly energetic PLD growth of ferroelectric thin films on graphene surface in the back-gated design. The asymmetric curves of drain current (I_d) as a function of V_d can be observed when V_g is swept from -5 V to 5 V. Figure 4.5(b) reveals the transfer characteristics of the VGFTH-based FET. It is noted that the I_d changes with V_g due to tunnel barrier height modulation by V_g, which meets the expectation of the aforementioned operation principle. The device exhibits large gate modulation of I_d under negative V_g, but small gate modulation under

positive V_g. The asymmetric features indicate that the carrier type of tunneling is hole. The observation of the charge transport may be ascribed to the p-type nature of graphene. It is commonly observed that graphene exhibits p-type property in air ambient as a result of the existence of water adsorbates [96, 125]. As seen from the transfer characteristic curve, when V_g is changed from -5 V to 5 V, the FET yields an I_{on}/I_{off} ratio of about 1.14 x 10^2 at a given V_d of 1 V, which is near the coercivity of the ferroelectric barrier for ferroelectric switching. The negligible gate leakage current in the order of 10^{-11} A indicates the high accuracy of the electrical measurement. In the high voltage regime, Fowler-Nordheim tunneling is considered for the main transport mechanism for our measurement. The Fowler-Nordheim tunneling shares the same physical phenomenon with direct tunneling through a triangular potential barrier of the ferroelectric thin film [76, 80]. It is interesting to note that VGFTH-based FET is a type of three-terminal device, which is different from the two-terminal FTJ device. Therefore, the VGFTH-based FET has the possibility to provide more degrees of freedom to modulate the transport behaviors of the device.

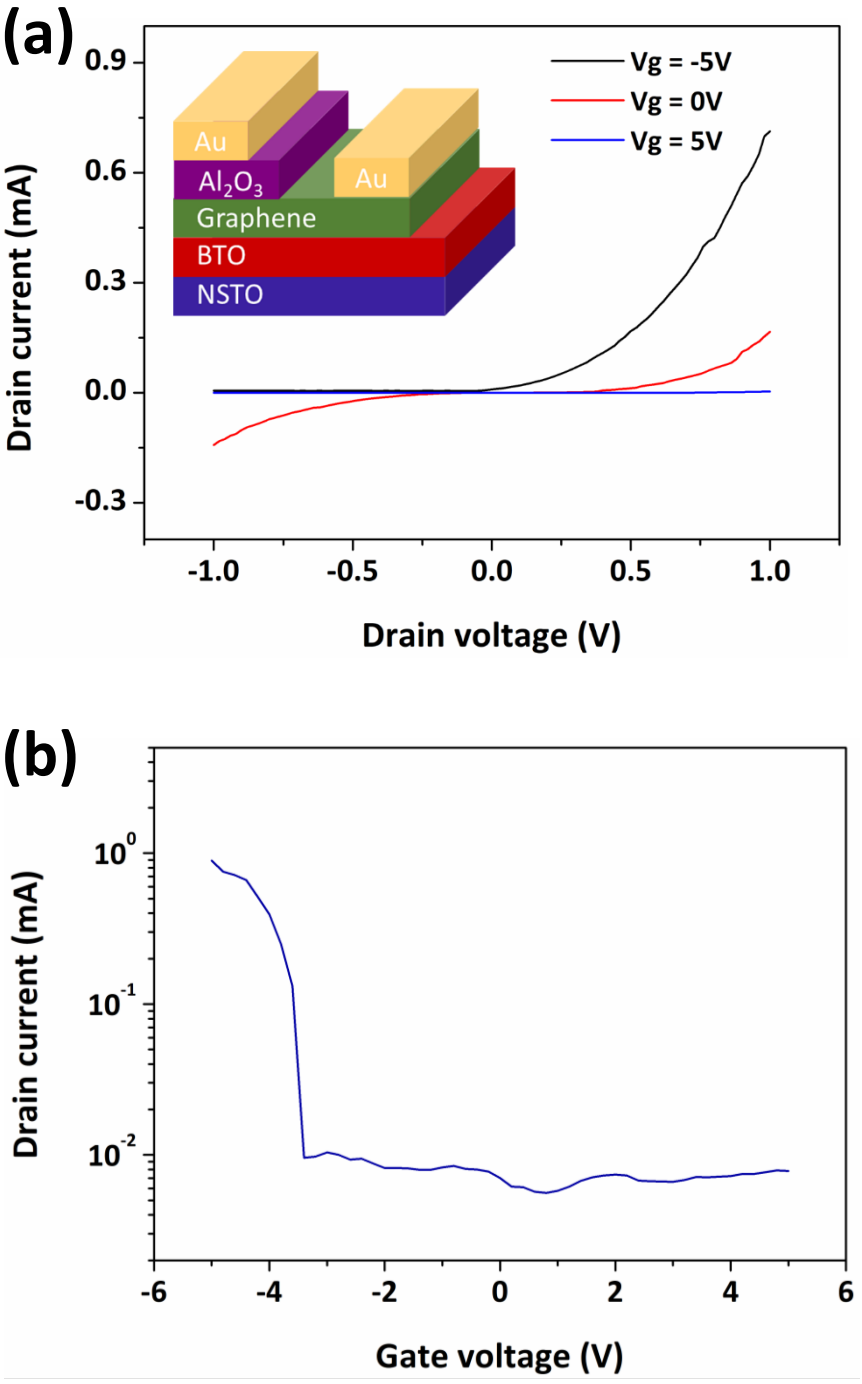


Figure 4. 5 (a) I_d-V_d output characteristics of the VGFTH-based FET with Au/Al_2O_3/graphene/BTO/NSTO heterostructure with different V_g. Inset is the schematic device geometry. (b) I_d-V_g transfer characteristics of the device at V_d = 1 V.

Meanwhile, we have fabricated the planar GFETs for comparison. The device is made by coupling graphene layer with SiO_2 (300 nm)/Si substrate. Figure 4.6(a) shows the output characteristics of the planar GFET. The inset indicates the photograph of electrode pattern. The linearity of I_d and V_d with V_g varying from -70 V to 70 V suggests the ohmic contact of the device. Figure 4.6(b) exhibits the transfer characteristics of the device. A typical p-type semiconductor behavior is observed with larger gate modulation of I_d under negative V_g. Due to finite energy bandgap of graphene, the I_{on}/I_{off} ratio of the GFET is found to be about 3.50, which is an order of magnitude lower than the VGFTH-based FET. Compared with the planar graphene-based FET, the vertical design of VGFTH-based FET seems to increase the switching ratio performance in different charge transport system.

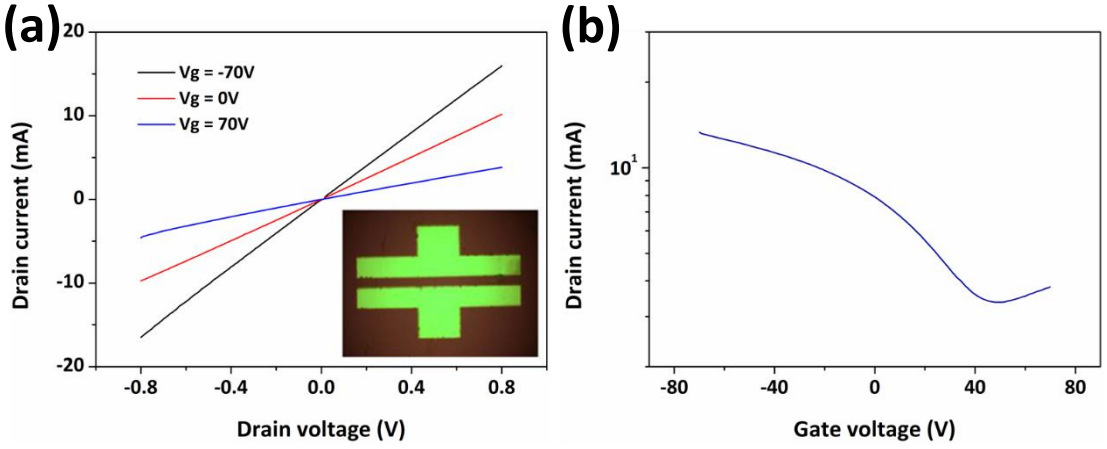


Figure 4. 6 (a) Output characteristics of the GFET with various V_g. Inset is the electrode pattern image. (b) Transfer characteristics of the device at $V_d = 0.8$ V.

4.3.2 Electrical characterization of Au/Al_2O_3/graphene/$BaTiO_3$/$La_{0.7}Sr_{0.3}MnO_3$ /$SrTiO_3$ heterostructure

Furthermore, we have proposed alternative approach to fabricate the VGFTH-based FETs. The device is based on Au/Al_2O_3/graphene/(10 nm) BTO/(30 nm) LSMO/STO heterostructure. Figure 4.7(a) presents the schematic device geometry. The optical image of the fabricated device taken by optical microscopy is shown in Figure 4.7(b). A three-terminal configuration was used to characterize the *I*-*V* behavior of the heterostructure at room temperature. In the experiment, a V_g is applied to the Al_2O_3 gate electrode and a V_d is applied between the graphene drain electrode and LSMO source electrode. Figure 4.7(c) exhibits the output characteristics of the VGFTH-based FET with Au/Al_2O_3/graphene/BTO/LSMO/STO heterostructure. An asymmetric behavior of I_d and V_d can be observed when V_g is changed from -5 V to 5 V. For the high voltage regime, Fowler-Nordheim tunneling may dominate the transport mechanism [80]. Figure 4.7(d) reveals the transfer characteristics of the device. A p-type feature can be identified from the larger I_d modulation with increasing negative V_g. The result is consistent with the p-type graphene where holes are the major tunneling carriers [126]. The gate leakage current in the order of 10^{-10} A is negligible to the electrical measurement. The I_{on}/I_{off} ratio of the device is only about 3.77. The possible reasons for this include the non-optimized growth of the LSMO thin film or the interfacial

influence between each layer of the multilayer heterostructure. The device performance will be optimized in the future work.

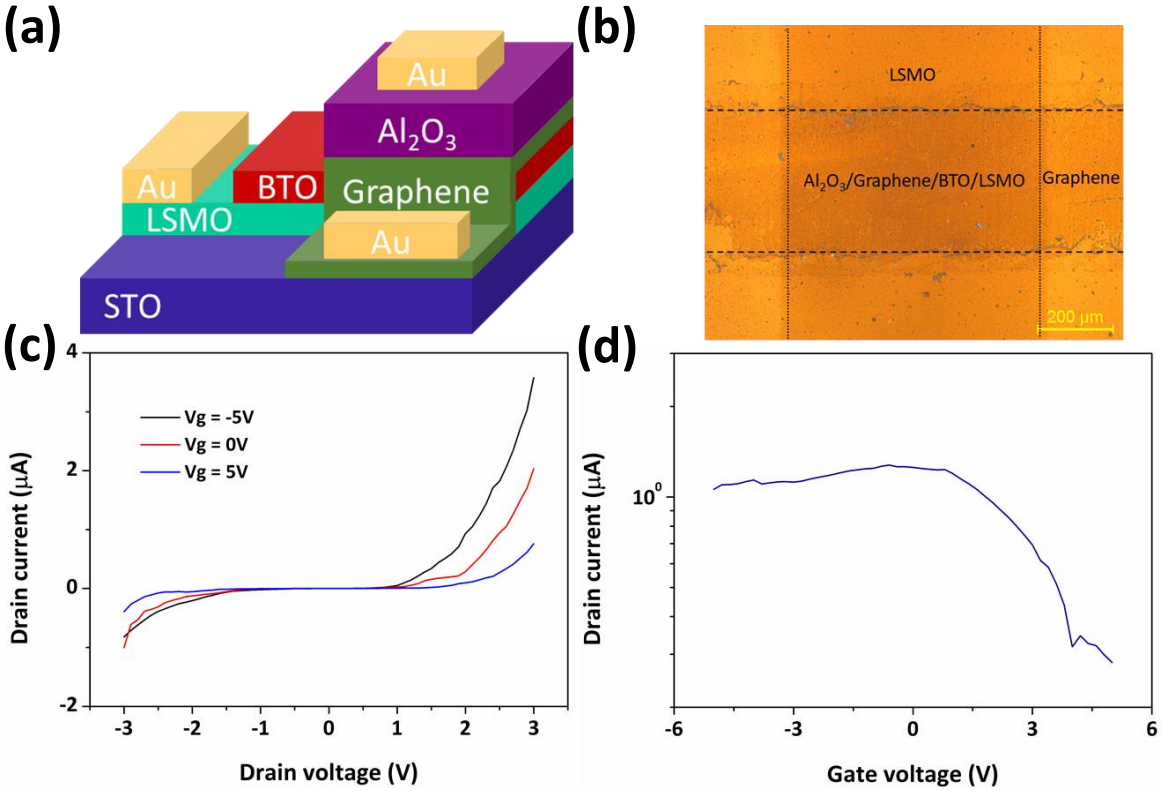


Figure 4. 7 (a) Schematic device architecture of the VGFTH-based FET with Au/Al_2O_3/graphene/BTO/LSMO/STO heterostructure. (b) Optical device micrograph. (c) I_d-V_d output characteristics of the device with different V_g applied. (d) I_d-V_g transfer characteristics of the device when V_d = 3 V.

4.4 Summary

In summary, we present a novel type of VGHFET employing ultrathin ferroelectric film as a tunnel barrier. The VGFTH-based FET is based on VGHFET where conventional insulator or semiconductor tunnel barrier is substituted by ferroelectric thin film. This is structurally different from the planar graphene-ferroelectric FET. The

integration of VGHFET and FTJ may add new functionality to the multilayer graphene-based heterostructure. For the back-gated VGFTH-based FET with Au/SBFO/graphene/SiO_2/Si heterostructure, the deposition of ferroelectric thin film on graphene by PLD method may bring a technical difficulty to the device fabrication. The top-gated VGFTH-based FET based on Au/Al_2O_3/graphene/BTO/NSTO heterostructure is fabricated and characterized. The output and transfer electrical characteristics can be obtained. A p-type behavior of the device is observed due to the p-type nature of graphene. The current ON/OFF ratio of the vertical graphene-based FET is measured to be about an order of magnitude higher than the conventional planar FET. Alternative top-gated VGFTH-based FET based on Au/Al_2O_3/graphene/BTO/LSMO/STO heterostructure is also designed. The output and transfer features show the p-type characteristics in the electrical measurement. The results provide a platform to engineer nanoscale two-dimensional heterostructure for logic electronic applications.

Chapter 5 Conclusion and Future Prospect

5.1 Conclusion

The emerging of 2D materials has drawn considerable attention for both fundamental research and device fabrication. Integration of graphene and ferroelectric material can yield functional hybrid structure with interesting characteristics for various practical applications. In this thesis, different kinds of electronic devices based on graphene tunneling heterostructure with ferroelectric thin film are fabricated and characterized. The details of the thesis are summarized as below.

Firstly, we present an asymmetrical FTJ employing both two-dimensional material and semiconductor electrode in the graphene/BTO/NSTO heterostructure. By using different characterization techniques such as Raman spectroscopy, XRD, XPS and PFM, the graphene nanosheets and BTO thin films are found to be of high quality. Compared with traditional metal electrodes, graphene electrodes possess the great advantages of atomic level thickness and optical transparency, which may facilitate the design of future ultra-broadband and high-speed optoelectronic devices. The NSTO semiconductor electrodes can tune the transport properties of the tunnel junction. The TER effect of the graphene/BTO/NSTO heterostructure is investigated. The ON/OFF resistance ratio increases with decreasing Nb doping concentration from 1.0 wt% to 0.1

wt% in the semiconductor electrodes, as a result of the ferroelectric-driven barrier tunability in both height and width on the semiconductor interface. An optimized ON/OFF ratio above 10^3 is obtained in the device when introducing 0.1 wt% Nb concentration at room temperature. Moreover, good retention property and switching reproducibility can be observed for the devices with different Nb concentration. The results provide an alternative pathway to design the graphene-based FTJs, which are helpful for developing non-volatile memory applications at nanoscale.

Secondly, we report a novel type of VGHFET using ultrathin ferroelectric film as a tunnel barrier, namely VGFTH-based FET. The ferroelectric switching action of FTJ may add new functionality and tunability to the VGHFET. The VGFTH-based FETs have been demonstrated in terms of back-gated and top-gated architecture. For the back-gated Au/SBFO/graphene/SiO_2/Si heterostructure, the PLD-growth of ferroelectric thin film on graphene surface poses an experimental challenge to the device fabrication. The top-gated device with Au/Al_2O_3/graphene/BTO/NSTO heterostructure is engineered. The output and transfer electrical characteristics of the device are observed. A p-type feature can be identified. The measured current ON/OFF ratio of the vertical graphene-based FET is higher than that of the conventional planar FET. In addition, alternative top-gated device with Au/Al_2O_3/graphene/BTO/LSMO/STO heterostructure is fabricated. The output and

transfer electrical behaviors exhibiting p-type characteristics can also be obtained in the device. The work opens up the possibility to develop atomic-scale and multifunctional heterostructure with enhanced performance.

5.2 Future Prospect

Due to good impermeability of graphene with gas or liquid, interface engineering should be implemented in the graphene/BTO/NSTO heterostructure by integrating functional molecules into the graphene/ferroelectric interface to further modulate the device properties. Graphene has the merits of atomic level thickness and optical transparency, which is very suitable for optoelectronic devices. As a future work, we may investigate the optoelectronic properties of the studied graphene/BTO/NSTO heterostructure. On the other hand, the PLD growth conditions of the SBFO ferroelectric film, as well as the LSMO or SRO conductive layer should be optimized to improve the thin film quality for device fabrication. Apart from the conventional inorganic ferroelectrics, organic ferroelectrics such as poly(vinylidene fluoride) (PVDF) and poly(vinylidene fluoride-co-trifluoroethylene) (PVDF-TrFE) exhibit good flexibility and robust ferroelectricity. Graphene can be integrated with the organic ferroelectric thin films to form flexible and rollable vertical graphene-ferroelectric electronic devices.

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